BAD40_HC
DIS/UMA Schematics Document
Sandy&Ivy Bridge
Intel PCH

DY :None Installed
DIS:DIS installed
DIS_Muxless :BOTH DIS or Muxless installed
DIS_PX:BOTH DIS or PX installed
DIS_PX_Muxless:DIS or PX or Muxless installed.
Muxless: Muxless installed.(PX4.0)
PX:MUX installed.(PX3.0)
PX_Muxless:BOTH PX or Muxless installed.
UMA:UMA installed
UMA_Muxless:BOTH UMA or Muxless installed
UMA_PX_Muxless:UMA or PX or Muxless installed

ANNIE: ONLY FOR ANNIE solution.
PSL: KBC795 PSL circuit for 10mW solution installed.
10mW: External circuit for 10mW solution installed.
65W: for 65W adaptor installed.
90W: for 90W adaptor installed.

<Variant Name>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Cover Page

Size: A3 | Document Number: BAD40_HC | Rev: 1

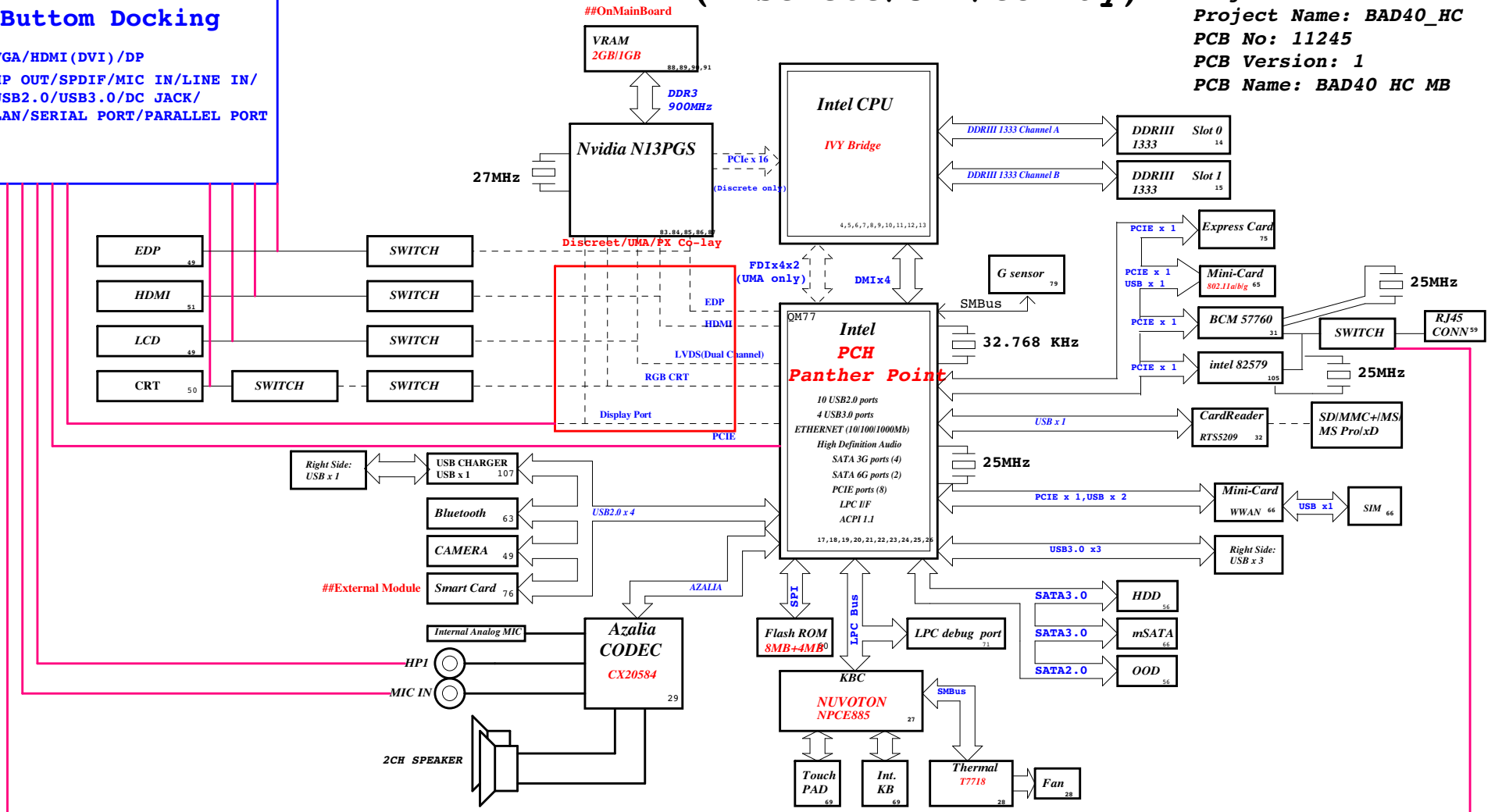
Date: Thursday, April 12, 2012 | Sheet 1 of 108

BAD40 HC Block Diagram (Discrete/UMA/co-lay)

Project Code: 91.4SA01.001
Project Name: BAD40_HC
PCB No: 11245
PCB Version: 1
PCB Name: BAD40 HC MB

Buttom Docking

VGA/HDMI(DVI)/DP
HP OUT/SPDIF/MIC IN/LINE IN/
USB2.0/USB3.0/DC JACK/
LAN/SERIAL PORT/PARALLEL PORT



SYSTEM DC/DC TPS5146 48	
INPUTS	OUTPUTS
5V_S5	0D85V_S0

CPU DC/DC VT1317SFCX 42~43	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC RT8237AGQW 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC RT8239CGQW 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC RT8207LGQW 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

SYSTEM DC/DC VT1317SFCX 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE_PWR

VGA RT8208AGQW 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

TI CHARGER BQ24745RHDR 40	
INPUTS	OUTPUTS
DCBATOUT	BT+

SYSTEM DC/DC RT8015AGQW 47	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

SYSTEM DC/DC	
INPUTS	OUTPUTS

Switches	
INPUTS	OUTPUTS
1D5V_S3	1D5V_VGA_S0
3D3V_S0	3D3V_VGA_S0

PCB LAYER

L1:Top	L5:Power
L2:GND	L6:Signal
L3:Signal	L7:GND
L4:Signal	L8:Bottom

HR PX

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Title: Block Diagram

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PCH Strapping

Huron River Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Huron River Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	0
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	1

POWER PLANE	VOLTAGE	Voltage Rails ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

PCIE Routing

LANE1	N/A
LANE2	Mini Card2(WWAN)
LANE3	Card Reader
LANE4	Mini Card1(WLAN)
LANE5	N/A
LANE6	Intel /BCM LAN
LANE7	New Card
LANE8	N/A

SATA Table

SATA	
Pair	Device
0	HDD1
1	mSATA
2	N/A
3	N/A
4	ODD
5	N/A

USB Table

Pair	Device
0	USB. port 1
1	USB. port 2
2	USB. port 3
3	Dock
4	X
5	Fingerprint
6	X
7	X
8	Mini Card2 (WWAN) &BT
9	
10	3G SIM
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

SMBus ADDRESSES

I² C / SMBus Addresses Device	Ref Des	HURON RIVER ORB Address	Hex	Bus
EC SMBus 1 Battery CHARGER				BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP				SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI				PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

<Variant Name>

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Title: Table of Content

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SSID = CPU

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.

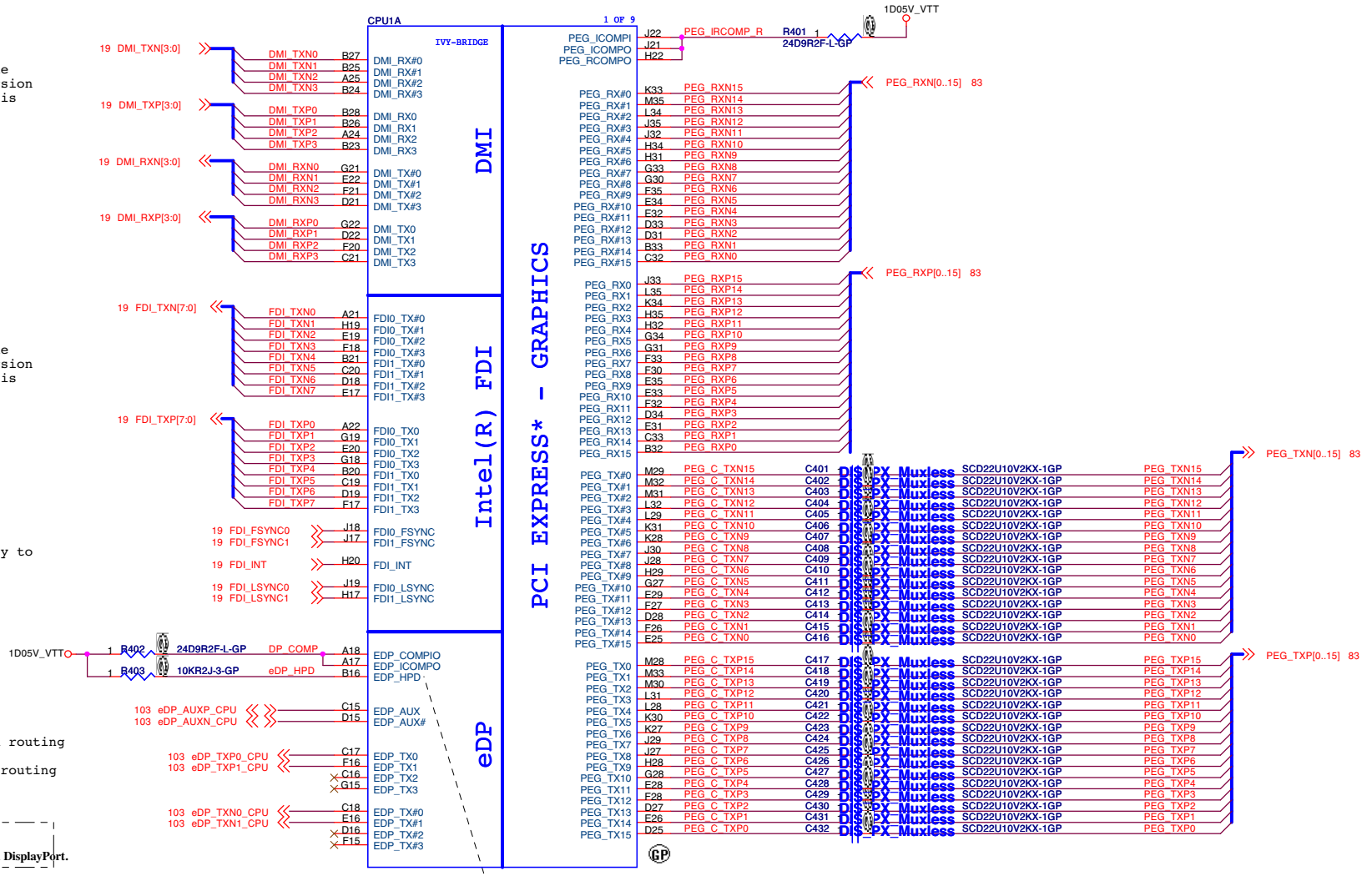
Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Lane reversal does not apply to FDI sideband signals.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.



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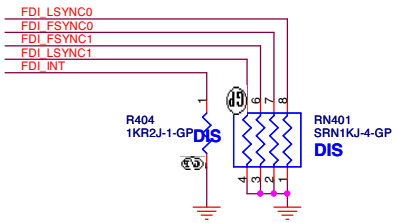
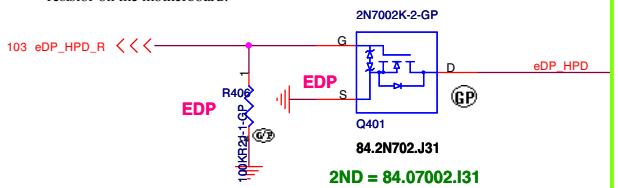
Stuff to disable internal graphics function for power saving.



SB 0923

20100614 V1.1

NOTE:
Select a Fast FET similar to 2N7002E whose rise/ fall time is less than 6 ns. If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up resistor on the motherboard.



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Title: **CPU (PCIE/DMI/FDI)**

Size	Document Number	Rev
A3	BAD40 HC	1

Date: Thursday, April 12, 2012 Sheet 4 of 108

SSID = CPU

Disabling Guidelines:
If motherboard only supports external graphics:
Connect DPLL_REF_SSCLK on Processor to GND through 1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K +/- 5% resistorpower (~15 mW) may be wasted.

RN502 SRN1KJ-2-GP
20100628 V1.3
DIS

1D05V_VTT
R501 62R2J-GP
H_PROCHOT#
C502 SC47P50V2JN-3GP

CRB : 47pf
CEKLT:43pf

IVY-BRIDGE

MISC
22 H_SNB_IVB# → C26 PROC_SELECT#
AN34 SKTOCC#

CLOCKS
BCLK A28 / BCLK# A27 → CLK_EXP_P 20 / CLK_EXP_N 20
DPLL_REF_CLK A16 / DPLL_REF_CLK# A15 → CLK_DP_P_R 20 / CLK_DP_N_R 20

THERMAL
AL33 CATERR#
22,27 H_PECI AN33 PECI
27,42 H_PROCHOT# → R513 56R2J-4-GP → H_PROCHOT# R AL32 PROCHOT#
22,36 H_THERMTRIP# AN32 THERMTRIP#

DDR3 MISC
SM_DRAMRST# R8 → R502 4K99R2F-L-GP → SM_DRAMRST# 37
SM_RCOMP0 AK1 → SM_RCOMP_0 R506 140R2F-GP
SM_RCOMP1 A5 → SM_RCOMP_1 R507 25D5R2F-GP
SM_RCOMP2 A4 → SM_RCOMP_2 R508 200R2F-L-GP

Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.

PWR MANAGEMENT
19 H_PM_SYNC AM34 PM_SYNC
R503 10KR2J-3-GP
22,36 H_CPUPWRGD AP33 UNCOREPWRGOOD
19,37 PM_DRAM_PWRGD → R505 0R2J-2-GP (DY) → V8 SM_DRAMPWROK
37 VDDPWRGOOD
BUF_CPU_RST# AR33 RESET#

JTAG & BPM
PRDY# AP29 / PREQ# AP27
TCK AR26 / TMS AR27 / TRST# AP30 → XDP_TRST#
TDI AR28 / TDO AP26 → XDP_TDO
DBR# AL35 → XDP_DBRESET#
BPM#0 AT28 / BPM#1 AR29 / BPM#2 AR30 / BPM#3 AT30 / BPM#4 AP32 / BPM#5 AR31 / BPM#6 AT31 / BPM#7 AR32

1D05V_VTT
RN501 SRN51J-GP
XDP_TDO
XDP_TRST#

3D3V_S0
RN503 SRN1K5J-1-GP
XDP_DBRESET#
7,31,32,36,65,66,71,75,82,83,97,105 PLT_RST# → BUF_CPU_RST#

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H_CPUPWRGD → EC501 SC120P50V2JN-1GP
BUF_CPU_RST# → EC502 SC5P50V2CN-2GP (DY)

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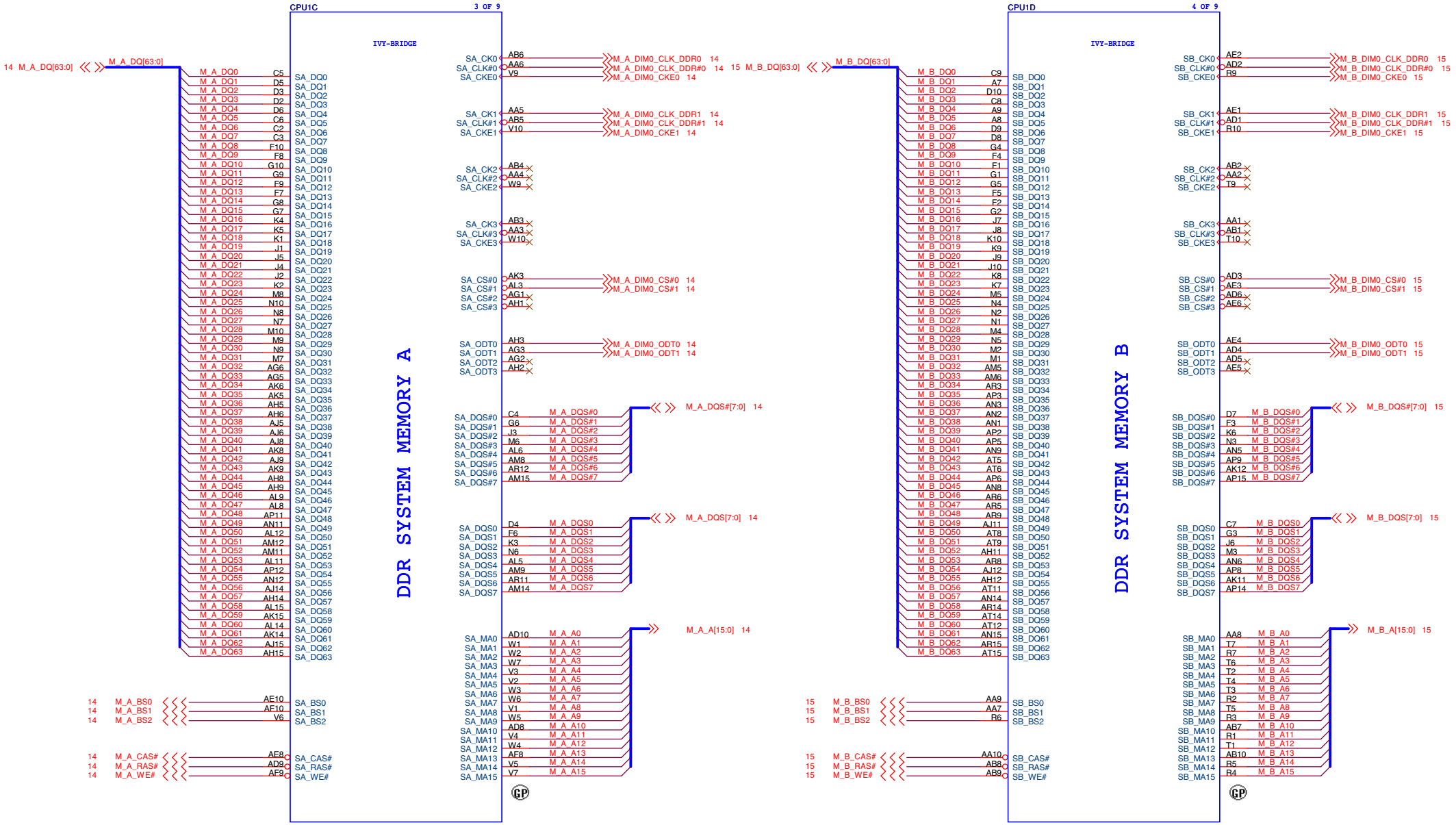
Title	CPU (THERMAL/CLOCK/PM)	
Size: Custom	Document Number: BAD40 HC	Rev: 1
Date: Thursday, April 12, 2012	Sheet 5 of 108	

SSID = CPU



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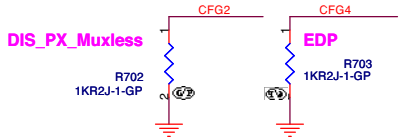
Title: ***CPU (DDR)***

Size	Document Number	Rev
A3	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 6 of 108

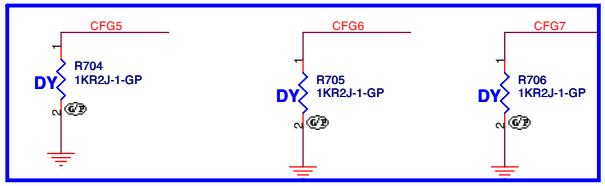
SSID = CPU



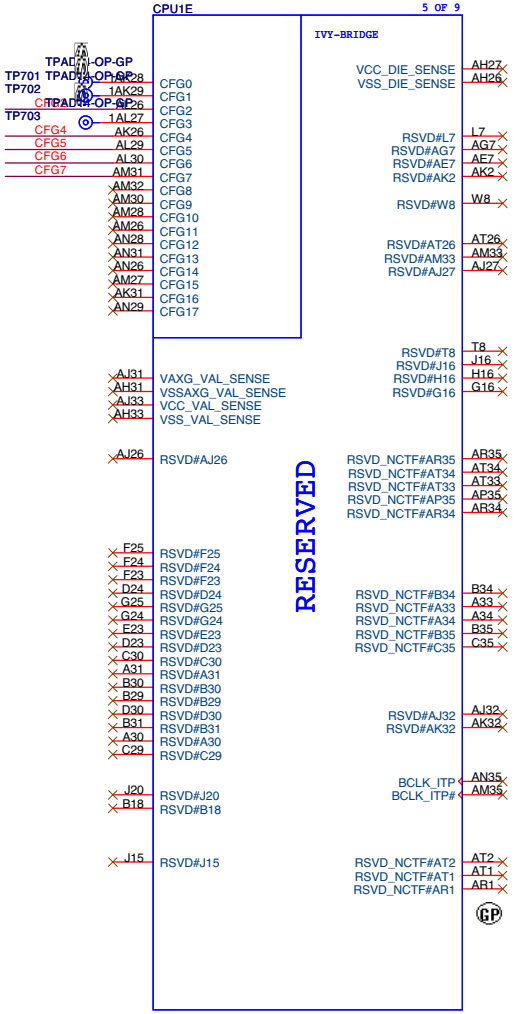
PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition
	0:Lane Reversed

PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled
	10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

SA



PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion
	0: PEG Wait for BIOS for training



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Title: CPU (RESERVED)

Size: A3 | Document Number: BAD40_HC | Rev: 1

Date: Thursday, April 12, 2012 | Sheet 7 of 108

SSID = CPU

POWER

PROCESSOR CORE POWER

53A

VCC_CORE

0308 -1
change to 78.2261T.5BL for acousit noice

0308 -1

0308 -1
change to 78.2261T.5BL for acousit noice

0312 -1

0308 -1

VCC Output Decoupling Recommendation:
4 x 470 uF at Bottom Socket Edge
8 x 22 uF at Top Socket Cavity
8 x 22 uF at Top Socket Edge
8 x 22 uF at Bottom Socket Cavity

CPU1F — IVY-BRIDGE — 6 OF 9

VCC_CORE

AG35 VCC1, AG34 VCC2, AG33 VCC3, AG32 VCC4, AG31 VCC5, AG30 VCC6, AG29 VCC7, AG28 VCC8, AG27 VCC9, AG26 VCC10, AF35 VCC11, AF34 VCC12, AF33 VCC13, AF32 VCC14, AF31 VCC15, AF30 VCC16, AF29 VCC17, AF28 VCC18, AF27 VCC19, AF26 VCC20, AD35 VCC21, AD34 VCC22, AD33 VCC23, AD32 VCC24, AD31 VCC25, AD30 VCC26, AD29 VCC27, AD28 VCC28, AD27 VCC29, AD26 VCC30, AC35 VCC31, AC34 VCC32, AC33 VCC33, AC32 VCC34, AC31 VCC35, AC30 VCC36, AC29 VCC37, AC28 VCC38, AC27 VCC39, AC26 VCC40, AA35 VCC41, AA34 VCC42, AA33 VCC43, AA32 VCC44, AA31 VCC45, AA30 VCC46, AA29 VCC47, AA28 VCC48, AA27 VCC49, AA26 VCC50, Y35 VCC51, Y34 VCC52, Y33 VCC53, Y32 VCC54, Y31 VCC55, Y30 VCC56, Y29 VCC57, Y28 VCC58, Y27 VCC59, Y26 VCC60, V35 VCC61, V34 VCC62, V33 VCC63, V32 VCC64, V31 VCC65, V30 VCC66, V29 VCC67, V28 VCC68, V27 VCC69, V26 VCC70, U35 VCC71, U34 VCC72, U33 VCC73, U32 VCC74, U31 VCC75, U30 VCC76, U29 VCC77, U28 VCC78, U27 VCC79, U26 VCC80, R35 VCC81, R34 VCC82, R33 VCC83, R32 VCC84, R31 VCC85, R30 VCC86, R29 VCC87, R28 VCC88, R27 VCC89, R26 VCC90, P35 VCC91, P34 VCC92, P33 VCC93, P32 VCC94, P31 VCC95, P30 VCC96, P29 VCC97, P28 VCC98, P27 VCC99, P26 VCC100

62.10055.321

VCCIO Output Decoupling Recommendation:
2 x 330 uF (3 x 330 uF for 2012 capable designs)
5 x 22 uF & 5 x 0805 no-stuff at Bottom
7 x 22 uF & 2 x 0805 no-stuff at Top

1D05V_VTT

VCCIO1 AH13, VCCIO2 AH10, VCCIO3 AG10, VCCIO4 AC10, VCCIO5 Y10, VCCIO6 U10, VCCIO7 P10, VCCIO8 L10, VCCIO9 J14, VCCIO10 J13, VCCIO11 J12, VCCIO12 J11, VCCIO13 H14, VCCIO14 H12, VCCIO15 H11, VCCIO16 G14, VCCIO17 G13, VCCIO18 G12, VCCIO19 F14, VCCIO20 F13, VCCIO21 F12, VCCIO22 F11, VCCIO23 F14, VCCIO24 E12

VCCIO25 E11, VCCIO26 D14, VCCIO27 D13, VCCIO28 D12, VCCIO29 D11, VCCIO30 C14, VCCIO31 C13, VCCIO32 C12, VCCIO33 C11, VCCIO34 B14, VCCIO35 B12, VCCIO36 A14, VCCIO37 A13, VCCIO38 A12, VCCIO39 A11

VCCIO40 J23

No-stuff sites outside the socket may be removed.
No-stuff sites inside the socket cavity need to remain.

close to CPU

H_CPU_SVIDDAT R804 130R2F-1-GP
VR_SVID_ALERT# R805 75R2F-2-GP

VIDALERT# AJ29 H_CPU_SVIDALRT# R803 43R2J-GP VR_SVID_ALERT# 42
VIDSCLK AJ30 H_CPU_SVIDCLK 42
VIDSOUT AJ28 H_CPU_SVIDDAT 42

0412 -1M

R801,R802 close to CPU

VCC_SENSE AJ35 VCCSENSE 42
VSS_SENSE AJ34 VSSSENSE 42

1215 SC

VCCIO_SENSE B10 VCCIO_SENSE TP801 TPAD14-OP-GP
VSS_SENSE_VCCIO A10 VSSIO_SENSE TP802 TPAD14-OP-GP

GP

<Variant Name>

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Title: CPU (VCC_CORE)
Size: Custom | Document Number: BAD40_HC | Rev: 1
Date: Thursday, April 12, 2012 | Sheet 8 of 108

SSID = CPU

VAXG Output Decoupling Recommendation:
2 x 470 uF at Bottom Socket Edge
2 x 22 uF at Top Socket Cavity
4 x 22 uF at Top Socket Edge
2 x 22 uF at Bottom Socket Cavity
4 x 22 uF at Bottom Socket Edge

R906,R907 close to CPU

POWER

VCC_GFXCORE

R906 100R2F-L1-GP-U
UMA_PX_Muxless
VCC_AXG_SENSE
VSS_AXG_SENSE
R907 100R2F-L1-GP-U
UMA_PX_Muxless

PROCESSOR VAXG: 38A

1201 SC

C901 C902 C903 C904 C905 C906
SC10U6D3V5KX-1GP
UMA_PX_Muxless
DY

1201 SC

C907 C908 C916 C919 C920 C921
SC10U6D3V5KX-1GP
UMA_PX_Muxless
DY

1201 SC

C923 C925 C926 C927 C928 C929 C930
SC22U6D3V5MX-2GP
UMA_PX_Muxless
DY

1201 SC

C931 C932
SC22U6D3V5MX-2GP
UMA_PX_Muxless
DY

CPU1G 7 OF 9
IVY-BRIDGE

VAXG1 VAXG2 VAXG3 VAXG4 VAXG5 VAXG6 VAXG7 VAXG8 VAXG9 VAXG10 VAXG11 VAXG12 VAXG13 VAXG14 VAXG15 VAXG16 VAXG17 VAXG18 VAXG19 VAXG20 VAXG21 VAXG22 VAXG23 VAXG24 VAXG25 VAXG26 VAXG27 VAXG28 VAXG29 VAXG30 VAXG31 VAXG32 VAXG33 VAXG34 VAXG35 VAXG36 VAXG37 VAXG38 VAXG39 VAXG40 VAXG41 VAXG42 VAXG43 VAXG44 VAXG45 VAXG46 VAXG47 VAXG48 VAXG49 VAXG50 VAXG51 VAXG52 VAXG53 VAXG54

VAXG_SENSE AK35 — VCC_AXG_SENSE 42
VSSAXG_SENSE AK34 — VSS_AXG_SENSE 42

Refer to the latest Huron River Mainstream PDG (Doc# 436735) for more details on S3 power reduction implementation.

+V_SM_VREF_CNT should have 10 mil trace width

SM_VREF AL1 — +V_SM_VREF_CNT 37

SA_DIMM_VREFDQ B4 — M_VREF_DQ_DIMM0_C 37
SB_DIMM_VREFDQ D1 — M_VREF_DQ_DIMM1_C 37

Chief River

SNB 上件，1010 back IVB
M_VREF_DQ_DIMM0_C
M_VREF_DQ_DIMM1_C
1D5V_S0
RN902 SRN1KJ-7-GP
DY

PROCESSOR VDDQ: 10A

VDDQ1 VDDQ2 VDDQ3 VDDQ4 VDDQ5 VDDQ6 VDDQ7 VDDQ8 VDDQ9 VDDQ10 VDDQ11 VDDQ12 VDDQ13 VDDQ14 VDDQ15
AF7 AF4 AF1 AC7 AC4 AC1 Y7 Y4 Y1 U7 U4 U1 P7 P4 P1

C909 C910 C911 C912 C913 C914
SC10U6D3V5KX-1GP
DY

VDDQ Output Decoupling Recommendation:
1 x 330 uF
6 x 10 uF

0D85V_S0

PROCESSOR VCCSA: 6A

C916 C915
SC10U6D3V5KX-1GP
DY

VCCSA1 VCCSA2 VCCSA3 VCCSA4 VCCSA5 VCCSA6 VCCSA7 VCCSA8
M27 M26 L26 J26 J25 J24 H26 H25

VCCSA Output Decoupling Recommendation:
1 x 330 uF
2 x 10 uF at Bottom Socket Cavity
1 x 10 uF at Bottom Socket Edge

R902 100R2F-L1-GP-U
R902 need be close to pin H23.

VCCSA_SENSE H23 — VCCSA_SENSE 48

VCCSA_VID0 C22 — VCCSA_VID0
VCCSA_VID1 C24 — VCCSA_VID1

VCCIO_SEL A19 — H_SNB_IVB#_PWRCTRL

SB 1020 change to DY for co-lay
3D3V_S5
R911 100KR2J-1-GP
DY
H_SNB_IVB#_PWRCTRL

1D05V_VTT 1D05V_VTT
R908 DY
R912 10KR2J-3-GP DY
VCCSA_VID0
VCCSA_VID1
R913 10KR2J-3-GP
R914 10KR2J-3-GP
VCCSA_VID0 48
VCCSA_VID1 48

PIn A19	
1.05V	H
1V	L

VCCSA Voltage Select		
VID[1]	VID[0]	VCCSA
0	0	0.9 V
1	0	0.8 V
0	1	0.725 V
1	1	0.675 V

1D8V_S0

PROCESSOR VCCPLL: 1.8A

VCCPLL1 VCCPLL2 VCCPLL3
B6 A6 A2

C922 SC1U10V2KX-1GP

VCCPLL Output Decoupling Recommendation:
1 x 330 uF
2 x 1 uF
1 x 10 uF

Disabling Guidelines for External Graphics Designs:
Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed.
Can be left floating (Gfx VR keeps VAXG rail from floating) if the VR is stuffed

VCC_GFXCORE

R903 0R3J-0-U-GP DIS
R904 0R3J-0-U-GP DIS
R905 0R3J-0-U-GP DIS
R901 0R3J-0-U-GP DIS

62.10055.321

<Variant Name>

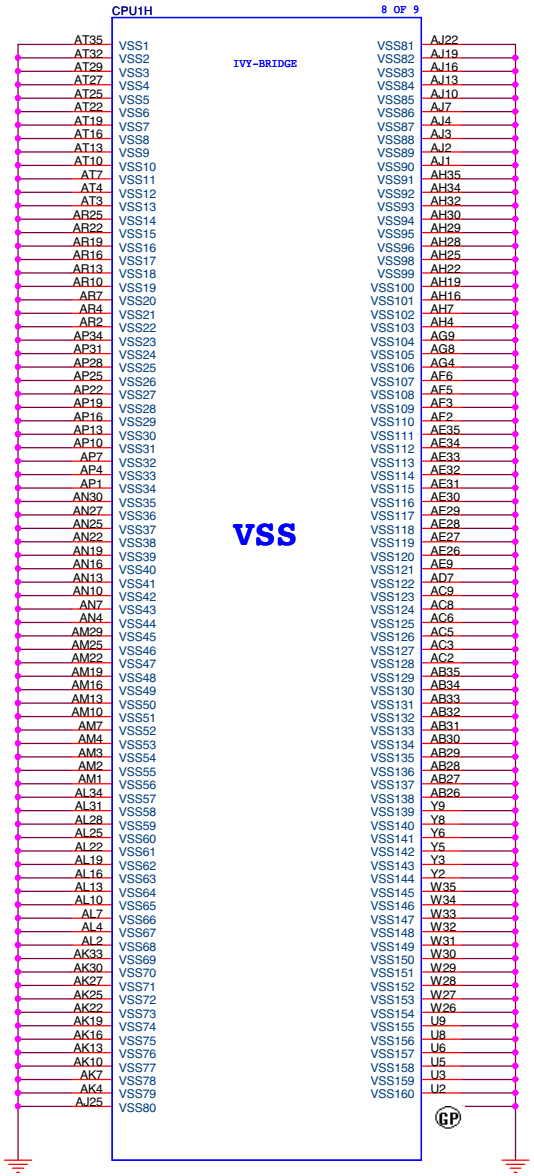
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VCC_GFXCORE)

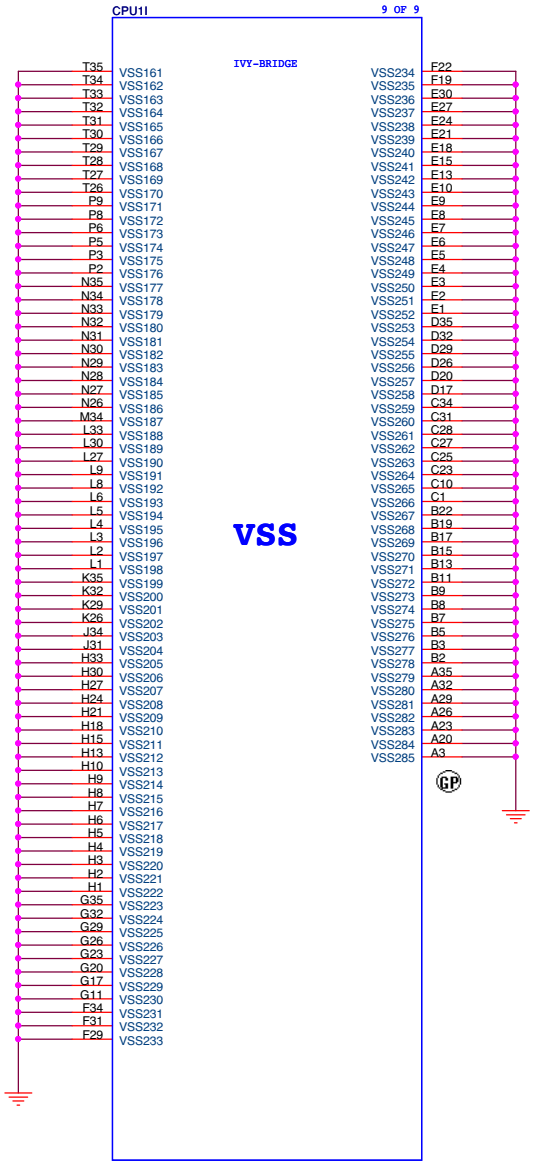
Size	Document Number	Rev
Custom	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 9 of 108

SSID = CPU



62.10055.321



62.10055.321

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU (VSS)***

Size	Document Number	Rev
A3	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 10 of 108

reserve

JE40 delete XDP function

HR PX

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***XDP***	
Size A4	Document Number **BAD40_HC**	Rev 1
Date: Thursday, April 12, 2012	Sheet 11 of 108	

(Blanking)

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A4	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 12 of 108

(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 13 of 108

SSID = MEMORY

DM1

DDR3-204P-122-GP

M_A_A[15:0] 6

M_A_BS2 6

M_A_BS0 6

M_A_BS1 6

M_A_DQ[63:0] 6

M_A_DQS#[7:0] 6

M_A_DQS[7:0] 6

M_A_DIM0_ODT0 6

M_A_DIM0_ODT1 6

DDR_VREF_S3

M_VREF_DQ_DIMM0

0308 -1

1228 SC

R1404 0R0603-PAD

M1

R1405 0R3J-0-U-GP

DY

DDR_WR_VREF01_B4 37

Tracew should be at least 20 mils wide

C1411 SCD1U10V2KX-5GP

C1413 SCD1U10V2KX-5GP

0D75V_S0

Place these caps close to VTT1 and VTT2.

1125 SC for RF

C1419 SC1U6D3V2KX-GP

C1420 SC1U6D3V2KX-GP

C1421 SC1U6D3V2KX-GP

C1422 SC220P50V2KX-2GP

C1418 SCD1U10V2KX-5GP

15,37 DDR3_DRAMRST#

0D75V_S0

H =4mm

62.10017.Z51

2nd = 62.10017.V51

PCH_SMBDATA 15,20,66,79

PCH_SMBCLK 15,20,66,79

TS#_DIMM0_1 15

3D3V_S0

1D5V_S3

C1401 SCD1U10V2KX-5GP

Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

Thermal EVENT

TS#_DIMM0_1 R1403 10KR2J-3-GP 3D3V_S0

SODIMM A DECOUPLING

1D5V_S3

C1403 SC10U6D3V5KX-1GP

C1404 SC10U6D3V5KX-1GP

C1405 SC10U10V5ZY-1GP

DY

C1406 SC10U6D3V5KX-1GP

C1407 SC10U6D3V5KX-1GP

DY C1408 SC10U10V5ZY-1GP

DY C1409 SC10U6D3V5KX-1GP

DY C1410 SC10U6D3V5KX-1GP

C1416 SCD1U10V2KX-5GP

C1417 SCD1U10V2KX-5GP

Layout Note:
Place these Caps near SO-DIMMA.

HR PX

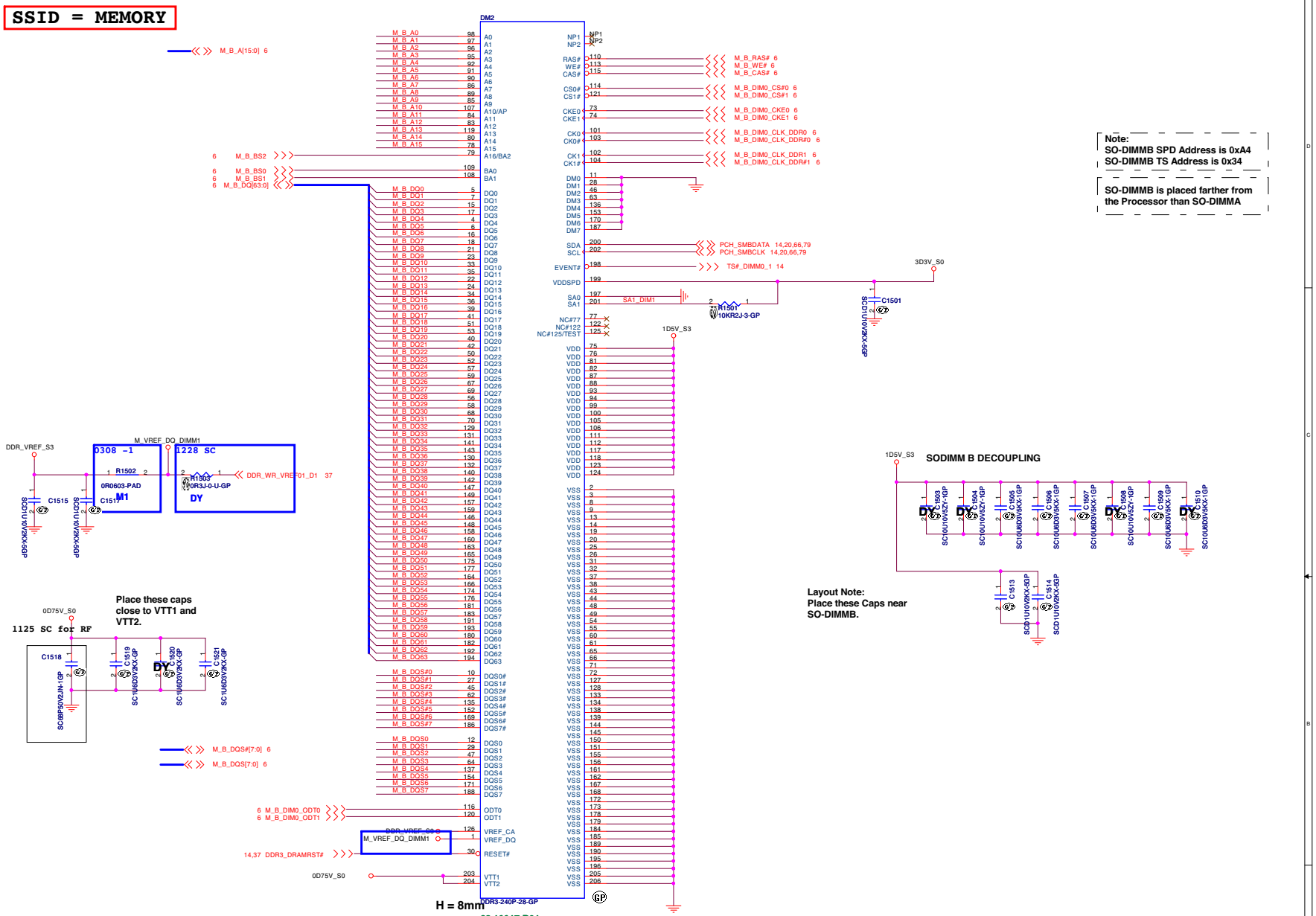
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM1

Size	Document Number	Rev
Custom	BAD40_HC	11

Date: Thursday, April 12, 2012 Sheet 14 of 108

SSID = MEMORY



HR PX

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***DDR3-SODIMM2***	
Size: Custom	Document Number: **BAD40_HC**	Rev: 1
Date: Thursday, April 12, 2012	Sheet 15 of 108	

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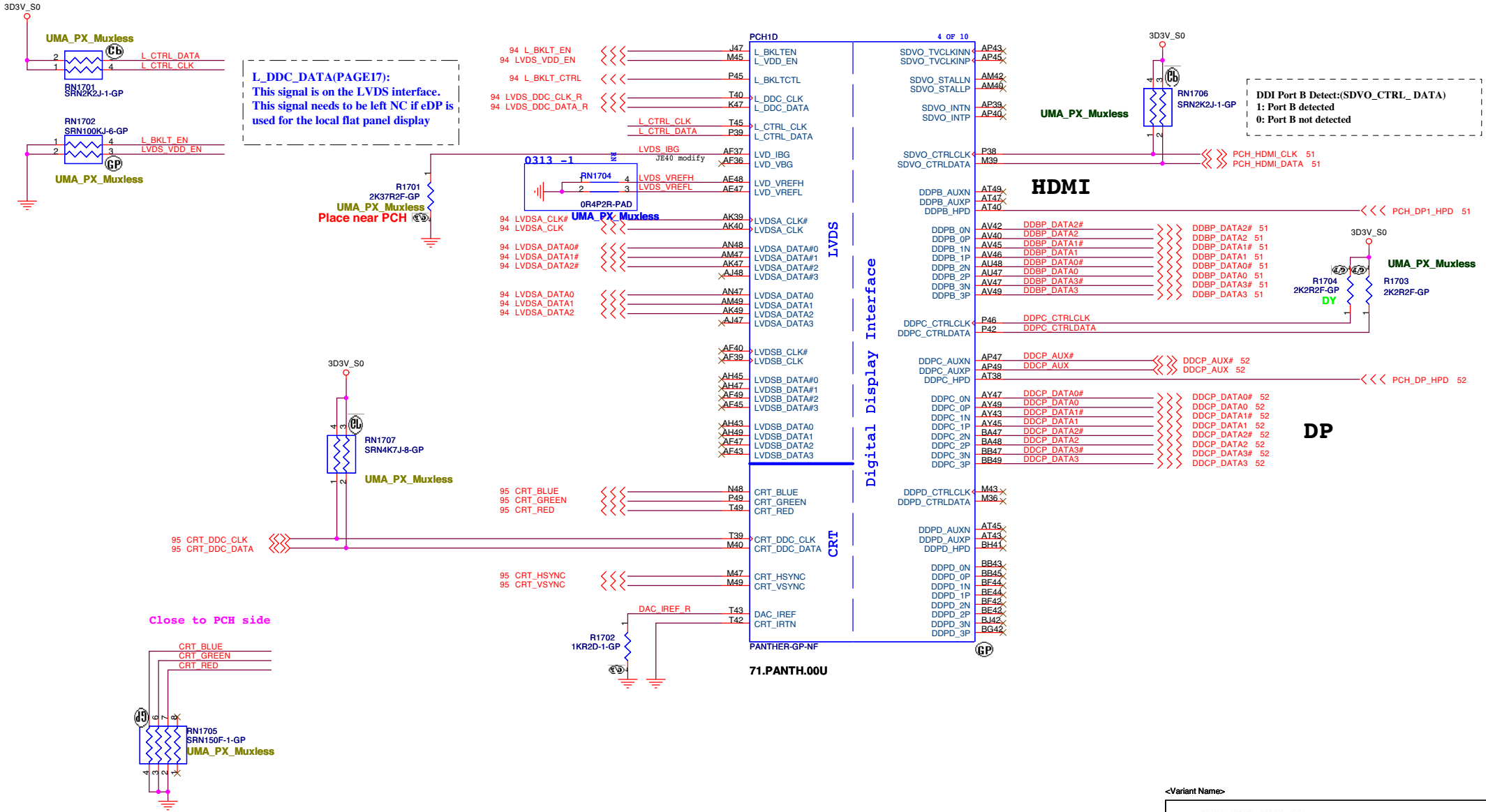
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *DDR3-SODIMM2*

Size	Document Number	Rev
A4	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 16 of 108



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

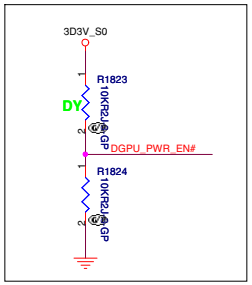
Title: **PCH (LVDS/CRT/DDI)**

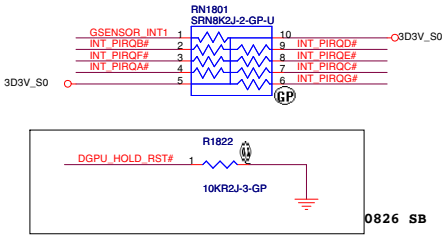
Size	Document Number	Rev
A3	BAD40_HC	11

Date: Thursday, April 12, 2012 Sheet 17 of 108

SSID = PCH

0826 SB





0826 SB

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

BOOT BIOS Strap

GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

USB Table

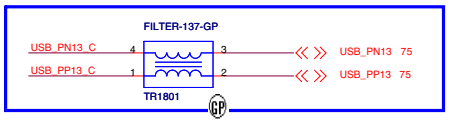
Pair	Device
0	USB port 2 on S/B
1	USB port 3 on S/B
2	USB port 4 on S/B(usb charger)
3	DOCK
4	BLUETOOTH(from port3)
5	Fingerprint(from port2)(NO USE)
6	X
7	X
8	Mini Card2 (WWAN)
9	USB port1(SATA Combo),on M/B
10	3G Card
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card or USB HUB(New/Smart)

OC[3:0]# for Device 29 (Ports 0-7)
OC[7:4]# for Device 26 (Ports 8-13)

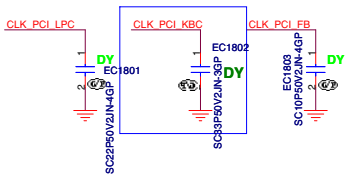
USB 2.0 Overcurrent Pin Default Usage

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

0314 -1 for EMI



1125 SC for RF



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

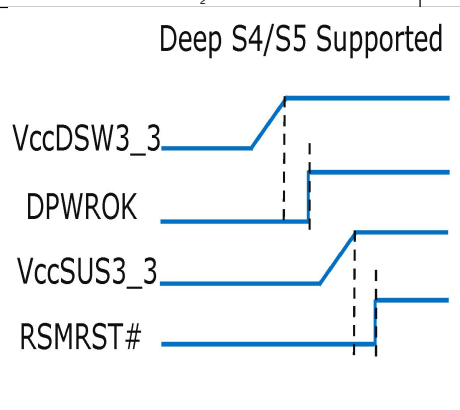
Title: PCH (PCI/USB/NVRAM)

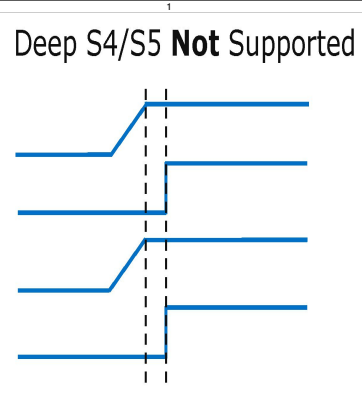
Size: Custom | Document Number: BAD40_HC | Rev: 1

Date: Thursday, April 12, 2012 | Sheet 18 of 108

SSID = PCH

Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.





For platforms not supporting Deep S4/S5
1.VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
2.DPWROK and RSMRST# will rise at the same time (connected on board)
3.SLP_SUS# and SUSACK# are left as 'no connect'
4.SUSWARN# used as SUSPWRDNACK/GPIO30

PCH1C — 3 OF 10 — DMI / FDI / System Power Management — PANTHER-GP-NF

0628 Modify: Change R1904 to 100K 0402 from 10K and default stuff.

JE40 modify

0302 -1 for SBA

1222 SC

Non_iAMT_SBA

iAMT_SBA

S0_PWR_GOOD after PM_SLP_S3# delay 200 ms

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

PCIE_WAKE#
CRB : 1K
CEKLT: 10K

PWRBTN#
This signal has an internal pull-up resistor

PM_RSMRST#
CRB : PL 10K
ANNIE : PL 100K

Q1901 2N7002KDW-GP
84.2N702.A3F
2nd = 84.2N702.F3F

71.PANTH.00U

<Variant Name>

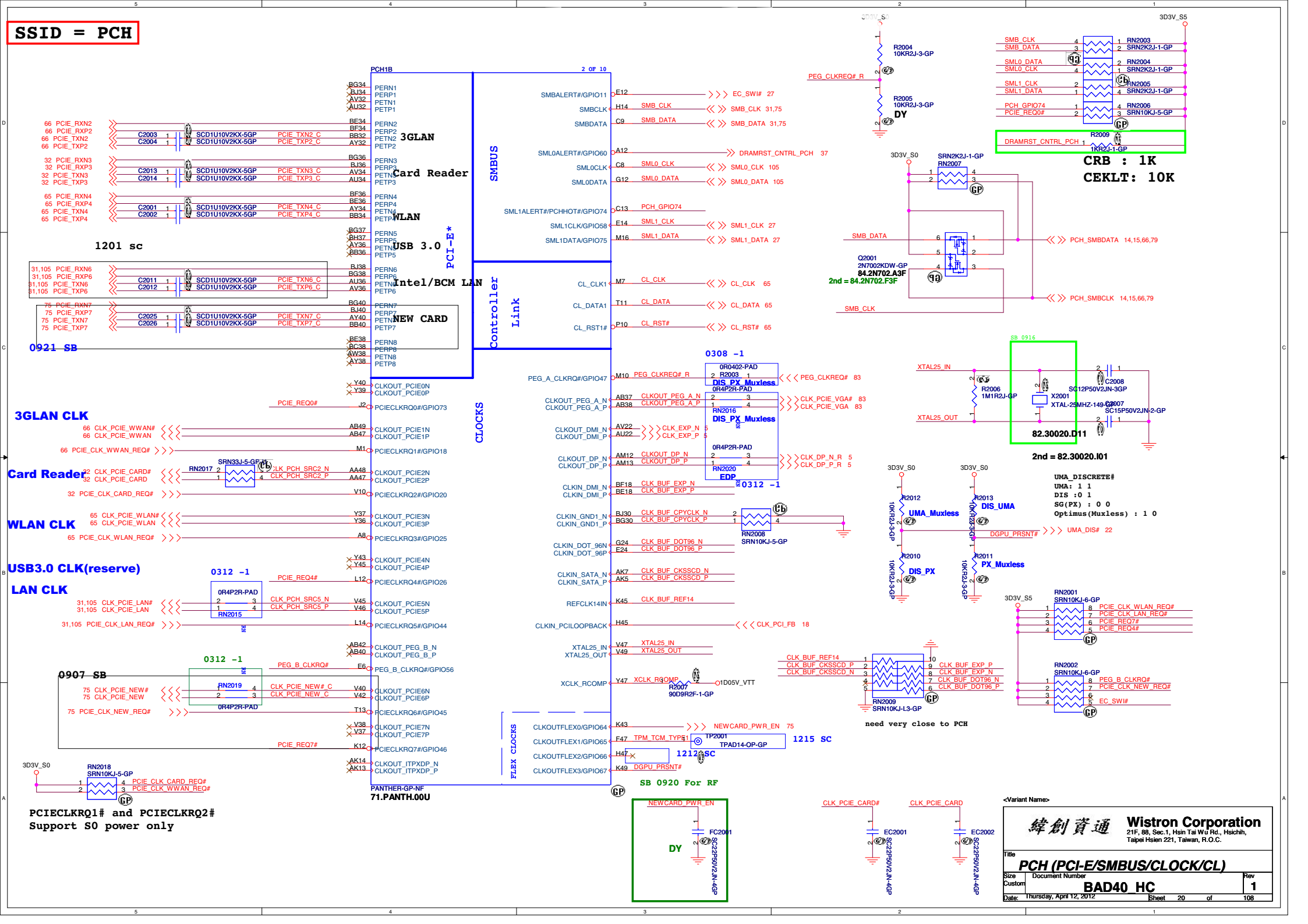
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (DM I/FDI/PM)**

Size	Document Number	Rev
A3	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 19 of 108

SSID = PCH


PCH1B
2 OF 10
PCI-E*
SMBUS
CLOCKS
Controller Link
FLEX CLOCKS
3GLAN
Card Reader
WLAN
USB 3.0
Intel/BCM LAN
NEW CARD
1201 sc
0921 SB
PANTHER-GP-NF
71.PANTH.00U
3GLAN CLK
Card Reader
WLAN CLK
USB3.0 CLK(reserve)
LAN CLK
0907 SB
0312 -1
0308 -1
SB 0920 For RF
1215 SC
1212 SC
PCIECLKRQ1# and PCIECLKRQ2#
Support S0 power only
need very close to PCH
CRB : 1K
CEKLT: 10K
2nd = 84.2N702.F3F
82.30020.D11
2nd = 82.30020.I01
UMA_DISCRETE#
UMA: 1 1
DIS :0 1
SG(PX) : 0 0
Optimus(Muxless) : 1 0
DIS_PX_Muxless
DIS_UMA
UMA_Muxless
DIS_PX
PX_Muxless
SB 0916
DY
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
PCH (PCI-E/SMBUS/CLOCK/CL)
BAD40_HC
Thursday, April 12, 2012
Sheet 20 of 108

SSID = PCH

SB 0923

82.30001.A41
2nd = 82.30001.841

RTC Reset

1103 SC for AFR

1103 SC

84.2N702.J31
2ND = 84.07002.I31

PCH1A

1 OF 10

PANTHER-GP-NF

71.PANTH.00U

1223 SC

1208 SC

ESATA

HDD1

mSATA

ODD

DUAL RGM

INTVRMEN- Integrated SUS 1.05V VRM Enable
High - Enable internal VRs
Low - Enable external VRs

Flash Descriptor Security Overide	
HDA_SDOUT	Low = Default High = Enable

No Reboot Strap	
HDA_SPKR	Low = Default High = No Reboot

PLL ODVR VOLTAGE	
HDA_SYNC	Low = 1.8V (Default) High = 1.5V

**This signal has a weak internal pull down.
On Die PLL VR is supplied by 1.5V when sampled high, 1.8 V when sampled low.
Needs to be pulled High for Huron River platform.
co-operate with R2310**

H->Smart Card
L->Non Smart Card

HDA_SYNC: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (SPI/RTC/LPC/SATA/HDA)

Size: A3 | Document Number: BAD40_HC | Rev: 1

Date: Thursday, April 12, 2012 | Sheet 21 of 108

SSID = PCH

Note:
For PCH debug with XDP, need to NO STUFF R2218

3D3V_S0 — RN2203 SRN10KJ-5-GP — H_RCIN# — H_A20GATE

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator, should not place external pull down.

3D3V_S5 — 0908 SB — DY — R2220 10KR2J-3-GP — PCH_GPIO24 — R2207 100KR2J-1-GP

	INTERNAL GFX	EXTERNAL GFX
R2205	DY	10K
R2206	100K	DY

	LVDS	eDP
EDP#_LVDS	H	L

3D3V_S0 — RN2201 SRN10KJ-5-GP — DGPU_HPD_INTR# — EC_SCI#

RN2202 SRN10KJ-8-GP — MFG_MODE — S_GPIO — PCH_TEMP_ALERT#

3D3V_S5 — RN2204 SRN10KJ-6-GP — USB3_PWR_ON — LAN_DIS# — PCH_GPIO15 — R2201 1KR2J-1-GP

VRAM Frequency
Pull high: 800MHZ
Pull low :900MHZ

3D3V_S0 — R2218 10KR2J-3-GP — UMA_VRAM800MHZ — PCH_GPIO22 — R2219 10KR2J-3-GP — VRAM900MHZ

VRAM Size

3D3V_S0 — R2214 10KR2J-3-GP — 2G — R2216 10KR2J-3-GP — 1G — VRAM_SIZE1 — VRAM_SIZE2 — R2215 10KR2J-3-GP — 1G_512M — R2217 10KR2J-3-GP — 512M_2G

PassWord Clear
G2201 GAP-OPEN

1124 SC
del R2206

1208 SC for Del e-SATA

3D3V_S0 — R2224 10KR2J-3-GP — eSATA_DET# — R2209 10KR2J-3-GP — DY

PCH1F — 6 OF 10 — PANTHER-GP-NF — 71.PANTH.00U

GPIO:
- S_GPIO T7
- 27 EC_VPS_SMI# A42
- DGPU_HPD_INTR# H36
- 27 EC_SCI# E38
- ICC_EN# C10
- 105 LAN_DIS# C4
- PCH_GPIO15 G2
- 56 SATA_ODD_PRSNT# U2
- 92,93 DGPU_PWROK D40
- PCH_GPIO22 T5
- PCH_GPIO24 E8
- TPAD14-OP-GFP2203 TP2203 — PCH_GPIO27 E16
- PLL_ODVR_EN P8
- 21 PSW_CLR# K1
- eSATA_DET# K4
- DMI_OVRVLTG V8
- FDI_OVRVLTG M5
- MFG_MODE N2
- 49 EDP#_LVDS M3
- TPAD14-OP-GFP TP2204 — TPM_TCM_TYPE2 V13
- TPAD14-OP-GFP TP2211 — PCH_TEMP_ALERT# V3
- TPAD14-OP-GFP2210 — USB3_PWR_ON D6
- TPAD14-OP-GFP2206 — PCH_NCTF_1 A4
- TPAD14-OP-GFP2208 — PCH_NCTF_3 A46
- TPAD14-OP-GFP2207 — PCH_NCTF_2 BF1
- TPAD14-OP-GFP2209 — PCH_NCTF_4 BF49

GPIO: BMBUSY#/GPIO0, TACH1/GPIO1, TACH2/GPIO6, TACH3/GPIO7, GPIO8, LAN_PHY_PWR_CTRL/GPIO12, GPIO15, SATA4GP/GPIO16, TACH0/GPIO17, SCLOCK/GPIO22, GPIO24, GPIO27, GPIO28, STP_PCI#/GPIO34, GPIO35, SATA2GP/GPIO36, SATA3GP/GPIO37, SLOAD/GPIO38, SDATAOUT0/GPIO39, SDATAOUT1/GPIO48, SATA5GP/GPIO49/TEMP_ALERT#, GPIO57

CPU/MISC: TACH4/GPIO68 C40 — SATA_ODD_PWRGT 56; TACH5/GPIO69 B41 — UMA_DIS# 20; TACH6/GPIO70 C41 VRAM_SIZE1; TACH7/GPIO71 A40 VRAM_SIZE2; A20GATE P4 — H_A20GATE 27; PECI AU16 H_PECI_R — DY R2203 0R2J-2-GP — H_PECI 5,27; RCIN# P5 — H_RCIN# 27; PROCPWRGD AY11 — H_CPUPWRGD 5,36; THRMTRIP# AY10 PCH_THERMTRIP_R; INIT3_3V# T14; DF_TVS AY1 NV_CLE; TS_VSS1 AH8; TS_VSS2 AK11; TS_VSS3 AH10; TS_VSS4 AK10; NC_1 P37

NCTF: VSS_NCTF_1#A4, VSS_NCTF_2#A44, VSS_NCTF_3#A45, VSS_NCTF_4#A46, VSS_NCTF_5#A5, VSS_NCTF_6#A6, VSS_NCTF_7#B3, VSS_NCTF_8#B47, VSS_NCTF_9#BD1, VSS_NCTF_10#BD49, VSS_NCTF_11#BE1, VSS_NCTF_12#BE49, VSS_NCTF_13#BF1, VSS_NCTF_14#BF49; VSS_NCTF_15#BG2, VSS_NCTF_16#BG48, VSS_NCTF_17#BH3, VSS_NCTF_18#BH47, VSS_NCTF_19#BJ4, VSS_NCTF_20#BJ44, VSS_NCTF_21#BJ45, VSS_NCTF_22#BJ46, VSS_NCTF_23#BJ5, VSS_NCTF_24#BJ6, VSS_NCTF_25#C2, VSS_NCTF_26#C48, VSS_NCTF_27#D1, VSS_NCTF_28#D49, VSS_NCTF_29#E1, VSS_NCTF_30#E49, VSS_NCTF_31#F1, VSS_NCTF_32#F49

NCTF TEST PIN: A4,A44,A45,A46,A5,A6,B3,B47, BD1,BD49,BE1,BE49,BF1,BF49, BG2,BG48,BH3,BH47,BJ4,BJ44, BJ45,BJ46,BJ5,BJ6,C2,C48,D1, D49,E1,E49,F1,F49

1D8V_S0 — R2221 2K2R2J-2-GP — NV_CLE — R2222 1KR2J-1-GP — H_SNB_IVB# 5

-1. 4/11

RN2205 SRN56J-4-GP — DY — 1D05V_VTT

PCH_THERMTRIP_R — R2204 390R2F-2GP — H_THERMTRIP# 5,36

FDI_OVRVLTG — R2208 10KR2J-3-GP

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI_OVRVLTG — R2210 10KR2J-3-GP

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

0908 SB

3D3V_S5 — R2223 10KR2J-3-GP — ICC_EN# — R2211 1KR2J-1-GP — DY

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY)- DISABLED [DEFAULT]
	LOW (R2211)- ENABLED

GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

PLL ON DIE VR ENABLE
NOTE:This signal has a weak internal pull-up 20K ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT DISABLED -- LOW (R2212 STUFFED)

PLL_ODVR_EN — DY 1 R2212 1KR2J-1-GP

<Core Design>

Wistron Corporation
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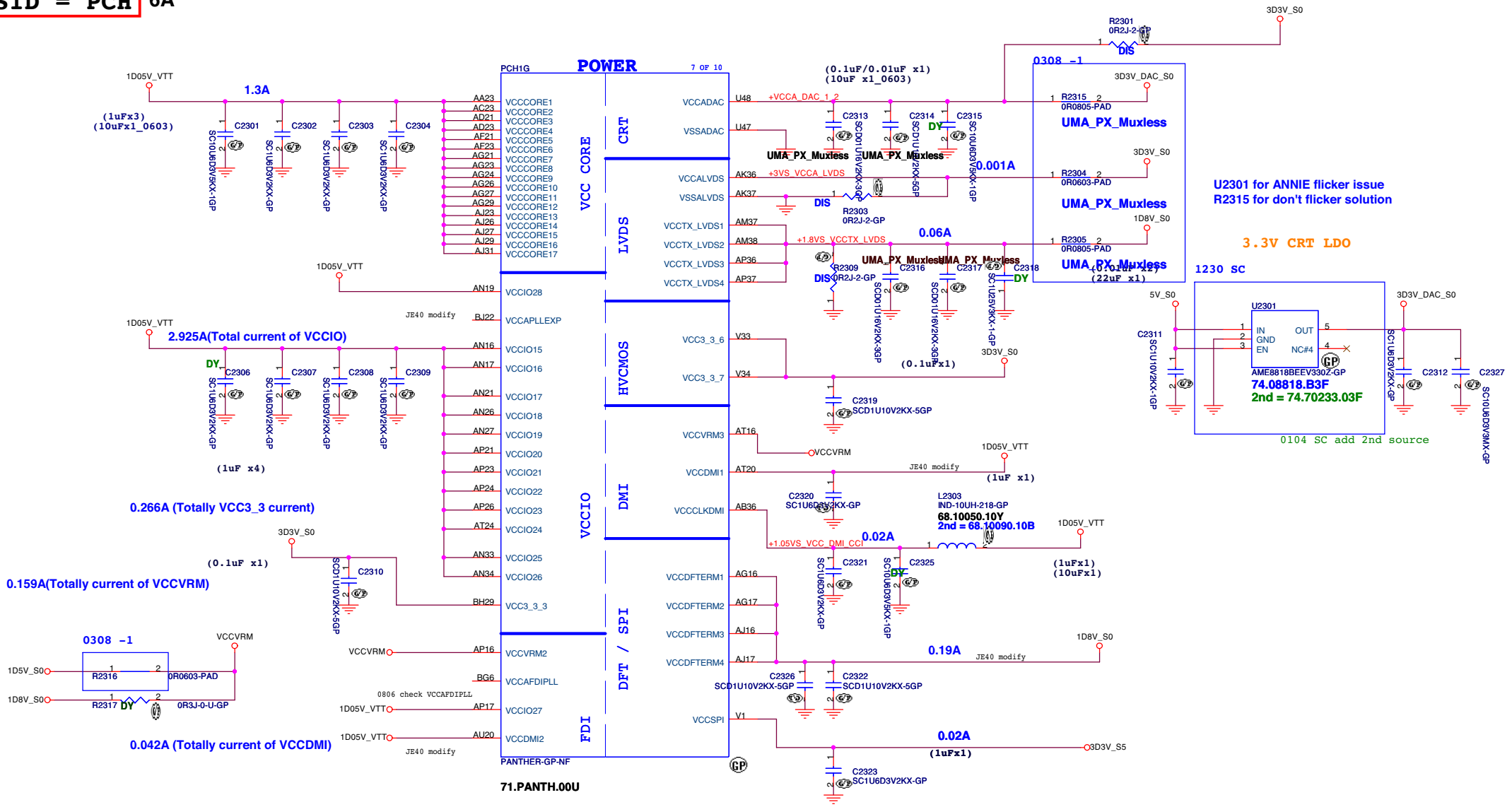
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (GPIO/CPU)
Size: Custom | Document Number: BAD40_HC | Rev: 1
Date: Thursday, April 12, 2012 | Sheet 22 of 108

SSID = PCH 6A



<Variant Name>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (POWER1)**

Size	Document Number	Rev
A3	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 23 of 108

SSID = PCH

POWER

PCH1J

PANTHER-GP-NF

71.PANTH.00U

USB

Clock and Miscellaneous

PCI/GPIO/LPC

SATA

CPU

MISC

RTC

HDA

10 OF 10

JE40 modify 07/16

JE40 modify 07/16

74.09090.A3F

83.R0304.D8F

0.002A

0.097A (Totally current of VCCSUS3_3)

0.001A

1.01A (Total current of VCCASW)

0.16A (Totally current of VCCVRM)

0.08A

0.08A

0.055A

0.095A

6uA

0.01A

68.10050.10Y

2nd = 68.10090.10B

68.10050.10Y

2nd = 68.10090.10B

0308 -1

<Variant Name>

Wistron Corporation
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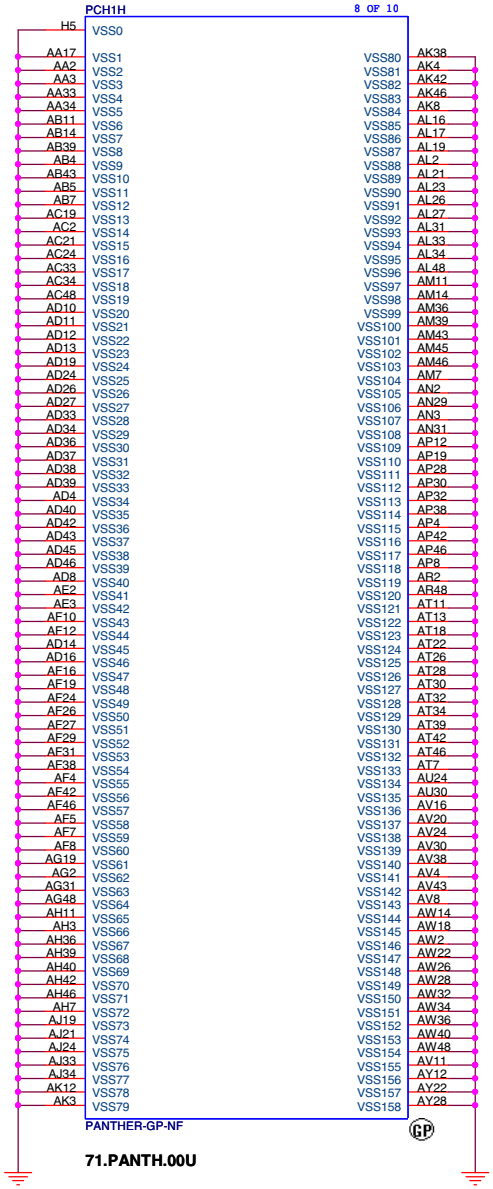
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (POWER2)

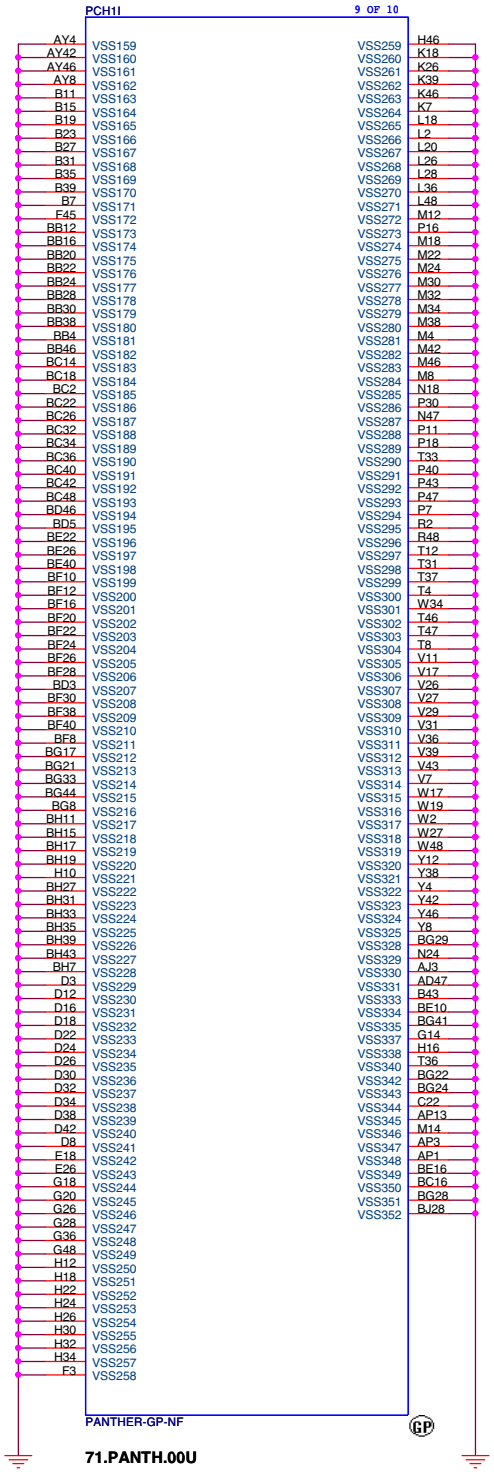
Size: A3 | Document Number: BAD40_HC | Rev: 1

Date: Thursday, April 12, 2012 | Sheet 24 of 108

SSID = PCH



71.PANTH.00U



71.PANTH.00U

<Variant Name>

緯創資通 **Wistron Corporation**
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Title: ***PCH (VSS)***

Size	Document Number	Rev
A3	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 25 of 108

<Variant Name>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title
Clock(colay)

Size	Document Number	Rev
A4	**BAD40_HC**	1

Date: Thursday, April 12, 2012 Sheet 26 of 108

SSID = KBC

H:MIC UNMUTE/L:MIC MUTE

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.48V
SD	100.0K	47.0K	2.24V
-1	100.0K	64.9K	2.0V
-2	100.0K	76.8	1.87V
-3	100.0K	100.0K	1.65V

1227 SC
Del USB_CHARGER_STATUS#

ADT_TYPE A/D(PIN99)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
65W	N/A	100.0K	3.3V
90W	100.0K	N/A	0V
30W	10.0K	100.0K	0.3V
40W	20.0K	100.0K	0.55V
120W	33.0K	100.0K	0.82V
Reserved	47.0K	100.0K	1.06V
Reserved	64.9K	100.0K	1.3V

65W_90W#
High: 65W / Low 90W
DISCRETE#
High: UMA / Low: Discrete

1128 SC for model ID reporting

MODEL_ID	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting
BAD50-HC	100.0 K	10.0 K	3.000 V	3.0054	>= 2.875 V
BAD40-HC	100.0 K	20.0 K	2.750 V	2.7591	>= 2.616 V < 2.875 V
BAD30-HC	100.0 K	33.0 K	2.481 V	2.4935	>= 2.363 V < 2.616 V

0604 Modify:
RN2704 pull-Low 10K Resistor to DY on BLUETOOTH_EN.

SB LID_CLOSE# can not pull high, because push pull suggest RN2708 Pin5 change FAN_TACH1

NOTE: Locate resistors R2719 and R2722 close to the NPCE791L.

NOTE: Connect GND and AGND planes via either 0R resistor or one point layout connection.

Prevent BIOS data loss

EC_GPIO47 High Active

NCT5606Y-0 (Addr: 0x32)

NCT5606Y-0 (Addr: 0x30)

1st = 71.00885.A0G

71.00795.00G

2nd = 84.03906.F11

84.T3906.A11

84.2N702.I31

2ND = 84.07002.I31

83.BAT54.PB1

2nd = 83.BAT54.N81

HR PX	
Title	KBC Nuvoton NPCE795
Size / Document Number	BAD40_HC
Rev	1
Date	Thursday, April 12, 2012
Sheet	27 of 108

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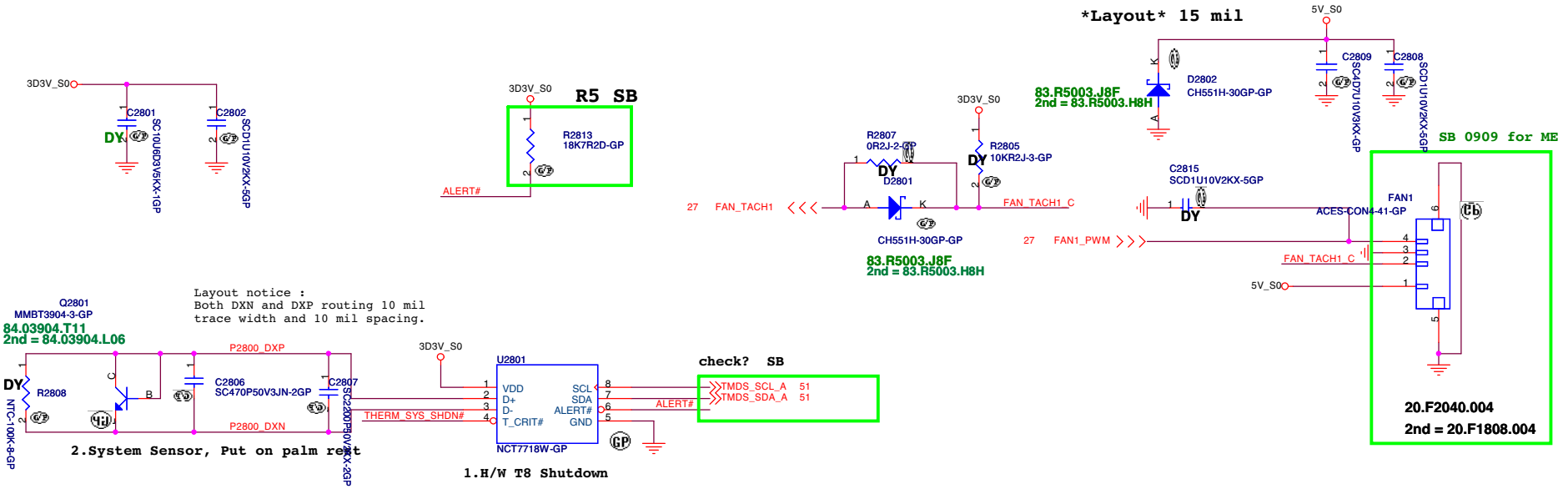
SSID = Thermal

Fan controller P2793

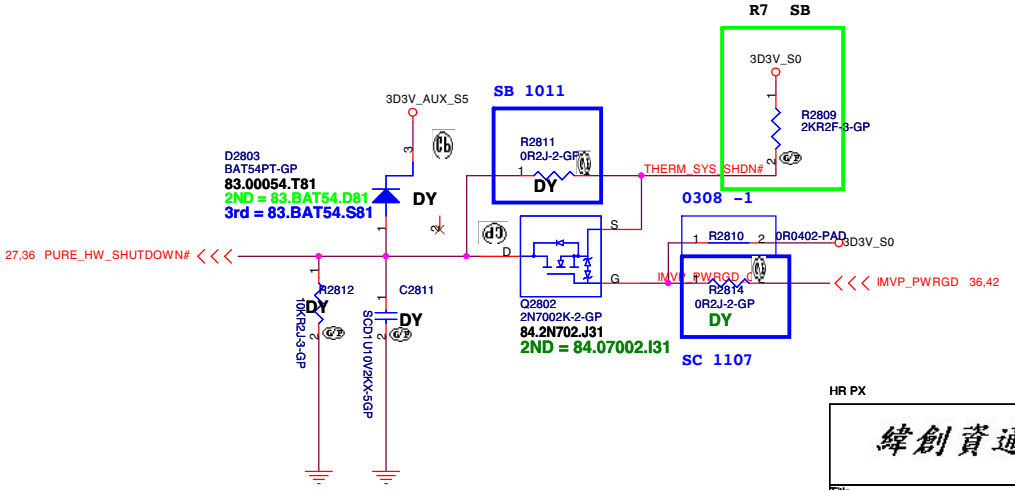
Layout 15 mil



ALERT# /T_CRIT#
Pull-up Resistor

R5 \ R7	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
2Kohm	77℃	87℃	97℃	107℃	117℃
7.5Kohm	79℃	89℃	99℃	109℃	119℃
10.5Kohm	81℃	91℃	101℃	111℃	121℃
14Kohm	83℃	93℃	103℃	113℃	123℃
18.7Kohm	85℃	95℃	105℃	115℃	125℃

T_CRIT temperature strapping point



HR PX

緯創資通 Wistron Corporation
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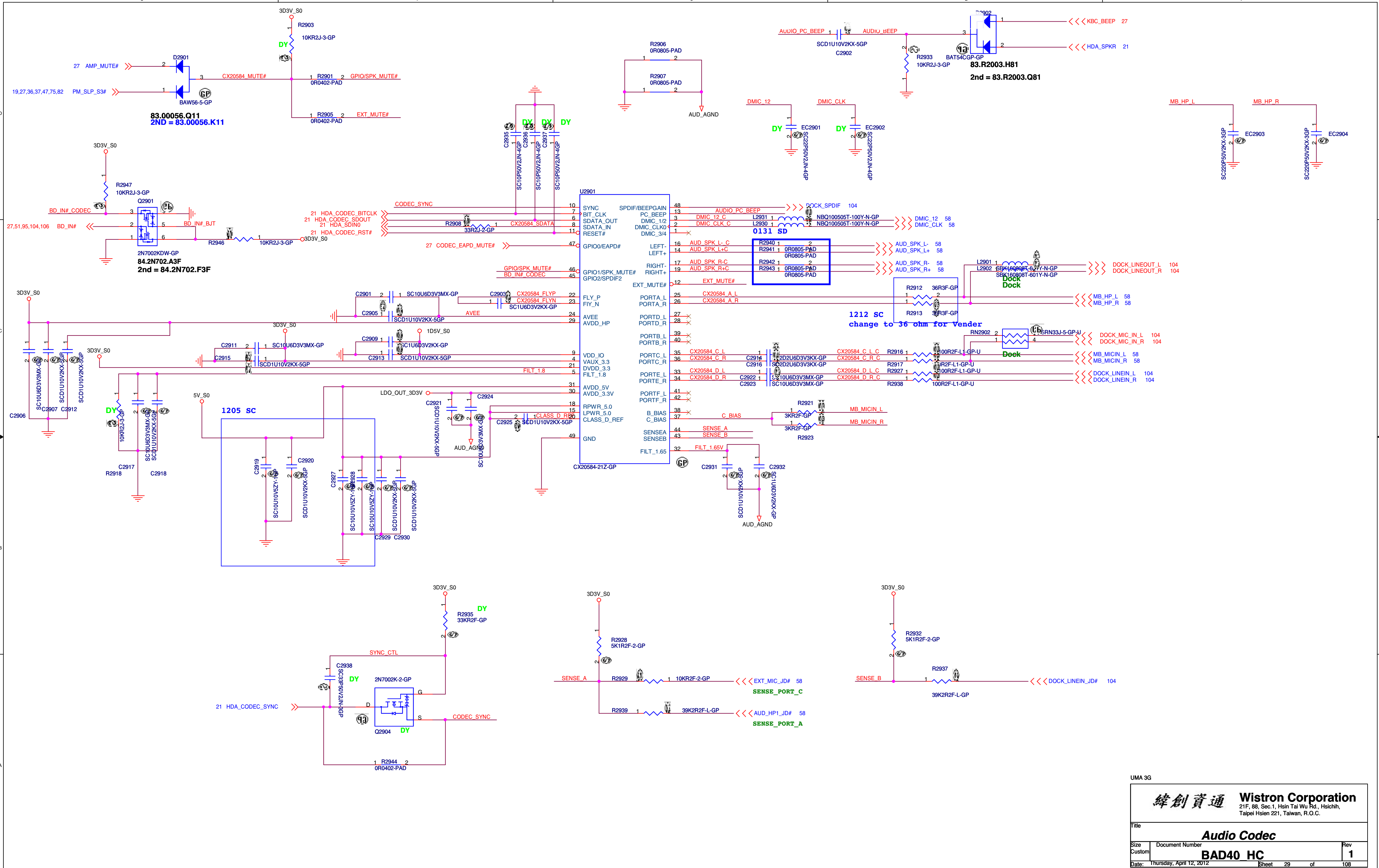
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal T7718/Fan Controllor P2793

Size	Document Number	Rev
Custom	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 28 of 108



UMA 3G

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	*Audio Codec*
Size: Custom	Document Number: BAD40_HC — Rev 1
Date: Thursday, April 12, 2012	Sheet 29 of 108

AUDIO OP AMPLIFIER

<Variant Name>

緯創資通 Wistron Corporation
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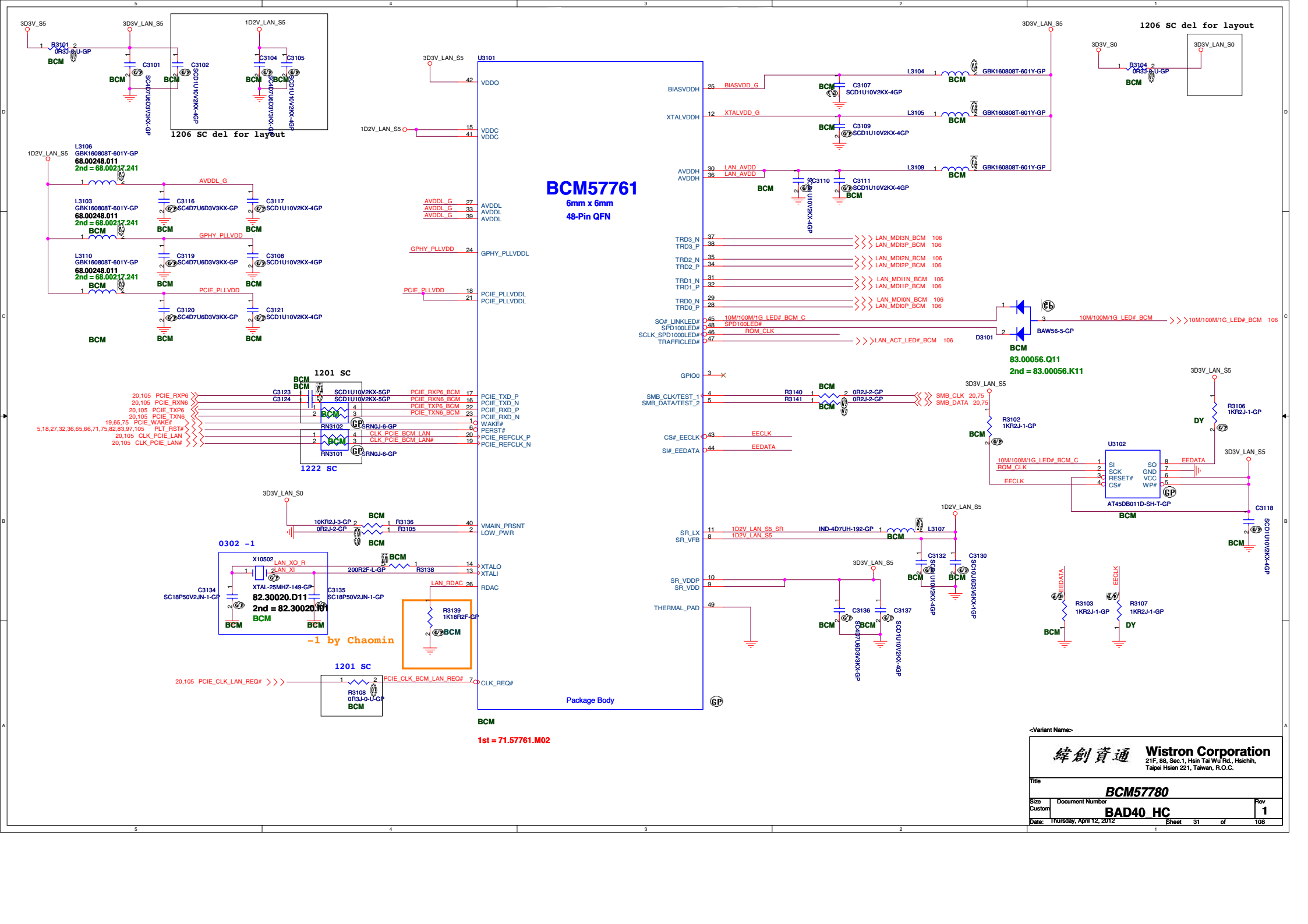
Title

Audio AMP

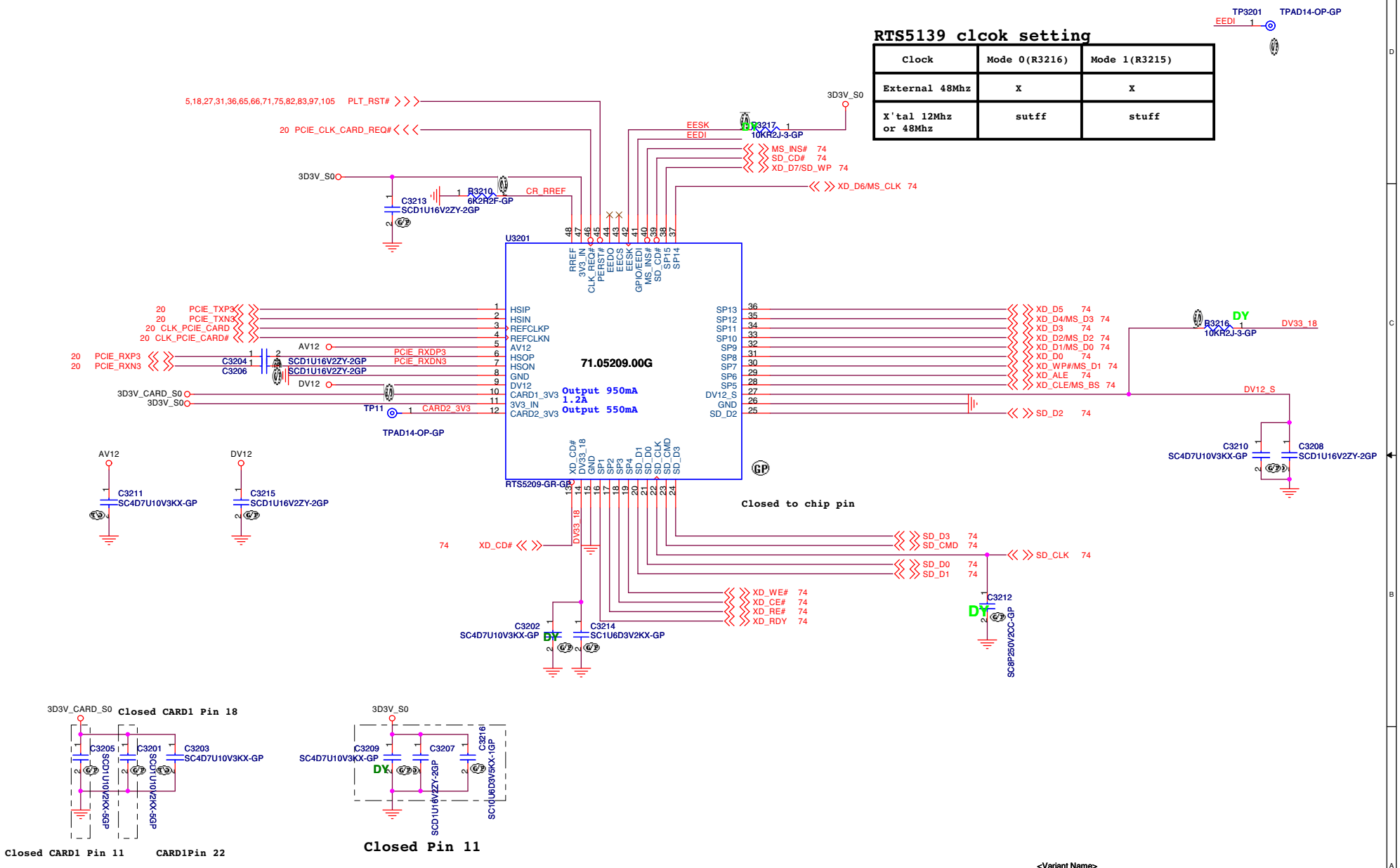
Size	Document Number	Rev
A4	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 30 of 108


BCM57761
6mm x 6mm
48-Pin QFN
Package Body
U3101
1206 SC del for layout
1201 SC
1222 SC
0302 -1
-1 by Chaomin
1206 SC del for layout
BCM
1st = 71.57761.M02
83.00056.Q11
2nd = 83.00056.K11
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
BCM57780
BAD40_HC
Rev 1
Thursday, April 12, 2012
Sheet 31 of 108

RTS5139 clcok setting

Clock	Mode 0(R3216)	Mode 1(R3215)
External 48Mhz	X	X
X'tal 12Mhz or 48Mhz	sutff	stuff



<Variant Name>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***RTS5209(CARD READER)***

Size	Document Number	Rev
A3	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 32 of 108

(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: ***Reserved***

Size	Document Number	Rev
A4	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 33 of 108

<Variant Name>

緯創資通 **Wistron Corporation**

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Title

Reserved

Size	Document Number	Rev
A3	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 34 of 108

reserve

HR

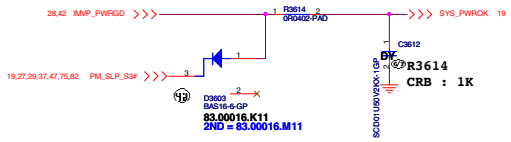
緯創資通 **Wistron Corporation**
21F, 68, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB 3.0 Controller***

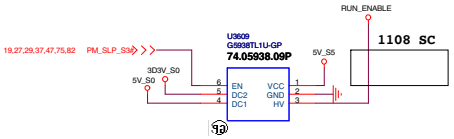
Size	Document Number	Rev
Custom	BAD40_HC	1

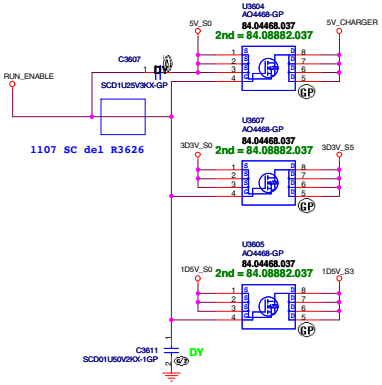
Date: Thursday, April 12, 2012 Sheet 35 of 108

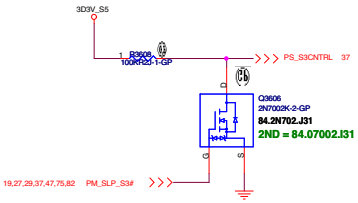
Power Sequence

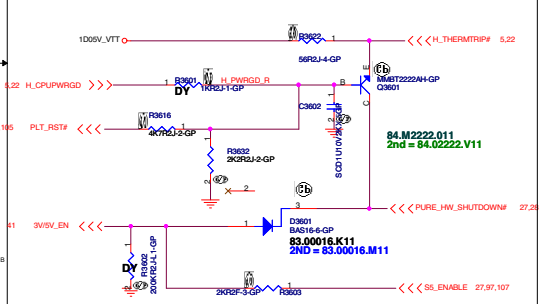


ANNIE Run Power

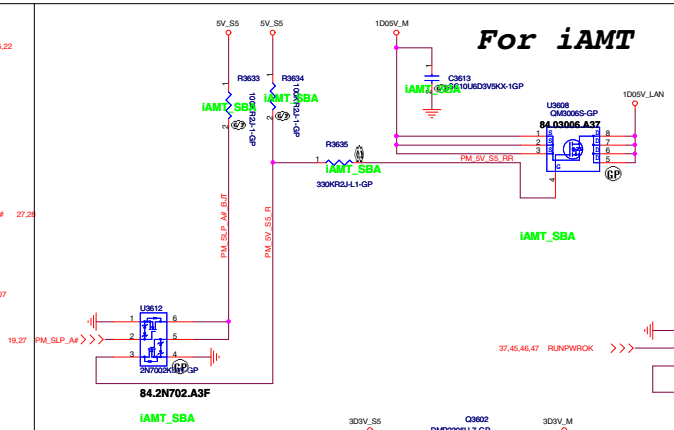


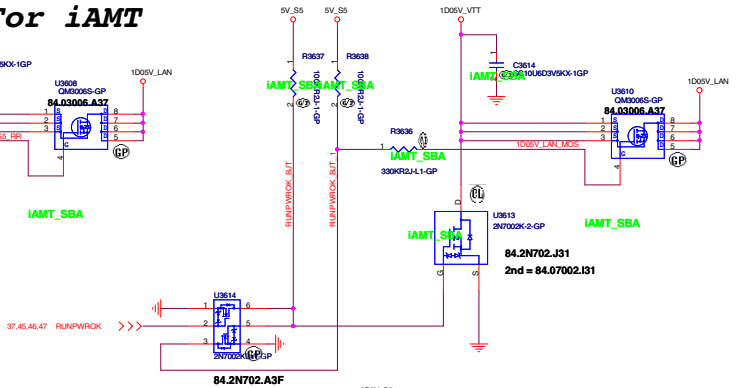






For iAMT

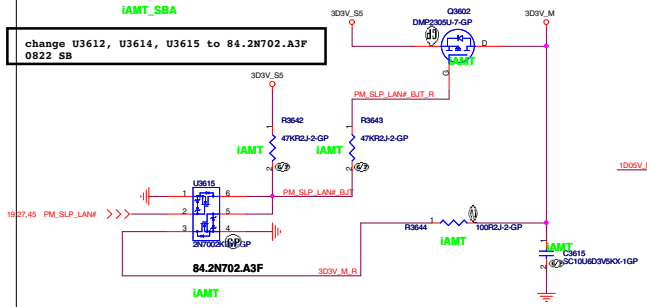


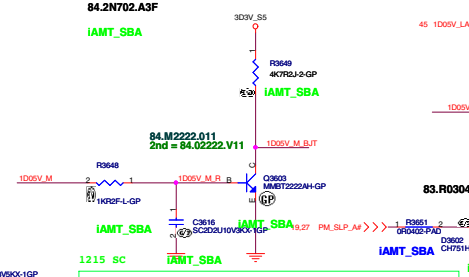


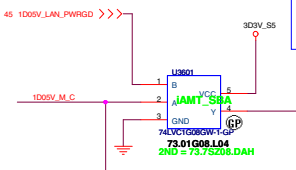
0312 -1 del for layout

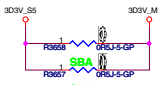
0412 -1M del for layout

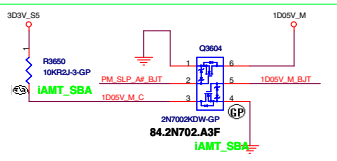
change U3612, U3614, U3615 to 84.2N702.A3F
0822 SB











HR PX

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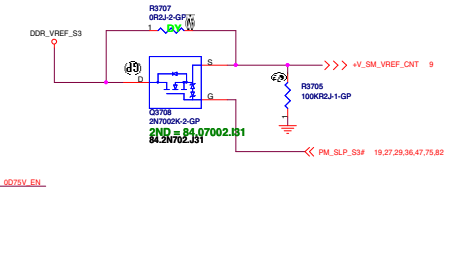
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable

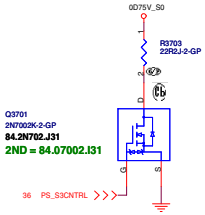
Size	Document Number	Rev
Custom	BAD40 HC	1

Date: Thursday, April 12, 2012 Sheet 36 of 108

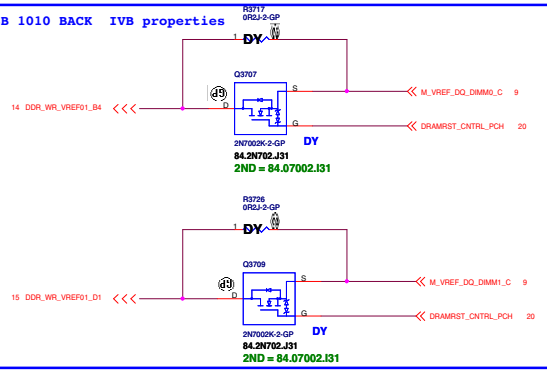
Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation

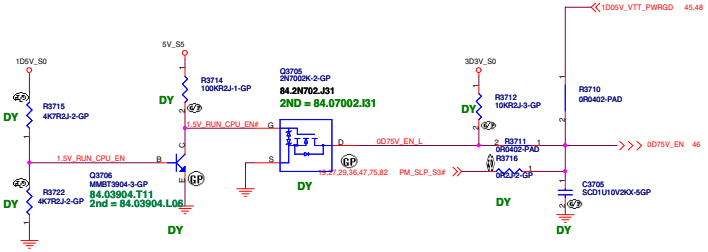


Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK

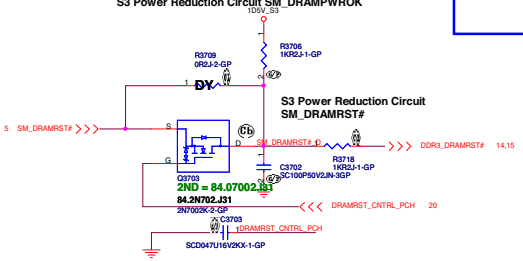


SB 1010 BACK IVB properties



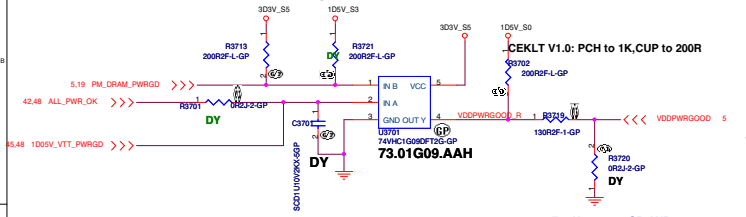


Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



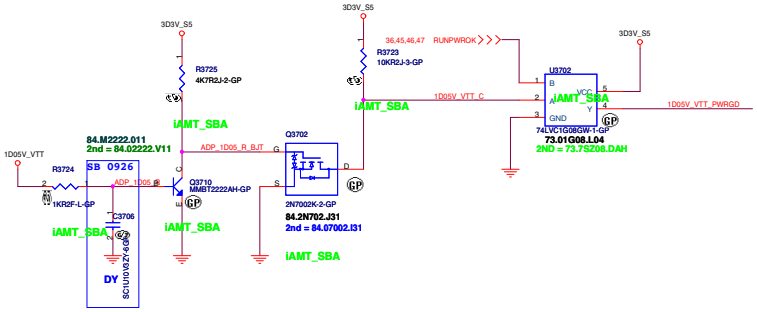
S3 Power Reduction Circuit
SM_DRAMRST#

Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



CEKLT V1.0: PCH to 1K,CUP to 200R

For U3701 not OD AND gate
R3719 to 64.15015.6DL
R3720 to 64.75005.6DL
R3702 to DY



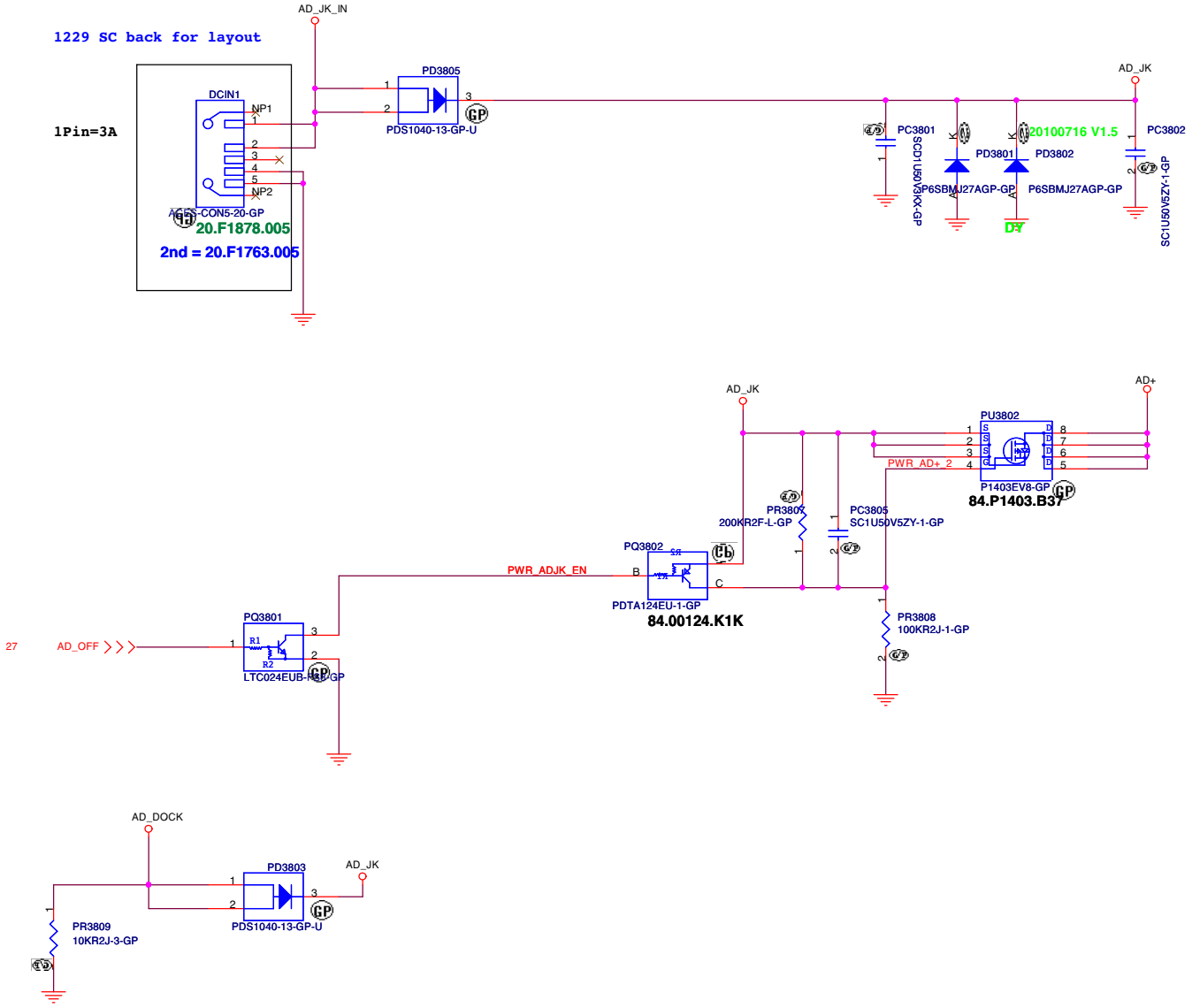
HR PX

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ADAPTER

Size	Document Number	Rev
Custom	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 37 of 108

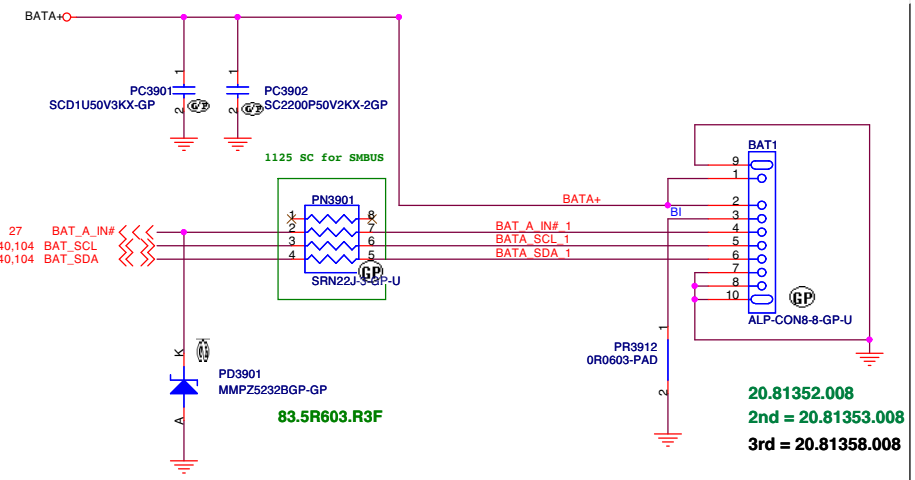


<Variant Name>

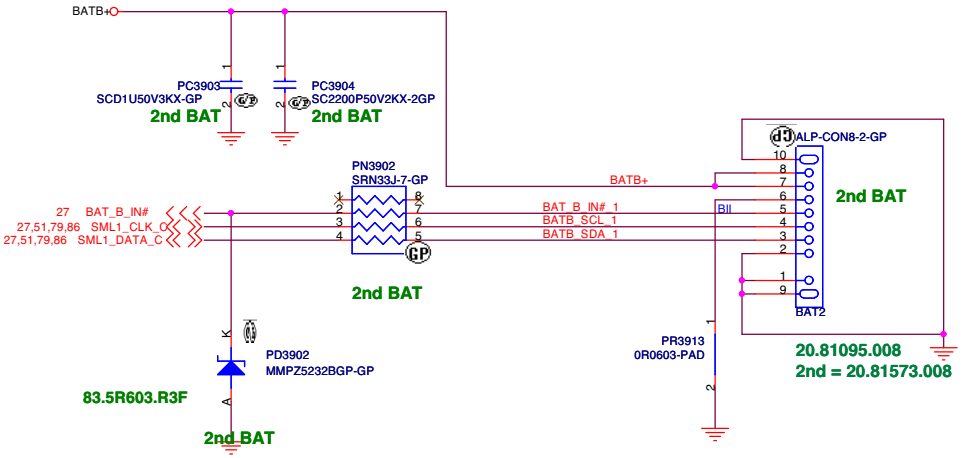
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***DCIN JACK***	
Size A3	Document Number **BAD40_HC**	Rev **1**
Date: Thursday, April 12, 2012	Sheet 38 of 108	

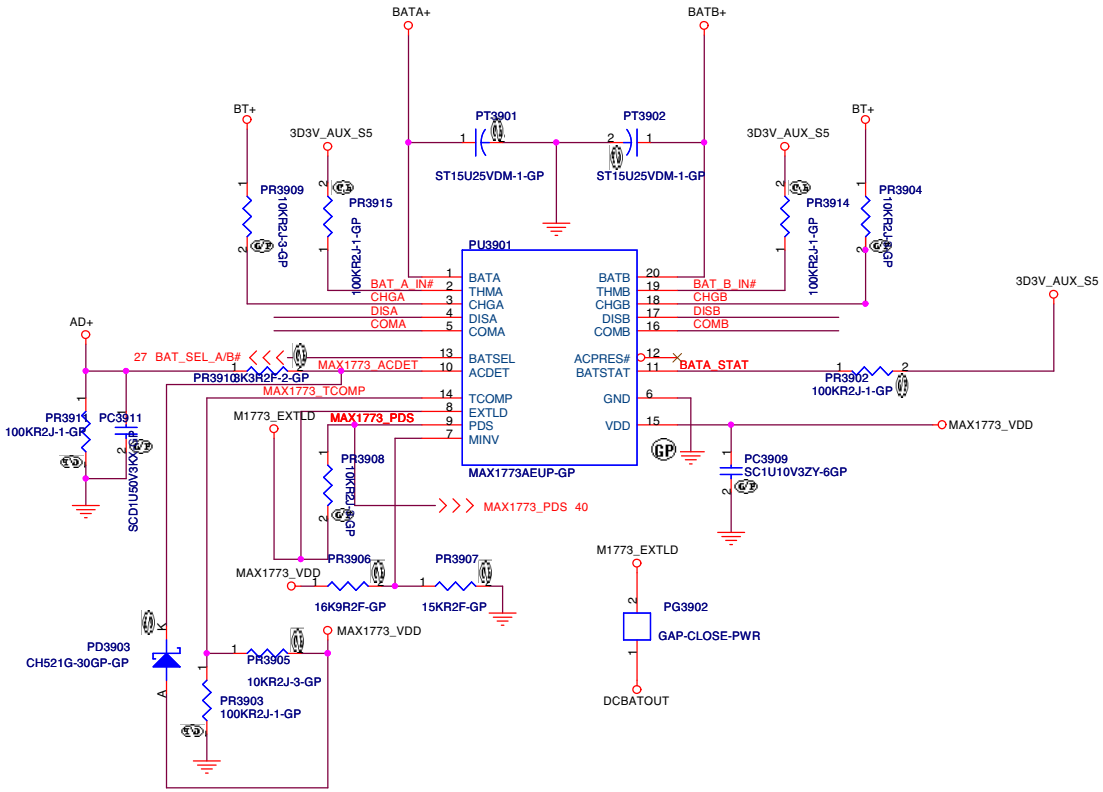
MAIN BATTERY CONNECTOR



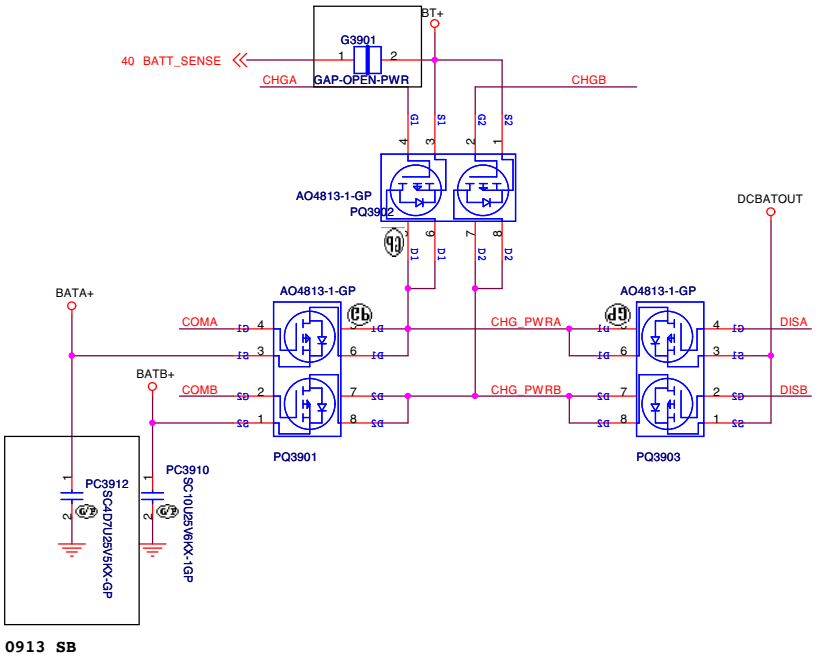
2nd BATTERY CONNECTOR



BATTERY SWITCH



1108 SC



0913 SB

HR PX

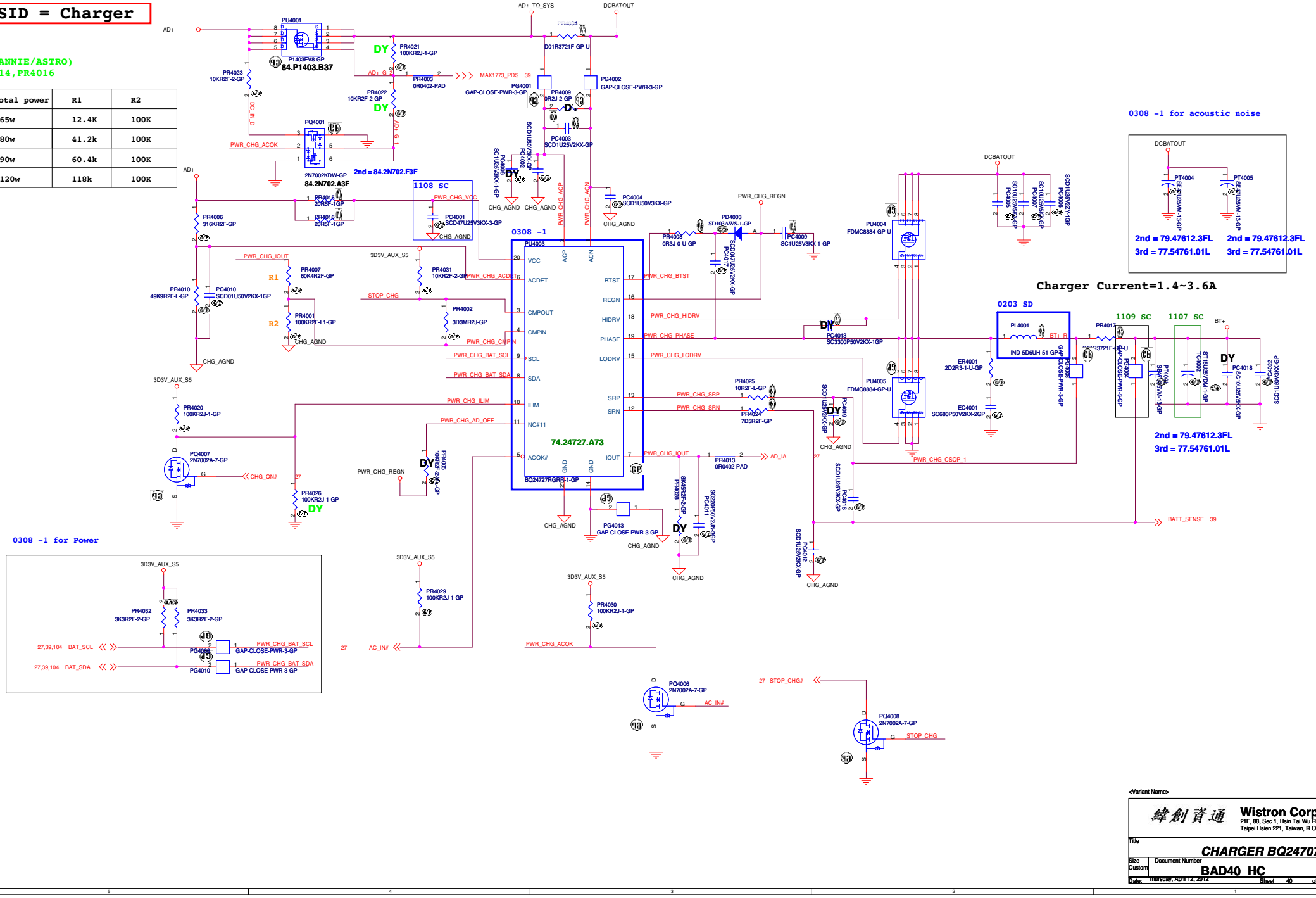
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	BATT_CONN	
Size A3	Document Number BAD40_HC	Rev 1
Date: Thursday, April 12, 2012	Sheet 39 of 108	

SSID = Charger

A8(ANNIE/ASTRO)
PR4014,PR4016

AD+ total power	R1	R2
65w	12.4K	100K
80w	41.2k	100K
90w	60.4k	100K
120w	118k	100K



<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: CHARGER BQ24707A		
Size: Custom	Document Number: BAD40_HC	Rev: 1
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0315 -1
del close gap for Layout

1205 SC for Power

PR4104 change to 41.2k

1222 SC del GAP for layout

1125 SC for RF

1212 SC change to 84.03664.037 for Power

1125 SC for RF

0308 -1
change to 47U
for acoustic noise

2nd = 79.47612.3FL
3rd = 77.54761.01L

Iomax=30A
OCP>40A

SB 0923

1114 SC For EMI

1107 SC

2nd = 79.22710.20L

Iomax=6A
OCP>10A

Vz=3.9V
UVP Function
DCBATOUT<7.5V 3/5V disable

0118 SD for Power

1114 SC for EMI

0308 -1
for acoustic noise

0308 -1

74.08239.B73

84.2N702.A3F
2nd = 84.2N702.F3F

83.3R903.D3F

<Variant Name>

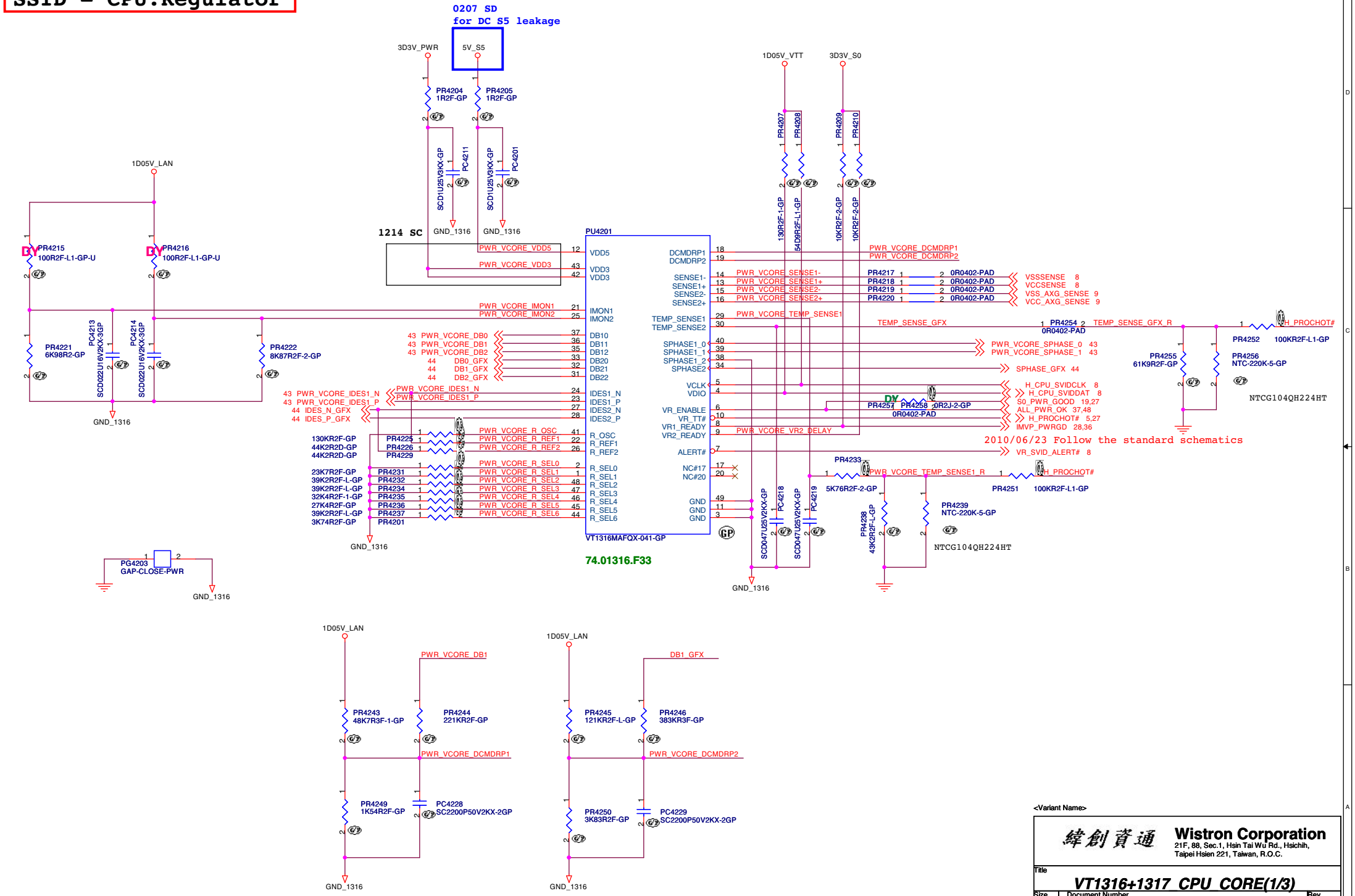
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

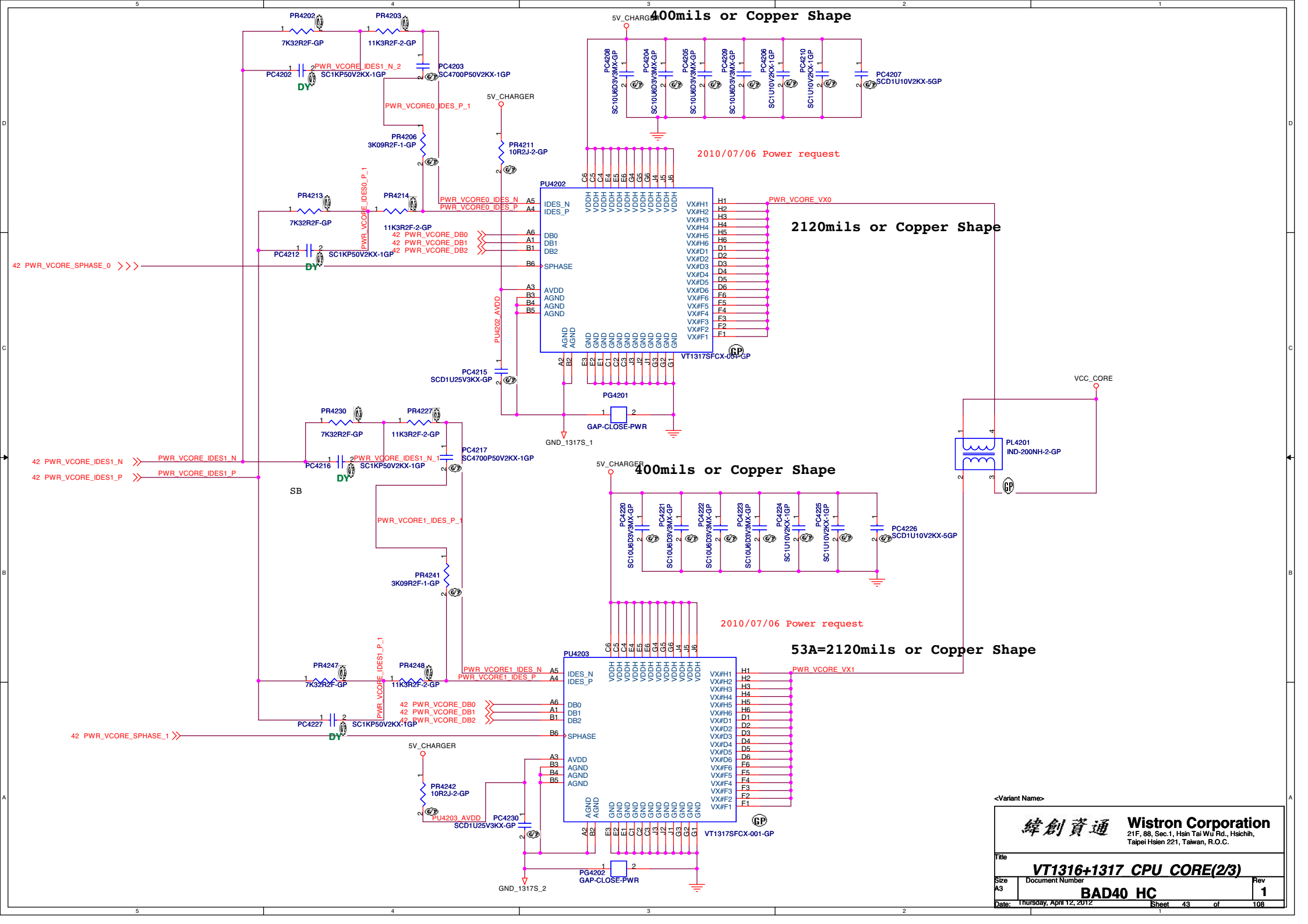
Title: RT8329 5V/3D3V

Size	Document Number	Rev
Custom	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 41 of 108

SSID = CPU.Regulator





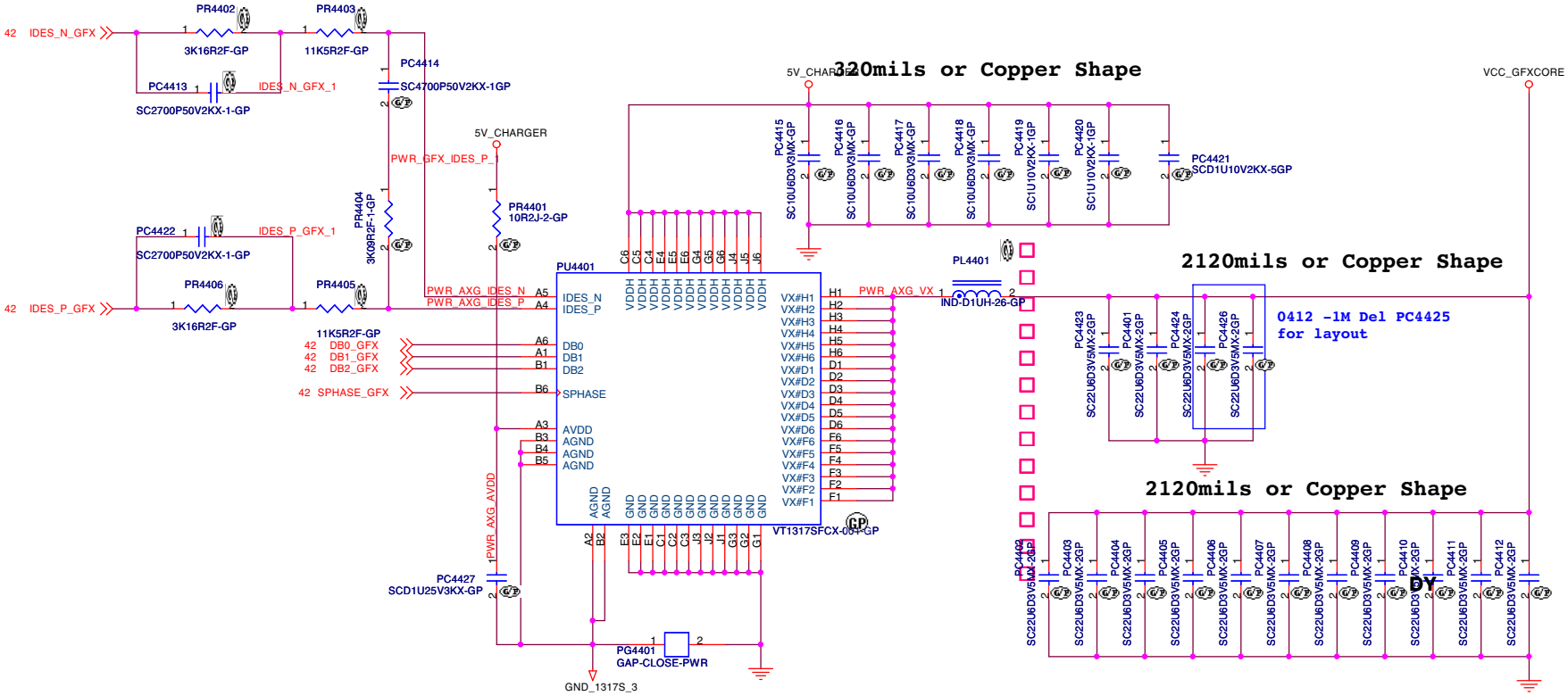
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VT1316+1317_CPU_CORE(2/3)

Size	Document Number	Rev
A3	BAD40 HC	1

Date: Thursday, April 12, 2012 Sheet 43 of 108



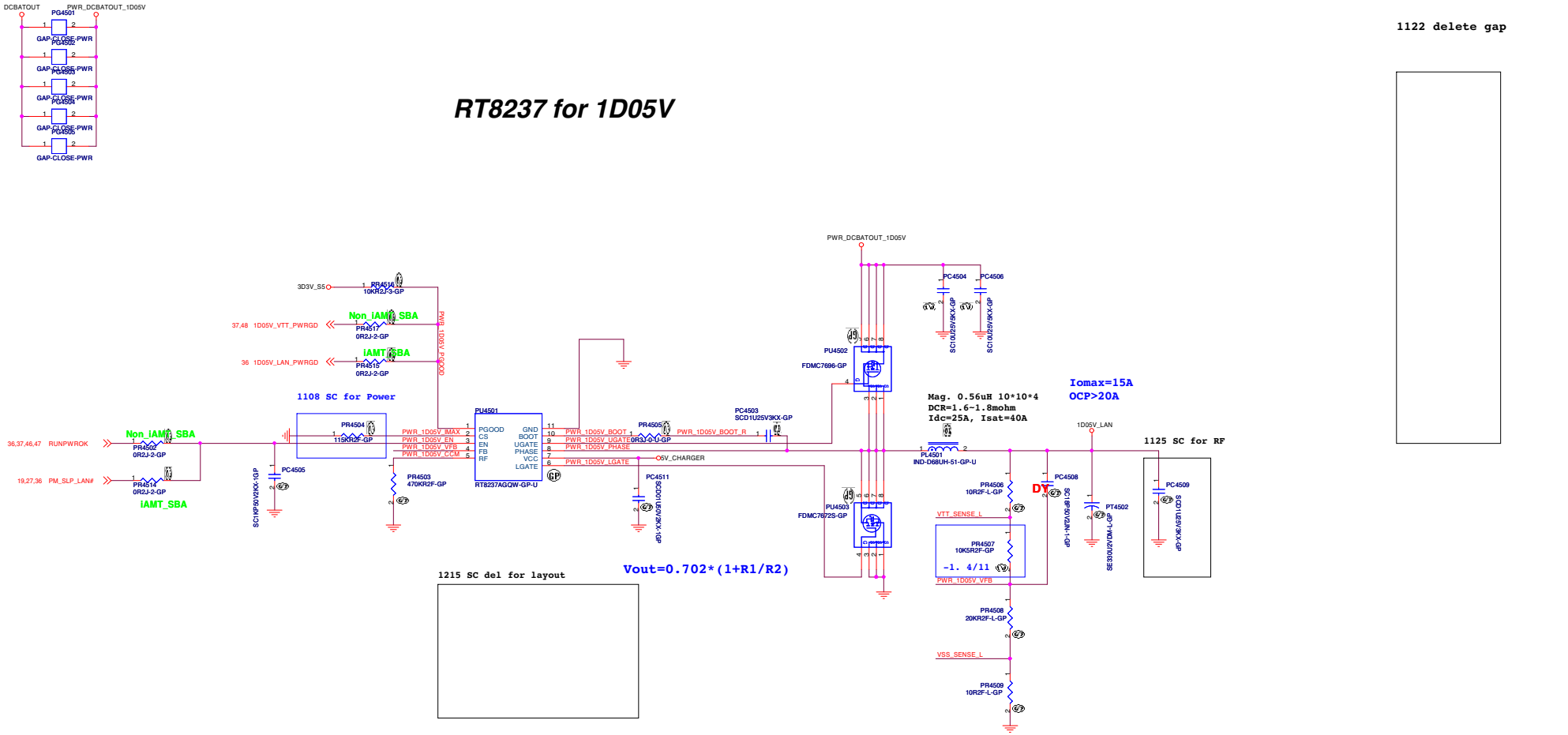
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VT1316+1317 CPU CORE(3/3)

Size: A3 | Document Number: BAD40 HC | Rev: 1

Date: Thursday, April 12, 2012 | Sheet 44 of 108



<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: DC to DC_1D05V(RT8237)		
Size: A2	Document Number: BAD40_HC	Rev: 1
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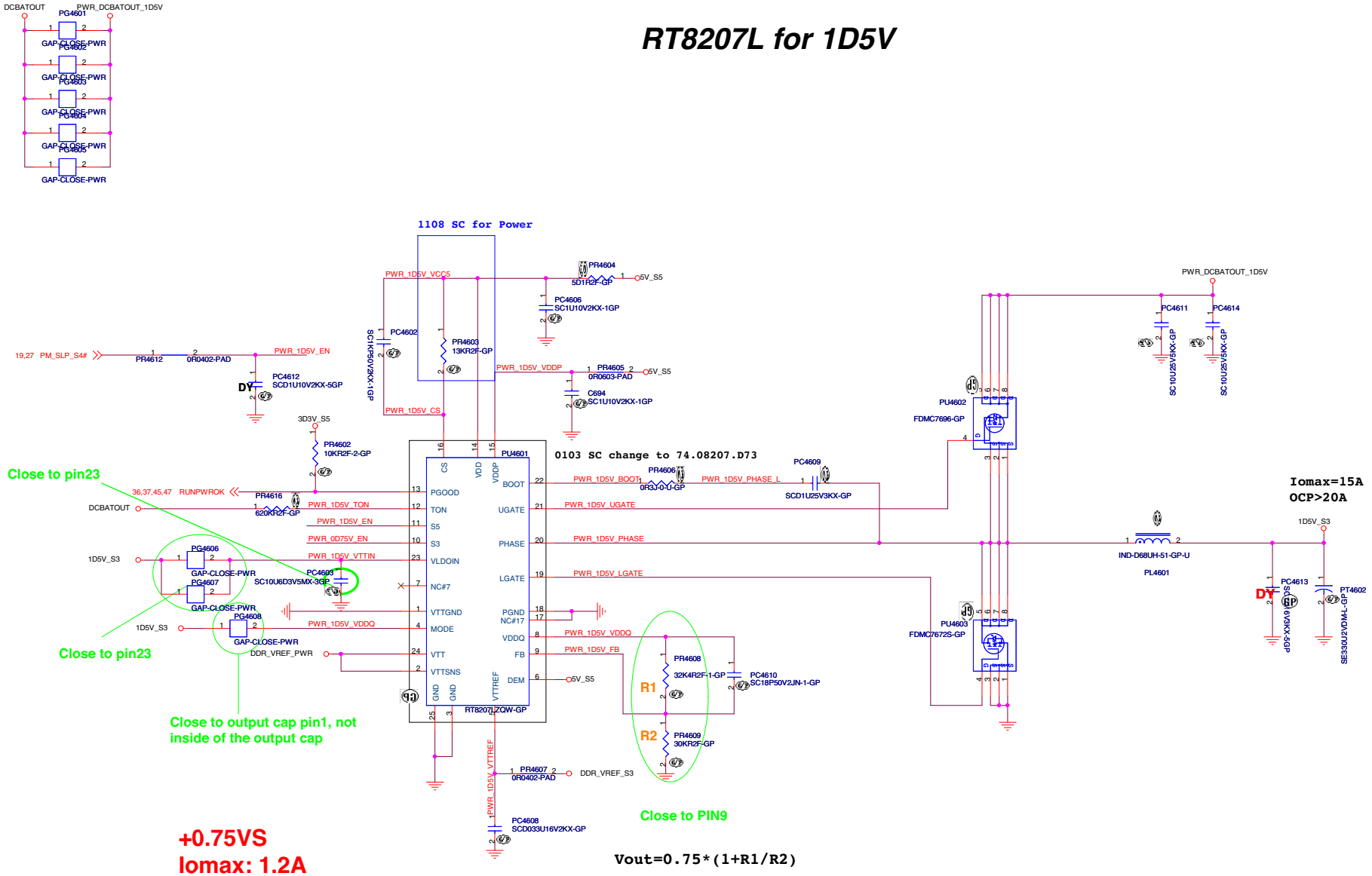
SSID = PWR.Plane.Regulator_1p5v0p75v

RT8207L for 1D5V

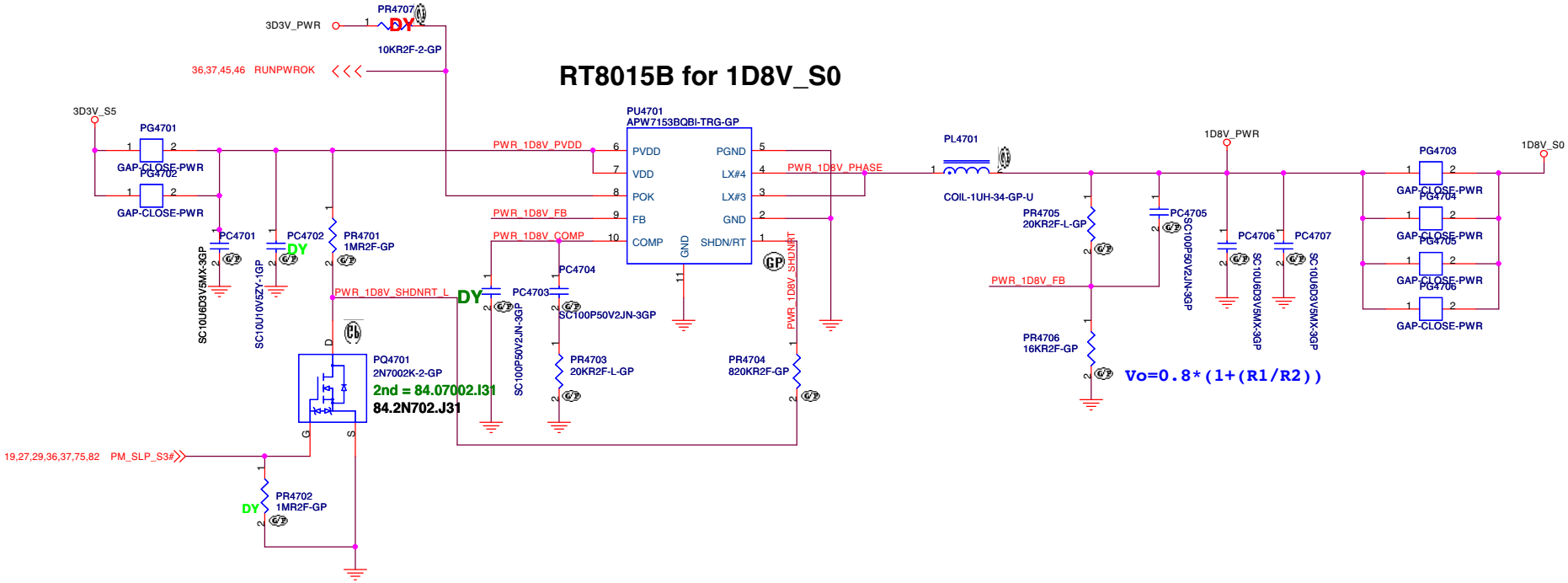


<variant_name>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	RT8207L_+1.5V_SUS	
Size: Custom	Document Number: BAD40_HC	Rev: 1
Date: Thursday, April 12, 2012	Sheet 46 of 108	

SSID = PWR.Plane.Regulator_1p8v

RT8015B for 1D8V_S0



<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***DC CONVERTER_1D8V(RT8015A)***	
Size A3	Document Number **BAD40_HC**	Rev **1**
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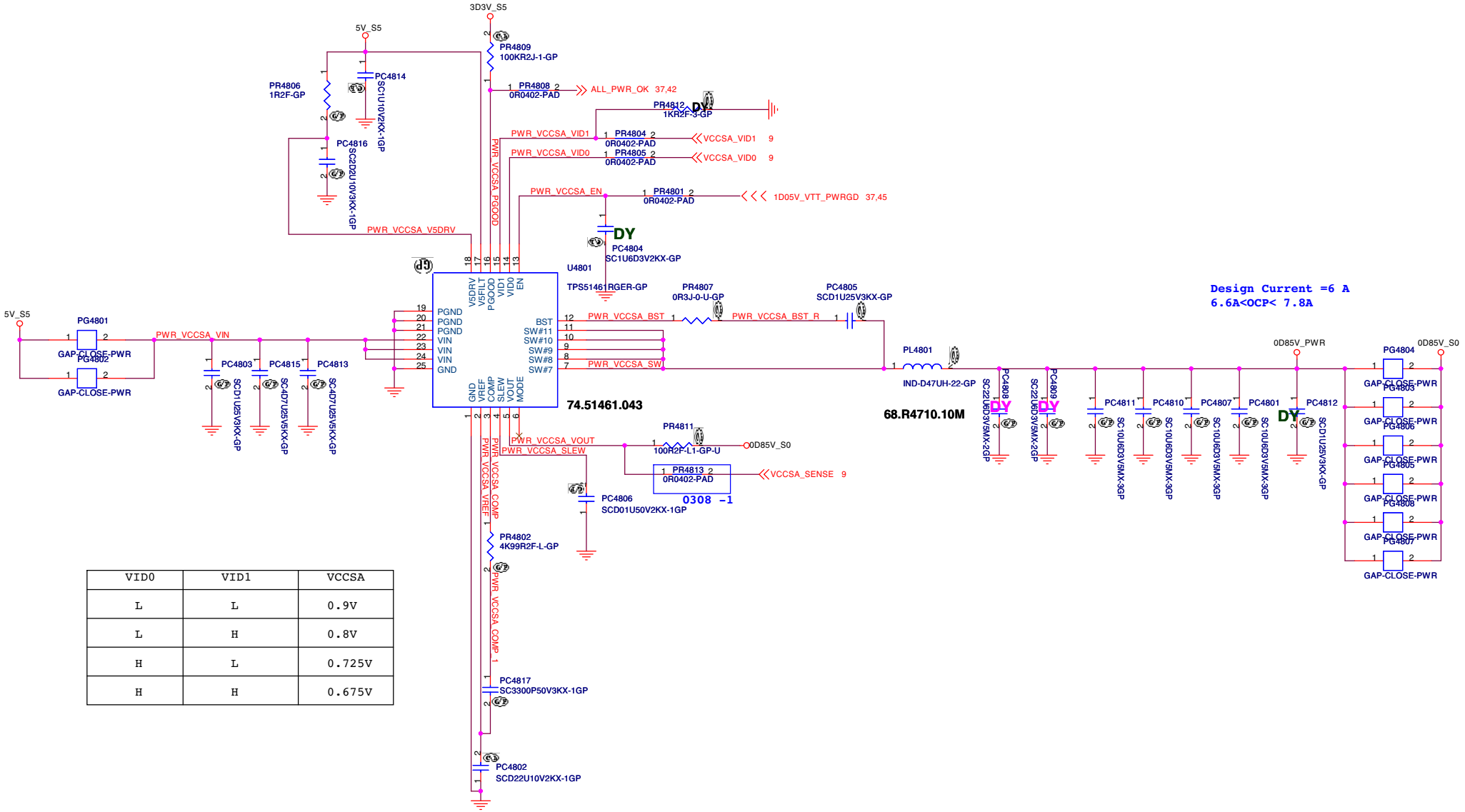
TPS51461 for VCCSA



VID0	VID1	VCCSA
L	L	0.9V
L	H	0.8V
H	L	0.725V
H	H	0.675V

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

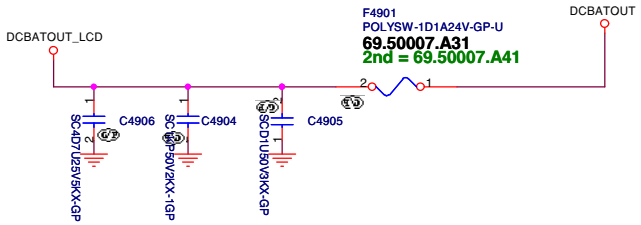
Title: DC CONVERTER VCCSA(TPS51461)

Size	Document Number	Rev
A3	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 48 of 108

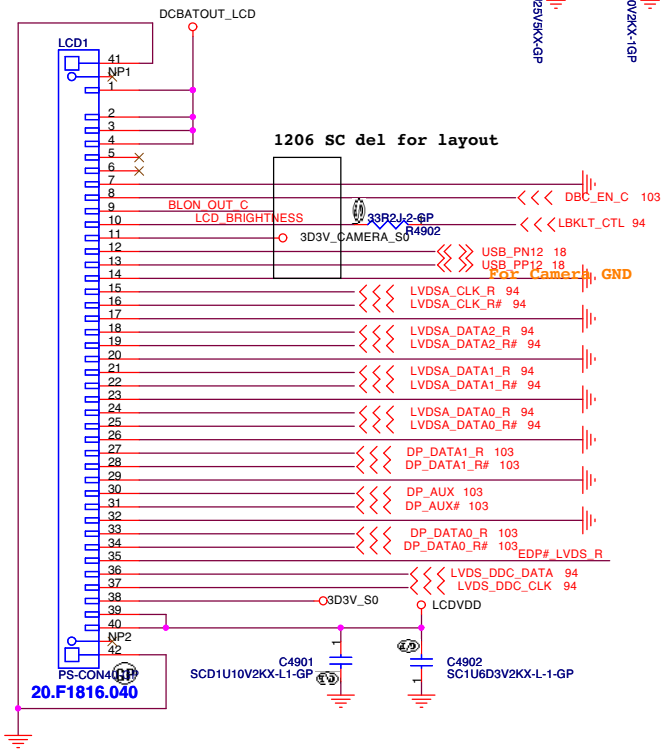
SSID = VIDEO

INVERTER POWER

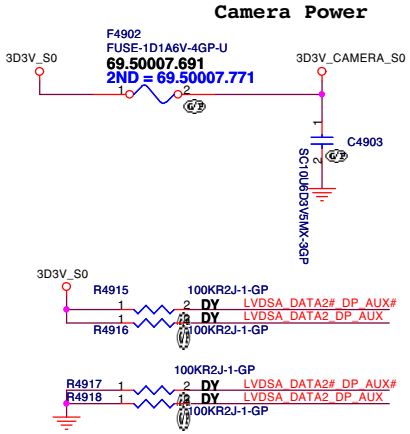


1122 SC del EDP&LVDS colay

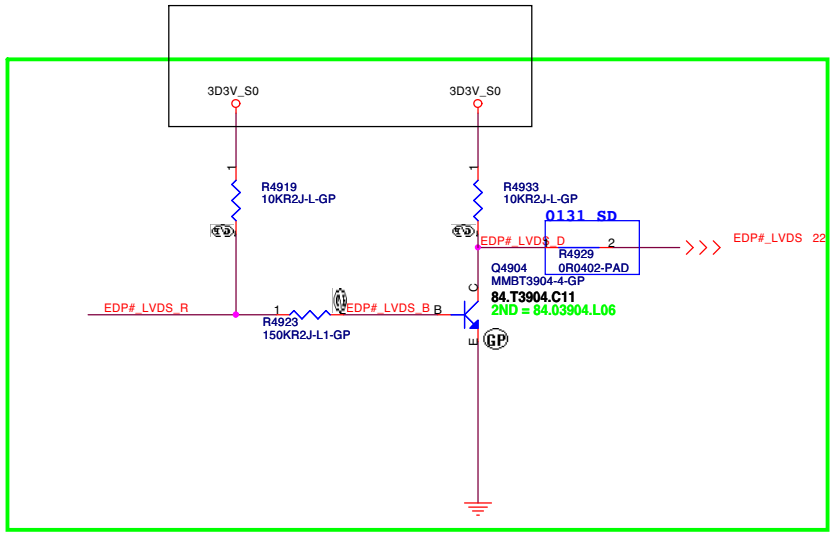
LVDS CONNECTOR



Camera Power

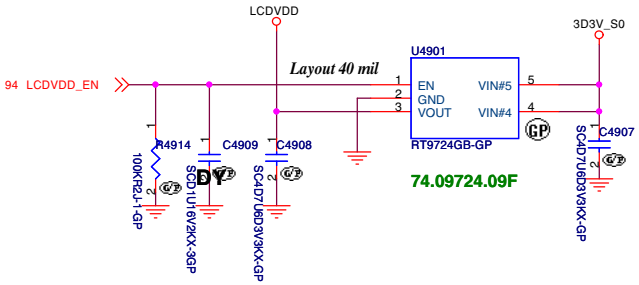


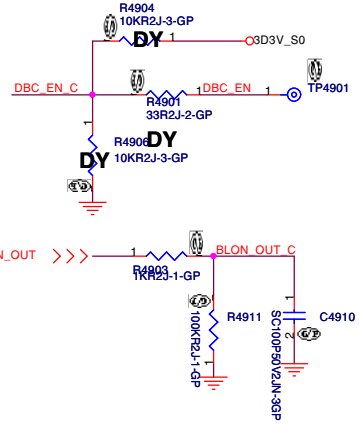
1121 SC



SSID = VIDEO

LCD POWER for ANNIE





<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD Connector

Size	Document Number	Rev
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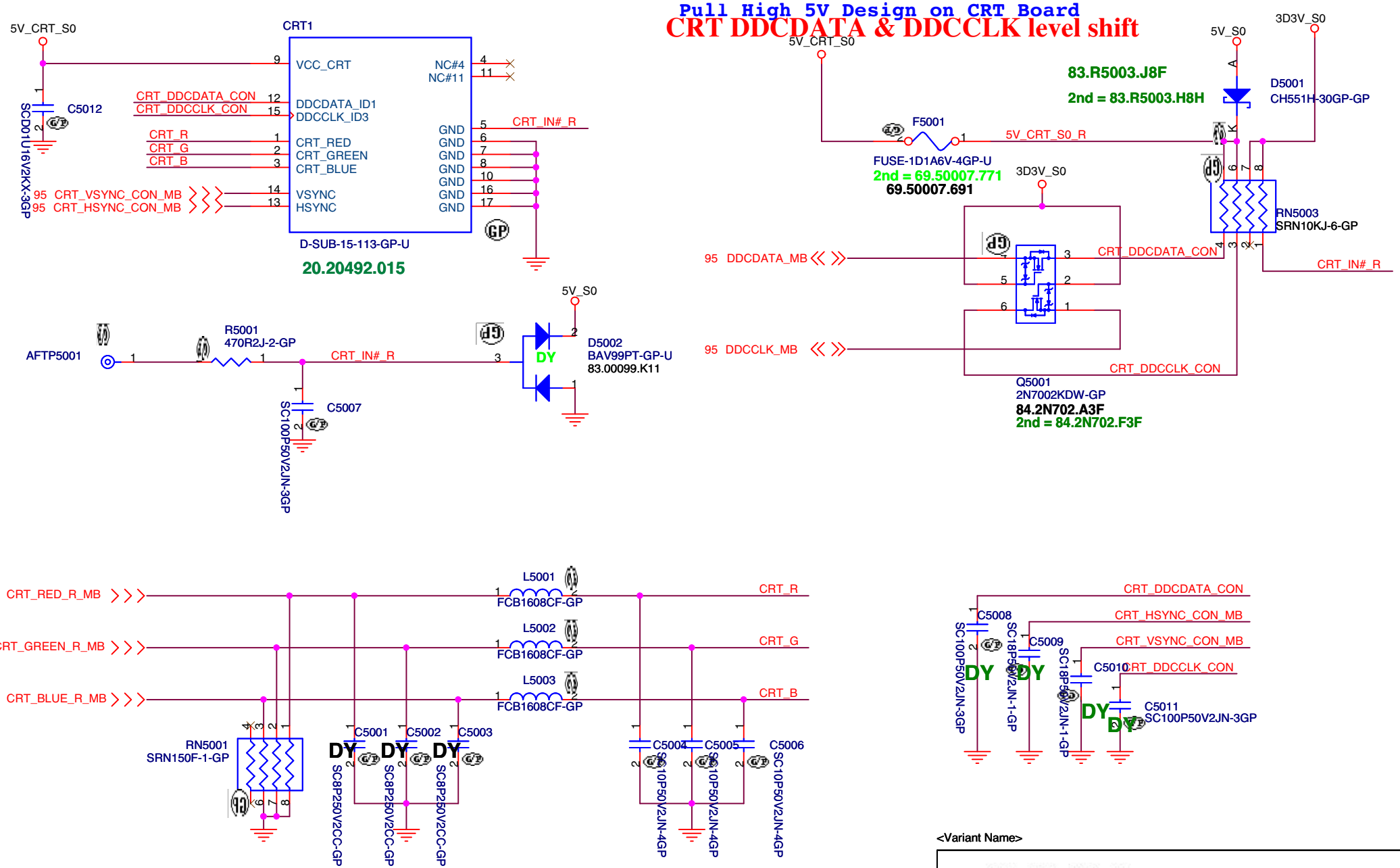
Pull High 5V Design on CRT Board

CRT DDCDATA & DDCCLK level shift



<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***CRT Connector***	
Size A4	Document Number **BAD40_HC**	Rev 1
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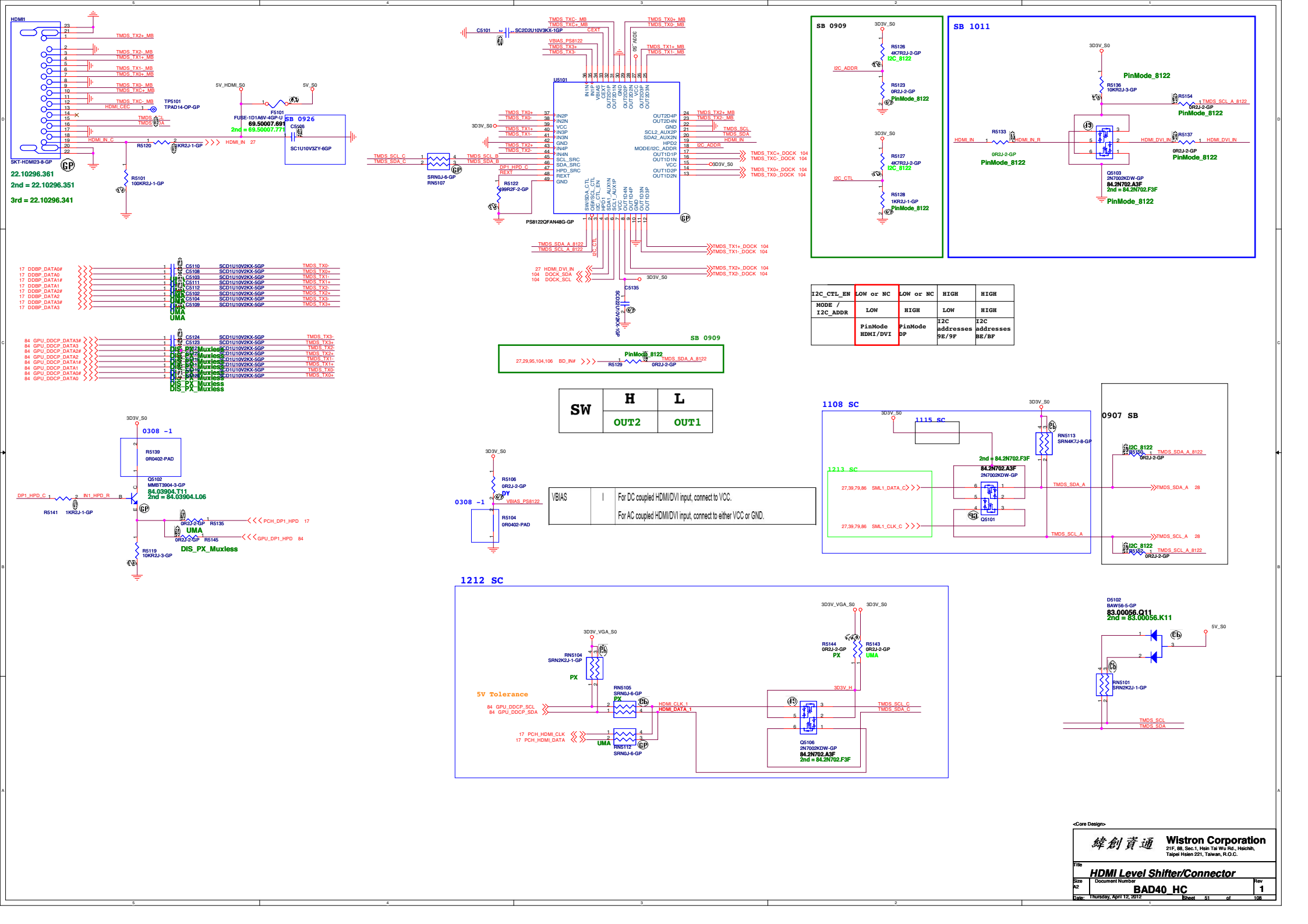

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter/Connector

Size: A2 | Document Number: BAD40_HC | Rev: 1

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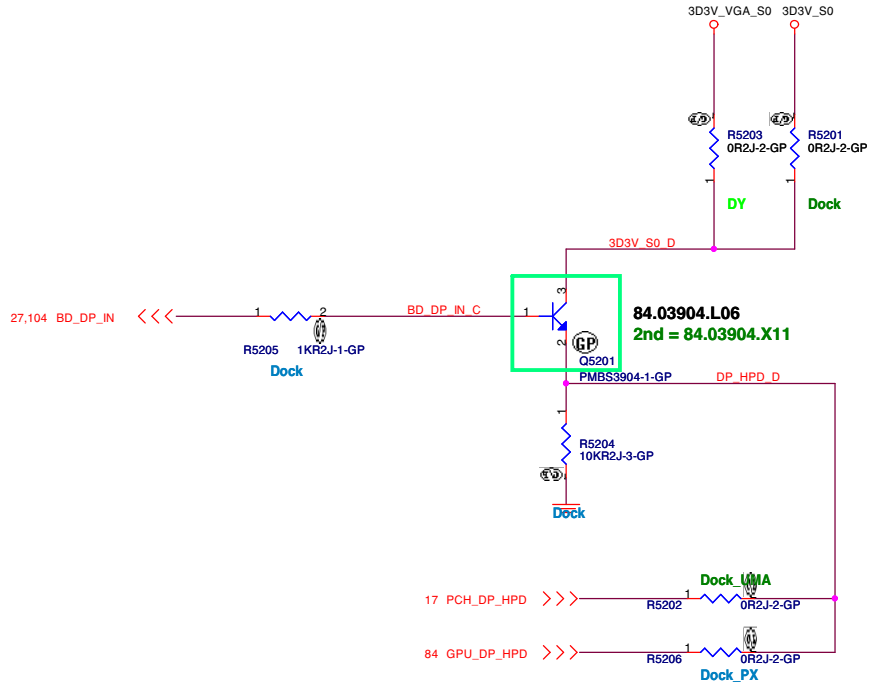
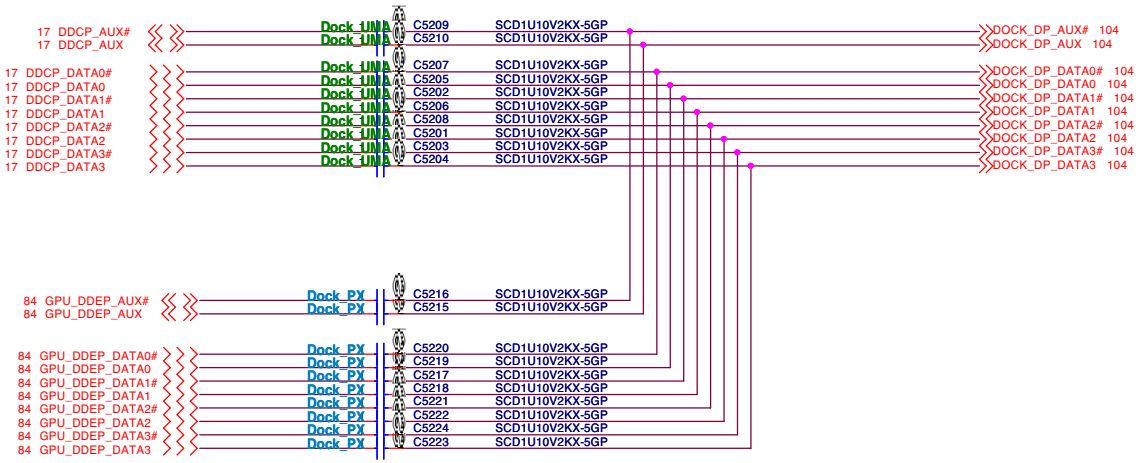
DP





HR PX

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Display Port***		
Size: A3	Document Number: **BAD40_HC**	Rev: 1
Date: Thursday, April 12, 2012	Sheet 52 of 108	

(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***S-VIDEO***

Size	Document Number	Rev
A4	BAD40_HC	1

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(Blanking)

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
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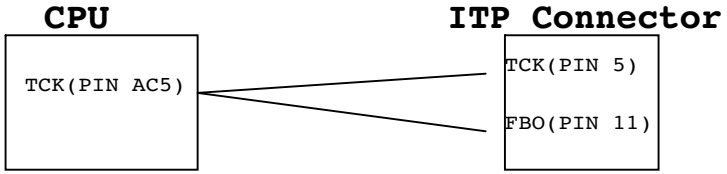
SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



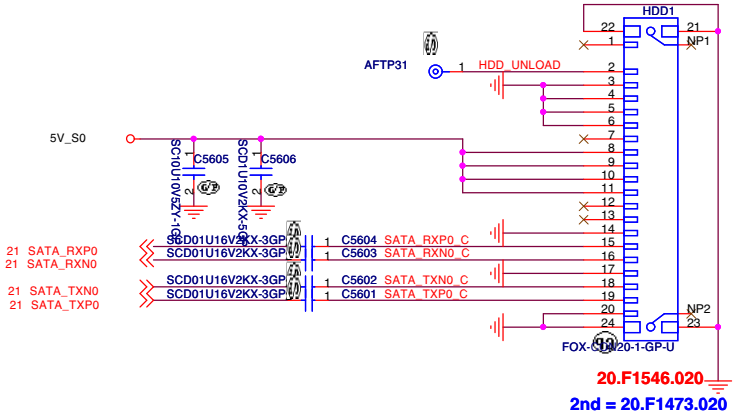
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

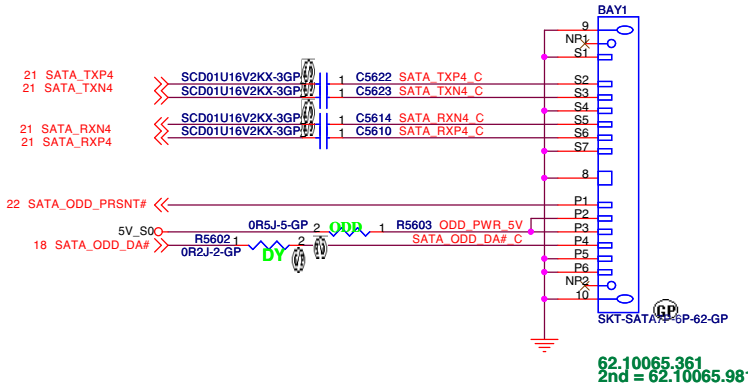
Title		
ITP		
Size: A4	Document Number: BAD40_HC	Rev: 1
Date: Thursday, April 12, 2012	Sheet 55 of 108	

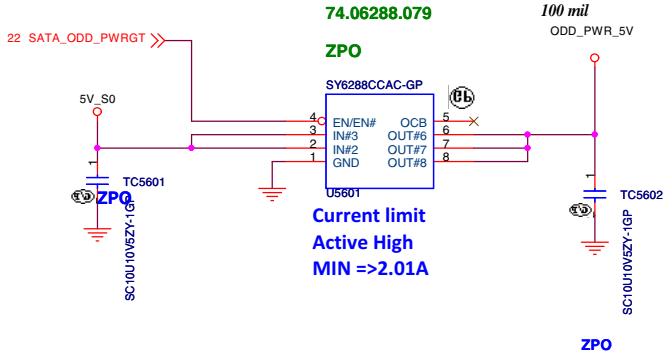
SSID = SATA

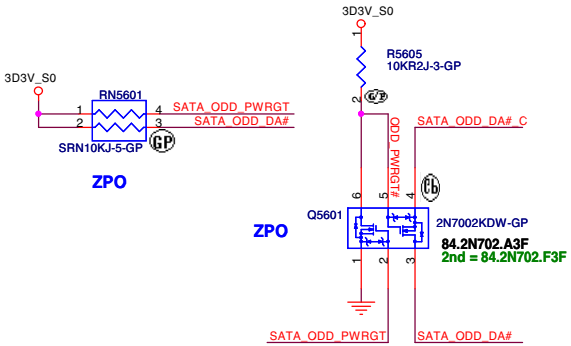
SATA HDD Connector



ODD Connector







<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/ODD

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reserved

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *E-SATA/USB CHARGER*

Size	Document Number	Rev
Custom	BAD40_HC	1

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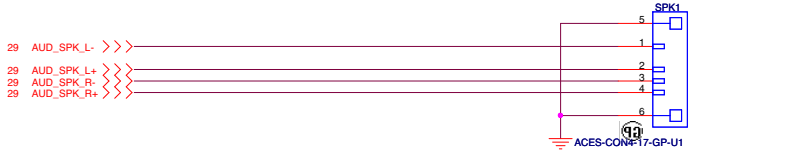
SSID = AUDIO

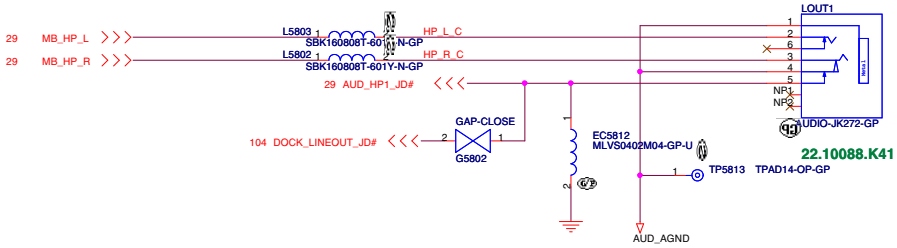
Speaker Connector



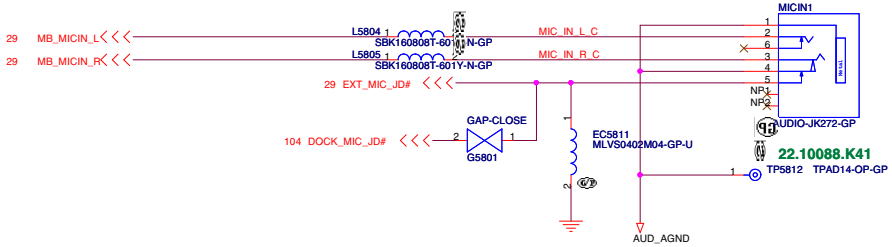
20.F1621.004

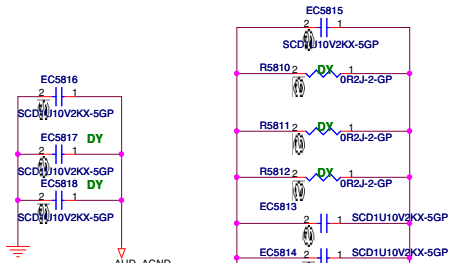
2nd = 20.F1937.004

LINE OUT

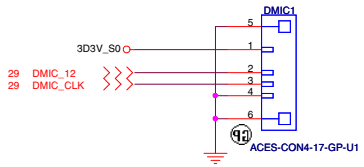


MIC IN





Internal Microphone

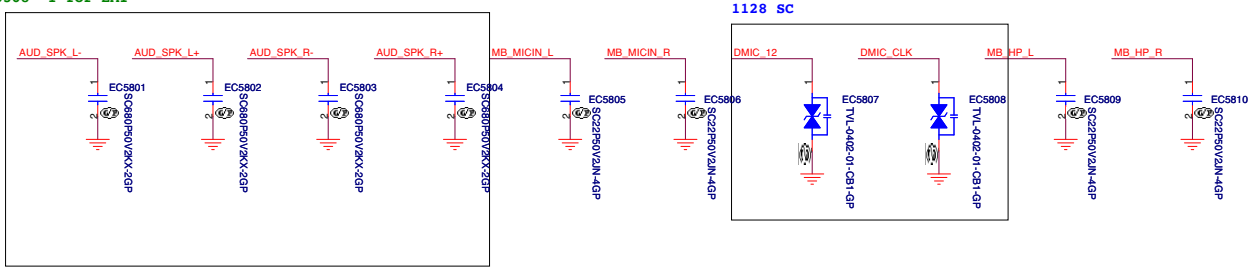


20.F1621.004

2nd = 20.F1937.004

0308 -1 for EMI

1128 SC



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Jack

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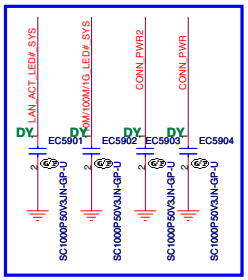
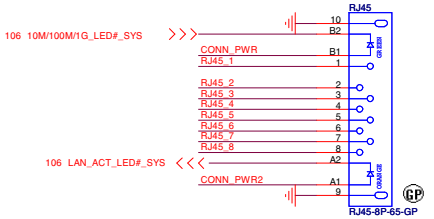
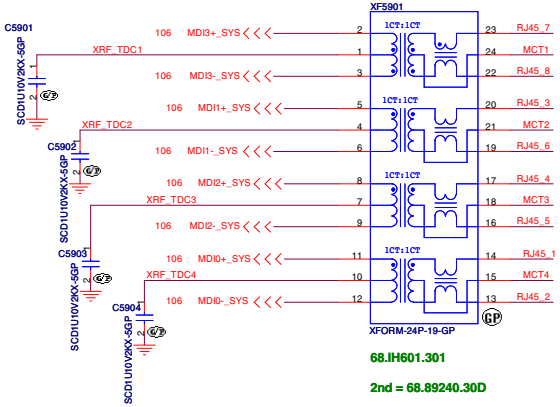
SSID = LOM

SB 0922

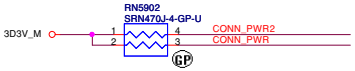


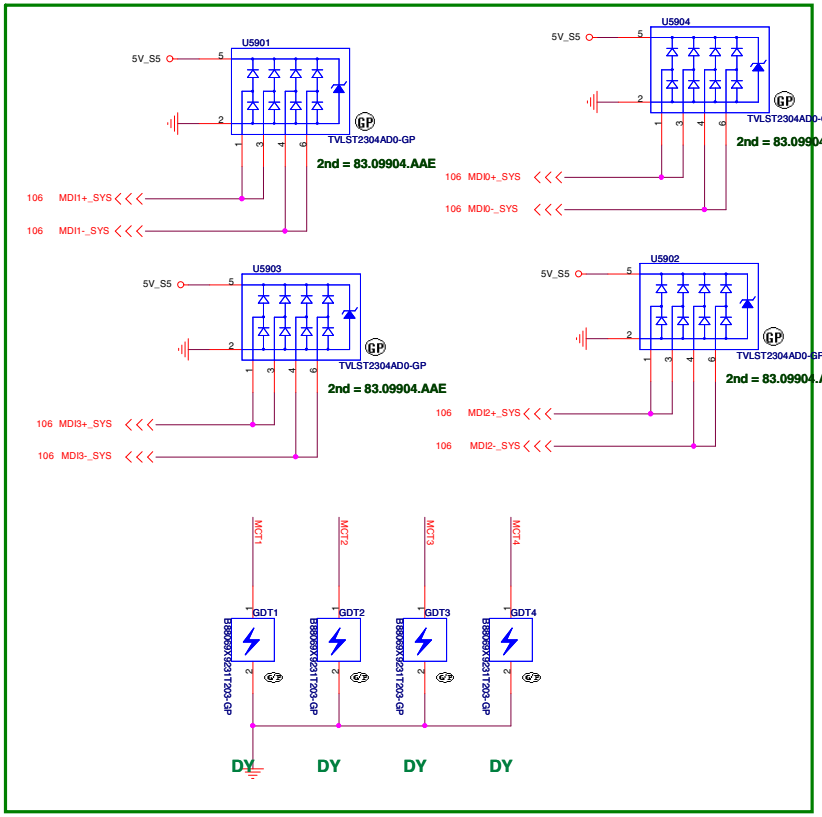


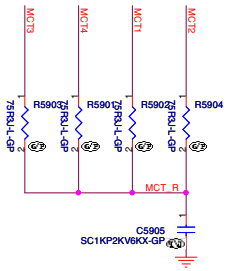
22.10177.J21
2nd = 22.10177.J51



68.IH601.301
2nd = 68.89240.30D







<variant_name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN CONNECTOR**

Size	Document Number	Rev
Custom	BAD40_HC	1

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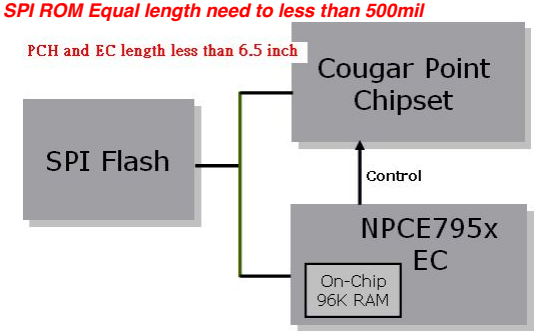
SPI FLASH ROM (8M byte) for PCH

SSID = Flash.ROM

SPI ROM Equal length need to less than 500mil

PCH and EC length less than 6.5 inch



1212 SC

64MB:72.25640.D01,72.25Q64.B01
32MB:72.25Q32.A01, 72.25320.C01

SYSTEM SPI ROM

1216 SC

3D3V_S5

R6011 4K7R2J-2-GP
R6016 4K7R2J-2-GP
R6017 4K7R2J-2-GP

SPI_HOLD_0#

C6002 SCD1U10V2KX-3GP
C6003 SCD1U10V2KX-3GP

21 SPI_CS0#_R
21 SPI_SO_R

R6001 33R2J-2-GP

SPI_SO_0
SPI_WP#_0

U6001
CE# VDD
SO HOLD#
WP# SCK
VSS SI

SST25VF032B-80-4I-S2AF-GP
72.25032.D01

SPI_CLK_R_0
SPI_SI_R_0

R6012 33R2J-2-GP
R6013 33R2J-2-GP

SPI_CLK_R_21
SPI_SI_R_21

R6008 4K7R2J-2-GP
R6009 4K7R2J-2-GP
R6010 4K7R2J-2-GP

DUAL ROM

21 SPI_CS1#_R
21 SPI_SO_R

R6007 33R2J-2-GP

SPI_SO_1
SPI_WP#_1
SPI_HOLD_1#

U6003
SST25VF032B-80-4I-S2AF-GP
72.25032.D01

SPI_CLK_R_1
SPI_SI_R_1

R6014 33R2J-2-GP
R6015 33R2J-2-GP

SPI_CLK_R_C
SPI_SI_R_C

1230 SC

RN6001 4RN0J-6-GP

SPI_CLK_R_21
SPI_SI_R_21

SSID = RBATT

3D3V_AUX_S5

D6001 BAS16-6-GP
DY

83.00016.K11
2nd = 83.00016.M11

+RTC_PWR_R

R6002 1KR2J-1-GP
DY

20.F1639.002
2nd = 20.F1804.002

RTC_AUX_S5

Q6001 CH715FGP-GP-U

RTC_PWR1

R6006 510R2J-1-GP

+RTC_PWR

RTC1
ACES-88092-20-GP

Width=20mils

83.R0304.D81
2nd = 83.R2004.G81

EC BIOS Flash ROM

256KB

for ENE FAE suggest,SPICS# is push-pull pin,
don't need to pull high

3D3V_AUX_S5

R6002 10KR2J-3-GP
R6004 DY 10KR2J-3-GP
R6003 10KR2J-3-GP

SPI_HOLD#

27 SPICS#
27 SPIDI
27 SPI_WP2#

150R2F-1-GP

ER6001
SPI_DI
SPI_WP2#

U6002
CE# VCC
SO HOLD#
WP# SCK
GND SIO

PM25LD020C-SCE-GP
72.25020.E01
2nd = 72.25020.00D

SPI_3D3V_VCC
SPI_HOLD#
SPICLK_1
SPI_DO

150R2F-1-GP

ER6004 0R0603-PAD
C6004 SCD22U16V3KX-2-GP
ER6003
ER6002

SPICLK 27
SPIDO 27

SPICLK_1
SPI_DO
SPIDI

EC6004 SC4D7P50V2CN-1GP DY
EC6005 SC4D7P50V2CN-1GP DY
EC6006 SC4D7P50V2CN-1GP DY

HR PX

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash/RTC

Size	Document Number	Rev
Custom	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 60 of 108

SSID = USB

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB Power SW***

Size	Document Number	Rev
A4	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 61 of 108

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
USB 3.0 Port

Size	Document Number	Rev
A3	**BAD40_HC**	1

Date: Thursday, April 12, 2012 Sheet 62 of 108

SSID = User.Interface

Bluetooth Module conn.

reserved 1216

<Variant Name>

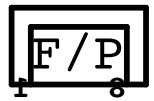
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Bluetooth***

Size	Document Number	Rev
A4	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 63 of 108

Finger printer



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

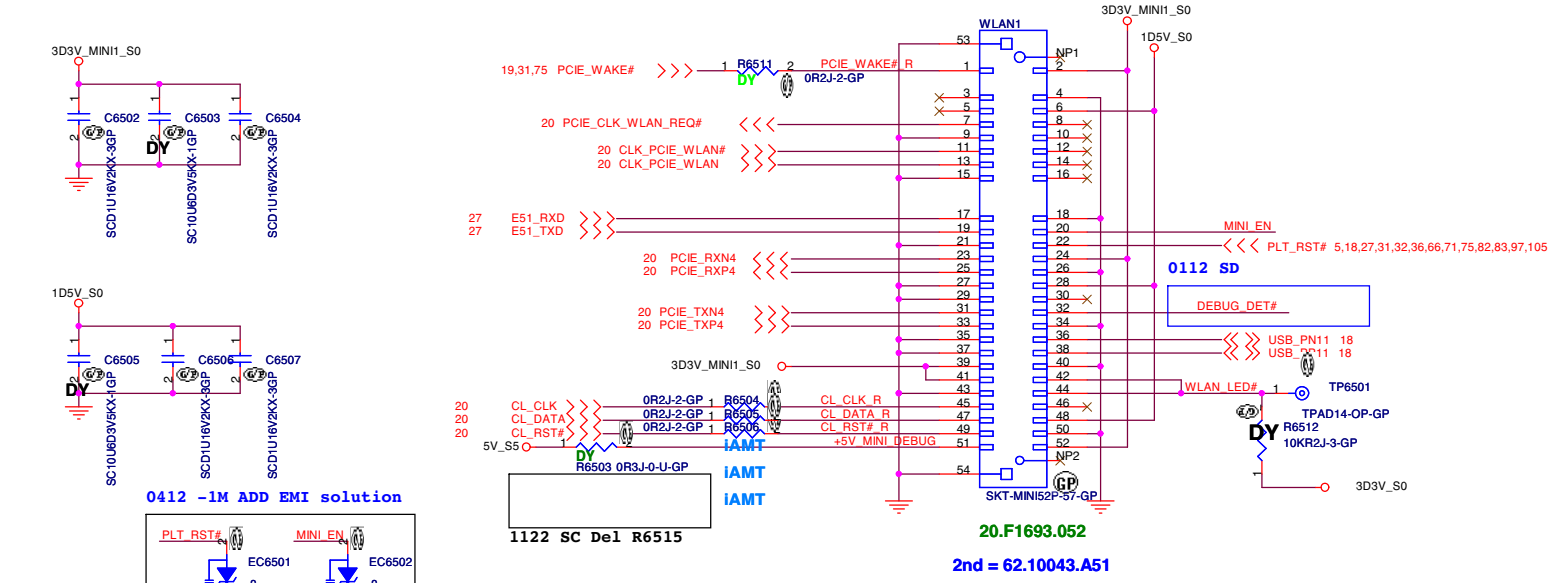
RESERVED

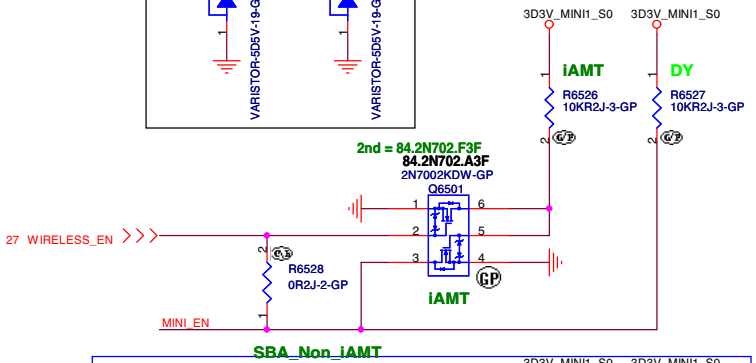
Size	Document Number	Rev
A4	**BAD40_HC**	1

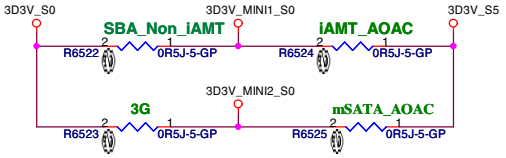
Date: Thursday, April 12, 2012 Sheet 64 of 108

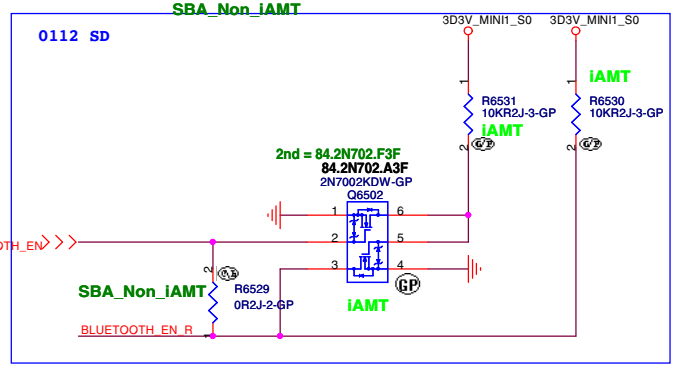
SSID = Wireless

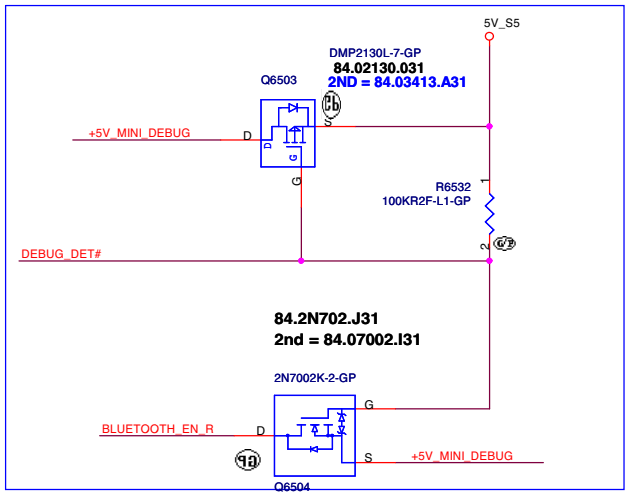
Mini Card Connector(802.11a/b/g/n)











<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***MINICARD(WLAN)/ITP CONN***

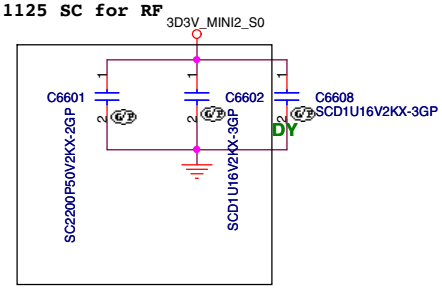
Size	Document Number	Rev
A3	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 65 of 108

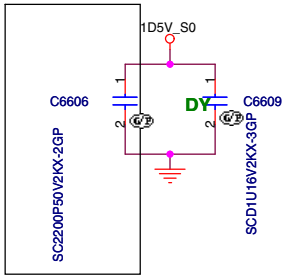
SSID = Wireless

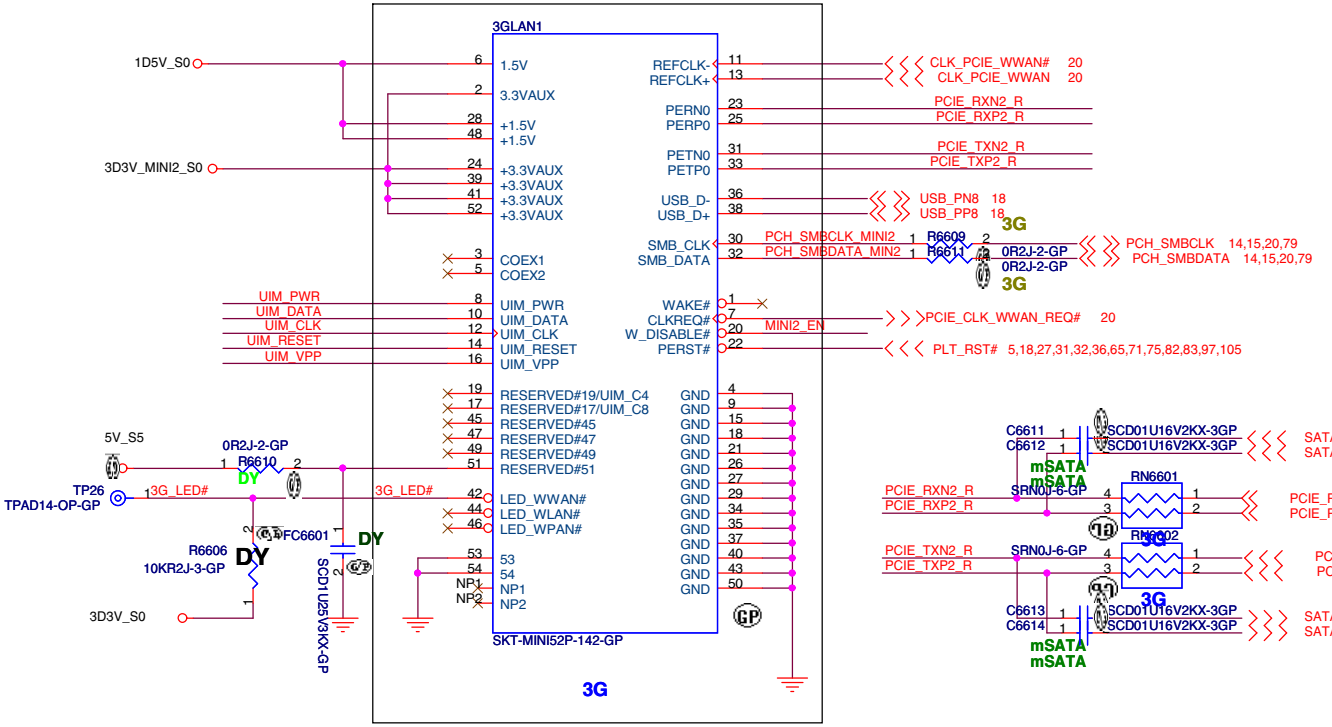
Mini Card Connector(3GLAN)

1125 SC for RF

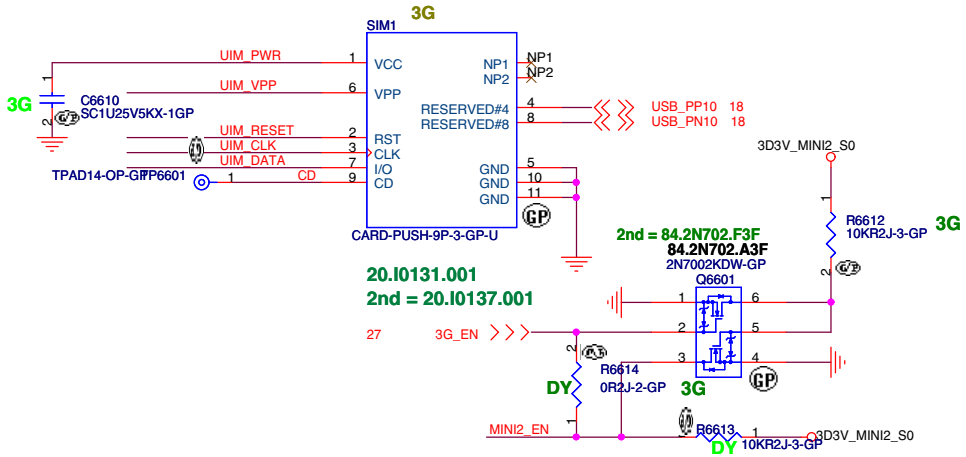


1125 SC for RF





0103 SC change to 62.10043.H61



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	3G	
Size: Custom	Document Number: BAD40_HC	Rev: 1
Date: Thursday, April 12, 2012	Sheet 66 of 108	

reserved

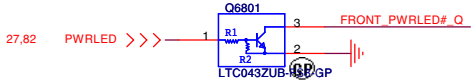
<Variant Name>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***mSATA***		
Size: A4	Document Number: **BAD40_HC**	Rev: 1
Date: Thursday, April 12, 2012	Sheet 67 of 108	

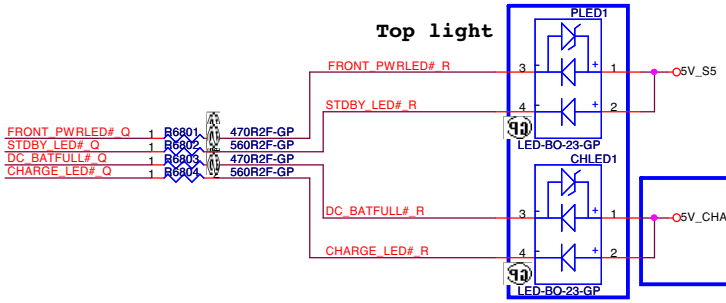
Power button LED



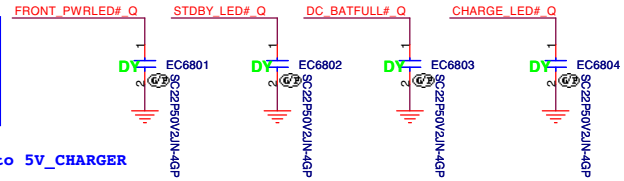
84.00043.011
2nd = 84.05143.011

0130 SD change PN

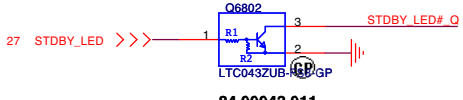
Top light



0130 SD change to 5V_CHARGER

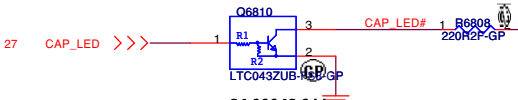


Power STDBY_LED



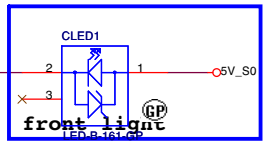
84.00043.011
2nd = 84.05143.011

Caps Lock LED

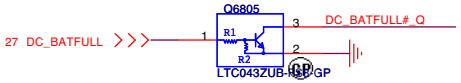


84.00043.011
2nd = 84.05143.011

0202 SD

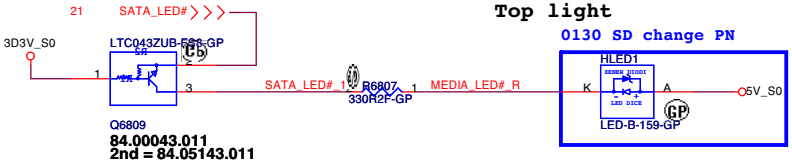


Battery LED2(DC_BATFULL)



84.00043.011
2nd = 84.05143.011

SATA HDD LED

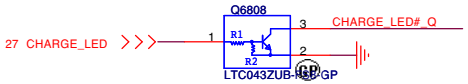


Top light

0130 SD change PN

84.00043.011
2nd = 84.05143.011

Battery LED1(CHARGE)



84.00043.011
2nd = 84.05143.011

0302 -1 Del PWR BTN

1107 SC Del BXD PWR LED

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED Bard/Power Button

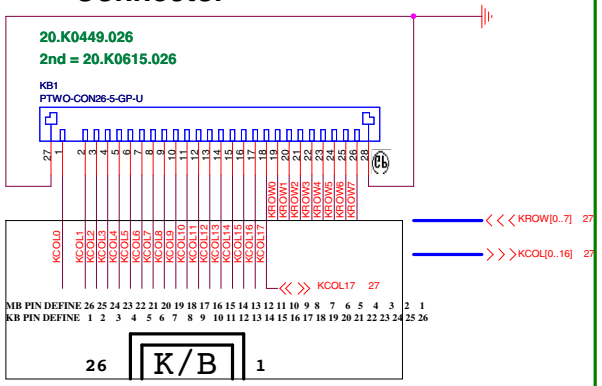
Size: Custom | Document Number: BAD40_HC | Rev: 1

Date: Thursday, April 12, 2012 | Sheet 68 of 108

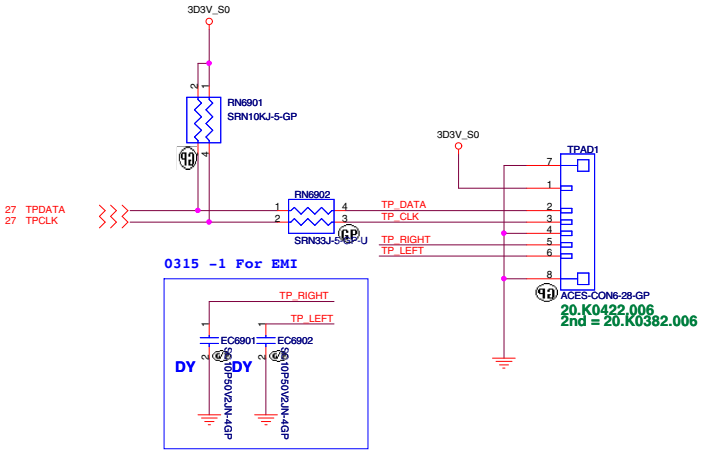
SSID = KBC

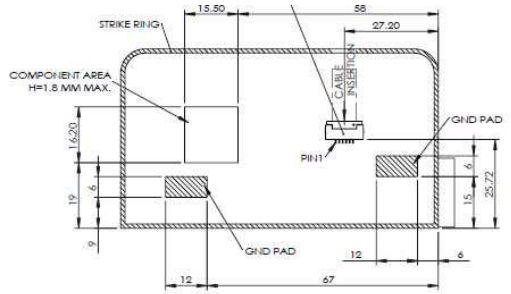
SB 0919 change PN for Layout

Internal KeyBoard Connector



TOUCH PAD 1.0 pitch



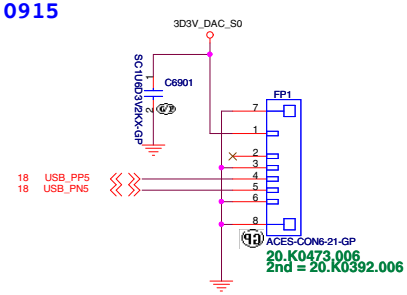


COMPONENT - BOTTOM VIEW

J1 PIN ASSIGNMENT:
PIN1 : TP_L
PIN2 : TP_R
PIN3 : GND
PIN4 : PS2_CLK
PIN5 : PS2_DAT
PIN6 : VDD

Finger Printer 0.5 pitch

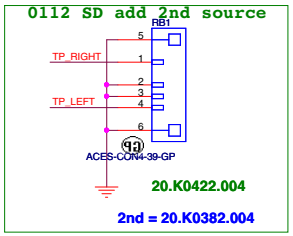
SB 0915



Pin No.	Define
1	ESD ground
2	USB D- Signal
3	USB D+ Signal
4	GND
5	NC
6	3.3V Power pin

Rubber Dome 1.0 pitch

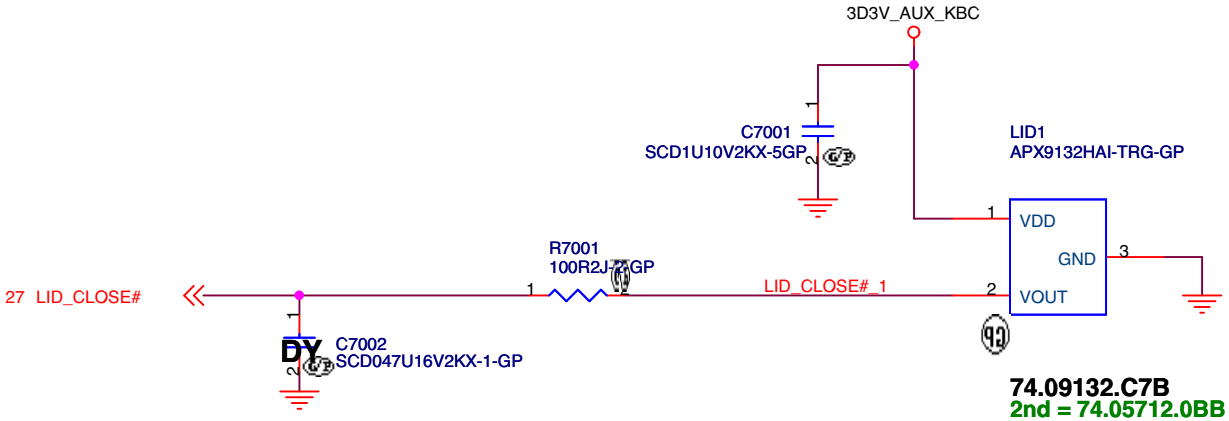
0909 SB
0112 SD add 2nd source



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Key Board/Touch Pad
Size: Custom | Document Number: BAD40_HC | Rev: 1
Date: Thursday, April 12, 2012 | Sheet 69 of 108



<Variant Name>

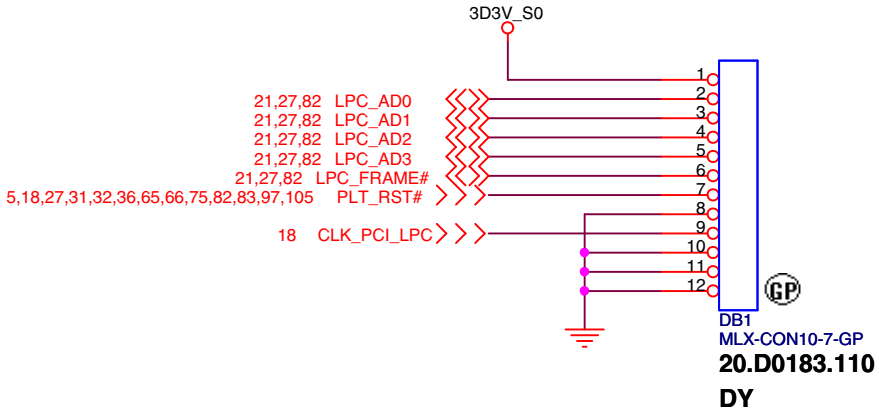
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Hall Sensor***

Size	Document Number	Rev
A4	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 70 of 108

SB modify to test pad



<Variant Name>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Dubug connector***

Size	Document Number	Rev
A4	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 71 of 108

(Blanking)

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	BAD40_HC	1

(Blanking)

<Variant Name>

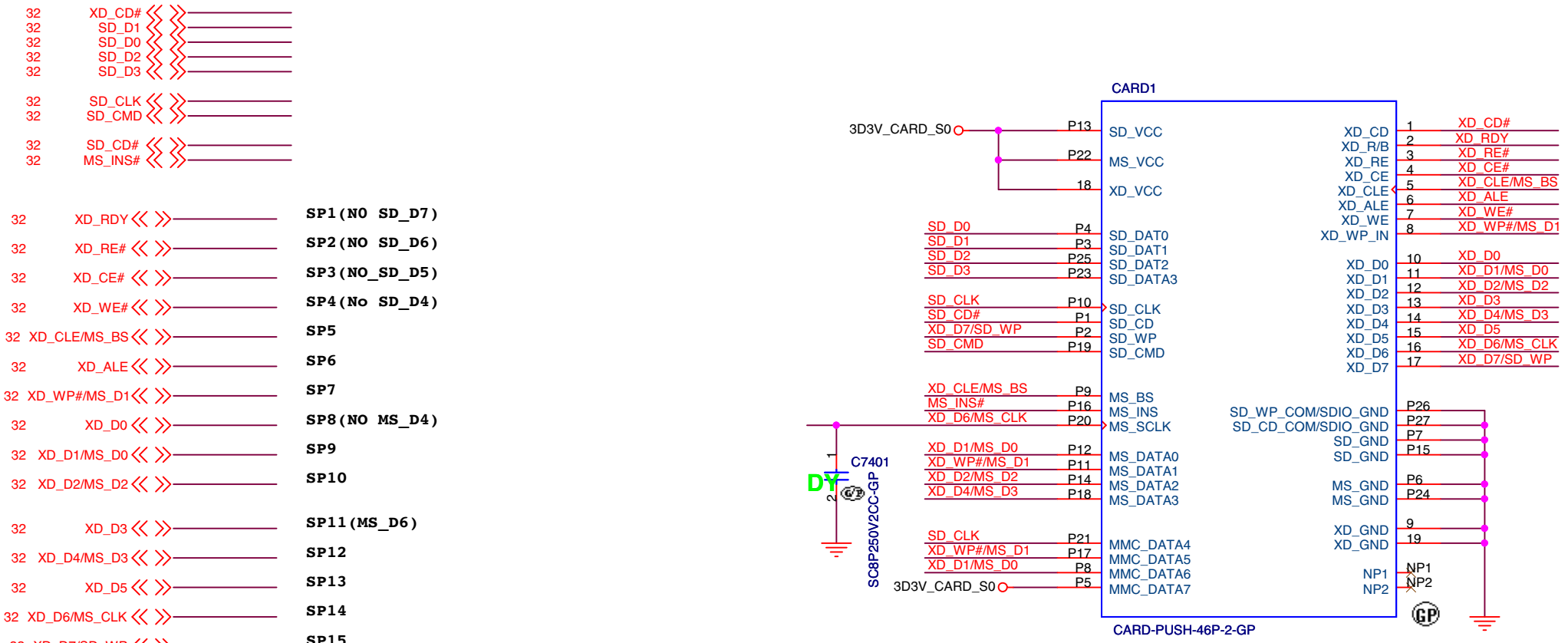
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	BAD40_HC	1

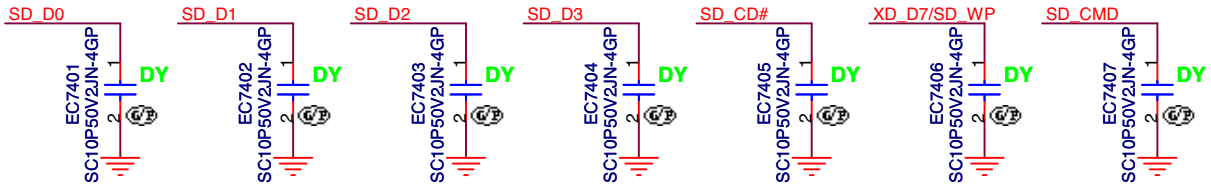
SD/XD/MS Card Reader

SSID = SDIO



20.I0135.001

2nd = 20.I0129.001



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CARD Reader CONN**

Size	Document Number	Rev
A4	BAD40_HC	1

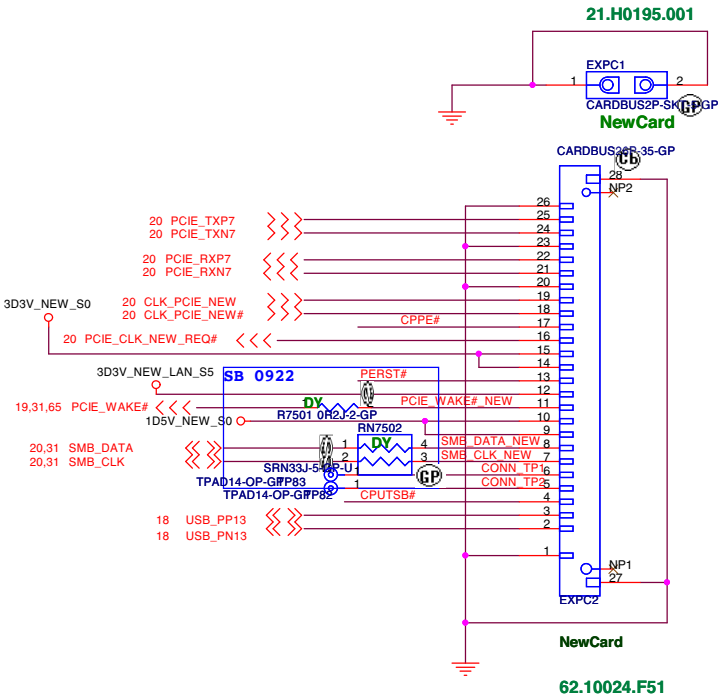
Date: Thursday, April 12, 2012 Sheet 74 of 108

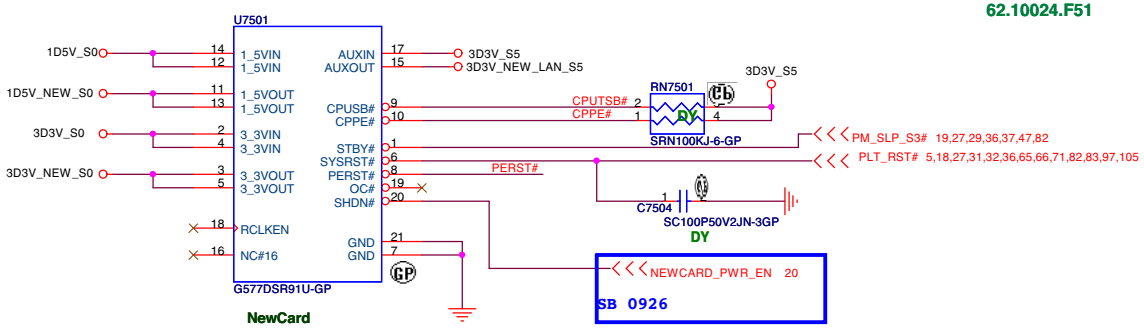
SSID = ExpressCard

DIP階 For Expresscard socket

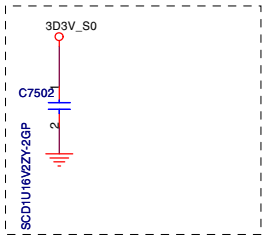
21.H0195.001

+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA

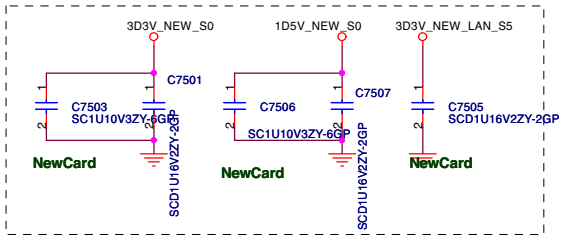




Place them Near to Chip



Place them Near to Connector



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***New Card***

Size	Document Number	Rev
A3	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 75 of 108

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A4	**BAD40_HC**	1

Date: Thursday, April 12, 2012 Sheet 76 of 108

<Variant Name>

緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A3	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 77 of 108

(Blanking)

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

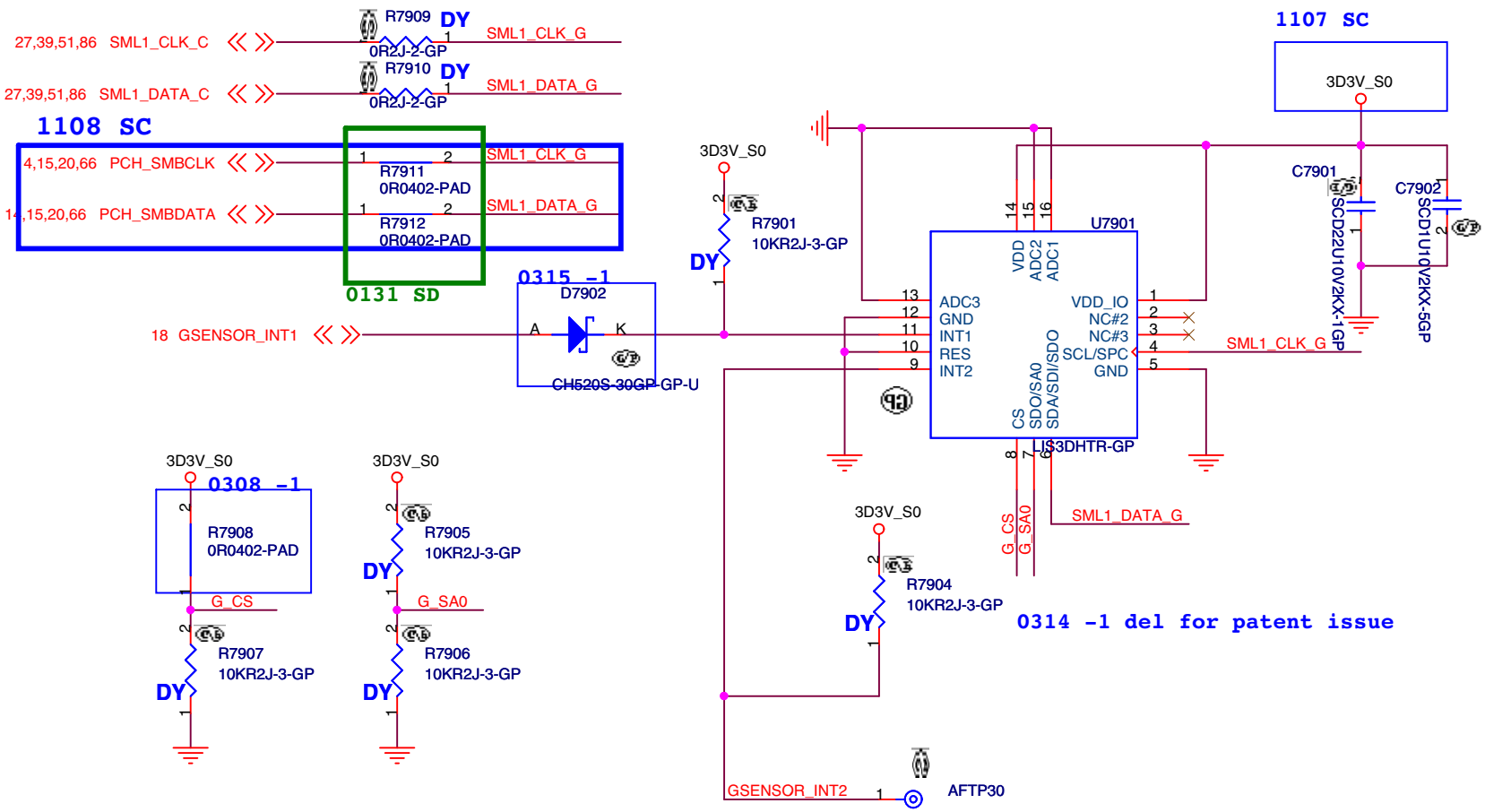
Size	Document Number	Rev
A4	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 78 of 108

SSID = User.Interface

Free Fall Sensor

Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



SDO="H"; address="3Ah"
*SDO="L"; address="38h"

*CS="H"; mode="I2C"
CS="L"; mode="SPI"

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Free Fall Sensor*

Size	Document Number	Rev
A4	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 79 of 108

(Blanking)

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A4	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 80 of 108

<Variant Name>

緯創資通

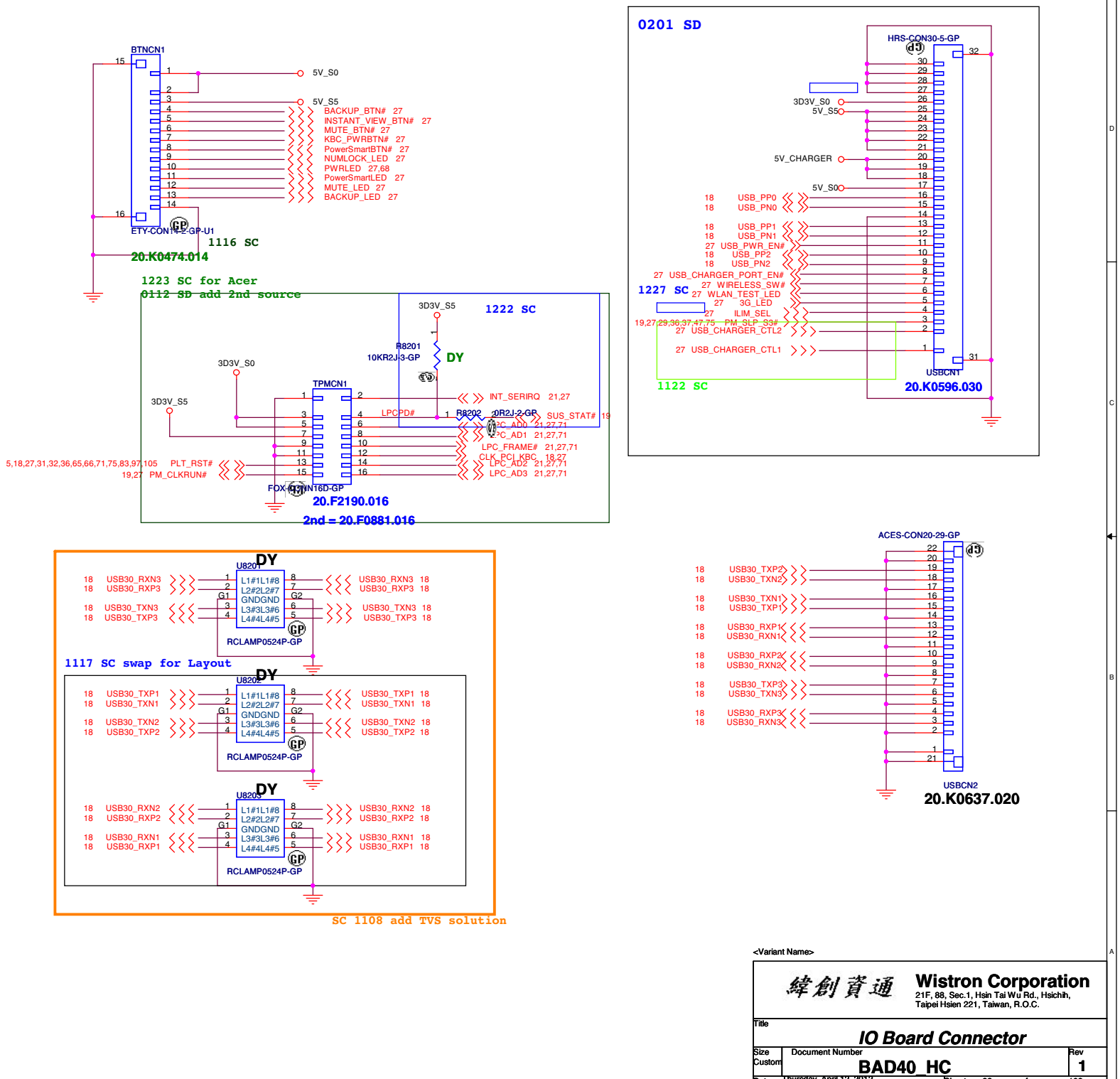
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A4	BAD40_HC	1

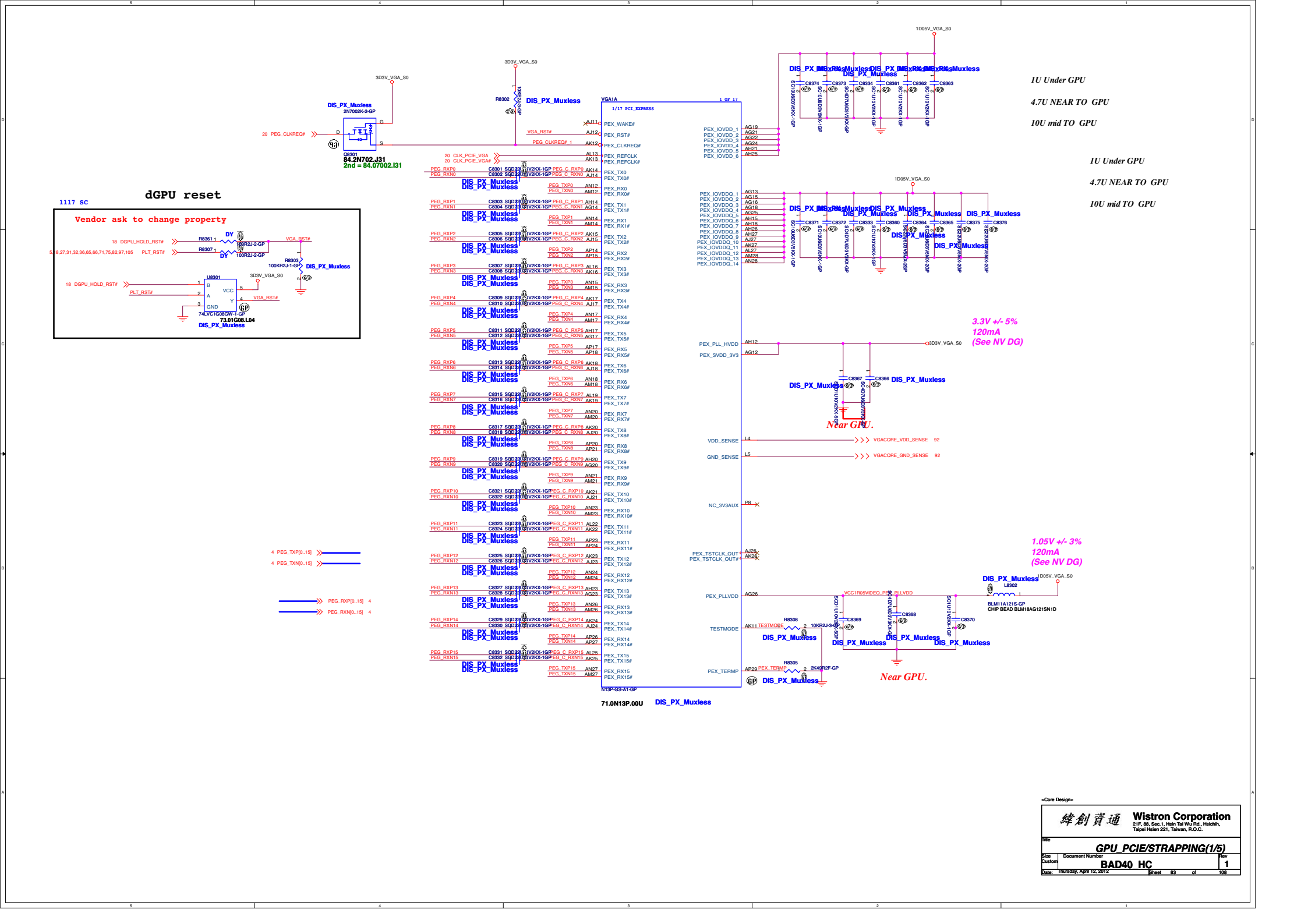
Date: Thursday, April 12, 2012 Sheet 81 of 108



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***IO Board Connector***	
Size: Custom	Document Number: **BAD40_HC**	Rev: **1**
Date: Thursday, April 12, 2012	Sheet 82 of 108	



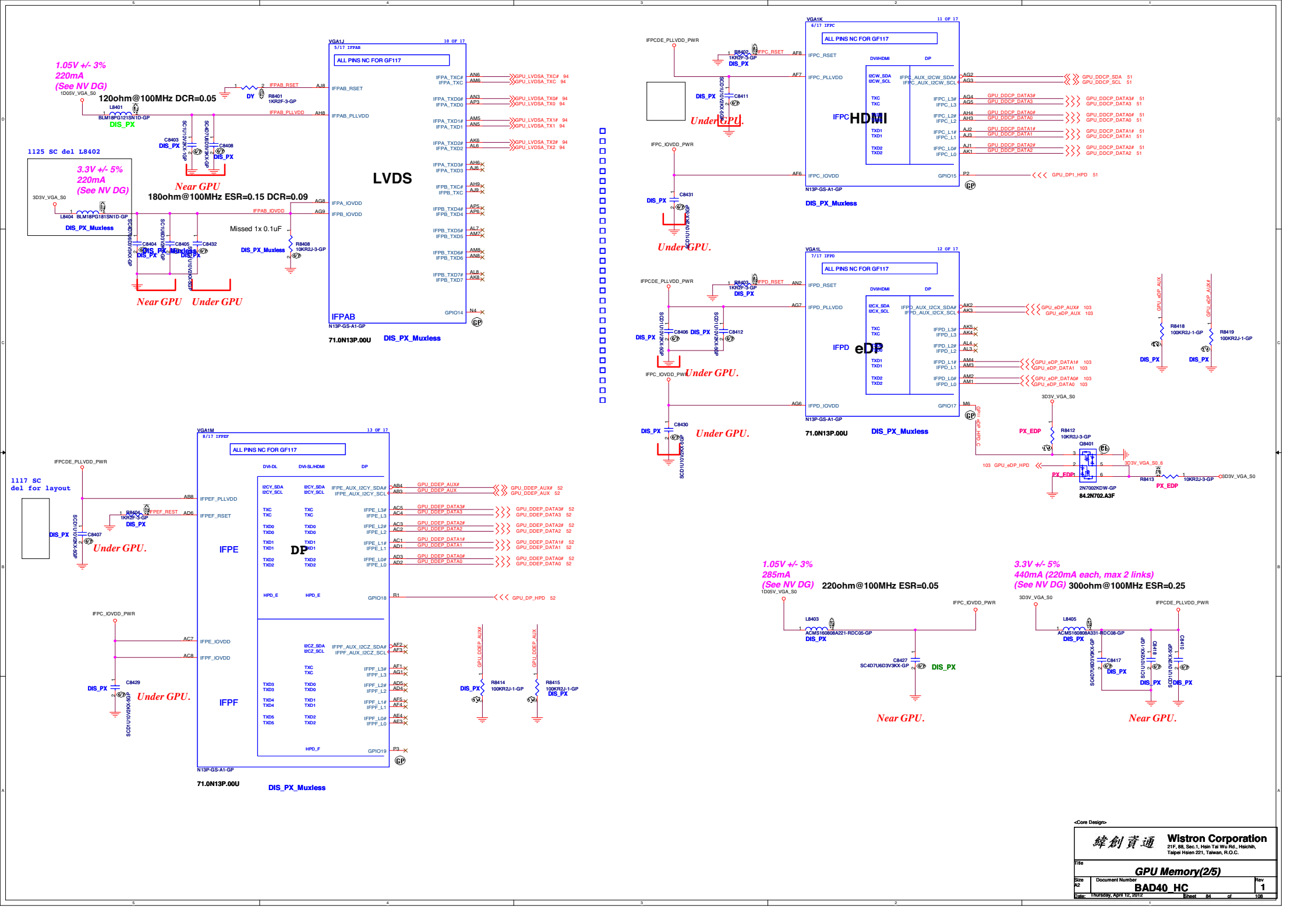
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_PCIE/STRAPPING(1/5)

Size: Custom | Document Number: BAD40_HC | Rev: 1

Date: Thursday, April 12, 2012 | Sheet 83 of 108


1.05V +/- 3%
220mA
(See NV DG)
1D05V_VGA_S0
120ohm@100MHz DCR=0.05
L8401
BLM18PG121SN1D-GP
DIS_PX
R8401
1KR2F-3-GP
IFPAB_RSET
IFPAB_PLLVDD
C8403
C8408
1125 SC del L8402
3.3V +/- 5%
220mA
(See NV DG)
3D3V_VGA_S0
L8404
BLM18PG181SN1D-GP
DIS_PX_Muxless
180ohm@100MHz ESR=0.15 DCR=0.09
IFPAB_IOVDD
Missed 1x 0.1uF
C8404
C8405
C8432
R8408
10KR2J-3-GP
Near GPU
Under GPU
VGA1J
5/17 IFPAB
ALL PINS NC FOR GF117
LVDS
IFPAB
N13P-GS-A1-GP
71.0N13P.00U
DIS_PX_Muxless
IFPA_TXC#
IFPA_TXC
IFPA_TXD0#
IFPA_TXD0
IFPA_TXD1#
IFPA_TXD1
IFPA_TXD2#
IFPA_TXD2
IFPA_TXD3#
IFPA_TXD3
IFPB_TXC#
IFPB_TXC
IFPB_TXD4#
IFPB_TXD4
IFPB_TXD5#
IFPB_TXD5
IFPB_TXD6#
IFPB_TXD6
IFPB_TXD7#
IFPB_TXD7
GPIO14
GPU_LVDSA_TXC# 94
GPU_LVDSA_TXC 94
GPU_LVDSA_TX0# 94
GPU_LVDSA_TX0 94
GPU_LVDSA_TX1# 94
GPU_LVDSA_TX1 94
GPU_LVDSA_TX2# 94
GPU_LVDSA_TX2 94
IFPCDE_PLLVDD_PWR
R8402
1KR2F-3-GP
IFPC_RSET
IFPC_PLLVDD
C8411
Under GPU.
IFPC_IOVDD_PWR
C8431
Under GPU.
VGA1K
6/17 IFPC
ALL PINS NC FOR GF117
IFPC HDMI
DVI/HDMI
DP
IFPC_IOVDD
GPIO15
N13P-GS-A1-GP
DIS_PX_Muxless
GPU_DDCP_SDA 51
GPU_DDCP_SCL 51
GPU_DDCP_DATA3# 51
GPU_DDCP_DATA3 51
GPU_DDCP_DATA0# 51
GPU_DDCP_DATA0 51
GPU_DDCP_DATA1# 51
GPU_DDCP_DATA1 51
GPU_DDCP_DATA2# 51
GPU_DDCP_DATA2 51
GPU_DP1_HPD 51
IFPCDE_PLLVDD_PWR
R8403
1KR2F-3-GP
IFPD_RSET
IFPD_PLLVDD
C8406
C8412
Under GPU.
IFPC_IOVDD_PWR
C8430
Under GPU.
VGA1L
7/17 IFPD
ALL PINS NC FOR GF117
IFPD eDP
DVI/HDMI
DP
IFPD_IOVDD
GPIO17
N13P-GS-A1-GP
71.0N13P.00U
DIS_PX_Muxless
GPU_eDP_AUX# 103
GPU_eDP_AUX 103
GPU_eDP_DATA1# 103
GPU_eDP_DATA1 103
GPU_eDP_DATA0# 103
GPU_eDP_DATA0 103
GPU_eDP_HPD 103
R8418
100KR2J-1-GP
R8419
100KR2J-1-GP
3D3V_VGA_S0
PX_EDP
R8412
10KR2J-3-GP
Q8401
2N7002KDW-GP
84.2N702.A3F
R8413
10KR2J-3-GP
1117 SC
del for layout
IFPCDE_PLLVDD_PWR
R8404
1KR2F-3-GP
IFPEF_REST
IFPEF_PLLVDD
IFPEF_RSET
C8407
Under GPU.
IFPC_IOVDD_PWR
C8429
Under GPU.
VGA1M
8/17 IFPEF
ALL PINS NC FOR GF117
IFPE
IFPF
DP
DVI-DL
DVI-SL/HDMI
DP
IFPF_PLLVDD
IFPF_RSET
IFPF_IOVDD
IFPE_AUX_I2CY_SDA#
IFPE_AUX_I2CY_SCL
IFPE_L3#
IFPE_L3
IFPE_L2#
IFPE_L2
IFPE_L1#
IFPE_L1
IFPE_L0#
IFPE_L0
IFPF_AUX_I2CZ_SDA#
IFPF_AUX_I2CZ_SCL
IFPF_L3#
IFPF_L3
IFPF_L2#
IFPF_L2
IFPF_L1#
IFPF_L1
IFPF_L0#
IFPF_L0
HPD_E
HPD_F
GPIO18
GPIO19
N13P-GS-A1-GP
71.0N13P.00U
DIS_PX_Muxless
GPU_DDEP_AUX#
GPU_DDEP_AUX
GPU_DDEP_DATA3#
GPU_DDEP_DATA3
GPU_DDEP_DATA2#
GPU_DDEP_DATA2
GPU_DDEP_DATA1#
GPU_DDEP_DATA1
GPU_DDEP_DATA0#
GPU_DDEP_DATA0
GPU_DP_HPD 52
R8414
100KR2J-1-GP
R8415
100KR2J-1-GP
1.05V +/- 3%
285mA
(See NV DG)
220ohm@100MHz ESR=0.05
1D05V_VGA_S0
L8403
ACMS1608080A221-RDC05-GP
C8427
Near GPU.
3.3V +/- 5%
440mA (220mA each, max 2 links)
(See NV DG)
300ohm@100MHz ESR=0.25
3D3V_VGA_S0
L8405
ACMS1608080A331-RDC08-GP
C8417
C8410
Near GPU.
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
GPU Memory(2/5)
Size
A2
Document Number
BAD40_HC
Rev
1
Date: Thursday, April 12, 2012
Sheet 84 of 108

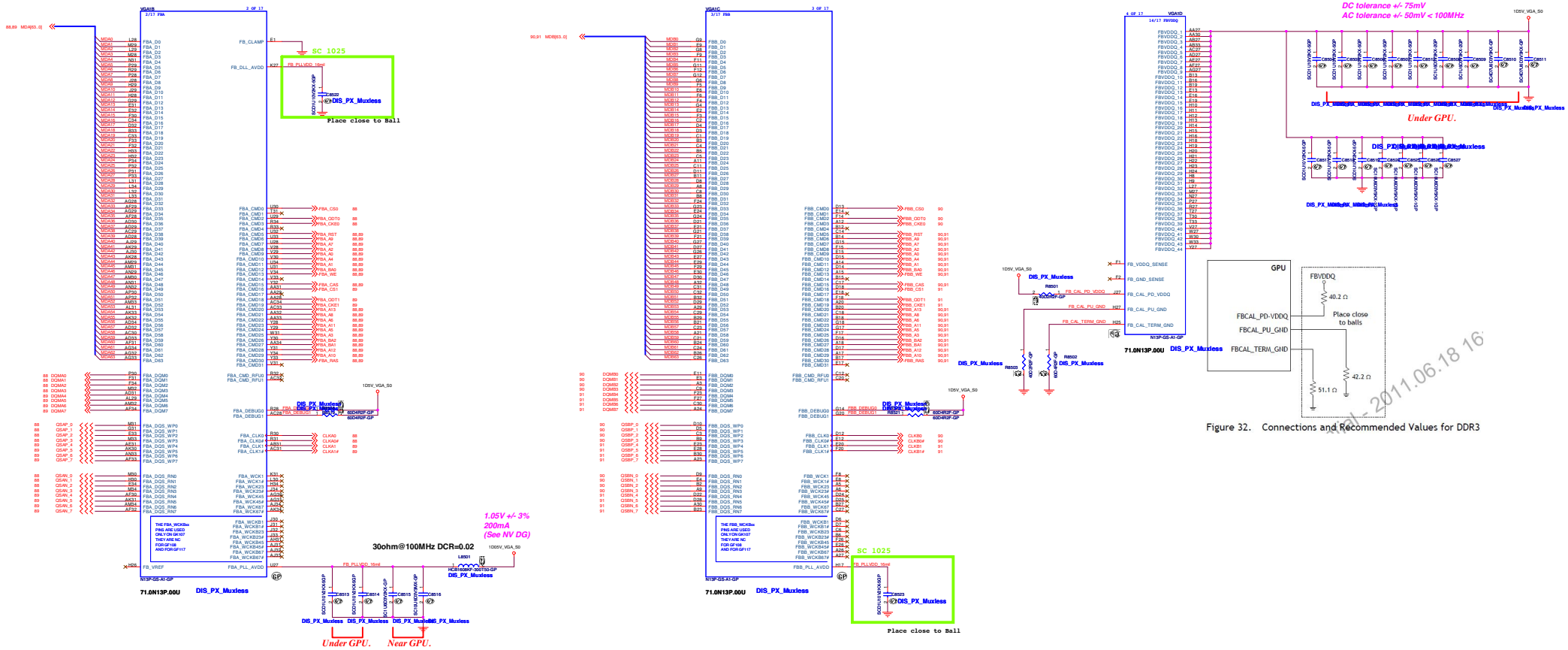
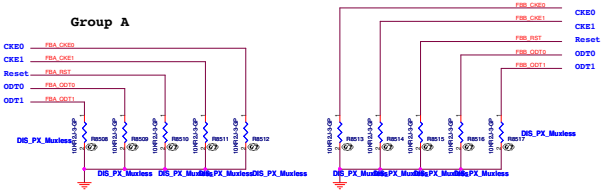


Figure 32. Connections and Recommended Values for DDR3

FBCLK Termination place on VRAM side



FBCLK Termination place on VRAM side

<Variant Name>			
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: GPU_DP/LVDS/CRT/GPIO(3/5)			
Size: Custom	Document Number: BAD40_HC		Rev: 1
Date: Thursday, April 14, 2011	Sheet 85 of 108		

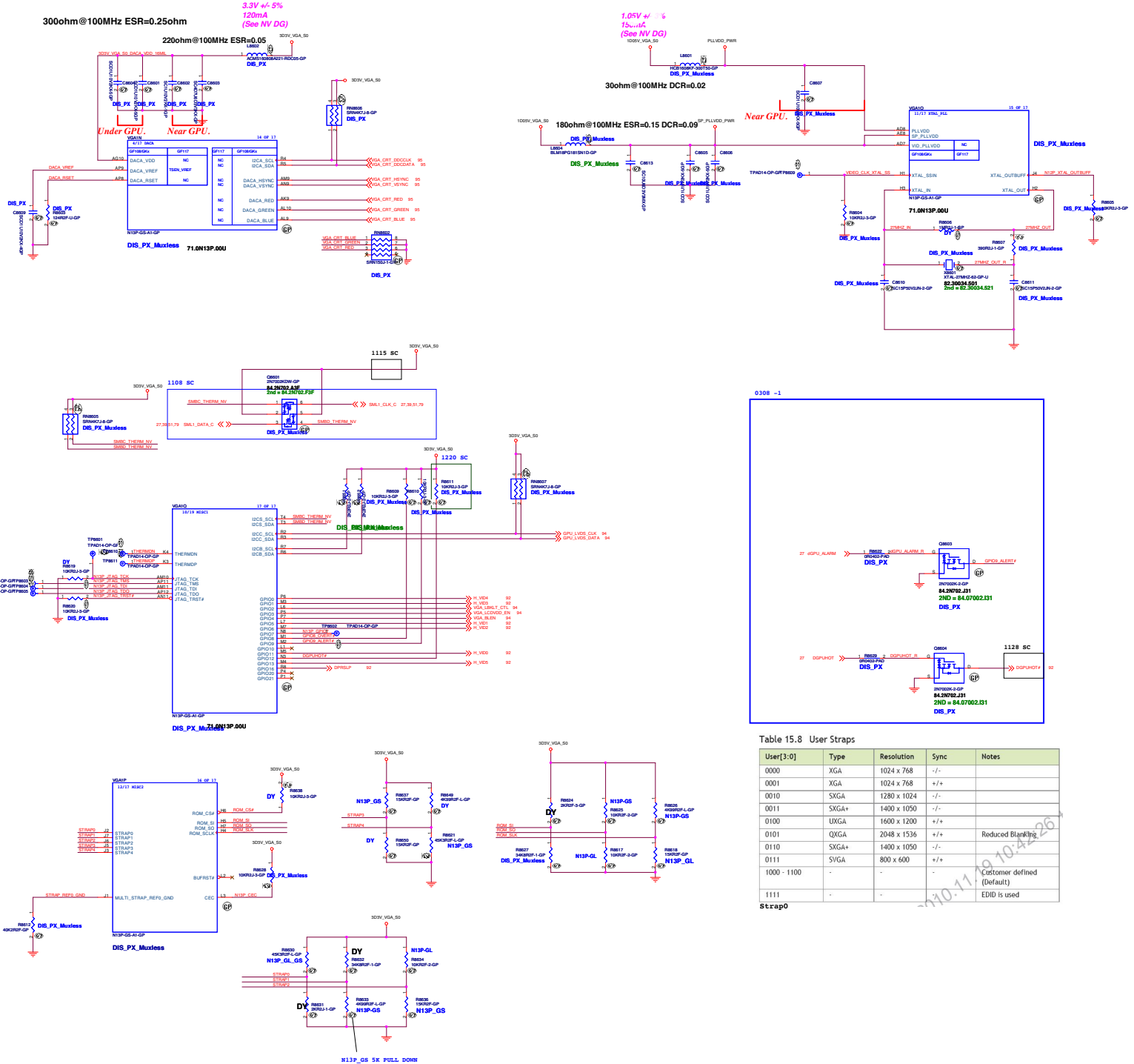


Table 15.3 Resistance Mapping to Hex Values

Resistor Values	Pull-up to VDD	Pull-down to GND
5k	1000	0000
10k	1001	0001
15k	1010	0010
20k	1011	0011
25k	1100	0100
30k	1101	0101
35k	1110	0110
45k	1111	0111

25Kohm	5Kohm	10Kohm	30Kohm
64.24925.6DL	64.49915.6DL	64.10025.6DL	64.30025.6DL

NVIDIA TABLE

	Hynix 2G 0110 128M*16*8 900MHZ	Hynix 1G 0010 64M*16*8 900MHZ	Samsung 1G 0011 64M*16*8 900MHZ	Samsung 2G 0111 128M*16*8 900MHZ
ROM_SI	34.8Kohm 64.34825.6DL	15Kohm 64.15025.6DL	20Kohm 64.20025.6DL	45Kohm 64.45325.6DL

Table 111. Display Link to SORx_EXPOSED Bit Mapping

Displays		DVI/HDMI/DP	LVDS	eDP	Not in Use
Dual Link Mode	IFPA/B		SOR0_EXPOSED = 0		SOR0_EXPOSED = 0
	IFPC	SOR1_EXPOSED = 1			SOR1_EXPOSED = 0
	IFPD	SOR2_EXPOSED = 1		SOR2_EXPOSED = 0	SOR2_EXPOSED = 0
	IFPE/F	SOR3_EXPOSED = 1			SOR3_EXPOSED = 0
Split Mode	IFPA/B				
	IFPC	SOR1_EXPOSED = 1			SOR1_EXPOSED = 0
	IFPD	SOR2_EXPOSED = 1		SOR2_EXPOSED = 0	SOR2_EXPOSED = 0
	IFPE	SOR3_EXPOSED = 1			SOR3_EXPOSED = 0
	IFPF	SOR0_EXPOSED = 1			SOR0_EXPOSED = 0

Strap3

	DEVID	ROM-SCLK		strap2	
N13P-GL-A1	0x0DE9	0010	PD 15K	1001	PU 10K
N13P-GS-ES-A1	0x0FD8	1000	PU 4.99K	1011	PU 20K
N13P-GS-A1	0x0FD2	1000	PU 4.99K	0010	PD 15K

For N13P-GS-A1 **0x0FD2**

Strap Pin Nmae	Logical strapping name bit#3	Logical strapping name bit#2	Logical strapping name bit#1	Logical strapping name bit#0	
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TER_MI	
	1	0	0	0	5K ohm pull-up
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[2]	RAMCFG[0]	
Hynix 2G	0	1	1	0	35K ohm pull-down
ROM_SO	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE	
	1	0	0	1	10K ohm pull-up
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	
	1	1	1	1	45K ohm pull-up
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	
	0	0	0	0	5K ohm pull-down
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	
	0	0	1	0	15K ohm pull-down
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	
	1	0	1	0	15K ohm pull-up
STRAP4	RESERVED	PCI_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V	
	0	1	1	1	45K ohm pull-down

Table 15.8 User Straps

User[3:0]	Type	Resolution	Sync	Notes
0000	XGA	1024 x 768	-/-	
0001	XGA	1024 x 768	+/+	
0010	SXGA	1280 x 1024	-/-	
0011	SXGA+	1400 x 1050	-/-	
0100	UXGA	1600 x 1200	+/+	
0101	QXGA	2048 x 1536	+/+	Reduced Blanking
0110	SXGA+	1400 x 1050	-/-	
0111	SVGA	800 x 600	+/+	
1000 - 1100	-	-	-	Customer defined (Default)
1111	-	-	-	EDID is used

Strap0

EDP 50A
(TDP 37W)

VGA_CORE

Under GPU

DIS_PX_Muxless

C8704 C8703 C8702 C8701

SC4D7U6D3V9KX-GP

Under GPU

DIS_PX_Muxless

C8712 C8711 C8708 C8707 C8706 C8705

SC4D7U6D3V9KX-GP

CLOSE TO GPU

DIS_PX_Muxless

C8720 C8719 C8718 C8717

SC1U10V2KX-4GP

NEAR TO GPU

DIS_PX_Muxless

C8731 C8730 C8729 C8728 C8727

SC10U6D3V3MX-GP

DIS_PX_Muxless

C8726 C8725 C8724 C8723 C8722

SC10U6D3V3MX-GP

VGA1F 6 OF 17

13/17 NVVDD

VDD_1 VDD_2 VDD_3 VDD_4 VDD_5 VDD_6 VDD_7 VDD_8 VDD_9 VDD_10 VDD_11 VDD_12 VDD_13 VDD_14 VDD_15 VDD_16 VDD_17 VDD_18 VDD_19 VDD_20 VDD_21 VDD_22 VDD_23 VDD_24 VDD_25 VDD_26 VDD_27 VDD_28 VDD_29 VDD_30 VDD_31 VDD_32 VDD_33 VDD_34 VDD_35 VDD_36 VDD_37 VDD_38 VDD_39 VDD_40 VDD_41 VDD_42 VDD_43 VDD_44 VDD_45 VDD_46 VDD_47 VDD_48 VDD_49 VDD_50 VDD_51 VDD_52 VDD_53 VDD_54 VDD_55 VDD_56 VDD_57 VDD_58 VDD_59 VDD_60 VDD_61 VDD_62 VDD_63 VDD_64 VDD_65 VDD_66 VDD_67 VDD_68 VDD_69 VDD_70 VDD_71 VDD_72

N13P-GS-A1-GP

71.0N13P.00U

DIS_PX_Muxless

VGA1I 9 OF 17

15/17 GND_1/2

GND_1 GND_5 GND_6 GND_7 GND_8 GND_9 GND_10 GND_11 GND_12 GND_13 GND_14 GND_2 GND_15 GND_16 GND_17 GND_18 GND_19 GND_20 GND_21 GND_22 GND_23 GND_24 GND_3 GND_25 GND_26 GND_27 GND_28 GND_29 GND_30 GND_31 GND_32 GND_33 GND_34 GND_4 GND_35 GND_36 GND_37 GND_38 GND_39 GND_40 GND_41 GND_42 GND_43 GND_44 GND_45 GND_46 GND_47 GND_48 GND_49 GND_50 GND_51 GND_52 GND_53 GND_54 GND_55 GND_56 GND_57 GND_58 GND_59 GND_60 GND_61 GND_62 GND_63 GND_64 GND_65 GND_66 GND_67 GND_68 GND_69 GND_70

GND_71 GND_72 GND_73 GND_74 GND_75 GND_76 GND_77 GND_78 GND_79 GND_80 GND_81 GND_82 GND_83 GND_84 GND_85 GND_86 GND_87 GND_88 GND_89 GND_90 GND_91 GND_92 GND_93 GND_94 GND_95 GND_96 GND_97 GND_98 GND_99 GND_100 GND_101 GND_102 GND_103 GND_104 GND_105 GND_106 GND_107 GND_108 GND_109 GND_110 GND_111 GND_112 GND_113 GND_114 GND_115 GND_116 GND_117 GND_118 GND_119 GND_120 GND_121 GND_122 GND_123 GND_124 GND_125 GND_126 GND_127 GND_128 GND_129 GND_130 GND_131 GND_132 GND_133 GND_134 GND_135 GND_136 GND_137 GND_138 GND_139 GND_140

N13P-GS-A1-GP

71.0N13P.00U

DIS_PX_Muxless

VGA1H 8 OF 17

16/17 GND_2/2

GND_141 GND_142 GND_143 GND_144 GND_145 GND_146 GND_147 GND_148 GND_149 GND_150 GND_151 GND_152 GND_153 GND_154 GND_155 GND_156 GND_157 GND_158 GND_159 GND_160 GND_161 GND_162 GND_163 GND_164 GND_165 GND_166 GND_167 GND_168 GND_169

GND_170 GND_171 GND_172 GND_173 GND_174 GND_175 GND_176 GND_177 GND_178 GND_179 GND_180 GND_181 GND_182 GND_183 GND_184 GND_185 GND_186 GND_187 GND_188 GND_189 GND_190 GND_191 GND_192 GND_193 GND_194 GND_195 GND_196 GND_197 GND_198

GND_F GND_H

GND_OPT_1 GND_OPT_2

Optional GND GNDs (2)
NC for 4-Layer cards

N13P-GS-A1-GP

71.0N13P.00U

DIS_PX_Muxless

VGA1G 7 OF 17

17/17 NC/VDD33

NC#AC6 NC#AJ28 NC#AJ4 NC#AJ5 NC#AL11 NC#C15 NC#D19 NC#D20 NC#D23 NC#D26 NC#H31 NC#T8 NC#V32

VDD33_1 VDD33_2 VDD33_3 VDD33_4

N13P-GS-A1-GP

71.0N13P.00U

DIS_PX_Muxless

3D3V_VGA_S0

C8710 C8735 C8739 C8740

SC1U6D3V2KX-GP

SC4D7U6D3V9KX-GP

DIS_PX_Muxless

0.1U Under GPU

4.7U NEAR TO GPU

1U NEAR TO GPU

VGA1E 5 OF 17

9/17 XVDD

CONFIGURABLE POWER CHANNELS

XVDD_1 XVDD_2 XVDD_3 XVDD_4 XVDD_5 XVDD_6 XVDD_7 XVDD_8 XVDD_9 XVDD_10 XVDD_11 XVDD_12 XVDD_13 XVDD_14 XVDD_15 XVDD_16 XVDD_17 XVDD_18 XVDD_19 XVDD_20 XVDD_21 XVDD_22 XVDD_23 XVDD_24 XVDD_25 XVDD_26 XVDD_27 XVDD_28 XVDD_29 XVDD_30 XVDD_31 XVDD_32 XVDD_33 XVDD_34 XVDD_35 XVDD_36 XVDD_37 XVDD_38

N13P-GS-A1-GP

DIS_PX_Muxless

71.0N13P.00U

<Core Design>

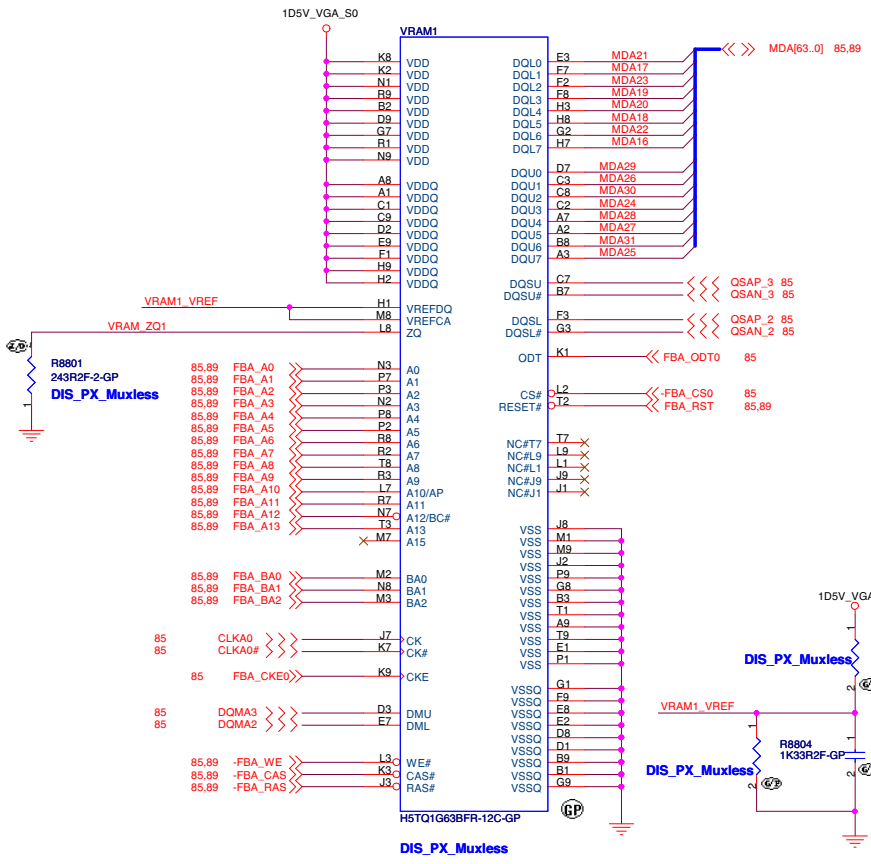
緯創資通 **Wistron Corporation**

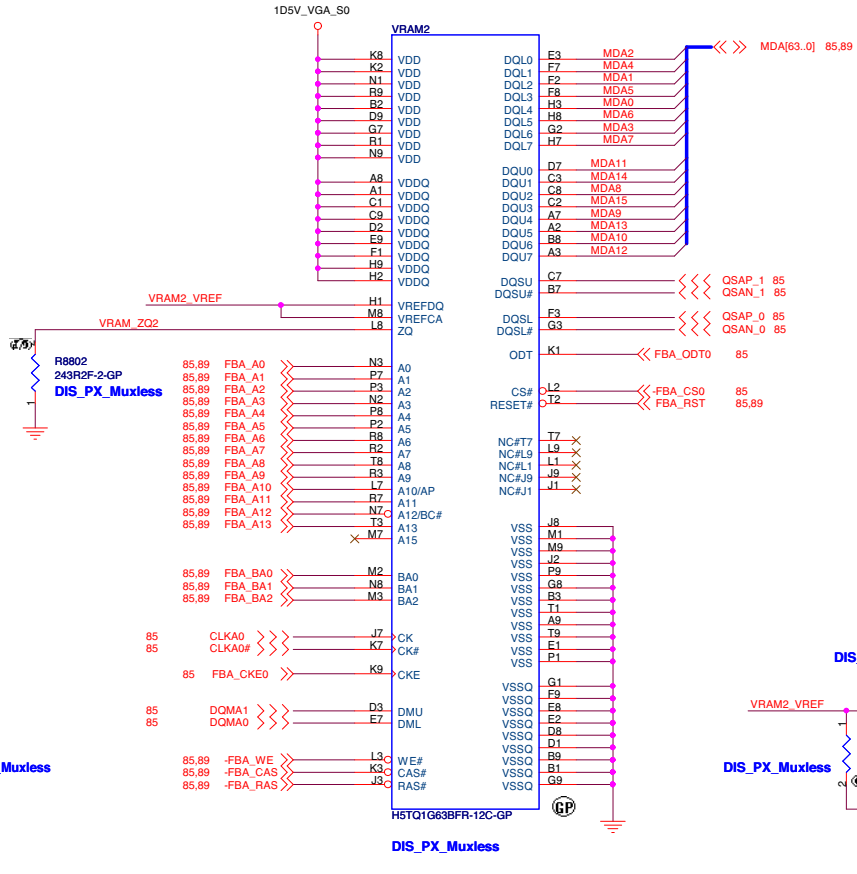
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GPU_DPPWR/GND(5/5)***

Size	Document Number	Rev
Custom	**BAD40_HC**	1

Date: Thursday, April 12, 2012 Sheet 87 of 108





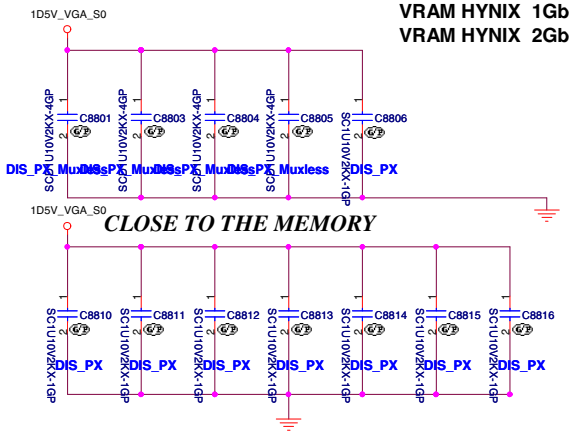
Hy2GX8_VR.2GB0G.001,Sam1GX8_VR.1GB0B.006,,Hy1GX8_72.51G63.C0U,Sam512X4_VR.1GB0B.006,Sam2GX8

VRAM = Hy2GX8,Sam1GX8,,Hy1GX8,Sam512X4,Sam2Gx8

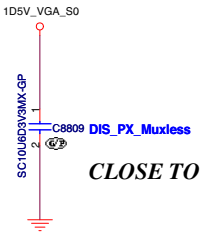
FB CMD mapping Mode D-N12x

VRAM SAMSUNG 1Gb VR.1GB0B.006
VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005
VRAM HYNIX 2Gb VR.2GB0G.001

DG requires 4x0.1uF and 8x1.0uF per VRAM chip



CLOSE TO THE MEMORY



CLOSE TO THE MEMORY

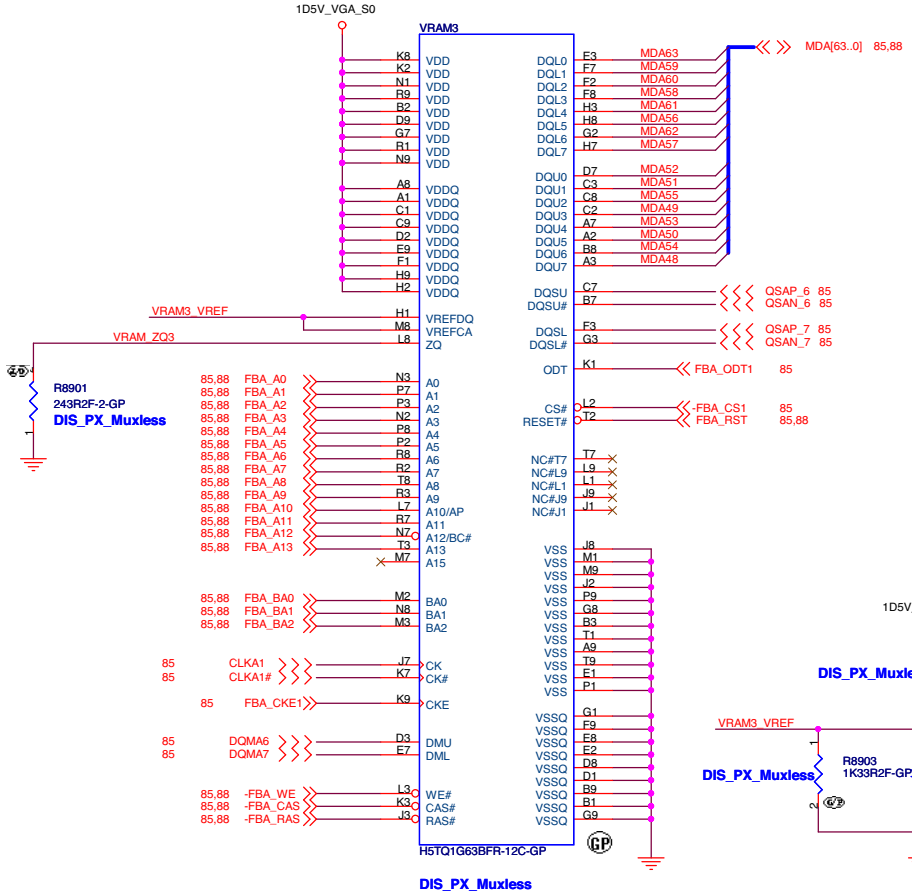
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

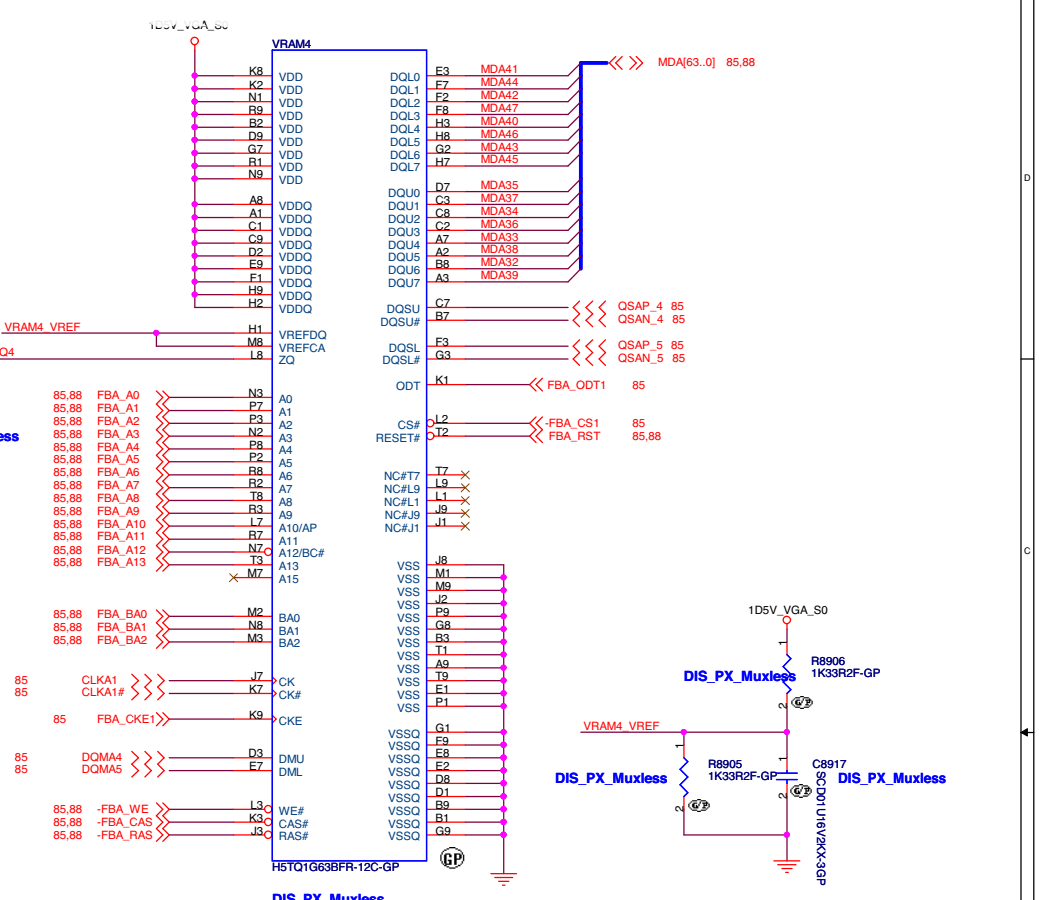
Title: ***GPU-VRAM1,2 (1/4)***

Size	Document Number	Rev
Custom	**BAD40_HC**	**1**

Date: Thursday, April 12, 2012 Sheet 88 of 108



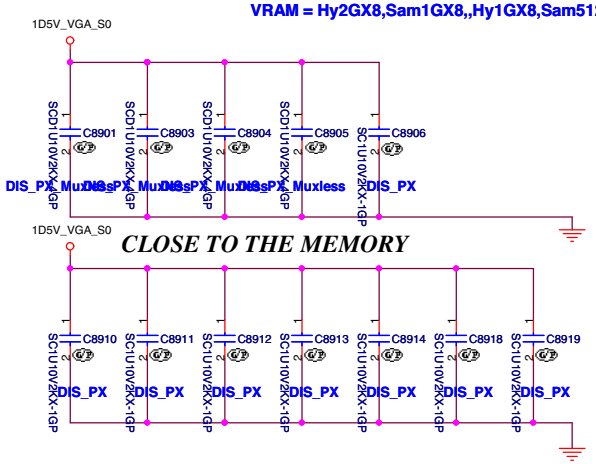
VRAM = Hy2GX8,Sam1GX8,,Hy1GX8,Sam512X4,Sam2Gx8



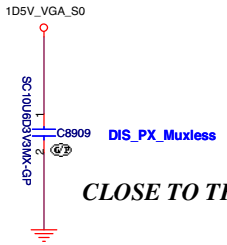
VRAM = Hy2GX8,Sam1GX8,,Hy1GX8,Sam512X4,Sam2Gx8

FB CMD mapping Mode D-N12x

VRAM SAMSUNG 1Gb VR.1GB0B.006
VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005
VRAM HYNIX 2Gb VR.2GB0G.001



CLOSE TO THE MEMORY

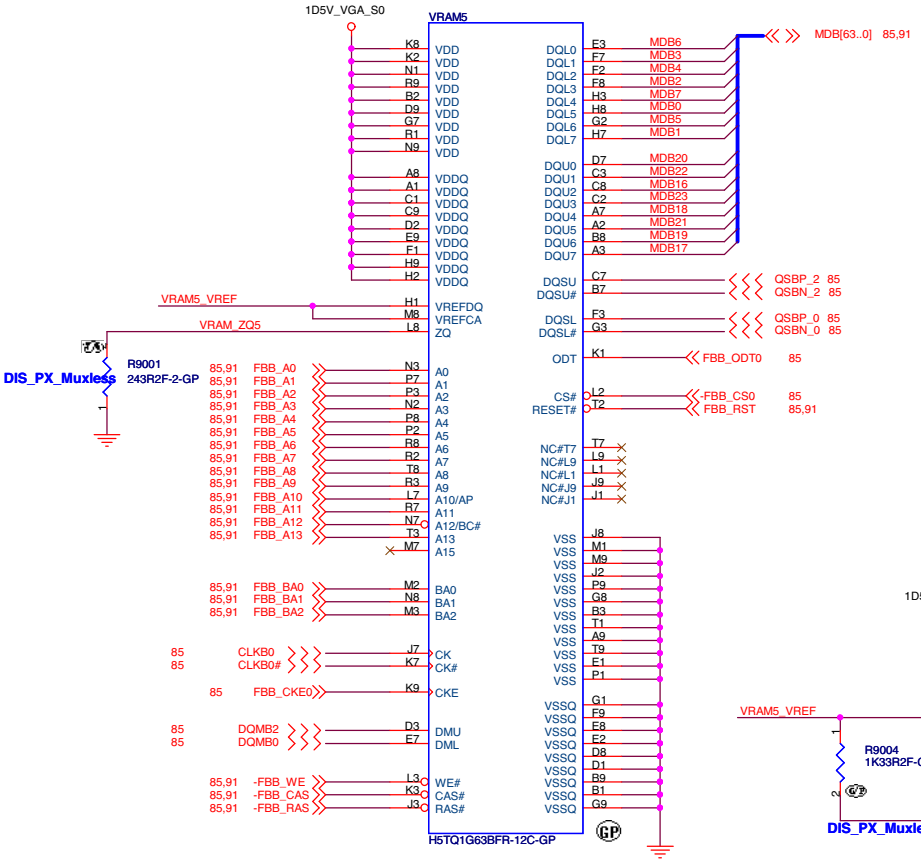


CLOSE TO THE MEMORY

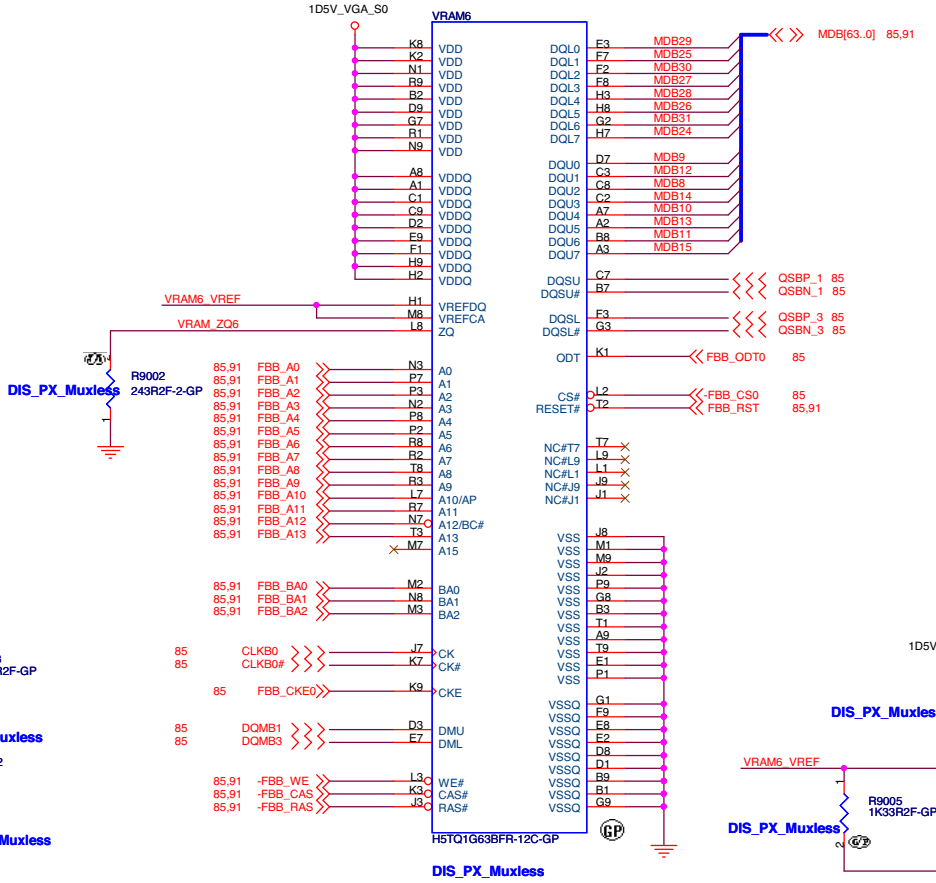
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***GPU-VRAM3,4 (2/4)***	
Size: Custom	Document Number: **BAD40_HC**	Rev: **1**
Date: Thursday, April 12, 2012	Sheet 89 of 108	

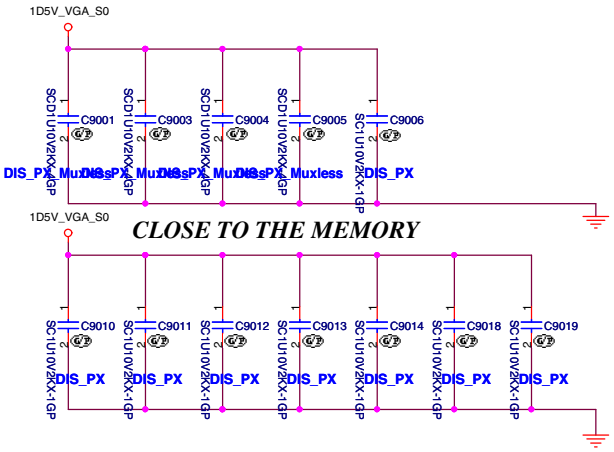


VRAM = Hy2GX8,Sam1GX8,Hynix1GX8,Sam2GX8



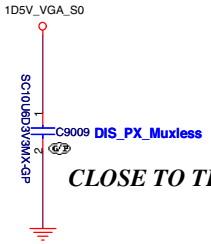
VRAM = Hy2GX8,Sam1GX8,Hynix1GX8,Sam2GX8

VRAM SAMSUNG 1Gb VR.1GB0B.006
VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005
VRAM HYNIX 2Gb VR.2GB0G.001



CLOSE TO THE MEMORY

DG requires 4x0.1uF and 8x1.0uF per VRAM chip



CLOSE TO THE MEMORY

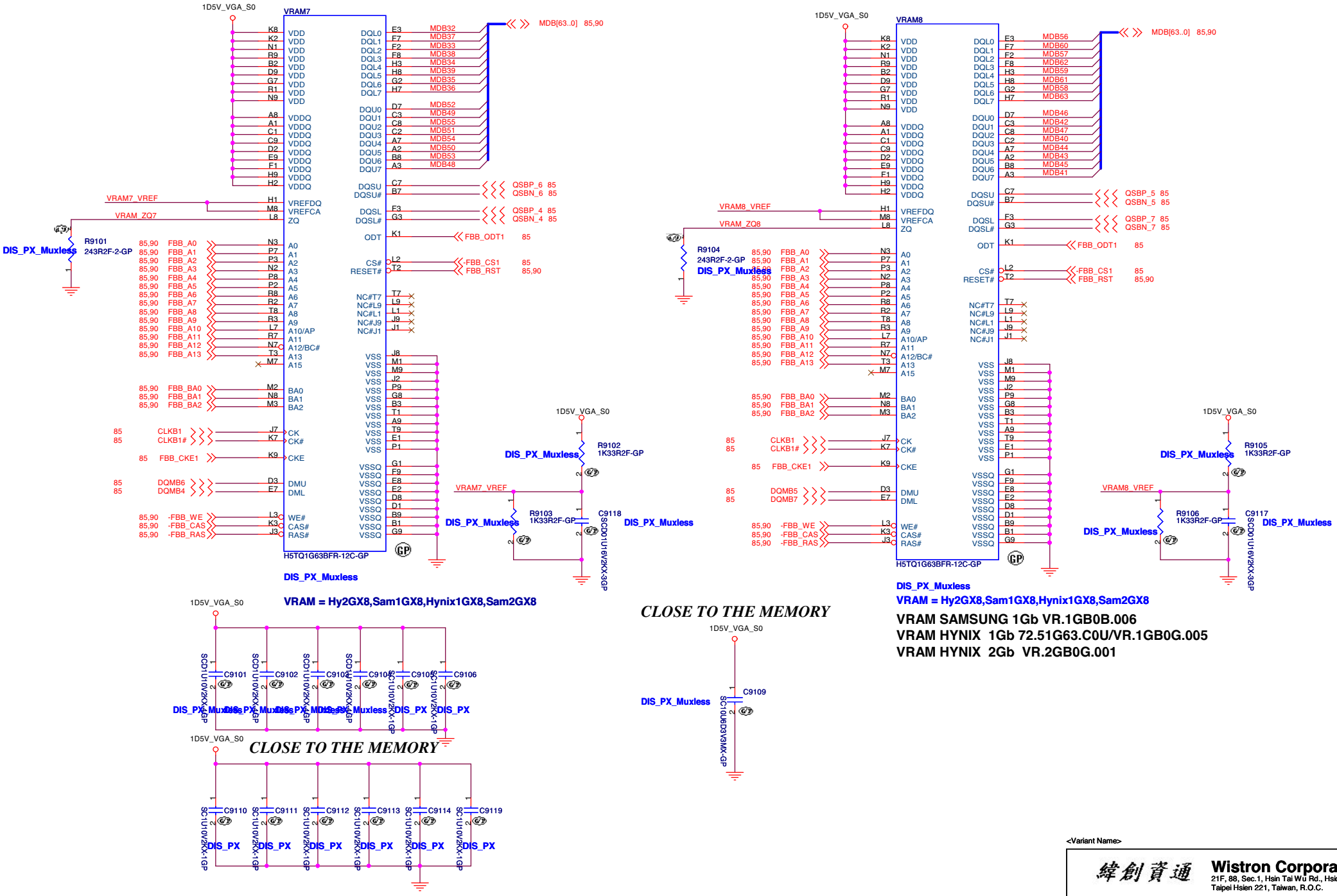
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GPU-VRAM5,6 (3/4)***

Size	Document Number	Rev
Custom	**BAD40_HC**	1

Date: Thursday, April 12, 2012 Sheet 90 of 108



<variant_name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***GPU-VRAM7,8 (4/4)***	
Size: Custom	Document Number: **BAD40_HC**	Rev: **1**
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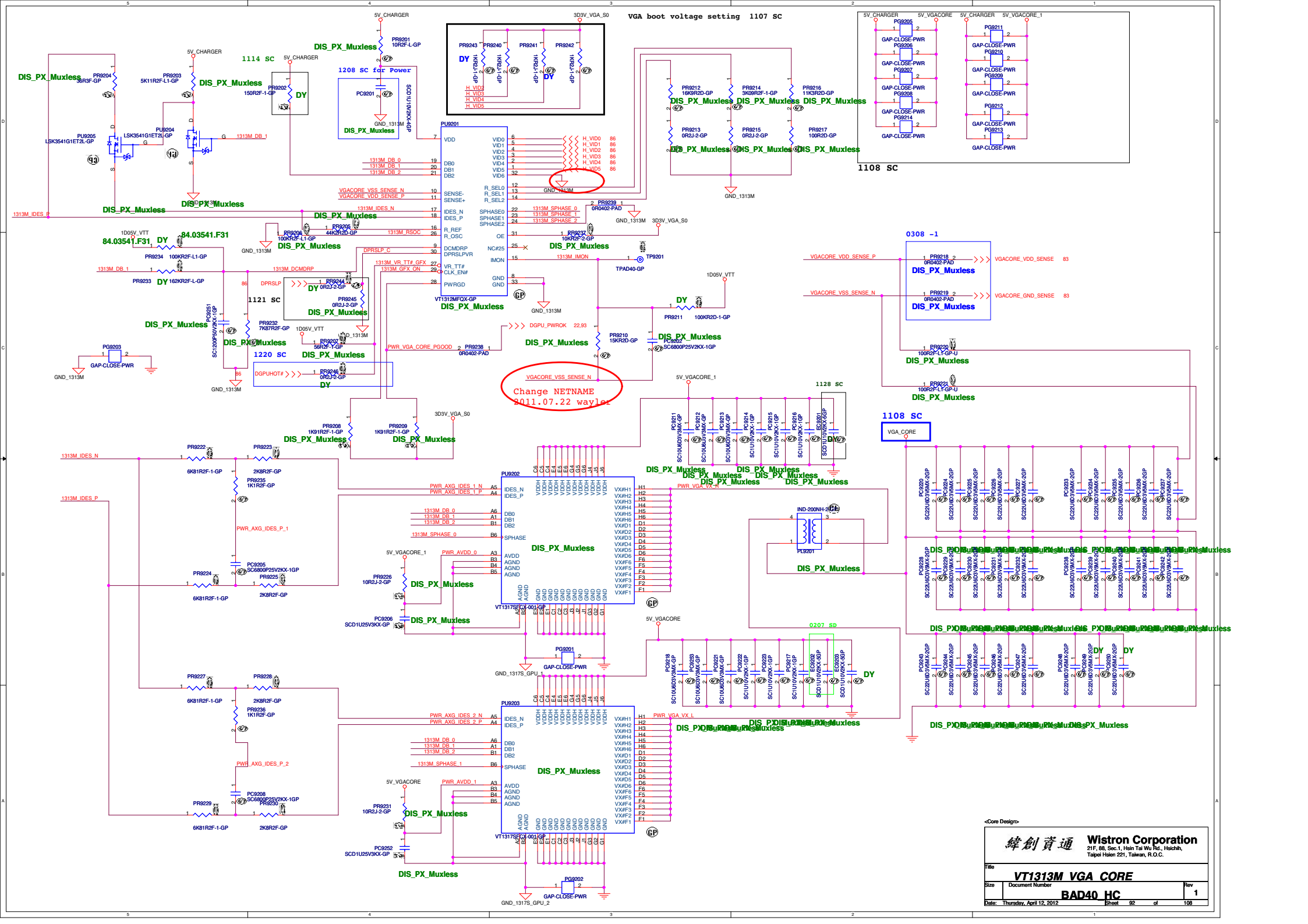
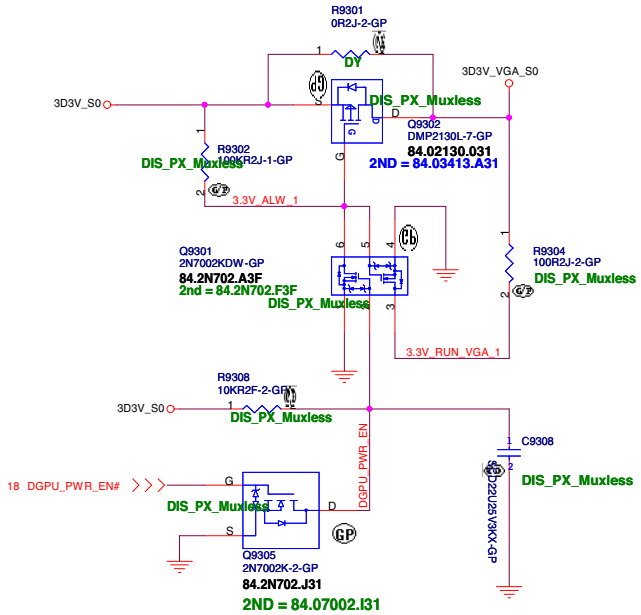
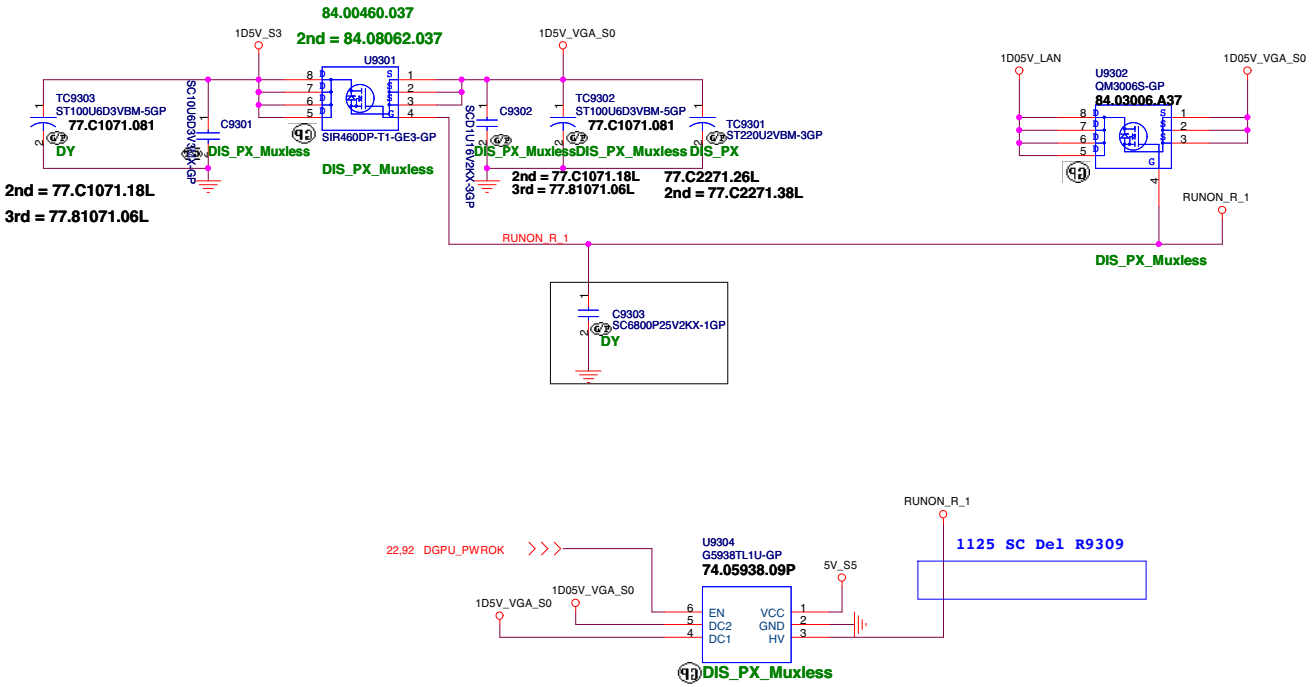

VGA boot voltage setting 1107 SC
1108 SC
1114 SC
1208 SC for Power
1121 SC
1220 SC
1128 SC
0308 -1
0207 SP
Change NETNAME
2011.07.22 waylee
VT1312MFQX-GP
VT1317SFCX-001-GP
DIS_PX_Muxless
Wistron Corporation
VT1313M VGA CORE
BAD40_HC

+3VS to 3.3V_DELAY Transfer



1D5V_VGA_S0



1D8V_S0 to 1D8V_VGA_S0

1125 SC Del Q9306

1D8V_S0_NV = IFPA_IOVDD & IFPB_IOVDD, it should be the latest ramp up rail.

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	DISCRETE VGA POWER	
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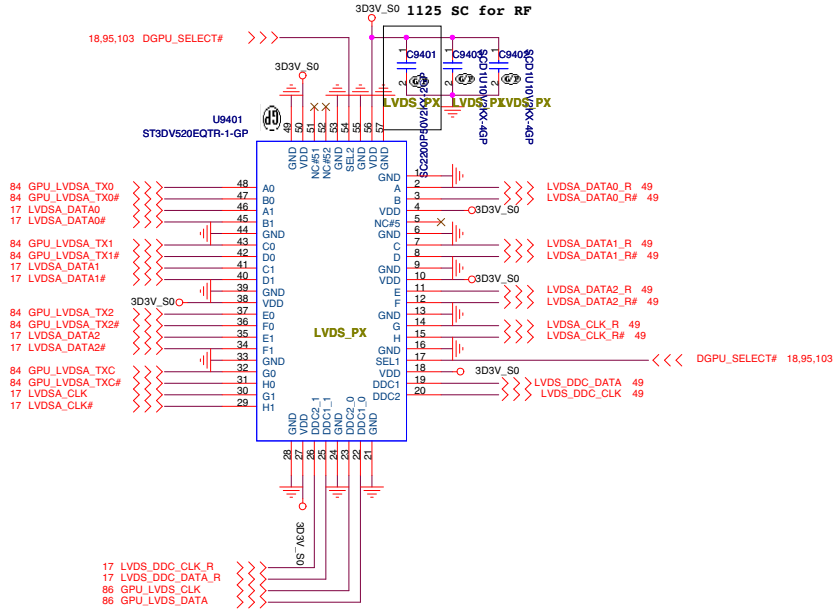
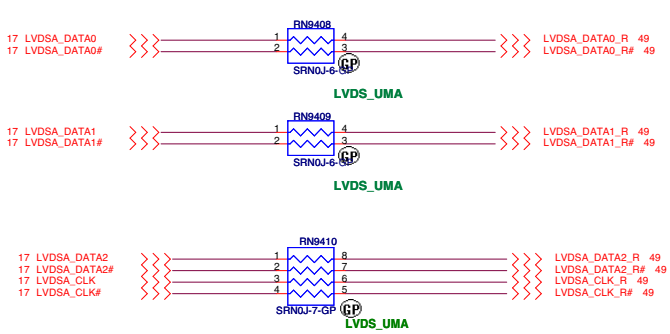
LVDS

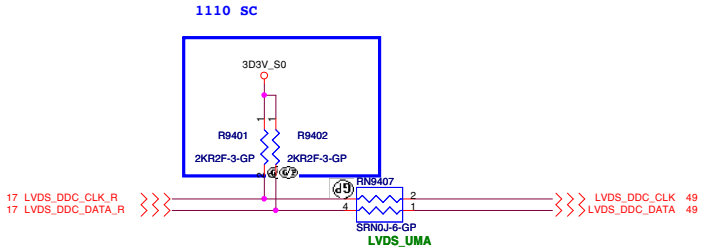




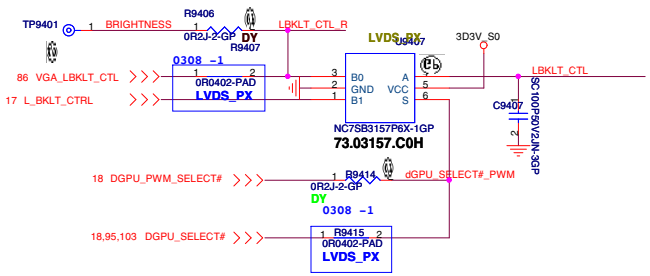
SEL->L(X=nX0),H(X=nX1)

SEL1 Control A~H

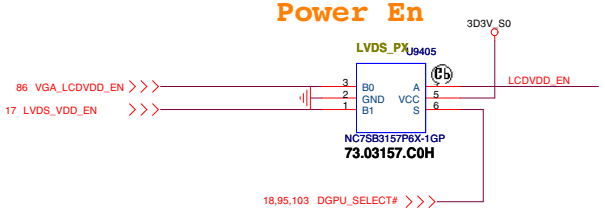
SEL2 Control DDC1,DDC2



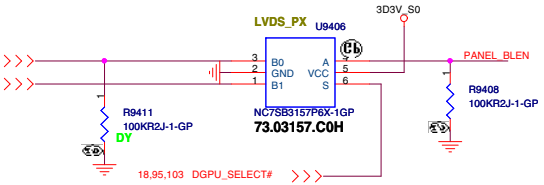
Panel BL brightness



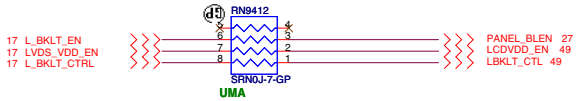
Power En



BL En



Panel BL brightness/Power En/BL En



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*LVDS_Switch*	
Size: Custom	Document Number: BAD40_HC	Rev: 1
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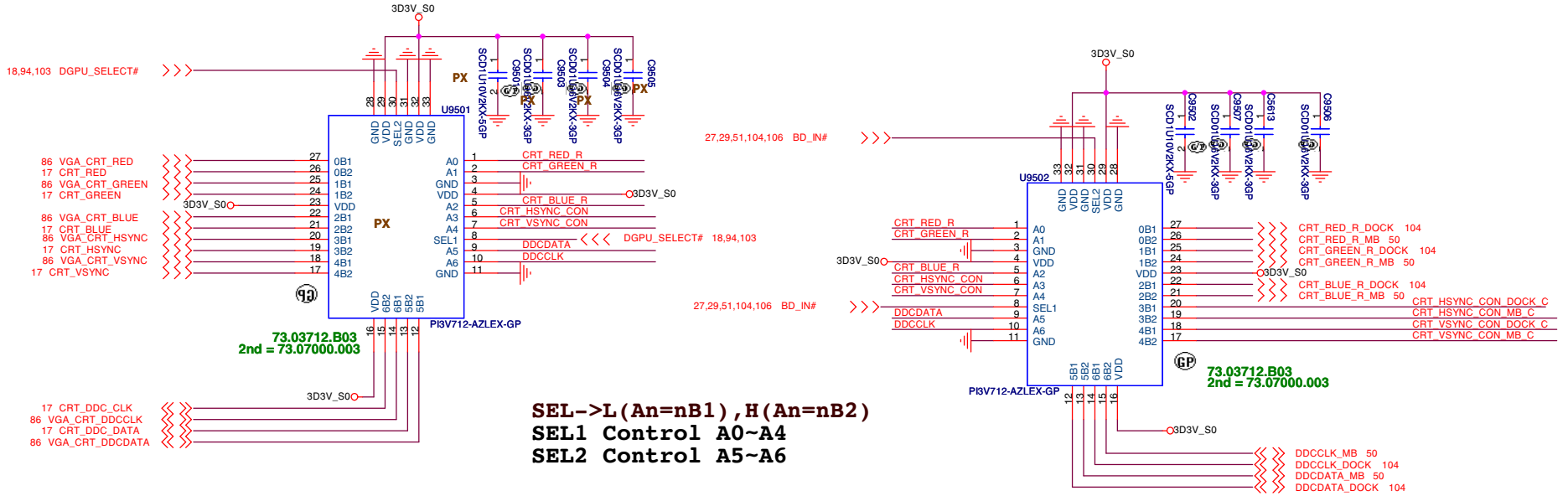
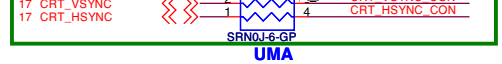
CRT DDCDATA & DDCCLK

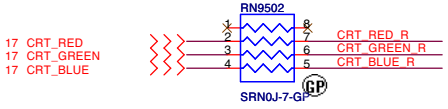


SEL->L(An=nB1),H(An=nB2)
SEL1 Control A0~A4
SEL2 Control A5~A6

SB 0915

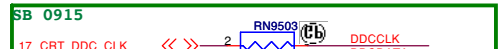


UMA



UMA

SB 0915



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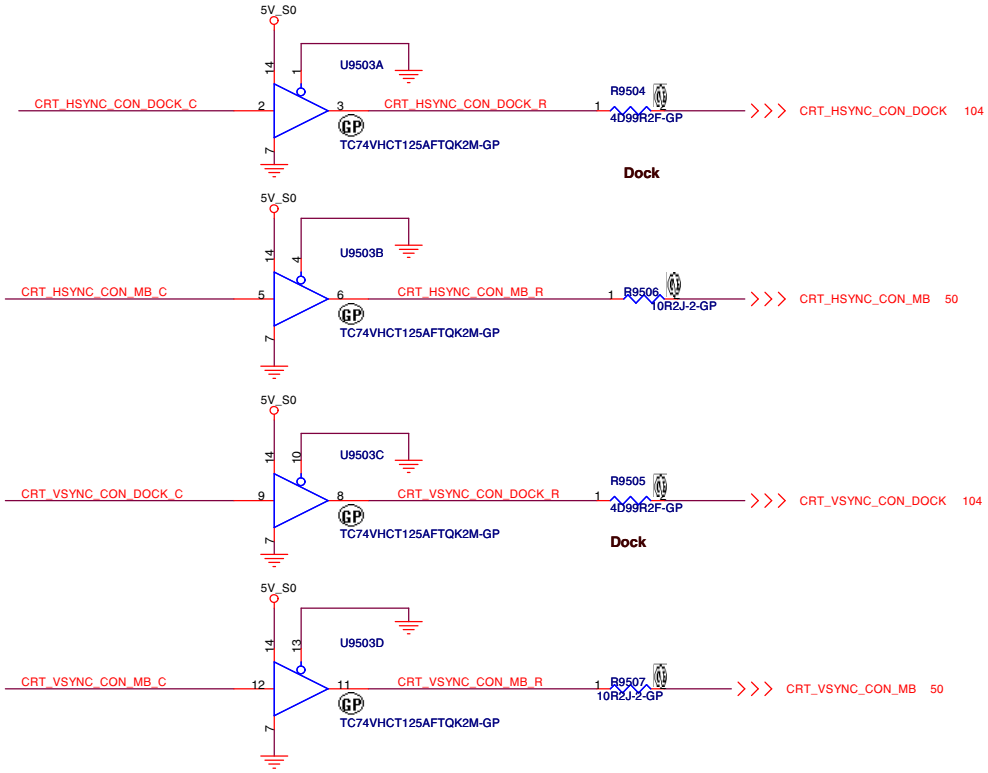

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CRT_Switch***

Size	Document Number	Rev
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SSID = SDIO

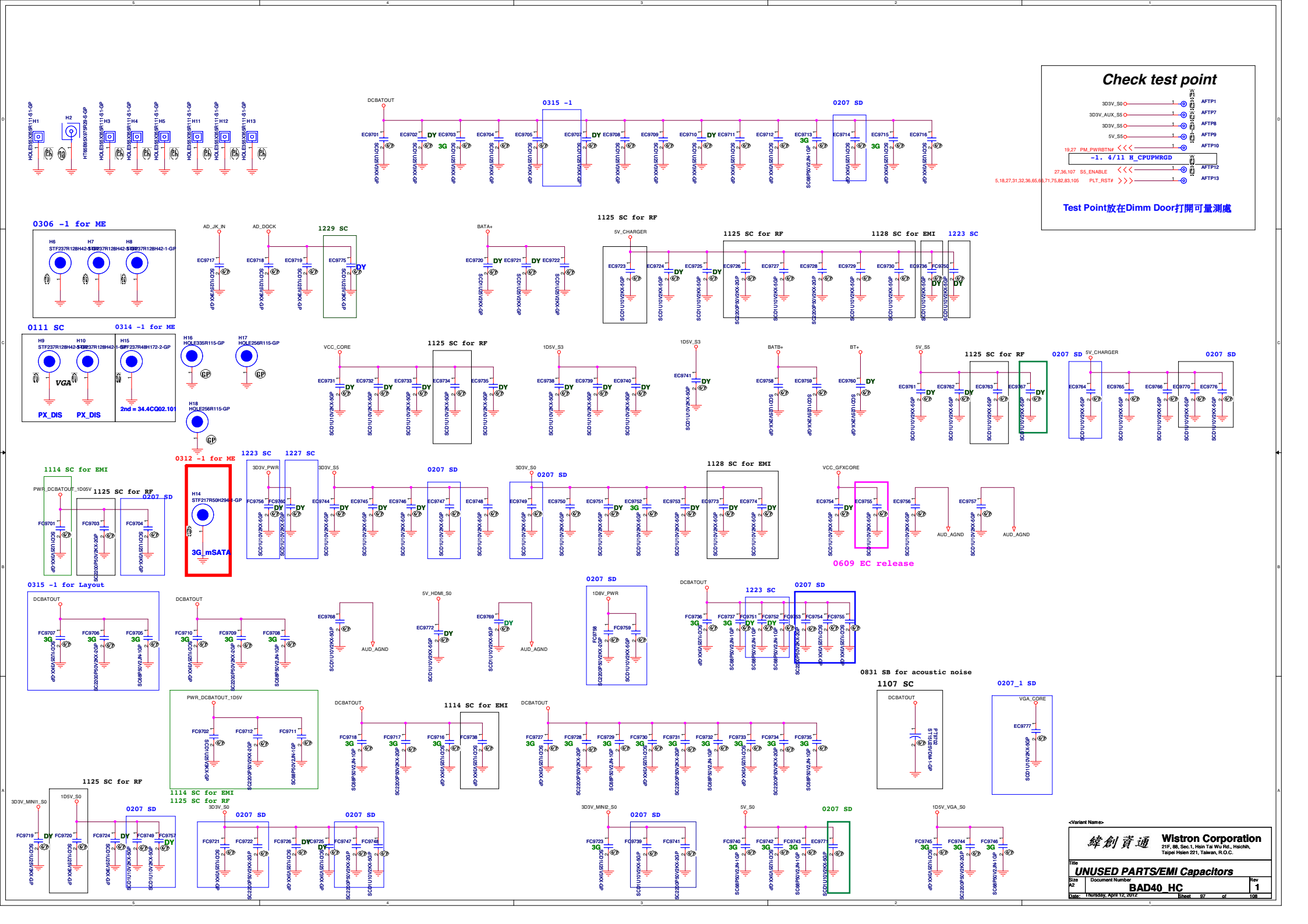
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

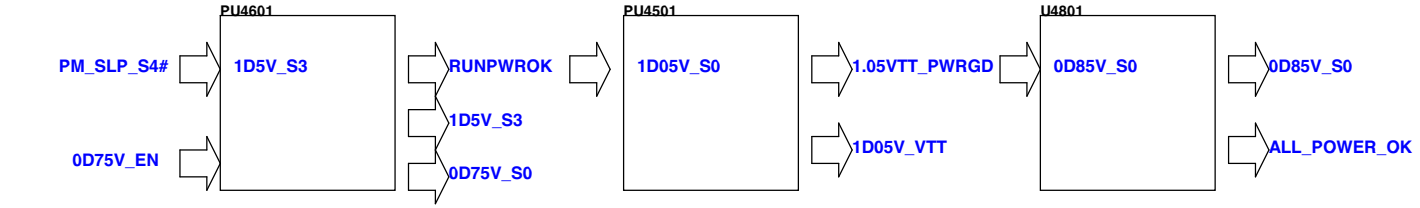
Title: ***TOUCH PANEL***

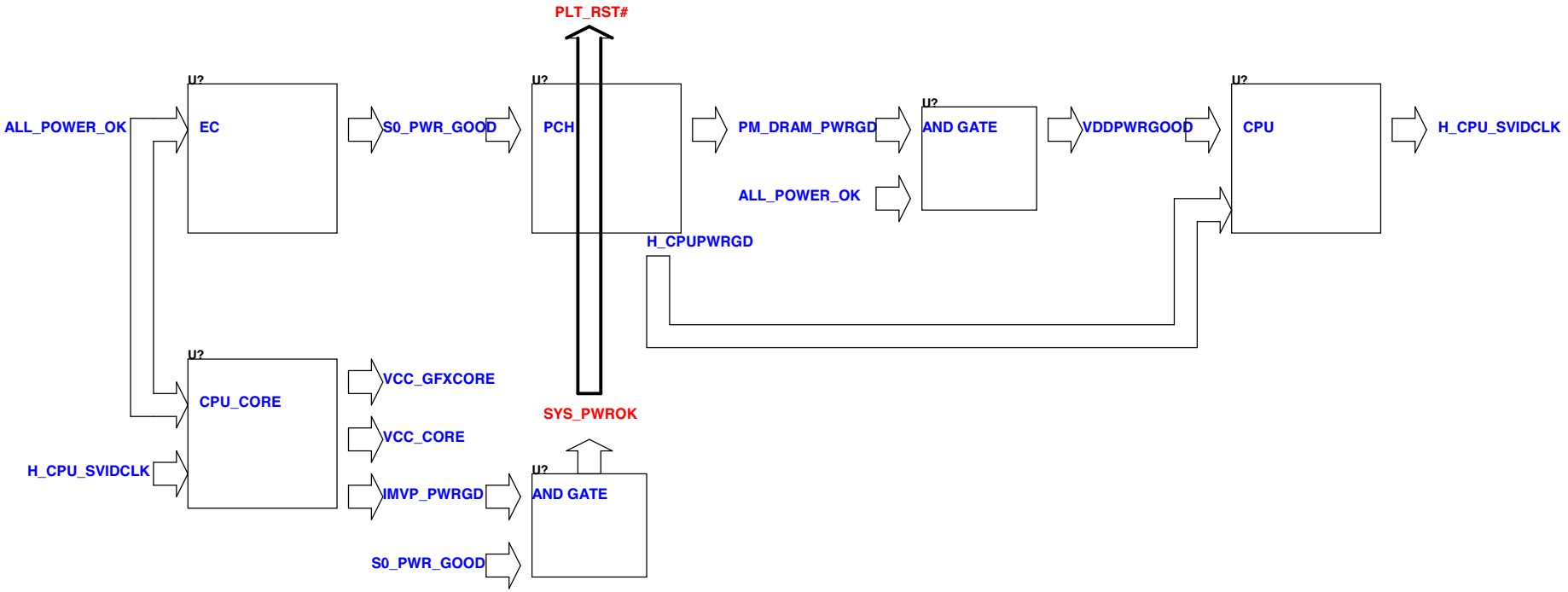
Size	Document Number	Rev
A2	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 96 of 108


Check test point
3D3V_S0
3D3V_AUX_S5
3D3V_S5
5V_S5
19,27 PM_PWRBTN#
-1. 4/11 H_CPUPWRGD
27,36,107 S5_ENABLE
5,18,27,31,32,36,65,68,71,75,82,83,105 PLT_RST#
AFTP1
AFTP7
AFTP8
AFTP9
AFTP10
AFTP12
AFTP13
Test Point放在Dimm Door打開可量測處
0306 -1 for ME
0315 -1
0207 SD
1125 SC for RF
1128 SC for EMI
1223 SC
1229 SC
0111 SC
0314 -1 for ME
VGA
PX_DIS
PX_DIS
0312 -1 for ME
3G_mSATA
1114 SC for EMI
1227 SC
0315 -1 for Layout
0609 EC release
0831 SB for acoustic noise
1107 SC
0207_1 SD
1125 SC for RF
1114 SC for EMI
1125 SC for RF
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
UNUSED PARTS/EMI Capacitors
BAD40_HC
Thursday, April 12, 2012

Power Sequence





<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Change History*

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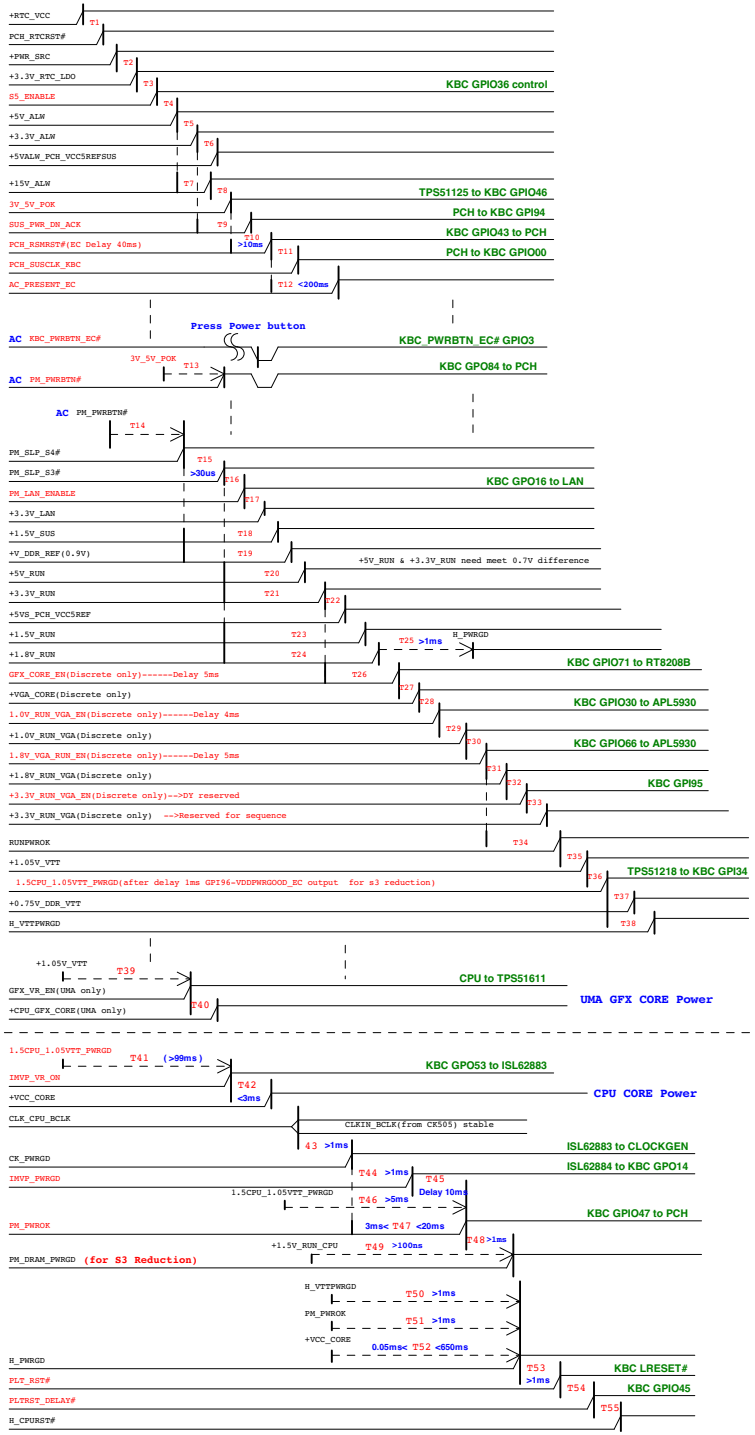
Intel-Power Up Sequence

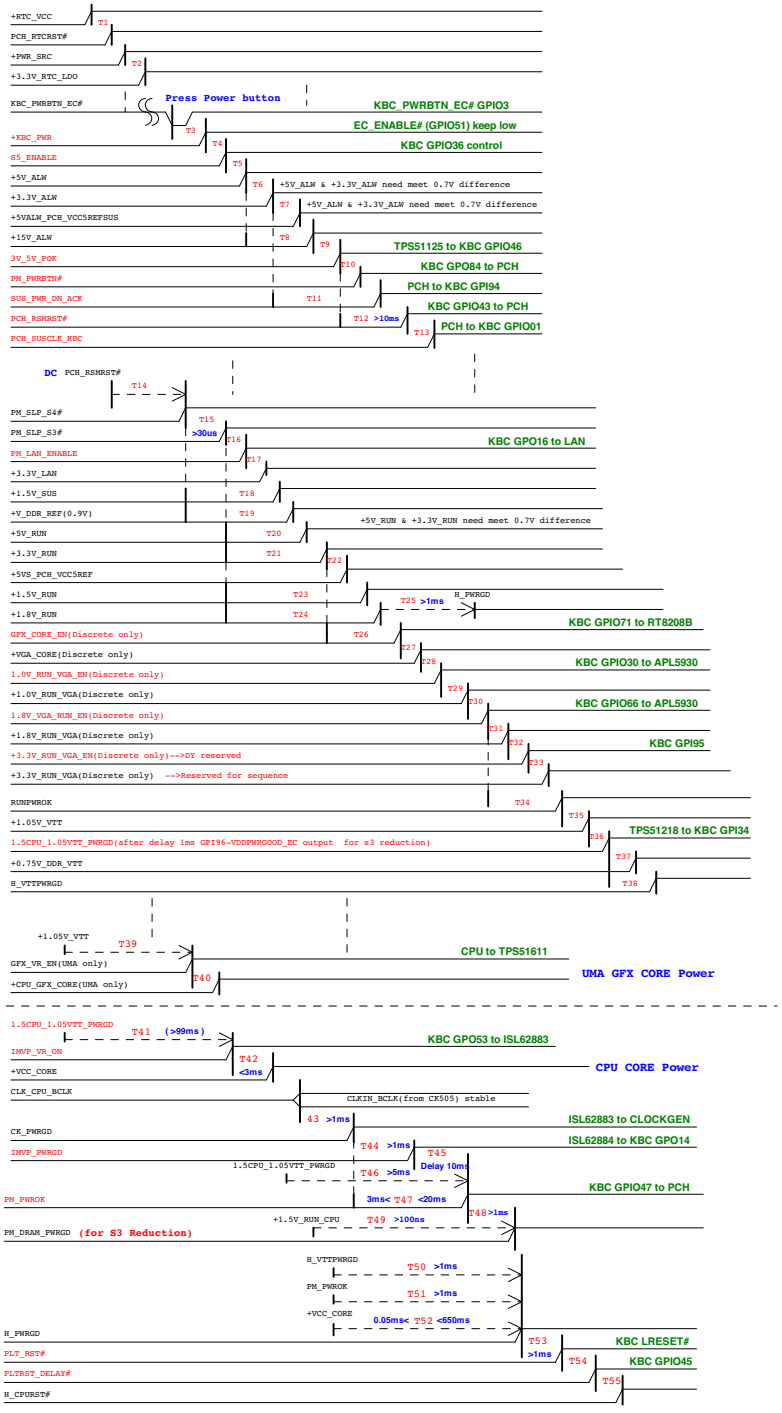
(AC mode)

red word: KBC GPIO



(DC mode)

red word: KBC GPIO



HR PX

Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Sequence

Size	Document Number	Rev
M	BAD40_HC	1

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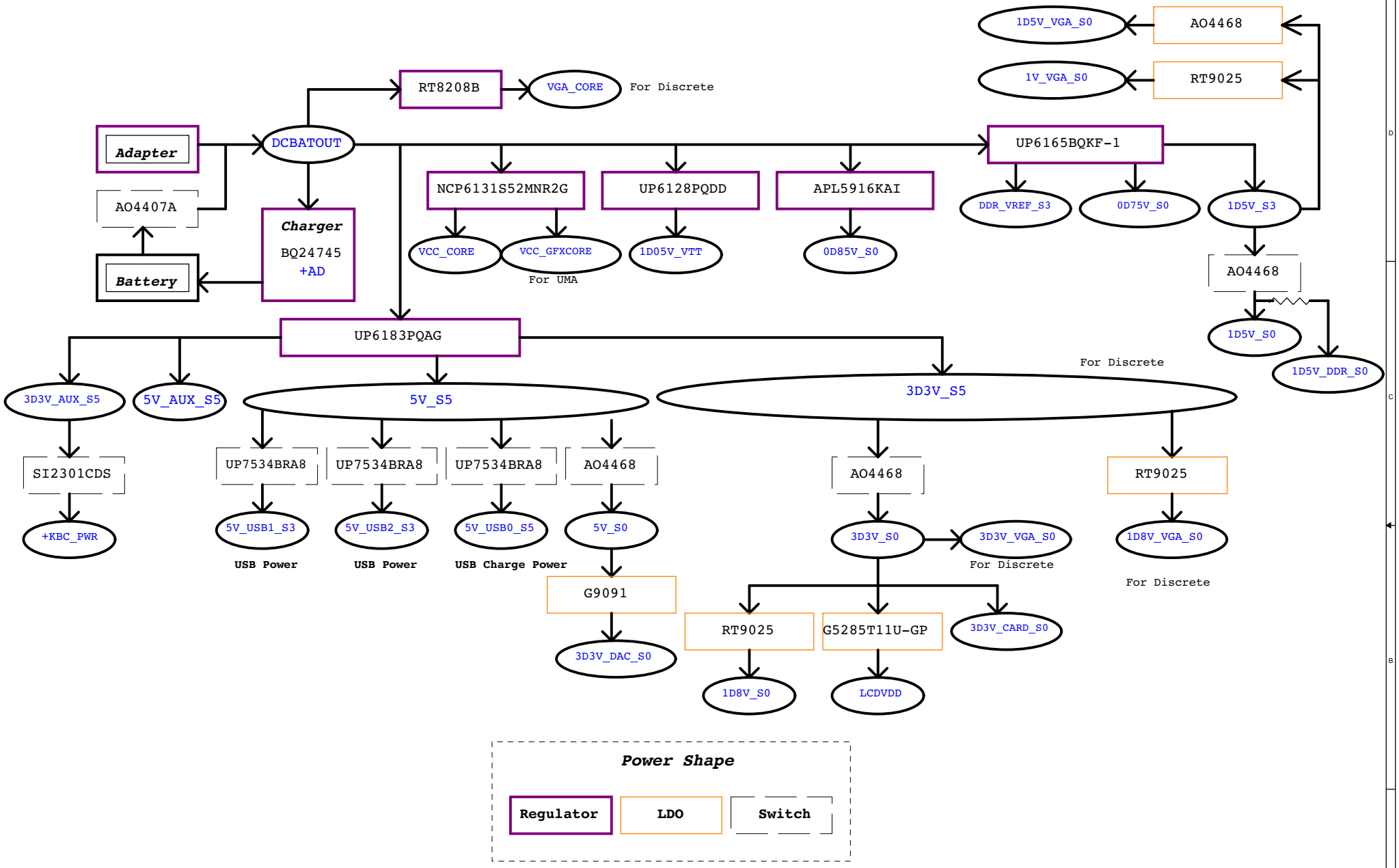

HR PX

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Block Diagram

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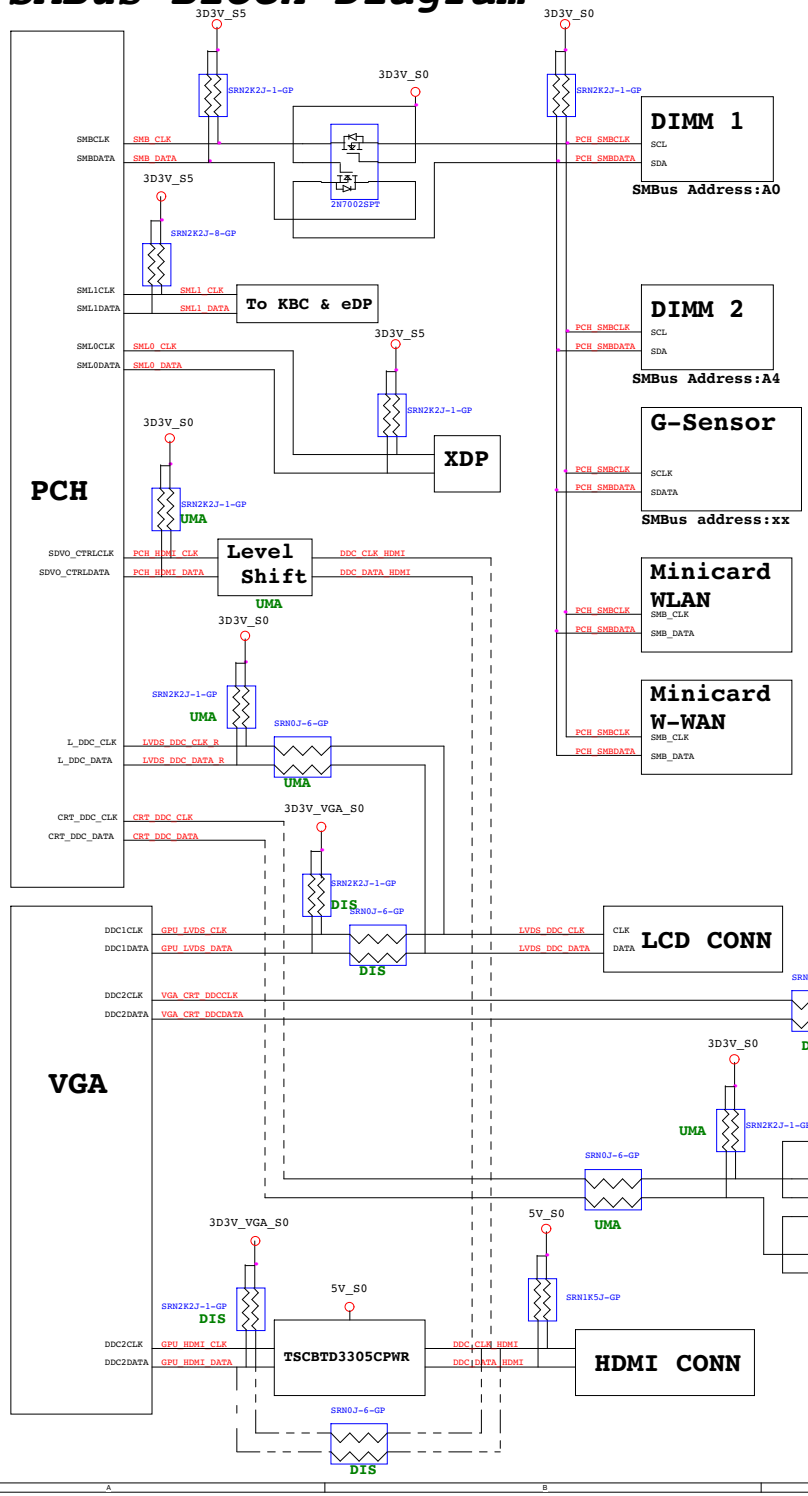
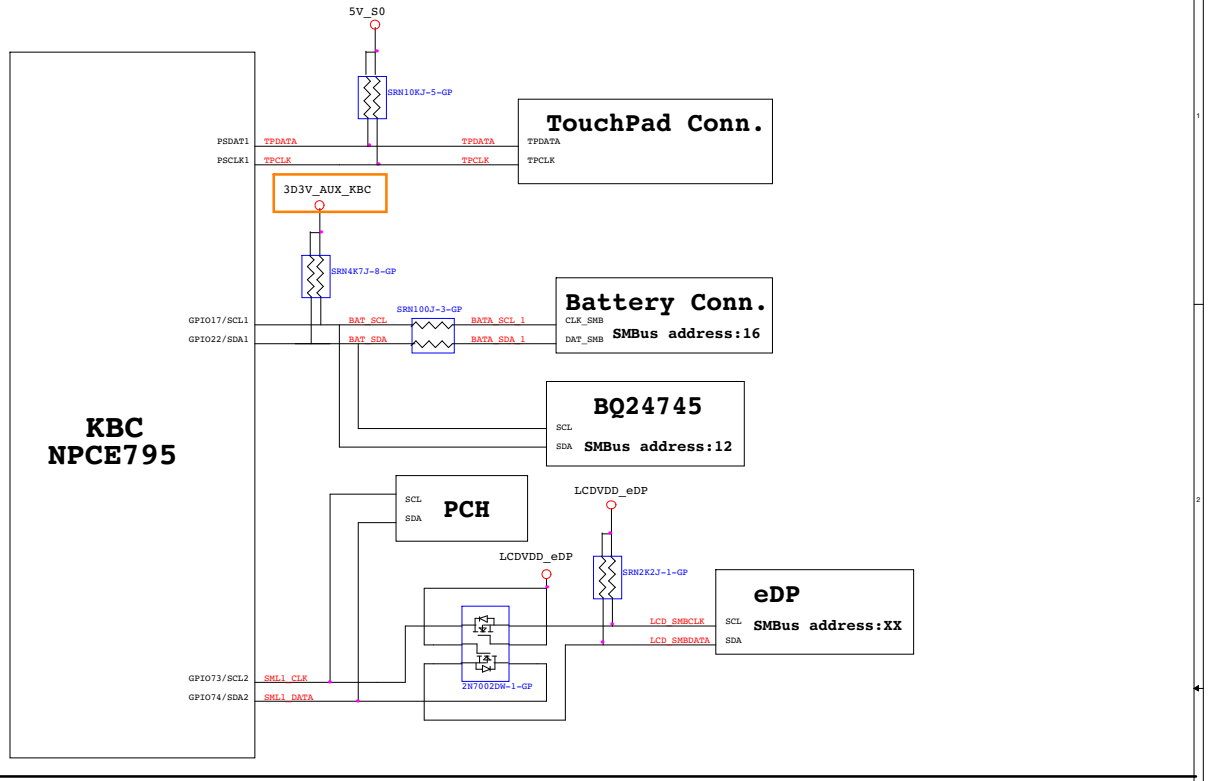
PCH SMBus Block Diagram



KBC SMBus Block Diagram



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SMBUS Block Diagram

Size: A2 | Document Number: BAD40_HC | Rev: 1

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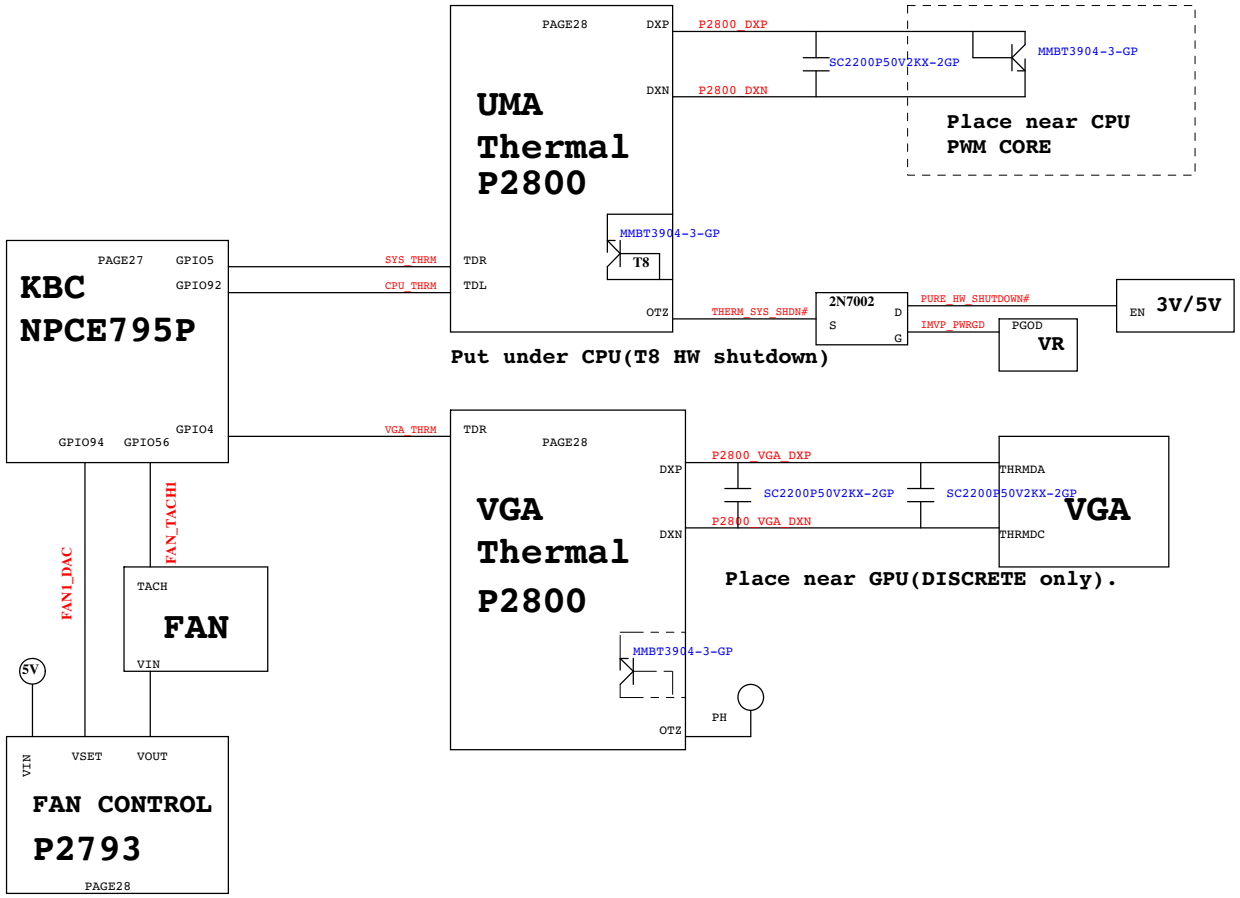
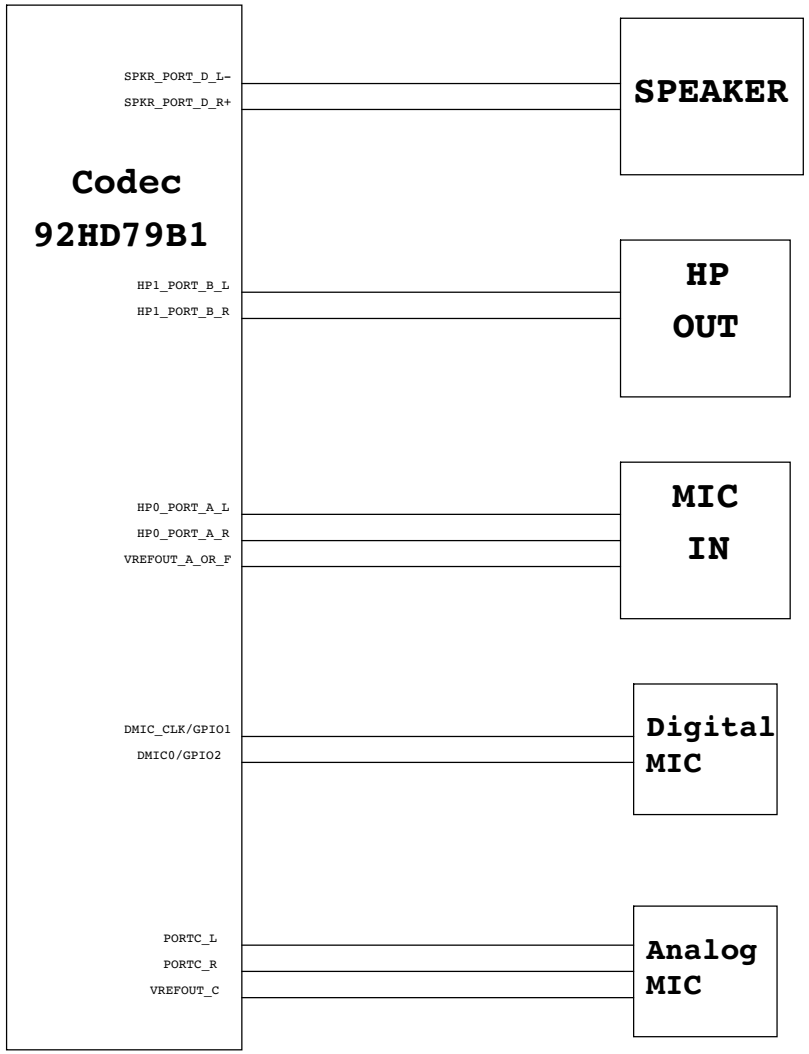
Thermal Block Diagram



Audio Block Diagram



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Audio Block Diagram

Size	Document Number	Rev
Custom	BAD40_HC	1

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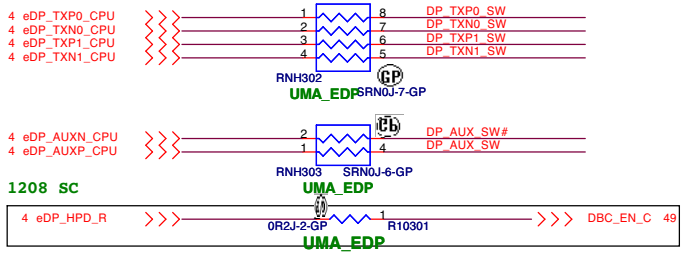
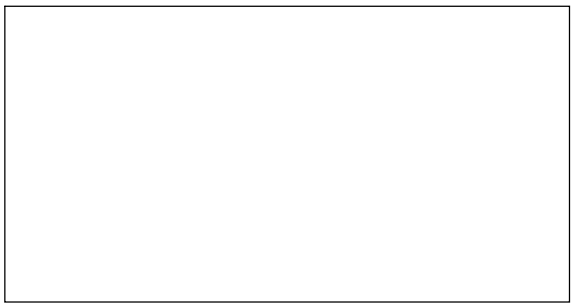
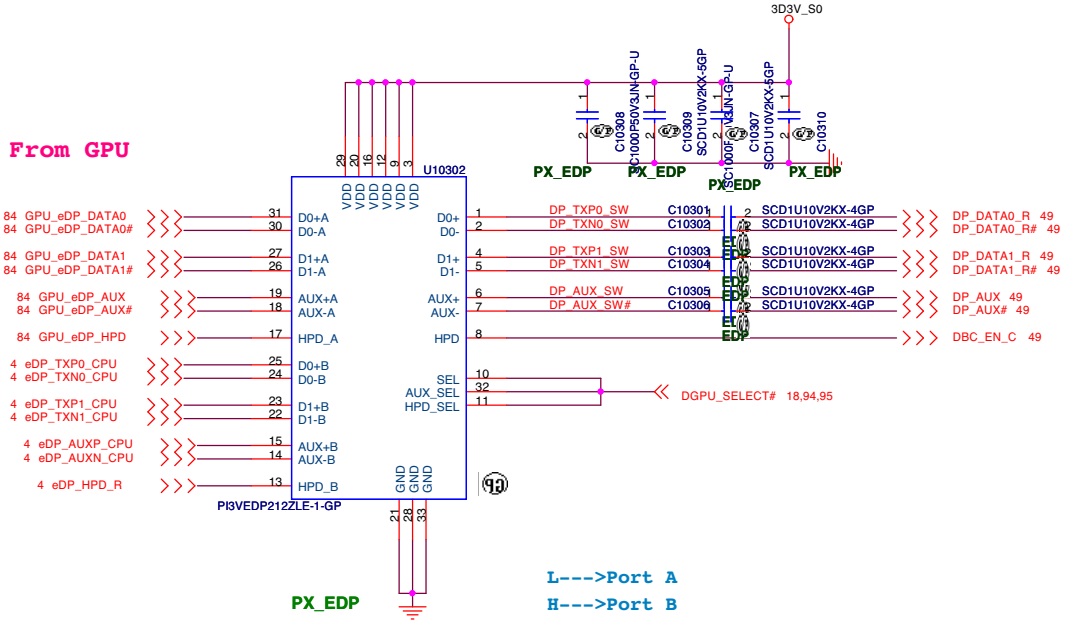


1117 SC del eDP SMBUS





<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: Switch GFX DP		
Size: A3	Document Number: BAD40_HC	Rev: 1
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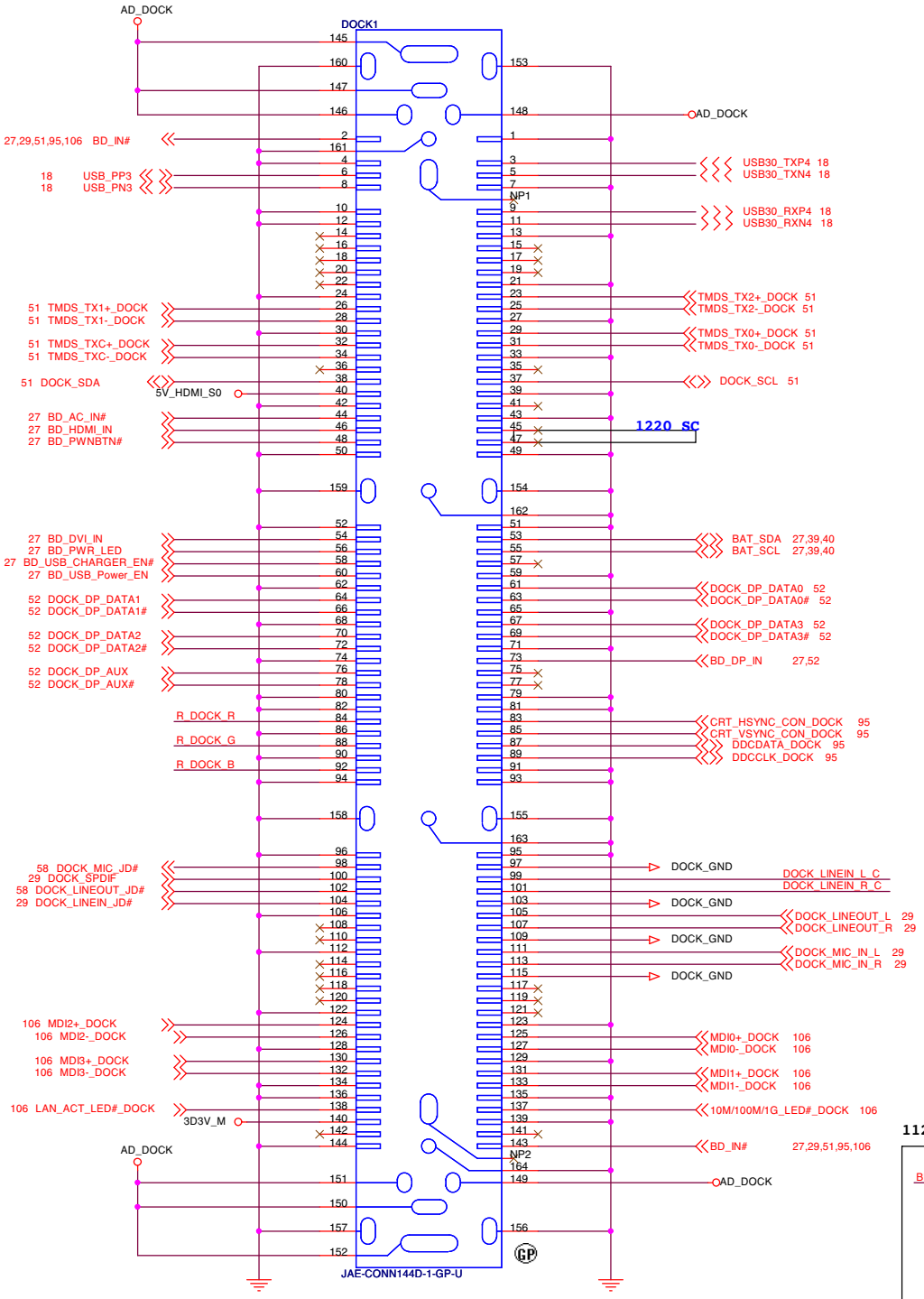
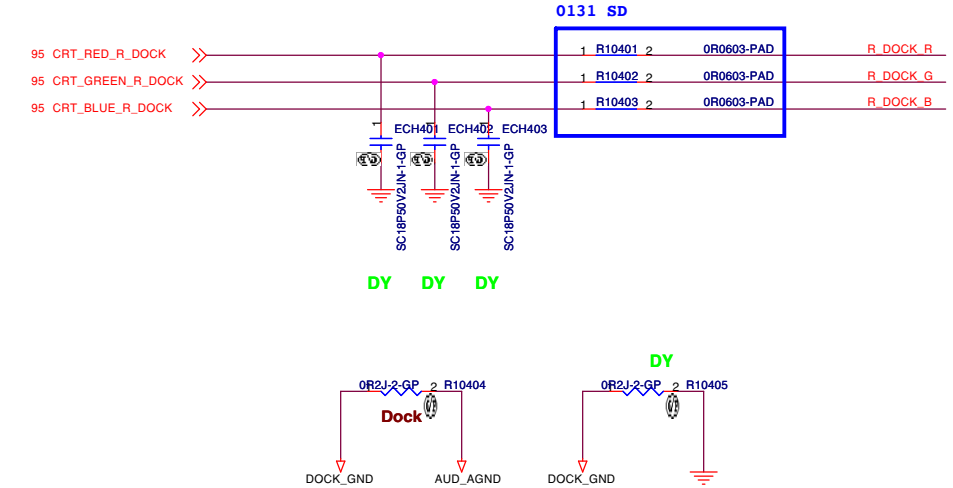
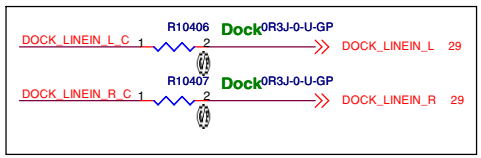
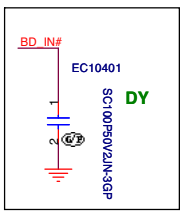




1128 SC for EMI



1128 SC for EMI



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BOTTOM DOCKING

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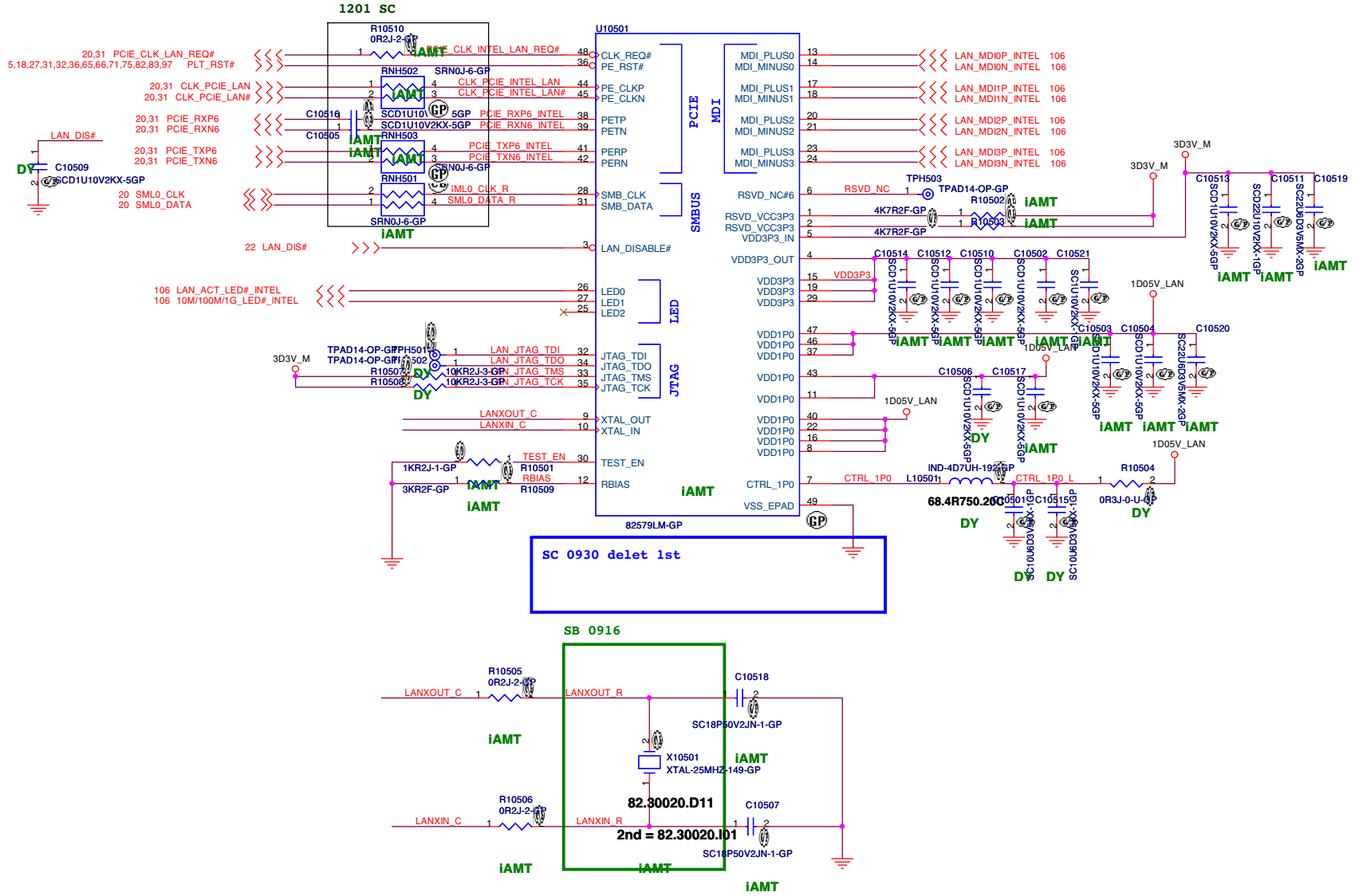

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN INTEL 82579

Size	Document Number	Rev
A3	BAD40_HC	1

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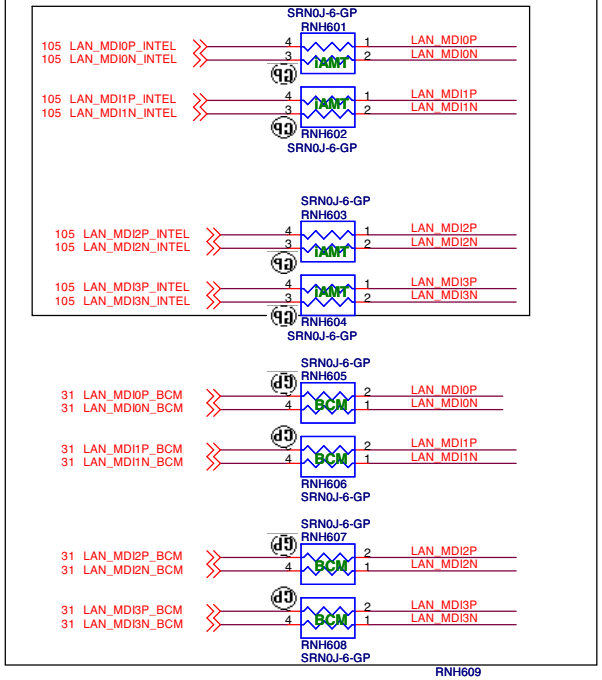
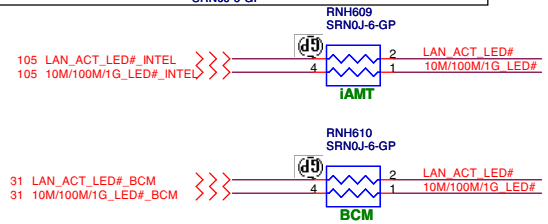
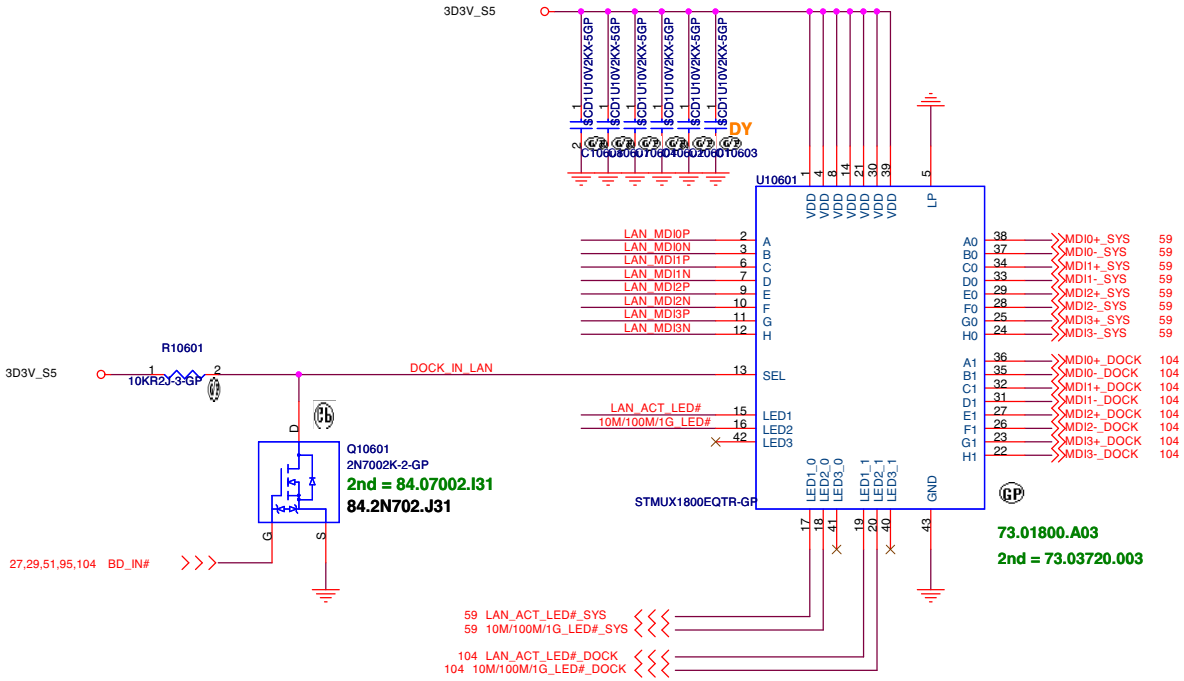
1201 SC

1206 SC swap for layout





LAN switch



Function	SEL	
to X0	L	SYSTEM
to X1	H	DOCK

<Variant Name>

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Title: LAN SWITCH

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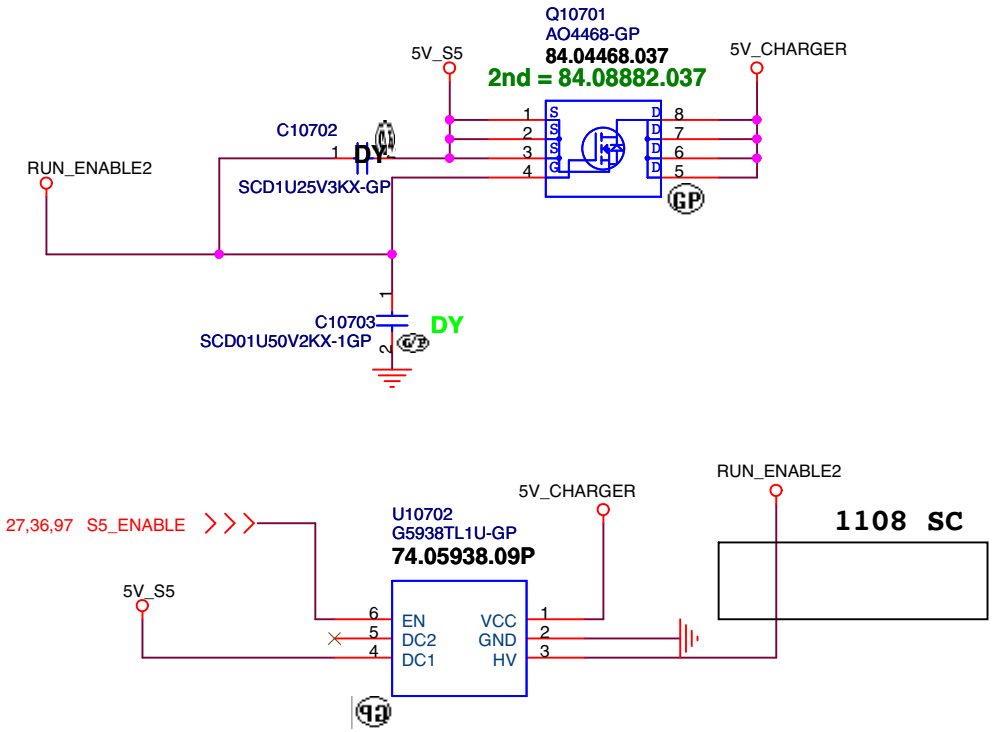

USB charger @ USB30 BD

<Variant Name>

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Title	*USB Charger/ 5V_S5*	
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reserve

<Core Design>

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Title: **USB2 HUB AU6256**

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