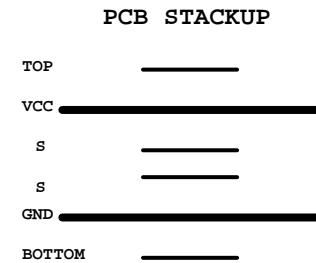
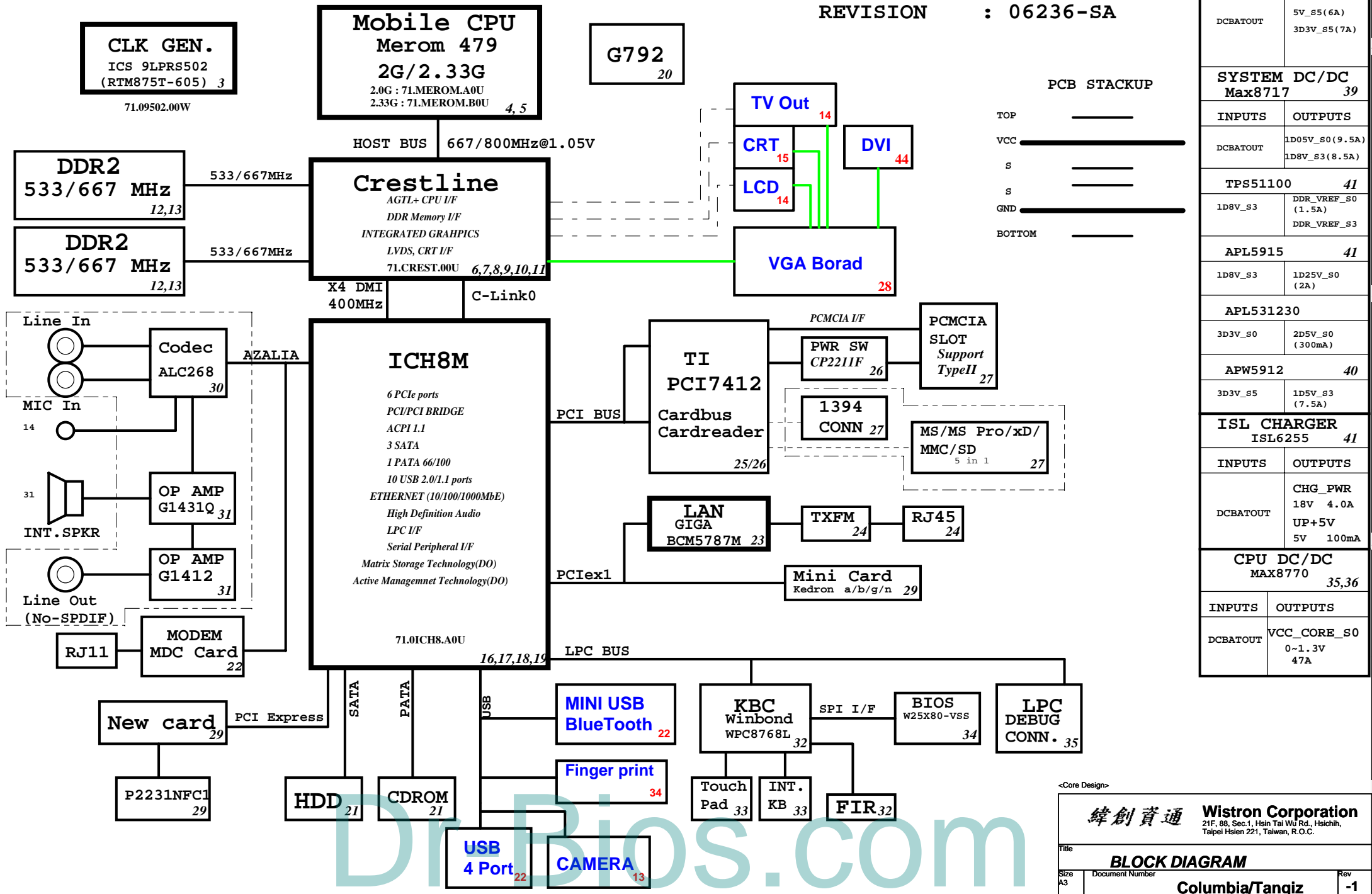


Columbia/Tangiz Block Diagram

Project code: 91.4T301.001
 PCB P/N : 48.4T301.0SA
 REVISION : 06236-SA



SYSTEM DC/DC MAX8744 38	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(7A)
SYSTEM DC/DC Max8717 39	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(9.5A) 1D8V_S3(8.5A)
TPS51100 41	
1D8V_S3	DDR_VREF_S0(1.5A) DDR_VREF_S3
APL5915 41	
1D8V_S3	1D25V_S0(2A)
APL531230	
3D3V_S0	2D5V_S0(300mA)
APW5912 40	
3D3V_S5	1D5V_S3(7.5A)
ISL CHARGER ISL6255 41	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 4.0A UP+5V 5V 100mA
CPU DC/DC MAX8770 35,36	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.3V 47A

ICH8M Functional Strap Definitions

ICH8-M EDS 21762 2.0V1 page 16

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers: offset 224h)
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE config2 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#/ SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05 and VccCL1_5 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05 and VccCL1_5 VRM's when sampled high
LAN100_SLP	Integrated VccLAN1_05 and VccCL1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccLAN1_05 and VccCL1_05 VRM's when sampled high
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	This signal has a weak internal pull-up. Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be used in manufacturing environments.

ICH8M Integrated Pull-up and Pull-down Resistors

ICH8-M EDS 21762 2.0V1

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 10K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH [3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	PULL-UP 13K

Crestline Strapping Signals and Configuration

Crestline EDS 20954 1.0 page 7

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG[8:6]	Reserved	
	Low Power PCI Express	0 = Normal mode 1 = Low Power mode (Default)
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. 1 = Normal operation(Default):Lane Numbered in order
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[15:14]	Reserved	Reserved
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal operation (Default):lane Numbered in order 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	0 = Only SDVO or PCIE x1 is operational (Default) 1 =SDVO and PCIE X1 are operating simultaneously via the PEG port
SDVOCRTL_DATA	SDVO Present	0 = No SDVO Card present (Default) 1 = SDVO Card present

NOTE: All strap signals are sampled with respect to the leading edge of the Crestline GMCH PWROK in signal.

History

ICH8M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ approximately 33 ohm

PCI Routing

page 17

	IDSEL	INT	REQ	GNT
TI7412	AD22	G:CARDBUS B:1394 F:Flash Media G:SD Host	0	0

USB Table

USB	
Pair	Device
0	USB1
1	NC
2	USB2
3	USB4
4	USB3
5	BLUETOOTH
6	WEBCAM
7	FT
8	MINICARD
9	NEW1

PCIE Routing

LANE1	LAN BCM5787M
LANE2	MiniCard WLAN
LANE3	NewCard WLAN

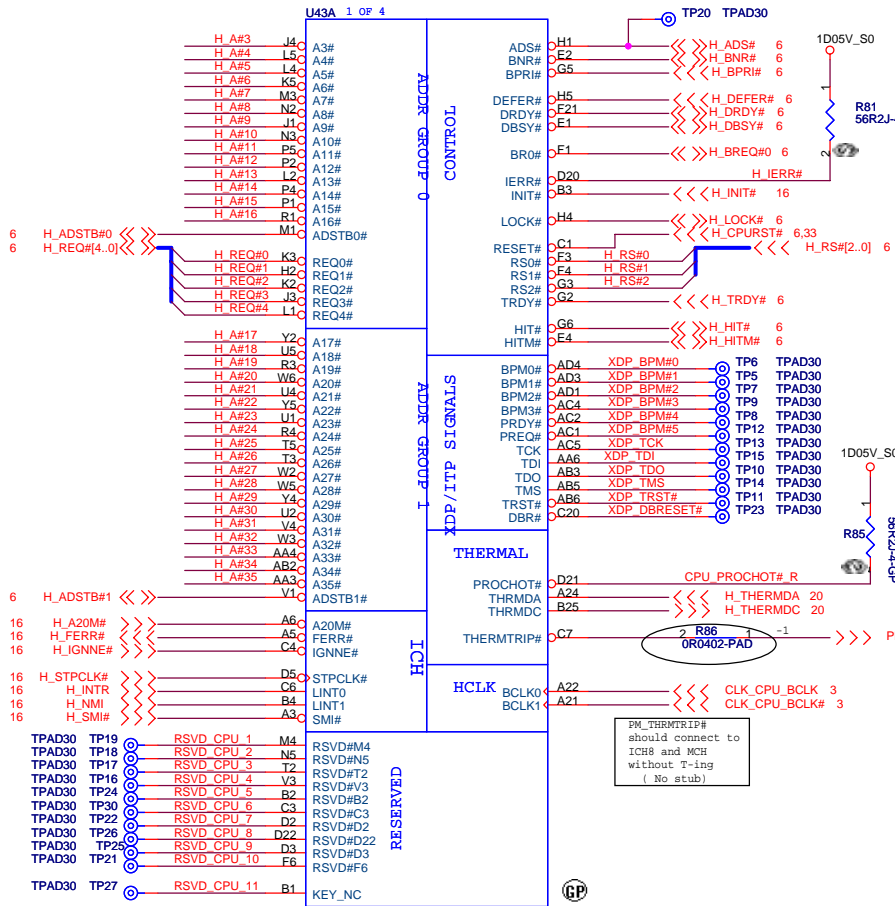
UMA

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Reference			
Title	Document Number		Rev
Size A3	Columbia/Tangiz		-1
Date: Monday, February 26, 2007	Sheet 2	of	45



6 H_A#(35..3) <<< H_A#(35..3)

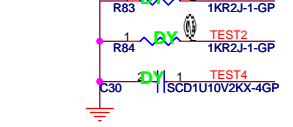
H_DINV#[3..0] <<>> H_DINV#[3..0] 6
H_DSTBN#[3..0] <<>> H_DSTBN#[3..0] 6
H_DSTBP#[3..0] <<>> H_DSTBP#[3..0] 6
H_D#(63..0) <<>> H_D#[63..0] 6



Place testpoint on H_IERR# with a GND 0.1" away

Layout Note: "CPU_GTLREF0" 0.5" max length.

PM_THRMTRIP# should connect to ICH8 and MCH without T-ling (No stub)

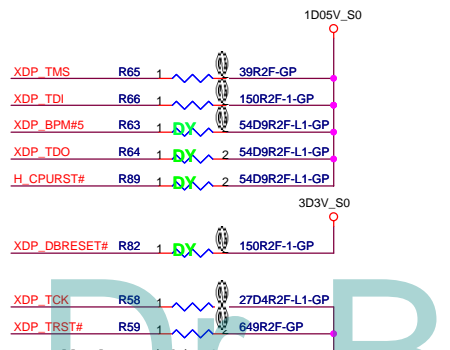


Net "TEST4" as short as possible, make sure "TEST4" routing is reference to GND and away other noisy signals

Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5"

BGA479-SKT6-GPU3
62.10079.001

BGA479-SKT6-GPU3



All place within 2" to CPU



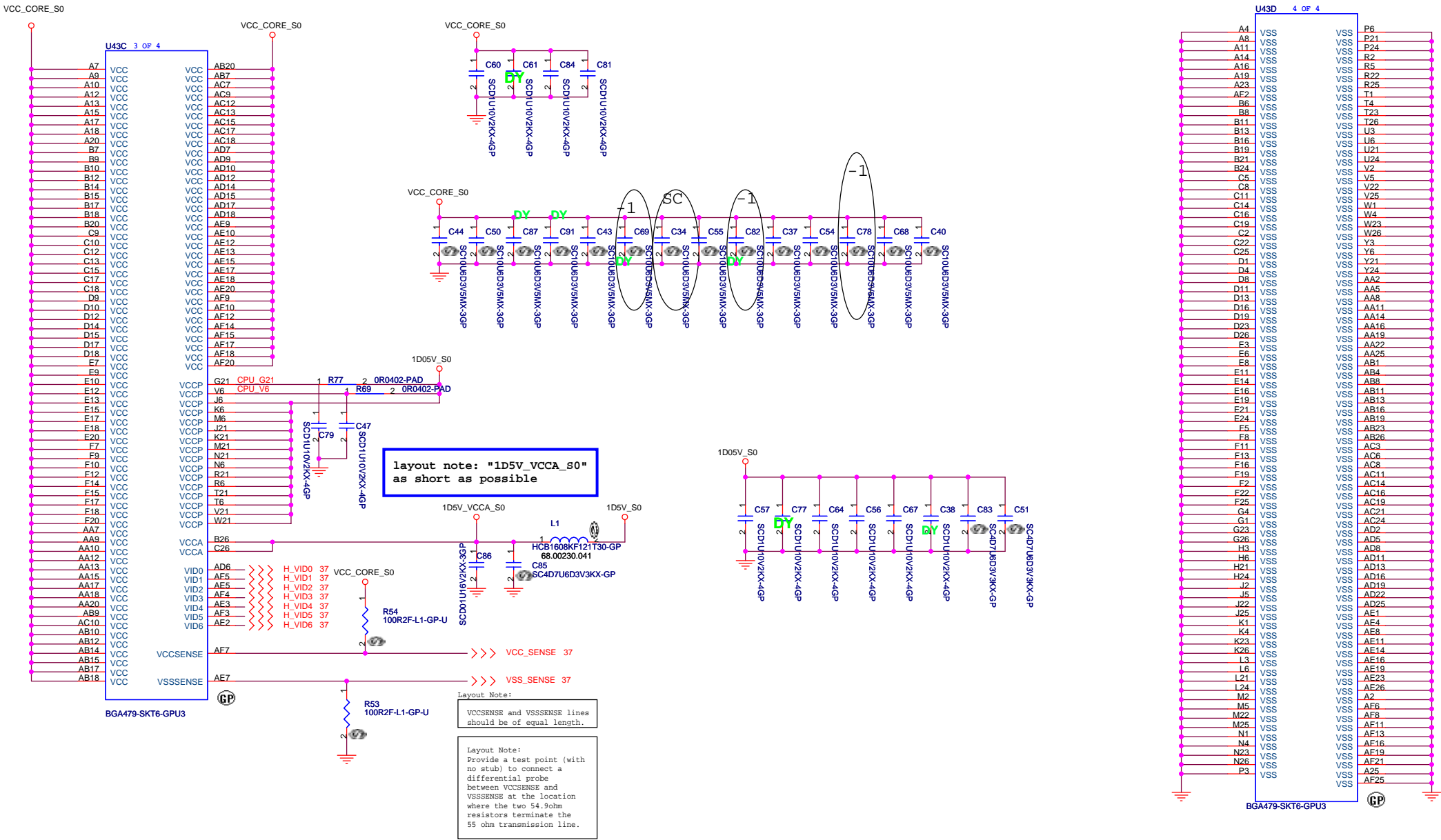
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Title: **CPU (1 of 2)**

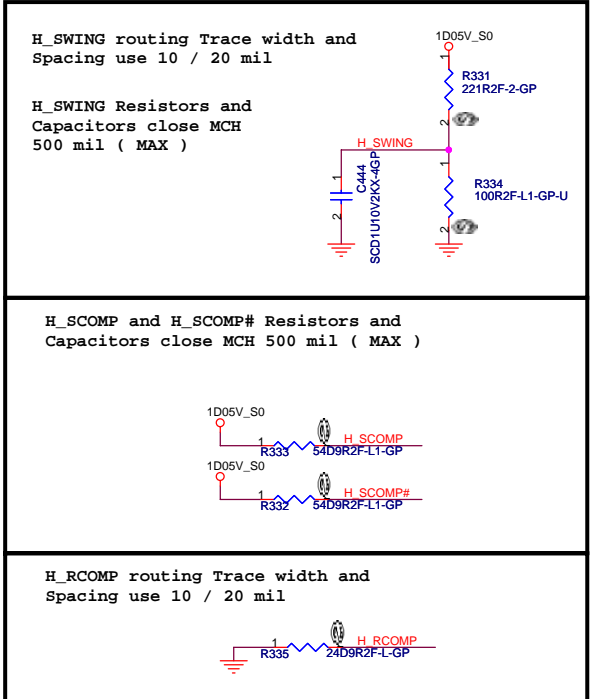
Size: Document Number Rev: -1

Date: Monday, February 26, 2007 Sheet 4 of 45



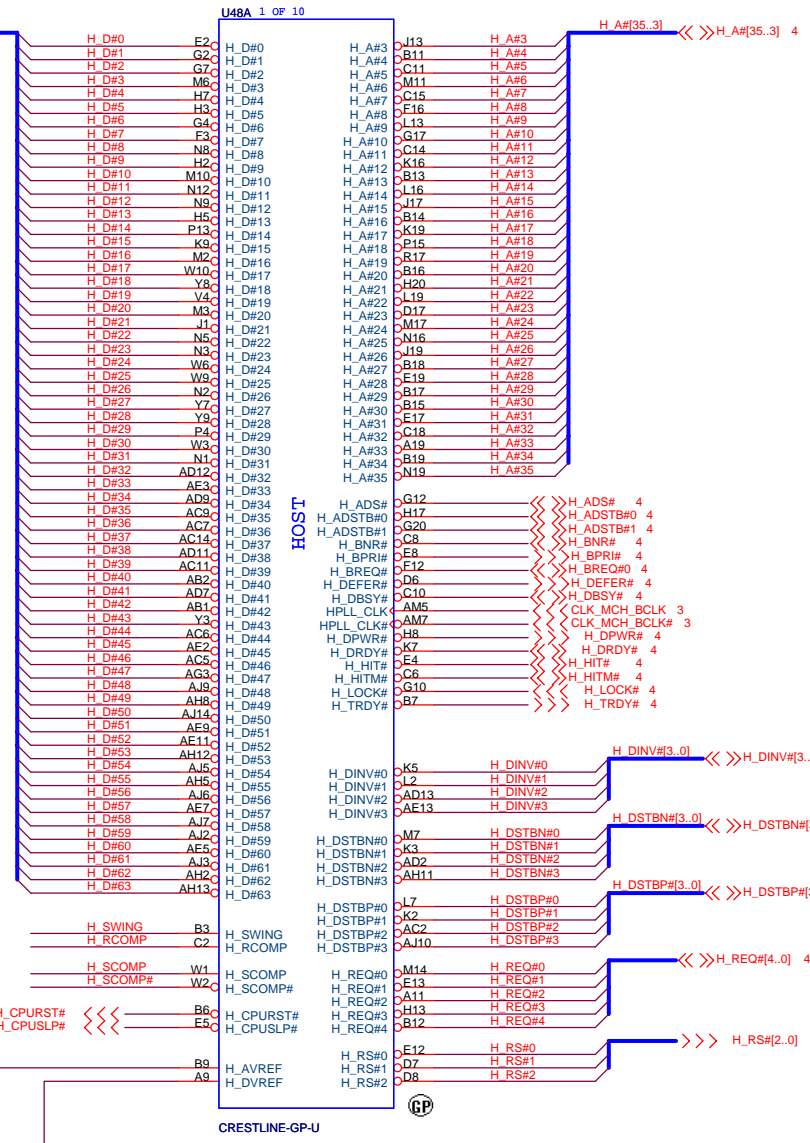
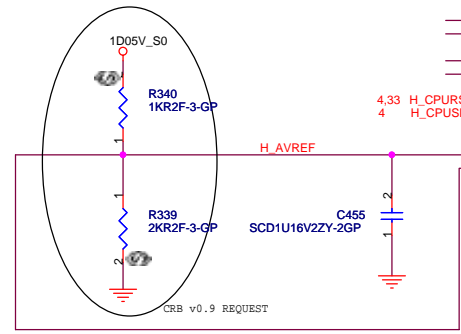
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CPU (2 of 2)			
Size	Document Number	Rev	-1
Date	Monday, February 26, 2007	Sheet	5 of 45



Place them near to the chip (< 0.5")

H_REF Decoupling Crestline close Crestline 100 mil



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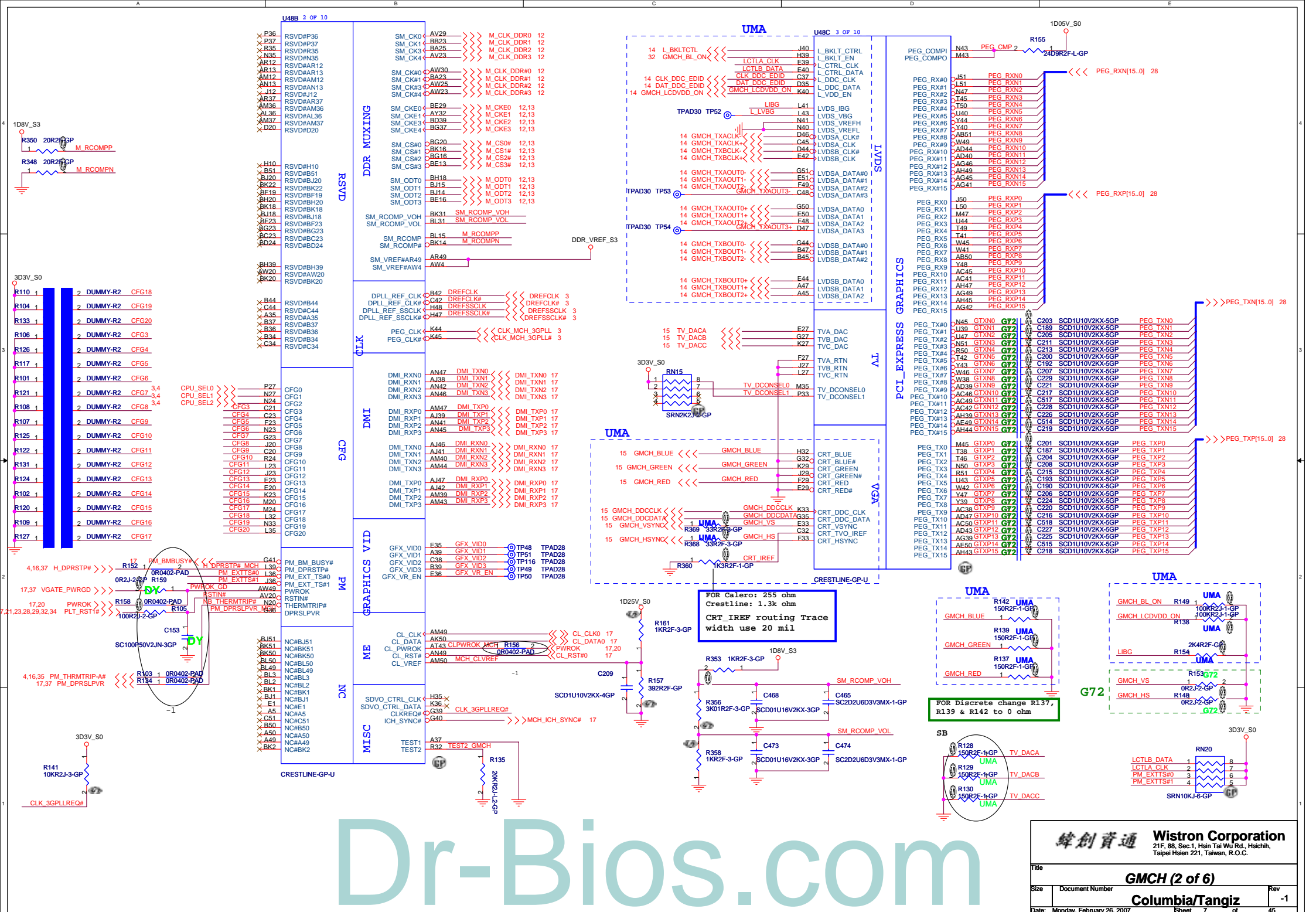
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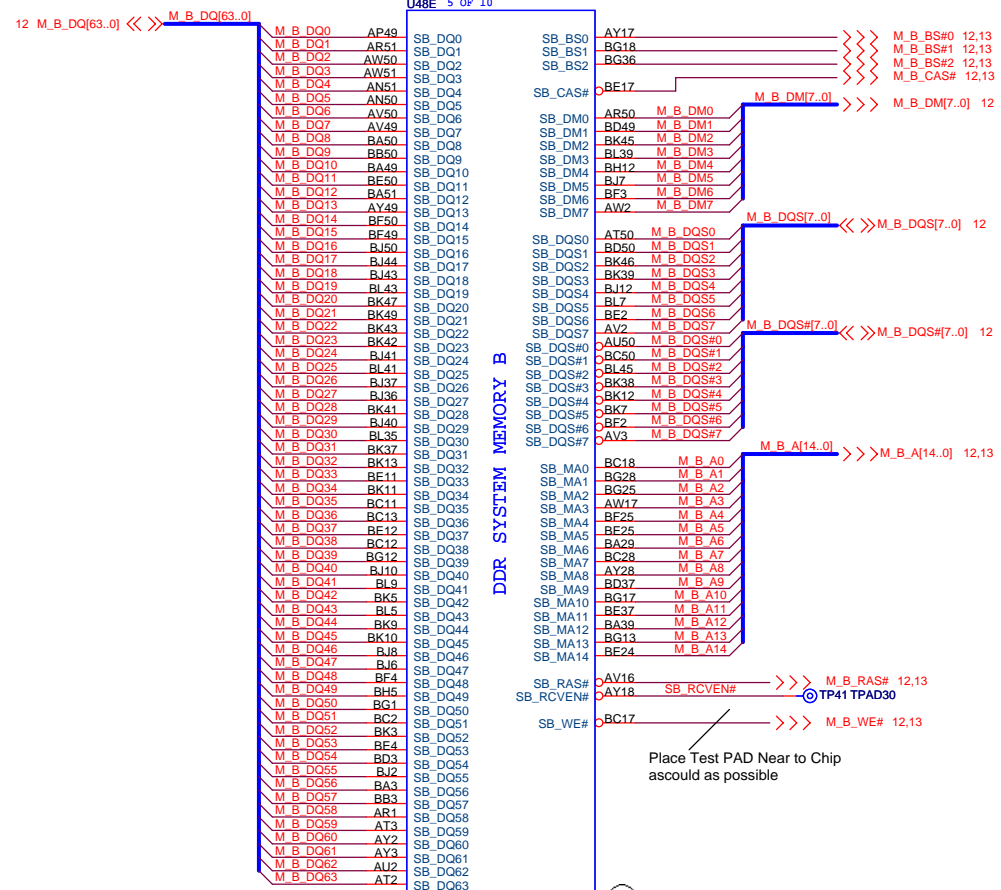
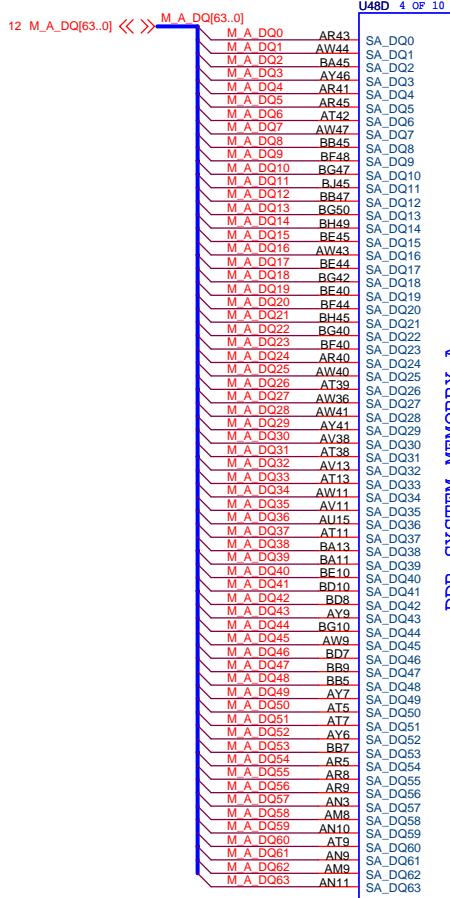


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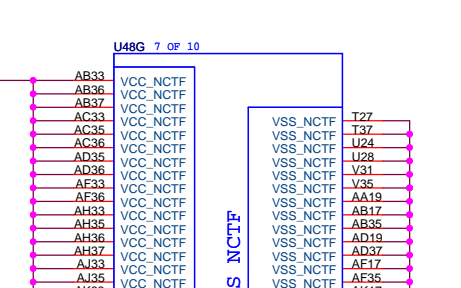
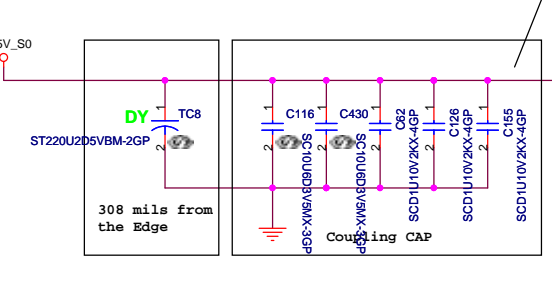
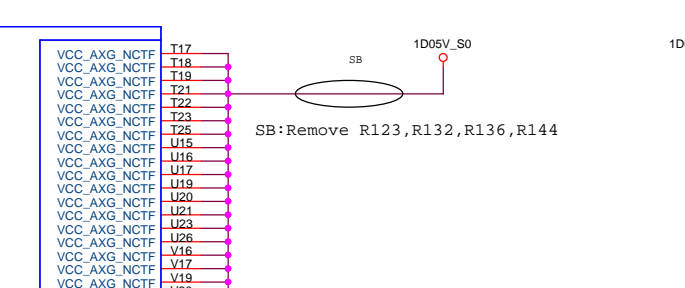
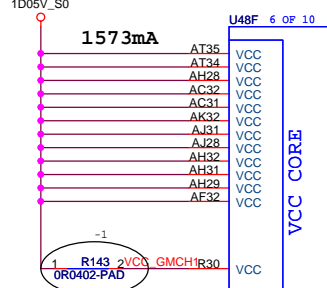
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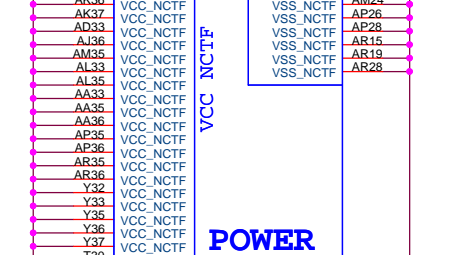
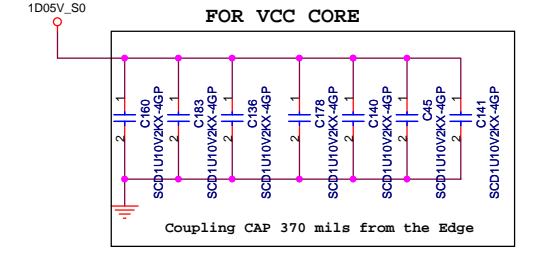
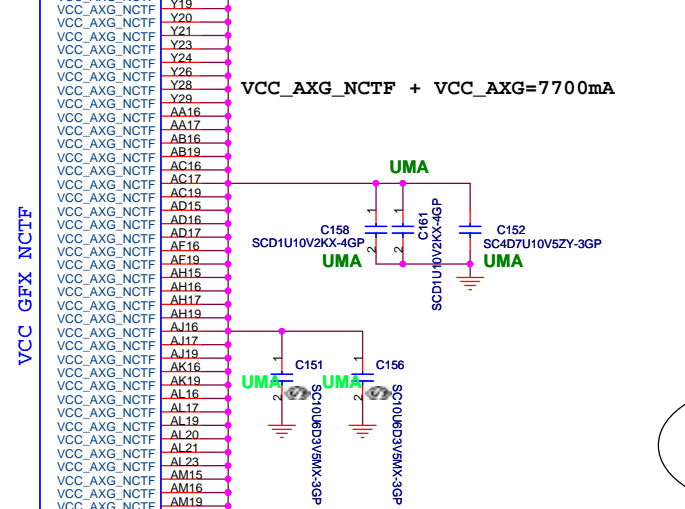
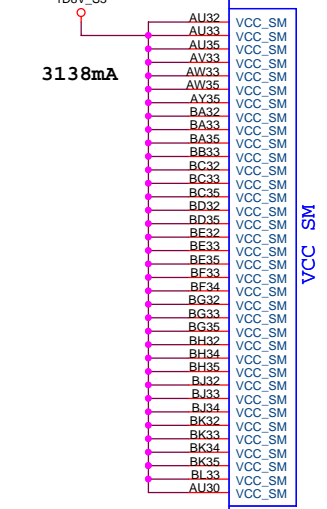
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VCC_NCTF + VCC=1573mA

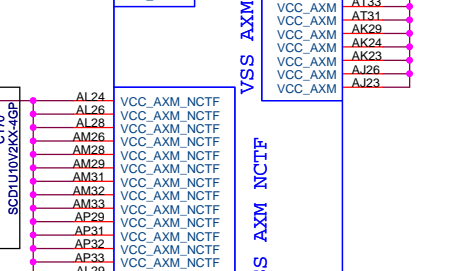
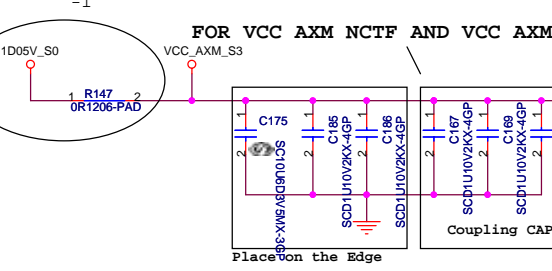
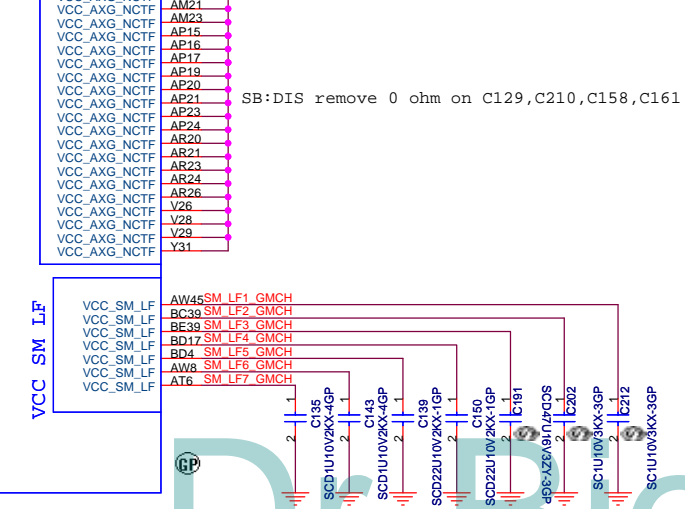
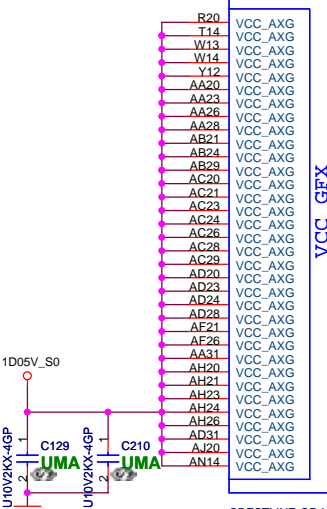
FOR VCC CORE AND VCC NCTF



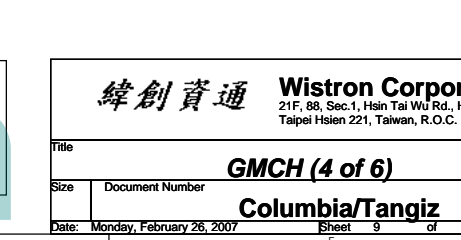
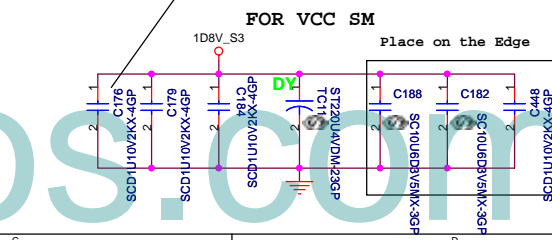
POWER



POWER



VCC_AXM_NCTF + VCC_AXM=540mA



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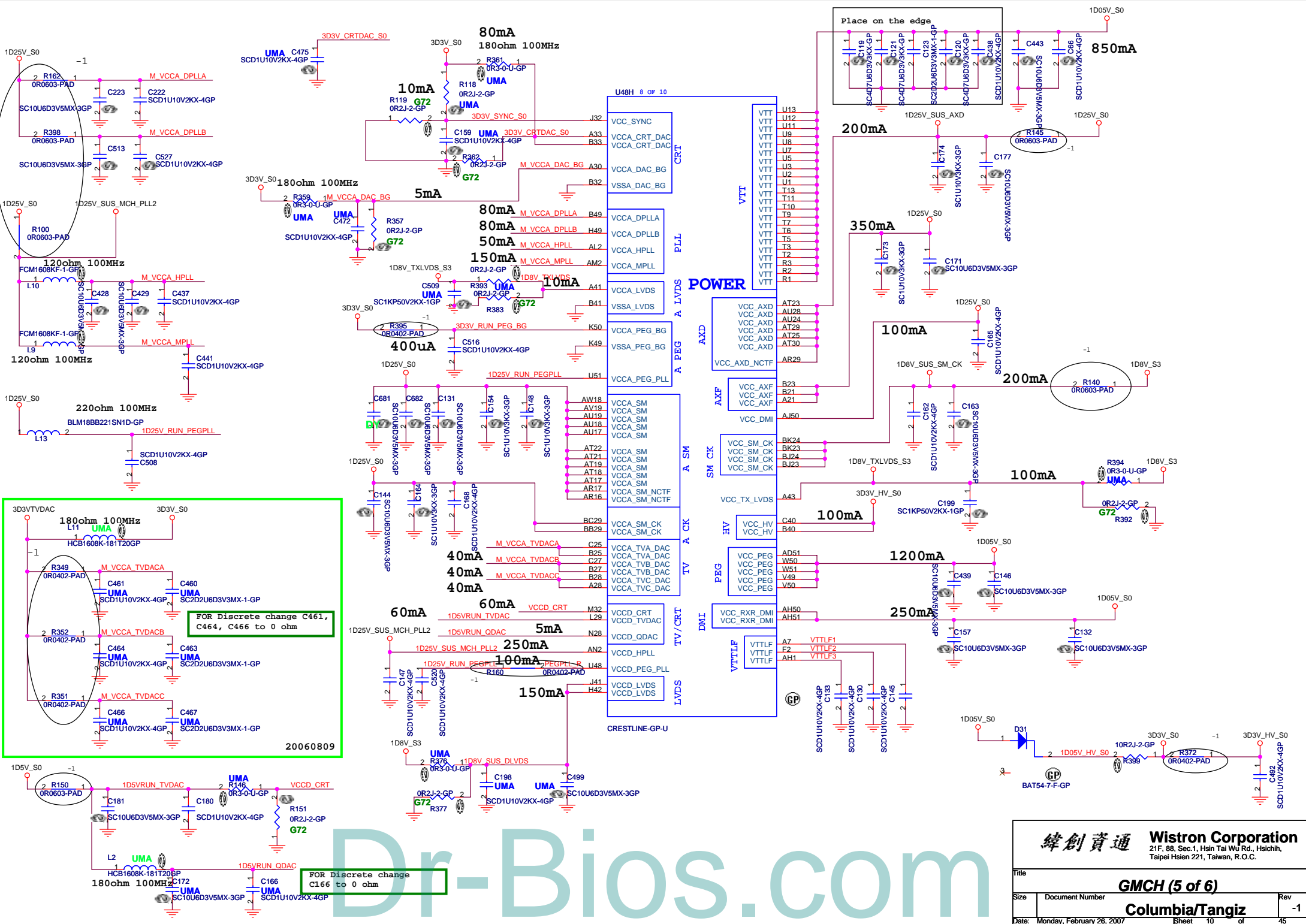
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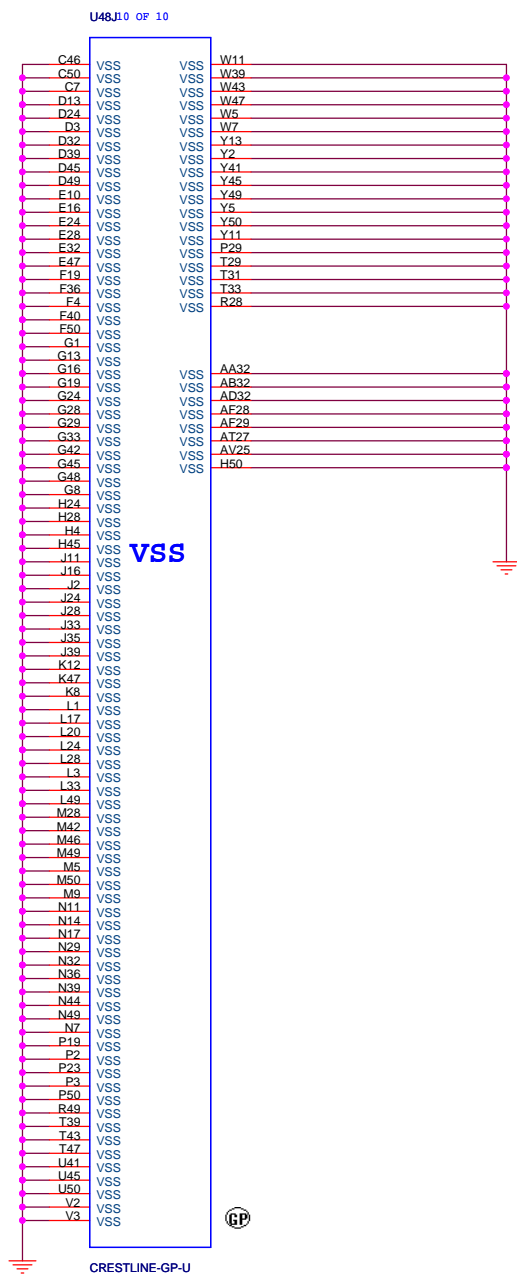
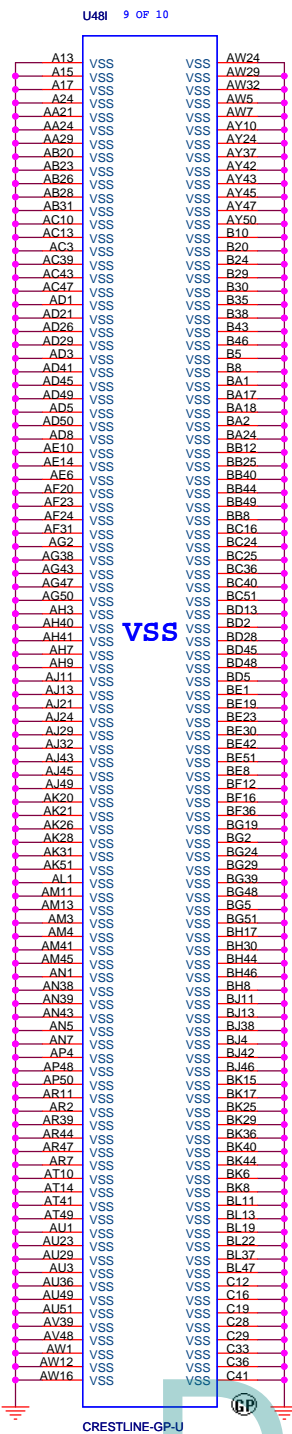
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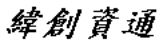
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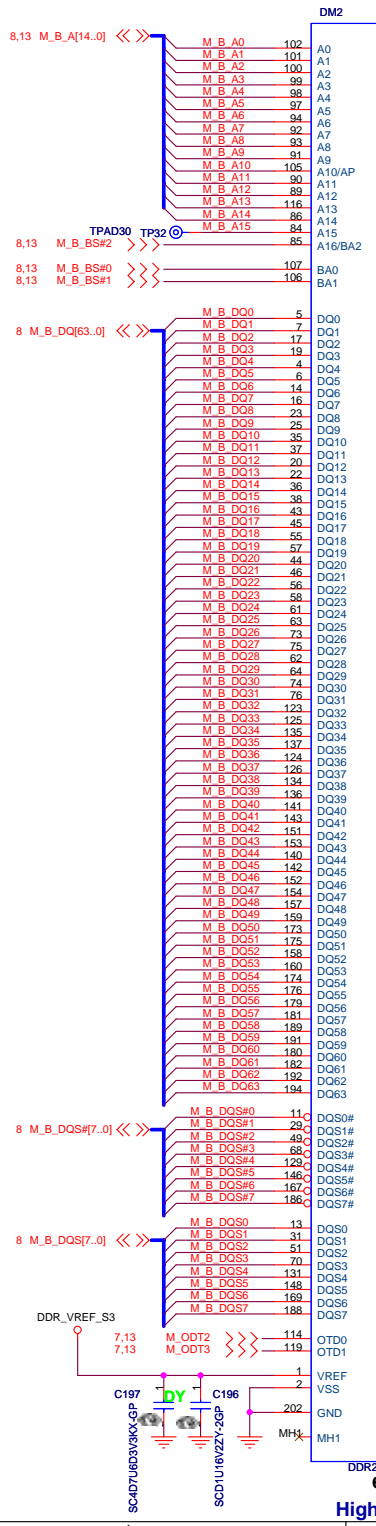
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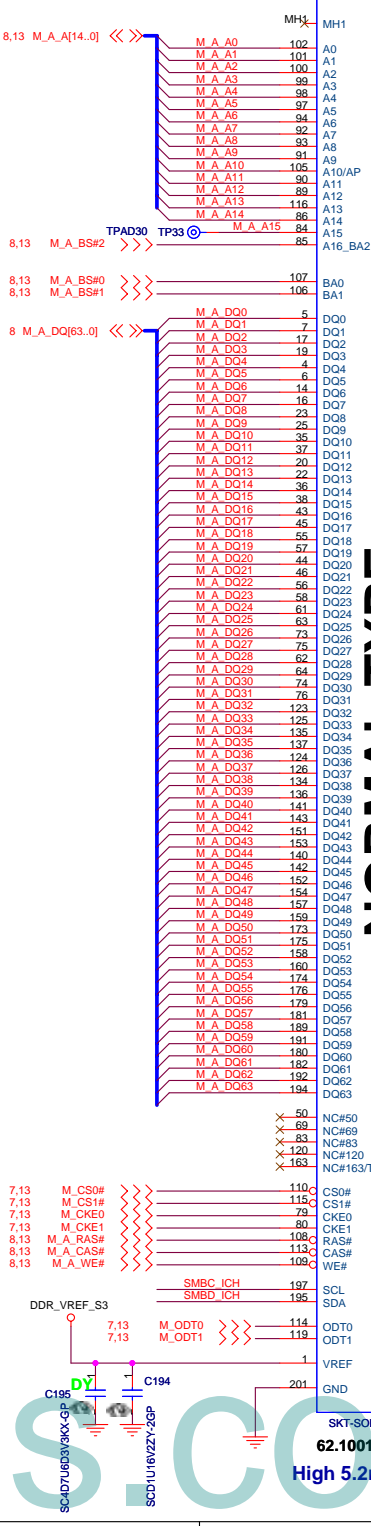
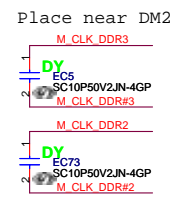
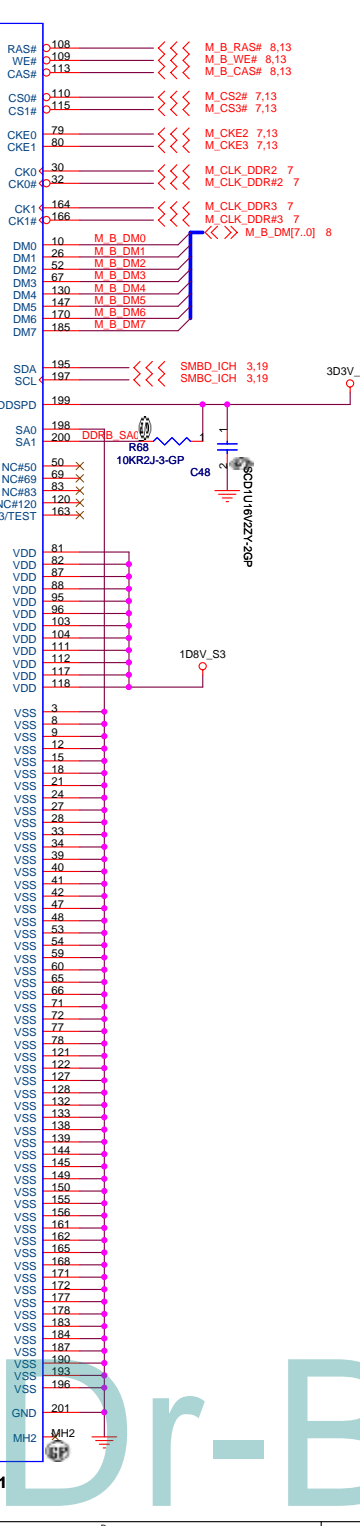


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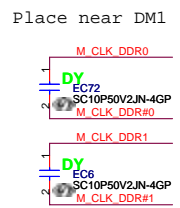
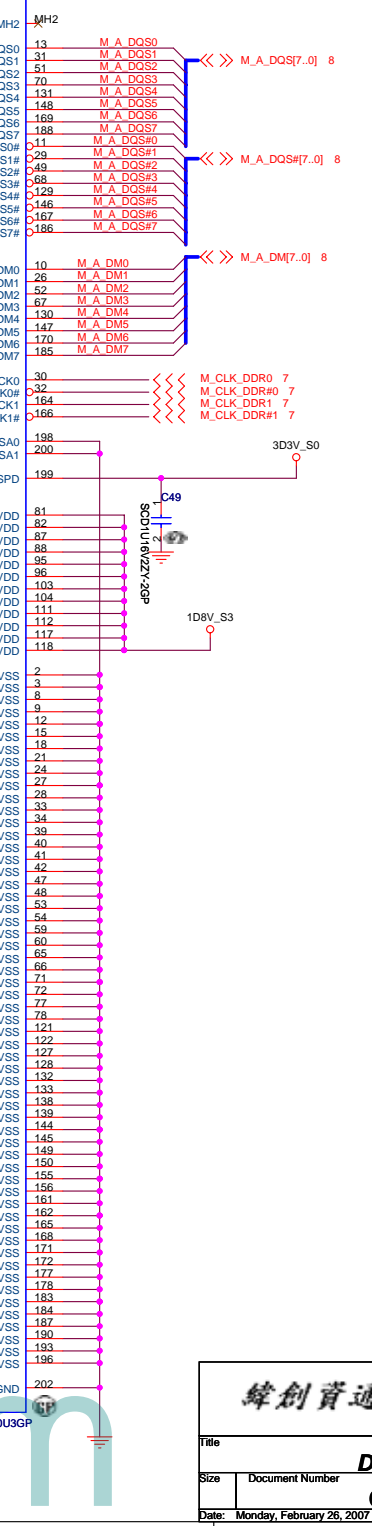
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NORMAL TYPE



NORMAL TYPE



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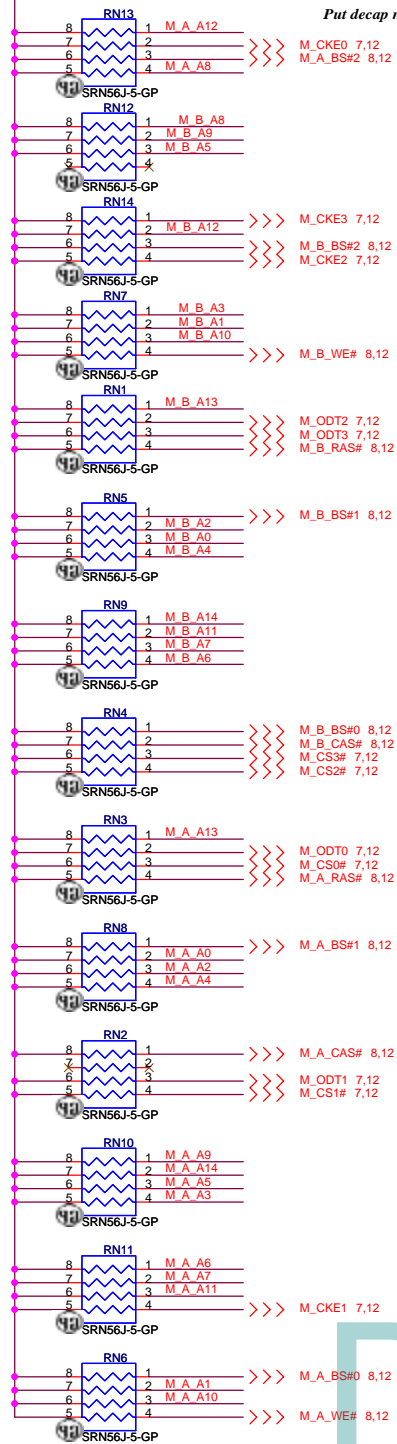
DDR2 Socket
Columbia/Tangiz

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PARALLEL TERMINATION

DDR_VREF_S0

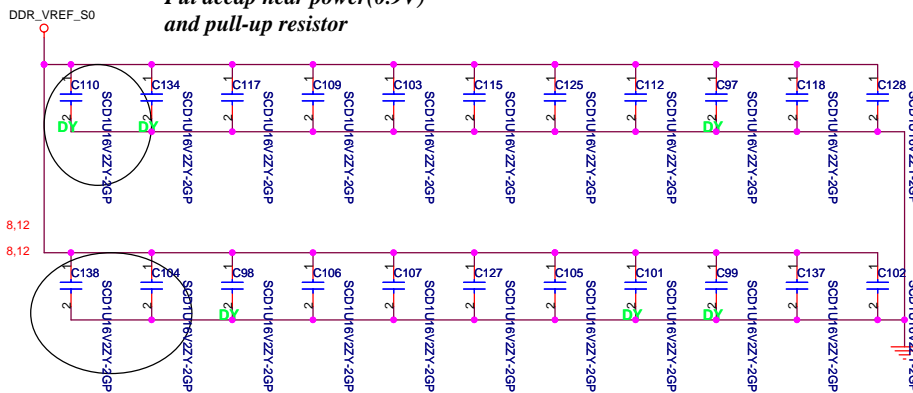
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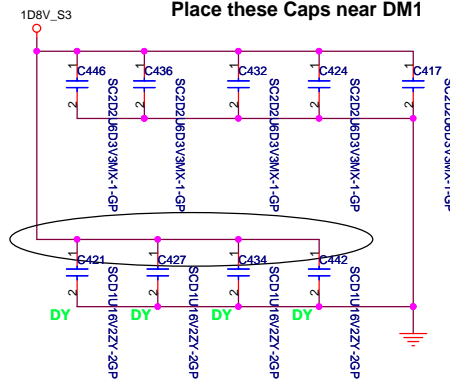
M_A_A[14..0] <<< M_A_A[14..0] 8,12
M_B_A[14..0] <<< M_B_A[14..0] 8,12

Decoupling Capacitor

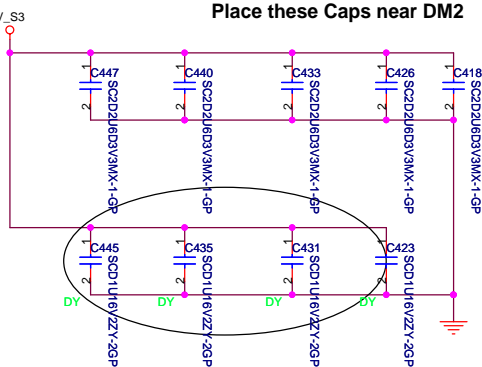
Put decap near power(0.9V) and pull-up resistor



Place these Caps near DM1



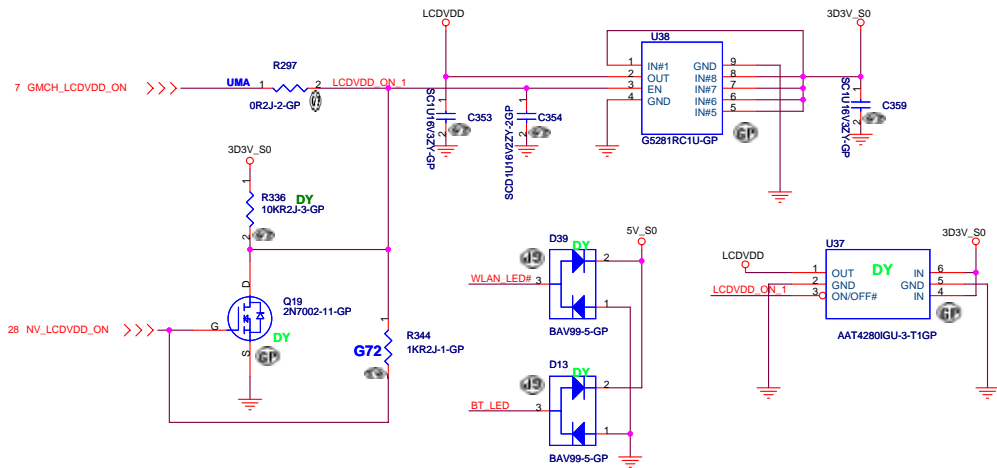
Place these Caps near DM2



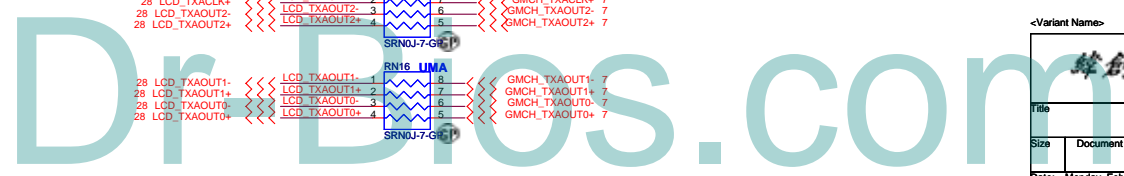
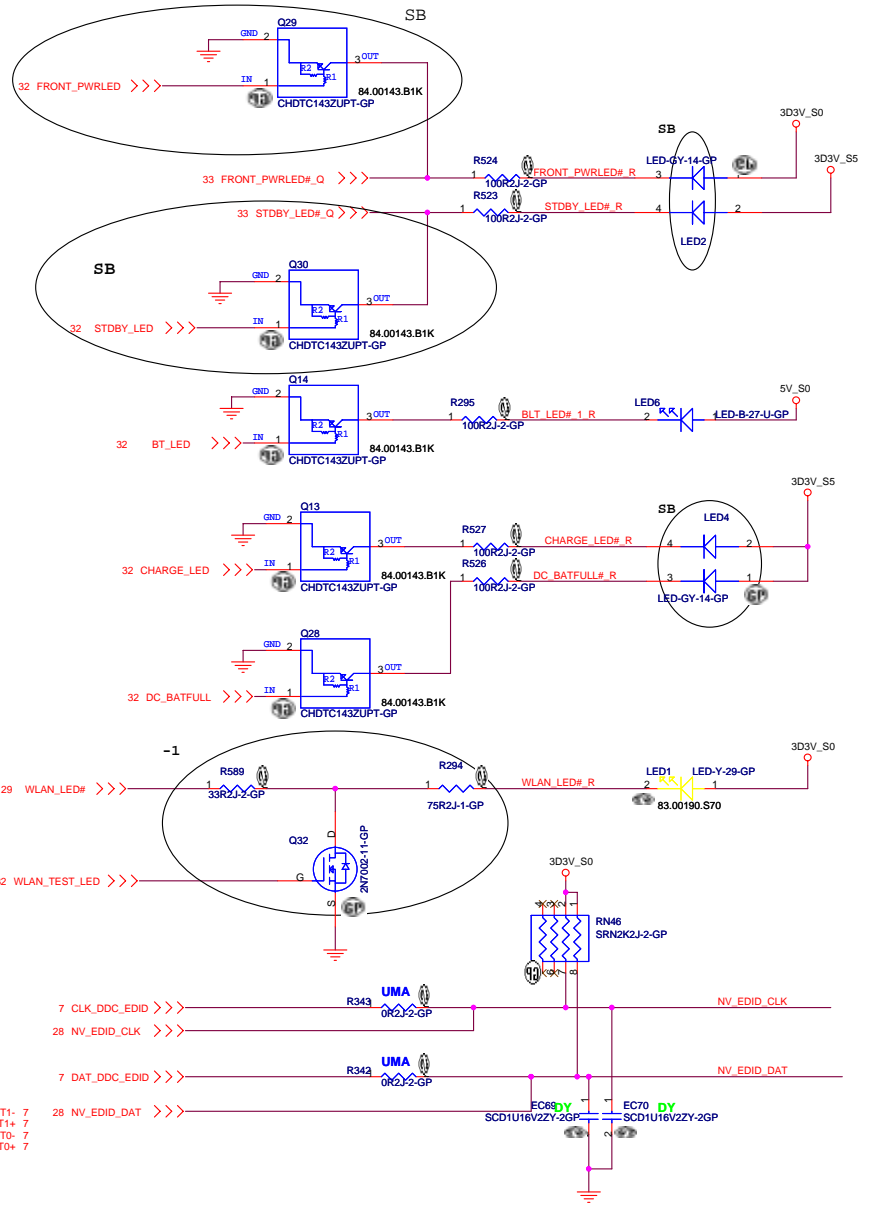
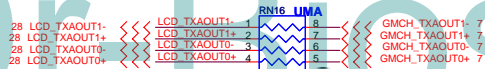
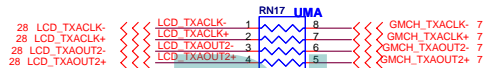
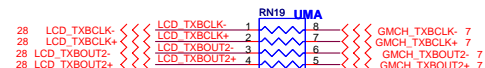
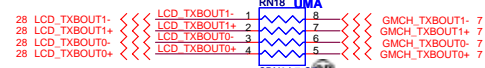
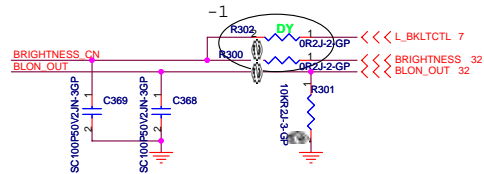
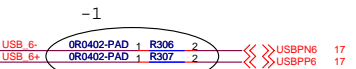
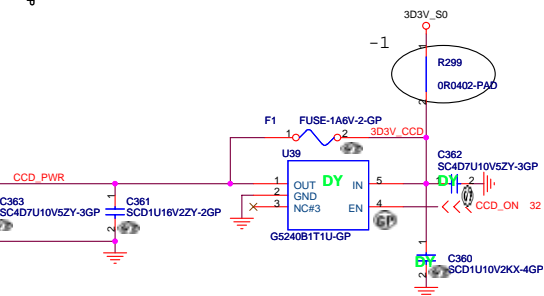
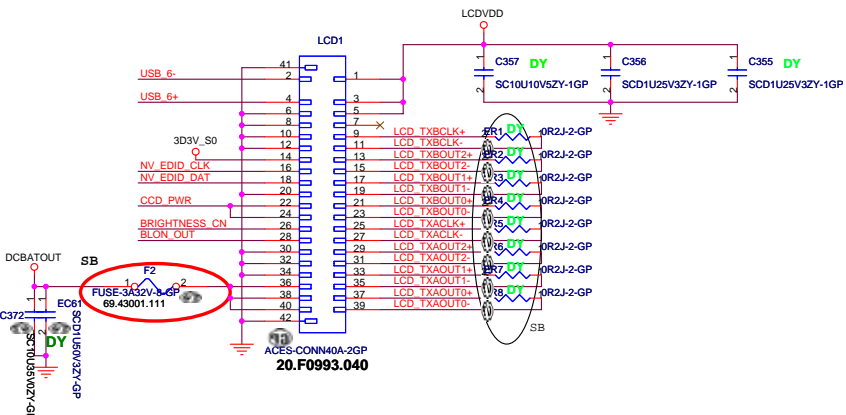
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LCD/INVERTER CONN



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LCD CONN & LED

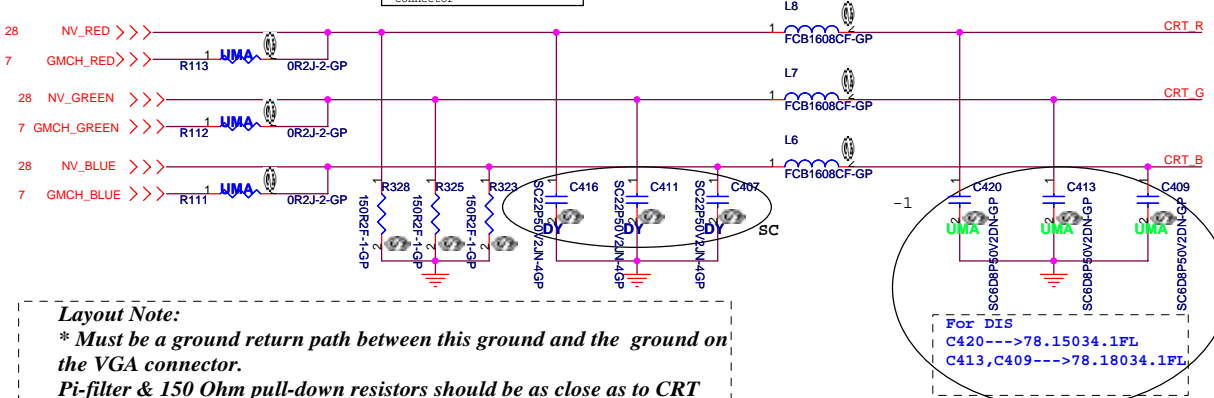
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Rev -1

CRT I/F & CONNECTOR

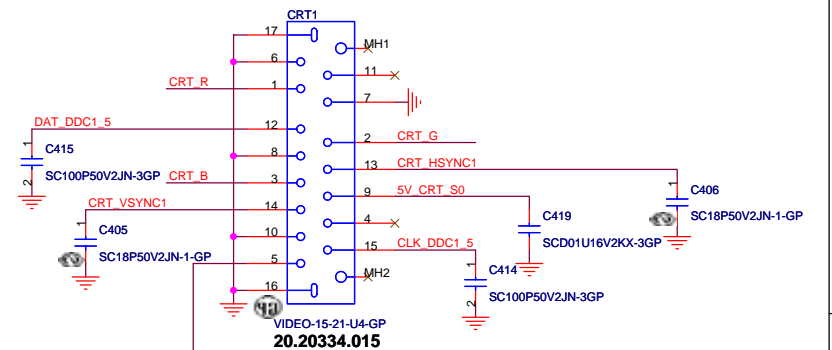
Layout Note:
Place these resistors close to the CRT-out connector

Ferrite bead impedance: 10 ohm@100MHz

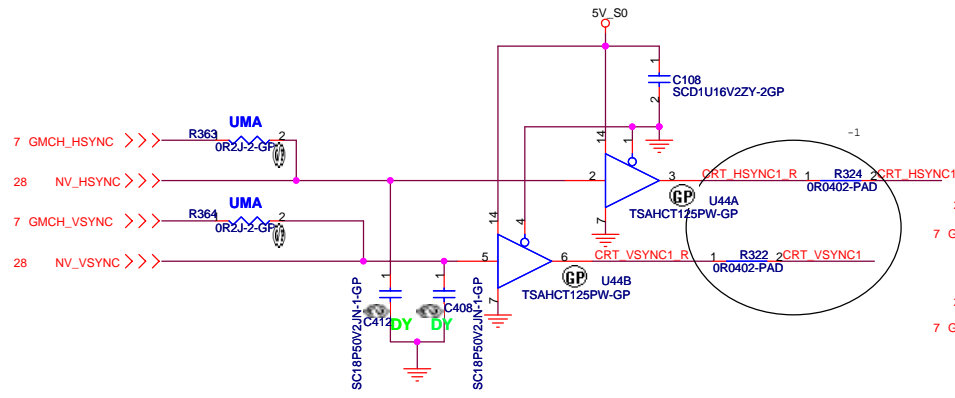


Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

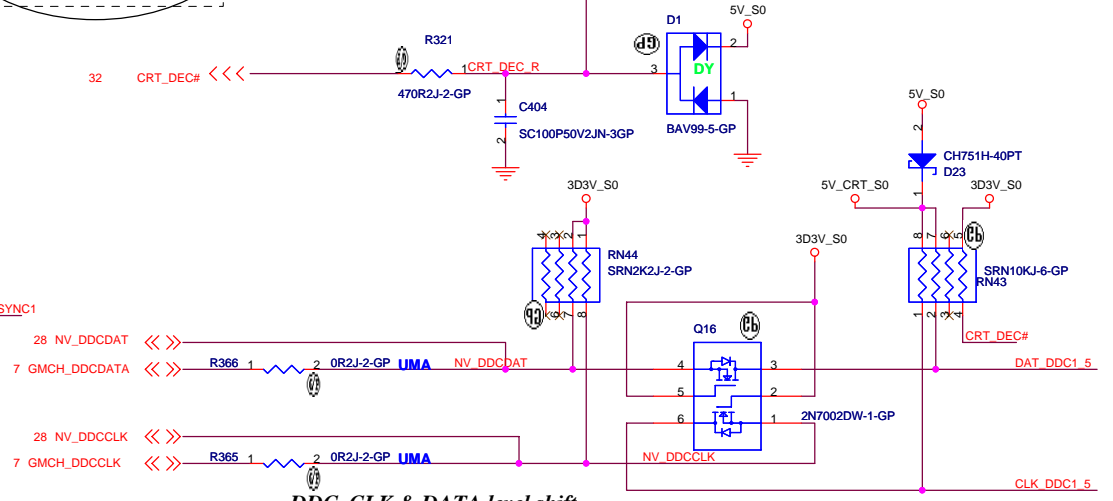
For DIS
C420--->78.15034.1FL
C413,C409--->78.18034.1FL



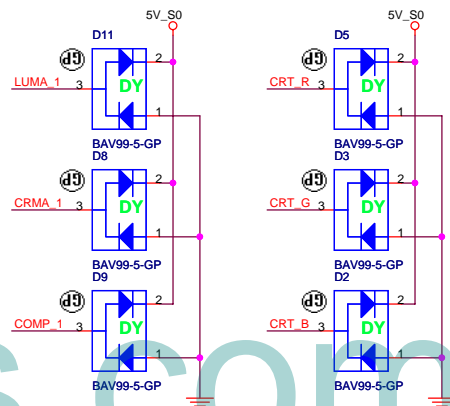
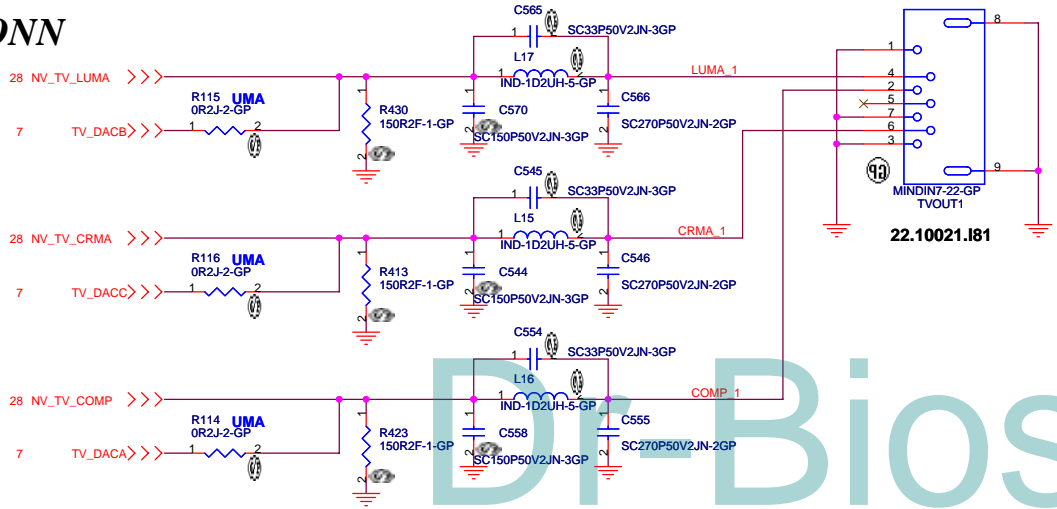
Hsync & Vsync level shift



DDC_CLK & DATA level shift



TV CONN

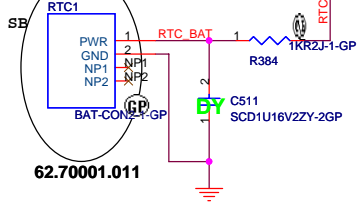


緯創資通 Wistron Corporation
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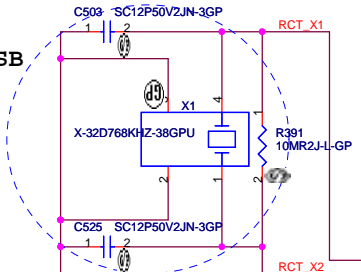
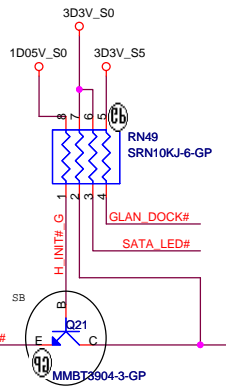
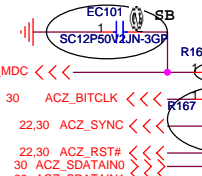
Title		CRT/TV Connector	
Size	Document Number	Rev	
Date: Monday, February 26, 2007		Sheet	15 of 45

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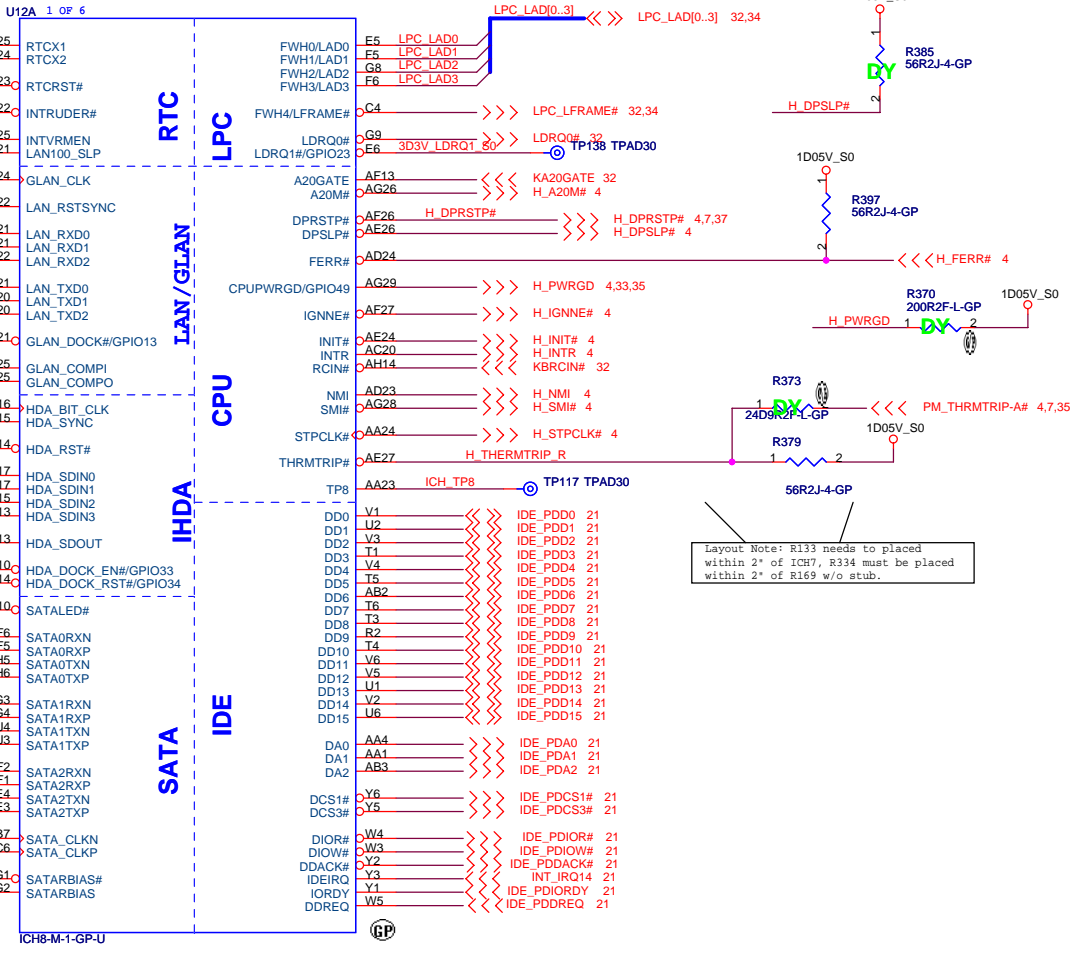
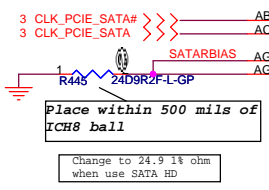
RTC circuitry



GLAN_COMP place within 500 mil of ICH8M



- 22 ACZ_BTCLK_MDC <<<
- 30 ACZ_BITCLK <<<
- 22.30 ACZ_SYNC <<<
- 22.30 ACZ_RST# <<<
- 30 ACZ_SDATAIN0 <<<
- 22 ACZ_SDATAIN1 <<<
- 22.30 ACZ_SDATAOUT <<<
- TPAD30 TP124 <<<
- TPAD30 TP130 <<<
- TPAD30 TP132 <<<
- TPAD30 TP133 <<<
- 33 SATA_LED# <<<
- 21 SATA_RXN0 >>>
- 21 SATA_RXP0 >>>
- 21 SATA_TXN0 >>>
- 21 SATA_TXP0 >>>
- 21 SATA_RXN1 >>>
- 21 SATA_RXP1 >>>
- 21 SATA_TXN1 >>>
- 21 SATA_TXP1 >>>



Layout Note: R133 needs to be placed within 2" of ICH7, R334 must be placed within 2" of R169 w/o stub.

Integrated VccSus1_05, VccSus1_5, VccCLL1_5		
INTVRMEN	High=Enable	Low=Disable
Integrated VccLan1_05VccCLL1_05		
LAN100_SLP	High=Enable	Low=Disable

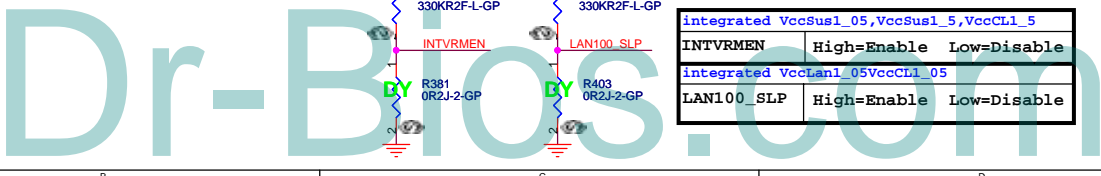
UMA

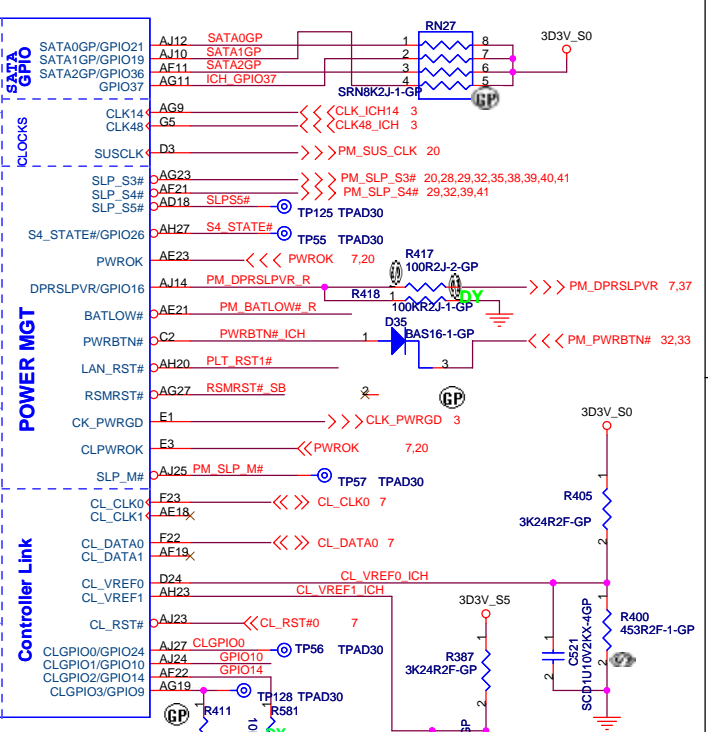
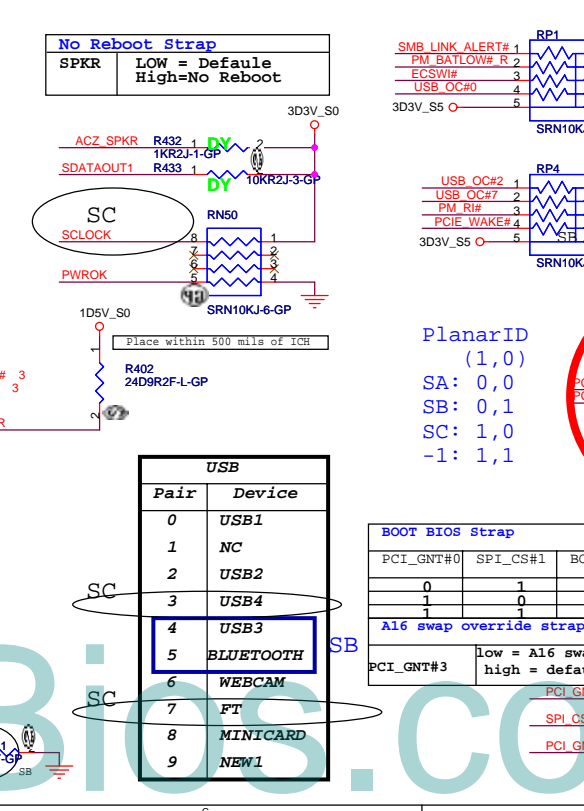
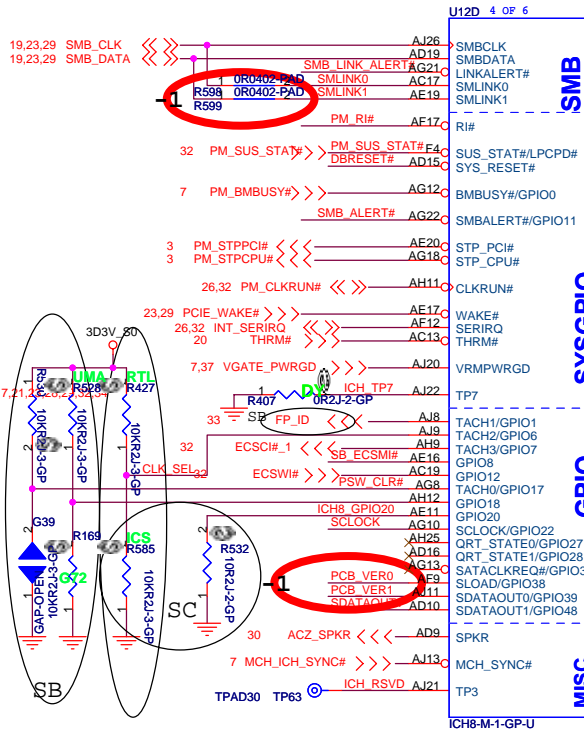
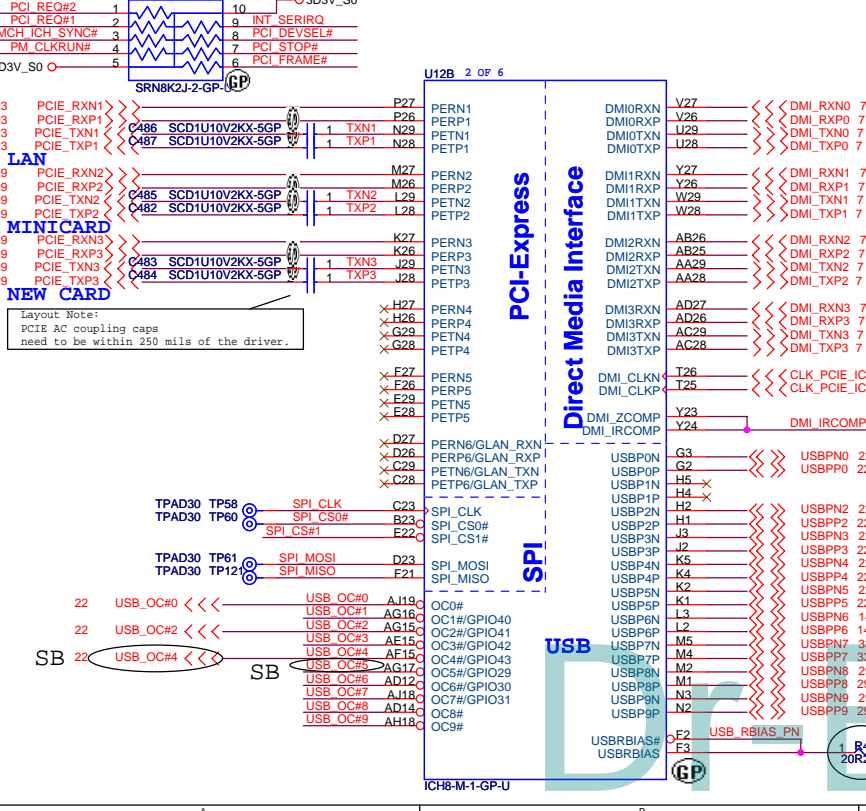
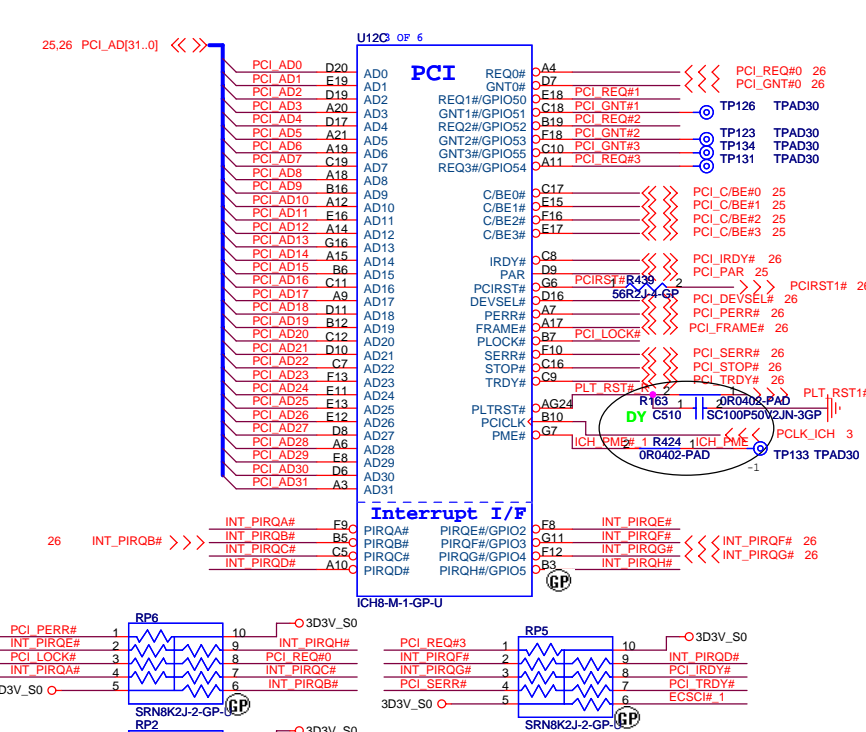
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **ICH8-M (1 of 4)**

Size: Document Number: Columbia/Tangiz Rev: -1

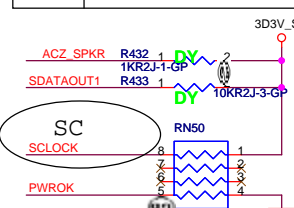
Date: Monday, February 26, 2007 Sheet 16 of 45





No Reboot Strap

SPKR LOW = Default High = No Reboot



Pair	Device
0	USB1
1	NC
2	USB2
3	USB4
4	USB3
5	BLUETOOTH
6	WEBCAM
7	FT
8	MINICARD
9	NEW1

PlanarID

(1, 0)
SA: 0, 0
SB: 0, 1
SC: 1, 0
-1: 1, 1

PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPT
1	0	PCT
1	1	LPC(Default)

A16 swap override strap

Low = A16 swap override enable
high = default

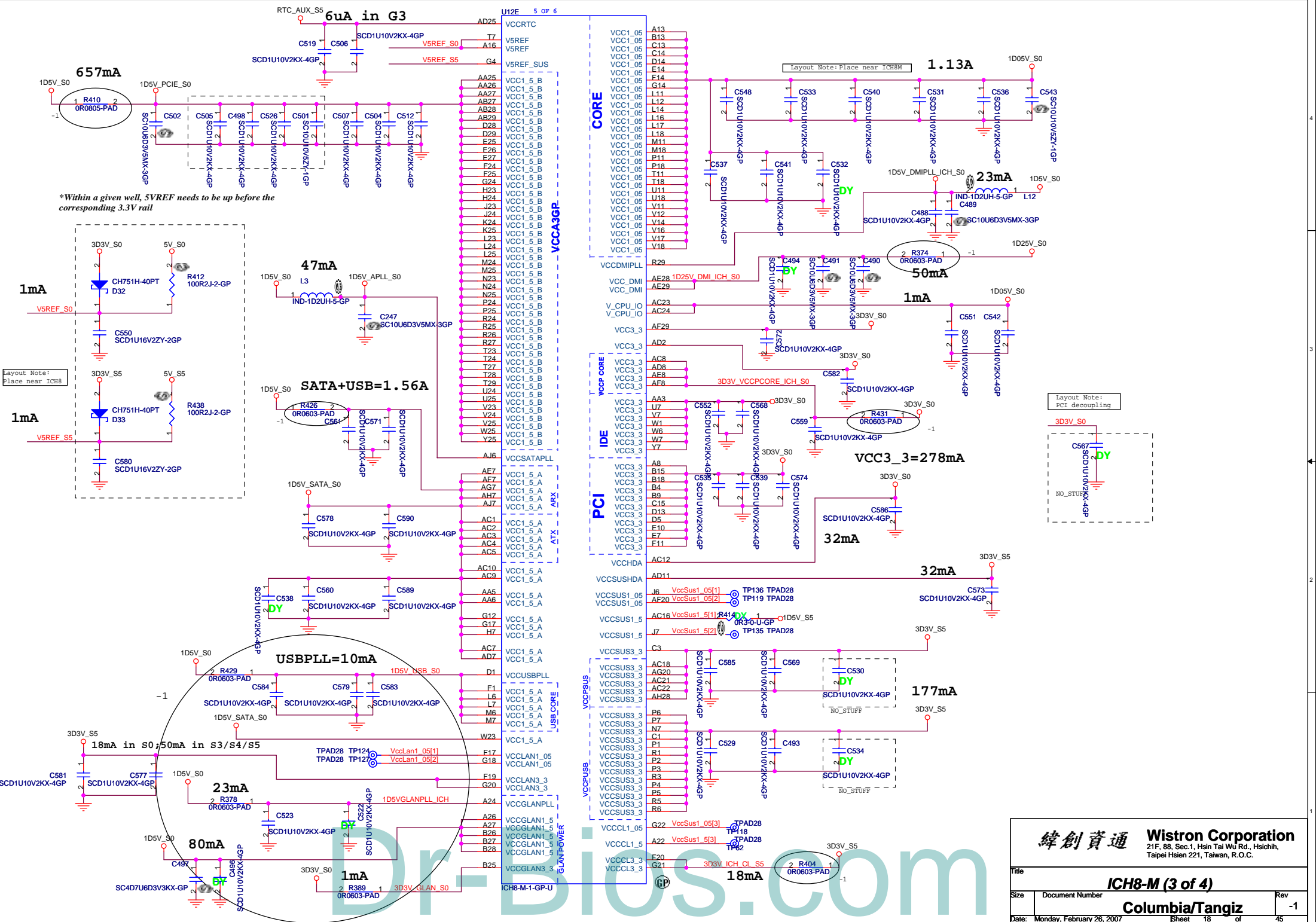
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

ICH8-M (2 of 4)

File: **ICH8-M (2 of 4)**

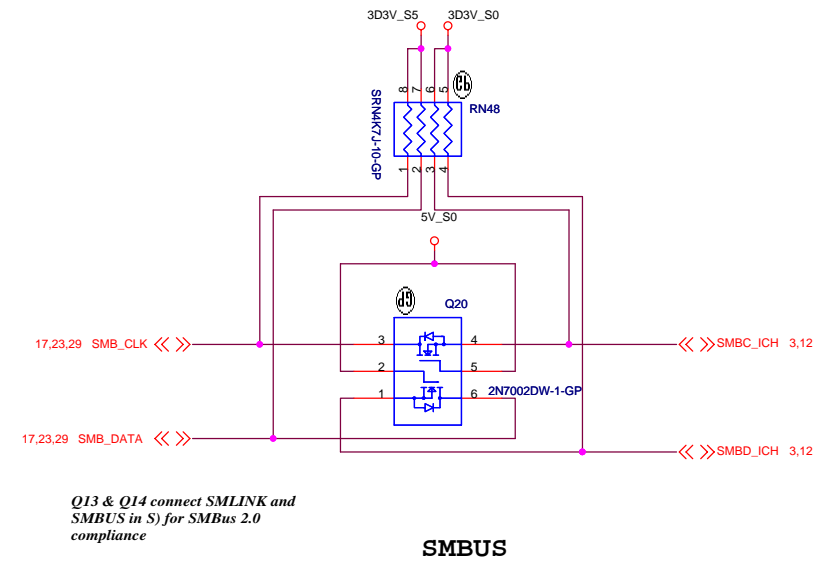
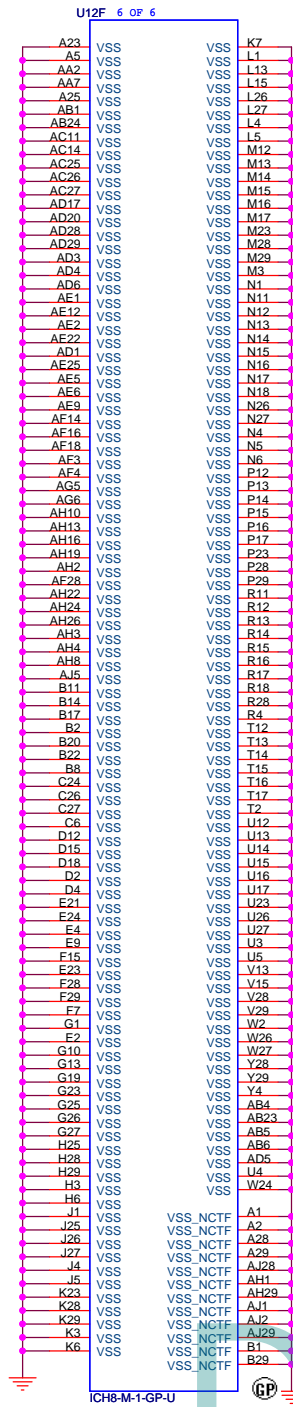
Size: **Columbia/Tangiz** Rev: **-1**

Date: Monday, February 26, 2007 Sheet: 17 of 45



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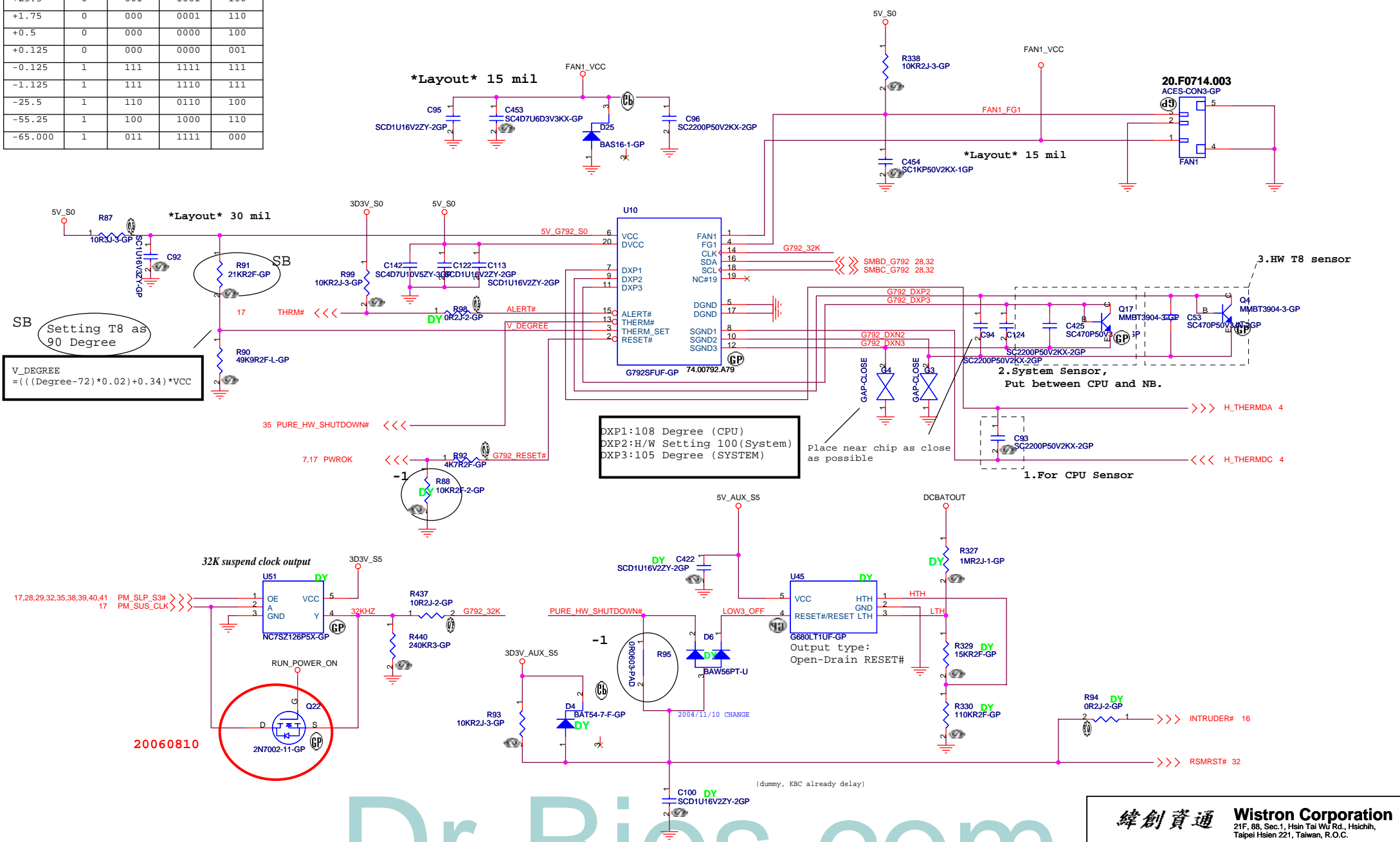
Title		ICH8-M (3 of 4)
Size	Document Number	Rev
Columbia/Tangiz		-1
Date: Monday, February 26, 2007	Sheet 18 of 45	



Q13 & Q14 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

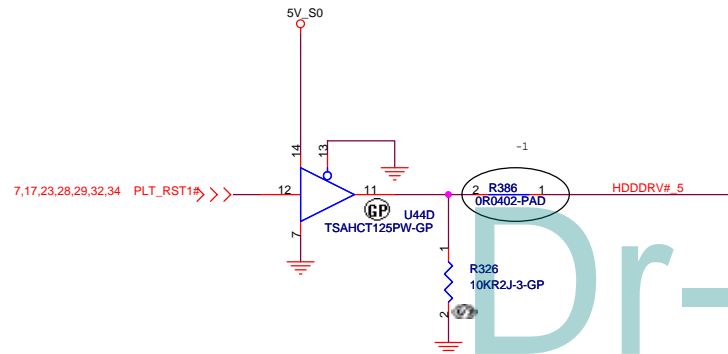
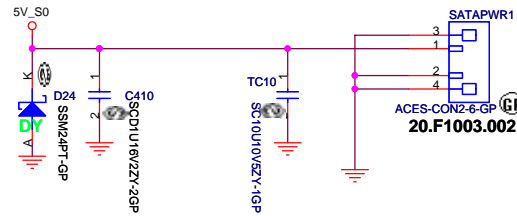
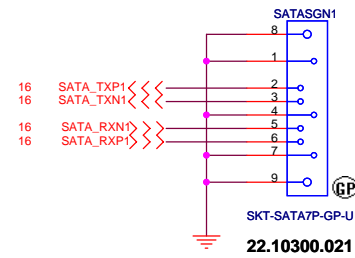
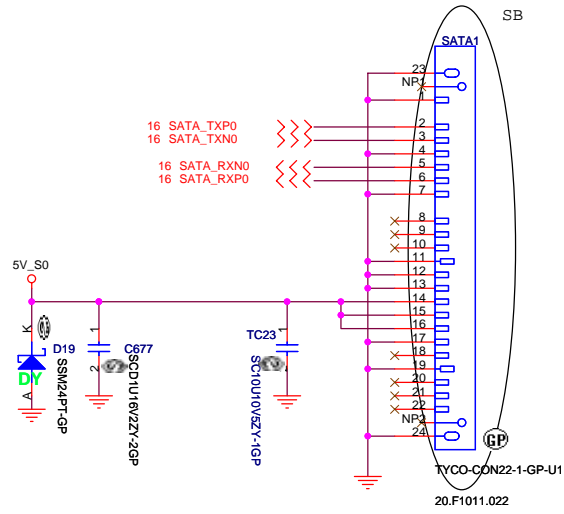


TEMP.	Digital Output Data Bits			
	Sign	MSB	LSB	EXT
+127.875	0	111	1111	111
+126.375	0	111	1110	011
+25.5	0	001	1001	100
+1.75	0	000	0001	110
+0.5	0	000	0000	100
+0.125	0	000	0000	001
-0.125	1	111	1111	111
-1.125	1	111	1110	111
-25.5	1	110	0110	100
-55.25	1	100	1000	110
-65.000	1	011	1111	000

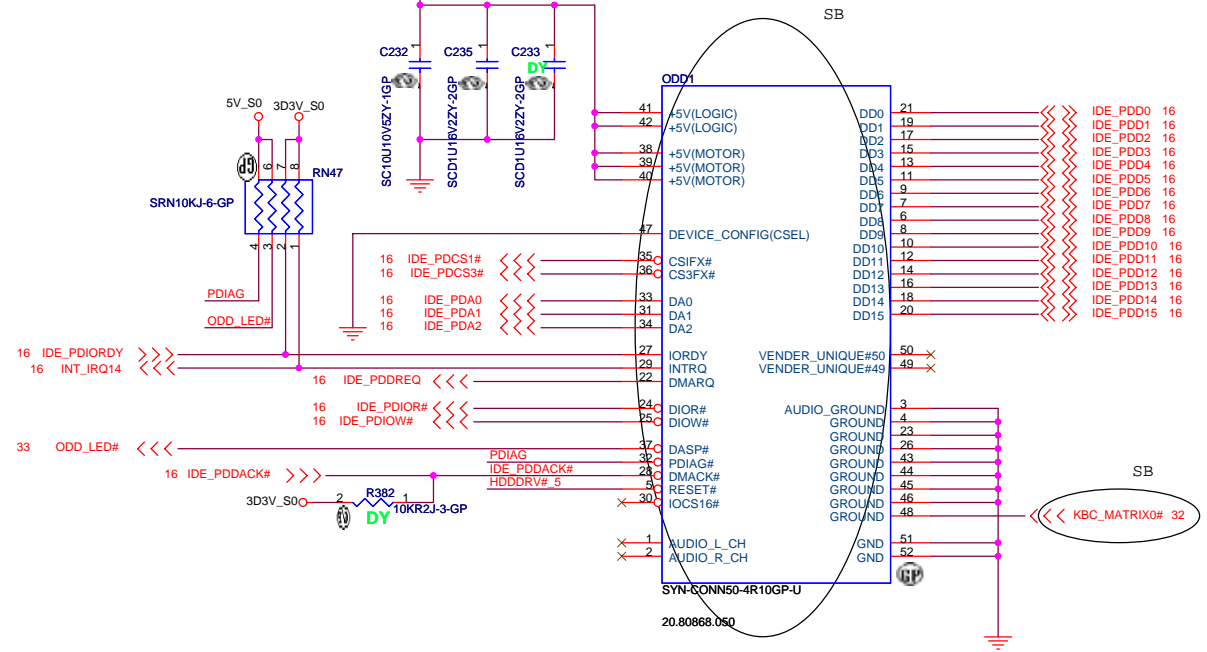


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SATA HD Connector



ODD Connector



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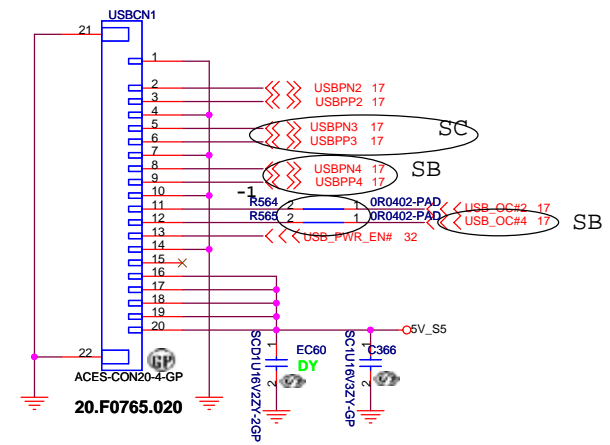
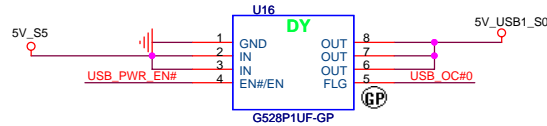
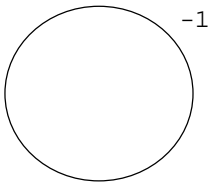
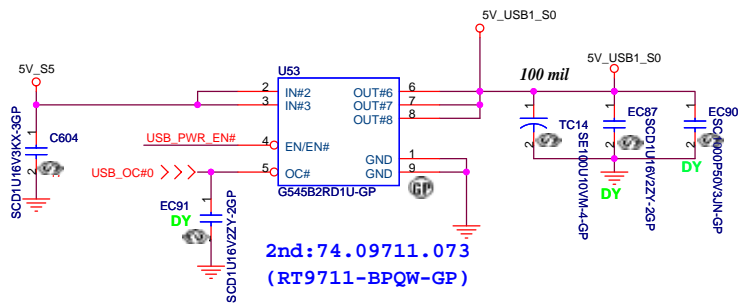
bom1

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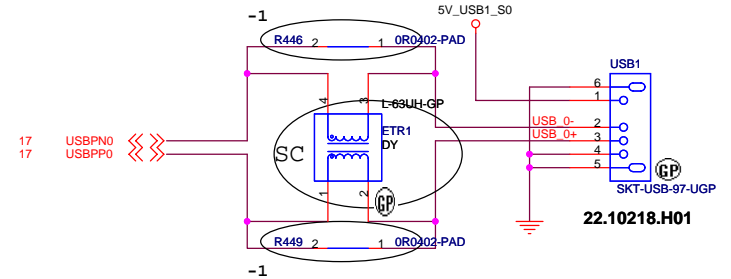
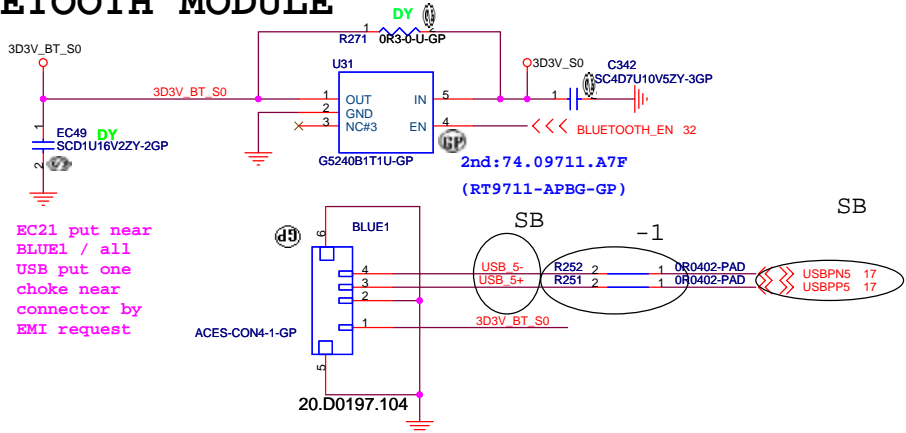
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Size: Document Number **Columbia/Tangiz** Rev: -1

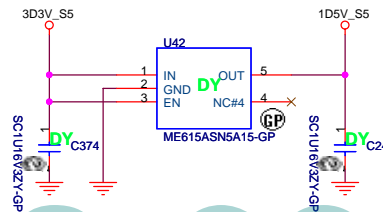
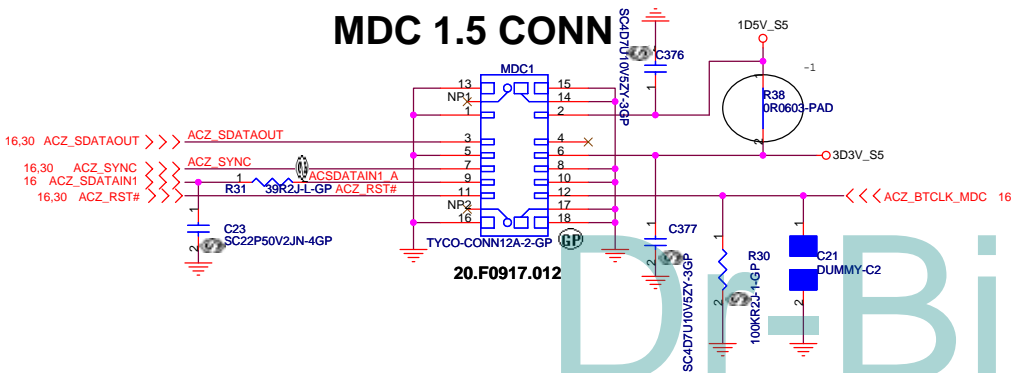
Date: Monday, February 26, 2007 Sheet 21 of 45



BLUETOOTH MODULE



MDC 1.5 CONN

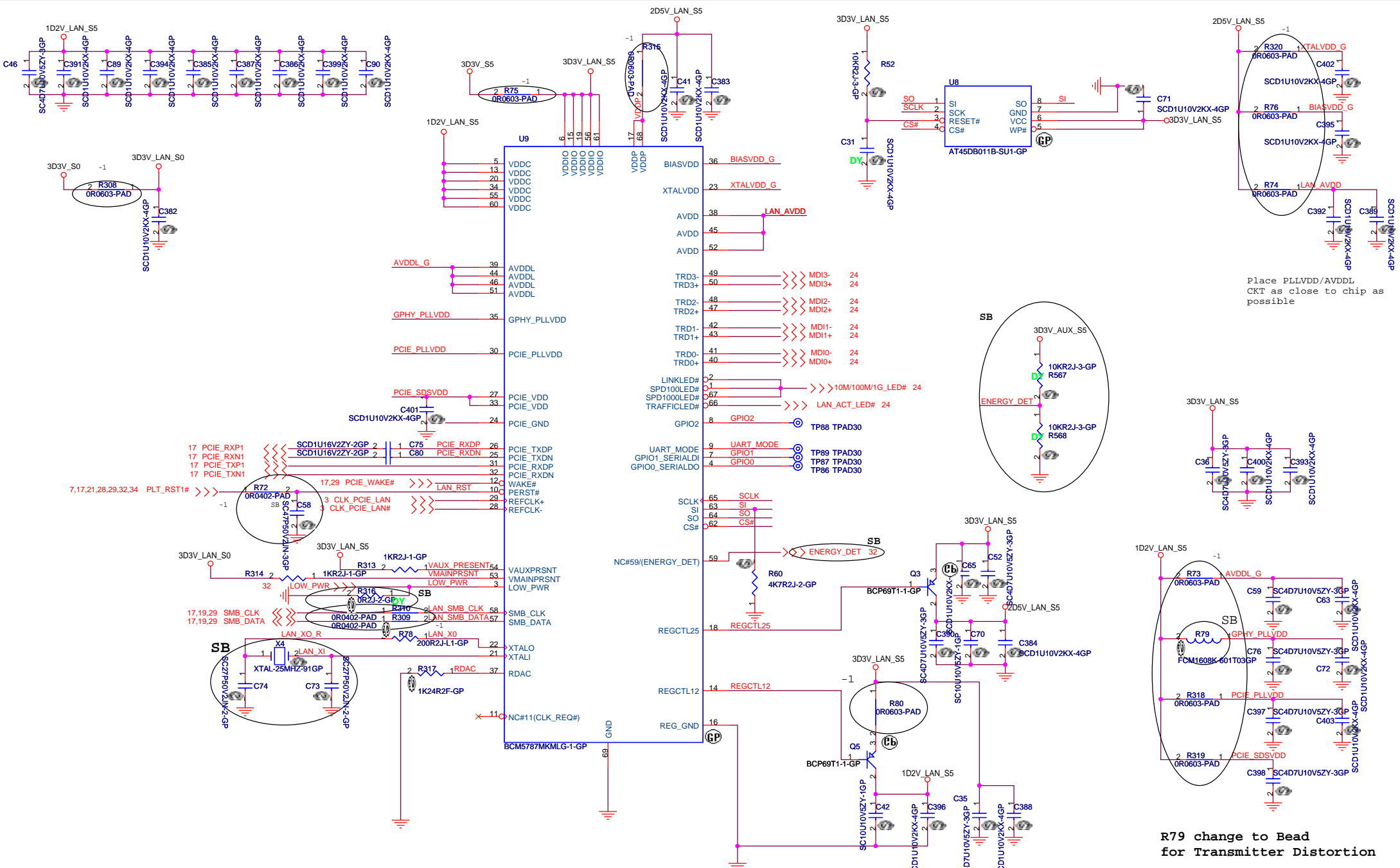


bom1

緯創資通 Wistron Corporation
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File			USB / MDC / BLUETOOTH	
Size	Document Number		Rev	
			-1	
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Di-Bios.com



Place PLLVDD/AVDDL
CKT as close to chip as
possible

R79 change to Bead
for Transmitter Distortion

Dr-Bios.com

<Variant Name>

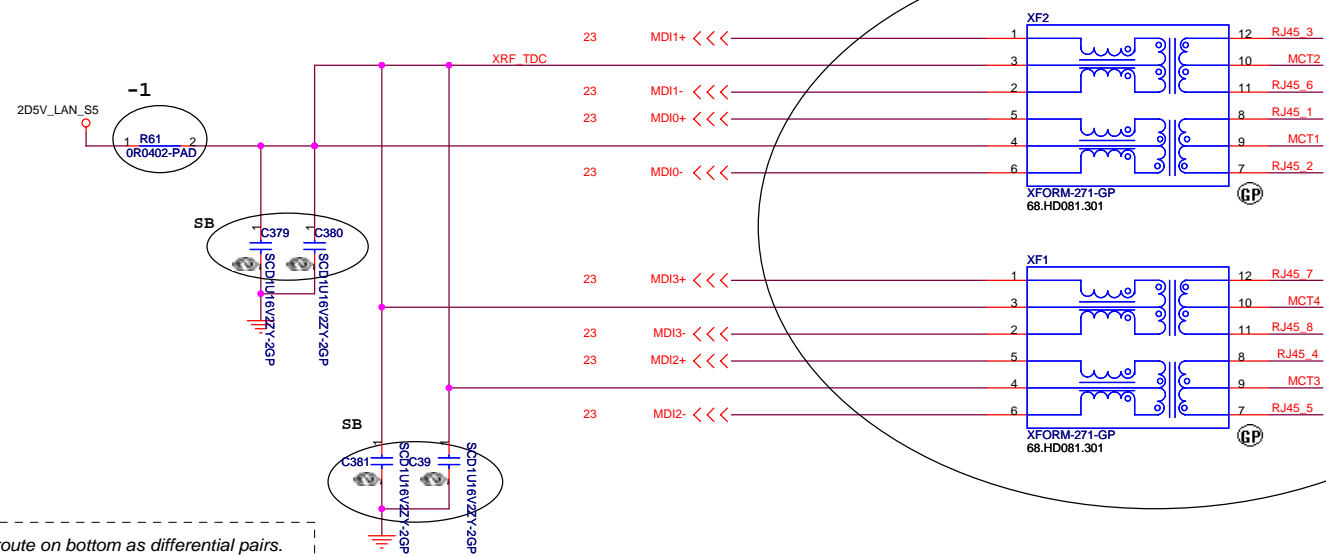
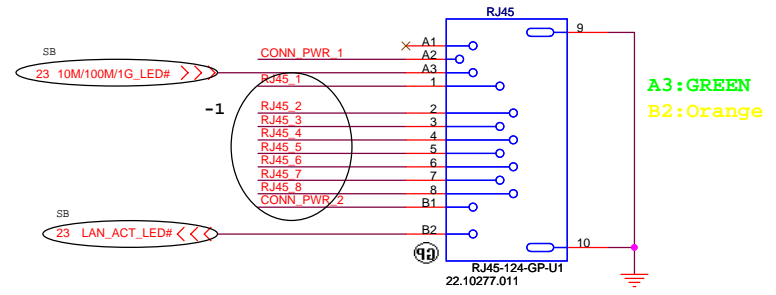
緯創資通 **Wistron Corporation**
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Taipei Hsein 221, Taiwan, R.O.C.

Title BCM5787MKMLG		
Size A3	Document Number Columbia/Tangiz	Rev -1
Date: Monday, February 26, 2007 Sheet 23 of 45		

LAN Connector

Voltage Rail	4401E	5789	5787
VDDIO_PCI	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDC	1D8V_LAN_S5	1D2V_LAN_S5	
VDDIO	3D3V_LAN_S5	3D3V_LAN_S5	
VESD	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDP	Don't Care	2D5V_S5	
3D3V_2D5V_S5	3D3V_S5	2D5V_S5	
1D8V_1D2V_S5	1D8V_LAN_S5	1D2V_S5	

GIGA Lan Transformer



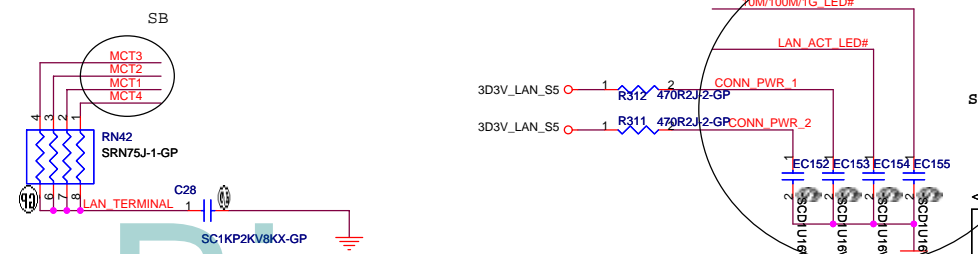
LAN Link: Green(A3), behavior is the same for 10/100/1000 bits
LAN Data: Yellow(B2), when LAN is transferring data.

- route on bottom as differential pairs.
- Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- No vias, No 90 degree bends.
- pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- Must not cross ground moat, except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP, DOC_RING, TIP, RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6



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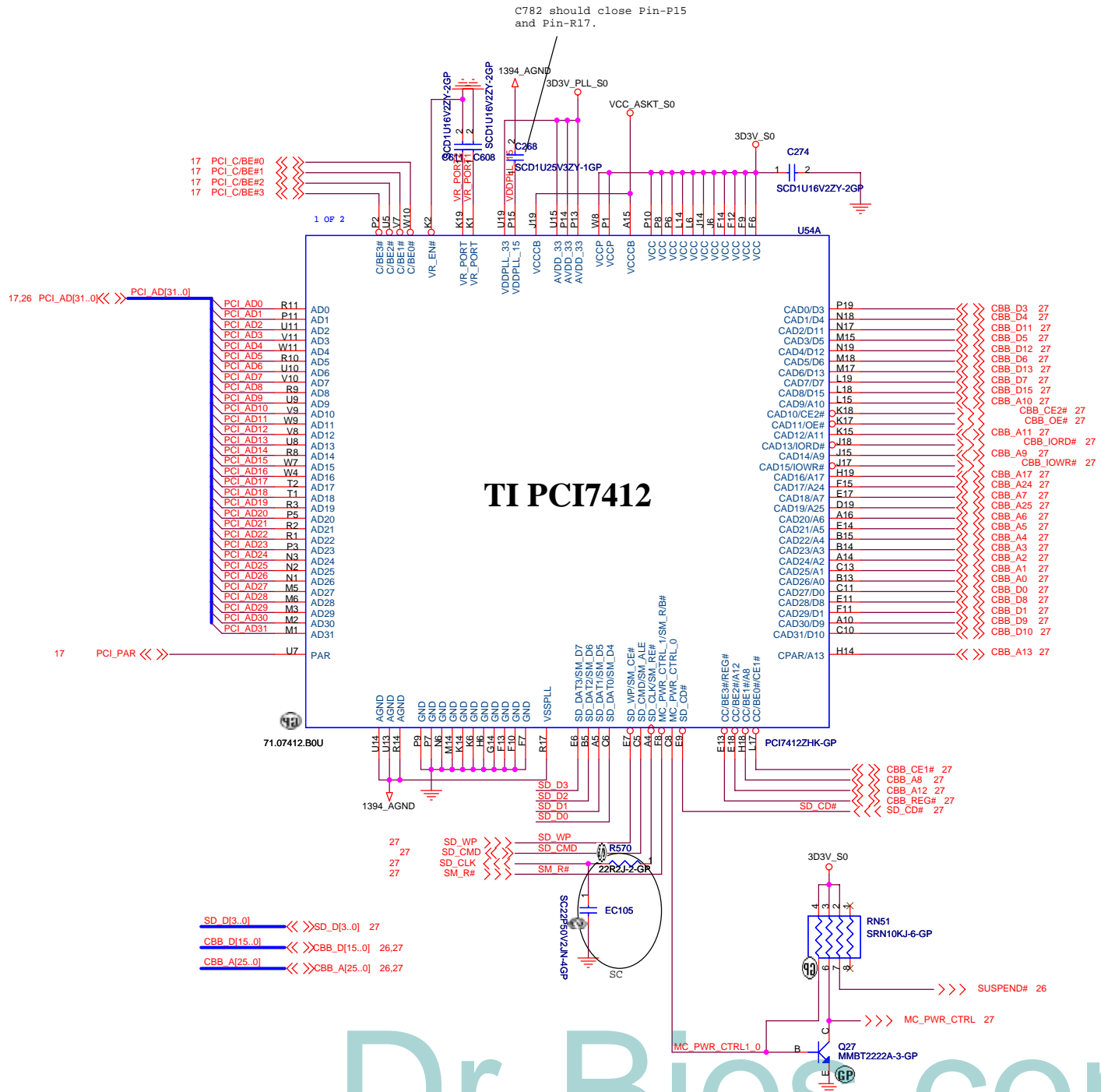
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN Connector

Size A3 Document Number Columbia/Tangiz Rev -1

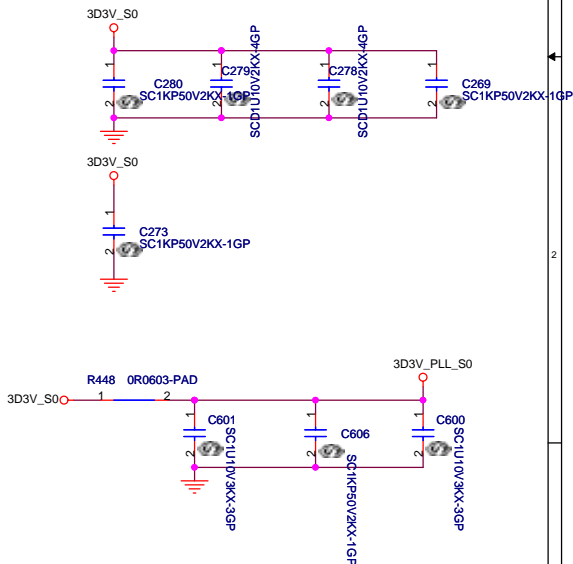
Date: Monday, February 26, 2007 Sheet 24 of 45

C782 should close Pin-P15 and Pin-R17.



- * All 1394 signals must be routed on top side only
- * Differential pairs of each ports should have equal trace length
- * Stubs must be keep as short as possible

Bypass/Decoupling Capacitors
Should be places as close to
PCI7412 as possible



SD_D[3..0] <<< SD_D[3..0] 27
CBB_D[15..0] <<< CBB_D[15..0] 26,27
CBB_A[25..0] <<< CBB_A[25..0] 26,27

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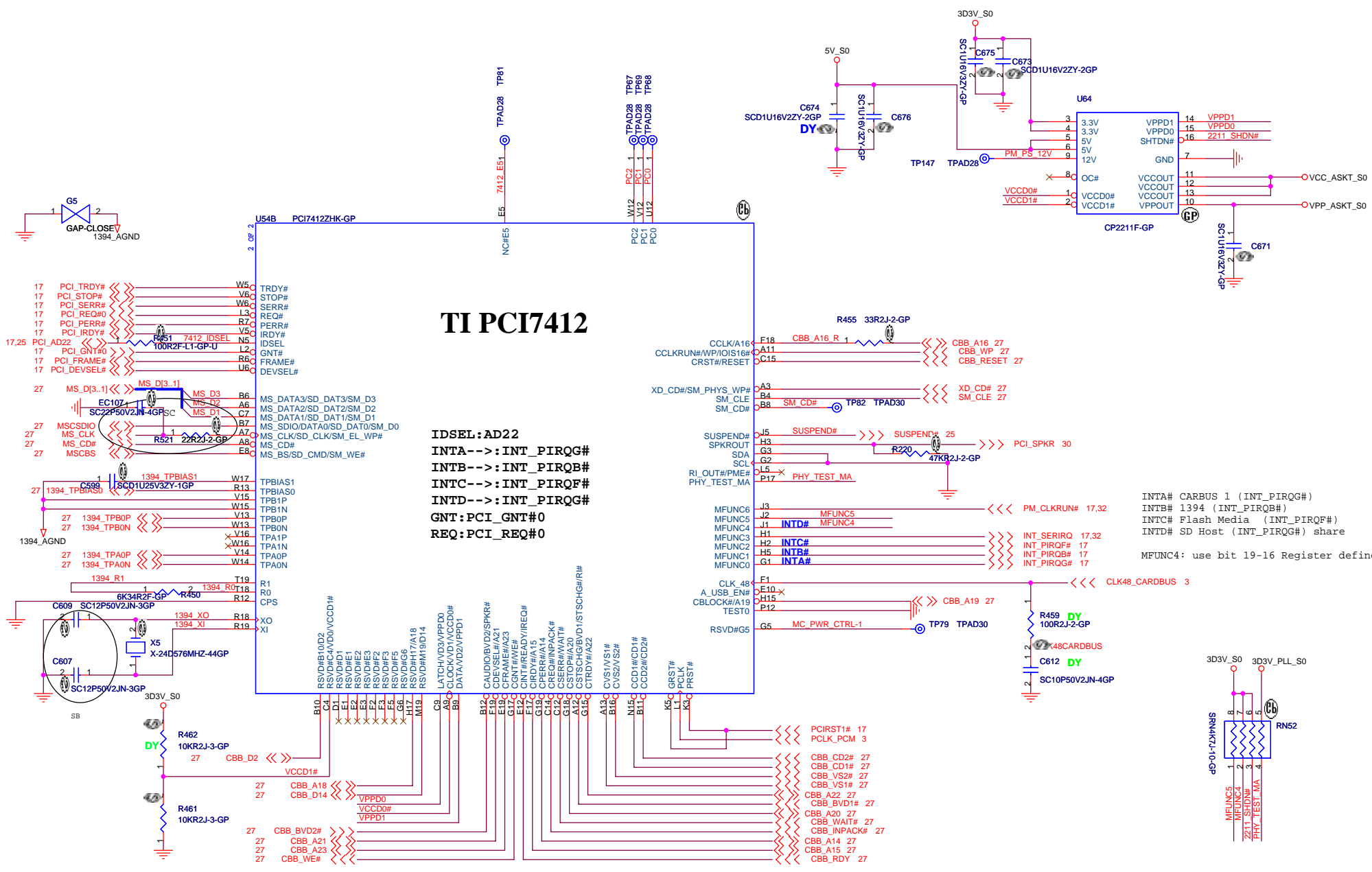
<Variant Name>

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Title: **TI PCI7412 (1 of 2)**

Size: Document Number Rev: -1

Date: Monday, February 26, 2007 Sheet 25 of 45



TI PCI7412

IDSEL: AD22
INTA-->: INT_PIRQ#
INTB-->: INT_PIRQ#
INTC-->: INT_PIRQ#
INTD-->: INT_PIRQ#
GNT: PCI_GNT#0
REQ: PCI_REQ#0

INTA# CARBUS 1 (INT_PIRQ#)
 INTB# 1394 (INT_PIRQ#)
 INTC# Flash Media (INT_PIRQ#)
 INTD# SD Host (INT_PIRQ#) share
 MFUNC4: use bit 19-16 Register define.



<Variant Name>

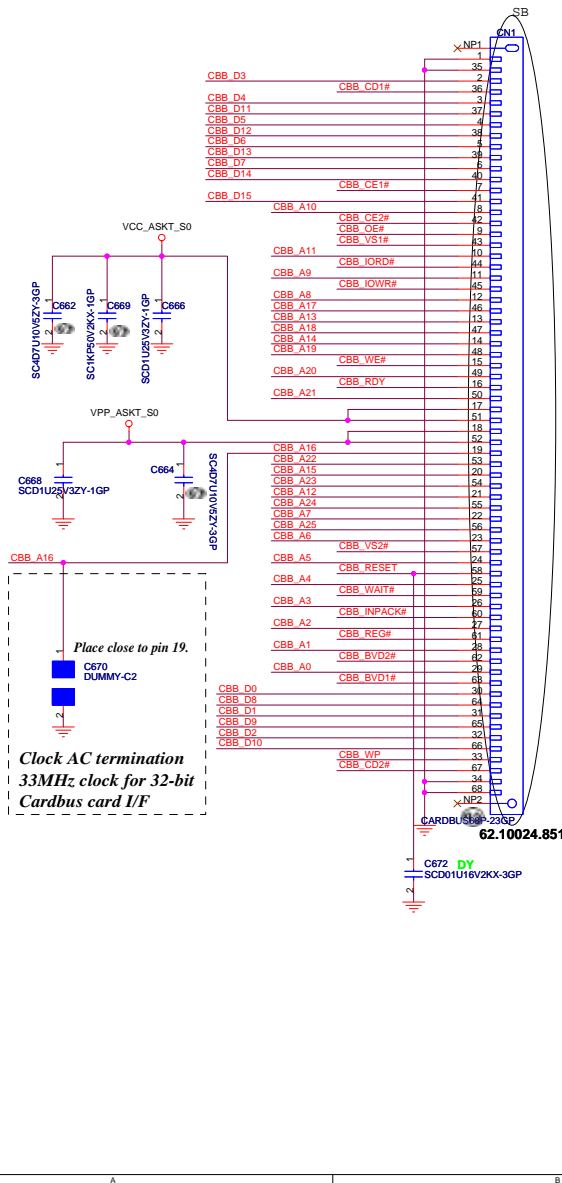
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **TI PCI7412 (2 of 2)**

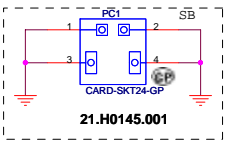
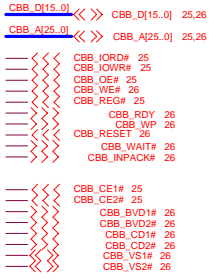
Size: Document Number Rev: **-1**

Date: Monday, February 26, 2007 Sheet 26 of 45

PCMCIA Socket



Cardbus I/F

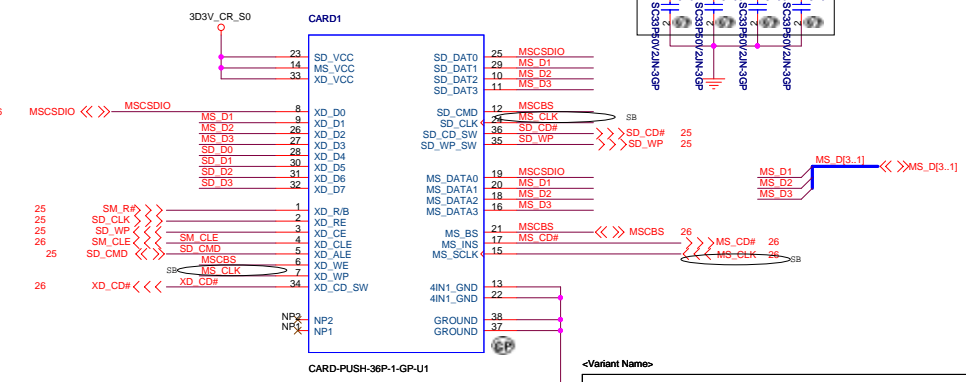
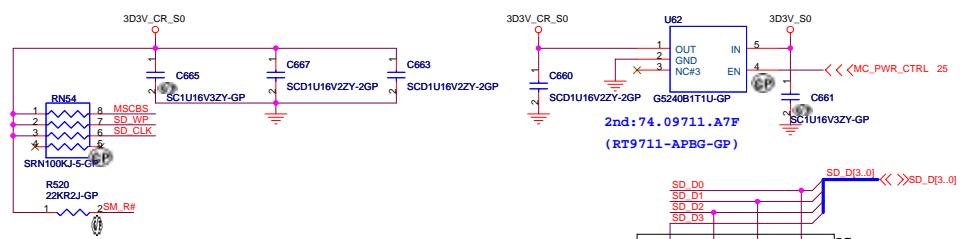
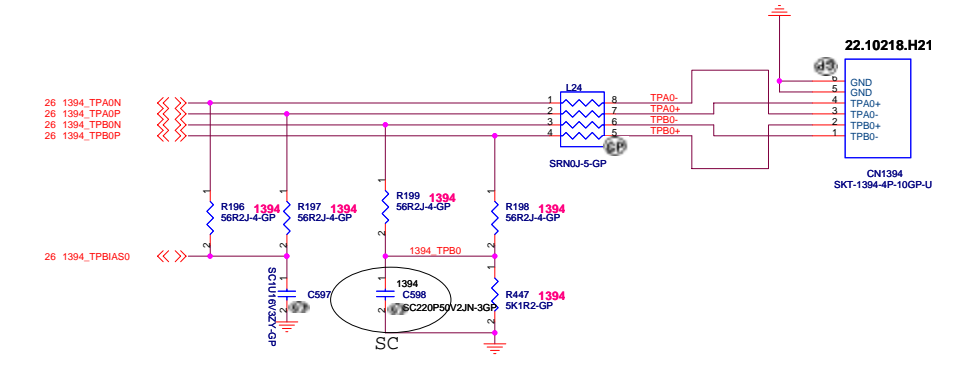


62.10024.851

Place close to pin 19.
 C670 DUMMY-C2

Clock AC termination
 33MHz clock for 32-bit
 Cardbus card I/F

1394 Connector



XD
 MS / MS PRO
 SD / SD IO / MMC

<Variant Name>

緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCMCIA / 1394 / CARD READER**

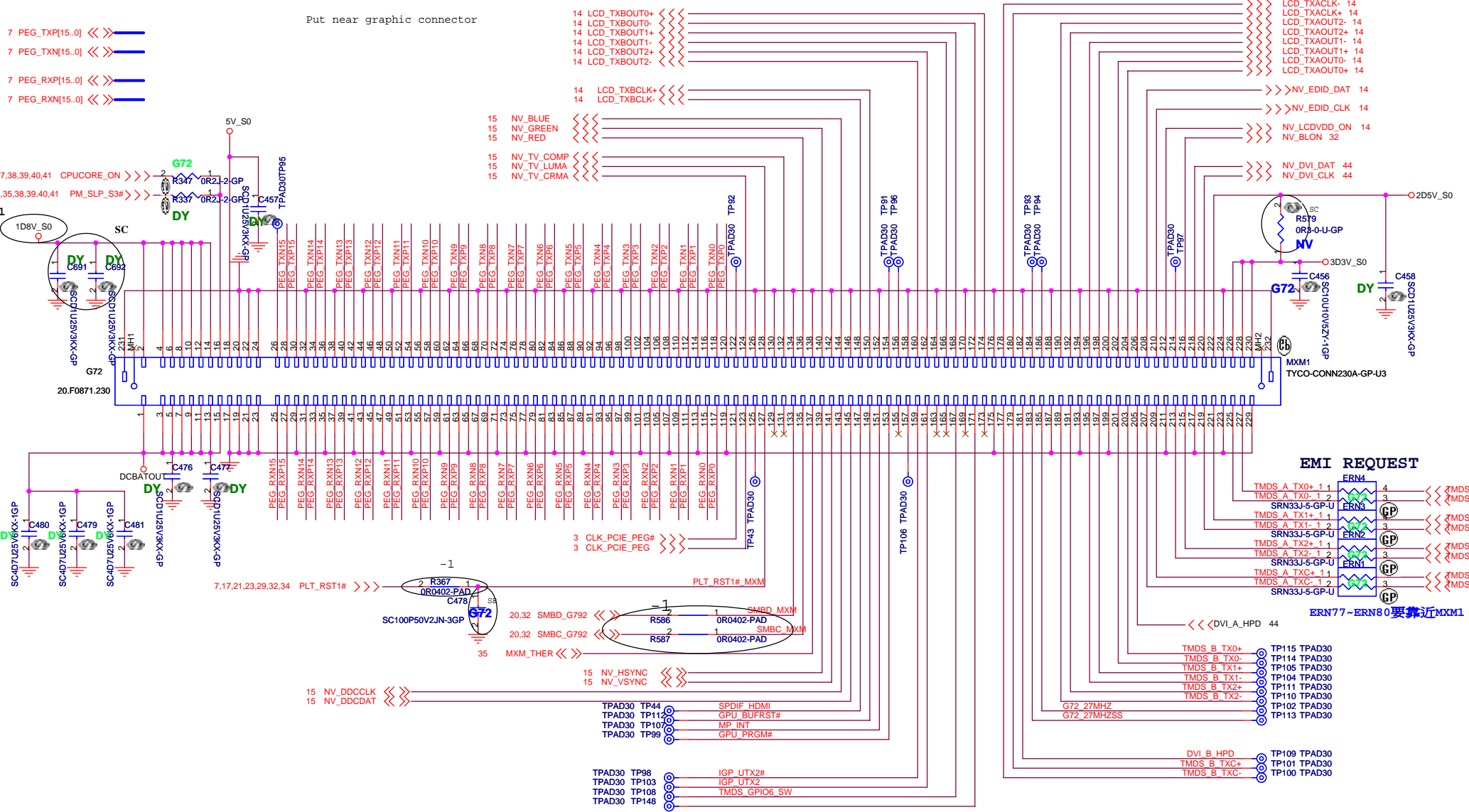
Size: Document Number

Rev: **-1**

Date: Monday, February 26, 2007 Sheet: 27 of 46

NV SMBus
 A(pin143&145) : VGA(CRT) / DOCK
 B(pin218&220) : DVI
 C(pin208&210) : HDMI / TPI / LVDS

Put near graphic connector



Dr-Bios.com

<Core Design>

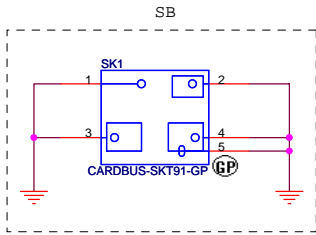
緯創資通 **Wistron Corporation**
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title
Graphic MXM CONN

Size A3	Document Number	Rev -1
Date: Monday, February 26, 2007		Sheet 28 of 45

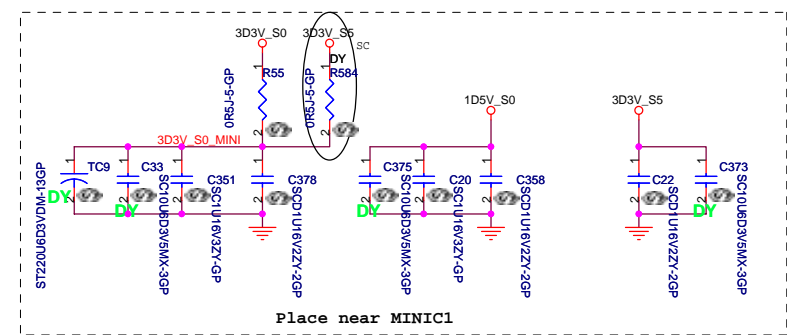
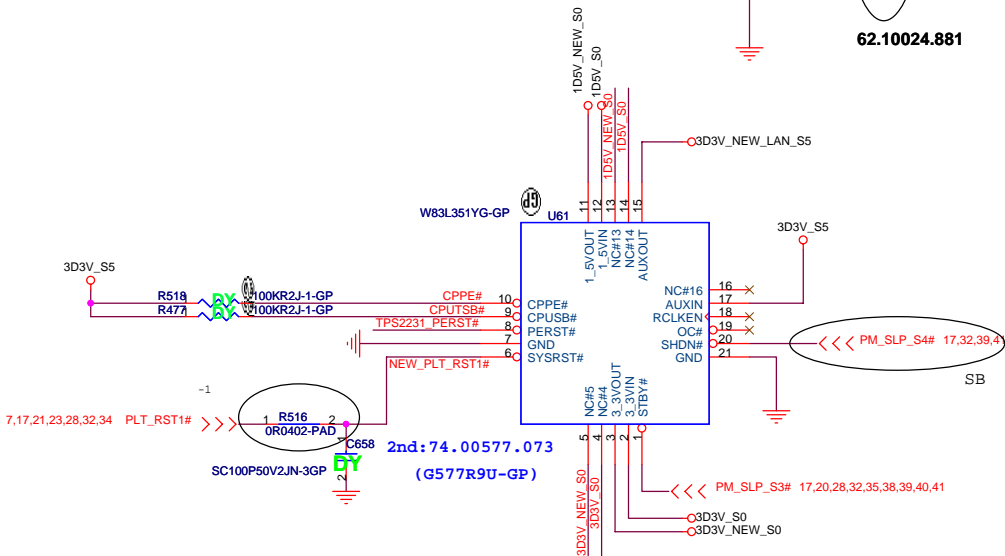
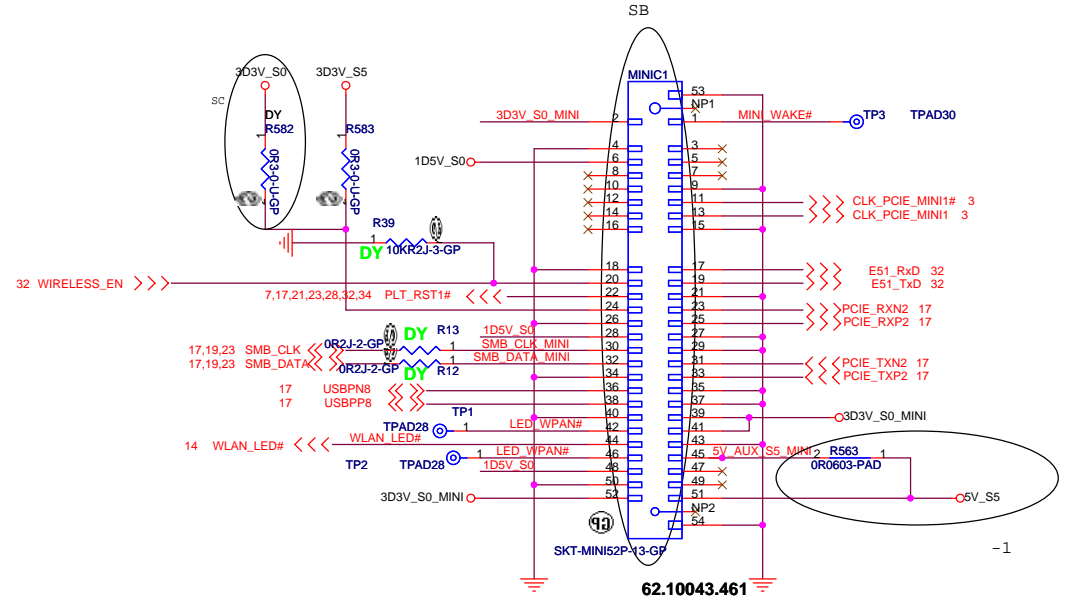
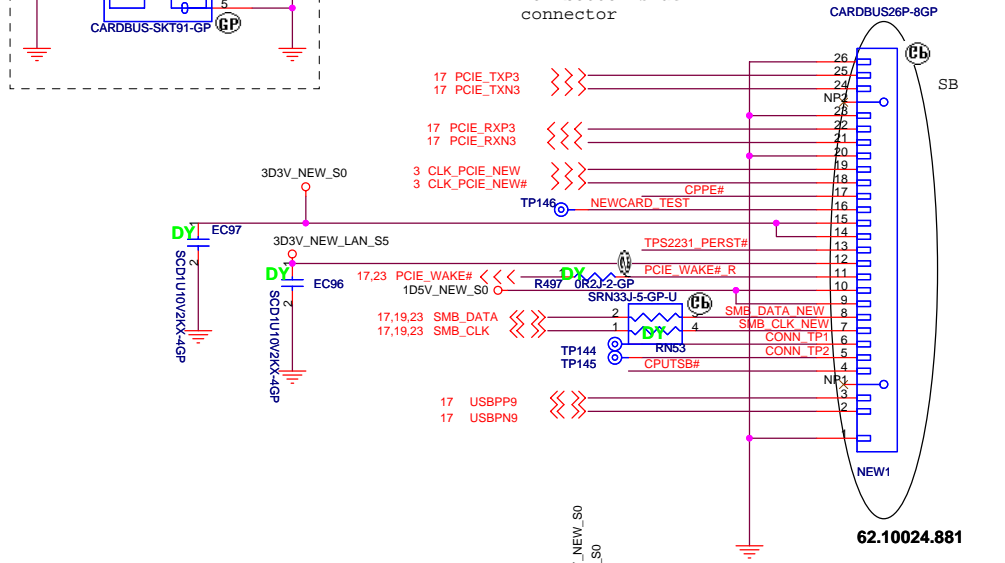
Columbia/Tangiz

Mini Card Connector

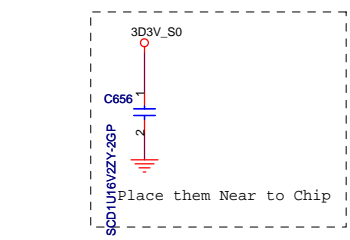


NEWCARD Connector

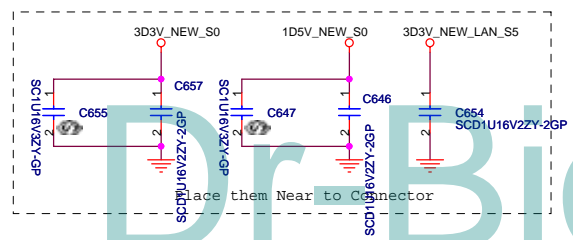
Reserve the symbol for bottom side connector



Place near MINIC1



Place them Near to Chip



Place them Near to Connector

bom1

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Title: **MINI CARD / NEW CARD**

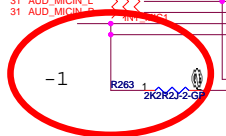
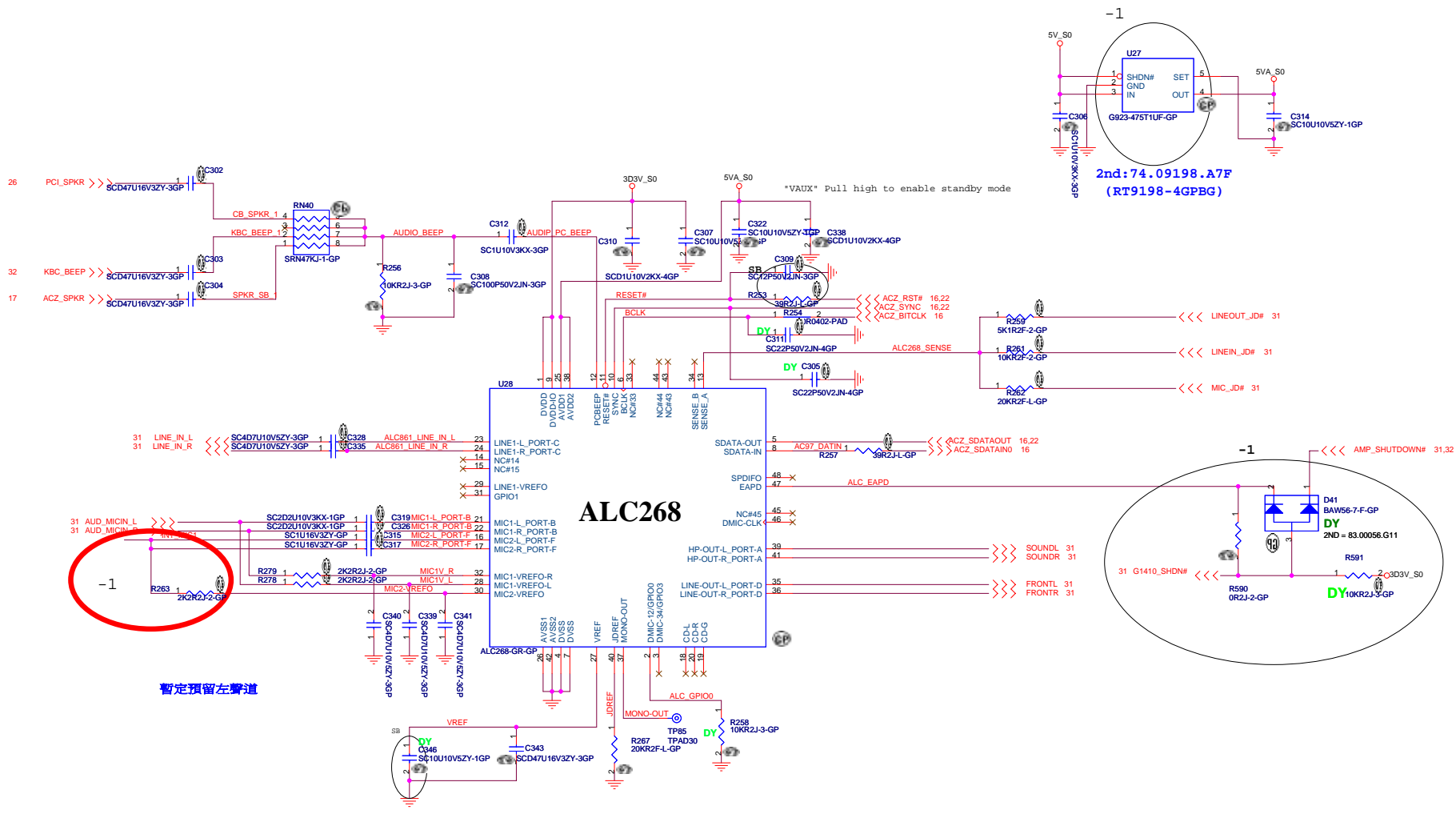
Size: Document Number

Date: Monday, February 26, 2007

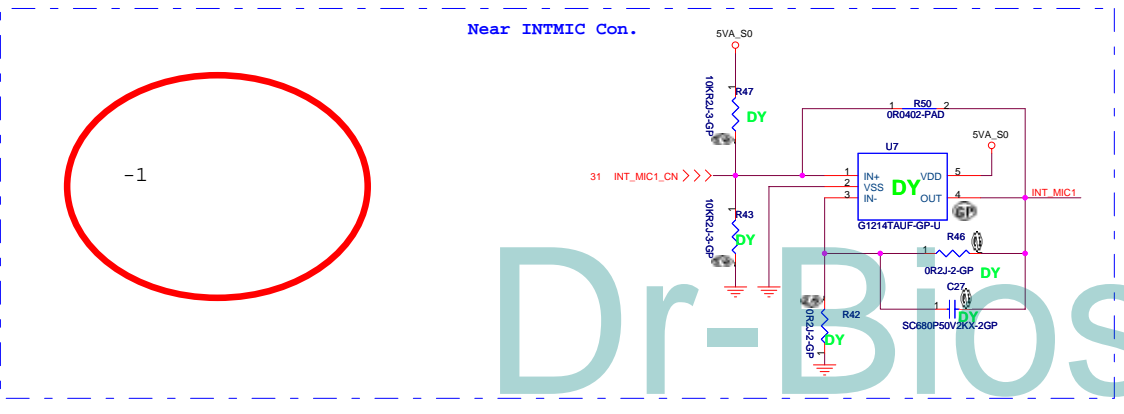
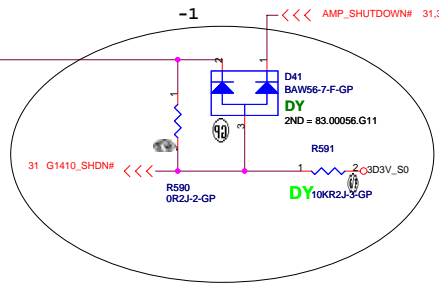
Sheet: 29 of 45

Rev: -1

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暫定預留左聲道



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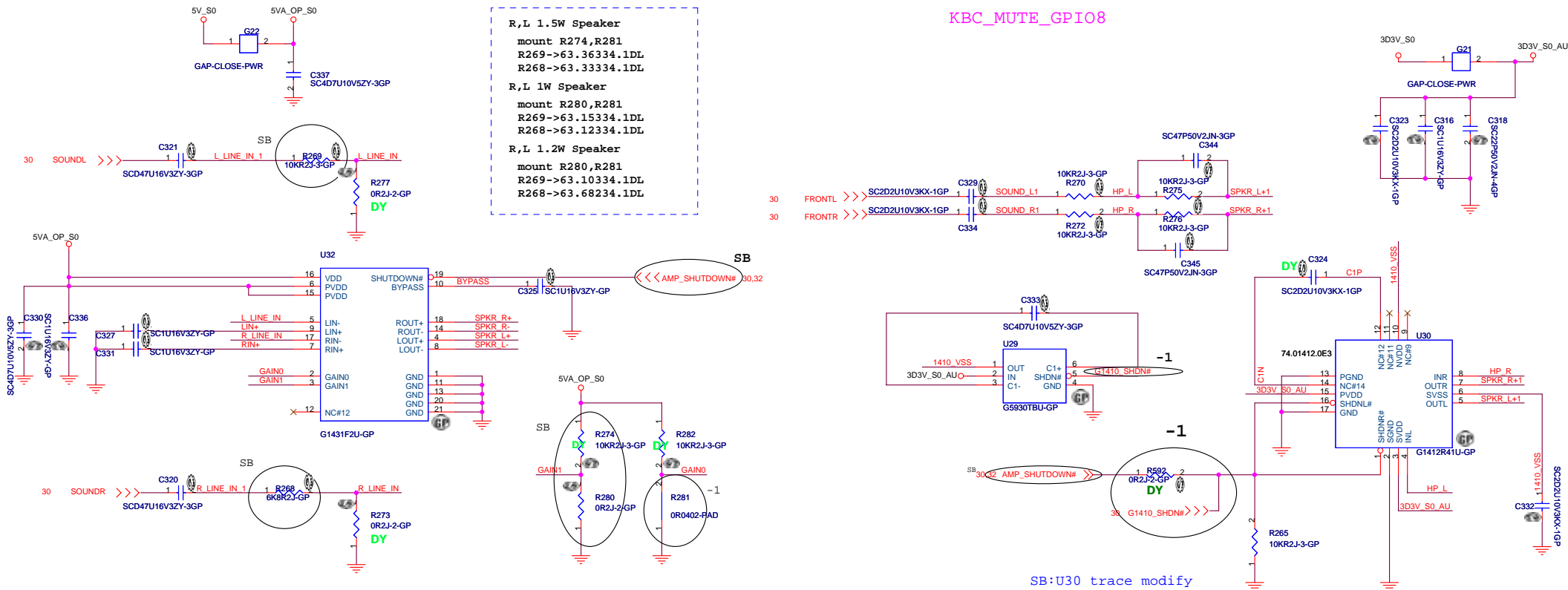
AUDIO OP AMPLIFIER

R,L 1.5W Speaker
 mount R274,R281
 R269->63.36334.1DL
 R268->63.33334.1DL

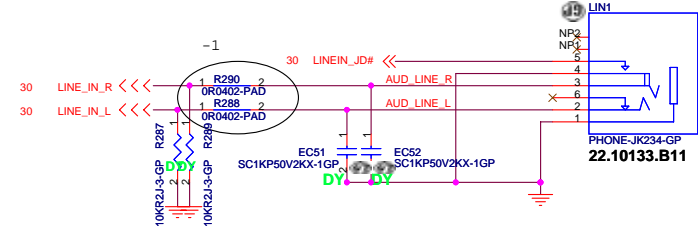
R,L 1W Speaker
 mount R280,R281
 R269->63.15334.1DL
 R268->63.12334.1DL

R,L 1.2W Speaker
 mount R280,R281
 R269->63.10334.1DL
 R268->63.68234.1DL

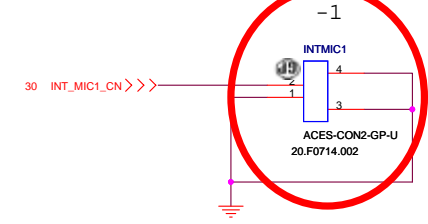
KBC_MUTE_GPIO8



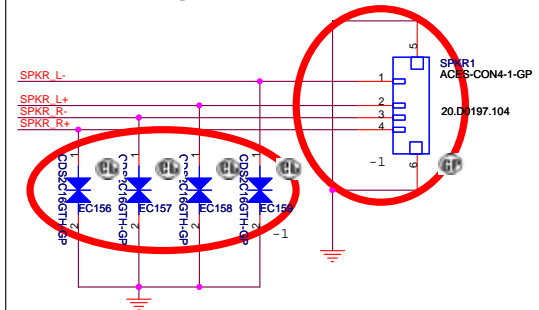
LINE IN



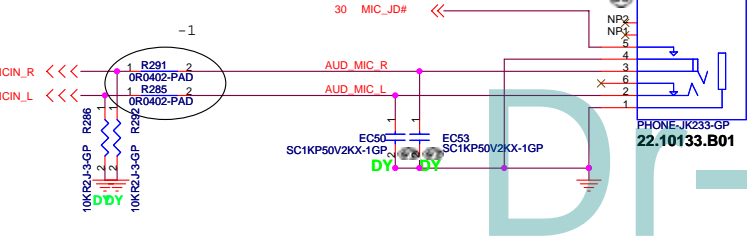
Internal Microphone



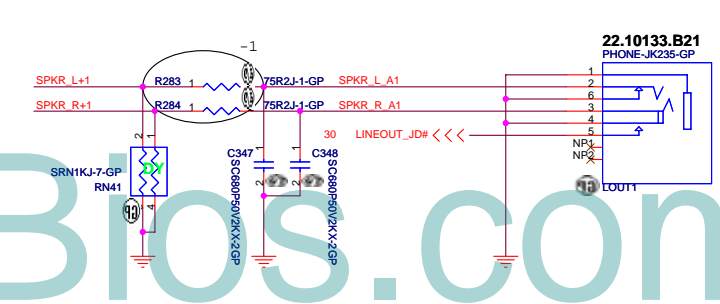
Internal Speaker



MIC IN



LINE OUT



<Variant Name>

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 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

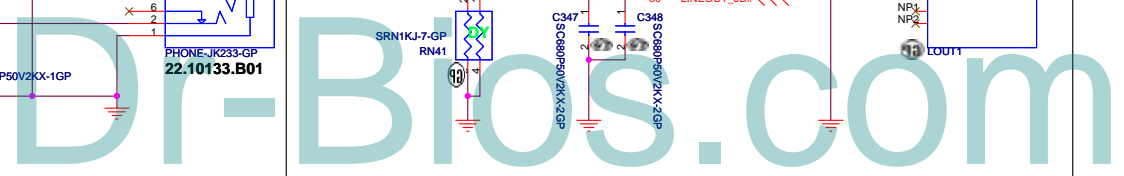
Title: **AUDIO AMP AND JACK**

Size: Document Number

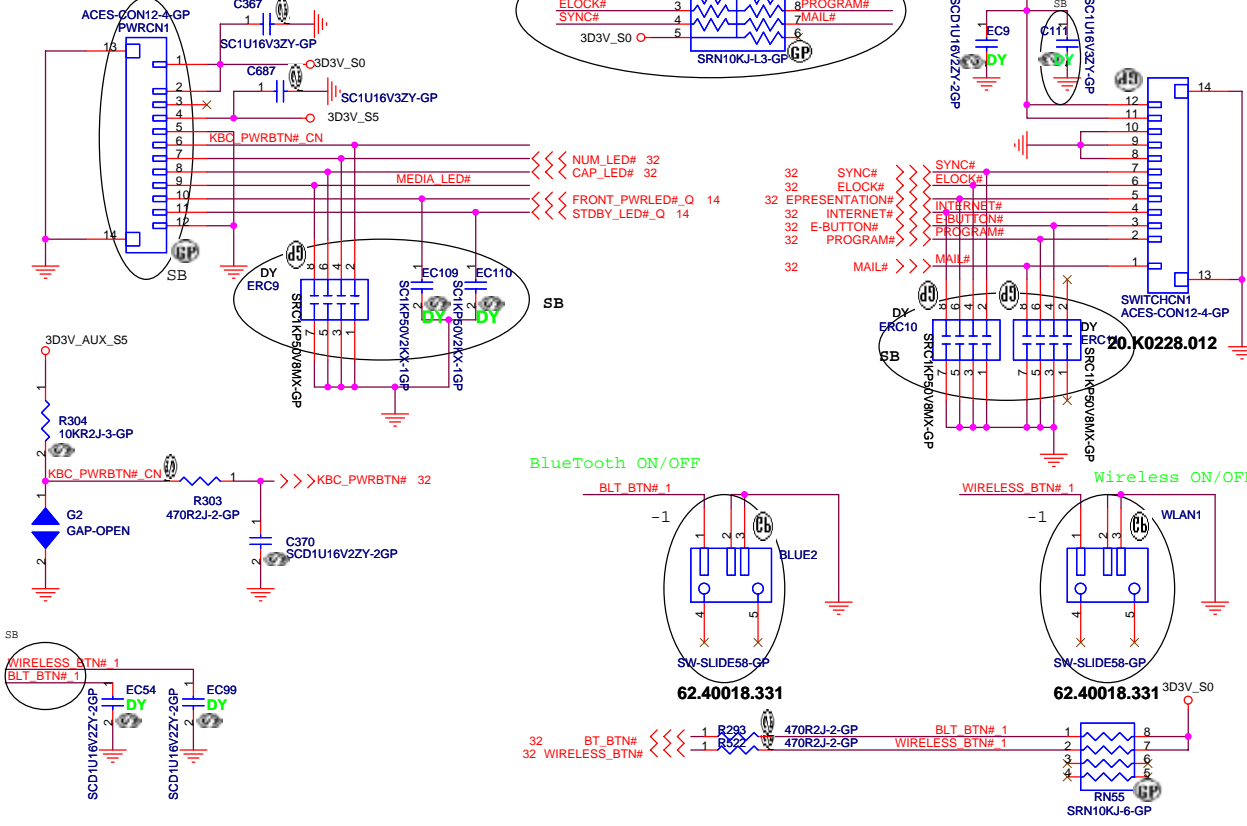
Date: Monday, February 26, 2007

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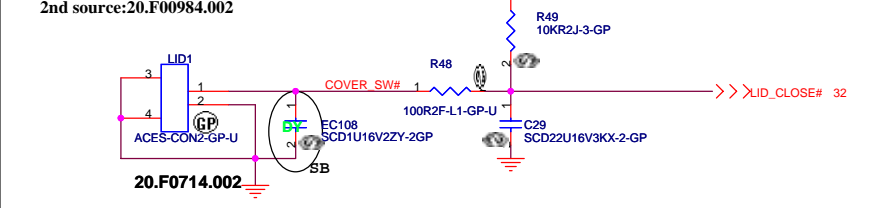
Rev -1



20.K0228.012



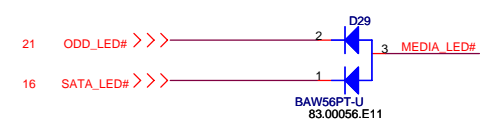
Cover Up Switch



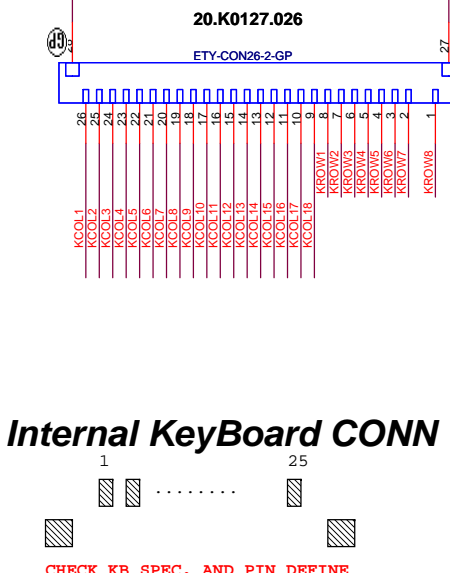
Check test point

- 3D3V_AUX_S5 TP139 TPAD30
- 3D3V_S5 TP143 TPAD30
- 5V_S5 TP142 TPAD30
- 17,32 PM_PWRBTN# TP141 TPAD30
- 4,16,35 H_PWRGD TP29 TPAD30
- 32,38 SS_ENABLE TP140 TPAD30
- 4,6 H_CPURST# TP90 TPAD30

Test Point 放在 Dimm Door 打開可量測處

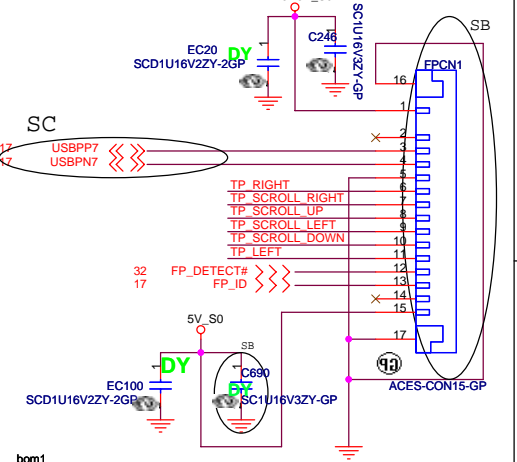
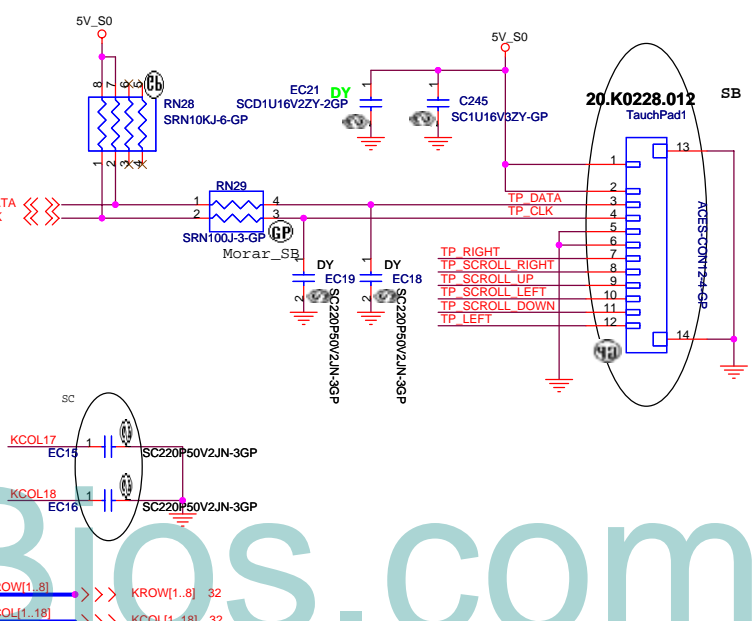


20.K0127.026



EMI Bypass cap.

KCOL13	EC128	SC220P50V2JN-3GP
KCOL14	EC129	SC220P50V2JN-3GP
KCOL15	EC130	SC220P50V2JN-3GP
KCOL16	EC131	SC220P50V2JN-3GP
KCOL17	EC132	SC220P50V2JN-3GP
KCOL18	EC133	SC220P50V2JN-3GP
KCOL1	EC134	SC220P50V2JN-3GP
KCOL2	EC135	SC220P50V2JN-3GP
KCOL3	EC136	SC220P50V2JN-3GP
KCOL4	EC137	SC220P50V2JN-3GP
KCOL5	EC138	SC220P50V2JN-3GP
KCOL6	EC139	SC220P50V2JN-3GP
KCOL7	EC140	SC220P50V2JN-3GP
KCOL8	EC141	SC220P50V2JN-3GP
KCOL9	EC142	SC220P50V2JN-3GP
KCOL10	EC143	SC220P50V2JN-3GP
KCOL11	EC144	SC220P50V2JN-3GP
KCOL12	EC145	SC220P50V2JN-3GP
KCOL13	EC146	SC220P50V2JN-3GP
KCOL14	EC147	SC220P50V2JN-3GP
KCOL15	EC148	SC220P50V2JN-3GP
KCOL16	EC149	SC220P50V2JN-3GP
KCOL17	EC150	SC220P50V2JN-3GP



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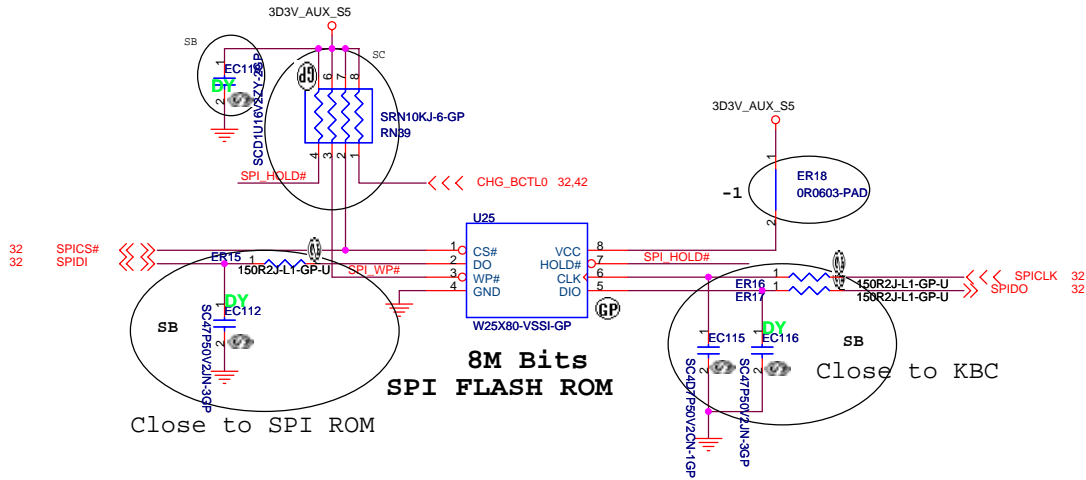
Buttons / KB / TOUCHPAD

Columbia/Tangiz

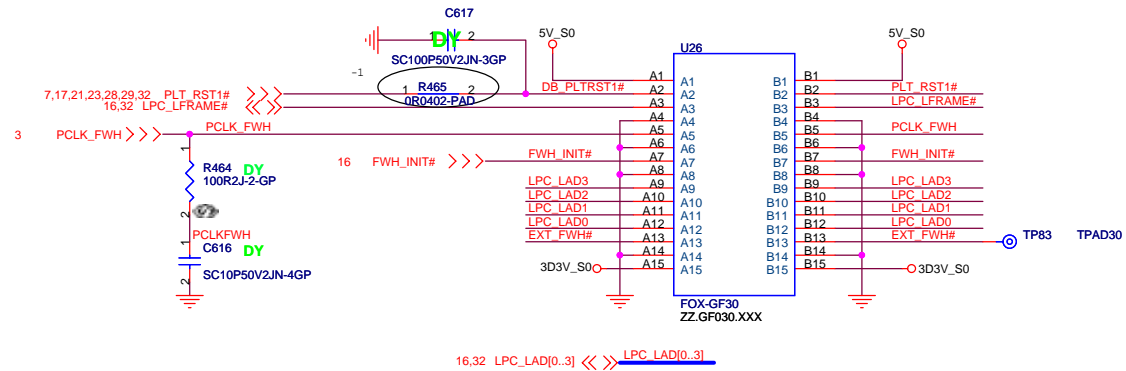
Monday, February 26, 2007

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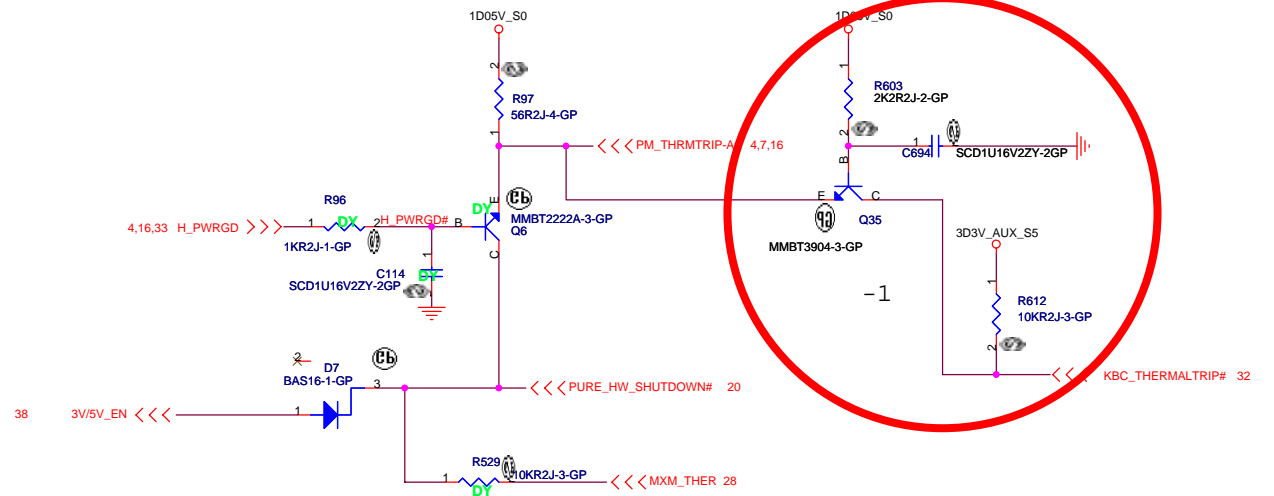
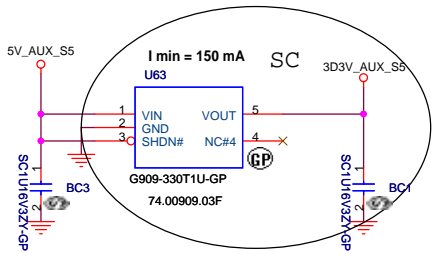
Rev -1



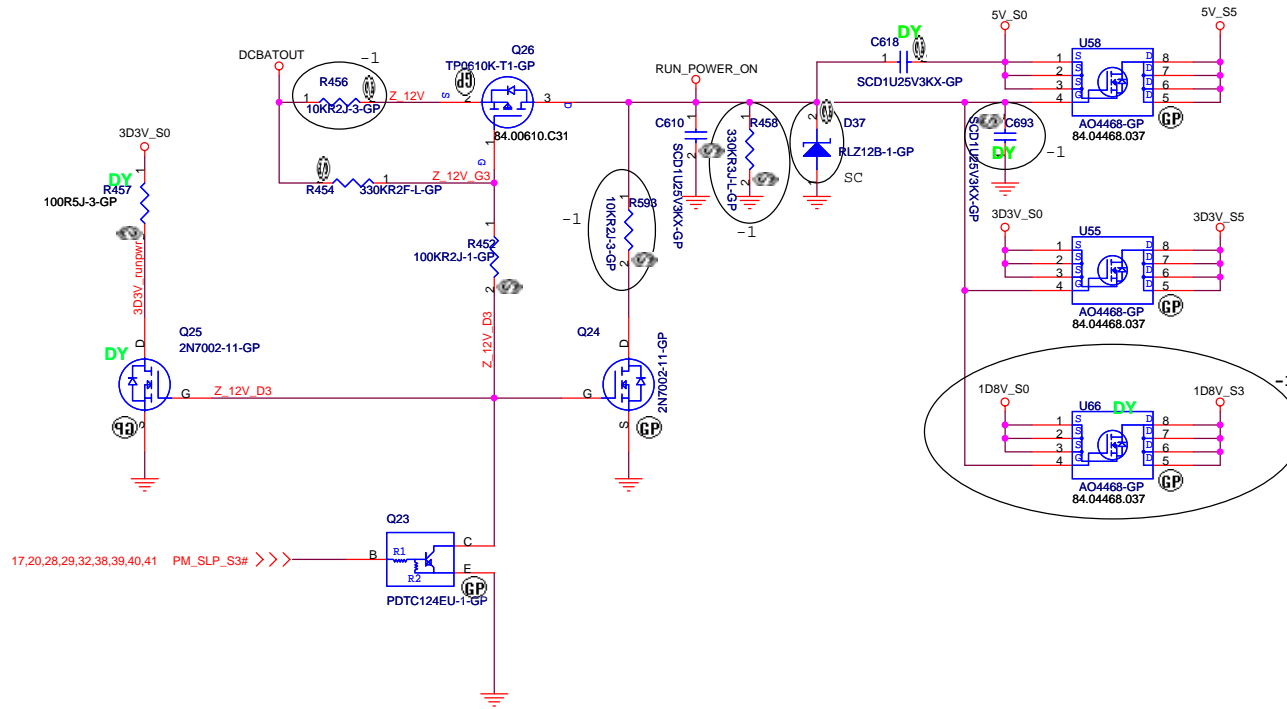
GOLDEN FINGER FOR DEBUG BOARD



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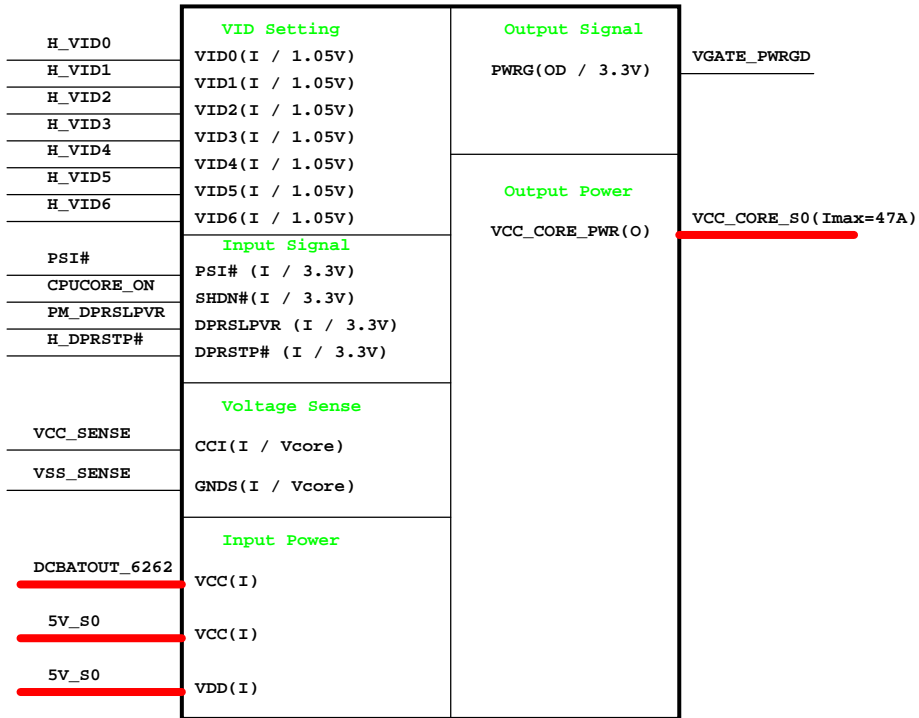


Run Power

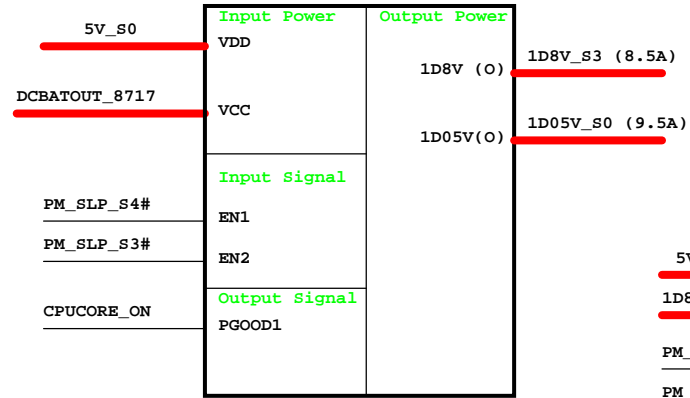


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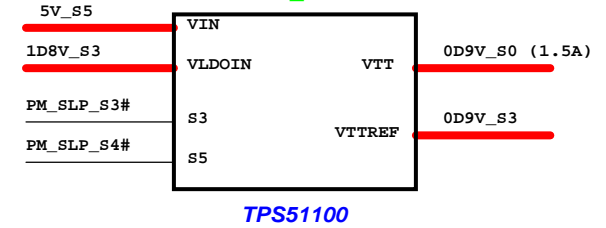
**CPU_CORE
MAX8770**



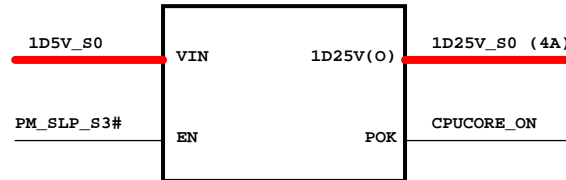
**MAX8717
1D8V/1D05V**



0D9V_S0

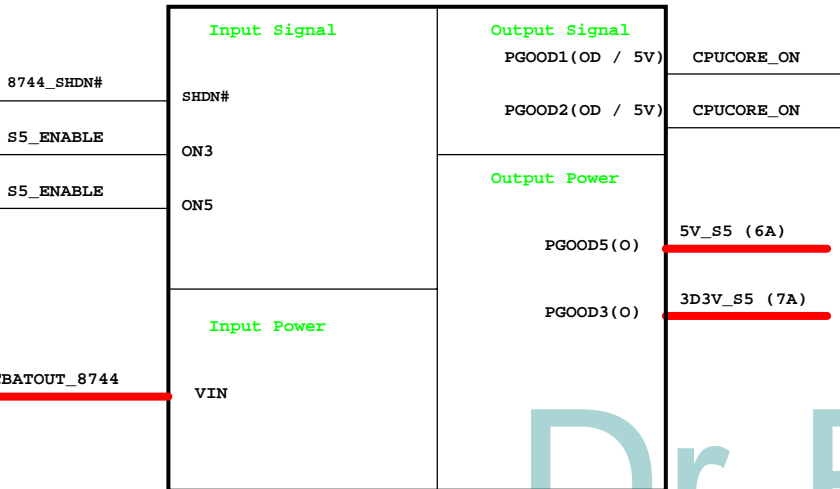


1D25V_S0

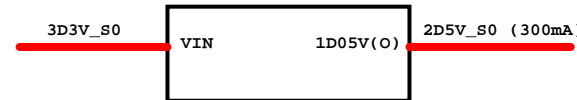


APL5915

**MAX8744
5V/3D3V**

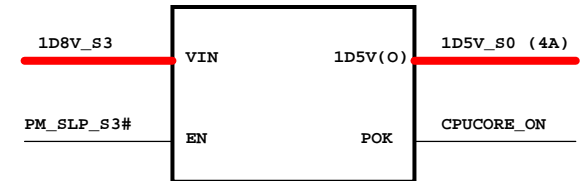


2D5V_S0



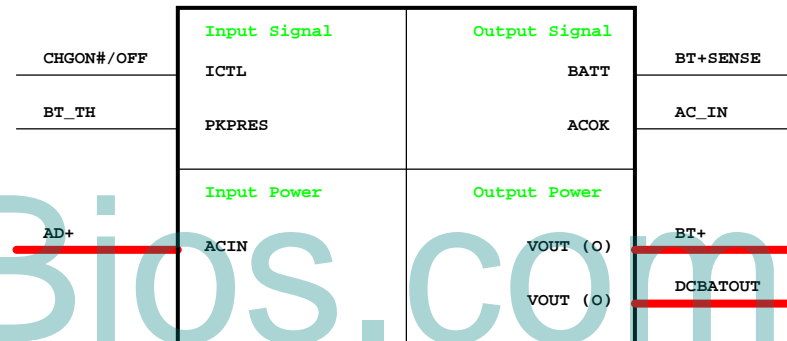
APL5308

1D5V_S0



APL5912

Charger ISL6255



<Variant Name>

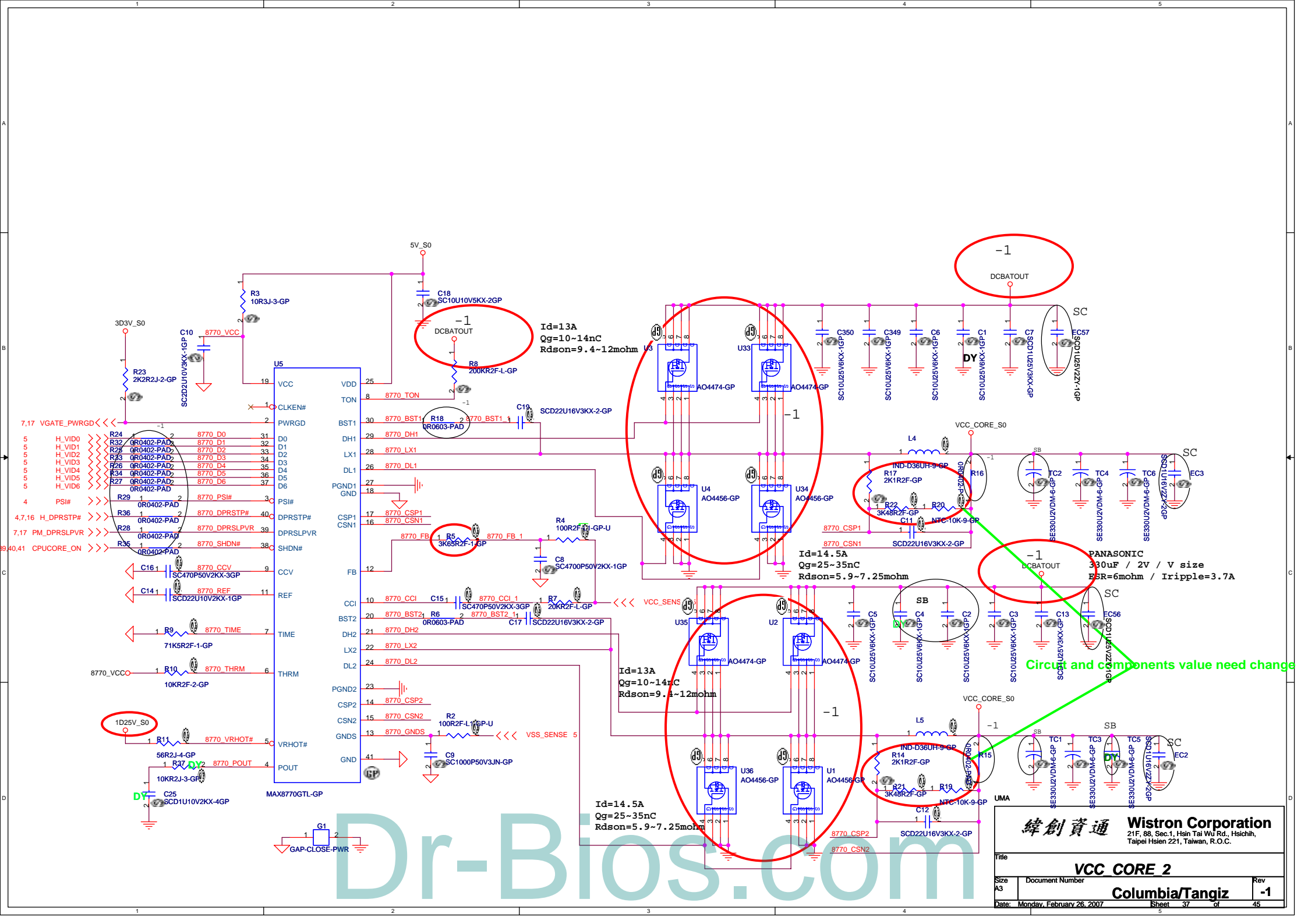
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

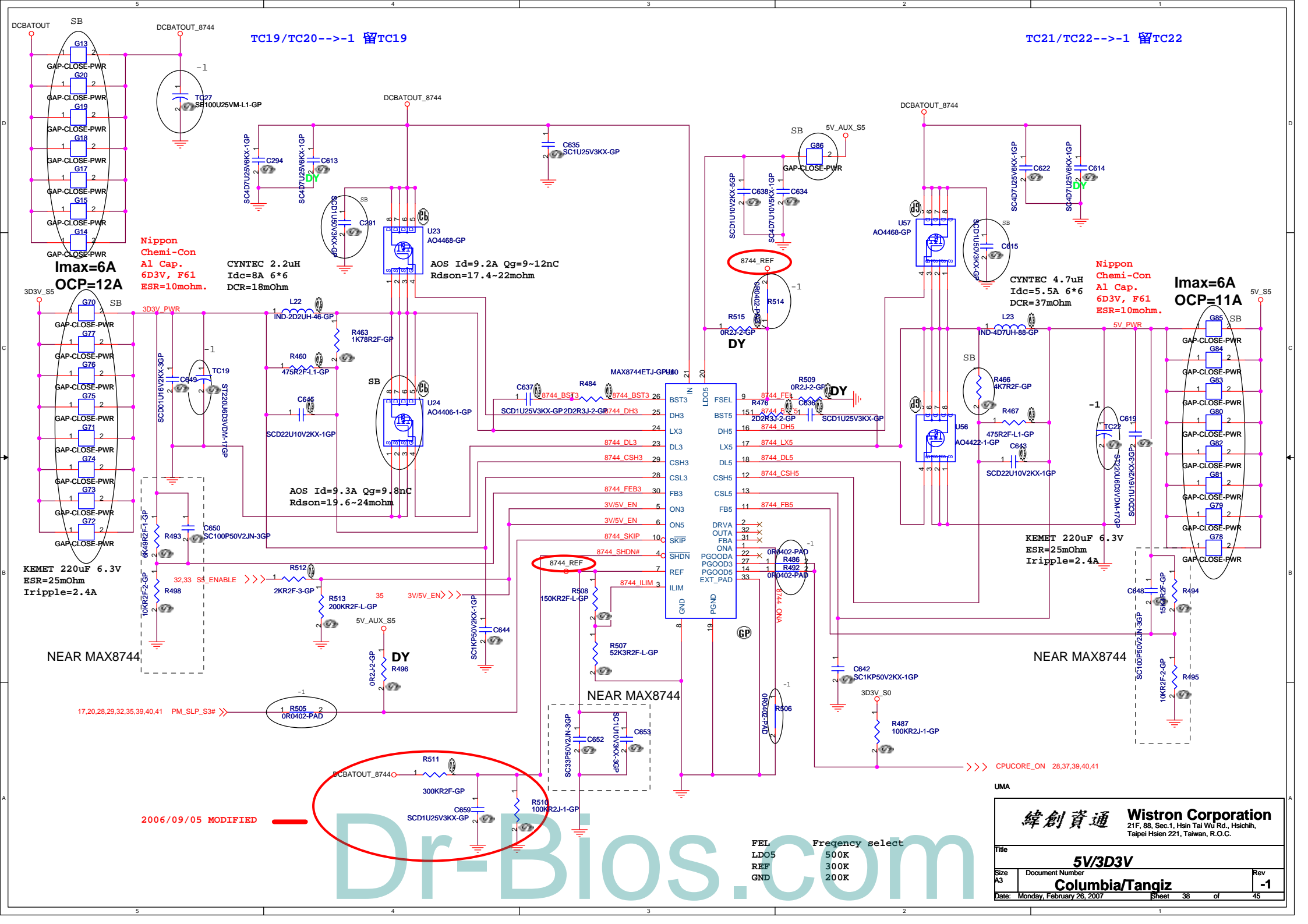
Title: **Power Block Diagram**

Size: A3 Document Number: **Columbia/Tangiz** Rev: -1

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TC19/TC20-->-1 留TC19

TC21/TC22-->-1 留TC22

**Imax=6A
OCP=12A**

**Imax=6A
OCP=11A**

KEMET 220uF 6.3V
ESR=25mOhm
Iripple=2.4A

KEMET 220uF 6.3V
ESR=25mOhm
Iripple=2.4A

**Nippon
Cheml-Con
Al Cap.
6D3V, F61
ESR=10mohm.**

CYNTec 2.2uH
Idc=8A 6*6
DCR=18mOhm

AOS Id=9.3A Qg=9.8nC
Rdson=19.6~24mohm

AOS Id=9.2A Qg=9~12nC
Rdson=17.4~22mohm

CYNTec 4.7uH
Idc=5.5A 6*6
DCR=37mOhm

8744_REF

8744_REF

FEL	Frequency select
LDO5	500K
REF	300K
GND	200K

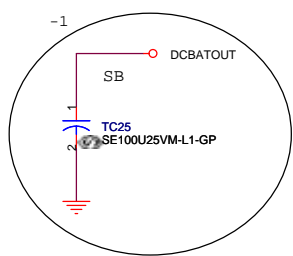
NEAR MAX8744

NEAR MAX8744

2006/09/05 MODIFIED

緯創資通 **Wistron Corporation**
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Title		
5V/3D3V		
Size	Document Number	Rev
A3	Columbia/Tangiz	-1
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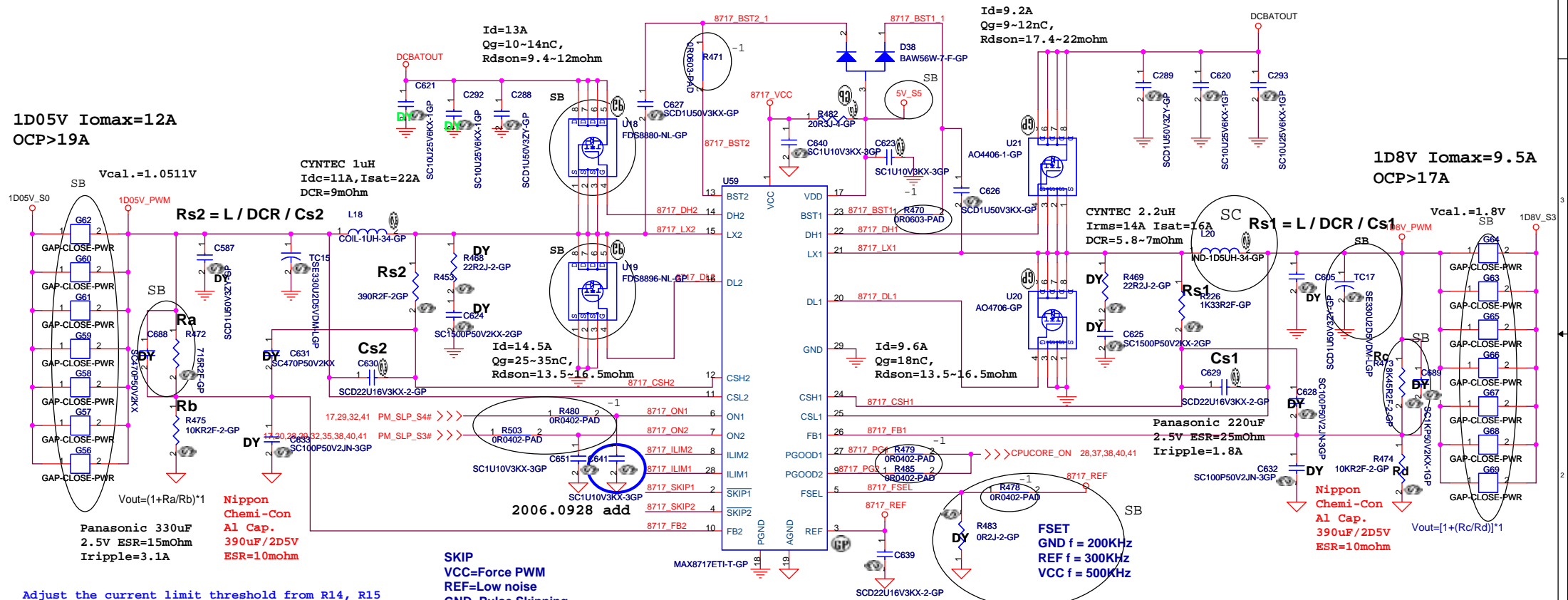


TC15/TC16-->-1 留TC15

TC17/TC18-->-1 留TC17

1D05V Iomax=12A
OCP>19A

1D8V Iomax=9.5A
OCP>17A



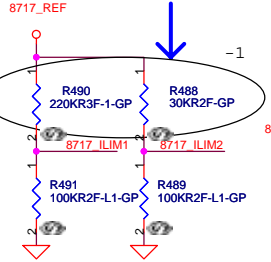
Panasonic 330uF
2.5V ESR=15mOhm
Iripple=3.1A

Nippon
Chemi-Con
Al Cap.
390uF/2D5V
ESR=1.0mohm

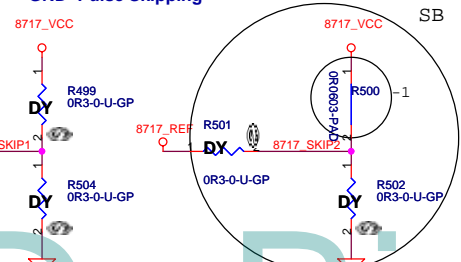
Adjust the current limit threshold from R14, R15

SKIP
VCC=Force PWM
REF=Low noise
GND= Pulse Skipping

FSET
GND f = 200KHz
REF f = 300KHz
VCC f = 500KHz



VILIM = 0.5V~2.0V
Output Current =
ILIM / 10 / LDCR - di/2



UMA

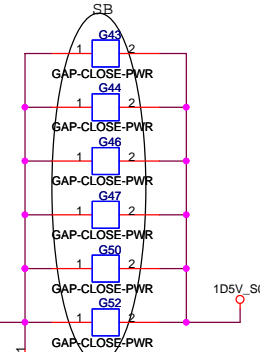
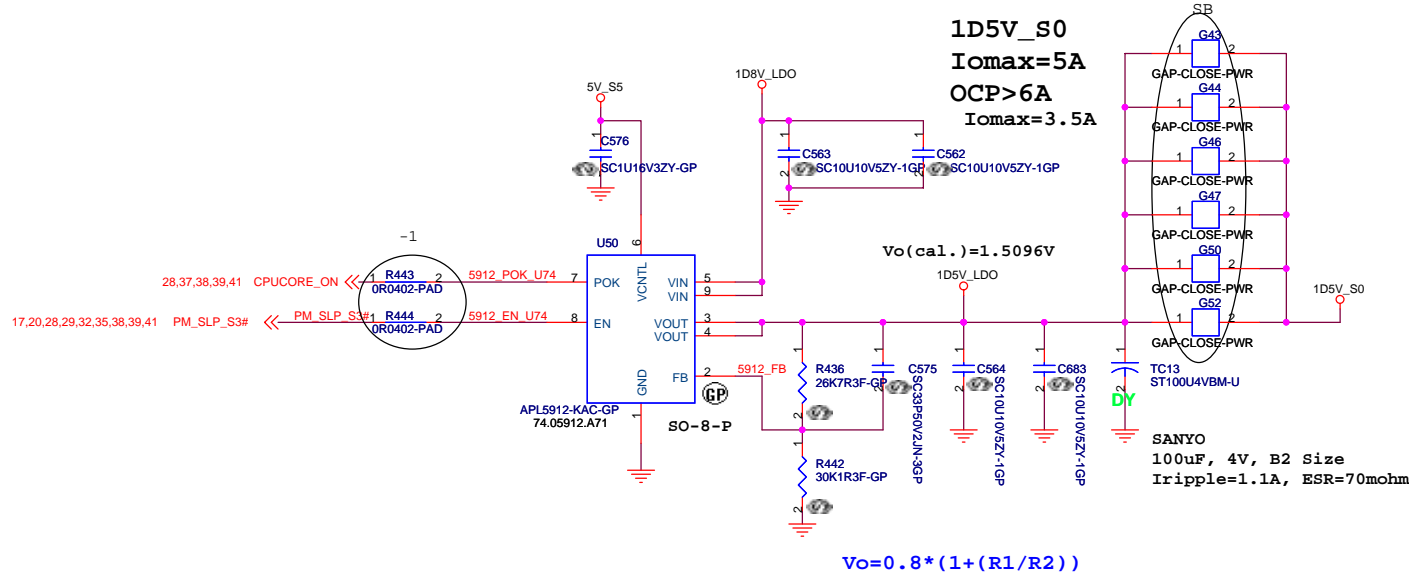
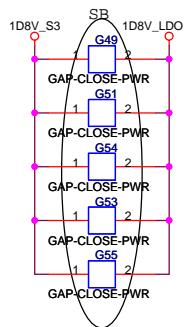
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Title
MAX8717 1D8V 1D05V

Size A3 Document Number
ColumbiaTangiz

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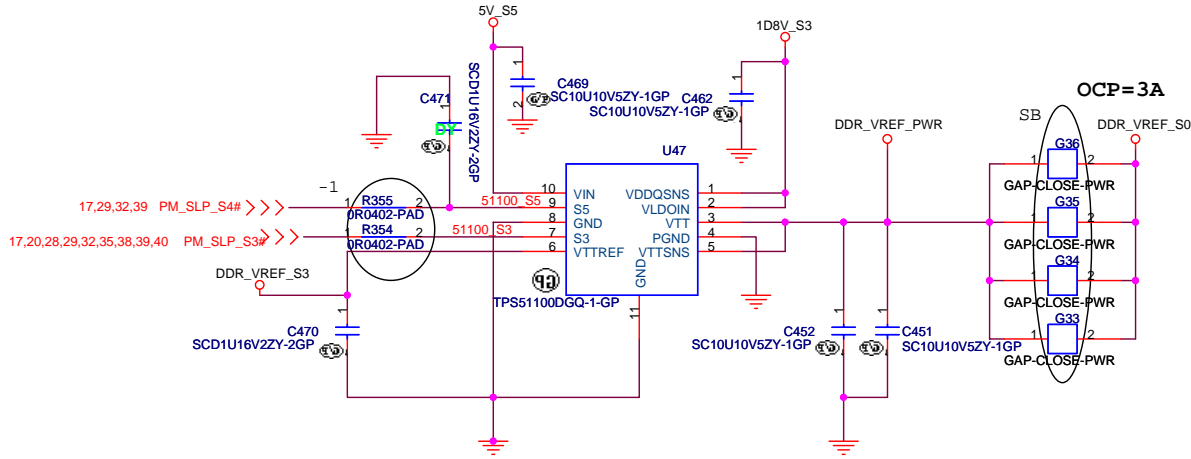


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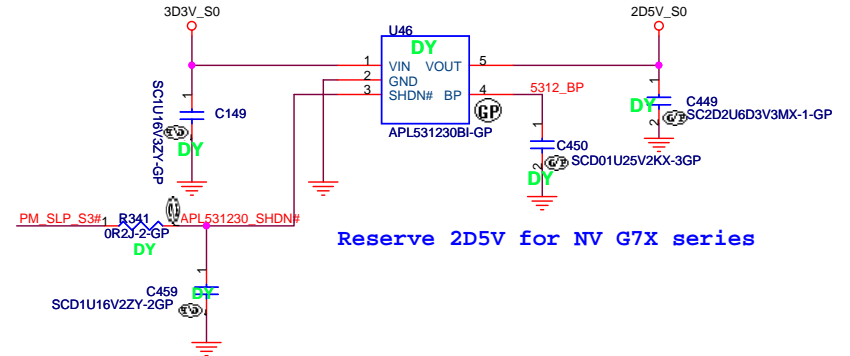
UMA

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APW5912_1D5V	
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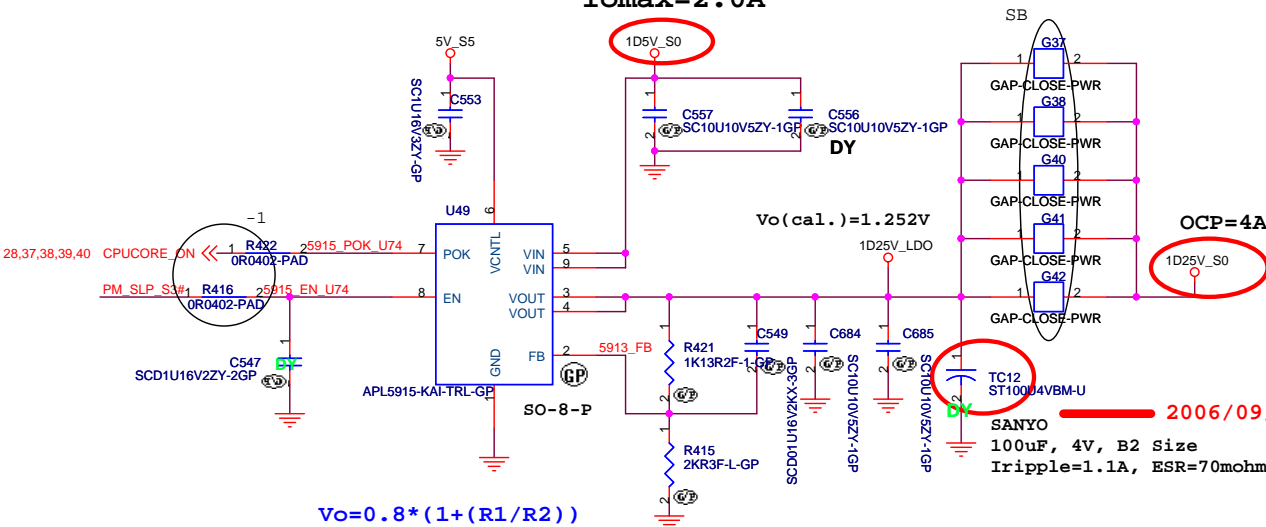
0D9V_S3
Iomax=1.2A



2D5V
Iomax=130mA



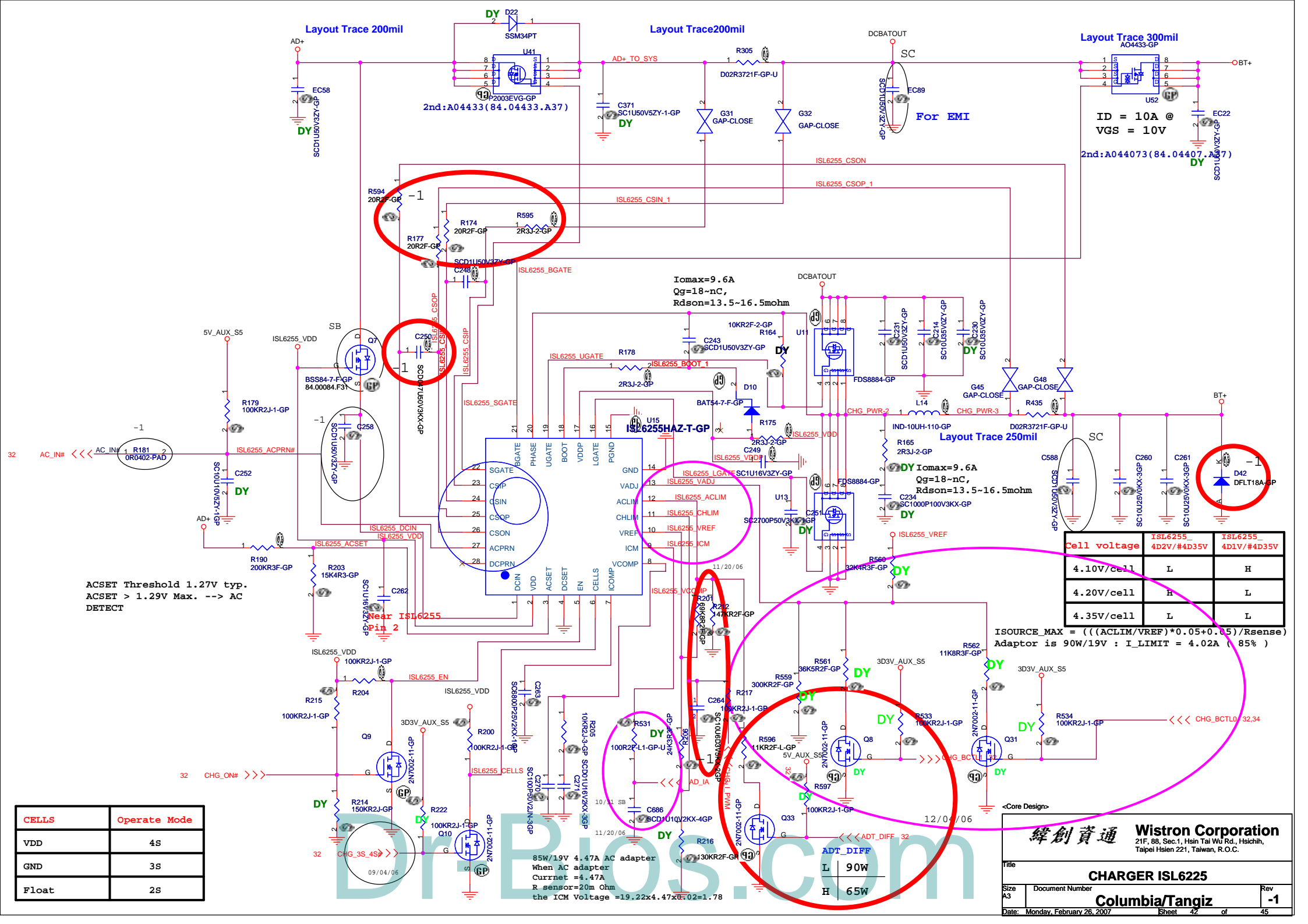
1D25V_S0
Iomax=2.0A



UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title		
1D25V/2D5V//1D05V/0D9V		
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ACSET Threshold 1.27V typ.
 ACSET > 1.29V Max. --- AC
 DETECT

$I_{omax} = 9.6A$
 $Q_g = 18-nC$,
 $R_{dson} = 13.5-16.5m\Omega$

$I_{omax} = 9.6A$
 $Q_g = 18-nC$,
 $R_{dson} = 13.5-16.5m\Omega$

$I_{SOURCE_MAX} = ((ACLIM/VREF) * 0.05 + 0.05) / R_{sense}$
 Adaptor is 90W/19V : $I_LIMIT = 4.02A$ (85%)

Cell voltage	ISL6255_4D2V/#4D35V	ISL6255_4D1V/#4D35V
4.10V/cell	L	H
4.20V/cell	H	L
4.35V/cell	L	L

CELLS	Operate Mode
VDD	4S
GND	3S
Float	2S

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 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CHARGER ISL6255**

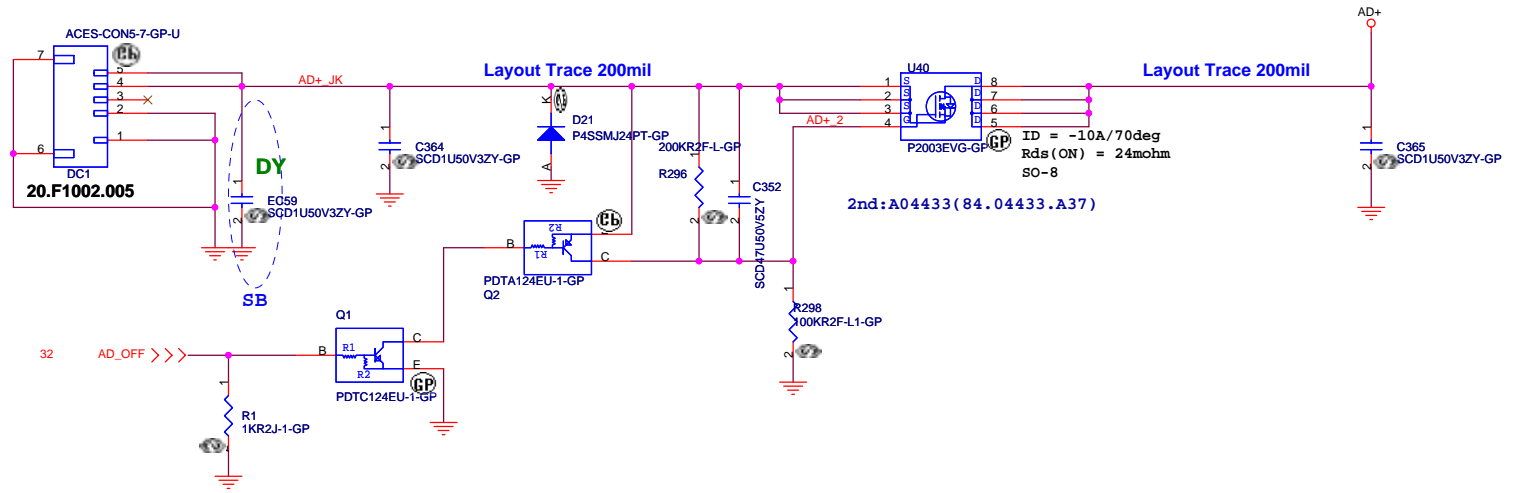
Size A3 Document Number: **Columbia/Tangiz** Rev **-1**

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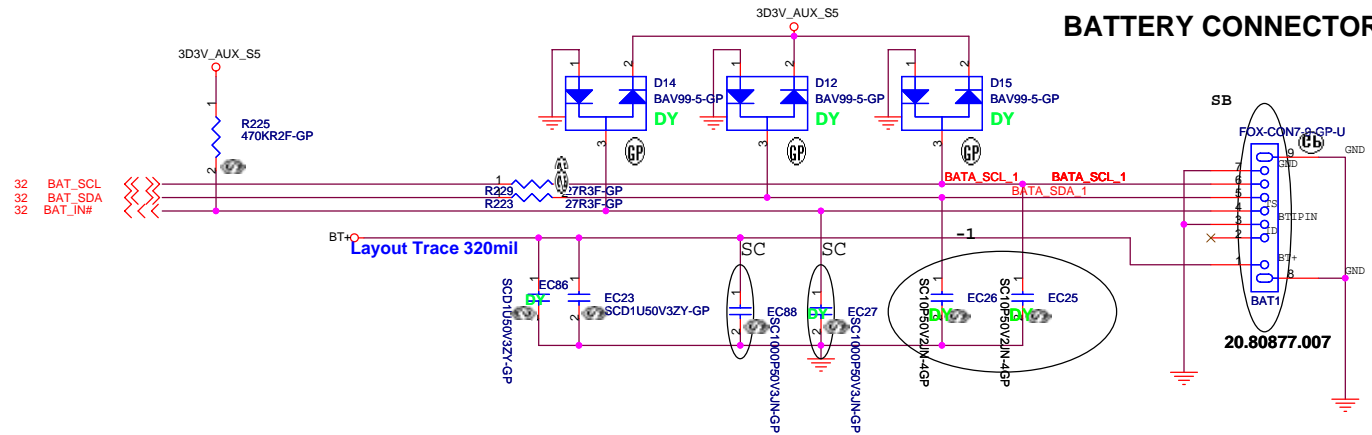
85W/19V 4.47A AC adapter
 When AC adapter
 Current = 4.47A
 R sensor = 20m Ohm
 the ICM Voltage = 19.22x4.47x0.02 = 1.78

ADT_DIFF
 L 90W
 H 65W

Adaptor in to generate DCBATOUT

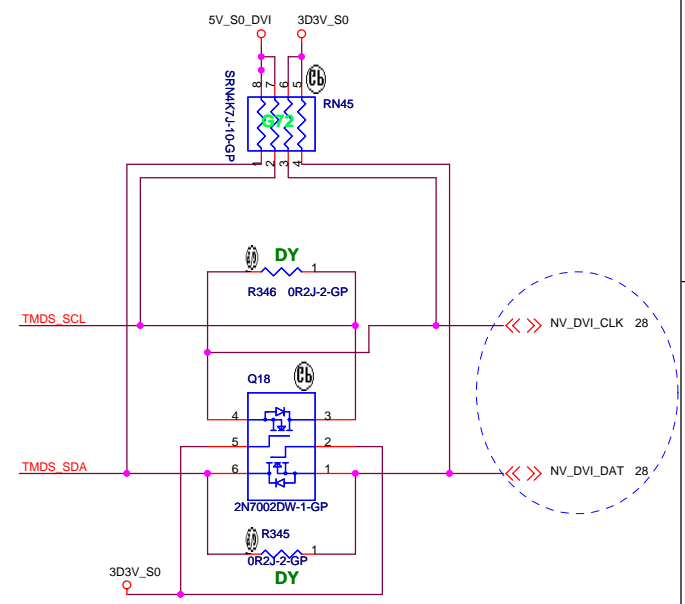
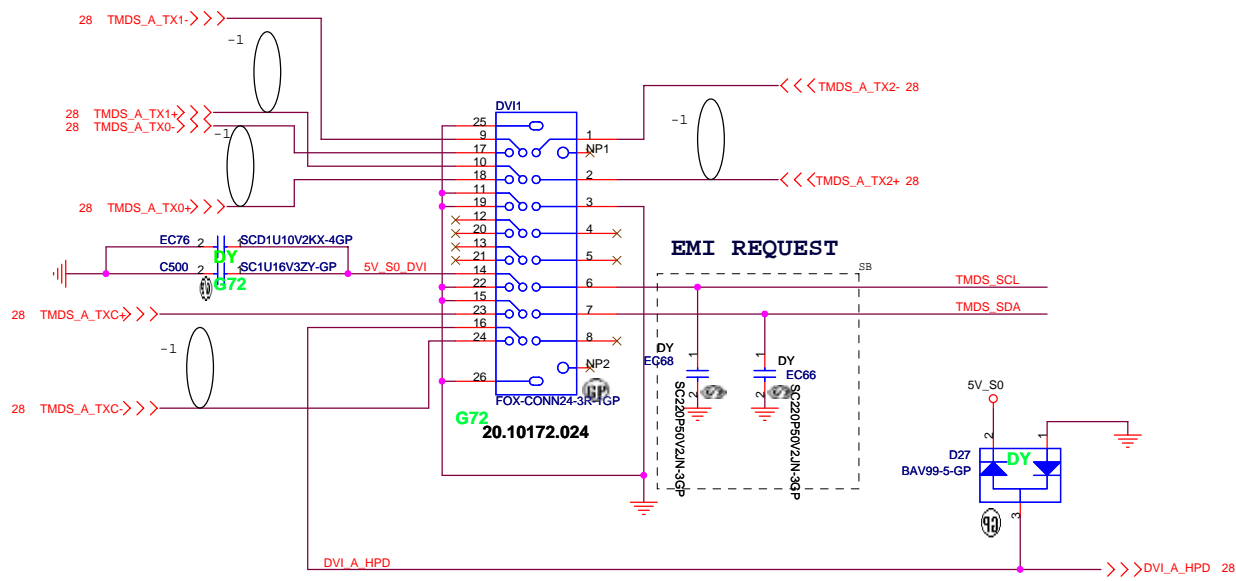


BATTERY CONNECTOR



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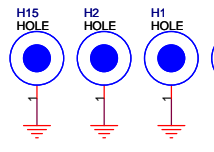
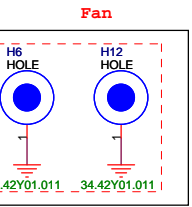
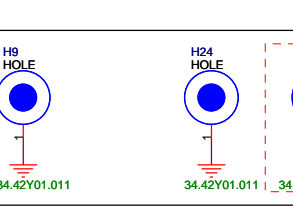
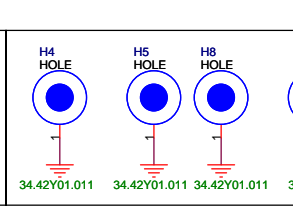
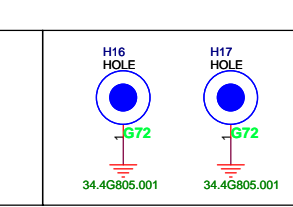
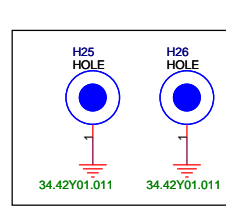
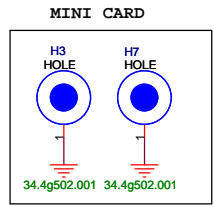
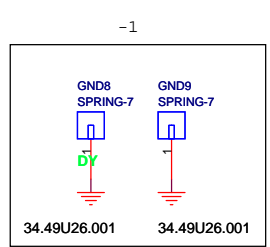
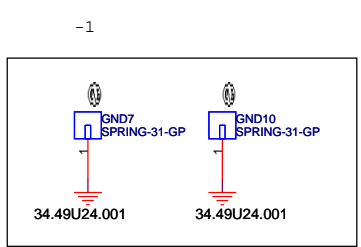
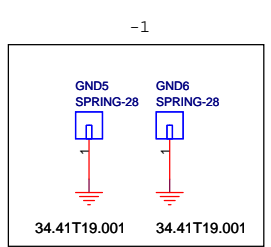
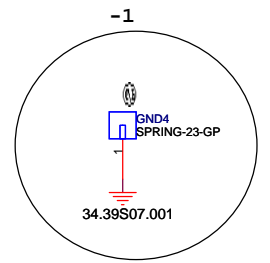
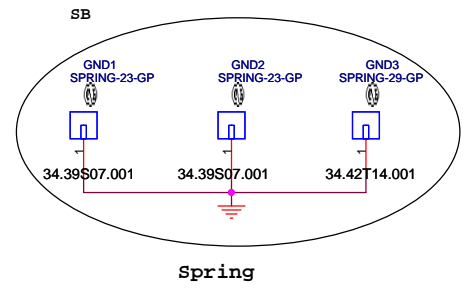
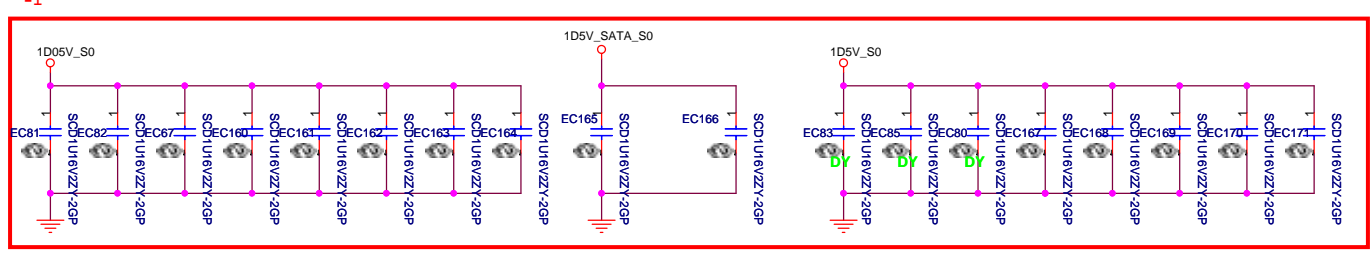
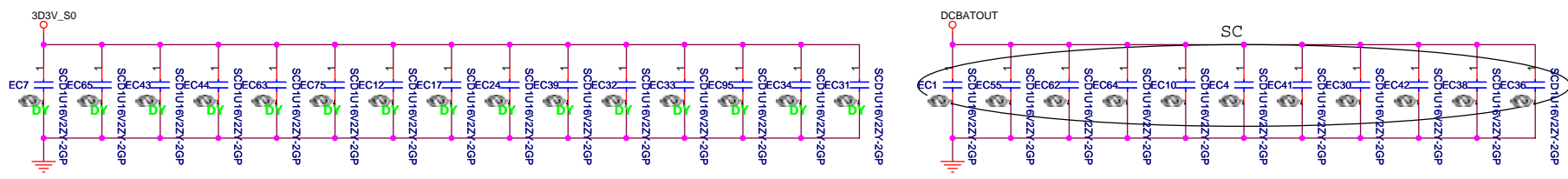
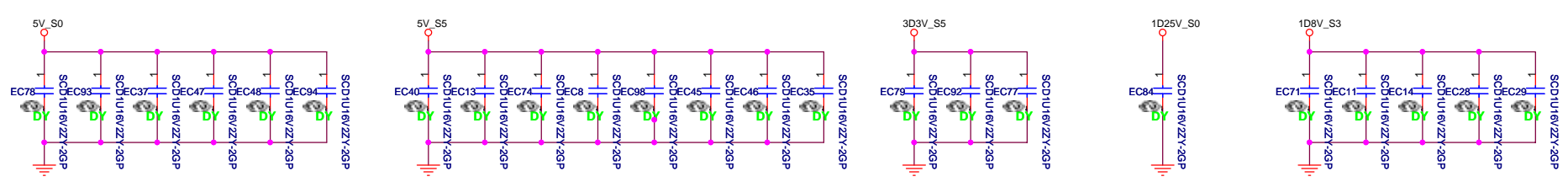
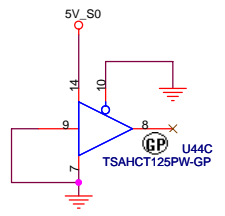
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Title		
AD/BATT CONN		
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<Variant Name>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
DVI CONNECTOR			
Size	Document Number	Rev	
A3	Columbia/Tangiz	-1	
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