

# EA40-CX UMA/Muxless Schematics Document Ivy Bridge Intel PCH

*DY :None Installed*  
*DIS:DIS installed*  
*DIS\_Muxless :BOTH DIS or Muxless installed*  
*DIS\_PX:BOTH DIS or PX installed*  
*DIS\_PX\_Muxless:DIS or PX or Muxless installed.*  
*Muxless: Muxless installed.(PX4.0)*  
*PX:MUX installed.(PX3.0)*  
*PX\_Muxless:BOTH PX or Muxless installed.*  
*UMA:UMA installed*  
*UMA\_Muxless:BOTH UMA or Muxless installed*  
*UMA\_PX\_Muxless:UMA or PX or Muxless installed*

*ANNIE: ONLY FOR ANNIE solution.*  
*PSL: KBC795 PSL circuit for 10mW solution installed.*  
*10mW: External circuit for 10mW solution installed.*  
*65W: for 65W adaptor installed.*  
*90W: for 90W adaptor installed.*

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UMA C

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Title		
Cover Page		
Size A3	Document Number EA40 CX	Rev -3
Date: Thursday, June 06, 2013	Sheet 1	of 103

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Name	Schematics Notes
SPKR	<b>Reboot option at power-up</b> Default Mode: Internal weak Pull-down. <b>No Reboot Mode with TCO Disabled:</b> Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	<b>Enable Danbury:</b> Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. <b>Disable Danbury:</b> Leave floating, no pull-down required.
NV_ALE	<b>Enable Danbury:</b> Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] <b>Disable Danbury:</b> Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	<b>Default = Do not connect (floating)</b> High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	<b>PCI-Express Static Lane Reversal</b>	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		Disabled - No Physical Display Port attached to 1: Embedded DisplayPort. Enabled - An external Display Port device is connect to the EMBEDDED display Port 0: connect to the EMBEDDED display Port	0
CFG[6:5]	<b>PCI-Express Port Bifurcation Straps</b>	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	<b>PEG DEFER TRAINING</b>	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training	

POWER PLANE	VOLTAGE	Voltage Rails		DESCRIPTION
		ACTIVE IN		
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_OPCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0		CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3		
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states		AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN		Legacy WOL
3D3V_AUX_KBC	3.3V	DSW_Sx		ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx		Powered by Li Coin Cell in G3 and +V3ALW in Sx

**USB Table**

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA / USB CHARGER
9	USB Ext. port 2
10	EDP CAMERA
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

**SMBus ADDRESSES**

I <sup>2</sup> C / SMBus Addresses		Ref Des	HURON RIVER ORB Bus	
Device	Address	Hex	Bus	
EC SMBus 1 Battery CHARGER			BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA	
EC SMBus 2 PCH eDP			SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA	
PCH SMBus SO-DIMM1 (SPD) SO-DIMM2 (SPD) Digital Pot G-Sensor MINI			PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK	

**PCIE Routing**

LANE1	Mini Card2(WWAN)
LANE2	Mini Card1(WLAN)
LANE3	Card Reader
LANE4	Onboard LAN
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	New Card

**SATA Table**

SATA	
Pair	Device
0	HDD1
1	N/A
2	N/A
3	N/A
4	ODD
5	ESATA

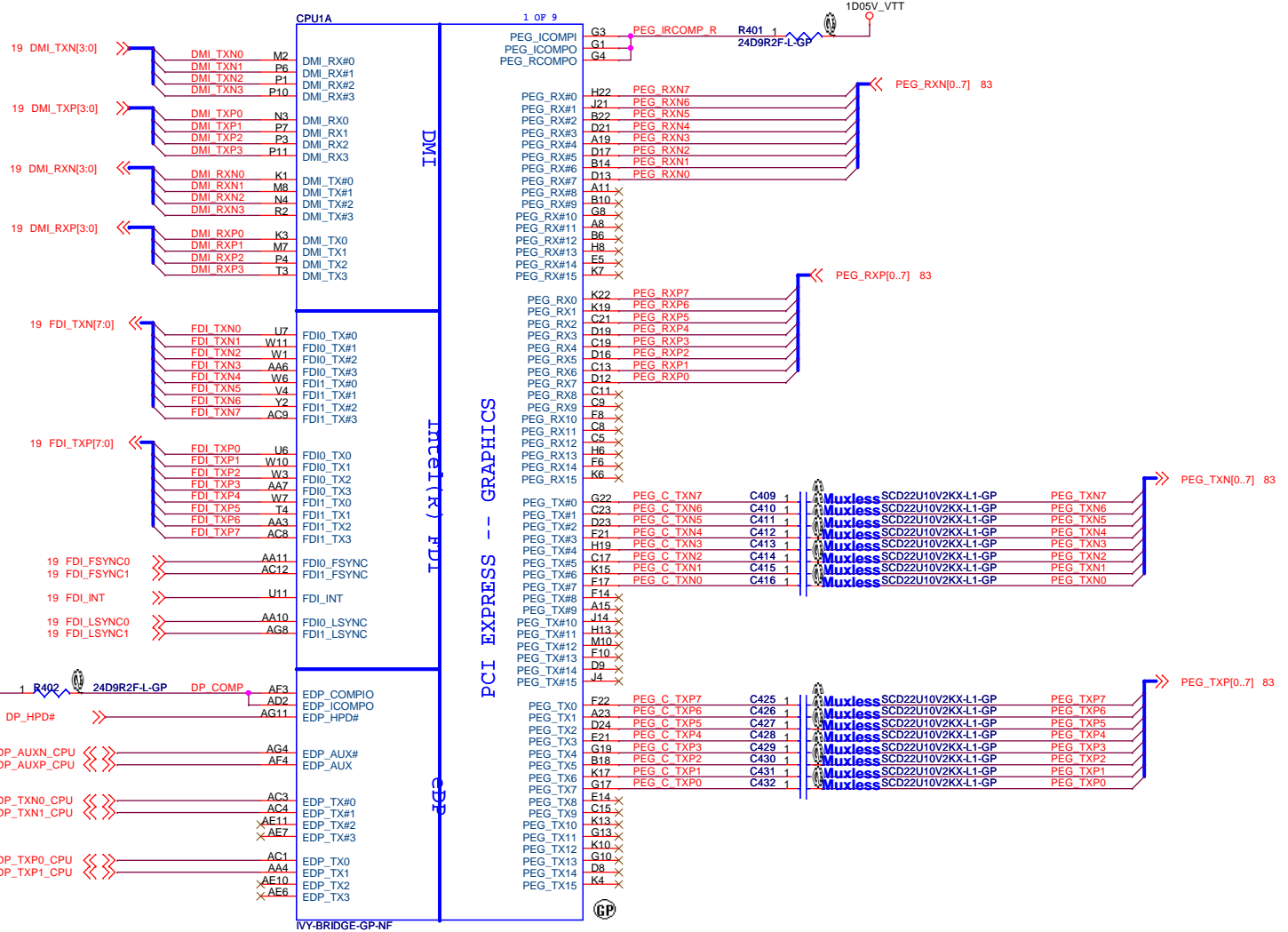
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Table of Content

SSID = CPU



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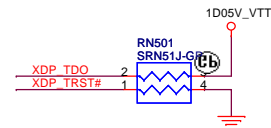
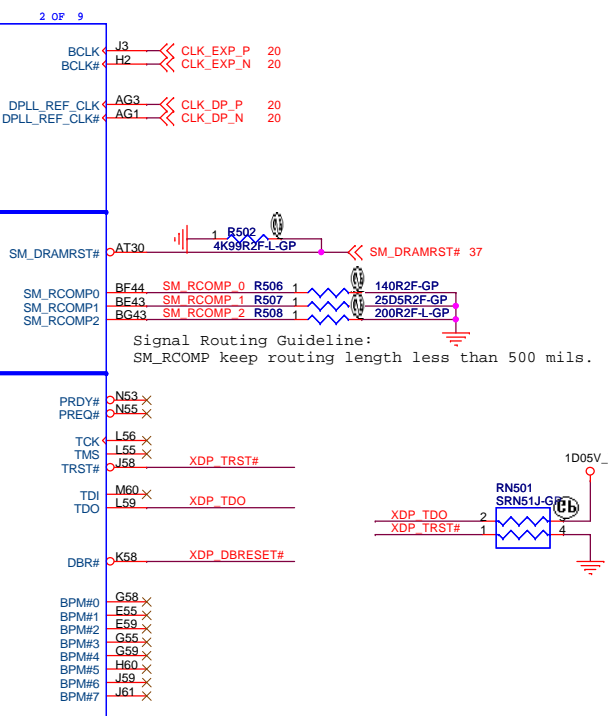
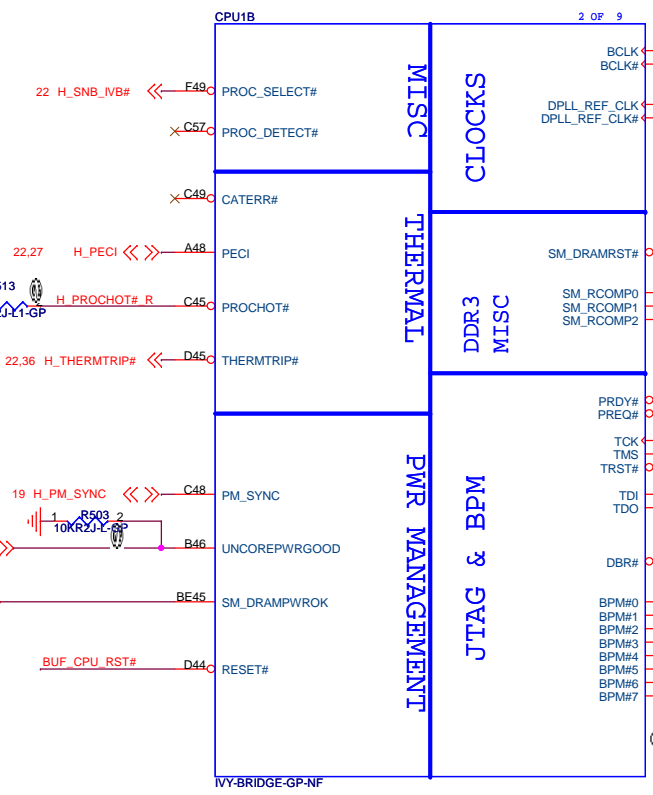
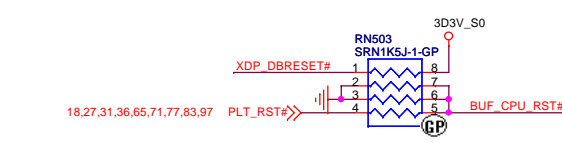
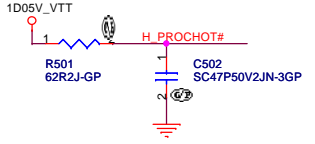
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Title: CPU (PCIe/DMI/FDI)

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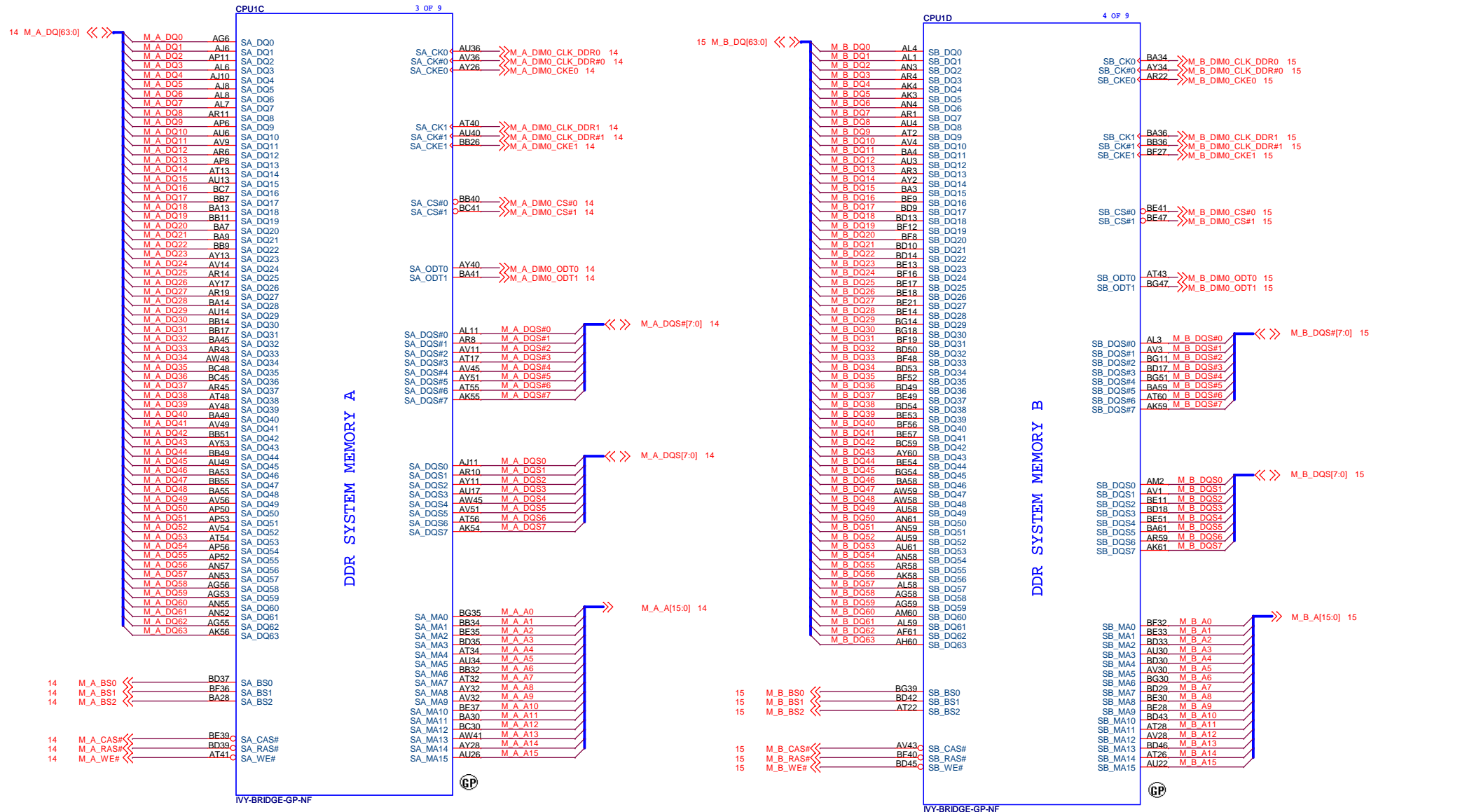
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Title CPU (THERMAL/CLOCK/PM)		
Size Custom	Document Number EA40 CX	Rev -3
Date: Thursday, June 20, 2013	Sheet 5 of	103



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Title: CPU (DDR)

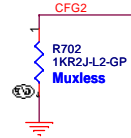
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Date: Thursday, June 20, 2013 Sheet 6 of 103

# SSID = CPU

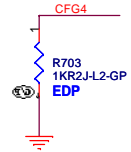
## PEG Static Lane Reversal

CFG2 1: Normal Operation; Lane # definition matches socket pin map definition  
0: Lane Reversed



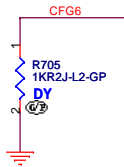
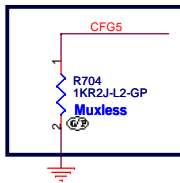
## Enabl EDP function

CFG4 1: Disable  
0: Enable



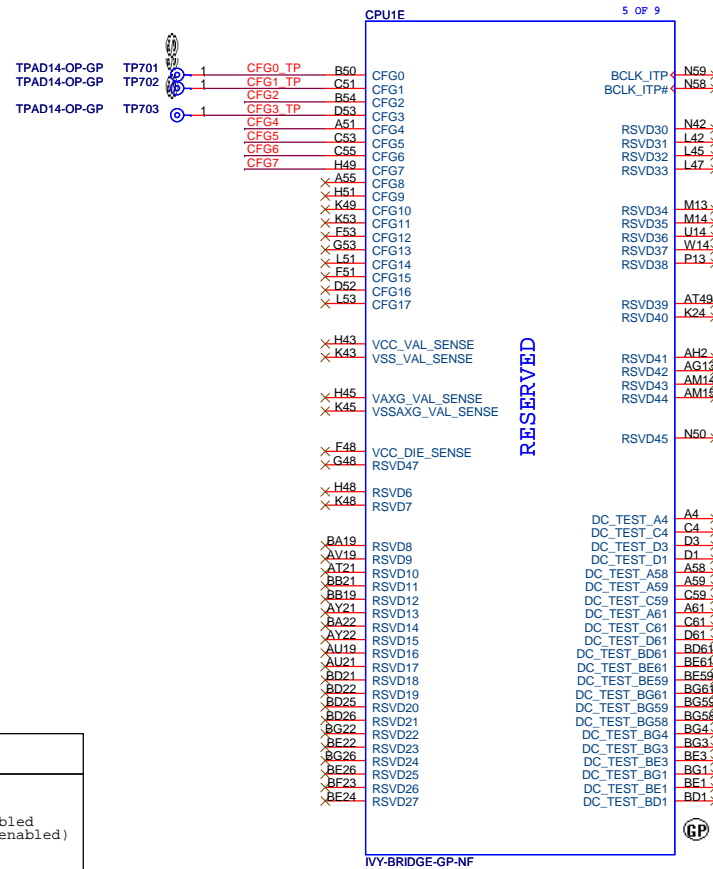
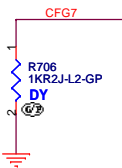
## PCIe Port Bifurcation Straps

CFG[6:5] 11: x16 - Device 1 functions 1 and 2 disabled  
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled  
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)  
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



## PEG DEFER TRAINING

CFG7 1: PEG Train immediately following xxRESETB de assertion  
0: PEG Wait for BIOS for training



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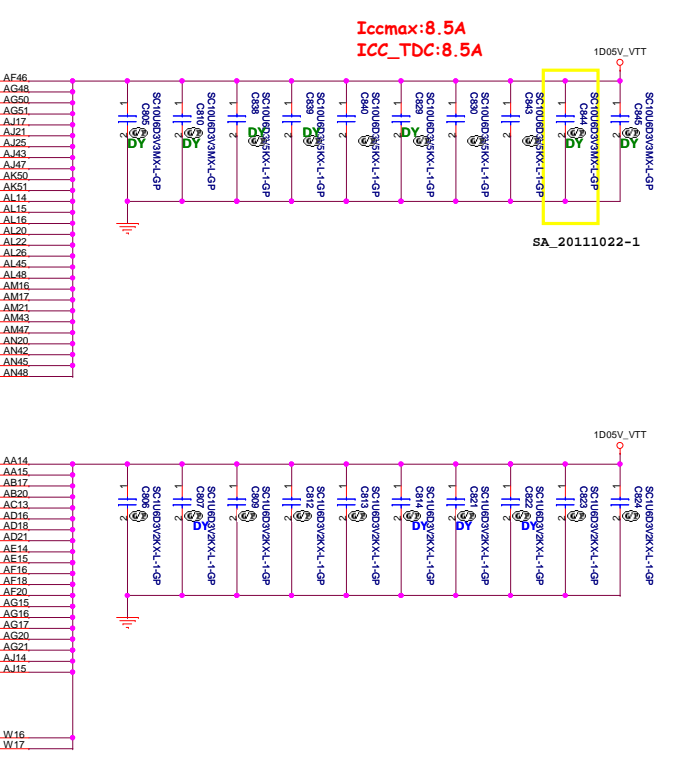
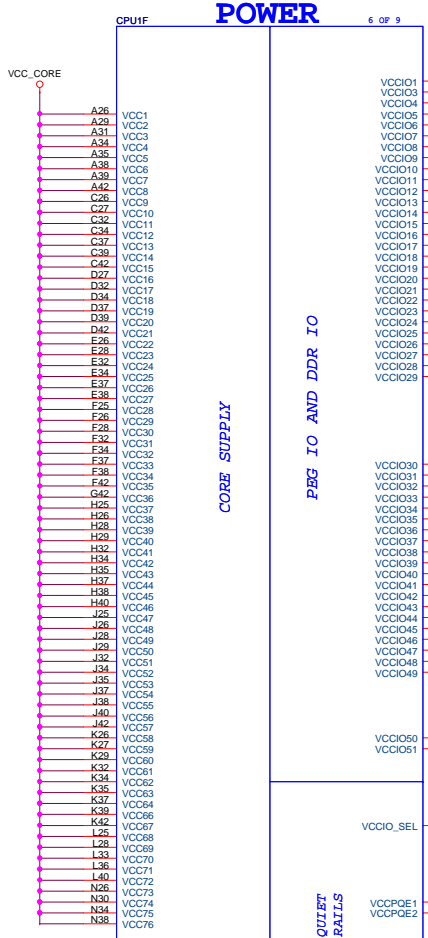
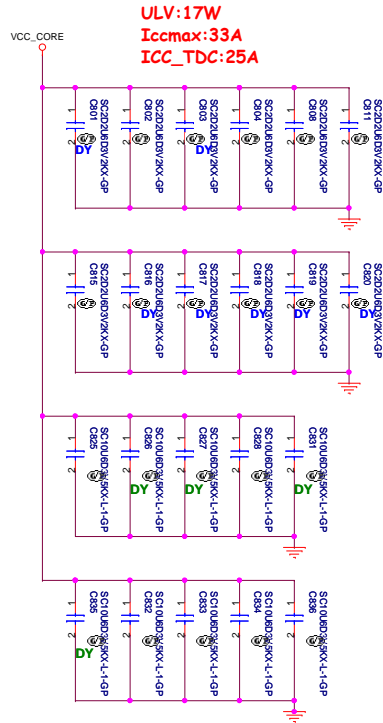
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Size	Document Number				Rev
A3	<b>EA40 CX</b>				<b>-3</b>
Date:	Thursday, June 06, 2013	Sheet	7	of	103

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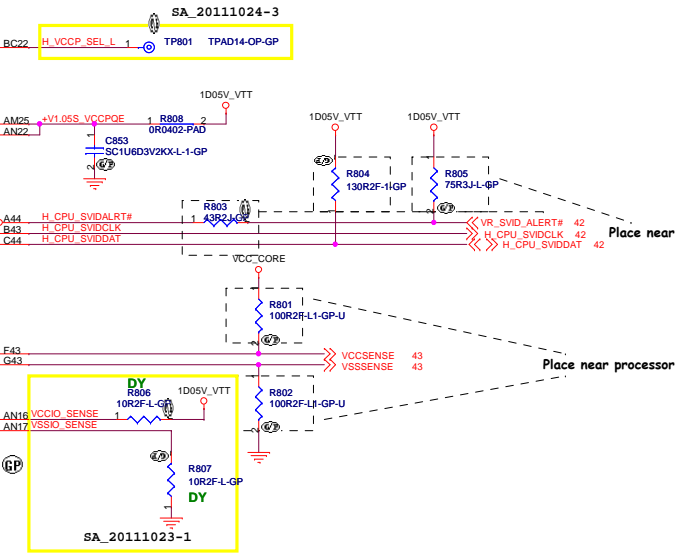
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Iccmax:8.5A  
ICC\_TDC:8.5A

SA\_20111022-1

1D05V\_VTT



Place near processor

Place near processor

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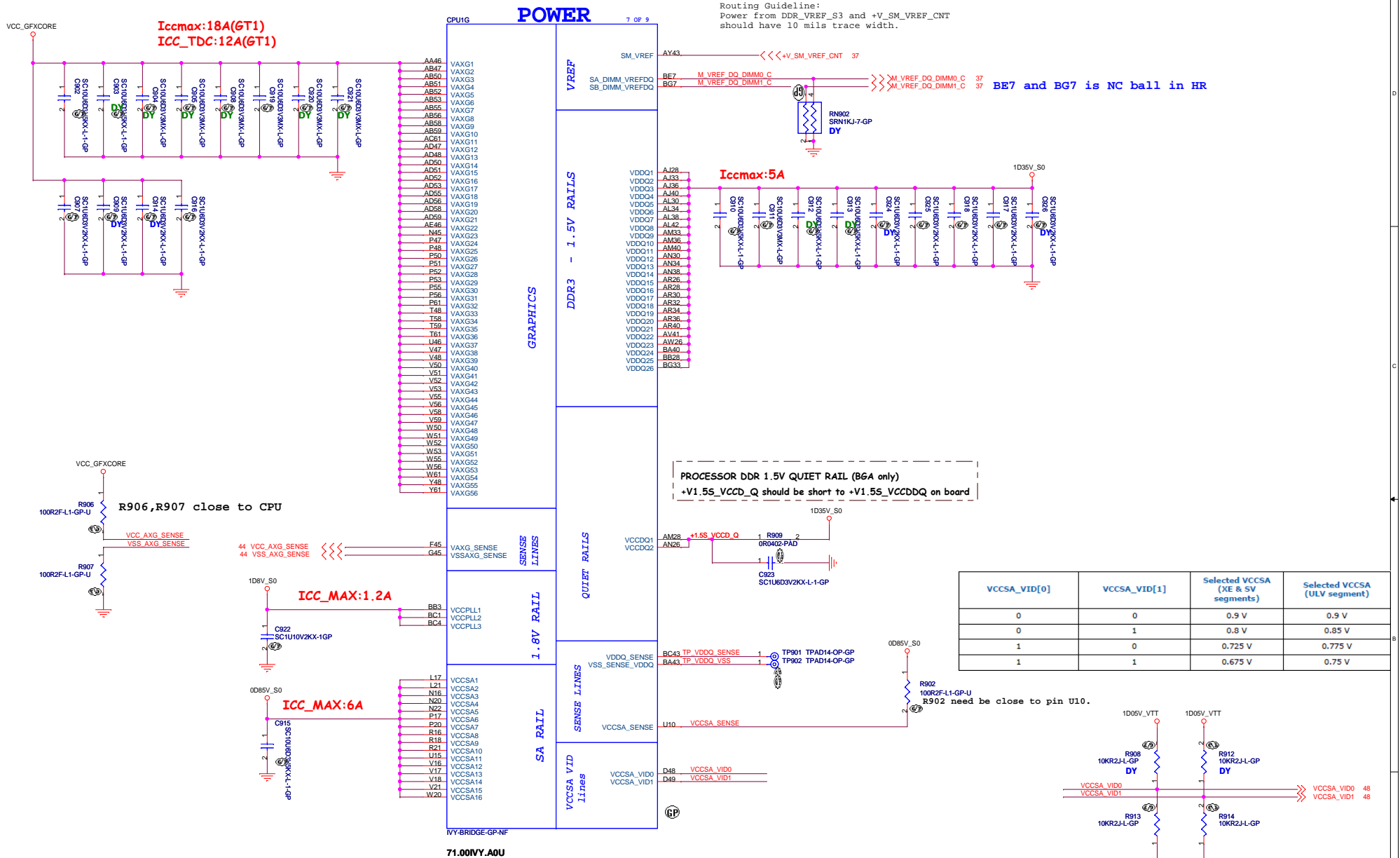
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Title		
CPU (VCC CORE)		
Size	Document Number	Rev
Custom	EA40 CX	-3
Date:	Thursday, June 20, 2013	Sheet 8 of 103

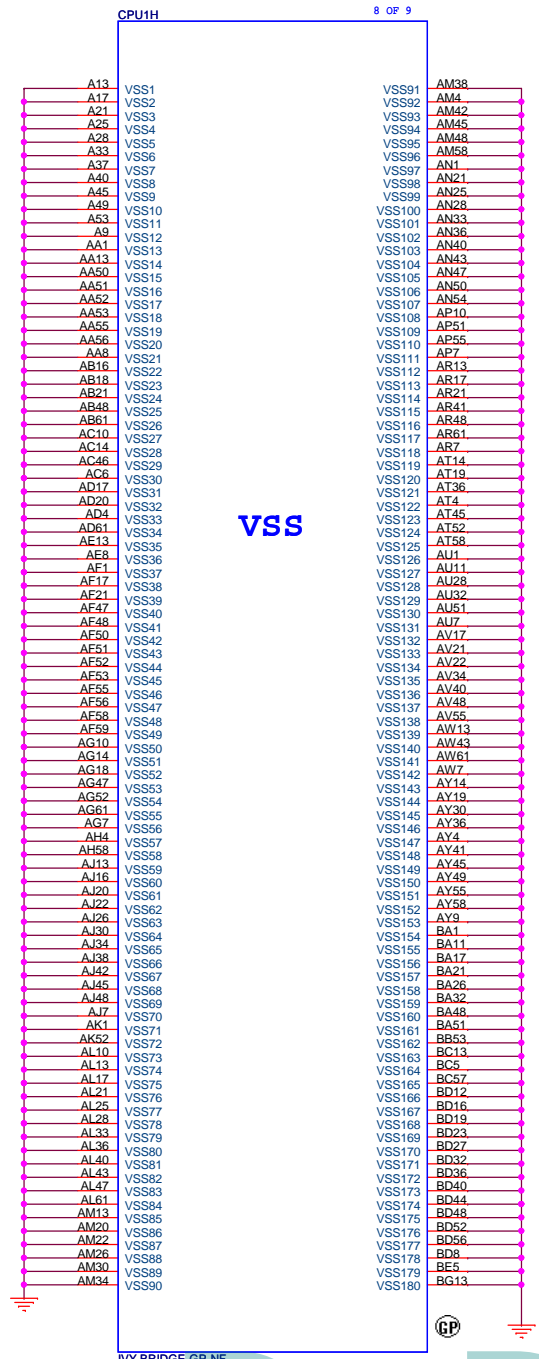
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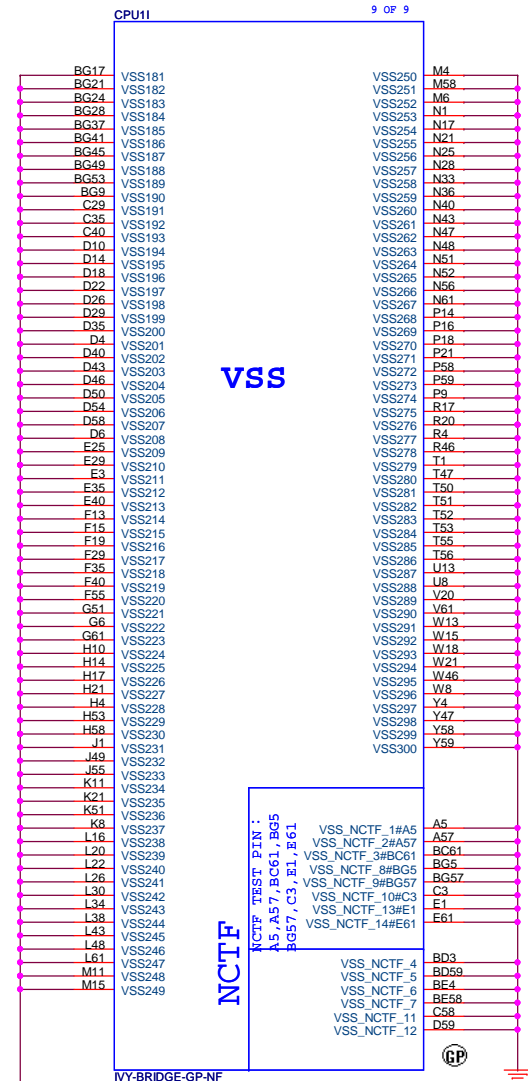


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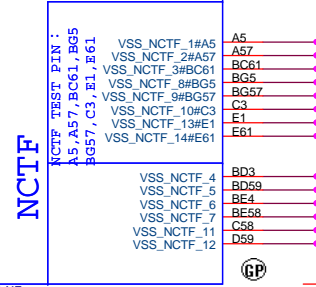
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A3	<b>EA40 CX</b>	<b>-3</b>
Date:	Thursday, June 06, 2013	Sheet 10 of 103



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A3	<b>EA40_CX</b>	<b>-3</b>	
Date:	Thursday, June 06, 2013	Sheet	11 of 103





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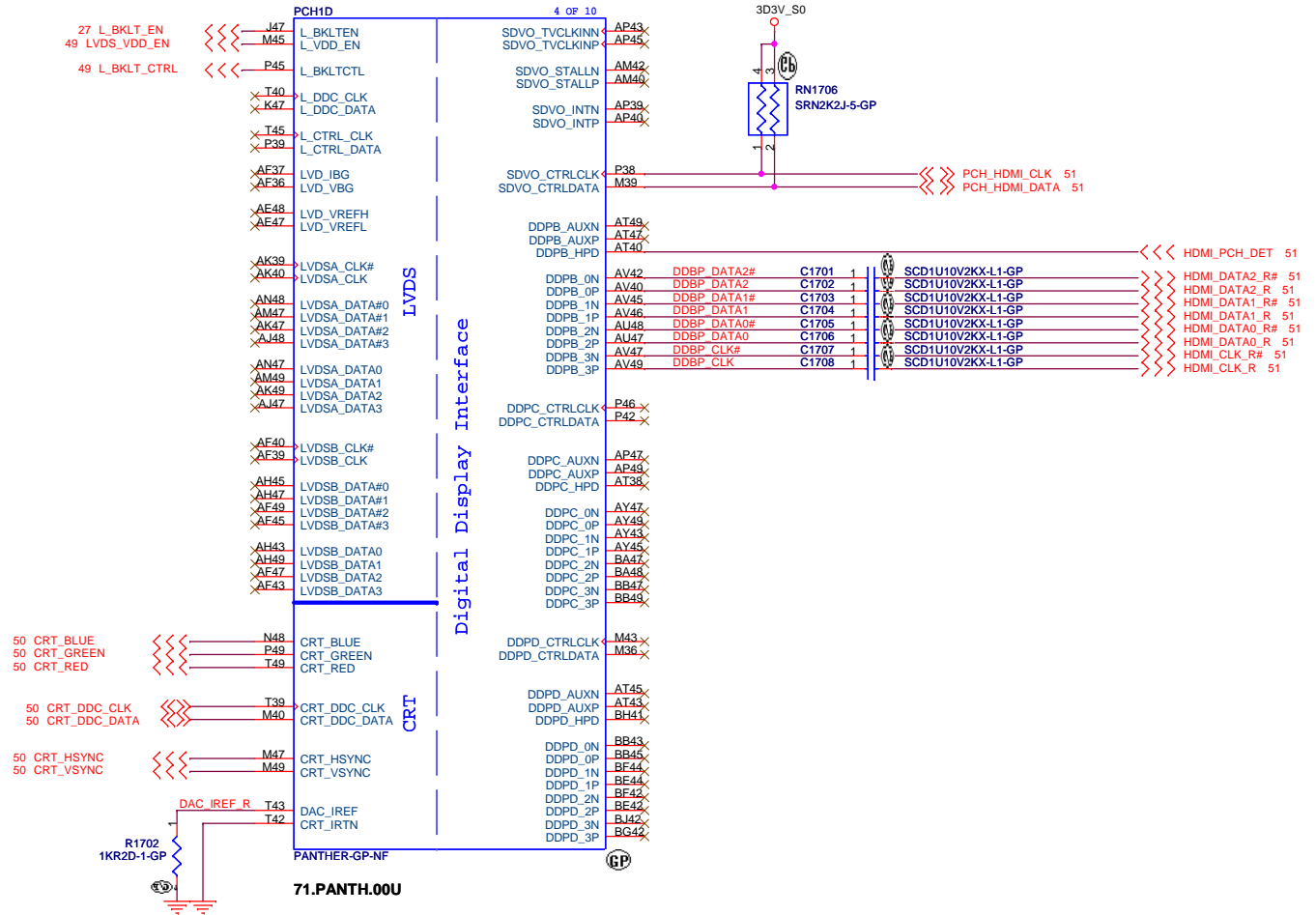
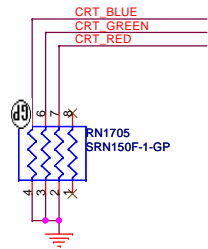
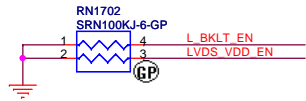
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Size	Document Number	Rev
A4	<b>EA40 CX</b>	<b>-3</b>
Date:	Thursday, June 06, 2013	Sheet 16 of 103

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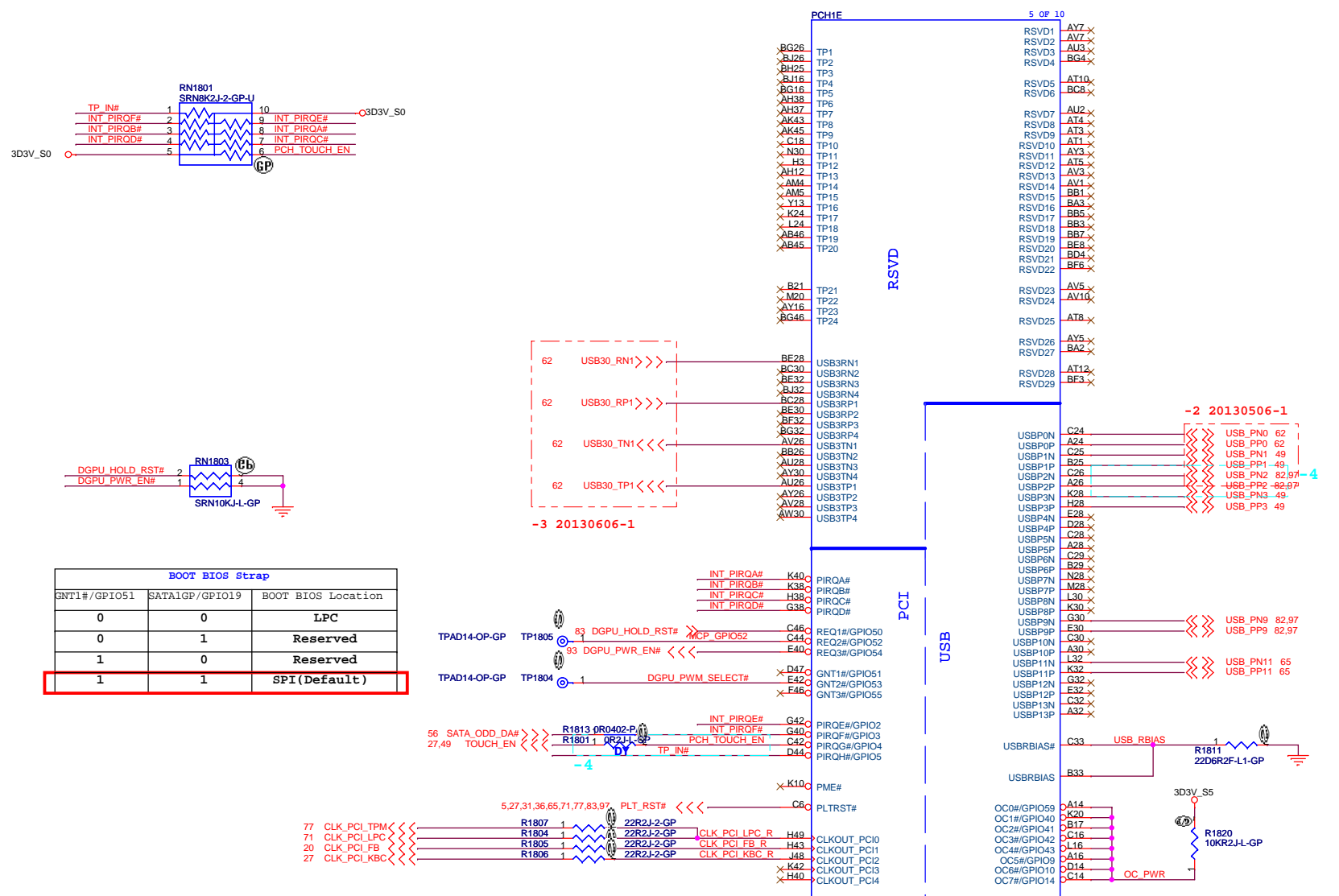
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Title: **PCH (LVDS/CRT/DDI)**

Size A3 Document Number: **EA40 CX** Rev: **-3**

Date: Thursday, June 20, 2013 Sheet 17 of 103



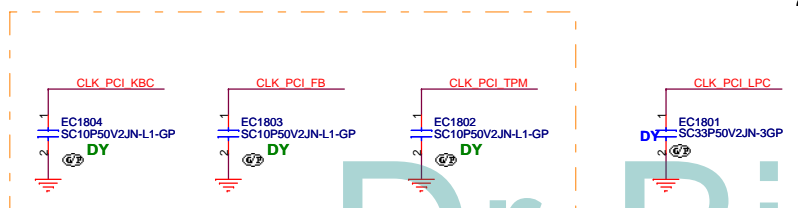


BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

USB Table

Pair	Device
0	USB2.0/USB3.0 Ext. port 1
1	Touch panel -3 20130606-1
2	USB2.0 Ext. port 1
3	CCD
4	
5	
6	may not be available
7	may not be available
8	
9	USB2.0 Ext. port 3
10	
11	Mini Card1 (WLAN+BT)
12	
13	

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Title: **PCH (PCI/USB/NVRAM)**

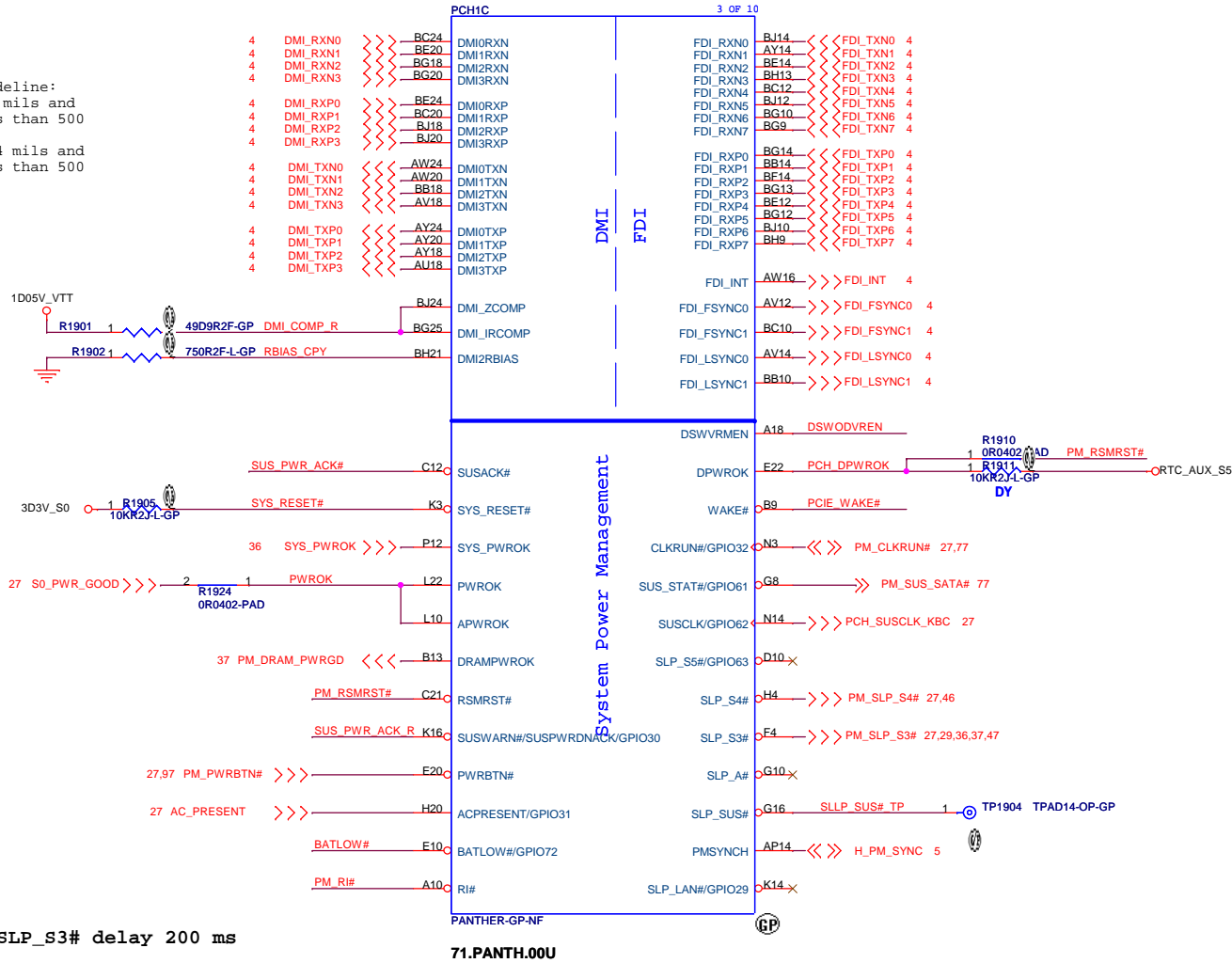
Size: Document Number **EA40 CX** Rev **-3**

Date: Friday, June 21, 2013 Sheet 18 of 103

**SSID = PCH**



Signal Routing Guideline:  
 DMI\_ZCOMP keep W=4 mils and routing length less than 500 mils.  
 DMI\_IRCOMP keep W=4 mils and routing length less than 500 mils.

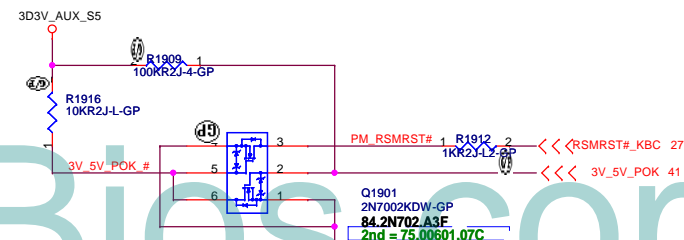
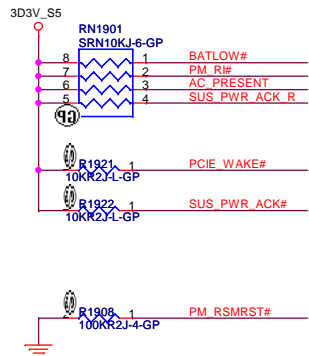


DSWODVREN - On Die DSW VR Enable

HIGH	Enabled (DEFAULT)
LOW	Disabled



S0\_PWR\_GOOD after PM\_SLP\_S3# delay 200 ms



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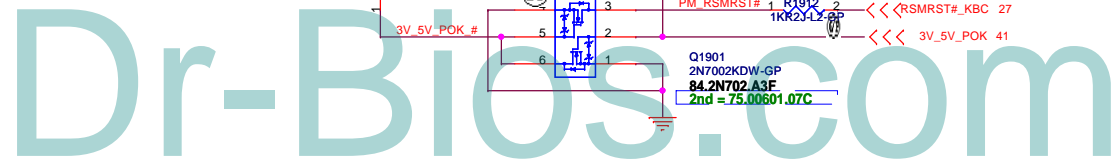
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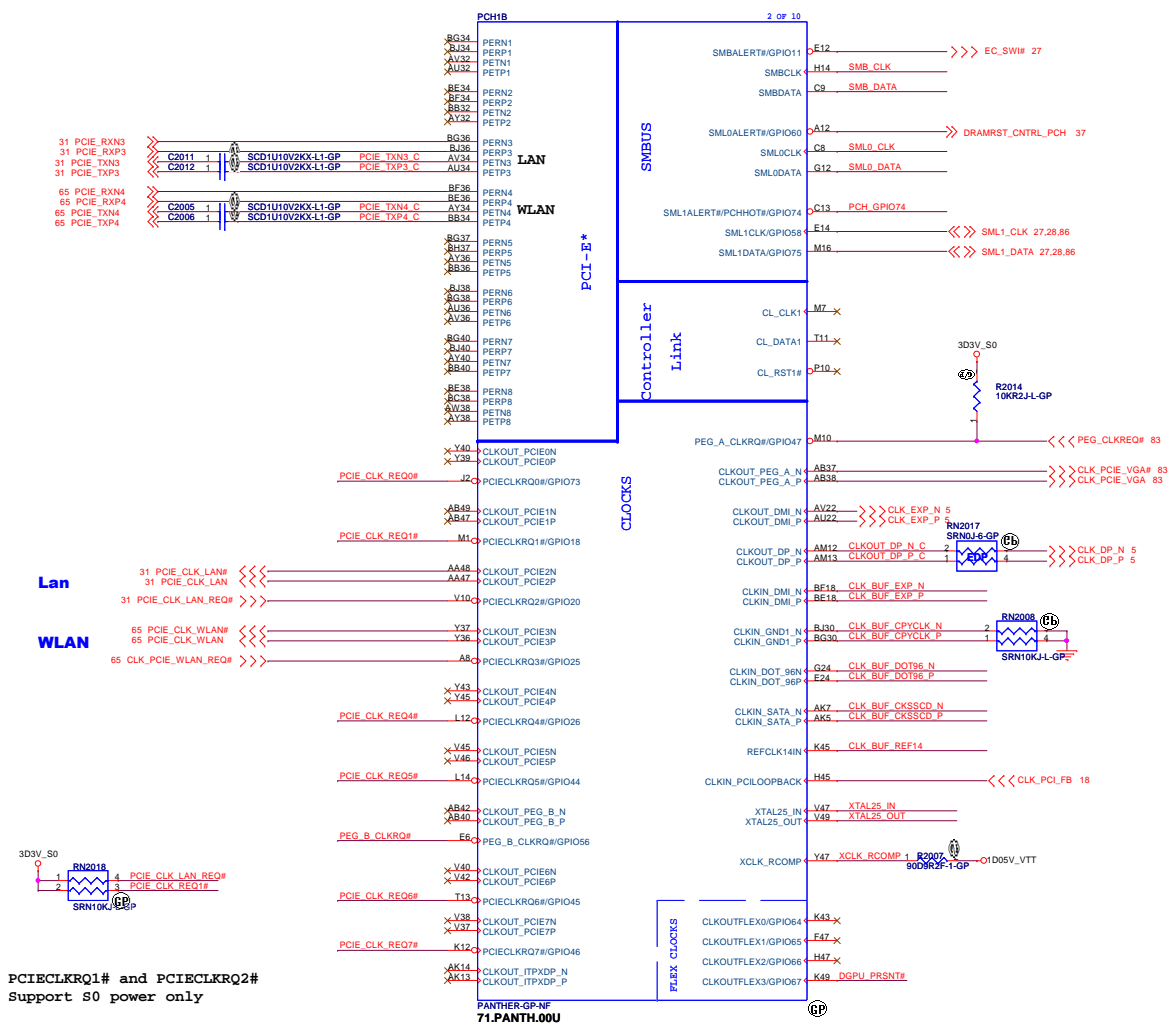
Title: **PCH (DM I/FDI/PM)**

Size A3 Document Number: **EA40 CX** Rev: **-3**

Date: Friday, June 21, 2013 Sheet 19 of 103



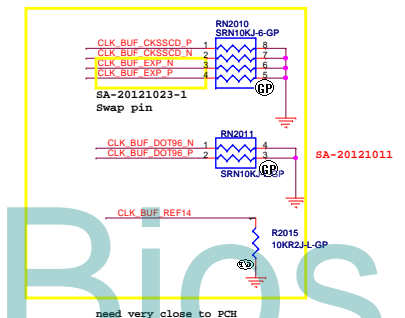
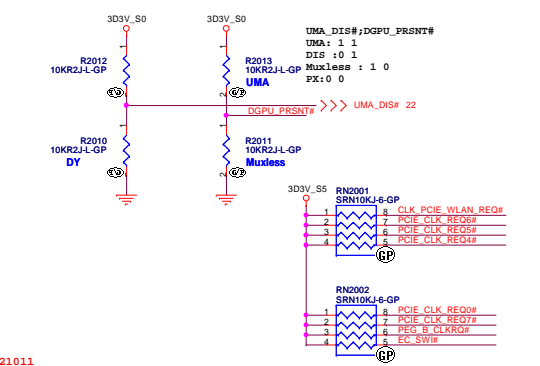
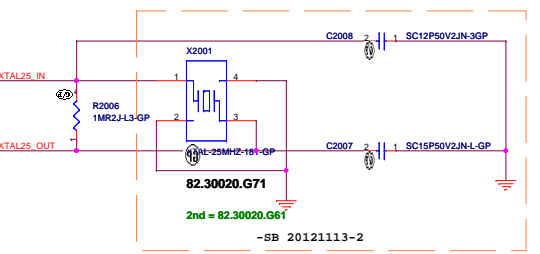
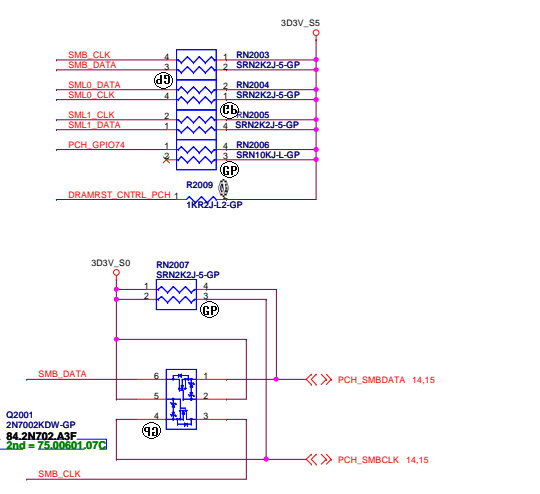
**SSID = PCH**



**Lan**  
31 PCIE\_CLK\_LAN# <<<<  
31 PCIE\_CLK\_LAN <<<<  
31 PCIE\_CLK\_LAN\_REQ# <<<<

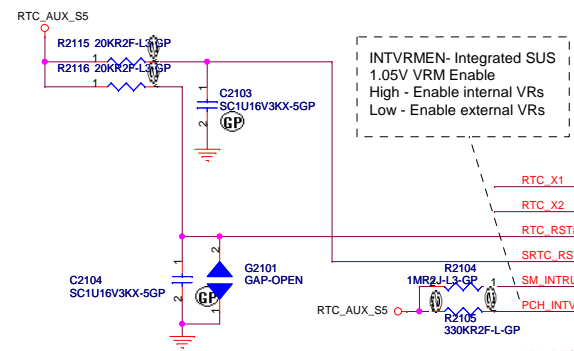
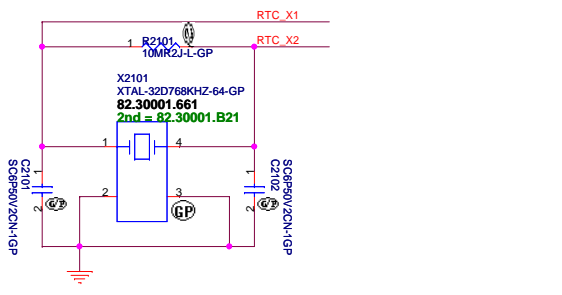
**WLAN**  
65 PCIE\_CLK\_WLAN# <<<<  
65 PCIE\_CLK\_WLAN <<<<  
65 CLK\_PCIE\_WLAN\_REQ# <<<<

PCIECLKRQ1# and PCIECLKRQ2#  
Support S0 power only

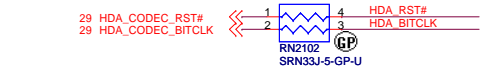
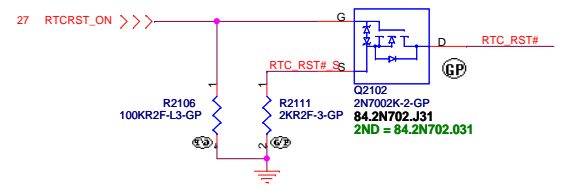


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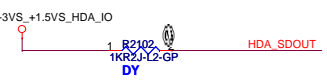
**SSID = PCH**



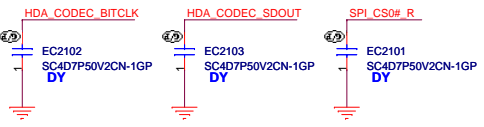
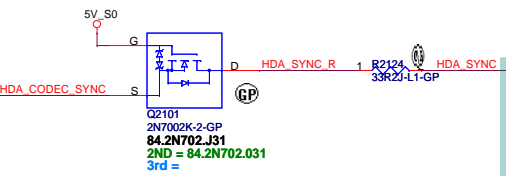
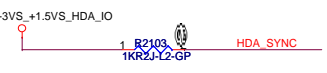
**RTC Reset**



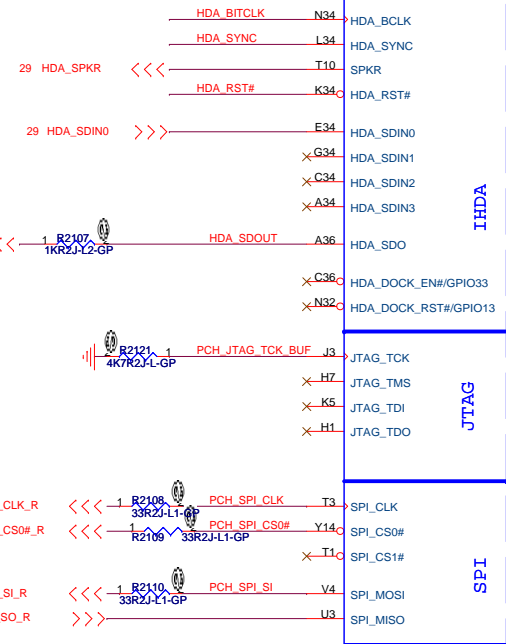
Flash Descriptor Security Override	
HDA_SDOUT	Low = Default High = Enable



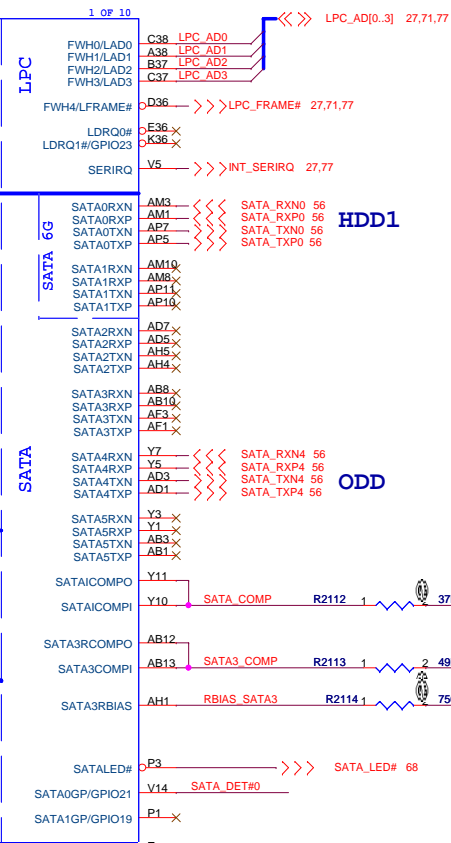
PLL ODVR VOLTAGE	
HDA_SYNC	Low = 1.8V (Default) High = 1.5V



**HDA\_SYNC:** This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA\_SYNC from the Audio Codec device until after the Strap sampling is complete.



71.PANTH.00U



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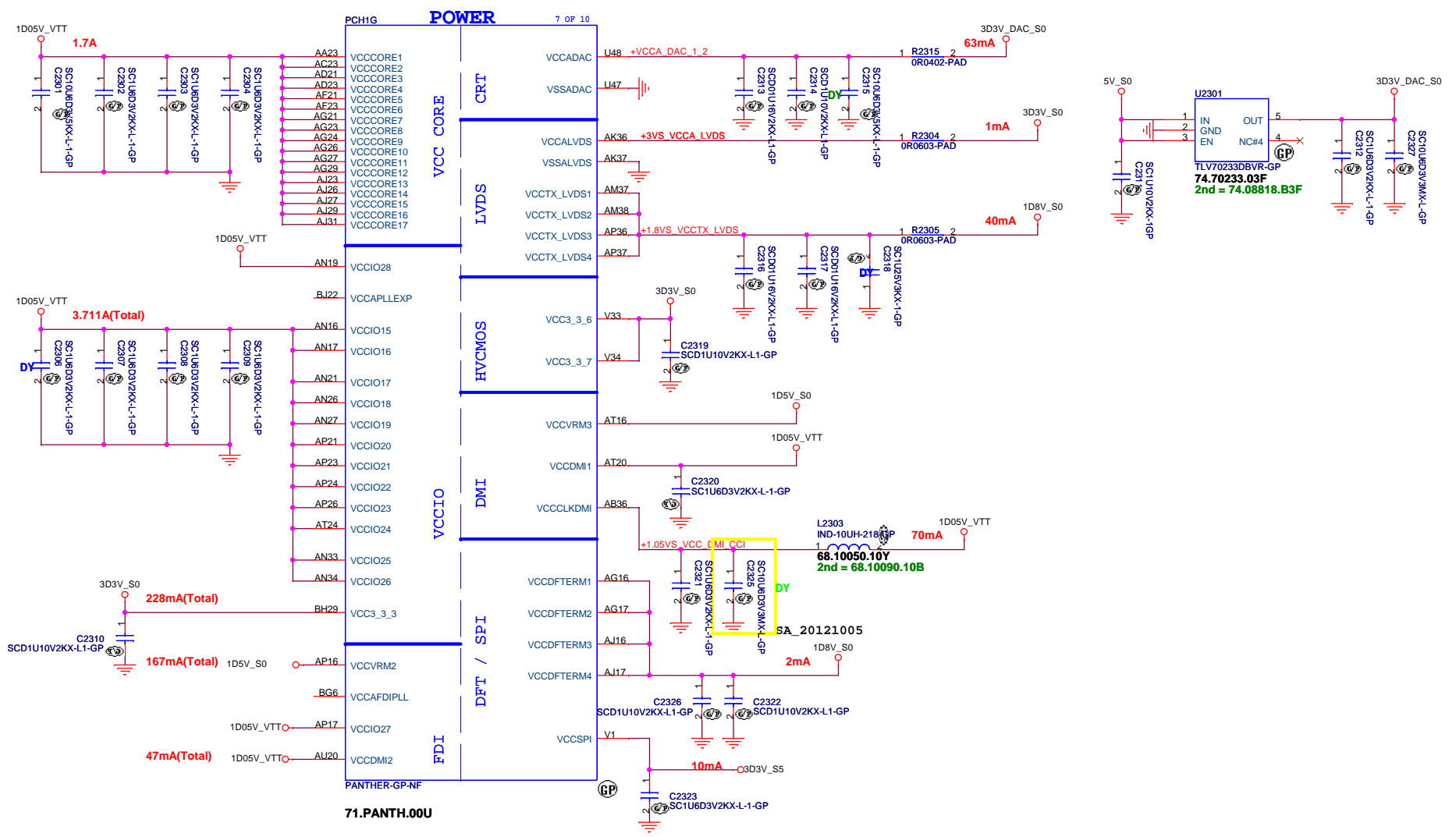
**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (SPI/RTC/LPC/SATA/IHDA)**

Size: Custom Document Number: **EA40 CX** Rev: **-3**

Date: Thursday, June 20, 2013 Sheet: 21 of 103





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Title: **PCH (POWER1)**

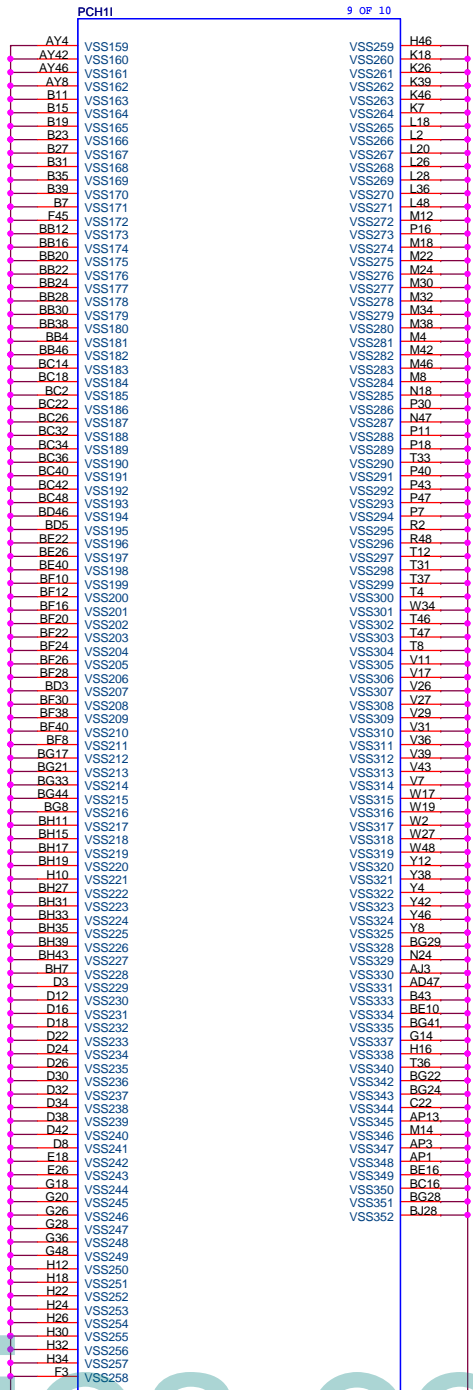
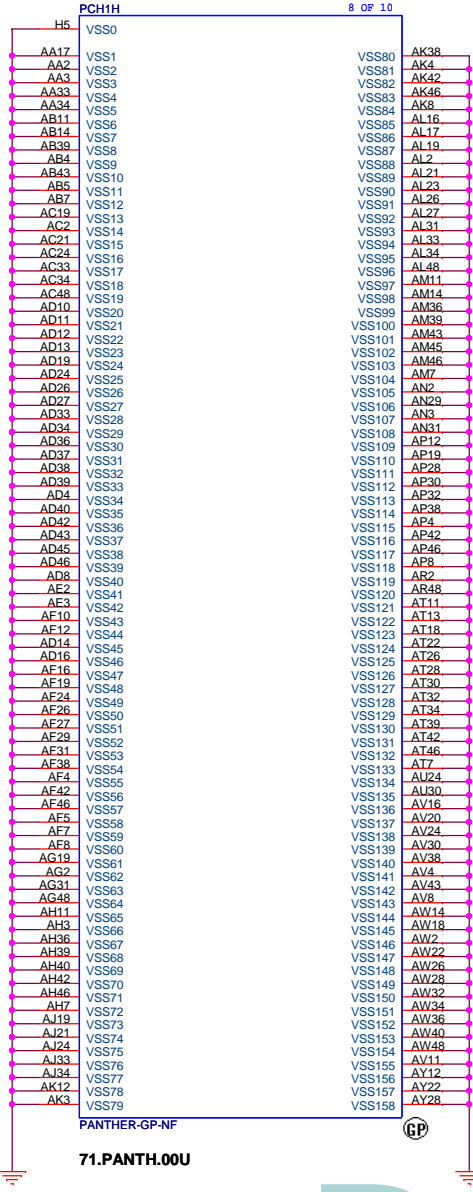
Size A3 Document Number: **EA40 CX** Rev: **-3**

Date: Friday, June 21, 2013 Sheet 23 of 103





SSID = PCH



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Title: **PCH (VSS)**

Size A3 Document Number: **EA40 CX** Rev: **-3**

Date: Thursday, June 06, 2013 Sheet 25 of 103

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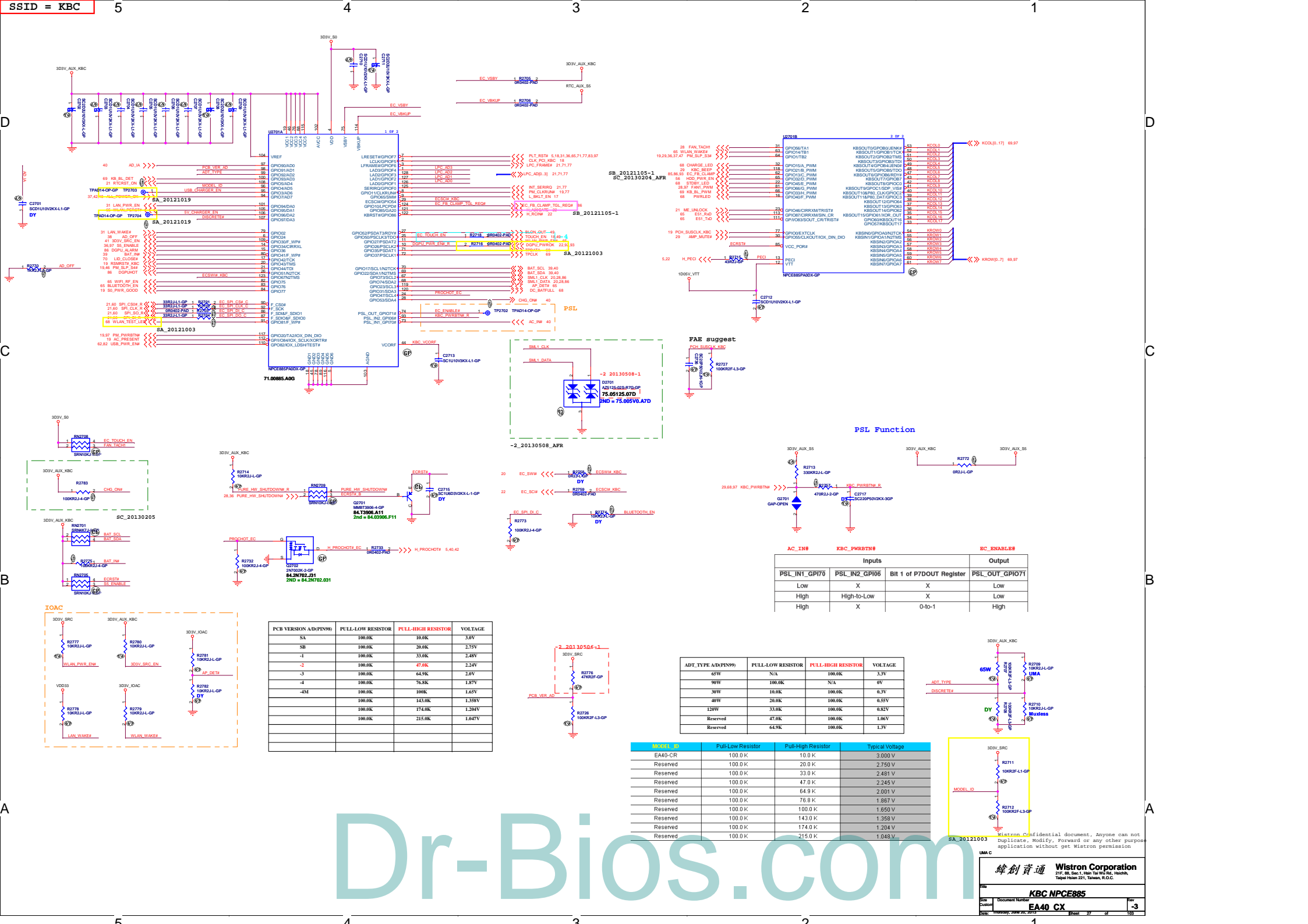
UMA C

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Title **Clock(colay)**

Size A4	Document Number <b>EA40 CX</b>	Rev <b>-3</b>
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PCB VERSION A/D/PIN#	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100.0K	10.0K	1.8V
SB	100.0K	20.0K	1.75V
-1	100.0K	33.0K	1.48V
-2	100.0K	47.0K	1.24V
-3	100.0K	64.9K	1.24V
-4	100.0K	76.5K	1.87V
-4M	100.0K	100K	1.65V
	100.0K	143.0K	1.358V
	100.0K	174.0K	1.204V
	100.0K	215.0K	1.047V

ADT_TYPE A/D/PIN#	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
65W	N/A	100.0K	1.3V
90W	100.0K	N/A	0V
30W	10.0K	100.0K	0.3V
40W	20.0K	100.0K	0.55V
120W	33.0K	100.0K	0.82V
Reserved	47.0K	100.0K	1.06V
Reserved	64.9K	100.0K	1.3V

Model ID	Pull-Low Resistor	Pull-High Resistor	Typical Voltage
EA40-CR	100.0 K	10.0 K	3.000 V
Reserved	100.0 K	20.0 K	2.750 V
Reserved	100.0 K	33.0 K	2.481 V
Reserved	100.0 K	47.0 K	2.245 V
Reserved	100.0 K	64.9 K	2.001 V
Reserved	100.0 K	76.8 K	1.867 V
Reserved	100.0 K	100.0 K	1.650 V
Reserved	100.0 K	143.0 K	1.358 V
Reserved	100.0 K	174.0 K	1.204 V
Reserved	100.0 K	215.0 K	1.048 V

	Inputs		Output	
	PSL_IN1_GPI70	PSL_IN2_GPI06	BIT 1 of P7DOUT Register	PSL_OUT_GPI071
Low	X		X	Low
High	High-to-Low		X	Low
High	X		0-to-1	High

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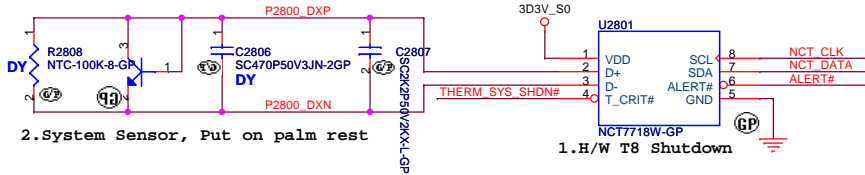
UMC  
**緯創資通** Wistron Corporation  
 21F, 88, Sec.1, Hsin Tai Wu Rd, Hsinshu, Taipei 10621, Taiwan, R.O.C.  
 Doc: KBC NPCE85  
 EA40 CX  
 Rev: 3  
 Date: 2012/09/27 Page: 27 of 103

**SSID = Thermal**

# Thermal sensor NCT 7718W

Layout notice :  
Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

Q2801  
PMB3904-1-GP  
84.03904.L06



2. System Sensor, Put on palm rest

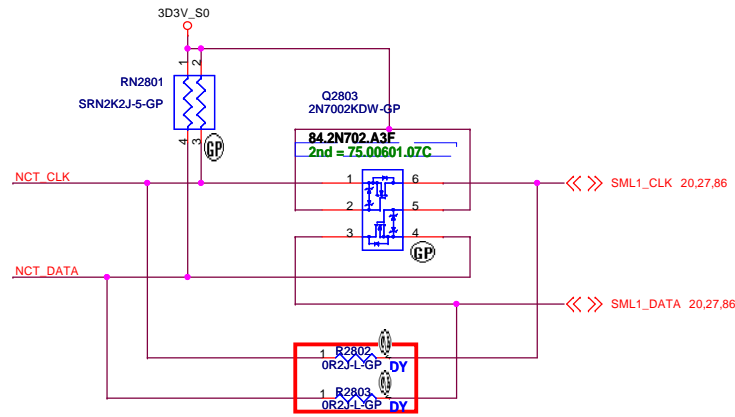
1. H/W T8 Shutdown

ALERT# /T CRIT#  
Pull-up Resistor

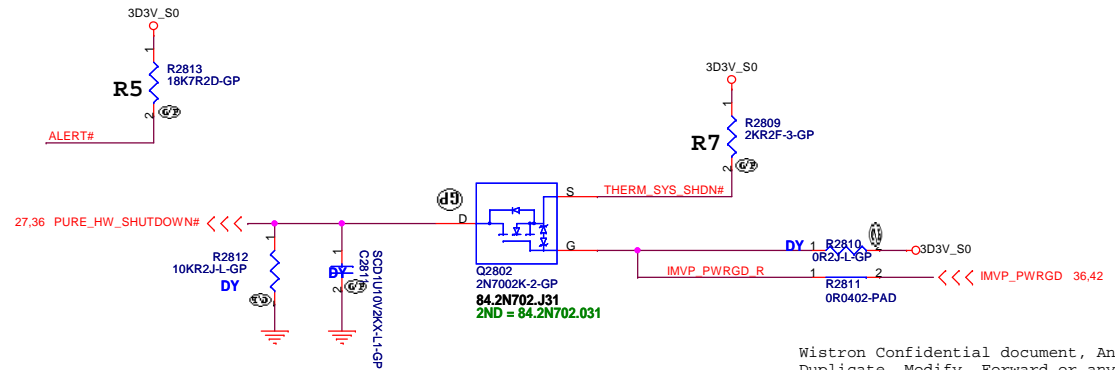
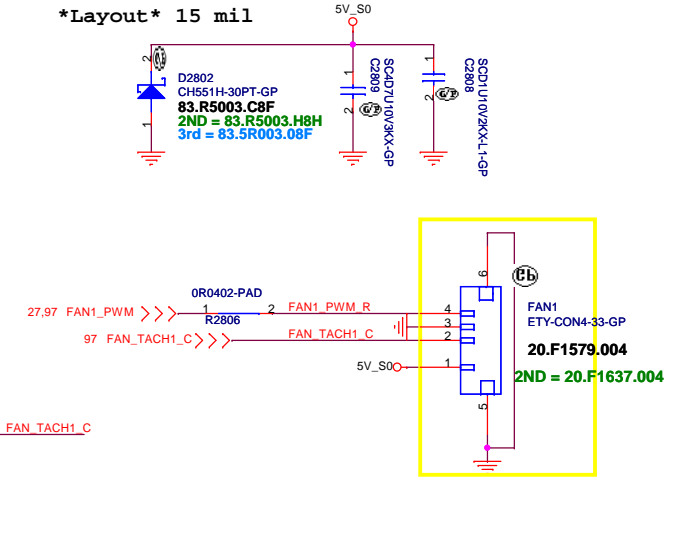
R5	R7				
	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
2Kohm	77°C	87°C	97°C	107°C	117°C
7.5Kohm	79°C	89°C	99°C	109°C	119°C
10.5Kohm	81°C	91°C	101°C	111°C	121°C
14Kohm	83°C	93°C	103°C	113°C	123°C
18.7Kohm	85°C	95°C	105°C	115°C	125°C

T\_CRIT temperature strapping point

SB T8=85 degree



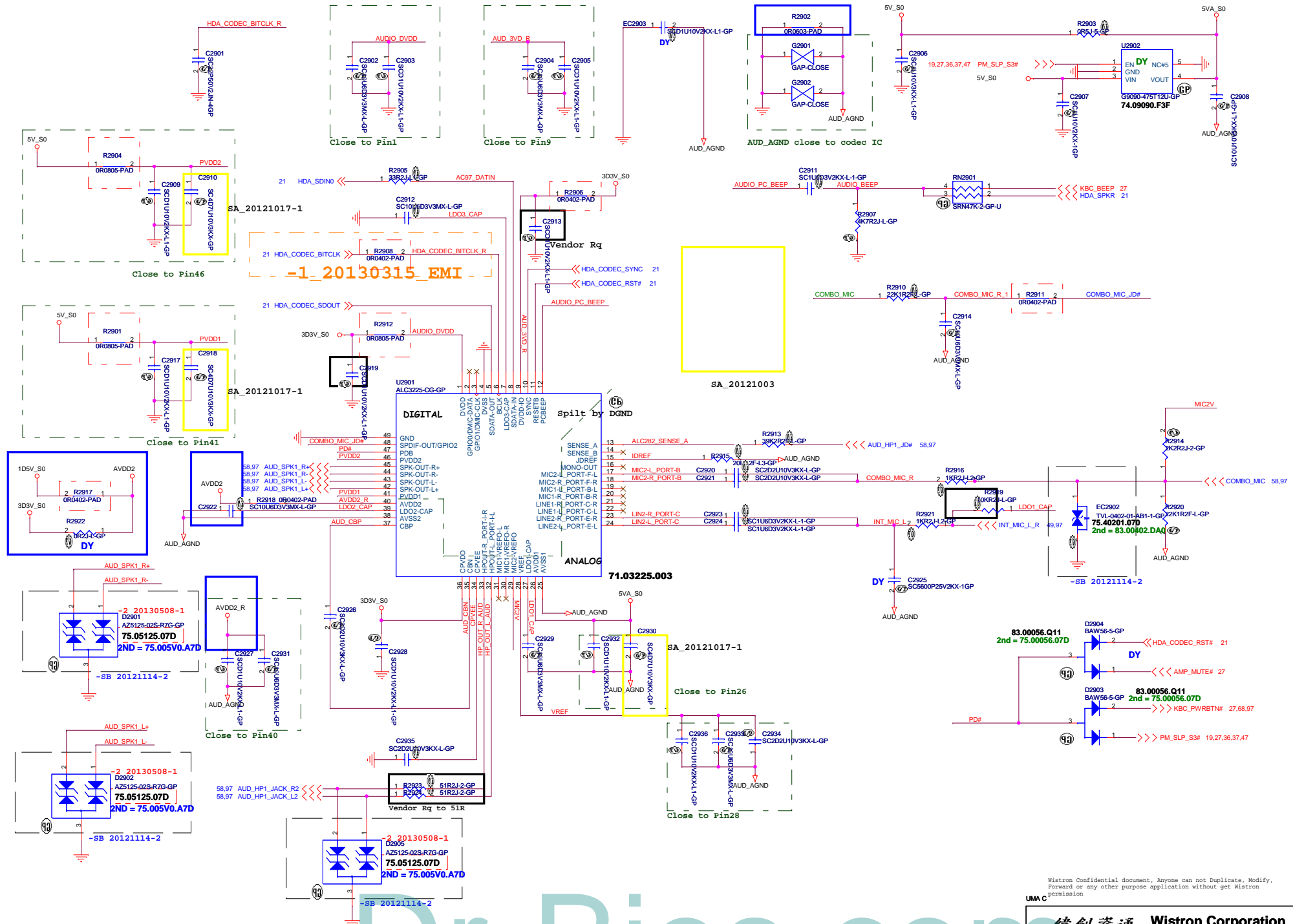
\*Layout\* 15 mil



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<b>Thermal NCT7718</b>			
Size	Document Number	Rev	
Custom	<b>EA40 CX</b>	<b>-3</b>	
Date:	Thursday, June 20, 2013	Sheet	28 of 103

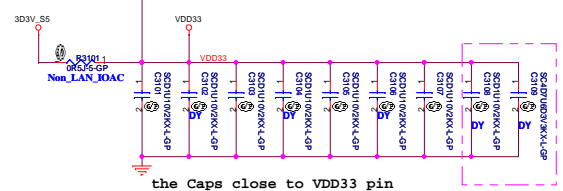
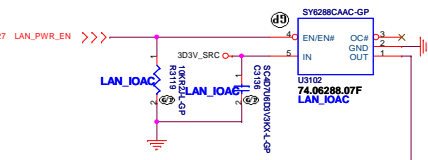


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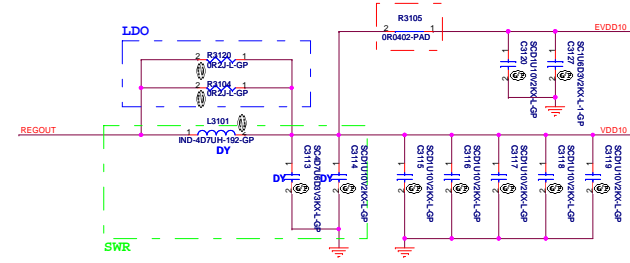
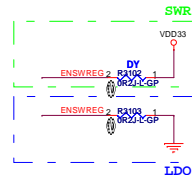
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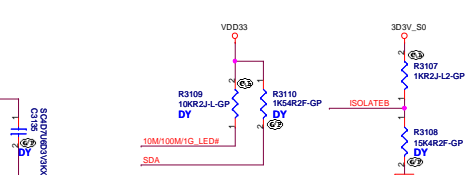
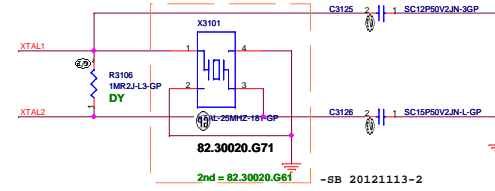
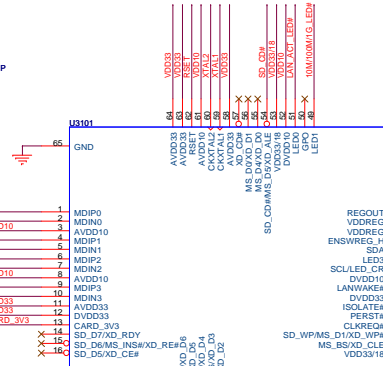
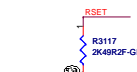
緯創資通		<b>Wistron Corporation</b> 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>Audio AMP</b>			
Size	Document Number	Rev	
A3	<b>EA40 CX</b>	-3	
Date:	Thursday, June 06, 2013	Sheet 30	of 103



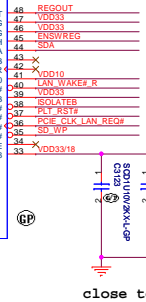
Close to VDDREG pin



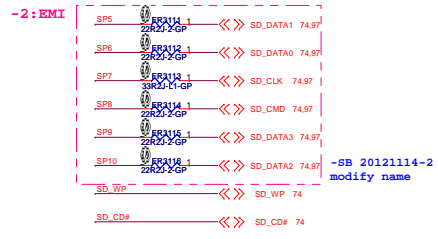
the Caps close to VDD33 pin



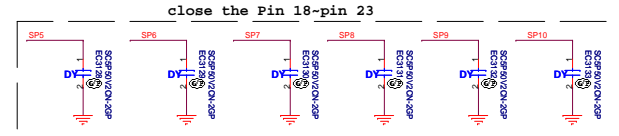
SP1	SD D7	xD_RDY
SP2	SD D6	MS_INS#
SP3	SD D5	xD_CE#
SP4	SD D4	xD_WE#
SP5	SD D1	MS_CLK
SP6	SD D0	xD_D5
SP7	SD CLK	MS D3
SP8	SD CMD	xD D3
SP9	SD D3	xD D2
SP10	SD D2	xD D7
SP11	MS BS	xD_CLE
SP12	SD_WP	MS D1
SP13	SD_CD#	xD_ALE
SP14	MS D4	xD_D0
SP15	MS D0	xD D1
SP16	MS D1	xD_CD#



close to pin33 and pin53



-SB 20121114-2  
modify name



-SB 20121114-2  
modify name



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Title: LAN(RTL8411)

Size: Document Number: EA40 CX Rev: -3

Date: Friday, June 21, 2012 Sheet: 31 of 189



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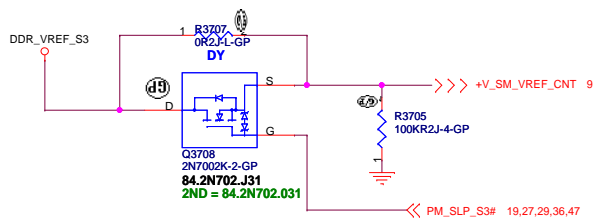
UMA C

<b>緯創資通</b>		<b>Wistron Corporation</b>	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>RTS5159 (CARD READER)</b>			
Size	Document Number	Rev	
Custom	<b>EA40 CX</b>		<b>-3</b>
Date:	Thursday, June 06, 2013	Sheet	32 of 103

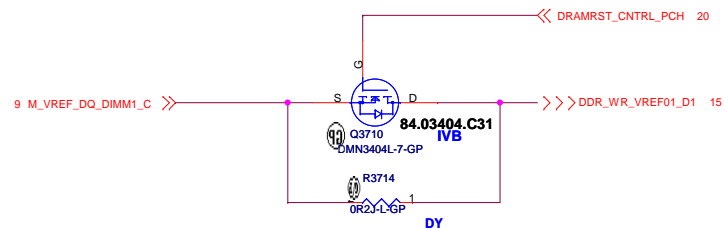
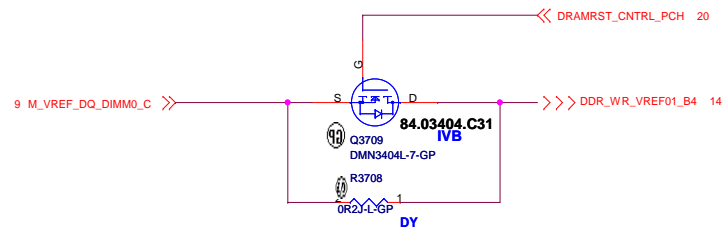
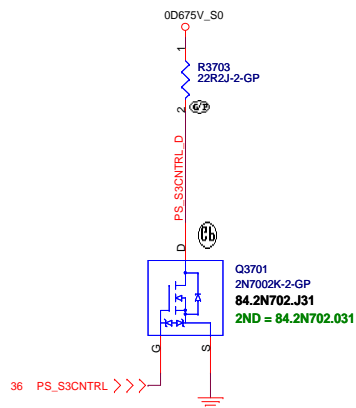
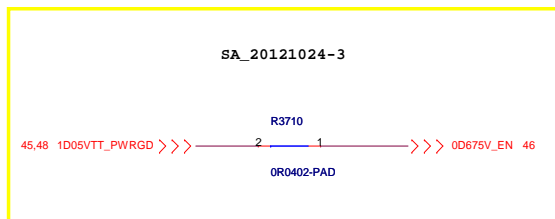
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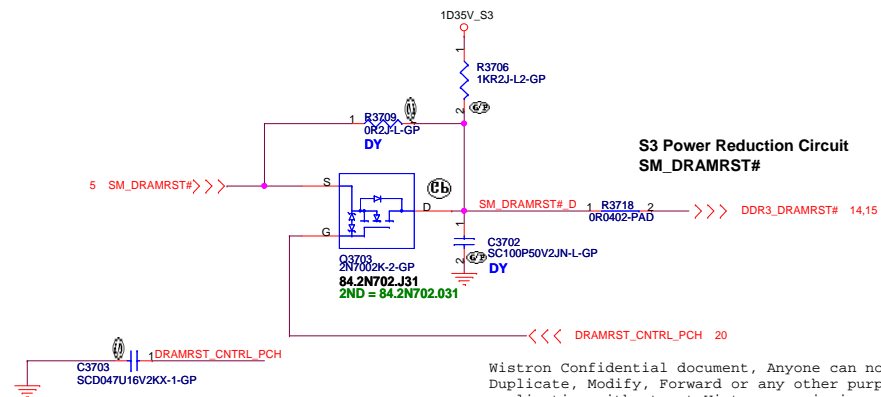
Close to CPU  
S3 Power Reduction Circuit Processor VREF\_DQ Implementation



Close to DIMM  
S3 Power Reduction Circuit SM\_DRAMPWROK



Close to CPU  
S3 Power Reduction Circuit SM\_DRAMPWROK

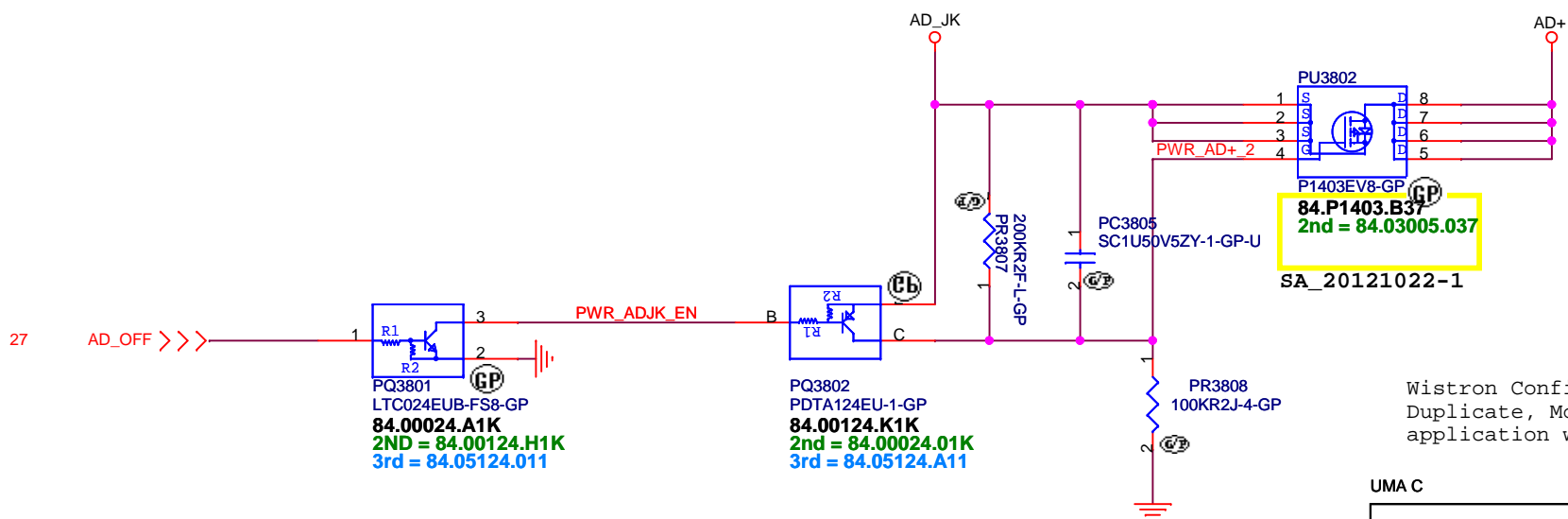
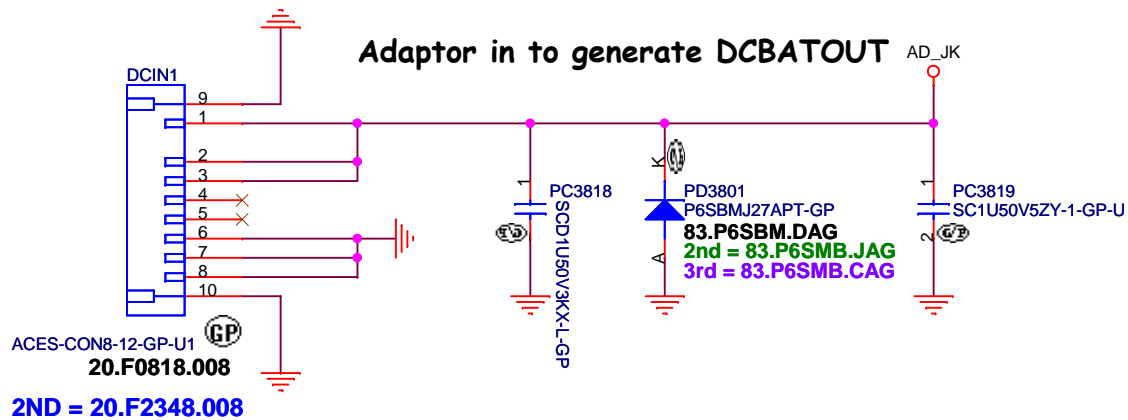


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<p>Title <b>ADAPTER</b></p>	
Size Custom	Document Number <b>EA40 CX</b>
Date: Thursday, June 20, 2013	Rev <b>-3</b>
<p>Sheet 37 of 103</p>	



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Title			<b>DCIN JACK</b>
Size	Document Number	Rev	
A4	<b>EA40 CX</b>	<b>-3</b>	
Date:	Thursday, June 20, 2013	Sheet	38 of 103

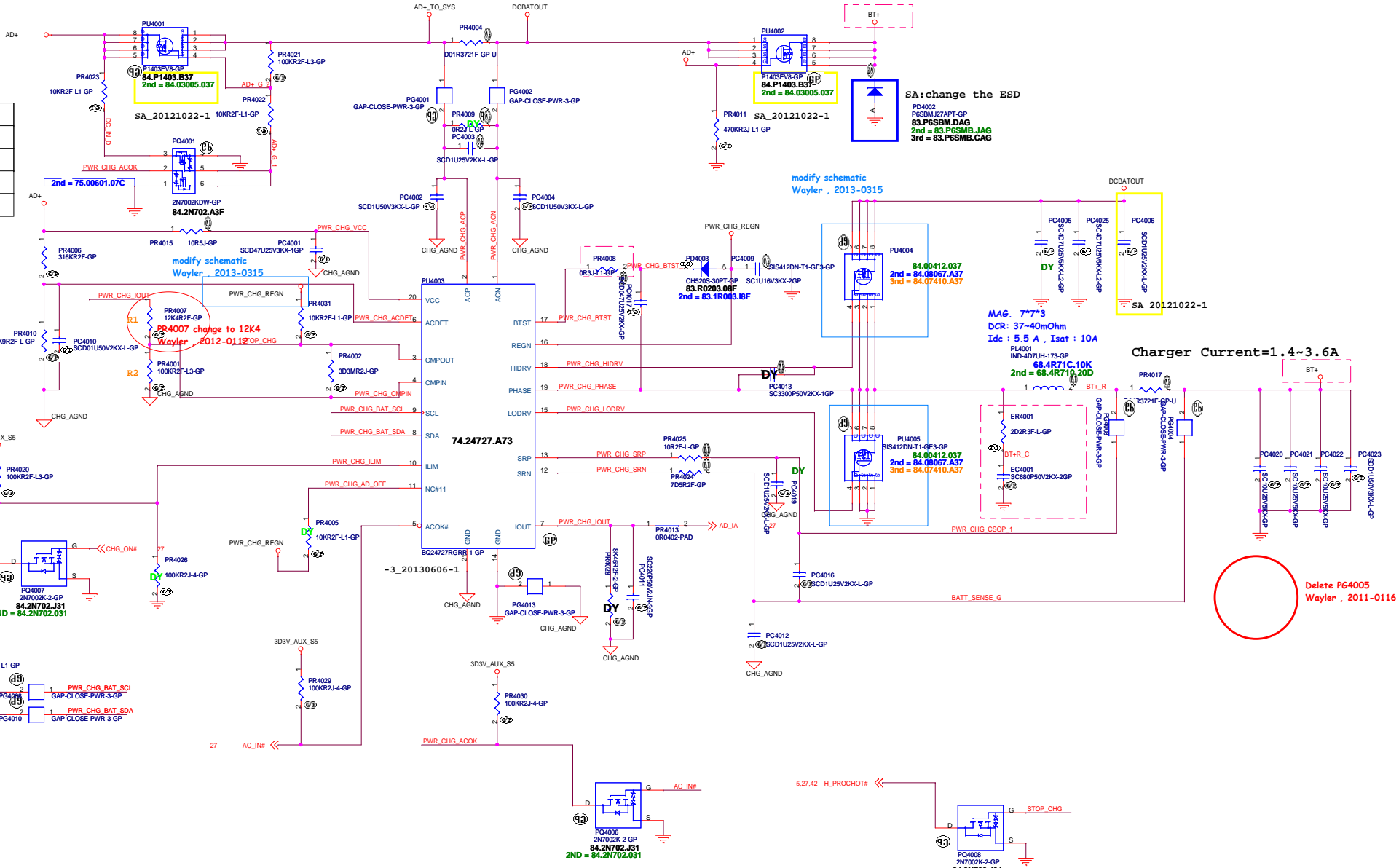
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**SSID = Charger**

A8 (ANNIE/ASTRO)  
PR4014, PR4016

AD+ total power	R1	R2
65w	1.2.4K	100K
80w	41.2k	100K
90w	60.4k	100K
120w	1.18k	100K

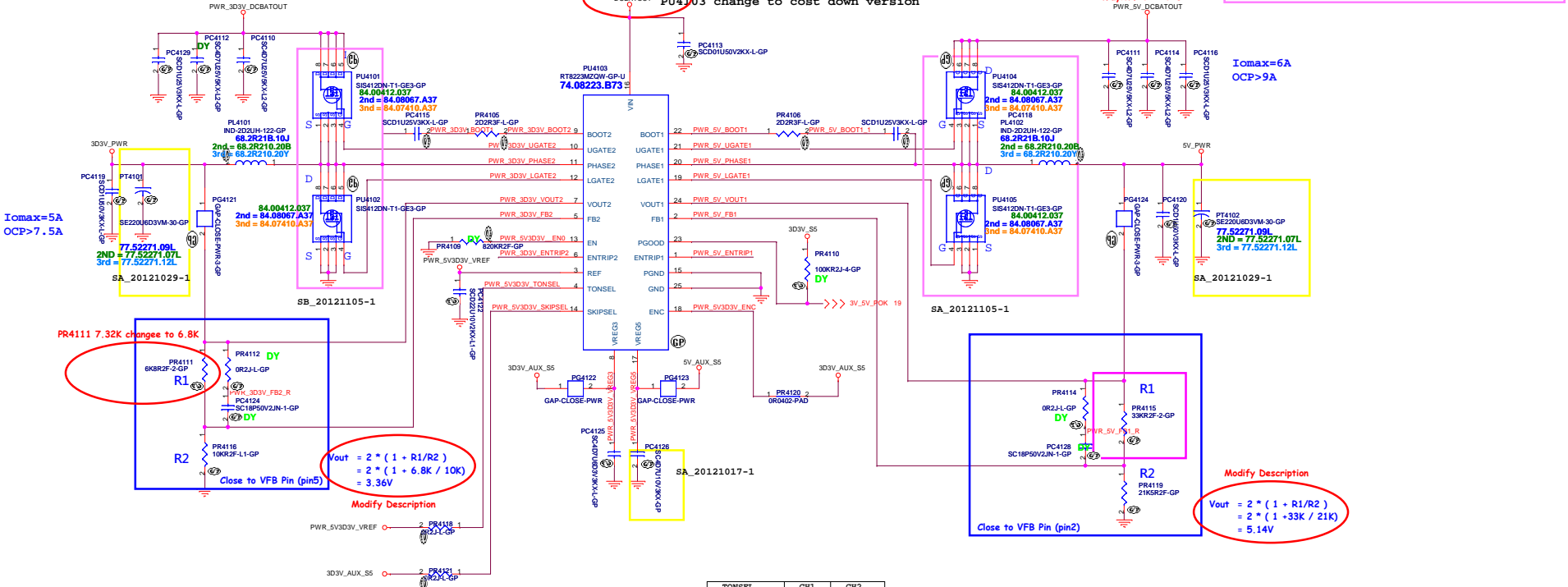
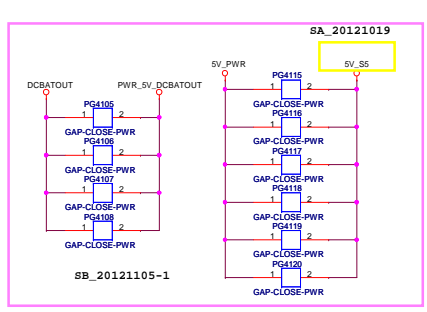
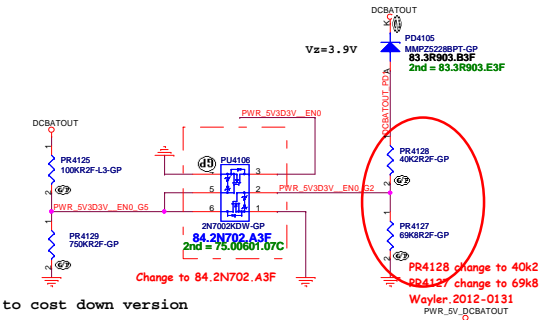
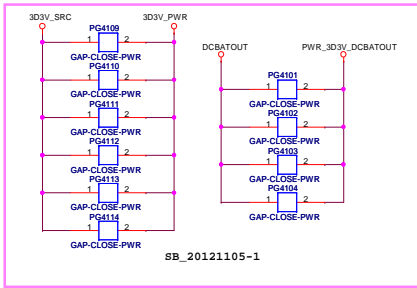


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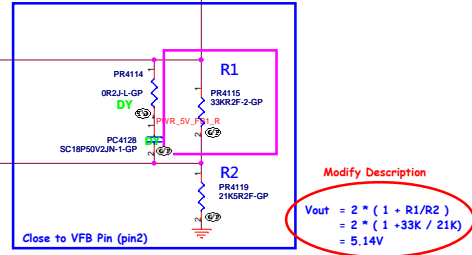
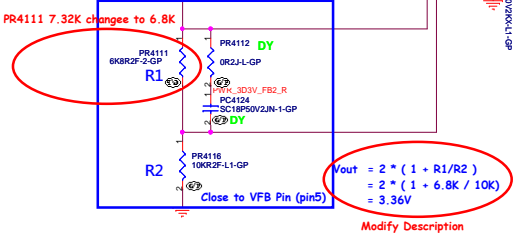
**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

File	<b>CHARGER BQ24727</b>	
Size	Document Number	Rev
Custom	<b>EA40 CX</b>	<b>-3</b>
Date	Friday, June 21, 2013	Sheet 40 of 103



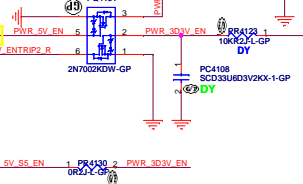
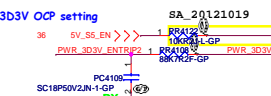
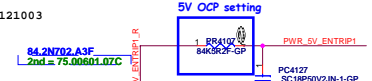
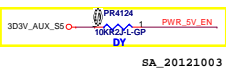
Iomax=5A  
OCP>7.5A

Iomax=6A  
OCP>9A



TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3 or VREG5	400kHz	500kHz

SKIPSEL	VREG3 or VREG5	VREF (2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only



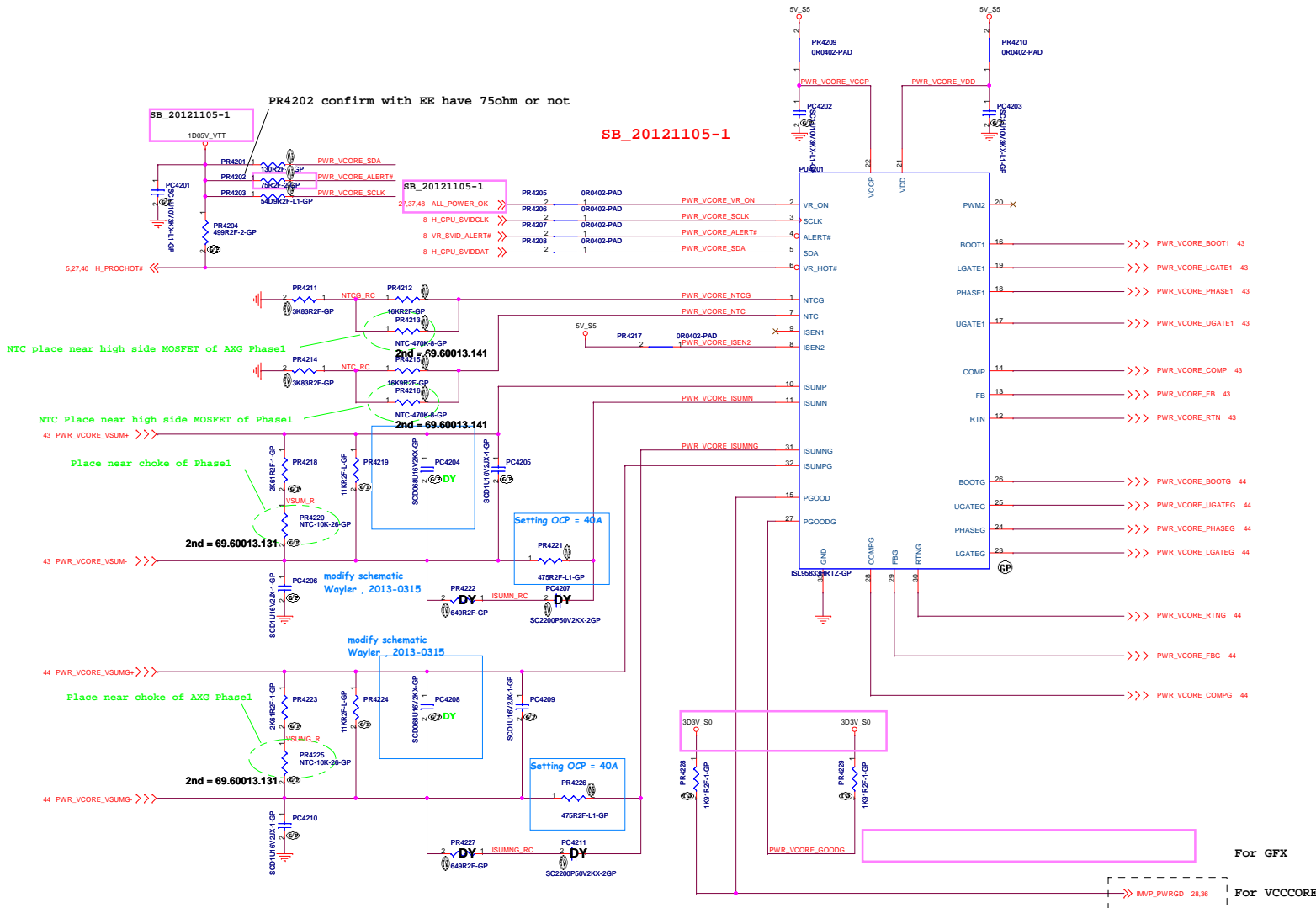
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Title: 5V/3D3V(RT8223M)  
Size: Document Number  
Customer: EA40 CX  
Date: P1659, June 21, 2013  
Sheet: 41 of 108  
Rev: -3





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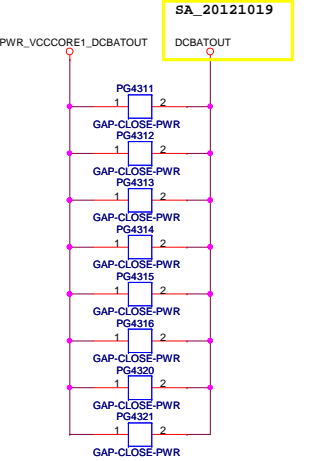
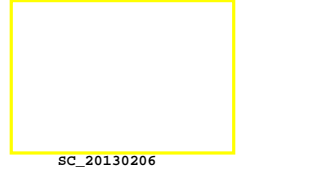
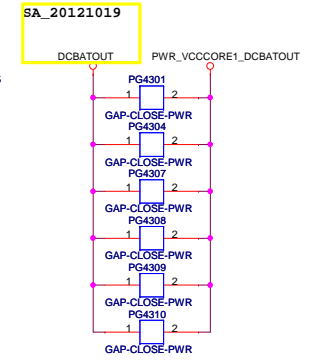
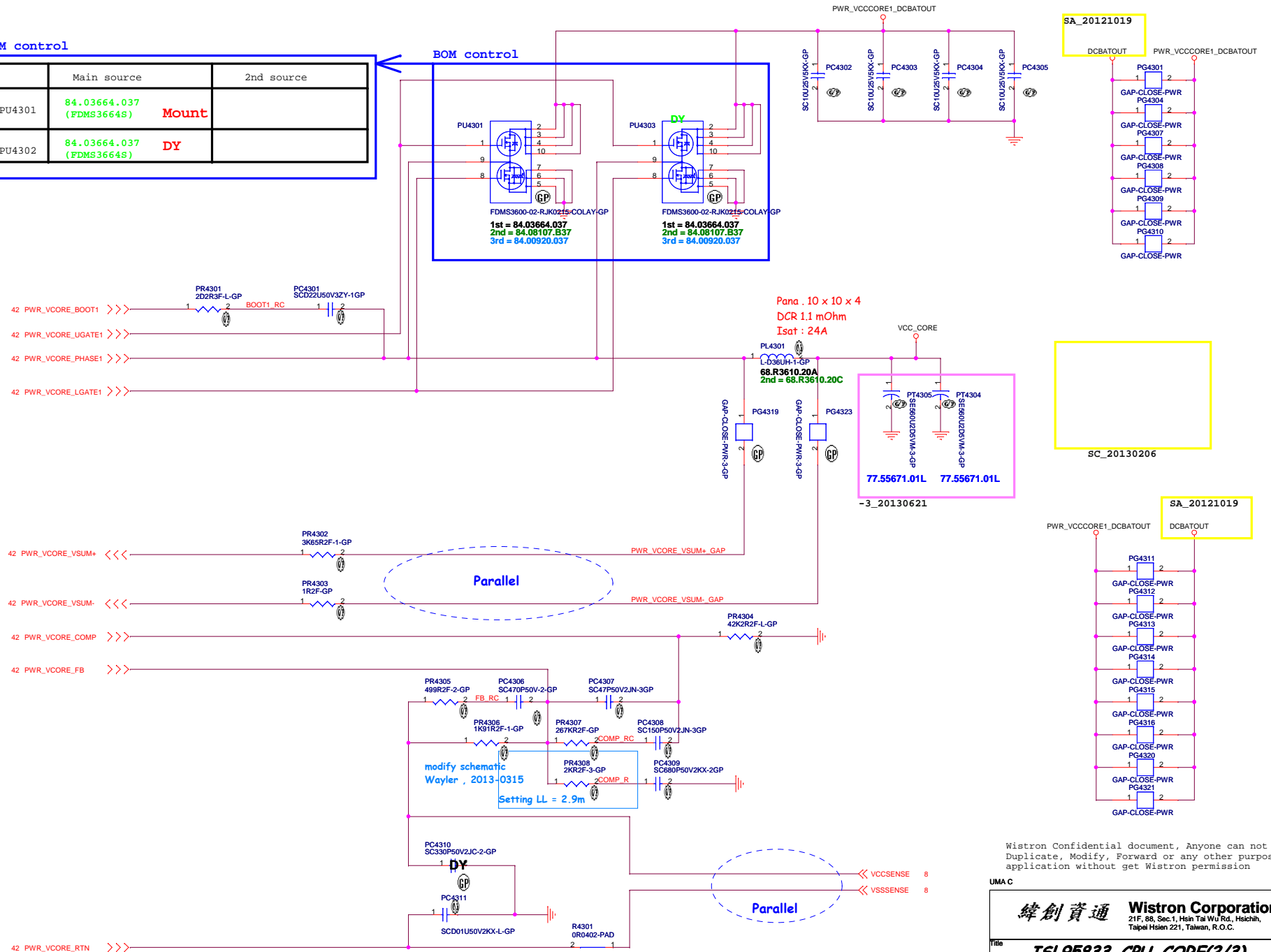
UMA C		
緯創資通		Wistron Corporation
21F, 8F, Sec.1, Hsin Tai Wu Rd., Hsinchi, Taipei Hsien 221, Taiwan, R.O.C.		
Title	ISL95833_CPU_CORE(1/3)	
Size	Document Number	Rev
Custom	EA40_CX	-3
Date: Friday, June 21, 2013	Sheet 42 of	103

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BOM control

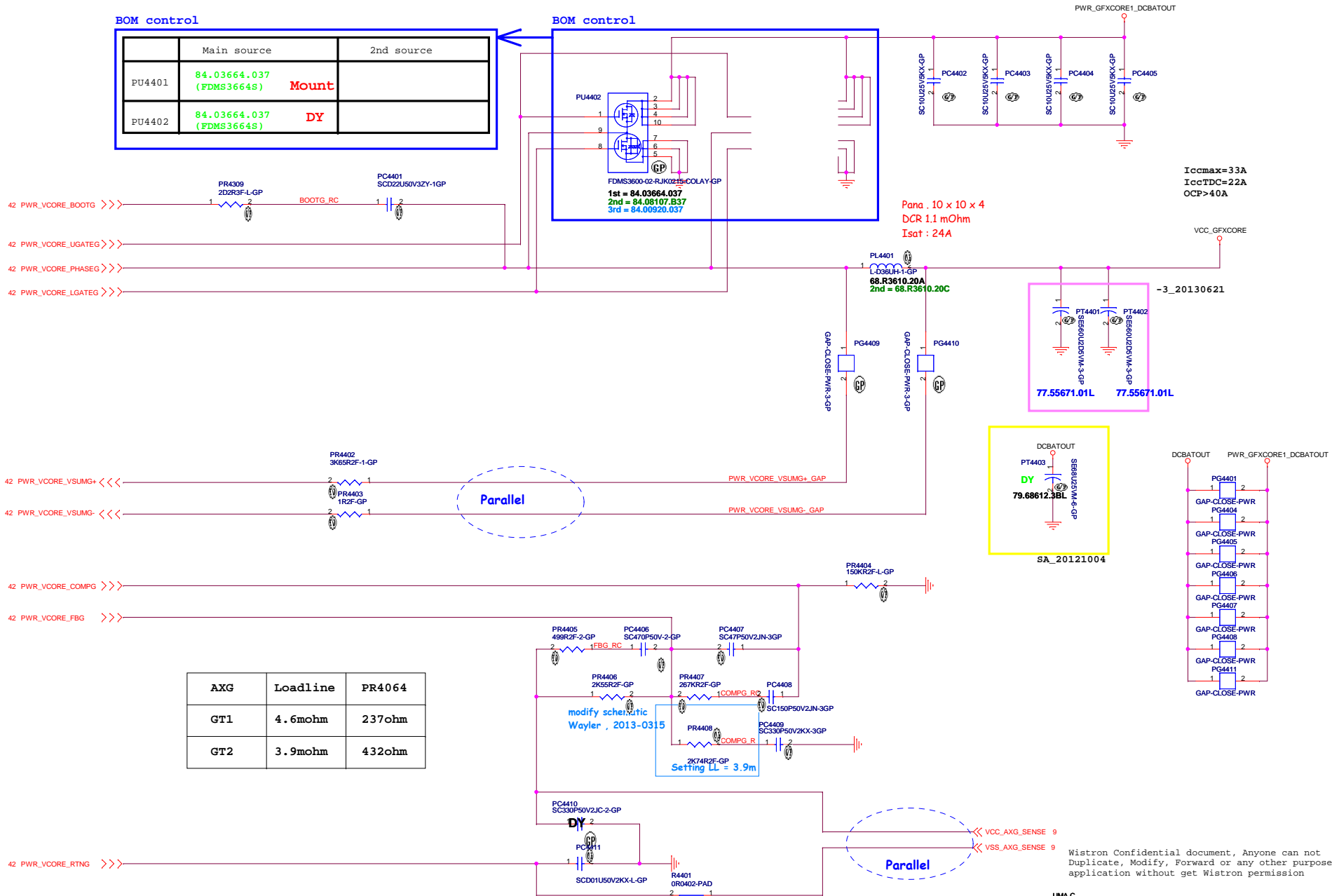
	Main source	2nd source
PU4301	84.03664.037 (FDMS3664S)	Mount
PU4302	84.03664.037 (FDMS3664S)	DY

BOM control



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Title	<b>ISL95833_CPU_CORE(2/3)</b>	
Size	Document Number	Rev
Custom	<b>EA40 CX</b>	<b>-3</b>
Date:	Friday, June 21, 2013	Sheet 43 of 103



AXG	Loadline	PR4064
GT1	4.6mohm	237ohm
GT2	3.9mohm	432ohm

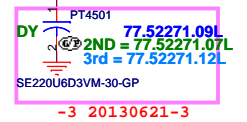
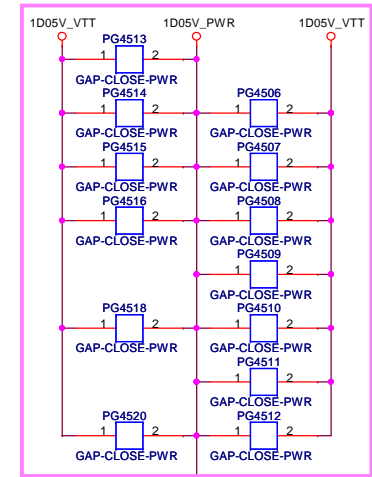
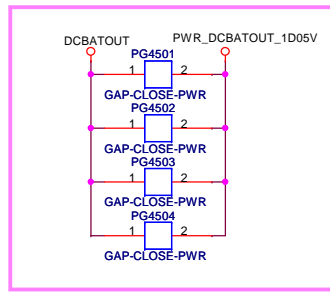
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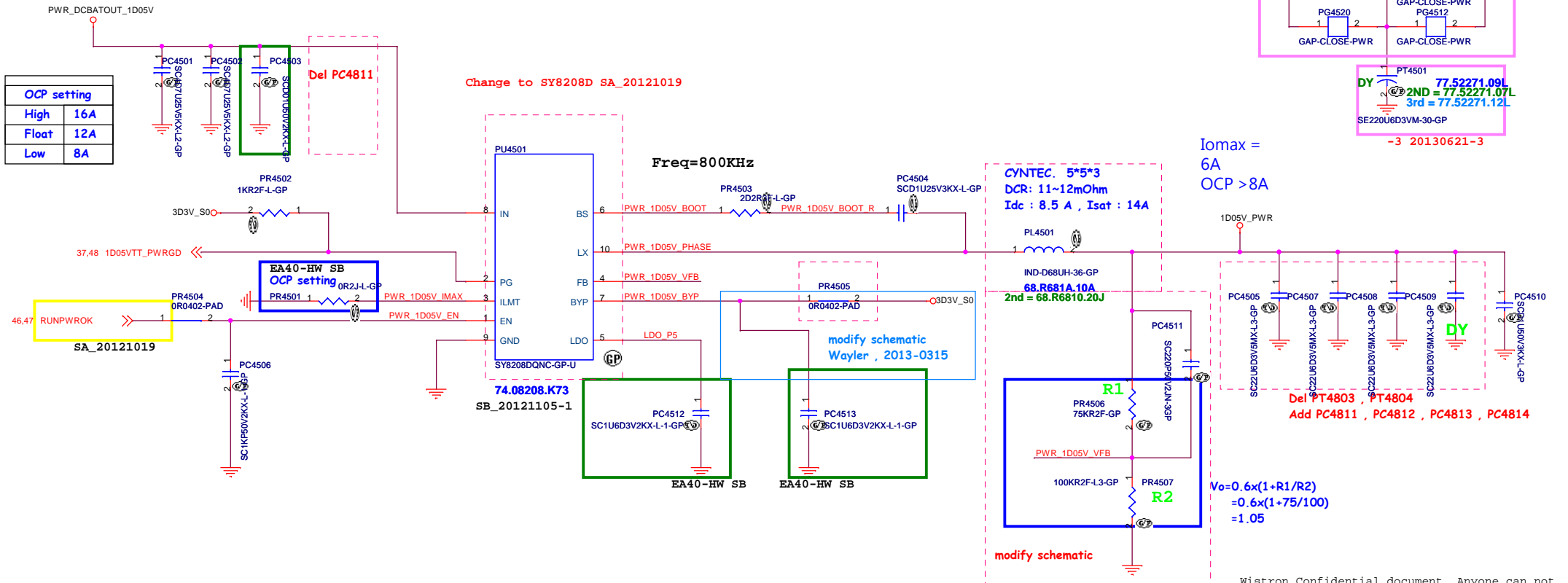
# SY8208D for 1D05V

SB\_20121105-1

SB\_20121105-1



OCP setting	
High	16A
Float	12A
Low	8A



Iomax =  
6A  
OCP > 8A

$$V_o = 0.6 \times (1 + R1/R2)$$

$$= 0.6 \times (1 + 75/100)$$

$$= 1.05$$

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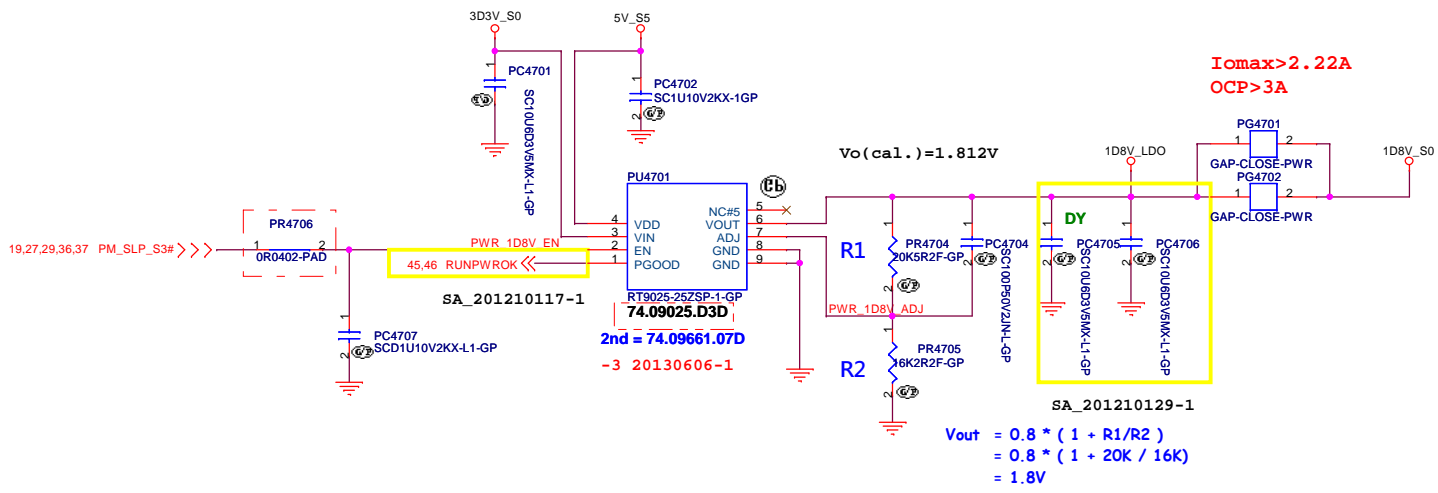
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Title	
<b>DC to DC 1D05V(SY8208D)</b>	
Size	Document Number
A3	<b>EA40_CX</b>
Date	Rev
Friday, June 21, 2013	<b>-3</b>
Sheet	of
45	103



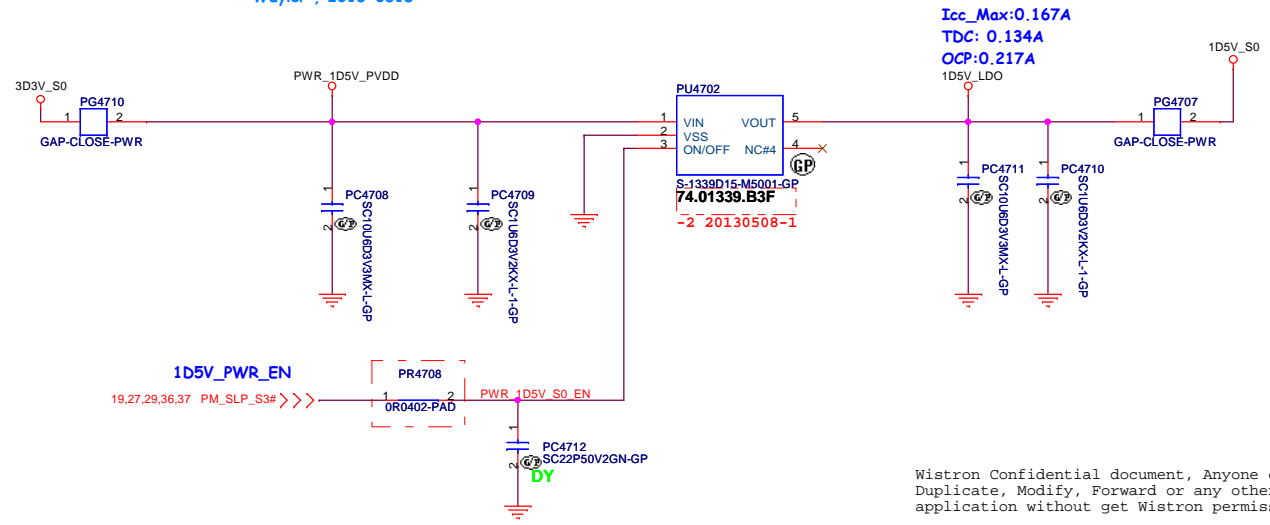
**SSID = PWR.Plane.Regulator\_1p8v**

**RT9025 for 1D8V\_S0**



**S-1339D15 for 1D5V\_S0**

modify schematic  
Wayler , 2013-0315



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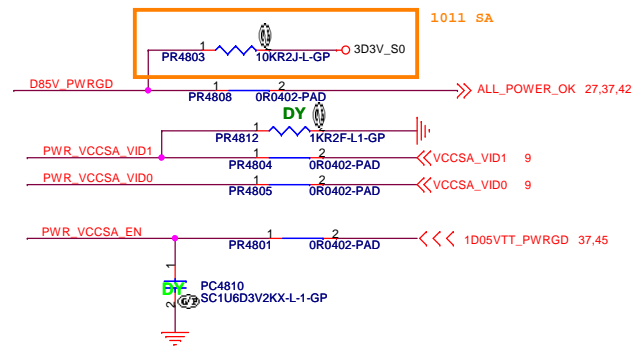
Title: **LDO 1D8V&1D5V(RT9025)**

Size: Custom Document Number: **EA40 CX** Rev: **-3**

Date: Thursday, June 20, 2013 Sheet 47 of 103



# LDO G978 for VCCSA



D0, D1 V<sub>0</sub> Selection Table

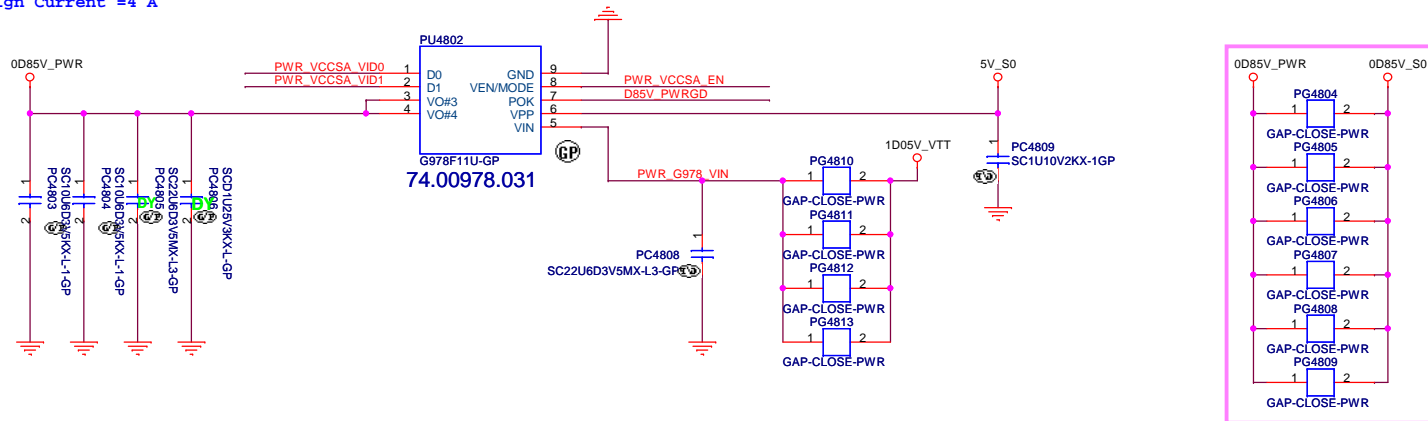
D0	D1	V <sub>0</sub> MODE=0	V <sub>0</sub> MODE=1
0	0	0.9V	0.9V
0	1	0.8V	0.85V
1	0	0.725V	0.775V
1	1	0.675V	0.75V

"x" means "don't care".

VEN/MODE Logic

VEN/MODE (VPP=5V)	EN logic	VEN/MODE (VPP=5V)	MODE logic
<0.6V	0	<2.0V	0
>1.0V	1	>2.6V	1

Design Current = 4 A



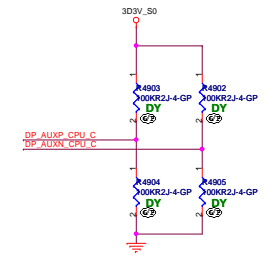
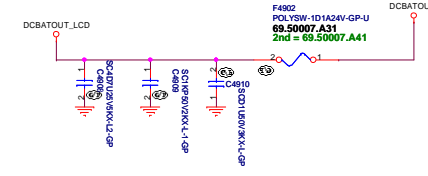
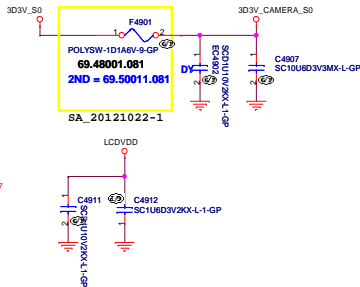
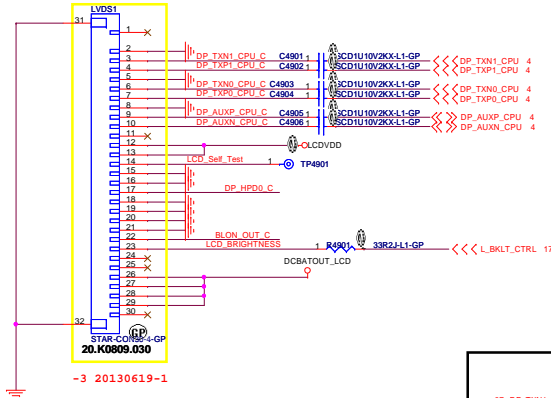
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Title: <b>VCCSA LDO G978</b>	
Size: A3	Document Number: <b>EA40_CX</b>
Date: Thursday, June 20, 2013	Rev: <b>-3</b>
Sheet 48 of 103	

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eDP Conn.

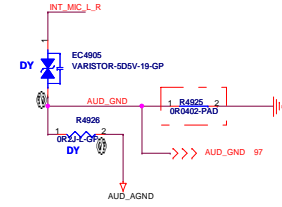
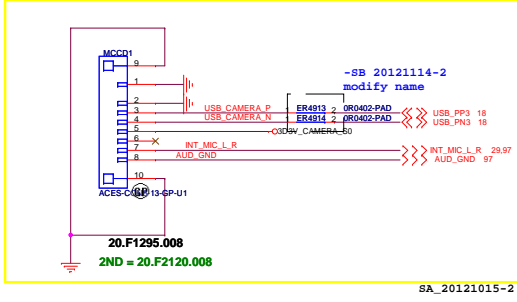
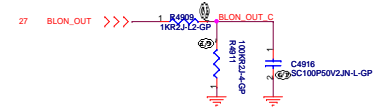
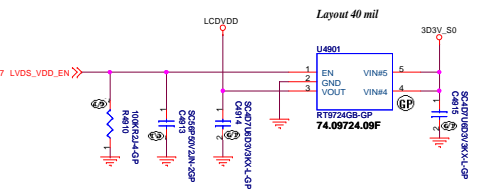
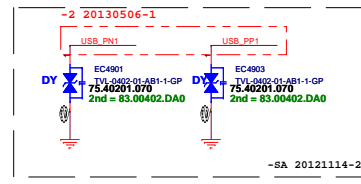
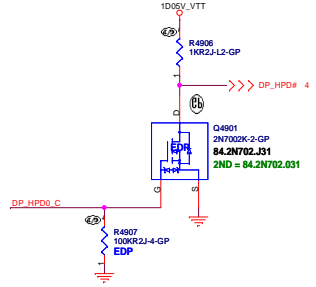


BY cable  
 L(pin5 GND):DMIC  
 H(pin5:floating):AMIC

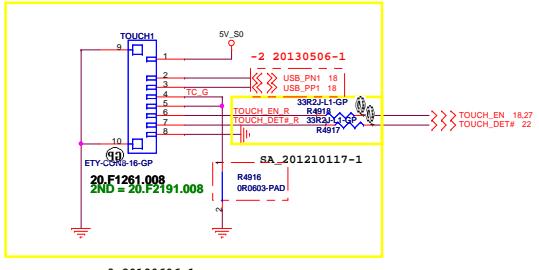
For TestPoint

97 DP_HPDD_C	>>>
97 BLON_OUT_C	>>>
97 LCD_BRIGHTNESS	>>>

97 DP_TXN1_CPU_C	>>>
97 DP_TXP1_CPU_C	>>>
97 DP_TXN0_CPU_C	>>>
97 DP_TXP0_CPU_C	>>>
97 DP_AUXP_CPU_C	>>>
97 DP_AUXN_CPU_C	>>>



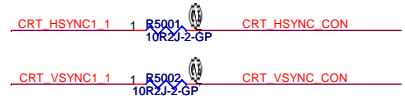
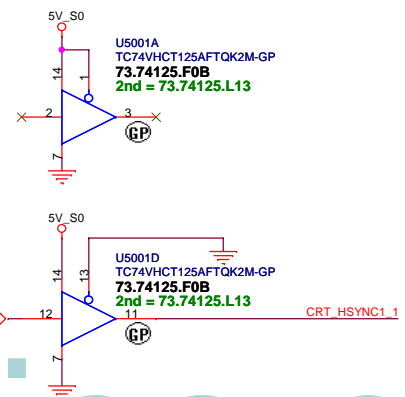
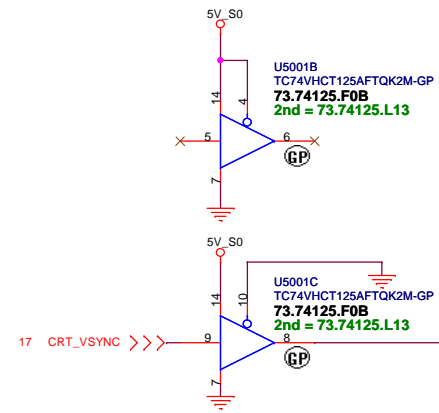
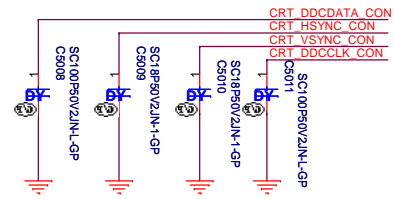
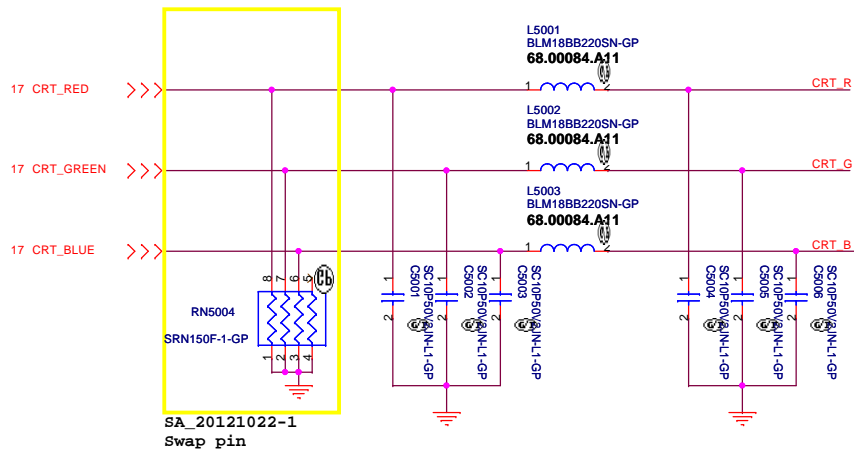
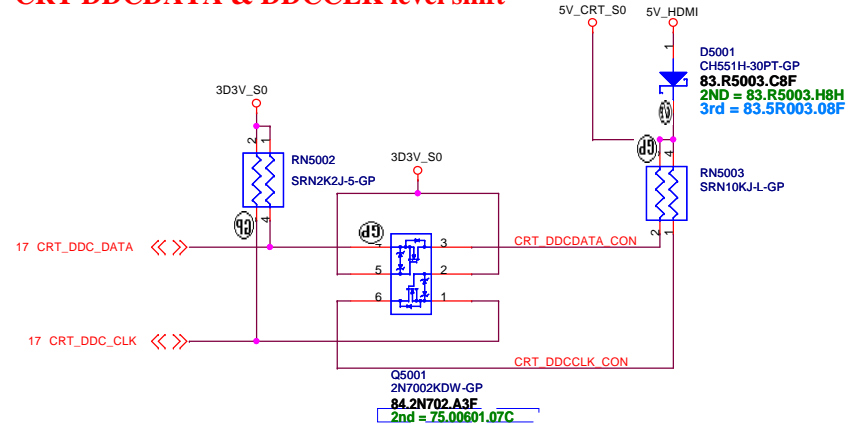
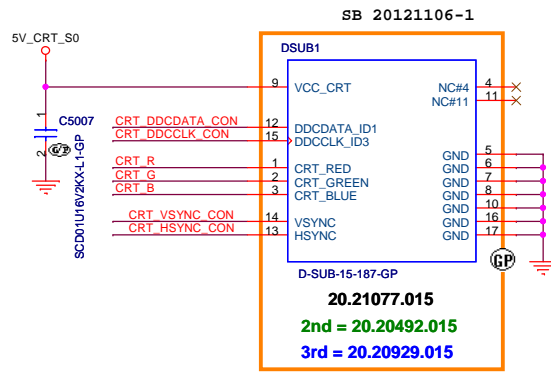
Touch Conn.



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# CRT DDCDATA & DDCCLK level shift



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Title	<b>CRT Connector</b>	
Size A3	Document Number	Rev
	<b>EA40_CX</b>	<b>-3</b>
Date: Thursday, June 20, 2013	Sheet 50 of 103	

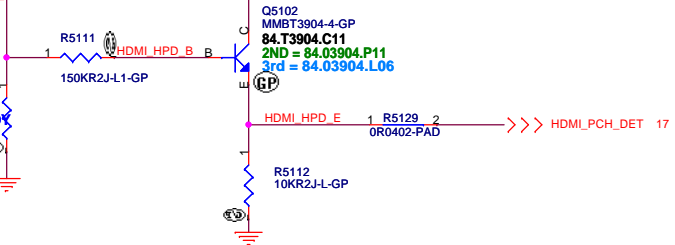
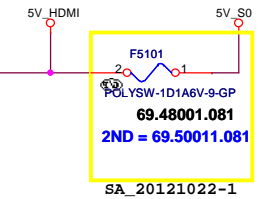
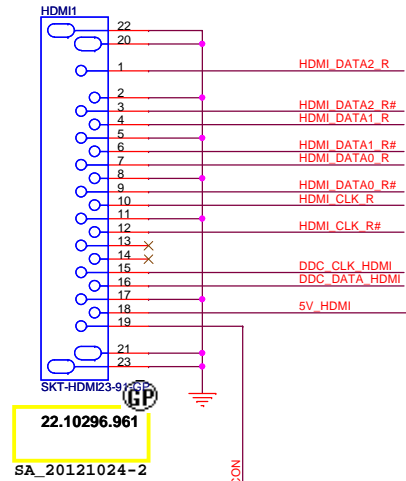
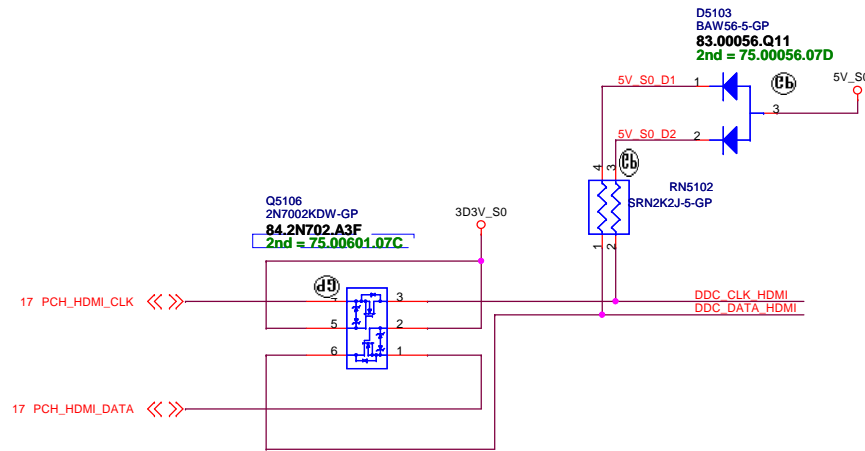
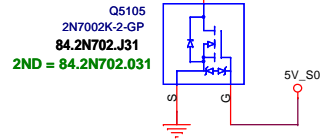
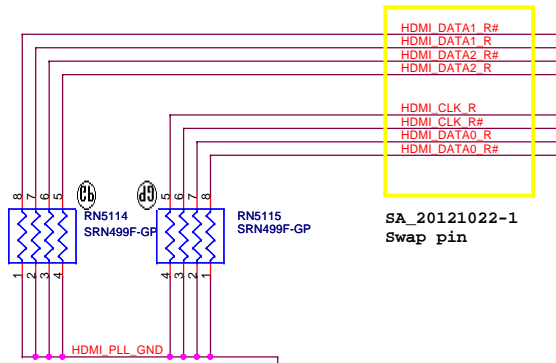
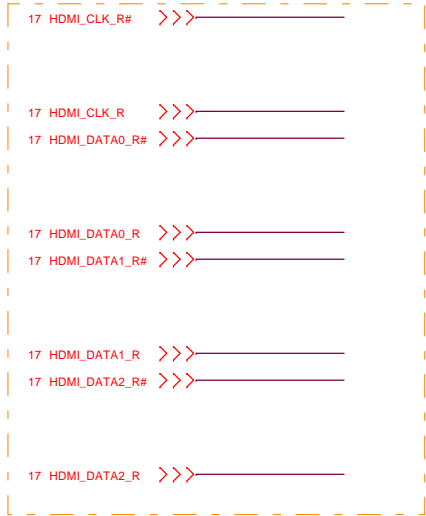
SSID = VIDEO

# HDMI Level Shifter & CONNECTOR

Close to HDMI Connector

change = DIS:499 ohm  
Fist = UMA Muxless:680 ohm

-1\_20130315A



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Title: **HDMI Level Shifter/Connector**

Size A3 Document Number: **EA40\_CX** Rev: **-3**

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Title		
eDP		
Size	Document Number	Rev
A3	EA40_CX	-3
Date:	Thursday, June 06, 2013	Sheet 52 of 103

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Title	<b>S-VIDEO</b>	
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Size	Document Number	Rev
A4	<b>EA40 CX</b>	<b>-3</b>

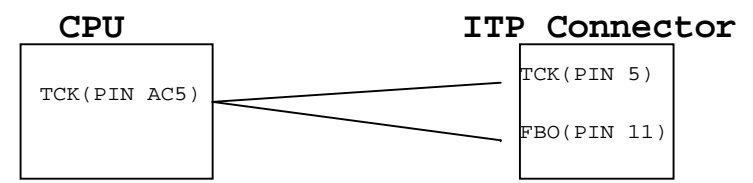
Date: Thursday, June 06, 2013	Sheet 53 of 103
-------------------------------	-----------------

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**SSID = User.Interface**

# *ITP Connector*

H\_CPURST# use pull-up Resistor close  
ITP connector 500 mil ( max ),  
others place near CPU side.



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Title			<b>ITP</b>		
Size	Document Number				Rev
A4	<b>EA40 CX</b>				<b>-3</b>
Date	Thursday, June 06, 2013			Sheet	55 of 103

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5

4

3

2

1

D

D

C

C

B

B

A

A

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Title		
<b>E-SATA/USB CHARGER</b>		
Size	Document Number	Rev
A3	<b>EA40_CX</b>	<b>-3</b>
Date:	Thursday, June 06, 2013	Sheet 57 of 103

5

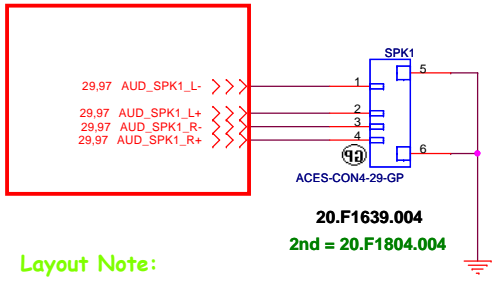
4

3

2

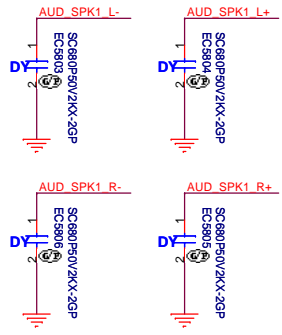
1

SSID = AUDIO *Speaker*

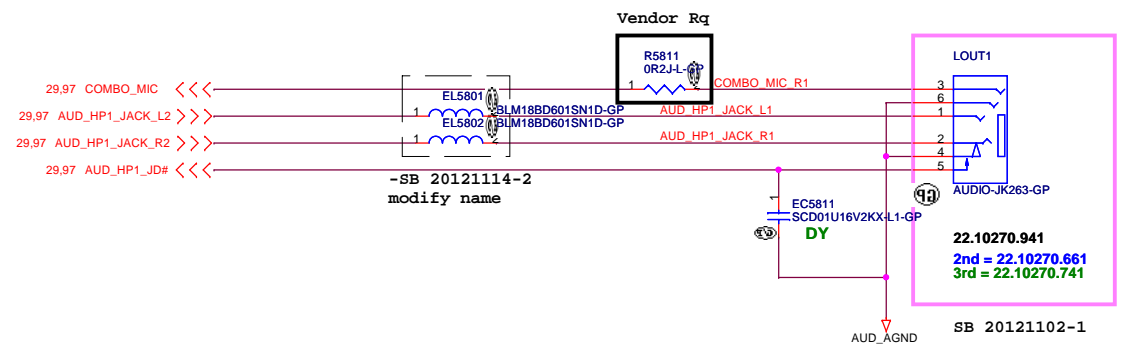


Layout Note:

Trace width=40mil



*Combo Jack*



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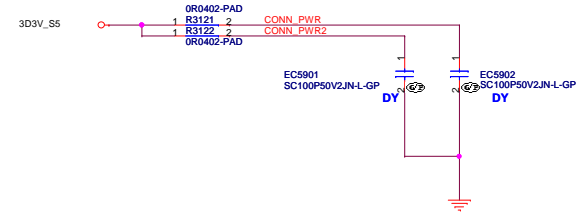
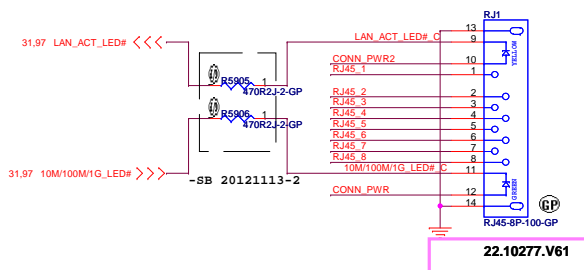
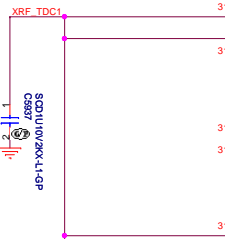
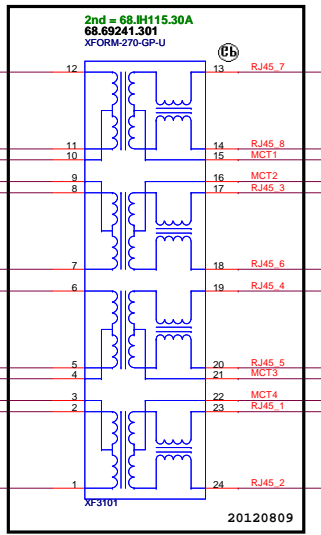
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<b>Audio Jack</b>	
Size A3	Document Number
Date: Thursday, June 06, 2013	EA40 CX
Sheet 58	of 103
Rev	<b>-3</b>

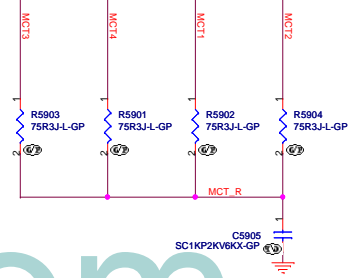
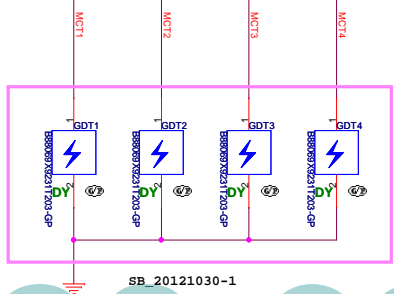
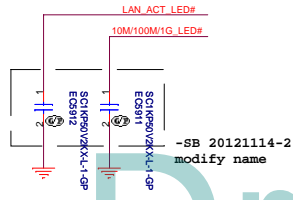
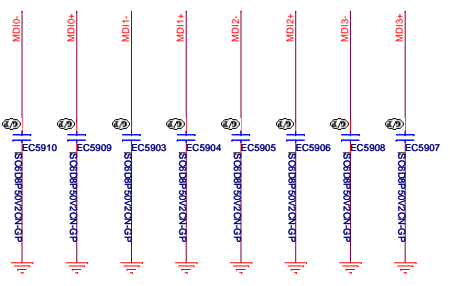
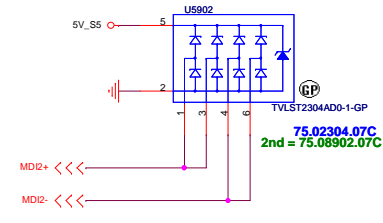
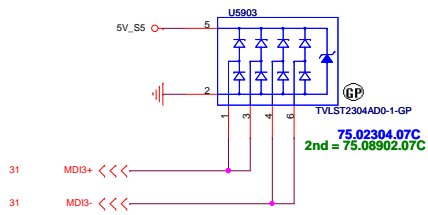
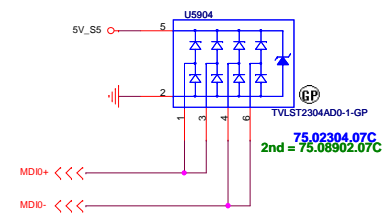
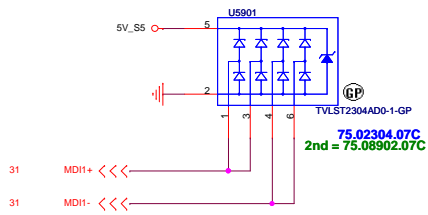


**SSID = LAN**



22.10277.V61  
 2nd 22.10327.141 wait to verify  
 -3\_20130606-1

- 97 RJ45\_1 >>>
- 97 RJ45\_2 >>>
- 97 RJ45\_3 >>>
- 97 RJ45\_4 >>>
- 97 RJ45\_5 >>>
- 97 RJ45\_6 >>>
- 97 RJ45\_7 >>>
- 97 RJ45\_8 >>>
- 31.97 LAN\_ACT\_LED# >>>
- 31.97 10M/100M/G\_LED# >>>
- 97 CONN\_PWR >>>
- 97 CONN\_PWR2 >>>



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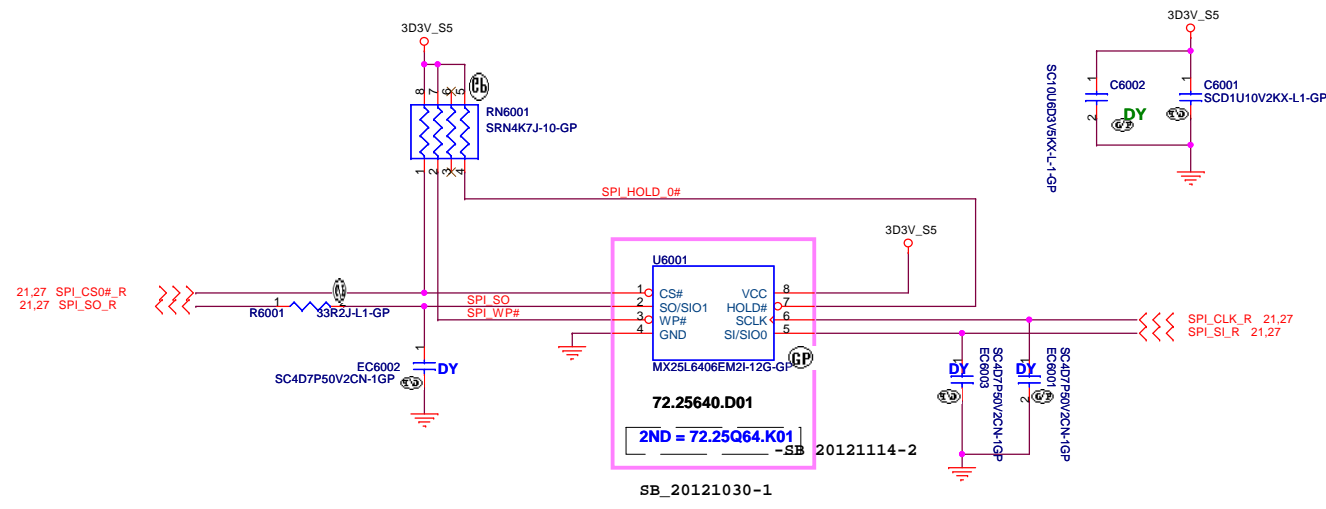
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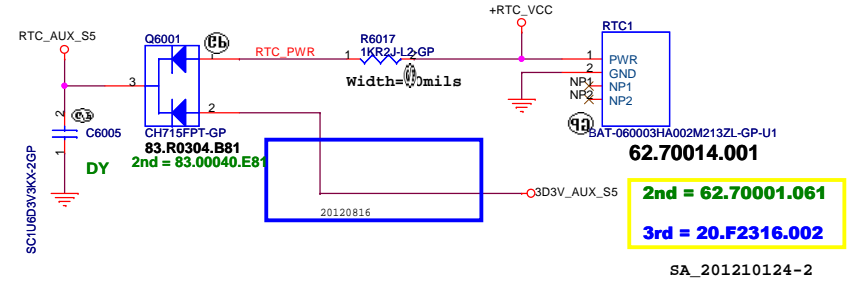
Title	LAN CONNECTOR	
Size	Document Number	Rev
Custom	EA40 CX	-3
Date	Thursday, June 20, 2013	Sheet 59 of 103

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**SSID = Flash.ROM**



**SSID = RTC**



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<b>Title</b>	
<b>Flash/RTC</b>	
<b>Size</b>	<b>Document Number</b>
Custom	<b>EA40 CX</b>
<b>Rev</b>	<b>-3</b>
<b>Date:</b> Thursday, June 20, 2013	<b>Sheet</b> 60 <b>of</b> 103

SSID = USB

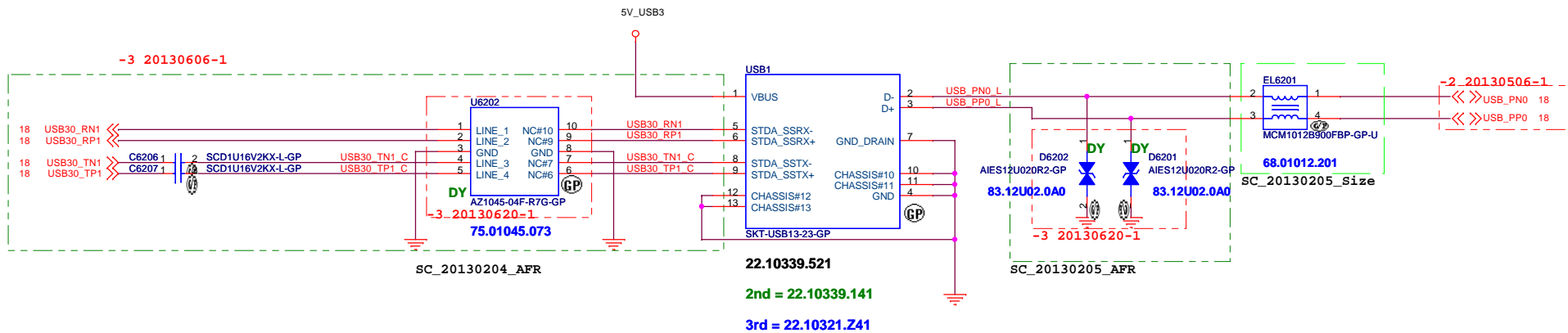
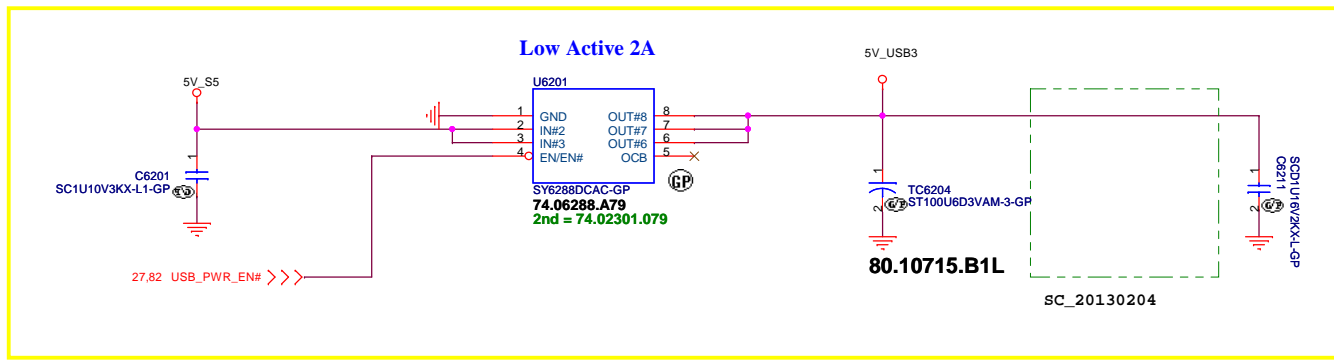
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Title			
<b>USB Power SW</b>			
Size	Document Number	Rev	
A3	<b>EA40_CX</b>	-3	
Date:	Thursday, June 06, 2013	Sheet	61 of 103

USB 3.0 Connector	
Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+



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Title <b>USB 3.0 Port</b>	
Size A3	Document Number <b>E440_CX</b>
Date: Thursday, June 20, 2013	Sheet 62 of 103
Rev <b>-3</b>	

**SSID = User.Interface**  
Bluetooth Module conn.

## *ANNIE Bluetooth Module*

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Title		
<b>Bluetooth</b>		
Size	Document Number	Rev
A4	<b>EA40 CX</b>	<b>-3</b>
Date:	Thursday, June 06, 2013	Sheet 63 of 103

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SSID = Wireless

# Mini Card Connector(WWAN)

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Title **WWAN Connector**

Size A4	Document Number <b>EA40 CX</b>	Rev <b>-3</b>
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Date: Thursday, June 06, 2013 Sheet 66 of 103

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Document Number

**EA40 CX**

Rev

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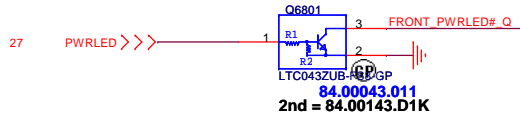
Sheet 67 of 103

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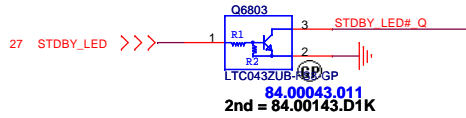


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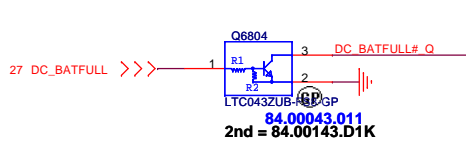
### Power button LED



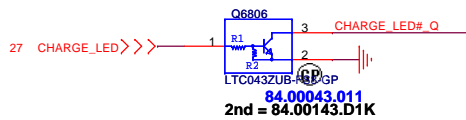
### Power STDBY\_LED



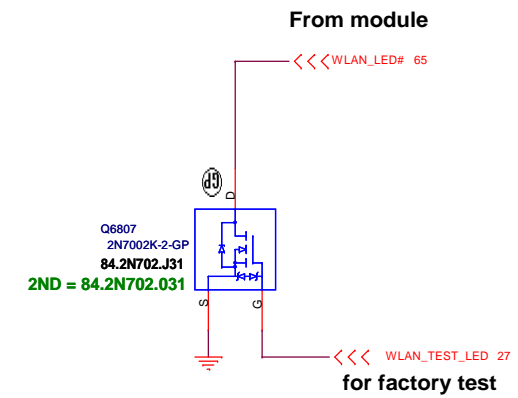
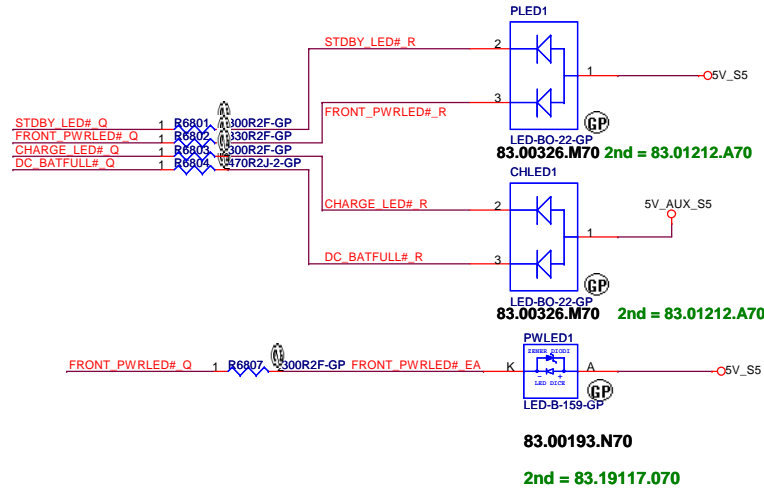
### Battery LED2 (DC\_BATFULL)



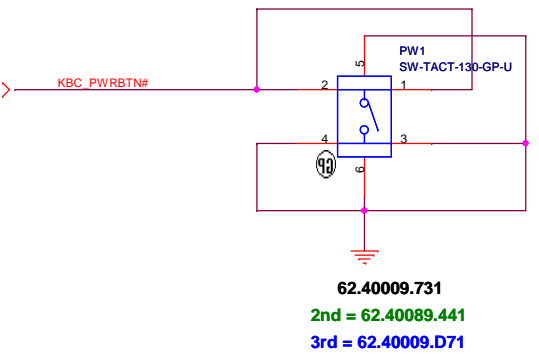
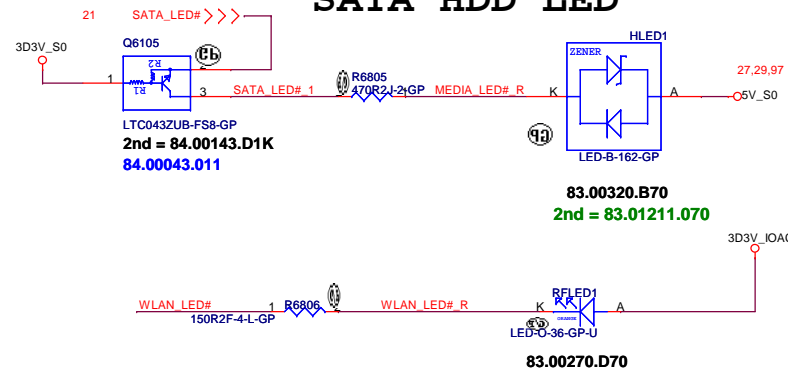
### Battery LED1 (CHARGE)



### WLAN\_LED



### SATA HDD LED



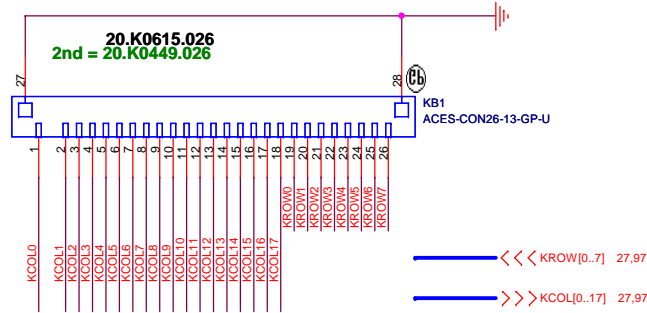
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<p>Title <b>LED Bard/Power Button</b></p>	
Size	Document Number
Custom	EA40_0X
Date	Thursday, June 20, 2013
Rev	-3
Sheet	68 of 103

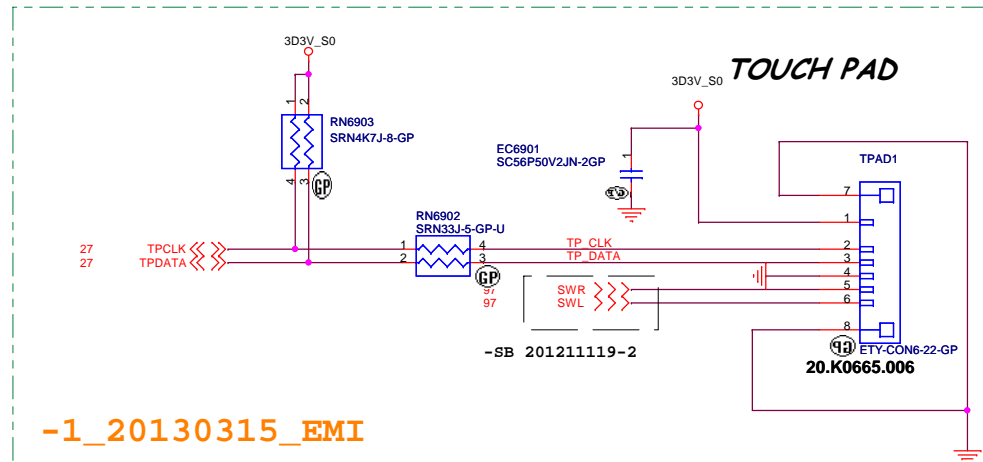
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# Internal KeyBoard Connector



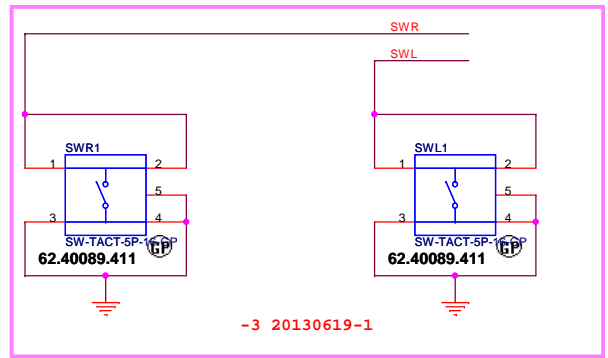
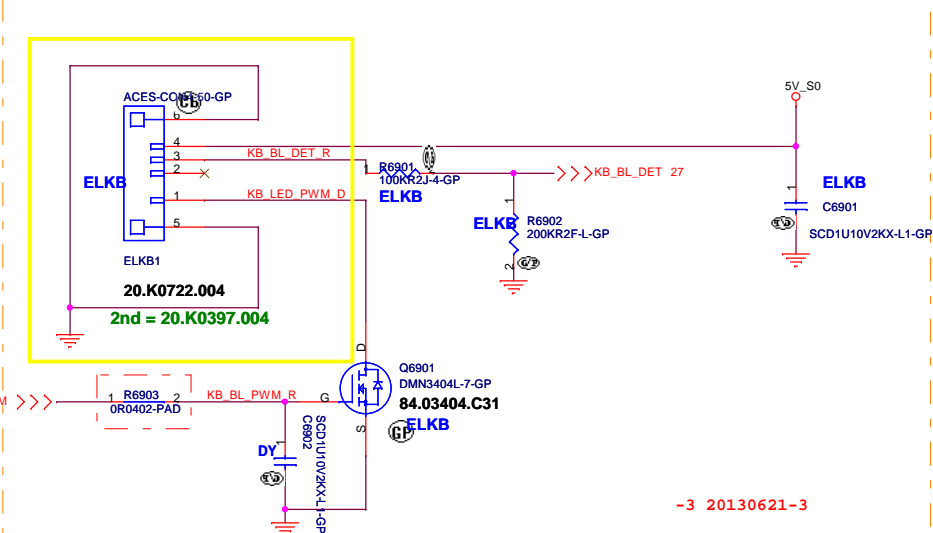
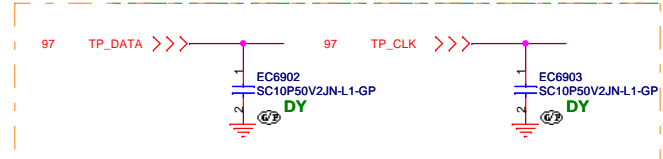
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 KB PIN DEFINE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26

26 K/B 1



-1\_20130315\_EMI

SC\_20130204\_SWAP



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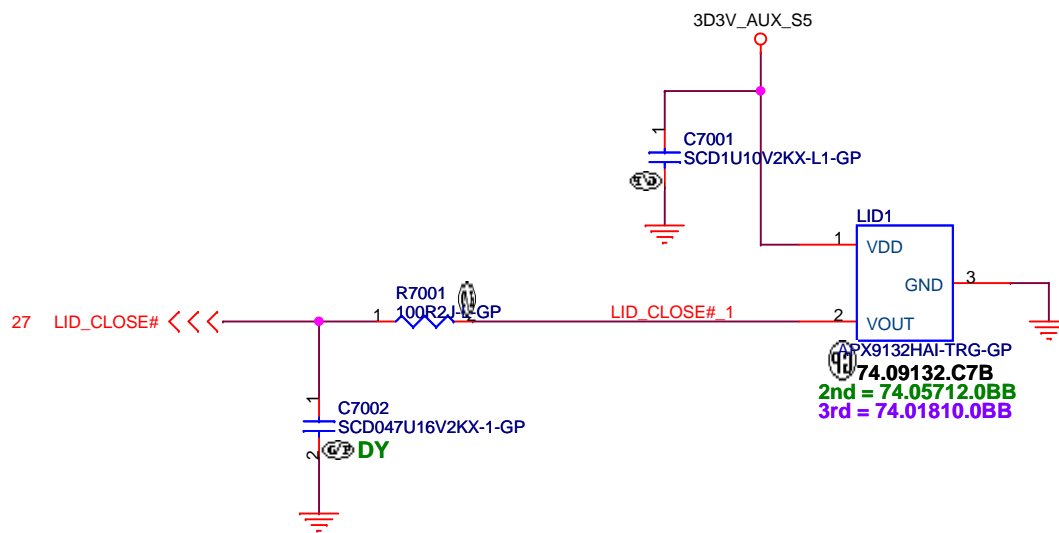
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Title **Key Board/Touch Pad**

Size A3 Document Number **EA40\_CX** Rev **-3**

Date: Friday, June 21, 2013 Sheet 69 of 103



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Title

**Hall Sensor**

Size  
A4

Document Number

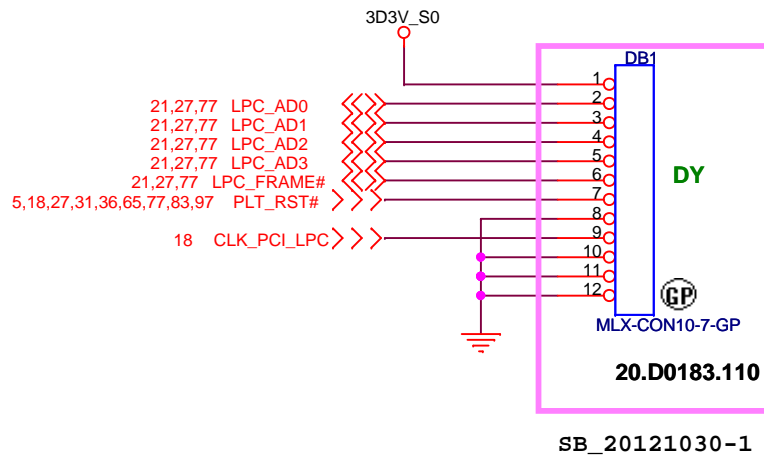
**EA40 CX**

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Sheet 70 of 103

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Size	Document Number	Rev
A4	<b>EA40 CX</b>	<b>-3</b>
Date:	Thursday, June 20, 2013	Sheet 71 of 103

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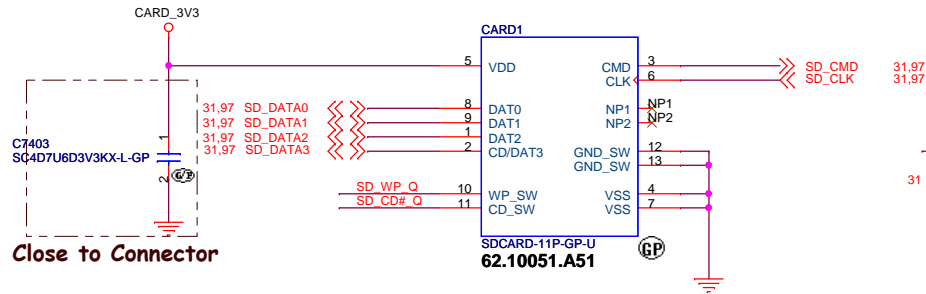
Date: Thursday, June 06, 2013

Sheet 73 of 103

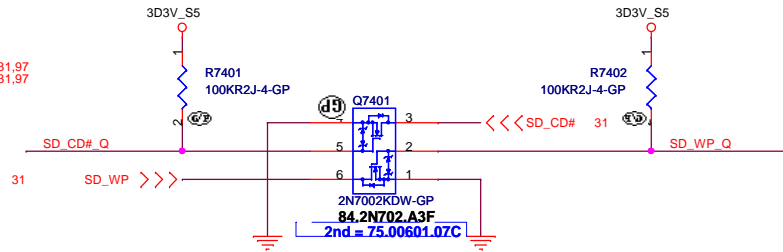
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**SSID = SDIO**

# SD/MMC Card Reader



Close to Connector



SP1	SP1	SD_D7	MS_INS#	xD_RDY
SP2	SP2	SD_D6	MS_INS#	xD_RE#
SP3	SP3	SD_D5	MS_INS#	xD_CE#
SP4	SP4	SD_D4	MS_INS#	xD_WE#
SP5	SP5	SD_D1	MS_CLK	xD_D6
SP6	SP6	SD_D0	MS_D7	xD_D5
SP7	SP7	SD_CLK	MS_D3	xD_D4
SP8	SP8	SD_CMD	MS_D6	xD_D3
SP9	SP9	SD_D3	MS_D2	xD_D2
SP10	SP10	SD_D2	MS_D2	xD_D7
SP11	SP11	MS_BS	MS_BS	xD_CLE
SP12	SP12	SD_WP	MS_D1	xD_WP#
SP13	SP13	SD_CD#	MS_D5	xD_ALE
SP14	SP14	MS_D4	MS_D4	xD_D0
SP15	SP15	MS_D0	MS_D0	xD_D1
SP16	SP16	xD_CD#	xD_CD#	xD_CD#



97 SD\_WP\_Q >>> \_\_\_\_\_  
 97 SD\_CD#\_Q >>> \_\_\_\_\_

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Size: Custom	Document Number: <b>EA40 CX</b>	Rev: <b>-3</b>
Date: Thursday, June 20, 2013 Sheet 74 of 103		

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SSID = ExpressCard

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Date:	Thursday, June 06, 2013	Sheet	75 of 103

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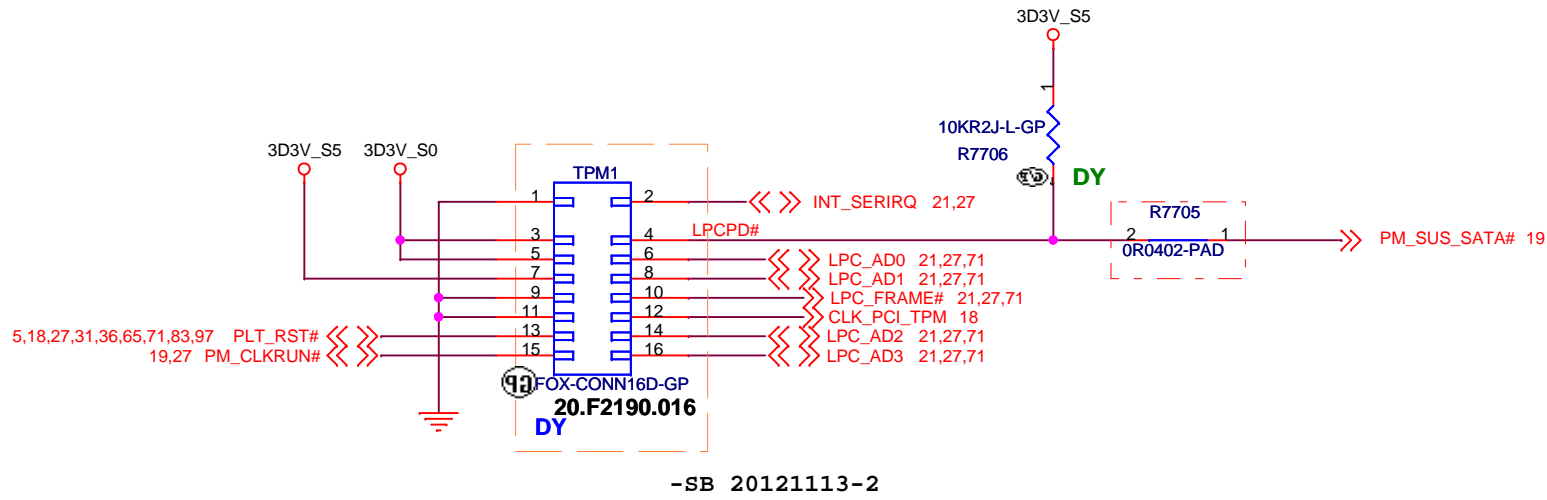
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Sheet 76 of 103


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Date: Thursday, June 20, 2013		Sheet 77 of 103

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Size

A4

Document Number

**EA40 CX**

Rev

**-3**

Date: Thursday, June 06, 2013

Sheet 78 of 103

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**SSID = User.Interface**

## Free Fall Sensor

Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

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<b>G- Sensor</b>			
Size	Document Number		Rev
A4	<b>EA40 CX</b>		<b>-3</b>
Date:	Thursday, June 06, 2013	Sheet 79	of 103

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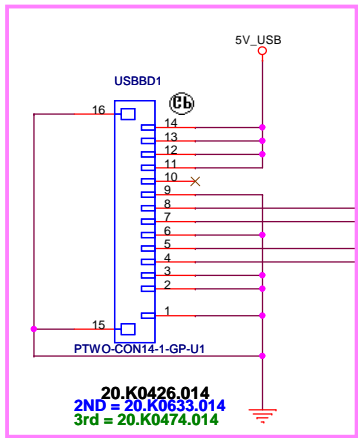
**EA40 CX**

**-3**

Date: Thursday, June 06, 2013

Sheet 81 of 103

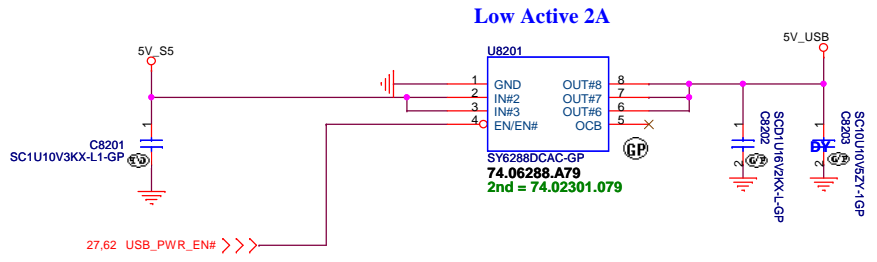
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 2ND = 20.K0633.014  
 3rd = 20.K0474.014

SB 20121102-1

-2 20130506-1  
 USB\_PN2 18,97  
 USB\_PP2 18,97  
 USB\_PN8 18,97  
 USB\_PP8 18,97



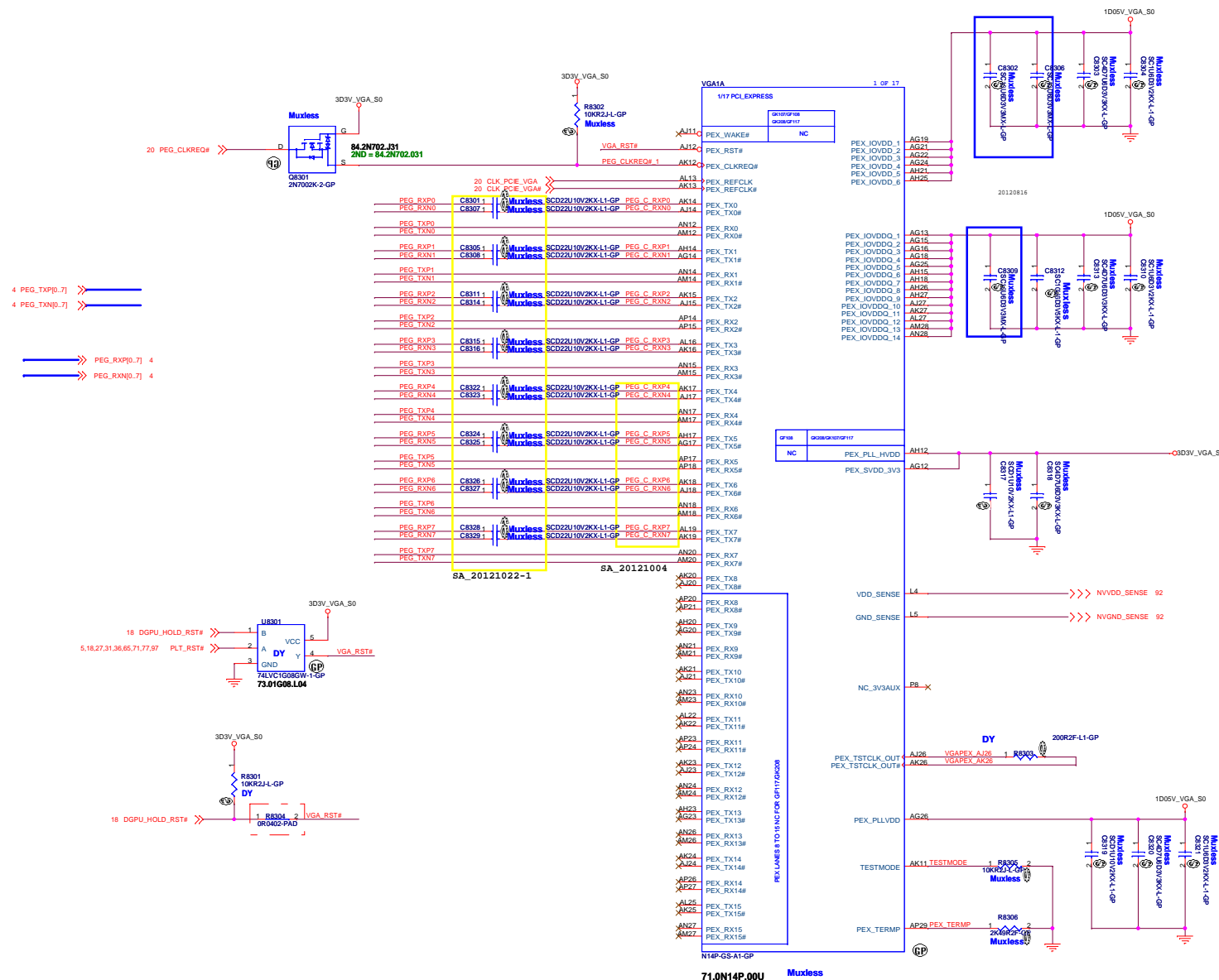
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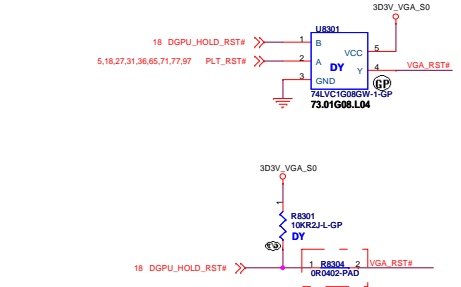
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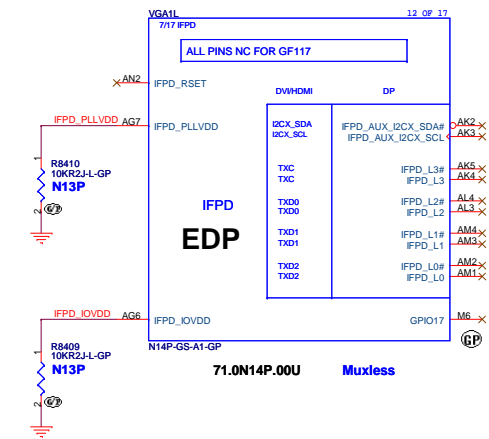
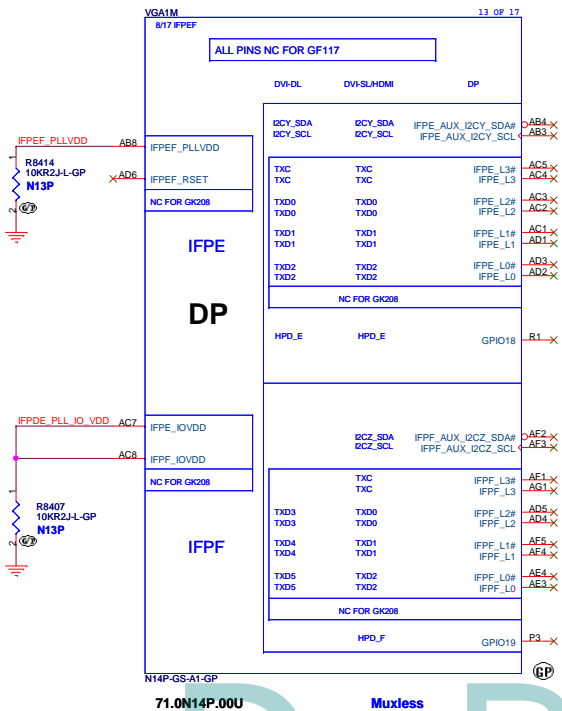
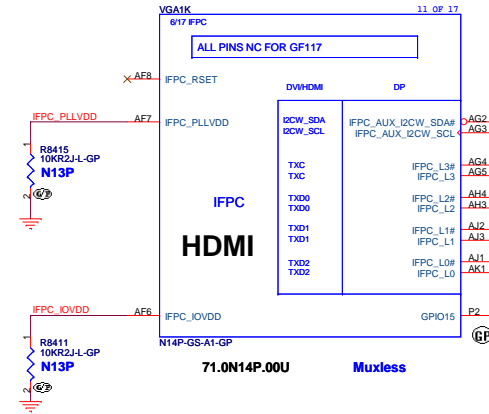
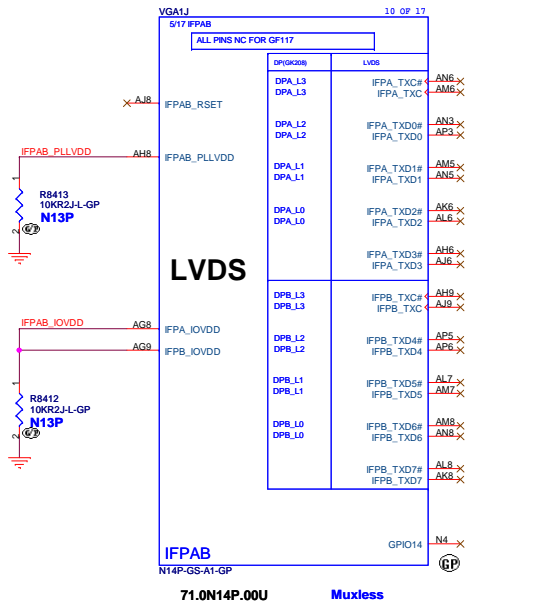
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Title: IO Board Connector		
Size: A3	Document Number: EA40_CX	Rev: -3
Date: Thursday, June 20, 2013	Sheet: 82	of: 103



4 PEG\_TXP[0..7] >>>  
 4 PEG\_TXN[0..7] >>>  
 4 PEG\_RXP[0..7] >>>  
 4 PEG\_RXN[0..7] >>>



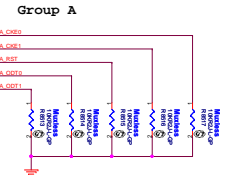
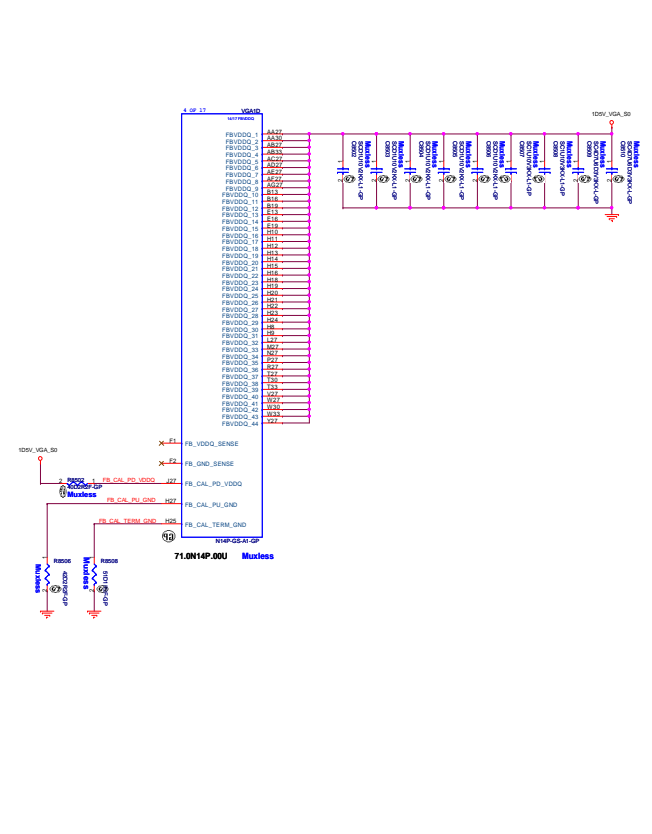
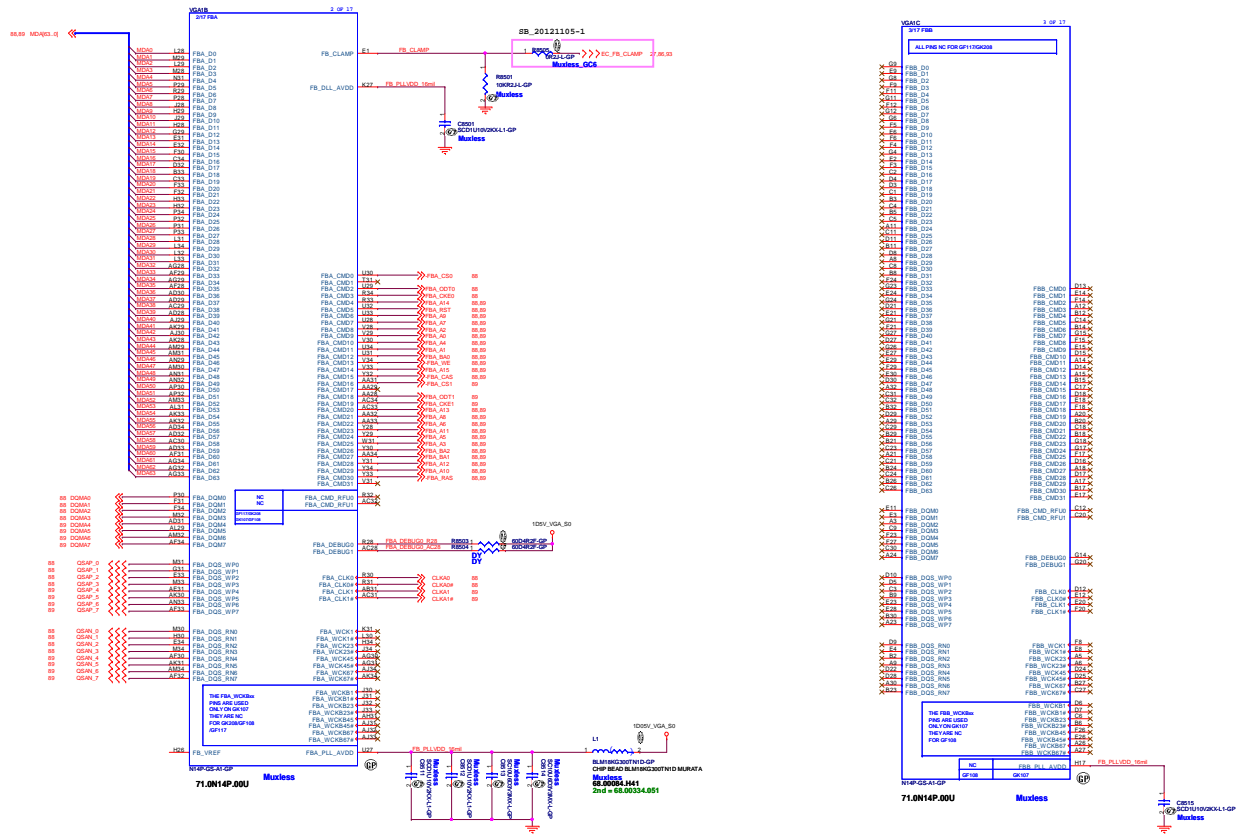
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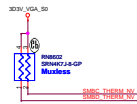
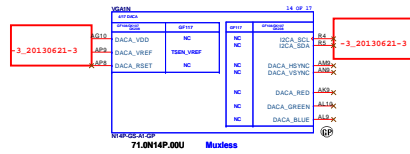
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<b>GPU (DIGITAL OUT)</b>			
Size	Document Number	Rev	
Custom	<b>EA40 CX</b>	-3	
Date:	Thursday, June 06, 2013	Sheet	84 of 103



FBCLK Termination place on VRAM side

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unknown function

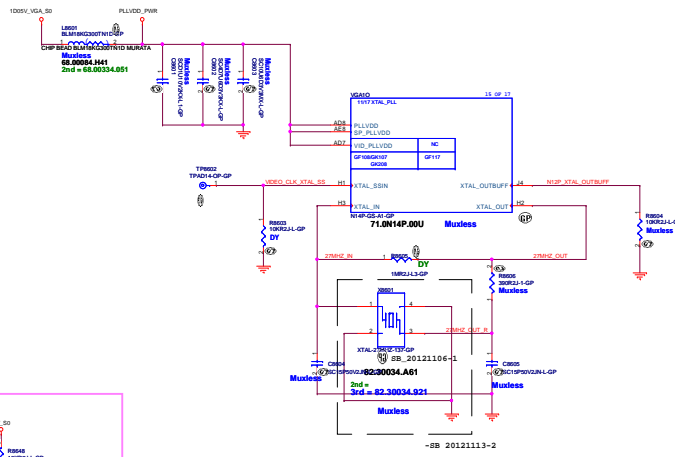
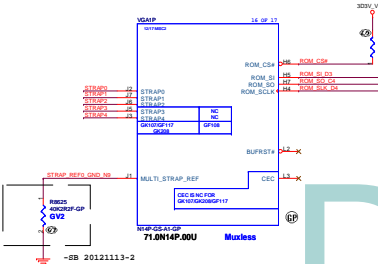
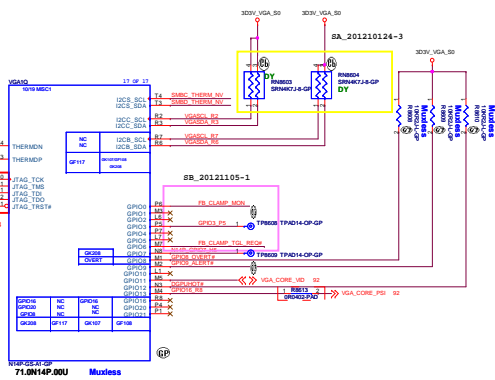
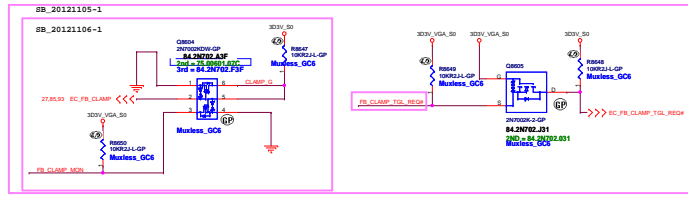
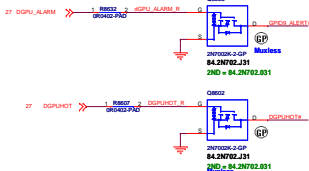


Table 113. Resistance Mapping to Hex Values

Resistor Values	Pull-up to VDD33	Pull-down to GND
4.99 k	1000	0000
10.0 k	1001	0001
15.0 k	1010	0010
20.0 k	1011	0011
24.9 k	1100	0100
30.1 k	1101	0101
34.8 k	1110	0110
45.3 k	1111	0111

4.99Kohm  
10Kohm  
15Kohm  
20Kohm  
24.9Kohm  
30.1Kohm  
34.8Kohm  
45Kohm

Table 1. N14M-GE/GL DDR3 Recommended Memories 128Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/FBVDQ	Manufacturer Part Number	Max Speed (MHz)	Memory Data Code Minimum	Status
128Mx16 DDR3	Micron	0x0	1.5 V / 1.5 V	MT41J128M16JF-093C-K	900	1130	Production ready
	Samsung	0x5	1.5 V / 1.5 V	K4V2G1644E-BC1A	1000	1204	Production ready
	Hynix	0x6	1.5V / 1.5V	H4V2G1644E-BC11	900	1204	Production ready
		0x7	1.5V / 1.5V	H5TQ2G63DFR-11C	1000	11/A	Production ready
		0xC	1.5V / 1.5V	H5TQ2G63DFR-11C	1000	11/A	Production ready

Table 2. N14M-GE/GL DDR3 Recommended Memories 256Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/FBVDQ	Manufacturer Part Number	Max Speed (MHz)	Memory Data Code Minimum	Status
256Mx16 DDR3	Samsung	0x0	1.5 V / 1.5 V	K4V4G1644E-HC11	900	N/A	Production ready
	Micron	0x0	1.5 V / 1.5 V	MT41H256M16HA-107G-E	900	N/A	Production ready
	Hynix	0x3	1.5V / 1.5V	H5TQ4G63MFR-11C	900	N/A	Production ready
		0x4	1.5V / 1.5V	H5TQ4G63MFR-11C	900	N/A	Production ready

N14M-GE use Binary Strap. Please see the below information.

Table 122 Binary Strap Mode Mapping

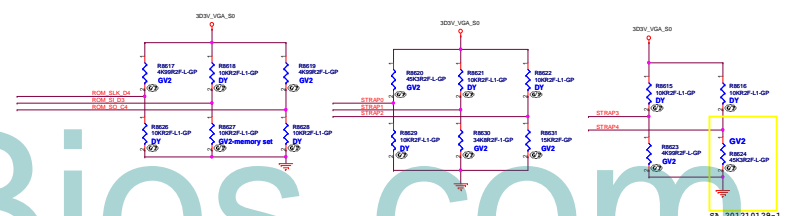
Strap Pin Name	Strap Mapping	Resistance	Polarity
ROM_SCLK	SMI_ALT_ADDR	10K Ω	Pull-down to GND
ROM_S1	SUB_VENDOR	10K Ω	Pull-up to 3V3 if VBIOS ROM exists Pull-down to GND if no VBIOS ROM
ROM_S0	VGA_DEVICE	10K Ω	Pull-down to GND (no display)
STRAP0	RAM_CFG[0]	10K Ω	See Note below
STRAP1	RAM_CFG[1]	10K Ω	See Note below
STRAP2	RAM_CFG[2]	10K Ω	See Note below
STRAP3	RAM_CFG[3]	10K Ω	See Note below
STRAP4	PCIE_MAX_SPEED	10K Ω	Pull-down to GND

N14P-GV2

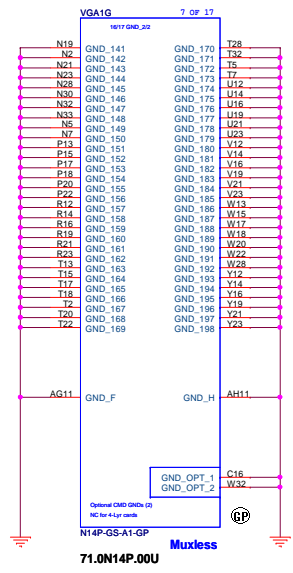
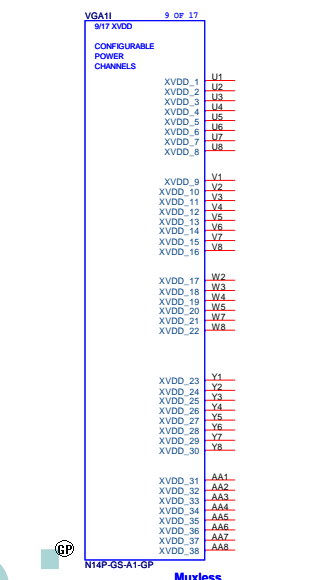
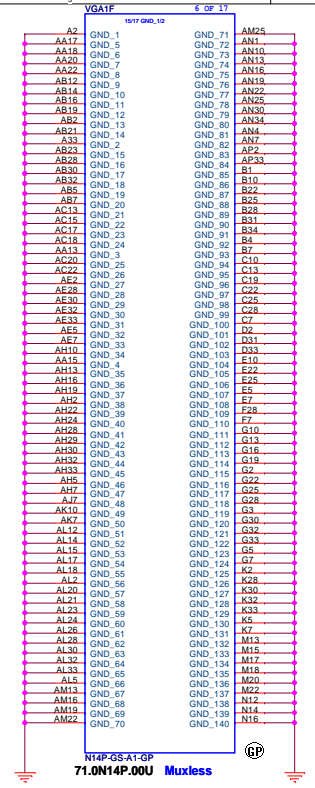
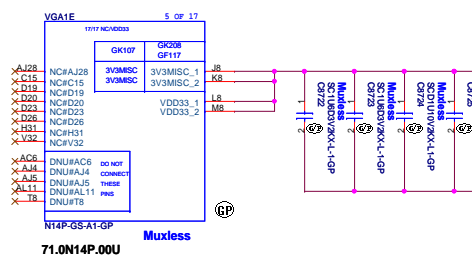
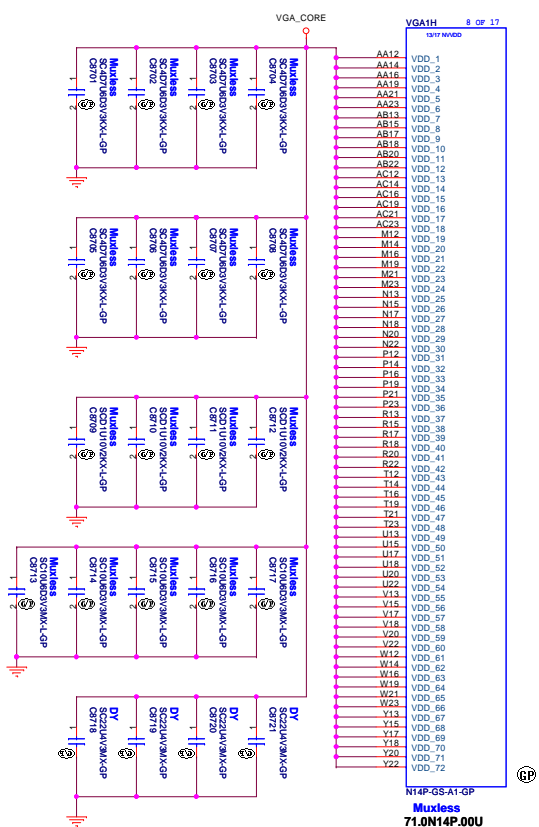
Strap Pin Name	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM
ROM_S1	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_S0	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP 0	USER[3]	USER[2]	USER[1]	USER[0]
STRAP 1	3G10_PADCFG[3]	3G10_PADCFG[2]	3G10_PADCFG[1]	3G10_PADCFG[0]
STRAP 2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP 3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP 4	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Support: 0x0

N14P-GT1-A2	0x0FE4	0010	15K ohm pull-down	0100	25K ohm pull-down
N14P-GV2-B-A1	0x1292	1000	5K ohm pull-up	0010	15K ohm pull-down



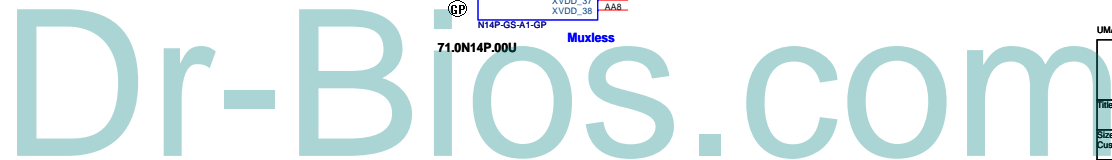
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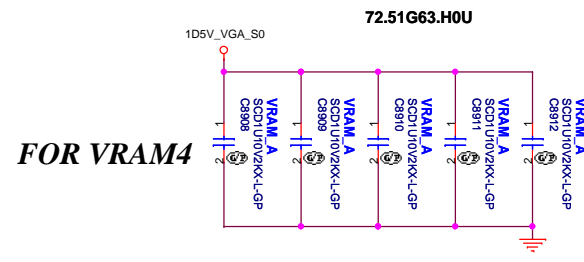
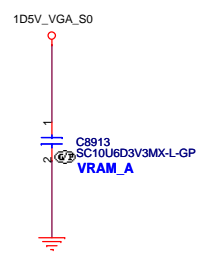
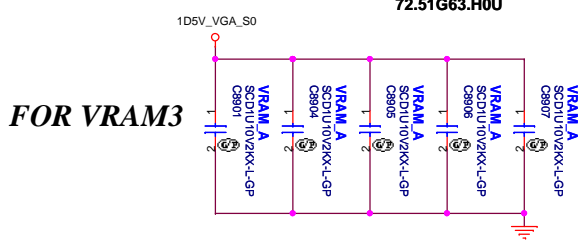
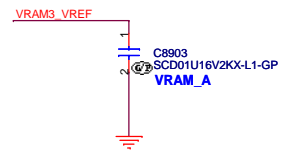
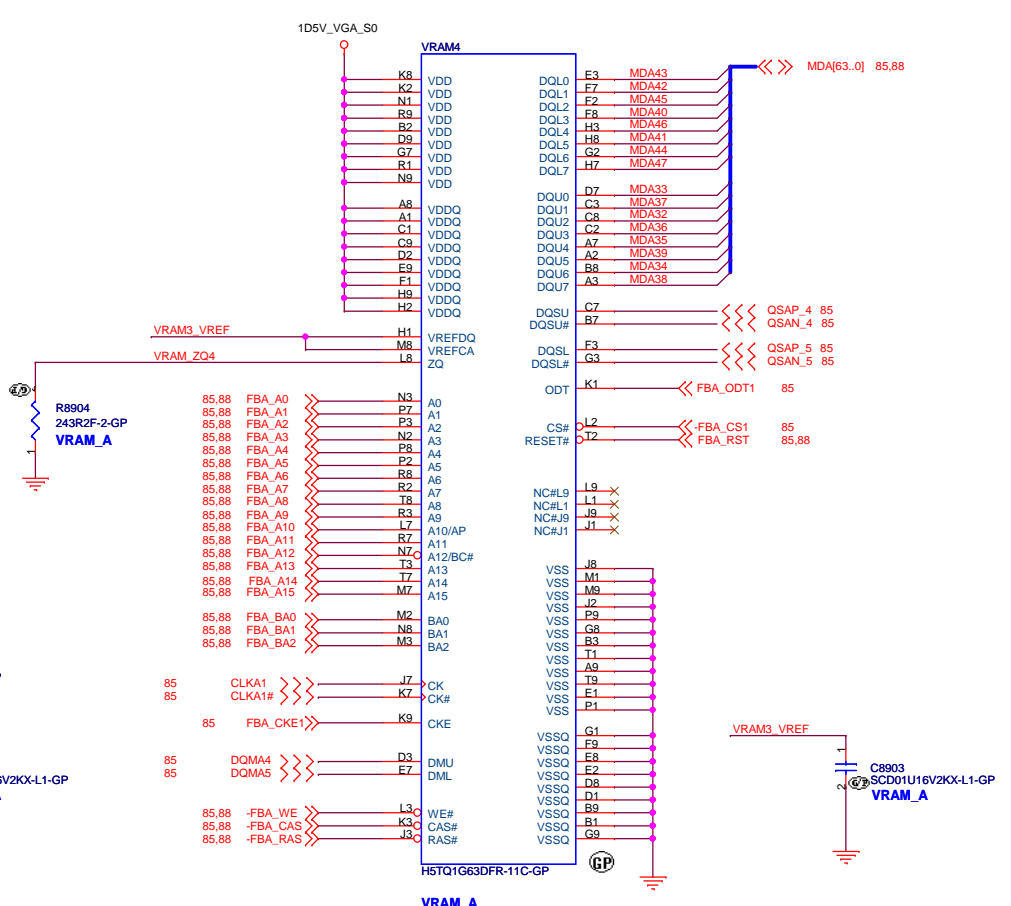
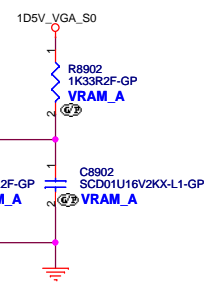
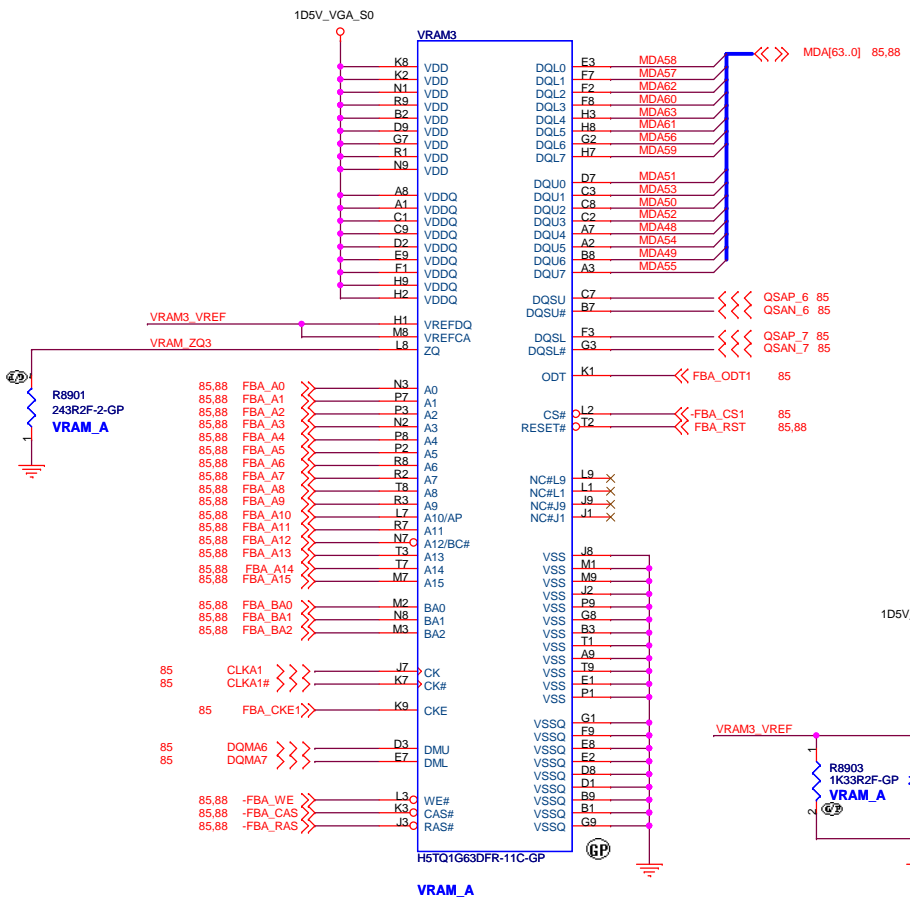
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Size	Document Number	Rev
Customer	<b>EA40 CX</b>	<b>-3</b>
Date	Friday, June 21, 2013	Sheet 87 of 103







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Size Custom	Document Number <b>EA40_CX</b>	Rev <b>-3</b>
Date: Thursday, June 06, 2013	Sheet 90 of 103	





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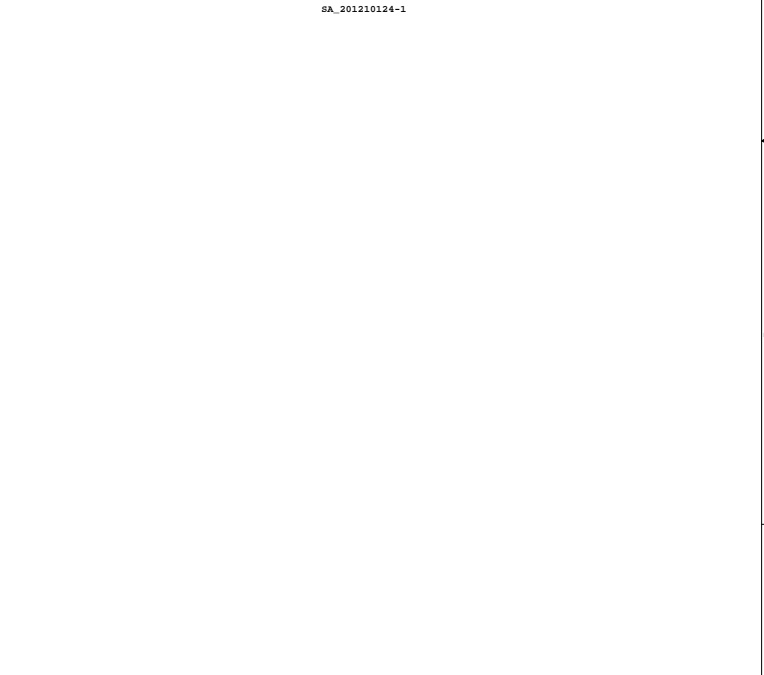
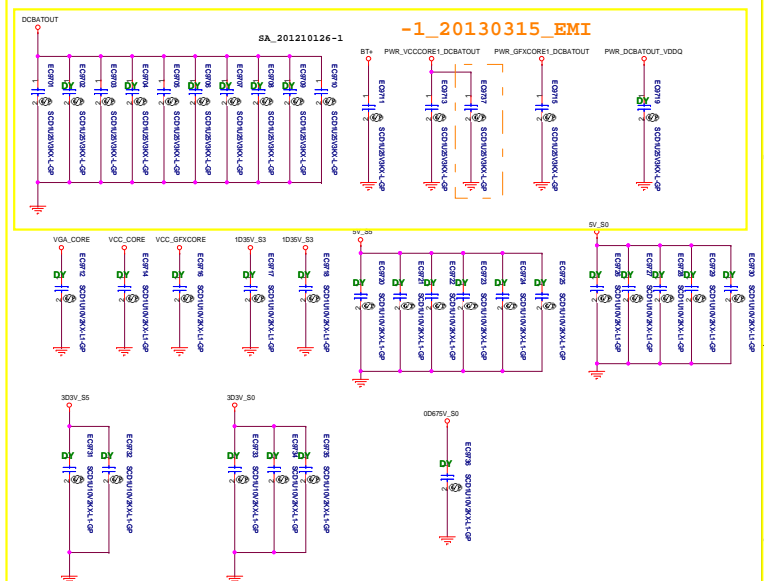
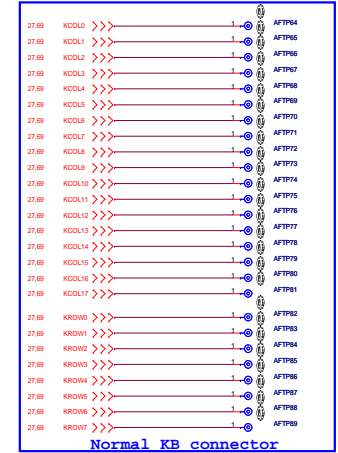
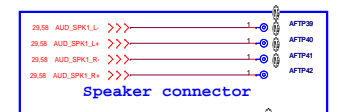
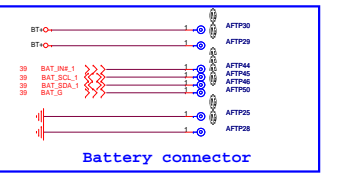
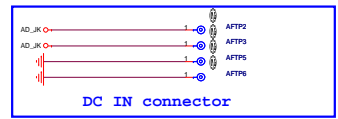
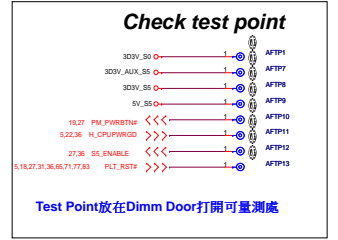
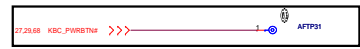
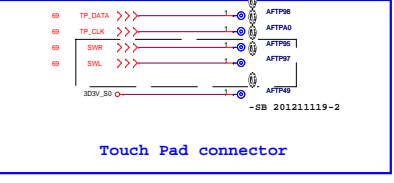
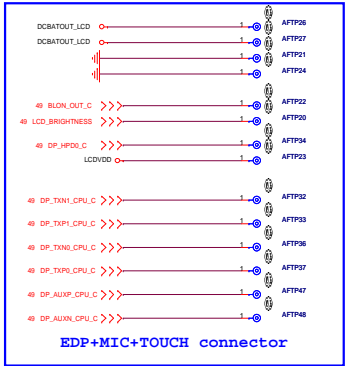
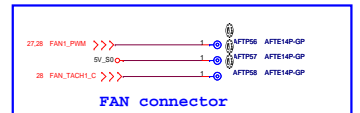
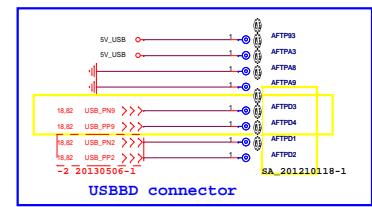
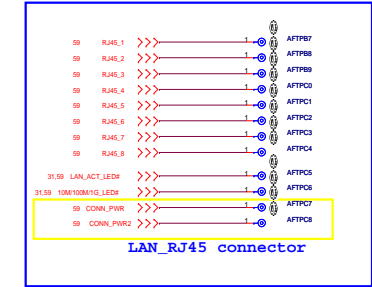
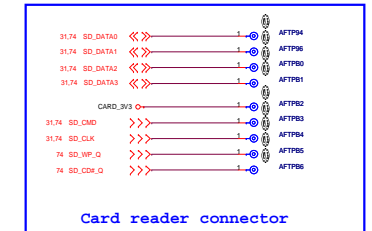
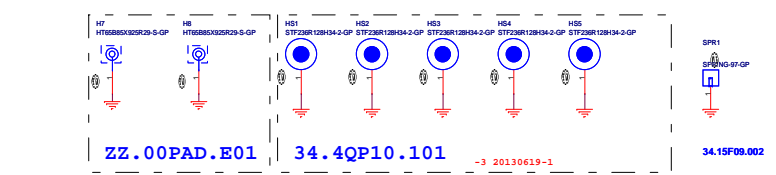
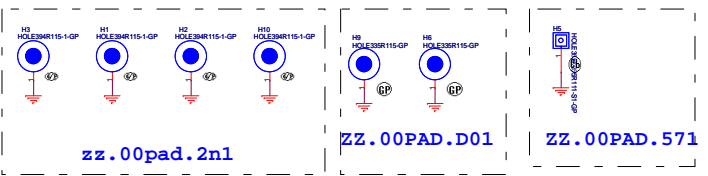
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TOUCH PANEL			
Size A2	Document Number	Rev	
	EA40 CX	-3	
Date: Thursday, June 06, 2013	Sheet 98	of	103

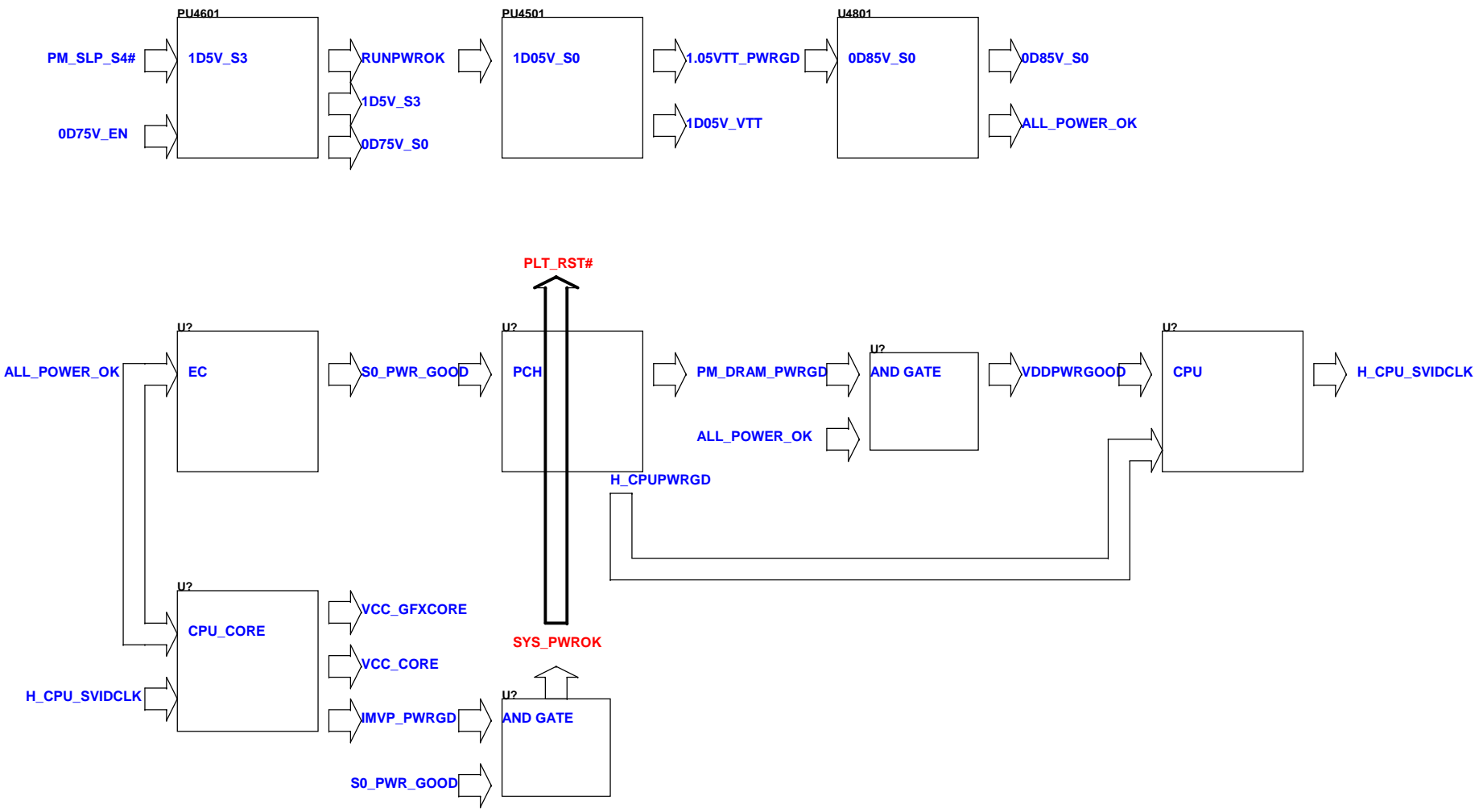




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# Power Sequence

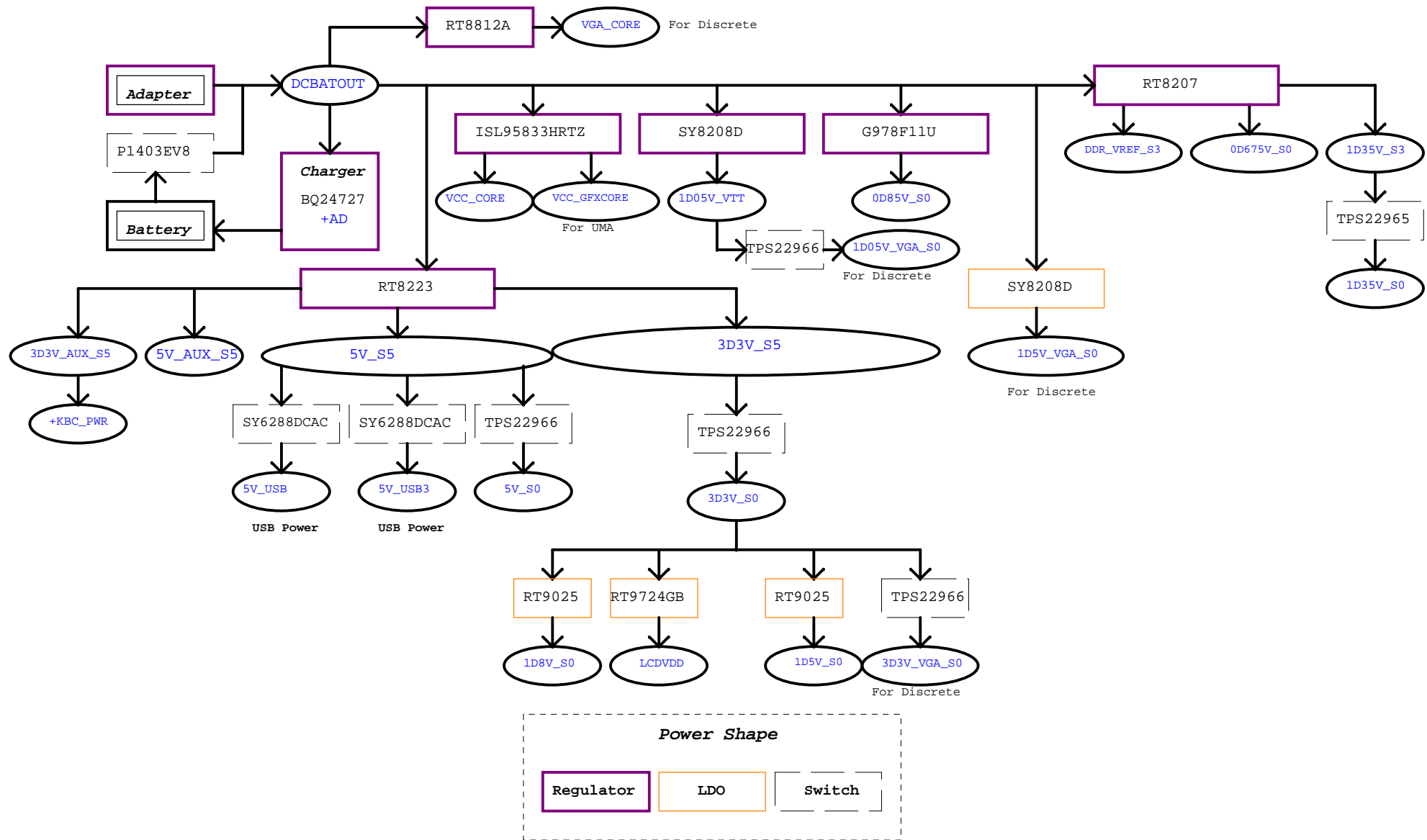


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Size A3	Document Number
Date: Thursday, June 06, 2013	EA40_CX
Sheet 98 of 103	Rev -3



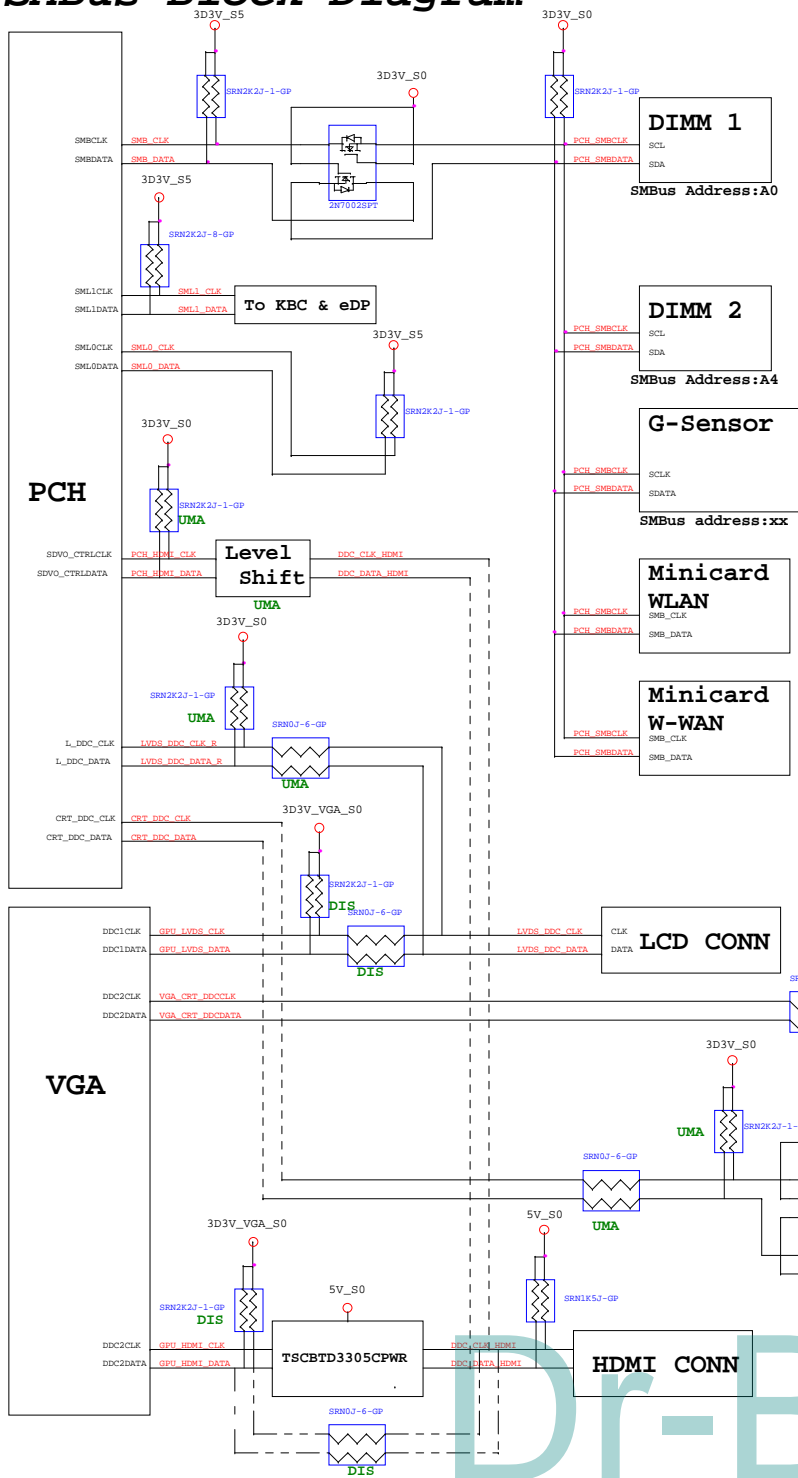


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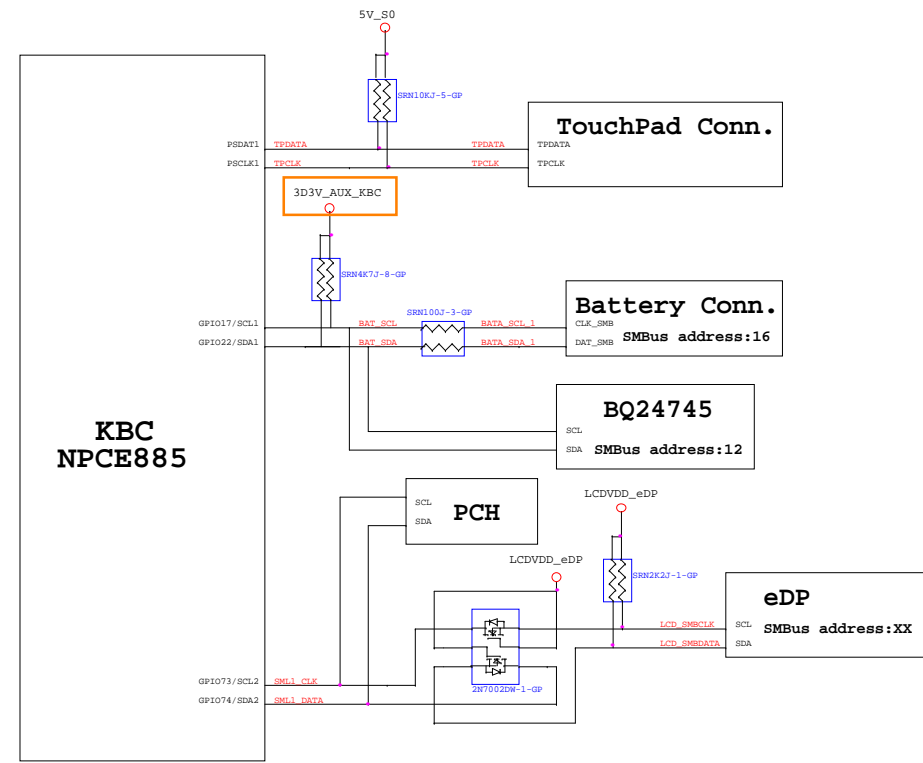
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Title <b>Power Block Diagram</b>			
Size A3	Document Number <b>EA40 CX</b>	Rev <b>-3</b>	
Date: Thursday, June 06, 2013	Sheet 100	of	103

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# PCH SMBus Block Diagram



# KBC SMBus Block Diagram

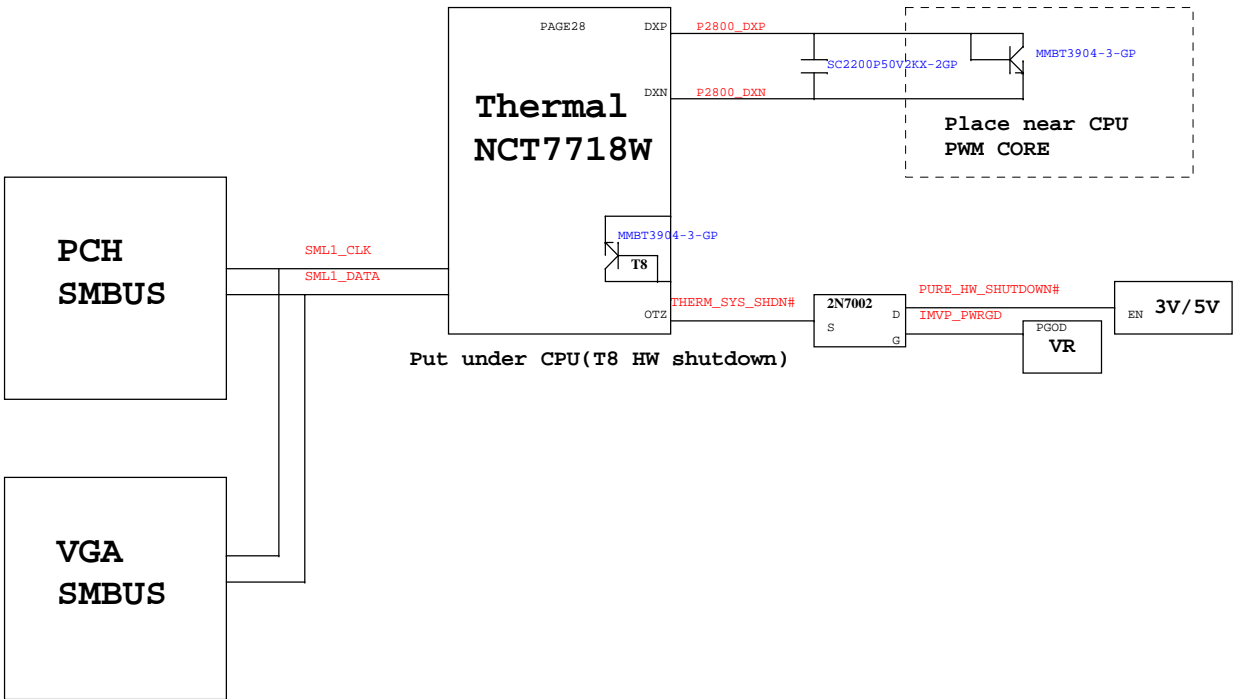


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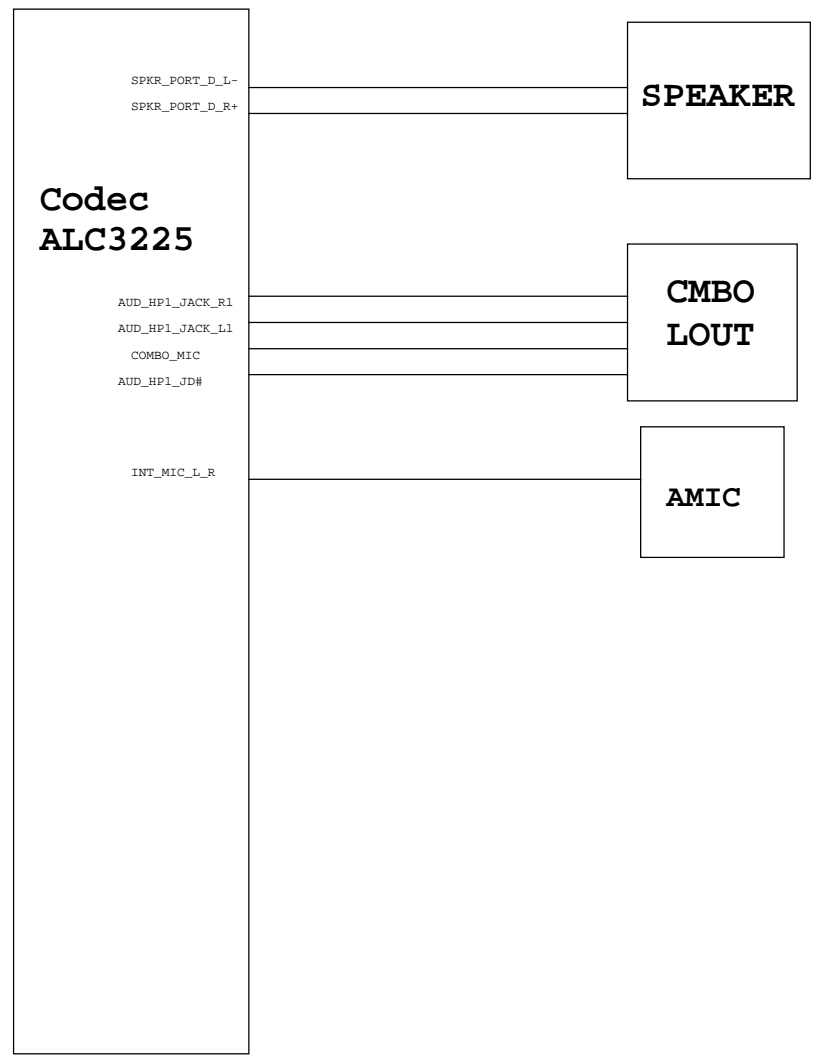
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File	EA40 CX	Document Number	Rev
Size		EA40 CX	3
Date:	1/16/2010, 10:08:18 AM	Sheet	101 of 108

# Thermal Block Diagram



# Audio Block Diagram



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Size	Document Number	Rev	
Custom	EA40 CX	-3	
Date:	Thursday, June 06, 2013	Sheet	102 of 103