

INTEL SYSTEM DIAGRAM

01

+3V/+5V S5
PG.39
+1.05V/+1.5V
PG.40/45
CPU Core
PG.42~43
DDR4
PG.41
Charge
PG.38
VGA POWER
PG.46~47
VCCGT/VCCSA
PG.44

SODIMM1
Max. 16GB
STD PG.17

2400MT/s
DDR4 L
Channel A

SODIMM2
Max. 16GB
STD PG.18

2400MT/s
DDR4 L
Channel B

INTEL SkyLake-H
Processor : Dual / Quad Core
Power : 45 (Watt)
Package : BGA1400
Size : 42 x 28 (mm)

PG.2~8

GPU N16P-GT
P19~P23

VRAM DDR3
P24~P27

INTEL PCH Lynx Point
Power : Watt
Package : FCBGA837
Size : 23 x 23 (mm)

PG.9~15

HDD
PG.33

SATA2 6GB/s

PCI-E x 1

Port4
LAN
RTL8111GSH
10/100/1000 PG.31

Port3
WLAN BT COMBO
PG.34

USB 2.0
PORT7

PCI-E x 4

SATA0~1 6GB/s
NGFF SSD
PG.34

KBC
ITE IT8987E/BX PG.37

LPC Interface

TPM
NPCT650 PAGE 33

KB PG.35

TP PG.35

ROM PG.12

FAN PG.35

SLG3NB3454
GreenCLK
PAGE 33

25MHz

G- Sensor
P35

AUDIO CODEC
ALC255 PG.32

Speaker PAGE 32

Dual Digital MIC PAGE 32

Universal HP
P32

USB3-1 & USB3-2
USB 3.0
PORT1,2

USB3.0 Ports
X2
PG.36

Webcam
PG.29

Card Reader
PG.36

USB 2.0
PORT1,2

DB IO Port
PG.36

Touch Screen
PG.29

PEG

GPU N16P-GT ↔ **VRAM DDR3**

X'TAL 27MHz

eDP (5.4Gb/s) eDP → **eDP Conn.** P29

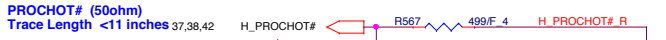
DDI2 → **ITE6515** P28 → **VGA Conn.** P29

DDI1 → **PS8407** P30 → **HDMI Conn.** P30

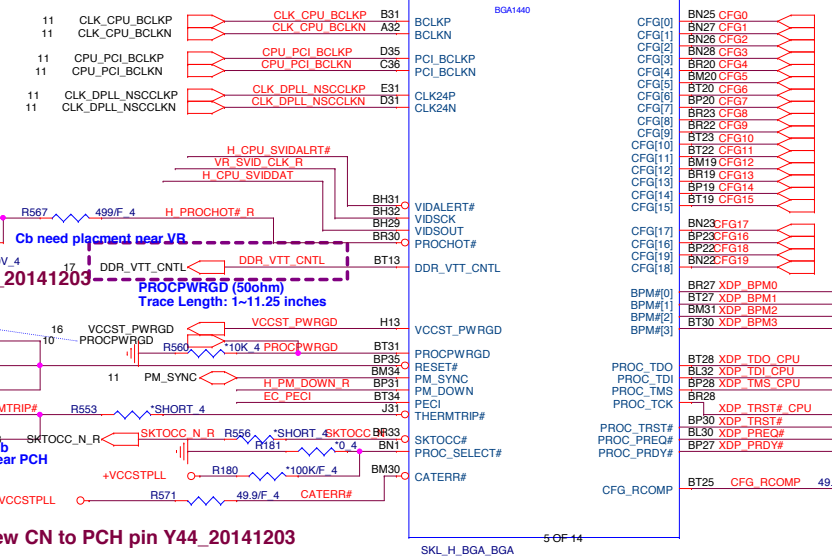
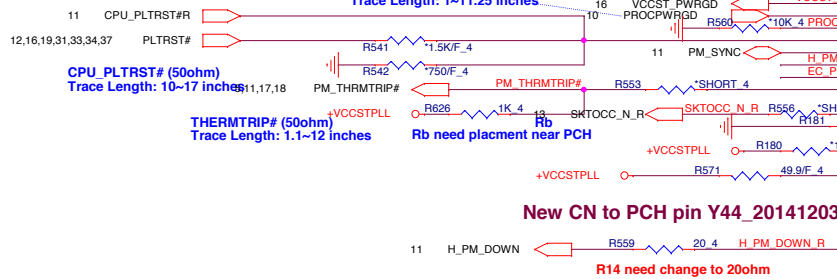
Dr-Bios.com

	PROJECT :ZRY		
	Quanta Computer Inc.		
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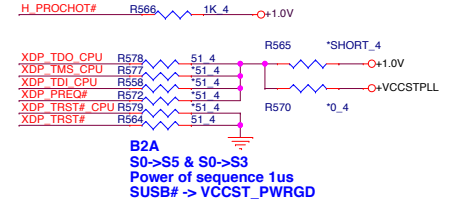
Host CLK: Trace length < 11000 MILS Trace spacing = 15, 20 MILS, Impedence 90 ohm



CPU RESET#

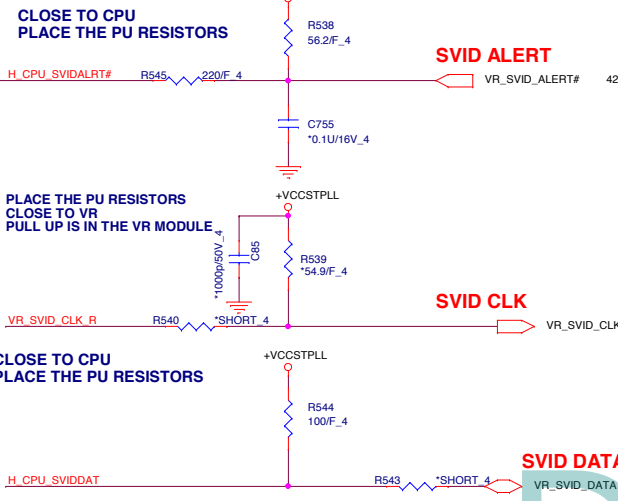


Processor pull-up (CPU)

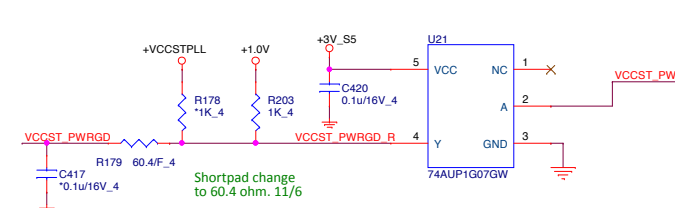


CPU CORE SVID

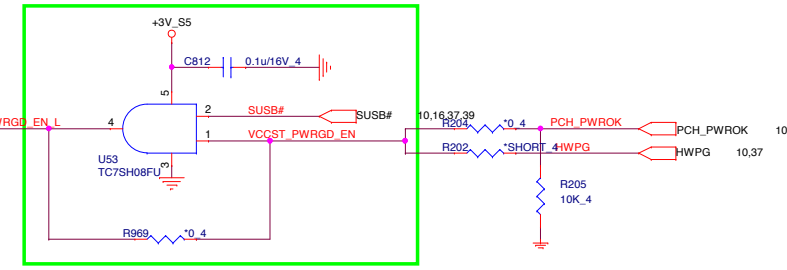
Layout note: need routing together and ALERT need between CLK and DATA.



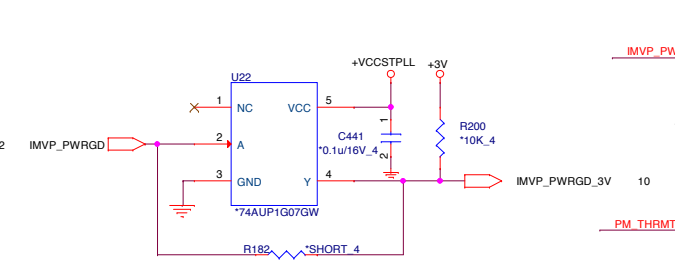
HWPDP VCCST PWRGD



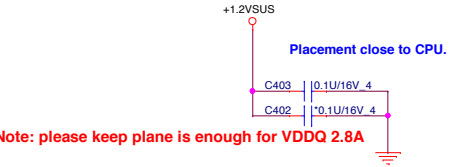
CRB is via +1.05V PG



CPU thermal trip

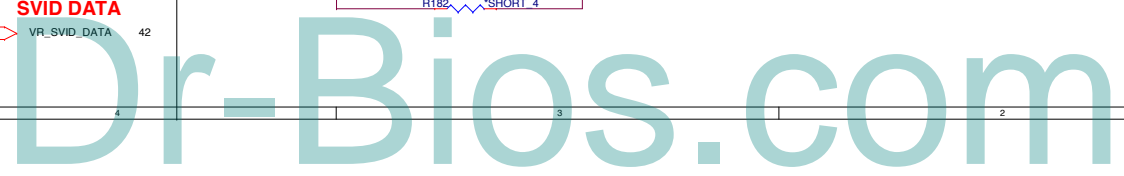


CPU VDDQ Del R2574_20141217



Note: please keep plane is enough for VDDQ 2.8A

Table with project information: PROJECT :ZRY Quanta Computer Inc., Document Number 02 - SKYPAKE 1/20(eDP/DDI), Date: Monday, September 07, 2015, Sheet 2 of 49.



SKYLAKE HALO (DMI PEG, PD)

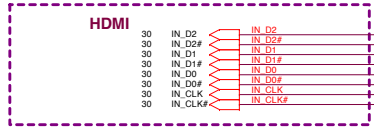
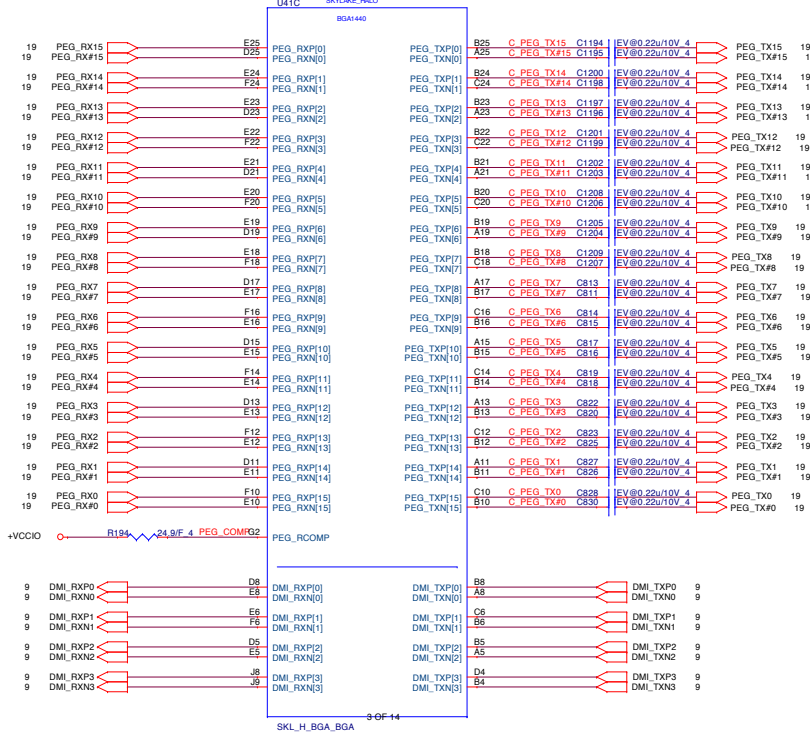
Lane Reversed

dGPU PEG*16

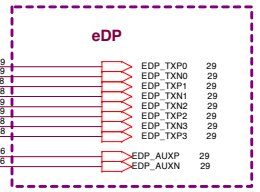
Lane Reversed

PEG_RCOMP
Trace length < 400 MILS
Trace width = 12 MILS
Trace spacing = 15 MILS

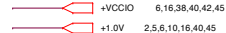
DMI



CRT



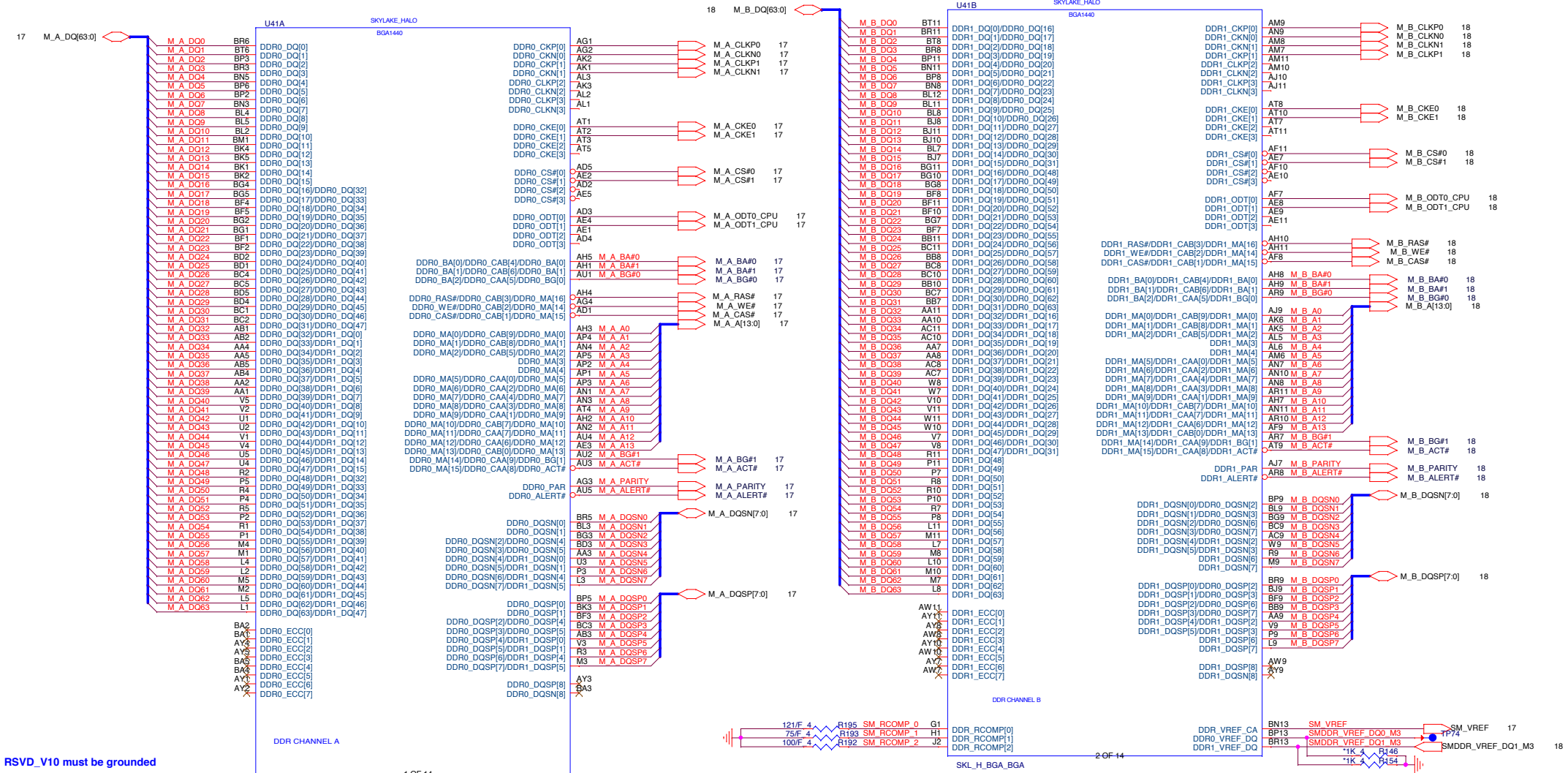
DP & PEG Compensation
eDP_RCOMP
Trace length < 100 Mils
Trace Width 20 Mils Trace Spacing 25 Mils



PROJECT :ZRY
Quanta Computer Inc.

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SKYLAKE Processor (DDR3)



RSVD_V10 must be grounded

SKL_H_BGA_BGA 1 OF 14

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		Quanta Computer Inc.	
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	SNB 2/5 (DDR3 I/F)		

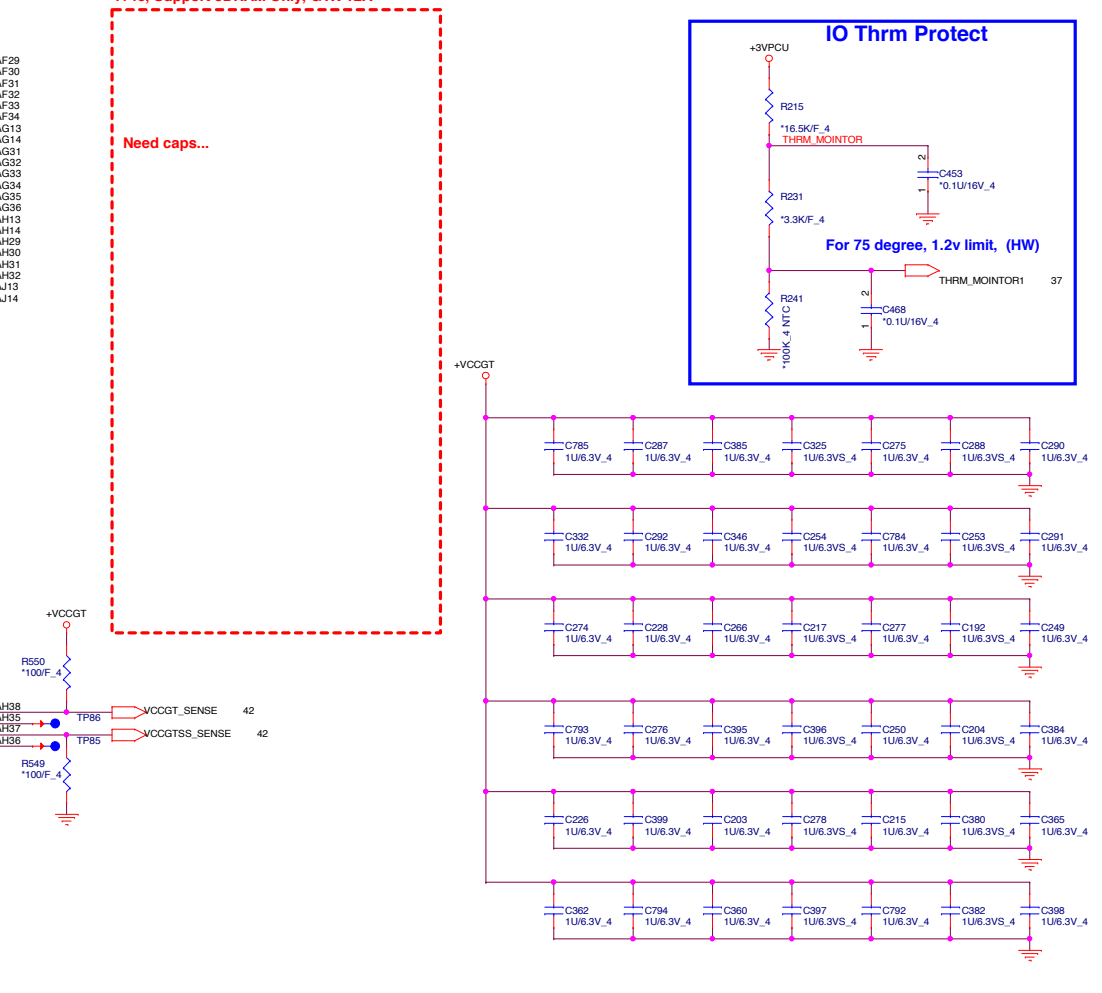
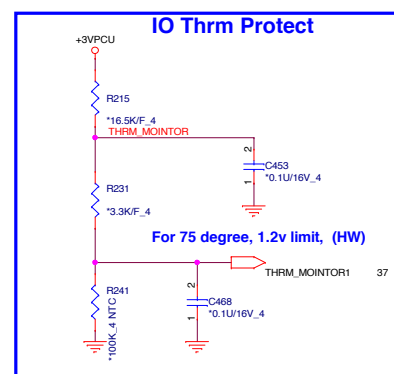
Follow SKL H EDS page 133 to 45W(GT4+OPC): +VCCGT=104A/12A (GTx)
 Follow SKL H EDS page 133 to 45W(GT2): +VCCGT=55A

+1.5V 14,30,32,34,45
 +1.2V5US 2,6,10,17,18,41

Follow SKL H DG page 574 to place Cap
 22uF x 14, 10uF x 35, 1uF x 68

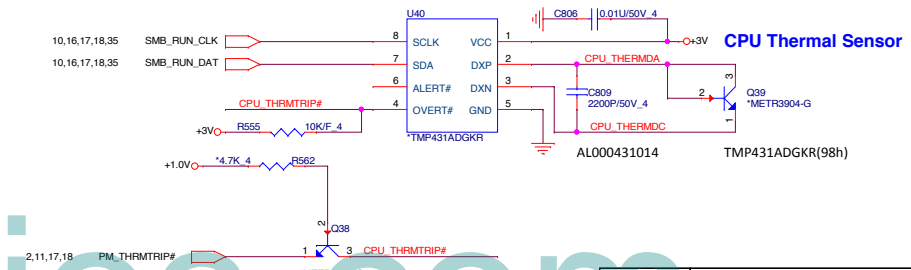
4+4e, Support eDRAM Only, GTX 12A

Need caps...



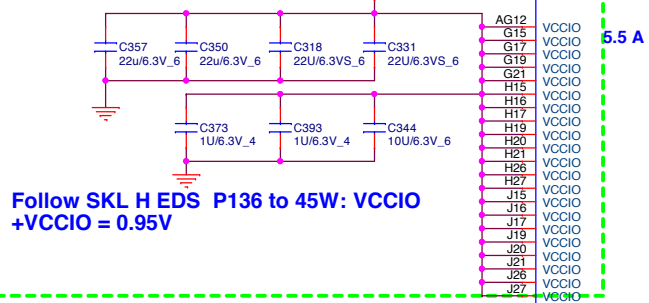
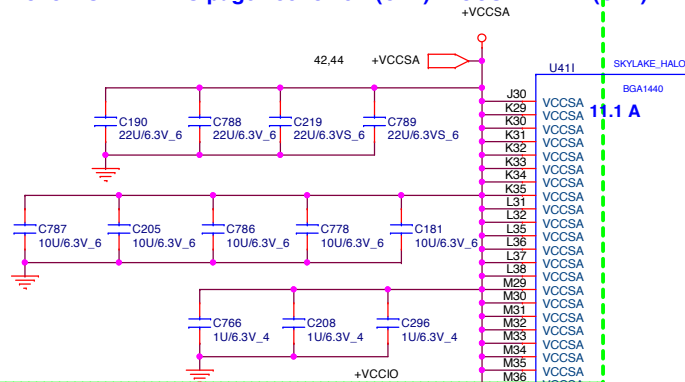
Capacitor Value	Quantity	Location
22uF	14	6.3V_6
10uF	35	6.3V_6
1uF	68	6.3V_6

Local CPU Thermal Sensor



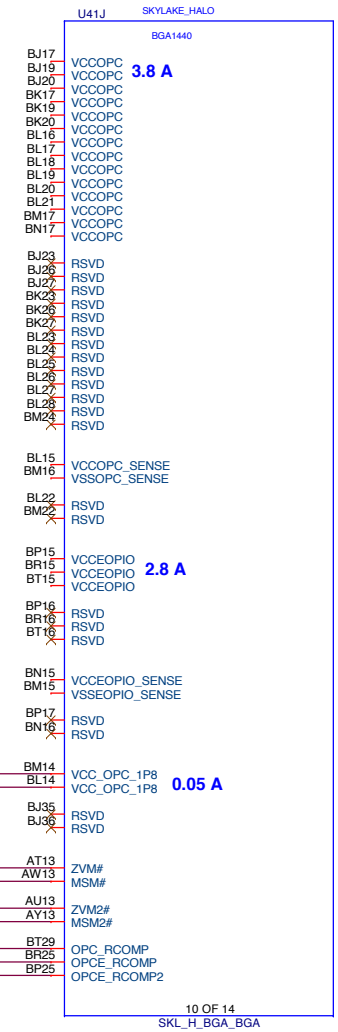
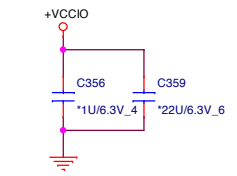
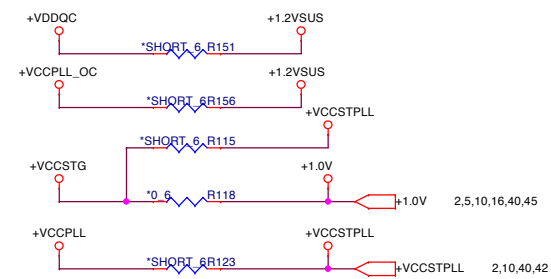
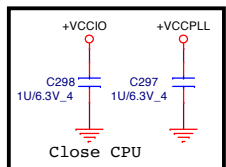
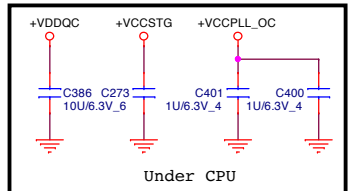
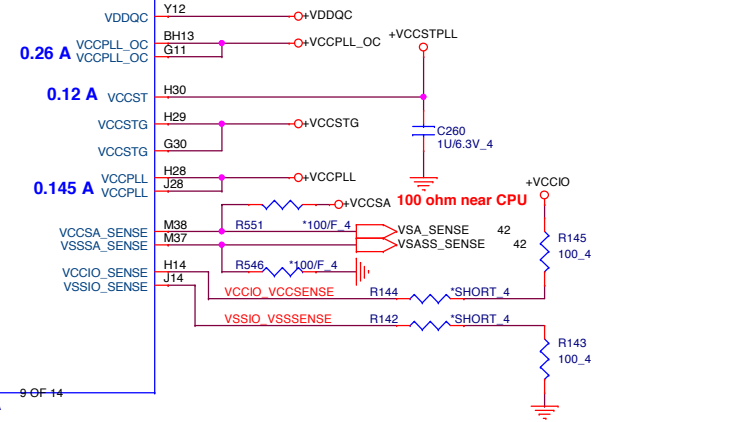
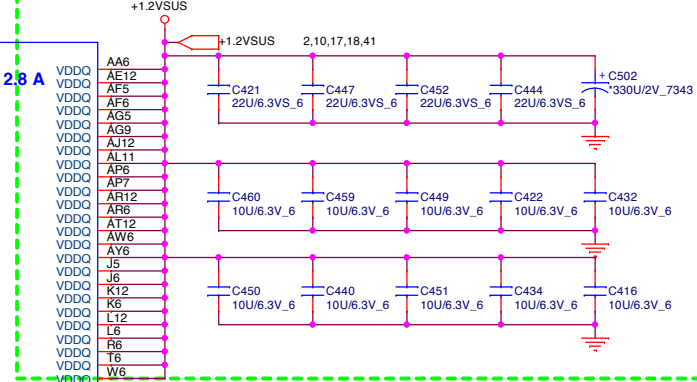
EDRAM Only, PLACE CAPS IN ACK SIDE

Follow SKL H EDS page 135 to 45W(GT2): VCCSA=11.1A (GTx)

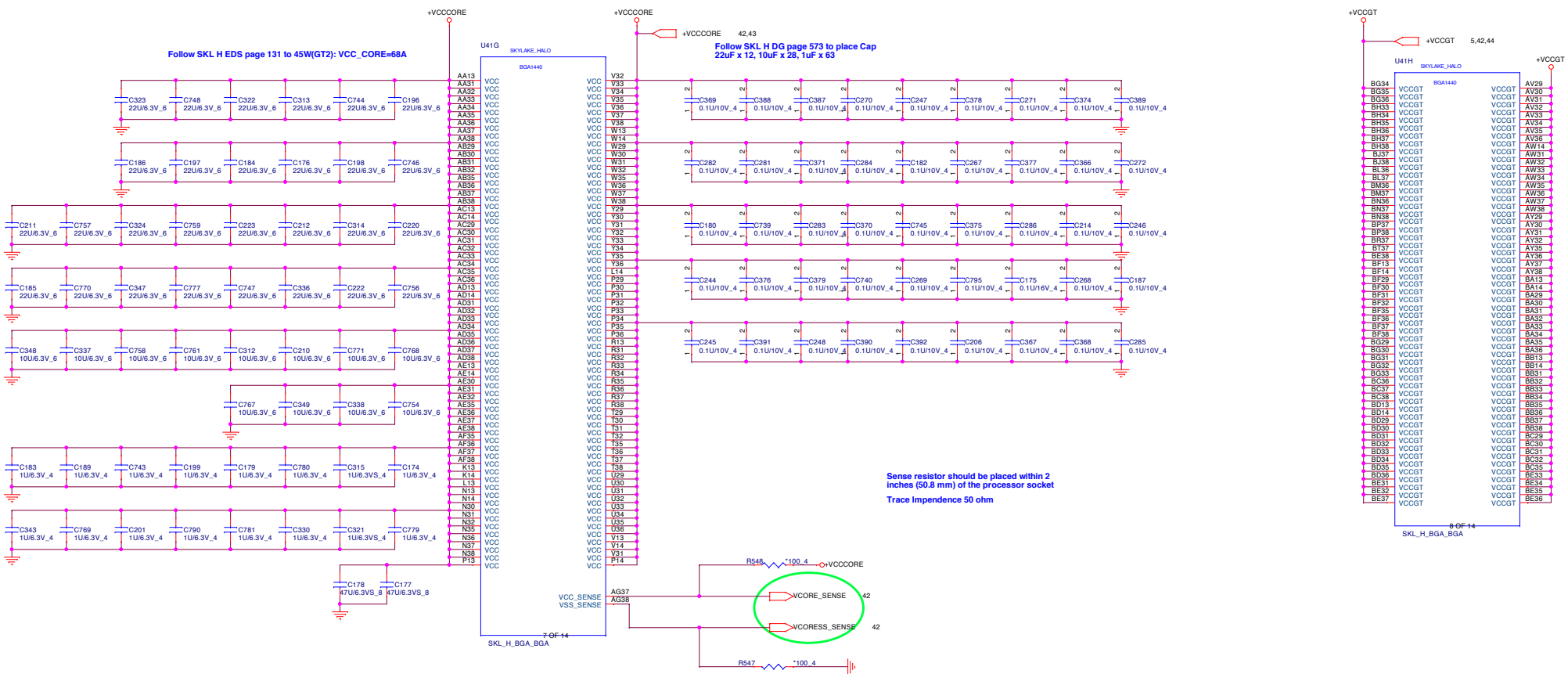


Follow SKL H EDS P136 to 45W: VCCIO +VCCIO = 0.95V

Follow SKL H EDS page 135 45W: VDDQ=2.8A



原本 net name



Change R2053 to NI_20141203

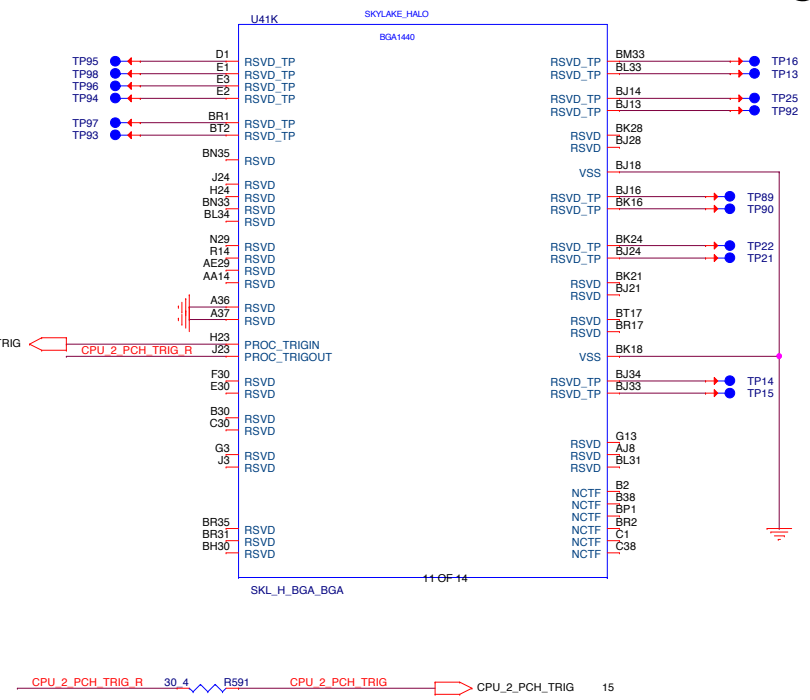


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		Quanta Computer Inc.		1A	
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Custom	SNB 4/5 (POWER & GND)	Tuesday, August 25, 2015		7	49

Haswell Processor (GND)



Haswell Processor (RESERVED, CFG)



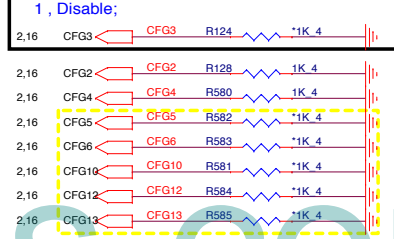
Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training

CFG[3] (PHYSICAL_DEBUG_ENABLED (DFX PRIVACY))

0 Enable; SET DFX ENABLED BIT IN DEBUG
 1, Disable;



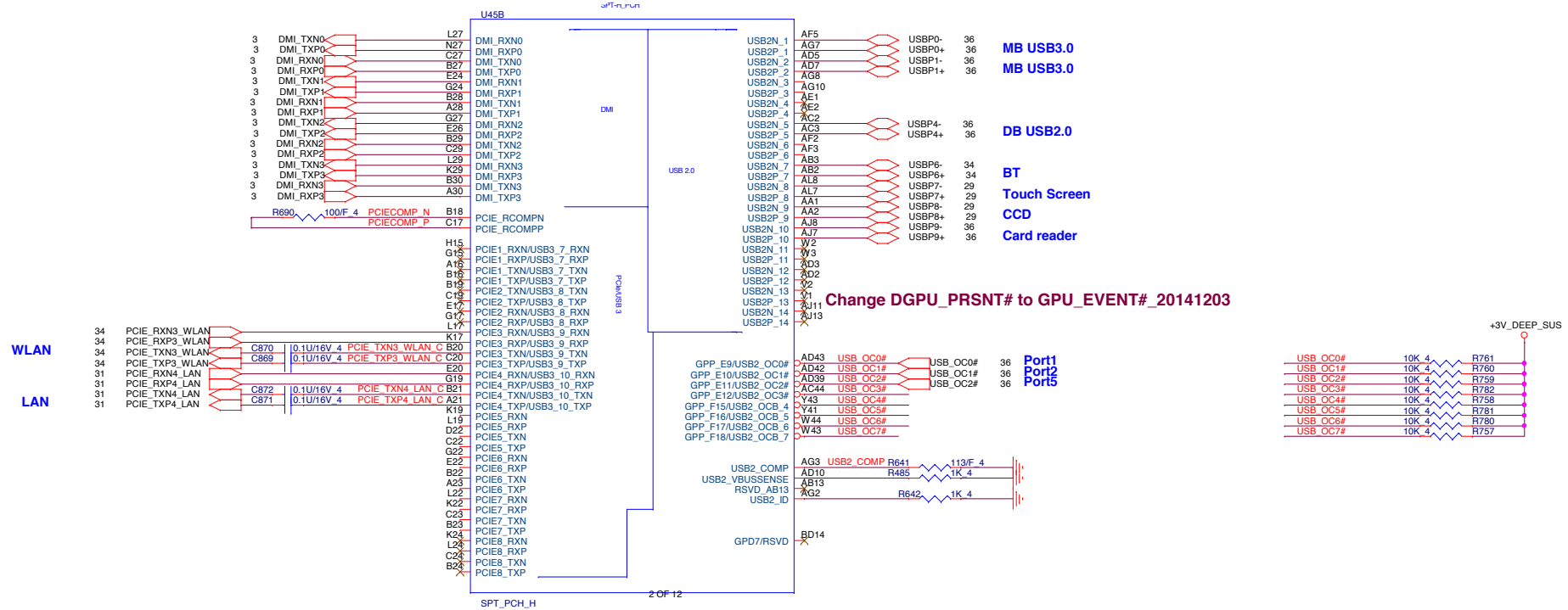
CFG[6:5] (PCIe Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
 10: x8, x8 - Device 1 function 1 enabled; function 2 disabled
 01: Reserved - (Device 1 function 1 disabled; function 2 enabled)
 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

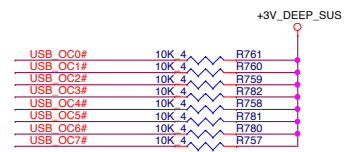
PROJECT :ZRY

Quanta Computer Inc.

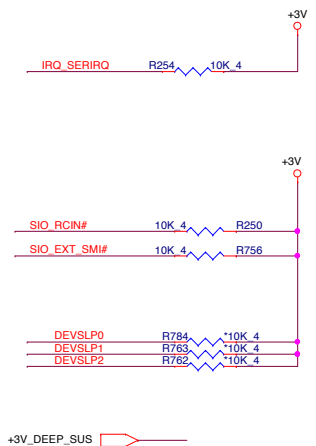
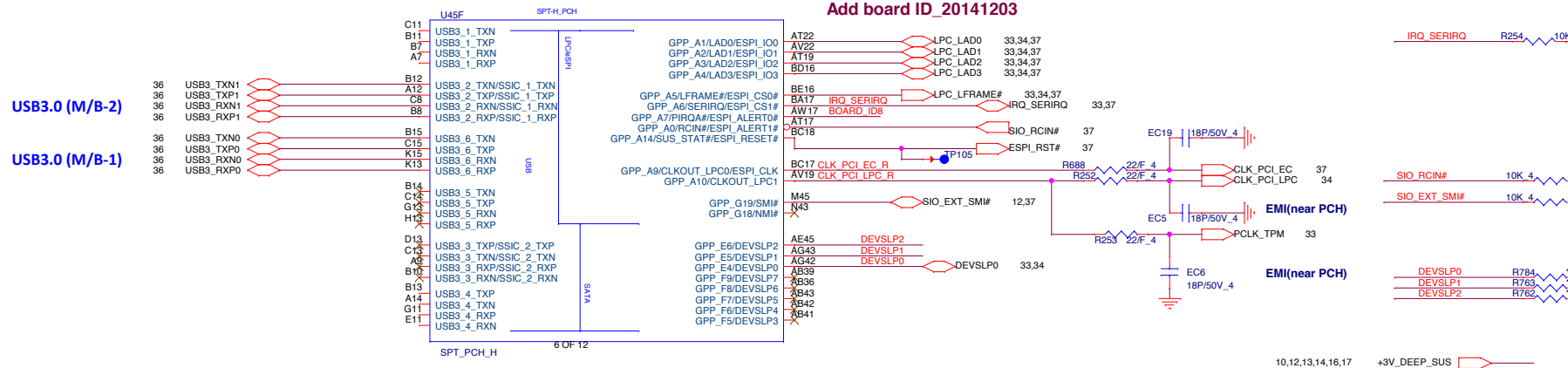
Size Custom	Document Number SNB 5/5 (GND)	Rev 1A
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Change DGPU_PRSENT# to GPU_EVENT#_20141203



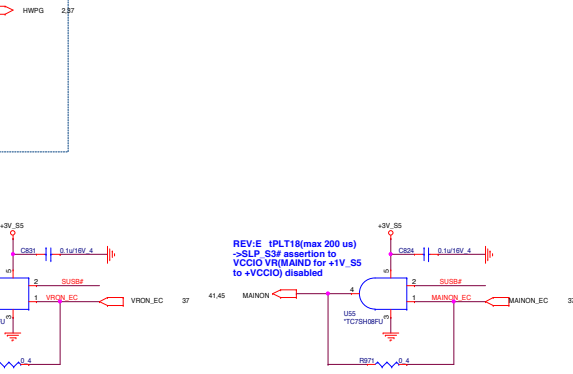
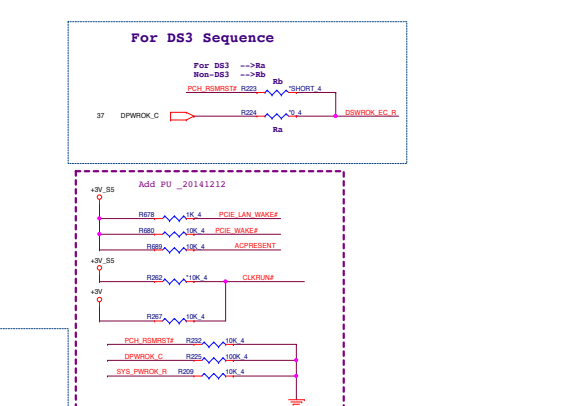
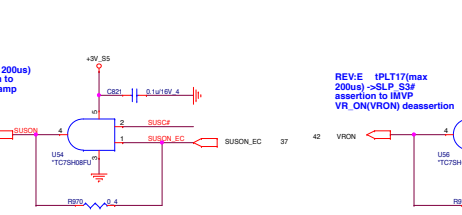
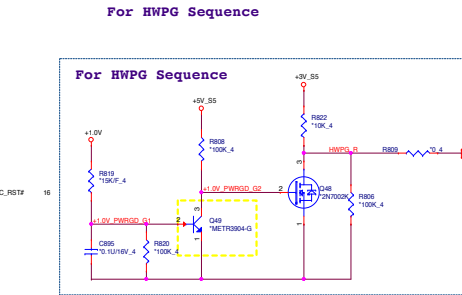
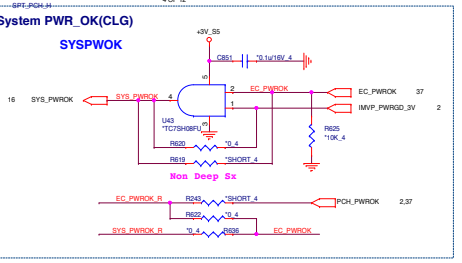
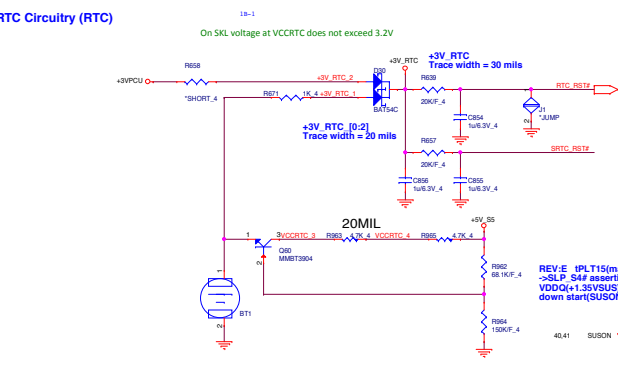
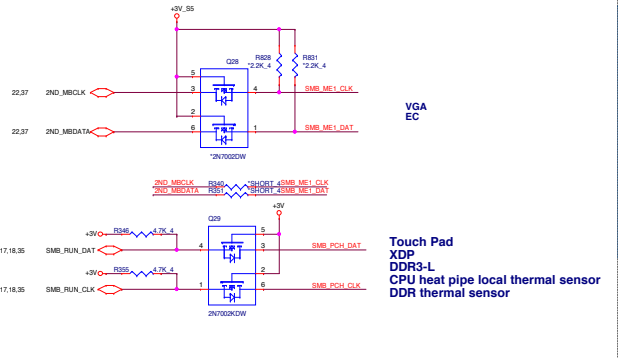
Add board ID_20141203

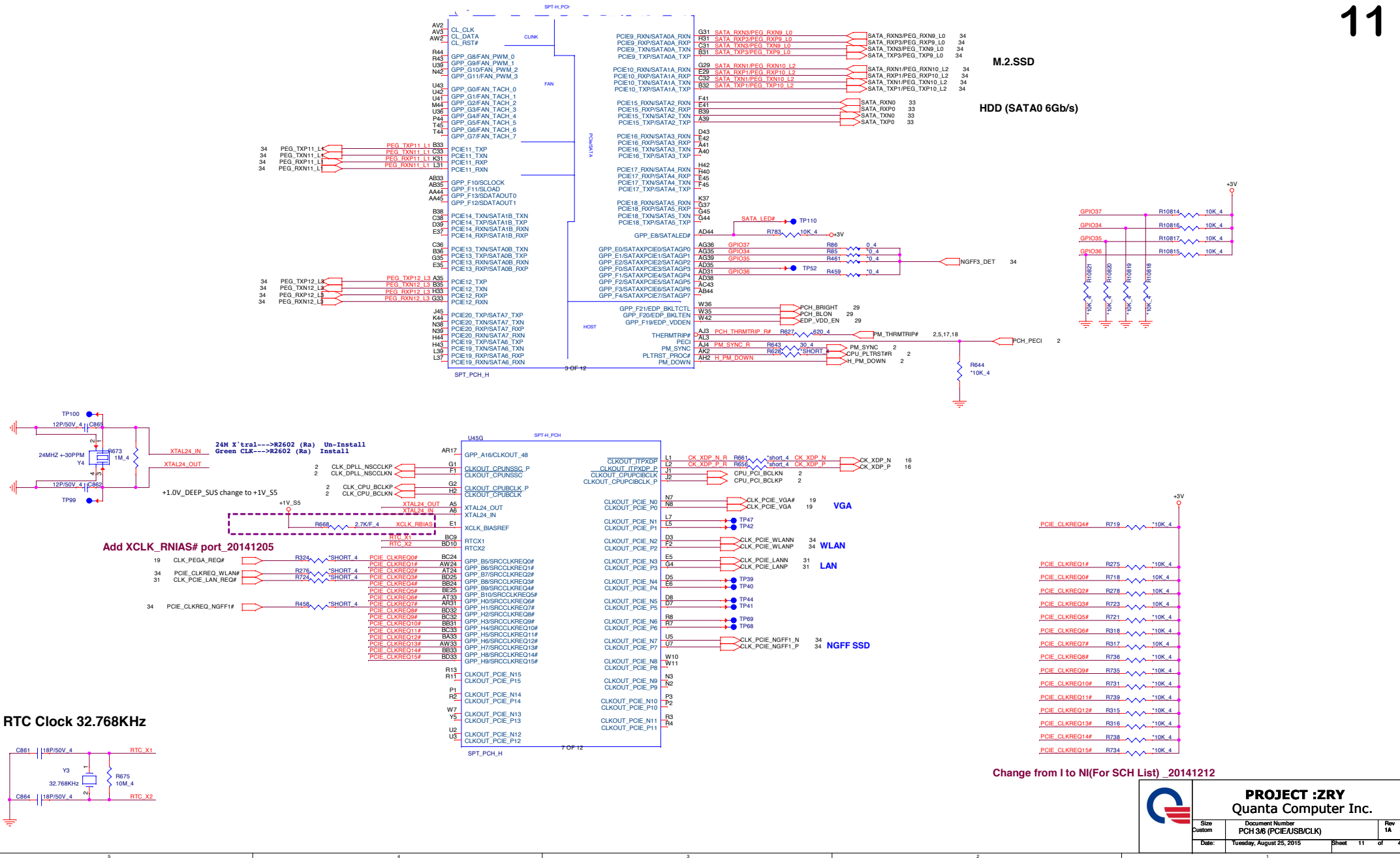


10,12,13,14,16,17 +3V_DEEP_SUS


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Quanta Computer Inc.

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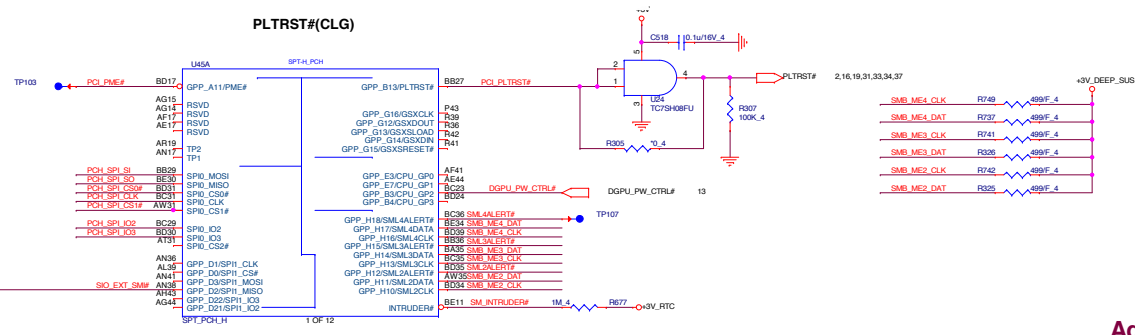


Change from I to NI(For SCH List) 20141212

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	Quanta Computer Inc.		
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PLTRST# Buffer

PLTRST#(CLG)

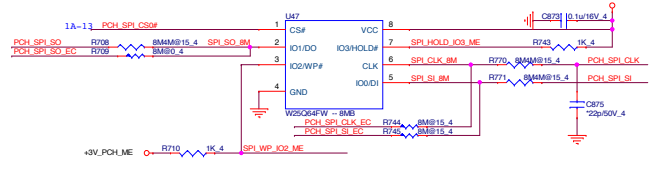


SP@ socket P/N: DFHS08FS023 only for A-TEST

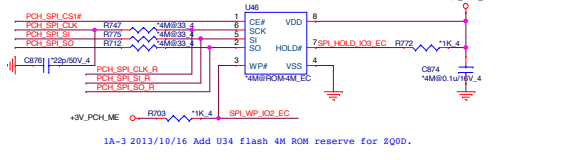
SPI ROM	Vender	Size	Quanta P/N	Vender P/N
Skylake 3.3V	WND	8M	AKE3EFPN007	W25Q64FVSSIQ
	GGD	8M	AKE2EZN0000	GD25B64CSIQR
	EON	8M	AKE3EZN0001	EN25QH64-104HIP
Skylake 3.3V	WND	16M	AKE3DZN001	W25Q128FVSIQ

PCH SPI ROM(8M+4M)

15ohm CS01502JB12
33ohm CS03302JB29

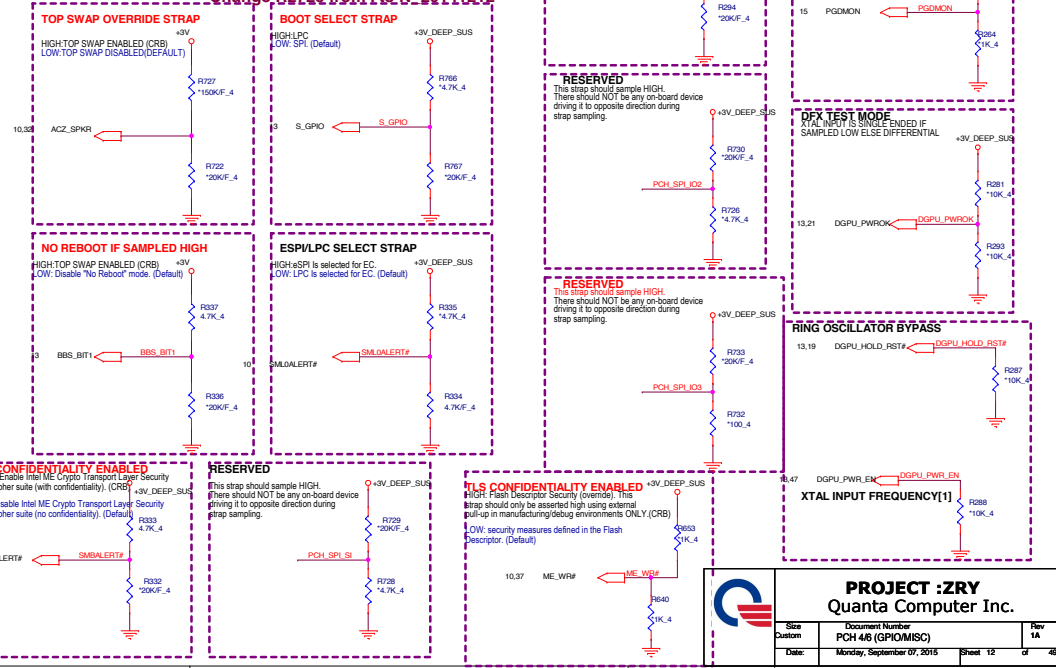


3.3K is original and for no support fast read function



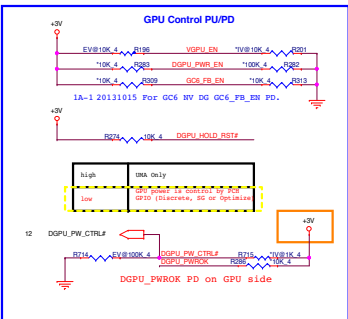
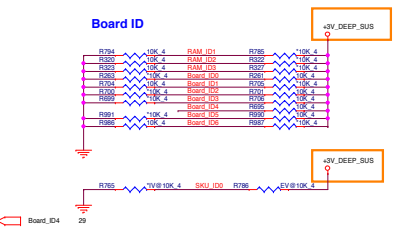
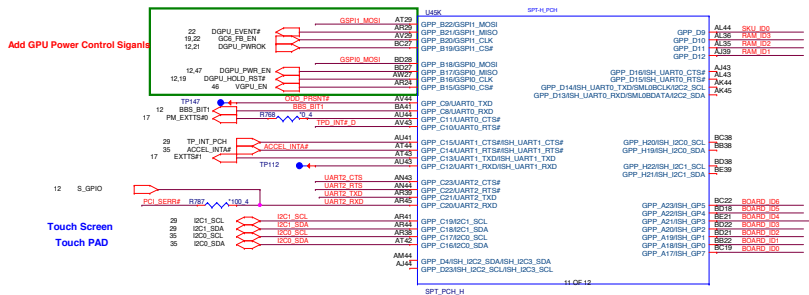
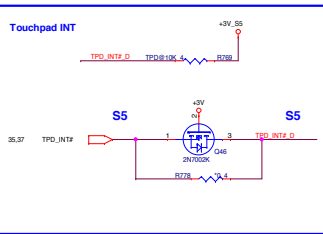
1A-3 2013/10/16 Add U34 flash 4M ROM reserve for ZQ0D.

Add PCH Strap Pin_20141203
Change B2725 from 1to N_20141212

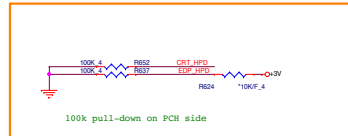
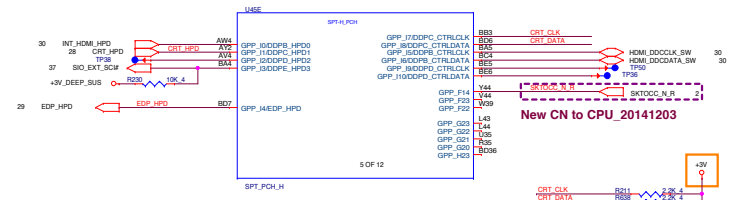


PROJECT :ZRY
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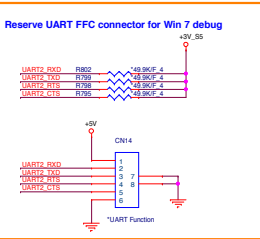
waiting for define!



	Low	High
BOARD_ID0	VRAM 2GB	VRAM 4GB
BOARD_ID1	Reserved (Default)	Reserve
BOARD_ID2	No G-sensor	G-sensor
BOARD_ID3	TPM	No TPM
BOARD_ID4	No touch panel	touch panel

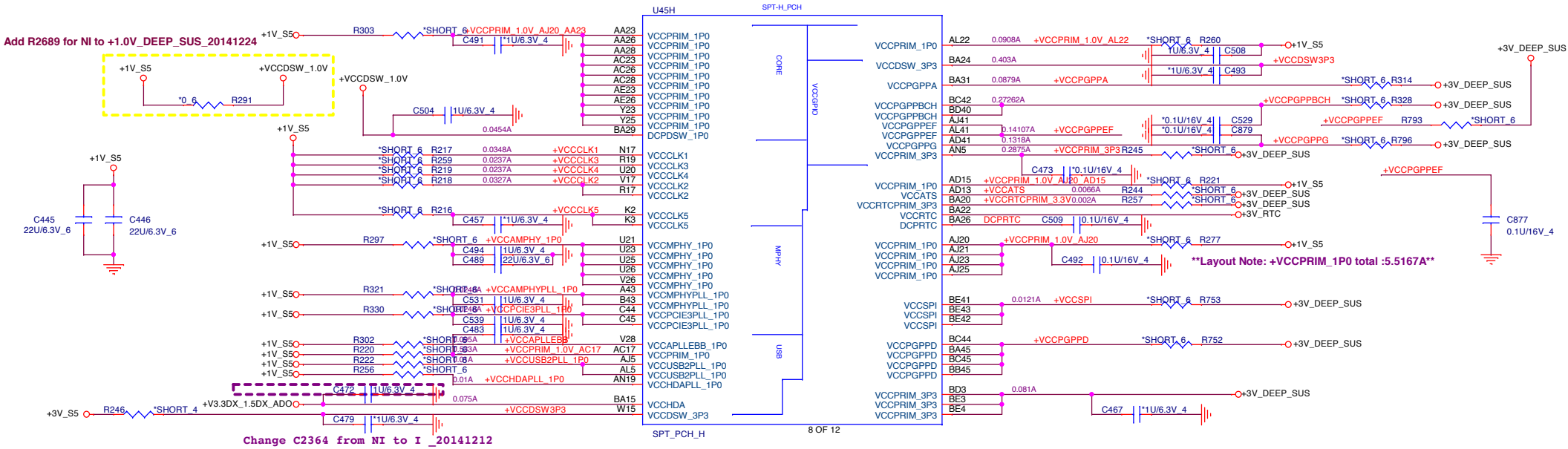
	Low	High
BOARD_ID5	Reserved (Before C1)	Reserved (After C2)
BOARD_ID6	Reserved (Default)	Reserve

	SRV_ID0	VRM M/N Signal	Setup Menu
UMA Only	0	UMA	Hidden
UMA boot	1	UMA	Hidden

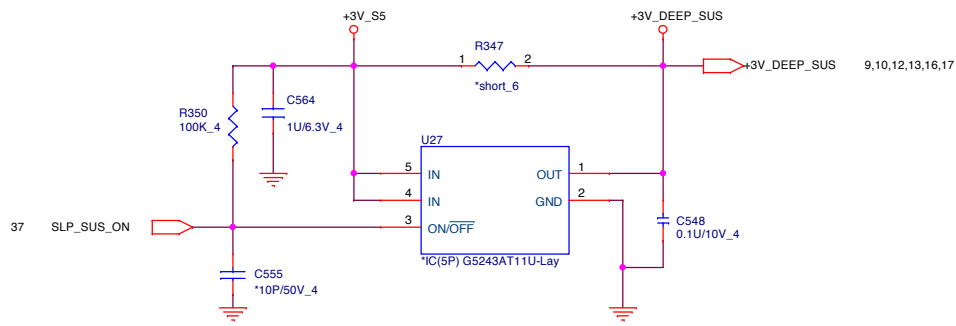


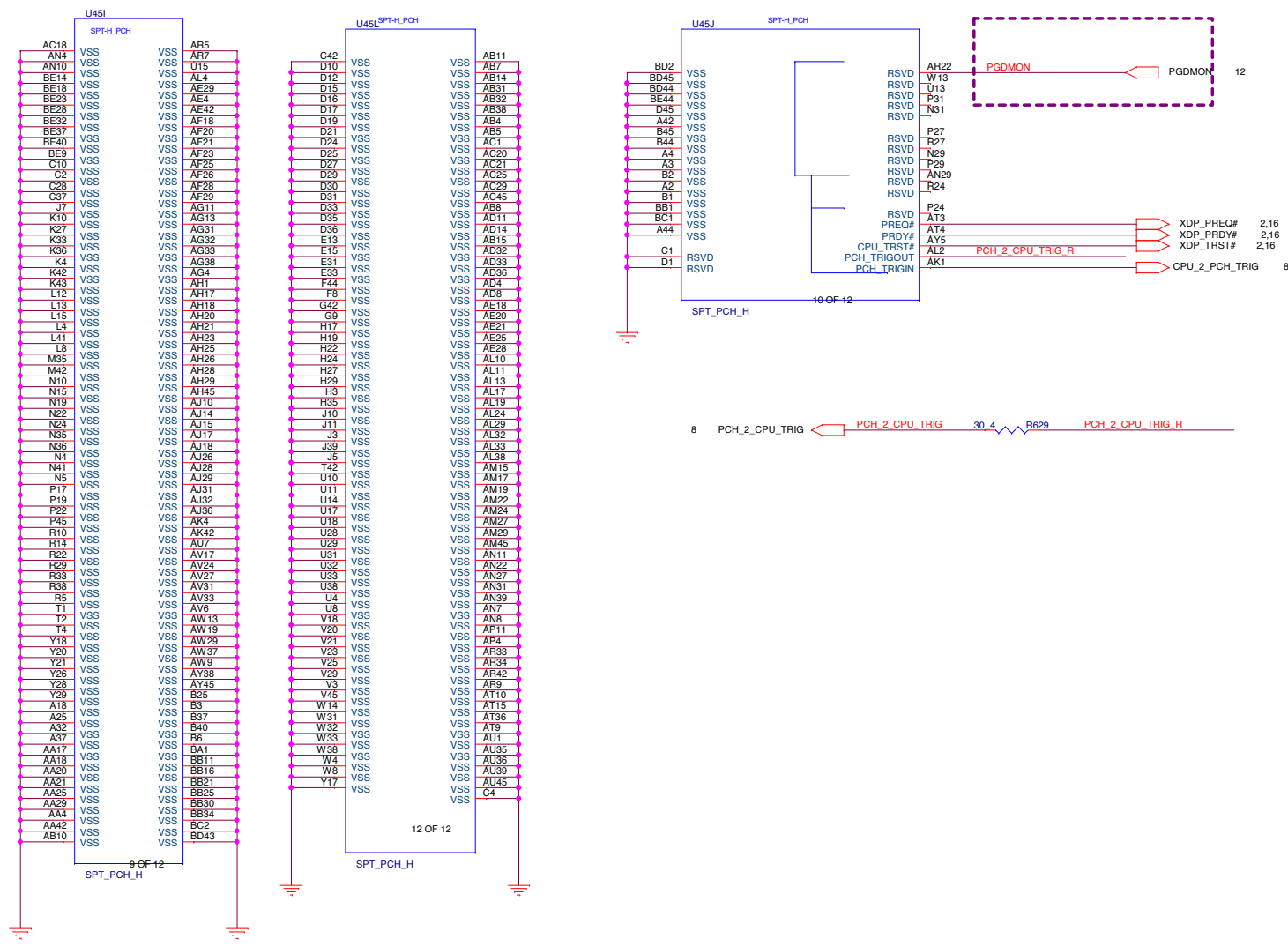
Skylake-H Strapping Table

Pin Name	Strap description	Sampled	Configuration	note
GPP_B14 (SPKR)	Top-Block Swap override	PCH_PWROK	0 = *Disable Top Swap (IPD 20K) 1 = Enable Top Swap Mode	
GPP_B18 (GSPD_MOSI)	No reboot	PCH_PWROK	0 = *Disable No Reboot (IPD 20K) 1 = Enable No Reboot Mode	+3V - R225 ~ 10K_4 - GSPD_MOSI
GPP_C2 (SMBALERT#)	TLS Confidentiality	RSMRST#	0 = *Disable Intel ME Crypt to TLS (IPD 20K) 1 = Enable Intel ME Crypt to TLS	
GPP_B22 (GSPD_MOSI)	Boot BIOS Strap Bit (BBS)	PCH_PWROK	0 = *SPI (IPD 20K) 1 = LPC	+3V - R217 ~ 10K_4 - GSPD_MOSI
GPP_C5 (SMLDUALERT#)	eSPI or LPC	RSMRST#	0 = *LPC is selected for EC (IPD 20K) 1 = eSPI selected for EC	
SPI0_MOSI	Reserved	RSMRST#	(IPU 15 ~ 40K)	
SPI0_MISO	Reserved	RSMRST#	(IPU 15 ~ 40K)	
GPP_B23 (SML1ALERT# /PCHHOT#)	Reserved	RSMRST#	(IPD 20K)	
SPI0_IO2	Reserved	RSMRST#	(IPU 15 ~ 40K)	
SPI0_IO3	Reserved	RSMRST#	(IPU 15 ~ 40K)	
HDA_SDO / I2S_TXD0	Flash Descriptor Security Override / Intel ME Debug Mode	PCH_PWROK	0 = *Enable security in the Flash Description (IPD 20K) 1 = Disable Flash Descriptor Security (Override)	
GPP_E19 (DDPB_CTRLDATA)	Display Port B Detected	PCH_PWROK	0 = *Port B is not detected (IPD 20K) 1 =Port B is detected	
GPP_E21 (DDPC_CTRLDATA)	Display Port C Detected	PCH_PWROK	0 = *Port C is not detected (IPD 20K) 1 =Port C is detected	




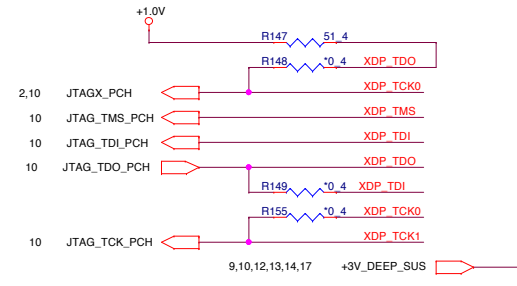
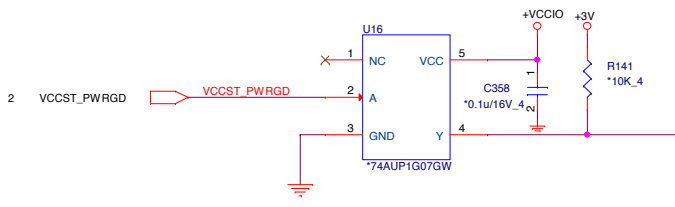
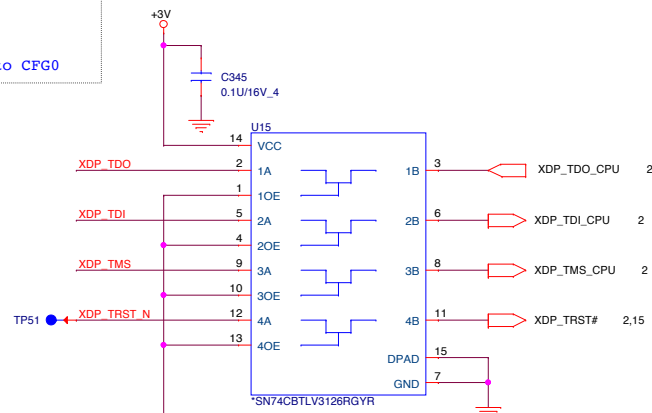
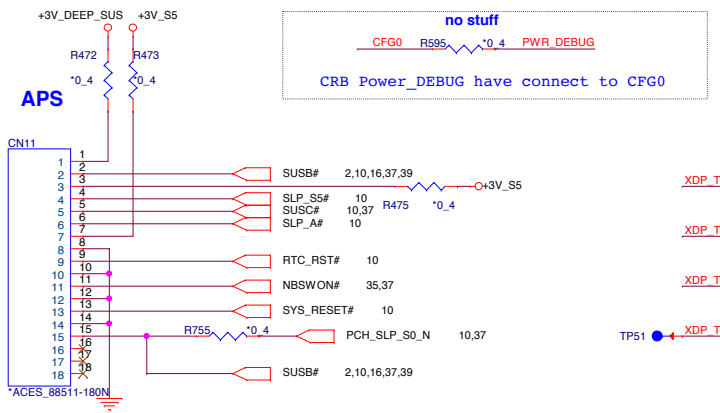
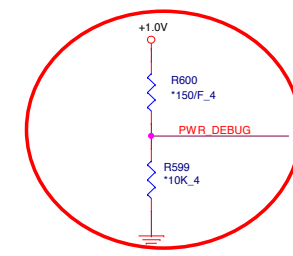
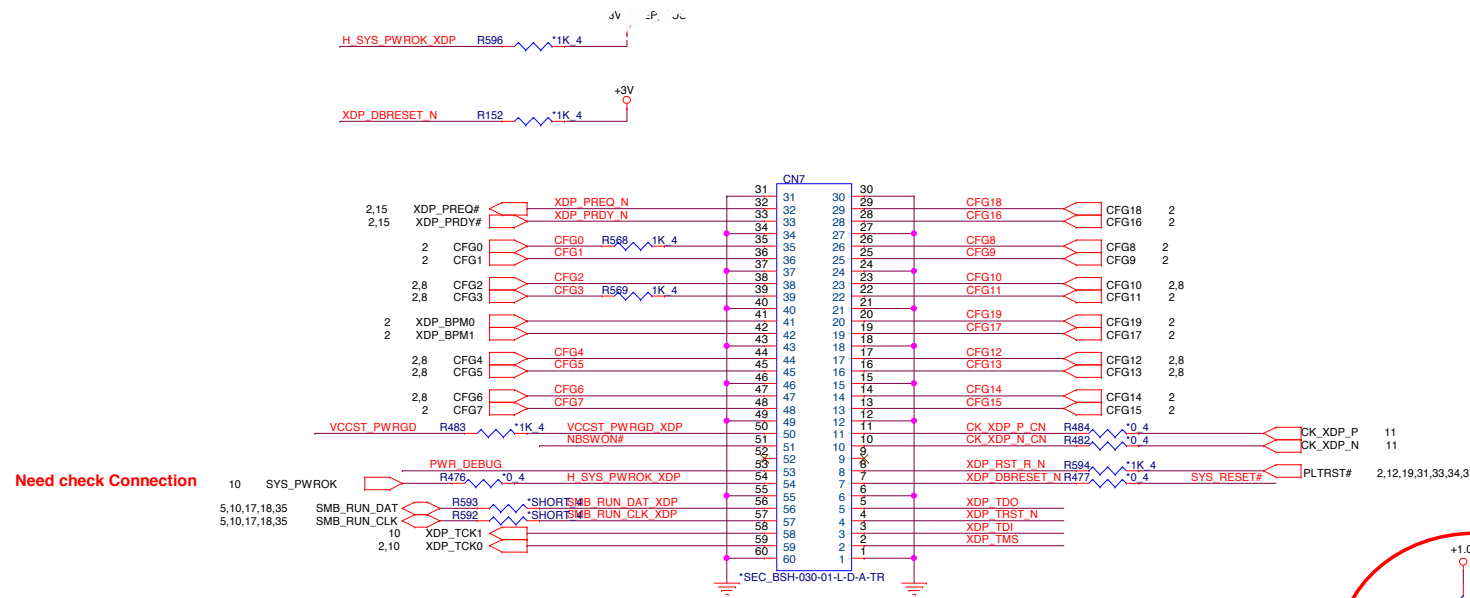
for DS3

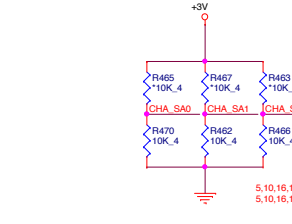
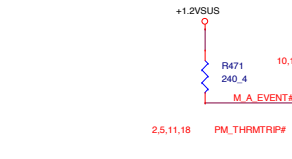
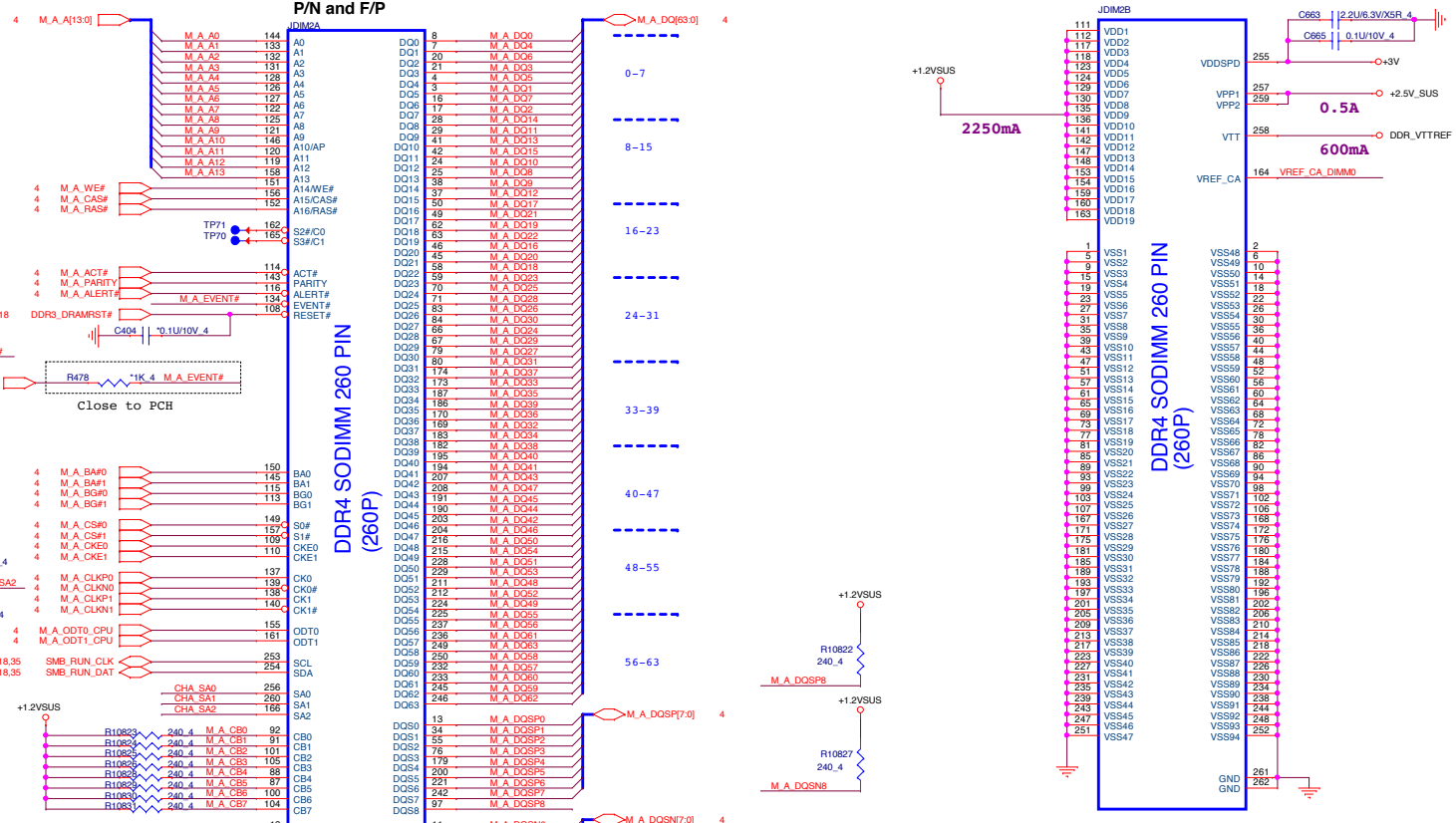




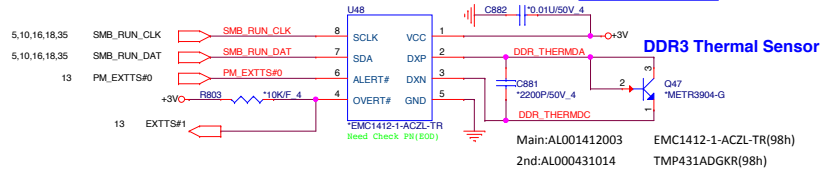
5,10,29,31,32,34,35,37,38,39,46,47 +3VPCU

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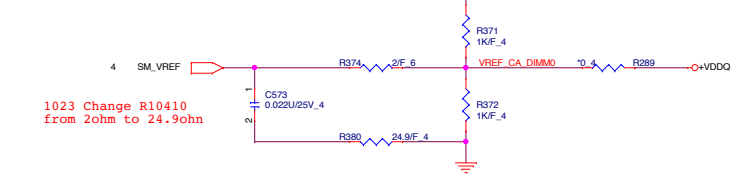




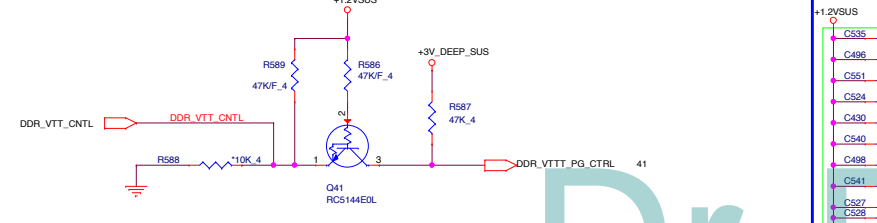
Local Thermal Sensor



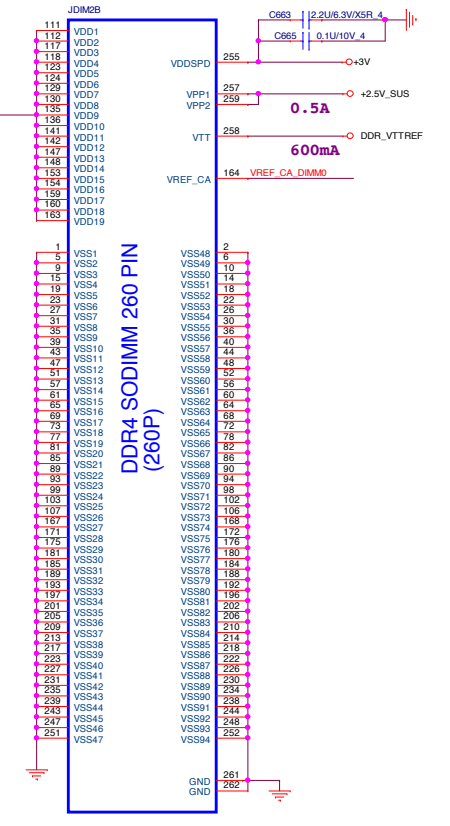
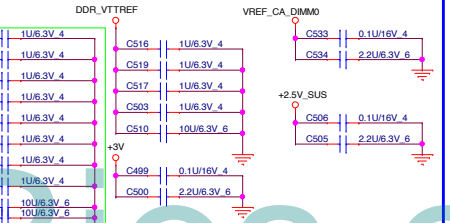
VREF DQ0 M1 Solution



Co-lay for ODT

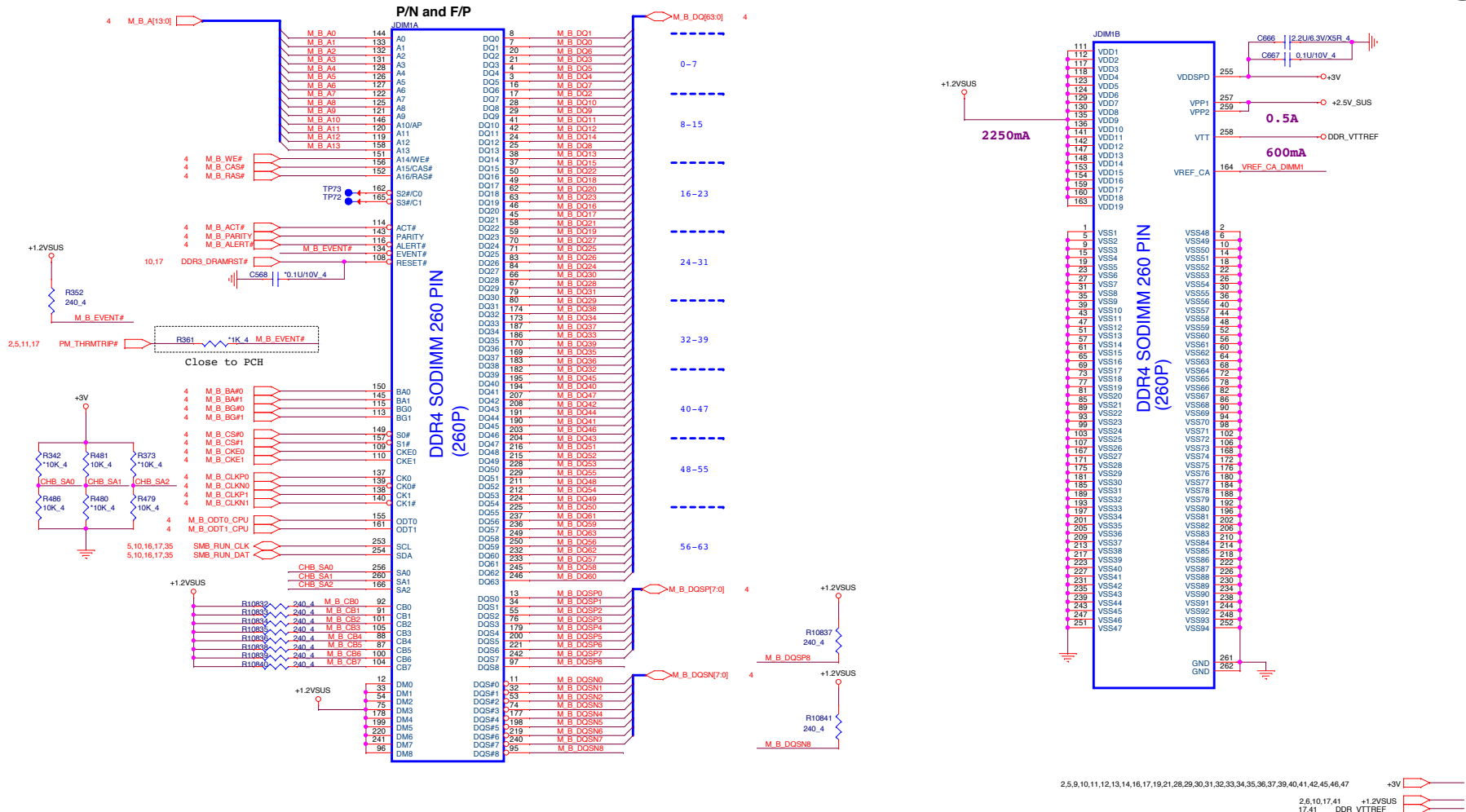


Place these Caps near So-Dimm1.

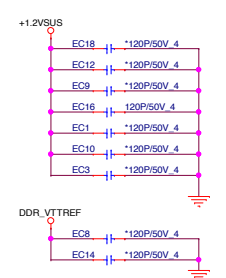


PROJECT :ZRY
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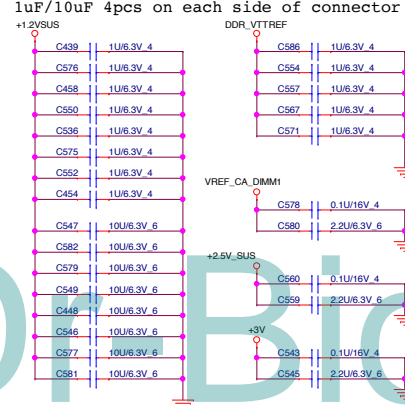
Size Custom	Document Number 18 -- DDR3 DIMM1-RV5(8.0H)	Rev 1A
Date: Tuesday, August 25, 2015	Sheet 17	of 49



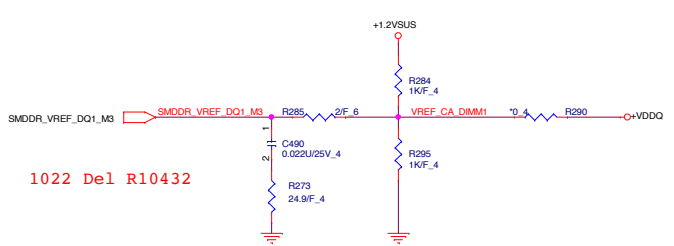
For EMI RESERVE



Place these Caps near So-Dimm0.

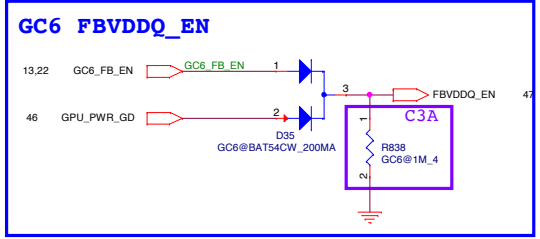
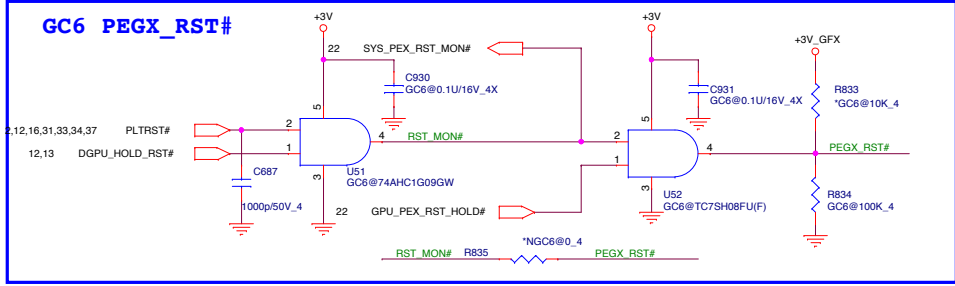
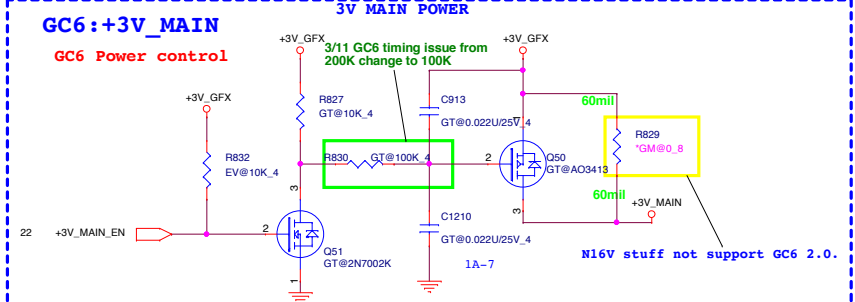
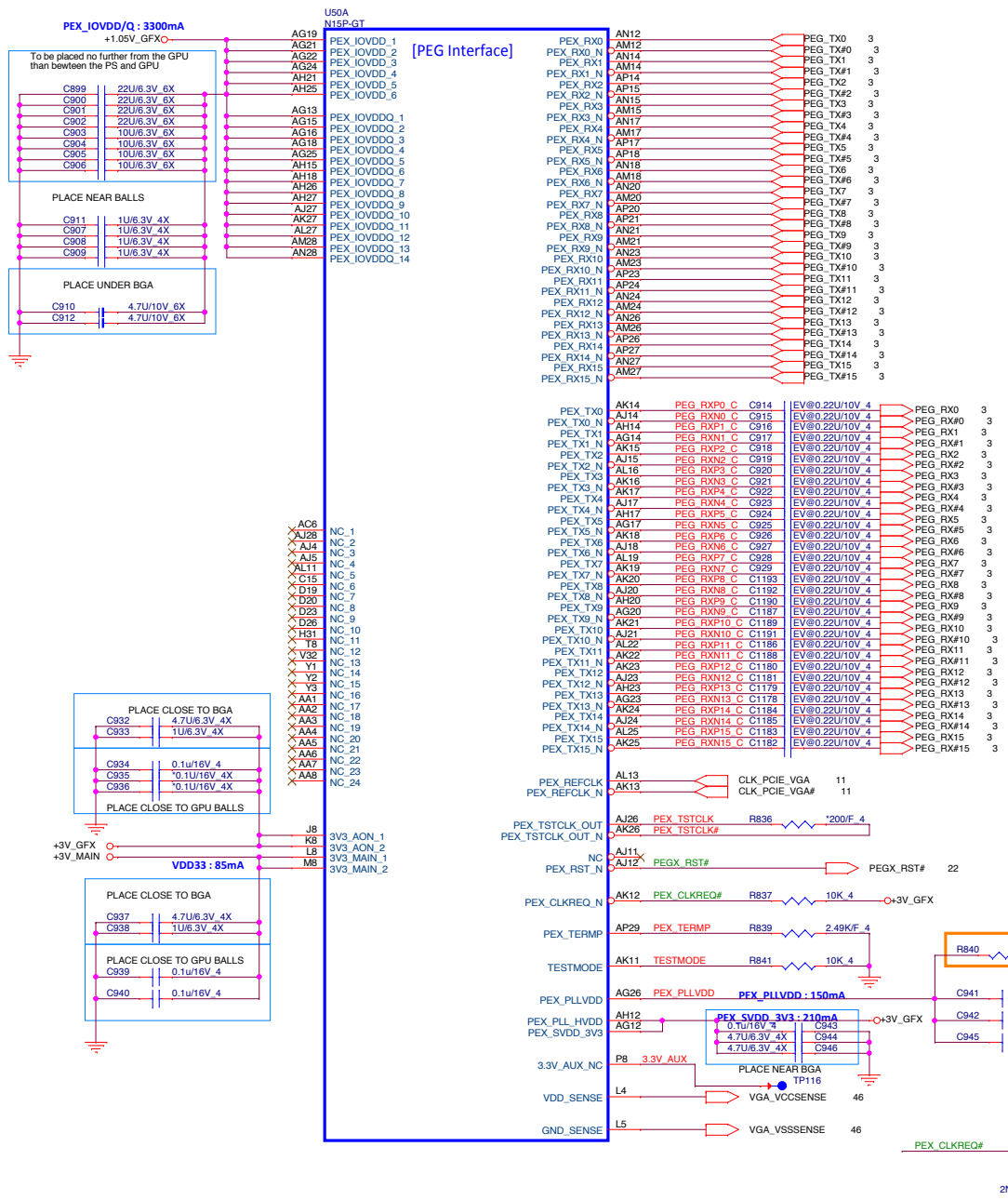


VREF DQ1 M1 Solution



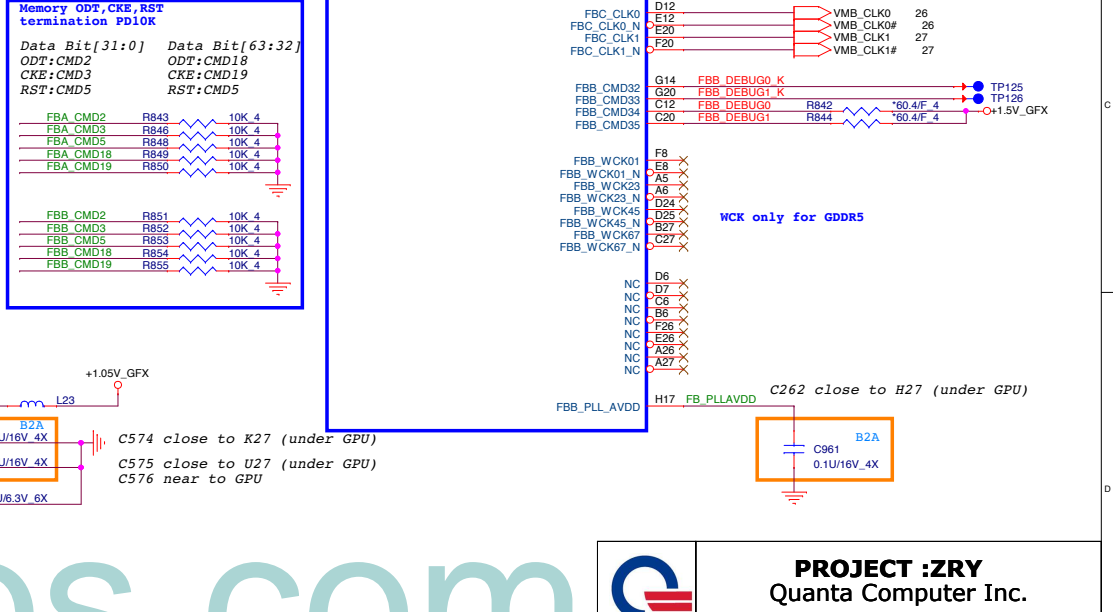
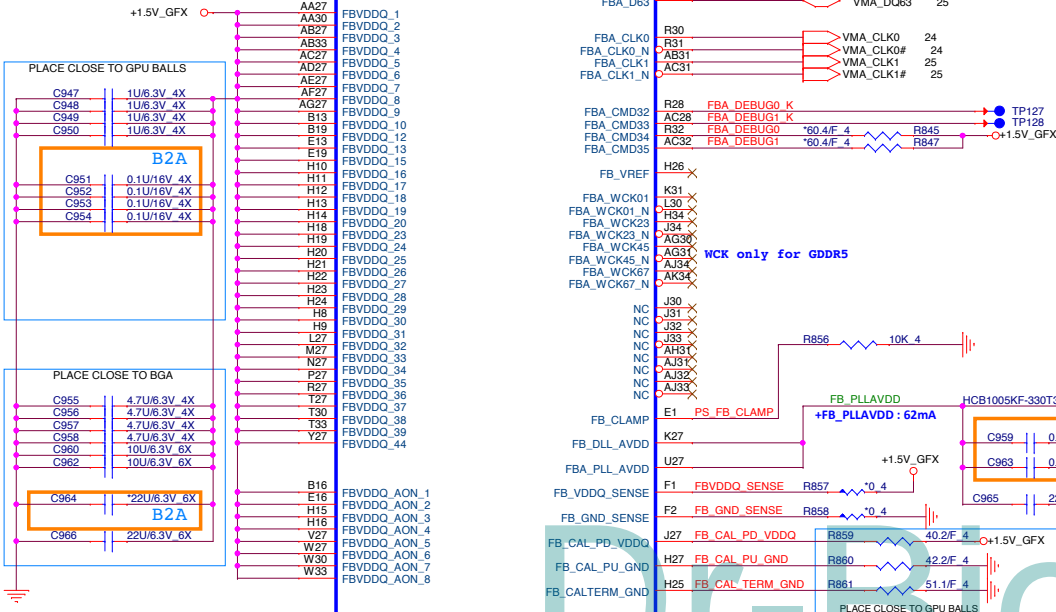
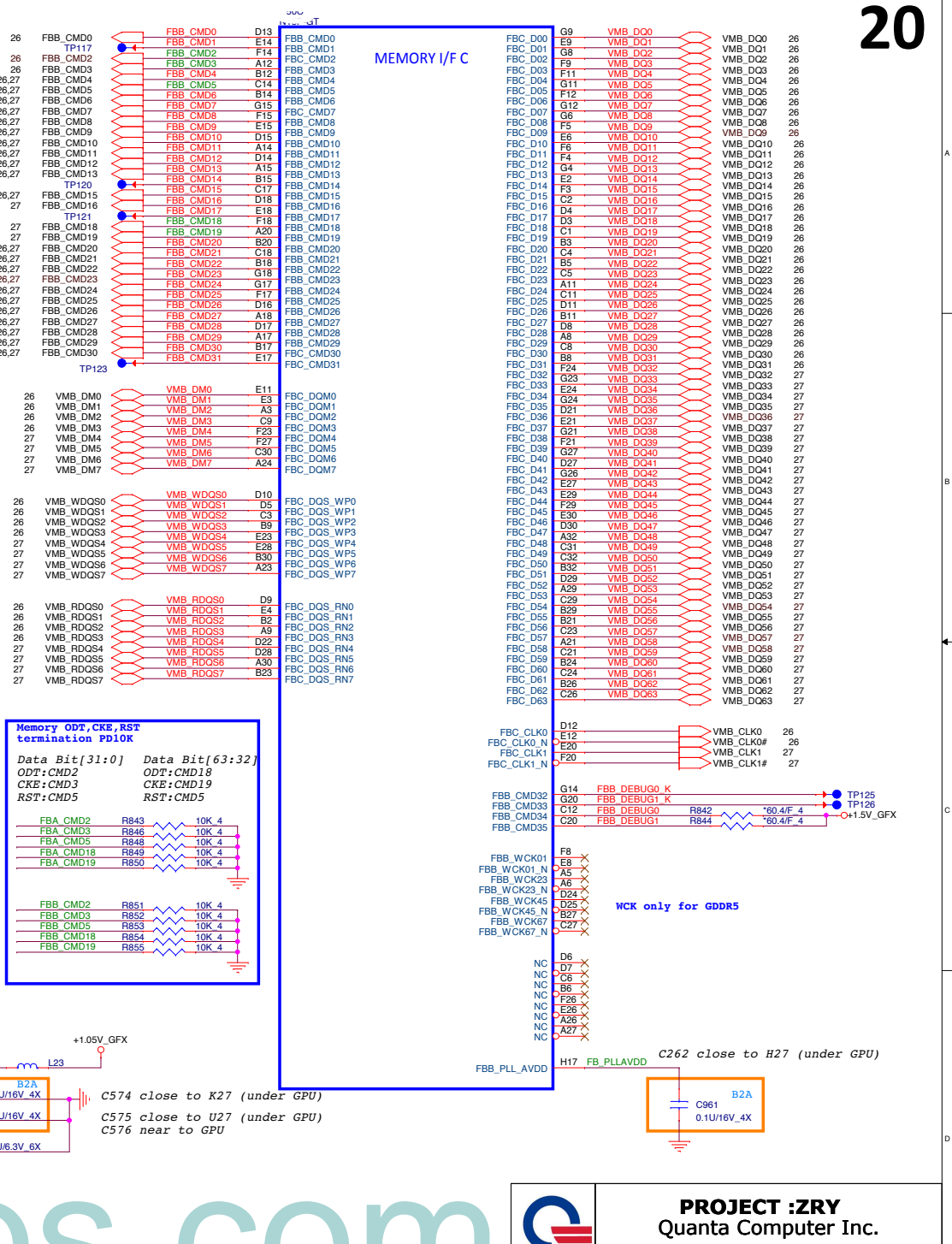
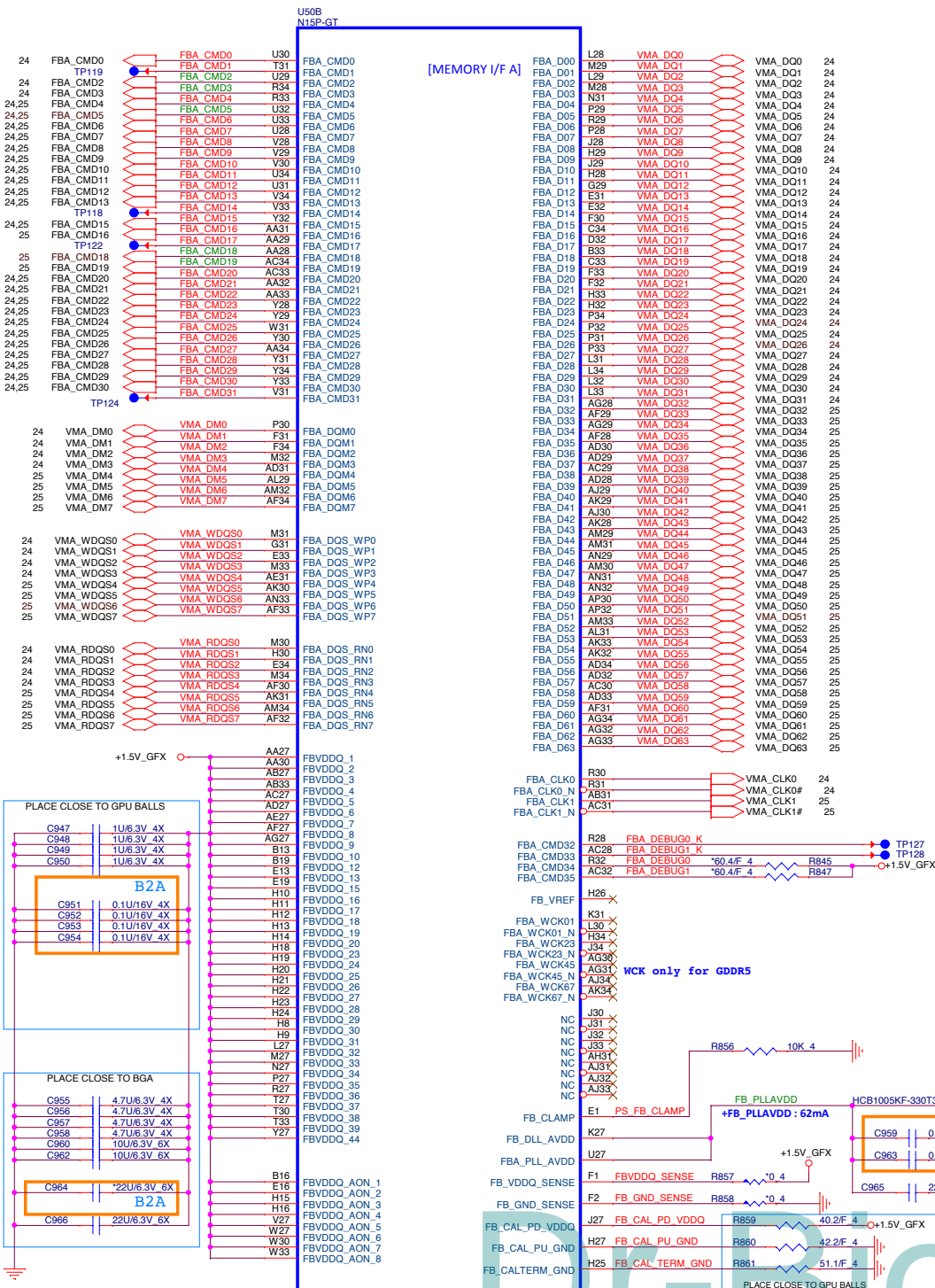
PROJECT :ZRY
Quanta Computer Inc.

Size Custom	Document Number 17 - DDR3 DIMM0-STD(4.0H)	Rev 1A
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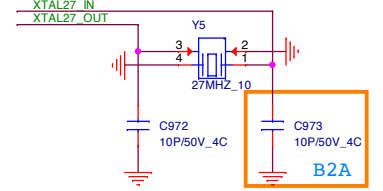
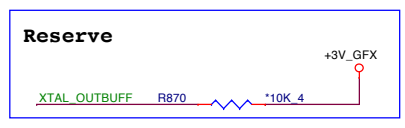
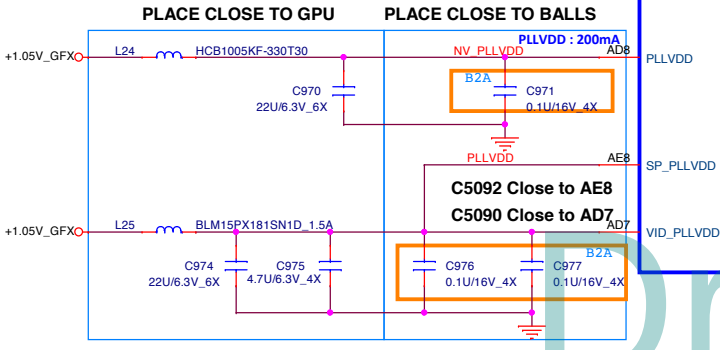
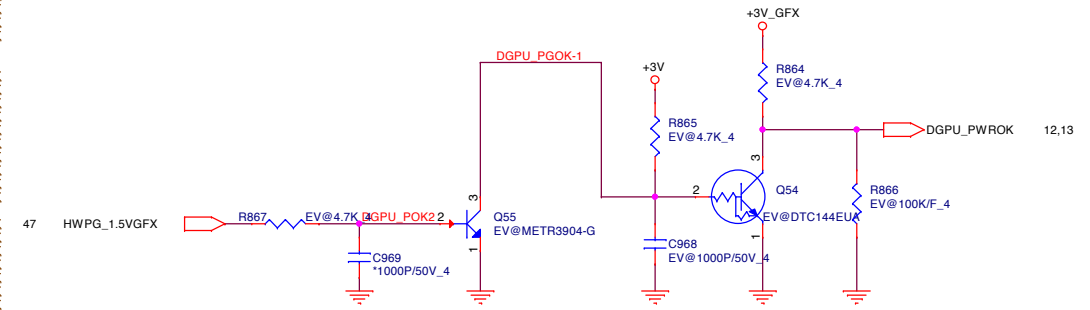
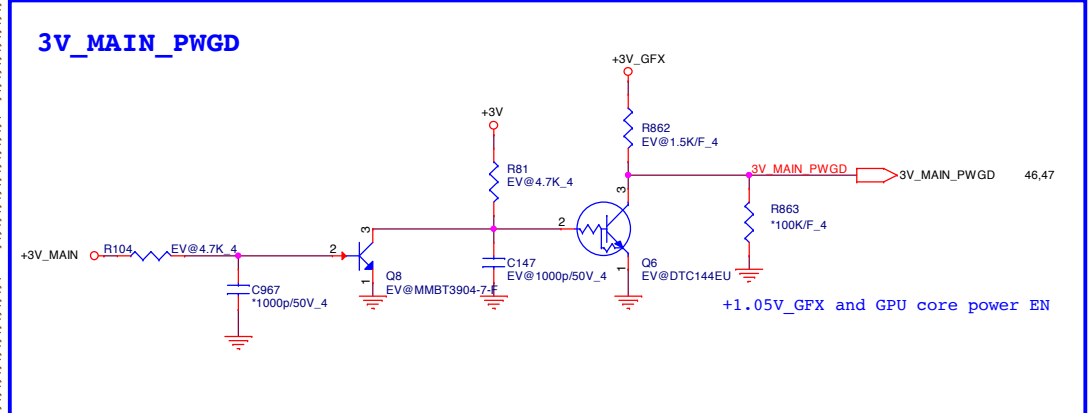


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Size	Document Number	Rev
	N16P-GT - 1/5 (PCIE)	1A
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U50D N15P-GT			
× AH8	IFPAB_PLLVDD	[IFPA/B_LVDS]	IFPA_TXC AM6 IFPA_TXC_N AN6 IFPA_TXD0 AN3 IFPA_TXD0_N AN5 IFPA_TXD1 AN5 IFPA_TXD1_N AN6 IFPA_TXD2 AJ6 IFPA_TXD2_N AH6 IFPA_TXD3 AH6 IFPA_TXD3_N
× AG8	IFPA_IOVDD		
× AG9	IFPB_IOVDD		
× AJ8	IFPAB_RSET		
			IFPB_TXC AH9 IFPB_TXC_N AP6 IFPB_TXD4 AP6 IFPB_TXD4_N AM7 IFPB_TXD5 AL7 IFPB_TXD5_N AN8 IFPB_TXD6 AM8 IFPB_TXD6_N AK8 IFPB_TXD7 AL8 IFPB_TXD7_N
× AF7	IFPC_PLLVDD	[IFPC/D_TMSD]	IFPC_AUX_I2CW_SCL AG3 IFPC_AUX_I2CW_SDA_N AG2 IFPC_L0 AK1 IFPC_L0_N AJ1 IFPC_L1 AJ3 IFPC_L1_N AJ2 IFPC_L2 AH3 IFPC_L2_N AH4 IFPC_L3 AG5 IFPC_L3_N AG4
× AG7	IFPD_PLLVDD		
× AF6	IFPC_IOVDD		
× AG6	IFPD_IOVDD		
× AF8	IFPC_RSET		
× AN2	NC		
			IFPD_AUX_I2CX_SCL AK3 IFPD_AUX_I2CX_SDA_N AK2 IFPD_L0 AM1 IFPD_L0_N AM2 IFPD_L1 AM3 IFPD_L1_N AM4 IFPD_L2 AL3 IFPD_L2_N AL4 IFPD_L3 AK4 IFPD_L3_N AK5
× AB8	IFPEF_PLLVDD	[IFPE/F_DP]	IFPE_AUX_I2CY_SCL AB3 IFPE_AUX_I2CY_SDA_N AB4 IFPE_L0 AD2 IFPE_L0_N AD3 IFPE_L1 AD1 IFPE_L1_N AC1 IFPE_L2 AC2 IFPE_L2_N AC3 IFPE_L3 AC4 IFPE_L3_N AC5
× AC7	IFPE_IOVDD		
× AC8	IFPF_IOVDD		
× AD6	IFPEF_RSET		
			IFPF_AUX_I2CZ_SCL AF3 IFPF_AUX_I2CZ_SDA_N AF2 IFPF_L0 AE3 IFPF_L0_N AF4 IFPF_L1 AF5 IFPF_L1_N AD4 IFPF_L2 AD5 IFPF_L2_N AG1 IFPF_L3 AF1 IFPF_L3_N
× AG10	DACA_VDD	[DACA/B_CRT]	DACA_RED AK9 DACA_GREEN AL10 DACA_BLUE AL9
× AP9	DACA_VREF		
× AP8	DACA_RSET		DACA_HSYNC AM9 DACA_VSYNC AN9
			I2CA_SCL R4 I2CA_SDA R5 I2CA_SCL 1.8K/F_4 R868 I2CA_SDA 1.8K/F_4 R869
			H3 XTAL27_IN H2 XTAL27_OUT J4 XTAL_OUTBUFF R871 H1 XTAL_SIN R872

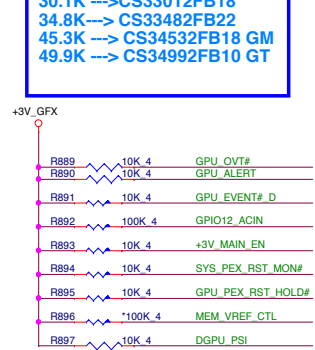


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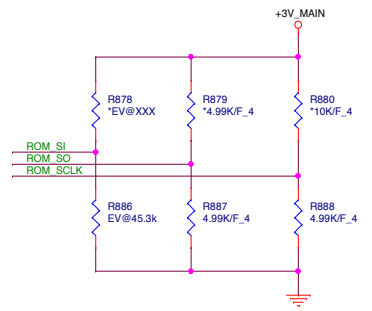
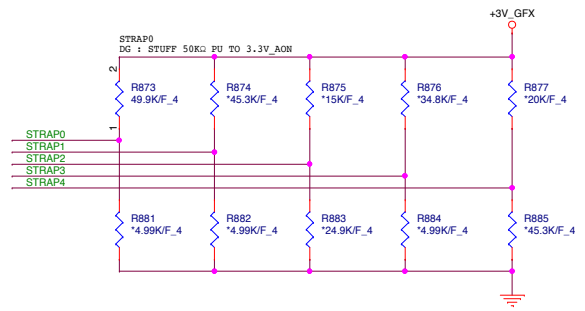
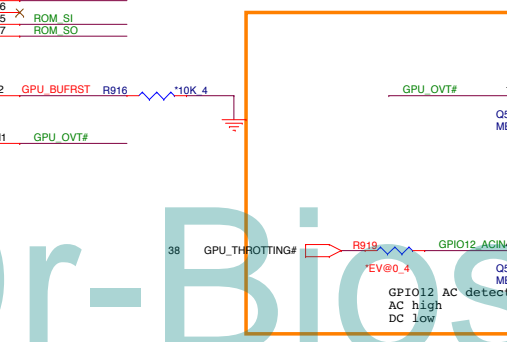
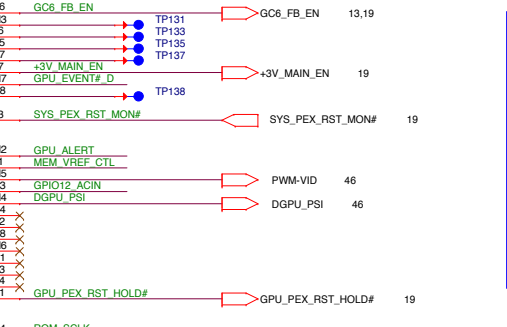
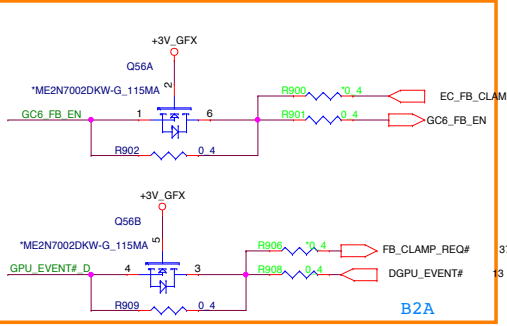
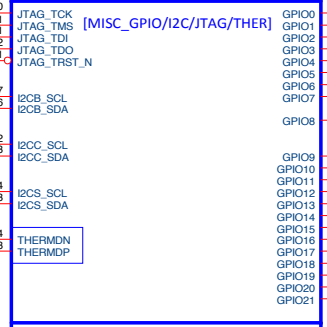
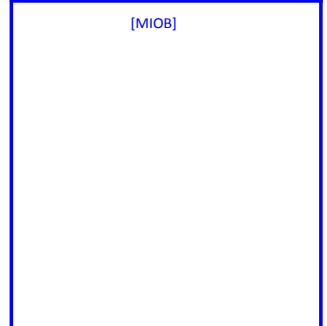
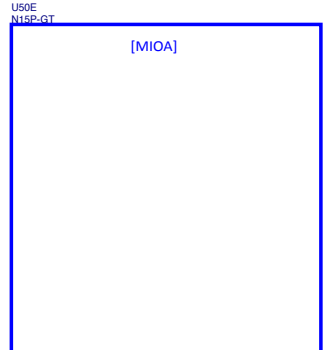
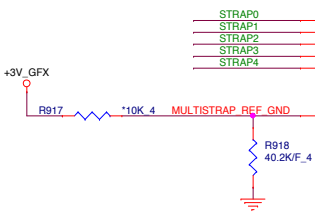
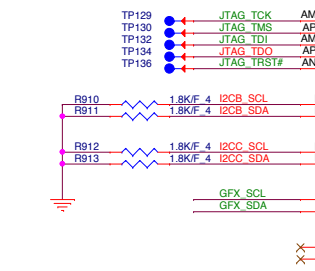
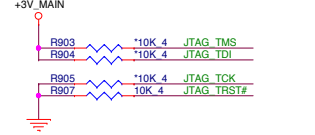
PROJECT :ZRY Quanta Computer Inc.		
Size	Document Number	Rev
	N15P-GT - 3/5 (Display)	1A
Date:	Tuesday, August 25, 2015	Sheet 21 of 49

- Resistor P/N
 4.99K -> CS24992FB26
 10K -> CS31002FB26
 15K -> CS31502FB24
 20K -> CS32002FB29
 24.9K -> CS32492FB16
 30.1K -> CS33012FB18
 34.8K -> CS33482FB22
 45.3K -> CS34532FB18 GM
 49.9K -> CS34992FB10 GT

Package	DevID	
N16P-GT-A2	GB4b-128	0x139A
N16V-GM-B1	GB2-64	0x1299
N16S-GM-S-A2	GB2b-64	0x1346



Reserve PU/PD for Debug



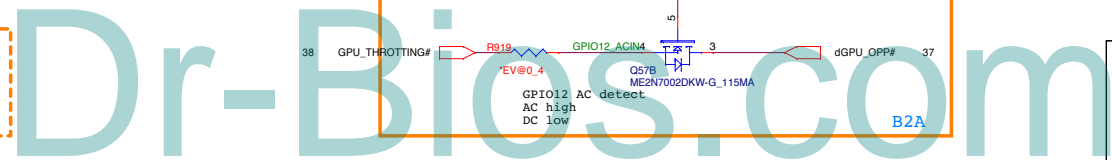
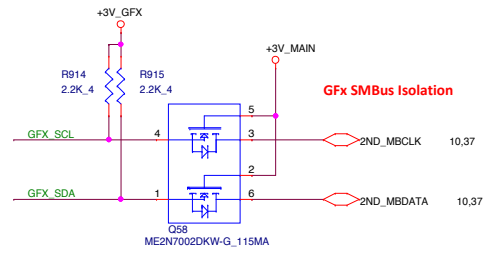
	PU +3V_MAIN	PD
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

Mult-level mode strapping:
 For N16P-GT-A2 :
 R886=40.2k PD
 1.ROM_SCLK =4.99K PD
 2.ROM_SO = 4.99K PD
 3.ROM_SI= Memory strap setting
 4.STRAP0 = 49.9k PU
 5.Strap4~1 = Reserve Pull up and Pull down

N16P-GT-A2 VRAM Configuration Table:

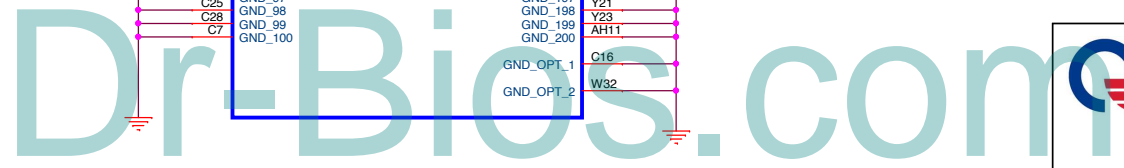
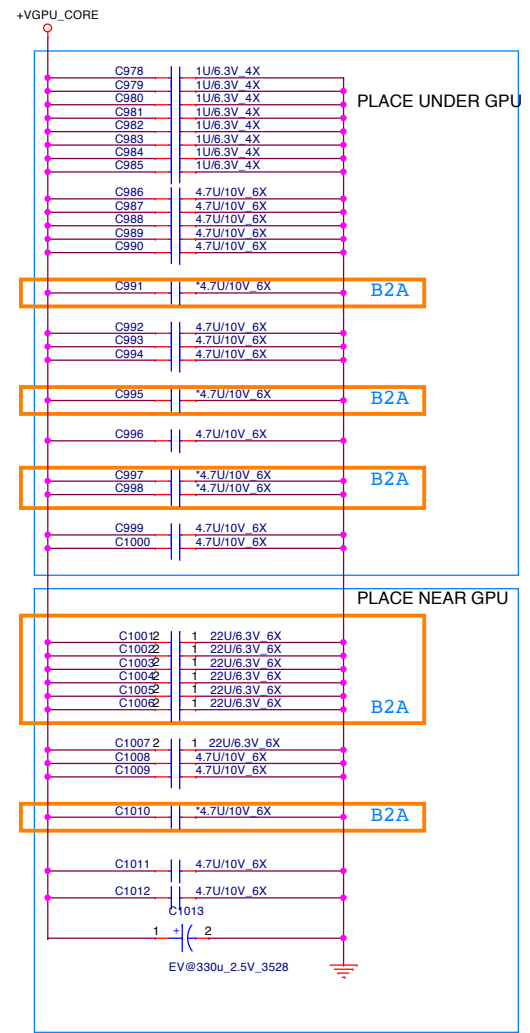
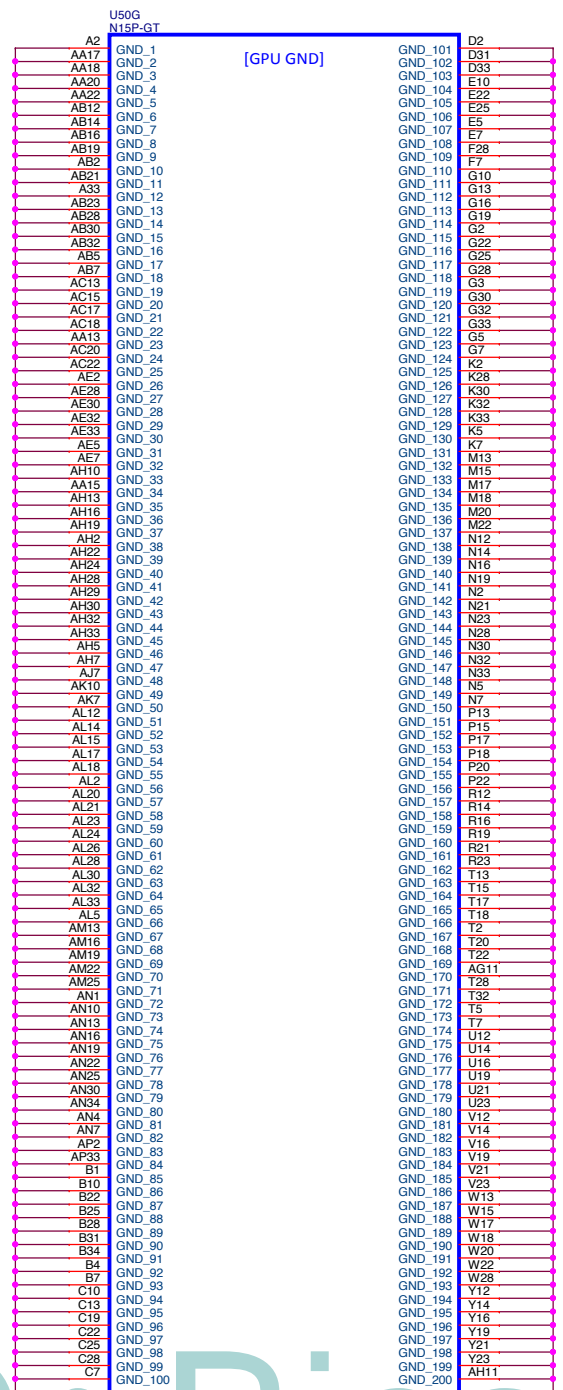
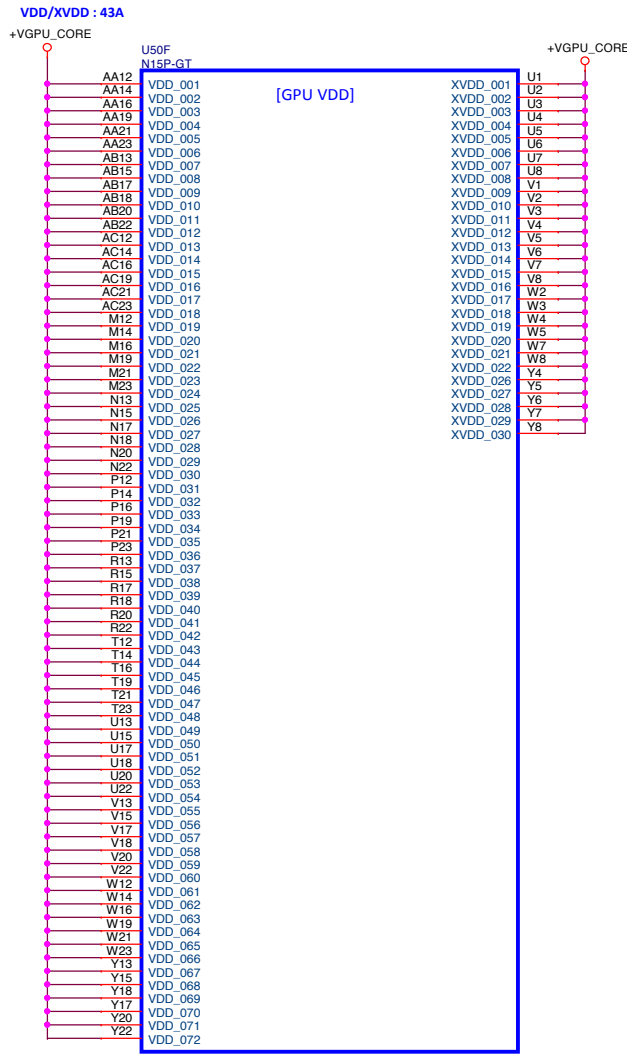
	ROM_SI	DESCRIPTION	Vendor	Vendor P/N	QCI P/N	ROM_SI
2Gb	0110 (0x6)	DDR3 128MBx16,1000MHz	HYNIX	H5TC2G63PFR-11C		34.8K Pull down
	0111 (0x7)	DDR3 128MBx16,1000MHz	MICRON	MT41J128M16JT-093G:K		45.3K Pull down
	1000 (0x8)	DDR3 128MBx16,1000MHz	SAMSUNG	K4W2G1646Q-BC1A		4.99K Pull UP
4Gb	0101 (0x5)	DDR3 256MBx16,1000MHz	HYNIX	H5TC4G63CFR-11C		30.1K Pull down
	0001 (0x1)	DDR3 256MBx16,1000MHz	MICRON	MT41J256M16HA-093G:E		10K Pull down
	0010 (0x2)	DDR3 256MBx16,1000MHz	SAMSUNG	K4W4G1646D-BC1A		15K Pull down


N16P-GT-A2 (GB4b-128)					
	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	0001
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE	0001
STRAP0	Keep footprint to PU to 3V3_AON and PD to GND [Stuff 49.9K PU]				0001
STRAP1					
STRAP2	Keep footprint to PU to 3V3_AON and PD to GND [Do Not Stuff]				
STRAP3					
STRAP4					

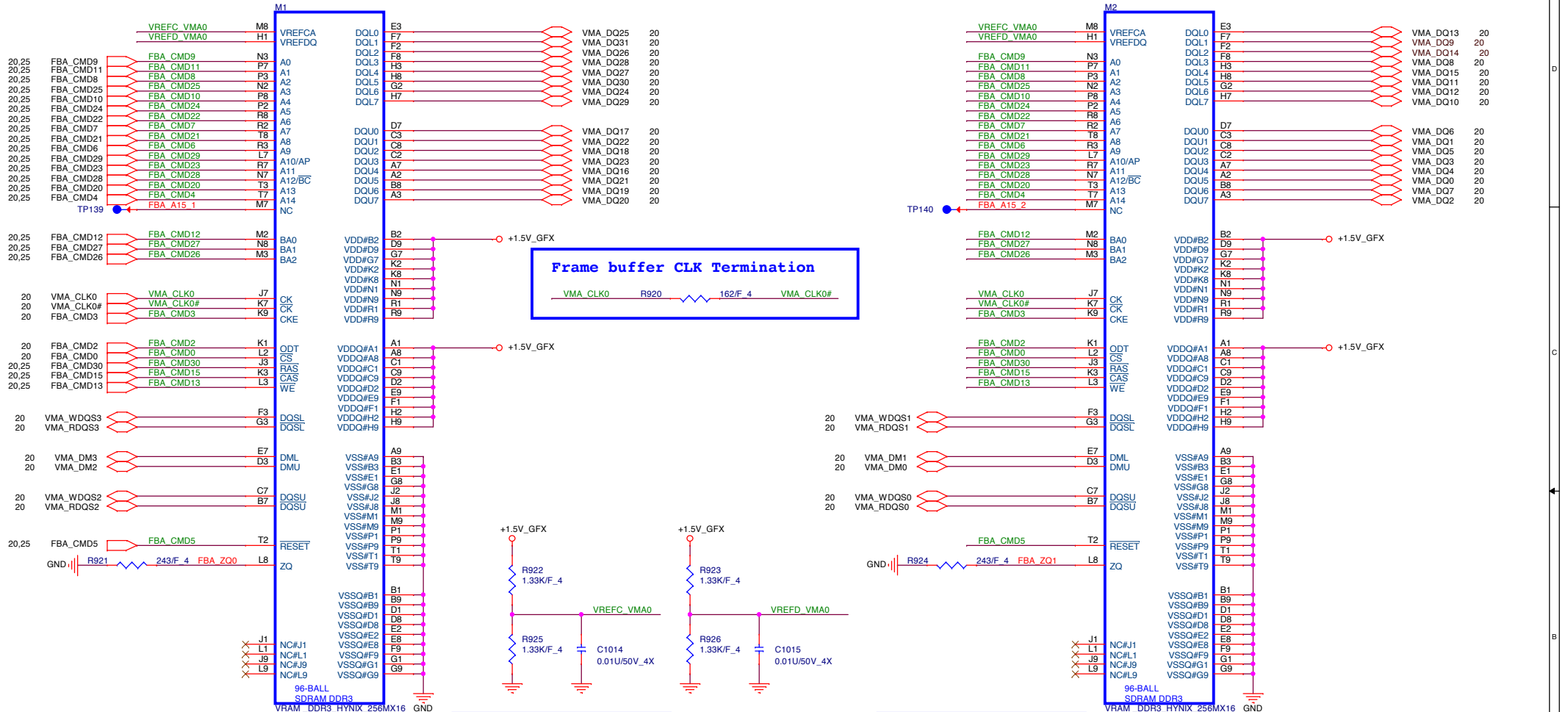


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	N16P-GT - 4/5 (MISC)	1A
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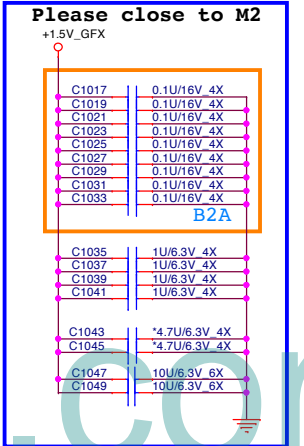
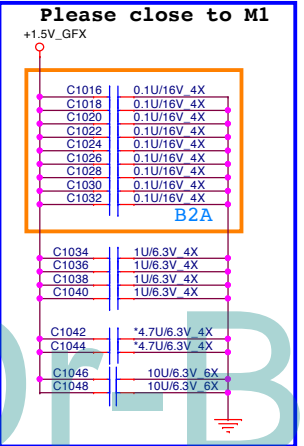


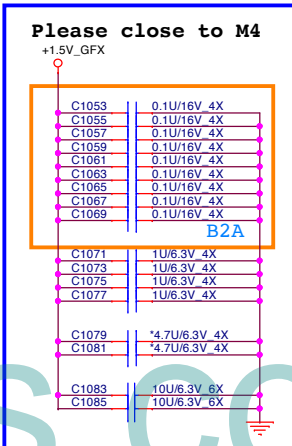
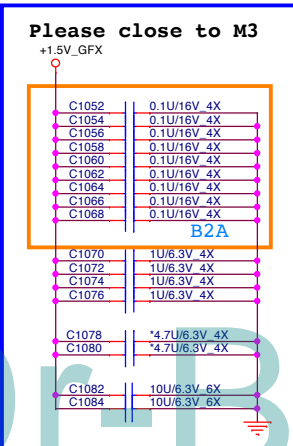
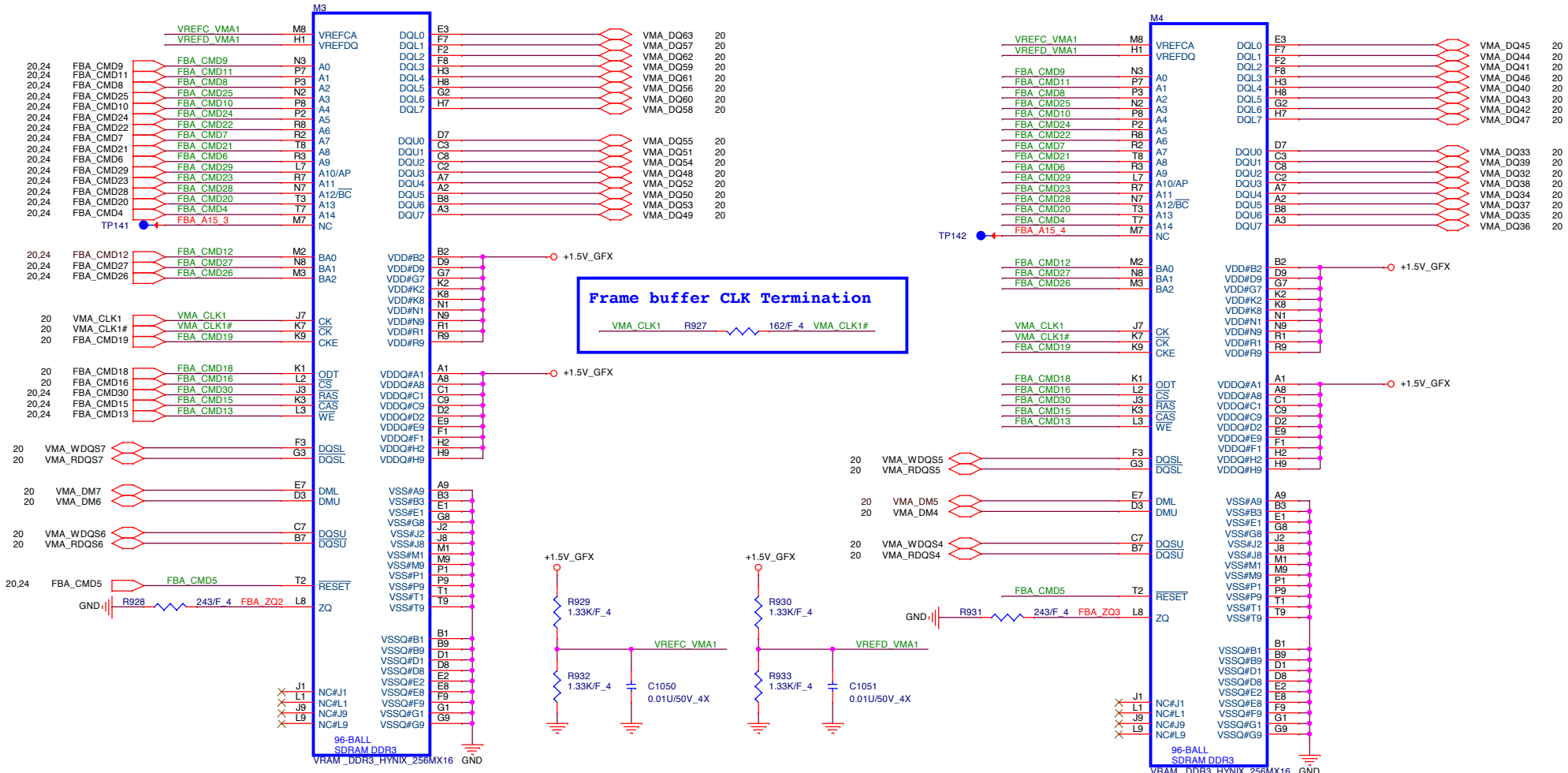
			PROJECT :ZRY	
			Quanta Computer Inc.	
Size	Document Number			Rev
	N16P-GT - 5/5 (Power)			1A
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Frame buffer CLK Termination

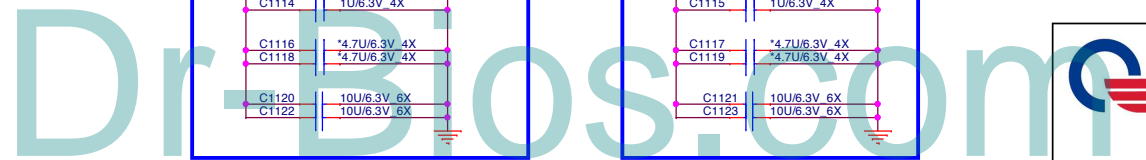
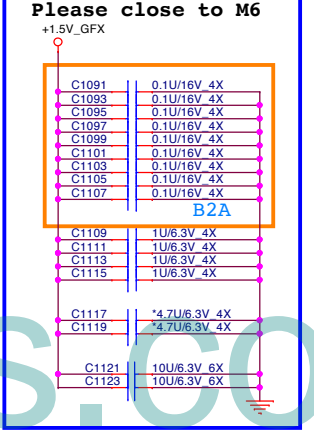
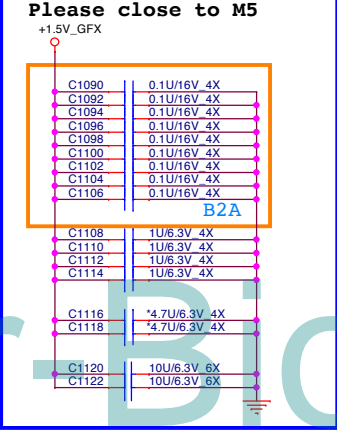
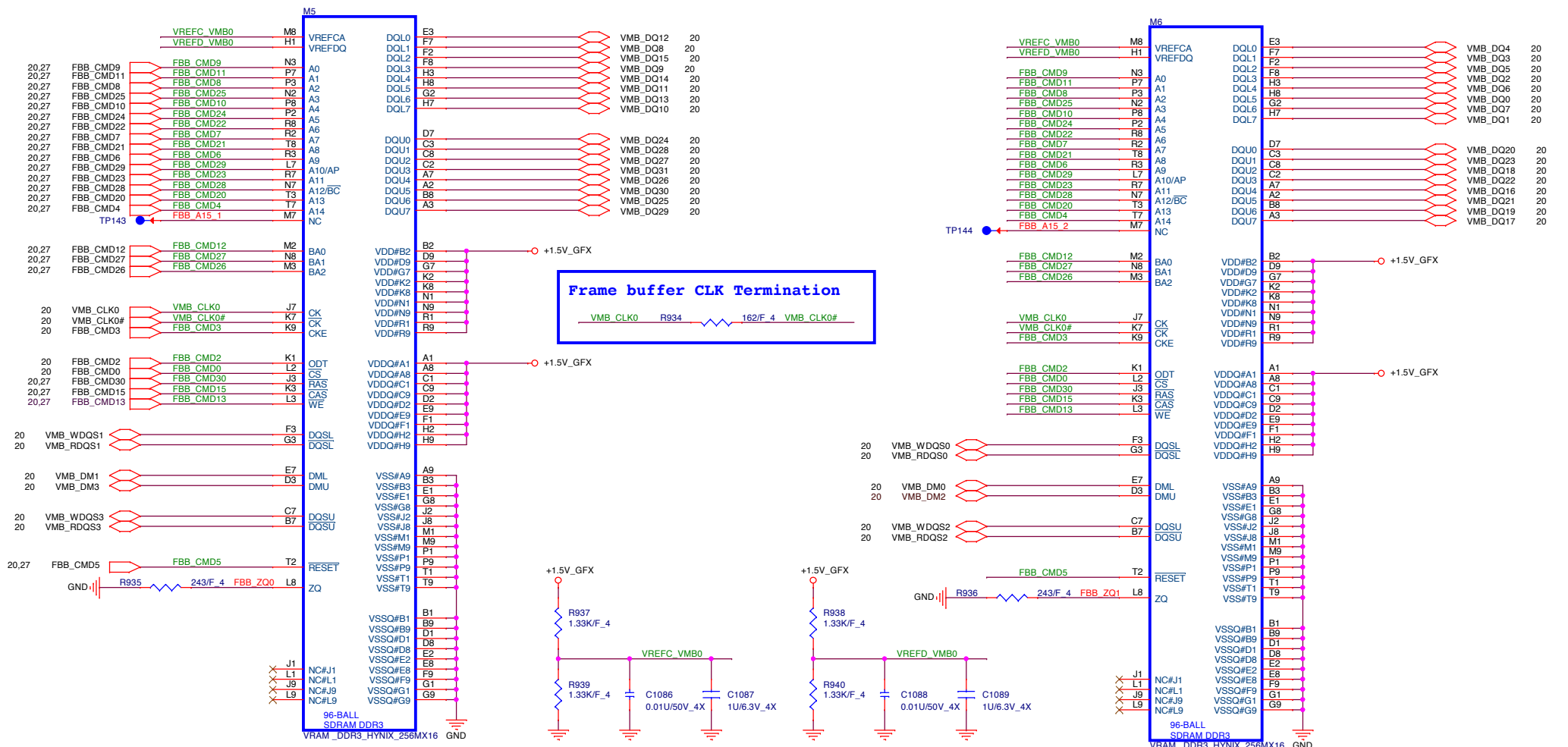
VMA_CLK0 R920 162/F 4 VMA_CLK0#





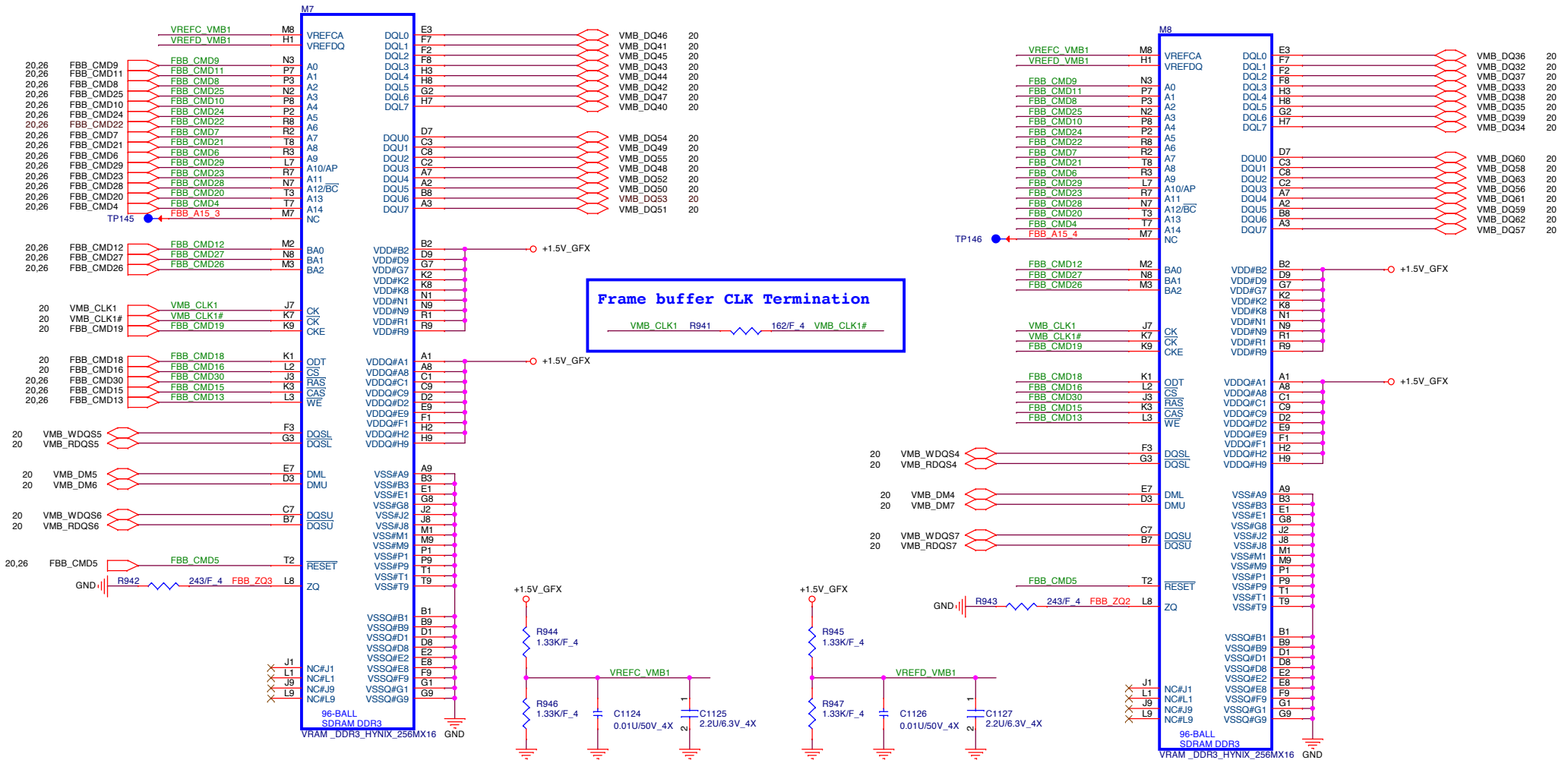
PROJECT :ZRY
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Size	Document Number	Rev
	N16P-GT_DDR3 - A2	1A
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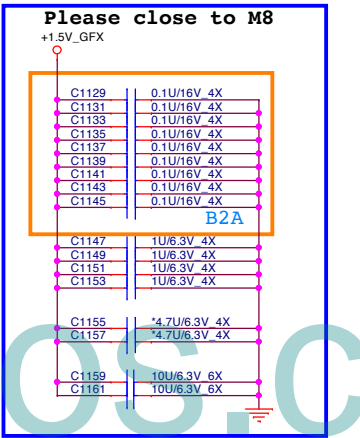
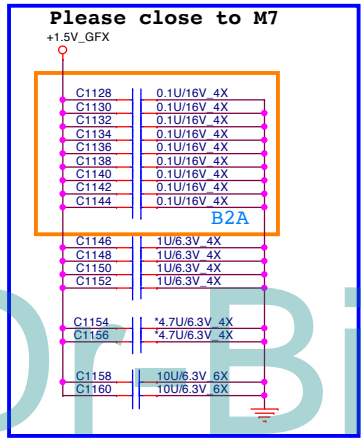
PROJECT :ZRY
Quanta Computer Inc.

Size	Document Number	Rev
	N16P-GT_DDR3 - B1	1A
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Frame buffer CLK Termination

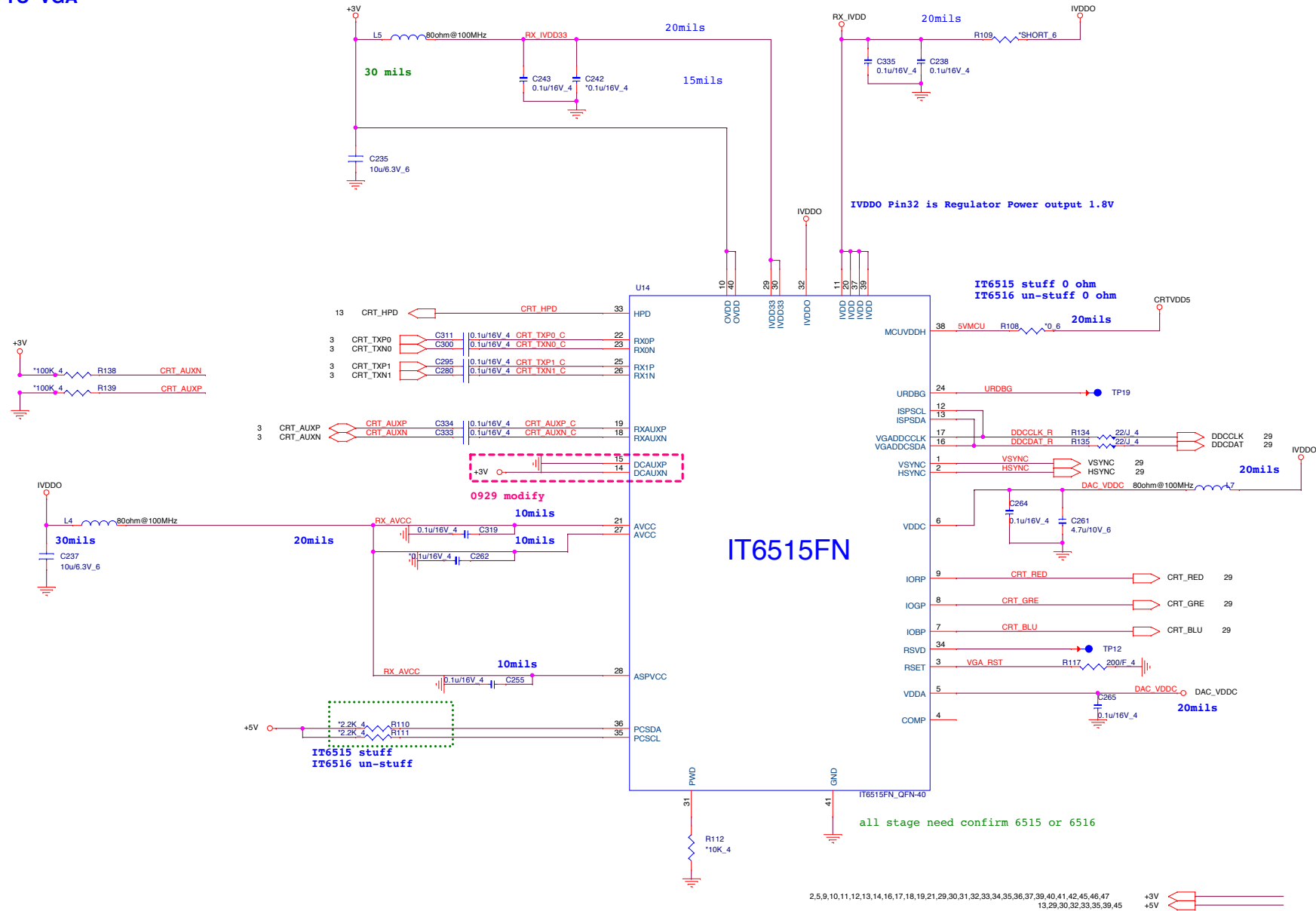
VMB_CLK1 R941 162/F 4 VMB_CLK1#



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	N16P-GT_DDR3 - B2	1A
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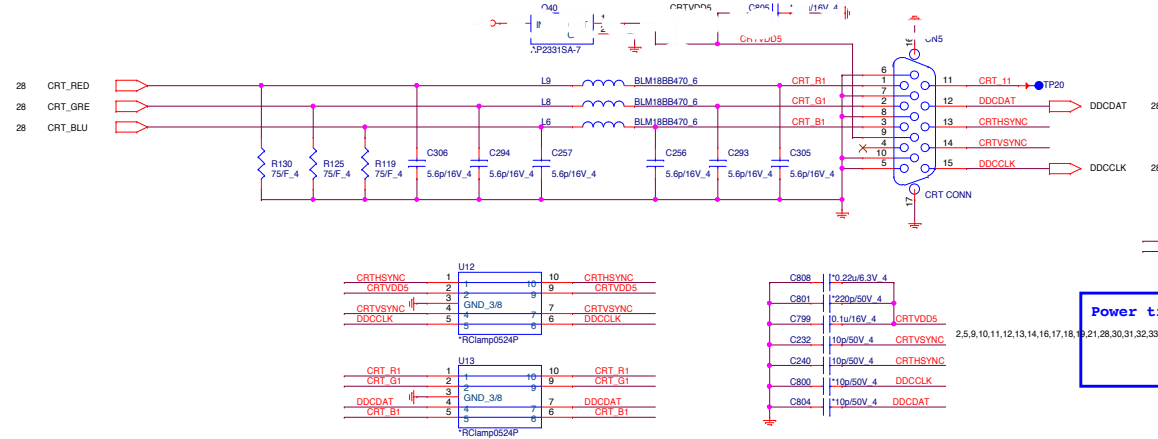
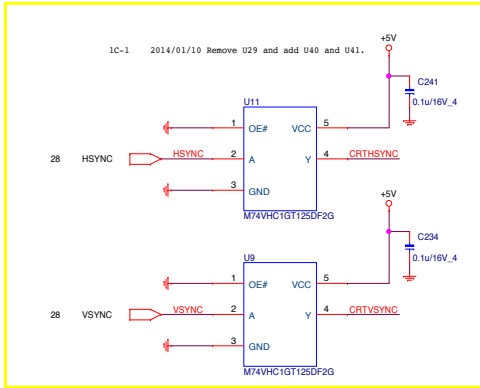
DP TO VGA



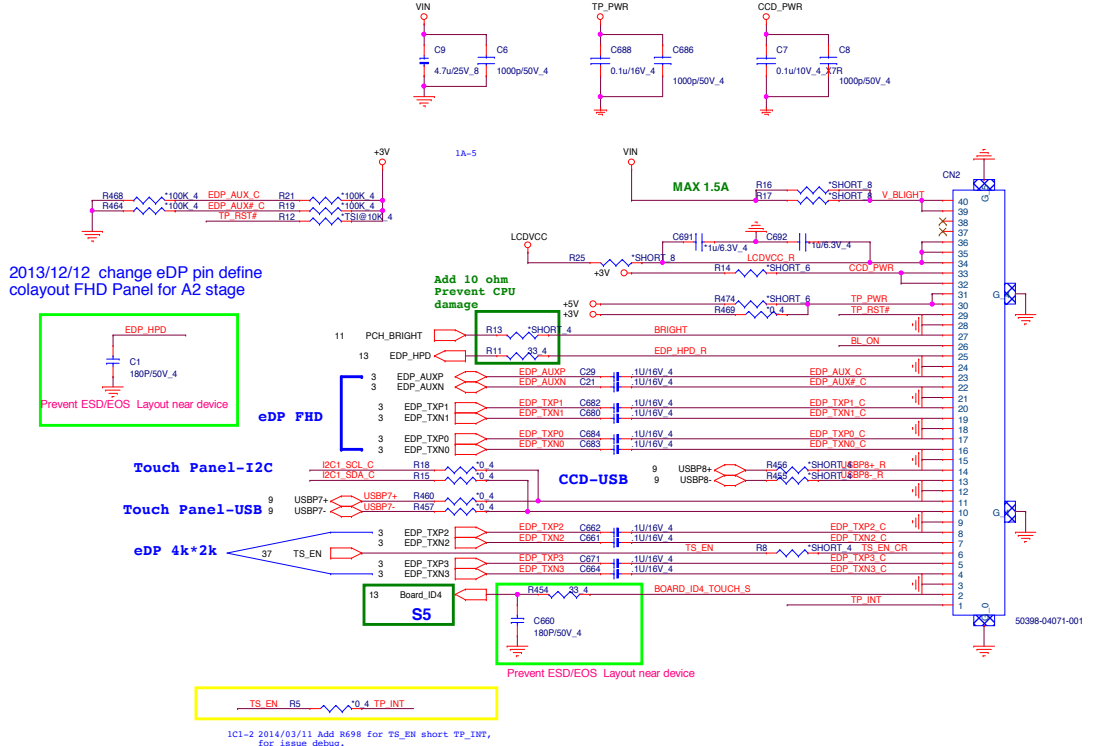
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PROJECT :ZRY
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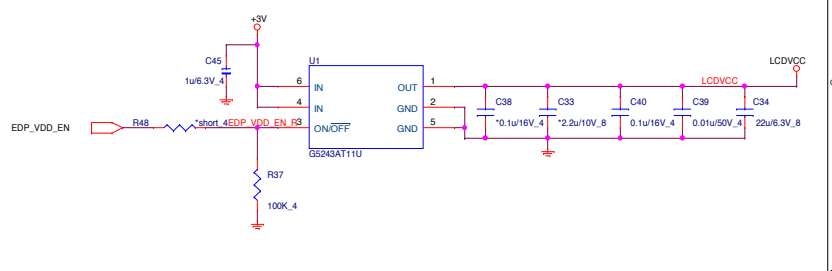
Size	Document Number	Rev
	DP to VGA IT6165	1A
Date:	Tuesday, August 25, 2015	Sheet 28 of 49



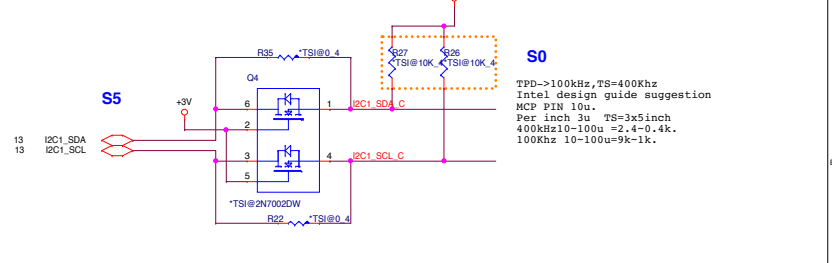
LCD CONNECTOR



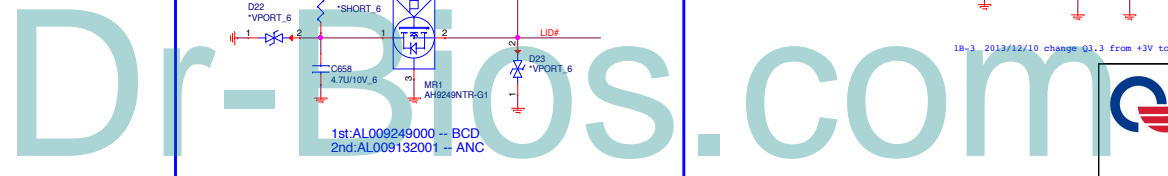
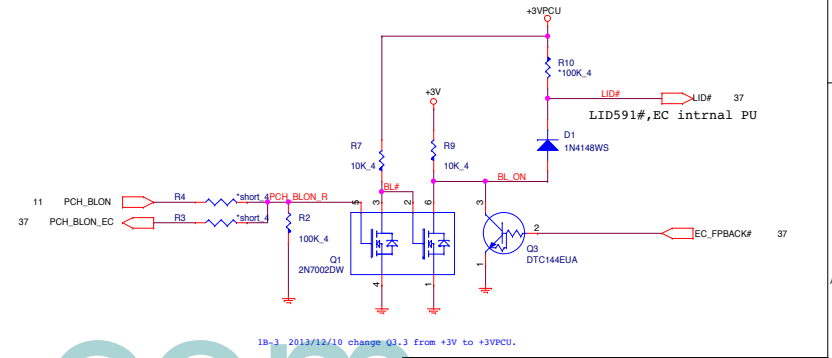
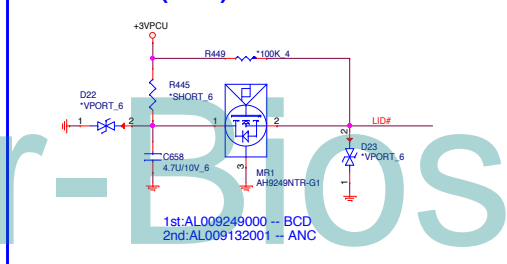
LCD Power



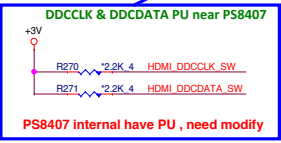
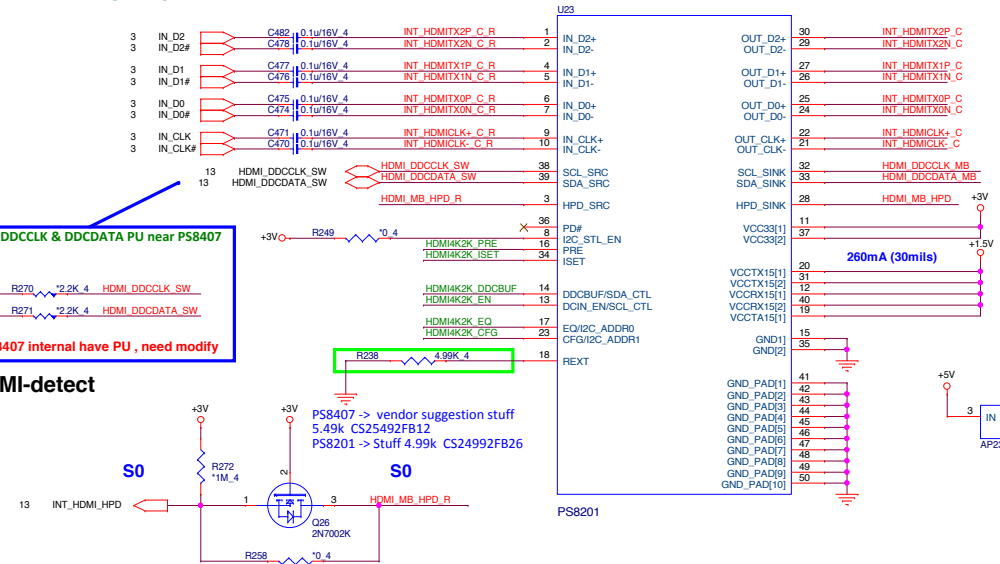
Touch screen level shift I2C(reserve)



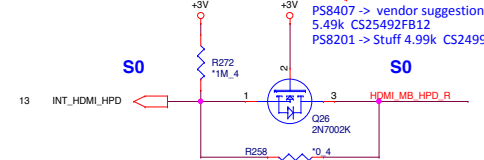
Hall Sensor (HSR)



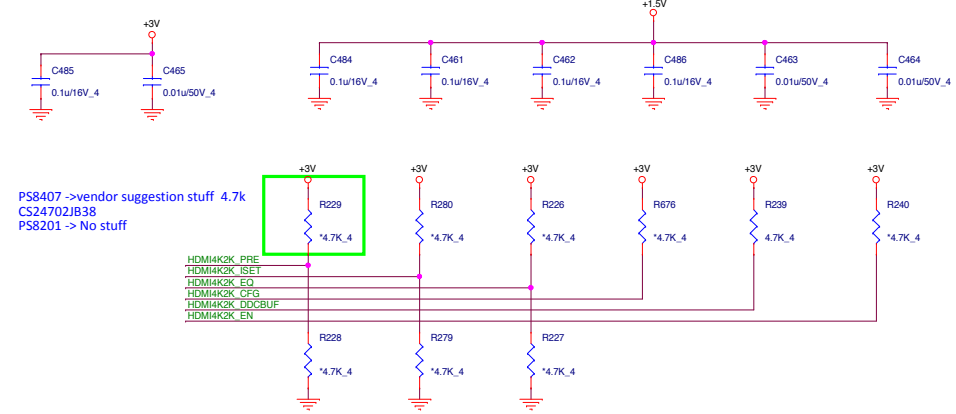
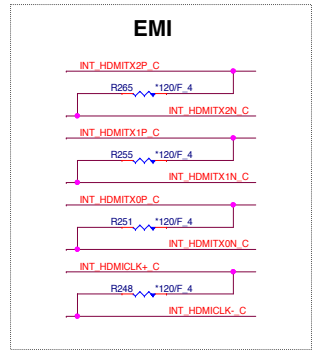
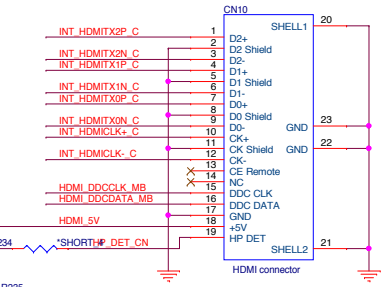
From PCH



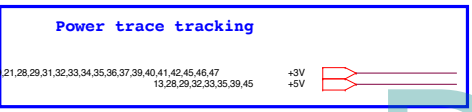
HDMI-detect



HDMI connector



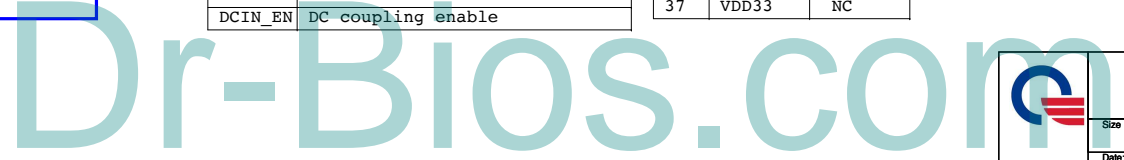
	Pre	ISET	EQ	CFG	DDCBUF	DCIN_EN
NC (Low)	0 dB	default	12.4 dB	HDMI ID disable	default	default, AC coupling input
1 (High)	1.6 dB	+13%	4.3 dB	HDMI ID enable	active DDC buffer with default threshold	DC coupling input
M	2.5 dB	-13%	8.6 dB	N/A	active DDC buffer without internal pull up resistor	N/A



Pre	Output pre-emphasis setting
ISET	TMDS output swing adjustment
EQ	Receiver equalization setting
CFG	Configuration pin
DDCBUF	enable active DDC buffer
DCIN_EN	DC coupling enable

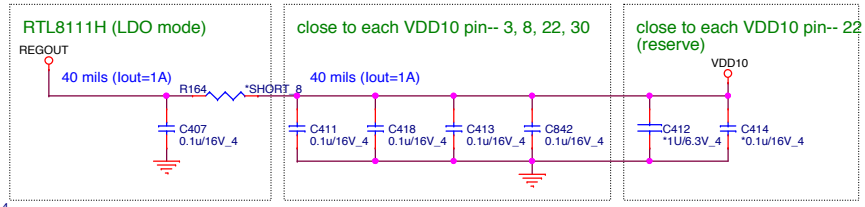
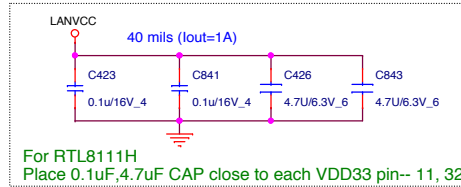
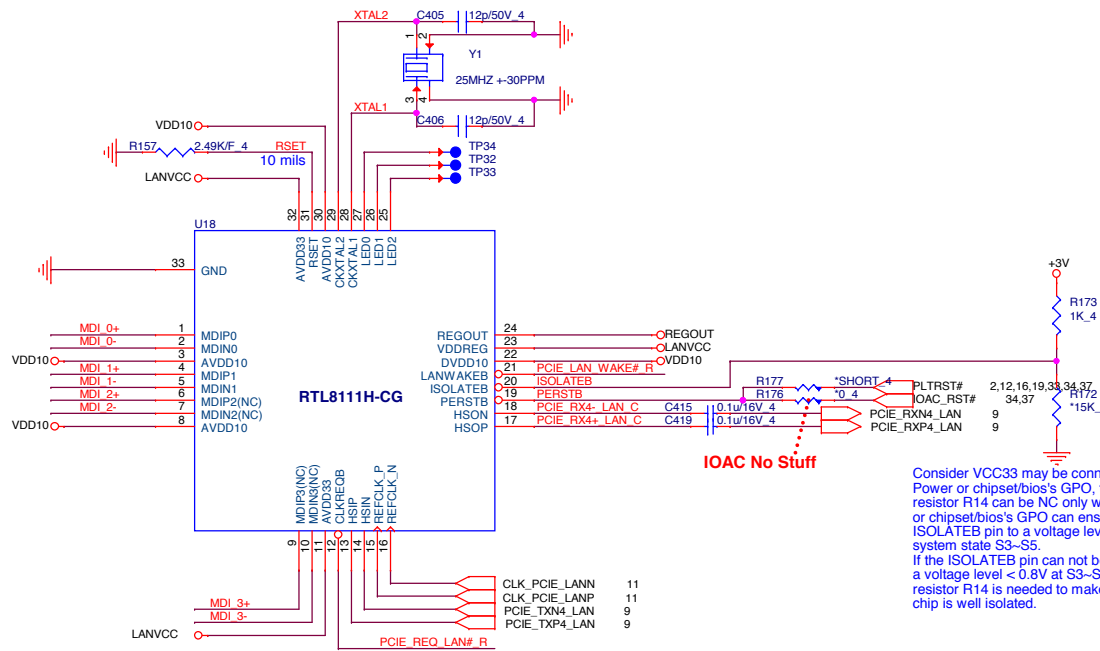
Pin	PS8401A	PS8201A
12	VDDRX	NC
15	GND	NC
34	ISET	NC
37	VDD33	NC

2,5,9,10,11,12,13,14,16,17,18,19,21,28,29,31,32,33,34,35,36,37,39,40,41,42,45,46,47
13,28,29,32,33,35,39,45



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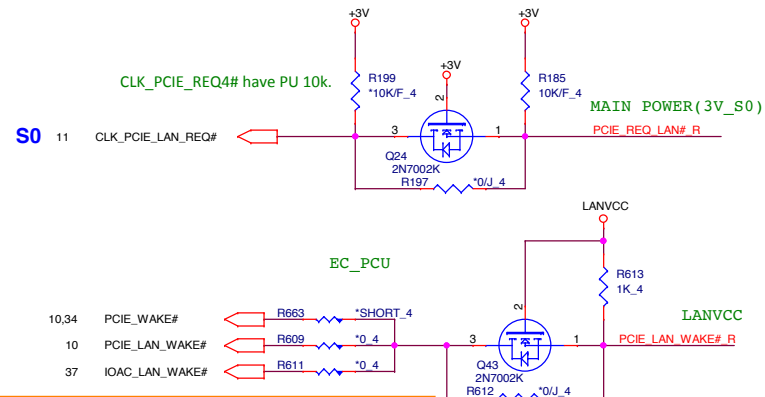
Size	Document Number	Rev
	HDMI (PS8407 4k*2k)	1A
Date:	Tuesday, August 25, 2015	Sheet 30 of 49



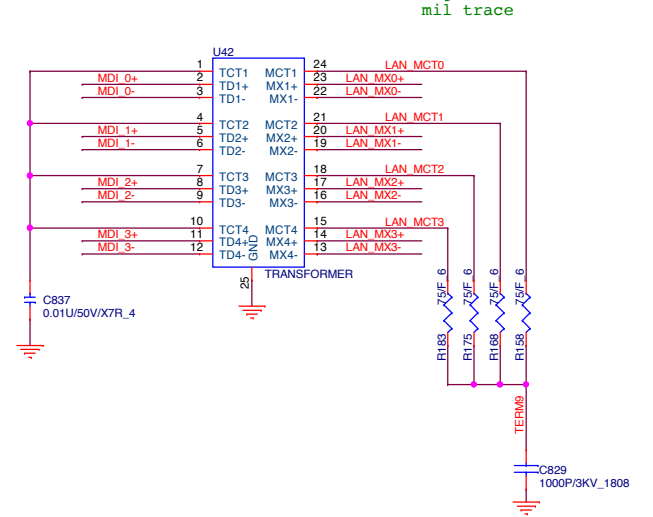
IOAC No Stuff

Consider VCC33 may be connected to Main Power or chipset/bios's GPO, the pull-low resistor R14 can be NC only when Main Power or chipset/bios's GPO can ensure to drive the ISOLATEB pin to a voltage level < 0.8V at the system state S3-S5.
If the ISOLATEB pin can not be well-controlled to a voltage level < 0.8V at S3-S5, the pull-low resistor R14 is needed to make sure the LAN chip is well isolated.

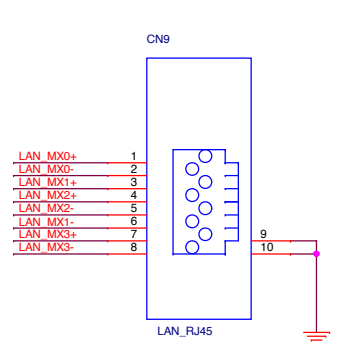
Leakage circuit (MPC)



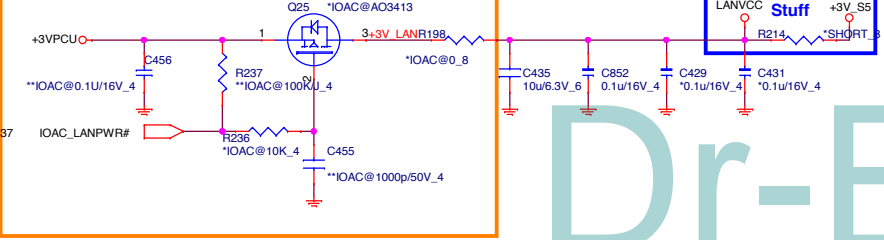
Transformer



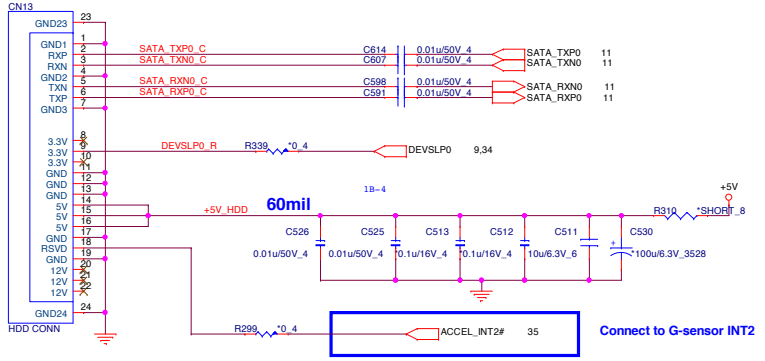
RJ45 Connector



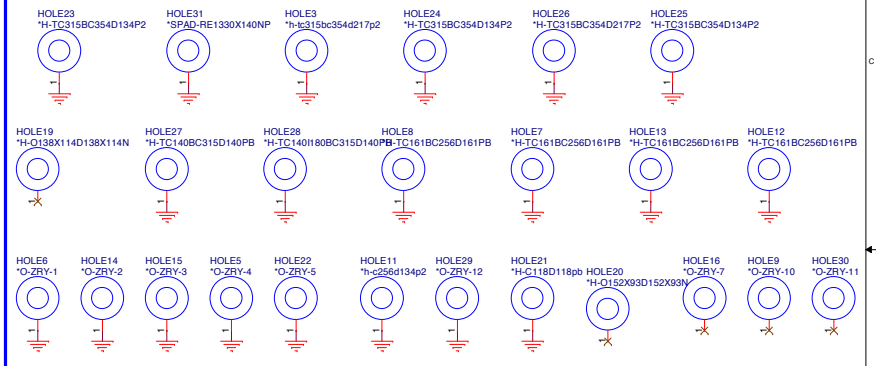
Reserve IOAC No Stuff



2.5" SATA HDD (HDD)



SATA HDD Connector(Remove)



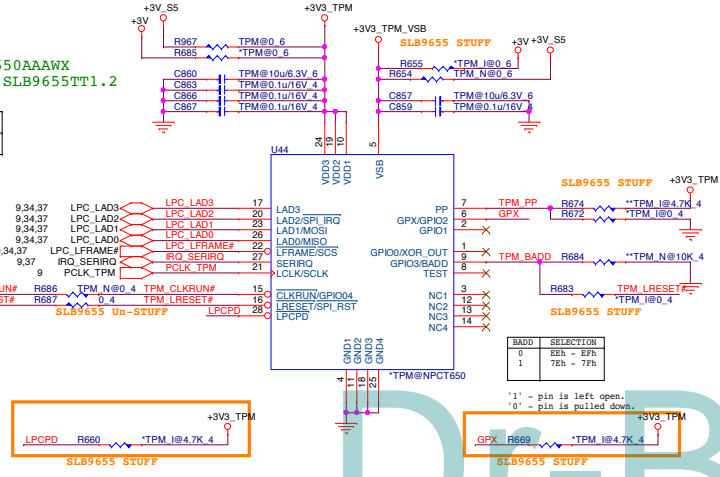
ODD Power (SATA)(Remove)

TPM NPCT650 (TPM)

SP8 BOM周邊上NPCT650
A,B,C P/N:AL009655K01(SLB9655TT1.2- FW4.31)
RAMP P/N: AL000650K01 (NPCT650AAAAX)

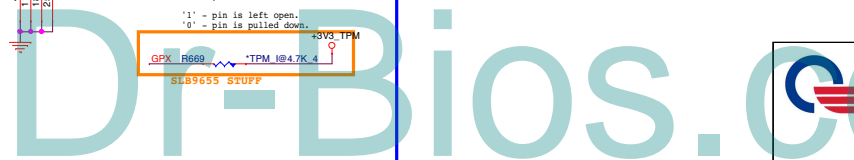
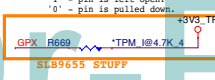
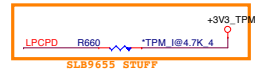
AL000650K01 :NPCT650AAAAX
AL009655K01 : SNI SLB9655TT1.2

TPMM 1.2	AL009655K01
TPMM 2.0	AL000650K01



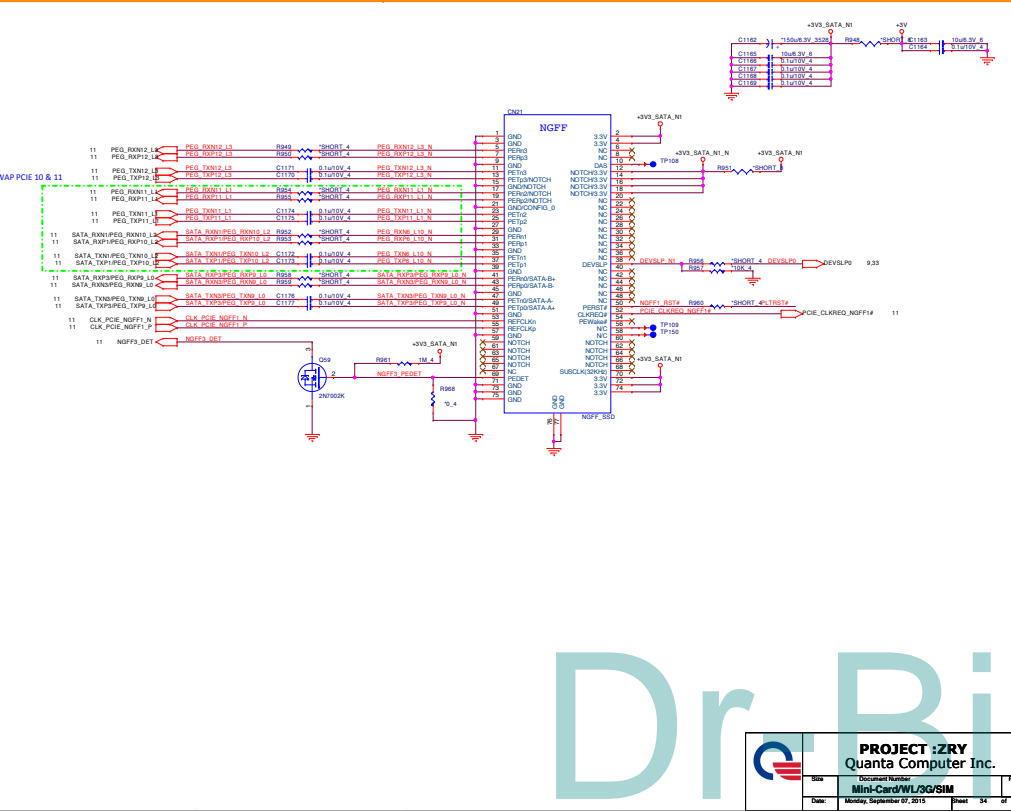
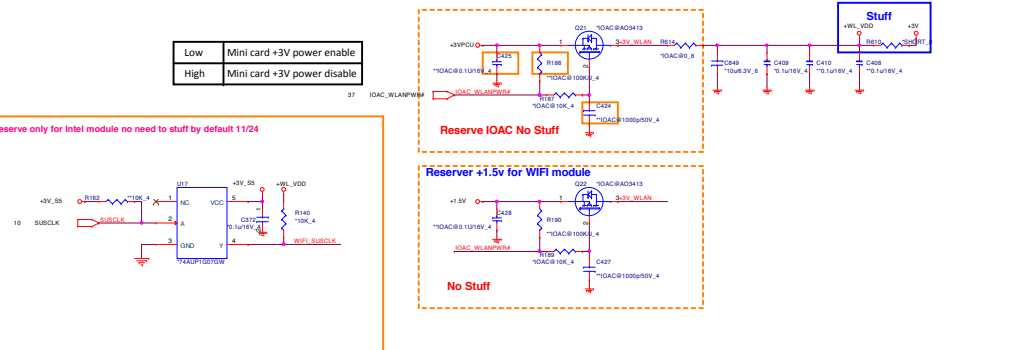
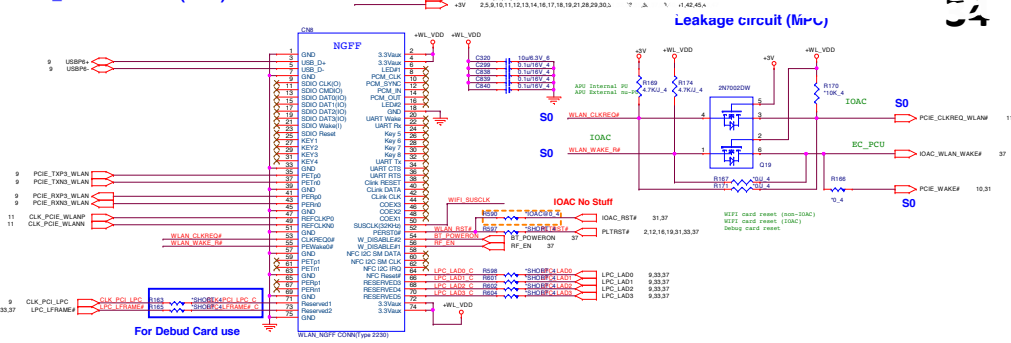
BADD	SELECTION
0	8Eh - 8Fh
1	7Eh - 7Fh

'1' - pin is left open.
'0' - pin is pulled down.

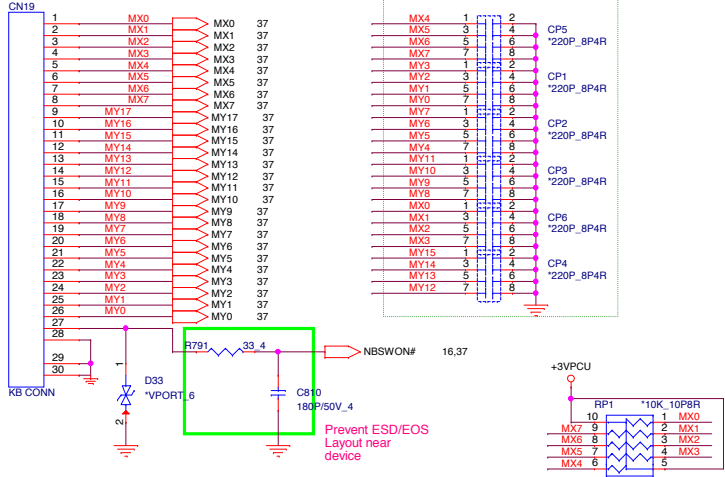


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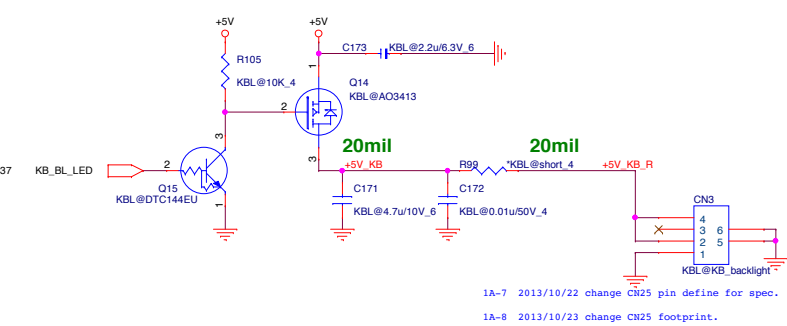
Size	Document Number	Rev
	HDD/ODD/TPM NPCT650	1A
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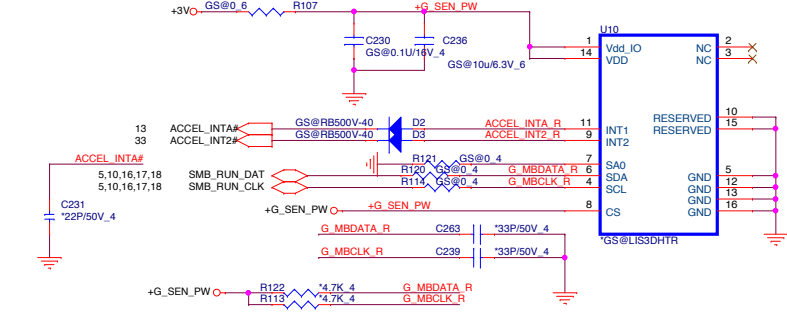
KEYBOARD (KBC)



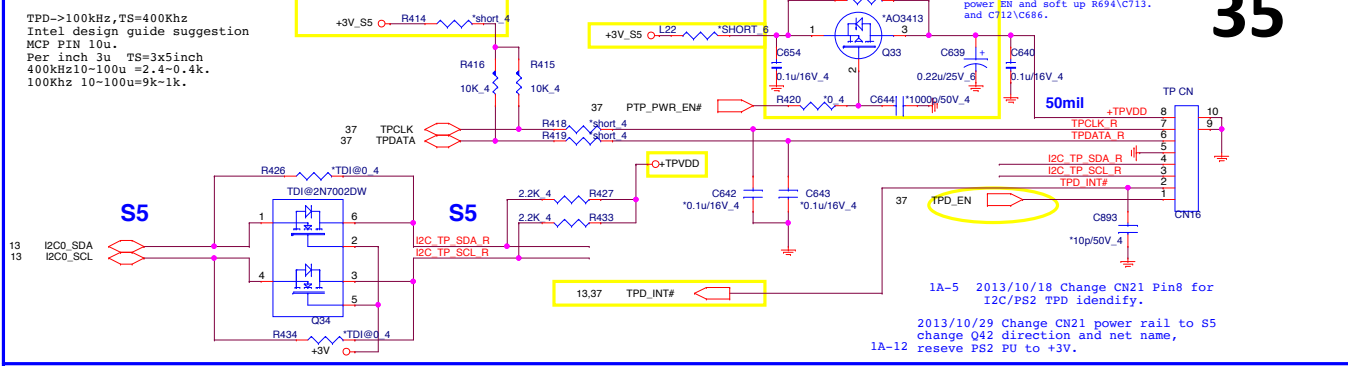
KB_LED (KBC)



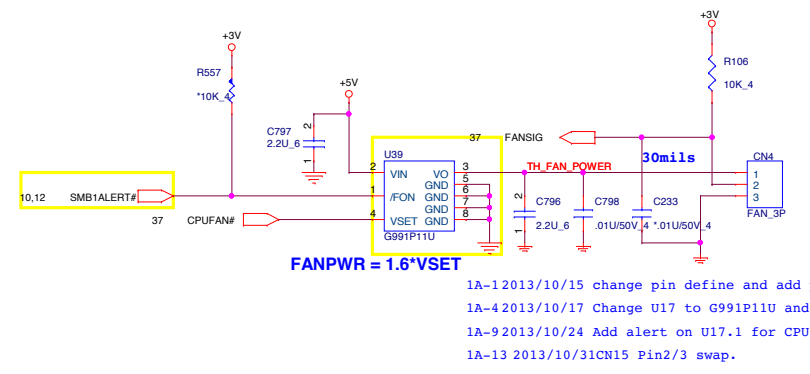
G-sensor (ACS)



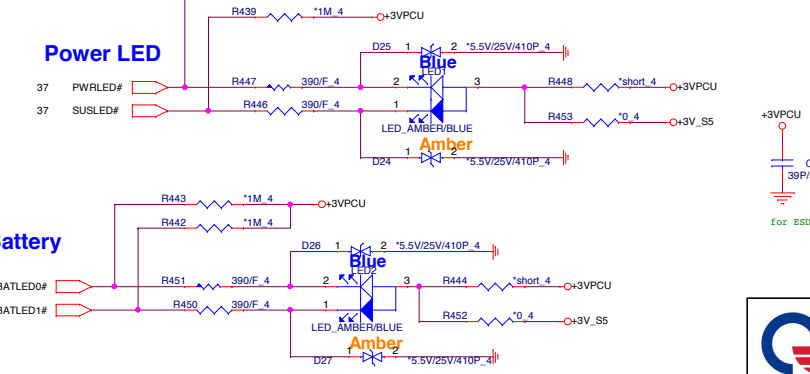
TPD (TPD)



CPU FAN (THM)

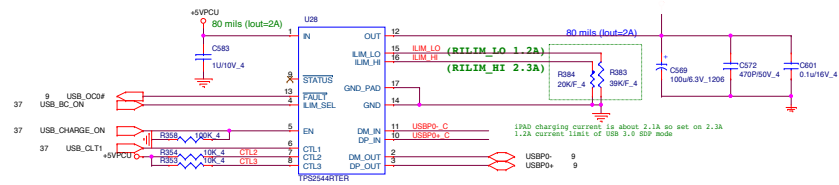


POWER LED (UIF)



PROJECT :ZRY Quanta Computer Inc.		
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	KB/TP/FAN	1A
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USB Charger to 3.0 (UBC)



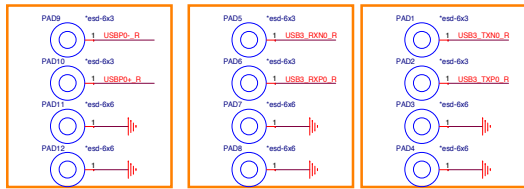
	CTL1	CTL2	CTL3	ILIM_SEL
SDP	1	1	1	0
CDP	1	1	1	1
DCP	0	1	1	X

36

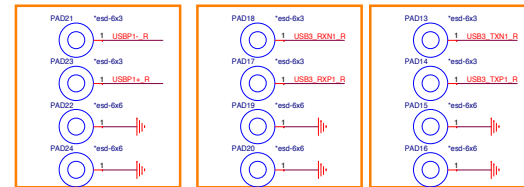
GMT:AL003703000(G3703)
 TI:AL002544001(TPS2544)
 Silergy:

RILIM_LO is optional and the ILIM_LO pin may be left unconnected if the following conditions are met:
 1. ILIM_SEL is always set high
 2. Load Detection / Port Power Management is not used
 3. Mouse / Keyboard wake function is not used
 If conditions 1 and 2 are met but the mouse / keyboard wake function is also desired, it is recommended to use RILIM_LO < 80.6 kΩ.
 The following equation programs the typical current limit:
 (1) $IOS_typ(mA) = 50.250 / (RILIM_XX(KΩ) + 0.1)$
 RILIM_XX corresponds to either RILIM_HI or RILIM_LO as appropriate.

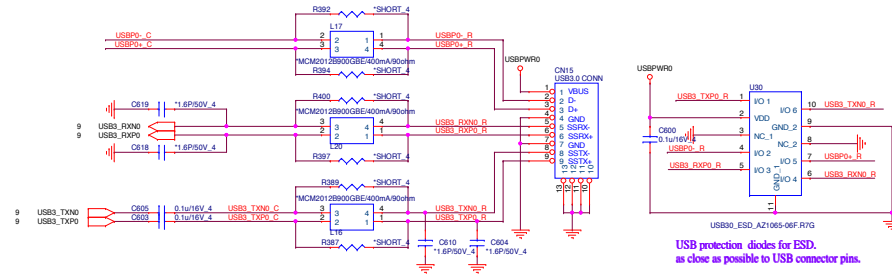
USB 3.0 Connector (UB3)



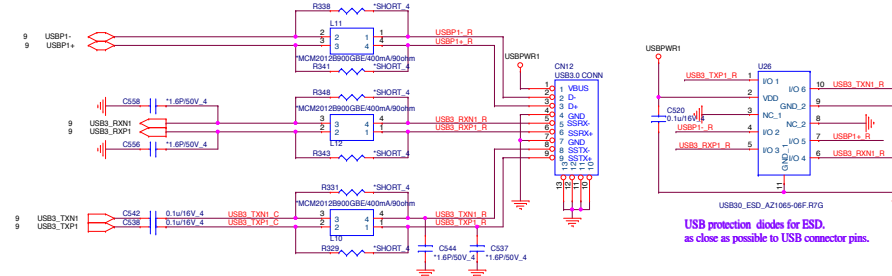
0722 Added PAD1-4 as ESD protection



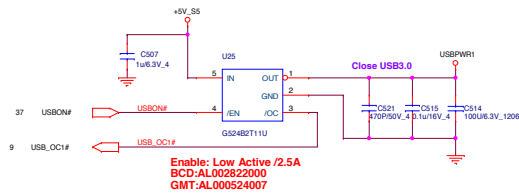
0722 Added PAD1-4 as ESD protection



USB protection diodes for ESD, as close as possible to USB connector pins.

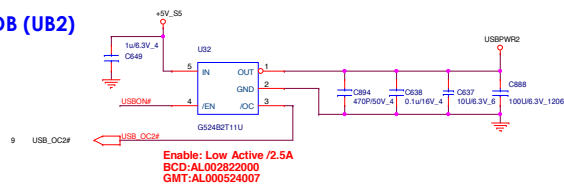


USB protection diodes for ESD, as close as possible to USB connector pins.



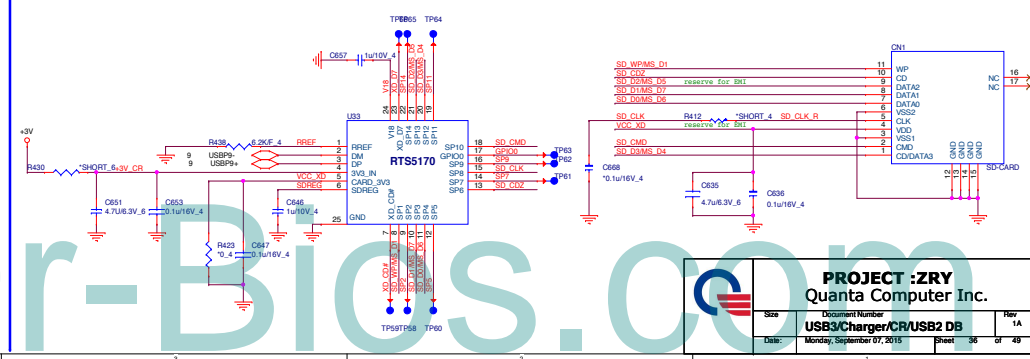
Enable: Low Active /2.5A
 BCD:AL002822000
 GMT:AL000524007

USB2.0 DB (UB2)



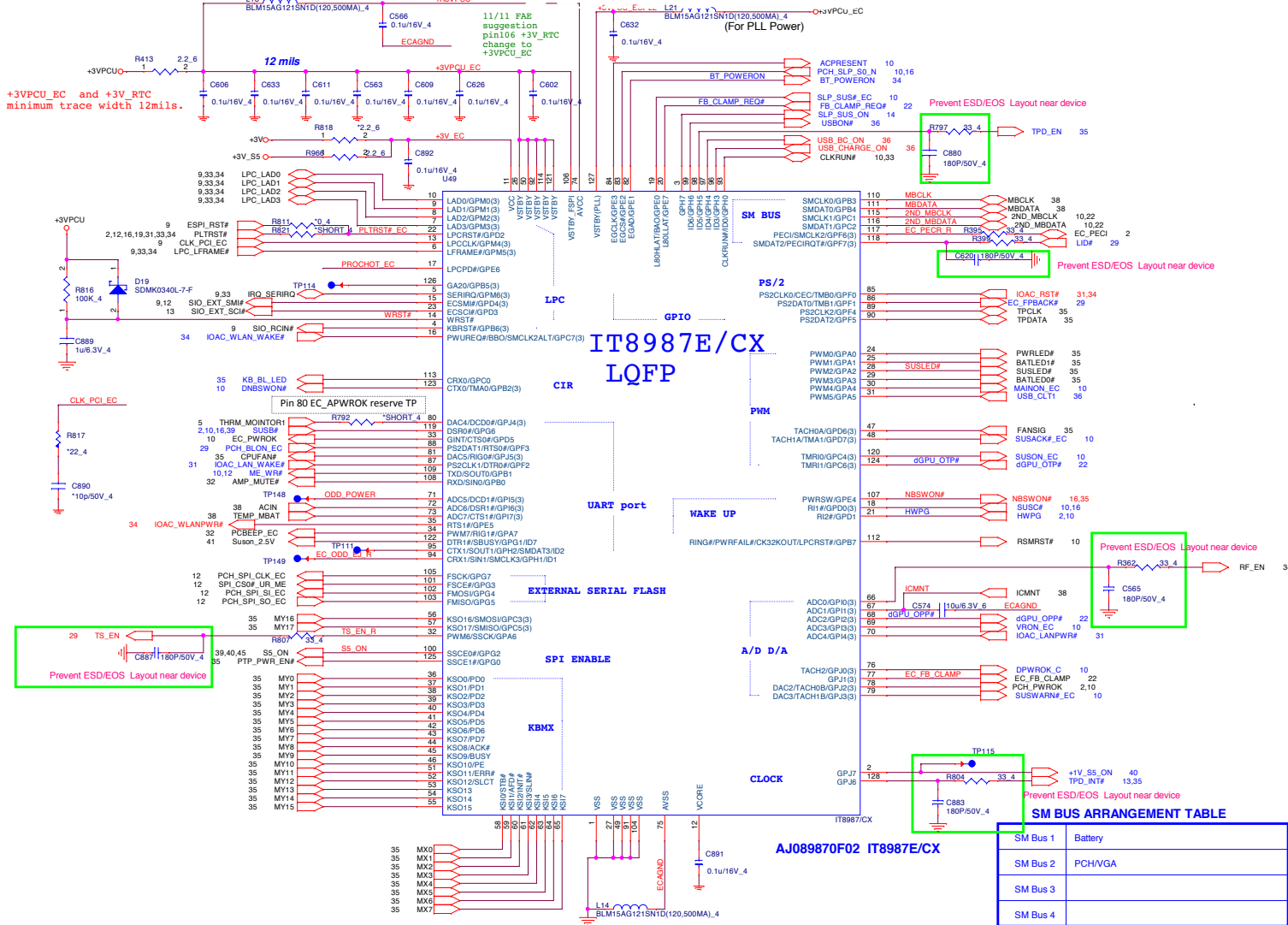
Enable: Low Active /2.5A
 BCD:AL002822000
 GMT:AL000524007

Card Reader (CRD)

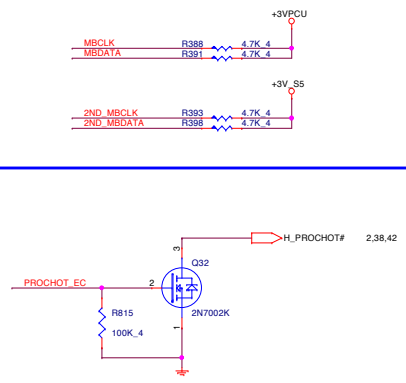


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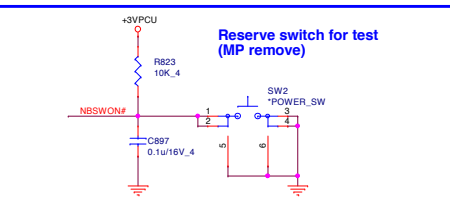
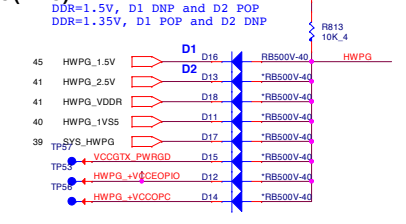
Doc No	Doc Name	Rev
1000000000	USB3/Charger/CRD/USB2 DB	1A
1000000000	Monday, September 07, 2015	Sheet 36 of 49



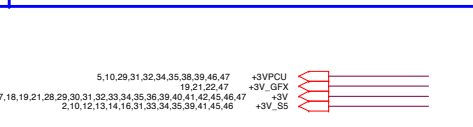
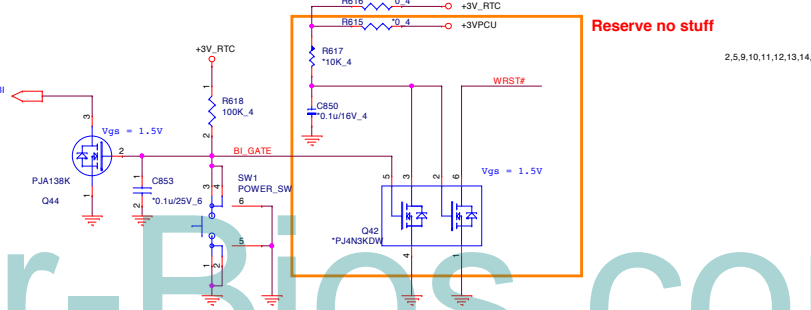
SM BUS PU(KBC)

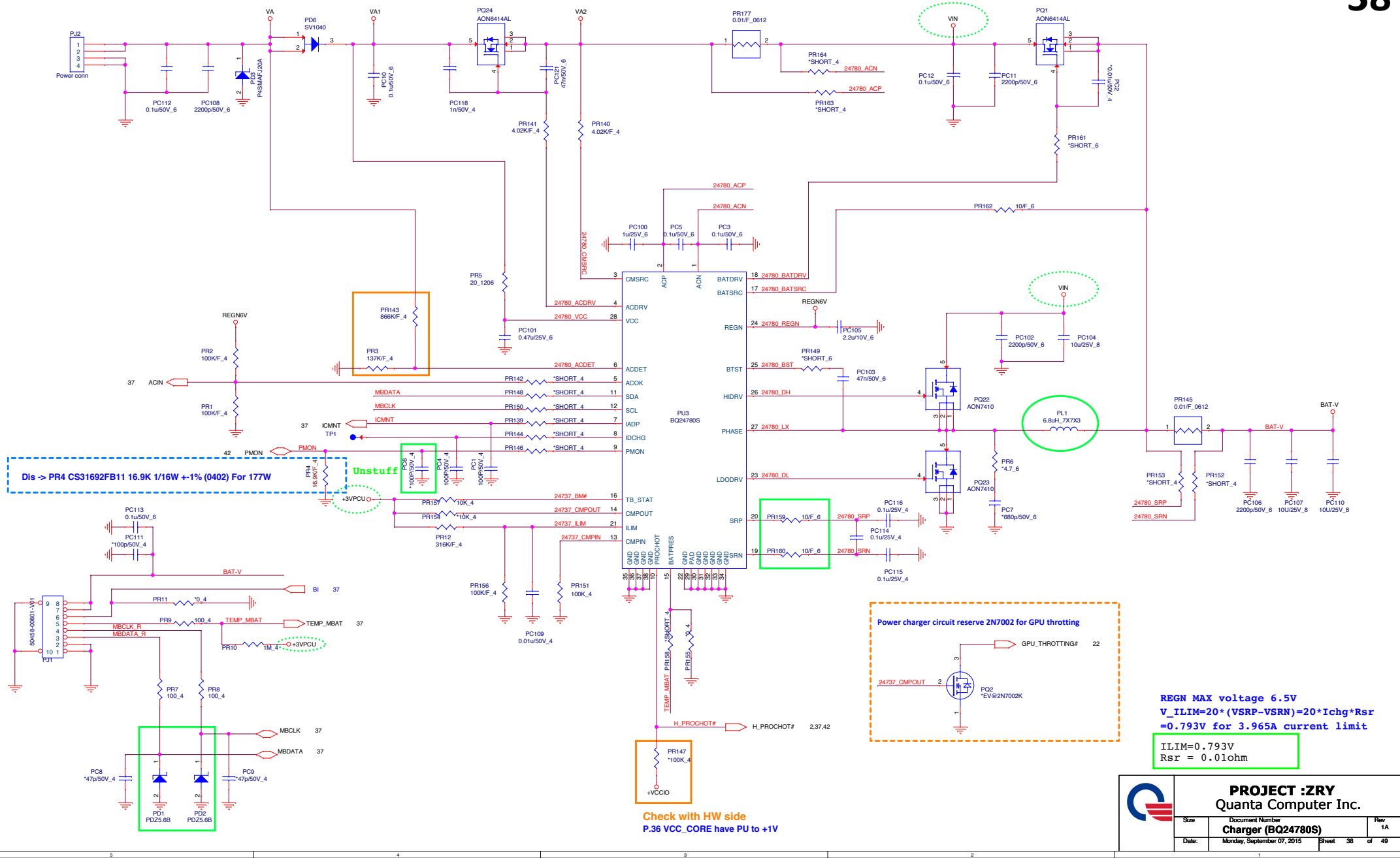


HWPG(KBC)

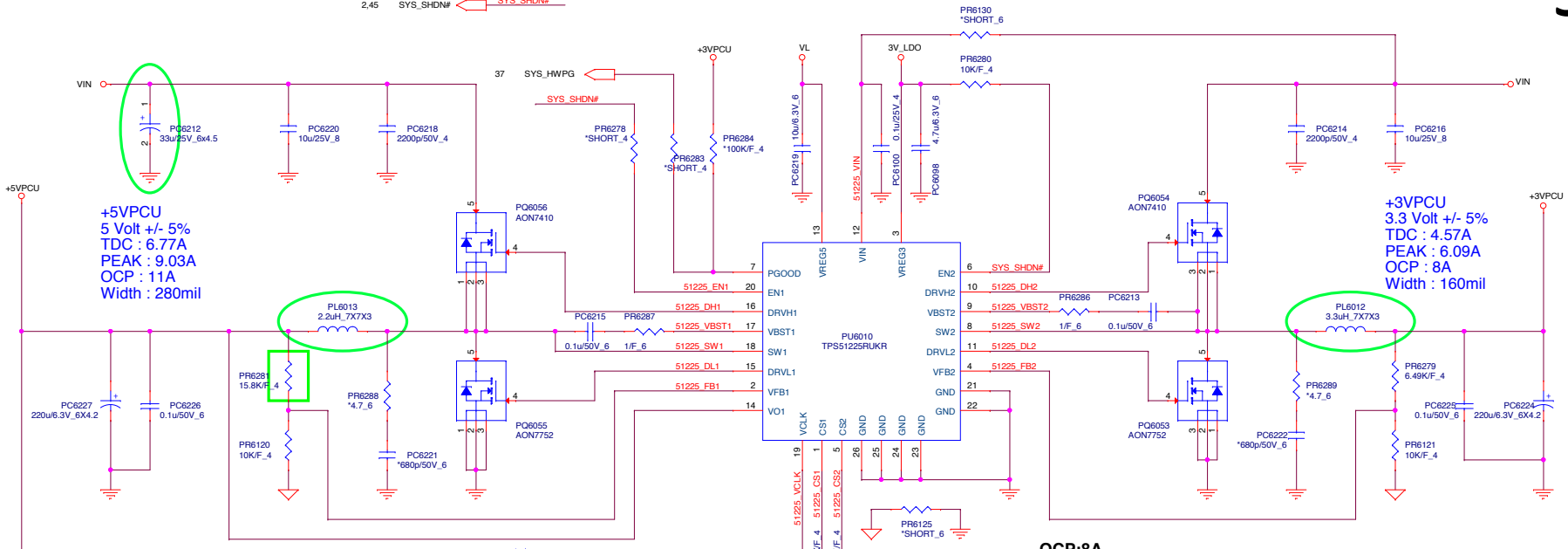


Reset SW (FSW)





2.45 SYS_SHDN# ← SYS_SHDN#

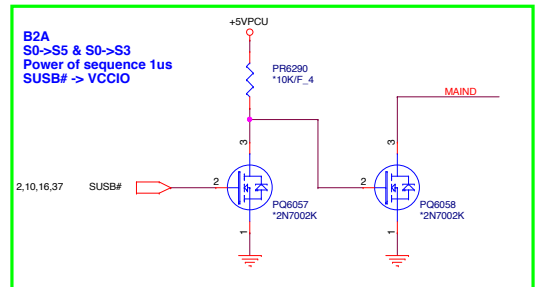


OCP:11A

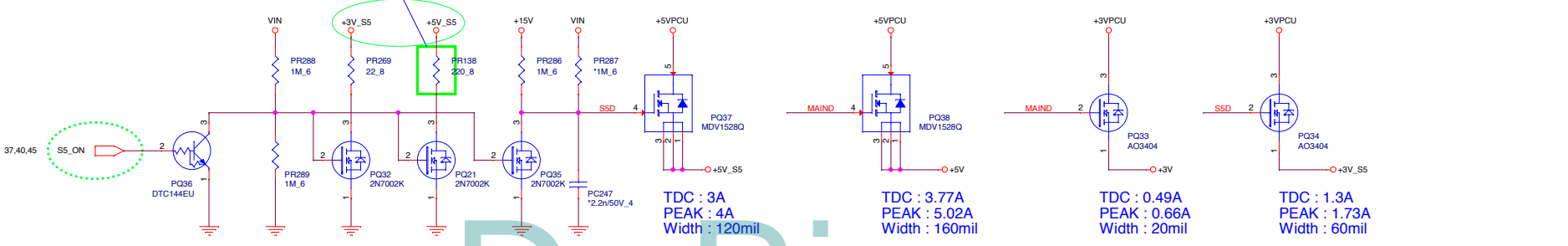
L(ripple current)
 $= (9-5) \cdot 5 / (2.2 \cdot 0.3 \cdot 9)$
 $= 3.367A$
 $l_{ocp} = 12 - (3.367 / 2) = 9.316A$
 $V_{th} = (9.316A \cdot 14.5m\Omega) + 1mV = 136.089mV$
 $R(lim) = (136.089mV \cdot 8) / 10uA$
 $\approx 108.87K$

OCP:8A

L(ripple current)
 $= (9-3.3) \cdot 3 / (3.3 \cdot 0.355 \cdot 9)$
 $\approx 1.784A$
 $l_{ocp} = 8 - (1.784 / 2) = 7.108A$
 $V_{th} = (7.108A \cdot 14.5m\Omega) + 1mV = 104.066mV$
 $R(lim) = (104.066mV \cdot 8) / 10uA$
 $\approx 83.25K$



3/11 Change 22 ohm to 220 ohm for Audio bo bo sound (S3)



TDC : 3A
PEAK : 4A
Width : 120mil

TDC : 3.77A
PEAK : 5.02A
Width : 160mil

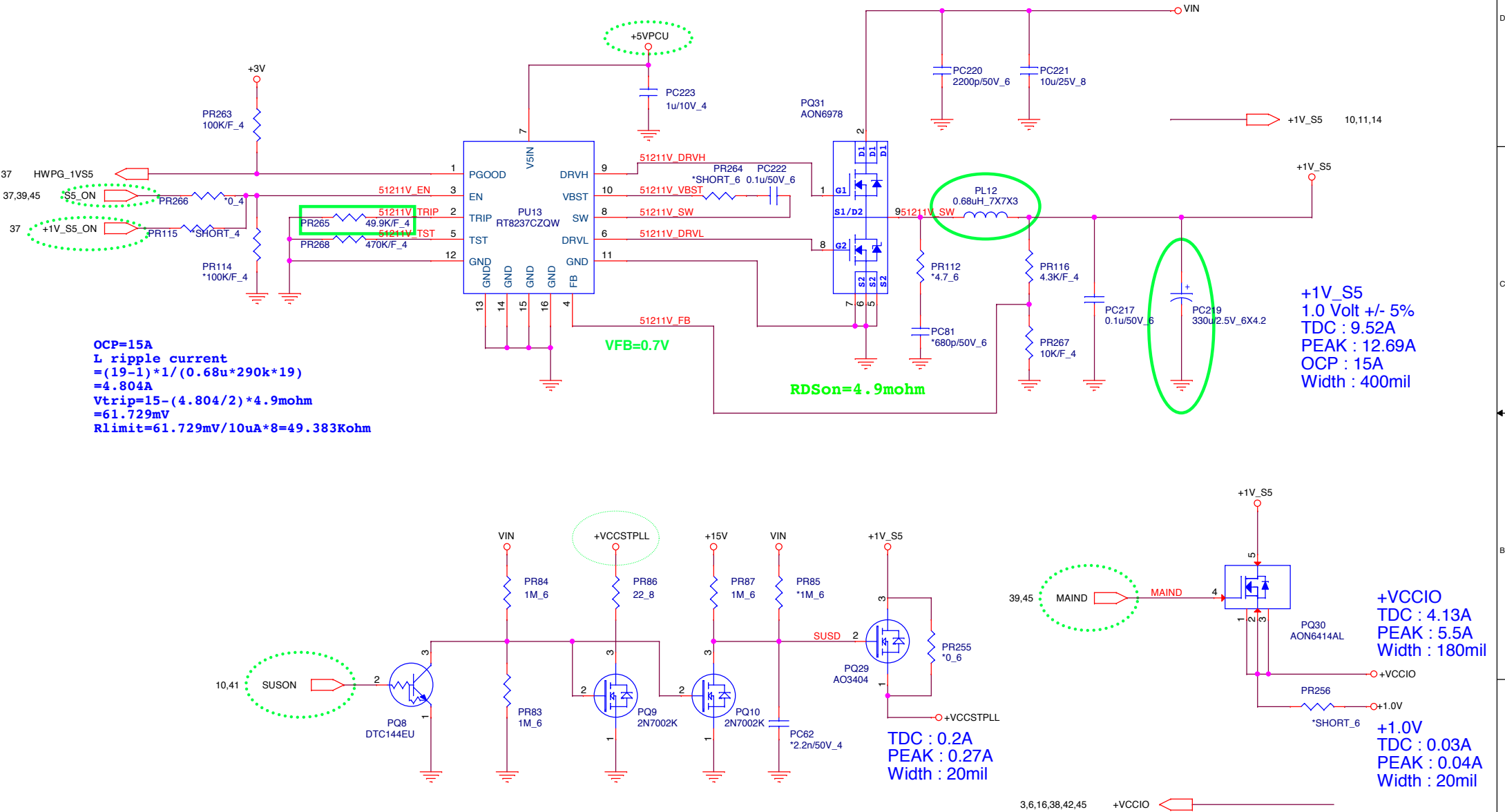
TDC : 0.49A
PEAK : 0.66A
Width : 20mil

TDC : 1.3A
PEAK : 1.73A
Width : 60mil

Dr-Bios.com

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	SYSTEM 5V/3V (TPS51225)	1A
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OCP=15A
 L ripple current
 $= (19-1) * 1 / (0.68u * 290k * 19)$
 $= 4.804A$
 $V_{trip} = 15 - (4.804 / 2) * 4.9mohm$
 $= 61.729mV$
 $R_{limit} = 61.729mV / 10uA * 8 = 49.383Kohm$

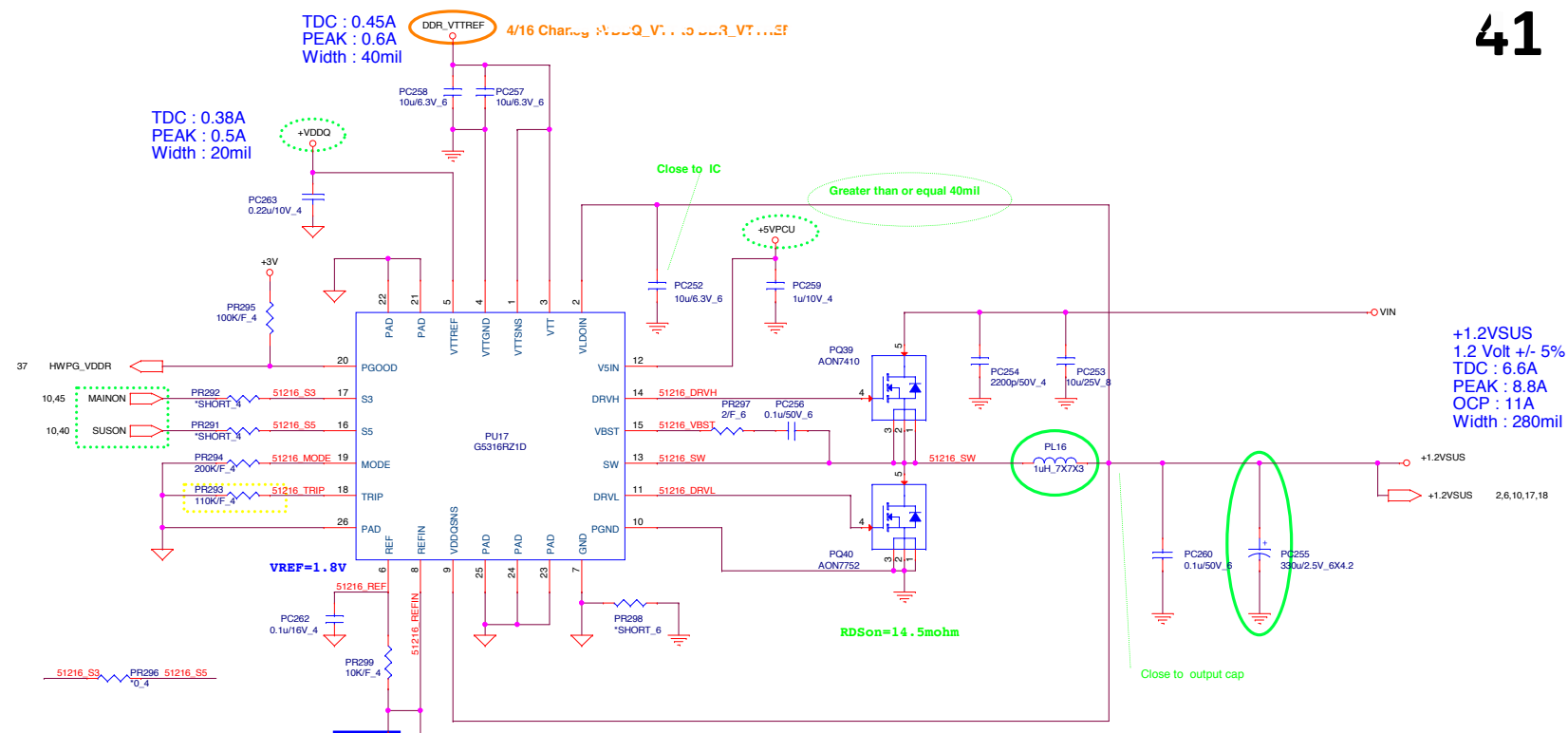
+1V_S5
 1.0 Volt +/- 5%
 TDC : 9.52A
 PEAK : 12.69A
 OCP : 15A
 Width : 400mil

TDC : 0.2A
 PEAK : 0.27A
 Width : 20mil

+VCCIO
 TDC : 4.13A
 PEAK : 5.5A
 Width : 180mil

+1.0V
 TDC : 0.03A
 PEAK : 0.04A
 Width : 20mil

Size	Document Number	Rev
	+1V_S5 (RT8237CZQW)	1A
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+1.2VSUS
1.2 Volt +/- 5%
TDC : 6.6A
PEAK : 8.8A
OCP : 11A
Width : 280mil

Mode **Frequency** **Discharge mode**

200K	400K	Tracking Discharge
100K	300K	Tracking Discharge

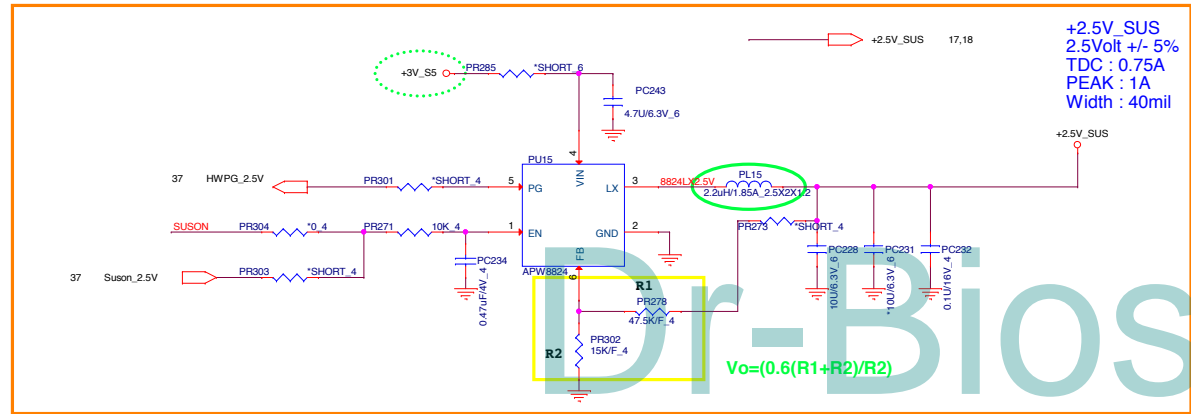
OCP=11A
L ripple current
= (19-1.2) * 1.2 / (1u * 400k * 19)
= 2.81A
Vtrip = 11 - (2.81/2) * 14.5mohm
= 139.123mV
Rlimit = 139.123mV / 10uA * 8 = 111.29Kohm

DDR4=1.2V
PR299=10K/F_4
PR300=20K/F_4

Mode	Frequency	Discharge mode
200K	400K	Tracking Discharge
100K	300K	Tracking Discharge

	S3	S5	+1.35VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (main on off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

4/16 Chaneg DDR3L to DDR4
Adding +2.5V Power Rail

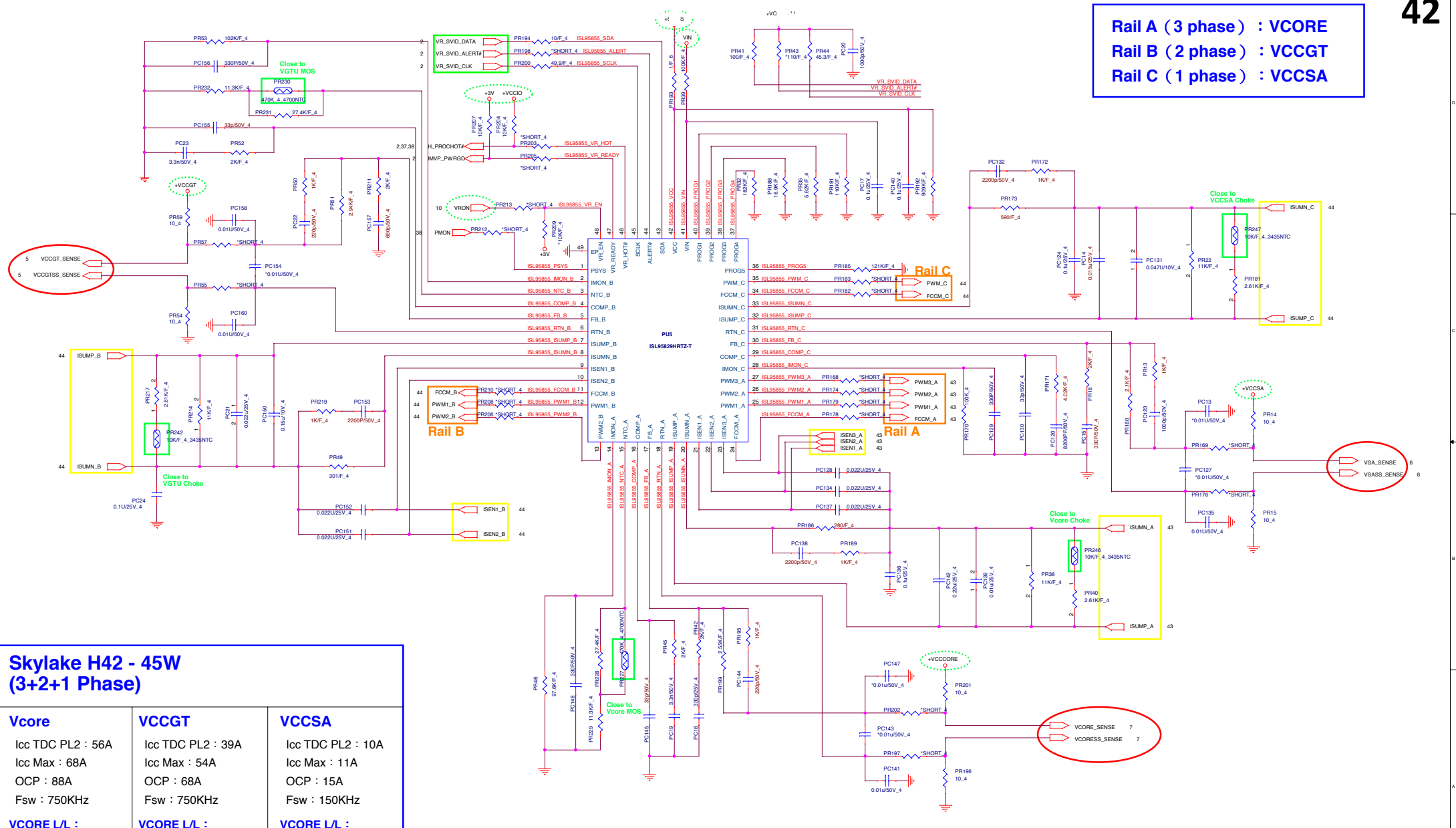


+2.5V_SUS
2.5Volt +/- 5%
TDC : 0.75A
PEAK : 1A
Width : 40mil

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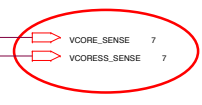
Size	Document Number	Rev
	DDR4 1.2V (G5316RZ1D)	1A
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Rail A (3 phase) : VCORE
Rail B (2 phase) : VCCGT
Rail C (1 phase) : VCCSA



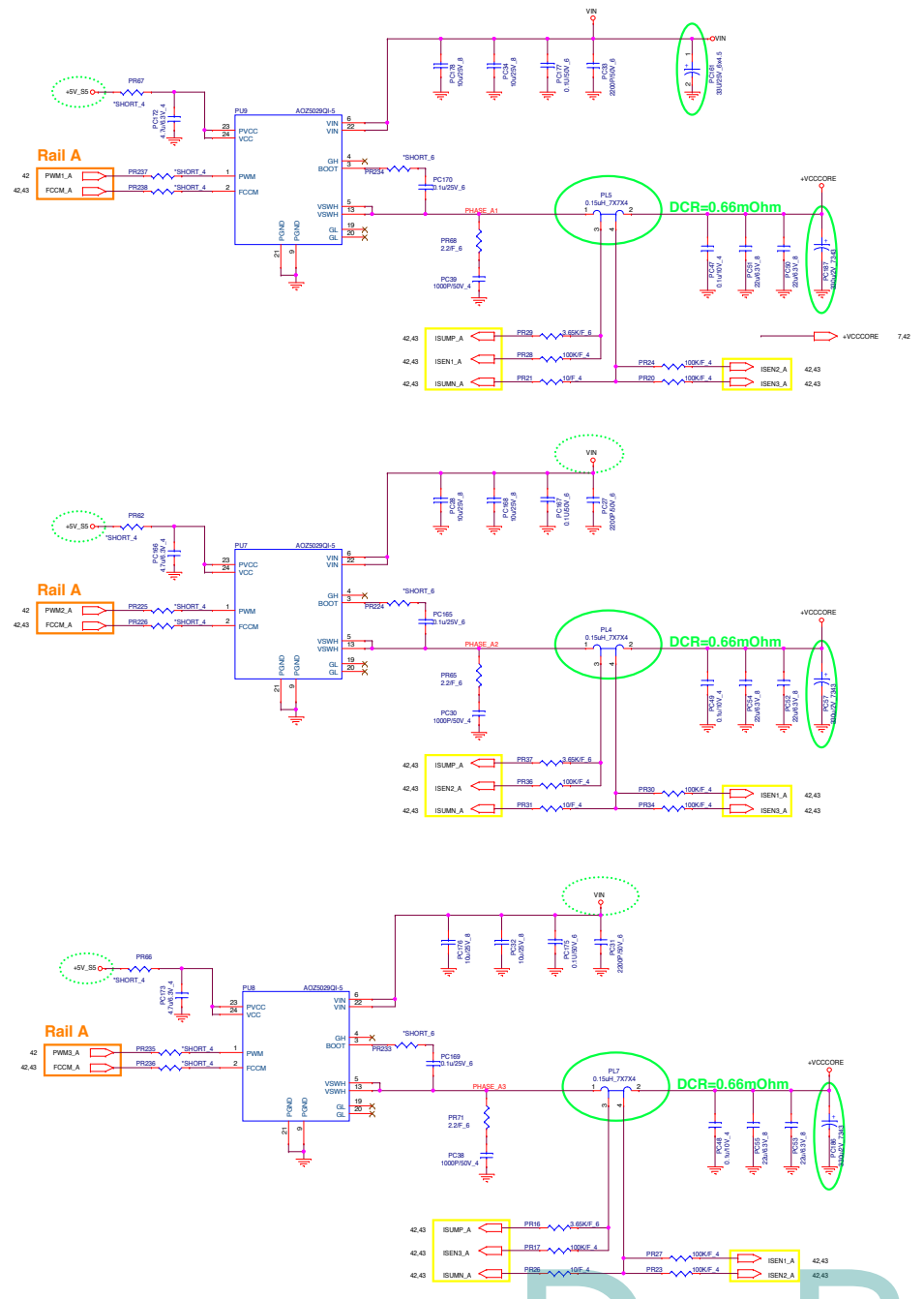
Skylake H42 - 45W (3+2+1 Phase)

Vcore	VCCGT	VCCSA
Icc TDC PL2 : 56A	Icc TDC PL2 : 39A	Icc TDC PL2 : 10A
Icc Max : 68A	Icc Max : 54A	Icc Max : 11A
OCP : 88A	OCP : 68A	OCP : 15A
Fsw : 750KHz	Fsw : 750KHz	Fsw : 150KHz
VCORE L/L :	VCORE L/L :	VCORE L/L :
R_DC_LL : 1.8mV/A	R_DC_LL : 2.65mV/A	R_DC_LL : 9.1mV/A
R_AC_LL : 1.8mV/A	R_AC_LL : 2.65mV/A	R_AC_LL : 9.1mV/A



	PROJECT :ZRY		
	Quanta Computer Inc.		
	Size	Document Number	Rev
		CPU_CORE (ISL95855HRTZ-T)	1A
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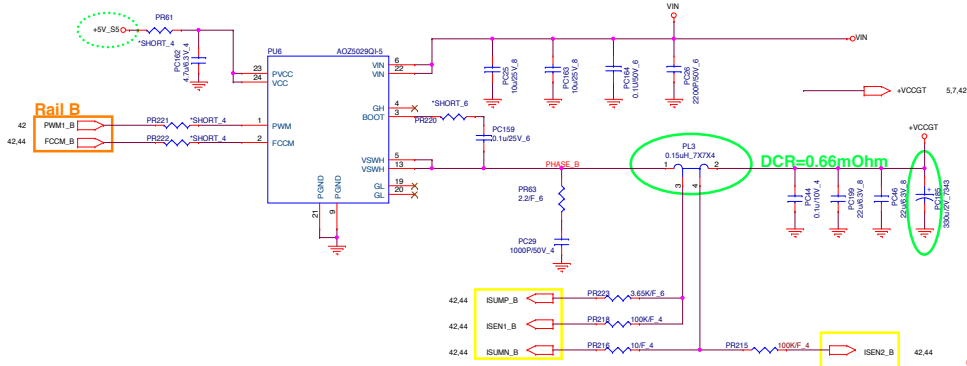
VCORE-3 phase



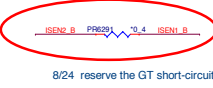
Vcore
 Icc TDC PL2 : 56A
 Icc Max : 68A
 OCP : A
 Fsw : MHz
VCORE L/L :
 R_DC_LL : 1.8mV/A
 R_AC_LL : 1.8mV/A

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	VCORE (ISL9585SHRTZ-T)	1A	1A
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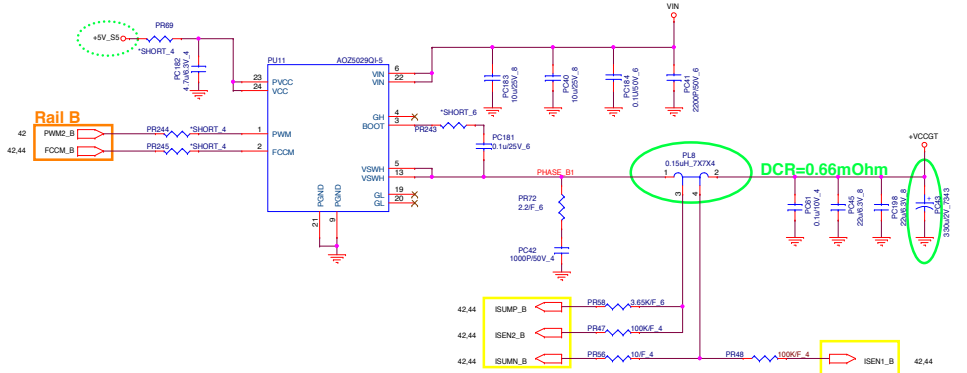
VCCGT-2 phase



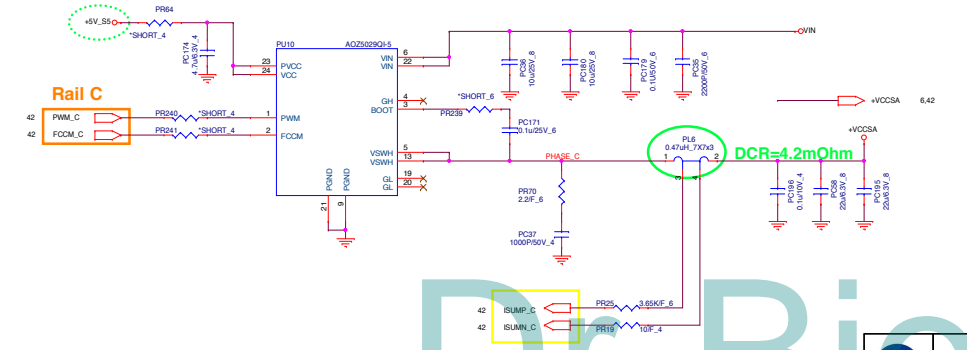
VCCGT
 Icc TDC PL2 : 39A
 Icc Max : 54A
 OCP : A
 Fsw : MHz
VCORE LL :
 R_DC_LL : 2.65mV/A
 R_AC_LL : 2.65mV/A



8/24 reserve the GT short-circuit

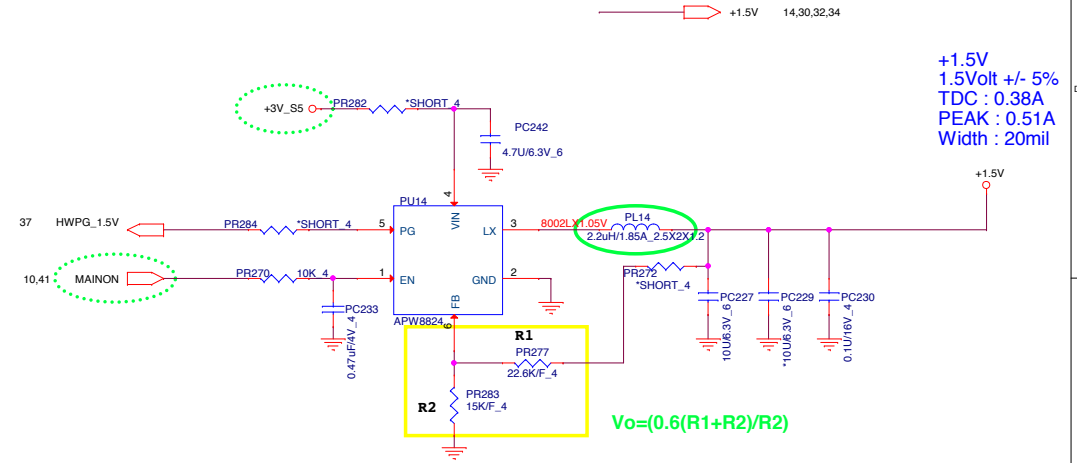


VCCSA-1 phase



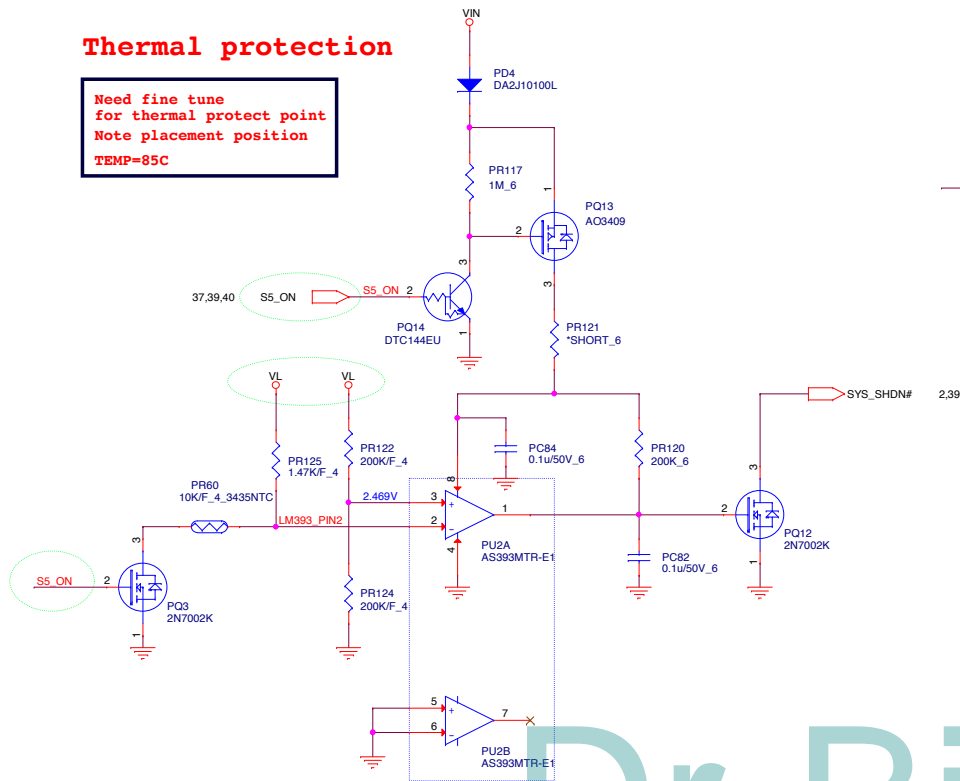
VCCSA
 Icc TDC PL2 : 10A
 Icc Max : 11A
 OCP : A
 Fsw : MHz
VCORE LL :
 R_DC_LL : 9.1mV/A
 R_AC_LL : 9.1mV/A

Remove 1.8V

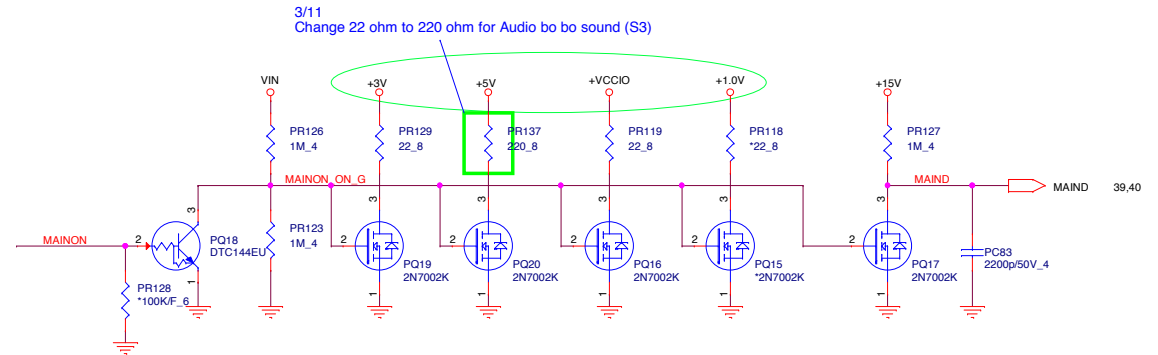


Thermal protection

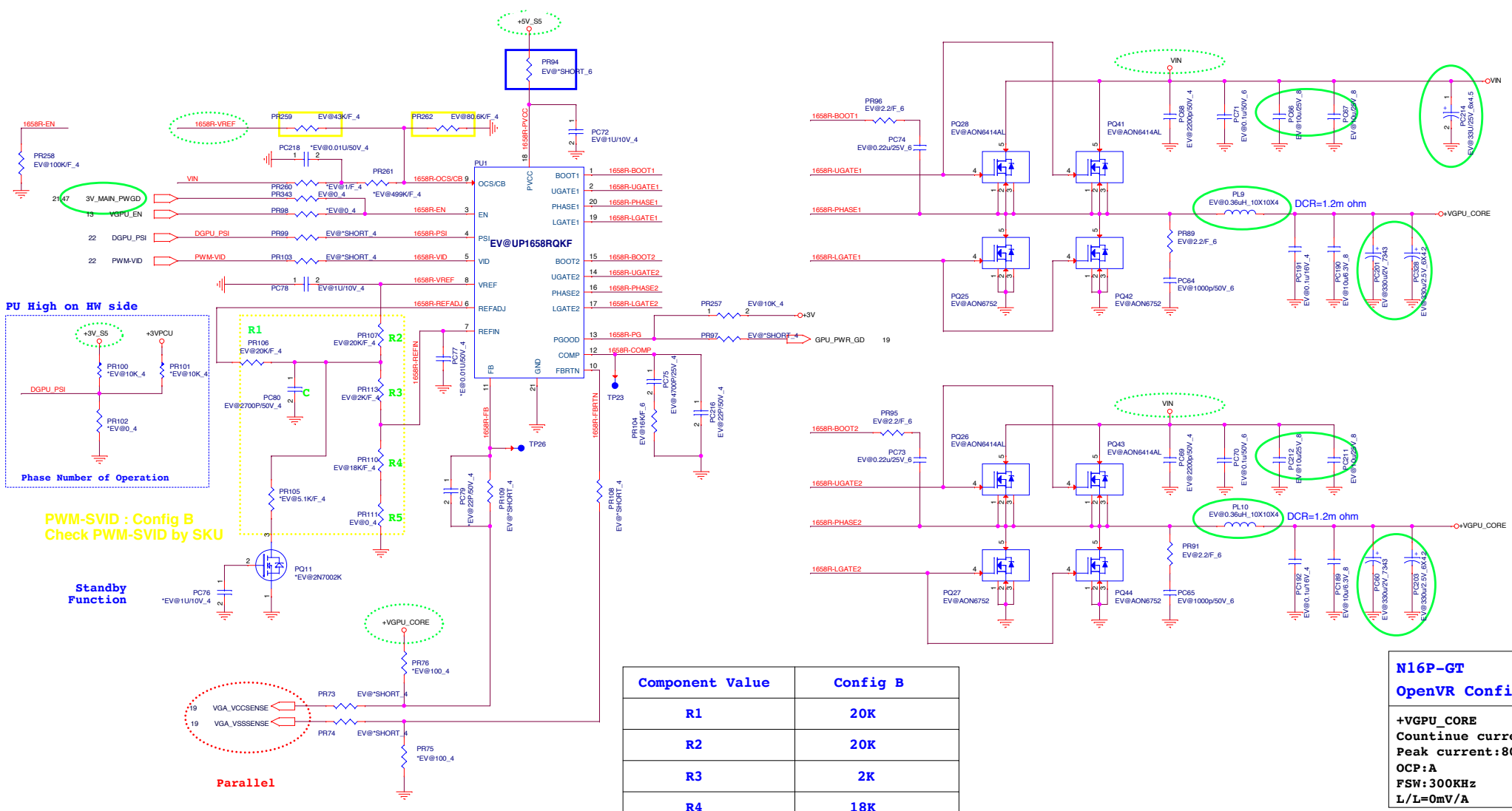
Need fine tune
for thermal protect point
Note placement position
TEMP=85C



For EC control thermal protection (output 3.3V)



3/11
Change 22 ohm to 220 ohm for Audio bo bo sound (S3)



PU High on HW side

Phase Number of Operation

PWM-SVID : Config B
Check PWM-SVID by SKU

Standby Function


Parallel

Component	Value	Config B
R1	20K	20K
R2	20K	20K
R3	2K	2K
R4	18K	18K
R5	0-ohm	0-ohm
C	2.7nF	2.7nF

N16P-GT
OpenVR Config:B

+VGPU_CORE
Continue current:42.2A
Peak current:80A
OCP:A
FSW:300KHz
L/L=0mV/A

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19,20,21 +1.05V_GFX
19,21,22,37 +3V_GFX

+1.05V_GFX
TDC : 1.57A
PEAK : 2.09A
Width : 80mil

$$V_o = 0.6 * (R1 + R2) / R2$$

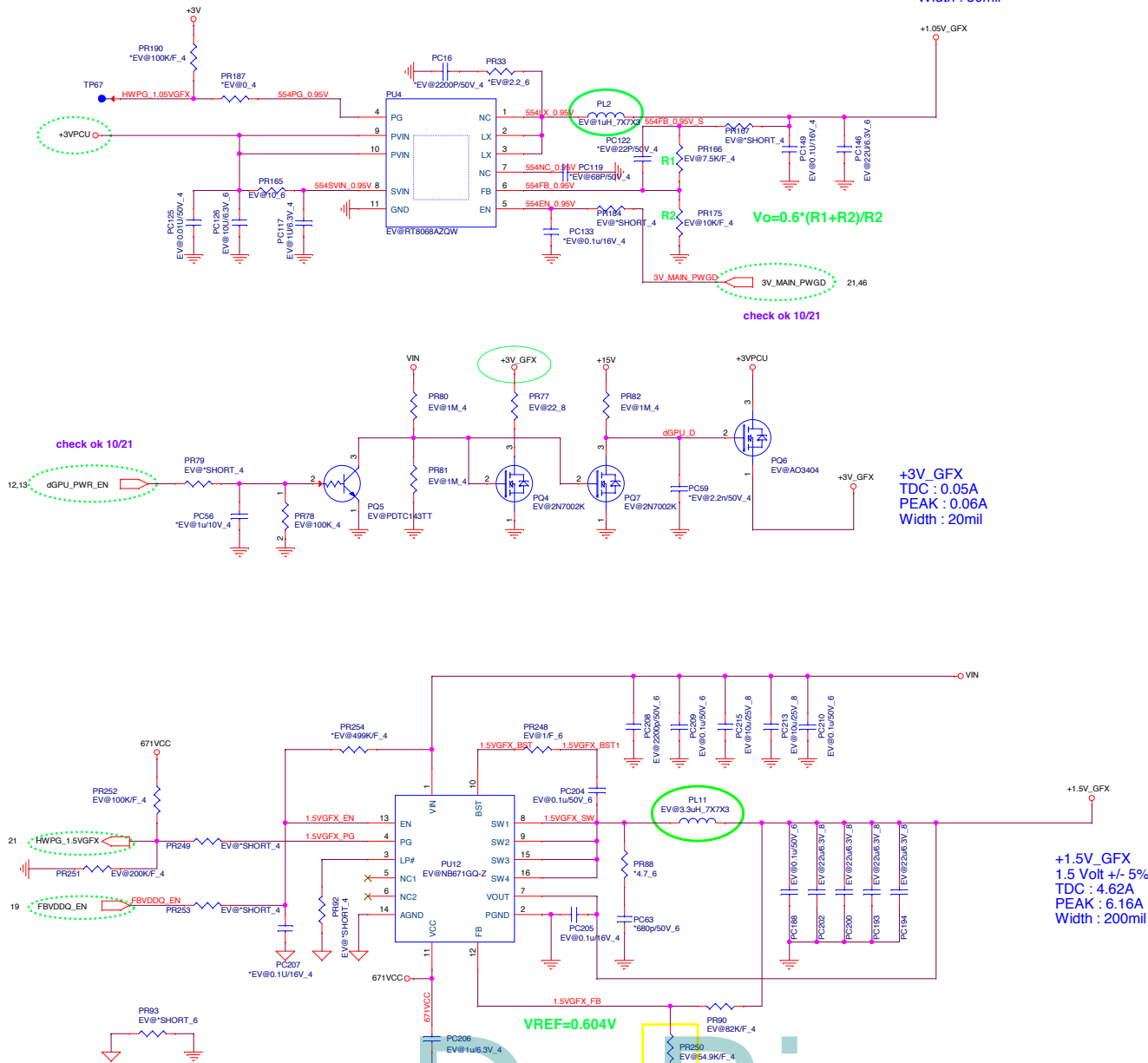
check ok 10/21

+3V_GFX
TDC : 0.05A
PEAK : 0.06A
Width : 20mil


check ok 10/21

+1.5V_GFX
1.5 Volt +/- 5%
TDC : 4.62A
PEAK : 6.16A
Width : 200mil

$$VREF = 0.604V$$



Model	Date	CHANGE LIST
A		1. FIRST RELEASED
	B	1. L23,L24 change to correct footprint 0402. 2. Correct CN14 UART from 3V to 5V. (Page13) 3. Nostuff R270,R271,and stuff R268,R2699,D31,D32 for DDC HDMI 7-13 issue. (Page30) 4. Nostuff U22,C441,R200,and stuff R182. (Page2) 5. Chagne HDA power to +3V R296,unstuff R247. (Page14) 6. Chagne Code DVDD-IO to +3V R370 ,unstuff R366. (Page32) 7. Add R204 and unstuff R178 for VCCST_PWRGD. (Page02) 8. Change R424,R431 to 62ohm for Audio EA. (Page32) 9. Unstuff R207 and stuff R208 for DMIC. (Page32) 10. Stuff 50ohm for CATERR#. (Page2) 11. Unstuff R132,R133,R576 for CPU_OPC_COMP. (Page6) 12. Reserve U54,U55,U56 and add R970,R971,R972. (Page10) 13. Add U53,C812 for VCCST_PWRGD timing issue. (Page2)
		C

 PROJECT ZRY Quanta Computer Inc.	DOC NO.	PROJECT MODEL : ZRY	APPROVED BY:	DATE:
		Part Number Change list	PART NUMBER:	DRAWING BY:
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Dr-Bios.com

Model Date **CHANGE LIST**

C2	<p>37. PR56 and PR216 change from 1ohm to 10ohm , it is fix black screen issue.</p> <p>38. Shortpad 0402: R202, R553, R127, R142, R144, R151, R156, R123, R243, R233, R631, R691, R223, R635, R658, R628, R458, R324, R276, R724, R246, R296, R592, R593, R455, R456, R13, R234, R435, R417, R377, R370, R952, R953, R163, R165, R958, R959, R598, R601, R602, R604, R949, R950, R960, R954, R955, R956, R792, R821</p> <p>39. Shortpad 0603: R754, R244, R245, R216, R256, R796, R219, R321, R218, R260, R314, R793, R277, R222, R217, R303, R302, R257, R220, R753, R328, R330, R259, R221, R297, R752, R109, R474, R14, R445, R810, R805, R824, R825, R396, R367, R368, L22, R429, R430</p> <p>40. Shortpad 0805: R25, R16, R17, R164, R214, R310, R951, R610, R948</p> <p>41. Reserve PR6291 for ISEN2_B and ISEN1B the GT short circuit. (page44)</p> <p>42. Change USB3 Tx and Rx signal from port1 to port6, it is fix crystal issue. (page9)</p> <p>43. Follow the change list 42, R991 change to NC and R990 connect to +3V_DEEP_SUS. (page13)</p> <p>44. PR229 and PR232 change from 10kohm to 11.3kohm for VR thermal alert follow ZRW setting 110 degree.</p> <p>45. PR125 change from 1.2kohm to 1.47kohm for h/w shut down sensor setting 85 degree.</p> <p>46. PR56 and PR216 change from 10ohm to 1ohm. Its short turn solution no run to next C2 stage (page44)</p>
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MV	<p>1. Shortpad 0402: R565 , R115 , R340 , R619 , R351 , R623 , R707 , R8 , R663 , R177 , R379 , R392 , R397 , R331 , R329 , R348 , R400 , R389 , R343 , R341 , R412 , R394 , R338 , R387</p> <p>2. Shortpad 0603: R369</p> <p>3. Remove R460 , R457 for touch panel (page29)</p> <p>4. Unstuff SW2 for cost down (page37)</p> <p>5. Reserve TPM U44 (page33) and G sensor U10 (page35)</p> <p>6. PR19 , PR21, PR31 , PR26 , PR216 , PR56 change from 1ohm to 10ohm for balck screen issue (pag43-44)</p> <p>7. R769 change from 100K to 10K follow TP issue</p> <p>8. U41.A36 and U41.A37 connect with GND, The reason to GND these pins is to minimize risk from ESD/EMI</p>
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	PROJECT :ZRY Quanta Computer Inc.		DOC NO.	PROJECT MODEL : ZRY	APPROVED BY:	DATE:
	Date: Tuesday, September 08, 2015	Change list		PART NUMBER:	DRAWING BY:	REVISION: