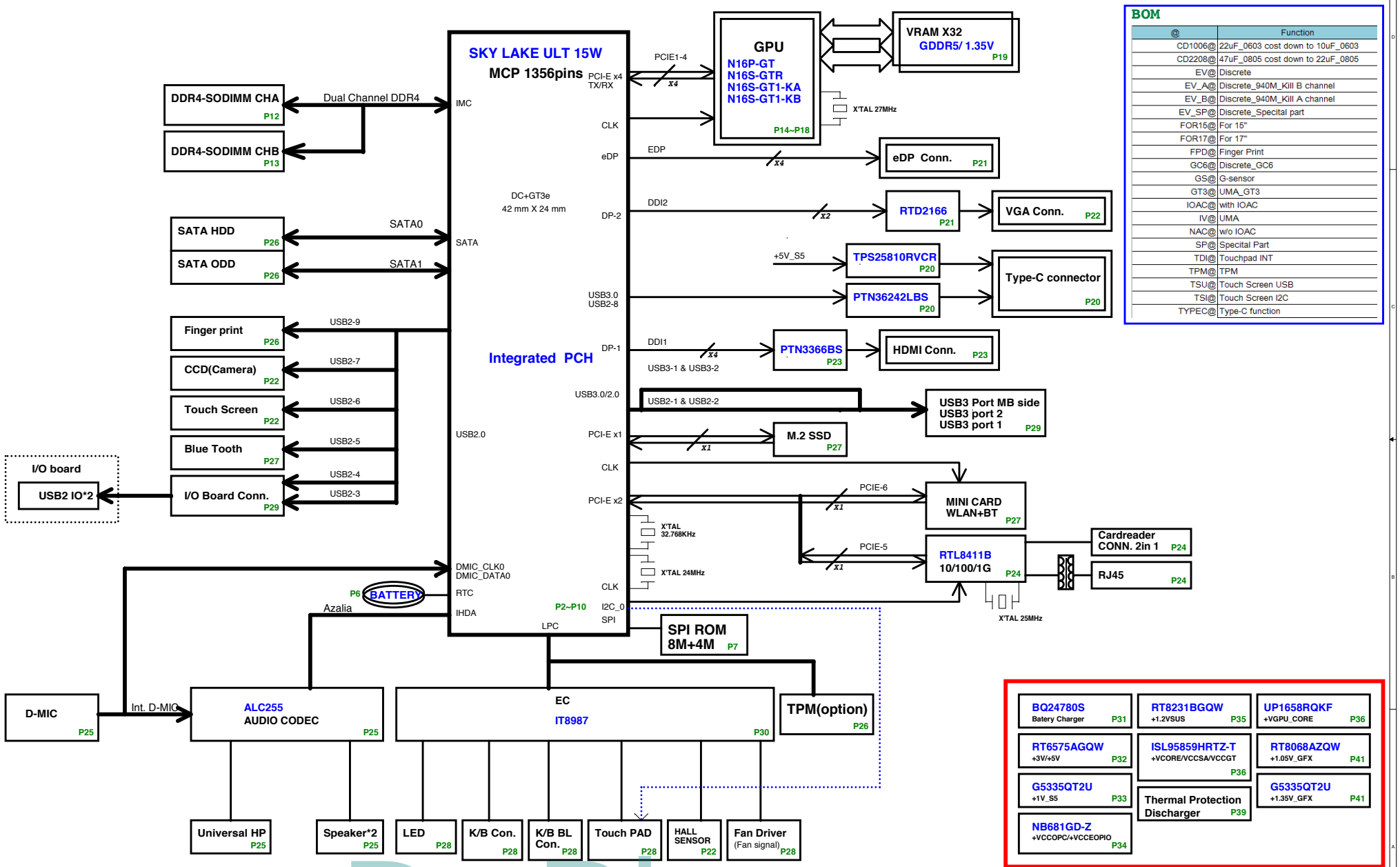
ZAAA Serials SkyLake-U SYSTEM BLOCK DIAGRAM

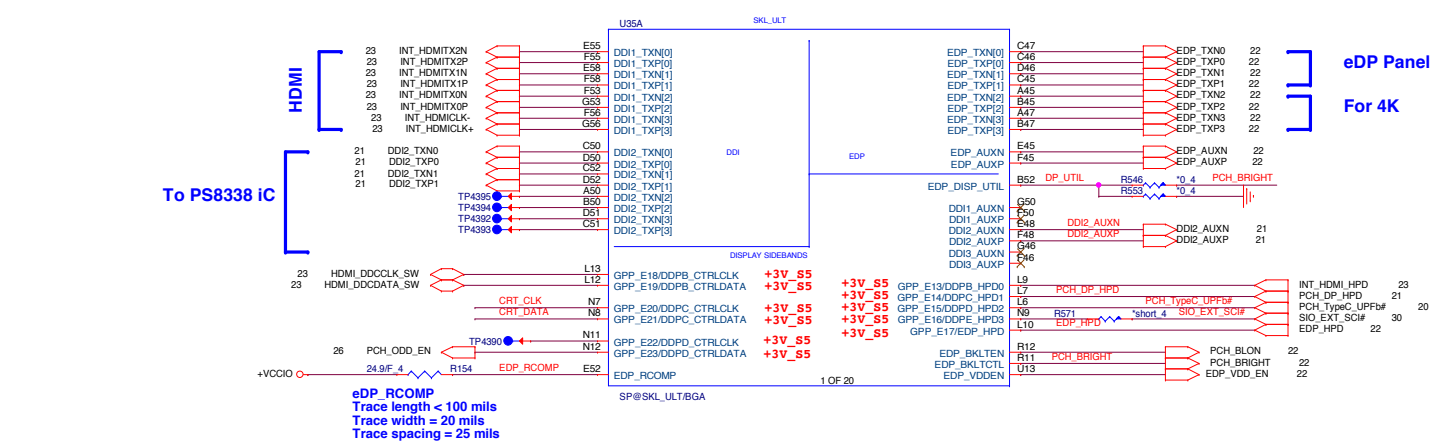


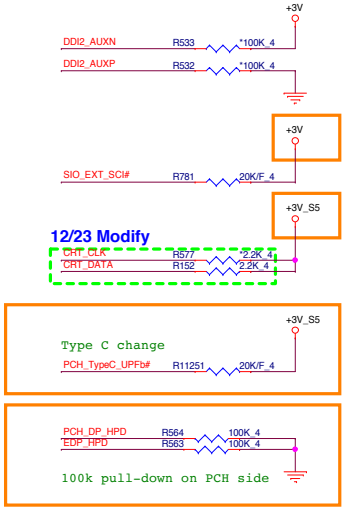
BOM

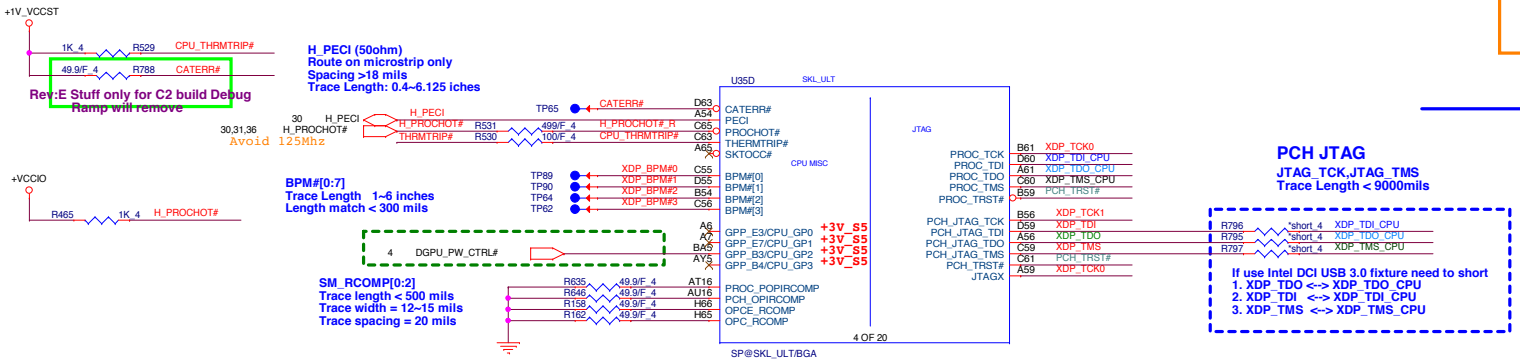
@	Function
CD1006@	22uF_0603 cost down to 10uF_0603
CD2208@	47uF_0805 cost down to 22uF_0805
EV@	Discrete
EV_A@	Discrete_940M_Kill B channel
EV_B@	Discrete_940M_Kill A channel
EV_SP@	Discrete_Specital part
FOR15@	For 15"
FOR17@	For 17"
FPD@	Finger Print
GC6@	Discrete_GC6
GS@	G-sensor
GT3@	UMA_GT3
IOAC@	with IOAC
IV@	UMA
NAC@	w/o IOAC
SP@	Specital Part
TDI@	Touchpad INT
TPM@	TPM
TSU@	Touch Screen USB
TSI@	Touch Screen I2C
TYPEC@	Type-C function

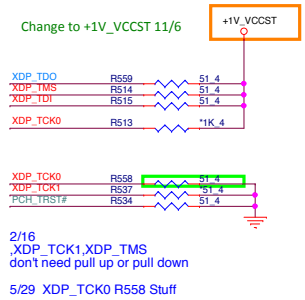
Quanta Computer Inc.
PROJECT : ZAA
Size | Document Number | Rev 1A
Block Diagram
Date: Monday, March 28, 2016 | Sheet 1 of 48

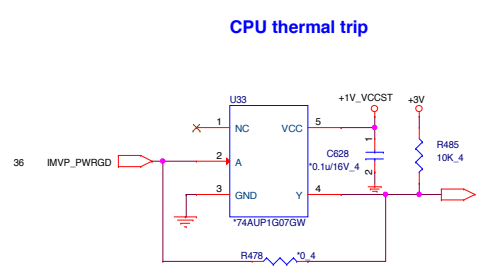
Skylake ULT (DISPLAY,eDP)

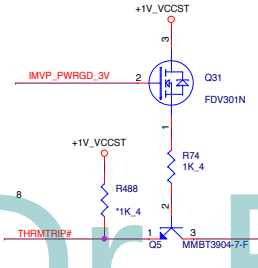


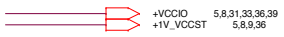








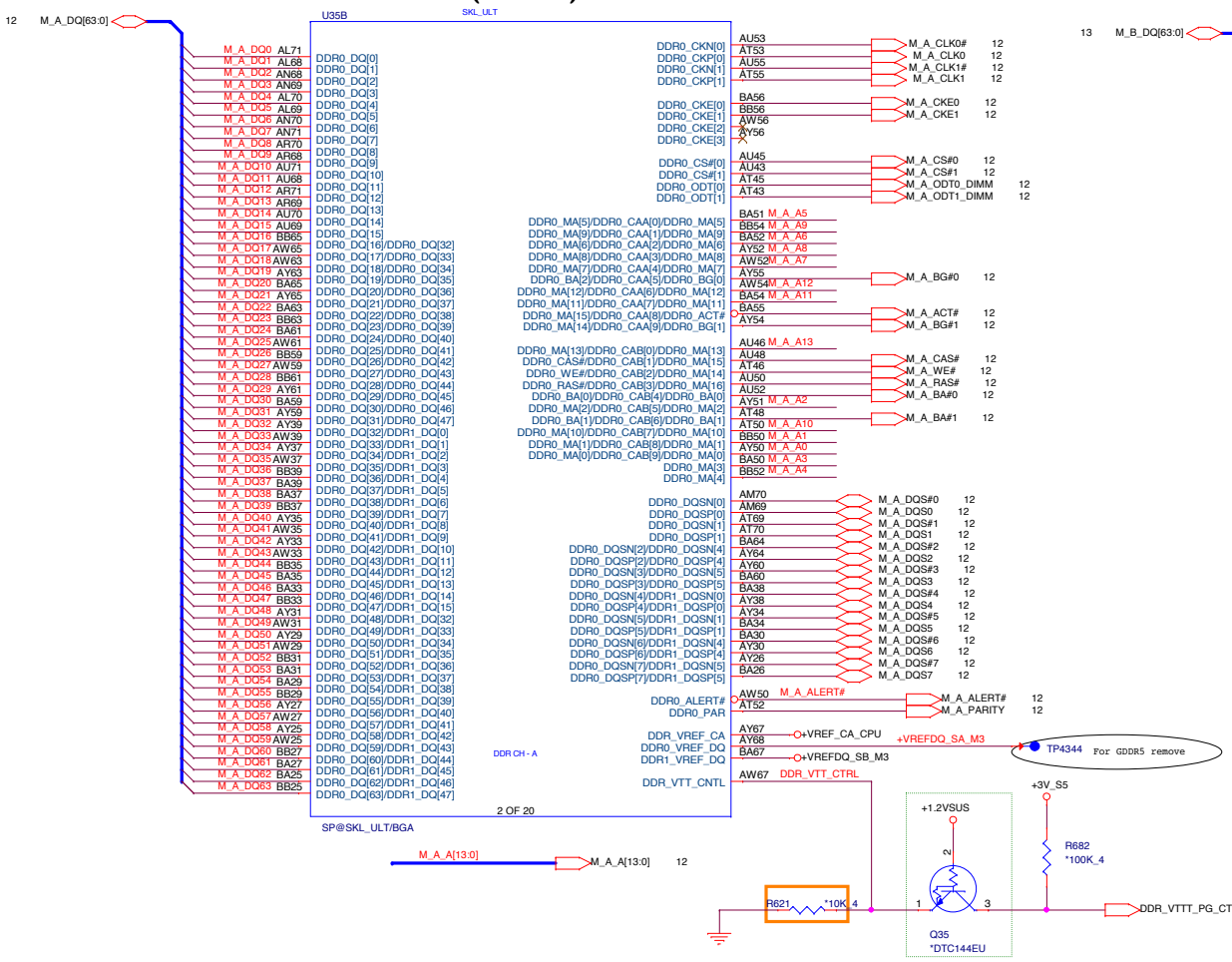




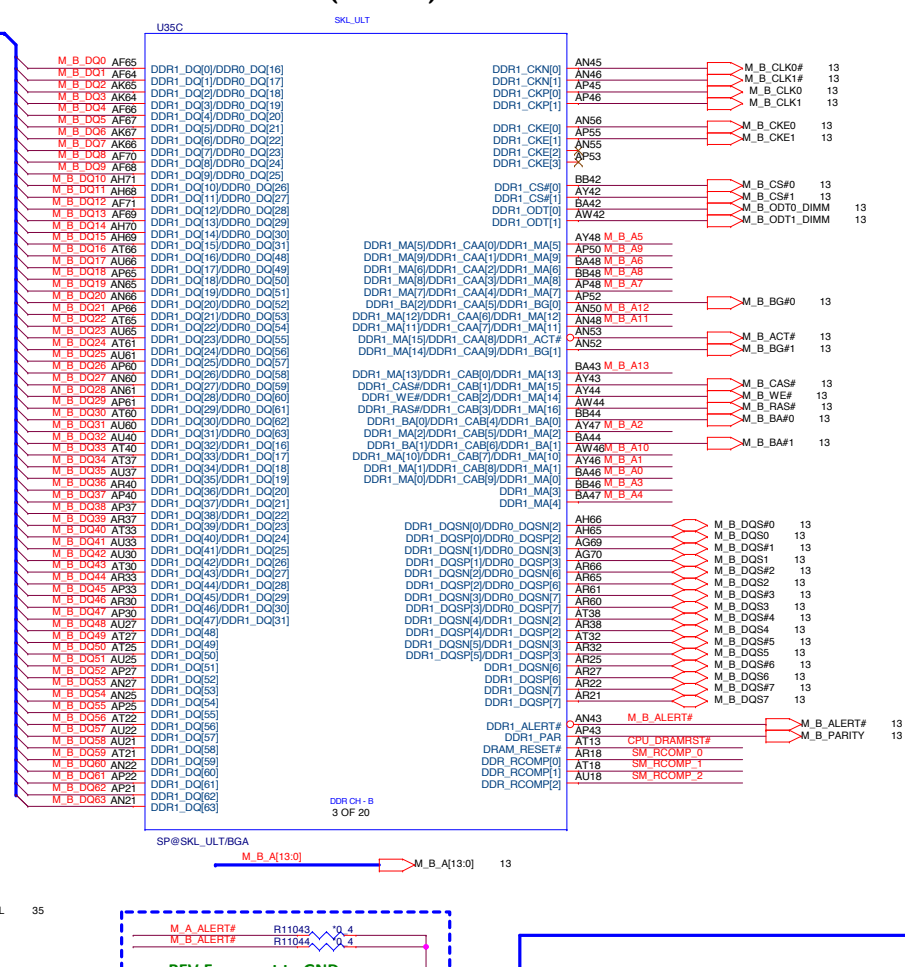
Quanta Computer Inc.			
PROJECT : ZAA			
Size	Document Number		Rev
	Skylake 1/4 (DDI/eDP)		1A
Date: Monday, March 28, 2016	Sheet 2	of 48	

Change Data and DQS to interleave.

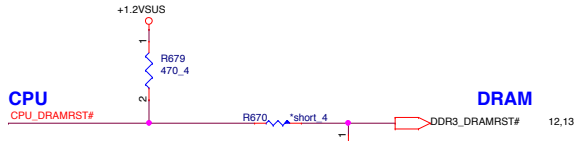
SKL ULT (DDR3L)



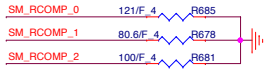
SKL ULT (DDR3L)



DRAMRST

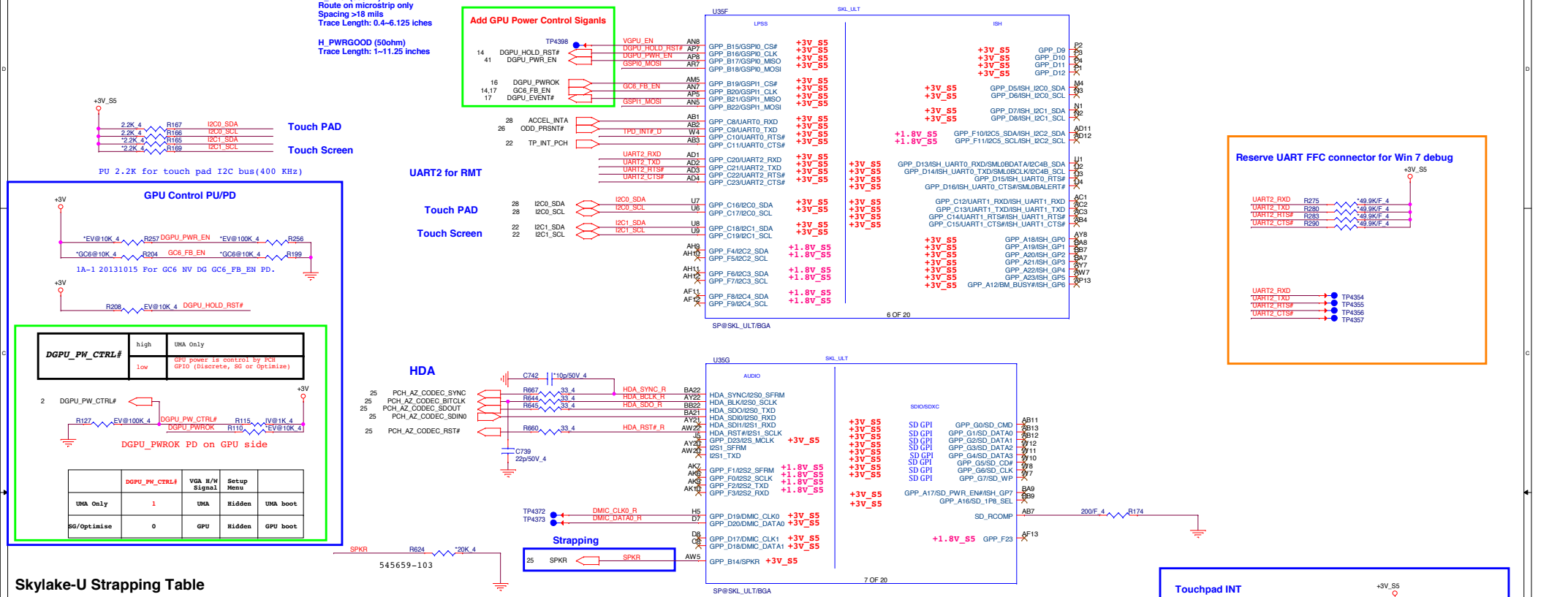


DRAM COMP



Quanta Computer Inc.		
PROJECT : ZAA		
Size	Document Number: Skylake 2/3 (DDR3 I/F)	Rev 1A
Date: Monday, March 28, 2016	Sheet 3 of 48	

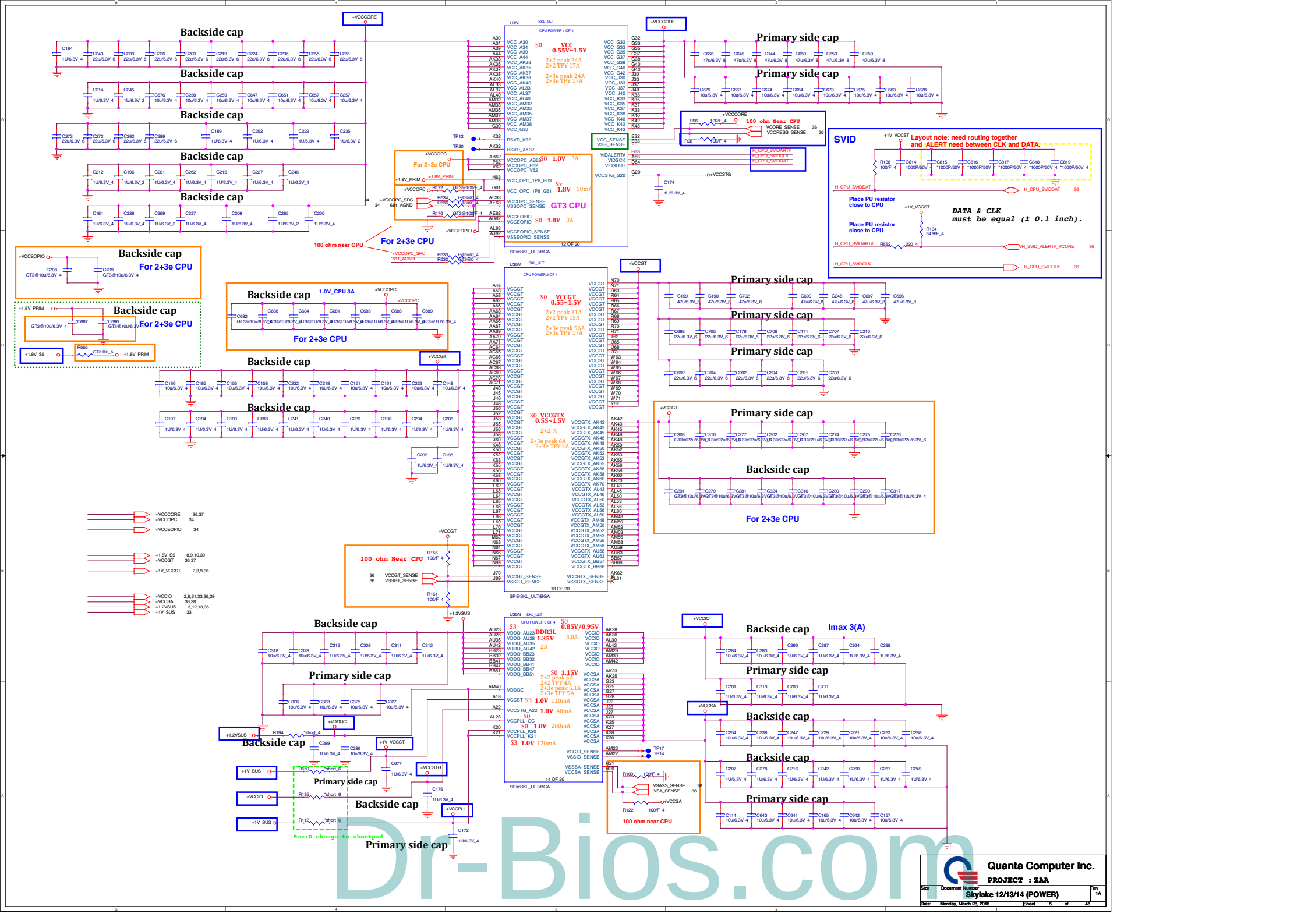
SKL ULT (SIDEBAND) GPIO



Skylake-U Strapping Table

Pin Name	Strap description	Sampled	Configuration	note
GPP_B14 (SPKR)	Top-Block Swap override	PCH_PWROK	0 = *Disable Top Swap (iPD 20K) 1 = Enable Top Swap Mode	
GPP_B18 (GSPI0_MOSI)	No reboot	PCH_PWROK	0 = *Disable No Reboot (iPD 20K) 1 = Enable No Reboot Mode	
GPP_C2 (SMBALERT#)	TLS Confidentiality	RSMRST#	0 = *Disable Intel ME Cryp to TLS(iPD 20K) 1 = Enable Intel ME Cryp to TLS	
GPP_B22 (GSPI1_MOSI)	Boot BIOS Strap Bit (BBS)	PCH_PWROK	0 = *SPI (iPD 20K) 1 = LPC	
GPP_C5 (SML0ALERT#)	eSPI or LPC	RSMRST#	0 = *LPC is selected for EC (iPD 20K) 1 = eSPI selected for EC	
SPI0_MOSI	Reserved	RSMRST#	(iPU 15 ~ 40K)	
SPI0_MISO	Reserved	RSMRST#	(iPU 15 ~ 40K)	
GPP_B23 (SML1ALERT# /PCHHOT#)	Reserved	RSMRST#	(iPD 20K)	
SPI0_IO2	Reserved	RSMRST#	(iPU 15 ~ 40K)	
SPI0_IO3	Reserved	RSMRST#	(iPU 15 ~ 40K)	
HDA_SDO / I2S_TXD0	Flash Descriptor Security Override / Intel ME Debug Mode	PCH_PWROK	0 = *Enable security in the Flash Description (iPD 20K) 1 = Disable Flash Descriptor Security (Override)	change location to near CPU to prevent impact HDA_SDO signal
GPP_E19 (DDPB_CTRLDATA)	Display Port B Detected	PCH_PWROK	0 = *Port B is not detected (iPD 20K) 1 =Port B is detected	
GPP_E21 (DDPC_CTRLDATA)	Display Port C Detected	PCH_PWROK	0 = *Port C is not detected (iPD 20K) 1 =Port C is detected	

Quanta Computer Inc.
PROJECT : ZAA
Size | Document Number: Skylake 6/7 (PEG/DMI/FDI) | Rev 1A
Date: Monday, March 28, 2016 | Sheet 4 of 48


Backside cap
Primary side cap
For 2+3e CPU
GT3 CPU
SVID
Layout note: need routing together and ALERT need between CLK and DATA.
DATA & CLK must be equal (± 0.1 inch).
Place PU resistor close to CPU
100 ohm Near CPU
Imax 3(A)
Rev:D change to shortpad
Quanta Computer Inc.
PROJECT : ZAA
Skylake 12/13/14 (POWER)
Monday, March 28, 2016
Dr-Bios.com

Skylake ULT (GPU, SATA , ODD, CLK ,USB2&3)

+3V 2,4,7,8,9,12,13,14,16,21,22,23,24,25,26,27,28,30,32,33,34,35,36,39,40,41
+3V_S5 2,3,4,7,8,9,11,20,24,26,27,28,30,32,34,35,40
+3VPCU 9,11,22,24,25,26,27,28,30,31,32,39,40,41
+3V_RTC 8,9,30
+1V_S5 9,33

U35H SKL_ULT

PCIE/USB3/SATA

dGPU PEG*4
14 PEG_RX#0 14 PEG_RX0 14 PEG_TX#0 14 PEG_TX0 — C653 EV@0.22u/10V_4 C_PEG_TX#0 — C652 EV@0.22u/10V_4 C_PEG_TX0 — H13 G13 B17 A17
14 PEG_RX#1 14 PEG_RX1 14 PEG_TX#1 14 PEG_TX1 — C656 EV@0.22u/10V_4 C_PEG_TX#1 — C655 EV@0.22u/10V_4 C_PEG_TX1 — G11 F11 D16 C16
14 PEG_RX#2 14 PEG_RX2 14 PEG_TX#2 14 PEG_TX2 — C661 EV@0.22u/10V_4 C_PEG_TX#2 — C662 EV@0.22u/10V_4 C_PEG_TX2 — H16 G16 D17 C17
14 PEG_RX#3 14 PEG_RX3 14 PEG_TX#3 14 PEG_TX3 — C654 EV@0.22u/10V_4 C_PEG_TX#3 — C660 EV@0.22u/10V_4 C_PEG_TX3 — G15 F15 B19 A19

PCIE1_RXN/USB3_5_RXN
PCIE1_RXP/USB3_5_RXP
PCIE1_TXN/USB3_5_TXN
PCIE1_TXP/USB3_5_TXP
PCIE2_RXN/USB3_6_RXN
PCIE2_RXP/USB3_6_RXP
PCIE2_TXN/USB3_6_TXN
PCIE2_TXP/USB3_6_TXP
PCIE3_RXN
PCIE3_RXP
PCIE3_TXN
PCIE3_TXP
PCIE4_RXN
PCIE4_RXP
PCIE4_TXN
PCIE4_TXP

For Thunderbolt
F16 E16 C19 D19 — PCIE5_RXN PCIE5_RXP PCIE5_TXN PCIE5_TXP
G18 F18 D20 C20 — PCIE6_RXN PCIE6_RXP PCIE6_TXN PCIE6_TXP

HDD
26 SATA_RXN0 26 SATA_RXP0 26 SATA_TXN0 26 SATA_TXP0 — F20 E20 B21 A21
PCIE7_RXN/SATA0_RXN
PCIE7_RXP/SATA0_RXP
PCIE7_TXN/SATA0_TXN
PCIE7_TXP/SATA0_TXP

ODD
26 SATA_RXN1 26 SATA_RXP1 26 SATA_TXN1 26 SATA_TXP1 — G21 F21 D21 C21
PCIE8_RXN/SATA1A_RXN
PCIE8_RXP/SATA1A_RXP
PCIE8_TXN/SATA1A_TXN
PCIE8_TXP/SATA1A_TXP

LAN
24 PCIE_RX5- 24 PCIE_RX5+_LAN 24 PCIE_TX5- 24 PCIE_TX5+_LAN — C668 0.1u/16V_4 PCIE_TX5- — C669 0.1u/16V_4 PCIE_TX5+ — E22 E23 B23 A23
PCIE9_RXN
PCIE9_RXP
PCIE9_TXN
PCIE9_TXP

WIFI
27 PCIE_RX6-_WLAN 27 PCIE_RX6+_WLAN 27 PCIE_TX6-_WLAN 27 PCIE_TX6+_WLAN — C648 0.1u/16V_4 PCIE_TX6- — C649 0.1u/16V_4 PCIE_TX6+ — F25 E25 D23 C23
PCIE10_RXN
PCIE10_RXP
PCIE10_TXN
PCIE10_TXP

R562 100/F_4 PCIE_RCOMPN PCIE_RCOMPP — E5
PCIE_RCOMPN
PCIE_RCOMPP

TP91 XDP_PRDY# — D56
TP92 XDP_PREQ# — D61
PIRQA# — BB11
PROC_PRDY#
PROC_PREQ#
GPP_A7/PIRQA# +3V_S5

For M.2 SSD -NA
For M.2 SSD -1
27 SATA_RXN3/PEG_RXN9_L0 27 SATA_RXP3/PEG_RXP9_L0 27 SATA_TXN3/PEG_TXN9_L0 27 SATA_TXP3/PEG_TXP9_L0 27 SATA_RXN3/PEG_RXN10_L1 27 SATA_RXP3/PEG_RXP10_L1 27 SATA_TXN3/PEG_TXN10_L1 27 SATA_TXP3/PEG_TXP10_L1 — E28 E27 D24 C24 E30 F30 A25 B25
PCIE11_RXN/SATA1B_RXN
PCIE11_RXP/SATA1B_RXP
PCIE11_TXN/SATA1B_TXN
PCIE11_TXP/SATA1B_TXP
PCIE12_RXN/SATA2_RXN
PCIE12_RXP/SATA2_RXP
PCIE12_TXN/SATA2_TXN
PCIE12_TXP/SATA2_TXP

8 OF 20
SP@SKL_ULT/BGA

SSIC / USB3

USB3_1_RXN H8 — USB3_RXN0 29
USB3_1_RXP G8 — USB3_RXP0 29
USB3_1_TXN C13 — USB3_TXN0 29
USB3_1_TXP D13 — USB3_TXP0 29
MB USB3.0 (Charger IC)

USB3_2_RXN/SSIC_1_RXN J6 — USB3_RXN1 29
USB3_2_RXP/SSIC_1_RXP H6 — USB3_RXP1 29
USB3_2_TXN/SSIC_1_TXN B13 — USB3_TXN1 29
USB3_2_TXP/SSIC_1_TXP A13 — USB3_TXP1 29
MB USB3.0

USB3_3_RXN/SSIC_2_RXN J10 — USB3_RXN2 20
USB3_3_RXP/SSIC_2_RXP H10 — USB3_RXP2 20
USB3_3_TXN/SSIC_2_TXN B15 — USB3_TXN2 20
USB3_3_TXP/SSIC_2_TXP A15 — USB3_TXP2 20
For TYPE-C

USB3_4_RXN E10 — USB3_RXN3 20
USB3_4_RXP F10 — USB3_RXP3 20
USB3_4_TXN C15 — USB3_TXN3 20
USB3_4_TXP D15 — USB3_TXP3 20

USB2

USB2N_1 USB2P_1 AB9 AB10 — USBP0- 29 USBP0+ 29
MB USB3.0 (Charger IC)

USB2N_2 USB2P_2 AD6 AD7 — USBP1- 29 USBP1+ 29
MB USB3.0

USB2N_3 USB2P_3 AH3 AJ3 — USBP2- 29 USBP2+ 29
DB USB2.0

USB2N_4 USB2P_4 AD9 AD10 — USBP3- 29 USBP3+ 29
For 17" DB use

USB2N_5 USB2P_5 AJ1 AJ2 — USBP4- 27 USBP4+ 27
BT

USB2N_6 USB2P_6 AF6 AF7 — USBP5- 22 USBP5+ 22
Touch Screen

USB2N_7 USB2P_7 AH1 AH2 — USBP6- 22 USBP6+ 22
CCD

USB2N_8 USB2P_8 AF8 AF9 — USBP7- 20 USBP7+ 20
For TYPE-C

USB2N_9 USB2P_9 AG1 AG2 — USBP8- 26 USBP8+ 26
POA

USB2N_10 USB2P_10 AH7 AH8 — TP4377 TP4378

USB2_COMP AB6 — USBCOMP — R178 113/F_4
USB2_ID AG3 — USB2_ID — R587 1K_4
USB2_VBUSSENSE AG4 — R778 1K_4
USBCOMP
Impedance = 50 ohm
Trace length < 500 mils
Trace spacing = 15 mils

+3V_S5 GPP_E9/USB2_OC0# A9 — USB_OC0# — USB_OC0# 29
+3V_S5 GPP_E10/USB2_OC1# C9 — USB_OC1# — USB_OC1# 29
+3V_S5 GPP_E11/USB2_OC2# D9 — USB_OC2# — USB_OC2# 29
+3V_S5 GPP_E12/USB2_OC3# B9 — USB_OC3# — USB_OC3# 20
MB U3
MB U3
DB U2
TYPE C

+3V_S5 GPP_E4/DEVSLP0 J1 — SATA_DEVSLP0 — DEVSLP0 26
+3V_S5 GPP_E5/DEVSLP1 J2 — SATA_DEVSLP1
+3V_S5 GPP_E6/DEVSLP2 J3 — SATA_DEVSLP2 — DEVSLP2 27

+3V_S5 GPP_E0/SATAXPCIE0/SATAGP0 H2 — SATAGP0
+3V_S5 GPP_E1/SATAXPCIE1/SATAGP1 H3 — SATAGP1
+3V_S5 GPP_E2/SATAXPCIE2/SATAGP2 G4 — NGFF_SATA_DET 27
+3V_S5 GPP_E8/SATALED# H1

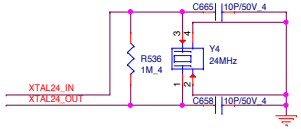
PCH PU/PD

+3V_S5
USB_OC0# R541 10K_4
USB_OC1# R540 10K_4
USB_OC2# R543 10K_4
USB_OC3# R542 10K_4

+3V
SATA_DEVSLP0 R573 *10K_4
SATA_DEVSLP1 R574 10K_4
SATA_DEVSLP2 R575 10K_4
PIRQA# R631 *10K_4
SATAGP1 R569 *10K_4

Add SSD ID 1/14
Hight is SSD , Low is ODD
+3V_S5
26 SSD_ID — R568 10K_4 SATAGP0 R570 100K_4

Skylake-U userd 24 MHz (50 Ohm ESR) XTAL



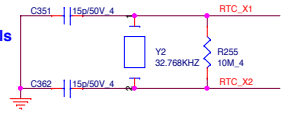
24MHz: BG624000078
38.4MHz : ?

Note: Change Y4 to 38.4 MHz(ESR 30 ohm) for Cannonlake U

RTC Clock 32.768KHz (RTC)

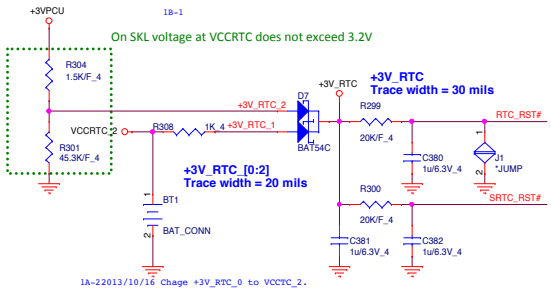
CH01006JB08 -> 10p
CH01506JB06 -> 15p
CH-6806TB01 -> 6.8p

Trace length < 1000 mils



BG332768453 -> SEG
BG332768104 -> TXC
ZAAA 2nd BG332768111

RTC Circuitry (RTC)



1. AHL03003057 DBV CR2032
2. AHL03003003 VDE CR2032

U35J SKL_ULT

CLOCK SIGNALS

N16 VGA
14 CLK_PCIE_VGA# 14 CLK_PCIE_VGA 14 CLK_PEGA_REQ# — R235 *short_4 CLK_PCIE_REQ0# — D42 C42 AR10
Rev:D change to shortpad

M.2 SSD
27 NGFF_SSD_CLK# 27 NGFF_SSD_CLK 27 PCIE_CLKREQ_NGFF_SSD# — R111112 *short_4 NGFF_SSD_CLK#_C — R111113 *short_4 NGFF_SSD_CLK_C — R111111 *short_4 CLK_PCIE_REQ1# — B42 A42 AT7

For Thunderbolt
CLK_PCIE_REQ2# — D41 C41 AT8

TP22 CLK_PCIE_REQ3# — D40 C40 AT10

WLAN LAN
24 CLK_PCIE_LANN 24 CLK_PCIE_LANP 24 CLK_PCIE_LAN_REQ# — R229 *short_4 CLK_PCIE_REQ4# — B40 A40 AU8
27 CLK_PCIE_WLANN 27 CLK_PCIE_WLANP 27 PCIE_CLKREQ_WLAN# — R224 *short_4 CLK_PCIE_REQ5# — E40 E38 AU7
Rev:D change to shortpad

CLKOUT_PCIE_N0 CLKOUT_PCIE_P0 GPP_B5/SRCCLKREQ0# +3V_S5
CLKOUT_PCIE_N1 CLKOUT_PCIE_P1 GPP_B6/SRCCLKREQ1# +3V_S5
CLKOUT_PCIE_N2 CLKOUT_PCIE_P2 GPP_B7/SRCCLKREQ2# +3V_S5
CLKOUT_PCIE_N3 CLKOUT_PCIE_P3 GPP_B8/SRCCLKREQ3# +3V_S5
CLKOUT_PCIE_N4 CLKOUT_PCIE_P4 GPP_B9/SRCCLKREQ4# +3V_S5
CLKOUT_PCIE_N5 CLKOUT_PCIE_P5 GPP_B10/SRCCLKREQ5# +3V_S5

CLKOUT_ITPXDP_N F43 CLK_PCIE_XDPN — TP93
CLKOUT_ITPXDP_P E43 CLK_PCIE_XDPP — TP94
+3V_S5 GPD8/SUSCLK BA17 SUSCLK_R R11279 *0_4 SUSCLK 27
XTAL24_IN E37 XTAL24_IN
XTAL24_OUT E35 XTAL24_OUT
XCLK_BIASREF E42 XCLK_BIASREF R512 2.7K/F_4 +1V_S5
RTCX1 AM18 RTC_X1
RTCX2 AM20 RTC_X2
SRTCRST# AN18 SRTC_RST#
RTCRST# AM16 RTC_RST# — RTC_RST# 11

10 OF 20
SP@SKL_ULT/BGA

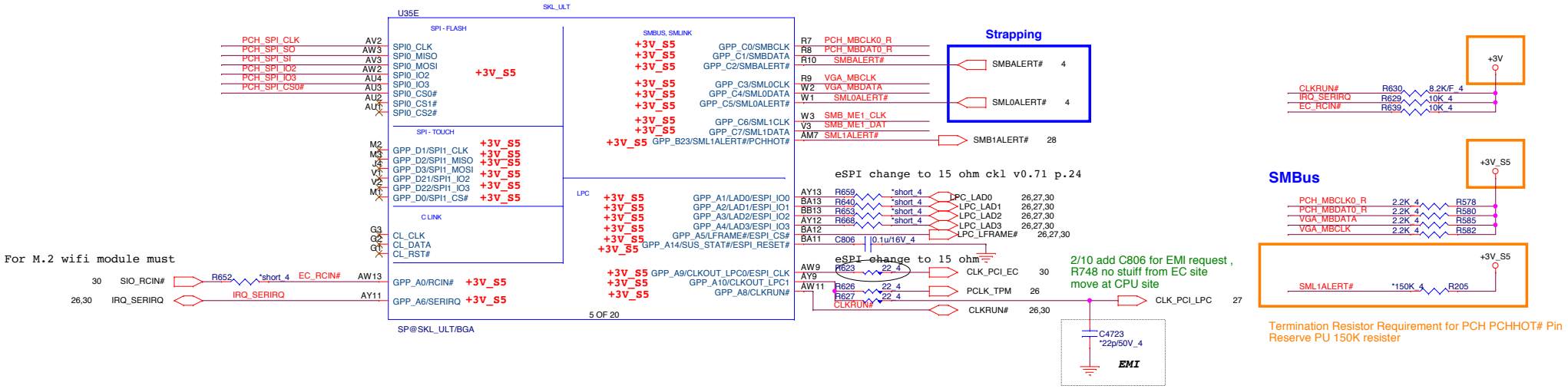
1V power plane
0.71 checklist p14

+3V
CLK_PCIE_REQ0# R234 EV@10K_4
CLK_PCIE_REQ1# R215 10K_4
CLK_PCIE_REQ2# R227 *10K_4
CLK_PCIE_REQ3# R618 *10K_4
CLK_PCIE_REQ4# R228 10K_4
CLK_PCIE_REQ5# R223 10K_4

Rev:D add for EC reset RTC

30 CLR_CMOS — CLR_CMOS — R786 100K_4 — Q6059 *2N7002K — SRTC_RST#
Rev:E Reserve only
CLR_CMOS — Q6060 2N7002K — RTC_RST#
Rev:E Reserve only

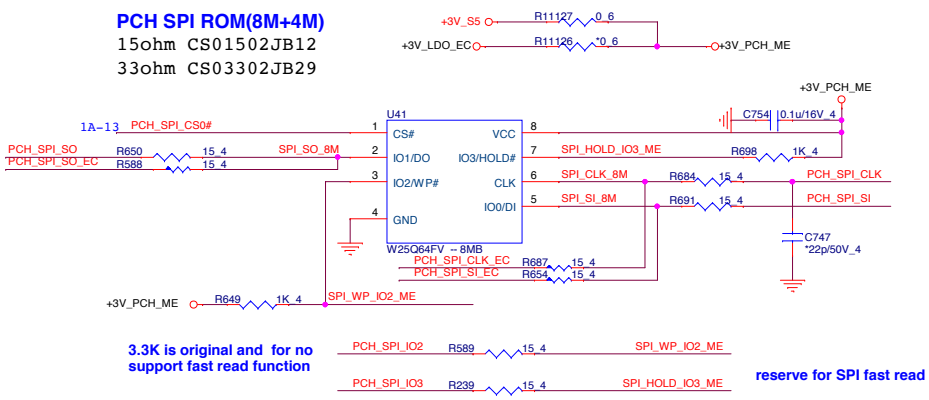
Quanta Computer Inc.
PROJECT : ZAA
Size | Document Number: Skylake 9/10 (PEG/USB/CLK) | Rev 1A
Date: Monday, March 28, 2016 | Sheet 6 of 48



SP@ socket P/N: DFHS08FS023 only for A-TEST

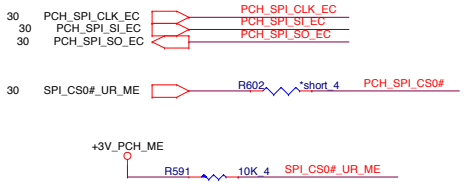
SPI ROM	Vender	Size	Quanta P/N	Vender P/N
Skylake 3.3V	WND	8M	AKE3EFP0N07	W25Q64FVSSIQ
	GGD	8M	AKE2EZN0Q00	GD25B64CSIGR

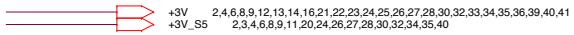
PCH SPI ROM(8M+4M)
15ohm CS01502JB12
33ohm CS03302JB29

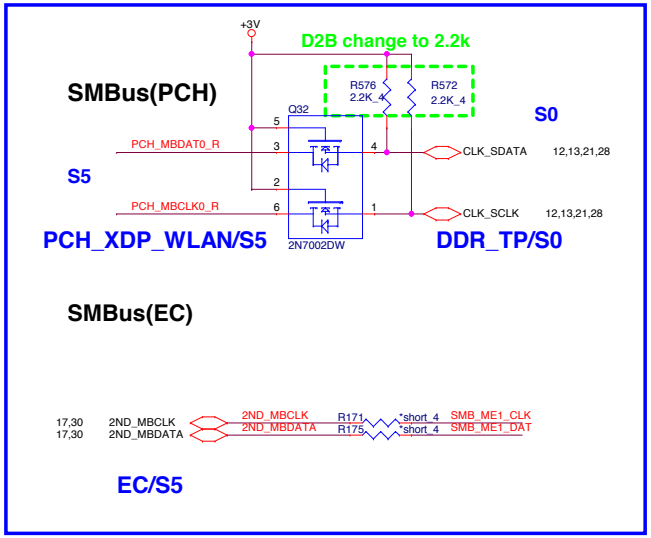


3.3K is original and for no support fast read function

reserve for SPI fast read







Quanta Computer Inc.
PROJECT : ZAA

Size	Document Number	Rev
	Skylake 5 (SATA/HDA/SPI)	1A
Date: Monday, March 28, 2016	Sheet 7 of 48	

11/12 Reserve PU 10K

EC only PD, so PD 10K

Rev:D change to shortpad

SKL_ULT

SYSTEM POWER MANAGEMENT

SP@SKL_ULT/BGA

12/23 Modify

Rev:F add

Board ID

	Low	High
BOARD_ID0	VRAM X32	VRAM X16
BOARD_ID1	Non IOAC	IOAC
BOARD_ID2	No G-sensor	G-sensor
BOARD_ID3	No TPM	TPM
BOARD_ID4	No touch panel	touch panel

	Low	High
BOARD_ID5	For 14"	For 15" & 17"
BOARD_ID6	Reserved	Reserve
BOARD_ID7	GPU--> KA	GPU--> KB GPU--> GTR GPU--> 950M

REV:E tPLT15(max 200us) ->SLP_S4# assertion to VDDQ(+1.35VSUS) ramp down start(SUSON)

REV:E tPLT17(max 200us) ->SLP_S3# assertion to IMVP VR_ON(VRON) deassertion

REV:E tPLT18(max 200 us) ->SLP_S3# assertion to VCCIO VR(MAIND for +1V_S5 to +VCCIO) disabled

Power Sequence

Non Deep Sx

Rev:D change to shortpad

For platforms not supporting Deep Sx, connect directly to RSMRST#

No Deep Sx Rev:D change to shortpad

VCCST PWRGD CRB is via +1.05V PG

B2A
S0->S5 & S0->S3
Power of sequence 1us
SUSB# -> VCCST_PWRGD

Shortpad change to 60.4 ohm. 11/6

Stuff 1000P/50V

Reserve 1000P/50V

PLTRST# Buffer

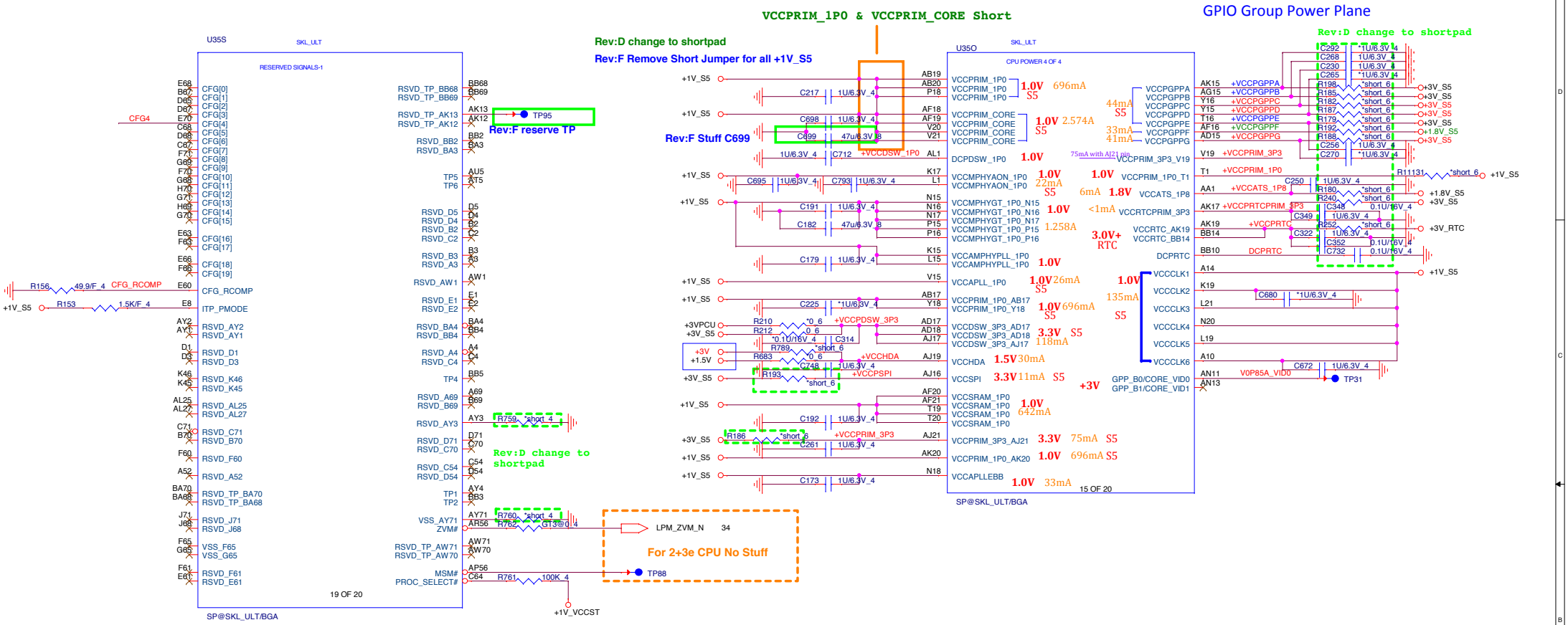
SYSPWOK

Rev:D change to shortpad

Quanta Computer Inc.

PROJECT : ZAA

Size	Document Number	Rev
	Skylake 9/11 (PWROK/Board_ID)	1A
Date: Monday, March 28, 2016	Sheet 8 of 48	



Pin Name	Strap description	Configuration	Note
CFG[0]	Stall reset sequence after PCU PLL lock until de-asserted	1 = *Normal Operation; No stall (iPU 3K) 0 = Stall	
CFG[1]	Reserved Configuration lane		
CFG[2]	PCI Express* Static x16 Lane Numbering Reversal	1 = *Normal Operation(iPU 3K) 0 = Lan number reversed	H & S processor used only
CFG[3]	Reserved Configuration lane		
CFG[4]	eDP enable	1 = Disabled (iPU 3K) 0 = *Enabled	
CFG[6:5]	PCI Express* Bifunction	00 = 1x8, 2x4 PCI Express* 01 = reserved 10 = 2x8 PCI Express* 11 = 1x16 PCI Express*	H & S processor used only
CFG[7]	PEG Training	1 = *PEG Train immediatedly follow RESET# de-assertion (iPU 3K) 0 = PEG wait for BIOS for training	H & S processor used only
CFG[19:8]	Reserved Configuration lane		

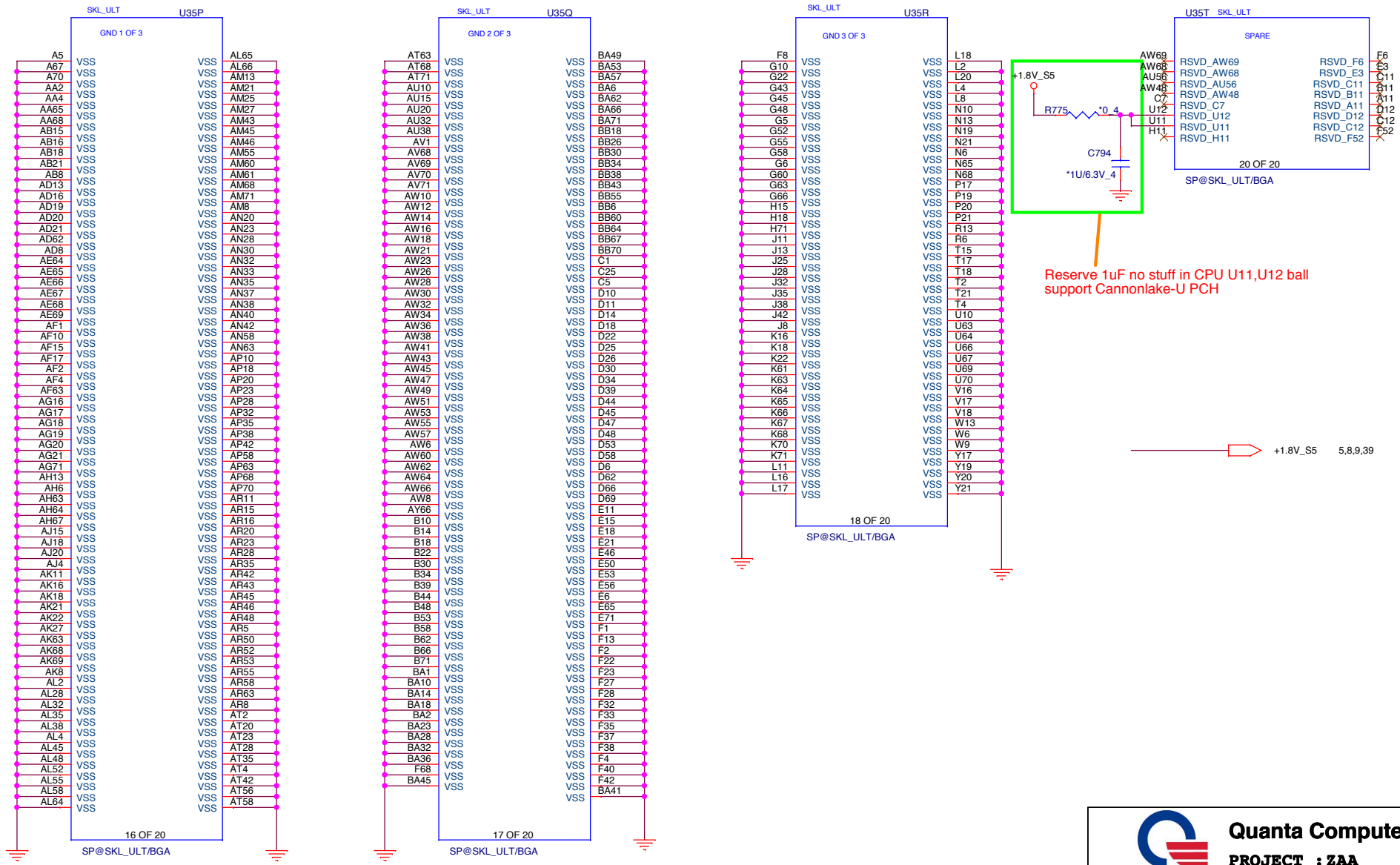
+1V_S5 6,33
+3VPCU 6,11,22,24,25,26,27,28,30,31,32,39,40,41
+3V_S5 2,3,4,6,7,8,11,20,24,26,27,28,30,32,34,35,40
+3V 2,4,6,7,8,12,13,14,16,21,22,23,24,25,26,27,28,30,32,33,34,35,36,39,40,41

+1V_VCCST 2,5,8,36
+1.8V_S5 5,8,10,39
+3V_RTC 6,8,30

Quanta Computer Inc.
PROJECT : ZAA

Size	Document Number	Rev
	Skylake PCH-LP 15/19 (POWER)	1A
Date: Monday, March 28, 2016	Sheet 9 of 48	

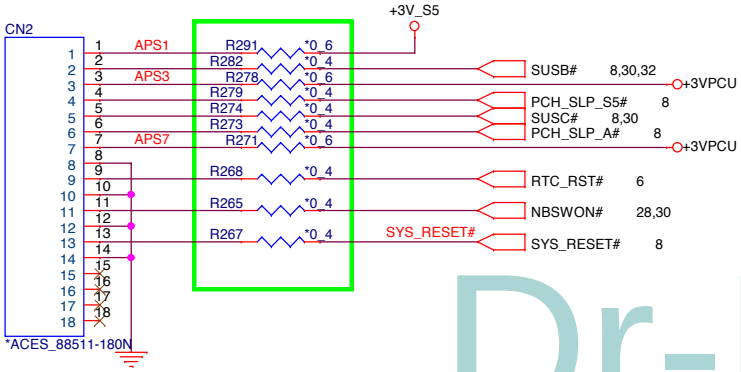
Skylake ULT (GND)



Quanta Computer Inc.		
PROJECT : ZAA		
Size	Document Number: Skylake 10/17/18 (GND)	Rev: 1A
Date: Monday, March 28, 2016	Sheet 10 of 48	

APS1 R289 *0_6 APS3 R272 *0_6 APS7

Intel APS Fixture use

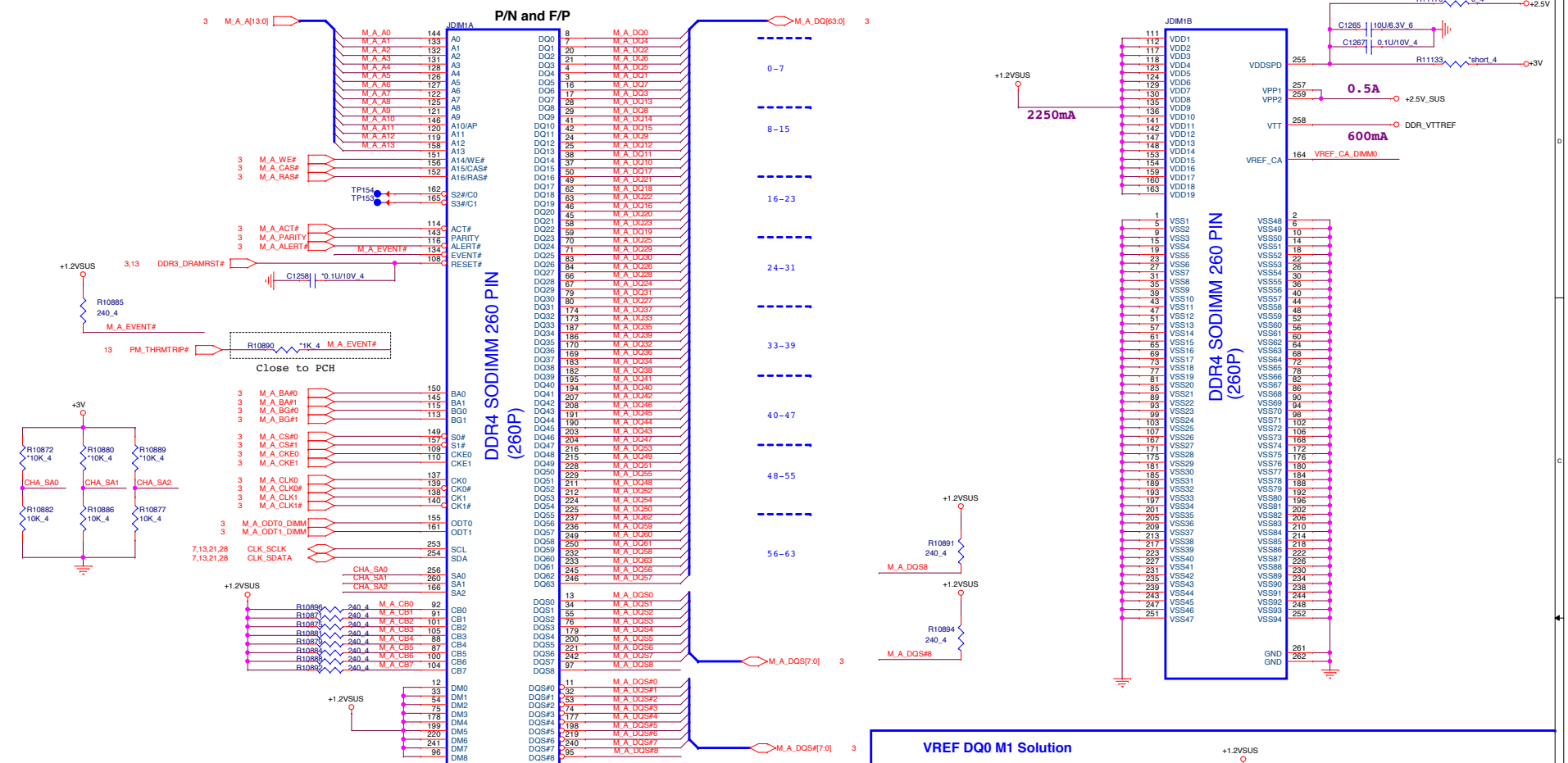


+3V_S5 2,3,4,6,7,8,9,20,24,26,27,28,30,32,34,35,40
+3VPCU 6,9,22,24,25,26,27,28,30,31,32,39,40,41

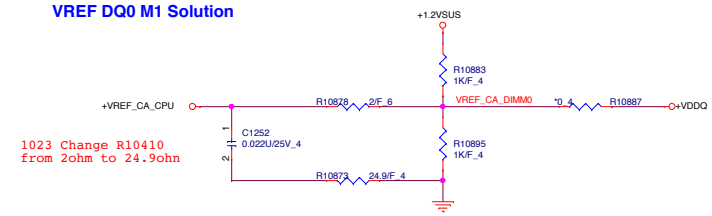
Quanta Computer Inc.

PROJECT : ZAA

Size	Document Number	Rev
	CPU/PCH XDP	1A
Date: Monday, March 28, 2016	Sheet 11 of 48	

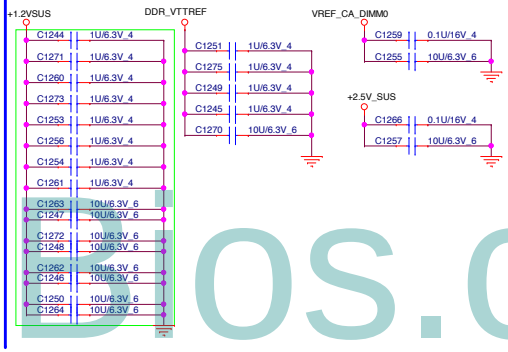


VREF DQ0 M1 Solution



Place these Caps near So-Dimm1.

1uF/10uF 4pcs on each side of connector



+1.2VSUS 3,5,13,35
+3V 2,4,6,7,8,9,13,14,16,21,22,23,24,25,26,27,28,30,32,33,34,35,36,39,40,41
+2.5V_SUS 13,35
DDR_VTTREF 13,35

+VDDQ 13,35
+VREF_CA_CPU 3

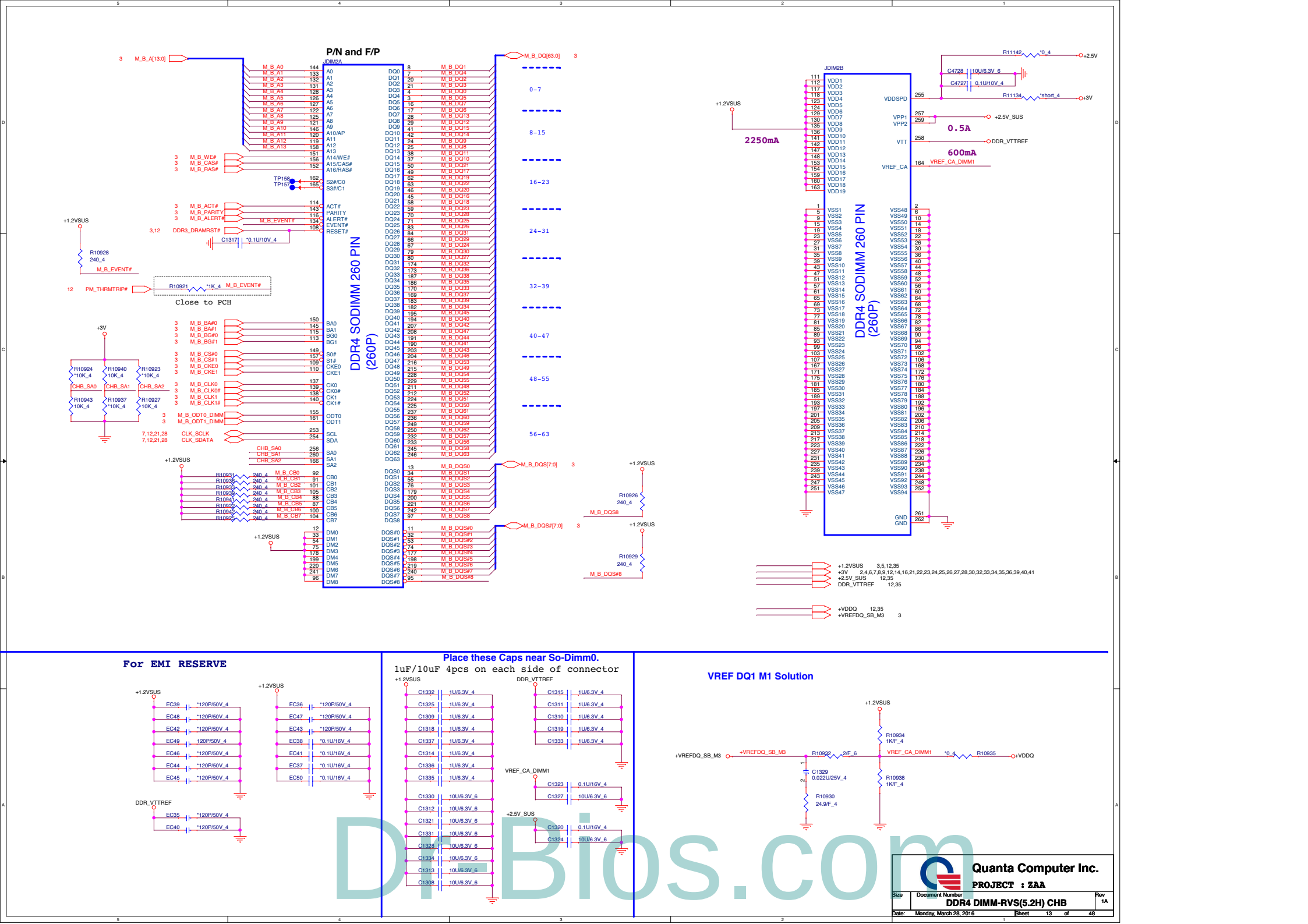
Table 4-56. DDR4 SODIMM Power Plane Decoupling

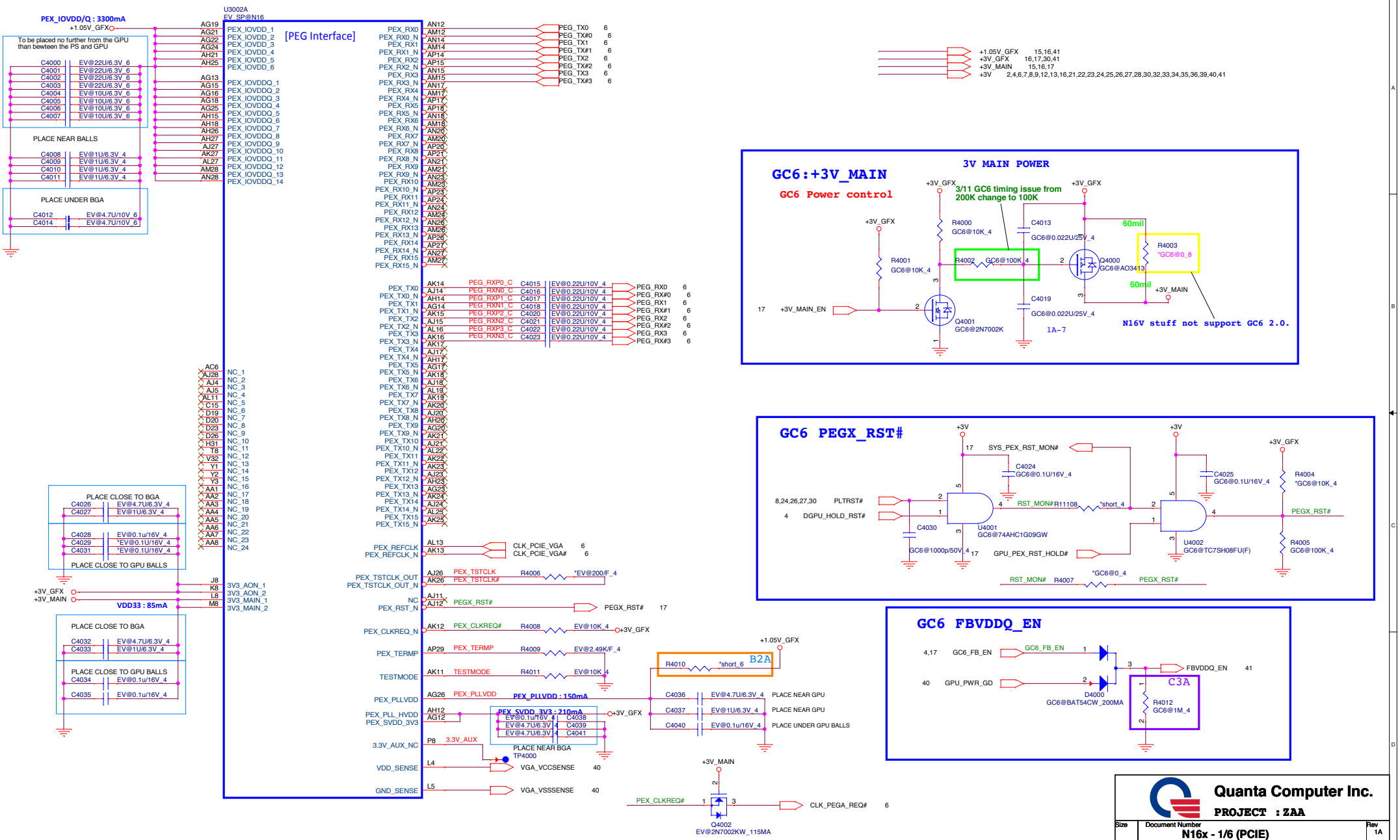
Memory Configuration	Power Domain	Decoupling Location	Qty x pF (size)	Note
DDR4 SODIMM 1DPC	VDDQ	4 near each side of the DIMM connector close to VDD pins	16x 10μF (0603)	
		4 near each side of the DIMM connector close to VDD pins	16x 1μF (0402)	
		1 placeholder	1x 330μF (7343)	
	VTT	Place these caps on the VTT plane close to SODIMM	1x 10μF (0805)	
		Placeholder Place these caps on the VTT plane close to SODIMM	1x 10μF (0805)	
		Place these caps on the VTT plane close to SODIMM	4x 1μF (0402)	
	VPP	DRAM Side	2x 10μF (0603)	
		DRAM Side	2x 1μF (0402)	
	VDDSPD	Place close to DIMM	1x 0.1μF (0402)	
		Place close to DIMM	1x 2.2μF (0402)	

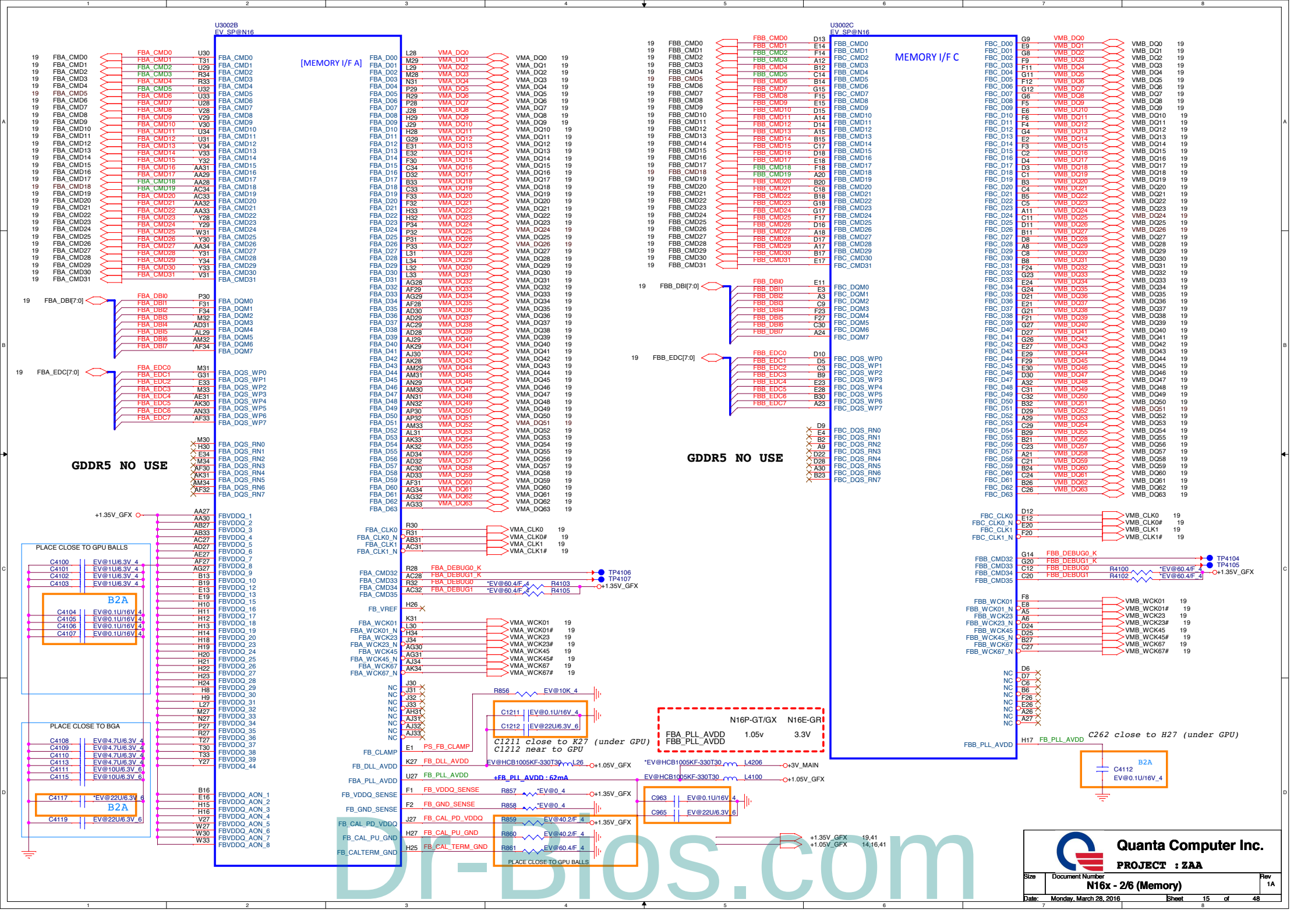
Notes:
1. Total quantity is referring to 2 channels.

Quanta Computer Inc.
PROJECT : ZAA

Size	Document Number	Rev
	DDR4 DIMM-STD(5.2H) CHA	1A
Date: Monday, March 28, 2016	Sheet 12 of 48	


P/N and F/P
JDIM2A
DDR4 SODIMM 260 PIN
(260P)
M_B_A[13:0]
M_B_DQ[63:0]
0~7
8~15
16~23
24~31
32~39
40~47
48~55
56~63
M_B_DQS[7:0]
M_B_DQS#[7:0]
Close to PCH
R10921 *1K_4 M_B_EVENT#
PM_THRMTRIP#
DDR3_DRAMRST#
C1317 *0.1U/10V_4
+1.2VSUS
+3V
CHB_SA0
CHB_SA1
CHB_SA2
CLK_SCLK
CLK_SDATA
JDIM2B
DDR4 SODIMM 260 PIN
(260P)
2250mA
0.5A
600mA
VDDSPD
VPP1
VPP2
VTT
VREF_CA
VREF_CA_DIMM1
DDR_VTTREF
+2.5V_SUS
+2.5VSUS
+3V
R11142 *0_4
C4728 10U/6.3V_6
C4727 0.1U/10V_4
R11134 *short_4
+VDDQ 12,35
+VREFDQ_SB_M3 3
For EMI RESERVE
Place these Caps near So-Dimm0.
1uF/10uF 4pcs on each side of connector
VREF DQ1 M1 Solution
+VREFDQ_SB_M3
R10932 2/F_6
R10934 1K/F_4
R10935 *0_4
R10938 1K/F_4
C1329 0.022U/25V_4
R10930 24.9/F_4
+VDDQ
Quanta Computer Inc.
PROJECT : ZAA
DDR4 DIMM-RVS(5.2H) CHB
Rev 1A
Date: Monday, March 28, 2016
Sheet 13 of 48


U3002A
EV_SP@N16
[PEG Interface]
PEX_IOVDD
PEX_IOVDDQ
PEX_RX0
PEX_RX0_N
PEX_TX0
PEX_TX0_N
PEX_REFCLK
PEX_REFCLK_N
PEX_TSTCLK_OUT
PEX_TSTCLK_OUT_N
NC
PEX_RST_N
PEX_CLKREQ_N
PEX_TERMP
TESTMODE
PEX_PLLVDD
PEX_PLL_HVDD
PEX_SVDD_3V3
3.3V_AUX_NC
VDD_SENSE
GND_SENSE
PEX_IOVDD : 3300mA
VDD33 : 85mA
PEX_PLLVDD : 150mA
PEX_SVDD_3V3 : 210mA
PLACE NEAR BALLS
PLACE UNDER BGA
PLACE CLOSE TO BGA
PLACE CLOSE TO GPU BALLS
PLACE NEAR GPU
PLACE UNDER GPU BALLS
PLACE NEAR BGA
GC6:+3V_MAIN
GC6 Power control
3V MAIN POWER
3/11 GC6 timing issue from 200K change to 100K
N16V stuff not support GC6 2.0.
GC6 PEGX_RST#
GC6 FBVDDQ_EN
Quanta Computer Inc.
PROJECT : ZAA
N16x - 1/6 (PCIE)
Monday, March 28, 2016
Sheet 14 of 48


U3002B
EV_SP@N16
[MEMORY I/F A]
GDDR5 NO USE
U3002C
EV_SP@N16
MEMORY I/F C
GDDR5 NO USE
PLACE CLOSE TO GPU BALLS
PLACE CLOSE TO BGA
B2A
N16P-GT/GX N16E-GR
FBA_PLL_AVDD 1.05v 3.3V
FBB_PLL_AVDD
C1211 close to K27 (under GPU)
C1212 near to GPU
C262 close to H27 (under GPU)
+FB_PLL_AVDD : 62mA
PLACE CLOSE TO GPU BALLS
Quanta Computer Inc.
PROJECT : ZAA
Size
Document Number
N16x - 2/6 (Memory)
Rev
1A
Date: Monday, March 28, 2016
Sheet 15 of 48

U3002D
EV_SP@N16

[IFPA/B_LVDS]
AH8 IFPAB_PLLVDD
AG8 IFPA_IOVDD
AG9 IFPB_IOVDD
AJ8 IFPAB_RSET
IFPA_TXC AM6
IFPA_TXC_N AN6
IFPA_TXD0 AP3
IFPA_TXD0_N AN3
IFPA_TXD1 AN5
IFPA_TXD1_N AM5
IFPA_TXD2 AL6
IFPA_TXD2_N AK6
IFPA_TXD3 AJ6
IFPA_TXD3_N AH6
IFPB_TXC AJ9
IFPB_TXC_N AH9
IFPB_TXD4 AP6
IFPB_TXD4_N AP5
IFPB_TXD5 AM7
IFPB_TXD5_N AL7
IFPB_TXD6 AN8
IFPB_TXD6_N AM8
IFPB_TXD7 AK8
IFPB_TXD7_N AL8

[IFPC/D_TMDS]
AF7 IFPC_PLLVDD
AG7 IFPD_PLLVDD
AF6 IFPC_IOVDD
AG6 IFPD_IOVDD
AF8 IFPC_RSET
AN2 NC
IFPC_AUX_I2CW_SCL AG3
IFPC_AUX_I2CW_SDA_N AG2
IFPC_L0 AK1
IFPC_L0_N AJ1
IFPC_L1 AJ3
IFPC_L1_N AJ2
IFPC_L2 AH3
IFPC_L2_N AH4
IFPC_L3 AG5
IFPC_L3_N AG4
IFPD_AUX_I2CX_SCL AK3
IFPD_AUX_I2CX_SDA_N AK2
IFPD_L0 AM1
IFPD_L0_N AM2
IFPD_L1 AM3
IFPD_L1_N AM4
IFPD_L2 AL3
IFPD_L2_N AL4
IFPD_L3 AK4
IFPD_L3_N AK5

[IFPE/F_DP]
AB8 IFPEF_PLLVDD
AC7 IFPE_IOVDD
AC8 IFPF_IOVDD
AD6 IFPEF_RSET
IFPE_AUX_I2CY_SCL AB3
IFPE_AUX_I2CY_SDA_N AB4
IFPE_L0 AD2
IFPE_L0_N AD3
IFPE_L1 AD1
IFPE_L1_N AC1
IFPE_L2 AC2
IFPE_L2_N AC3
IFPE_L3 AC4
IFPE_L3_N AC5
IFPF_AUX_I2CZ_SCL AF3
IFPF_AUX_I2CZ_SDA_N AF2
IFPF_L0 AE3
IFPF_L0_N AE4
IFPF_L1 AF4
IFPF_L1_N AF5
IFPF_L2 AD4
IFPF_L2_N AD5
IFPF_L3 AG1
IFPF_L3_N AF1

[DACA/B_CRT]
AG10 DACA_VDD
AP9 DACA_VREF
AP8 DACA_RSET
DACA_RED AK9
DACA_GREEN AL10
DACA_BLUE AL9
DACA_HSYNC AM9
DACA_VSYNC AN9
I2CA_SCL
I2CA_SDA

[XTAL IN]
AD7 VID_PLLVDD
XTAL_IN
XTAL_OUT
XTAL_OUTBUFF
XTAL_SSIN

+3V_MAIN 14,15,17
+1.05V_GFX 14,15,41
+3V_GFX 14,17,30,41
+3V 2,4,6,7,8,9,12,13,14,21,22,23,24,25,26,27,28,30,32,33,34,35,36,39,40,41

3V_MAIN_PWGD

+3V_MAIN R4203 EV@4.7K_4 C4201 *EV@1000p/50V_4
Q4201 EV@MMBT3904-7-F
R4201 EV@4.7K_4 C4200 EV@1000p/50V_4
Q4200 EV@DTC144EU
R4200 EV@1.5K/F_4 R4202 *EV@100K/F_4
+3V_GFX
3V_MAIN_PWGD → 3V_MAIN_PWGD 40,41

+1.05V_GFX and GPU core power EN

DGPU_PWROK

DGPU_PGOK-1
41 HWPG_1.35VGFX
R4207 EV@4.7K_4 C4203 *EV@1000P/50V_4
Q4203 EV@METR3904-G
R4205 EV@4.7K_4 C4202 EV@1000P/50V_4
Q4202 EV@DTC144EUA
R4204 EV@4.7K_4 R4206 EV@100K/F_4
DGPU_PWROK 4

R4 I2CA_SCL EV@1.8K/F_4 R4208
R5 I2CA_SDA EV@1.8K/F_4 R4209

Reserve

XTAL_OUTBUFF R4210 *EV@10K_4 +3V_GFX

XTAL27_IN
XTAL27_OUT
Y4200 EV@27MHZ_10
C4206 EV@10P/50V_4C
C4207 EV@10P/50V_4C
B2A

H3 XTAL27_IN
H2 XTAL27_OUT
J4 XTAL_OUTBUFF
H1 XTAL_SSIN
R4211 EV@10K_4
R4212 EV@10K_4

PLACE CLOSE TO GPU / PLACE CLOSE TO BALLS

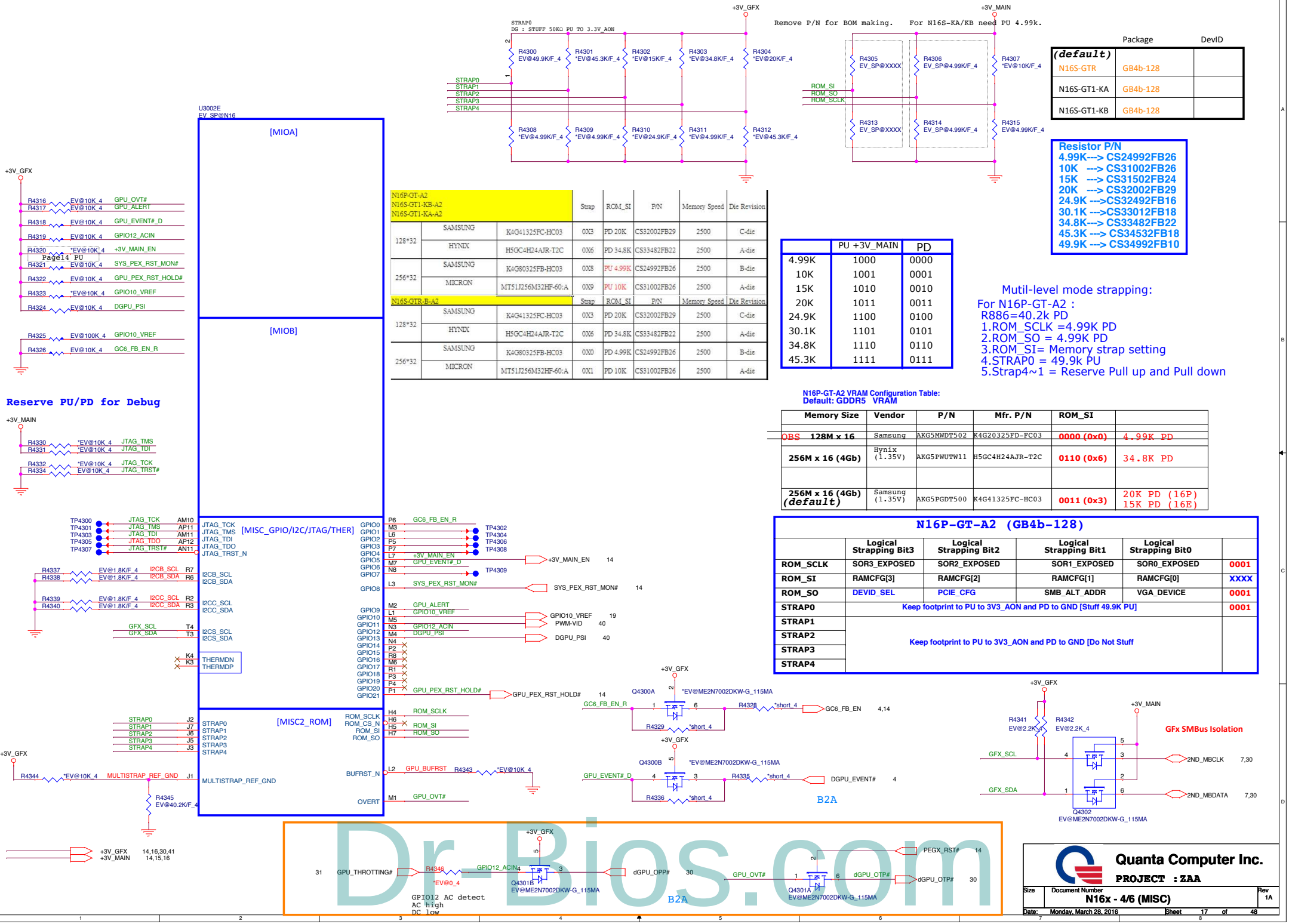
PLLVDD : 200mA

+1.05V_GFX L4200 EV@HCB1005KF-330T30
C4204 EV@22U/6.3V_6
NV_PLLVDD AD8 → PLLVDD
B2A C4205 EV@0.1U/16V_4
PLLVDD AE8 → SP_PLLVDD

C5092 Close to AE8
C5090 Close to AD7

+1.05V_GFX L4201 EV@BLM15PX181SN1D_1.5A
C4208 EV@22U/6.3V_6
C4209 EV@4.7U/6.3V_4
B2A C4210 EV@0.1U/16V_4 C4211 EV@0.1U/16V_4

Quanta Computer Inc.
PROJECT : ZAA
Size | Document Number: N16x - 3/6 (Display) | Rev 1A
Date: Monday, March 28, 2016 | Sheet 16 of 48



N16P-GT-A2 N16S-GT1-KB-A2 N16S-GT1-KA-A2			Strap	ROM_SI	P/N	Memory Speed	Die Revision
128*32	SAMSUNG	K4G41325FC-HC03	0X3	PD 20K	CS32002FB29	2500	C-die
	HYNIX	H5GC4H24AJR-T2C	0X6	PD 34.8K	CS33482FB22	2500	A-die
256*32	SAMSUNG	K4G80325FB-HC03	0X8	PU 4.99K	CS24992FB26	2500	B-die
	MICRON	MT51J256M32HF-60:A	0X9	PU 10K	CS31002FB26	2500	A-die
N16S-GTR-B-A2			Strap	ROM_SI	P/N	Memory Speed	Die Revision
128*32	SAMSUNG	K4G41325FC-HC03	0X3	PD 20K	CS32002FB29	2500	C-die
	HYNIX	H5GC4H24AJR-T2C	0X6	PD 34.8K	CS33482FB22	2500	A-die
256*32	SAMSUNG	K4G80325FB-HC03	0X0	PD 4.99K	CS24992FB26	2500	B-die
	MICRON	MT51J256M32HF-60:A	0X1	PD 10K	CS31002FB26	2500	A-die

	PU +3V_MAIN	PD
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

	Package	DevID
(default) N16S-GTR	GB4b-128	
N16S-GT1-KA	GB4b-128	
N16S-GT1-KB	GB4b-128	

Resistor P/N
4.99K---> CS24992FB26
10K ---> CS31002FB26
15K ---> CS31502FB24
20K ---> CS32002FB29
24.9K --->CS32492FB16
30.1K --->CS33012FB18
34.8K---> CS33482FB22
45.3K ---> CS34532FB18
49.9K ---> CS34992FB10

Mutil-level mode strapping:
For N16P-GT-A2 :
R886=40.2k PD
1.ROM_SCLK =4.99K PD
2.ROM_SO = 4.99K PD
3.ROM_SI= Memory strap setting
4.STRAP0 = 49.9k PU
5.Strap4~1 = Reserve Pull up and Pull down

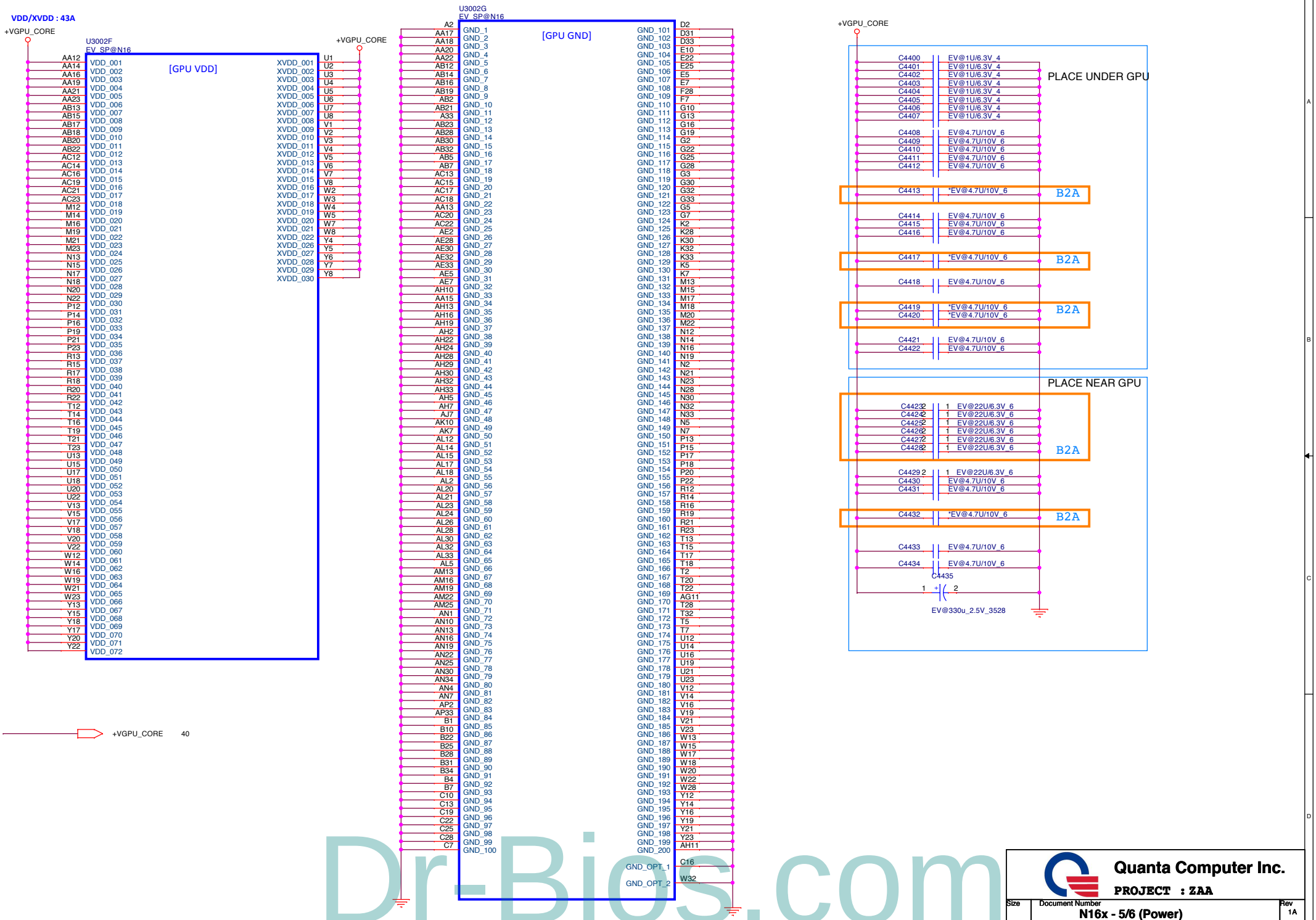
N16P-GT-A2 VRAM Configuration Table:
Default: GDDR5 VRAM

Memory Size	Vendor	P/N	Mfr. P/N	ROM_SI	
OBS 128M x 16	Samsung	AKG5MWDT502	K4G20325FD-FC03	0000 (0x0)	4.99K PD
256M x 16 (4Gb)	Hynix (1.35V)	AKG5PWUTW11	H5GC4H24AJR-T2C	0110 (0x6)	34.8K PD
256M x 16 (4Gb) *(default)*	Samsung (1.35V)	AKG5PGDT500	K4G41325FC-HC03	0011 (0x3)	20K PD (16P) 15K PD (16E)

N16P-GT-A2 (GB4b-128)

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	0001
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE	0001
STRAP0	Keep footprint to PU to 3V3_AON and PD to GND [Stuff 49.9K PU]				0001
STRAP1	Keep footprint to PU to 3V3_AON and PD to GND [Do Not Stuff				
STRAP2					
STRAP3					
STRAP4					

Quanta Computer Inc.
PROJECT : ZAA
Size | Document Number: N16x - 4/6 (MISC) | Rev 1A
Date: Monday, March 28, 2016 | Sheet 17 of 48



Quanta Computer Inc.
PROJECT : ZAA

Size	Document Number	Rev
	N16x - 5/6 (Power)	1A

Date: Monday, March 28, 2016 Sheet 18 of 48

CHANNEL A: 1024MB GDDR5x32

15 VMA_DQ[63..0] VMA_DQ[63..0]
15 VMB_DQ[63..0] VMB_DQ[63..0]

Non-mirror, MF=0 Channel A <0-31>

DQA24~31
DQA16~23
DQA8~15
DQA0~7

Mirror, MF=1 Channel A <32-63>

DQA32~39
DQA40~47
DQA48~55
DQA56~63

KB OnlyA

Non-mirror, MF=0 Channel B <0-31>

DQB24~31
DQB16~23
DQB8~15
DQB0~7

Mirror, MF=1 Channel B <32-63>

DQB32~39
DQB40~47
DQB48~55
DQB56~63

KA OnlyB

CKE* is strap pin to set ODT value of memory chip

RST PD place @ the end of daisy-chain.

GDDR5 Mode H Mapping

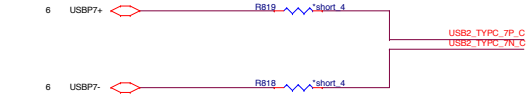
< 0~31 >	< 32~63 >	Memory
CMD0	CMD16	CS*
CMD1	CMD17	A3_BA3
CMD2	CMD18	A2_BA0
CMD3	CMD19	A4_BA2
CMD4	CMD20	A5_BA1
CMD5	CMD21	WE*
CMD6	CMD22	A7_A8
CMD7	CMD23	A6_A11
CMD8	CMD24	ABI*
CMD9	CMD25	A12_RFU
CMD10	CMD26	A0_A10
CMD11	CMD27	A1_A9
CMD12	CMD28	RAS*
CMD13	CMD29	RST*
CMD14	CMD30	CKE*
CMD15	CMD31	CAS*

Quanta Computer Inc.
PROJECT : ZAA
Size: Document Number: N16x - 6/6 (GDDR5x32) Rev: 1A
Date: Monday, March 28, 2016 Sheet 19 of 48

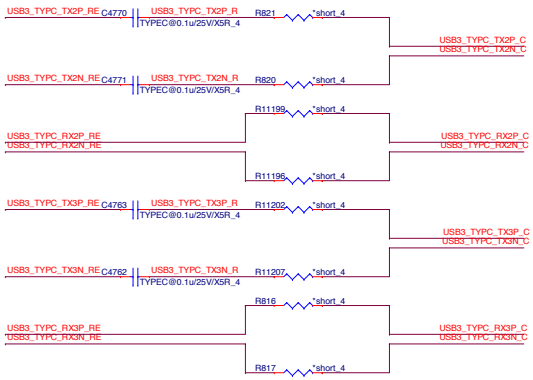
USB TYPE-C

USB2.0 ESD

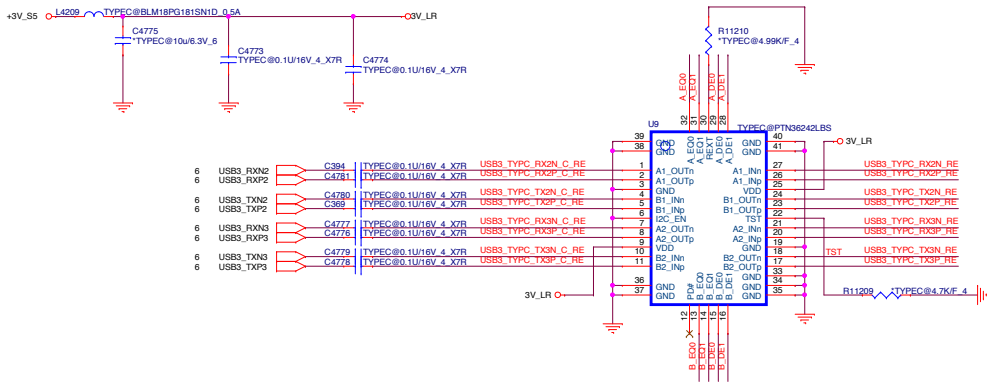
Close to connector



Type C1 HSIO ESD

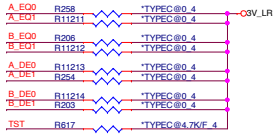


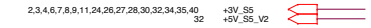
USB3 Re-Driver



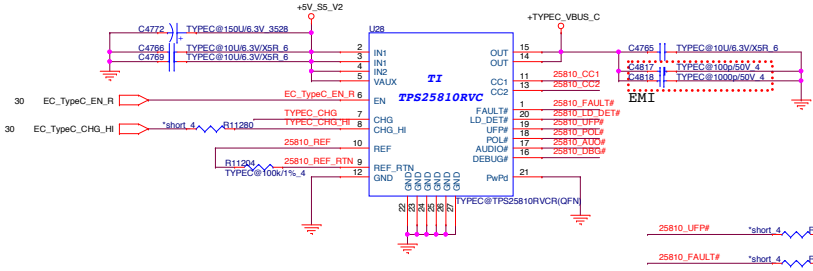
A_EQ0 / B_EQ0	A_EQ1 / B_EQ1		A_DE0 / B_DE0	A_DE1 / B_DE1	
0	0	9dB	0	0	-3.5dB
0	1	3dB	0	1	no de-emphasis
1	0	6dB	1	0	-7dB
1	1	7.5dB	1	1	-5dB

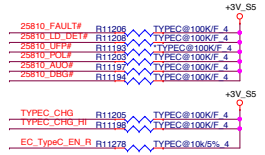
TST : Low = Normal LFPS swing / Hight =Turn down LFPS swing





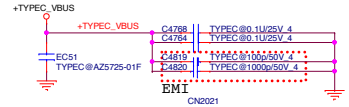
Vendor suggest input cap 120u

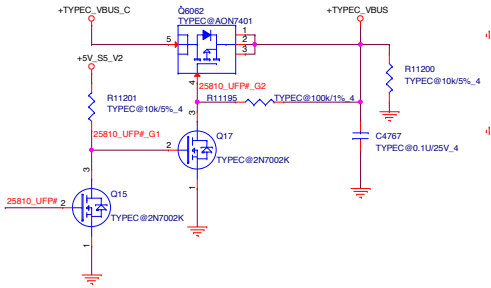


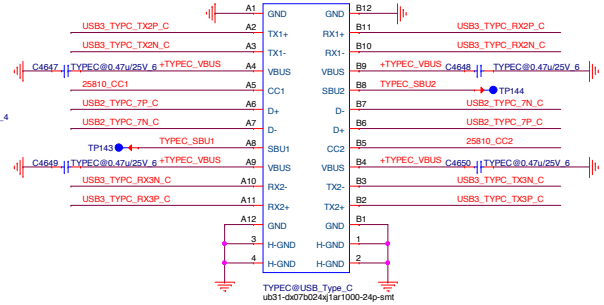


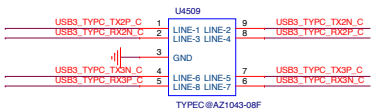
TPS25810 Port	CC1	CC2	TPS25810 Response OUT	VCONN On CC1 or CC2	POLb	UFPb	AUDIOb	DEBUGb
Nothing Attached	OPEN	OPEN	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
UFP Connected	Rd	OPEN	IN1	NO	Hi-Z	LOW	Hi-Z	Hi-Z
UFP Connected	OPEN	Rd	IN1	NO	LOW	LOW	Hi-Z	Hi-Z
Powered Cable/No UFP Connected	OPEN	Ra	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Powered Cable/No UFP Connected	Ra	OPEN	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Powered Cable/UFP Connected	Rd	Ra	IN1	CC2	Hi-Z	LOW	Hi-Z	Hi-Z
Powered Cable/UFP Connected	Ra	Rd	IN1	CC1	LOW	LOW	Hi-Z	Hi-Z
Debug Accessory Connected	Rd	Rd	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	LOW
Audio Adapter Accessory Connected	Ra	Ra	OPEN	NO	Hi-Z	Hi-Z	LOW	Hi-Z

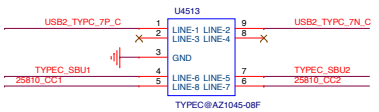
CHG	CHG_HI	CC Capability Broadcast	Current Limit	Load Detect Threshold
0	0	STD	1.67 A	NA
0	1	STD	1.67 A	NA
1	0	1.5 A	1.67 A	NA
1	1	3.0 A	3.34 A	1.77 A











Quanta P/NAMAZING P/NUSD保護位置
BC104308Z00AZ1043-08F.R7G0.08TX RX (USB3.0 GEN1 5G)
BC104508Z00AZ1045-08F.R7G0.08D+ D- SBU1 SBU2 CC1 CC2
BC005725Z00AZ5725-01F.R7G0.009 PD 5V (follow ZAA)

Quanta Computer Inc.
PROJECT : ZAA

Size	Document Number	Rev
	USB_Type C_25810	1A

Date: Monday, March 28, 2016 Sheet 20 of 48

DP TO VGA

Close to CPU side of CAP.

2	DDI2_TXP0	R10842 *short_4	CRT_TXP0	
2	DDI2_TXN0	R10843 *short_4	CRT_TXN0	
2	DDI2_TXP1	R10844 *short_4	CRT_TXP1	
2	DDI2_TXN1	R10845 *short_4	CRT_TXN1	
2	PCH_DP_HPD	R10846 *short_4	CRT_HPD	
2	DDI2_AUXN	R10847 *short_4	CRT_AUXN	
2	DDI2_AUXP	R10848 *short_4	CRT_AUXP	

Power

+3V — L4 100MHz_6 — AVCC33

+3V — L4208 100MHz_6 — VDD_DAC_33

CRT_AUXN	C343	0.1U/16V_4	AUX_CH_N
CRT_AUXP	C341	0.1U/16V_4	AUX_CH_P
CRT_TXP0	C335	0.1U/16V_4	LANE0_P
CRT_TXN0	C331	0.1U/16V_4	LANE0_N
CRT_TXP1	C329	0.1U/16V_4	LANE1_P
CRT_TXN1	C315	0.1U/16V_4	LANE1_N

7,12,13,28 CLK_SDATA — R11190 *0_4

7,12,13,28 CLK_SCLK — R11189 *0_4

C4752 0.1U/16V_4

C4751 0.1U/16V_4

C4754 2.2U/6.3V_6

VCCK_V12

C4748 0.1U/16V_4

U13 RTD2166

Pin		Pin	
33	EPAD	1	AVCC33
32	HPD	2	AUX_CH_P
31	EXT1.2V_CTRL	3	AUX_CH_N
30	SMB_SCL	4	VCCK_V12
29	SMB_SDA	5	LANE0_P
28	XI	6	LANE0_N
27	LDO_RSTB	7	LANE1_P
26	PVCC_33	8	LANE1_N
25	VCCK_12	24	GND
		23	RED_P → CRT_RED
		22	GREEN_P → CRT_GRE
		21	BLUE_P → CRT_BLU
		20	VDD_DAC_33
		19	HSYNC → HSYNC_C
		18	VSYNC → VSYNC_C
		17	HVSYNC_PWR
9	POL2		
10	POL1/SPI_CEB		
11	SPI_CLK		
12	SPI_SI		
13	SPI_SO		
14	VCC_33		
15	VGA_SCL		
16	VGA_SDA		

+5V

C4749 0.1U/16V_4

C4753 4.7U/10V_6

C4750 0.1U/16V_4

+3V

R11187 4.7K_4

R11285 *4.7K_4

R11286 4.7K_4

R11188 4.7K_4

R11287 *4.7K_4

TP4376

VGA

DDCDAT		DDCDAT	22
DDCCLK		DDCCLK	22
HSYNC_C	R11191 *short_4	HSYNC	22
VSYNC_C	R11192 *short_4	VSYNC	22
CRT_RED		CRT_RED	22
CRT_GRE		CRT_GRE	22
CRT_BLU		CRT_BLU	22

Note:

1- C1,C3,C4,C5,C11,C16, C21 should be placed close to chip

2- C5 shold be X5R material

3- R6, R7, R8 should be 75 ohm with +/-1%

4- Suggest to connect Pin 29 and Pin 30 to PCH SMBUS for debug purpose.

5- This configuration is for internal ROM mode and using embedded LDO mode.

+3V 2,4,6,7,8,9,12,13,14,16,22,23,24,25,26,27,28,30,32,33,34,35,36,39,40,41

+5V 22,23,25,26,28,32,39

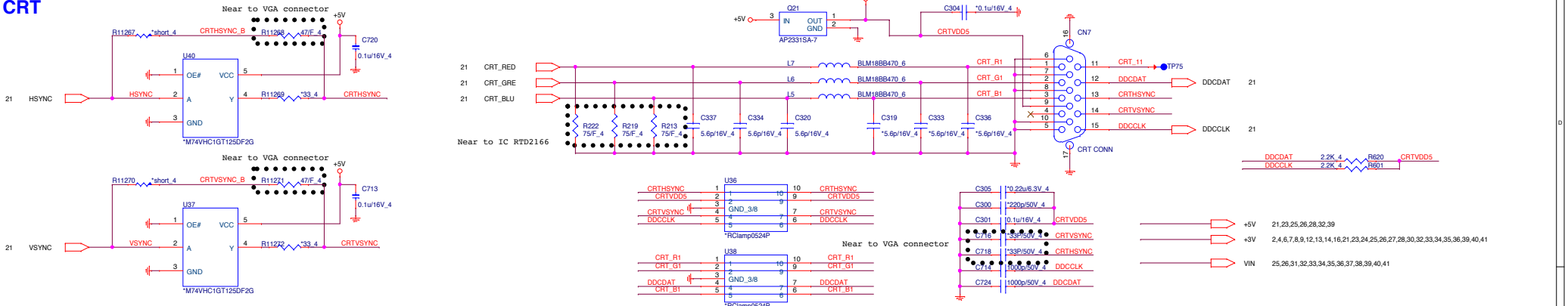
Quanta Computer Inc.

PROJECT : ZAA

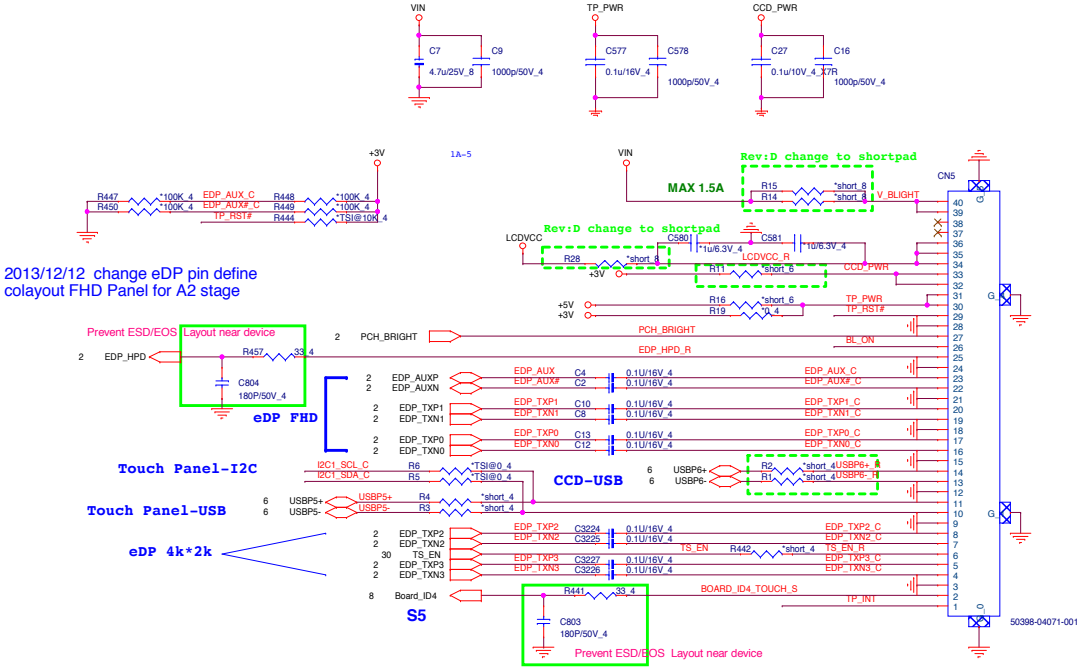
Size	Document Number	Rev
	RTD2166-CG	1A

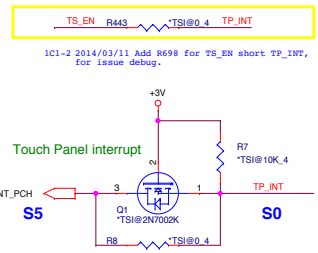
Date: Monday, March 28, 2016 Sheet 21 of 48

CRT

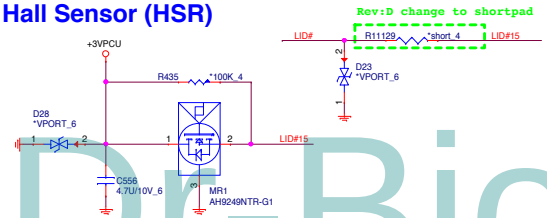


LCD CONNECTOR

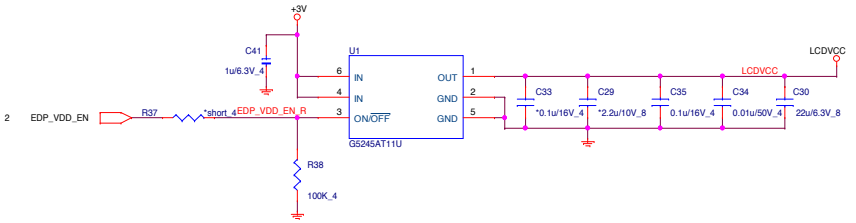




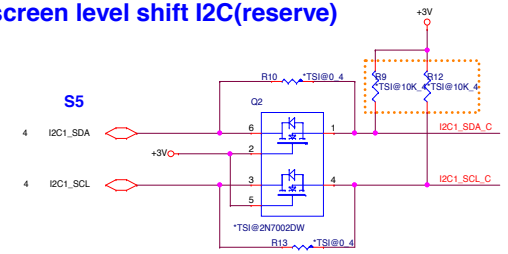
Hall Sensor (HSR)

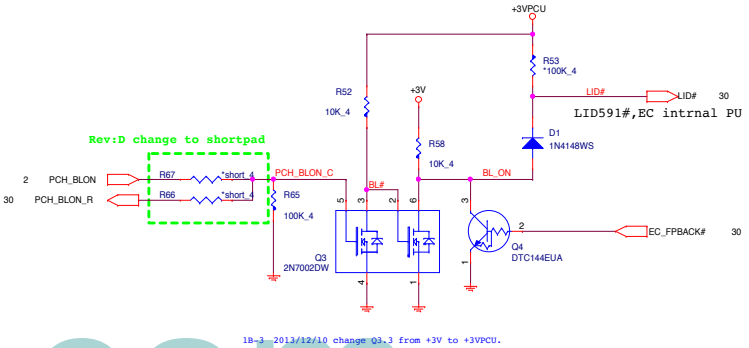


LCD Power



Touch screen level shift I2C(reserve)

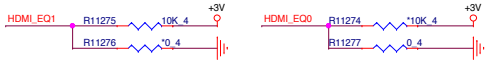




Quanta Computer Inc.			
PROJECT : ZAA			
Size	Document Number		Rev
	CRT/LVDS/CAMERA/LID		1A
Date: Monday, March 28, 2016		Sheet 22 of 48	

HDMI

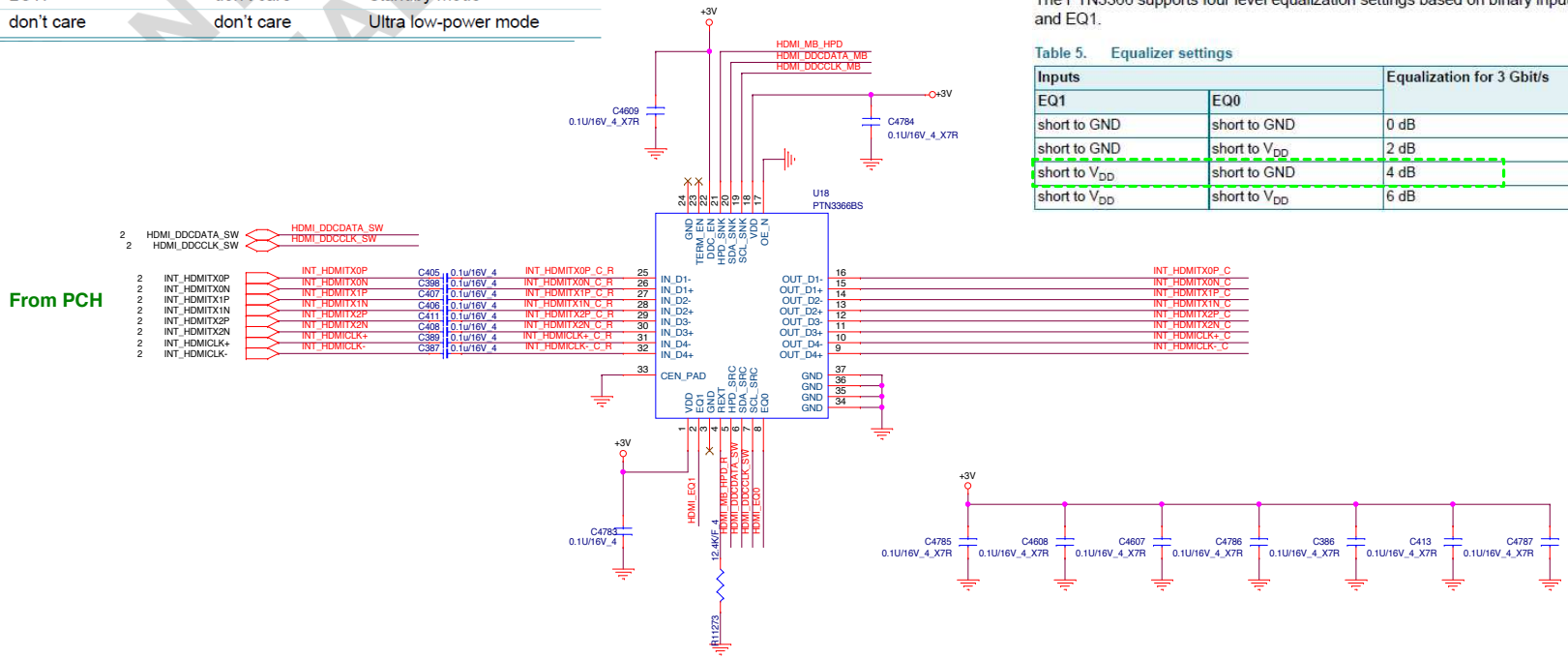
OE_N	DDC_EN	HPD_SINK	Source output	PTN3366 power mode
LOW	HIGH	HIGH	source active	Active mode; DDC active
LOW	LOW	LOW	don't care	Standby mode
HIGH	LOW	don't care	don't care	Ultra low-power mode

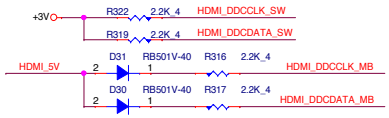


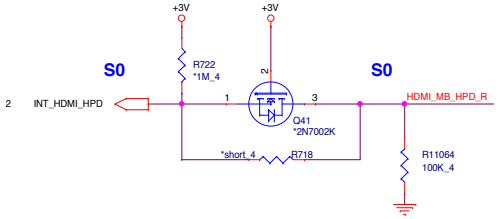
The PTN3366 supports four level equalization settings based on binary input pins EQ0 and EQ1.

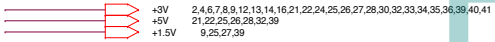
Table 5. Equalizer settings

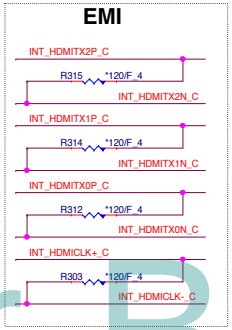
Inputs		Equalization for 3 Gbit/s
EQ1	EQ0	
short to GND	short to GND	0 dB
short to GND	short to V_{DD}	2 dB
short to V_{DD}	short to GND	4 dB
short to V_{DD}	short to V_{DD}	6 dB

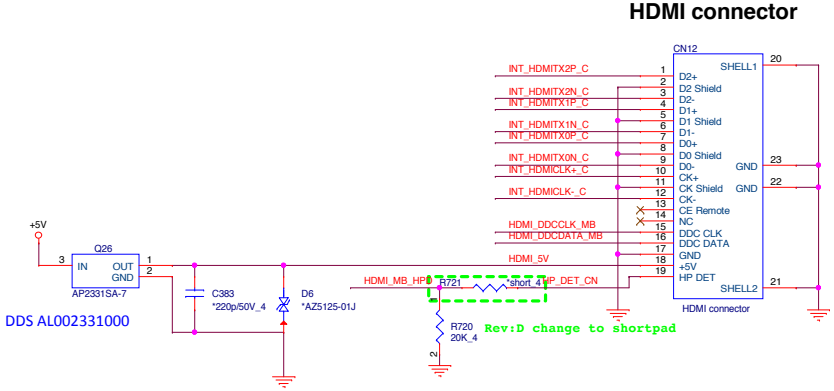








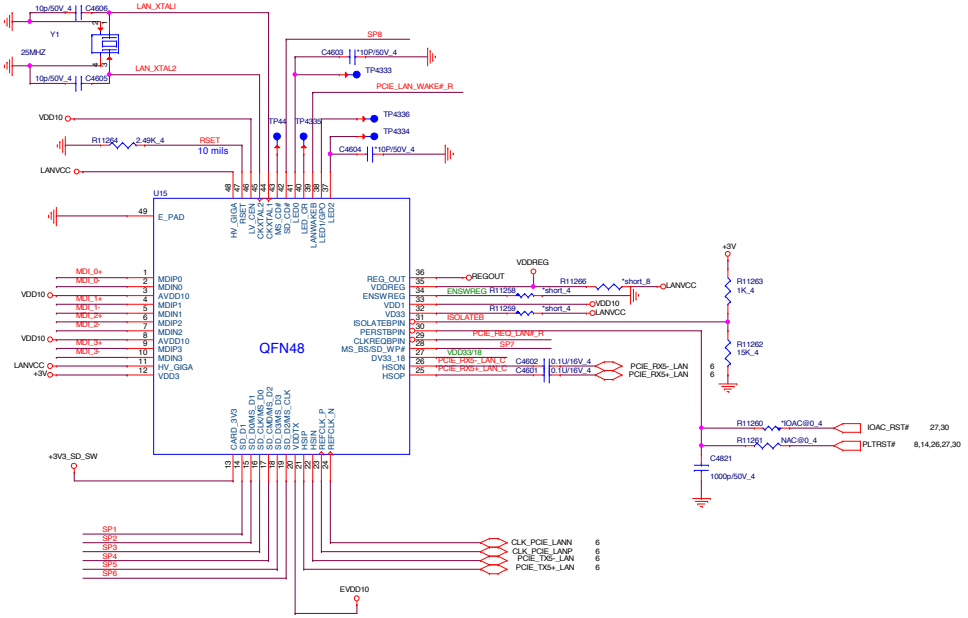




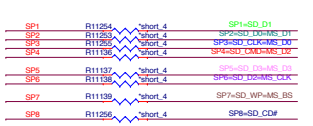
Quanta Computer Inc.			
PROJECT : ZAA			
Size	Document Number	HDMI (PTN3366BS)	Rev 1A
Date: Monday, March 28, 2016	Sheet 23 of 48		

LAN & Card reader Combo (LAN)

Giga LAN (LAN)

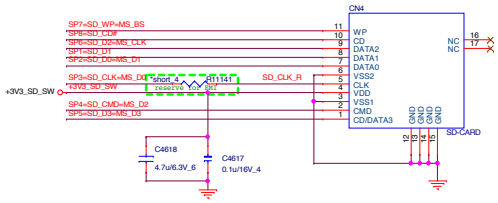


Card Reader (CRD)

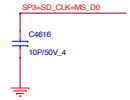


Share Pin

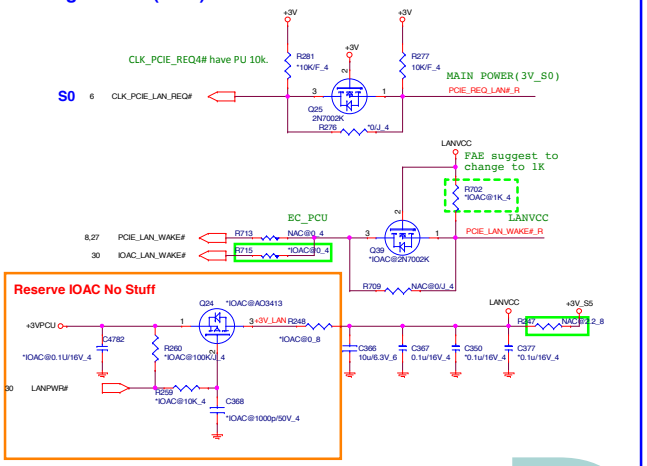
SP1	SD_D1	
SP2	SD_D0	MS_D1
SP3	SD_CLK	MS_D0
SP4	SD_CMD	MS_D2
SP5	SD_D3	MS_D3
SP6	SD_D2	MS_CLK
SP7	SD_WP	MS_BS
SP8	SD_CD#	
SP9		MS_INS#

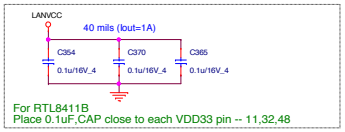


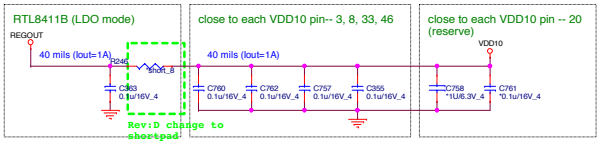
EMI

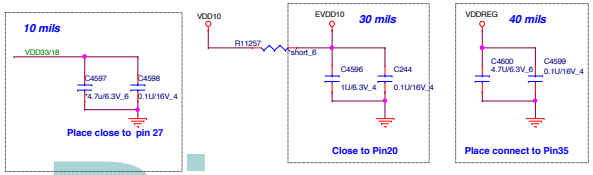


Leakage circuit (MPC)



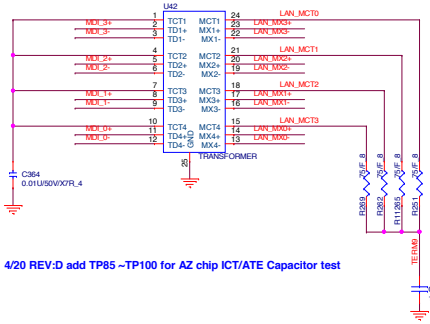




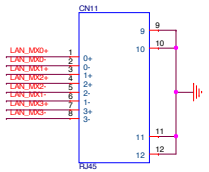


Tramsformer

Layout:All termination signal should have 30 mil trace



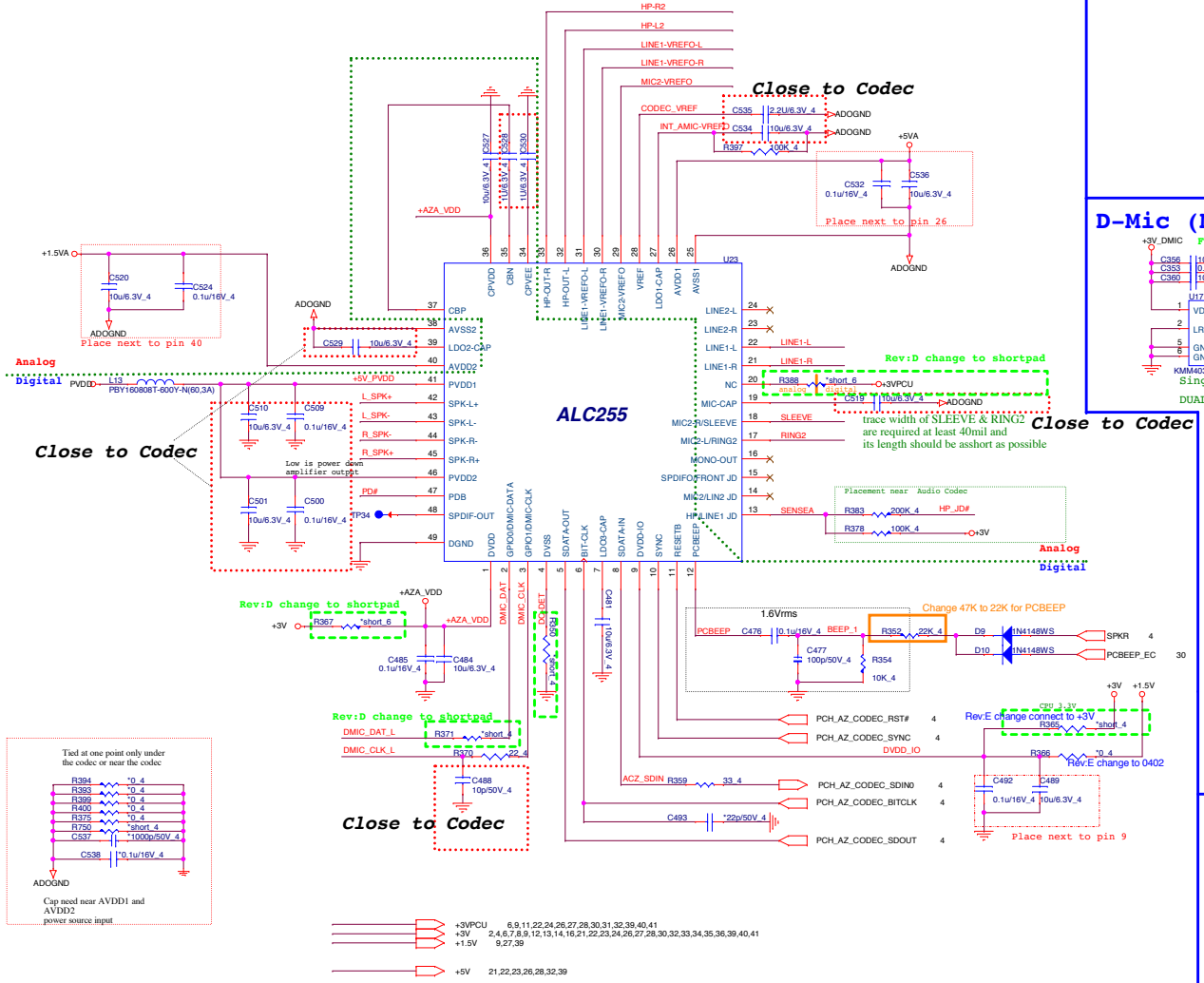
RJ45 Connector



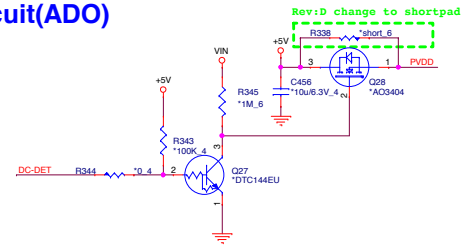
4/20 REV:D add TP85 ~TP100 for AZ chip ICT/ATE Capacitor test

Quanta Computer Inc.			
PROJECT : ZAA			
Size	Document Number		Rev
	LAN/CRD COMBO - RTL8411B		1A
Date: Monday, March 28, 2016	Sheet 24 of 48		

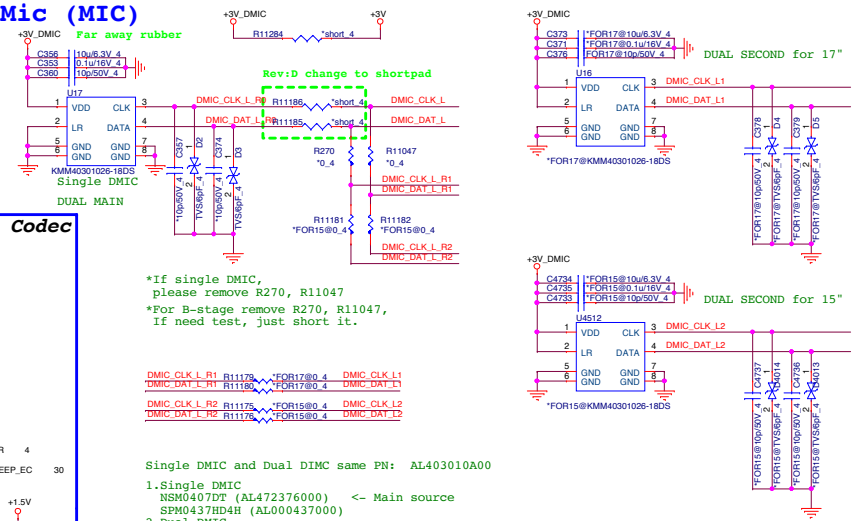
Codec(ADO)



DC-DET circuit(ADO)



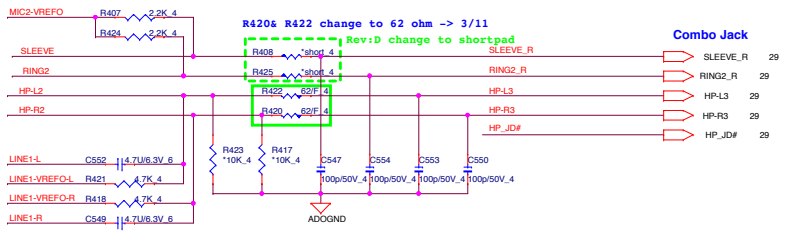
D-Mic (MIC)



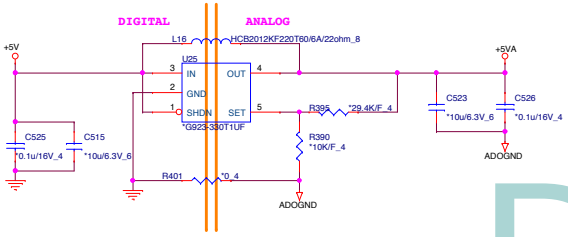
Single DMIC and Dual DIMC same PN: AL403010A00

1.Single DMIC
NSM0407DT (AL472376000) <- Main source
SPM0437HD4H (AL000437000)
2.Dual DMIC
NSM0410DT (W/ Fortemedia algorithm)
Main MIC CS need connect to second MIC DATA

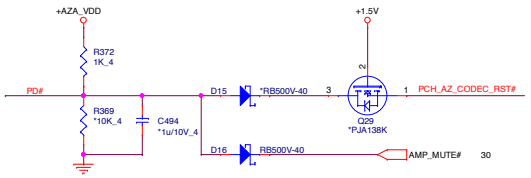
Universal Audio Jack HEADPHONE/MIC/LINE combo (ADO)



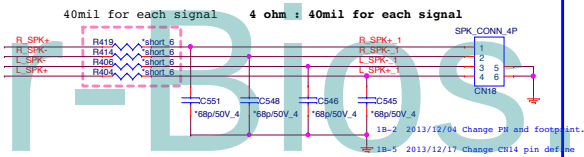
Codec PWR 5V(ADO)



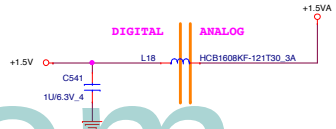
Mute(ADO)



Internal Speaker



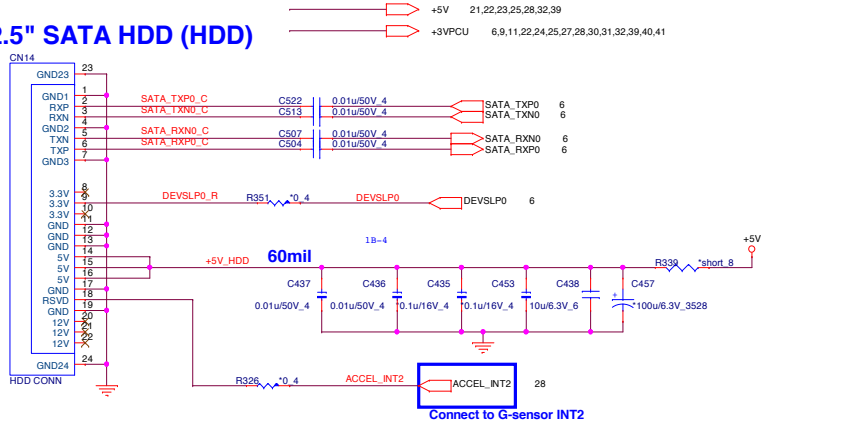
Codec PWR 1.5V(ADO)



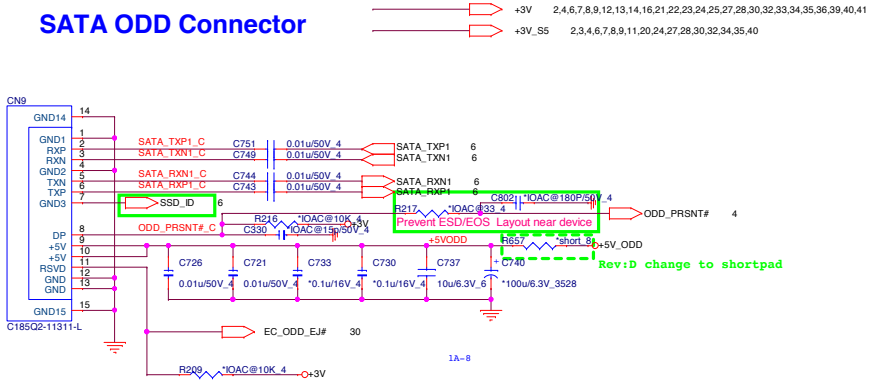
Quanta Computer Inc.
PROJECT : ZAA

Size	Document Number	Rev
	ALC255/HP/SPK	1A
Date: Monday, March 28, 2016	Sheet 25 of 48	

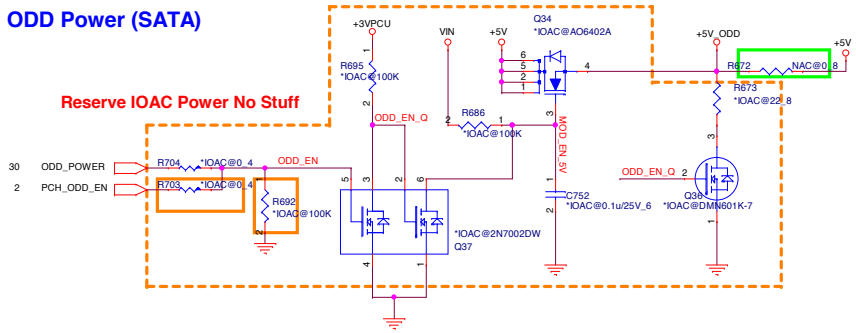
2.5" SATA HDD (HDD)



SATA ODD Connector



ODD Power (SATA)

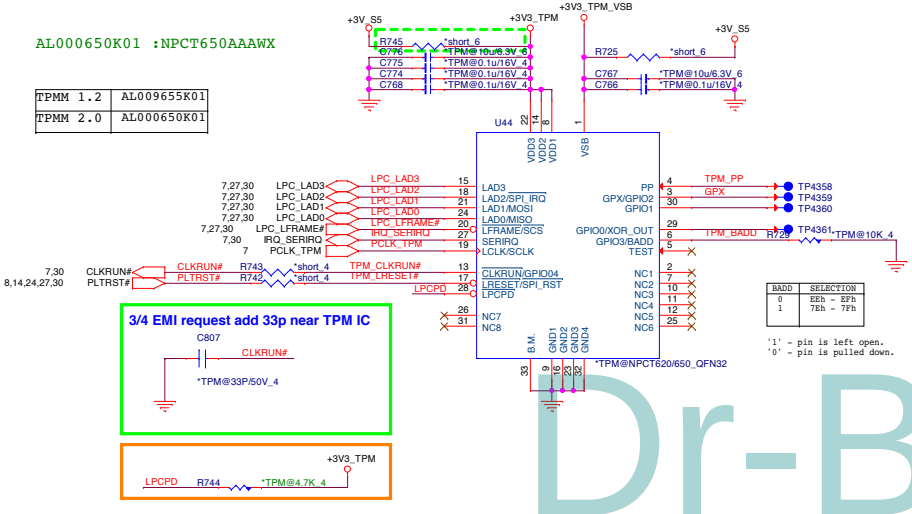


TPM NPCT650 (TPM)

SP@ BOM周邊上NPCT650
A,B,C P/N:AL009655K01(SLB9655TT1.2- FW4.31)
RAMP P/N: AL000650K01 (NPCT650AAAWX)

AL000650K01 :NPCT650AAAWX

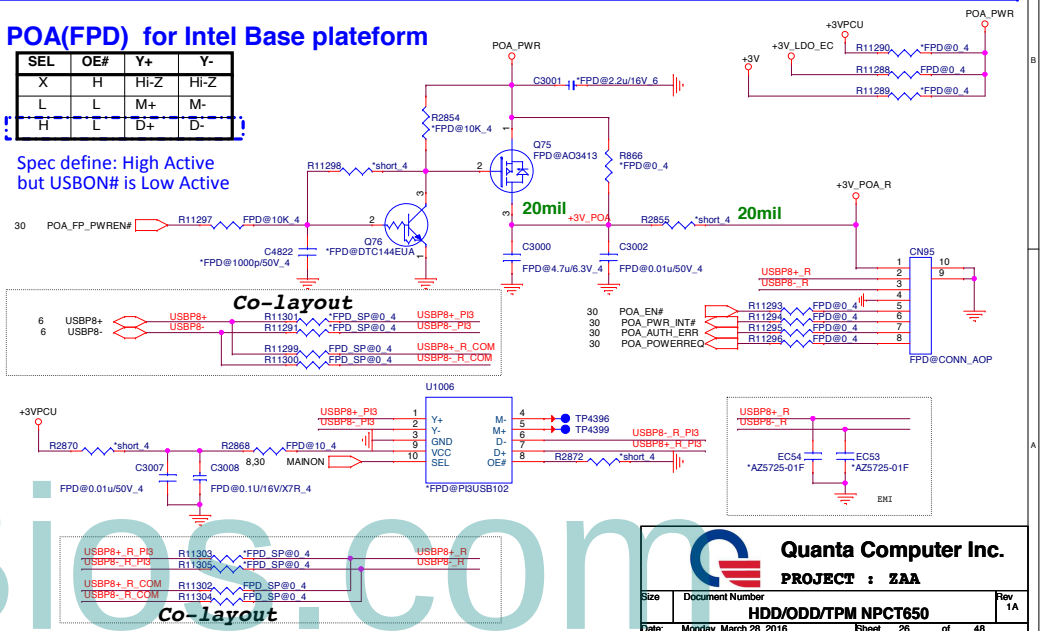
TPMM 1.2	AL009655K01
TPMM 2.0	AL000650K01



POA(FPD) for Intel Base plateform

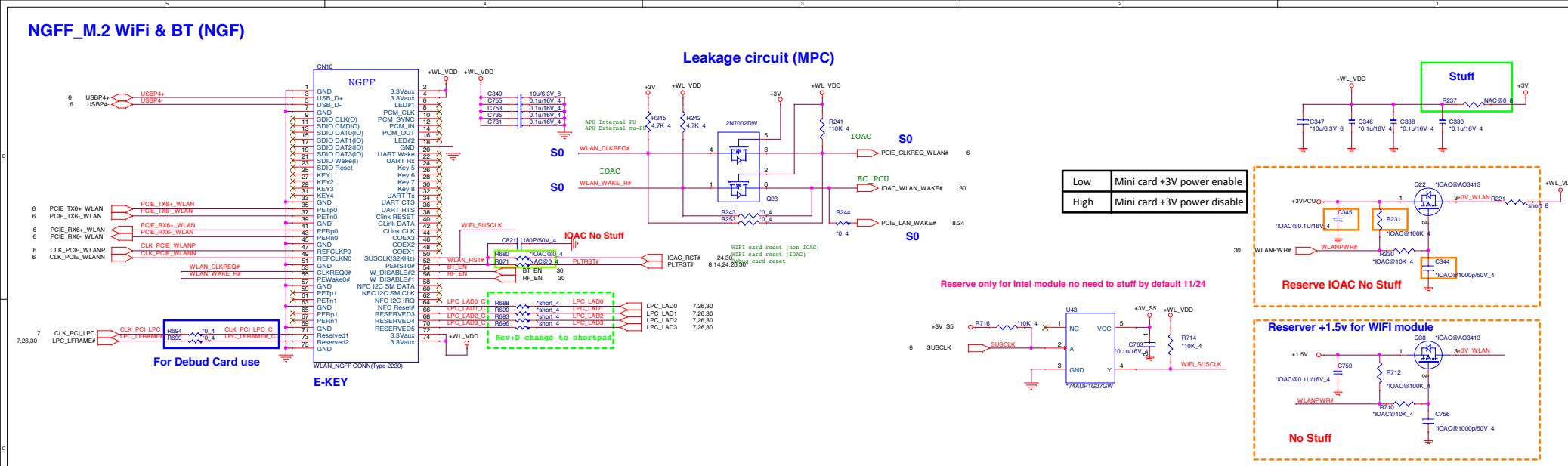
SEL	OE#	Y+	Y-
X	H	Hi-Z	Hi-Z
L	L	M+	M-
H	L	D+	D-

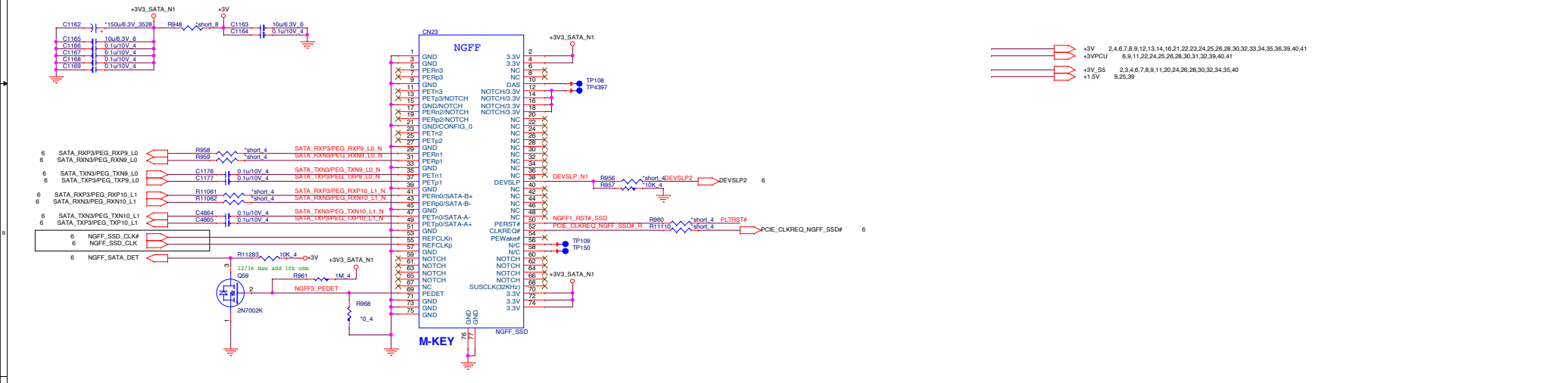
Spec define: High Active
but USBON# is Low Active



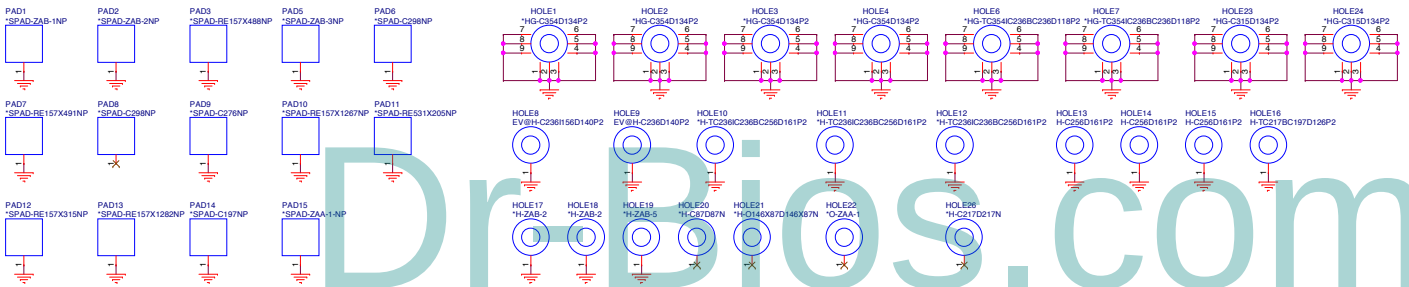
Quanta Computer Inc.
PROJECT : ZAA
Size | Document Number | Rev 1A
HDD/ODD/TPM NPCT650
Date: Monday, March 28, 2016 | Sheet 26 of 48

NGFF_M.2 WiFi & BT (NGF)



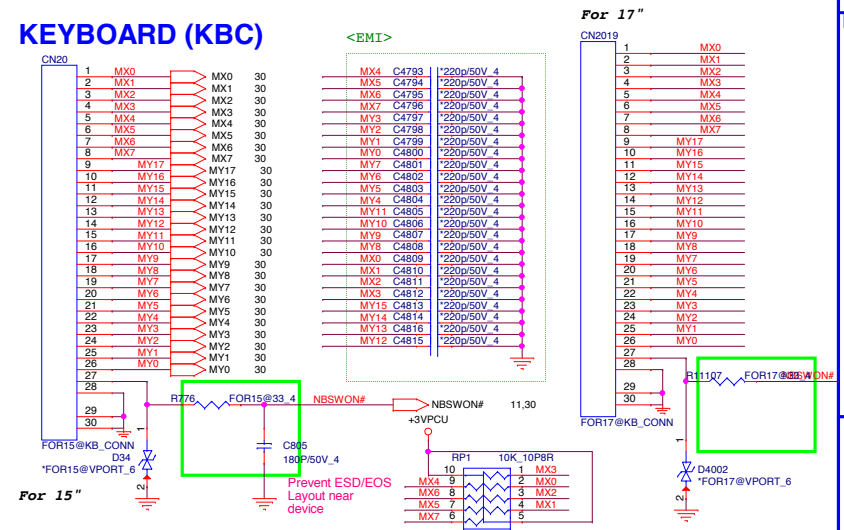


PAD and HOLE

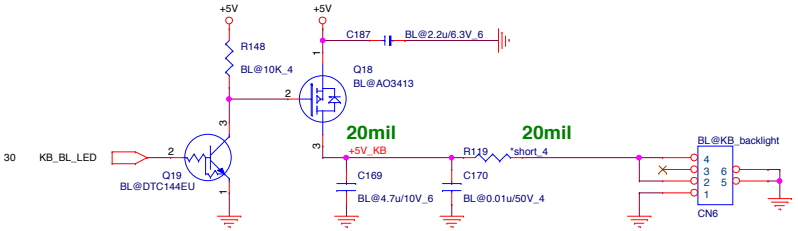


Quanta Computer Inc.
PROJECT : ZAA
Size | Document Number: Mini-Card/WL/3G/SIM | Rev: 1A
Date: Monday, March 28, 2016 | Sheet 27 of 48

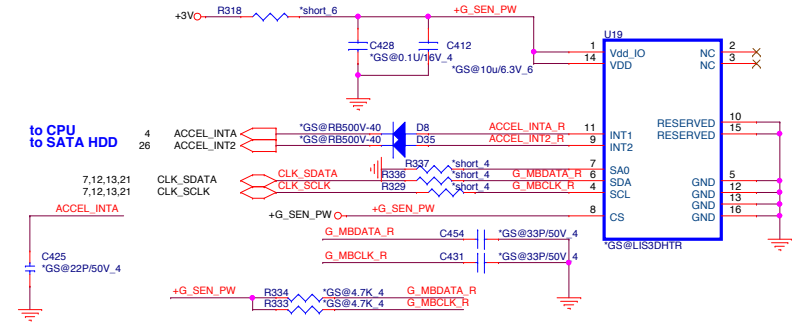
KEYBOARD (KBC)



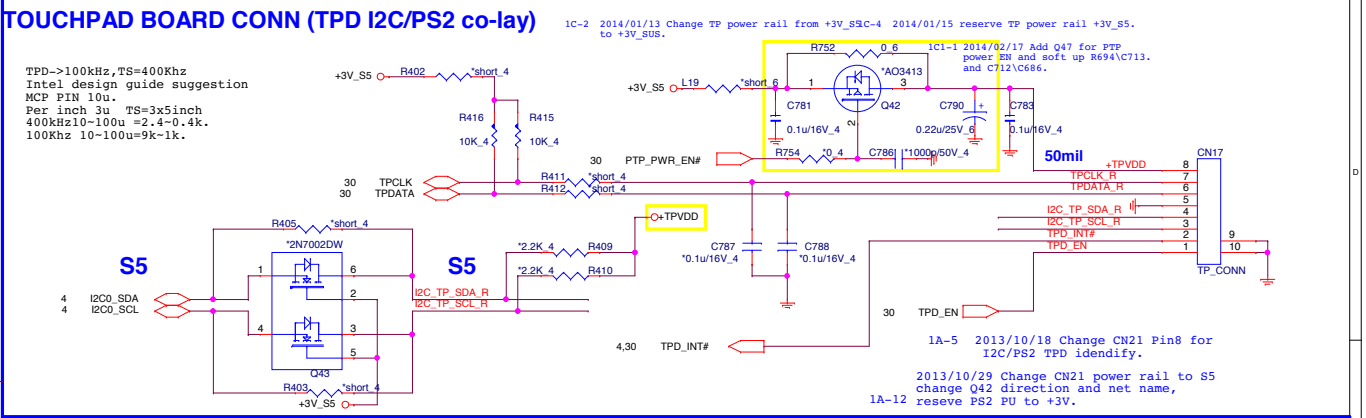
KB_BL LED (KBC)



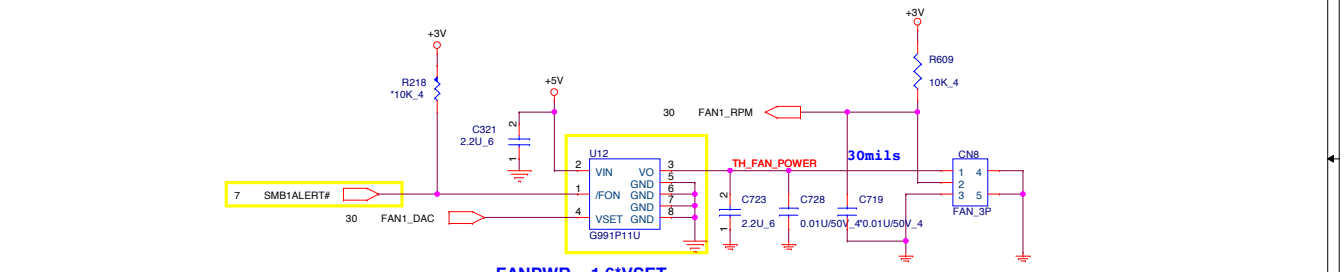
G-sensor(ACS)



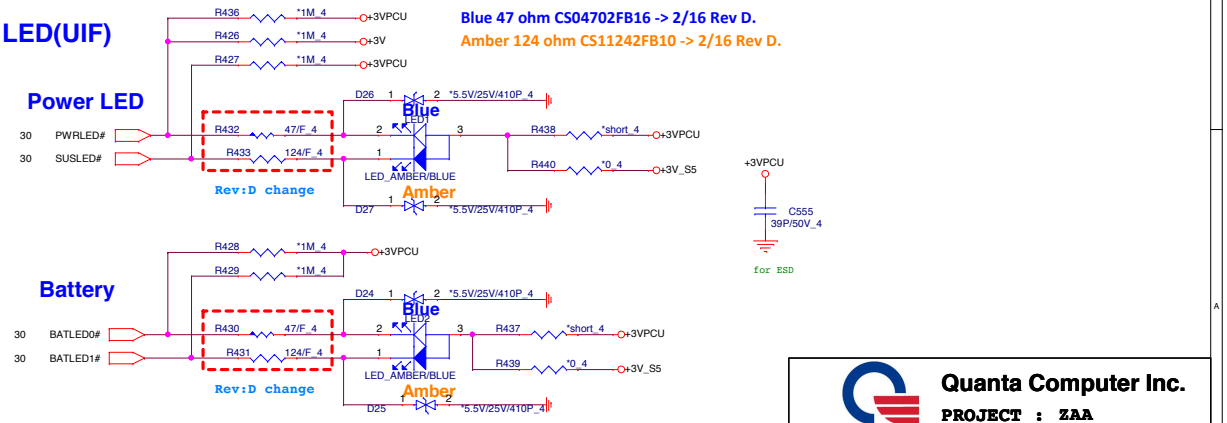
TOUCHPAD BOARD CONN (TPD I2C/PS2 co-lay)



CPU FAN (THM)

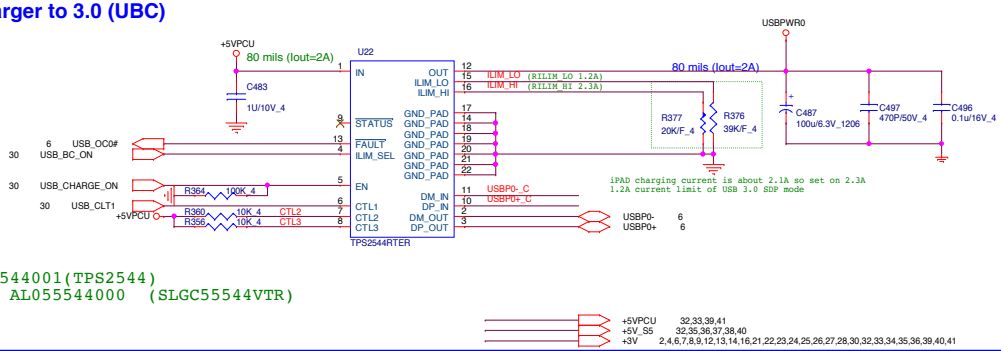


POWER LED(UIF)



Quanta Computer Inc.		
PROJECT : ZAA		
Size	Document Number	Rev
	KB/TP/FAN	1A
Date: Monday, March 28, 2016	Sheet 28 of 48	

USB Charger to 3.0 (UBC)



	CTL1	CTL2	CTL3	ILIM_SEL
SDP	1	1	1	0
CDP	1	1	1	1
DCP	0	1	1	X

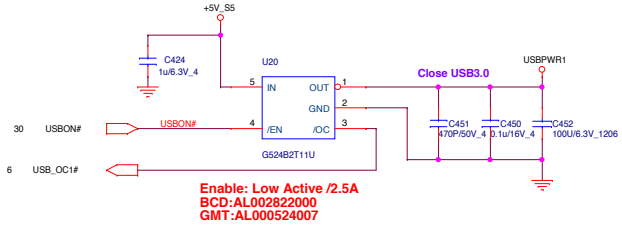
RILIM_LO is optional and the ILIM_LO pin may be left unconnected if the following conditions are met:
1. ILIM_SEL is always set high
2. Load Detection - Port Power Management is not used
3. Mouse / Keyboard wake function is not used
If conditions 1 and 2 are met but the mouse / keyboard wake function is also desired, it is recommended to use RILIM_LO < 80.6 kΩ.
The following equation programs the typical current limit:
(1)
RILIM_XX corresponds to either RILIM_HI or RILIM_LO as appropriate.

$$IOS\_typ(mA) = 50{,}250/\{RILIM\_XX(K\Omega)+0.1\}$$

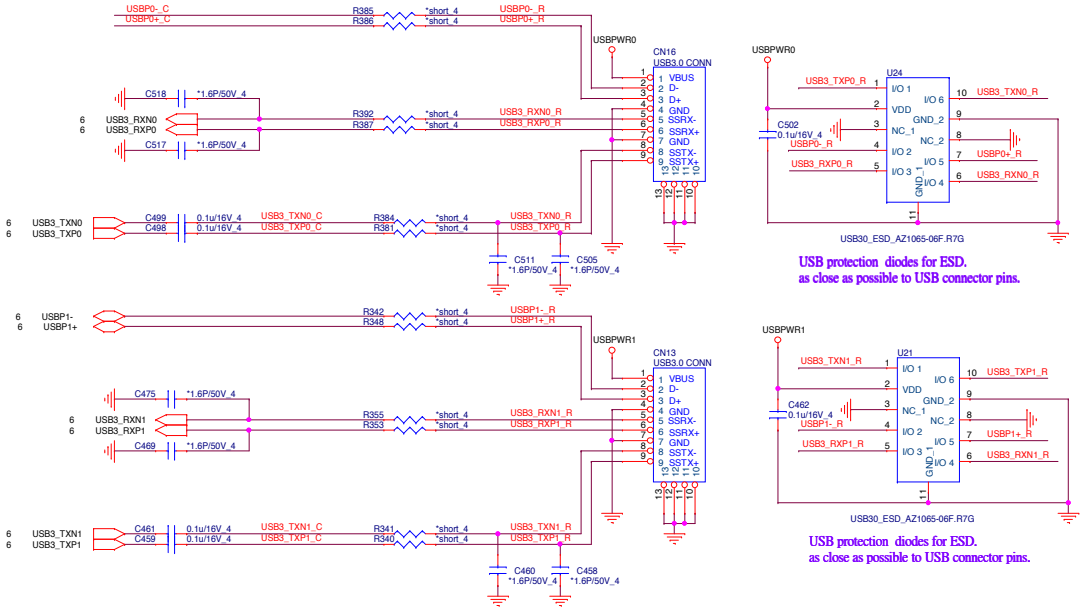
TI:AL002544001(TPS2544)
Silergy: AL055544000 (SLGC55544VTR)

+5VPCU 32,33,39,41
+5V_S5 32,35,36,37,38,40
+3V 2,4,6,7,8,9,12,13,14,16,21,22,23,24,25,26,27,28,30,32,33,34,35,36,39,40,41

USB 3.0 Connector (UB3)



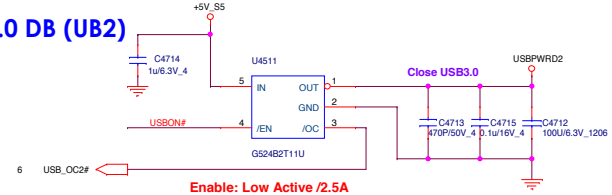
Enable: Low Active /2.5A
BCD:AL002822000
GMT:AL000524007



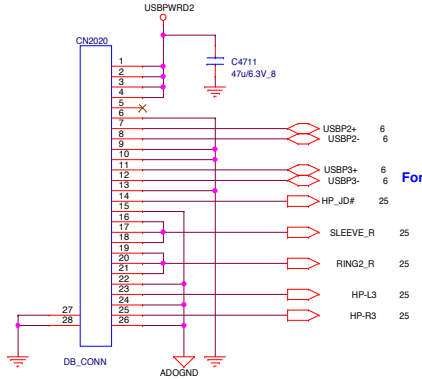
USB protection diodes for ESD.
as close as possible to USB connector pins.

USB protection diodes for ESD.
as close as possible to USB connector pins.

USB2.0 DB (UB2)



Enable: Low Active /2.5A
BCD:AL002822000
GMT:AL000524007



Quanta Computer Inc.
PROJECT : ZAA

Size	Document Number	Rev
	USB3/Charger/CR/USB2 DB	1A

Date: Monday, March 28, 2016 Sheet 29 of 48

EC(KBC)

11/11 FAE suggestion pin106
+3V_RTC change to +3VPCU_EC

+3VPCU_EC and +3V_RTC minimum trace width 12mils.

12 mils

IT8987E/CX
LQFP

AJ089870F02 IT8987E/CX

Output for type-c Apling ridge reset timming "Low" Active

Rev:D Add

SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH/VGA
SM Bus 3	
SM Bus 4	

SM BUS PU(KBC)

Battery module

UMA& VGA SKU
Need Stuff

HWPG(KBC)

DDR=1.5V, D1 DNP and D2 POP
DDR=1.35V, D1 POP and D2 DNP

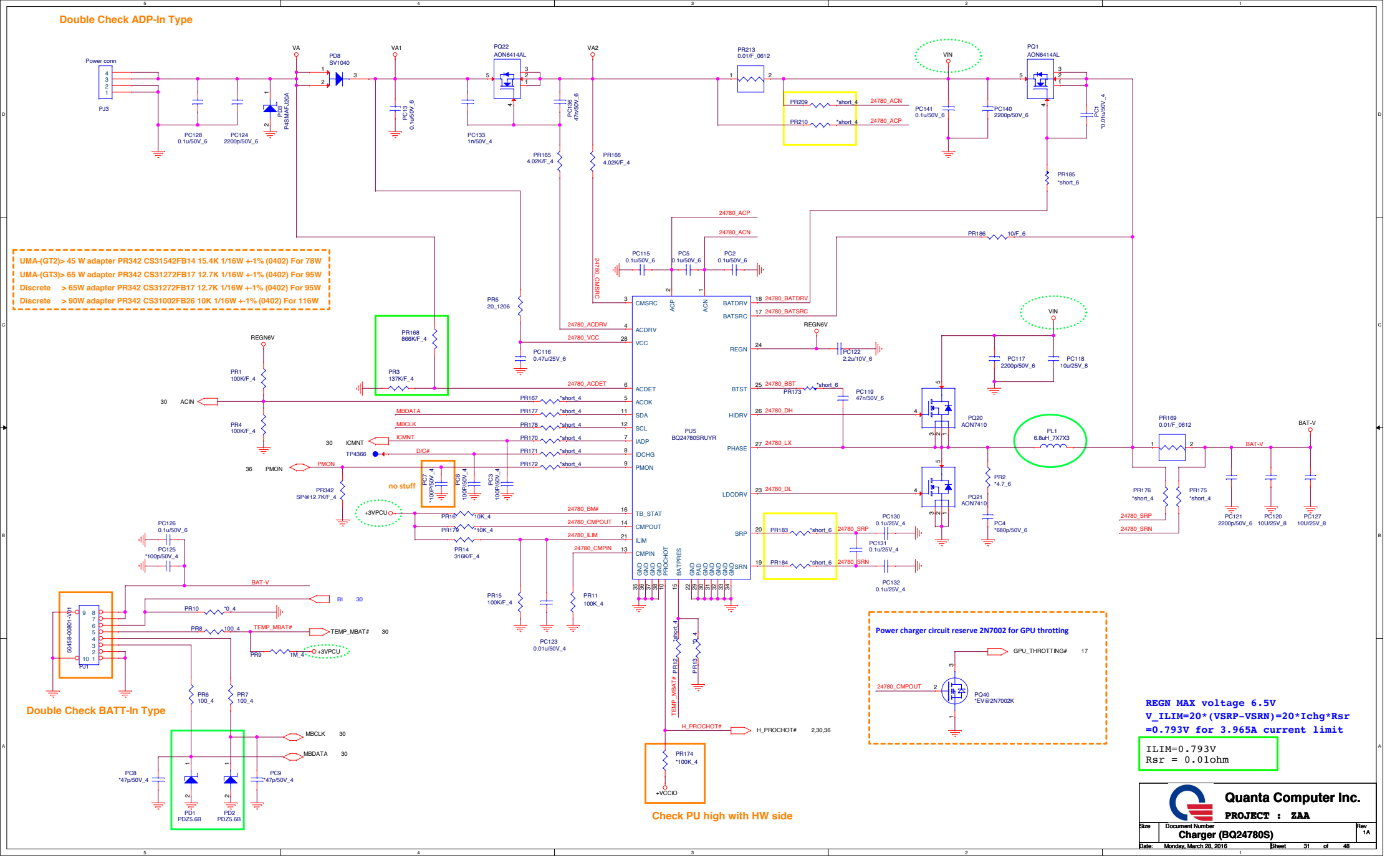
Reset SW (FSW)

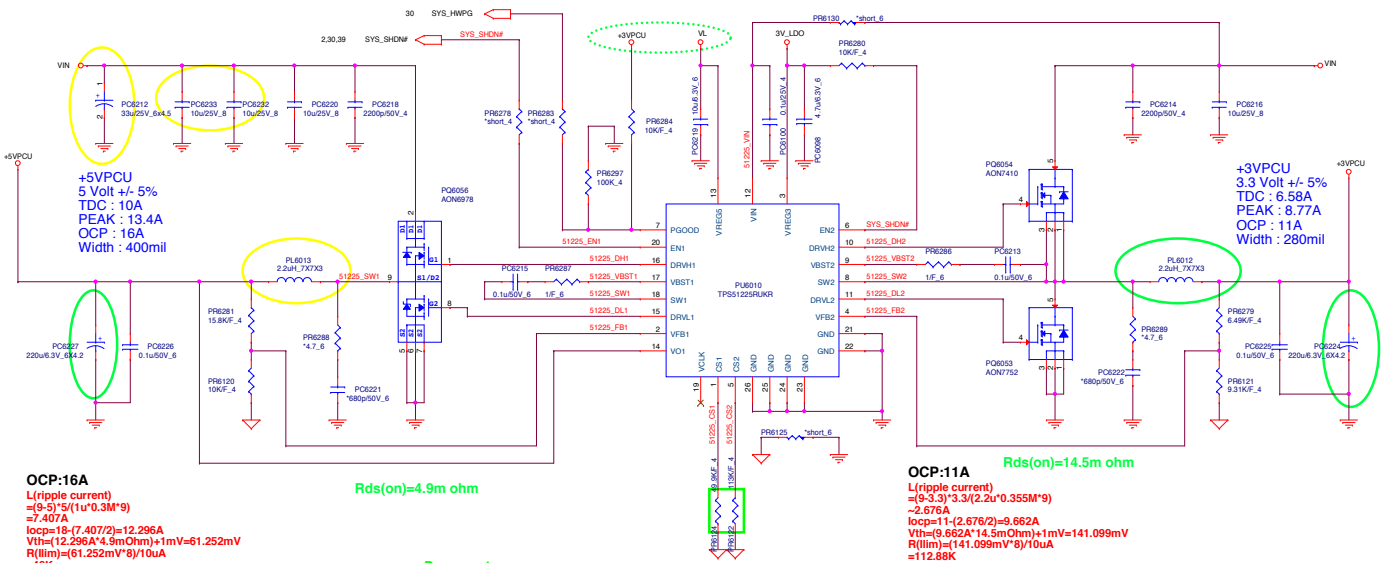
Reserve switch for test (MP remove)

Reserve no stuff

Battery Detect Switch

Quanta Computer Inc.			
PROJECT : ZAA			
Size	Document Number	KBC IT8587	Rev 1A
Date: Monday, March 28, 2016	Sheet 30 of 48		


Double Check ADP-In Type
UMA-(GT2)> 45 W adapter PR342 CS31542FB14 15.4K 1/16W +-1% (0402) For 78W
UMA-(GT3)> 65 W adapter PR342 CS31272FB17 12.7K 1/16W +-1% (0402) For 95W
Discrete > 65W adapter PR342 CS31272FB17 12.7K 1/16W +-1% (0402) For 95W
Discrete > 90W adapter PR342 CS31002FB26 10K 1/16W +-1% (0402) For 116W
Power conn
PJ3
PD8 SV1040
PD4 P4SMAFL20A
PQ22 AON6414AL
PQ1 AON6414AL
PR213 0.01/F_0612
PR209 *short_4
PR210 *short_4
24780_ACN
24780_ACP
PC141 0.1u/50V_6
PC140 2200p/50V_6
PC1 *0.01u/50V_4
PR185 *short_6
PR186 10/F_6
PC128 0.1u/50V_6
PC124 2200p/50V_6
PC13 0.1u/50V_6
PC133 1n/50V_4
PC136 47n/50V_6
PR165 4.02K/F_4
PR166 4.02K/F_4
PC115 0.1u/50V_6
PC5 0.1u/50V_6
PC2 0.1u/50V_6
PR5 20_1206
PC116 0.47u/25V_6
PR168 866K/F_4
PR3 137K/F_4
PR1 100K/F_4
PR4 100K/F_4
REGN6V
ACIN
PU5 BQ24780SRUYR
CMSRC
ACDRV
VCC
ACDET
ACOK
SDA
SCL
IADP
IDCHG
PMON
TB_STAT
CMPOUT
ILIM
CMPIN
PROCHOT
BATPRES
BATDRV
BATSRC
REGN
BTST
HIDRV
PHASE
LDODRV
SRP
SRN
PC122 2.2u/10V_6
PR173 *short_6
PC119 47n/50V_6
PQ20 AON7410
PQ21 AON7410
PR2 *4.7_6
PC4 *680p/50V_6
PL1 6.8uH_7X7X3
PC117 2200p/50V_6
PC118 10u/25V_8
PR169 0.01/F_0612
PR176 *short_4
PR175 *short_4
PC121 2200p/50V_6
PC120 10U/25V_8
PC127 10U/25V_8
BAT-V
24780_SRP
24780_SRN
PR342 SP@12.7K/F_4
no stuff
PC7 *100P/50V_4
PC6 100P/50V_4
PC3 100P/50V_4
+3VPCU
TP4366
D/C#
ICMNT
PMON
PR16 10K_4
PR17 *10K_4
PR14 316K/F_4
PR15 100K/F_4
PR11 100K_4
PC123 0.01u/50V_4
PC130 0.1u/25V_4
PC131 0.1u/25V_4
PC132 0.1u/25V_4
PC126 0.1u/50V_6
PC125 *100p/50V_4
PR10 *0_4
PR8 100_4
PR9 1M_4
TEMP_MBAT#
BI
50458-00801-V01
PJ1
PR6 100_4
PR7 100_4
MBCLK
MBDATA
PC8 *47p/50V_4
PC9 *47p/50V_4
PD1 PDZ5.6B
PD2 PDZ5.6B
PR12 *short_4
PR13 0_4
H_PROCHOT#
PR174 *100K_4
+VCCIO
Check PU high with HW side
Power charger circuit reserve 2N7002 for GPU throtting
GPU_THROTTING#
PQ40 *EV@2N7002K
REGN MAX voltage 6.5V
V_ILIM=20*(VSRP-VSRN)=20*Ichg*Rsr
=0.793V for 3.965A current limit
ILIM=0.793V
Rsr = 0.01ohm
Quanta Computer Inc.
PROJECT : ZAA
Charger (BQ24780S)
Rev 1A
Monday, March 28, 2016
Sheet 31 of 48



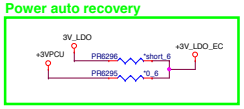
OCP:16A

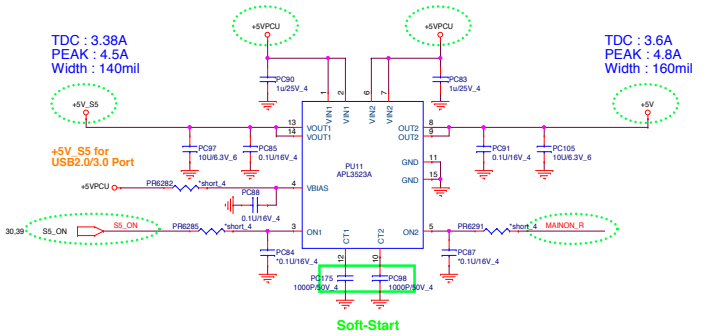
L(ripple current)
=(9-5)*5/(1u*0.3M*9)
=7.407A
Iocp=18-(7.407/2)=12.296A
Vth=(12.296A*4.9mOhm)+1mV=61.252mV
R(Ilim)=(61.252mV*8)/10uA
~49K

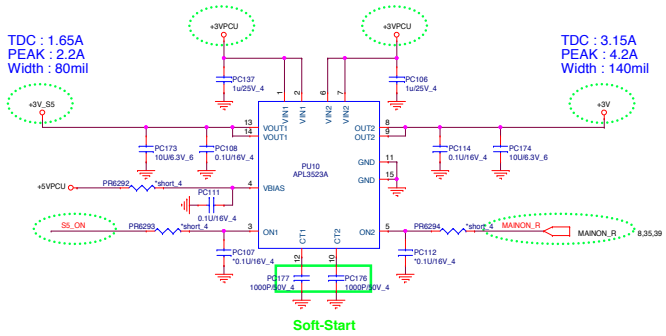
OCP:11A

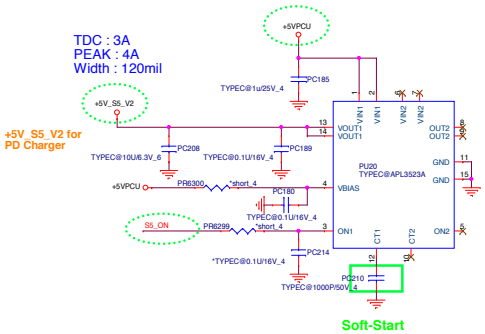
L(ripple current)
=(9-3.3)*3.3/(2.2u*0.355M*9)
~2.676A
Iocp=11-(2.676/2)=9.662A
Vth=(9.662A*14.5mOhm)+1mV=141.099mV
R(Ilim)=(141.099mV*8)/10uA
=112.88K

Power auto recovery

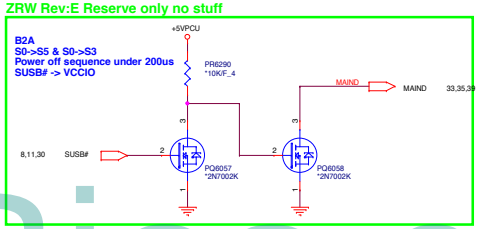




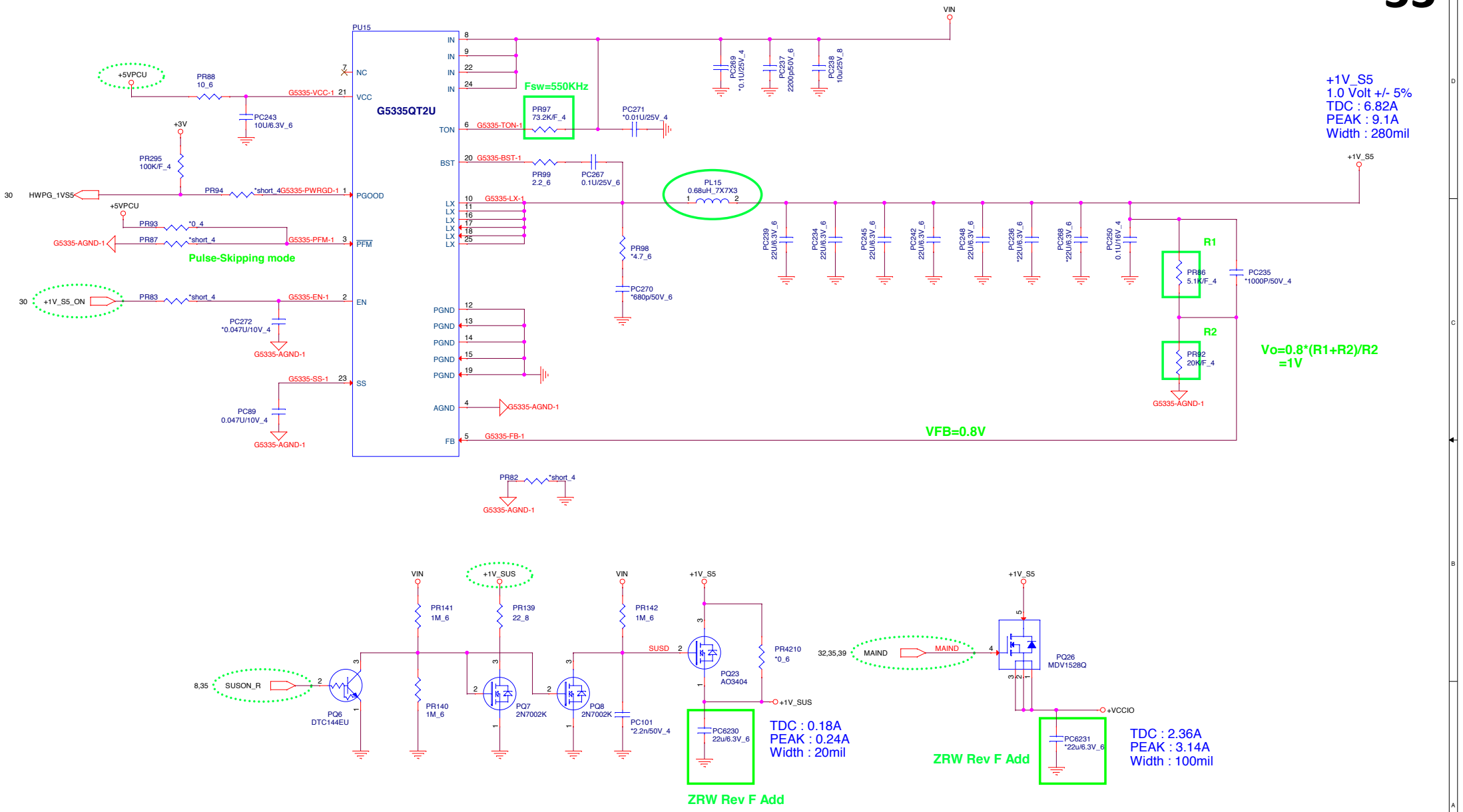




ZRW Rev:E Reserve only no stuff

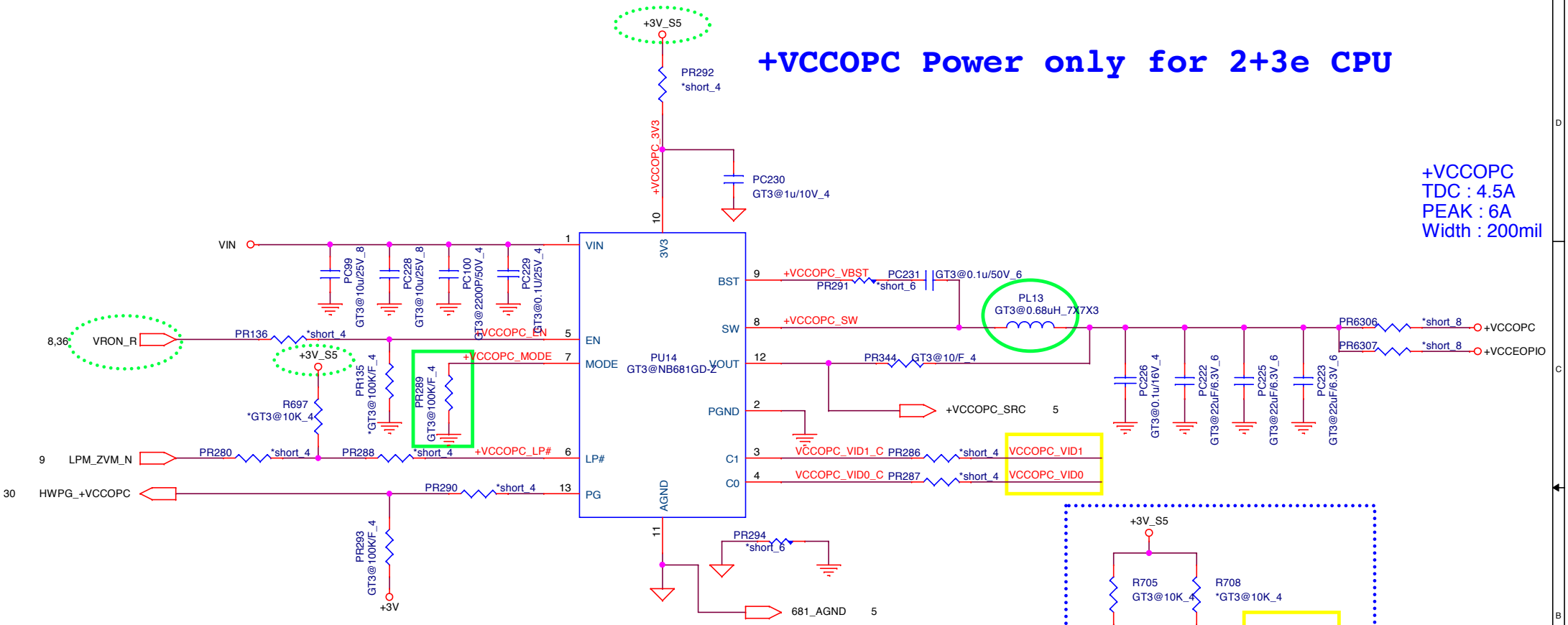


Quanta Computer Inc.			
PROJECT : ZAA			
Size	Document Number		Rev
	)SYSTEM 5V/3V (RT6575AGQW)		1A
Date: Monday, March 28, 2016		Sheet 32 of 48	



Quanta Computer Inc.		
PROJECT : ZAA		
Size	Document Number: +1V_S5 (G5335QT2U)	Rev: 1A
Date: Monday, March 28, 2016	Sheet 33 of 48	

+VCCOPC Power only for 2+3e CPU



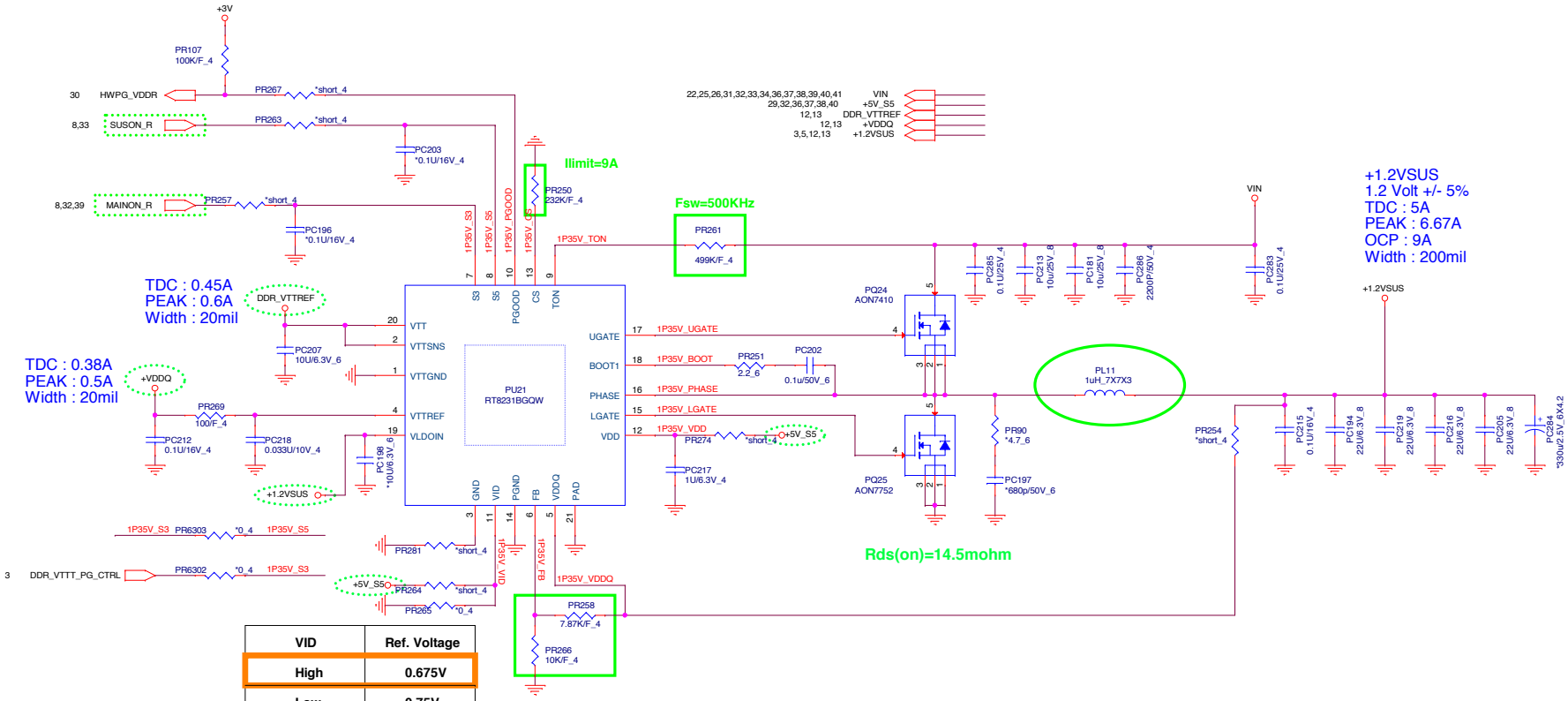
Mode	VR Rail
0 ohm	VCCIO
Floating	PRIMCORE
100K	EDRAM/EOPIO
150K	Other

	LP#	C1	C0	Vo
VCCEDRAM	0	X	X	0V
	1	0	0	0.8V(MSM)
	1	0	1	0.95V
	1	1	0	1.0V
	1	1	1	1.05V

5 +VCCOPC
22,25,26,31,32,33,35,36,37,38,39,40,41 VIN
2,4,6,7,8,9,12,13,14,16,21,22,23,24,25,26,27,28,30,32,33,35,36,39,40,41 +3V
2,3,4,6,7,8,9,11,20,24,26,27,28,30,32,35,40 +3V_S5

Quanta Computer Inc.
PROJECT : ZAA

Size	Document Number	Rev
	+VCCOPC (NB681GD-Z)	1A
Date: Monday, March 28, 2016	Sheet 34 of 48	



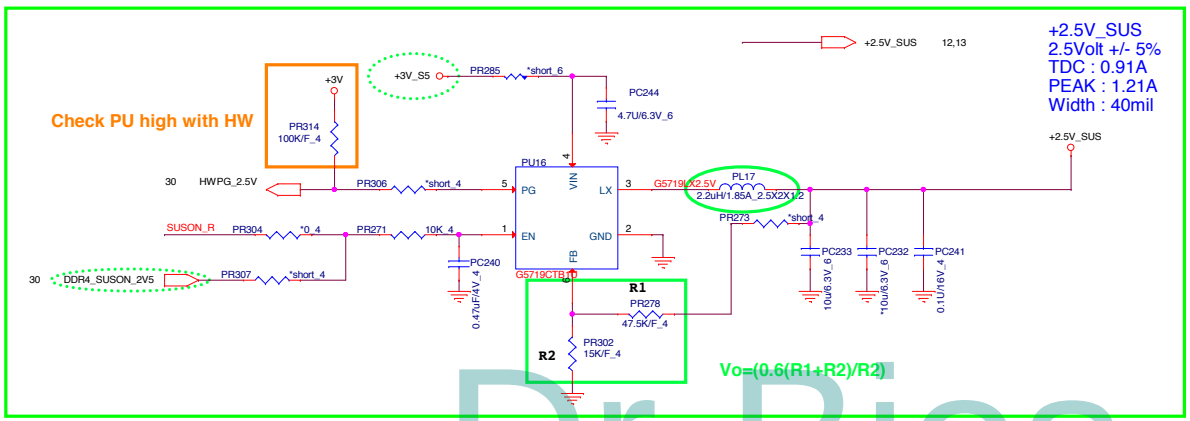
VID	Ref. Voltage
High	0.675V
Low	0.75V

OCP=9A
L ripple current
=(19-1.2)*1.2/(1u*500k*19)
=2.248A
Vtrip=9-(2.248/2)*14.5mohm
=114.202mV
Rlimit=114.202mV/5uA*10=228.4Kohm

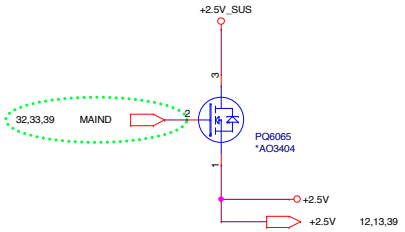
DDR=1.2V
PR255=7.87K/F_4
PR240=10K/F_4

	S3	S5	VDDQ	VTTREF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

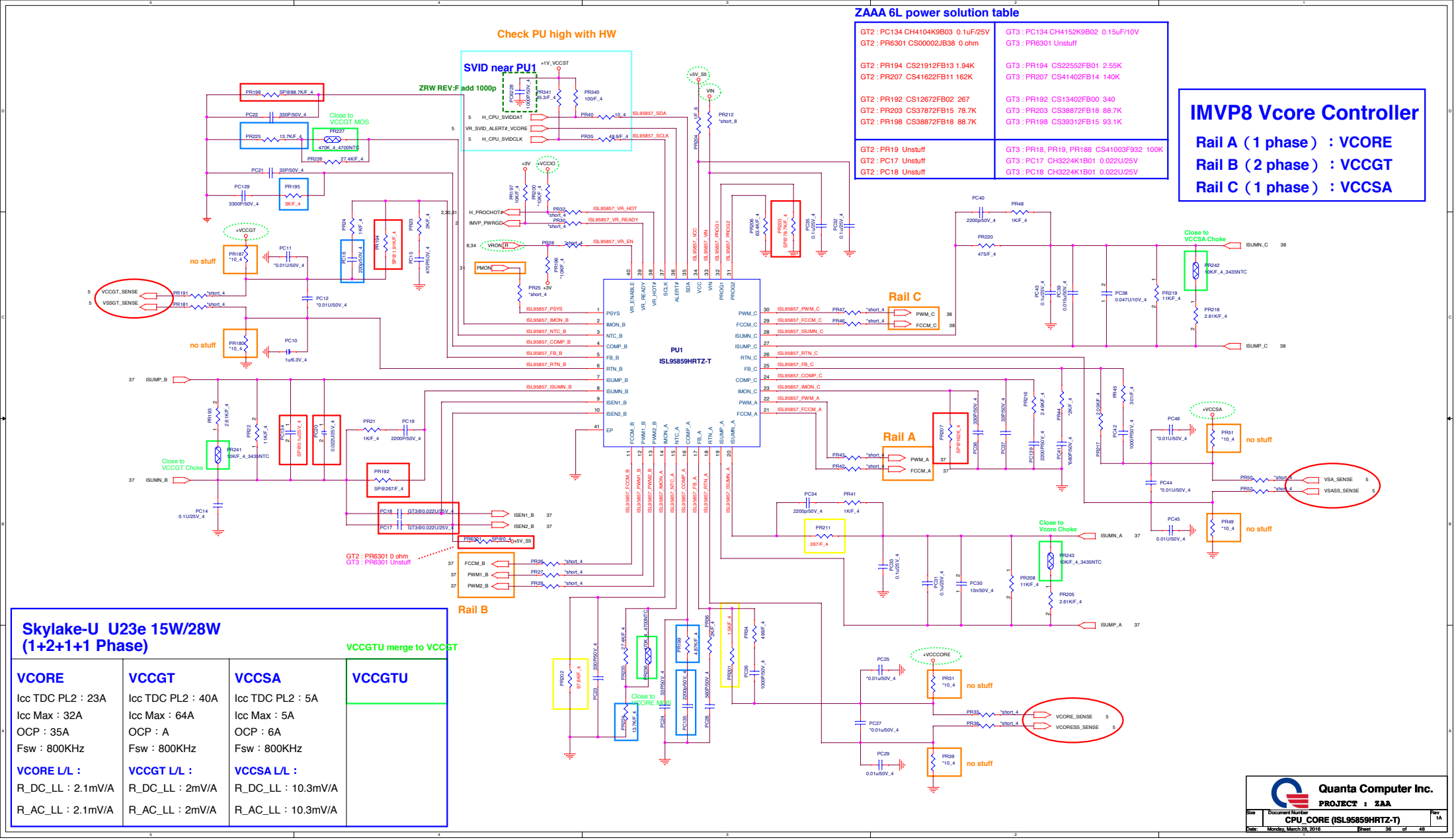
+2.5VSUS Power Rail For DDR4



10/26 Reserve +2.5V for DDR4 VDDSPD

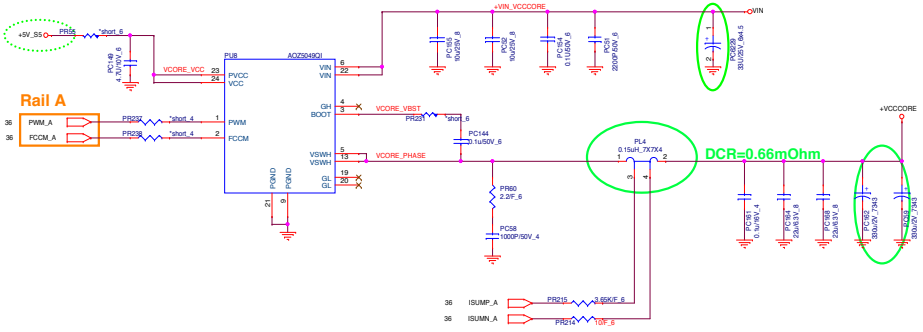


Quanta Computer Inc.
PROJECT : ZAA
Size | Document Number: DDR4_+1.2VSUS (RT8231BGQW) | Rev 1A
Date: Monday, March 28, 2016 | Sheet 35 of 48


Check PU high with HW
SVID near PU1
ZRW REV:F add 1000p
ZAAA 6L power solution table
GT2 : PC134 CH4104K9B03 0.1uF/25V
GT2 : PR6301 CS00002JB38 0 ohm
GT2 : PR194 CS21912FB13 1.94K
GT2 : PR207 CS41622FB11 162K
GT2 : PR192 CS12672FB02 267
GT2 : PR203 CS37872FB15 78.7K
GT2 : PR198 CS38872FB18 88.7K
GT2 : PR19 Unstuff
GT2 : PC17 Unstuff
GT2 : PC18 Unstuff
GT3 : PC134 CH4152K9B02 0.15uF/10V
GT3 : PR6301 Unstuff
GT3 : PR194 CS22552FB01 2.55K
GT3 : PR207 CS41402FB14 140K
GT3 : PR192 CS13402FB00 340
GT3 : PR203 CS38872FB18 88.7K
GT3 : PR198 CS39312FB15 93.1K
GT3 : PR18, PR19, PR188 CS41003F932 100K
GT3 : PC17 CH3224K1B01 0.022U/25V
GT3 : PC18 CH3224K1B01 0.022U/25V
IMVP8 Vcore Controller
Rail A (1 phase) : VCORE
Rail B (2 phase) : VCCGT
Rail C (1 phase) : VCCSA
PU1
ISL95859HRTZ-T
Rail A
Rail B
Rail C
Close to VCCGT MOS
Close to VCCGT Choke
Close to VCCSA Choke
Close to Vcore Choke
Close to VCORE MOS
no stuff
GT2 : PR6301 0 ohm
GT3 : PR6301 Unstuff
Skylake-U U23e 15W/28W
(1+2+1+1 Phase)
VCCGTU merge to VCCGT
VCORE
Icc TDC PL2 : 23A
Icc Max : 32A
OCP : 35A
Fsw : 800KHz
VCORE L/L :
R_DC_LL : 2.1mV/A
R_AC_LL : 2.1mV/A
VCCGT
Icc TDC PL2 : 40A
Icc Max : 64A
OCP : A
Fsw : 800KHz
VCCGT L/L :
R_DC_LL : 2mV/A
R_AC_LL : 2mV/A
VCCSA
Icc TDC PL2 : 5A
Icc Max : 5A
OCP : 6A
Fsw : 800KHz
VCCSA L/L :
R_DC_LL : 10.3mV/A
R_AC_LL : 10.3mV/A
VCCGTU
Quanta Computer Inc.
PROJECT : ZAA
CPU_CORE (ISL95859HRTZ-T)
Monday, March 28, 2016
Sheet 36 of 48

GT2 : PR19 Unstuff	GT3 : PR19 CS41003F932 100K

VCORE



VCORE

Icc TDC PL2 : 23A

Icc Max : 32A

OCP : 35A

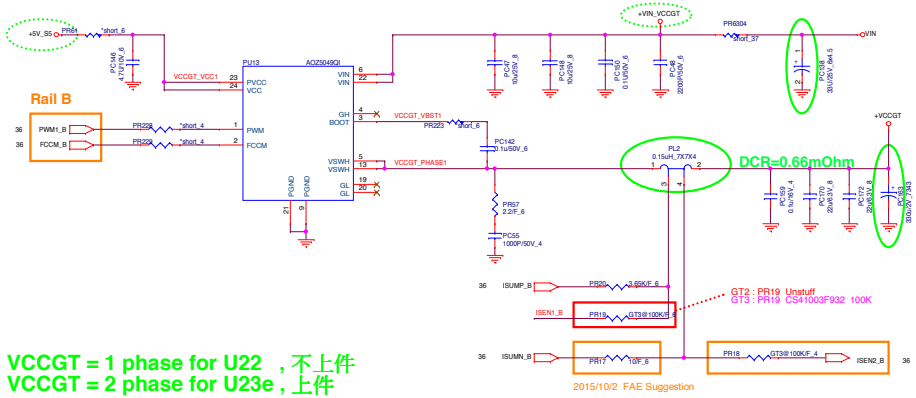
Fsw : 800KHz

VCORE L/L :

R_DC_LL : 2.1mV/A

R_AC_LL : 2.1mV/A

VCCGT



VCCGT

Icc TDC PL2 : 40A

Icc Max : 64A

OCP : A

Fsw : 800KHz

VCCGT L/L :

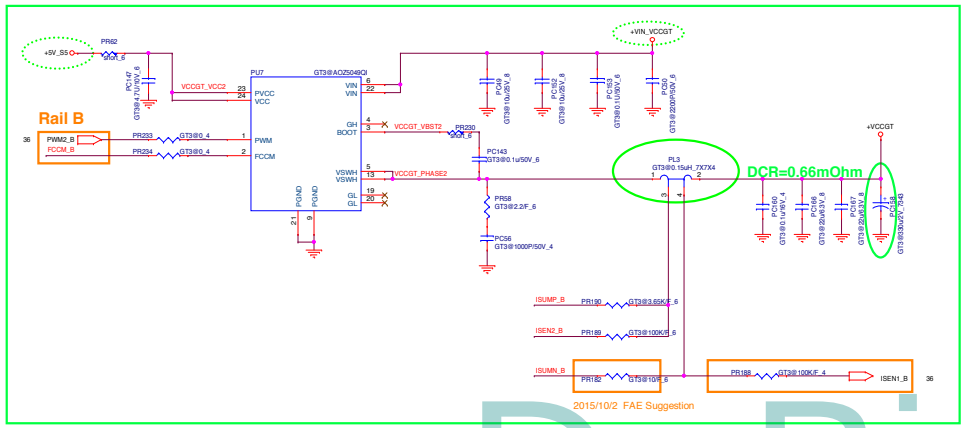
R_DC_LL : 2mV/A

R_AC_LL : 2mV/A

VCCGT = 1 phase for U22 ，不上件

VCCGT = 2 phase for U23e , 上件

2015/10/2 FAE Suggestion



2015/10/2 FAE Suggestion

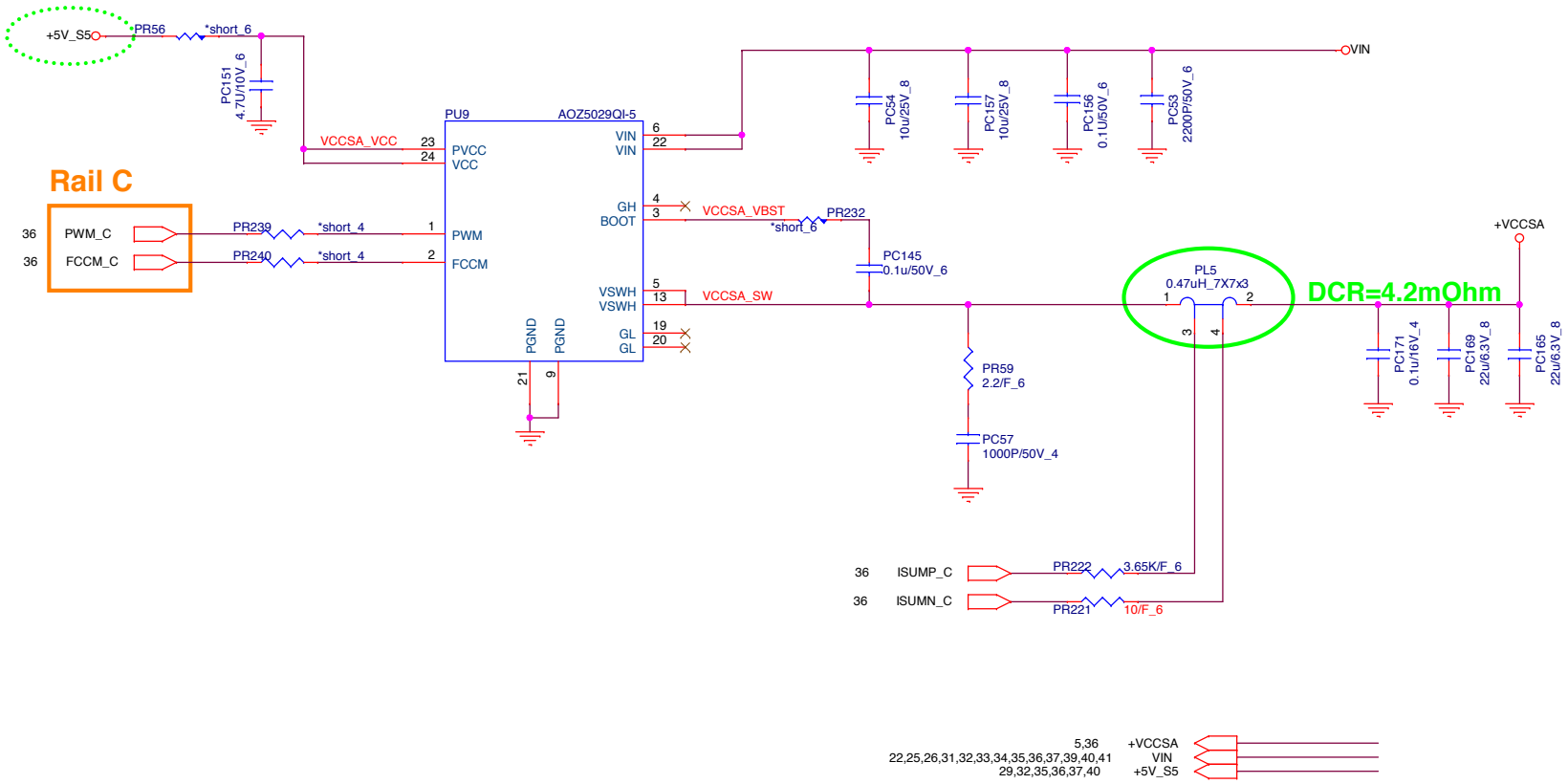
5,36	+VCCCORE	
22,25,26,31,32,33,34,35,36,38,39,40,41	VIN	
5,36	+VCCGT	
29,32,35,36,38,40	+5V_S5	

Quanta Computer Inc.

PROJECT : ZAA

Size	Document Number	Rev
	VCORE/VCCGT (ISL95808HRZ-T)	1A
Date: Monday, March 28, 2016	Sheet 37 of 48	

VCCSA



VCCSA

Icc TDC PL2：5A

Icc Max：5A

OCP：6A

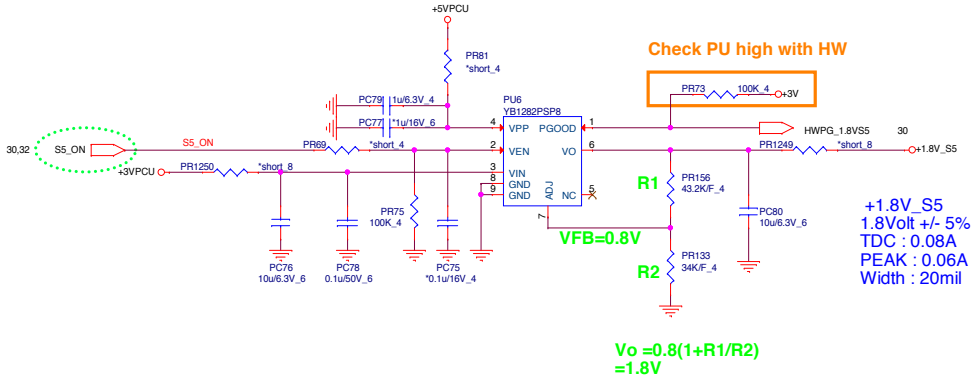
Fsw：800KHz

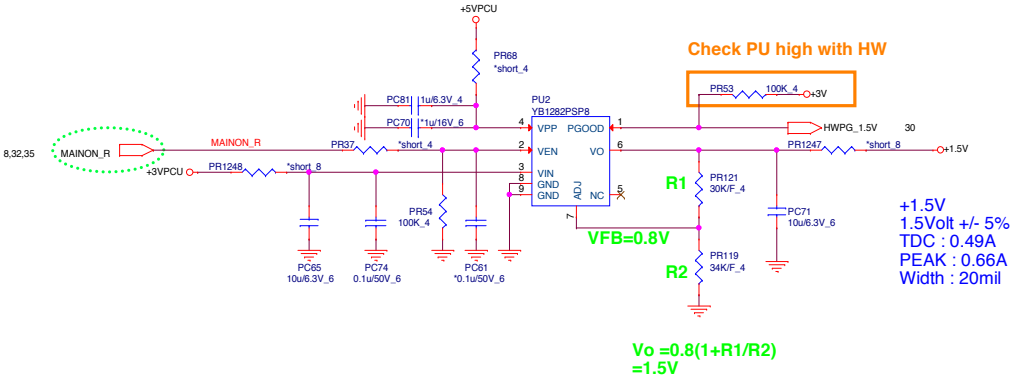
VCCSA L/L：

R_DC_LL：10.3mV/A

R_AC_LL：10.3mV/A

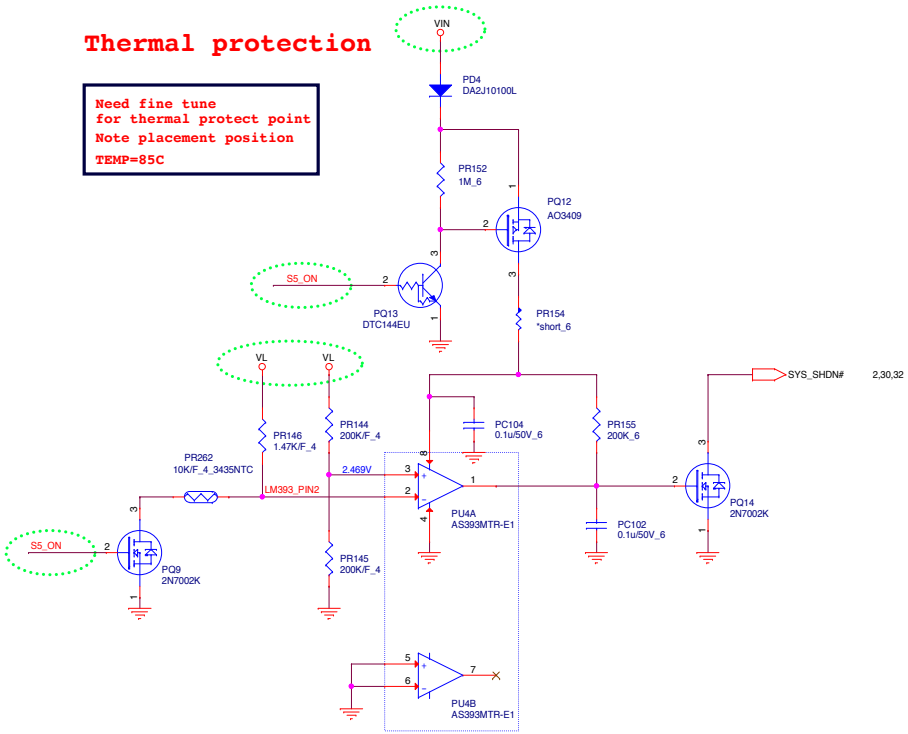
Quanta Computer Inc.		
PROJECT : ZAA		
Size	Document Number: VCCSA (ISL95808HRZ-T)	Rev: 1A
Date: Monday, March 28, 2016	Sheet 38 of 48	





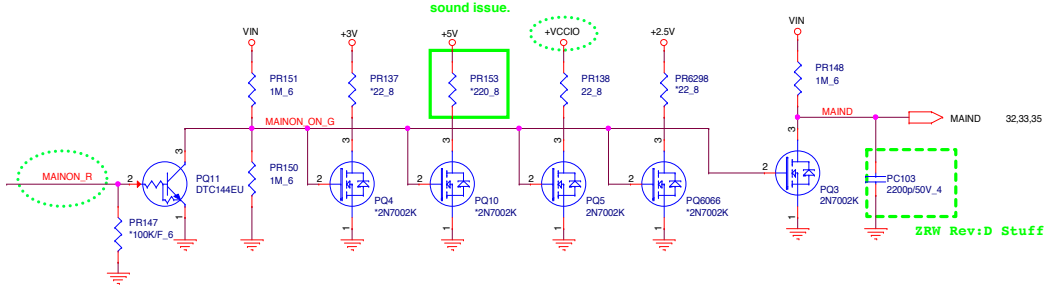
Thermal protection

Need fine tune
for thermal protect point
Note placement position
TEMP=85C



For EC control thermal protection (output 3.3V)

PR153 Change to
220 ohm for bo bo
sound issue.



Quanta Computer Inc.
PROJECT : ZAA

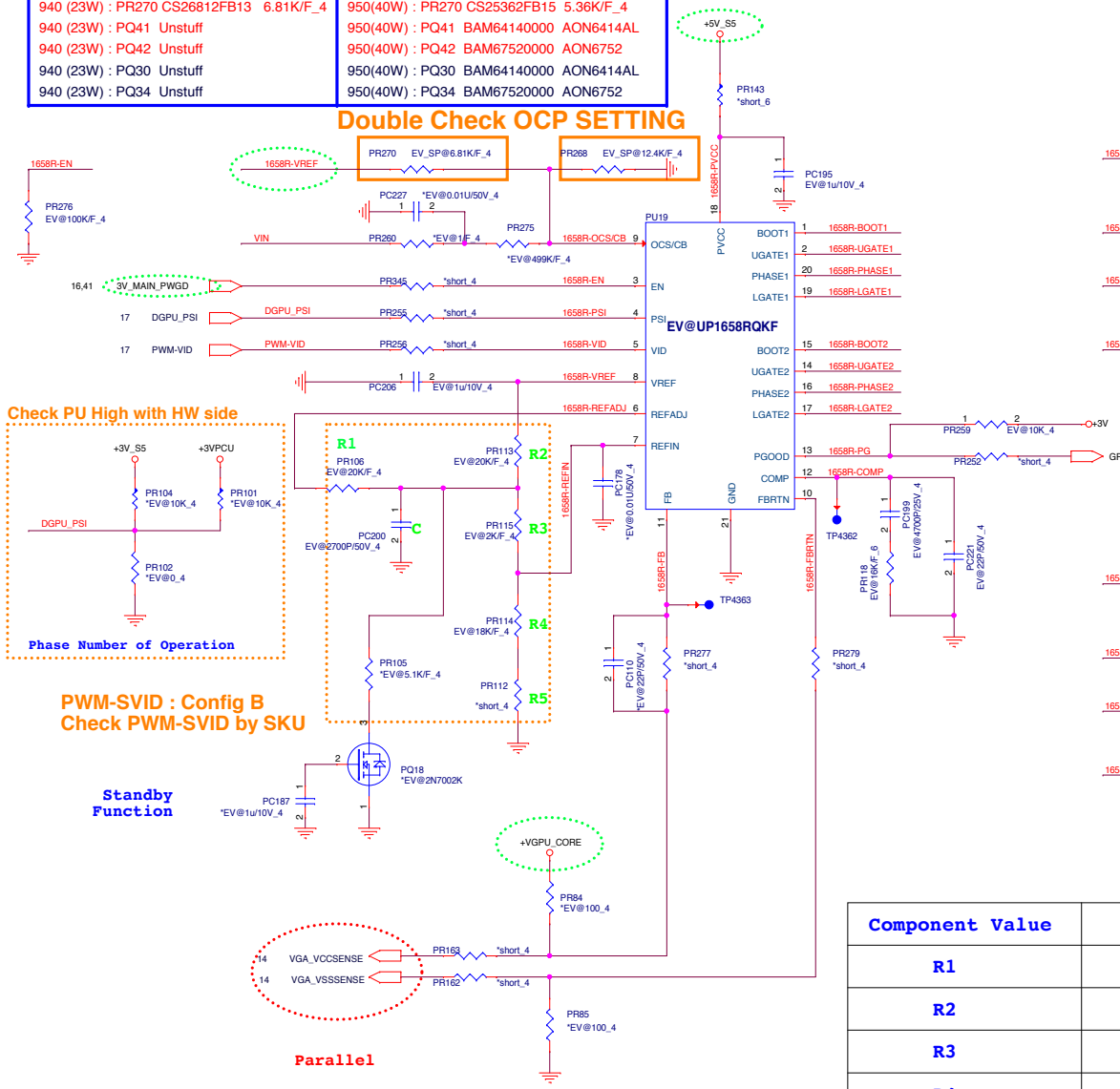
Size	Document Number	Rev
	+1.8V/+1.5V/Thermal Protect	1A

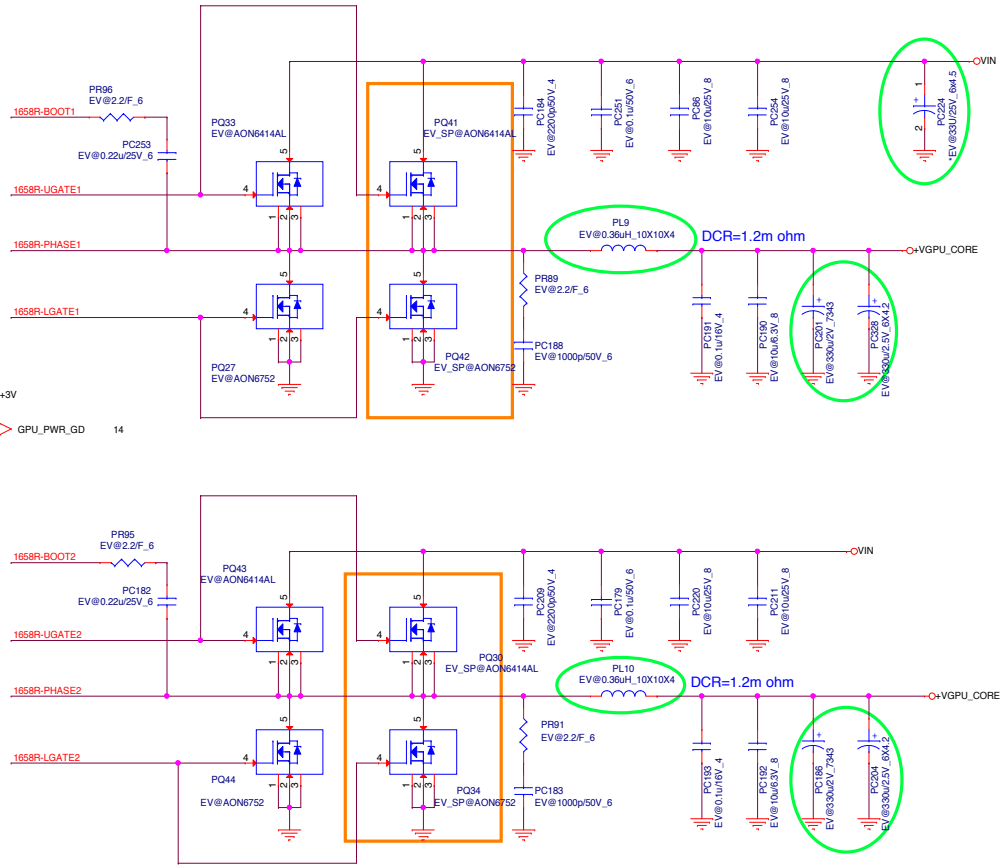
Date: Monday, March 28, 2016 Sheet 39 of 48

ZAAA 6L power solution table

940 (23W) : PR268 CS31242FB13 12.4K/F_4	950(40W) : PR268 CS31002FB26 10K/F_4
940 (23W) : PR270 CS26812FB13 6.81K/F_4	950(40W) : PR270 CS25362FB15 5.36K/F_4
940 (23W) : PQ41 Unstuff	950(40W) : PQ41 BAM64140000 AON6414AL
940 (23W) : PQ42 Unstuff	950(40W) : PQ42 BAM67520000 AON6752
940 (23W) : PQ30 Unstuff	950(40W) : PQ30 BAM64140000 AON6414AL
940 (23W) : PQ34 Unstuff	950(40W) : PQ34 BAM67520000 AON6752

Double Check OCP SETTING





Component	Value	Config B
R1		20K
R2		20K
R3		2K
R4		18K
R5		0-ohm
C		2.7nF

N16S-GT(23W/GDDR5)
OpenVR Config:B

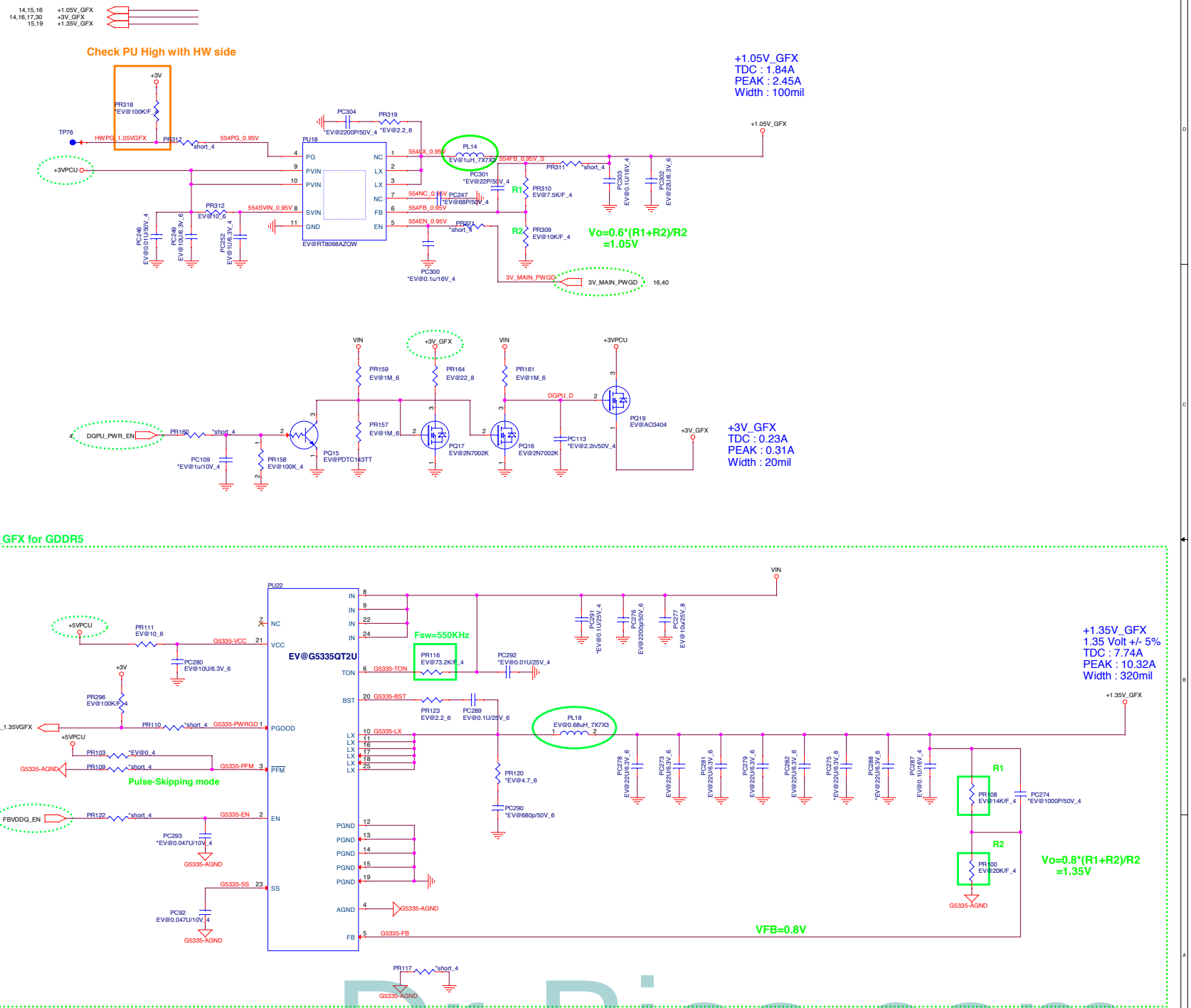
+VGPU_CORE
Countinue current:26.5A
Peak current:53A
OCP:72A
FSW:300KHz
L/L=0mV/A

N16E-GR(GDDR5)
OpenVR Config:B

+VGPU_CORE
Countinue current:62A
Peak current:119A
OCP:144A
FSW:300KHz
L/L=0mV/A

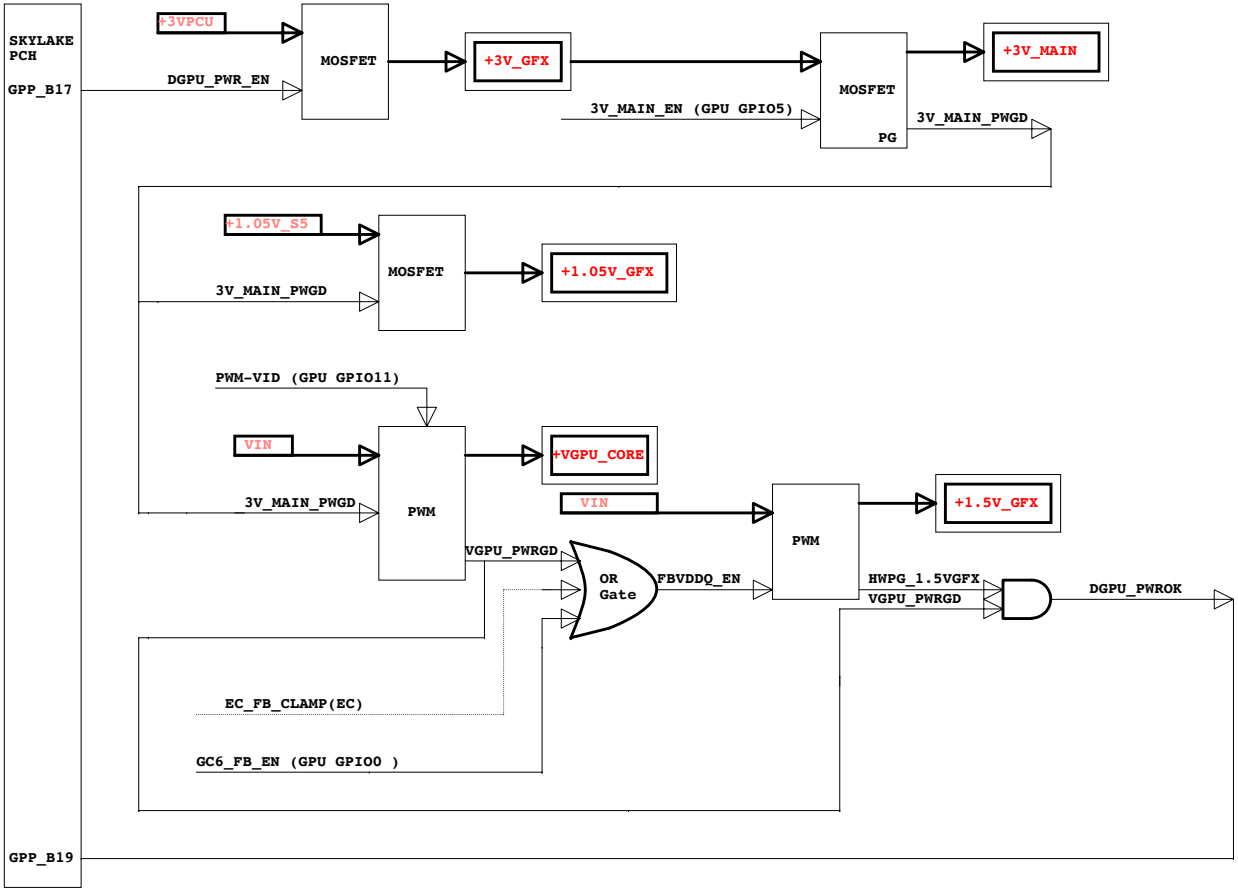
Quanta Computer Inc.
PROJECT : ZAA

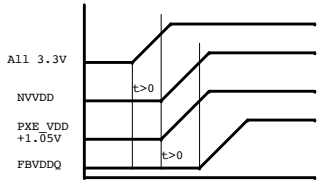
Size	Document Number	Rev
	+VGPU_CORE(UP1658RQKF)	1A
Date: Monday, March 28, 2016	Sheet 40 of 48	



Quanta Computer Inc.			
PROJECT : ZAA			
Size	Document Number		Rev
	+1.35V_GFX/+1.05V_GFX/+3V_GFX		1A
Date: Monday, March 28, 2016	Sheet 41 of 48		

VGA power up sequence

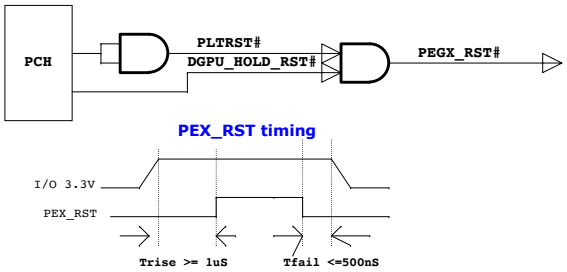




N15x Power on sequance

Notes: -All 3.3V includes all rails powered at 3.3V
-PEX_VDD 1.05V inculdes all rails that are shared

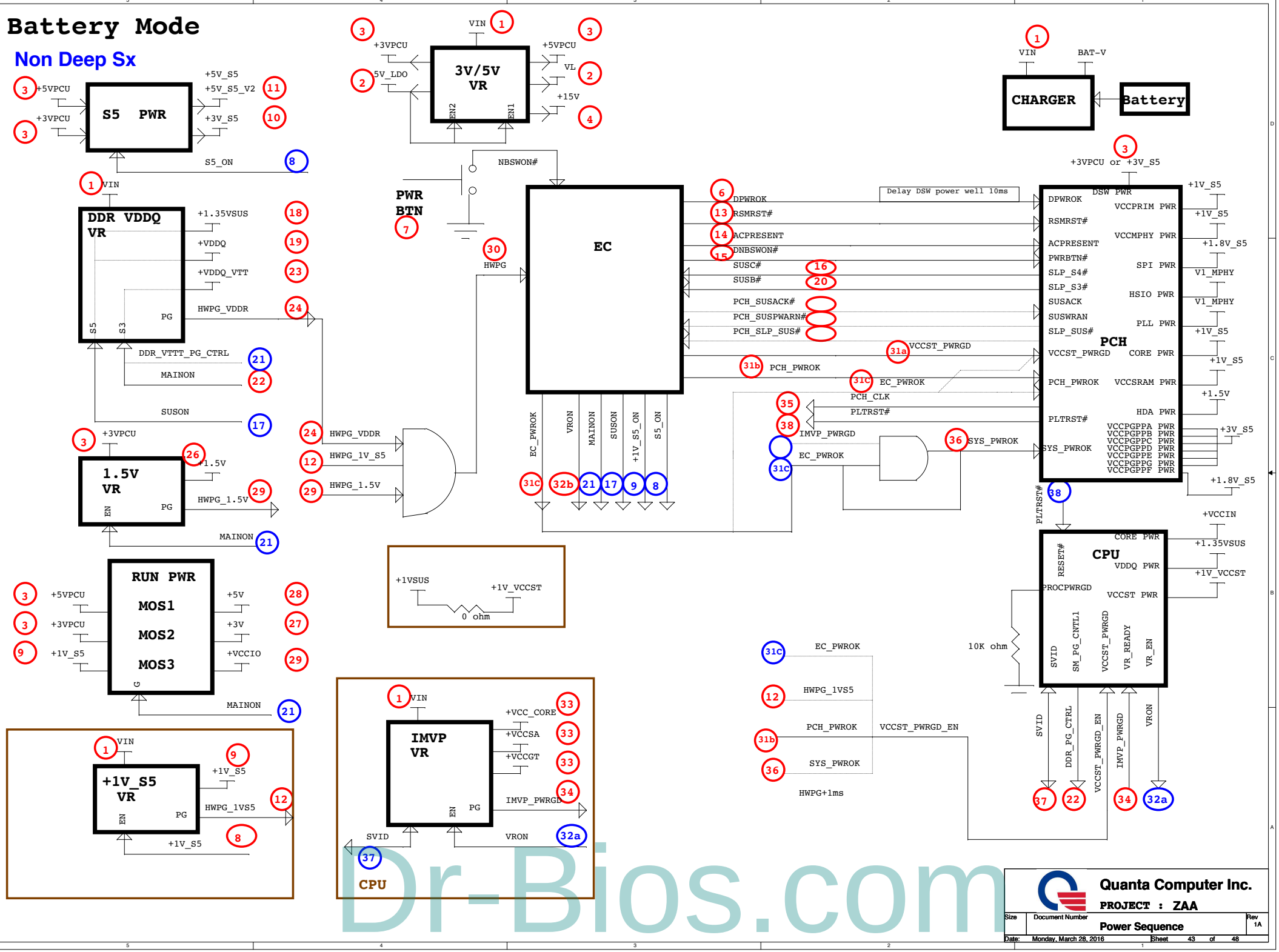
VGA Reset



Quanta Computer Inc.
PROJECT : ZAA
Size | Document Number: GPU PWR CRL | Rev 1A
Date: Monday, March 28, 2016 | Sheet 42 of 48

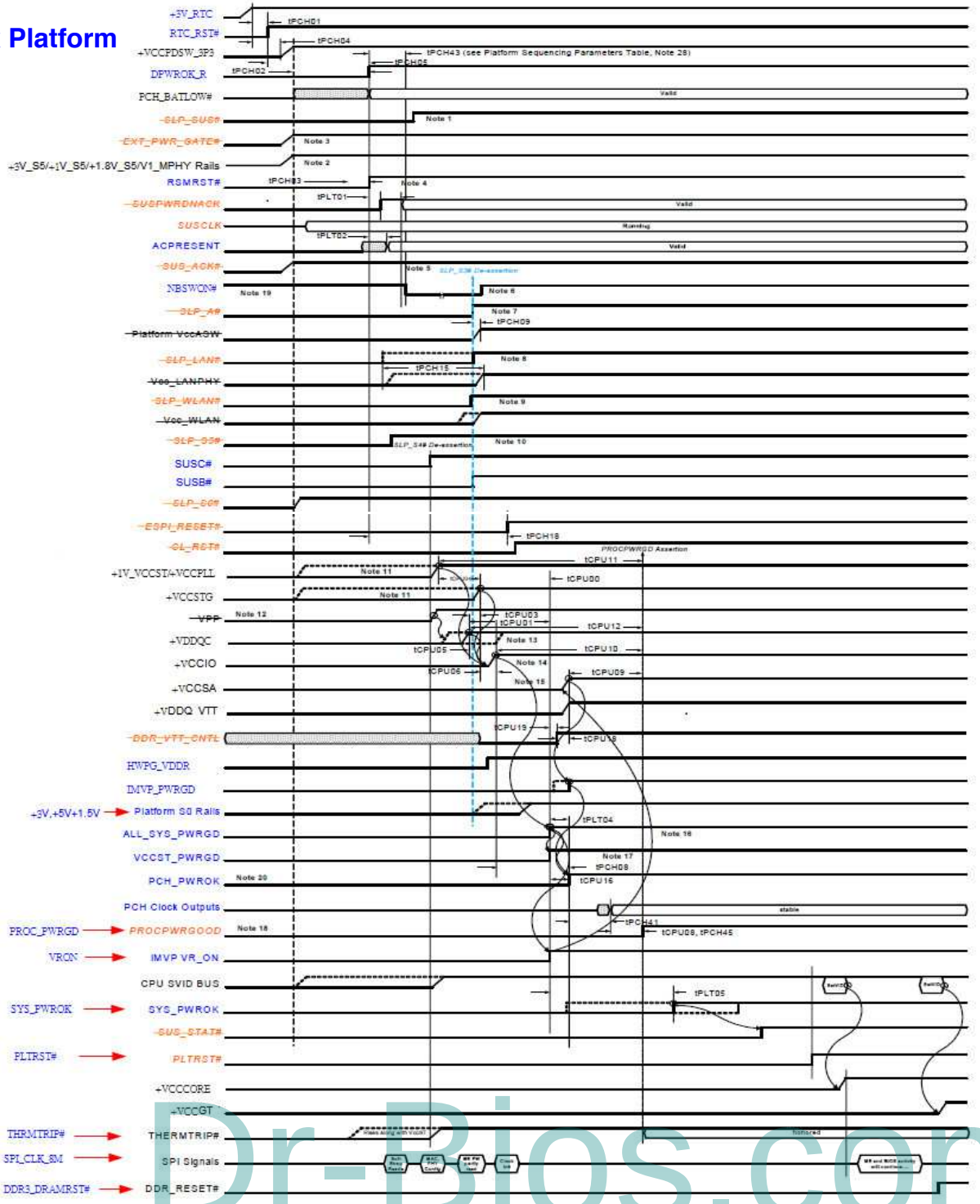
Battery Mode

Non Deep Sx



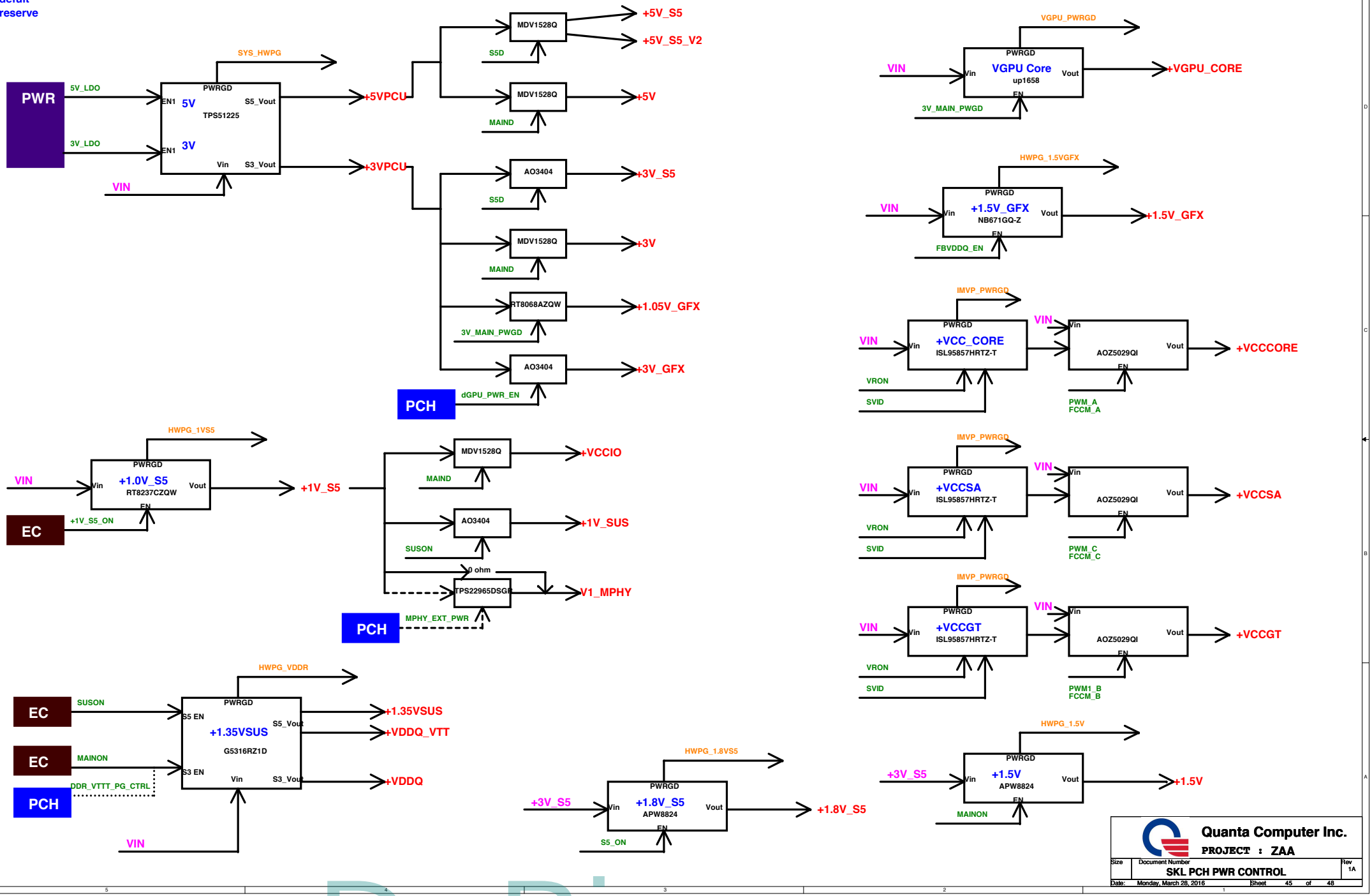
Quanta Computer Inc.	
PROJECT : ZAA	
Size	Document Number: Power Sequence
Rev	1A
Date: Monday, March 28, 2016	Sheet 43 of 48

Skylake U Non-Deep Sx Platform Power on sequence



Quanta Computer Inc.		
PROJECT : ZAA		
Size	Document Number: Power on Sequence	Rev: 2A
Date: Monday, March 28, 2016	Sheet 44 of 48	

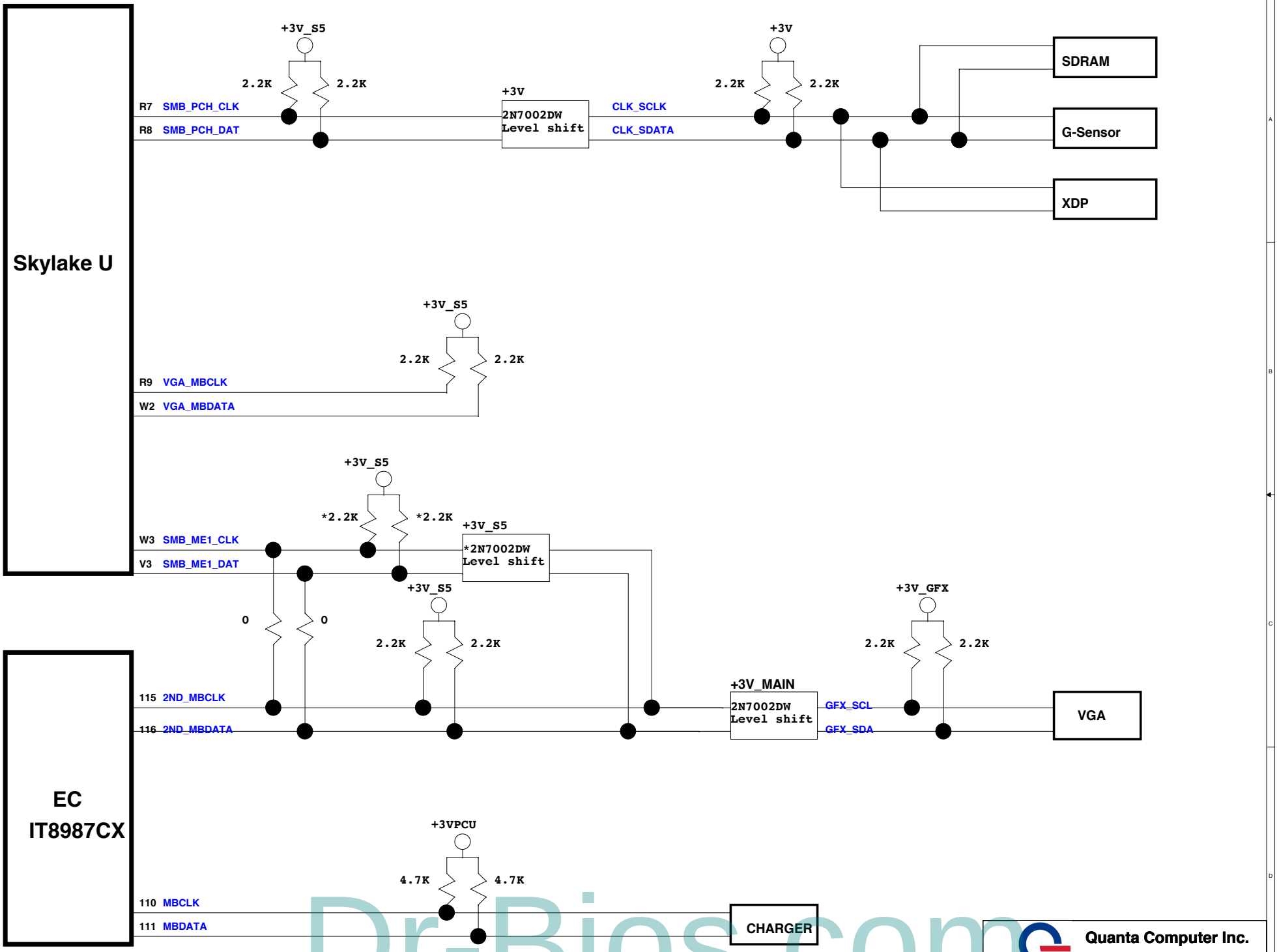
實線表defult
虛線表reserve



Quanta Computer Inc.
PROJECT : ZAA

Size	Document Number	Rev
	SKL PCH PWR CONTROL	1A

Date: Monday, March 28, 2016 Sheet 45 of 48



Quanta Computer Inc.
PROJECT : ZAA
Size | Document Number: SMBUS Block Diagram | Rev 1A
Date: Monday, March 28, 2016 | Sheet 46 of 48

Stage	Date	CHANGE LIST
A	11/25	1. FIRST RELEASED
B	12/11	1. Update DFDS15FR421, DFFC28FR026, DFFC08FR055, DFFC04FR127 to new footprint. 2. Remove IOAC@ part and change BOARD_ID3 to low (page 8.) 3. Change FAN connector CN8 to 3-pin, and add releven circuits. (page 28.) 4. For FAN function change, swap U45 pin-81 with pin-32. (page 30.) 5. Reserve G-sensor circuit. (page 28.) 6. Internal speaker signal short pad R419, R414, R406 & R404 change to 0603 0 ohm. (page 25.) 7. Remove extra hall-sensor circuit on 17". (page 22.) 8. Modify touchpad INT circuit by using R164. (page 4.) 9. Add EC52 TVS diode. (page 30.) 10. Dual DMIC LR pin change to pull-high. (page 25.) 11. Change R4314 & R4306 of value for KA/KB (page 17.) 12. Change R247 value from 0 to 2.2 Ohm (CS-2204FA00) (page 24.) 13. Change R251, R262, R269, R11265 footprint from 0603 to 0805 (page 24.) 14. Reserve R11282 for battery. (page 30.) 15. Change CN23 H=5.0 part number (page 28.) 16. R512 Change to 1% tolerance part number (page 6.)
	12/14	1. Update CN6, CN8, CN18 part nmuber and foot print (page 25.) 2. Change U1006 part number to AL000103006 (page 26.) 3. Q6060 change to stuff (page 6.) 4. R628, R512, R630, R651, R4006 Change to 1% tolerance part number.
	12/15	1. Update HOLE1, HOLE2 foot print to new Rev (page 27.) 2. Add HOLE25, PAD14 foot print (page 27.) 3. Change CN13, CN16 foot print to new Rev (page 23.) 4. Change cap CP to normal cap for keyboard (page 22.) 5. Reserve POA(FPD) circuit (page 26.)
	12/20	1. Change PJ3 foot print to 50320-0040n-001-4p-l-smt for SMT issue (page 31.) 2. Change CPU 0201 Cap to 0402 besides C245, C196, C269, C285, C235 (page 5.) 3. Change SW4 foot print and part number for B-stage, and swap the pin (page 30.) 4. Modify some SPAD and HOLE (page 27.) 5. Change CN6 foot print to 50591-00401-001-4p-l (page 28.) 6. Modify U22 Block GND pin 18-22 (page 29.) 7. Modify CN12, JDIM1, JDIM2, CN23, SW1, SW2 foot print to newer.
	12/21	1. Change CN2021 foot print to ub31-dx07b024xj1ar1000-24p (page 20.) 2. Change CN10 foot print to ngff-nase0-s6701-ts48-ke-smt(page 27.) 3. Add R11284 reserve DMIC power supply (page 25.) 4. Change C739 to 22pF and stuff for bit clock issue (page 4.)
	12/22	1. Change C1255, C1257, C1265, C1270, C1327, C4728 to 10uF cap for cost down (page 12, page 13.)
	12/23	1. Modify R211, R152 to +3V_S5 for +3V leakage issue (page 8, page2.) 2. Modify R577 to reserved (NC), because no used (page 2.) 3. Add C4817, C4818, C4819, C4820 for EMI issue (page 20.) 4. Change CN2021 foot print to ub31-dx07b024xj1ar1000-24p-smt (page 20.) 5. Change CN13, C16 foot print to ub3-yusb0021-p001a-9p-smt (page 29.) 6. Stuff R786, R568, R570, and unstuff U33, C628 (page 2, page 6.) 7. Swap PJ3 (page 31.)
	12/24	1. Change CN4 foot print to sdcard-psdat4-11glbs1nn4h4-11p (page 24.) 2. Change R11267, R11270 to short pad, and change R11268, R11271 form 33 ohm to 47 ohm (page 22.) 3. Unstuff C319, C333, C336, C716, C718 (page 22.) 4. Reserve R11285, R11286 pull up to +3V, and R11287 pull down to GND for CRT issue (page 21.) 5. Stuff R11286 for CRT issue (page 21.) 6. Remove all type-C re-driver short resistor and capactor (page 20.)
	12/25	1. Change HOLE16 foot print to H-TC217BC197D126P2(page 24.)
	12/29	1. Modify the power solution between GT2 and GT3e, see the table (page 36.) 2. Change the power value, PC10 to 1uF CH5101K9B01 (page 36.) 3. Change the power value, PC20 to 0.022uF CH3224K1B01 (page 36.) 4. Change the power value, PC28 to 560pF CH1566K1B09 (page 36.) 5. Change the power value, PC39 to 0.015uF CH3154K1B00 (page 36.) 6. Change the power value, PR220 to 475 ohm CS14752FB11 (page 36.) 7. Modify BOARD_ID7. GPU GT, KB, GTR PU 10k ohm, KA PD 10k. (page 8.) 8. Change the RTC clock crystal Y2 part number to BG3327680C6 (page 6.) 9. Change Q115, Q129 part number to BAM70020076 (page 19.) 10. Modify R11283 to +3V fixed the SSD issue (page 27.) 11. Change the HOLE16 NUT part number to MBZAA002010 (page 27.)
B2	1/7	1. Remove R11274 and mount R11277 for change equalizer setting from 6dB to 4dB (page. 23) 2. Change 15" and 17" keyboard part number to DFFC28FR030 (page 28.)
	1/18	1. Update the System Block Diagram (page 1.) 2. Update the part number option same as B-SMT BOM.
	1/19	1. Power team remove JUMP and change 0 ohm to shortpad (page 31~41.) 2. Modify some description, value and part number have blank.
	1/20	1. Change C144,C150,C190,C199,C248,C645,C650,C659,C666,C690,C696,C697,C702 to 22uF, part number : CH6221M9A00 (page 5.) 2. Change C171,C178,C203,C219,C224,C226,C233,C236,C243,C251,C255,C272,C273,C282,C289,C691,C692,C693,C694,C703,C704, C705,C706,C707,C202,C210 to 10uF, part number : CH6101M9905 (page 5.)
	1/21	1. Change D2,D3,D4,D5,D4013,D4014,EC51,EC52 main source part number from BC040201Z00 to BC005725Z00.

Stage	Date	CHANGE LIST
C	1/22	1. Reserve R11288, R11289, R11290, R11291 0ohm for POA NC function (page 26.) 2. Change Q115, Q129 main source to BAM70020002 3. Change Q5, Q4201 main source to BA039040020. 4. Change D7, D4000 main source to BCBAT54CZ01. 5. Change Q3, Q32, Q4301 main source to BAM70020047.
	1/26	1. Change CN5 part number to DFHS40FS036 (page 22.) 2. Change CN4 part number to DFHS11FR170 (page 4.) 3. Modify POA circuit for C-stage test (page 26.)
	1/27	1. Change the TPS25810RVC pu-high power from +5V_S5_V2 to +3V_S5 (page 20.) 2. Reserve R11193 for Type-C detec issue (page 20.) 3. Change 0 Ohm to short pad R11,R14,R15,R28,R66,R67,R11129,R102,R194,R224,R229,R235,R790,R791,R792,R11111,R11112,R11113,R11140, R112,R135,R179,R180,R182,R185,R187,R188,R192,R193,R198,R240,R252,R11131,R164,R246,R339,R350,R11185,R11186,R550,R657,R718,R721, R782,R11153,R11283,R795,R796,R797,R816,R817,R818,R819,R820,R821,R11196,R11199,R11202,R11207,R11279,R11280,R11281,R948,R951,R956, R958,R959,R960,R11061,R11062,R11110,R11133,R11134,R11136,R11137,R11138,R11139,R11141,R11253,R11254,R11255,R11256,R11267,R11270, R4328,R4335,R2855,R2870,R318,R221,R403,R405,R742,R743,R725,R745,L19,R2872. 4. Add TYPE@ part at Type-C power function (page 32.) 5. Add BL@ part at keyboard back-light (page 28.) 6. Reserve 15" 17" Dual DMIC circuit part (page 25.) 7. Reserve C4821 for NAC function (page 24.)
	1/28	1. Add EV@ part at HOLE8, HOLE9 (page 27.)
	1/29	1. Stuff PR233, PR234 for GT3e power function (page 37.) 2. Add D22@, D10@ part at CPU power side (page 5.) 3. Change PR209, PR210 from short pad to 10 ohm (page 31.)
	2/2	1. Modify POA circuit for C-stage test (page 26.) 2. Remove HOLE25 because not used (page 25.) 3. Change HOLE13, HOLE14, HOLE15 foot print to H-C256D161P2 (page 25.)
	2/3	1. Modify POA circuit for C-stage test (page 26.) 2. Change PC115 from CH5104K9906 to CH41006K911 for FAE suggest (page31.) 3. Stuff PC138 for FAE suggest (page 37.)
	2/4	1. Update C-test BOM.
	2/16	1. Change PR6121 from CS31002FB26 to CS29312FB13 (page 32.) 2. Add C376 distinguish ZAA/ZAAA 15" serial and ZYJ/ZYI 17" serial (page 25.) 3. Change LED current limiting resistor blue and orange to 47 ohm and 124 ohm (page 28.)
	2/17	1. Change PU6010 from AL006575002 to AL051225003 for 3/5V IC noise issue (page 32.)
RAMP	2/22	1. Stuff PC6229, PC6212 for 3/5 voltage IC noise and charging issue (page 32, 37.) 2. Change PR183, PR184, PR209, PR210 to shortpad for 3/5 voltage IC noise and charging issue (page 31.) 3. Modify RP1 circuit (page 28.)
	3/3	1. Unstuff R694, R699 (page 27.) 2. Change 0 Ohm to shortpad R3, R4 R365, R640, R653, R659, R668, R11191, R11192, R16, R212, R404, R406, R414, R419, R752, R789, R237, R672. 3. Remove RP2, RP3, RP4, RP5, L69 for SMT colay issue. (page 20.)
	3/9	1. Change 0 Ohm to shortpad R11284, R2870, R2872, R11298, PR6296, R4329, R4336, PR112. 2. Change PR201, PR202 and PR211 to 1.5k, 97.6k and 267 ohm for GT2 and GT3 (page 36.) 3. Add PC6232, PC6233 at 3/5 V Vin (page 32.) 4. Change PL6013 from 1uH_7X7X3 to 2.2uH_7X7X3 (page 32.)
	3/10	1. Change C714 and C724 value from 10p to 1000p for projector issue (page 22.) 2. Remove SW2 for RAMP-stage (page 30.) 3. Change PU10, PU11, PU20 footprint to son14-3x2-4-15p-smt (page 32.)
	3/15	1. Change RTC crystal circuit C351 and C362 value from 6.8p to 15p for EA issue (page 22.) 2. Modify GPU power solution for cost down (page 40.)
	3/25	1. Change R237 shortpad to 0 ohm for next PCB rev. F (page 27.) 2. Reserve POA function (page 26.)

Quanta Computer Inc.	DOC NO.	PROJECT MODEL :	ZWA	APPROVED BY:	DATE:
PROJECT : ZAA		PART NUMBER:		DRAWING BY:	REVISON:
Size: Document Number: Change list Rev: 1A					
Date: Monday, March 28, 2016 Sheet 48 of 48					