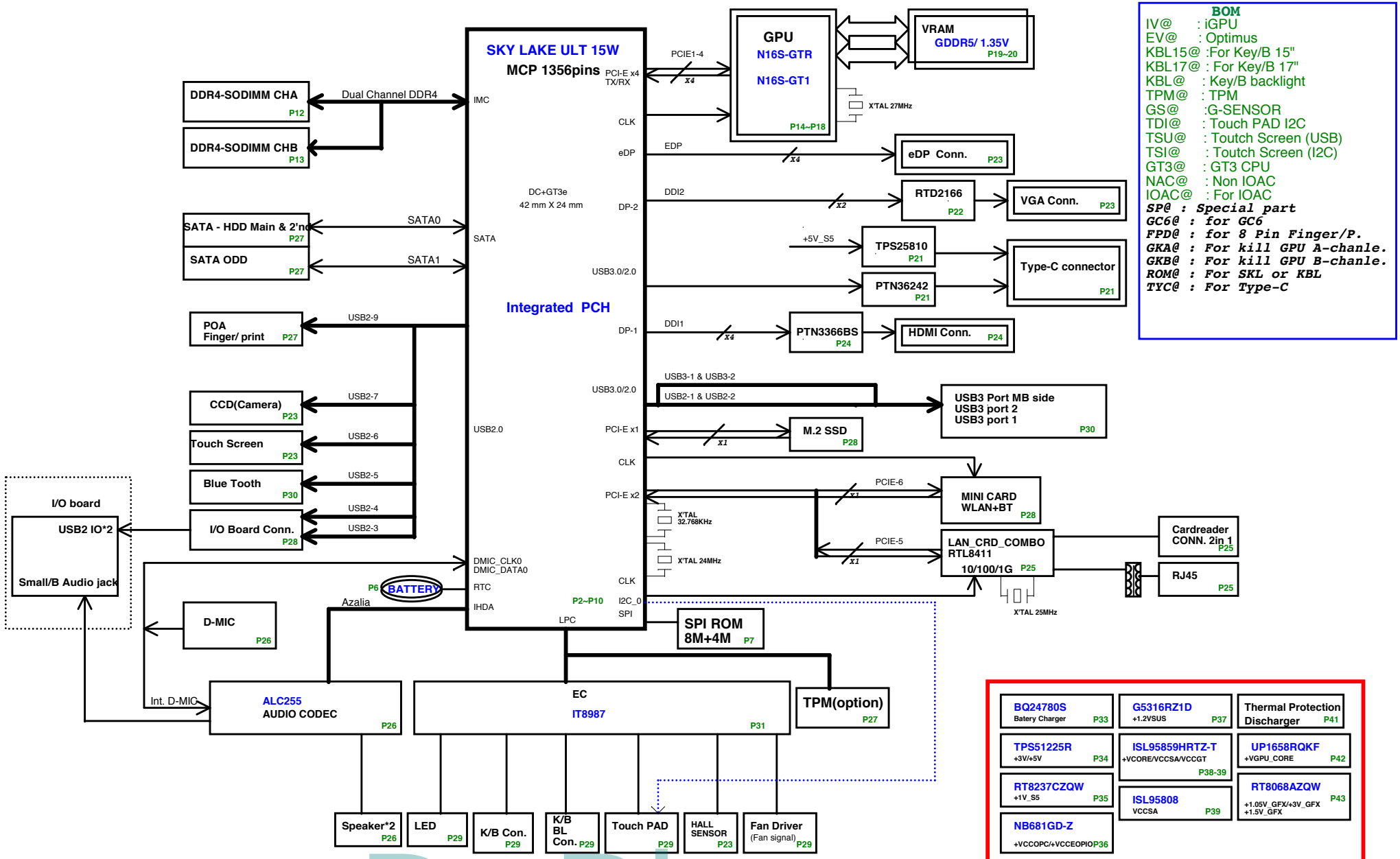
ZAA Serials SKL ULT SYSTEM BLOCK DIAGRAM



BOM

IV@ : iGPU
EV@ : Optimus
KBL15@ :For Key/B 15"
KBL17@ : For Key/B 17"
KBL@ : Key/B backlight
TPM@ : TPM
GS@ :G-SENSOR
TDI@ : Touch PAD I2C
TSU@ : Toutch Screen (USB)
TSI@ : Toutch Screen (I2C)
GT3@ : GT3 CPU
NAC@ : Non IOAC
IOAC@ : For IOAC
SP@ : Special part
GC6@ : for GC6
FPD@ : for 8 Pin Finger/P.
GKA@ : For kill GPU A-chanle.
GKB@ : For kill GPU B-chanle.
ROM@ : For SKL or KBL
TYC@ : For Type-C

BQ24780S Batery Charger P33	G5316RZ1D +1.2VSUS P37	Thermal Protection Discharger P41
TPS51225R +3V/+5V P34	ISL95859HRTZ-T +VCORE/VCCSA/VCCGT P38-39	UP1658RQKF +VGPU_CORE P42
RT8237CZQW +1V_S5 P35	ISL95808 VCCSA P39	RT8068AZQW +1.05V_GFX/+3V_GFX +1.5V_GFX P43
NB681GD-Z +VCCOPC/+VCCEOPIO P36		

CH6221M9A00 CAP CHIP 22U 6.3V(+-20%,X5R,0805)H1.25
CH6221M9A01 CAP CHIP 22U 6.3V(+-20%,X5R,0805)H1.25
CH6221M9A02 CAP CHIP 22U 6.3V(+-20%,X5R,0805)H1.25

remove TPM from SKL , KBL keeps it.---- for B2
add POA FUNCTION, , add 0hm*4 between EC to POA conn & server VST * 7 pcs
POA (change FP power from 3v to 5v)

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Block Diagram
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AJ0QKKQVT00 -->CPU(1356P)KBL 1.7G QKKQ(FCBGA) -----no use
AJ0QKKSUT00 -->CPU(1356P)KBL 2.4G QKKS(FCBGA)
AJ0QKJWQT02 -->CPU(1356P)KBL-U 2.6G QKJW(BGA) QCI PN ---- C-test

i3-6100U AJSR2EUUT07
i5-6200U AJSR2EYUT07
i7-6500U AJSR2EZRT07
i5-6267U AJSR2JK8T02--no use

Skylake ULT (DISPLAY,eDP)

HDMI

To RTS2166 iC

U35A SKL_ULT

DDI1_TXN[0] DDI1_TXP[0] DDI1_TXN[1] DDI1_TXP[1] DDI1_TXN[2] DDI1_TXP[2] DDI1_TXN[3] DDI1_TXP[3]

DDI2_TXN[0] DDI2_TXP[0] DDI2_TXN[1] DDI2_TXP[1] DDI2_TXN[2] DDI2_TXP[2] DDI2_TXN[3] DDI2_TXP[3]

DDI DISPLAY SIDEBANDS EDP

GPP_E18/DDPB_CTRLCLK GPP_E19/DDPB_CTRLDATA GPP_E20/DDPC_CTRLCLK GPP_E21/DDPC_CTRLDATA GPP_E22/DDPD_CTRLCLK GPP_E23/DDPD_CTRLDATA EDP_RCOMP

EDP_TXN[0] EDP_TXP[0] EDP_TXN[1] EDP_TXP[1] EDP_TXN[2] EDP_TXP[2] EDP_TXN[3] EDP_TXP[3] EDP_AUXN EDP_AUXP EDP_DISP_UTIL

DDI1_AUXN DDI1_AUXP DDI2_AUXN DDI2_AUXP DDI3_AUXN DDI3_AUXP

GPP_E13/DDPB_HPD0 GPP_E14/DDPC_HPD1 GPP_E15/DDPD_HPD2 GPP_E16/DDPE_HPD3 GPP_E17/EDP_HPD

EDP_BKLTEN EDP_BKLTCTL EDP_VDDEN

<PART_SYM_NUM>

SP@SKL_ULT/BGA

eDP Panel

For 4K

eDP_RCOMP
Trace length < 100 mils
Trace width = 20 mils
Trace spacing = 25 mils

Change for leakage

For Type-C change

100k pull-down on PCH side

H_PECI (50ohm)
Route on microstrip only
Spacing >18 mils
Trace Length: 0.4~6.125 iches

Avoid 125Mhz

U35D SKL_ULT

CATERR# PECI PROCHOT# THERMTRIP# SKTOCC# CPU MISC BPM#[0] BPM#[1] BPM#[2] BPM#[3]

JTAG PROC_TCK PROC_TDI PROC_TDO PROC_TMS PROC_TRST# PCH_JTAG_TCK PCH_JTAG_TDI PCH_JTAG_TDO PCH_JTAG_TMS PCH_TRST# JTAGX

GPP_E3/CPU_GP0 GPP_E7/CPU_GP1 GPP_B3/CPU_GP2 GPP_B4/CPU_GP3 PROC_POPIRCOMP PCH_OPIRCOMP OPCE_RCOMP OPC_RCOMP

<PART_SYM_NUM>

SP@SKL_ULT/BGA

BPM#[0:7]
Trace Length 1~6 inches
Length match < 300 mils

SM_RCOMP[0:2]
Trace length < 500 mils
Trace width = 12~15 mils
Trace spacing = 20 mils

PCH JTAG
JTAG_TCK,JTAG_TMS
Trace Length < 9000mils

If use Intel DCI USB 3.0 fixture need to short
1. XDP_TDO <--> XDP_TDO_CPU
2. XDP_TDI <--> XDP_TDI_CPU
3. XDP_TMS <--> XDP_TMS_CPU

MP remove(Intel)

Change to +1V_VCCST 11/6

2/16
,XDP_TCK1,XDP_TMS
don't need pull up or pull down

5/29 XDP_TCK0 R558 Stuff

CPU thermal trip

U33 NC VCC A GND Y *74AUP1G07GW

Q31 FDV301N

Q5 MMBT3904-7-F

+VCCIO <5,8,32,34,37,40>
+1V_VCCST <5,8,9,37>

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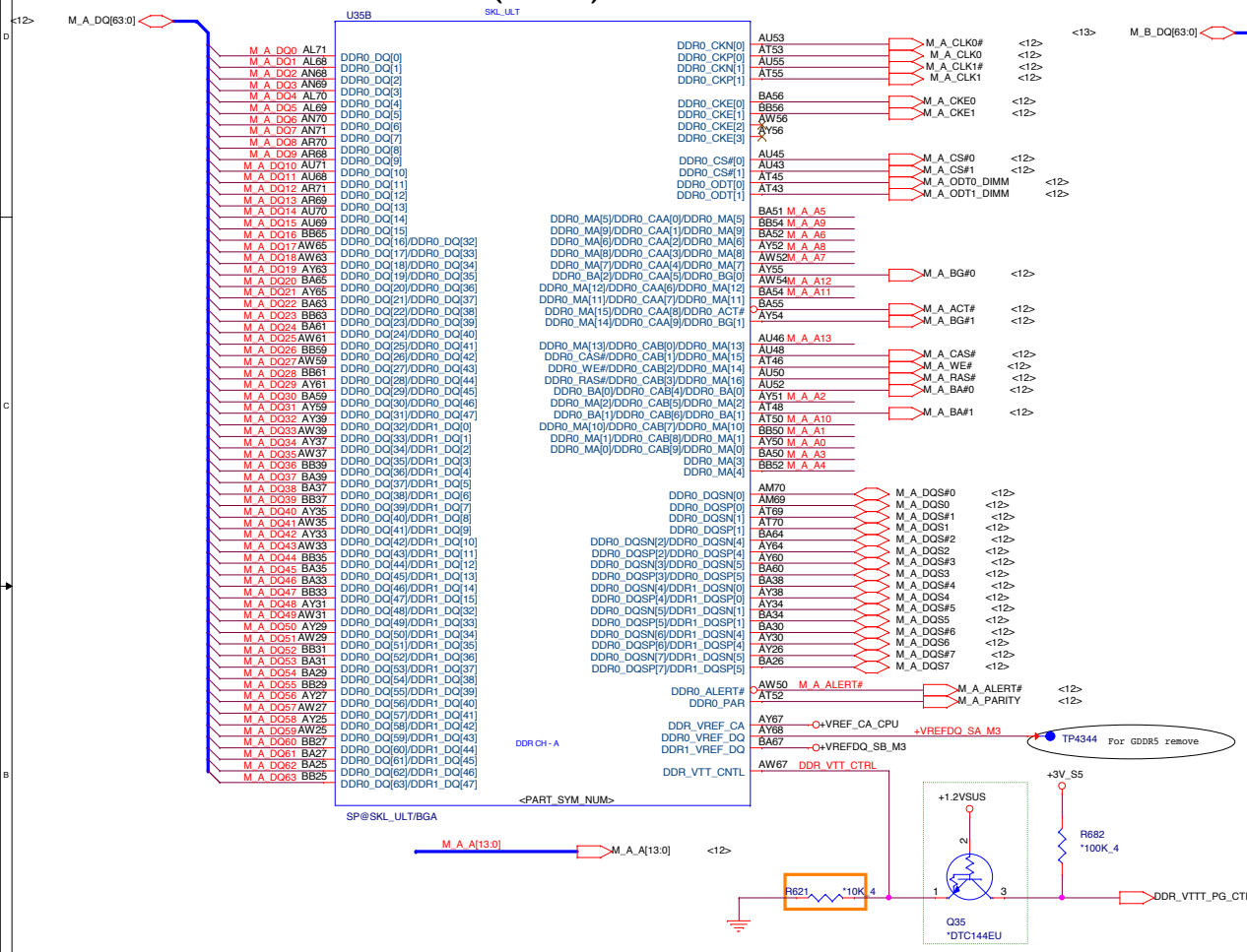
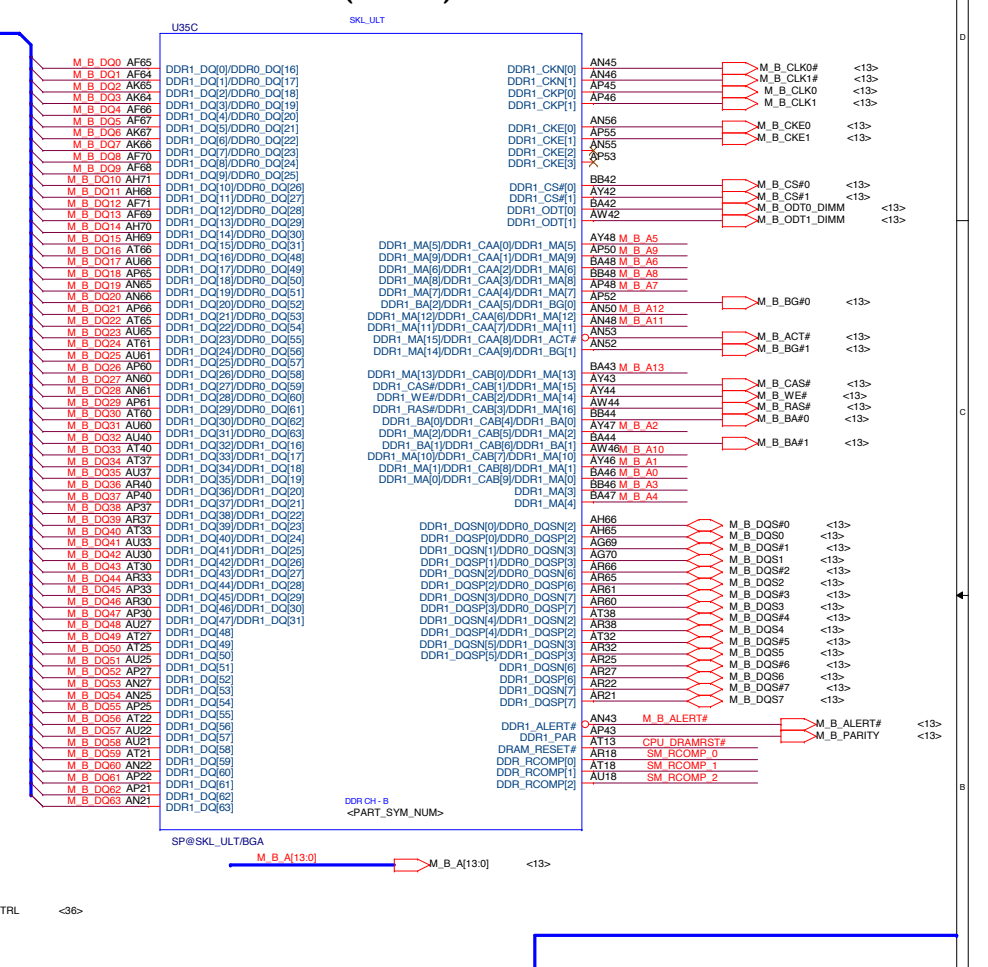
Change Data and DQS to interleave.

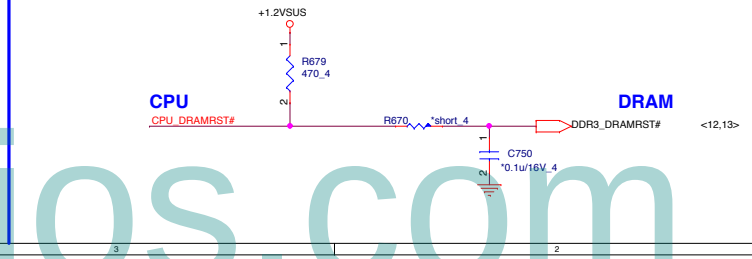
SKL ULT (DDR3L)



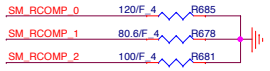
SKL ULT (DDR3L)



DRAMRST



DRAM COMP



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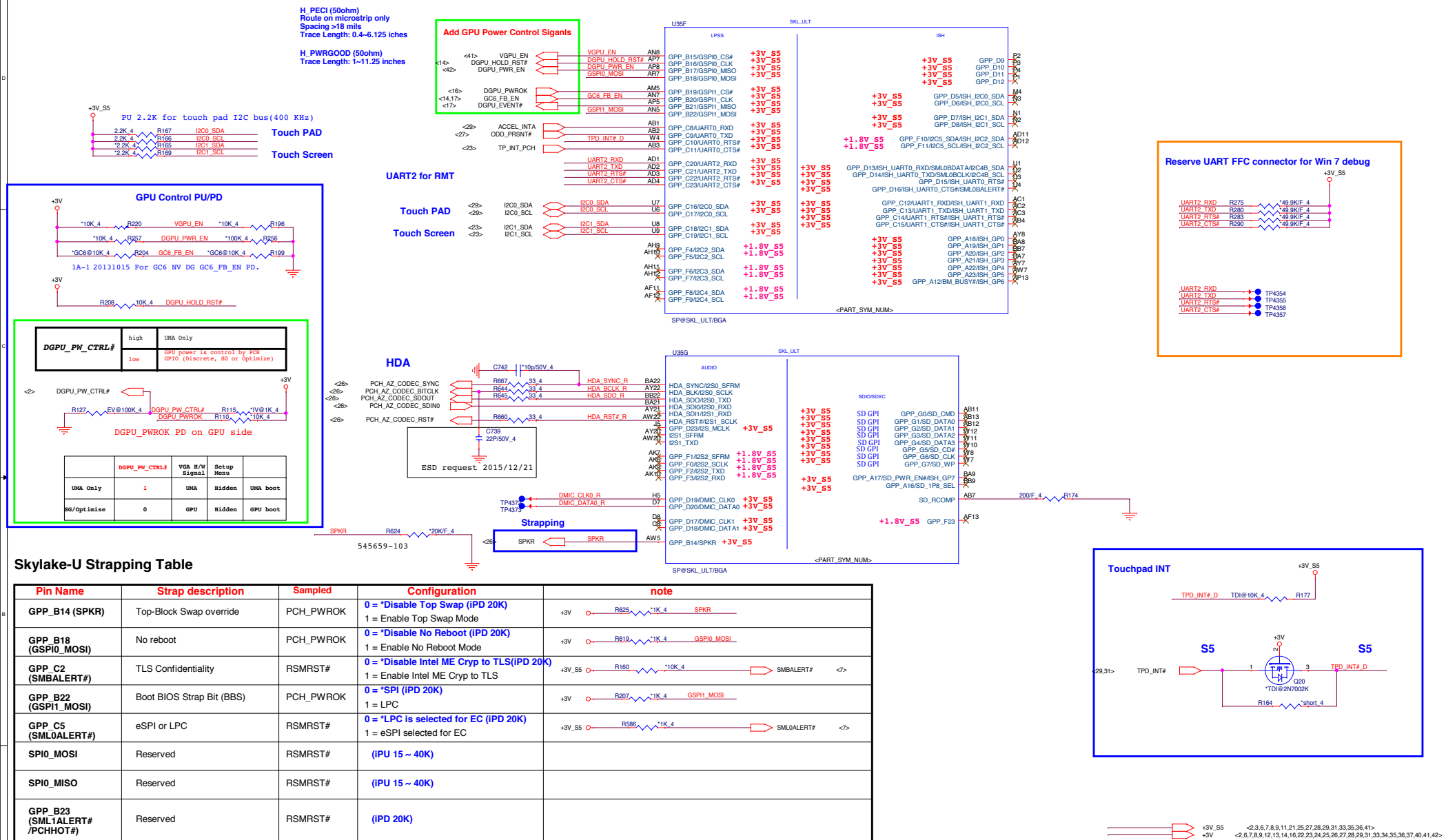
SKL ULT (SIDEBAND) GPIO



Skylake-U Strapping Table

Pin Name	Strap description	Sampled	Configuration	note
GPP_B14 (SPKR)	Top-Block Swap override	PCH_PWROK	0 = *Disable Top Swap (iPD 20K) 1 = Enable Top Swap Mode	
GPP_B18 (GSPI0_MOSI)	No reboot	PCH_PWROK	0 = *Disable No Reboot (iPD 20K) 1 = Enable No Reboot Mode	
GPP_C2 (SMBALERT#)	TLS Confidentiality	RSMRST#	0 = *Disable Intel ME Cryp to TLS(iPD 20K) 1 = Enable Intel ME Cryp to TLS	
GPP_B22 (GSPI1_MOSI)	Boot BIOS Strap Bit (BBS)	PCH_PWROK	0 = *SPI (iPD 20K) 1 = LPC	
GPP_C5 (SML0ALERT#)	eSPI or LPC	RSMRST#	0 = *LPC is selected for EC (iPD 20K) 1 = eSPI selected for EC	
SPI0_MOSI	Reserved	RSMRST#	(iPU 15 ~ 40K)	
SPI0_MISO	Reserved	RSMRST#	(iPU 15 ~ 40K)	
GPP_B23 (SML1ALERT# /PCHHOT#)	Reserved	RSMRST#	(iPD 20K)	
SPI0_IO2	Reserved	RSMRST#	(iPU 15 ~ 40K)	
SPI0_IO3	Reserved	RSMRST#	(iPU 15 ~ 40K)	
HDA_SDO / I2S_TXD0	Flash Descriptor Security Override / Intel ME Debug Mode	PCH_PWROK	0 = *Enable security in the Flash Description (iPD 20K) 1 = Disable Flash Descriptor Security (Override)	change location to near CPU to prevent impact HDA_SDO signal
GPP_E19 (DDPB_CTRLDATA)	Display Port B Detected	PCH_PWROK	0 = *Port B is not detected (iPD 20K) 1 =Port B is detected	
GPP_E21 (DDPC_CTRLDATA)	Display Port C Detected	PCH_PWROK	0 = *Port C is not detected (iPD 20K) 1 =Port C is detected	

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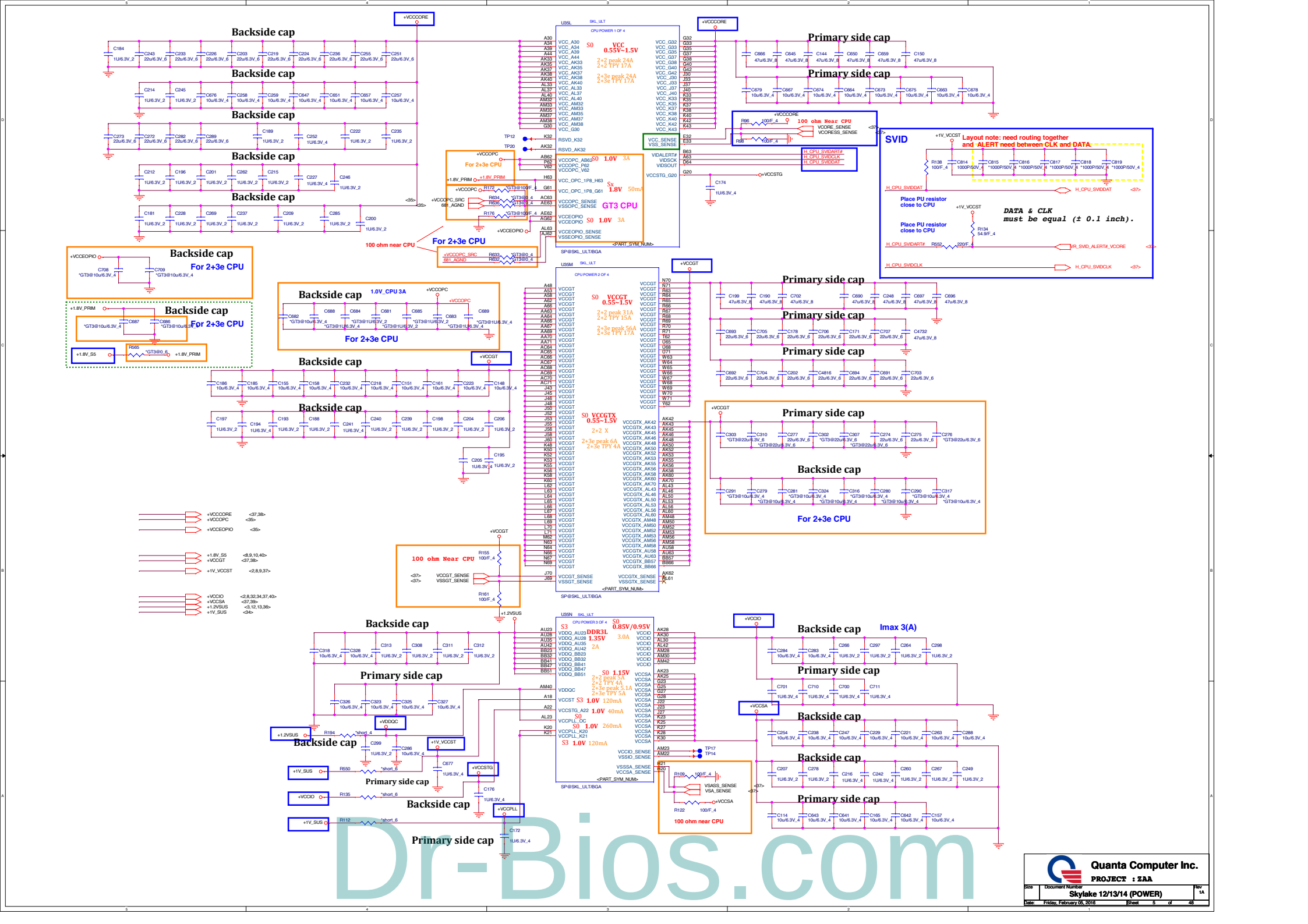
Backside cap
Primary side cap
SVID
Layout note: need routing together and ALERT need between CLK and DATA.
DATA & CLK must be equal (± 0.1 inch).
Place PU resistor close to CPU
For 2+3e CPU
100 ohm near CPU
GT3 CPU
Imax 3(A)
SP@SKL_ULT/BGA
Quanta Computer Inc.
PROJECT : ZAA
Skylake 12/13/14 (POWER)
Rev 1A
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Skylake ULT (GPU, SATA , ODD, CLK ,USB2&3)

+3V <2,4,7,8,9,12,13,14,16,22,23,24,25,26,27,28,29,31,33,34,35,36,37,40,41,42>
+3V_S5 <2,3,4,7,8,9,11,21,25,27,28,29,31,33,35,36,41>
+3VPCU <9,11,23,25,26,27,28,29,31,32,33,40,41,42>
+3V_RTC <8,9,31>
+1V_S5 <9,34>

U35H SKL_ULT

PCIE/USB3/SATA

dGPU PEG*4
<14> PEG_RX#0 / PEG_RX0 / PEG_TX#0 / PEG_TX0 — C653 EV@0.22u/10V_4 C_PEG_TX#0 — C652 EV@0.22u/10V_4 C_PEG_TX0
<14> PEG_RX#1 / PEG_RX1 / PEG_TX#1 / PEG_TX1 — C656 EV@0.22u/10V_4 C_PEG_TX#1 — C655 EV@0.22u/10V_4 C_PEG_TX1
<14> PEG_RX#2 / PEG_RX2 / PEG_TX#2 / PEG_TX2 — C661 EV@0.22u/10V_4 C_PEG_TX#2 — C662 EV@0.22u/10V_4 C_PEG_TX2
<14> PEG_RX#3 / PEG_RX3 / PEG_TX#3 / PEG_TX3 — C654 EV@0.22u/10V_4 C_PEG_TX#3 — C660 EV@0.22u/10V_4 C_PEG_TX3

H13 PCIE1_RXN/USB3_5_RXN
G13 PCIE1_RXP/USB3_5_RXP
B17 PCIE1_TXN/USB3_5_TXN
A17 PCIE1_TXP/USB3_5_TXP
G11 PCIE2_RXN/USB3_6_RXN
F11 PCIE2_RXP/USB3_6_RXP
D16 PCIE2_TXN/USB3_6_TXN
C16 PCIE2_TXP/USB3_6_TXP
H16 PCIE3_RXN
G16 PCIE3_RXP
D17 PCIE3_TXN
C17 PCIE3_TXP
G15 PCIE4_RXN
F15 PCIE4_RXP
B19 PCIE4_TXN
A19 PCIE4_TXP

For Thunderbolt
TP4380 TP4379 TP4382 TP4381 — F16 PCIE5_RXN, E16 PCIE5_RXP, C19 PCIE5_TXN, D19 PCIE5_TXP
TP4385 TP4383 TP4386 TP4384 — G18 PCIE6_RXN, F18 PCIE6_RXP, D20 PCIE6_TXN, C20 PCIE6_TXP

HDD
<27> SATA_RXN0 / <27> SATA_RXP0 / <27> SATA_TXN0 / <27> SATA_TXP0
F20 PCIE7_RXN/SATA0_RXN
E20 PCIE7_RXP/SATA0_RXP
B21 PCIE7_TXN/SATA0_TXN
A21 PCIE7_TXP/SATA0_TXP

ODD
<27> SATA_RXN1 / <27> SATA_RXP1 / <27> SATA_TXN1 / <27> SATA_TXP1
G21 PCIE8_RXN/SATA1A_RXN
F21 PCIE8_RXP/SATA1A_RXP
D21 PCIE8_TXN/SATA1A_TXN
C21 PCIE8_TXP/SATA1A_TXP

LAN
<25> PCIE_RX5-_LAN / <25> PCIE_RX5+_LAN / <25> PCIE_TX5-_LAN / <25> PCIE_TX5+_LAN
C668 0.1u/16V_4 PCIE_TX5- — C669 0.1u/16V_4 PCIE_TX5+
E22 PCIE9_RXN
E23 PCIE9_RXP
B23 PCIE9_TXN
A23 PCIE9_TXP

WIFI
<28> PCIE_RX6-_WLAN / <28> PCIE_RX6+_WLAN / <28> PCIE_TX6-_WLAN / <28> PCIE_TX6+_WLAN
C648 0.1u/16V_4 PCIE_TX6- — C649 0.1u/16V_4 PCIE_TX6+
F25 PCIE10_RXN
E25 PCIE10_RXP
D23 PCIE10_TXN
C23 PCIE10_TXP
R562 100/F_4 PCIE_RCOMPN / PCIE_RCOMPP
E5 PCIE_RCOMPN
E5 PCIE_RCOMPP

TP91 XDP_PRDY# — D56 PROC_PRDY#
TP92 XDP_PREQ# / PIRQA# — D61 PROC_PREQ# / BB11 GPP_A7/PIRQA# +3V_S5

For M.2 SSD -NA
<28> SATA_RXN3/PEG_RXN9_L0 / <28> SATA_RXP3/PEG_RXP9_L0 / <28> SATA_TXN3/PEG_TXN9_L0 / <28> SATA_TXP3/PEG_TXP9_L0
E28 PCIE11_RXN/SATA1B_RXN
E27 PCIE11_RXP/SATA1B_RXP
D24 PCIE11_TXN/SATA1B_TXN
C24 PCIE11_TXP/SATA1B_TXP

For M.2 SSD -1
<28> SATA_RXN3/PEG_RXN10_L1 / <28> SATA_RXP3/PEG_RXP10_L1 / <28> SATA_TXN3/PEG_TXN10_L1 / <28> SATA_TXP3/PEG_TXP10_L1
E30 PCIE12_RXN/SATA2_RXN
F30 PCIE12_RXP/SATA2_RXP
A25 PCIE12_TXN/SATA2_TXN
B25 PCIE12_TXP/SATA2_TXP

SP@SKL_ULT/BGA

SSIC / USB3

USB3_1_RXN H8 — USB3_RXN0 <30>
USB3_1_RXP G8 — USB3_RXP0 <30>
USB3_1_TXN C13 — USB3_TXN0 <30>
USB3_1_TXP D13 — USB3_TXP0 <30>
MB USB3.0 (Charger IC)

USB3_2_RXN/SSIC_1_RXN J6 — USB3_RXN1 <30>
USB3_2_RXP/SSIC_1_RXP H6 — USB3_RXP1 <30>
USB3_2_TXN/SSIC_1_TXN B13 — USB3_TXN1 <30>
USB3_2_TXP/SSIC_1_TXP A13 — USB3_TXP1 <30>
MB USB3.0

USB3_3_RXN/SSIC_2_RXN J10 — USB3_RXN2 <21>
USB3_3_RXP/SSIC_2_RXP H10 — USB3_RXP2 <21>
USB3_3_TXN/SSIC_2_TXN B15 — USB3_TXN2 <21>
USB3_3_TXP/SSIC_2_TXP A15 — USB3_TXP2 <21>

USB3_4_RXN E10 — USB3_RXN3 <21>
USB3_4_RXP F10 — USB3_RXP3 <21>
USB3_4_TXN C15 — USB3_TXN3 <21>
USB3_4_TXP D15 — USB3_TXP3 <21>
For TYPE-C

USB2

USB2N_1 / USB2P_1 AB9 AB10 — USBP0- / USBP0+ <30>
MB USB3.0 Charger IC)

USB2N_2 / USB2P_2 AD6 AD7 — USBP1- / USBP1+ <30>
MB USB3.0

USB2N_3 / USB2P_3 AH3 AJ3 — USBP2- / USBP2+ <30>
DB USB2.0

USB2N_4 / USB2P_4 AD9 AD10 — USBP3- / USBP3+ <30>
For 17" DB use

USB2N_5 / USB2P_5 AJ1 AJ2 — USBP4- / USBP4+ <28>
BT

USB2N_6 / USB2P_6 AF6 AF7 — USBP5- / USBP5+ <23>
Touch Screen

USB2N_7 / USB2P_7 AH1 AH2 — USBP6- / USBP6+ <23>
CCD

USB2N_8 / USB2P_8 AF8 AF9 — USBP7- / USBP7+ <21>
For TYPE-C

USB2N_9 / USB2P_9 AG1 AG2 — USBP8- / USBP8+ <27>
POA

USB2N_10 / USB2P_10 AH7 AH8 — TP4377 TP4378

USB2_COMP AB6 — USBCOMP — R178 113/F_4
USB2_ID AG3 — USB2_ID — R587 1K_4
VSS AG4 — R778 1K_4
USB2_VBUSSENSE
USBCOMP
Impedance = 50 ohm
Trace length < 500 mils
Trace spacing = 15 mils

+3V_S5 GPP_E9/USB2_OC0# A9 — USB_OC0# <30>
+3V_S5 GPP_E10/USB2_OC1# C9 — USB_OC1# <30>
+3V_S5 GPP_E11/USB2_OC2# D9 — USB_OC2# <30>
+3V_S5 GPP_E12/USB2_OC3# B9 — USB_OC3# <21>
MB U3
MB U3
DB U2
For Type-C

+3V_S5 GPP_E4/DEVSLP0 J1 — DEVSLP0 <27>
+3V_S5 GPP_E5/DEVSLP1 J2 — SATA_DEVSLP1
+3V_S5 GPP_E6/DEVSLP2 J3 — SATA_DEVSLP2 <28>

+3V_S5 GPP_E0/SATAXPCIE0/SATAGP0 H2 — SATAGP0
+3V_S5 GPP_E1/SATAXPCIE1/SATAGP1 H3 — SATAGP1
+3V_S5 GPP_E2/SATAXPCIE2/SATAGP2 G4 — NGFF_SATA_DET <28>
+3V_S5 GPP_E8/SATALED# H1

<PART_SYM_NUM>

PCH PU/PD

+3V_S5
USB_OC0# R541 10K_4
USB_OC1# R540 10K_4
USB_OC2# R543 10K_4
USB_OC3# R542 10K_4

+3V
DEVSLP0 R573 *10K_4
SATA_DEVSLP1 R574 *10K_4
SATA_DEVSLP2 R575 *10K_4
PIRQA# R631 *10K_4
SATAGP1 R569 *10K_4

Add SSD ID 1/14
Hight is SSD , Low is ODD
+3V_S5
<27> SSD_ID — R568 10K_4 — SATAGP0 — R570 100K_4

Skylake-U userd 24 MHz (50 Ohm ESR) XTAL

C665 10P/50V_4
R536 1M_4
Y4 24MHz
C658 10P/50V_4
XTAL24_IN
XTAL24_OUT

24MHz: BG624000078
38.4MHz : ?

Note: Change Y4 to 38.4 MHz(ESR 30 ohm) for Cannonlake U

RTC Clock 32.768KHz (RTC)

CH01006JB08 -> 10p
CH01506JB06 -> 15p
CH-6806TB01 -> 6.8p

Trace length < 1000 mils

C351 18.2p/50V_4 — RTC_X1
Y2 32.768KHZ
R255 10M_4
C362 18.2p/50V_4 — RTC_X2

BG332768453 -> SEG
BG332768104 -> TXC

RTC Circuitry (RTC)

+3VPCU
On SKL voltage at VCCRTC does not exceed 3.2V
R304 1.5K/F_4
R301 45.3K/F_4
VCCRTC
R308 1K_4 +3V_RTC_1 +3V_RTC_2
D7 BAT54C
+3V_RTC
+3V_RTC
Trace width = 30 mils
R299 20K/F_4 RTC_RST#
C380 1u/6.3V_4
J1 *JUMP
R300 20K/F_4 SRTC_RST#
C381 1u/6.3V_4
C382 1u/6.3V_4
+3V_RTC_2 [0:2]
Trace width = 20 mils
BT1
BAT_CONN

1A-22013/10/16 Chage +3V_RTC_0 to VCCTC_2.

1. AHL03003057 DBV CR2032
2. AHL03003003 VDE CR2032

U35J SKL_ULT

CLOCK SIGNALS

N16S VGA
<14> CLK_PCIE_VGA# / <14> CLK_PCIE_VGA / <14> CLK_PEGA_REQ# — R235 *short_4 CLK_PCIE_REQ0# — AR10 CLKOUT_PCIE_N0 / AR10 CLKOUT_PCIE_P0 — GPP_B5/SRCCLKREQ0# +3V_S5

M.2 SSD
<28> NGFF_SSD_CLK# / <28> NGFF_SSD_CLK / <28> PCIE_CLKREQ_NGFF_SSD# — R11112 *short_4 NGFF_SSD_CLK#_C — R11113 *short_4 NGFF_SSD_CLK_C — R11111 *short_4 CLK_PCIE_REQ1# — AT7 CLKOUT_PCIE_N1 / A42 CLKOUT_PCIE_P1 — GPP_B6/SRCCLKREQ1# +3V_S5

For Thunderbolt
TP4389 TP4387 — CLK_PCIE_REQ2# — AT8 CLKOUT_PCIE_N2 / D41 CLKOUT_PCIE_P2 — GPP_B7/SRCCLKREQ2# +3V_S5

TP22 — CLK_PCIE_REQ3# — AT10 CLKOUT_PCIE_N3 / C40 CLKOUT_PCIE_P3 — GPP_B8/SRCCLKREQ3# +3V_S5

LAN
<25> CLK_PCIE_LANN / <25> CLK_PCIE_LANP / <25> CLK_PCIE_LAN_REQ# — R229 *short_4 CLK_PCIE_REQ4# — AU8 CLKOUT_PCIE_N4 / A40 CLKOUT_PCIE_P4 — GPP_B9/SRCCLKREQ4# +3V_S5

WLAN
<28> CLK_PCIE_WLANN / <28> CLK_PCIE_WLANP / <28> PCIE_CLKREQ_WLAN# — R224 *short_4 CLK_PCIE_REQ5# — AU7 CLKOUT_PCIE_N5 / E38 CLKOUT_PCIE_P5 — GPP_B10/SRCCLKREQ5# +3V_S5

CLKOUT_ITPXDP_N F43 CLK_PCIE_XDPN — TP93
CLKOUT_ITPXDP_P E43 CLK_PCIE_XDPP — TP94
+3V_S5 GPD8/SUSCLK BA17 SUSCLK — SUSCLK <28>
XTAL24_IN E37 XTAL24_IN
XTAL24_OUT E35 XTAL24_OUT
XCLK_BIASREF E42 XCLK_BIASREF — R512 2.7K/F_4 — +1V_S5
RTCX1 AM18 RTC_X1
RTCX2 AM20 RTC_X2
SRTCRST# AN18 SRTC_RST#
RTCRST# AM16 RTC_RST# — RTC_RST# <11>

<PART_SYM_NUM>

SP@SKL_ULT/BGA

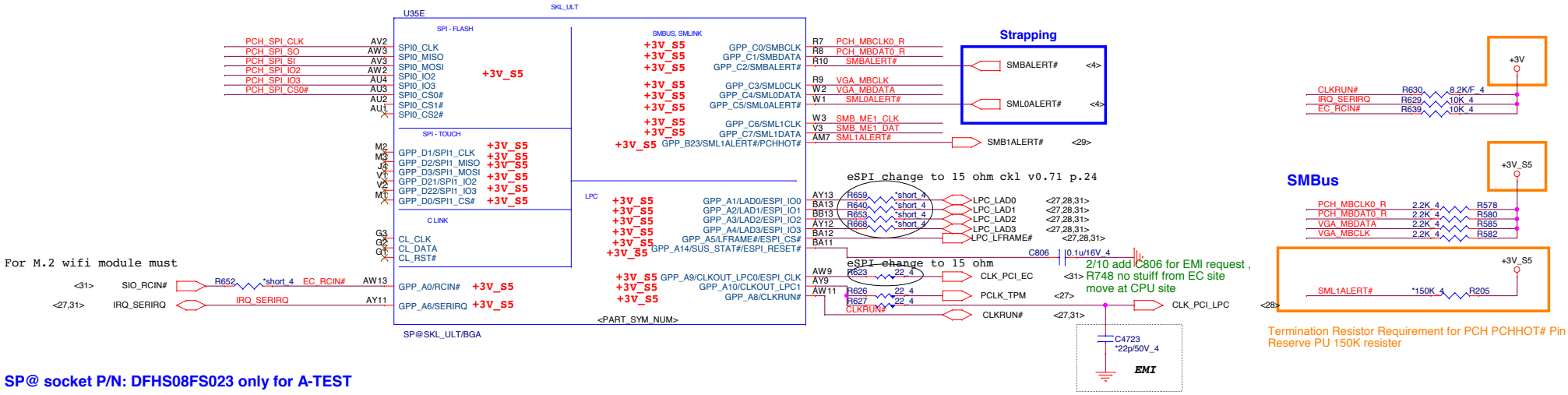
1V power plane
0.71 checklist p14

+3V
CLK_PCIE_REQ0# R234 10K_4
CLK_PCIE_REQ1# R215 10K_4
CLK_PCIE_REQ2# R227 *10K_4
CLK_PCIE_REQ3# R618 *10K_4
CLK_PCIE_REQ4# R228 10K_4
CLK_PCIE_REQ5# R223 10K_4

Rev:D add for EC reset RTC

<31> CLR_CMOS — CLR_CMOS — R786 100K_4 — Q6050 *2N7002K — SRTC_RST#
CLR_CMOS — Q6060 2N7002K — RTC_RST#

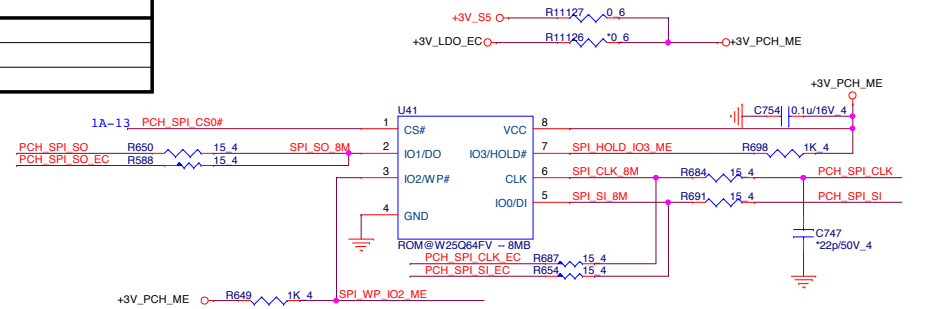
Quanta Computer Inc.
PROJECT : ZAA
Size | Document Number: Skylake 9/10 (PEG/USB/CLK) | Rev: 1A
Date: Friday, February 05, 2016 | Sheet 6 of 48

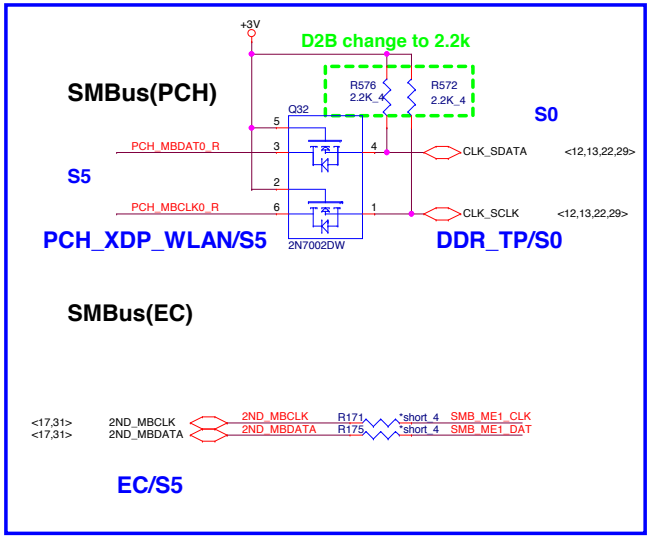


SP@ socket P/N: DFHS08FS023 only for A-TEST

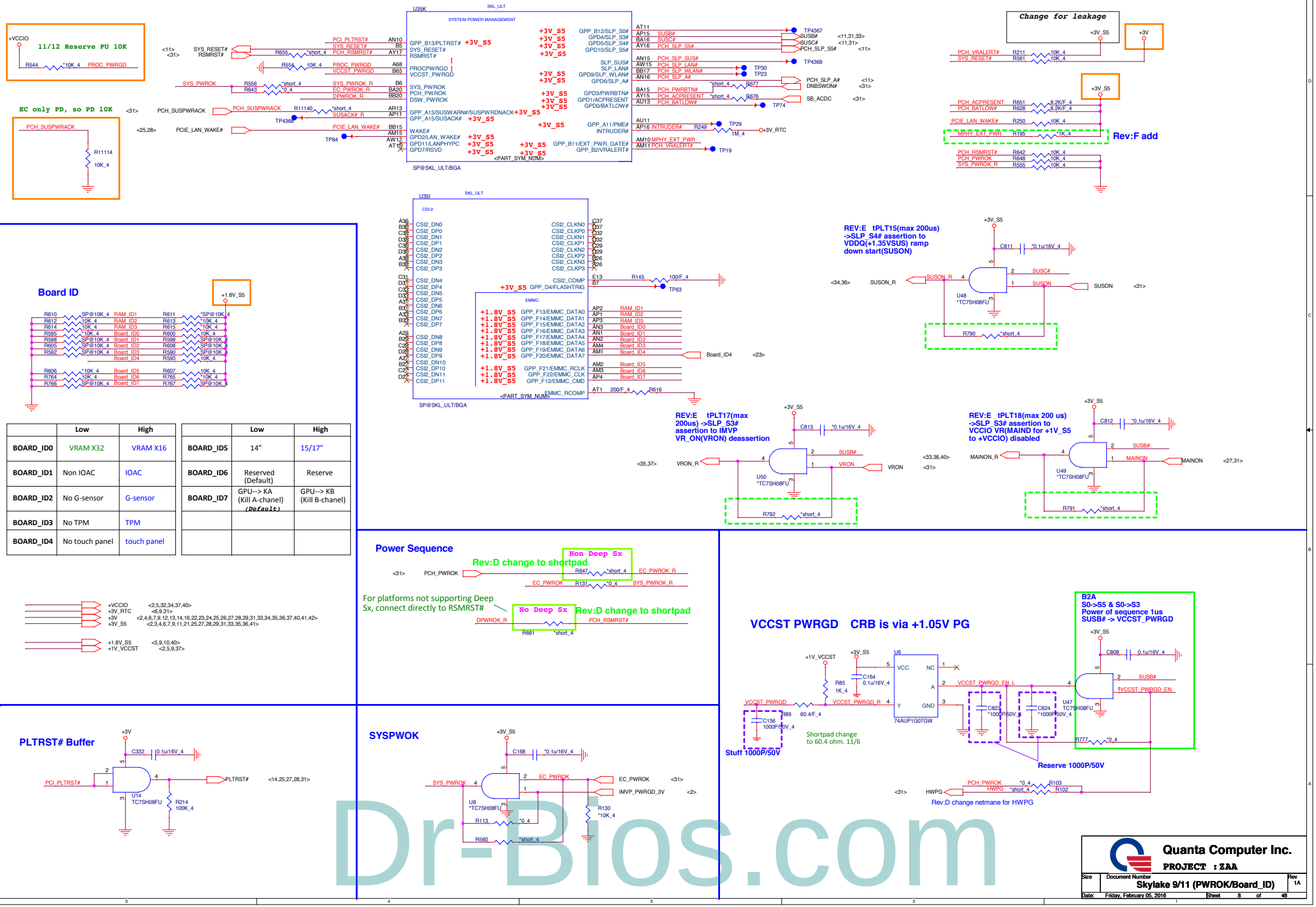
SPI ROM	Vender	Size	Quanta P/N	Vender P/N	Platform
Skylake 3.3V	WND	8M	AKE3EFP0N07	W25Q64FVSSIQ	SKL
	GGD	8M	AKE2EZN0Q00	GD25B64CSIGR	KBL

Winbound for SKL / Giga for KBL





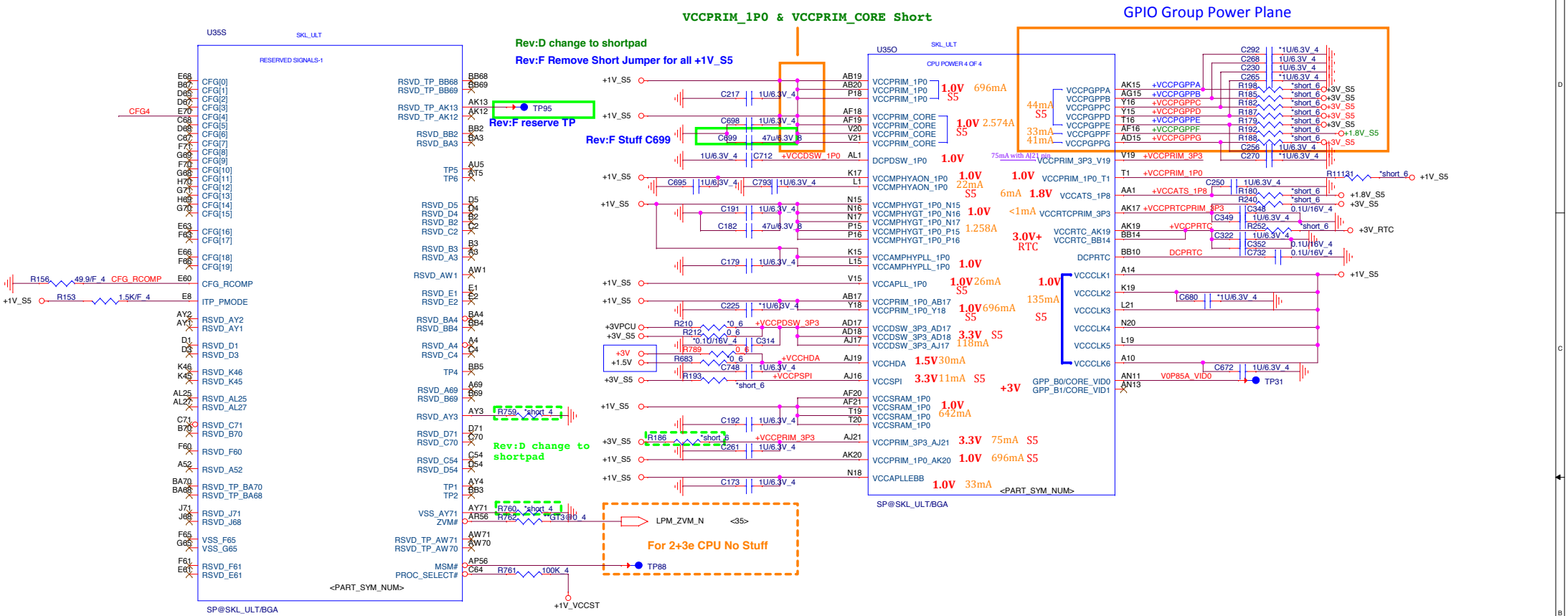
Quanta Computer Inc.			
PROJECT : ZAA			
Size	Document Number		Rev
	Skylake 5 (SATA/HDA/SPI)		1A
Date: Friday, February 05, 2016	Sheet 7	of	48



	Low	High
BOARD_ID0	VRAM X32	VRAM X16
BOARD_ID1	Non IOAC	IOAC
BOARD_ID2	No G-sensor	G-sensor
BOARD_ID3	No TPM	TPM
BOARD_ID4	No touch panel	touch panel

	Low	High
BOARD_ID5	14"	15/17"
BOARD_ID6	Reserved (Default)	Reserve
BOARD_ID7	GPU--> KA (Kill A-chanel) (Default)	GPU--> KB (Kill B-chanel)

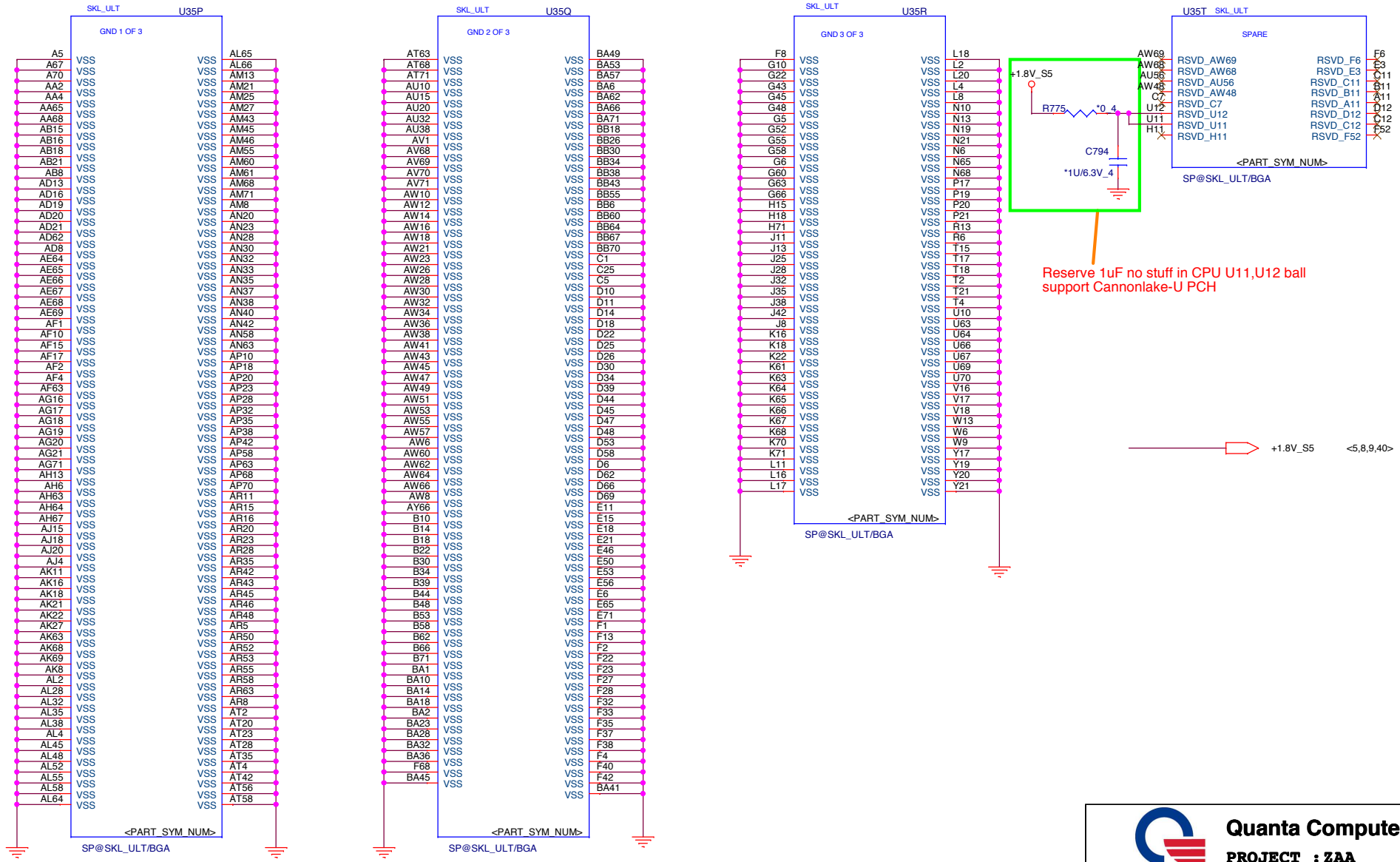
Quanta Computer Inc.
PROJECT : ZAA
Size | Document Number: Skylake 9/11 (PWROK/Board_ID) | Rev 1A
Date: Friday, February 05, 2016 | Sheet 8 of 48



Pin Name	Strap description	Configuration	Note
CFG[0]	Stall reset sequence after PCU PLL lock until de-asserted	1 = *Normal Operation; No stall (iPU 3K) 0 = Stall	
CFG[1]	Reserved Configuration lane		
CFG[2]	PCI Express* Static x16 Lane Numbering Reversal	1 = *Normal Operation(iPU 3K) 0 = Lan number reversed	H & S processor used only
CFG[3]	Reserved Configuration lane		
CFG[4]	eDP enable	1 = Disabled (iPU 3K) 0 = *Enabled	CFG4 R548 1K_4
CFG[6:5]	PCI Express* Bifunction	00 = 1x8, 2x4 PCI Express* 01 = reserved 10 = 2x8 PCI Express* 11 = 1x16 PCI Express*	H & S processor used only
CFG[7]	PEG Training	1 = *PEG Train immediatedly follow RESET# de-assertion (iPU 3K) 0 = PEG wait for BIOS for training	H & S processor used only
CFG[19:8]	Reserved Configuration lane		

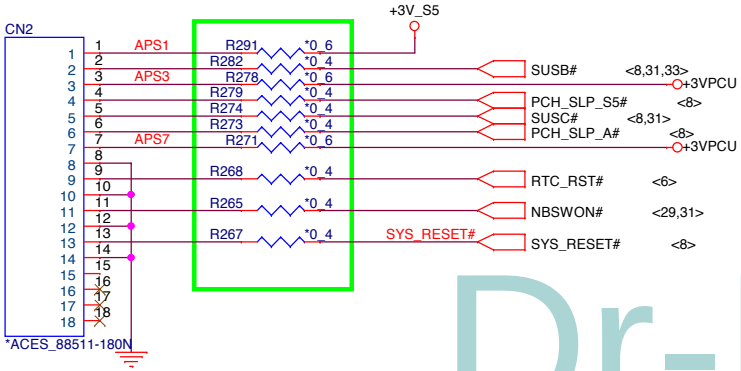
Quanta Computer Inc.	PROJECT : ZAA	
Size	Document Number: Skylake PCH-LP 15/19 (POWER)	Rev 1A
Date: Friday, February 05, 2016	Sheet 9 of 48	

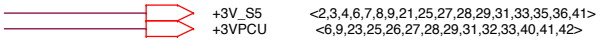
Skylake ULT (GND)



Quanta Computer Inc.			
PROJECT : ZAA			
Size	Document Number		Rev
	Skylake 10/17/18 (GND)		1A
Date: Friday, February 05, 2016	Sheet 10 of 48		

Intel APS Fixture use

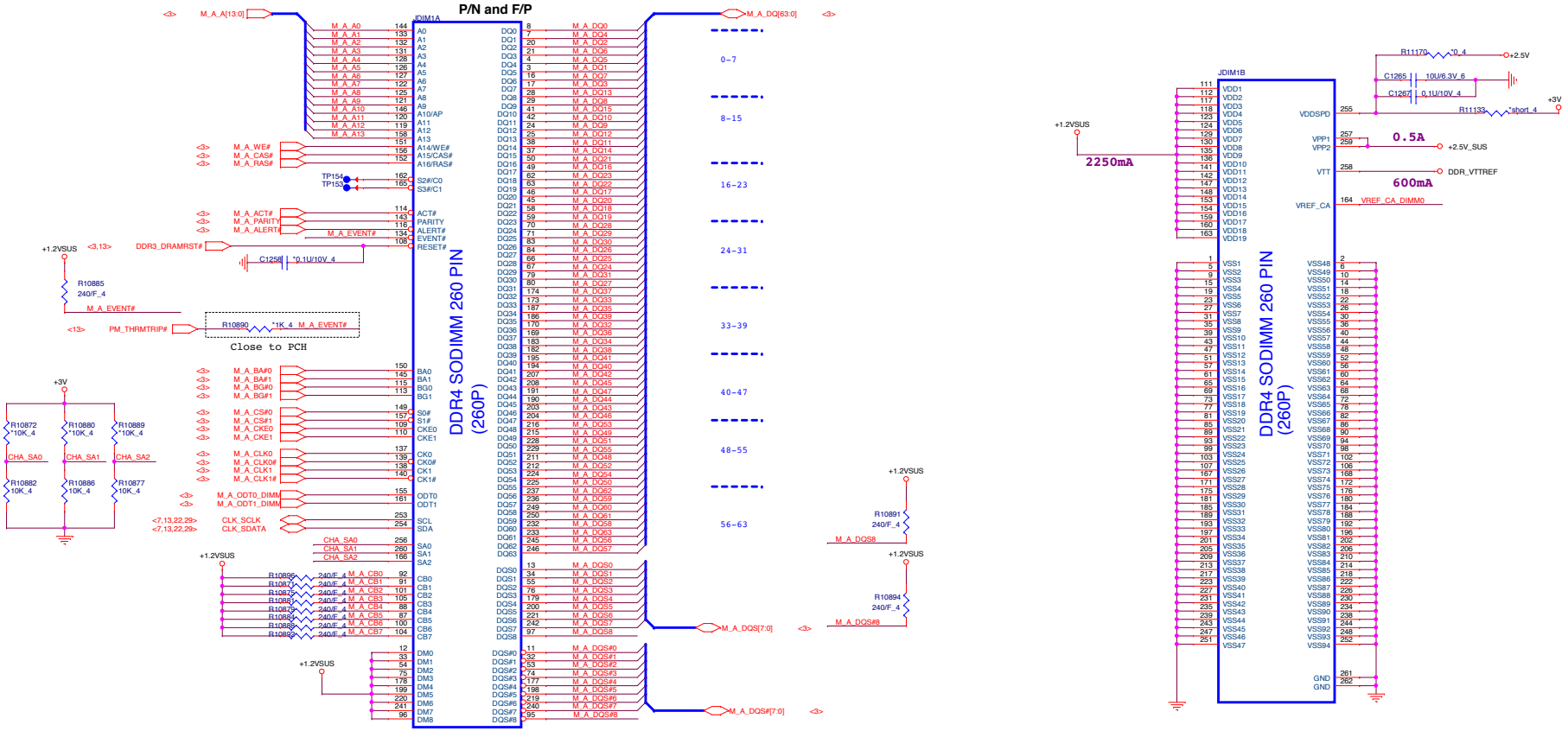


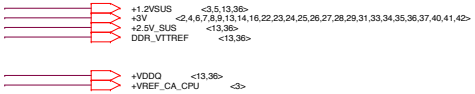


Quanta Computer Inc.

PROJECT : ZAA

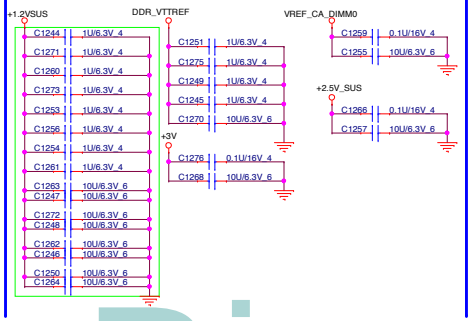
Size	Document Number	Rev
	CPU/PCH XDP	1A
Date: Friday, February 05, 2016	Sheet 11 of 48	



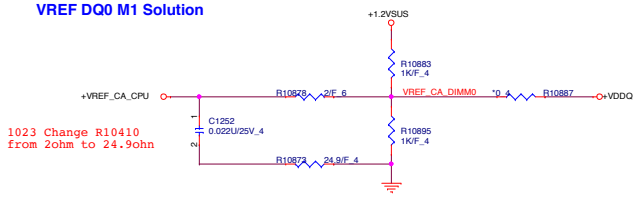


Place these Caps near So-Dimm1.

1uF/10uF 4pcs on each side of connector

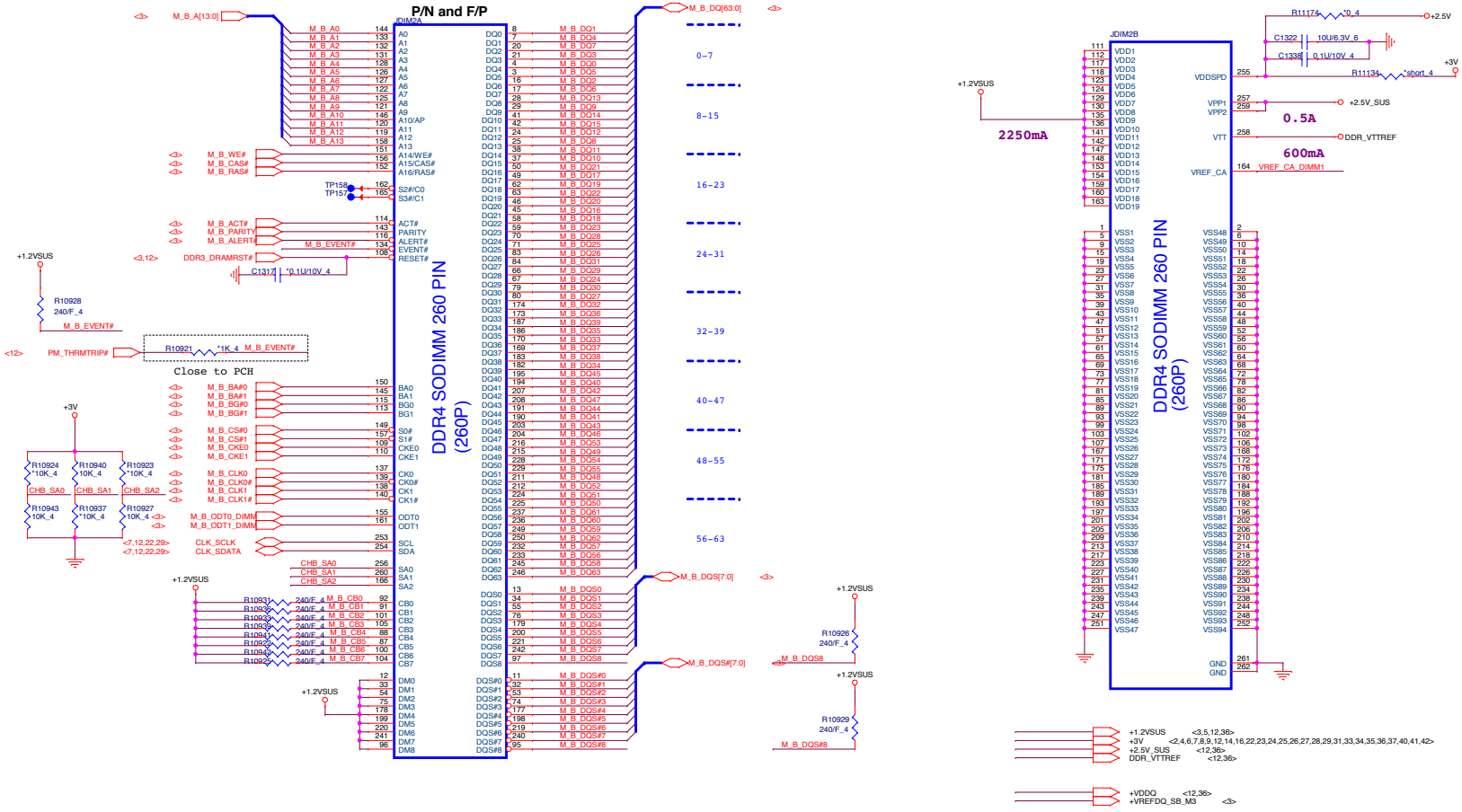


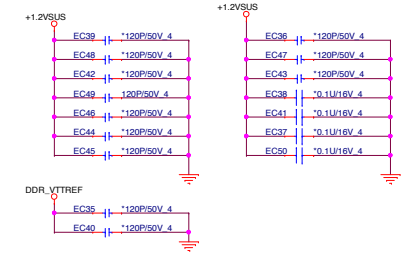
VREF DQ0 M1 Solution

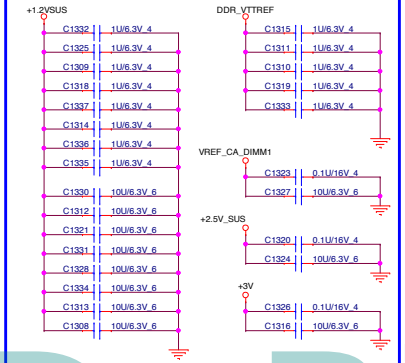


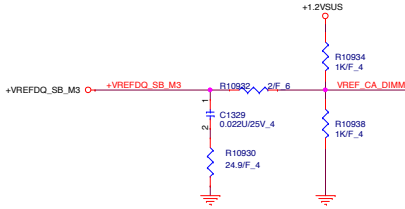
1023 Change R10410
from 2ohm to 24.9ohn

Quanta Computer Inc.		
PROJECT : ZAA		
Size	Document Number: DDR4 DIMM-STD(5.2H) CHA	Rev: 1A
Date: Friday, February 05, 2016	Sheet 12 of 48	









Quanta Computer Inc.

PROJECT : ZAA

Size	Document Number	Rev
	DDR4 DIMM-RVS(5.2H) CHB	1A

Date: Friday, February 05, 2016 Sheet 13 of 48

N16S-GT1-KA-A2 GM107-710-KA-A2 AJ0N16S0T22 B/S PN
N16S-GT1-KB-A2 GM107-710-KB-A2 AJSR2JK8T02
N16S-GTR-B-A2 GM108-770-A2 AJ0N16S0T24

U3002A
SP@N16P-GT
[PEG Interface]

PEX_IOVDD/Q : 3300mA
+1.05V_GFX
To be placed no further from the GPU than bewteen the PS and GPU
C4000 EV@22U/6.3V_6
C4001 EV@22U/6.3V_6
C4002 EV@22U/6.3V_6
C4003 EV@22U/6.3V_6
C4004 EV@10U/6.3V_6
C4005 EV@10U/6.3V_6
C4006 EV@10U/6.3V_6
C4007 EV@10U/6.3V_6
PLACE NEAR BALLS
C4008 EV@1U/6.3V_4
C4009 EV@1U/6.3V_4
C4010 EV@1U/6.3V_4
C4011 EV@1U/6.3V_4
PLACE UNDER BGA
C4012 EV@4.7U/6.3V_4
C4014 EV@4.7U/6.3V_4

AG19 PEX_IOVDD_1
AG21 PEX_IOVDD_2
AG22 PEX_IOVDD_3
AG24 PEX_IOVDD_4
AH21 PEX_IOVDD_5
AH25 PEX_IOVDD_6
AG13 PEX_IOVDDQ_1
AG15 PEX_IOVDDQ_2
AG16 PEX_IOVDDQ_3
AG18 PEX_IOVDDQ_4
AG25 PEX_IOVDDQ_5
AH15 PEX_IOVDDQ_6
AH18 PEX_IOVDDQ_7
AH26 PEX_IOVDDQ_8
AH27 PEX_IOVDDQ_9
AJ27 PEX_IOVDDQ_10
AK27 PEX_IOVDDQ_11
AL27 PEX_IOVDDQ_12
AM28 PEX_IOVDDQ_13
AN28 PEX_IOVDDQ_14

PEX_RX0 AN12
PEX_RX0_N AM12
PEX_RX1 AN14
PEX_RX1_N AM14
PEX_RX2 AP14
PEX_RX2_N AP15
PEX_RX3 AN15
PEX_RX3_N AM15
PEX_RX4 AN17
PEX_RX4_N AM17
PEX_RX5 AP17
PEX_RX5_N AP18
PEX_RX6 AN18
PEX_RX6_N AM18
PEX_RX7 AN20
PEX_RX7_N AM20
PEX_RX8 AP20
PEX_RX8_N AP21
PEX_RX9 AN21
PEX_RX9_N AM21
PEX_RX10 AN23
PEX_RX10_N AM23
PEX_RX11 AP23
PEX_RX11_N AP24
PEX_RX12 AN24
PEX_RX12_N AM24
PEX_RX13 AN26
PEX_RX13_N AM26
PEX_RX14 AP26
PEX_RX14_N AP27
PEX_RX15 AN27
PEX_RX15_N AM27

PEG_TX0 <6>
PEG_TX#0 <6>
PEG_TX1 <6>
PEG_TX#1 <6>
PEG_TX2 <6>
PEG_TX#2 <6>
PEG_TX3 <6>
PEG_TX#3 <6>

PEX_TX0 AK14 PEG_RXP0_C C4015 EV@0.22U/10V_4 PEG_RX0 <6>
PEX_TX0_N AJ14 PEG_RXN0_C C4016 EV@0.22U/10V_4 PEG_RX#0 <6>
PEX_TX1 AH14 PEG_RXP1_C C4017 EV@0.22U/10V_4 PEG_RX1 <6>
PEX_TX1_N AG14 PEG_RXN1_C C4018 EV@0.22U/10V_4 PEG_RX#1 <6>
PEX_TX2 AK15 PEG_RXP2_C C4020 EV@0.22U/10V_4 PEG_RX2 <6>
PEX_TX2_N AJ15 PEG_RXN2_C C4021 EV@0.22U/10V_4 PEG_RX#2 <6>
PEX_TX3 AL16 PEG_RXP3_C C4022 EV@0.22U/10V_4 PEG_RX3 <6>
PEX_TX3_N AK16 PEG_RXN3_C C4023 EV@0.22U/10V_4 PEG_RX#3 <6>
PEX_TX4 AK17
PEX_TX4_N AJ17
PEX_TX5 AH17
PEX_TX5_N AG17
PEX_TX6 AK18
PEX_TX6_N AJ18
PEX_TX7 AL19
PEX_TX7_N AK19
PEX_TX8 AK20
PEX_TX8_N AJ20
PEX_TX9 AH20
PEX_TX9_N AG20
PEX_TX10 AK21
PEX_TX10_N AJ21
PEX_TX11 AL22
PEX_TX11_N AK22
PEX_TX12 AK23
PEX_TX12_N AJ23
PEX_TX13 AH23
PEX_TX13_N AG23
PEX_TX14 AK24
PEX_TX14_N AJ24
PEX_TX15 AL25
PEX_TX15_N AK25

AC6 NC_1
AJ28 NC_2
AJ4 NC_3
AJ5 NC_4
AL11 NC_5
C15 NC_6
D19 NC_7
D20 NC_8
D23 NC_9
D26 NC_10
H31 NC_11
T8 NC_12
V32 NC_13
Y1 NC_14
Y2 NC_15
Y3 NC_16
AA1 NC_17
AA2 NC_18
AA3 NC_19
AA4 NC_20
AA5 NC_21
AA6 NC_22
AA7 NC_23
AA8 NC_24

PLACE CLOSE TO BGA
C4026 EV@4.7U/6.3V_4
C4027 EV@1U/6.3V_4
C4028 EV@0.1u/16V_4
C4029 *EV@0.1U/16V_4
C4031 *EV@0.1U/16V_4
PLACE CLOSE TO GPU BALLS
+3V_GFX
+3V_MAIN
VDD33 : 85mA
J8 3V3_AON_1
K8 3V3_AON_2
L8 3V3_MAIN_1
M8 3V3_MAIN_2
PLACE CLOSE TO BGA
C4032 EV@4.7U/6.3V_4
C4033 EV@1U/6.3V_4
PLACE CLOSE TO GPU BALLS
C4034 EV@0.1u/16V_4
C4035 EV@0.1u/16V_4

PEX_REFCLK AL13 CLK_PCIE_VGA <6>
PEX_REFCLK_N AK13 CLK_PCIE_VGA# <6>
PEX_TSTCLK_OUT AJ26 PEX_TSTCLK R4006 *EV@200/F_4
PEX_TSTCLK_OUT_N AK26 PEX_TSTCLK#
NC AJ11
PEX_RST_N AJ12 PEGX_RST# PEGX_RST# <17>
PEX_CLKREQ_N AK12 PEX_CLKREQ# R4008 EV@10K_4 +3V_GFX
PEX_TERMP AP29 PEX_TERMP R4009 EV@2.49K/F_4
TESTMODE AK11 TESTMODE R4011 EV@10K_4
PEX_PLLVDD AG26 PEX_PLLVDD PEX_PLLVDD : 150mA
PEX_PLL_HVDD AH12
PEX_SVDD_3V3 AG12
PEX_SVDD_3V3 : 210mA
EV@0.1u/16V_4 C4038
EV@4.7U/6.3V_4 C4039
EV@4.7U/6.3V_4 C4041
PLACE NEAR BGA
3.3V_AUX_NC
P8 3.3V_AUX
TP4000
VDD_SENSE L4 VGA_VCCSENSE <41>
GND_SENSE L5 VGA_VSSSENSE <41>

+1.05V_GFX
R4010 *short_6 B2A
C4036 EV@4.7U/6.3V_4 PLACE NEAR GPU
C4037 EV@1U/6.3V_4 PLACE NEAR GPU
C4040 EV@0.1u/16V_4 PLACE UNDER GPU BALLS

+3V_MAIN
PEX_CLKREQ# 1 2 3 CLK_PEGA_REQ# <6>
Q4002
EV@2N7002KW_115MA

+1.05V_GFX <15,16,42>
+3V_GFX <16,17,31,42>
+3V_MAIN <15,16,17>
+3V <2,4,6,7,8,9,12,13,16,22,23,24,25,26,27,28,29,31,33,34,35,36,37,40,41,42>

GC6:+3V_MAIN

GC6 Power control

3V MAIN POWER

3/11 GC6 timing issue from 200K change to 100K

+3V_GFX
R4000 EV@10K_4
C4013 EV@0.022U/25V_4
60mil
R4003 *0_8
R4001 EV@10K_4
R4002 EV@100K_4
Q4000 EV@AO3413
60mil
+3V_MAIN
+3V_MAIN_EN <17>
Q4001 EV@2N7002K
C4019 EV@0.022U/25V_4
N16V stuff not support GC6 2.0.

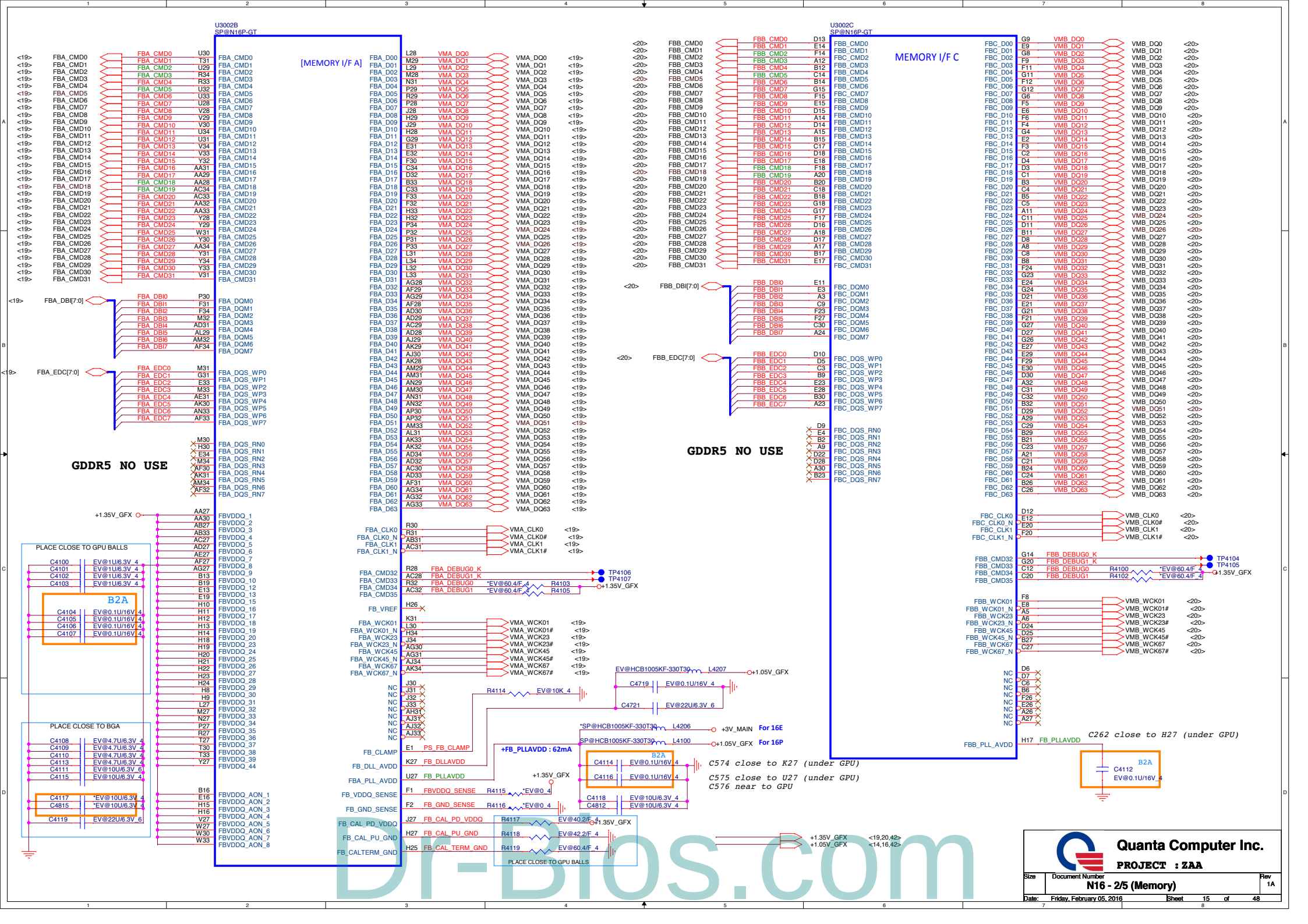
GC6 PEGX_RST#

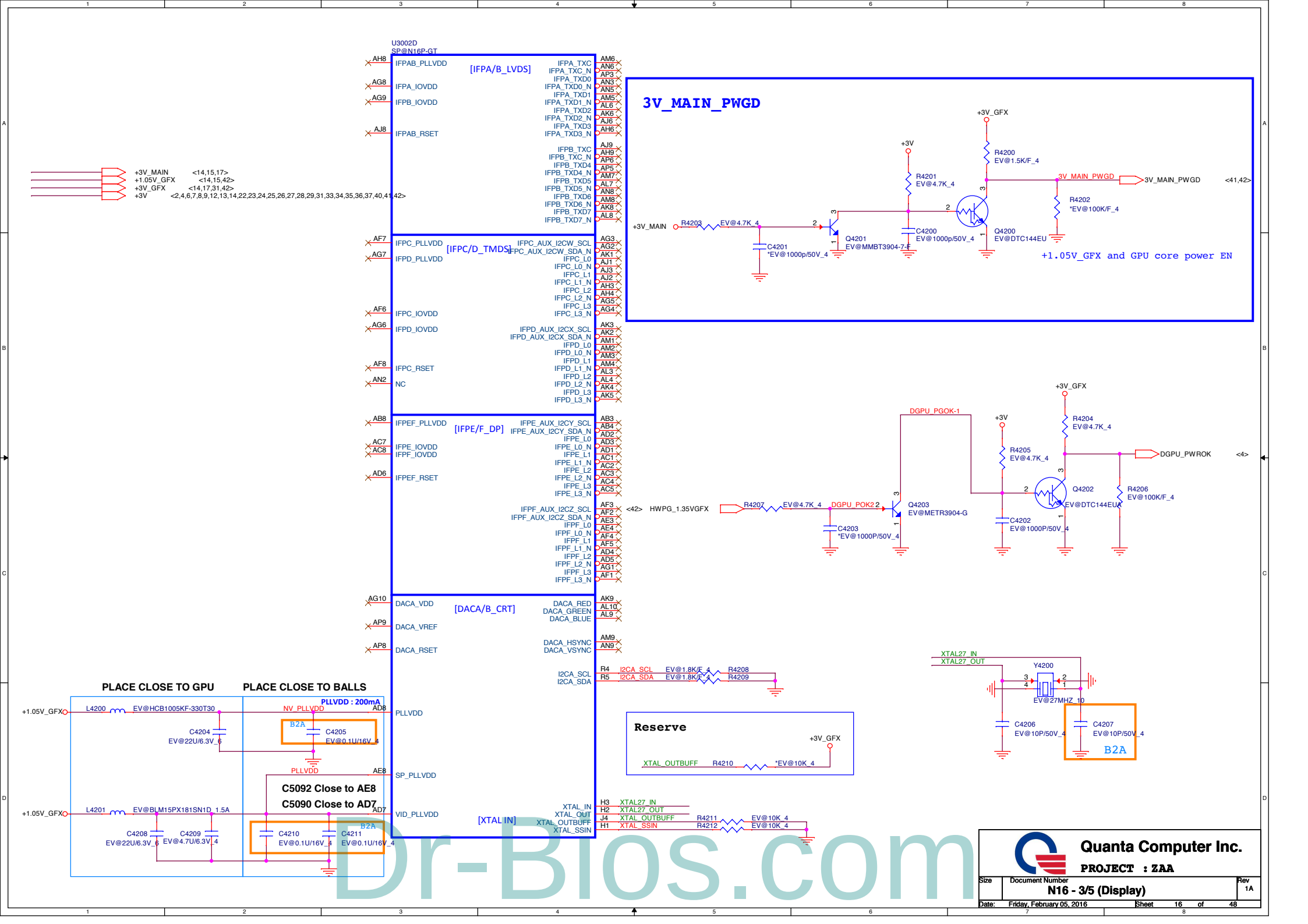
+3V
<17> SYS_PEX_RST_MON#
C4024 GC6@0.1U/16V_4
<8,25,27,28,31> PLTRST#
<4> DGPU_HOLD_RST#
C4030 EV@1000p/50V_4
U4001 GC6@74AHC1G09GW
RST_MON# R11108 *short_4
GPU_PEX_RST_HOLD#
U4002 GC6@TC7SH08FU(F)
C4025 GC6@0.1U/16V_4
R4004 *GC6@10K_4
PEGX_RST#
R4005 GC6@100K_4
*NGC6@0_4
RST_MON# R4007 PEGX_RST#

GC6 FBVDDQ_EN

<4,17> GC6_FB_EN GC6_FB_EN
<41> GPU_PWR_GD
D4000 GC6@BAT54CW_200MA
FBVDDQ_EN <42>
C3A
R4012 GC6@1M_4

Quanta Computer Inc.
PROJECT : ZAA
Size
Document Number N16 - 1/5 (PCIE)
Rev 1A
Date: Friday, February 05, 2016
Sheet 14 of 48


U3002B
SP@N16P-GT
[MEMORY I/F A]
U3002C
SP@N16P-GT
MEMORY I/F C
GDDR5 NO USE
GDDR5 NO USE
PLACE CLOSE TO GPU BALLS
PLACE CLOSE TO BGA
B2A
B2A
B2A
+FB_PLLAVDD : 62mA
C574 close to K27 (under GPU)
C575 close to U27 (under GPU)
C576 near to GPU
C262 close to H27 (under GPU)
For 16E
For 16P
PLACE CLOSE TO GPU BALLS
Quanta Computer Inc.
PROJECT : ZAA
Size
Document Number
N16 - 2/5 (Memory)
Rev
1A
Date: Friday, February 05, 2016
Sheet 15 of 48

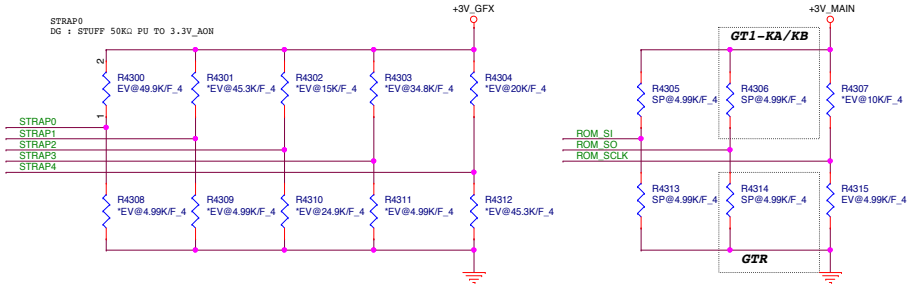

U3002D
SP@N16P-GT
[IFPA/B_LVDS]
[IFPC/D_TMDS]
[IFPE/F_DP]
[DACA/B_CRT]
[XTAL IN]
3V_MAIN_PWGD
+1.05V_GFX and GPU core power EN
Reserve
PLACE CLOSE TO GPU
PLACE CLOSE TO BALLS
PLLVDD : 200mA
C5092 Close to AE8
C5090 Close to AD7
Quanta Computer Inc.
PROJECT : ZAA
N16 - 3/5 (Display)
Date: Friday, February 05, 2016
Sheet 16 of 48
Dr-Bios.com

Default setting : N16S-GTR, Sansung 4GB

x16 (8L) #2					
SKU15 (B6)	SKU16 (B6)	SKU17 (B5)	SKU19 (B5)	SKU18	SKU20
GT3	(B6)			For VRAM Timing Tuning	
i5-6200U	i7-6500U	i5-6200U	i5-6200U	i5-6200U	i5-6200U
N16S-GTR	N16S-GTR	940M KA	940M KB	940M KA	940M KB
4G	4G	4G	4G	4G	4G
512x16x4	512x16x4	512x16x4	512x16x4	512x16x4	512x16x4
K4G80325FB-HC03 (Samsung)	MT51J256M32HF-60:A(Micron) (Micron)	K4G80325FB-HC03 (Samsung)	K4G80325FB-HC03 (Samsung)	MT51J256M32HF-60:A(Micron) (Micron)	MT51J256M32HF-60:A(Micron) (Micron)

	Package	DevID
(default) N16S-GTR	GB4b-128	0x134D
N16S-GT1-KA	GB4b-128	0x179c
N16S-GT1-KB	GB4b-128	0x179c

Resistor P/N
4.99K---> CS24992FB26
10K ---> CS31002FB26
15K ---> CS31502FB24
20K ---> CS32002FB29
24.9K --->CS32492FB16
30.1K --->CS33012FB18
34.8K---> CS33482FB22
45.3K ---> CS34532FB18
49.9K ---> CS34992FB10



	PU +3V_MAIN	PD
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

Mutil-level mode strapping:
Rx=40.2k PD
1.ROM_SCLK =4.99K PD
2.ROM_SO = 4.99K PD for GTR ;
4.99K UP for GT1-KA/KB
3.ROM_SI= VRAM Configuration Table
4.STRAP0 = 49.9k PU
5.Strap4~1 = Reserve Pull up and Pull down

N16S-GTR VRAM Configuration Table: *N16S-GTR-B-A2 GM108-770-A2 AJON16S0T24*

	ROM_SI	DESCRIPTION	Vendor	Vendor P/N	STN P/N	ROM_SI
4GbX2 (1GB)	0011 (0x3) 0110 (0x6)	GDDR5 128MBx32,2500MHz GDDR5 128MBx32,2500MHz	SAMSUNG HYNIX	K4G41325FC-HC03 --C die H5GC4H24AJR-T2C --A die	AKG5PGDT505 AKG5PWUTW21	20K Pull down 34.8K Pull down
4GbX4 (2GB)	0011 (0x3) 0110 (0x6)	GDDR5 256MBx16,2500MHz GDDR5 256MBx16,2500MHz	SAMSUNG HYNIX	K4G41325FC-HC03 --C die H5GC4H24AJR-T2C --A die	AKG5PGDT505 AKG5PWUTW21	20K Pull down 34.8K Pull down
8GbX2 (2GB)	0000 (0x0) 0001 (0x1)	GDDR5 256MBx32,2500MHz GDDR5 256MBx32,2500MHz	SAMSUNG MICRON	K4G80325FB-HC03 --B die MT51J256M32HF-60:A--A die	AKG5QGDT502 AKG5LGUTL04	4.99K Pull down 10K Pull down
8GbX4 (4GB)	0000 (0x0) 0001 (0x1)	GDDR5 512MBx16,2500MHz GDDR5 512MBx16,2500MHz	SAMSUNG MICRON	K4G80325FB-HC03 --B die MT51J256M32HF-60:A--A die	AKG5QGDT502 AKG5LGUTL04	4.99K Pull down 10K Pull down

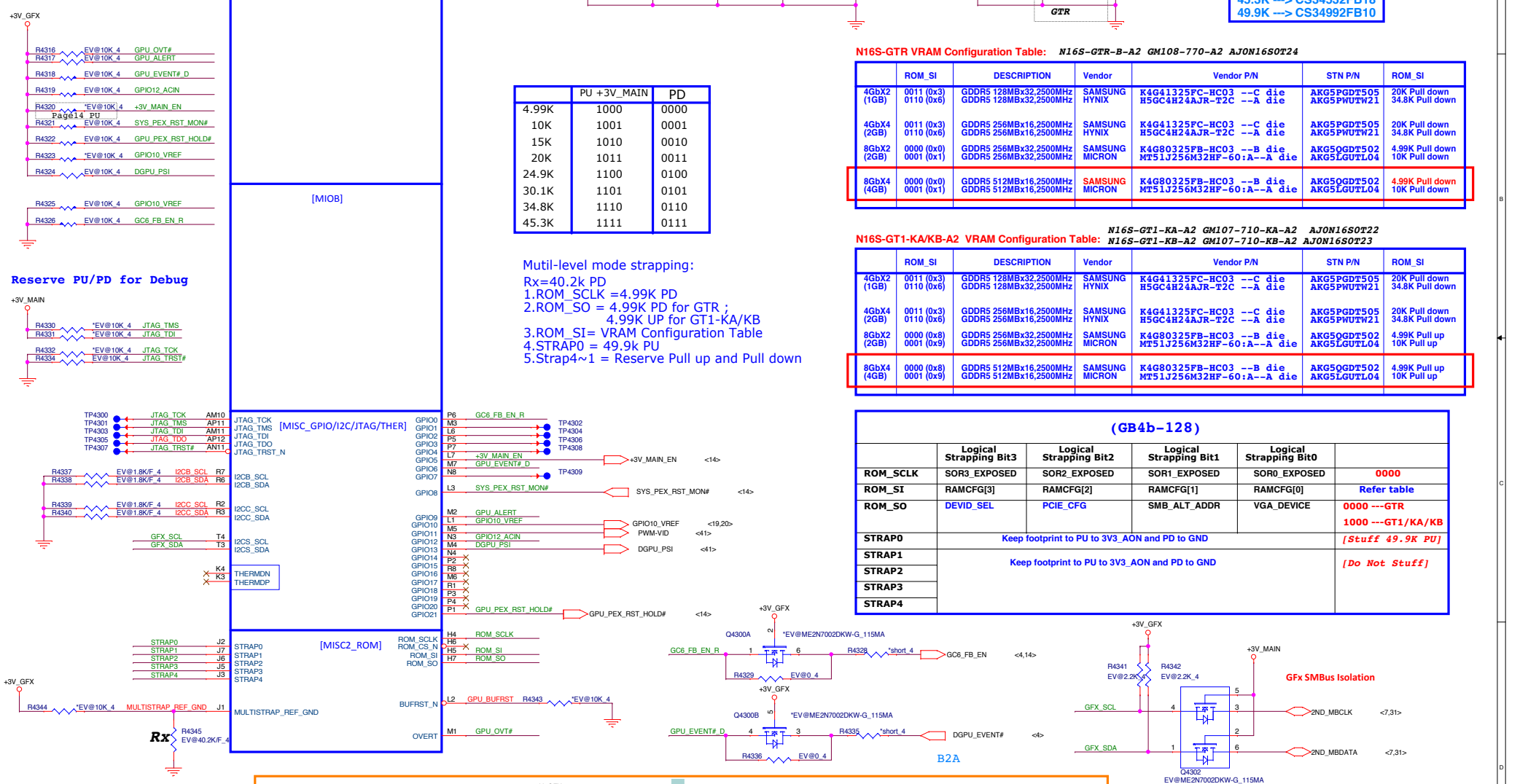
N16S-GT1-KA/KB-A2 VRAM Configuration Table: *N16S-GT1-KA-A2 GM107-710-KA-A2 AJON16S0T22* *N16S-GT1-KB-A2 GM107-710-KB-A2 AJON16S0T23*

	ROM_SI	DESCRIPTION	Vendor	Vendor P/N	STN P/N	ROM_SI
4GbX2 (1GB)	0011 (0x3) 0110 (0x6)	GDDR5 128MBx32,2500MHz GDDR5 128MBx32,2500MHz	SAMSUNG HYNIX	K4G41325FC-HC03 --C die H5GC4H24AJR-T2C --A die	AKG5PGDT505 AKG5PWUTW21	20K Pull down 34.8K Pull down
4GbX4 (2GB)	0011 (0x3) 0110 (0x6)	GDDR5 256MBx16,2500MHz GDDR5 256MBx16,2500MHz	SAMSUNG HYNIX	K4G41325FC-HC03 --C die H5GC4H24AJR-T2C --A die	AKG5PGDT505 AKG5PWUTW21	20K Pull down 34.8K Pull down
8GbX2 (2GB)	0000 (0x8) 0001 (0x9)	GDDR5 256MBx32,2500MHz GDDR5 256MBx32,2500MHz	SAMSUNG MICRON	K4G80325FB-HC03 --B die MT51J256M32HF-60:A--A die	AKG5QGDT502 AKG5LGUTL04	4.99K Pull up 10K Pull up
8GbX4 (4GB)	0000 (0x8) 0001 (0x9)	GDDR5 512MBx16,2500MHz GDDR5 512MBx16,2500MHz	SAMSUNG MICRON	K4G80325FB-HC03 --B die MT51J256M32HF-60:A--A die	AKG5QGDT502 AKG5LGUTL04	4.99K Pull up 10K Pull up

(GB4b-128)

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	0000
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	Refer table
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE	0000 ---GTR 1000 ---GT1/KA/KB
STRAP0	Keep footprint to PU to 3V3_AON and PD to GND				[Stuff 49.9K PU]
STRAP1	Keep footprint to PU to 3V3_AON and PD to GND				[Do Not Stuff]
STRAP2					
STRAP3					
STRAP4					

Reserve PU/PD for Debug



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PROJECT : ZAA

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	N16 - 4/5 (MISC)	1A
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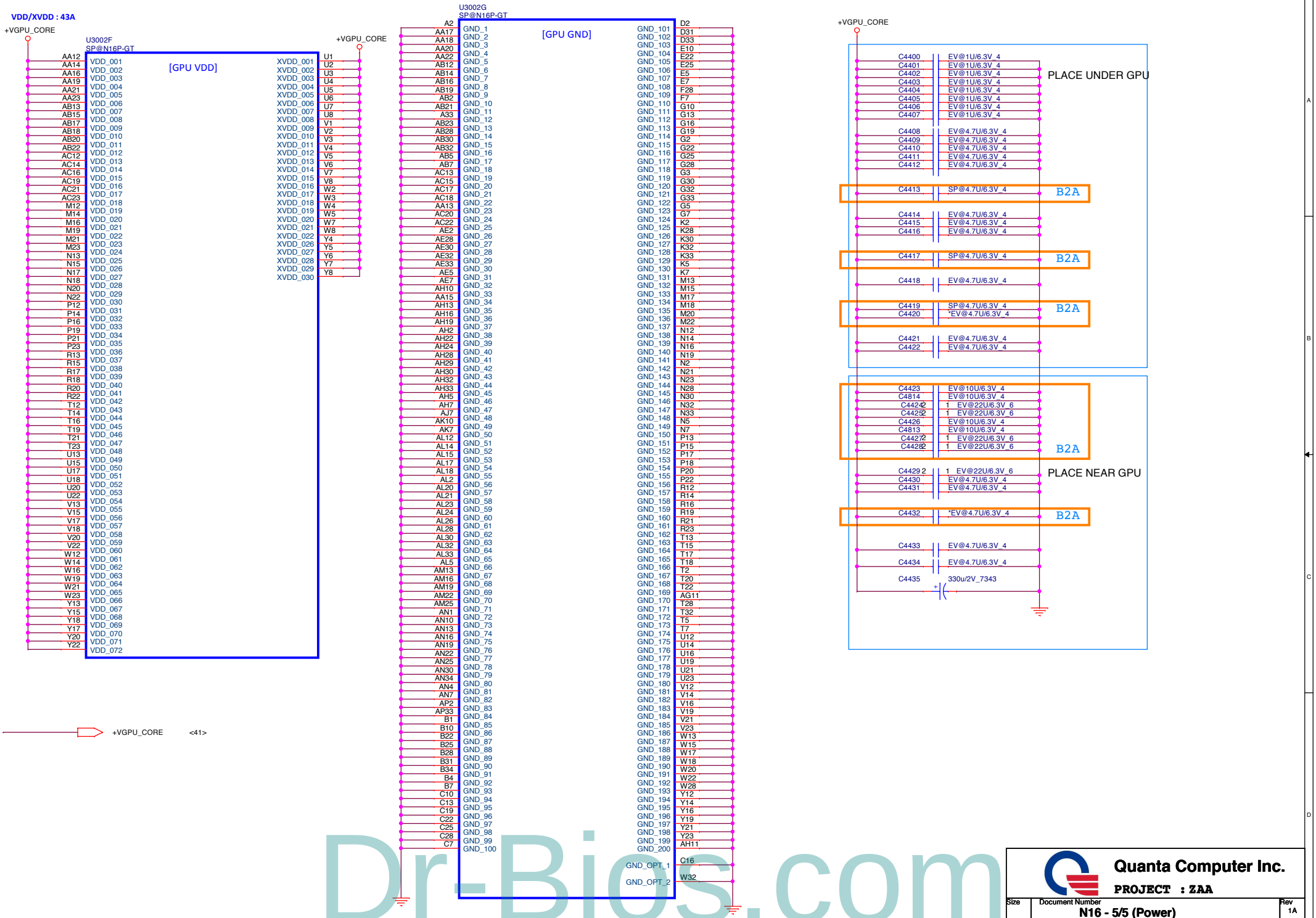
VDD/XVDD : 43A
+VGPU_CORE
U3002F
SP@N16P-GT
[GPU VDD]
VDD_001 VDD_002 VDD_003 VDD_004 VDD_005 VDD_006 VDD_007 VDD_008 VDD_009 VDD_010 VDD_011 VDD_012 VDD_013 VDD_014 VDD_015 VDD_016 VDD_017 VDD_018 VDD_019 VDD_020 VDD_021 VDD_022 VDD_023 VDD_024 VDD_025 VDD_026 VDD_027 VDD_028 VDD_029 VDD_030 VDD_031 VDD_032 VDD_033 VDD_034 VDD_035 VDD_036 VDD_037 VDD_038 VDD_039 VDD_040 VDD_041 VDD_042 VDD_043 VDD_044 VDD_045 VDD_046 VDD_047 VDD_048 VDD_049 VDD_050 VDD_051 VDD_052 VDD_053 VDD_054 VDD_055 VDD_056 VDD_057 VDD_058 VDD_059 VDD_060 VDD_061 VDD_062 VDD_063 VDD_064 VDD_065 VDD_066 VDD_067 VDD_068 VDD_069 VDD_070 VDD_071 VDD_072
AA12 AA14 AA16 AA19 AA21 AA23 AB13 AB15 AB17 AB18 AB20 AB22 AC12 AC14 AC16 AC19 AC21 AC23 M12 M14 M16 M19 M21 M23 N13 N15 N17 N18 N20 N22 P12 P14 P16 P19 P21 P23 R13 R15 R17 R18 R20 R22 T12 T14 T16 T19 T21 T23 U13 U15 U17 U18 U20 U22 V13 V15 V17 V18 V20 V22 W12 W14 W16 W19 W21 W23 Y13 Y15 Y18 Y17 Y20 Y22
+VGPU_CORE
XVDD_001 XVDD_002 XVDD_003 XVDD_004 XVDD_005 XVDD_006 XVDD_007 XVDD_008 XVDD_009 XVDD_010 XVDD_011 XVDD_012 XVDD_013 XVDD_014 XVDD_015 XVDD_016 XVDD_017 XVDD_018 XVDD_019 XVDD_020 XVDD_021 XVDD_022 XVDD_026 XVDD_027 XVDD_028 XVDD_029 XVDD_030
U1 U2 U3 U4 U5 U6 U7 U8 V1 V2 V3 V4 V5 V6 V7 V8 W2 W3 W4 W5 W7 W8 Y4 Y5 Y6 Y7 Y8
+VGPU_CORE <41>
U3002G
SP@N16P-GT
[GPU GND]
GND_1 GND_2 GND_3 GND_4 GND_5 GND_6 GND_7 GND_8 GND_9 GND_10 GND_11 GND_12 GND_13 GND_14 GND_15 GND_16 GND_17 GND_18 GND_19 GND_20 GND_21 GND_22 GND_23 GND_24 GND_25 GND_26 GND_27 GND_28 GND_29 GND_30 GND_31 GND_32 GND_33 GND_34 GND_35 GND_36 GND_37 GND_38 GND_39 GND_40 GND_41 GND_42 GND_43 GND_44 GND_45 GND_46 GND_47 GND_48 GND_49 GND_50 GND_51 GND_52 GND_53 GND_54 GND_55 GND_56 GND_57 GND_58 GND_59 GND_60 GND_61 GND_62 GND_63 GND_64 GND_65 GND_66 GND_67 GND_68 GND_69 GND_70 GND_71 GND_72 GND_73 GND_74 GND_75 GND_76 GND_77 GND_78 GND_79 GND_80 GND_81 GND_82 GND_83 GND_84 GND_85 GND_86 GND_87 GND_88 GND_89 GND_90 GND_91 GND_92 GND_93 GND_94 GND_95 GND_96 GND_97 GND_98 GND_99 GND_100
A2 AA17 AA18 AA20 AA22 AB12 AB14 AB16 AB19 AB2 AB21 A33 AB23 AB28 AB30 AB32 AB5 AB7 AC13 AC15 AC17 AC18 AA13 AC20 AC22 AE2 AE28 AE30 AE32 AE33 AE5 AE7 AH10 AA15 AH13 AH16 AH19 AH2 AH22 AH24 AH28 AH29 AH30 AH32 AH33 AH5 AH7 AJ7 AK10 AK7 AL12 AL14 AL15 AL17 AL18 AL2 AL20 AL21 AL23 AL24 AL26 AL28 AL30 AL32 AL33 AL5 AM13 AM16 AM19 AM22 AM25 AN1 AN10 AN13 AN16 AN19 AN22 AN25 AN30 AN34 AN4 AN7 AP2 AP33 B1 B10 B22 B25 B28 B31 B34 B4 B7 C10 C13 C19 C22 C25 C28 C7
GND_101 GND_102 GND_103 GND_104 GND_105 GND_106 GND_107 GND_108 GND_109 GND_110 GND_111 GND_112 GND_113 GND_114 GND_115 GND_116 GND_117 GND_118 GND_119 GND_120 GND_121 GND_122 GND_123 GND_124 GND_125 GND_126 GND_127 GND_128 GND_129 GND_130 GND_131 GND_132 GND_133 GND_134 GND_135 GND_136 GND_137 GND_138 GND_139 GND_140 GND_141 GND_142 GND_143 GND_144 GND_145 GND_146 GND_147 GND_148 GND_149 GND_150 GND_151 GND_152 GND_153 GND_154 GND_155 GND_156 GND_157 GND_158 GND_159 GND_160 GND_161 GND_162 GND_163 GND_164 GND_165 GND_166 GND_167 GND_168 GND_169 GND_170 GND_171 GND_172 GND_173 GND_174 GND_175 GND_176 GND_177 GND_178 GND_179 GND_180 GND_181 GND_182 GND_183 GND_184 GND_185 GND_186 GND_187 GND_188 GND_189 GND_190 GND_191 GND_192 GND_193 GND_194 GND_195 GND_196 GND_197 GND_198 GND_199 GND_200
D2 D31 D33 E10 E22 E25 E5 E7 F28 F7 G10 G13 G16 G19 G2 G22 G25 G28 G3 G30 G32 G33 G5 G7 K2 K28 K30 K32 K33 K5 K7 M13 M15 M17 M18 M20 M22 N12 N14 N16 N19 N2 N21 N23 N28 N30 N32 N33 N5 N7 P13 P15 P17 P18 P20 P22 R12 R14 R16 R19 R21 R23 T13 T15 T17 T18 T2 T20 T22 AG11 T28 T32 T5 T7 U12 U14 U16 U19 U21 U23 V12 V14 V16 V19 V21 V23 W13 W15 W17 W18 W20 W22 W28 Y12 Y14 Y16 Y19 Y21 Y23 AH11
GND_OPT_1 C16
GND_OPT_2 W32
+VGPU_CORE
PLACE UNDER GPU
C4400 EV@1U/6.3V_4
C4401 EV@1U/6.3V_4
C4402 EV@1U/6.3V_4
C4403 EV@1U/6.3V_4
C4404 EV@1U/6.3V_4
C4405 EV@1U/6.3V_4
C4406 EV@1U/6.3V_4
C4407 EV@1U/6.3V_4
C4408 EV@4.7U/6.3V_4
C4409 EV@4.7U/6.3V_4
C4410 EV@4.7U/6.3V_4
C4411 EV@4.7U/6.3V_4
C4412 EV@4.7U/6.3V_4
C4413 SP@4.7U/6.3V_4 B2A
C4414 EV@4.7U/6.3V_4
C4415 EV@4.7U/6.3V_4
C4416 EV@4.7U/6.3V_4
C4417 SP@4.7U/6.3V_4 B2A
C4418 EV@4.7U/6.3V_4
C4419 SP@4.7U/6.3V_4 B2A
C4420 *EV@4.7U/6.3V_4
C4421 EV@4.7U/6.3V_4
C4422 EV@4.7U/6.3V_4
C4423 EV@10U/6.3V_4
C4814 EV@10U/6.3V_4
C4424 1 EV@22U/6.3V_6
C4425 1 EV@22U/6.3V_6
C4426 EV@10U/6.3V_4
C4813 EV@10U/6.3V_4
C4427 1 EV@22U/6.3V_6
C4428 1 EV@22U/6.3V_6 B2A
PLACE NEAR GPU
C4429 1 EV@22U/6.3V_6
C4430 EV@4.7U/6.3V_4
C4431 EV@4.7U/6.3V_4
C4432 *EV@4.7U/6.3V_4 B2A
C4433 EV@4.7U/6.3V_4
C4434 EV@4.7U/6.3V_4
C4435 330u/2V_7343
Quanta Computer Inc.
PROJECT : ZAA
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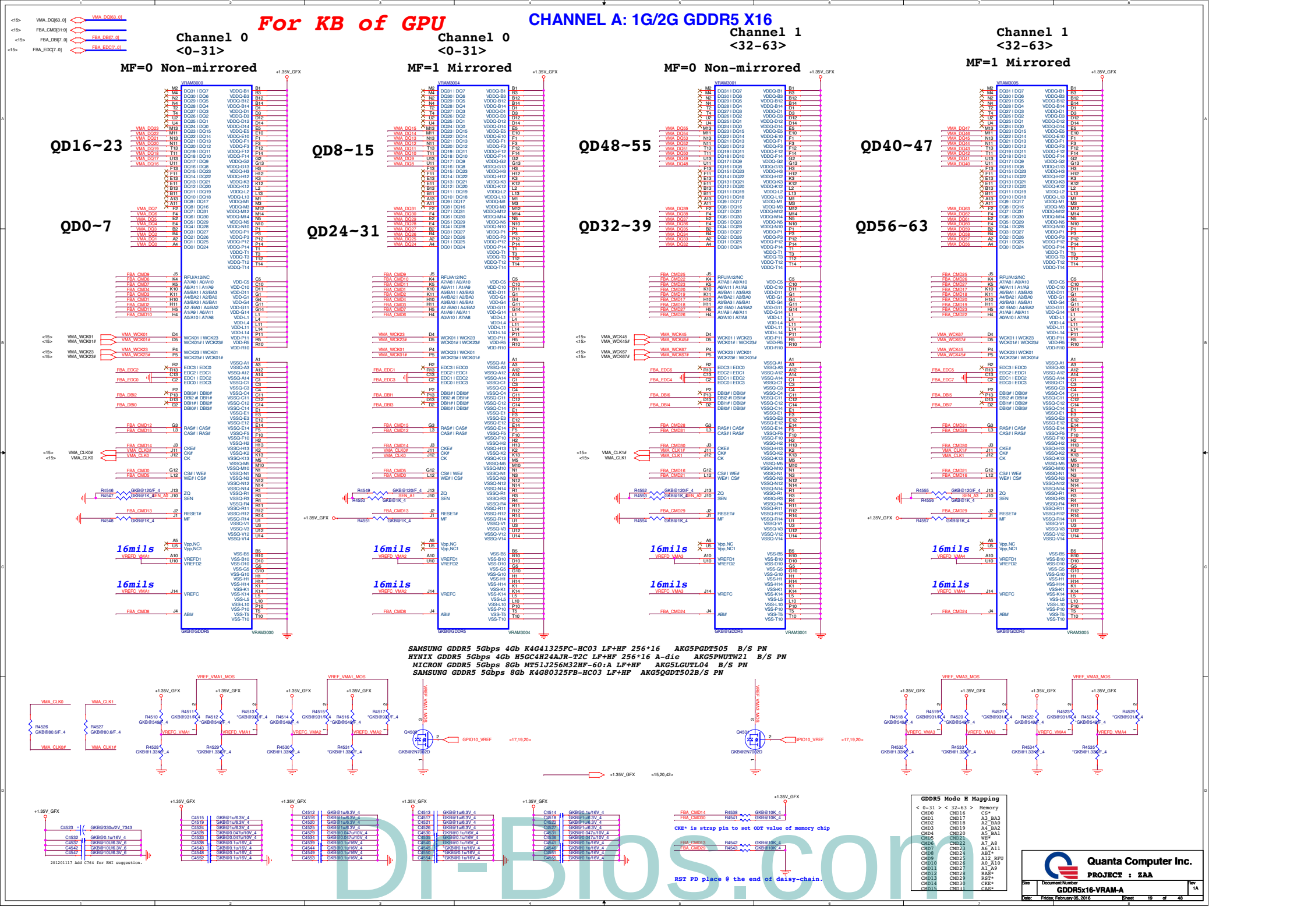

For KB of GPU
CHANNEL A: 1G/2G GDDR5 X16
Channel 0 <0-31>
MF=0 Non-mirrored
Channel 0 <0-31>
MF=1 Mirrored
Channel 1 <32-63>
MF=0 Non-mirrored
Channel 1 <32-63>
MF=1 Mirrored
QD16~23
QD8~15
QD48~55
QD40~47
QD0~7
QD24~31
QD32~39
QD56~63
VMA_DQ[63..0]
FBA_CMD[31:0]
FBA_DBI[7..0]
FBA_EDC[7..0]
+1.35V_GFX
16mils
SAMSUNG GDDR5 5Gbps 4Gb K4G41325FC-HC03 LF+HF 256*16 AKG5PGDT505 B/S PN
HYNIX GDDR5 5Gbps 4Gb H5GC4H24AJR-T2C LF+HF 256*16 A-die AKG5PWUTW21 B/S PN
MICRON GDDR5 5Gbps 8Gb MT51J256M32HF-60:A LF+HF AKG5LGUTL04 B/S PN
SAMSUNG GDDR5 5Gbps 8Gb K4G80325FB-HC03 LF+HF AKG5QGDT502B/S PN
CKE* is strap pin to set ODT value of memory chip
RST PD place @ the end of daisy-chain.
GDDR5 Mode H Mapping
Quanta Computer Inc.
PROJECT : ZAA
GDDR5x16-VRAM-A
Friday, February 05, 2016

For KA of GPU

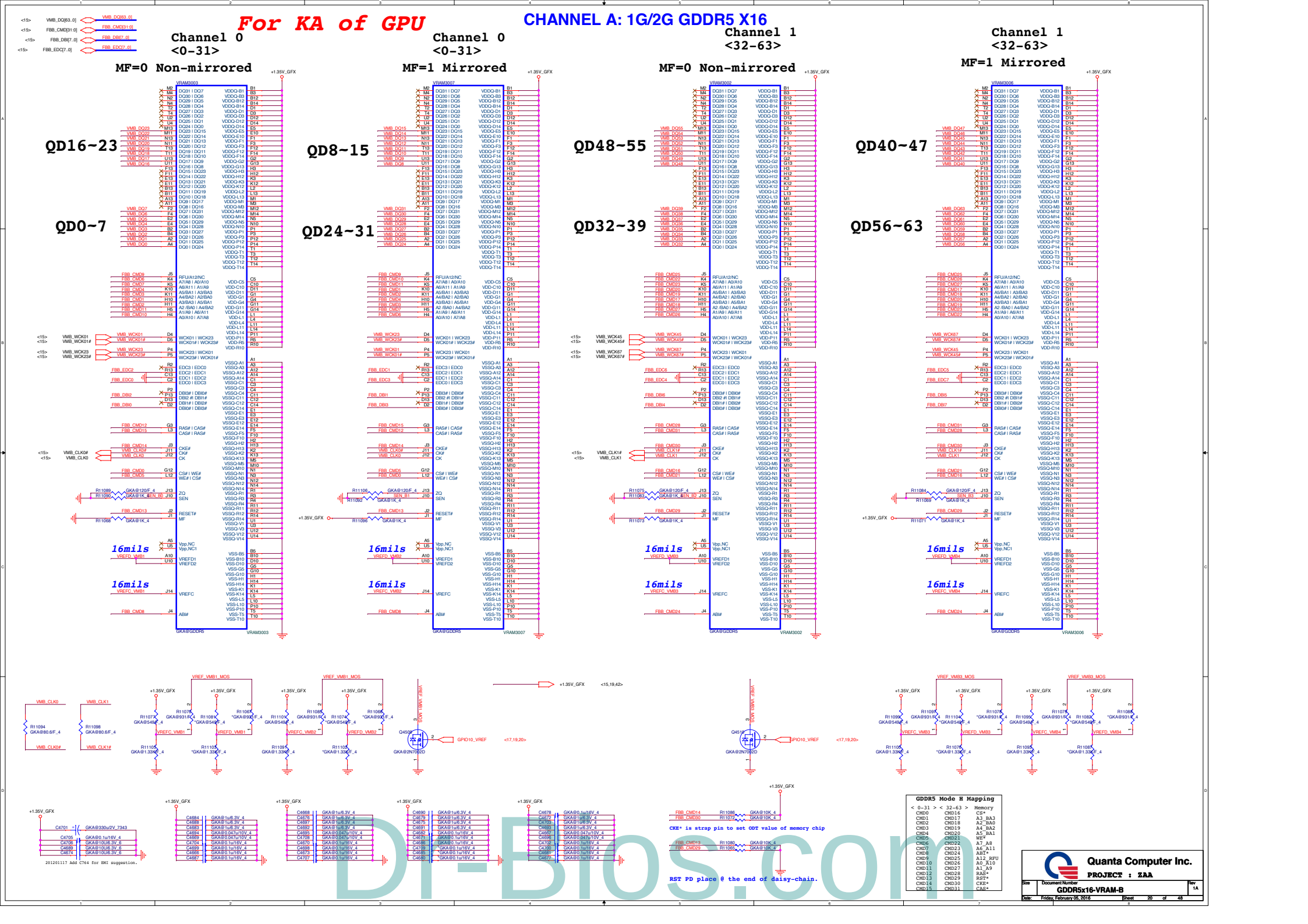
CHANNEL A: 1G/2G GDDR5 X16

Channel 0 <0-31> — MF=0 Non-mirrored — QD16~23 / QD0~7

Channel 0 <0-31> — MF=1 Mirrored — QD8~15 / QD24~31

Channel 1 <32-63> — MF=0 Non-mirrored — QD48~55 / QD32~39

Channel 1 <32-63> — MF=1 Mirrored — QD40~47 / QD56~63



USB TYPE-C

USB2.0 ESD

Close to connector

Type C1_HSIO_ ESD

USB3 Re-Driver

Vendor suggest input cap 120u

CHG	CHG_HI	CC Capability Broadcast	Current Limit	Load Detect Threshold
0	0	STD	1.67 A	NA
0	1	STD	1.67 A	NA
1	0	1.5 A	1.67 A	NA
1	1	3.0 A	3.34 A	1.77 A

TPS25810 Port	CC1	CC2	TPS25810 Response					
			OUT	VCONN On CC1 or CC2	POLb	UFPb	AUDIOb	DEBUGb
Nothing Attached	OPEN	OPEN	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
UFP Connected	Rd	OPEN	IN1	NO	Hi-Z	LOW	Hi-Z	Hi-Z
UFP Connected	OPEN	Rd	IN1	NO	LOW	LOW	Hi-Z	Hi-Z
Powered Cable/No UFP Connected	OPEN	Ra	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Powered Cable/No UFP Connected	Ra	OPEN	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Powered Cable/UFP Connected	Rd	Ra	IN1	CC2	Hi-Z	LOW	Hi-Z	Hi-Z
Powered Cable/UFP Connected	Ra	Rd	IN1	CC1	LOW	LOW	Hi-Z	Hi-Z
Debug Accessory Connected	Rd	Rd	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	LOW
Audio Adapter Accessory Connected	Ra	Ra	OPEN	NO	Hi-Z	Hi-Z	LOW	Hi-Z

A_EQ0 B_EQ0	A_EQ1 B_EQ1		A_DE0 B_DE0	A_DE1 B_DE1	
0	0	9dB	0	0	-3.5dB
0	1	3dB	0	1	no de-emphasis
1	0	6dB	1	0	-7dB
1	1	7.5dB	1	1	-5dB

TST : Low = Normal LFPS swing / Hight =Turn down LFPS swing

Quanta P/NAMAZING P/NUSD保護位置
BC104308Z00AZ1043-08F.R7G0.08TX RX (USB3.0 GEN1 5G)
BC104508Z00AZ1045-08F.R7G0.08D+ D- SBU1 SBU2 CC1 CC2
BC005725Z00AZ5725-01F.R7G0.009 PD 5V (follow ZAA)

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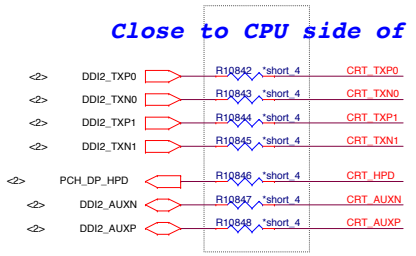
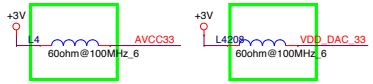
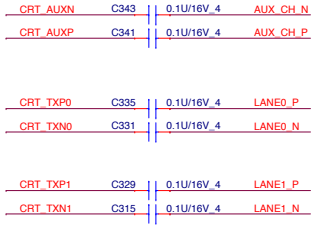
DP TO VGA

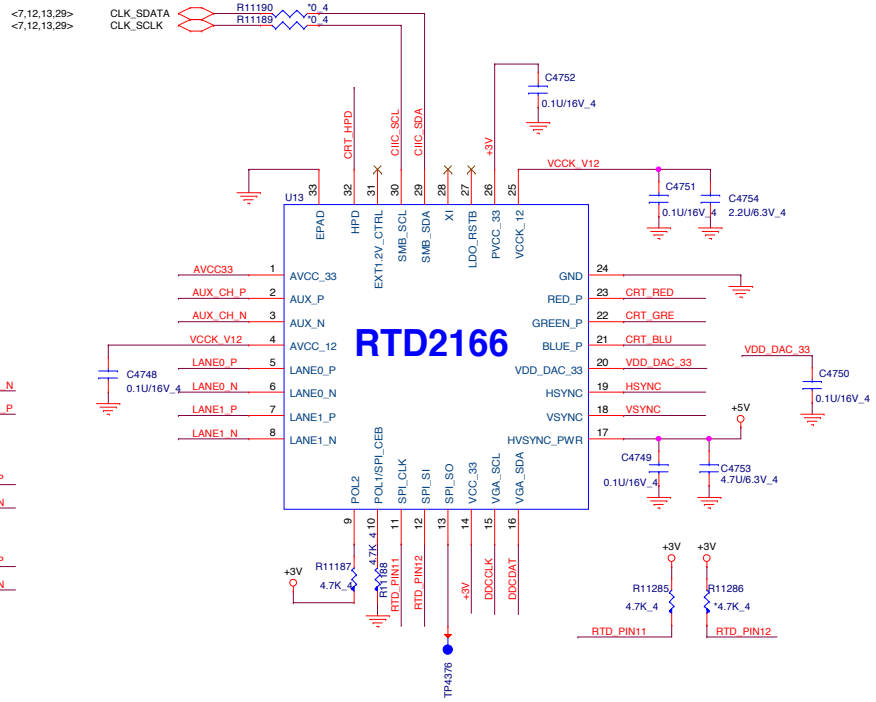
Close to CPU side of CAP.



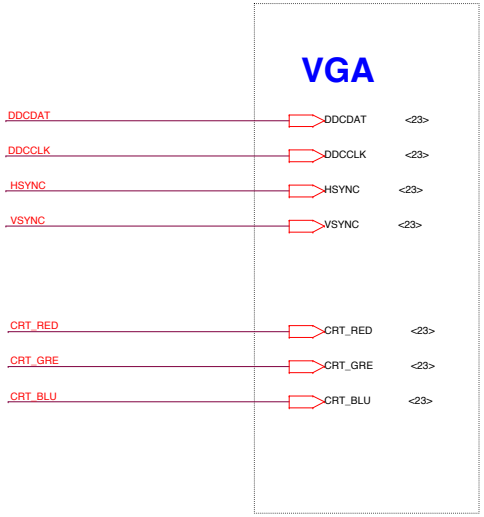
Power







VGA



Note:

1- C1,C3,C4,C5,C11,C16, C21 should be placed close to chip

2- C5 shold be X5R material

3- R6, R7, R8 should be 75 ohm with +/-1%

4- Suggest to connect Pin 29 and Pin 30 to PCH SMBUS for debug purpose.

5- This configuration is for internal ROM mode and using embedded LDO mode.

Quanta Computer Inc.		
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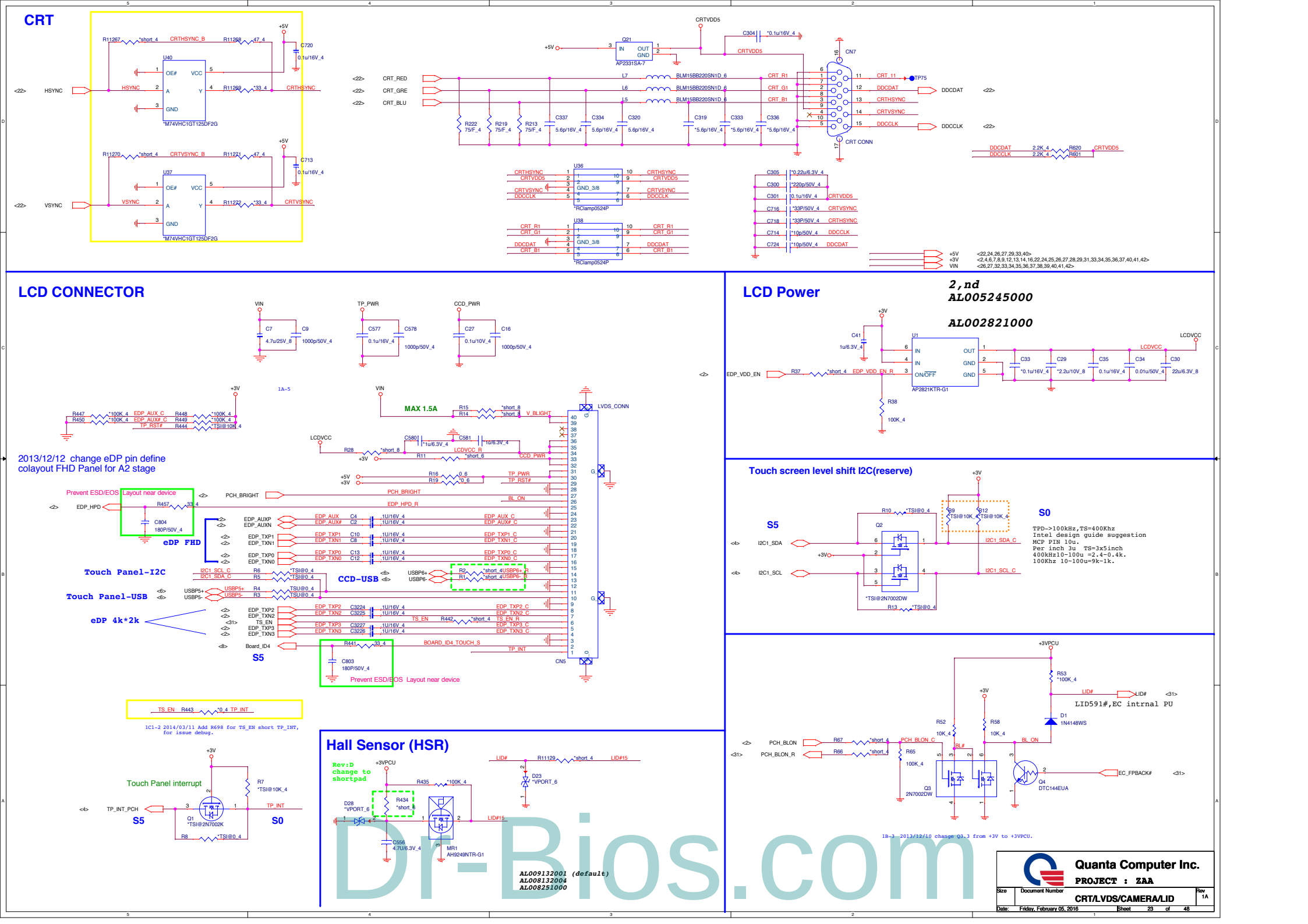
CRT
LCD CONNECTOR
LCD Power
2,nd
AL005245000
AL002821000
Touch screen level shift I2C(reserve)
S5
S0
Touch Panel-I2C
Touch Panel-USB
eDP 4k*2k
eDP FHD
CCD-USB
Prevent ESD/EOS Layout near device
2013/12/12 change eDP pin define
colayout FHD Panel for A2 stage
MAX 1.5A
LVDS_CONN
CN5
CN7
CRT CONN
Touch Panel interrupt
Hall Sensor (HSR)
Rev:D change to shortpad
AL009132001 (default)
AL008132004
AL008251000
LID591#,EC intrnal PU
Quanta Computer Inc.
PROJECT : ZAA
CRT/LVDS/CAMERA/LID
Rev 1A
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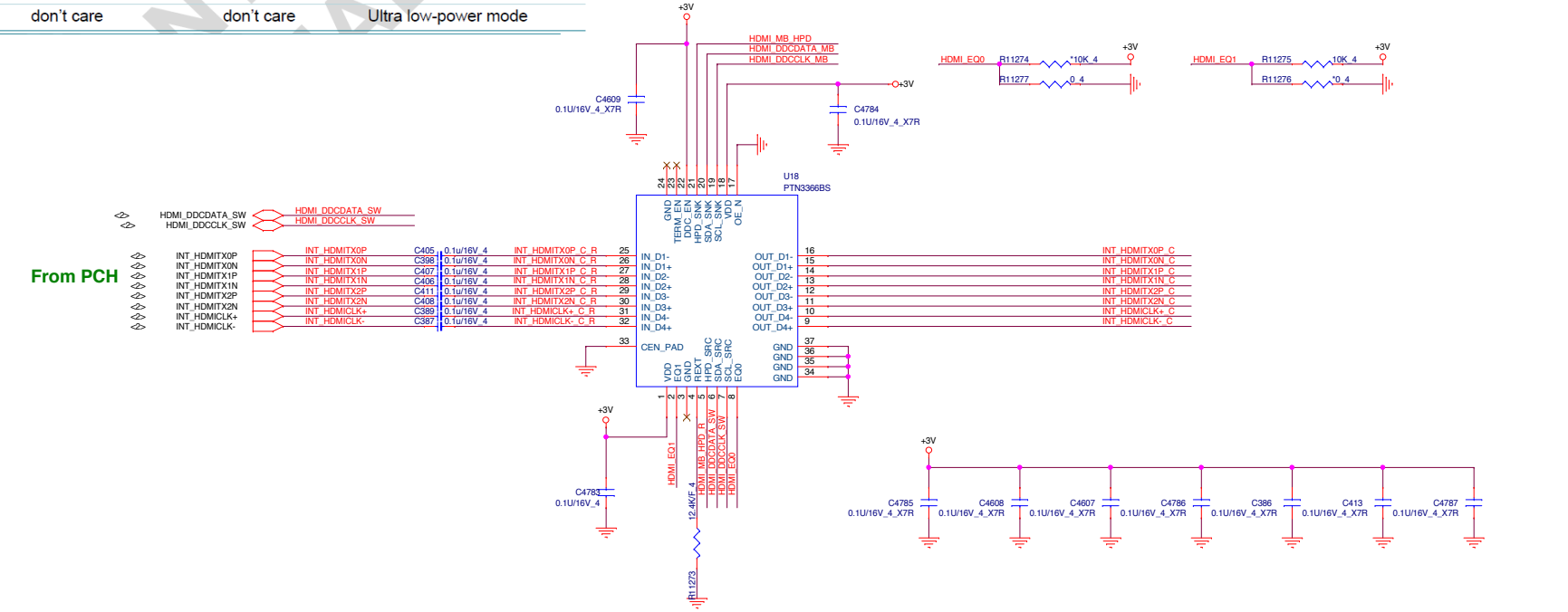
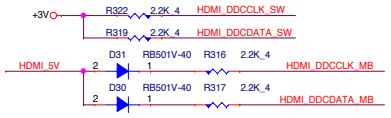
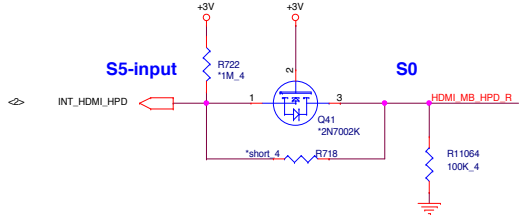
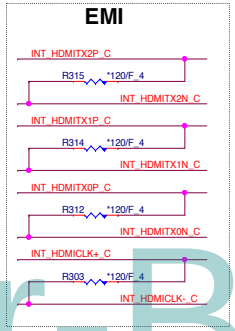
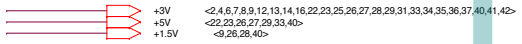
OE_N	DDC_EN	HPD_SINK	Source output	PTN3366 power mode
LOW	HIGH	HIGH	source active	Active mode; DDC active
LOW	LOW	LOW	don't care	Standby mode
HIGH	LOW	don't care	don't care	Ultra low-power mode



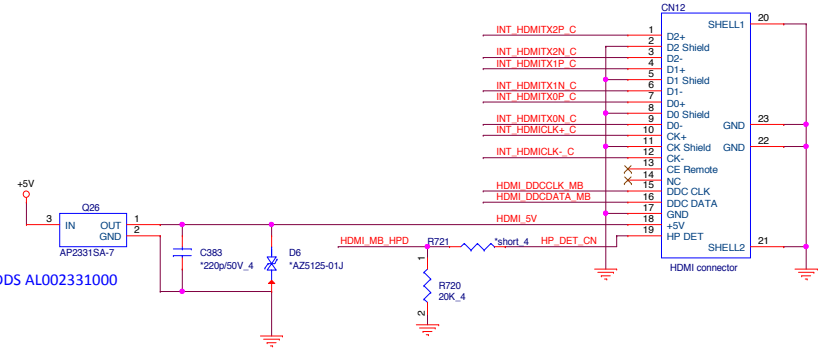








HDMI connector



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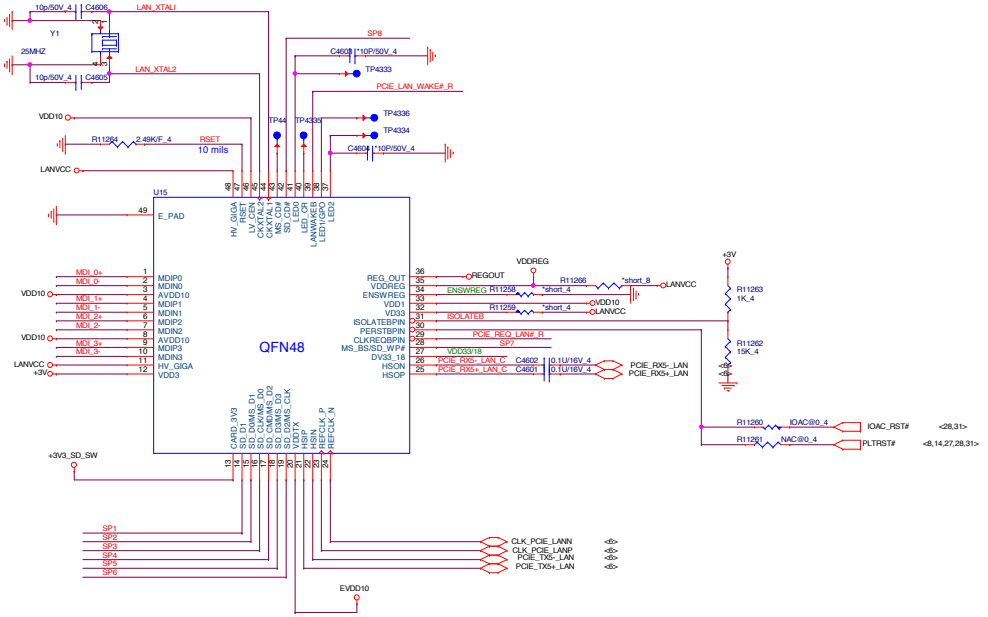
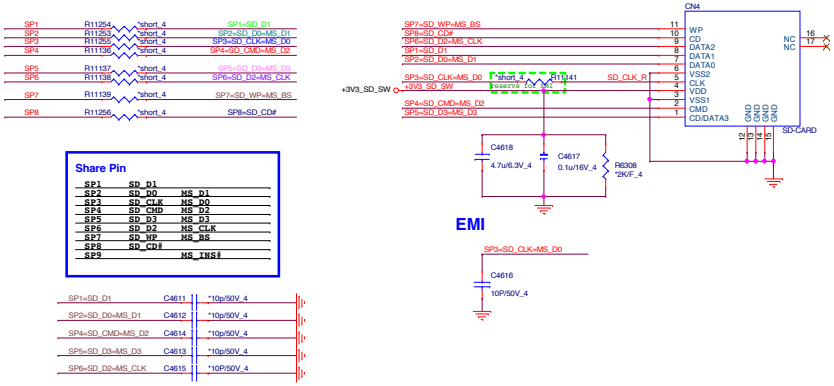
LAN & Card reader Combo (LAN)

Giga LAN (LAN)

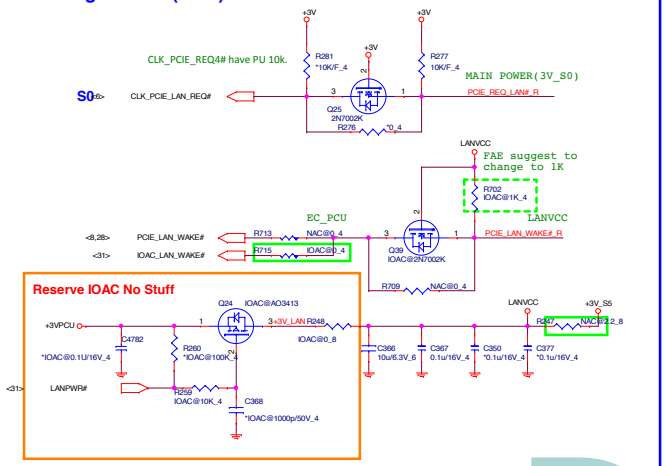


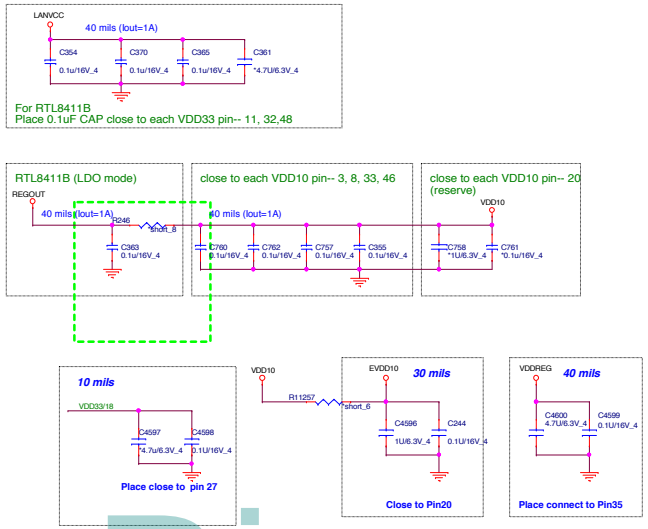
Card Reader (CRD)

2'nd source
-->DFHS11FR170



Leakage circuit (MPC)

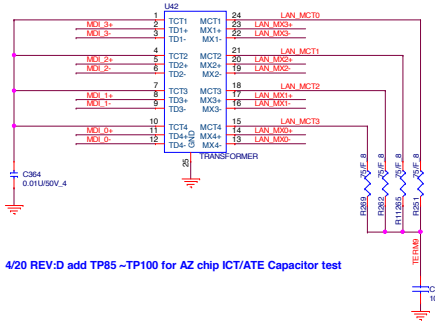




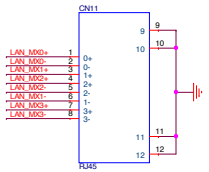
Tramsformer

DB0LL1LAN00 --> Main
DB0Z06LAN00 --> 2'nd
DB0X81LAN00 --> 2'nd

Layout:All termination signal should have 30 mil trace



RJ45 Connector



4/20 REV:D add TP85 ~TP100 for AZ chip ICT/ATE Capacitor test

Quanta Computer Inc.
PROJECT : ZAA
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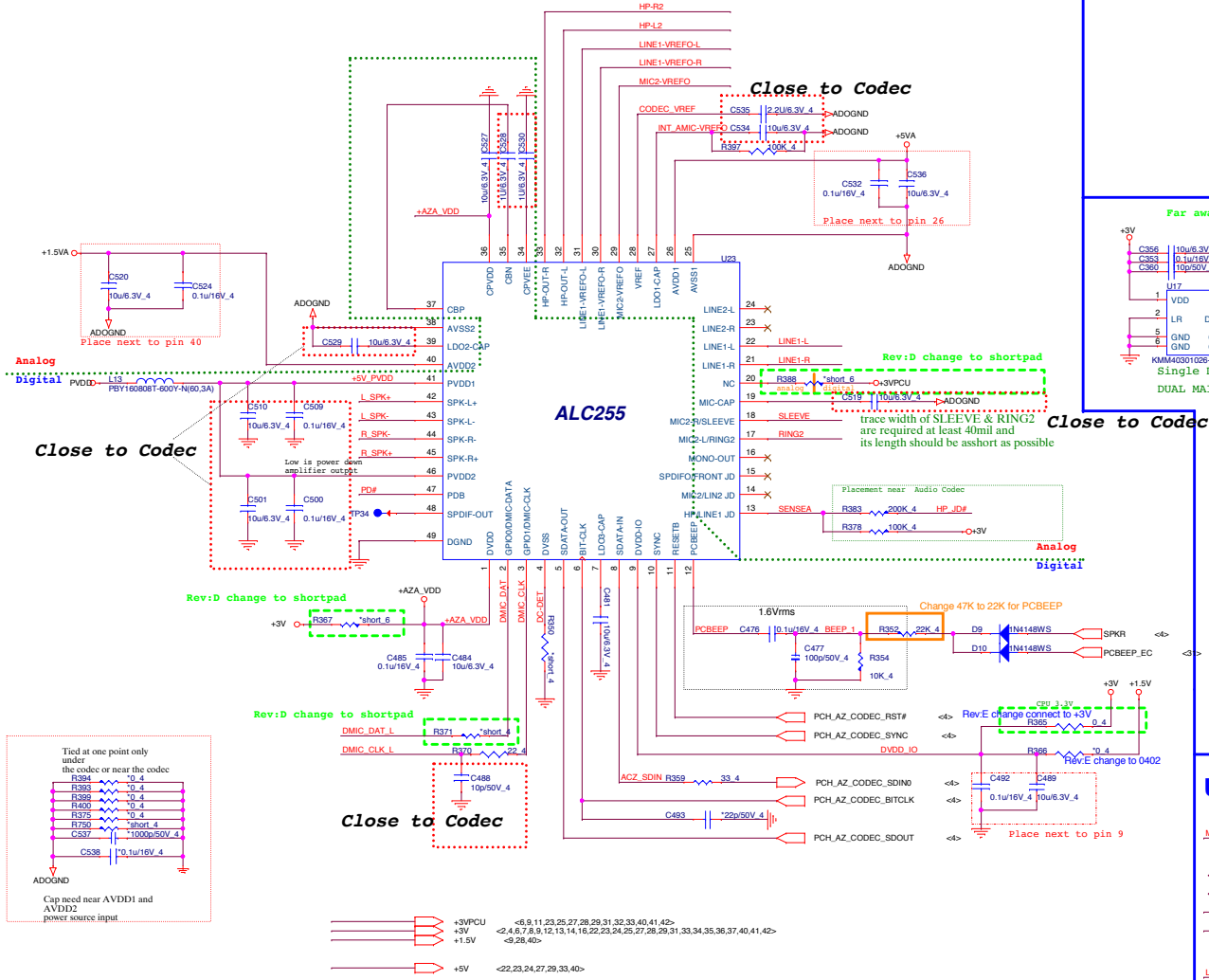
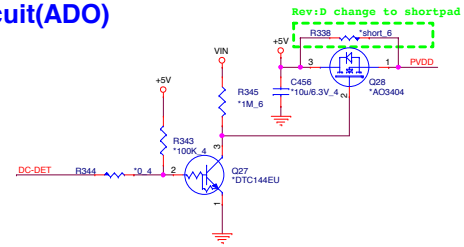
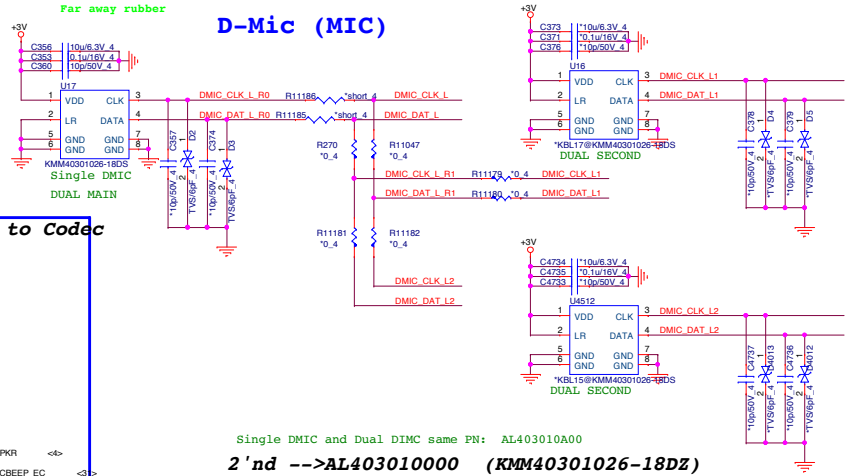
Codec(ADO)



DC-DET circuit(ADO)



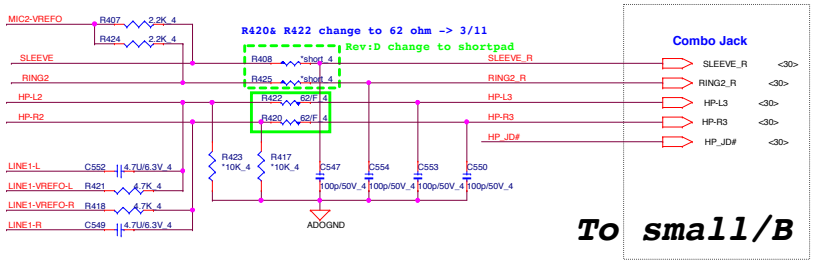
D-Mic (MIC)



Single DMIC and Dual DIMC same PN: AL403010A00

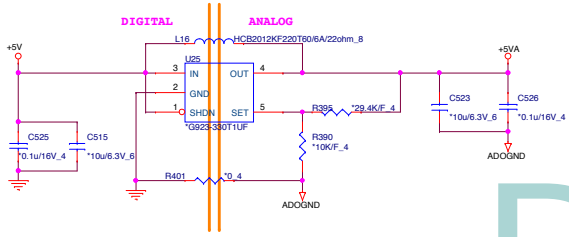
2'nd -->AL403010000 (KMM40301026-18DZ)

Universal Audio Jack HEADPHONE/MIC/LINE combo (ADO)

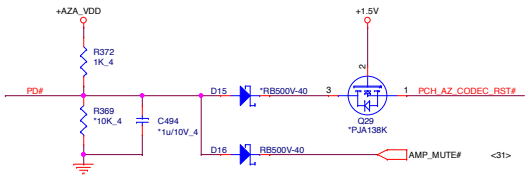


To small/B

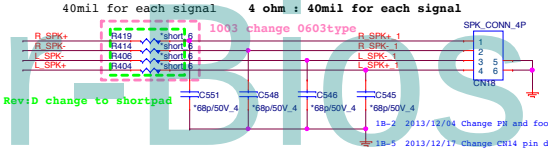
Codec PWR 5V(ADO)



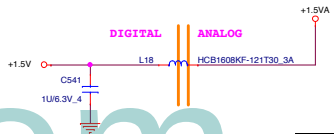
Mute(ADO)



Internal Speaker



Codec PWR 1.5V(ADO)



Quanta Computer Inc.
PROJECT : ZAA

Size	Document Number	Rev
	ALC255/HP/SPK	1A
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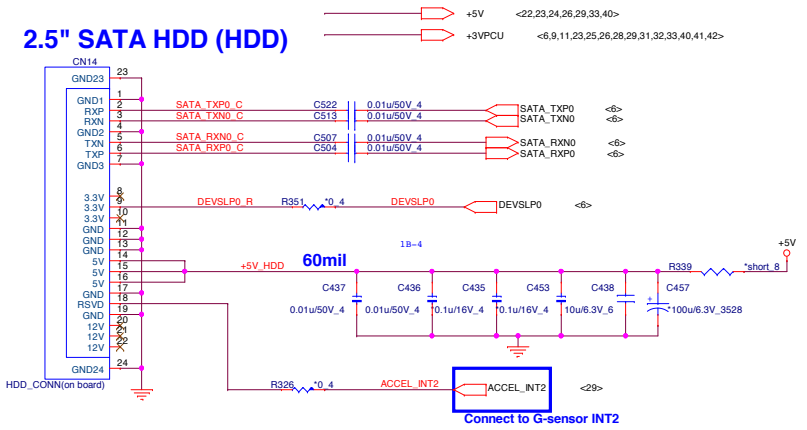
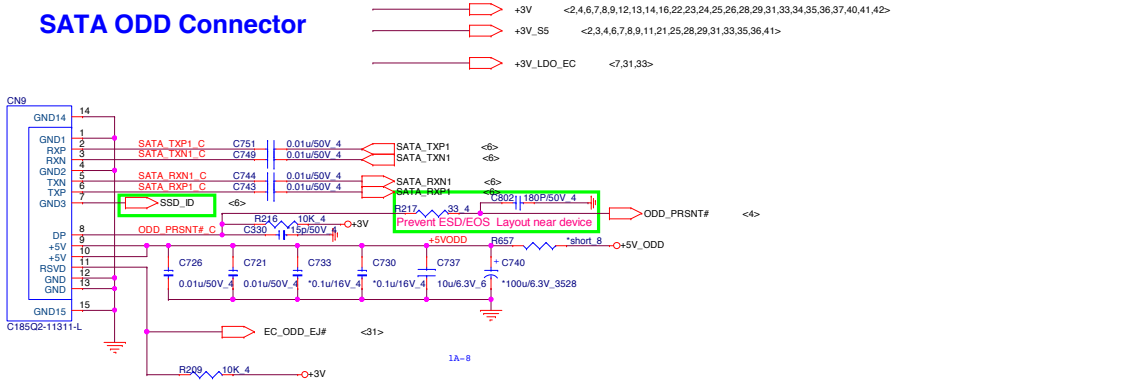
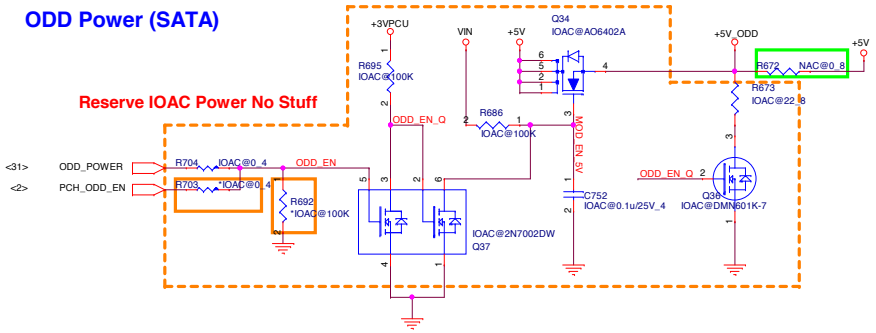
2.5" SATA HDD (HDD)



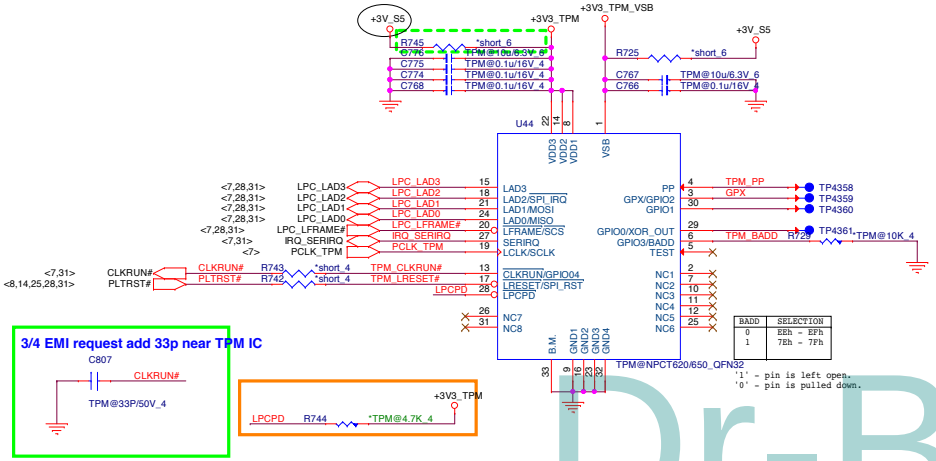
SATA ODD Connector



ODD Power (SATA)



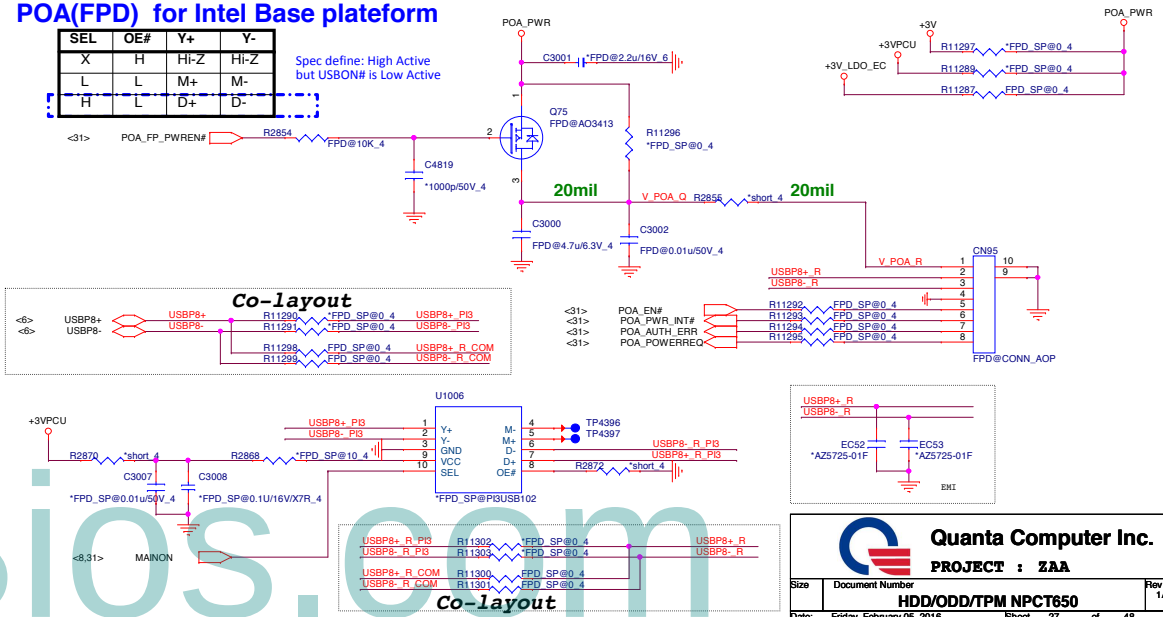
TPM NPCT650 (TPM)



POA(FPD) for Intel Base plateform

SEL	OE#	Y+	Y-
X	H	Hi-Z	Hi-Z
L	L	M+	M-
H	L	D+	D-

Spec define: High Active
but USBON# is Low Active



Quanta Computer Inc.
PROJECT : ZAA

Size	Document Number	Rev
	HDD/ODD/TPM NPCT650	1A

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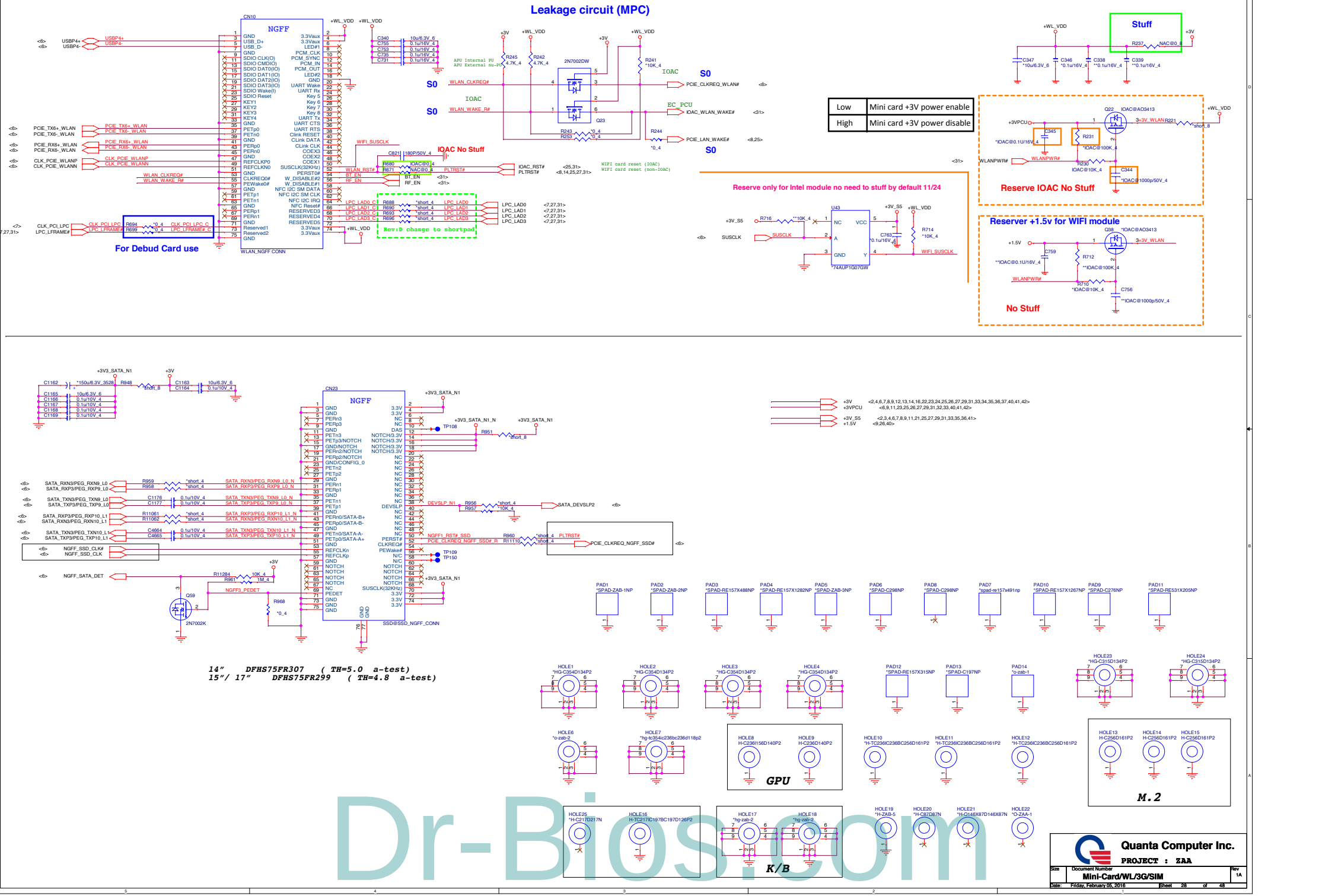
NGFF_M.2 WiFi & BT (NGF)



Quanta Computer Inc.	PROJECT : ZAA
Size	Document Number: Mini-Card/WL/3G/SIM
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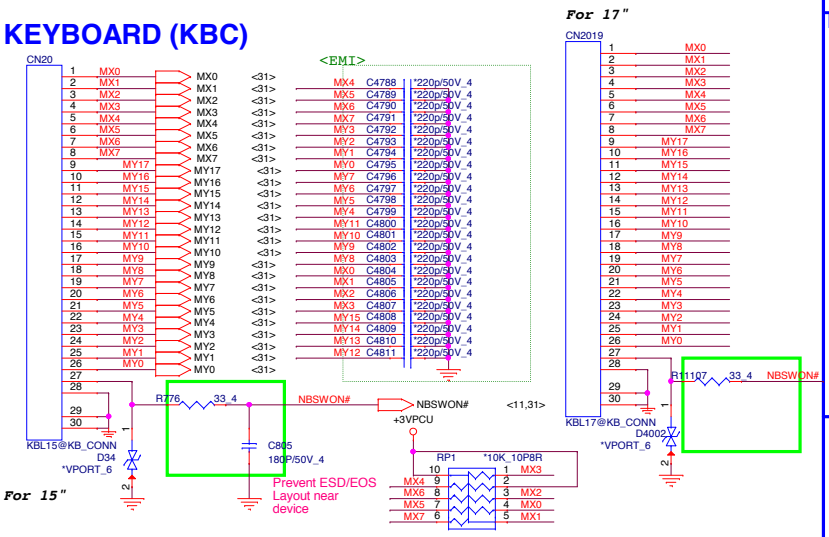
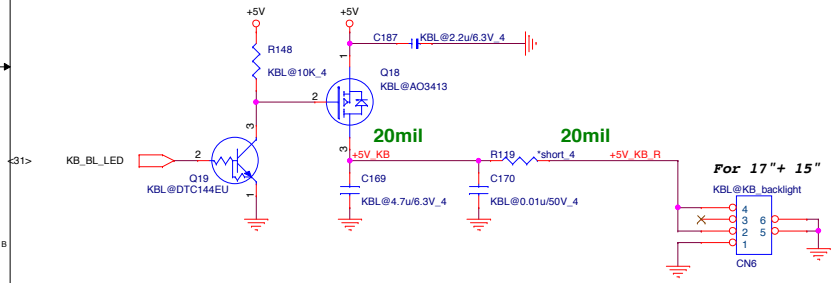
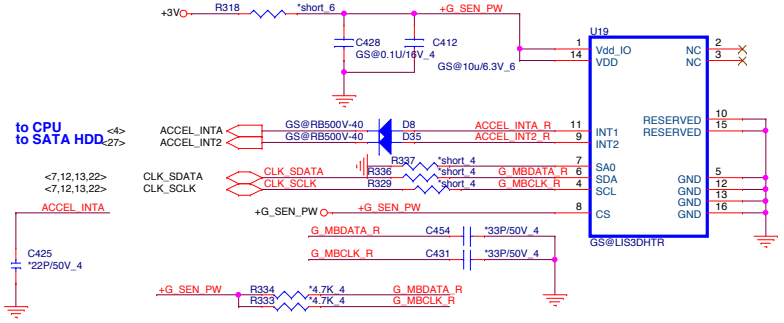
KEYBOARD (KBC)



KB_BL LED (KBC)



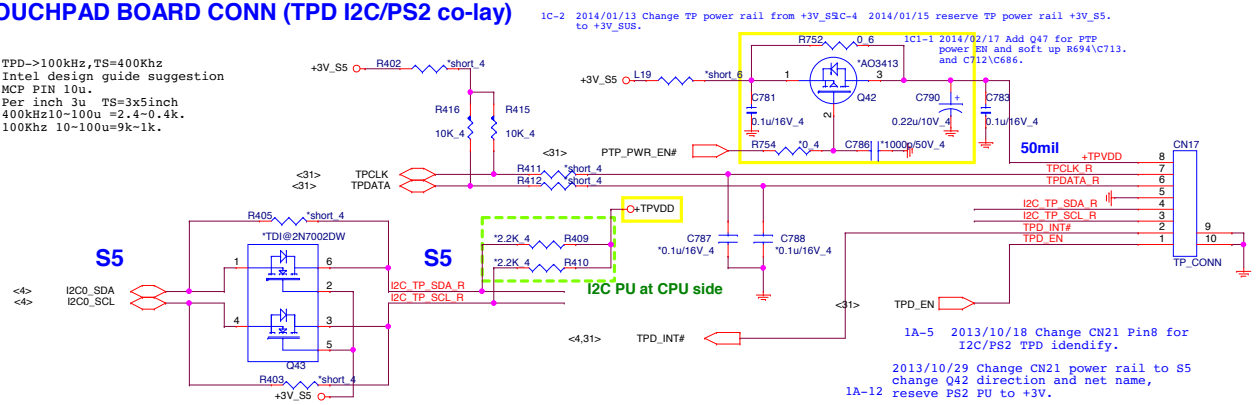
G-sensor(ACS)



TOUCHPAD BOARD CONN (TPD I2C/PS2 co-lay)

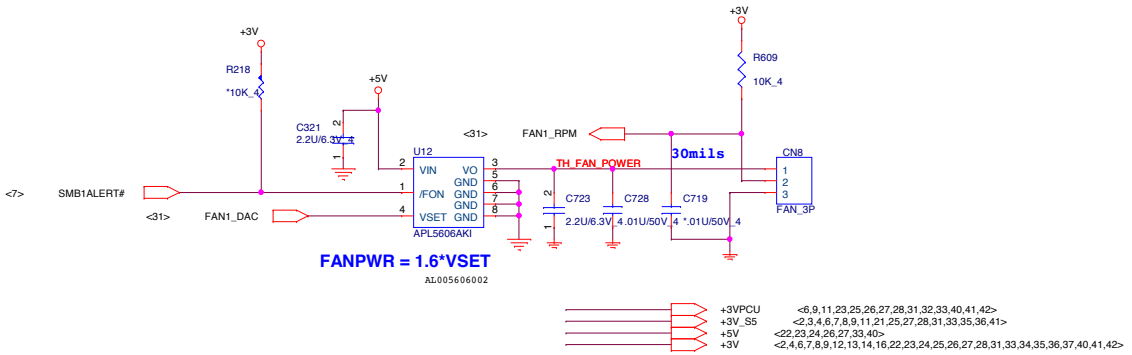
1C-2 2014/01/13 Change TP power rail from +3V_S5 to +3V_SUS.
1C-4 2014/01/15 reserve TP power rail +3V_S5.
1C1-1 2014/02/17 Add Q47 for PTP power EN and soft up R694\C713. and C712\C686.

TPD->100kHz,TS=400Khz
Intel design guide suggestion
MCP PIN 10u.
Per inch 3u TS=3x5inch
400kHz10~100u =2.4~0.4k.
100Khz 10~100u=9k~1k.



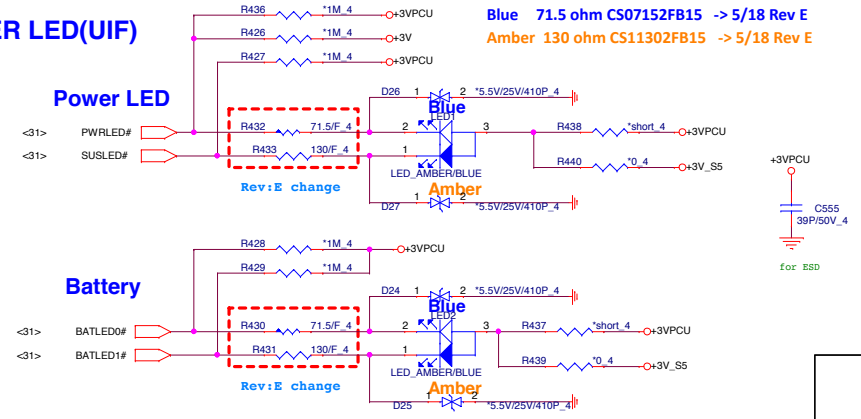
CPU FAN (THM)

Prevent ESD/EOS
Layout near
device



POWER LED(UIF)

Blue 71.5 ohm CS07152FB15 -> 5/18 Rev E
Amber 130 ohm CS11302FB15 -> 5/18 Rev E



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	KB/TP/FAN	1A

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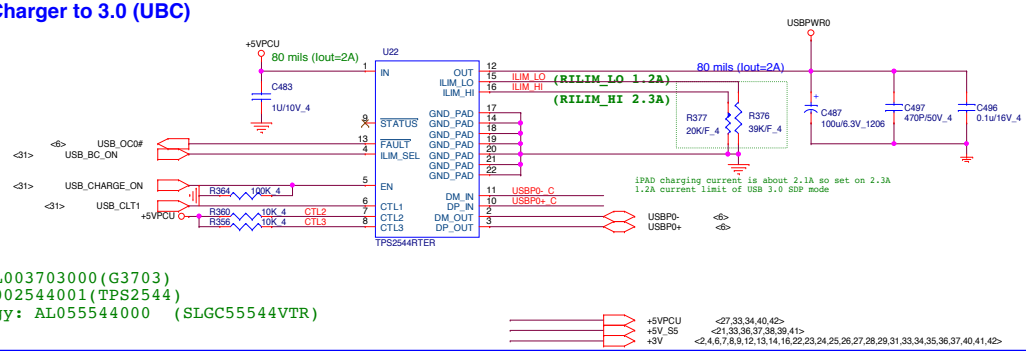
USB Charger to 3.0 (UBC)



	CTL1	CTL2	CTL3	ILIM_SEL
SDP	1	1	1	0
CDP	1	1	1	1
DCP	0	1	1	X

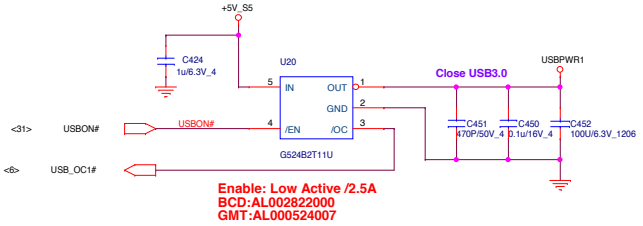
RILIM_LO is optional and the ILIM_LO pin may be left unconnected if the following conditions are met:
1. ILIM_SEL is always set high
2. Load Detection - Port Power Management is not used
3. Mouse / Keyboard wake function is not used
If conditions 1 and 2 are met but the mouse / keyboard wake function is also desired, it is recommended to use RILIM_LO < 80.6 kΩ.
The following equation programs the typical current limit:
(1)
RILIM_XX corresponds to either RILIM_HI or RILIM_LO as appropriate.

$$IOS\_typ(mA) = 50{,}250/\{RILIM\_XX(K\Omega)+0.1\}$$

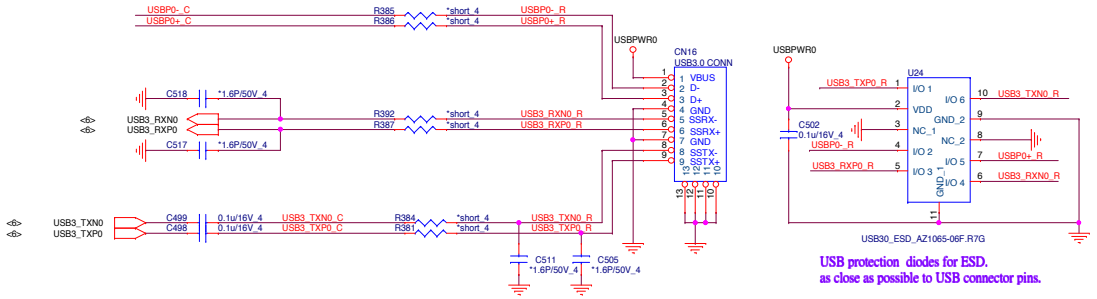
GMT:AL003703000(G3703)
TI:AL002544001(TPS2544)
Silergy: AL055544000 (SLGC55544VTR)

+5VPCU <27,33,34,40,42>
+5V_S5 <21,33,36,37,38,39,41>
+3V <2,4,6,7,8,9,12,13,14,16,22,23,24,25,26,27,28,29,31,33,34,35,36,37,40,41,42>

USB 3.0 Connector (UB3)

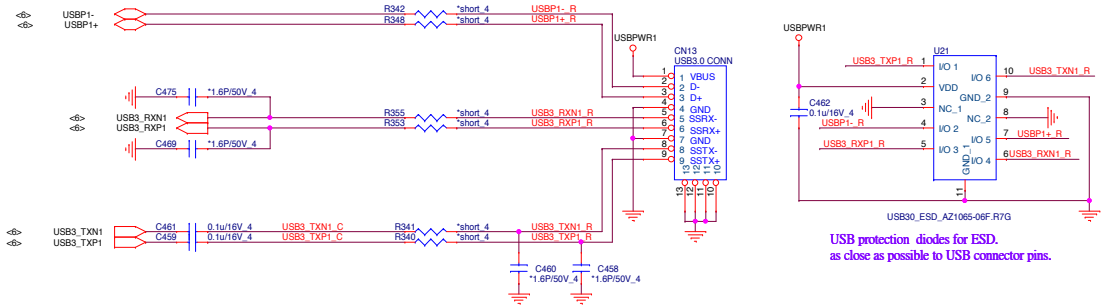


Enable: Low Active /2.5A
BCD:AL002822000
GMT:AL000524007



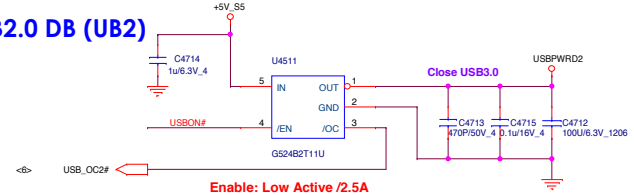
USB protection diodes for ESD.
as close as possible to USB connector pins.

USB3.0 conn, 2'nd : DFHS09FR679

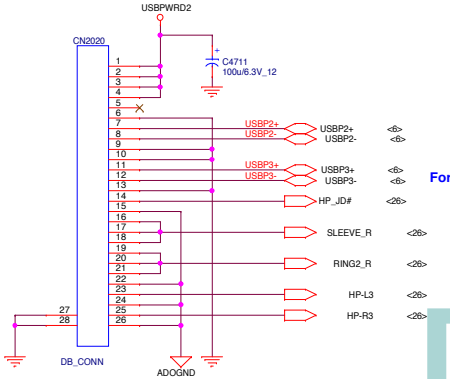


USB protection diodes for ESD.
as close as possible to USB connector pins.

USB2.0 DB (UB2)



Enable: Low Active /2.5A
BCD:AL002822000
GMT:AL000524007



For 17" DB use

Quanta Computer Inc.
PROJECT : ZAA

Size	Document Number	Rev
	USB3/Charger/USB2 DB	1A
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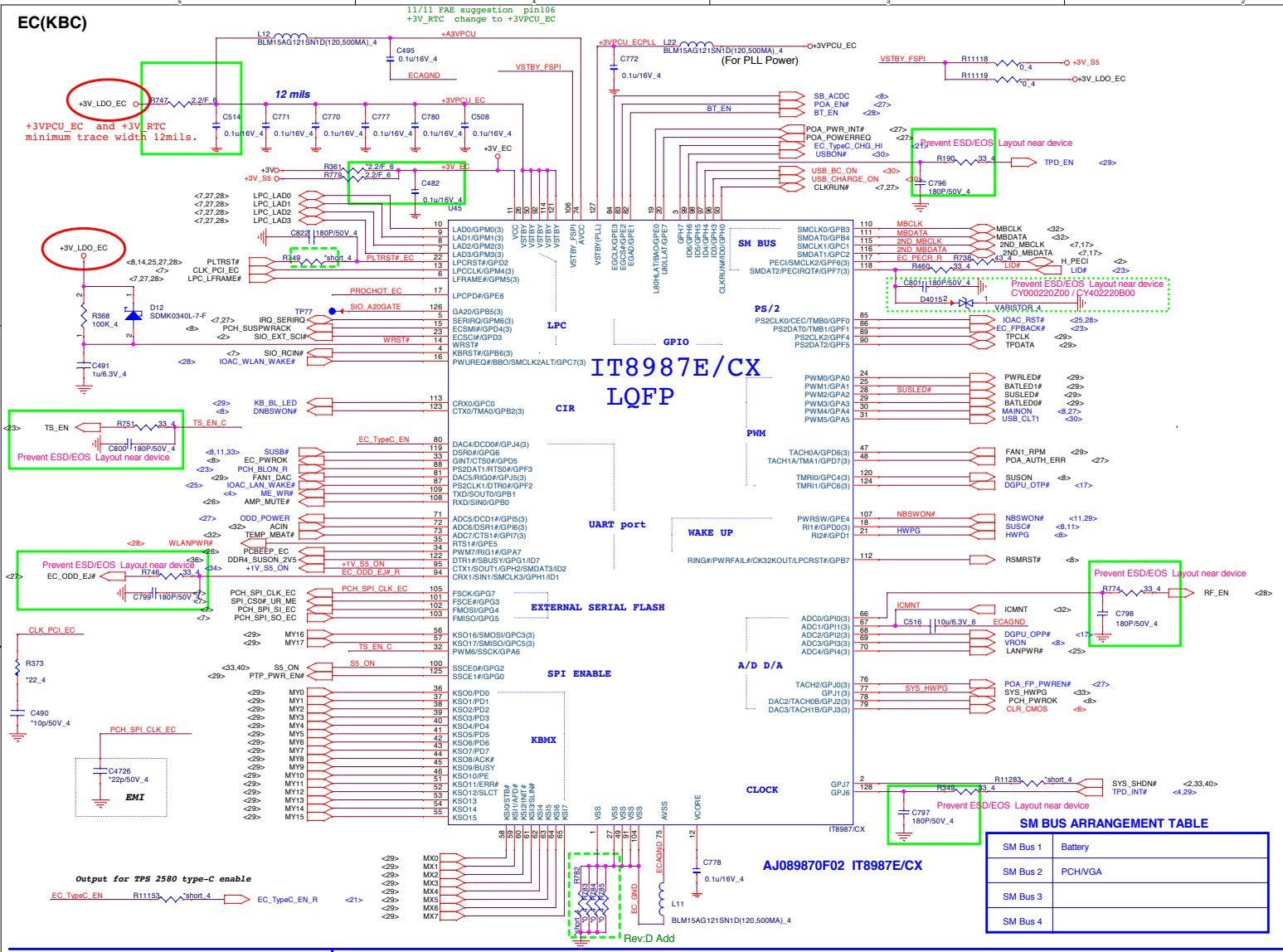
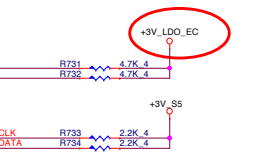
EC(KBC)

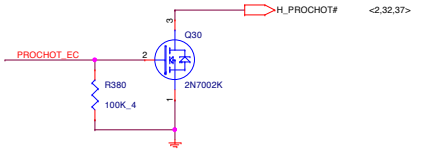


SM BUS ARRANGEMENT TABLE

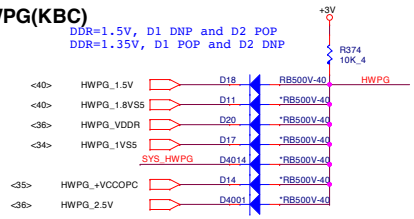
SM Bus 1	Battery
SM Bus 2	PCH/VGA
SM Bus 3	
SM Bus 4	

SM BUS PU(KBC)

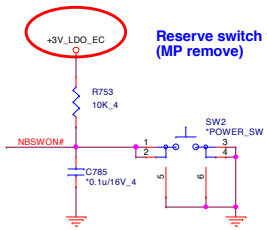




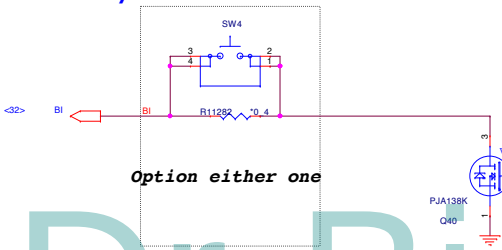
HWPG(KBC)



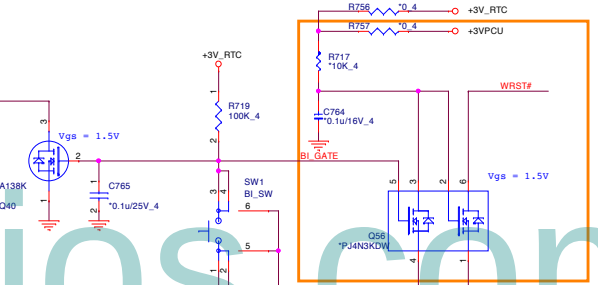
Reserve switch for test (MP remove)



Battery Detect Switch



Reset SW (FSW)



Reserve no stuff

Quanta Computer Inc.			
PROJECT : ZAA			
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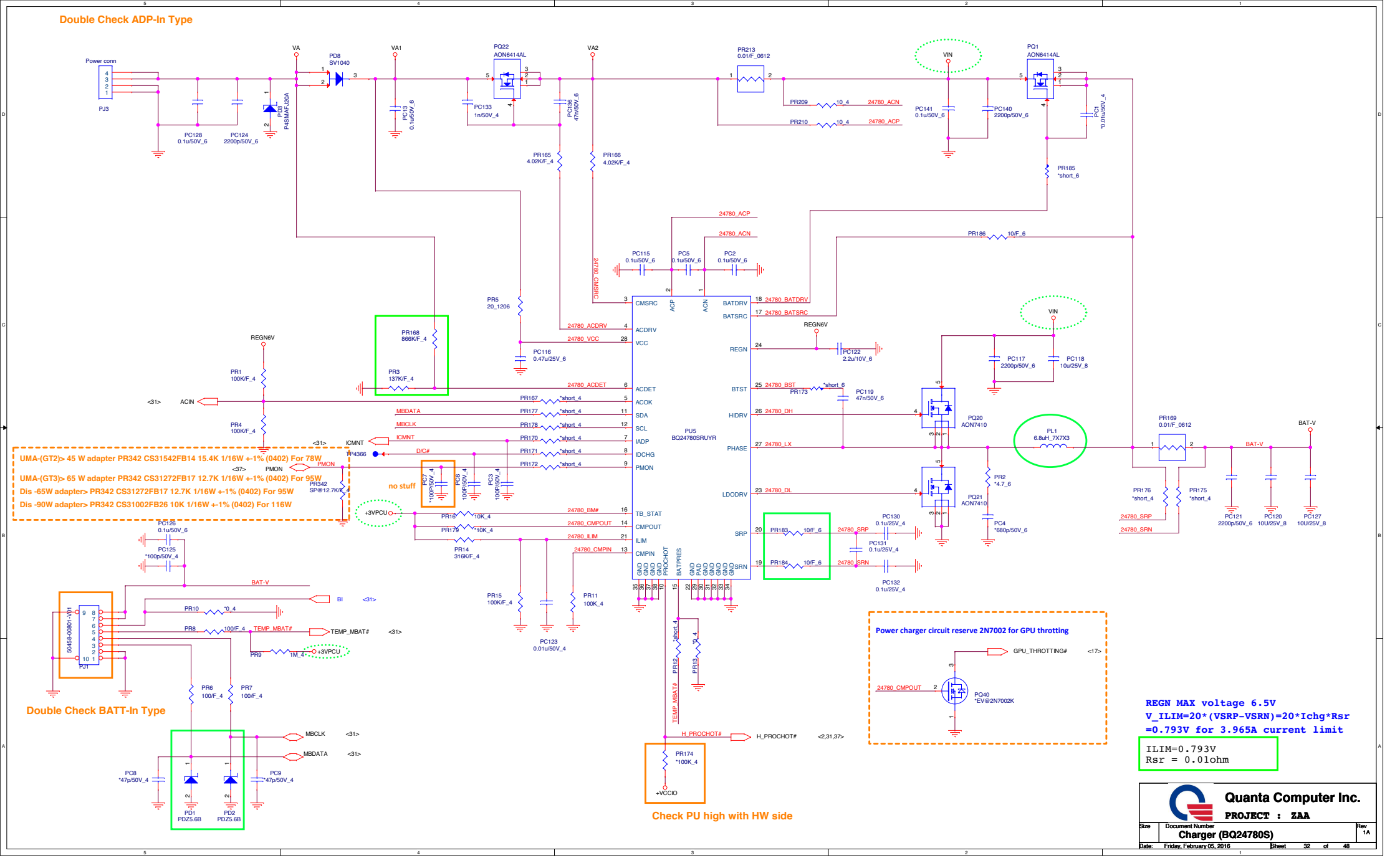
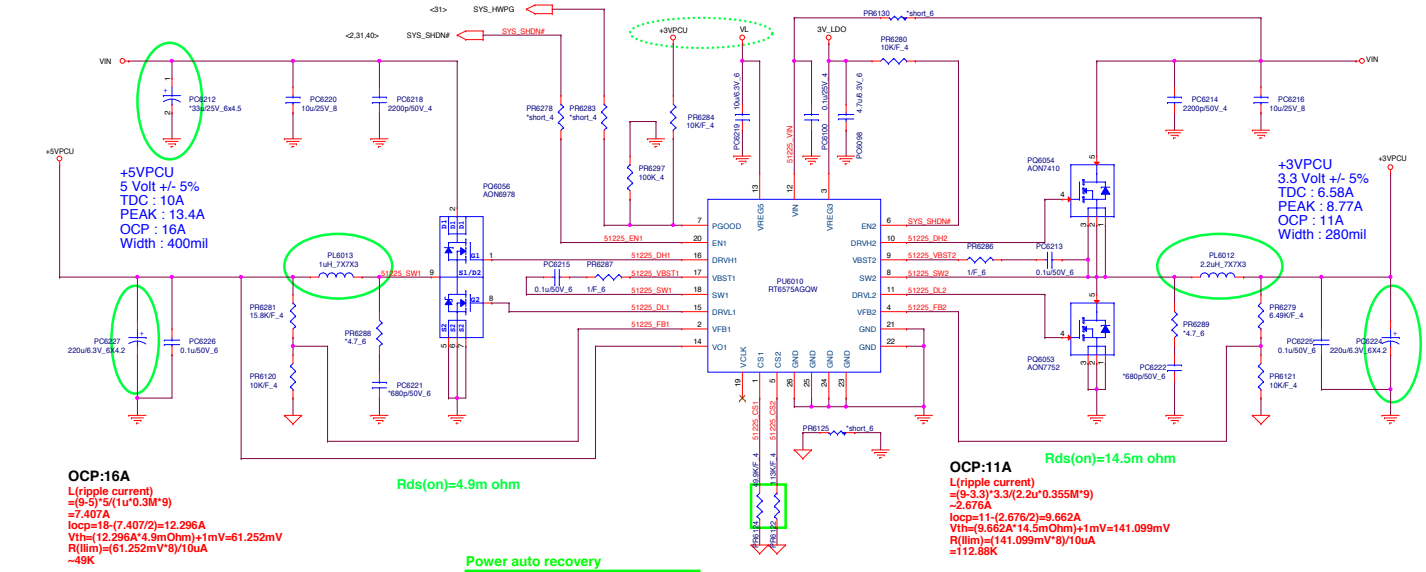

Double Check ADP-In Type
Power conn
PJ3
PD8
SV1040
PD3
P4SMAFL20A
PC128
0.1u/50V_6
PC124
2200p/50V_6
PC13
0.1u/50V_6
PQ22
AON6414AL
PC133
1n/50V_4
PC136
47n/50V_6
PR213
0.01/F_0612
PR209
10_4
24780_ACN
PR210
10_4
24780_ACP
PC141
0.1u/50V_6
PC140
2200p/50V_6
PQ1
AON6414AL
PC1
*0.01u/50V_4
PR185
*short_6
PR165
4.02K/F_4
PR166
4.02K/F_4
24780_CMSRC
PC115
0.1u/50V_6
PC5
0.1u/50V_6
PC2
0.1u/50V_6
PR186
10/F_6
PR5
20_1206
PC116
0.47u/25V_6
PR168
866K/F_4
PR3
137K/F_4
REGN6V
PR1
100K/F_4
PR4
100K/F_4
ACIN
ICMNT
TP4366
D/C#
PMON
PR342
SP@12.7K/F
PR167
PR177
PR178
PR170
PR171
PR172
*short_4
MBDATA
MBCLK
ICMNT
PC7
*100P/50V_4
PC6
100P/50V_4
PC3
100P/50V_4
no stuff
+3VPCU
PR16
10K_4
PR179
*10K_4
PR14
316K/F_4
PR15
100K/F_4
PC123
0.01u/50V_4
PR11
100K_4
PU5
BQ24780SRUYR
CMSRC
ACDRV
VCC
ACDET
ACOK
SDA
SCL
IADP
IDCHG
PMON
TB_STAT
CMPOUT
ILIM
CMPIN
PROCHOT
BATPRES
ACP
ACN
BATDRV
BATSRC
REGN
BTST
HIDRV
PHASE
LDODRV
SRP
SRN
24780_ACDRV
24780_VCC
24780_ACDET
24780_BM#
24780_CMPOUT
24780_ILIM
24780_CMPIN
24780_BATDRV
24780_BATSRC
24780_BST
24780_DH
24780_LX
24780_DL
24780_SRP
24780_SRN
PC122
2.2u/10_6
PR173
*short_6
PC119
47n/50V_6
PQ20
AON7410
PQ21
AON7410
PR2
*4.7_6
PC4
*680p/50V_6
PL1
6.8uH_7X7X3
PC130
0.1u/25V_4
PC131
0.1u/25V_4
PC132
0.1u/25V_4
PR183
10/F_6
PR184
10/F_6
PC117
2200p/50V_6
PC118
10u/25V_8
PR169
0.01/F_0612
PR176
*short_4
PR175
*short_4
PC121
2200p/50V_6
PC120
10U/25V_8
PC127
10U/25V_8
BAT-V
UMA-(GT2)> 45 W adapter PR342 CS31542FB14 15.4K 1/16W +-1% (0402) For 78W
UMA-(GT3)> 65 W adapter PR342 CS31272FB17 12.7K 1/16W +-1% (0402) For 95W
Dis -65W adapter> PR342 CS31272FB17 12.7K 1/16W +-1% (0402) For 95W
Dis -90W adapter> PR342 CS31002FB26 10K 1/16W +-1% (0402) For 116W
PC126
0.1u/50V_6
PC125
*100p/50V_4
BAT-V
BI
PR10
*0_4
PR8
100/F_4
TEMP_MBAT#
PR9
1M_4
+3VPCU
50458-00801-V01
PJ1
PR6
100/F_4
PR7
100/F_4
Double Check BATT-In Type
MBCLK
MBDATA
PC8
*47p/50V_4
PC9
*47p/50V_4
PD1
PDZ5.6B
PD2
PDZ5.6B
PR12
*short_4
PR13
0_4
H_PROCHOT#
PR174
*100K_4
+VCCIO
Check PU high with HW side
Power charger circuit reserve 2N7002 for GPU throtting
GPU_THROTTING#
PQ40
*EV@2N7002K
REGN MAX voltage 6.5V
V_ILIM=20*(VSRP-VSRN)=20*Ichg*Rsr
=0.793V for 3.965A current limit
ILIM=0.793V
Rsr = 0.01ohm
Quanta Computer Inc.
PROJECT : ZAA
Charger (BQ24780S)
Rev 1A
Date: Friday, February 05, 2016
Sheet 32 of 48



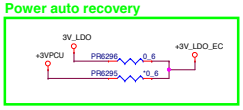
OCP:16A

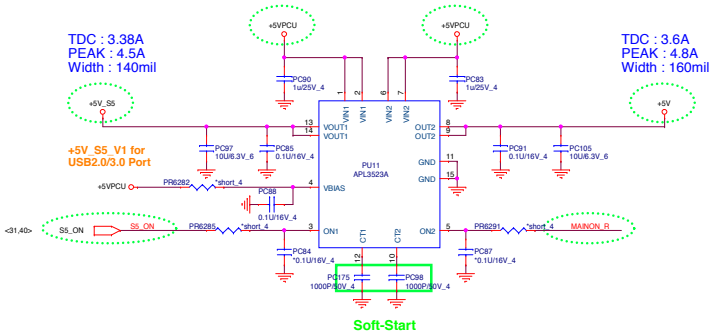
L(ripple current)
=(9-5)*5/(1u*0.3M*9)
=7.407A
Iocp=18-(7.407/2)=12.296A
Vth=(12.296A*4.9mOhm)+1mV=61.252mV
R(Ilim)=(61.252mV*8)/10uA
~49K

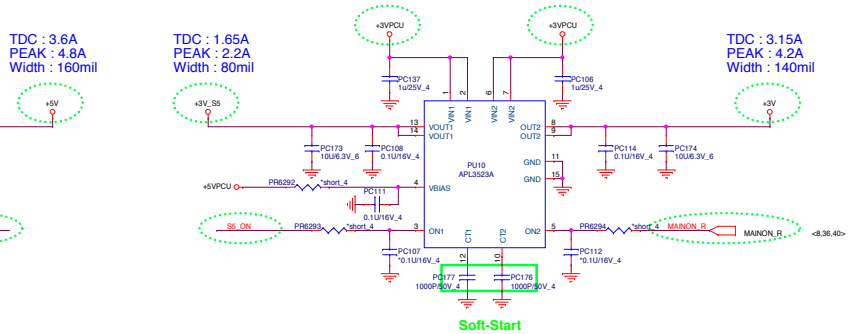
OCP:11A

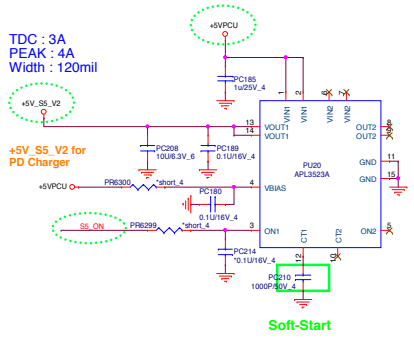
L(ripple current)
=(9-3.3)*3.3/(2.2u*0.355M*9)
~2.676A
Iocp=11-(2.676/2)=9.662A
Vth=(9.662A*14.5mOhm)+1mV=141.099mV
R(Ilim)=(141.099mV*8)/10uA
=112.88K

Power auto recovery

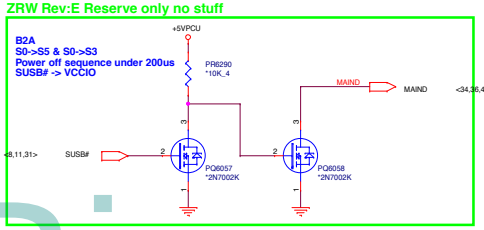




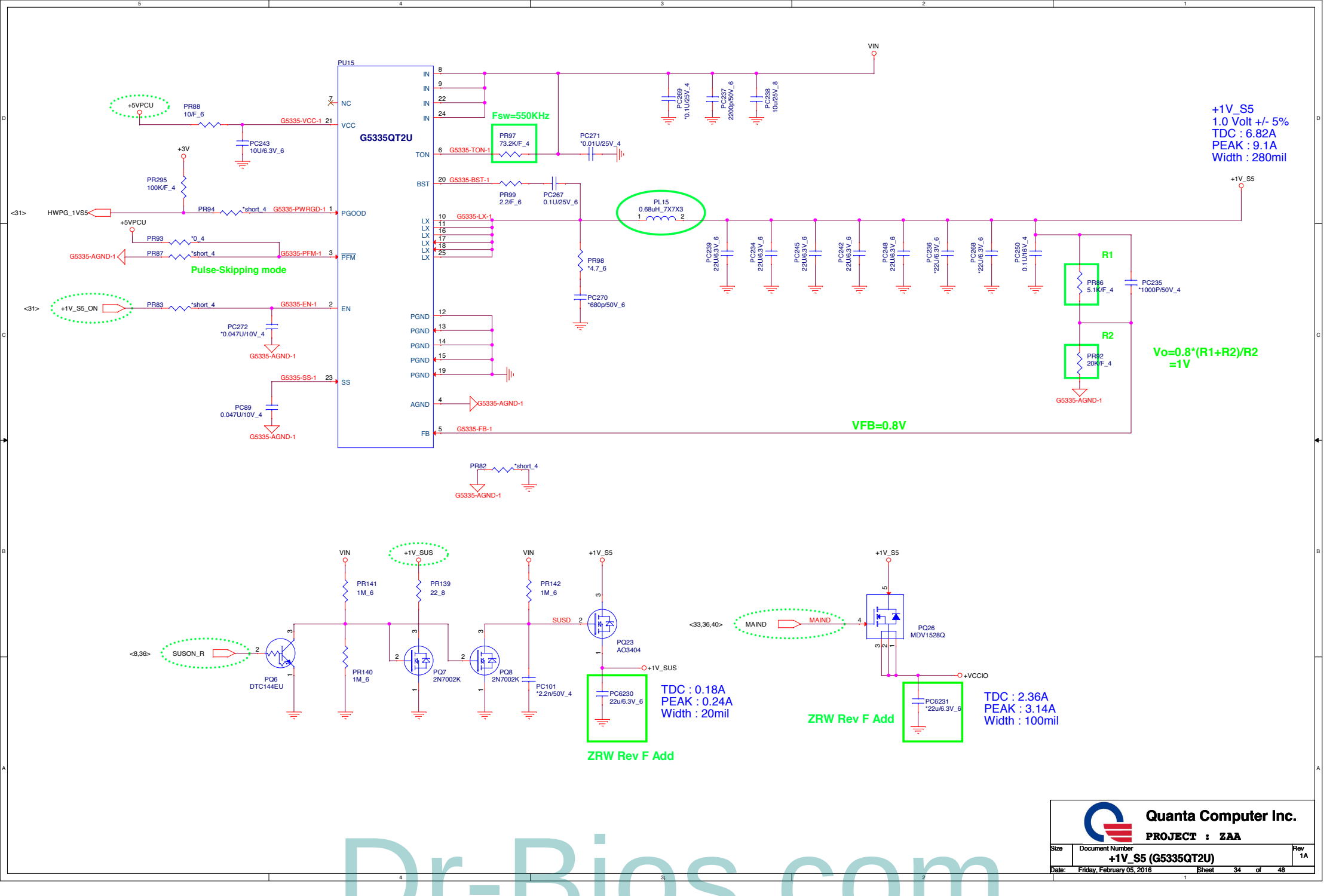




ZRW Rev:E Reserve only no stuff



Quanta Computer Inc.			
PROJECT : ZAA			
Size	Document Number		Rev
	SYSTEM 5V/3V (RT6575AGQW)		1A
Date: Friday, February 05, 2016		Sheet 33 of 48	

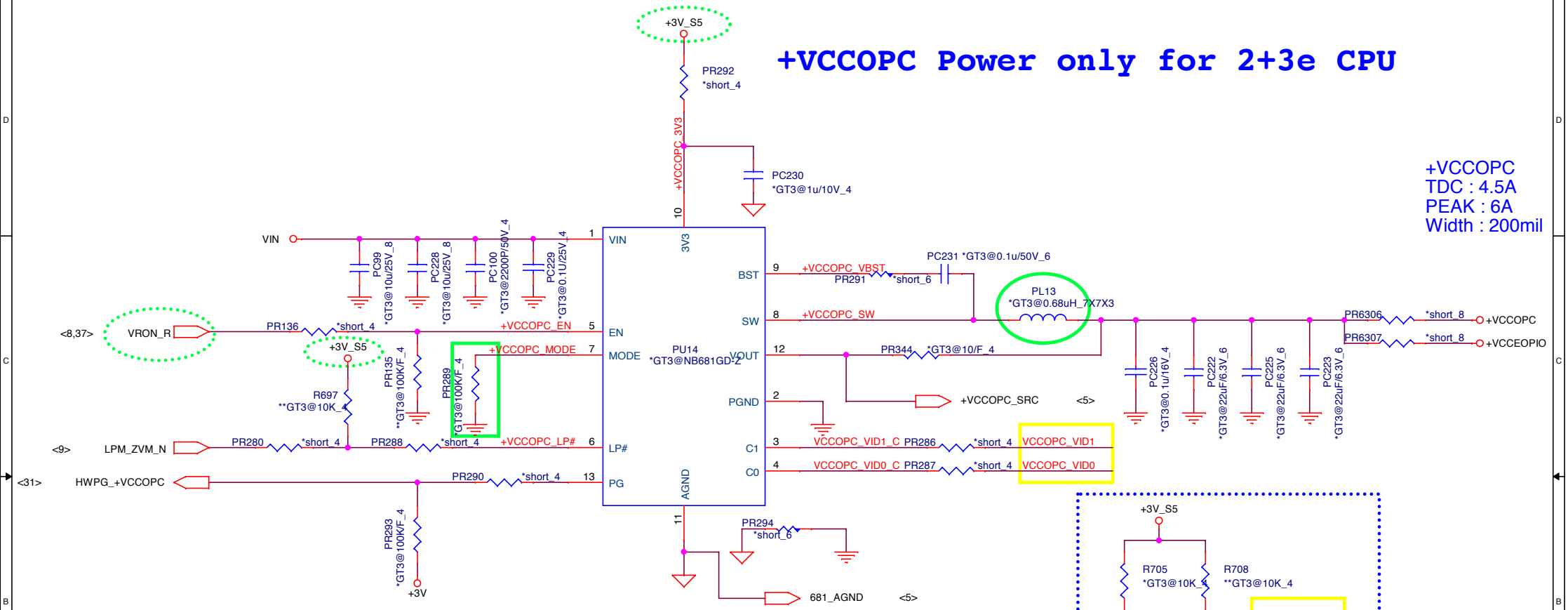


Quanta Computer Inc.

PROJECT : ZAA

Size	Document Number	Rev
	+1V_S5 (G5335QT2U)	1A
Date: Friday, February 05, 2016	Sheet 34 of 48	

+VCCOPC Power only for 2+3e CPU



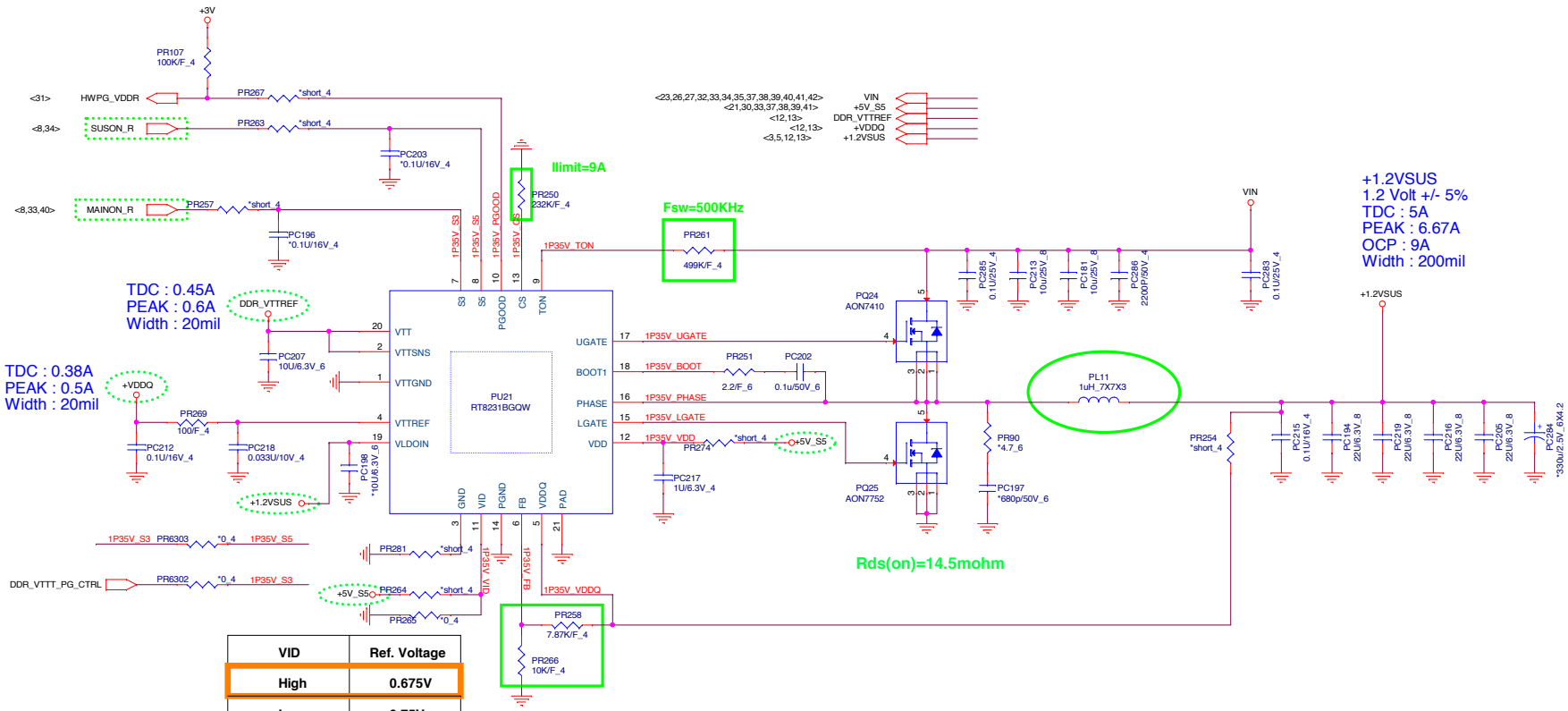
Mode	VR Rail
0 ohm	VCCIO
Floating	PRIMCORE
100K	EDRAM/EOPIO
150K	Other

	LP#	C1	C0	Vo
VCCEDRAM	0	X	X	0V
	1	0	0	0.8V(MSM)
	1	0	1	0.95V
	1	1	0	1.0V
	1	1	1	1.05V

<5> +VCCOPC
<23,26,27,32,33,34,36,37,38,39,40,41,42> VIN
<2,4,6,7,8,9,12,13,14,16,22,23,24,25,26,27,28,29,31,33,34,36,37,40,41,42> +3V
<2,3,4,6,7,8,9,11,21,25,27,28,29,31,33,36,41> +3V_S5

Quanta Computer Inc.
PROJECT : ZAA

Size	Document Number	Rev
	+VCCOPC (NB681GD-Z)	1A
Date: Friday, February 05, 2016	Sheet 35 of 48	

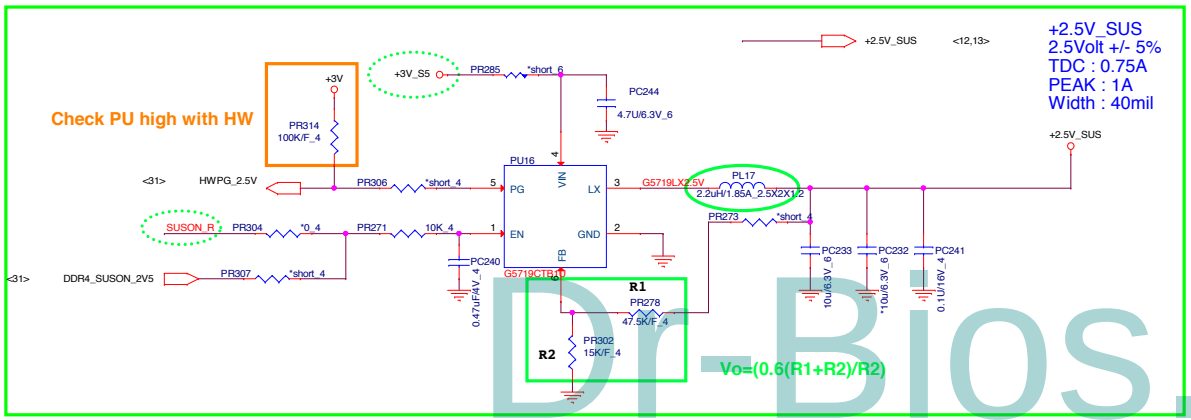


VID	Ref. Voltage
High	0.675V
Low	0.75V

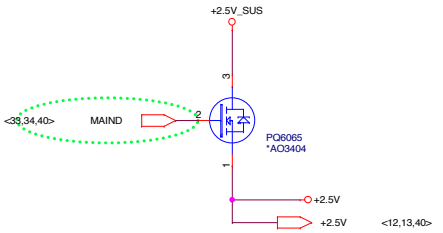
OCP=9A
L ripple current
=(19-1.2)*1.2/(1u*500k*19)
=2.248A
Vtrip=9-(2.248/2)*14.5mohm
=114.202mV
Rlimit=114.202mV/5uA*10=228.4Kohm

	S3	S5	VDDQ	VTTREF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

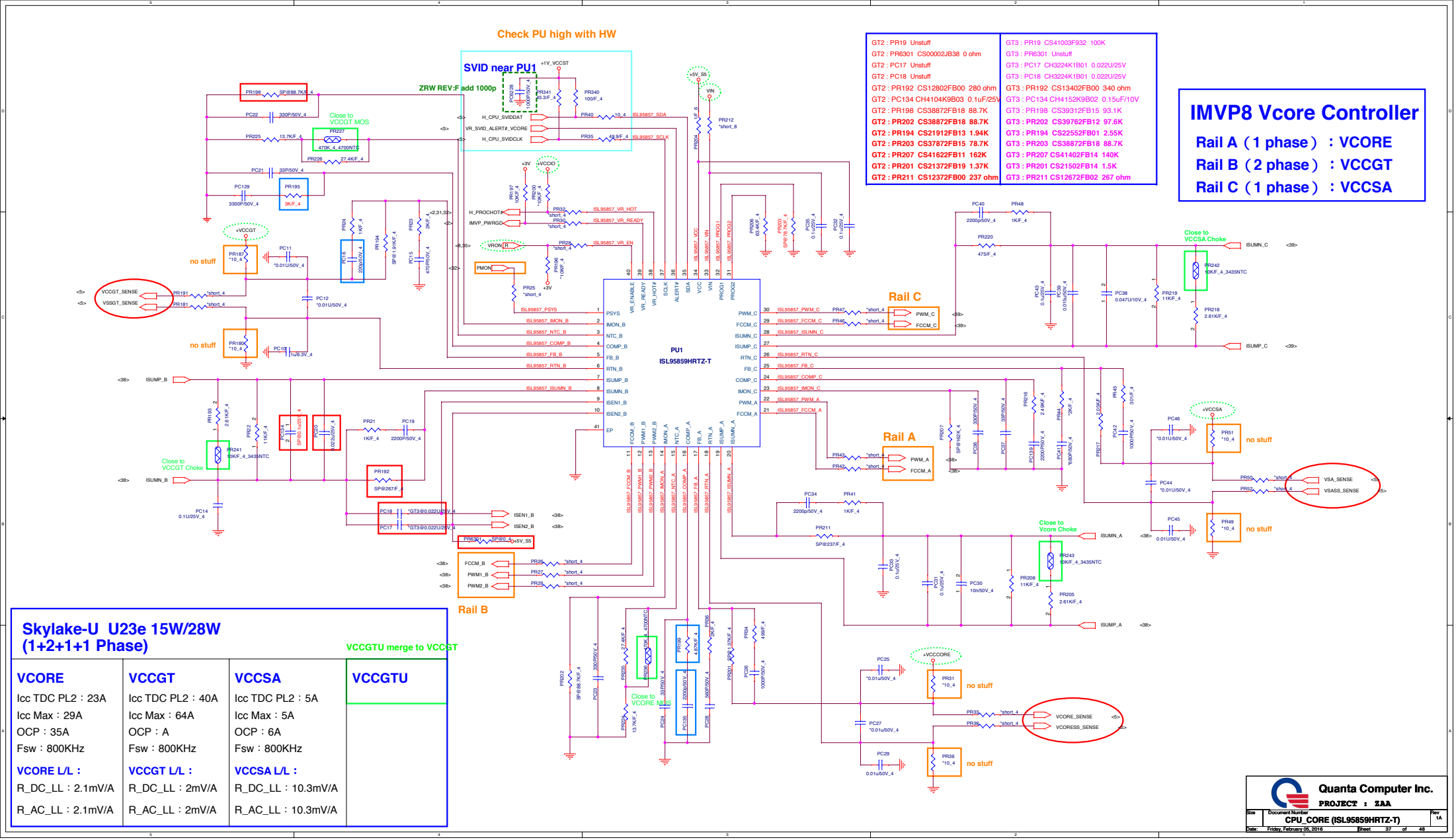
+2.5VSUS Power Rail For DDR4



10/26 Reserve +2.5V for DDR4 VDDSPD



Quanta Computer Inc.
PROJECT : ZAA
Size | Document Number: DDR4_+1.2VSUS (RT8231B) | Rev 1A
Date: Friday, February 05, 2016 | Sheet 36 of 48


Check PU high with HW
SVID near PU1
ZRW REV:F add 1000p
PU1
ISL95859HRTZ-T
Rail A
Rail B
Rail C
Close to VCCGT MOS
Close to VCCGT Choke
Close to VCCSA Choke
Close to Vcore Choke
Close to VCORE MOS
no stuff
VCCGTU merge to VCCGT
GT2 : PR19 Unstuff
GT2 : PR6301 CS00002JB38 0 ohm
GT2 : PC17 Unstuff
GT2 : PC18 Unstuff
GT2 : PR192 CS12802FB00 280 ohm
GT2 : PC134 CH4104K9B03 0.1uF/25V
GT2 : PR198 CS38872FB18 88.7K
GT2 : PR202 CS38872FB18 88.7K
GT2 : PR194 CS21912FB13 1.94K
GT2 : PR203 CS37872FB15 78.7K
GT2 : PR207 CS41622FB11 162K
GT2 : PR201 CS21372FB19 1.37K
GT2 : PR211 CS12372FB00 237 ohm
GT3 : PR19 CS41003F932 100K
GT3 : PR6301 Unstuff
GT3 : PC17 CH3224K1B01 0.022U/25V
GT3 : PC18 CH3224K1B01 0.022U/25V
GT3 : PR192 CS13402FB00 340 ohm
GT3 : PC134 CH4152K9B02 0.15uF/10V
GT3 : PR198 CS39312FB15 93.1K
GT3 : PR202 CS39762FB12 97.6K
GT3 : PR194 CS22552FB01 2.55K
GT3 : PR203 CS38872FB18 88.7K
GT3 : PR207 CS41402FB14 140K
GT3 : PR201 CS21502FB14 1.5K
GT3 : PR211 CS12672FB02 267 ohm
IMVP8 Vcore Controller
Rail A (1 phase) : VCORE
Rail B (2 phase) : VCCGT
Rail C (1 phase) : VCCSA
Skylake-U U23e 15W/28W
(1+2+1+1 Phase)
VCORE
Icc TDC PL2 : 23A
Icc Max : 29A
OCP : 35A
Fsw : 800KHz
VCORE L/L :
R_DC_LL : 2.1mV/A
R_AC_LL : 2.1mV/A
VCCGT
Icc TDC PL2 : 40A
Icc Max : 64A
OCP : A
Fsw : 800KHz
VCCGT L/L :
R_DC_LL : 2mV/A
R_AC_LL : 2mV/A
VCCSA
Icc TDC PL2 : 5A
Icc Max : 5A
OCP : 6A
Fsw : 800KHz
VCCSA L/L :
R_DC_LL : 10.3mV/A
R_AC_LL : 10.3mV/A
VCCGTU
Quanta Computer Inc.
PROJECT : ZAA
CPU_CORE (ISL95859HRTZ-T)
Friday, February 05, 2016
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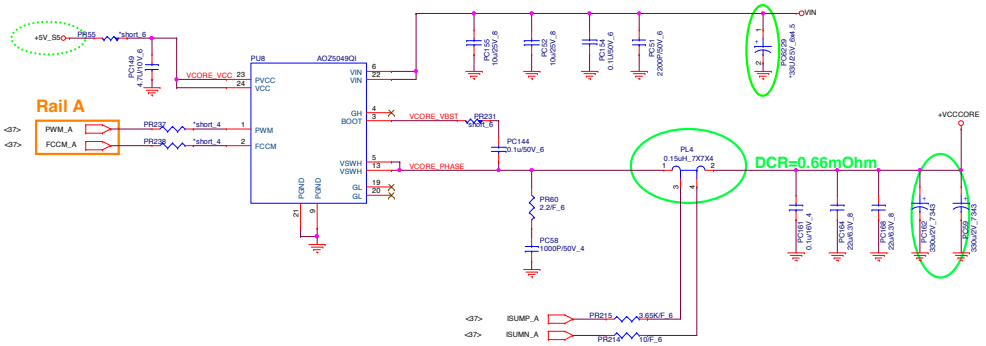
GT2 : PR19 Unstuff	GT3 : PR19 CS41003F932 100K

VCORE



VCORE

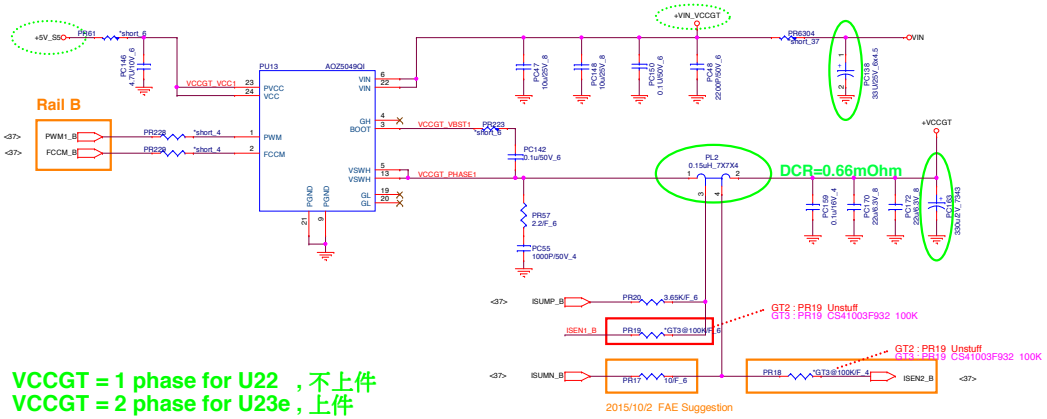
Icc TDC PL2 : 23A
Icc Max : 29A
OCP : 35A
Fsw : 800KHz

VCORE L/L :

R_DC_LL : 2.1mV/A

R_AC_LL : 2.1mV/A

VCCGT



VCCGT

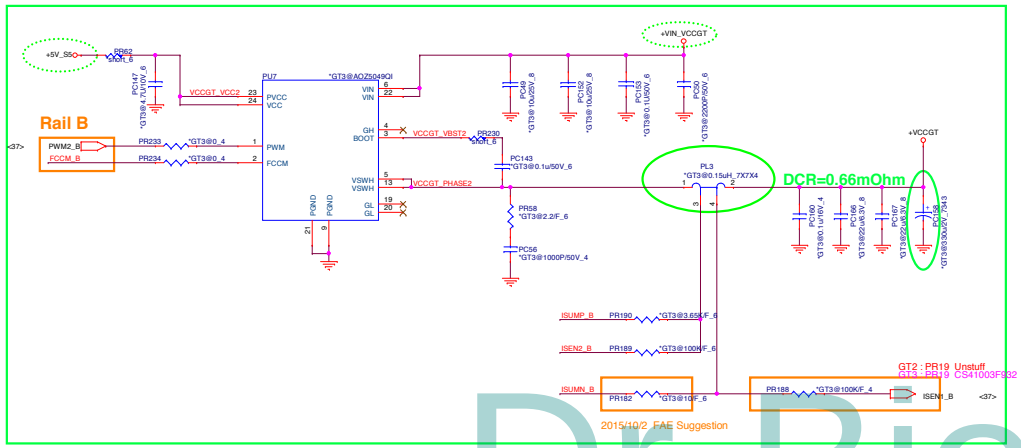
Icc TDC PL2 : 40A
Icc Max : 64A
OCP : A
Fsw : 800KHz

VCCGT L/L :

R_DC_LL : 2mV/A

R_AC_LL : 2mV/A

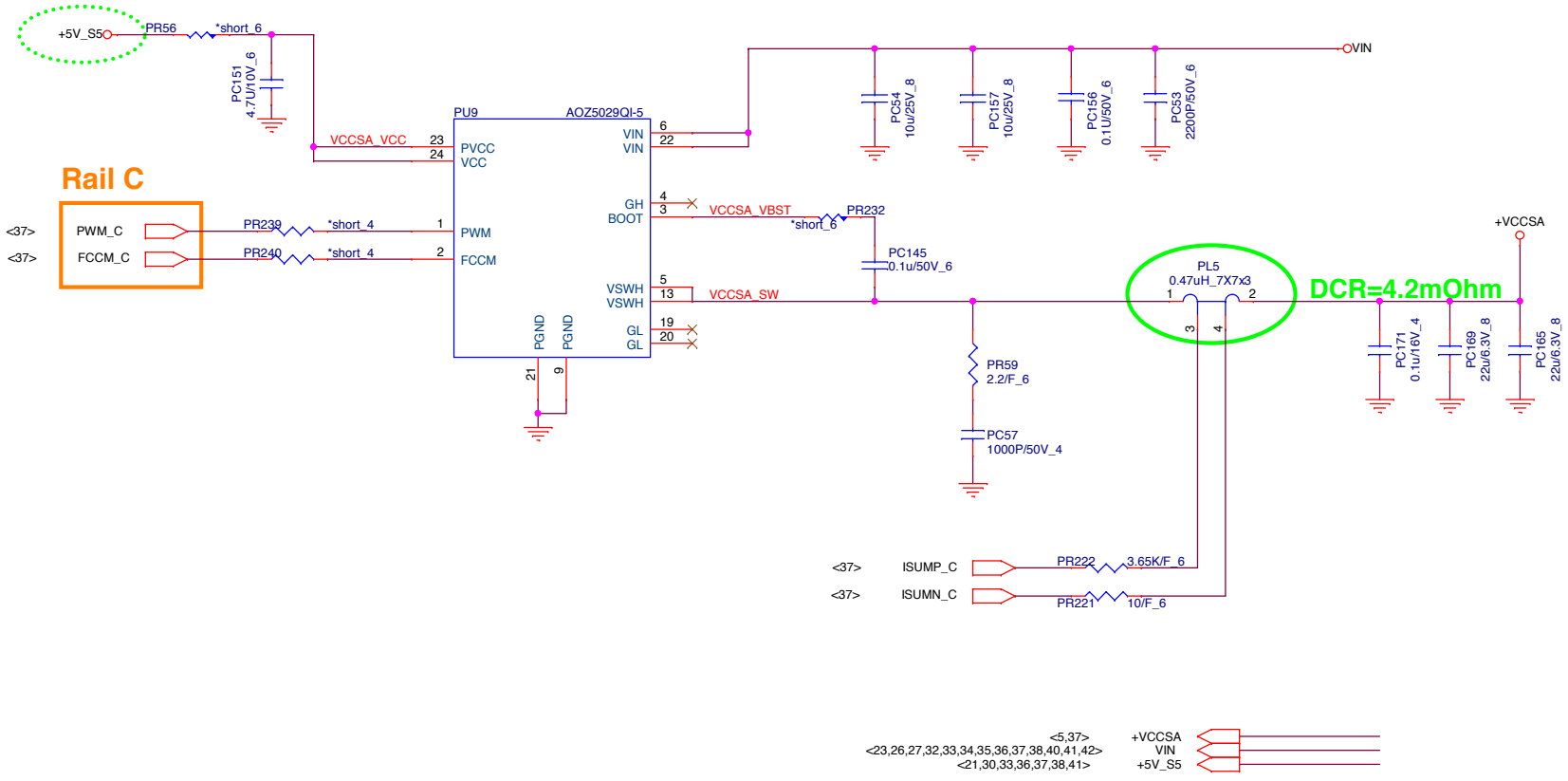
VCCGT = 1 phase for U22 ，不上件
VCCGT = 2 phase for U23e , 上件



<5,37>	+VCCCORE	
<23,26,27,32,33,34,35,36,37,39,40,41,42>	VIN	
<5,37>	+VCCGT	
<21,30,33,36,37,39,41>	+5V_S5	

Quanta Computer Inc.
PROJECT : ZAA
Size: Document Number: VCORE/VCCGT (ISL95808HRZ-T) Rev: 1A
Date: Friday, February 05, 2016 Sheet 38 of 48

VCCSA



VCCSA

Icc TDC PL2：5A

Icc Max：5A

OCP：6A

Fsw：800KHz

VCCSA L/L：

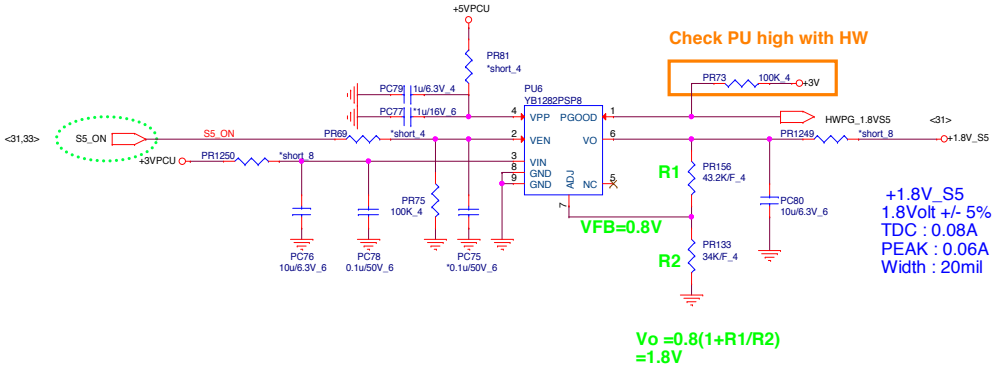
R_DC_LL：10.3mV/A

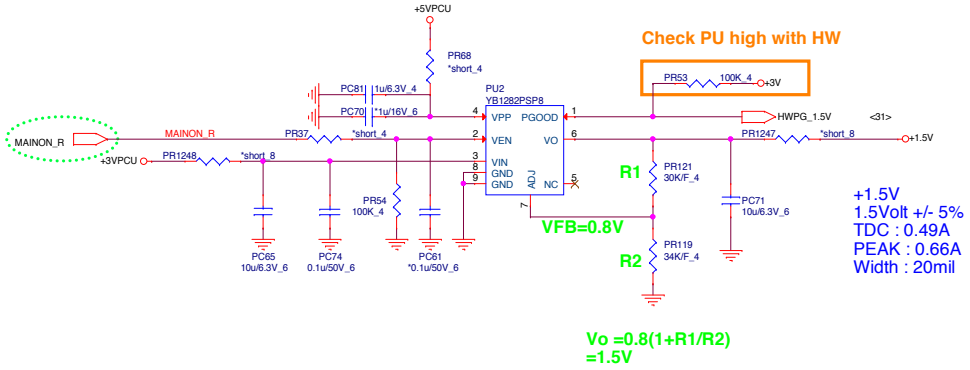
R_AC_LL：10.3mV/A

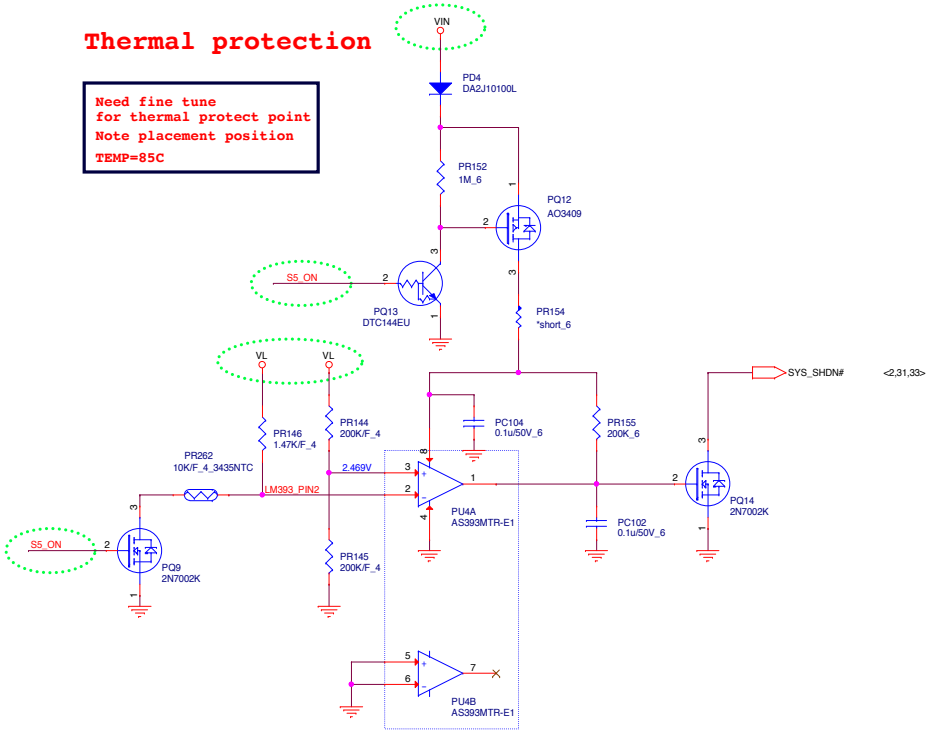
Quanta Computer Inc.

PROJECT : ZAA

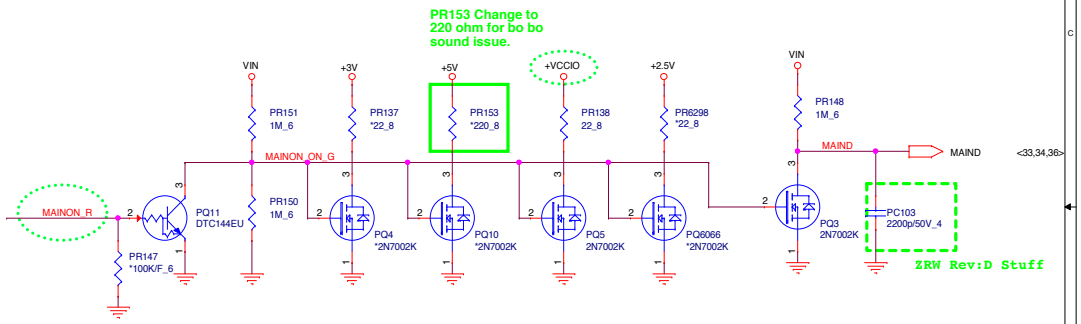
Size	Document Number	Rev
	VCCSA (ISL95808HRZ-T)	1A
Date: Friday, February 05, 2016	Sheet 39 of 48	







For EC control thermal protection (output 3.3V)

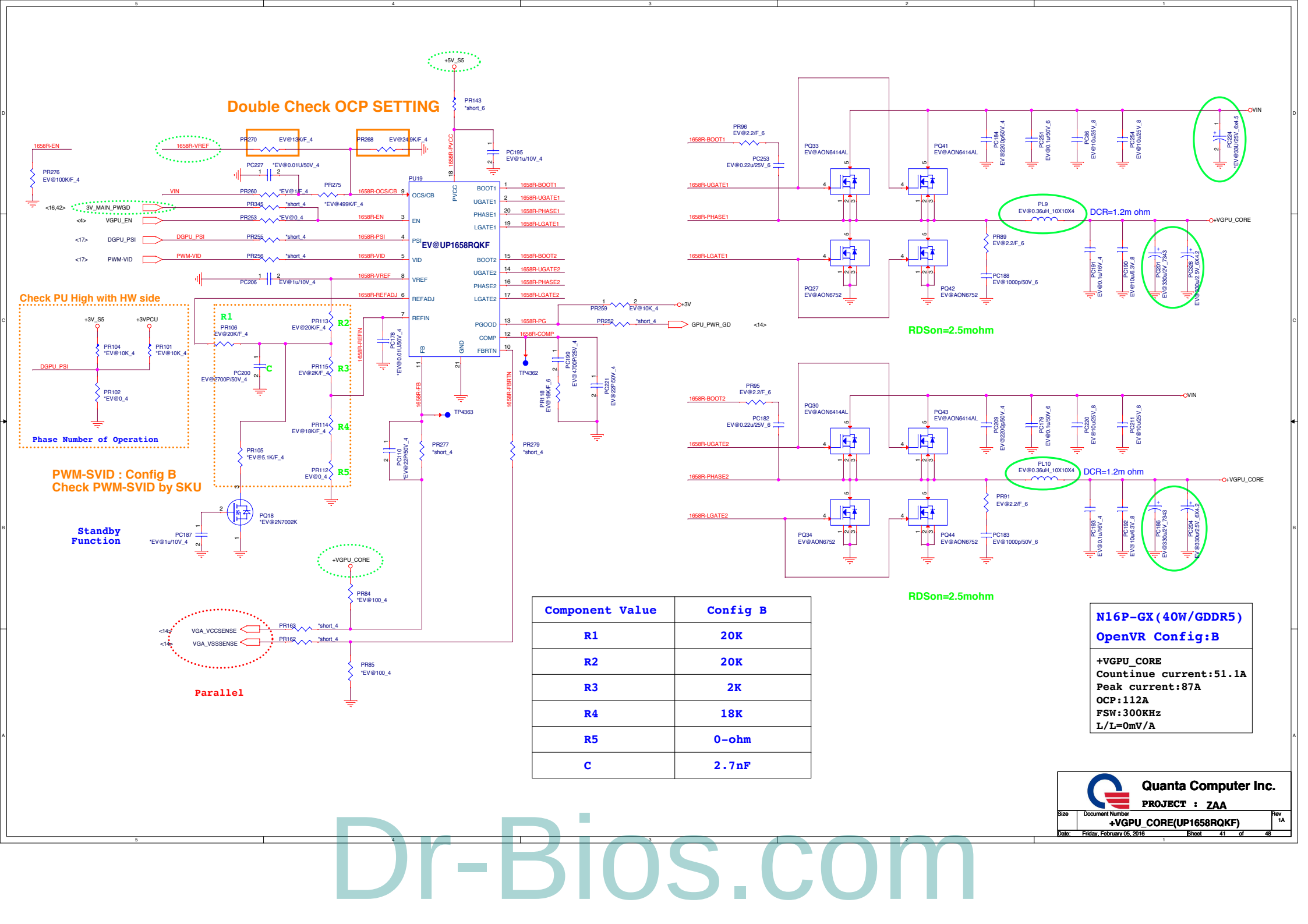


Quanta Computer Inc.

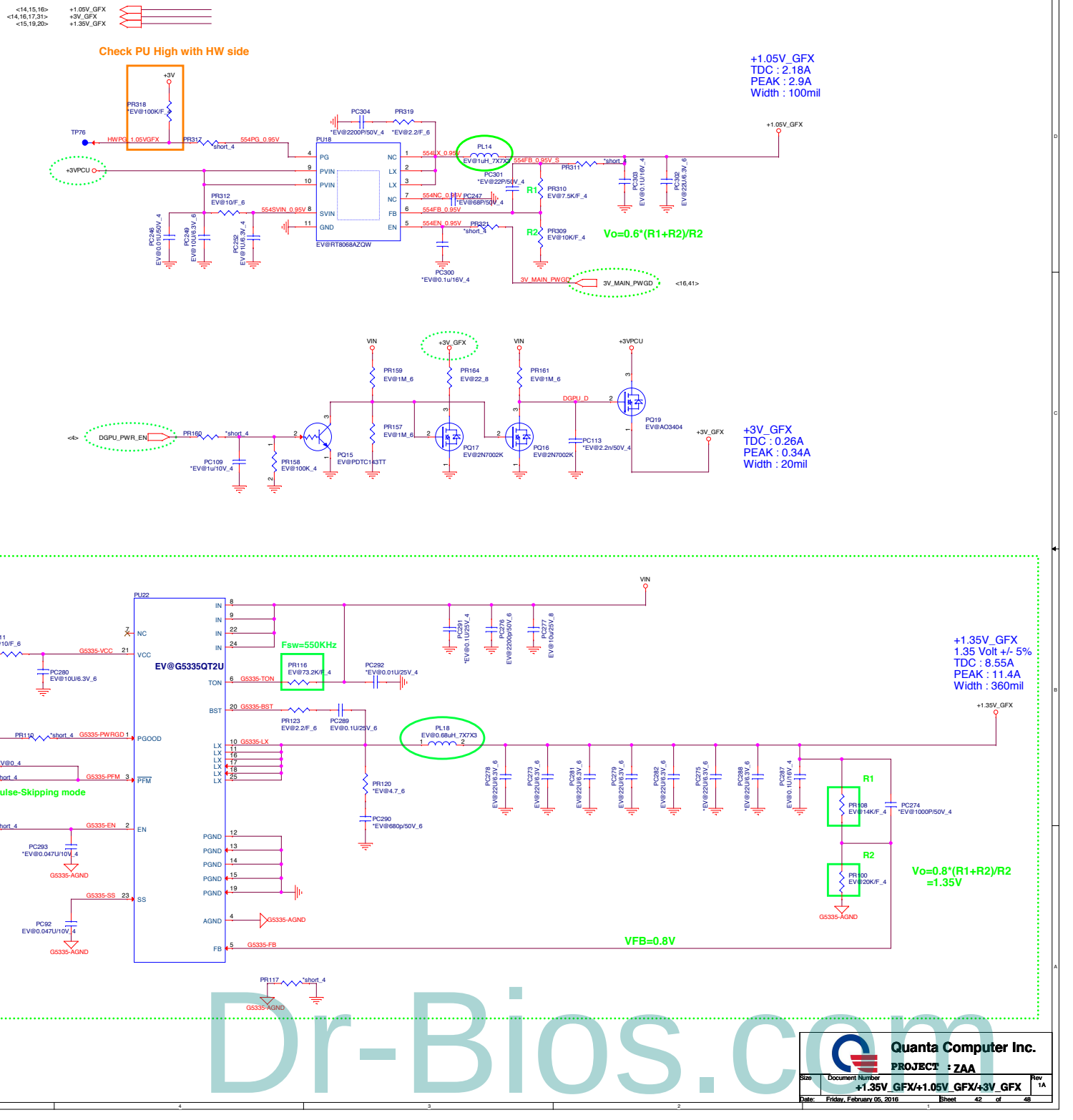
PROJECT : ZAA

Size	Document Number	Rev
	+1.8V/+1.5V/Thermal Protect	1A

Date: Friday, February 05, 2016 Sheet 40 of 48



Component Value	Config B
R1	20K
R2	20K
R3	2K
R4	18K
R5	0-ohm
C	2.7nF


Check PU High with HW side
+1.05V_GFX
TDC : 2.18A
PEAK : 2.9A
Width : 100mil
Vo=0.6*(R1+R2)/R2
+3V_GFX
TDC : 0.26A
PEAK : 0.34A
Width : 20mil
+1.35V_GFX for GDDR5
Fsw=550KHz
Pulse-Skipping mode
EV@G5335QT2U
+1.35V_GFX
1.35 Volt +/- 5%
TDC : 8.55A
PEAK : 11.4A
Width : 360mil
Vo=0.8*(R1+R2)/R2
=1.35V
VFB=0.8V
Quanta Computer Inc.
PROJECT : ZAA
+1.35V_GFX/+1.05V_GFX/+3V_GFX
Date: Friday, February 05, 2016
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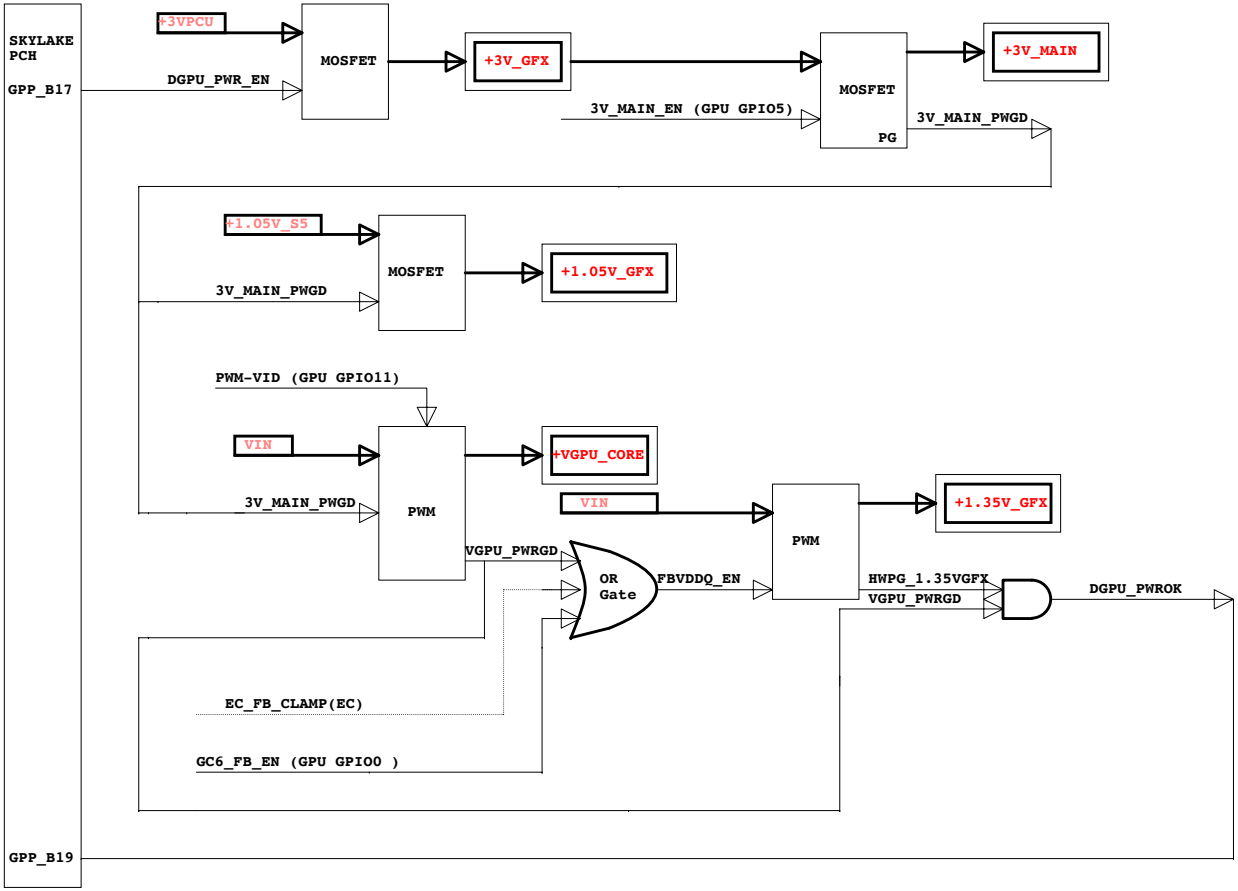
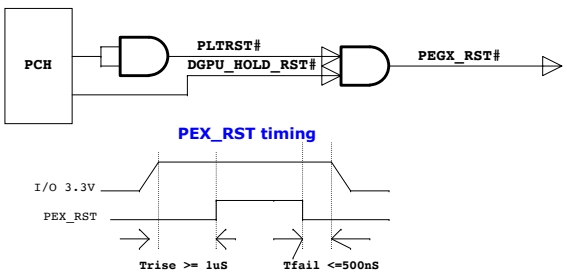
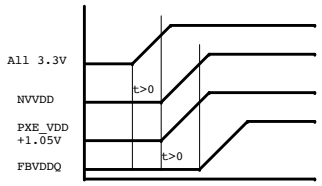
VGA power up sequence



Power plane	Description	Voltage	S0	S3	S5
+VCCCORE	Core voltage for CPU	0.55~1.5	ON	OFF	OFF
+VCCGT	Voltage for on-Die VGA of CPU	0.55~1.5	ON	OFF	OFF
+VCCGTX	Voltage for on-Die VGA of CPU	0.55~1.5	ON	OFF	OFF
+VDDQ_VTT	0.6V switched power rail for DDR4 terminator	0.6	ON	ON	OFF
+VDDQ	0.6V switched power rail for DDR4	0.6	ON	ON	OFF
+VCCSA	Voltage for system agent of CPU	0.55~1.15	ON	OFF	OFF
+1.2VSUS	1.2V switched power rail for DDR4	1.2	ON	ON	OFF
+1V_S5	1V switched power rail	1	ON	ON	ON
+1V_SUS	1V switched power rail	1	ON	ON	OFF
+VCCIO	Voltage for I/O of CPU	1	ON	OFF	OFF
+VCCOPC	Voltage for on package cache of CPU	1	ON	OFF	OFF
+2.5V_SUS	2.5V switched power rail for DDR4	2.5	ON	ON	OFF
+1.8V_S5	1.8V switched power rail	1.8	ON	ON	ON
+1.5V	1.5V switched power rail	1.5	ON	OFF	OFF
+3V_S5	3.3V switched power rail	3.3	ON	ON	ON
+3VPCU	3.3V always on power rail	3.3	ON	ON	ON
+3V	3.3V switched power rail	3.3	ON	OFF	OFF
+5VPCU	5V always on power rail	5	ON	ON	ON
+5V_S5	5V switched power rail for system	5	ON	ON	ON
+5V	5V switched power rail	5	ON	OFF	OFF
VIN	Adaptor power supply	19	ON	ON	ON
+2.5V	2.5V switched power rail for DDR4	2.5	ON	OFF	OFF
+3V_RTC	RTC power	3.3	ON	ON	ON
+VGPU_CORE	VGA power	0.6~1.2	ON	OFF	OFF
+1.05V_GFX	VGA power	1.05	ON	OFF	OFF
+1.35V_GFX	VGA power	1.35	ON	OFF	OFF
+3V_GFX	VGA power	3.3	ON	OFF	OFF
+5V_S5_V2	5V for Type-C source power rail	5	ON	ON	ON
+TYPEC_VBUS	5V Type-C power rail	5	ON	ON	ON

VGA Reset





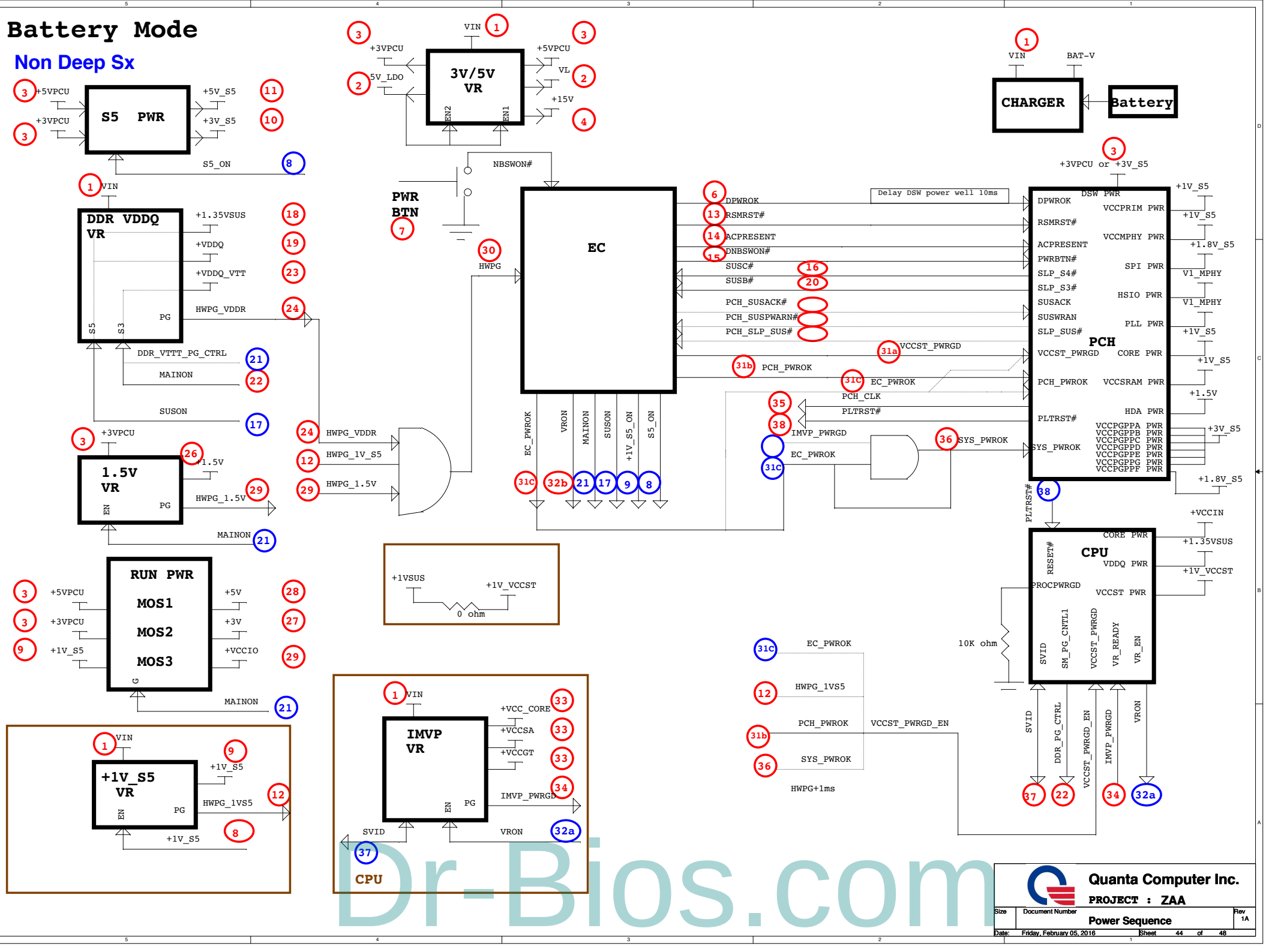
N15x Power on sequance

Notes: -All 3.3V includes all rails powered at 3.3V
-PEX_VDD 1.05V inculdes all rails that are shared

Quanta Computer Inc.
PROJECT : ZAA
Size | Document Number: GPU PWR CRL | Rev 1A
Date: Friday, February 05, 2016 | Sheet 43 of 48

Battery Mode

Non Deep Sx



Quanta Computer Inc.	PROJECT : ZAA		
Size	Document Number	Power Sequence	Rev 1A
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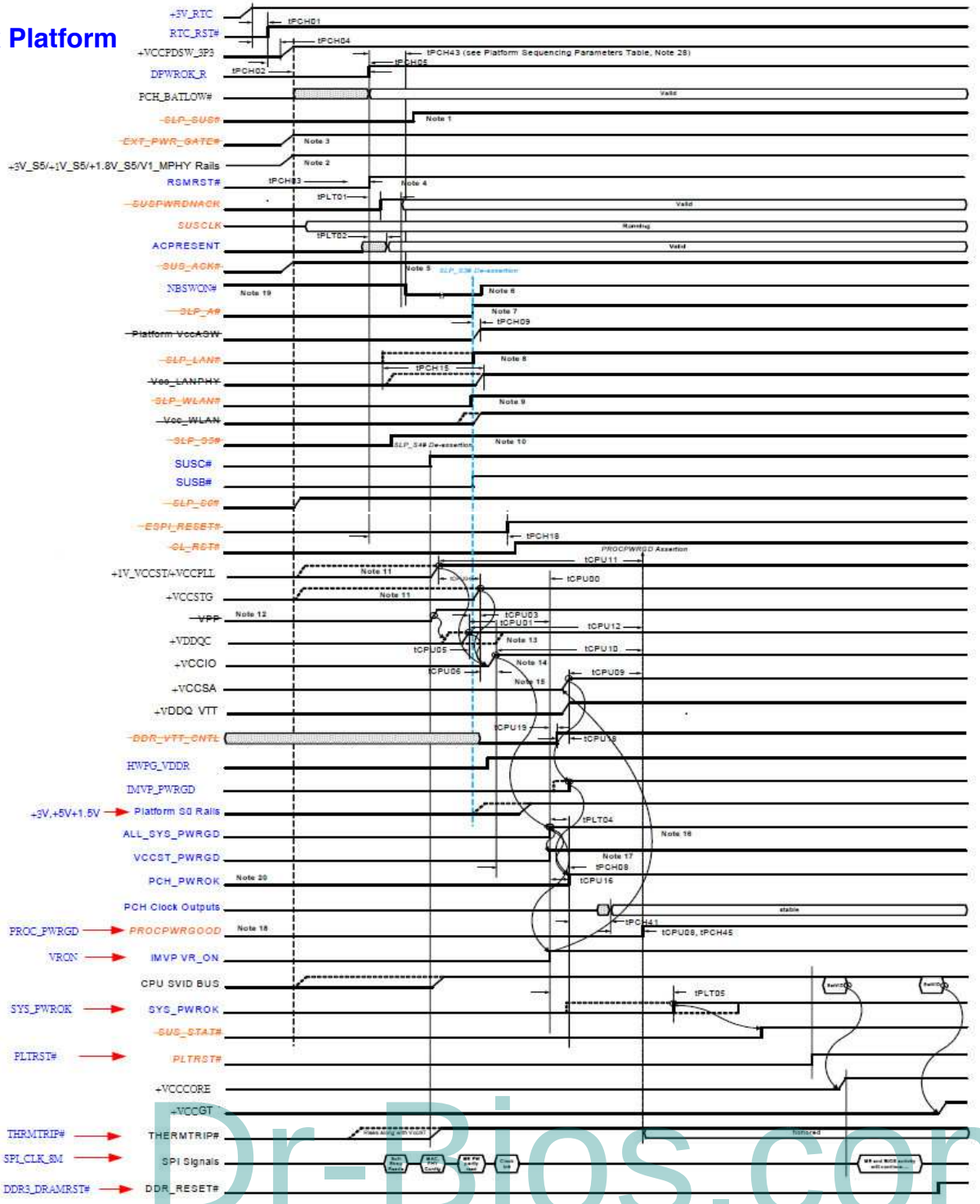
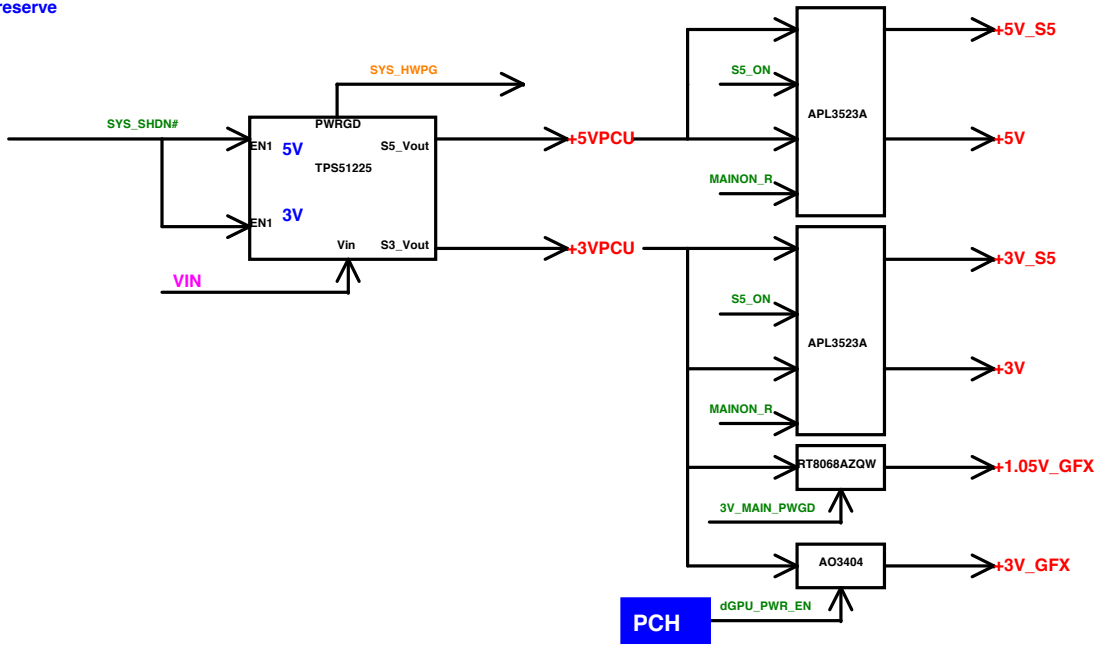
Skylake U Non-Deep Sx Platform Power on sequence

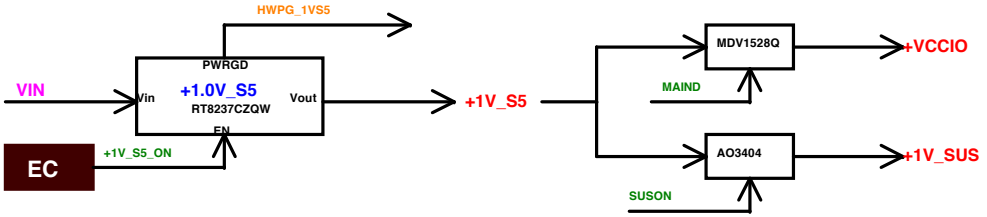


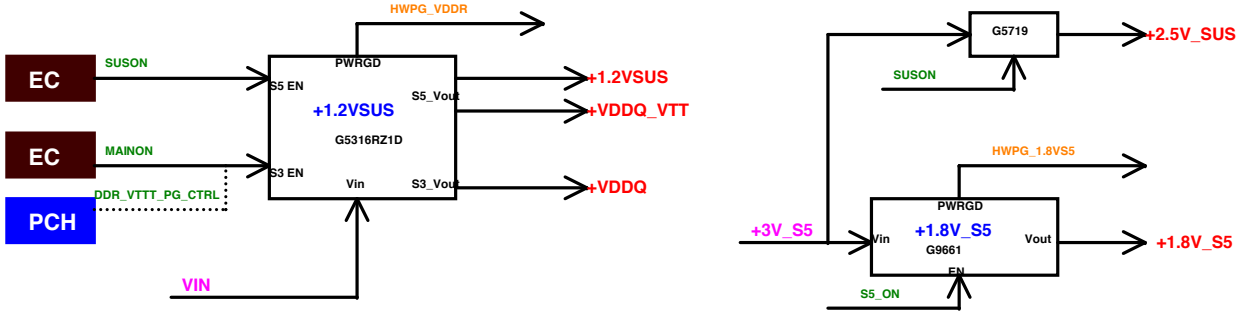
Quanta Computer Inc.
PROJECT : ZAA

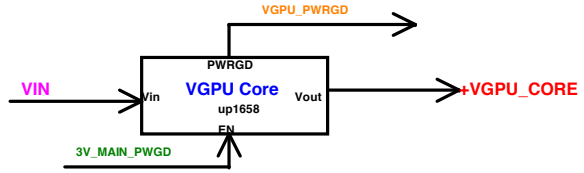
Size	Document Number	Rev
	Power on Sequence	2A
Date: Friday, February 05, 2016	Sheet 45 of 48	

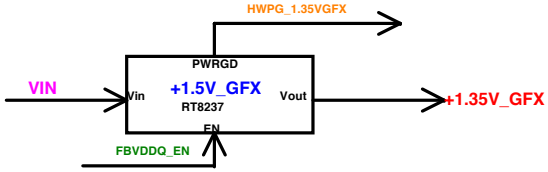
實線表defult
虛線表reserve

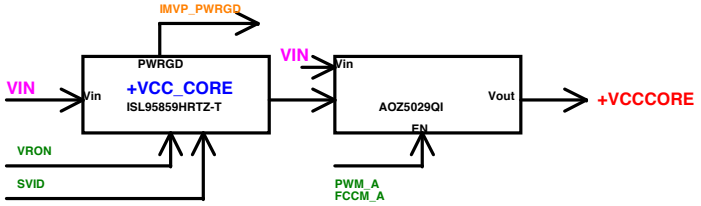


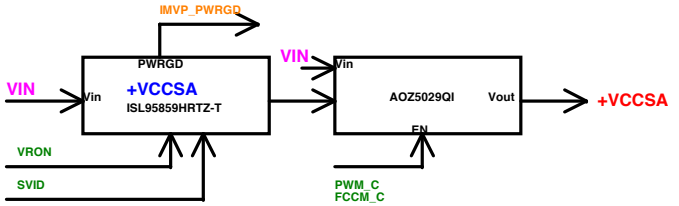


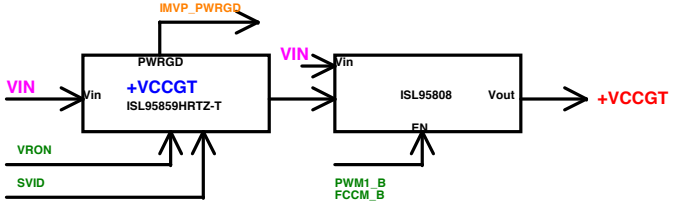


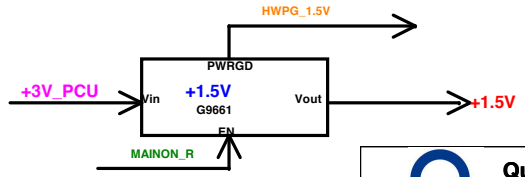












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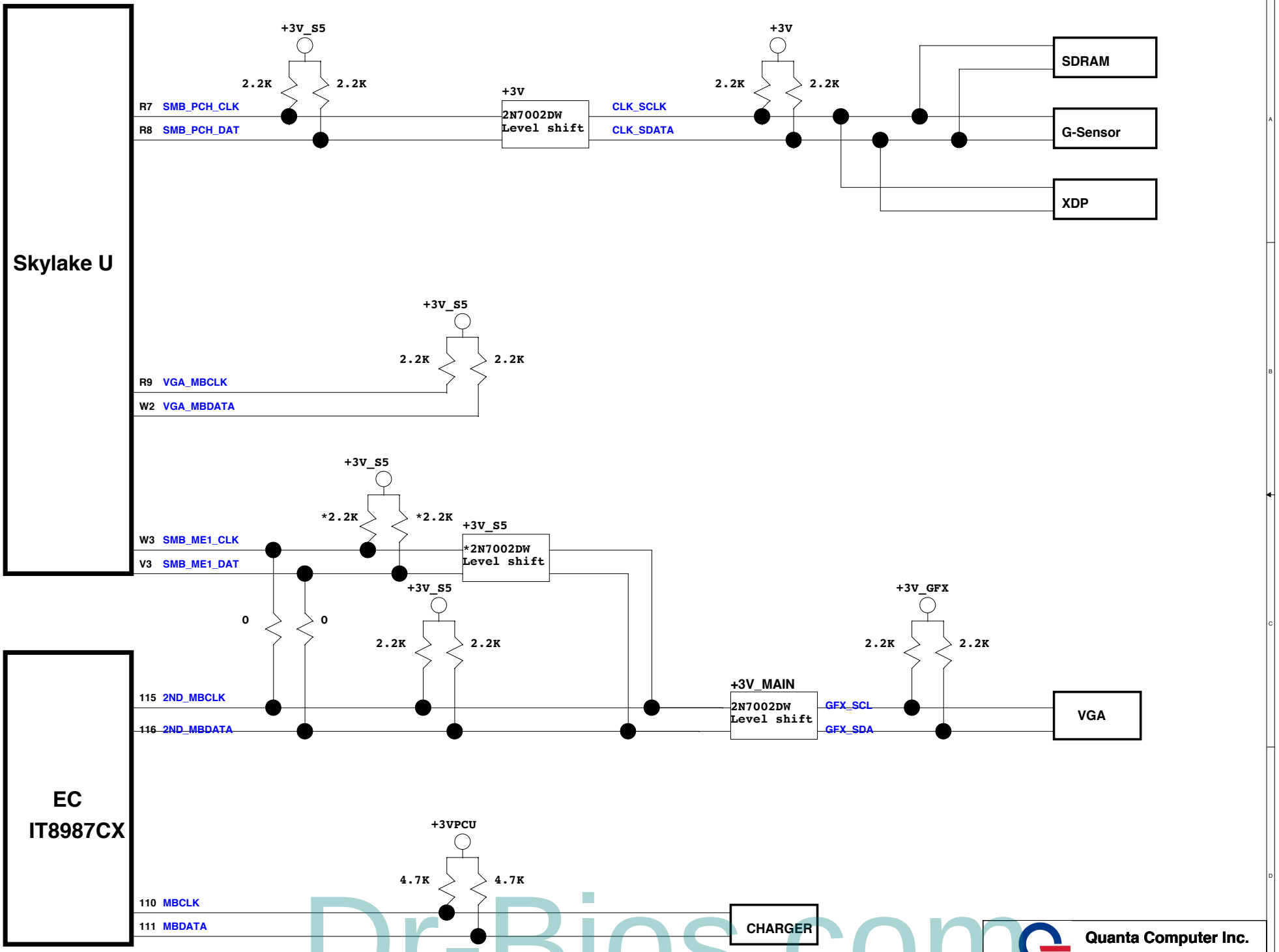

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Model Date

CHANGE LIST

B-CHANGE

B0. Change FP from 0201 to 0402; C689,C688,C683,C194,C241,C227,C216,C242,C205,C252 for RDC request.
B1. Change CN95, CN6, CN20,CN2019, CN7,JDIM1, JDIM2,CN10 of foot-print
B2. Page 33 Mount PR6296, remove PR6295 for EC can't boot issue
B3. Page 12 Delete R11170, mount R11133 for DDR4's SPD
B4. Page 13 Delete R11174, mount R11134 for DDR4's SPD
B5. Page 27 Change POA IC U1006's P/N. (ALD00103006)
B6. Page 28 Change CN23's P/N--- 5H; Reserve R11284
B7. Page 25 change R247 value from 0 to 2.2 Ohm (CS-2204FA00); Change R251, R262, R269, R11265 footprint from 0603 to 0805 (LAN)--(CS07504FA11)
B8. Page 2 Mount R485 for THRMTRIP#
B9. Page 17 Change R4314 & R4306 of value for KA/KB
B10. Page 6 Mount Q6060 for CMOS issue
B11. Page 31 Swap U45 Pin81 & Pin32 for DAC Fan; Add D4015 for ESD; Reserve R11282 for battery
B12. Page 6 R512 Change P/N from 5% to 1 % (CS22702FB14)
B13. Page 8 IOAC setting change into none IOAC R598 mount , R599 remove.
B14. Page 29 Delete R328,R11109,R327,R347,R346,C4716,C4718,C4717,C4558 & Q6061; Add C321,C723,C728,C719,R218 & U12 for DAC Fan; Change CN8's P/N
B15. Page 29 Change KB/BL connector CN's FP,P/N. (DFFC04FR111) & remove CN2018 for ME request
B16. Page 29 Chage CP1-CP6 into 0402 size, from C4788-C4811
B17. Page 26 Change Speaker connector CN18's FP,P/N. (DFHD04MR176)
B18. Page 26 Modify U16,U4512 pin2 to +3V , then off U16 & U4512
B19. Page 15 Change C4117,C4118 from 22U into 10U, and Add C4815, C4812 (10U-0402) for layout speace.
B20. Page 18 Change C4423,C4426 from 22U into 10U, and Add C4813, C4814 (10U-0402) for layout speace.
B21. Page 31 Change SW4's P/N & FP; Add R1283 for EC AUTO RECOVERY.
B22. Page 28 Change Hole16's P/N & FP, Add Hole25, Hole26 for ME modify ; Add R11284
B23. Page 5 Change C202 value from 47U to 22U & add C4816
B24. Page 23 Change R11268,R11271 from 33 to 47 Ohm ; Change L5,L6,L7's P/N; Not mount C718,C716,C319,C333,C336
B25. Page 32 Change PJ3's FP
B26. Page 30 Change U22's FP
B27. Page 24 Change CN12's FP
B28. Page 4 Change C739 from 10 to 22P & mount for EMI request
B29. Page 21 Add C4817 & C4818 for EMI request
B30. Page 2 Change R577 & R152 power to +3V_S5 for leakage
B31. Page 8 Change R211 power to +3V_S5 for leakage
B32. Page 22 Add R11285, R11286(reserve)
B33. Page 21 Cancle co-layout R11225,R11226,R11227,R11228,R11229,R11230,R11231 & R11232.
B34. Page 14 Change C356 & 362 for vendor recommend
B35. Page 24 Mount R11277, Remove R11274 change to -4db

Power-CHANGE

B36. Page 33 Delete JP18, JP20 ,PR248,PR249,PR6127,PR6219,PR345,PR244,,PR247,PR246,PR266,PR272
B37. Page 34 Delete JP9
B38. Page 35 Delete JP16
B39. Page 36 Delete JP22,JP29
B40. Page 37 Change PR225,PR224's value from 10k to 13.7K; Add SP@ at PR194,PR203,PR207,PR202
B41. Page 38 Delete JP24, change JP25 to PR6304
B42. Page 39 Delete JP26
B43. Page 40 Delete PR6298,PQ6066,PR137,PQ4,PR153,PQ10; Change PU2 & PU6's P/N for ESD.
B44. Page 41 Delete JP34
B45. Page 42 Delete JP10,JP35
B46. Change DDR solution to RT8231B
Change +1V_S5 solution to G5335
Change +1.35V_GFX solution to G5335
Revise LDO P/N to AL001282000 (YB1282PSP8)
LDO (PU2 & PU6) Pin4 adding 1u/6.3
B47. Page 37 Change PC10, PC20, PR192,PC28,PR211,PR220 & PC39 of value.
B48. Page 25 Add R6308

C-CHANGE
C1. Change 0 Ohm to short pad & remove JP,
R11,R14,R15,R28,R66,R67,R11129,R102,R194,R224,R229,R235,R790,R791,R792,R11111,R11112,R11113,R11140,R112,R135,R179,R180,R182,R185,R187,
R188,R192,R193,R198,R240,R252,R11131,R164,R246,R339,R350,R11185,R11186,R550,R657,R718,R721,R782,R11153,R11283,R795,R796,R797,R816,
R817,R818,R819,R820,R821,R11196,R11199,R11202,R11207,R11279,R11280,R11281,R948,R951,R956,R958,R959,R960,R11061,R11062,R11110,R11133,
R11134,R11136,R11137,R11138,R11139,R11141,R11253,R11254,R11255,R11256,R11267,R11270,PR257,PR263,PR267,PR274,PR281,PR82,PR83,PR94.
PR87,PR254,PR264,PR109,PR110,PR117,PR122,JP8,JP10,JP14,JP15,JP17,JP22,JP33,JP19,JP21
R4328,R4335,R2855,R2870,R318,R221,R403,R405,R742,R743,R725,R745,L19,R2872
C2. Page 31 remove SW2 -- power bottom
C3. Page 29 Change CN20 & CN2019 K/B connector of P/N
C4. Page 27 Delete Q76, R11288; Add C4819, R11290 ,R11291,R11298,R11299,R11302,R11303,R11300,R11301,R11292,R11293,R11294,R11295 for co-layout POA & PBA ; Reseeve EC52,EC53,R11289 & R11287
C5. Page 21 remove R11193, double mount at type-C
C6. Page 32 for power request change short pad to 10 Ohm, location PR209 & PR210; Change PC115 of value
C7. Page 8 remove R618, it can't mount, because none device.
C8. Page 38 mount PC138 -- power request.

U12,Q31,PR192

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		PART NUMBER:		DRAWING BY:	REVISON: