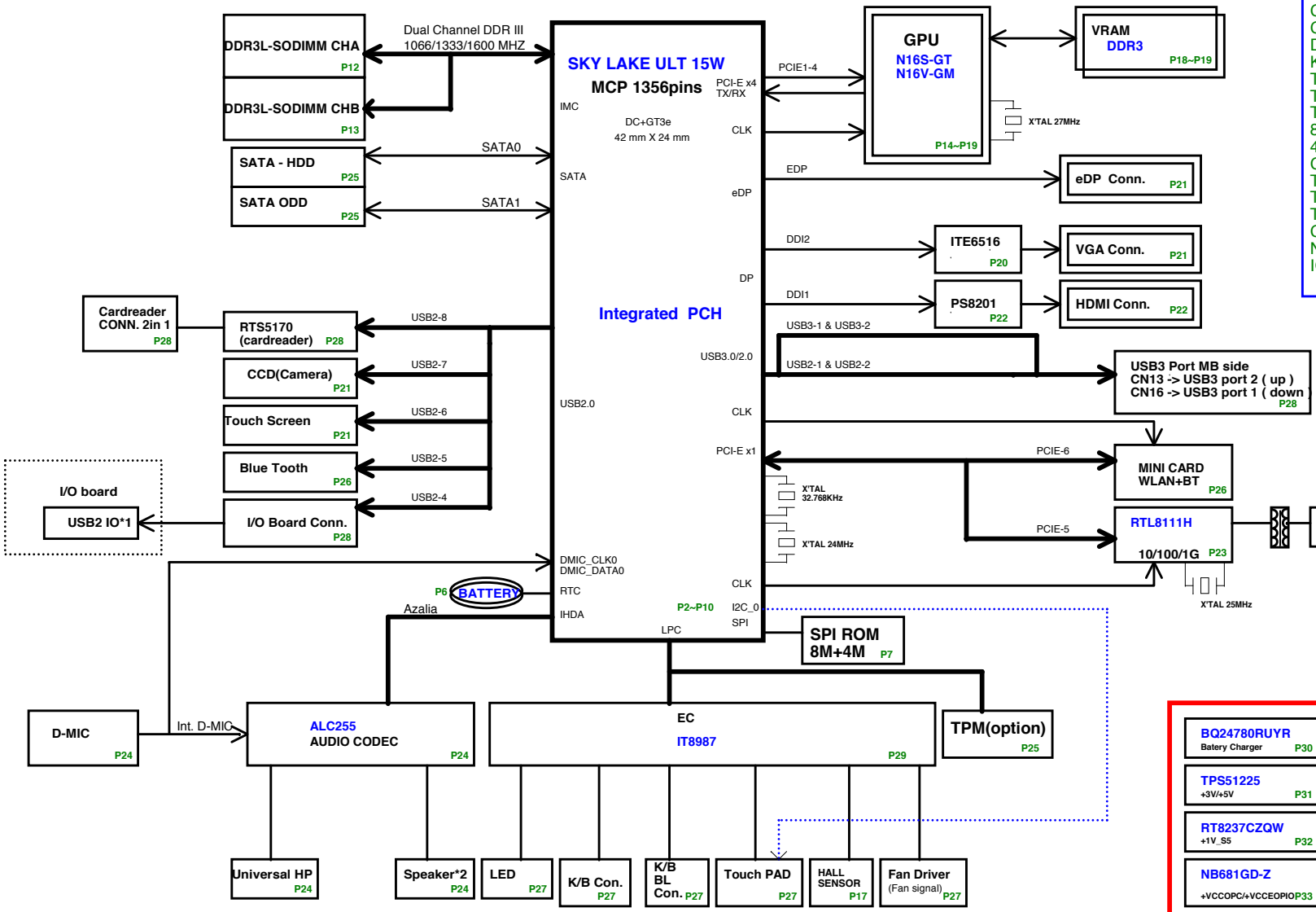
Zoro_SL (ZRW) SKL ULT SYSTEM BLOCK DIAGRAM



BOM

IV@ : iGPU
EV@ : Optimus
GT@ : N16S-GT / GC6
GM@ : N16V-GM / WO GC6
DR@ : For Dual Rank (VRAM 8 pcs)
KBL@ : Keyboard backlight
TPM@ : TPM
TPM_N@: For TPM 2.0
TPM_I@ : For TPM 1.2
8M@ : 8M FLASH ROM
4M@ : 4M FLASH ROM
GS@ :G-SENSOR
TDI@ : TOUCH PAD I2C
TSU@ : TOUCH SCREEN USB
TSI@ : TOUCH SCREEN I2C
GT3@ : GT3 CPU
NAC@ : Non IOAC
IOAC@ : For IOAC

BQ24780RUYR Batery Charger P30	G5316RZ1D +1.35VSUS P35	Thermal Protection Discharger P40
TPS51225 +3V/+5V P31	MDV1528Q +5V_S5/+3V_S5/+3V/+5V P31	UP1658RQKF +VGPU_CORE P41
RT8237CZQW +1V_S5 P32	ISL95859HRTZ-T +VCORE/VCCSA/VCCGT P38	RT8068AZQW +1.05V_GFX/+3V_GFX +1.5V_GFX P42
NB681GD-Z +VCCOPC/+VCCEOPIO P33		

Quanta Computer Inc.
PROJECT : ZRW
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Block Diagram
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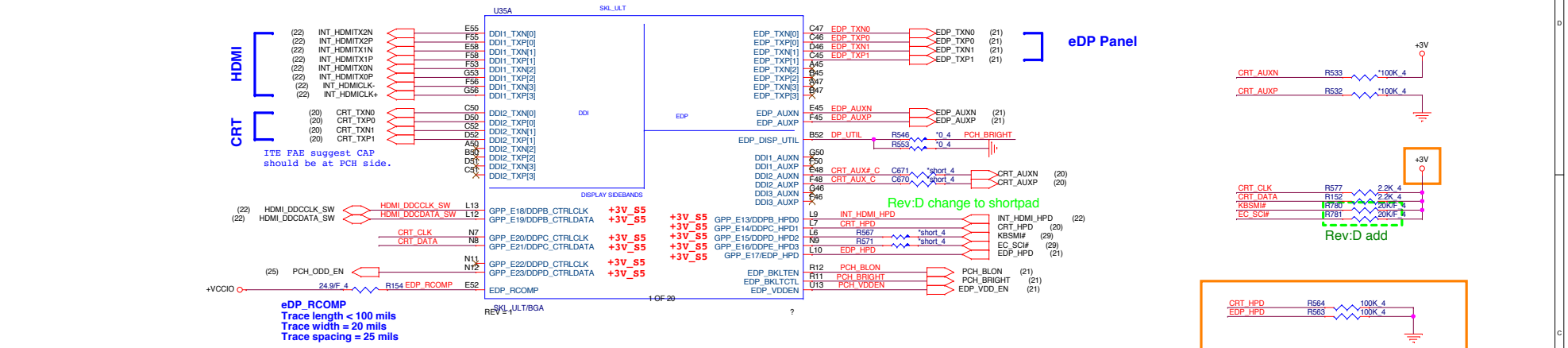
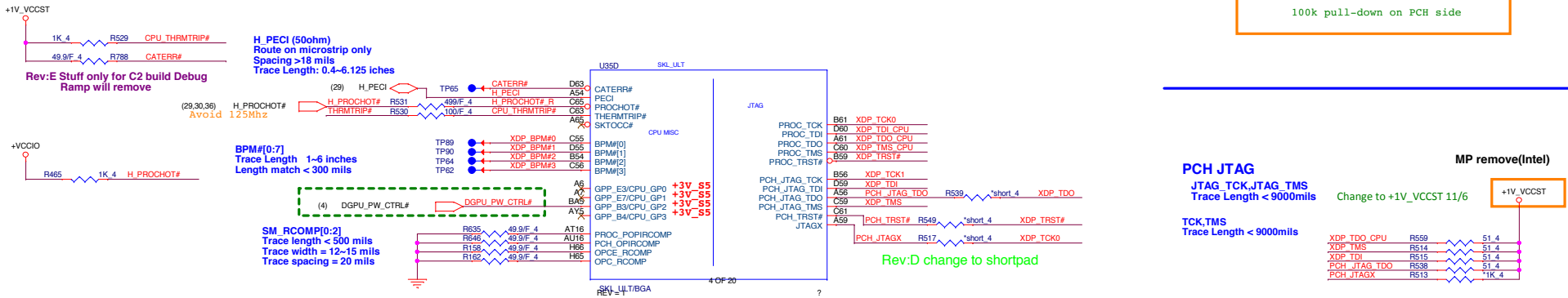
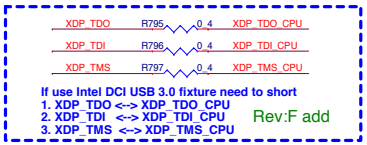
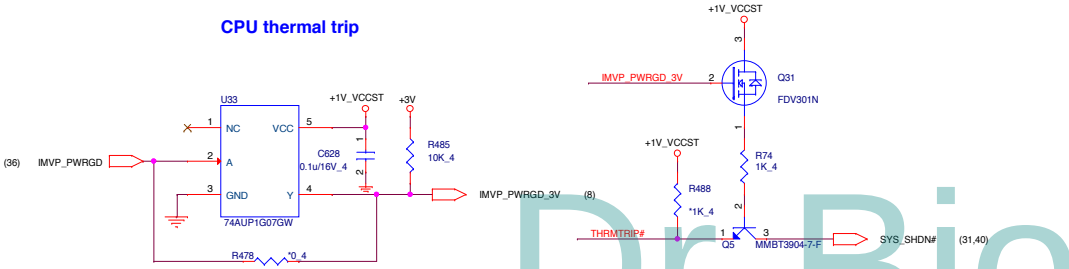
Skylake ULT (DISPLAY,eDP)

02







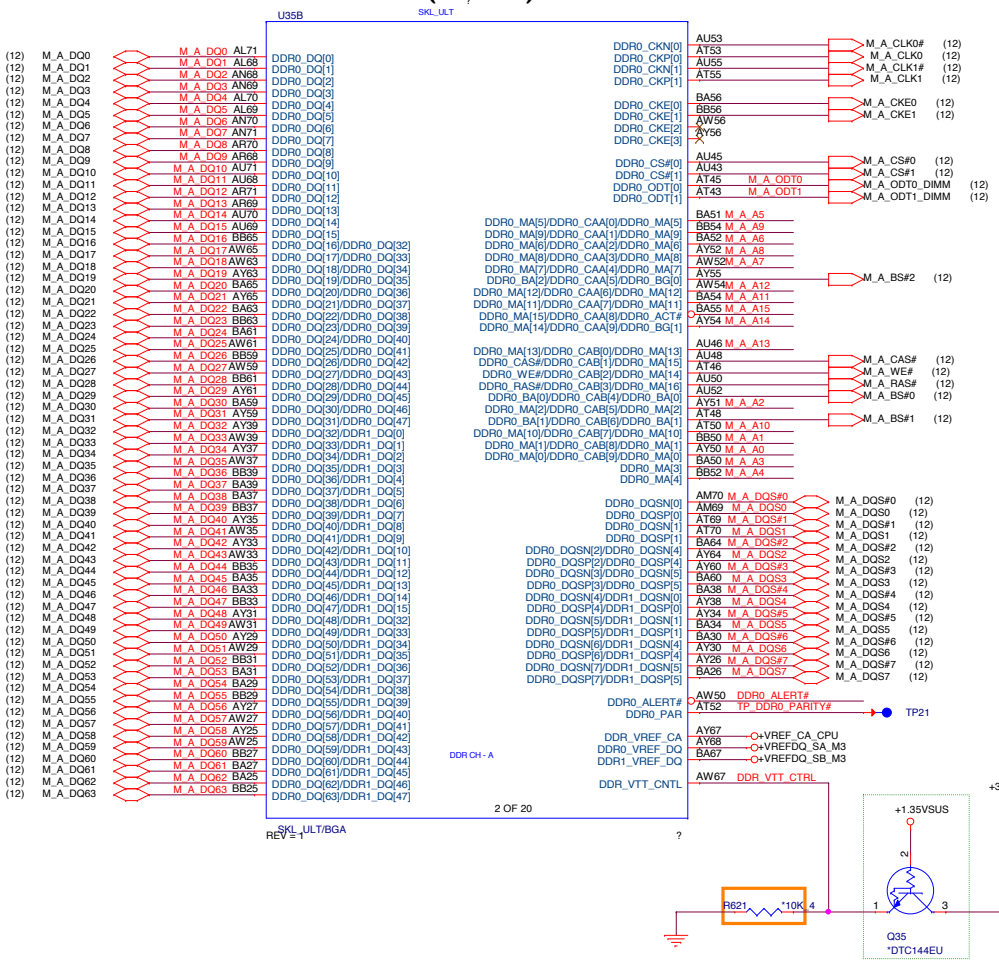


Quanta Computer Inc.
PROJECT : ZRW

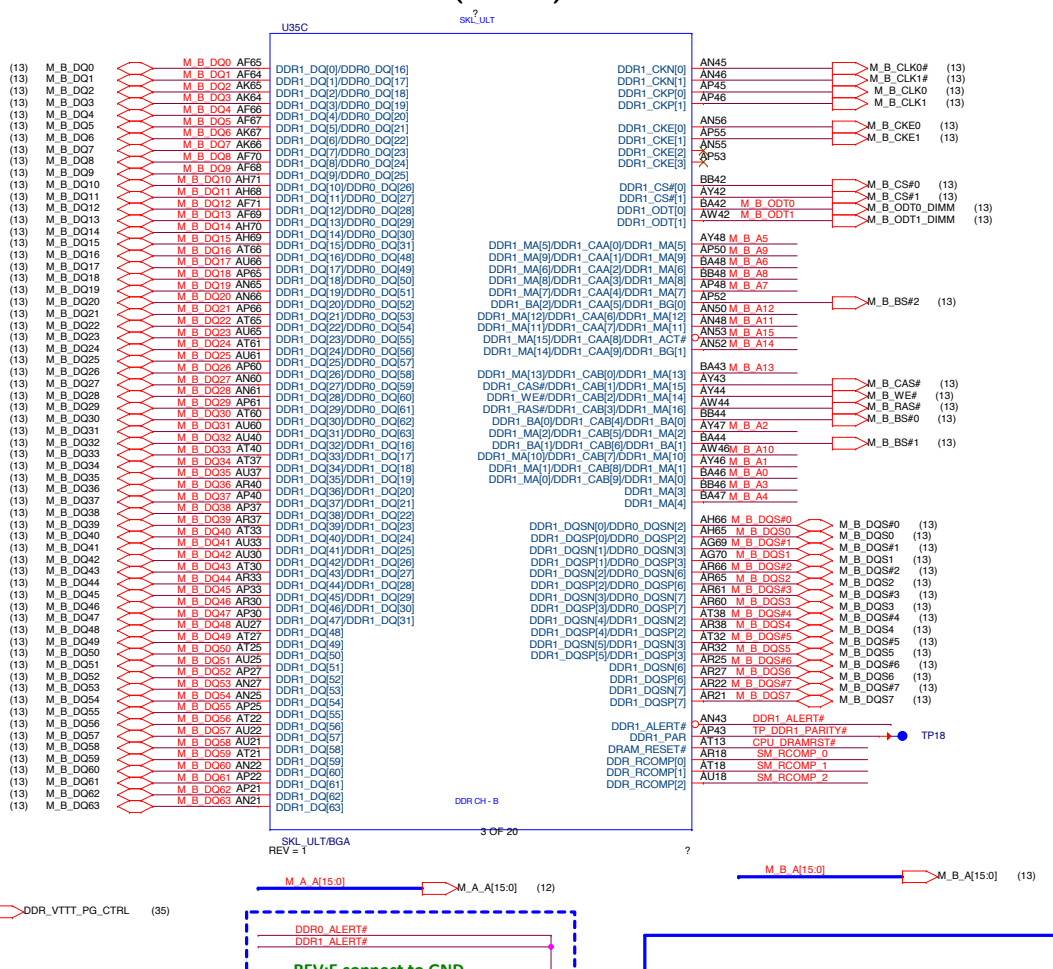
Size	Document Number	Rev
	Skylake 1/4 (DDI/eDP)	3A
Date: Monday, July 20, 2015	Sheet 2 of 48	

Change Data and DQS to interleave.

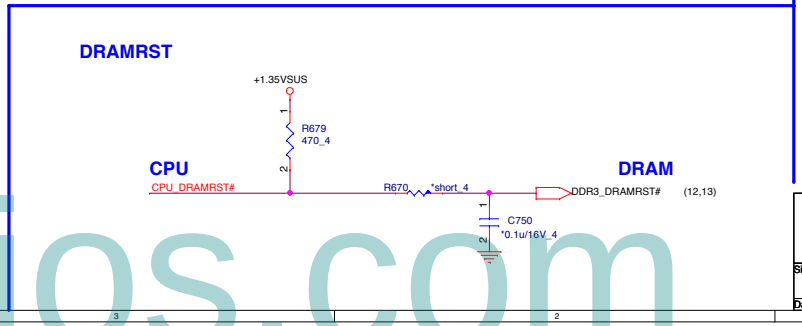
SKL ULT (DDR3L)

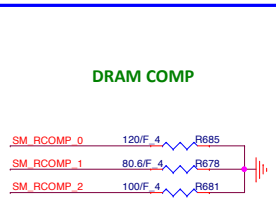


SKL ULT (DDR3L)



Stuff Q54 for both UMA and GPU in DDR_VTT_CNTL





Quanta Computer Inc.			
PROJECT : ZRW			
Size	Document Number		Rev
	Skylake 2/3 (DDR3 I/F)		3A
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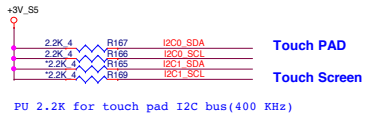
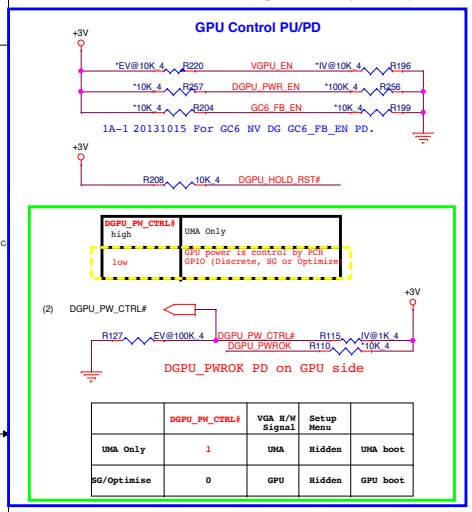
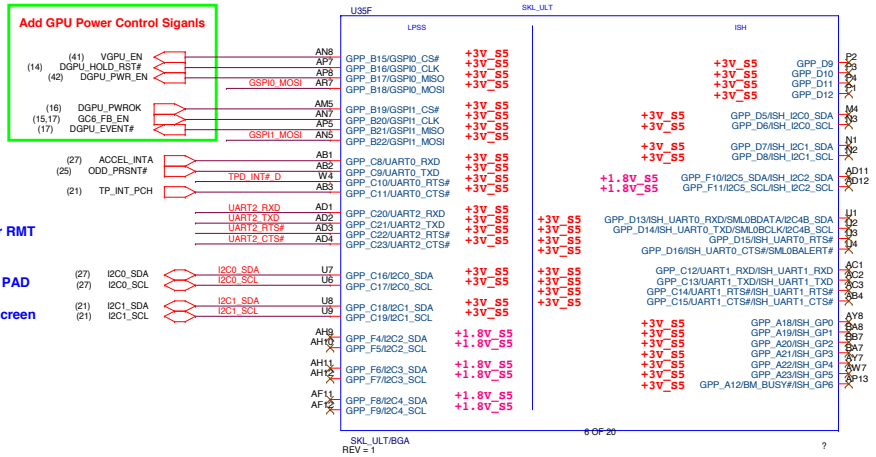
SKL ULT (SIDEBAND) GPIO

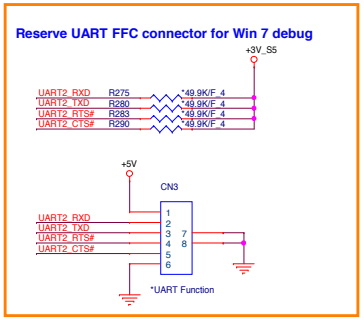
H_PECI (50ohm)
Route on microstrip only
Spacing >18 mils
Trace Length: 0.4~6.125 iches

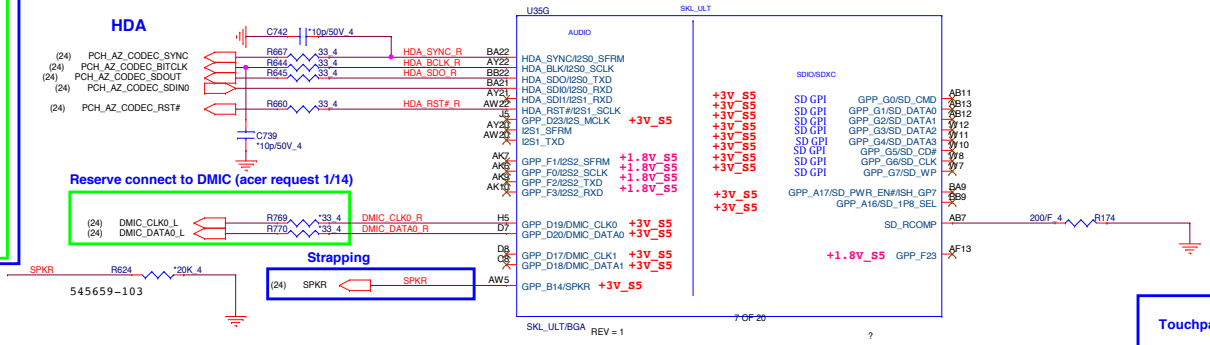
H_PWRGOOD (50ohm)
Trace Length: 1~11.25 inches

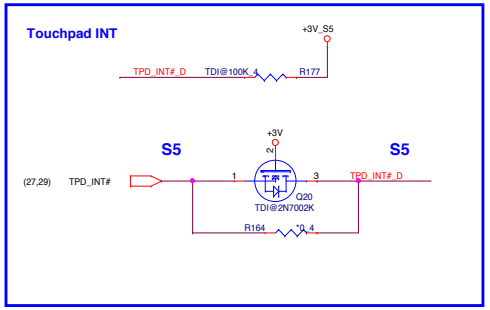












Skylake-U Strapping Table

Pin Name	Strap description	Sampled	Configuration	note
GPP_B14 (SPKR)	Top-Block Swap override	PCH_PWROK	0 = *Disable Top Swap (iPD 20K) 1 = Enable Top Swap Mode	+3V R625 *1K_4 SPKR
GPP_B18 (GSPI0_MOSI)	No reboot	PCH_PWROK	0 = *Disable No Reboot (iPD 20K) 1 = Enable No Reboot Mode	+3V R619 *1K_4 GSPI0_MOSI
GPP_C2 (SMBALERT#)	TLS Confidentiality	RSMRST#	0 = *Disable Intel ME Cryp to TLS(iPD 20K) 1 = Enable Intel ME Cryp to TLS	+3V_S5 R160 *10K_4 SMBALERT# (7)
GPP_B22 (GSPI1_MOSI)	Boot BIOS Strap Bit (BBS)	PCH_PWROK	0 = *SPI (iPD 20K) 1 = LPC	+3V R207 *1K_4 GSPI1_MOSI
GPP_C5 (SML0ALERT#)	eSPI or LPC	RSMRST#	0 = *LPC is selected for EC (iPD 20K) 1 = eSPI selected for EC	+3V_S5 R586 *1K_4 SML0ALERT# (7)
SPI0_MOSI	Reserved	RSMRST#	(iPU 15 ~ 40K)	
SPI0_MISO	Reserved	RSMRST#	(iPU 15 ~ 40K)	
GPP_B23 (SML1ALERT# /PCHHOT#)	Reserved	RSMRST#	(iPD 20K)	
SPI0_IO2	Reserved	RSMRST#	(iPU 15 ~ 40K)	
SPI0_IO3	Reserved	RSMRST#	(iPU 15 ~ 40K)	
HDA_SDO / I2S_TXD0	Flash Descriptor Security Override / Intel ME Debug Mode	PCH_PWROK	0 = *Enable security in the Flash Description (iPD 20K) 1 = Disable Flash Descriptor Security (Override)	change location to near CPU to prevent impact HDA_SDO signal HDA_SDO_R R737 *1K_4 ME_WR# (29)
GPP_E19 (DDPB_CTRLDATA)	Display Port B Detected	PCH_PWROK	0 = *Port B is not detected (iPD 20K) 1 =Port B is detected	
GPP_E21 (DDPC_CTRLDATA)	Display Port C Detected	PCH_PWROK	0 = *Port C is not detected (iPD 20K) 1 =Port C is detected	

Quanta Computer Inc.
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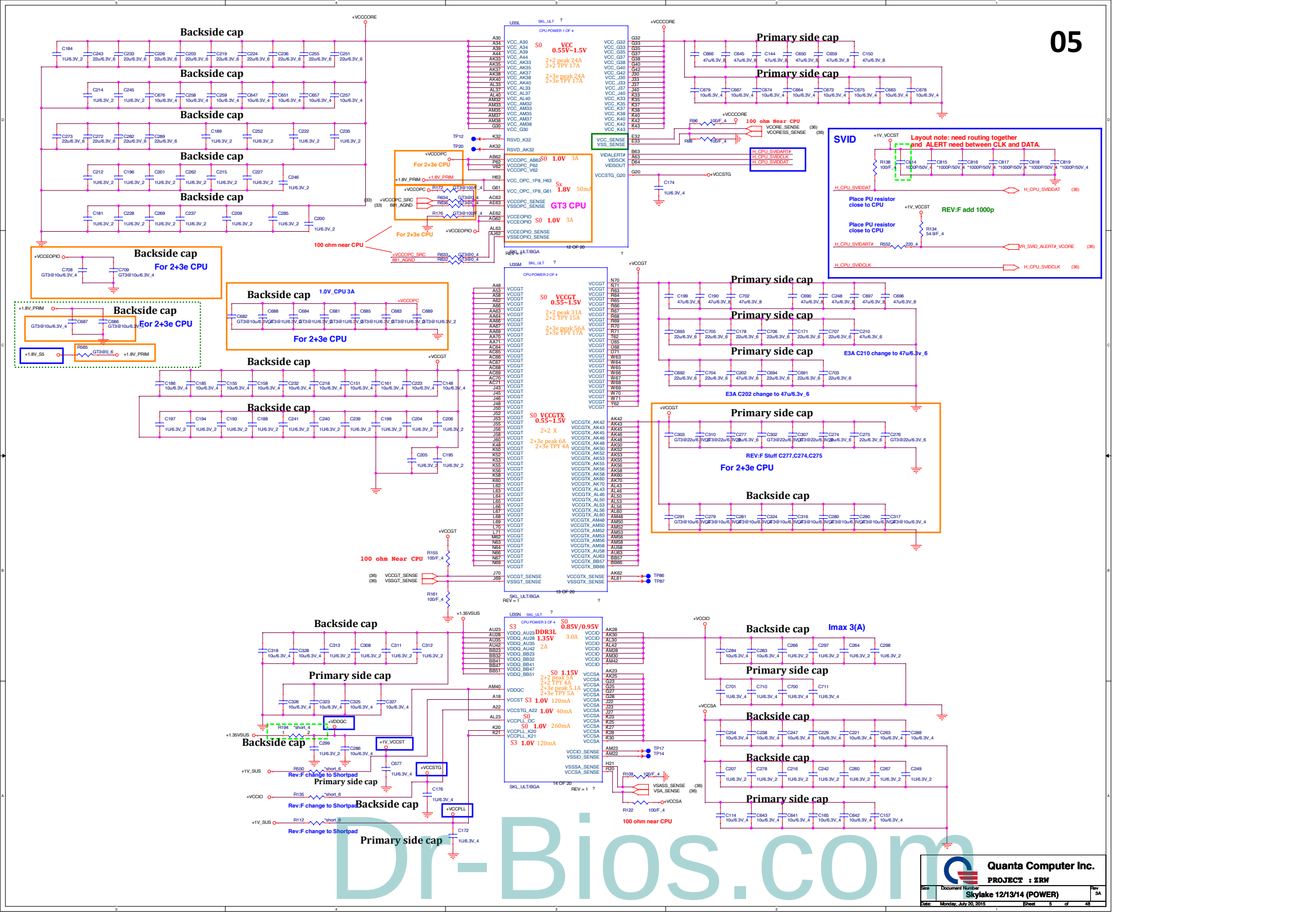
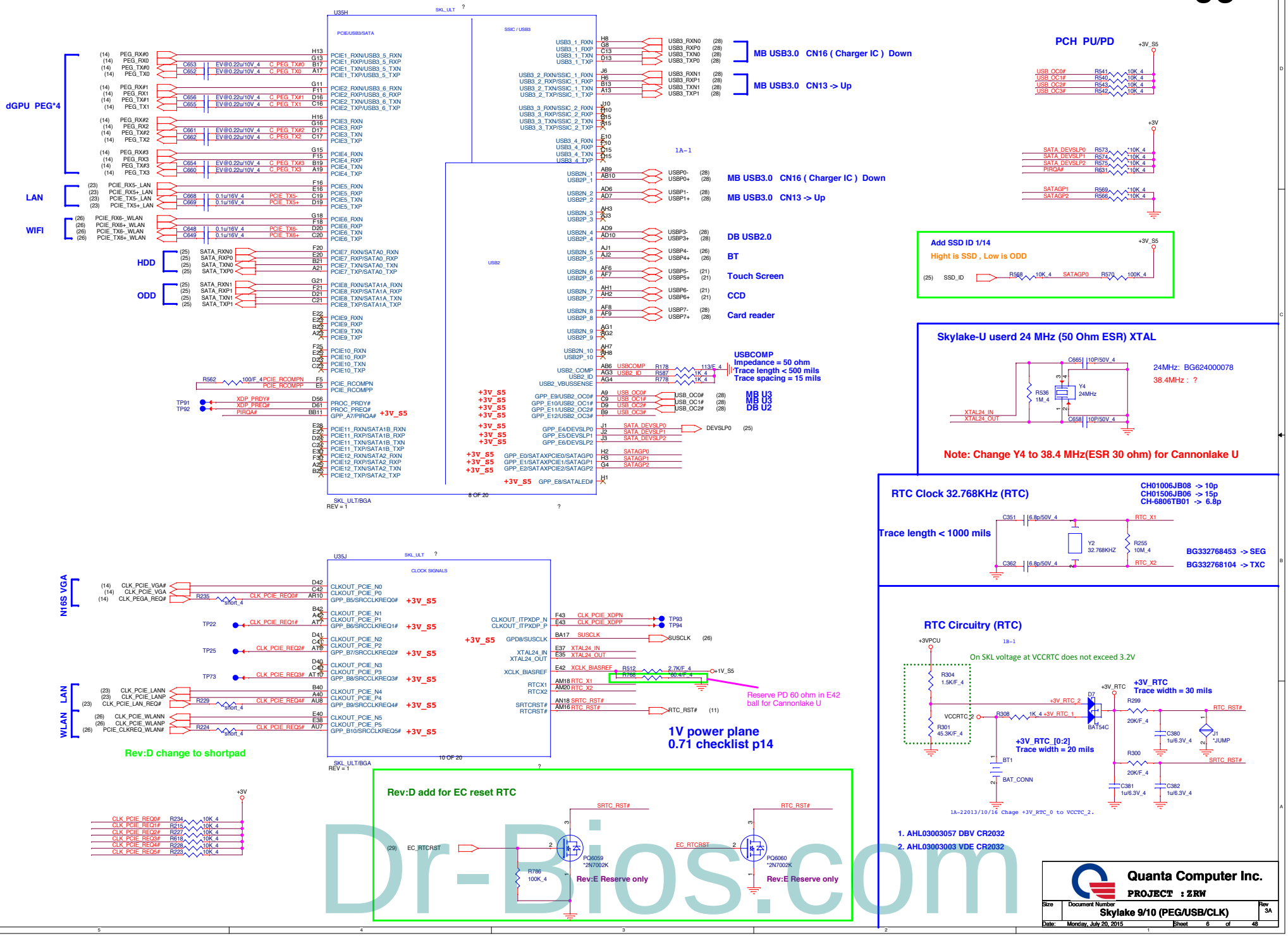
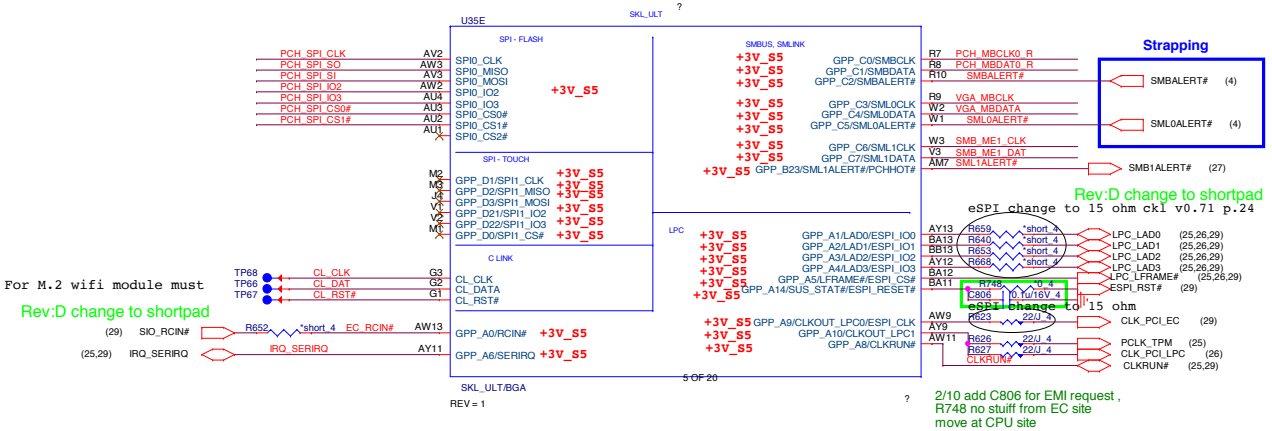

05
Backside cap
Primary side cap
SVID
Layout note: need routing together and ALERT need between CLK and DATA.
Place PU resistor close to CPU
REV:F add 1000p
For 2+3e CPU
GT3 CPU
100 ohm near CPU
E3A C210 change to 47u/6.3v_6
E3A C202 change to 47u/6.3v_6
REV:F Stuff C277,C274,C275
Imax 3(A)
REV:F change to Shortpad
Quanta Computer Inc.
PROJECT : ZRW
Skylake 12/13/14 (POWER)
Monday, July 20, 2015

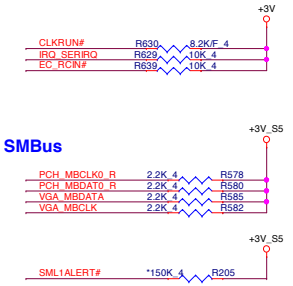
Skylake ULT (GPU, SATA , ODD, CLK ,USB2&3)

06





2/10 add C806 for EMI request , R748 no stuff from EC site move at CPU site



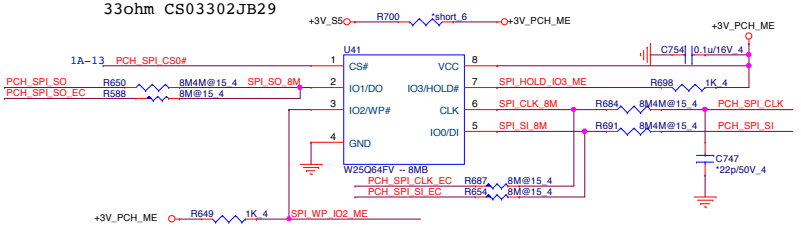
Termination Resistor Requirement for PCH PCHHOT# Pin
Reserve PU 150K resister

SPI ROM	Vender	Size	Quanta P/N	Vender P/N
Skylake 3.3V	WND	8M	AKE3EFP0N07	W25Q64FVSSIQ
	GGD	8M	AKE2EZN0Q00	GD25B64CSIGR

PCH SPI ROM(8M+4M)

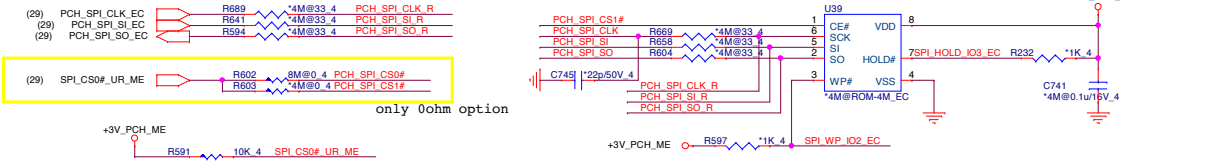
15ohm CS01502JB12
33ohm CS03302JB29

Rev:D change to shortpad

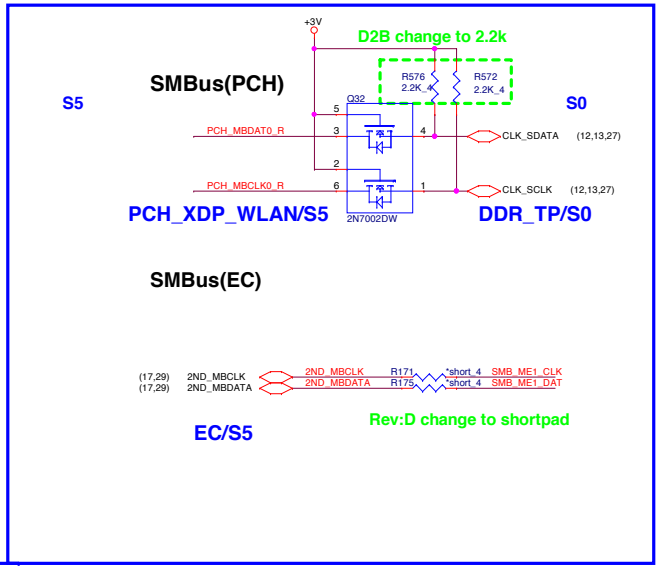


3.3K is original and for no support fast read function

reserve for SPI fast read



1A-3 2013/10/16 Add U34 flash 4M ROM reserve for ZQ0D.



Quanta Computer Inc.
PROJECT : ZRW

Size	Document Number	Rev
	Skylake 5 (SATA/HDA/SPI)	3A

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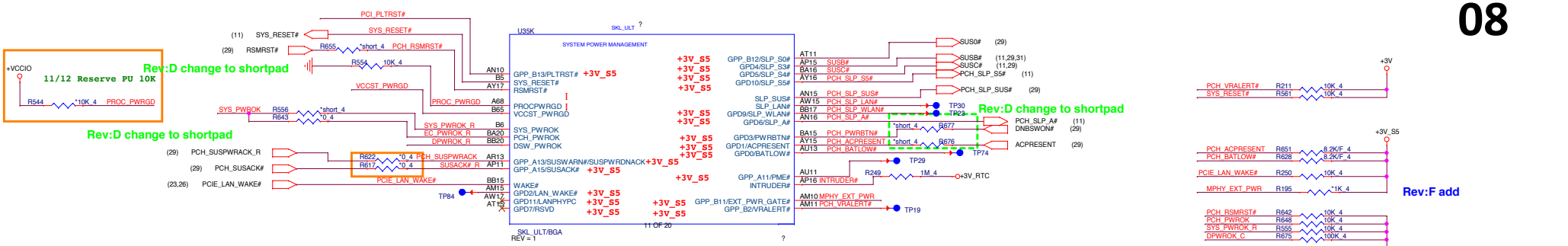
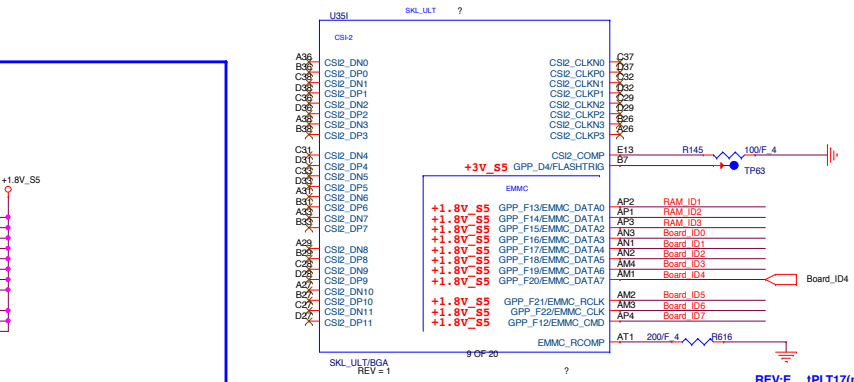
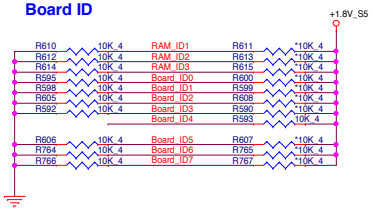


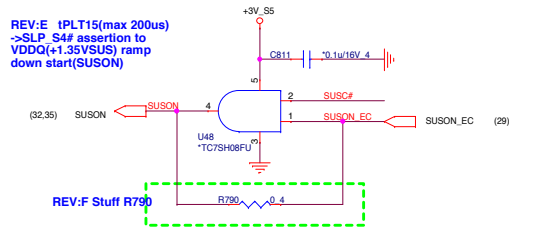


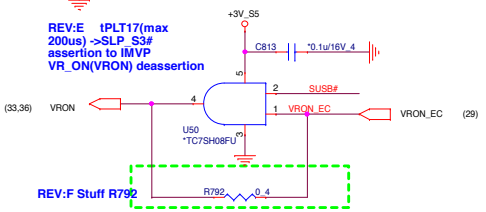
Board ID

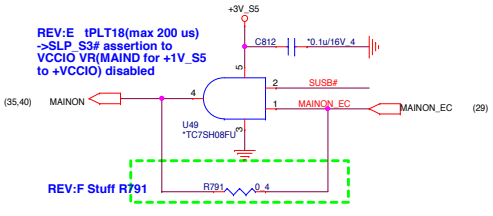


	Low	High
BOARD_ID0	VRAM 2GB	VRAM 4GB
BOARD_ID1	Non IOAC	IOAC
BOARD_ID2	No G-sensor	G-sensor
BOARD_ID3	No TPM	TPM
BOARD_ID4	No touch panel	touch panel

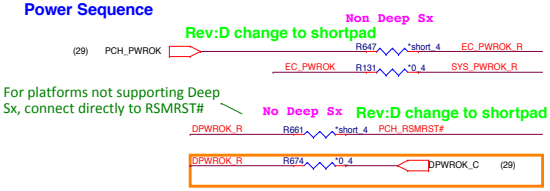
	Low	High
BOARD_ID5	Realtek Audio codec	CPU DSP
BOARD_ID6	Reserved (Default)	Reserve
BOARD_ID7	Reserved (Default)	Reserve



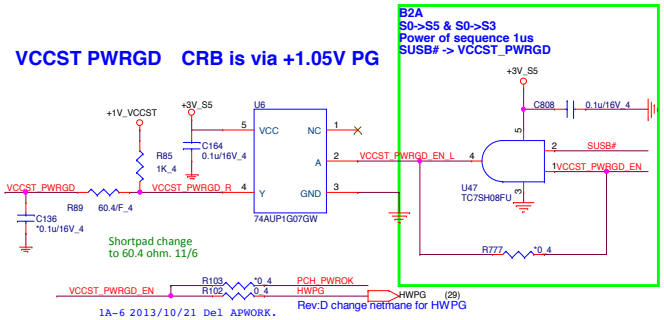




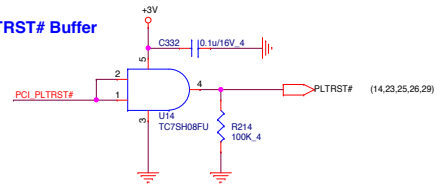
Power Sequence



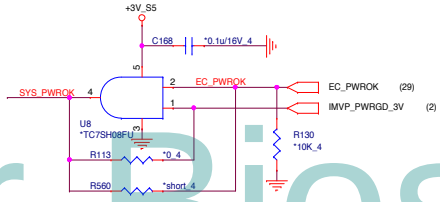
VCCST PWRGD CRB is via +1.05V PG



PLTRST# Buffer



SYSPWOK



Quanta Computer Inc.
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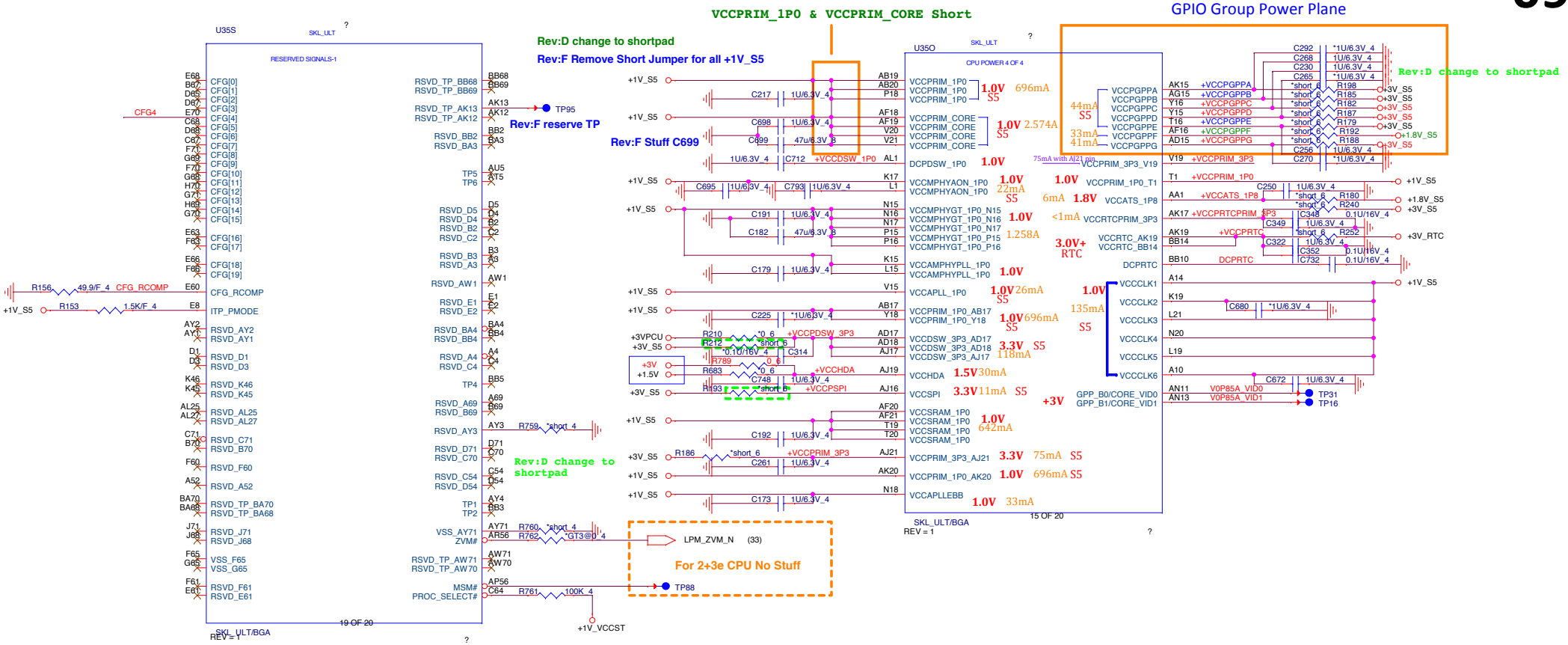

Pin Name	Strap description	Configuration	Note
CFG[0]	Stall reset sequence after PCU PLL lock until de-asserted	1 = *Normal Operation; No stall (iPU 3K) 0 = Stall	
CFG[1]	Reserved Configuration lane		
CFG[2]	PCI Express* Static x16 Lane Numbering Reversal	1 = *Normal Operation(iPU 3K) 0 = Lan number reversed	H & S processor used only
CFG[3]	Reserved Configuration lane		
CFG[4]	eDP enable	1 = Disabled (iPU 3K) 0 = *Enabled	CFG4 R548 1K_4
CFG[6:5]	PCI Express* Bifunction	00 = 1x8, 2x4 PCI Express* 01 = reserved 10 = 2x8 PCI Express* 11 = 1x16 PCI Express*	H & S processor used only
CFG[7]	PEG Training	1 = *PEG Train immediatedly follow RESET# de-assertion (iPU 3K) 0 = PEG wait for BIOS for training	H & S processor used only
CFG[19:8]	Reserved Configuration lane		

Quanta Computer Inc.
PROJECT : ZRW

Size	Document Number	Rev
	Skylake PCH-LP 15/19 (POWER)	3A
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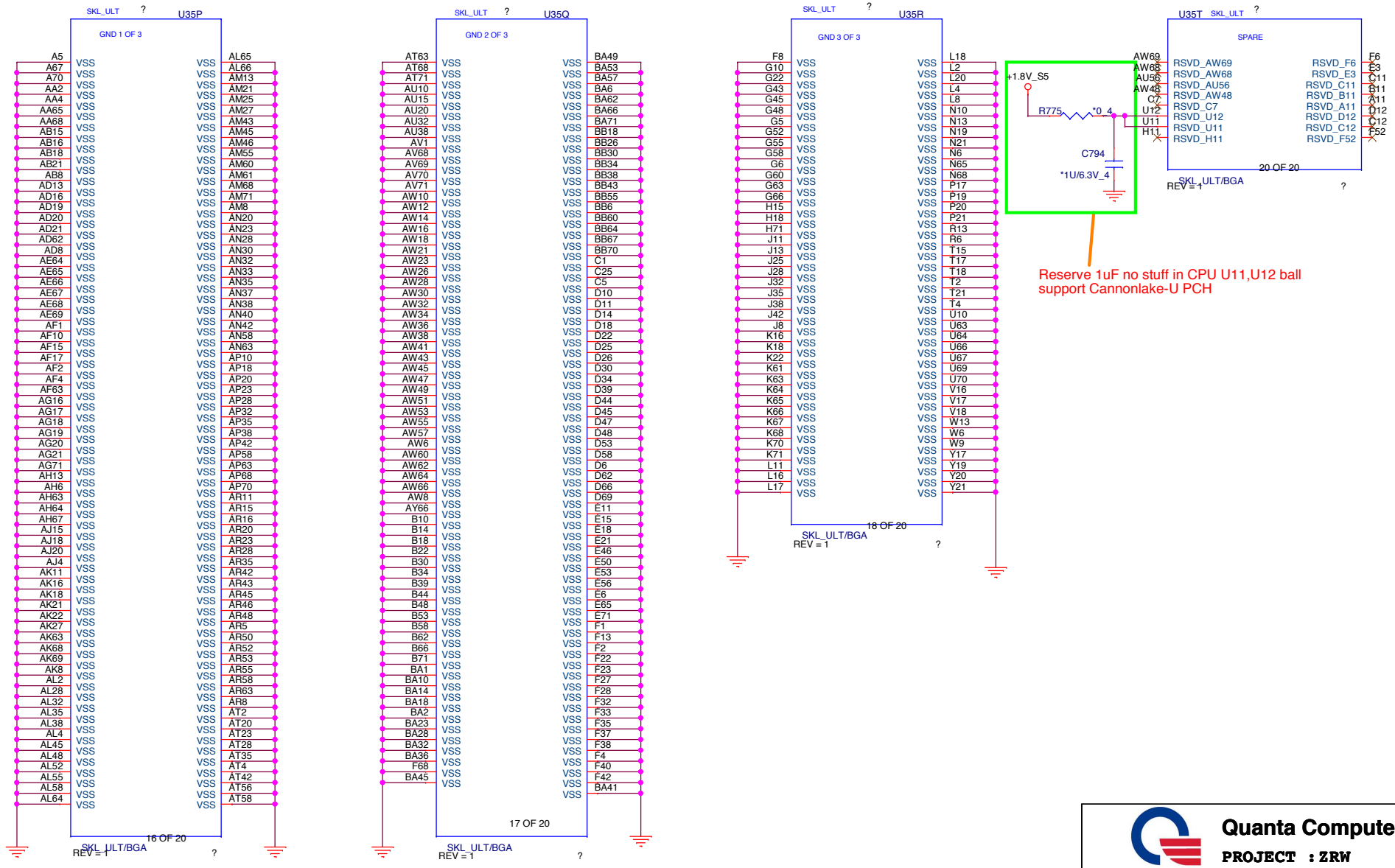
Skylake ULT (GND)



Quanta Computer Inc.		
PROJECT : ZRW		
Size	Document Number: Skylake 10/17/18 (GND)	Rev: 3A
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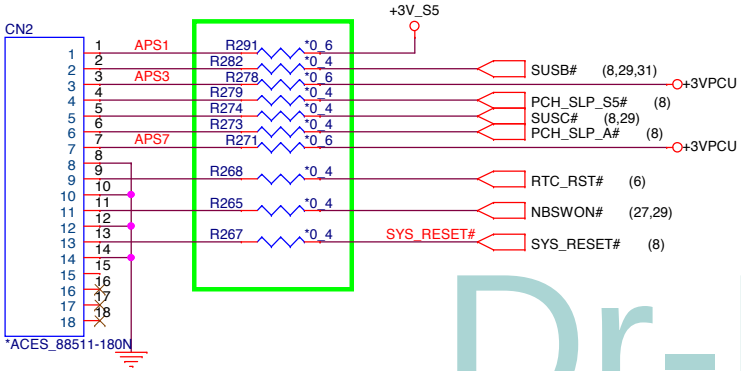
Intel APS Fixture use



Quanta Computer Inc.		
PROJECT : ZRW		
Size	Document Number: CPU/PCH XDP	Rev: 3A
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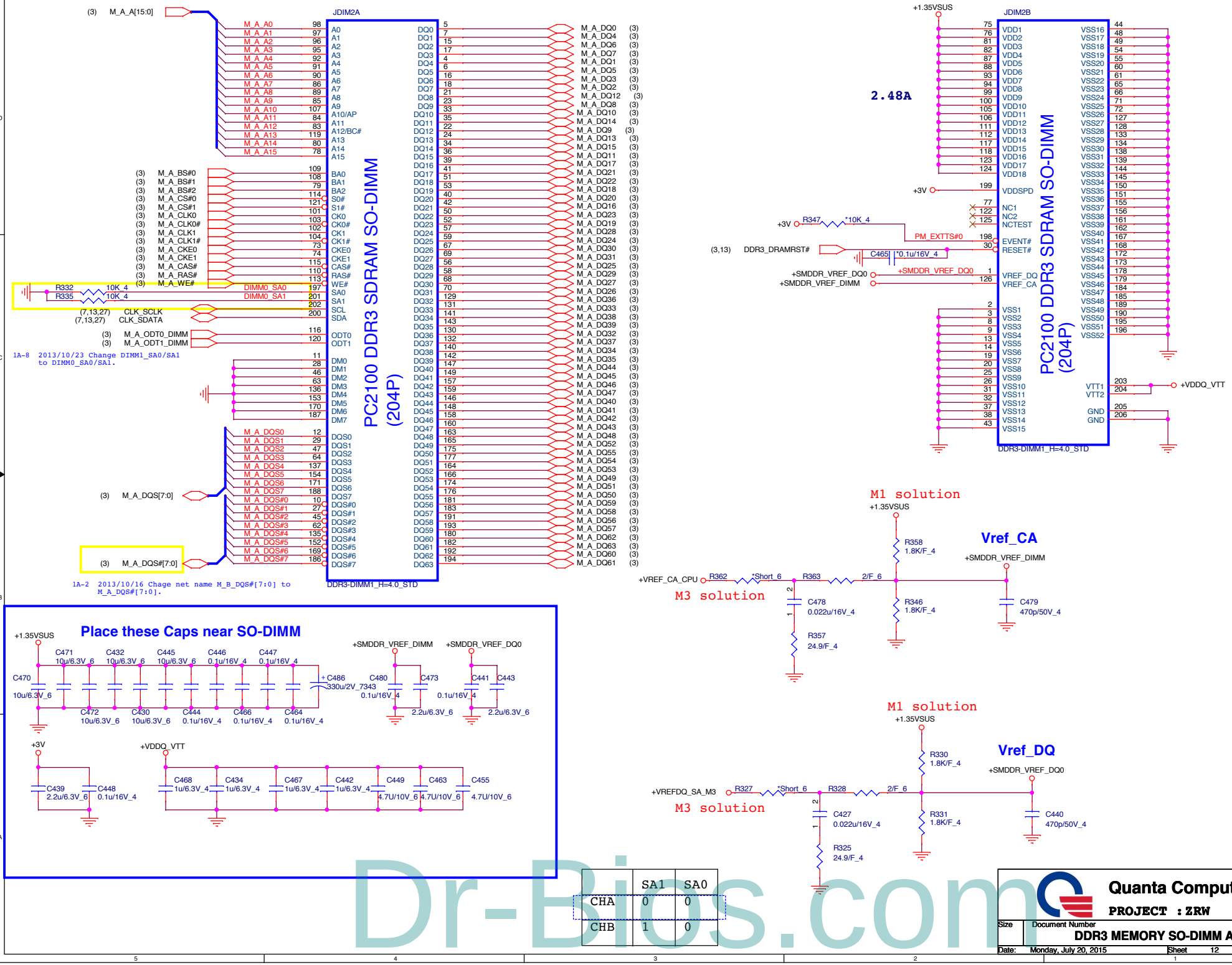
JDIM2A
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDR3-DIMM1_H=4.0_STD
(3) M_A_A[15:0]
M_A_A0 M_A_A1 M_A_A2 M_A_A3 M_A_A4 M_A_A5 M_A_A6 M_A_A7 M_A_A8 M_A_A9 M_A_A10 M_A_A11 M_A_A12 M_A_A13 M_A_A14 M_A_A15
(3) M_A_BS#0 M_A_BS#1 M_A_BS#2 M_A_CS#0 M_A_CS#1 M_A_CLK0 M_A_CLK0# M_A_CLK1 M_A_CLK1# M_A_CKE0 M_A_CKE1 M_A_CAS# M_A_RAS# (3) M_A_WE#
R332 10K_4 R335 10K_4
DIMM0_SA0 DIMM0_SA1
(7,13,27) CLK_SCLK (7,13,27) CLK_SDATA
(3) M_A_ODT0_DIMM (3) M_A_ODT1_DIMM
1A-8 2013/10/23 Change DIMM1_SA0/SA1 to DIMM0_SA0/SA1.
M_A_DQS0 M_A_DQS1 M_A_DQS2 M_A_DQS3 M_A_DQS4 M_A_DQS5 M_A_DQS6 M_A_DQS7
(3) M_A_DQS[7:0]
M_A_DQS#0 M_A_DQS#1 M_A_DQS#2 M_A_DQS#3 M_A_DQS#4 M_A_DQS#5 M_A_DQS#6 M_A_DQS#7
(3) M_A_DQS#[7:0]
1A-2 2013/10/16 Chage net name M_B_DQS#[7:0] to M_A_DQS#[7:0].
M_A_DQ0 M_A_DQ4 M_A_DQ6 M_A_DQ7 M_A_DQ1 M_A_DQ5 M_A_DQ3 M_A_DQ2 M_A_DQ12 M_A_DQ8 M_A_DQ10 M_A_DQ14 M_A_DQ9 M_A_DQ13 M_A_DQ15 M_A_DQ11 M_A_DQ17 M_A_DQ21 M_A_DQ22 M_A_DQ18 M_A_DQ20 M_A_DQ16 M_A_DQ23 M_A_DQ19 M_A_DQ28 M_A_DQ24 M_A_DQ30 M_A_DQ31 M_A_DQ25 M_A_DQ29 M_A_DQ27 M_A_DQ26 M_A_DQ36 M_A_DQ33 M_A_DQ38 M_A_DQ39 M_A_DQ32 M_A_DQ37 M_A_DQ34 M_A_DQ35 M_A_DQ44 M_A_DQ45 M_A_DQ46 M_A_DQ47 M_A_DQ40 M_A_DQ41 M_A_DQ42 M_A_DQ43 M_A_DQ48 M_A_DQ52 M_A_DQ55 M_A_DQ54 M_A_DQ53 M_A_DQ49 M_A_DQ51 M_A_DQ50 M_A_DQ59 M_A_DQ58 M_A_DQ56 M_A_DQ57 M_A_DQ62 M_A_DQ63 M_A_DQ60 M_A_DQ61
JDIM2B
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDR3-DIMM1_H=4.0_STD
+1.35VSUS
2.48A
+3V
R347 *10K_4
(3,13) DDR3_DRAMRST#
C465 *0.1u/16V_4
PM_EXTTS#0
+SMDDR_VREF_DQ0
+SMDDR_VREF_DIMM
VDD1 VDD2 VDD3 VDD4 VDD5 VDD6 VDD7 VDD8 VDD9 VDD10 VDD11 VDD12 VDD13 VDD14 VDD15 VDD16 VDD17 VDD18
VDDSPD
NC1 NC2 NCTEST
EVENT# RESET#
VREF_DQ VREF_CA
VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7 VSS8 VSS9 VSS10 VSS11 VSS12 VSS13 VSS14 VSS15
VSS16 VSS17 VSS18 VSS19 VSS20 VSS21 VSS22 VSS23 VSS24 VSS25 VSS26 VSS27 VSS28 VSS29 VSS30 VSS31 VSS32 VSS33 VSS34 VSS35 VSS36 VSS37 VSS38 VSS39 VSS40 VSS41 VSS42 VSS43 VSS44 VSS45 VSS46 VSS47 VSS48 VSS49 VSS50 VSS51 VSS52
VTT1 VTT2
GND GND
+VDDQ_VTT
M1 solution
+1.35VSUS
Vref_CA
+SMDDR_VREF_DIMM
+VREF_CA_CPU
R362 *Short_6 R363 2/F_6
M3 solution
R358 1.8K/F_4
R346 1.8K/F_4
R357 24.9/F_4
C478 0.022u/16V_4
C479 470p/50V_4
M1 solution
+1.35VSUS
Vref_DQ
+SMDDR_VREF_DQ0
+VREFDQ_SA_M3
R327 *Short_6 R328 2/F_6
M3 solution
R330 1.8K/F_4
R331 1.8K/F_4
R325 24.9/F_4
C427 0.022u/16V_4
C440 470p/50V_4
Place these Caps near SO-DIMM
+1.35VSUS
C471 10u/6.3V_6 C432 10u/6.3V_6 C445 10u/6.3V_6 C446 0.1u/16V_4 C447 0.1u/16V_4
C470 10u/6.3V_6
C472 10u/6.3V_6 C430 10u/6.3V_6 C444 0.1u/16V_4 C466 0.1u/16V_4 C464 0.1u/16V_4
C486 330u/2V_7343
+SMDDR_VREF_DIMM +SMDDR_VREF_DQ0
C480 0.1u/16V_4 C473 2.2u/6.3V_6
C441 0.1u/16V_4 C443 2.2u/6.3V_6
+3V
C439 2.2u/6.3V_6 C448 0.1u/16V_4
+VDDQ_VTT
C468 1u/6.3V_4 C434 1u/6.3V_4 C467 1u/6.3V_4 C442 1u/6.3V_4 C449 4.7U/10V_6 C463 4.7U/10V_6 C455 4.7U/10V_6
SA1 SA0
CHA 0 0
CHB 1 0
Quanta Computer Inc.
PROJECT : ZRW
Size
Document Number
DDR3 MEMORY SO-DIMM A
Rev 3A
Date: Monday, July 20, 2015
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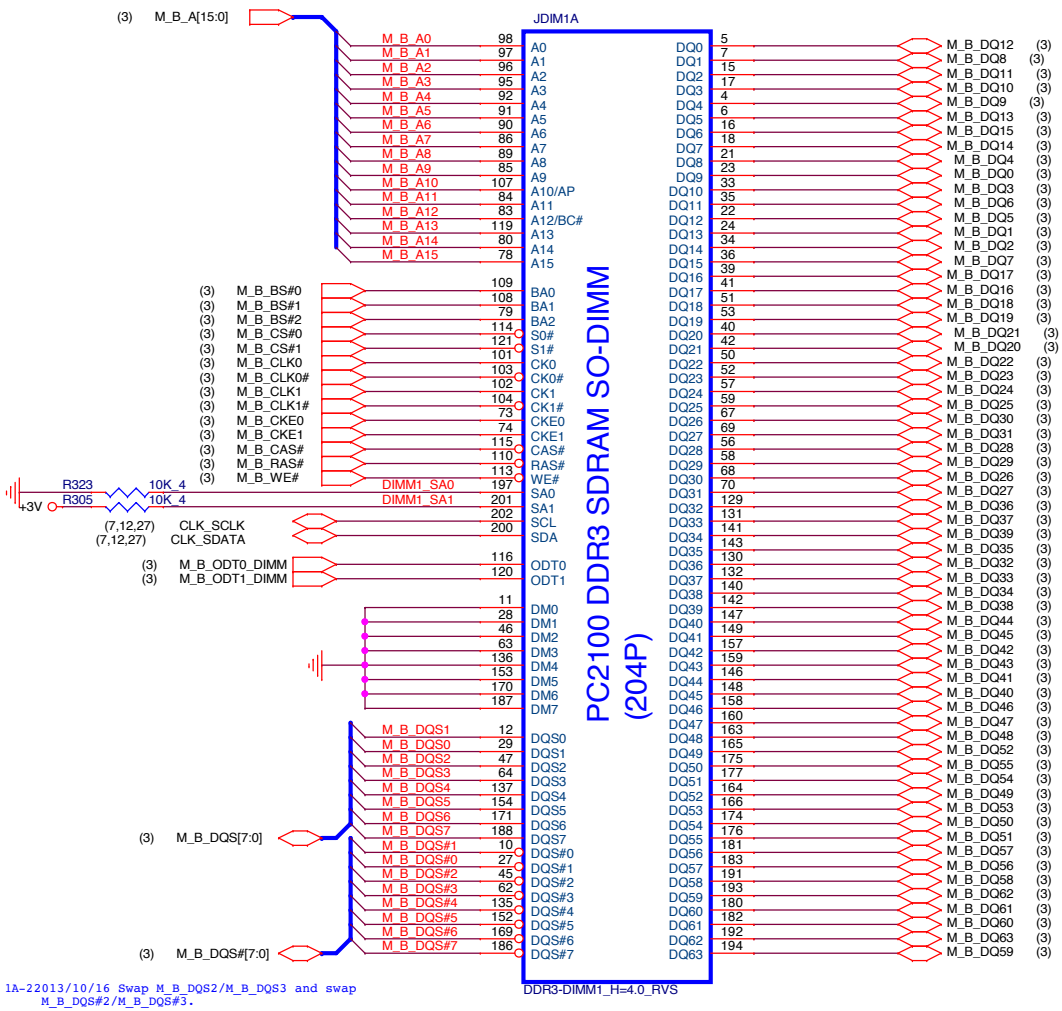
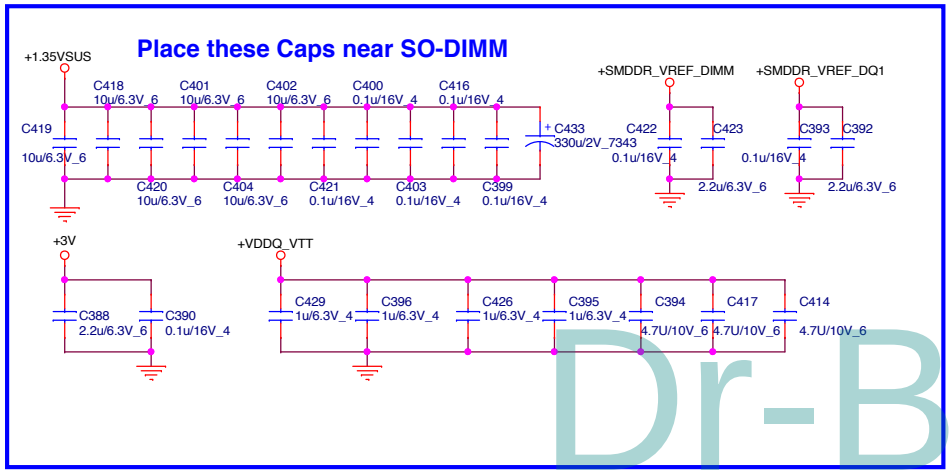
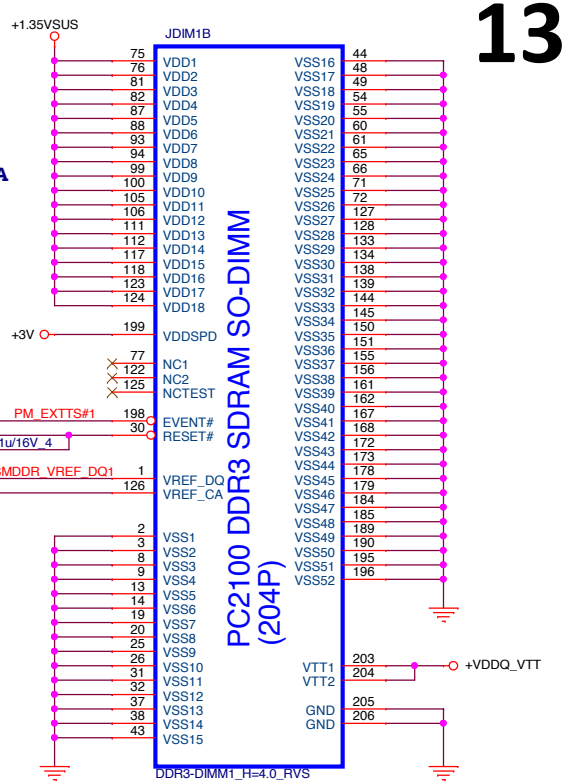
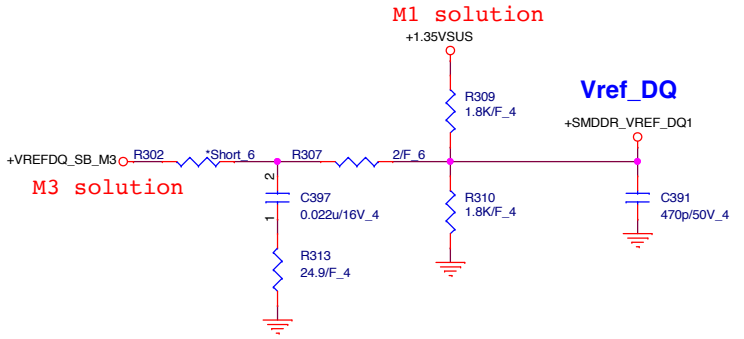


1A-22013/10/16 Swap M_B_DQS2/M_B_DQS3 and swap M_B_DQS#2/M_B_DQS#3.







	SA1	SA0
CHA	0	0
CHB	1	0

Quanta Computer Inc.

PROJECT : ZRW

Size	Document Number	Rev
	DDRIII Memory SO-DIMM B	3A
Date: Monday, July 20, 2015	Sheet 13 of 48	

PEX_IOVDD + PEX_IOVDDQ = 1.042A

PEX_PLL_HVDD + PEX_SVDD_3V3 = 143mA

PEX_PLLVDD = 130mA

NVDD = 32.22 ~ 26.66 A

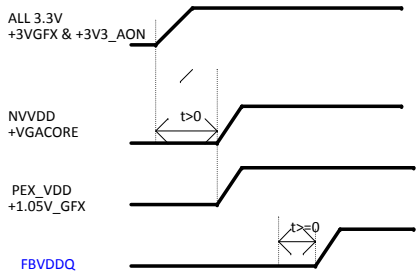
VDD33 = 56mA

100 ohm near GPU

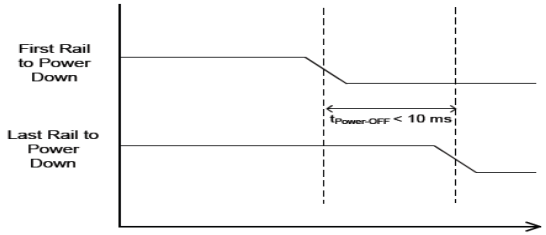
N16V stuff it, not support GC6 2.0

Follow Z09 to isolate CLK_REQ#

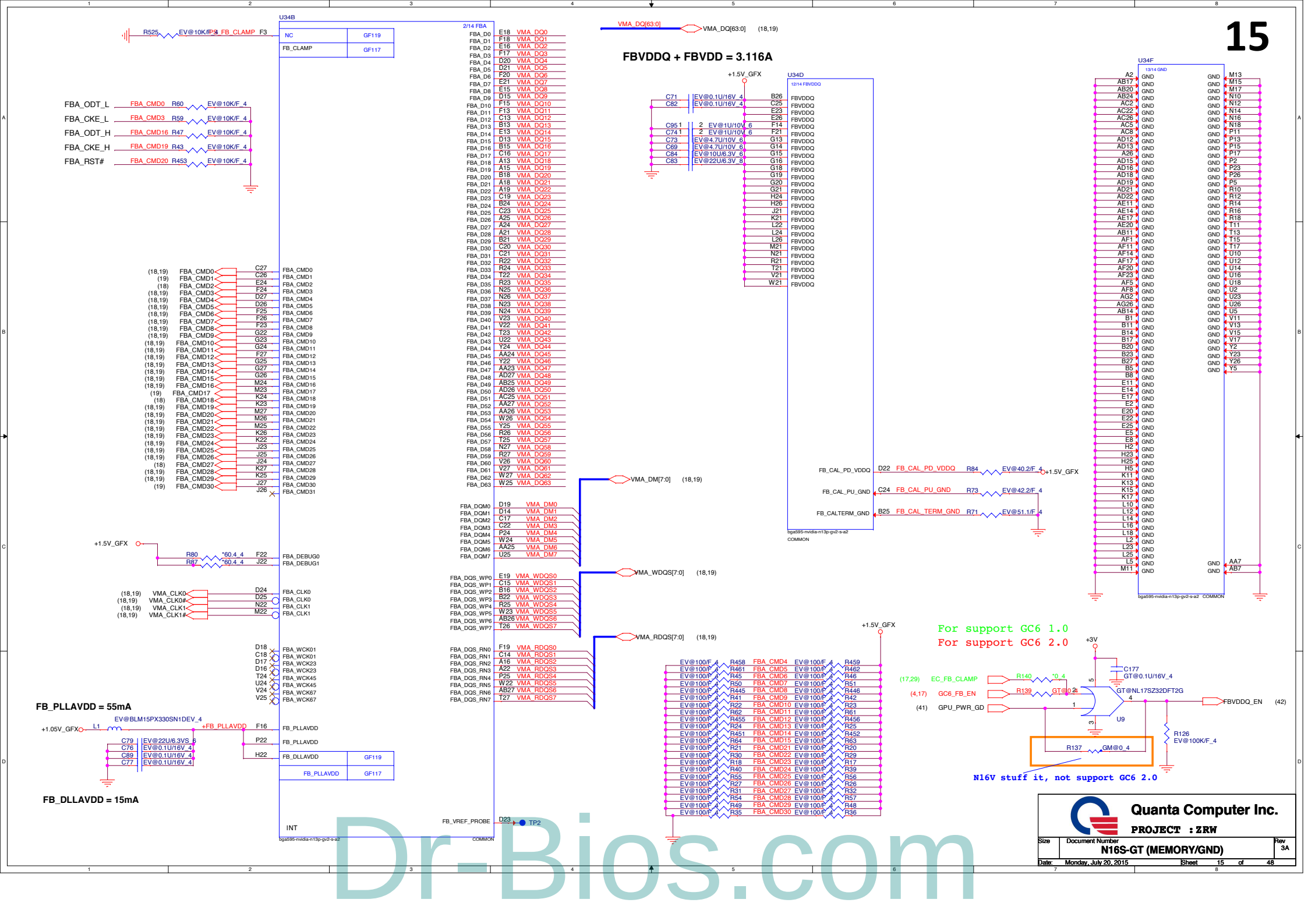
Power up sequence



Power down sequence



Quanta Computer Inc.		
PROJECT : ZRW		
Size	Document Number: N16S-GT (PCIE I/F) /NVDD	Rev: 3A
Date: Monday, July 20, 2015	Sheet 14 of 48	



Quanta Computer Inc.	PROJECT : ZRW
Size	Document Number: N16S-GT (MEMORY/GND) — Rev 3A
Date: Monday, July 20, 2015	Sheet 15 of 48

U34G 4/14 IFPAB

IFPAB

U34J 7/14 IFPEF

IFPE

IFPF

U34K 3/14 DACA

U34H 5/14 IFPC

IFPC

U34I 6/14 IFPD

IFPD

U34M 9/14 XTAL_PLL

3V MAIN POWER

GC6 Power control

3/11 GC6 timing issue from 200K change to 100K

N16V stuff not support GC6 2.0.

PLLVDD = 38mA

SP_PLLVDD = 17mA

VID_PLLVDD = 41mA

+1.05V_GFX and GPU core power EN

DB-->SI change 10/25
Use G-CLK

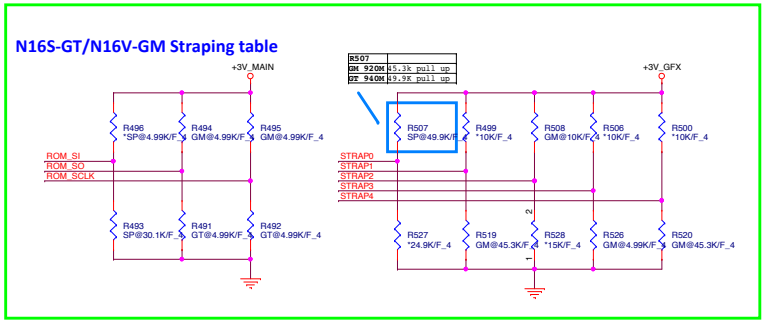
DB-->SI change 10/25
Use G-CLK

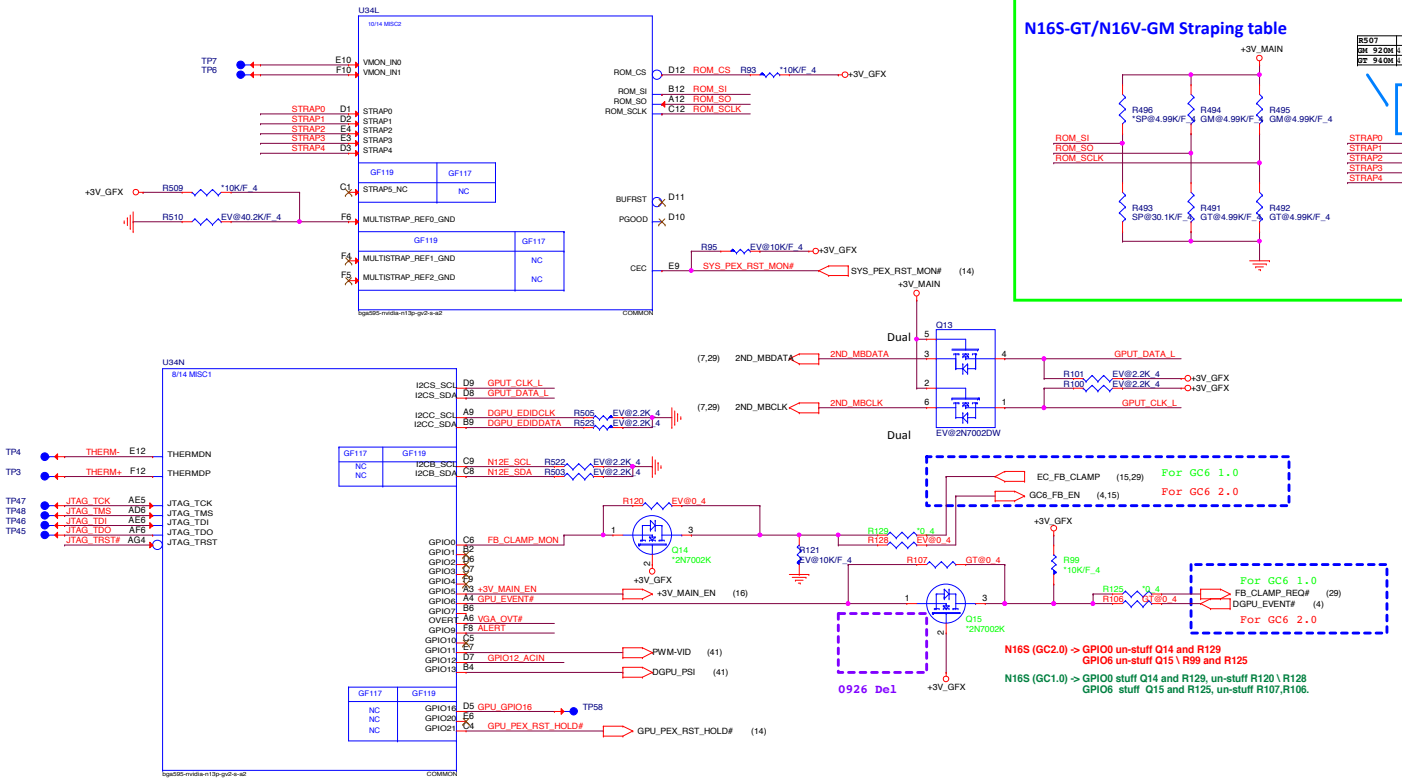
Quanta Computer Inc.

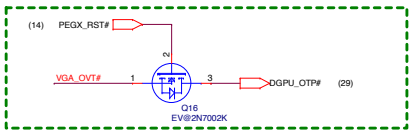
PROJECT : ZRW

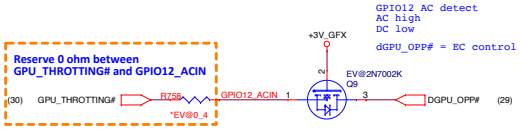
Size	Document Number	Rev
	N16S-GT (DISPLAY)	3A

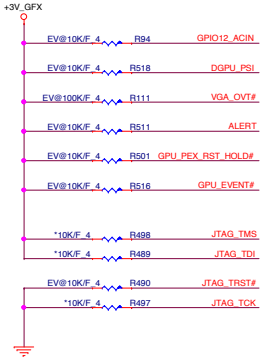
Date: Monday, July 20, 2015 Sheet 16 of 48











N16S-GT DID=0x1347 [940M]

ROM_SCLK	=	Stuff 4.99K pull down
ROM_SO	=	Stuff 4.99K pull down
STRAP0	=	Stuff 49.9K pull up
STRAP1	=	NC
STRAP2	=	NC
STRAP3	=	NC
STRAP4	=	NC
ROM_SI	=	VRAM Configuration follow below table

N16V-GM DID=0x1299 [920M]

ROM_SCLK	=	Stuff 4.99K pull up
ROM_SO	=	Stuff 4.99K pull up.
STRAP0	=	Stuff 45.3k pull up. (EDID Panel)
STRAP1	=	Stuff 45.3k pull down.(Gen3 support)
STRAP2	=	Stuff 10k pull up.(DID 0x1299)
STRAP3	=	Stuff 4.99k pull down.(No display out)
STRAP4	=	Stuff 45.3k pull down. (Gen3/max speed)
ROM_SI	=	VRAM Configuration follow below table

Note: GC6 2.0 is supported by N16x GPU in the GB2B ,GB4B-128,and GB3B-256 packages.

GPIO ASSIGNMENTS

GPIO	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor (GC6 1.0)
0	OUT	GC6_FB_EN	GC6 FB Enable (GC6 2.0)
5	OUT	+3V_MAIN_EN	Enable GC6 +3V_MAIN
6	OUT	FB_CLAMP_REQ#	Active low FB Clamp toggle request (GC6 1.0)
6	IN	DGPU_EVENT#	DGPU EVENT from CPU (GC6 2.0)
8	OUT	VGA_OVT#	ACTIVE LOW THERMAL OVER TEMP
9	OUT	ALERT	ACTIVE LOW THERMAL ALERT
11	OUT	PWR_VID	GPU CORE_VDD PWM Control signal
12	IN	PWR_DET	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding

N16S-GT/N16V-GM Straping table

ROM_SI N16S-GT [940M]
2G Hynix 128Mx16 -->34.8K PD
2G Micron 128Mx16 -->45.3K PD
2G Samsung 128Mx16 -->4.99K PU
4G Hynix 256Mx16 -->30.1K PU Single Rank
4G Hynix 256Mx16 -->24.9K PU Dual Rank
4G Micron 256Mx16 -->10K PD
4G Samsung 256Mx16 -->15K PD

ROM_SI N16V-GM [920M Single RAM]
2G Hynix 128Mx16 -->20K PD
2G Micron 128Mx16 -->30.1K PD
2G Samsung 128Mx16 -->34.8K PD
4G Micron 256Mx16 -->10K PD
4G Hynix 256Mx16 -->10K PD
4G Samsung 256Mx16 -->24.9K PD

Resistor P/N
4.99K---> CS24992FB26
10K ---> CS31002FB26
15K ---> CS31502FB24
20K ---> CS32002FB29
24.9K --->CS32492FB16
30.1K --->CS33012FB18
34.8K---> CS33482FB22
45.3K ---> CS34532FB18 GM
49.9K ---> CS34992FB10 GT

ROM_SO
N16S-GT --> 4.99K PD
N16V-GM --> 4.99K PU

ROM_SCLK
N16S-GT --> 4.99K PD
N16V-GM --> 4.99K PU

STRAP0
N16S-GT --> 49.9K PU
N16V-GM --> 45.3K PU

Logical Strap Bit Mapping

	PU-VDD	PD
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

N16S-GM/-GT/-LP VRAM Configuration Table ROM_SI

RAMCFG [3:0]	DESCRIPTION 1.5V DDR3	Vendor	Vendor P/N	ROM_SI	STN B/S	Configuration
0101 0x5	DDR3L 256Mx16, 64bit, 4Gb,1000MHz (256Mx16)	HYNIX C-die	H5TC4G63CFR-N0C	PD 30.1K ohm	AKD5PZDTW03	Single Rank 2GB
1100 0xC	DDR3L 256Mx16, 64bit, 4Gb,1000MHz	HYNIX C-die	H5TC4G63CFR-N0C	PU 24.9K ohm	AKD5PZDTW03	Dual Rank 4GB
0001 0x1	DDR3L 256Mx16, 64bit, 4Gb,1000MHz	Micron E-die	MT41J256M16HA-093G:E	PD 10K ohm	AKD5PZSTL05	Single Rank Dual Rank
0010 0x2	DDR3L 256Mx16, 64bit, 4Gb,1000MHz	SAMSUNG D-die	K4W4G1646D-BC1A	PD 15K ohm	AKD5PGWT504	Single Rank Dual Rank
0100 0x4	DDR3L 256Mx16, 64bit, 4Gb,1000MHz	SAMSUNG E-die	K4W4G1646E-BC1A	PD 24.9K ohm	AKD5PGDT504	Single Rank 2GB
1101 0xD	DDR3L 256Mx16, 64bit, 4Gb,1000MHz	SAMSUNG E-die	K4W4G1646E-BC1A	PU 30.1K ohm	AKD5PGDT504	Dual Rank 4GB

N16V-GM/GL VRAM Configuration Table ROM_SI

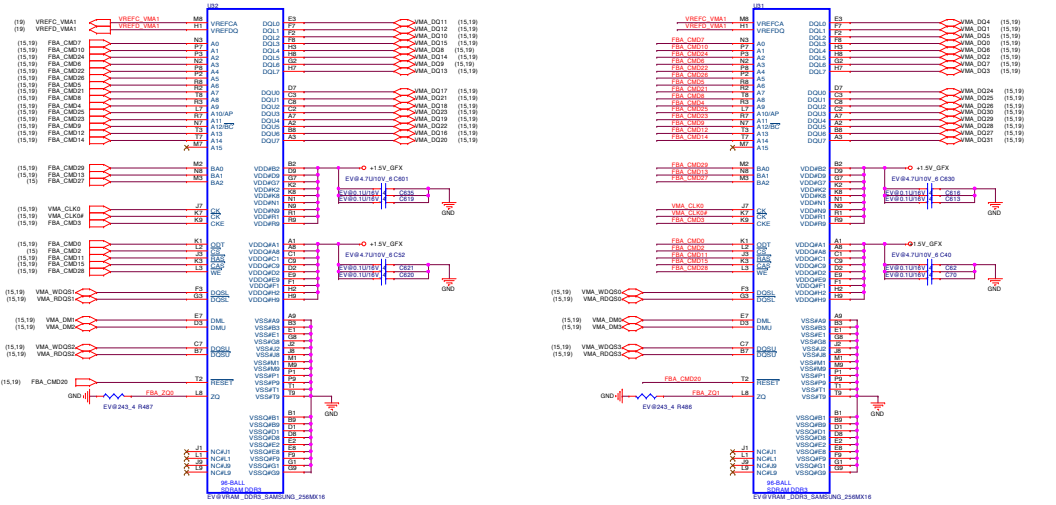
RAMCFG [3:0]	DESCRIPTION 1.5V DDR3	Vendor	Vendor P/N	ROM_SI	STN B/S	Configuration
0001 0x1	DDR3L 256Mx16, 64bit, 4Gb,1000MHz (256Mx16)	Micron E-die	MT41J256M16HA-093G:E	PD 10K ohm	AKD5PZSTL05	
1001 0x9	DDR3L 256Mx16, 64bit, 4Gb,1000MHz	HYNIX C-die	H5TC4G63CFR-N0C	PU 10K ohm	AKD5PZDTW03	Single Rank or Single Rank stuffing for Dual Rank
0100 0x4	DDR3L 256Mx16, 64bit, 4Gb,1000MHz	SAMSUNG D-die	K4W4G1646D-BC1A	PD 24.9K ohm	AKD5PGWT504	
1010 0xA	DDR3L 256Mx16, 64bit, 4Gb,1000MHz	SAMSUNG E-die	K4W4G1646E-BC1A	PU 15K ohm	AKD5PGDT504	

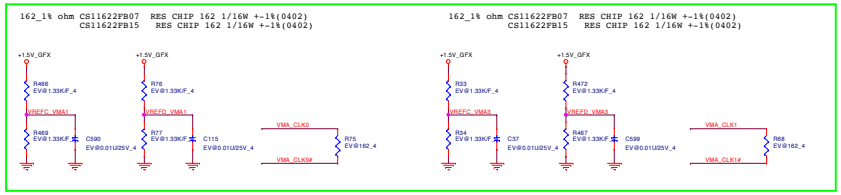
N16V-GM strap0-3 table

STRAP0 = Stuff 45.3k pull up. (EDID Panel)
STRAP1 = Stuff 45.3k pull down.(Gen3 support)
STRAP2 = Stuff 10k pull up.(DID 0x1299)
STRAP3 = Stuff 4.99k pull down.(No display out)
STRAP4 = Stuff 45.3k pull down. (Gen3/max speed)

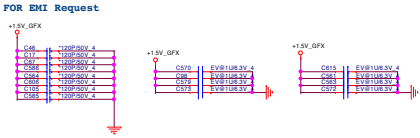
Quanta Computer Inc.
PROJECT : ZRW
Size | Document Number: N16S-GT (GPIO/STRAPS) | Rev 3A
Date: Monday, July 20, 2015 | Sheet 17 of 48

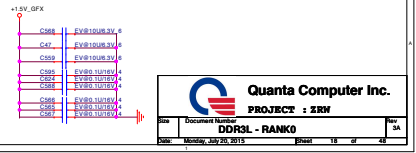
HYU 256Mx16, H5TC4G63CFR-NOC QBC PN : ---TOP B/S PN : AKD5PZDTW03
MIC 256Mx16, MT41J256M16HA-093G:E QBC PN : ---TOP B/S PN : AKD5PZSTL05
SAM 256Mx16, K4W4G1646D-BC1A QBC PN : ---TOP B/S PN : AKD5PGWT504





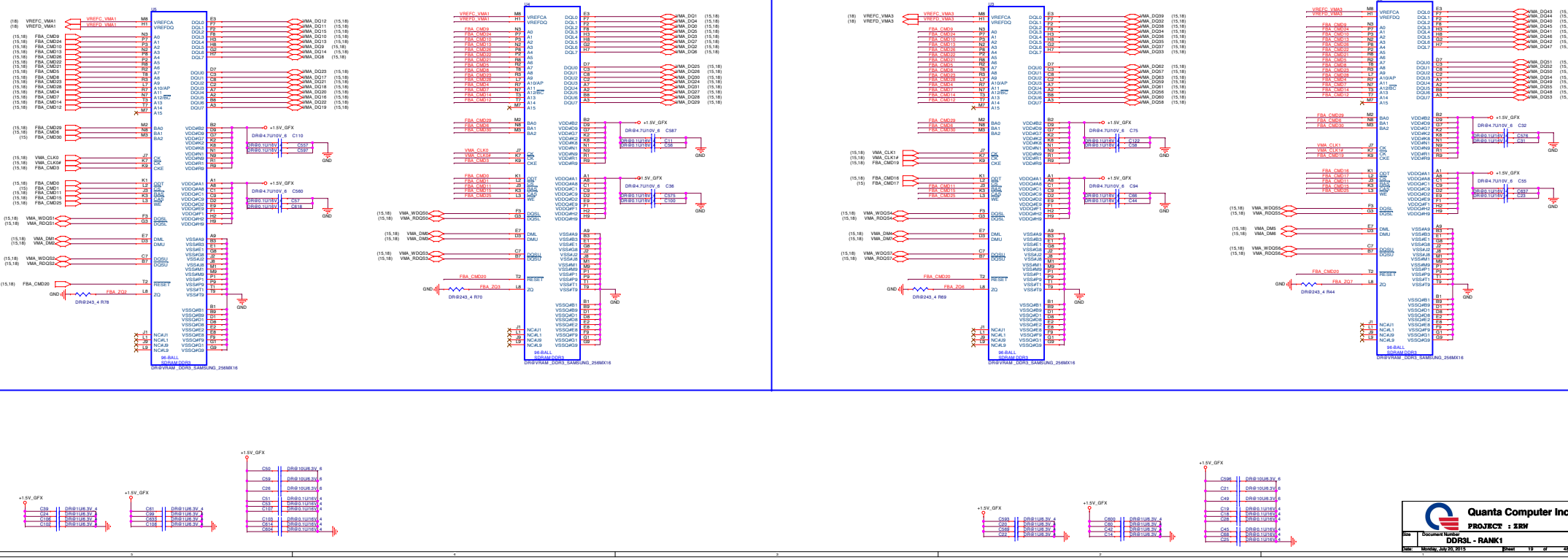
FOR EMI Request





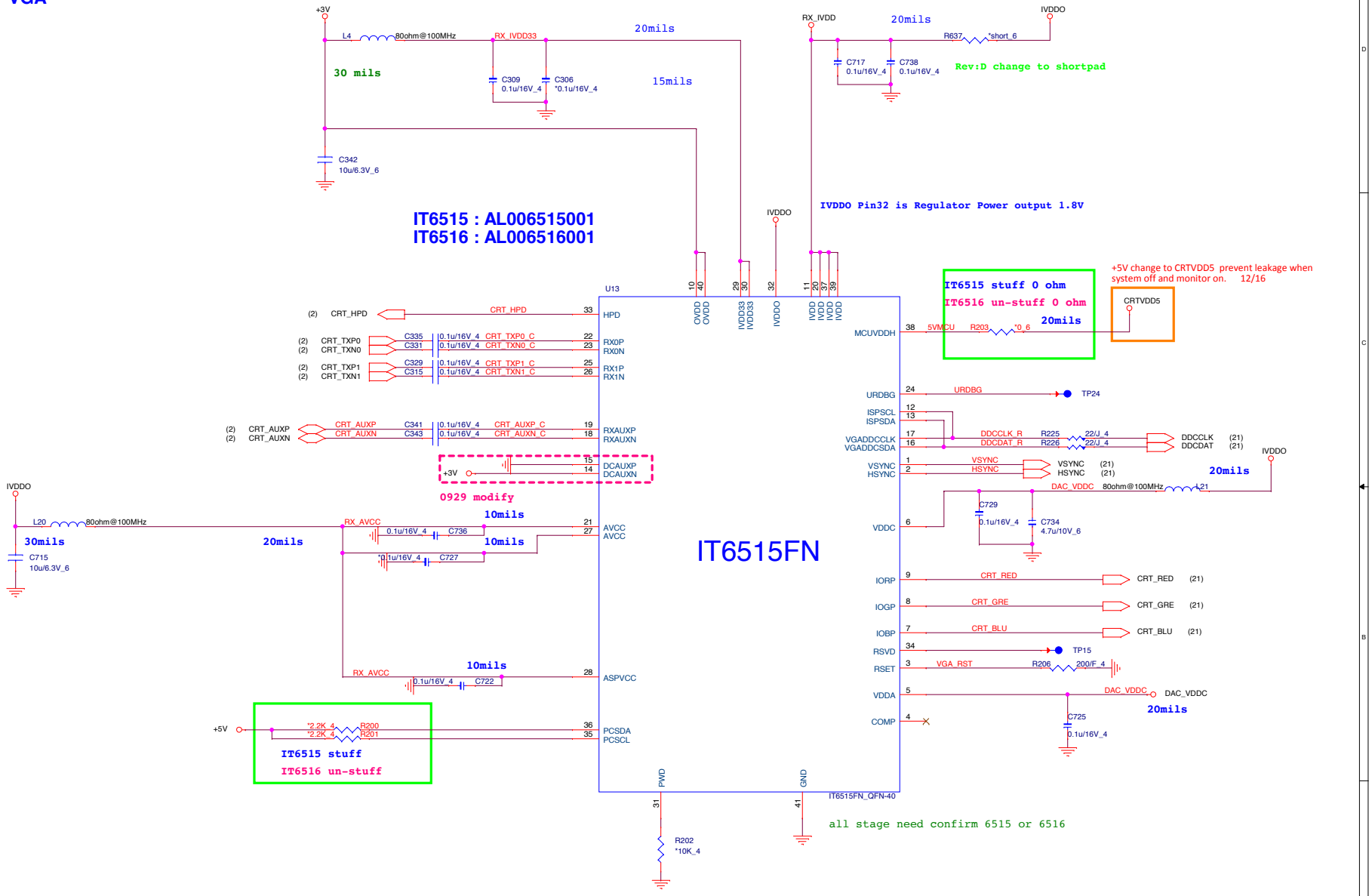
Quanta Computer Inc.
PROJECT : ZRW
Size: Document Number: DDR3L - RANK0 Rev: 3A
Date: Monday, July 20, 2015 Sheet 18 of 48

HYU 256Mx16, H5TC4G63CFR-NOC QBC PN : ---TOP B/S PN : AKD5PZDTW03
MIC 256Mx16, MT41J256M16HA-093G:E QBC PN : ---TOP B/S PN : AKD5PZSTL05
SAM 256Mx16, K4W4G1646D-BC1A QBC PN : ---TOP B/S PN : AKD5PGWT504



Quanta Computer Inc.
PROJECT : ZRW
DDR3L - RANK1
Size: Document Number: Rev: 3A
Date: Monday, July 20, 2015 Sheet 19 of 48

DP TO VGA



Quanta Computer Inc.			
PROJECT : ZRW			
Size	Document Number		Rev
	DP to VGA iT6165		3A
Date: Monday, July 20, 2015		Sheet 20 of 48	

CRT

1C-1 2014/01/10 Remove U29 and add U40 and U41.

U40 M74VHC1GT125DF2G — HSYNC → CRTHSYNC
U37 M74VHC1GT125DF2G — VSYNC → CRTVSYNC

Q21 AP2331SA-7 (+5V → CRTVDD5)

(20) CRT_RED, (20) CRT_GRE, (20) CRT_BLU
L7 BLM18BB470_6, L6 BLM18BB470_6, L5 BLM18BB470_6
CRT_R1, CRT_G1, CRT_B1
R222 75/F_4, R219 75/F_4, R213 75/F_4
C337 5.6p/16V_4, C334 5.6p/16V_4, C320 5.6p/16V_4, C319 5.6p/16V_4, C333 5.6p/16V_4, C336 5.6p/16V_4

CN7 CRT CONN
CRT_11 → TP75
DDCDAT (20)
CRTHSYNC
CRTVSYNC
DDCCLK (20)

DDCDAT 2.2K_4 R620 CRTVDD5
DDCCLK 2.2K_4 R601

U36 *RClamp0524P — CRTHSYNC, CRTVSYNC, DDCCLK
U38 *RClamp0524P — CRT_R1, CRT_G1, DDCDAT, CRT_B1

C305 *0.22u/6.3V_4
C300 *220p/50V_4
C301 0.1u/16V_4 CRTVDD5
C716 10p/50V_4 CRTVSYNC
C718 10p/50V_4 CRTHSYNC
C714 *10p/50V_4 DDCCLK
C724 *10p/50V_4 DDCDAT

Power trace tracking
(2,4,6,7,8,9,12,13,14,15,16,20,22,23,24,25,26,27,28,29,31,32,33,35,36,40,41,42) +3V
(4,20,22,24,25,27,31,40) +5V
(6,9,11,23,24,25,26,27,29,30,31,41,42) +3VPCU
(30,31,32,33,35,36,37,38,40,41,42) VIN

LCD CONNECTOR

VIN: C7 4.7u/25V_8, C9 1000p/50V_4
TP_PWR: C577 0.1u/16V_4, C578 1000p/50V_4
CCD_PWR: C27 0.1u/10V_4_X7R, C16 1000p/50V_4

1A-5
R447 *100K_4 EDP_AUX_C, R450 *100K_4 EDP_AUX#_C, R448 *100K_4, R449 *100K_4, R444 *TSI@10K_4 TP_RST#

Rev:D change to shortpad
MAX 1.5A
R15 *short_8, R14 *short_8 V_BLIGHT
C580 *1u/6.3V_4, C581 *1u/6.3V_4
R28 *short_8 LCDVCC, R11 *short_6 LCDVCC_R
R16 *short_6, R19 *short_6 TP_PWR
CCD_PWR, TP_PWR, TP_RST#

CN5 50398-04071-001

2013/12/12 change eDP pin define
colayout FHD Panel for A2 stage

Prevent ESD/EOS Layout near device
(2) EDP_HPD — R457 33_4 — C804 180P/50V_4
eDP FHD

(2) PCH_BRIGHT → PCH_BRIGHT, BL_ON
EDP_HPD_R

(2) EDP_AUXP, (2) EDP_AUXN — EDP_AUX C4 .1U/16V_4, EDP_AUX# C2 .1U/16V_4 → EDP_AUX_C, EDP_AUX#_C
(2) EDP_TXP1, (2) EDP_TXN1 — EDP_TXP1 C10 .1U/16V_4, EDP_TXN1 C8 .1U/16V_4 → EDP_TXP1_C, EDP_TXN1_C
(2) EDP_TXP0, (2) EDP_TXN0 — EDP_TXP0 C13 .1U/16V_4, EDP_TXN0 C12 .1U/16V_4 → EDP_TXP0_C, EDP_TXN0_C

Touch Panel-I2C: I2C1_SCL_C R6 *TSI@0_4, I2C1_SDA_C R5 *TSI@0_4
Touch Panel-USB: (6) USBP5+ R4 TSU@0_4, (6) USBP5- R3 TSU@0_4
CCD-USB: (6) USBP6+ R2 *short_4 USBP6+_R, (6) USBP6- R1 *short_4 USBP6-_R

Rev:D change to shortpad
(29) TS_EN — R442 *short_4 TS_EN_R
(8) Board_ID4 — R441 33_4 BOARD_ID4_TOUCH_S — TP_INT
S5
C803 180P/50V_4
Prevent ESD/EOS Layout near device

TS_EN R443 *0_4 TP_INT
1C1-2 2014/03/11 Add R698 for TS_EN short TP_INT, for issue debug.

Touch Panel interrupt
(4) TP_INT_PCH — Q1 *TSI@2N7002K — R7 *TSI@10K_4 — TP_INT
R8 *TSI@0_4
S5 S0

LCD Power

+3V → C41 1u/6.3V_4 → U1 G5243AT11U (IN, IN, ON/OFF, OUT, GND, GND) → LCDVCC
C33 *0.1u/16V_4, C29 *2.2u/10V_8, C35 0.1u/16V_4, C34 0.01u/50V_4, C30 22u/6.3V_8
(2) EDP_VDD_EN — R37 *short_8 EDP_VDD_EN_R
Rev:D change to shortpad
R38 100K_4

Touch screen level shift I2C(reserve)

+3V
R10 *TSI@0_4, R9 TSI@10K_4, R12 TSI@10K_4
Q2 *TSI@2N7002DW
(4) I2C1_SDA, (4) I2C1_SCL
I2C1_SDA_C, I2C1_SCL_C
R13 *TSI@0_4

S5
S0

TPD->100kHz,TS=400Khz
Intel design guide suggestion
MCP PIN 10u.
Per inch 3u TS=3x5inch
400kHz10-100u =2.4-0.4k.
100Khz 10-100u=9k-1k.

+3VPCU
R53 *100K_4 — LID# → (29) LID#
LID591#,EC intrnal PU
+3V
R52 10K_4, R58 10K_4
D1 1N4148WS
BL#, BL_ON
(2) PCH_BLON — R67 *short_4 PCH_BLON_R
(29) PCH_BLON_EC — R66 *short_4
R65 100K_4
Q3 2N7002DW
Q4 DTC144EUA → EC_FPBACK# (29)
Rev:D change to shortpad
1B-3 2013/12/10 change Q3.3 from +3V to +3VPCU.

Hall Sensor (HSR)

+3VPCU
Rev:D change to shortpad
R435 *100K_4
R434 *short_6
D28 *VPORT_6
C556 4.7U/10V_6
MR1 AH9249NTR-G1
D23 *VPORT_6
LID#

1st:AL009249000 -- BCD
2nd:AL009132001 -- ANC

Quanta Computer Inc.
PROJECT : ZRW
Size | Document Number: CRT/LVDS/CAMERA/LID | Rev 3A
Date: Monday, July 20, 2015 | Sheet 21 of 48

HDMI

<HDM>

22

From PCH

2/16 FAE confirmed stuff

2/16 FAE confirmed don't stuff

HDMI connector

HDMI-detect

EMI

260mA (30mils)

PS8201ATQFN40GTR2-A0

AL008201003 PS8201ATQFN40GTR2-A0 REV:E Change

DDS AL002331000

	Pre	ISET	EQ	CFG	DDCBUF	DCIN_EN
NC(Low)	0 dB	default	12.4 dB	HDMI ID disable	default	default,AC coupling input
1(High)	1.6 dB	+13%	4.3 dB	HDMI ID enable	active DDC buffer with default threshold	DC coupling input
M	2.5 dB	-13%	8.6 dB	N/A	active DDC buffer without internal pull up resistor	N/A

Pre	Output pre-emphasis setting
ISET	TMDS output swing adjustment
EQ	Receiver equalization setting
CFG	Configuration pin
DDCBUF	enable active DDC buffer
DCIN_EN	DC coupling enable

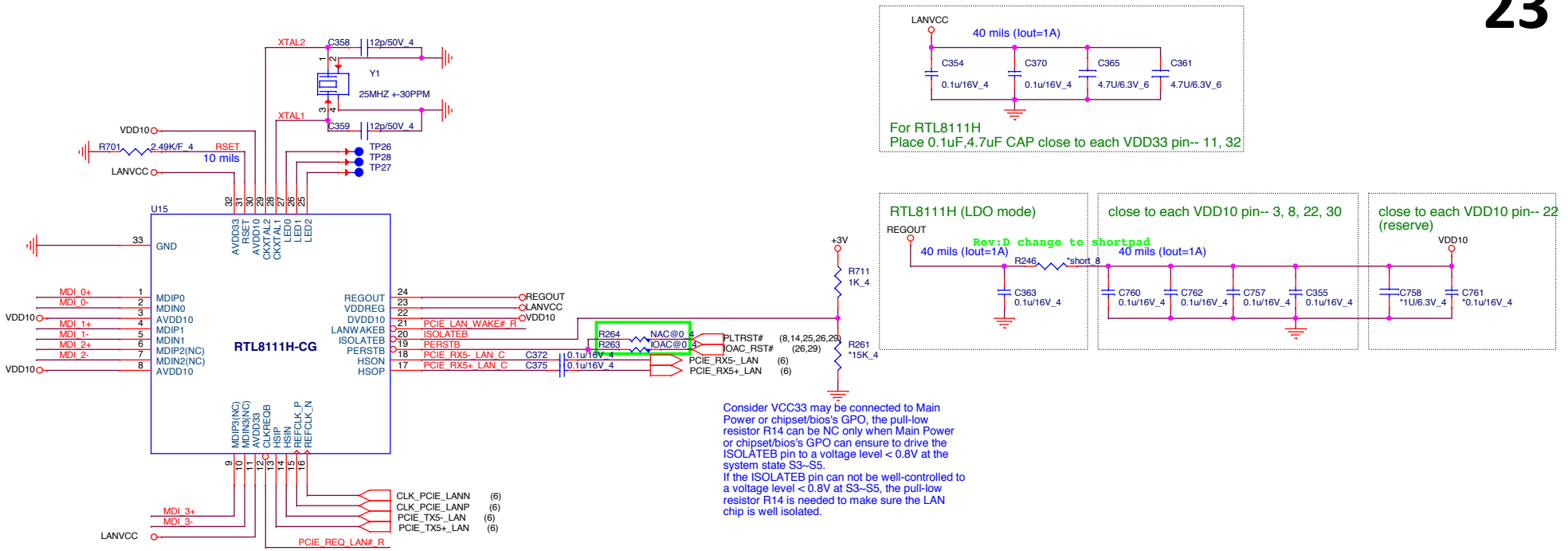
Pin	PS8401A	PS8201A
12	VDDRX	NC
15	GND	NC
34	ISET	NC
37	VDD33	NC

Power trace tracking

(2,4,6,7,8,9,12,13,14,15,16,20,21,23,24,25,26,27,28,29,31,32,33,35,36,40,41,42) +3V
(4,20,21,24,25,27,31,40) +5V

Quanta Computer Inc.
PROJECT : ZRW
Size | Document Number | Rev 3A
HDMI (PS8201 4k*2k)
Date: Monday, July 20, 2015 Sheet 22 of 48

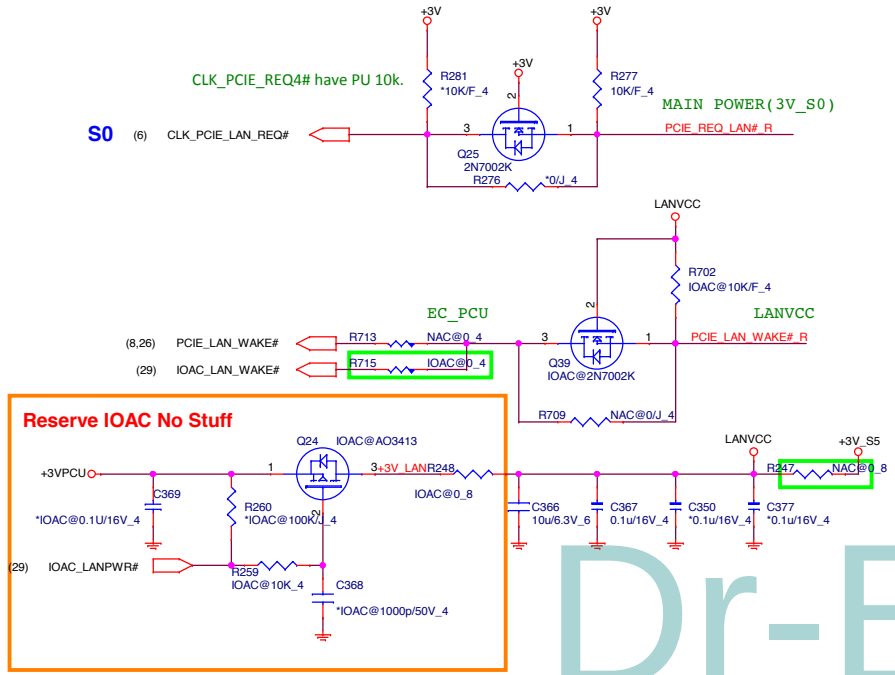
Giga LAN (LAN)



Consider VCC33 may be connected to Main Power or chipset/bios's GPO, the pull-low resistor R14 can be NC only when Main Power or chipset/bios's GPO can ensure to drive the ISOLATEB pin to a voltage level < 0.8V at the system state S3~S5.
If the ISOLATEB pin can not be well-controlled to a voltage level < 0.8V at S3~S5, the pull-low resistor R14 is needed to make sure the LAN chip is well isolated.

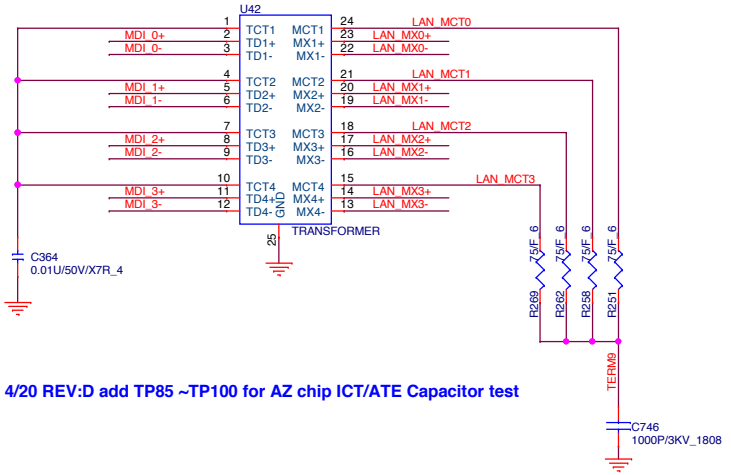
For RTL8111H
Place 0.1uF,4.7uF CAP close to each VDD33 pin-- 11, 32

Leakage circuit (MPC)



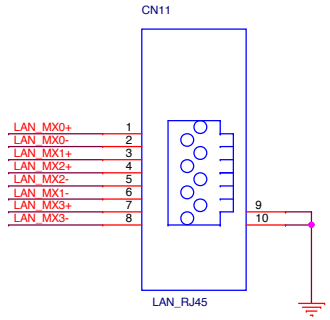
Tramsformer

Layout:All termination signal should have 30 mil trace



4/20 REV:D add TP85 ~TP100 for AZ chip ICT/ATE Capacitor test

RJ45 Connector



Quanta Computer Inc.
PROJECT : ZRW

Size	Document Number	Rev
	LAN(RTL8111H)	3A
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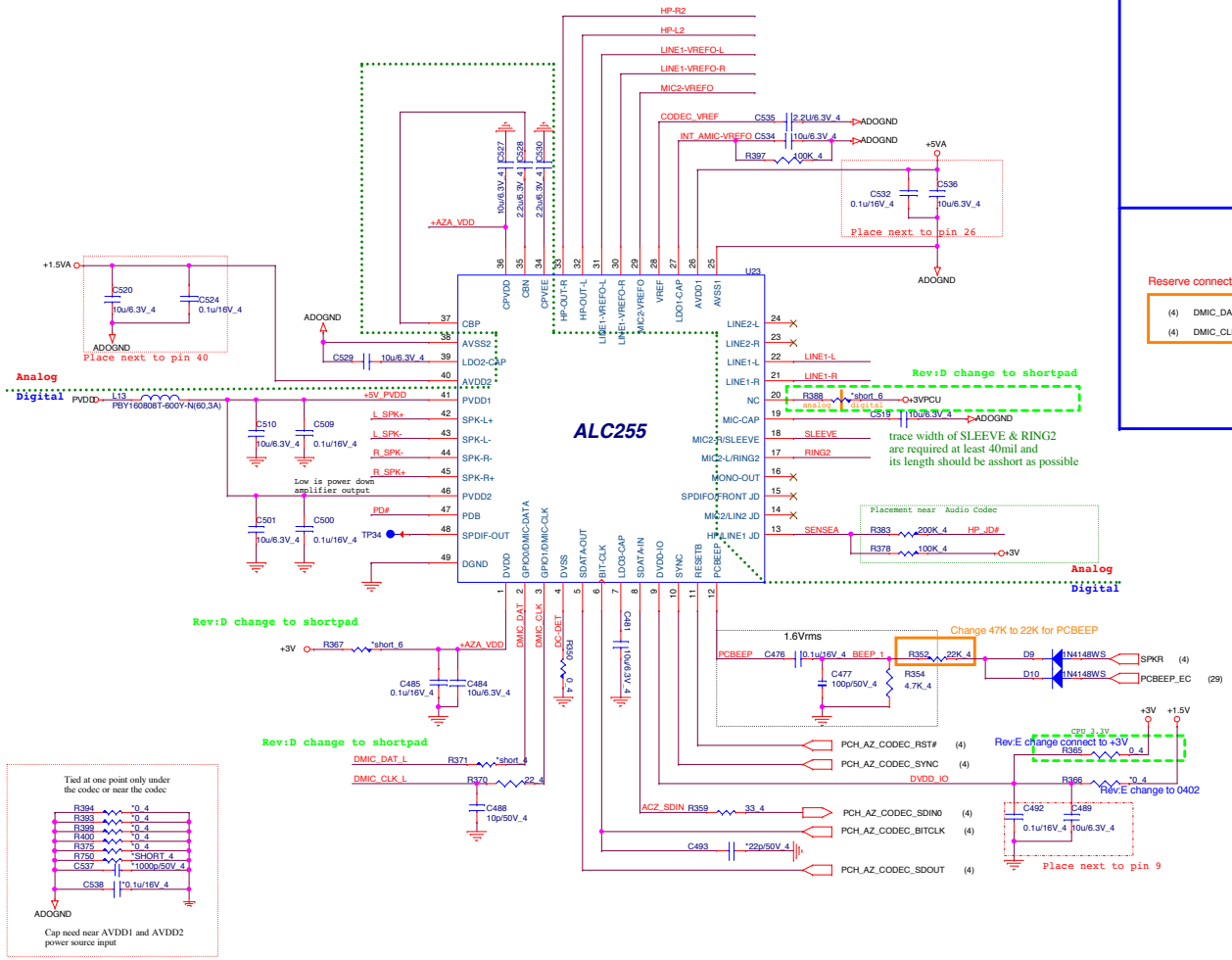
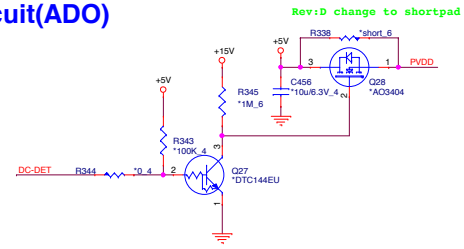
Codec(ADO)

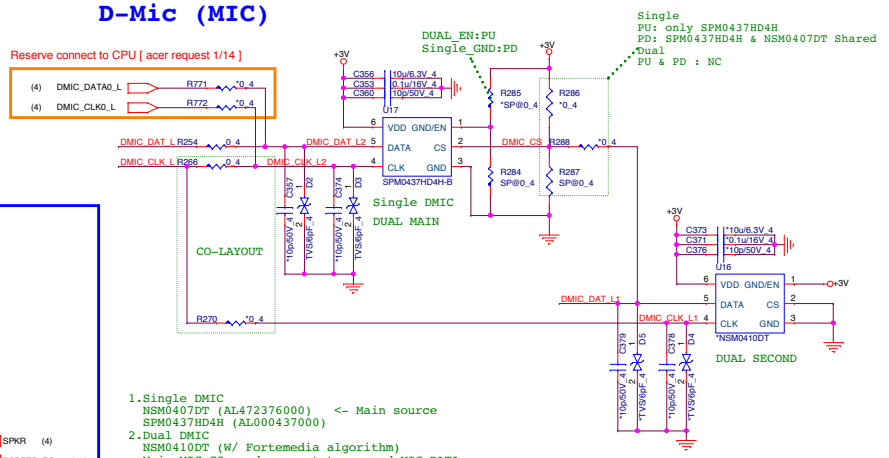


DC-DET circuit(ADO)

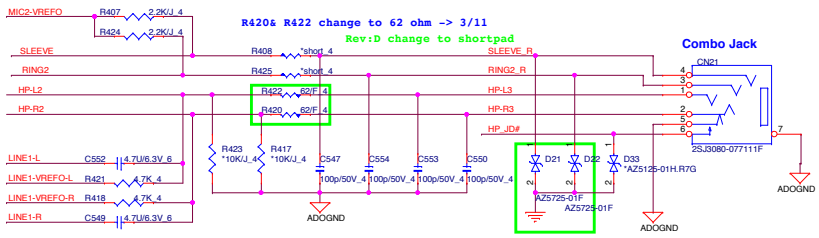


24

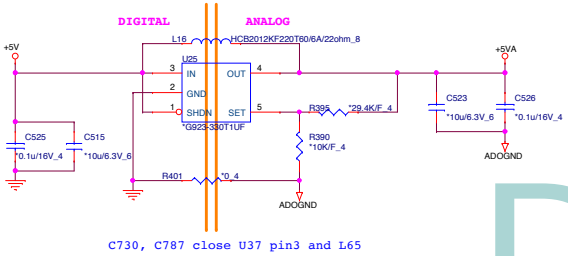
D-Mic (MIC)



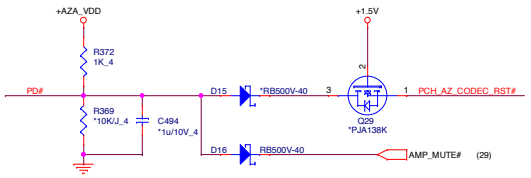
Universal Audio Jack HEADPHONE/MIC/LINE combo (ADO)



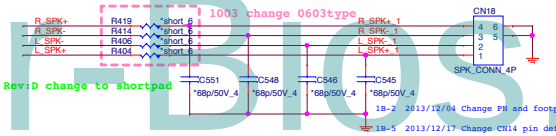
Codec PWR 5V(ADO)



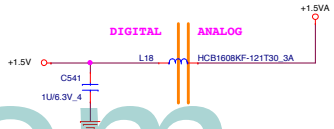
Mute(ADO)



Internal Speaker



Codec PWR 1.5V(ADO)



Quanta Computer Inc.
PROJECT : ZRW

Size	Document Number	Rev
	ALC255/HP/SPK	3A
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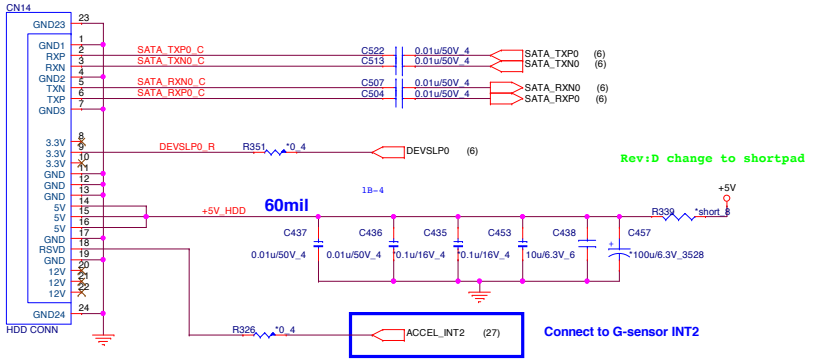
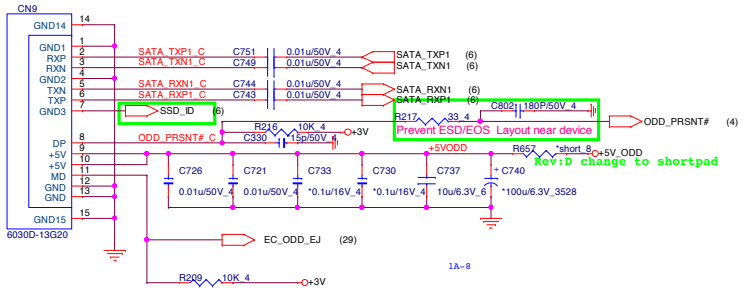
2.5" SATA HDD (HDD)

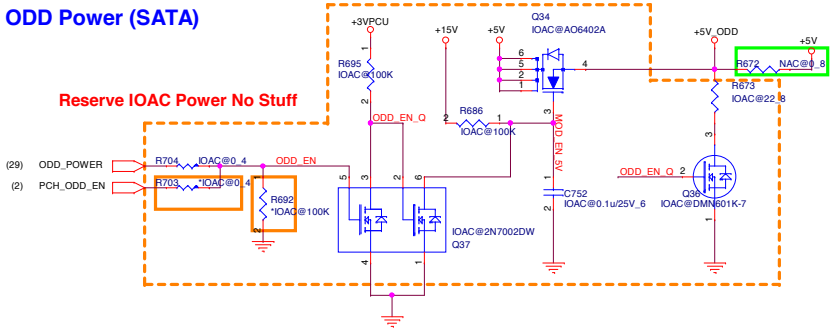


SATA ODD Connector



25

ODD Power (SATA)



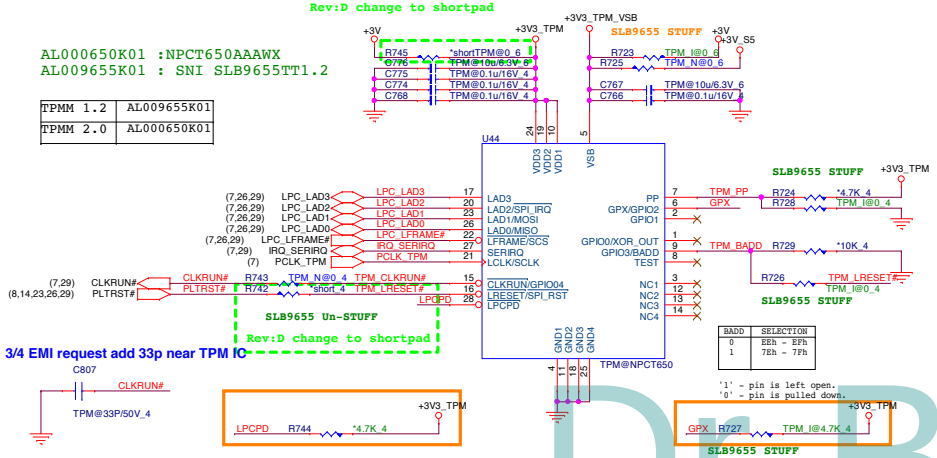
TPM NPCT650 (TPM)

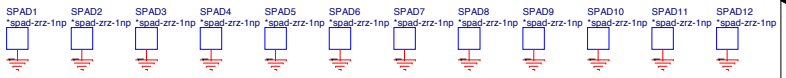
SP@ BOM周邊上NPCT650
A,B,C P/N:AL009655K01(SLB9655TT1.2- FW4.31)
RAMP P/N: AL000650K01 (NPCT650AAAWX)

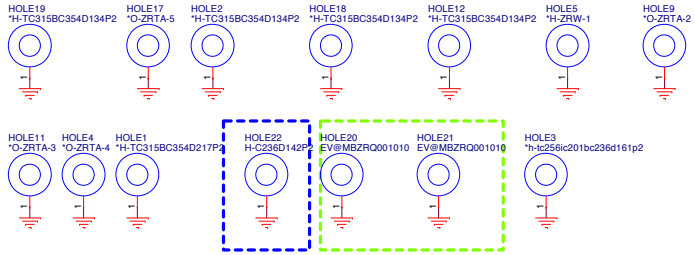
Rev:D change to shortpad

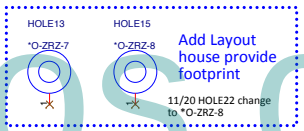
AL000650K01 :NPCT650AAAWX
AL009655K01 : SNI SLB9655TT1.2

TPMM 1.2	AL009655K01
TPMM 2.0	AL000650K01









Quanta Computer Inc.
PROJECT : ZRW

Size	Document Number	Rev
	HDD/ODD/TPM NPCT650	3A

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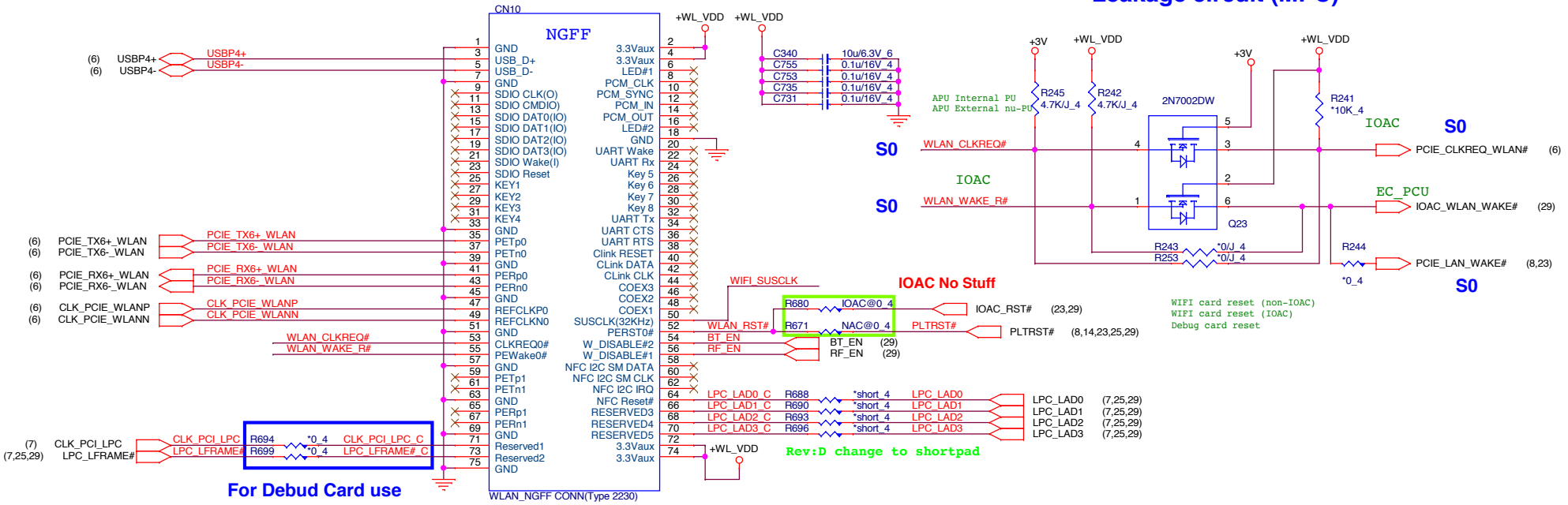
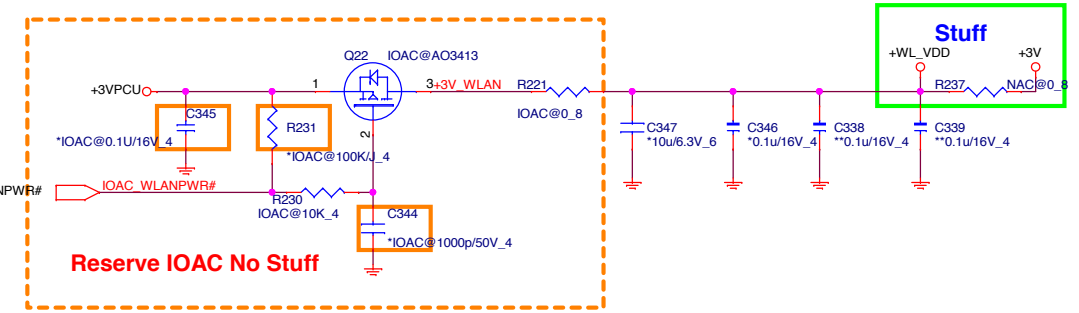
NGFF_M.2 WiFi & BT (NGF)

+3VPCU (6,9,11,21,23,24,25,27,30,31,41,42)
+1.5V (9,22,24,40)
+3V (2,4,6,7,8,9,12,13,14,15,16,21,22,23,24,25,27,28,31,32,35,36,40,41,42)

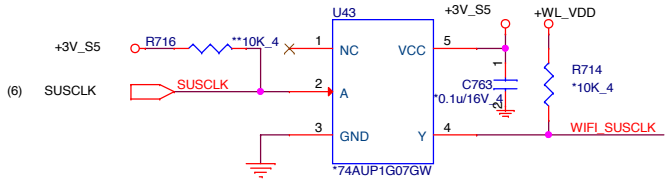
Leakage circuit (MPC)

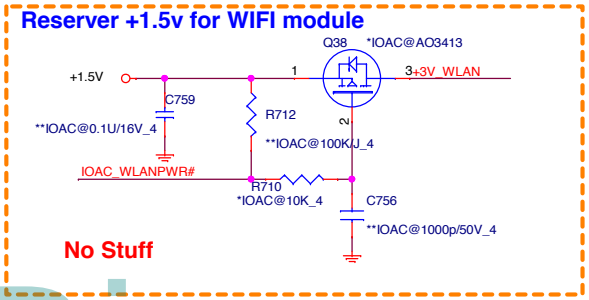


Low	Mini card +3V power enable
High	Mini card +3V power disable



Reserve only for Intel module no need to stuff by default 11/24





Quanta Computer Inc.
PROJECT : ZRW
Size | Document Number: Mini-Card/WL/3G/SIM | Rev: 3A
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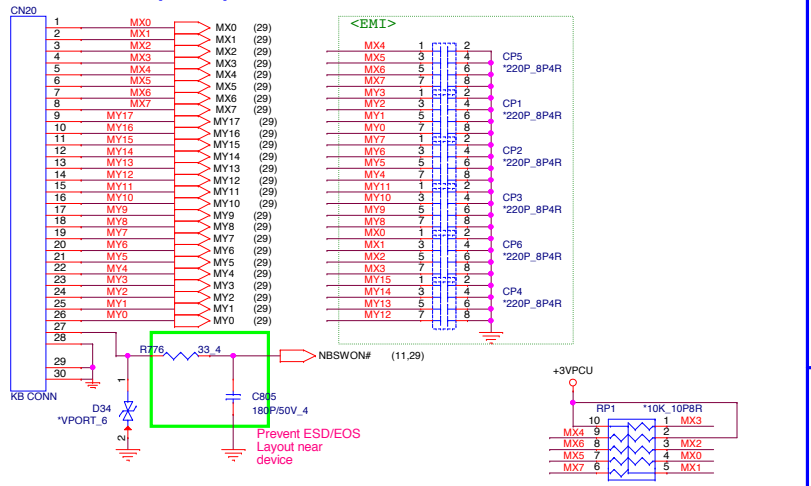
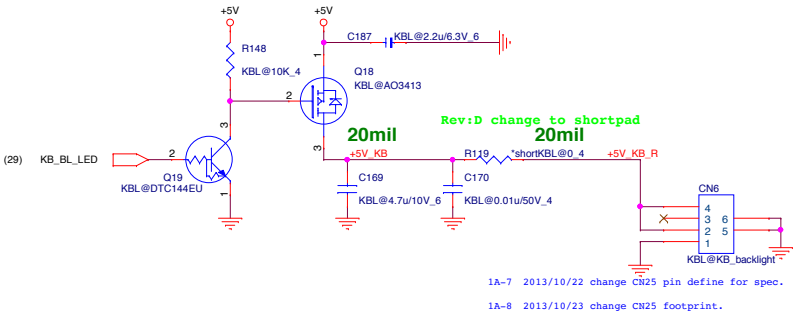
KEYBOARD (KBC)

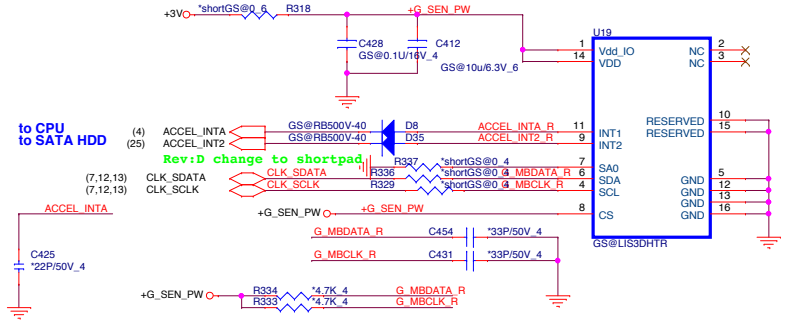


KB_BL LED (KBC)



G-sensor(ACS)

Rev:D change to shortpad

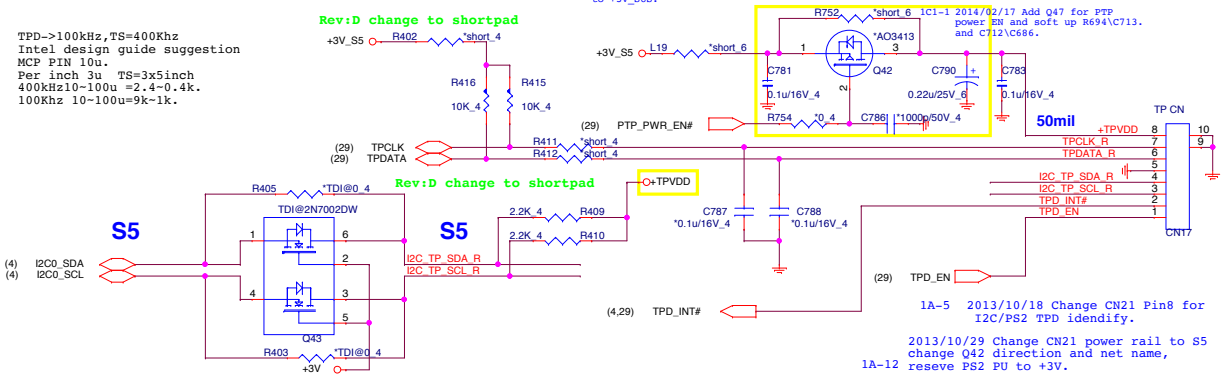


TOUCHPAD BOARD CONN (TPD I2C/PS2 co-lay)

Rev:D change to shortpad

1C-2 2014/01/13 Change TP power rail from +3V_S5 to +3V_SUS.
1C-4 2014/01/15 reserve TP power rail +3V_S5.

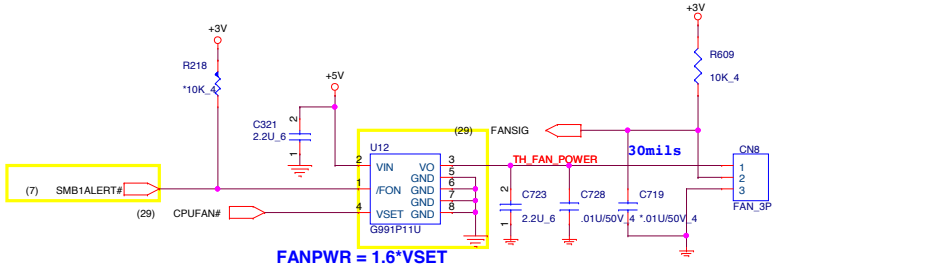
TPD->100kHz,TS=400Khz
Intel design guide suggestion
MCP PIN 10u.
Per inch 3u TS=3x5inch
400kHz10~100u =2.4~0.4k.
100kHz 10~100u=9k~1k.



1A-5 2013/10/18 Change CN21 Pin8 for I2C/PS2 TPD idendify.

2013/10/29 Change CN21 power rail to S5 change Q42 direction and net name,
1A-12 reseve PS2 PU to +3V.

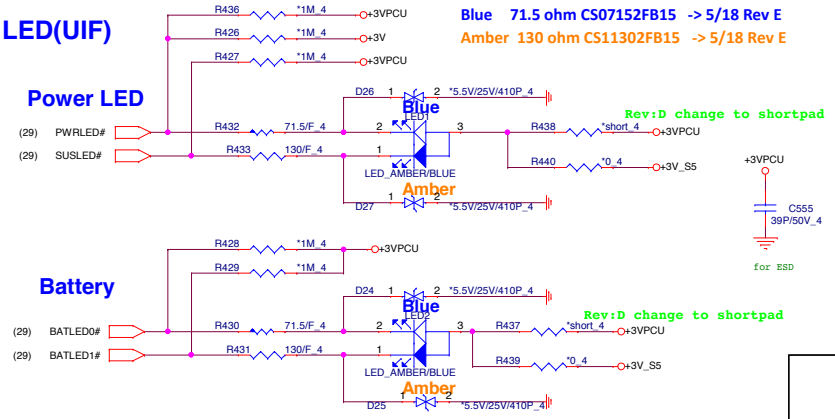
CPU FAN (THM)



1A-1 2013/10/15 change pin define and add pwm IC U17.
1A-4 2013/10/17 Change U17 to G991P11U and PU U17 pin1.
1A-9 2013/10/24 Add alert on U17.1 for CPU themal tempture.
1A-13 2013/10/31CN15 Pin2/3 swap.

POWER LED(UIF)

Blue 71.5 ohm CS07152FB15 -> 5/18 Rev E
Amber 130 ohm CS11302FB15 -> 5/18 Rev E



Quanta Computer Inc.
PROJECT : ZRW

Size	Document Number	Rev
	KB/TP/FAN	3A
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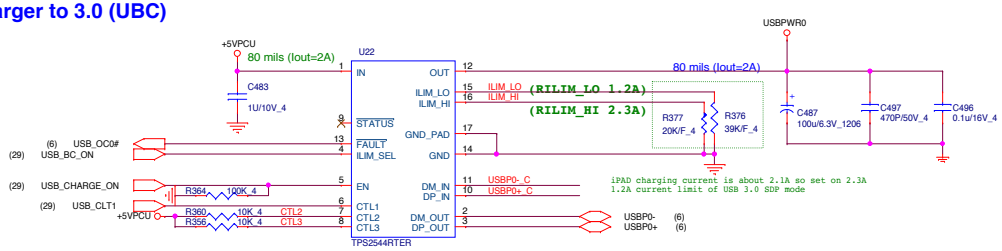
USB Charger to 3.0 (UBC)



	CTL1	CTL2	CTL3	ILIM_SEL
SDP	1	1	1	0
CDP	1	1	1	1
DCP	0	1	1	X

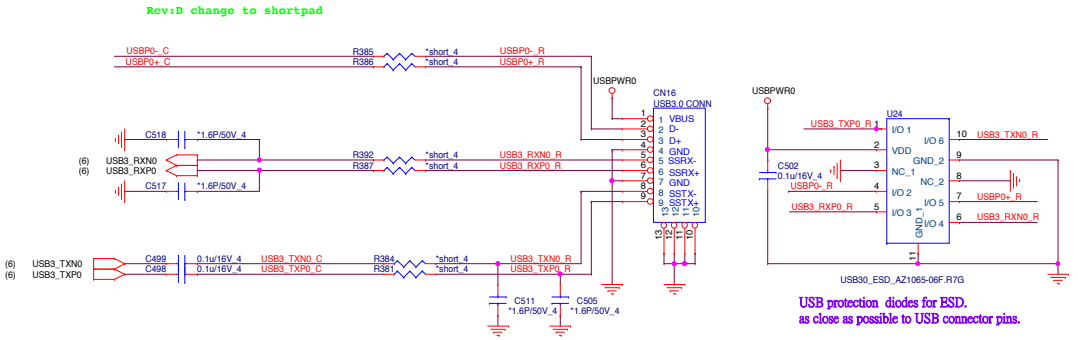
RILIM_LO is optional and the ILIM_LO pin may be left unconnected if the following conditions are met:
1. ILIM_SEL is always set high
2. Load Detection - Port Power Management is not used
3. Mouse / Keyboard wake function is not used
If conditions 1 and 2 are met but the mouse / keyboard wake function is also desired, it is recommended to use RILIM_LO < 80.6 kΩ.
The following equation programs the typical current limit:
(1)
RILIM_XX corresponds to either RILIM_HI or RILIM_LO as appropriate.

$$IOS\_typ(mA) = 50{,}250/\{RILIM\_XX(K\Omega)+0.1\}$$

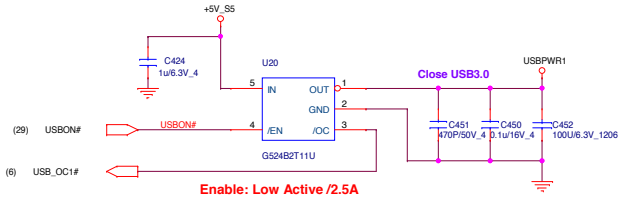
GMT:AL003703000(G3703)
TI:AL002544001(TPS2544)
Silergy: AL055544000 (SLGC55544VTR)

USB 3.0 Connector (UB3)

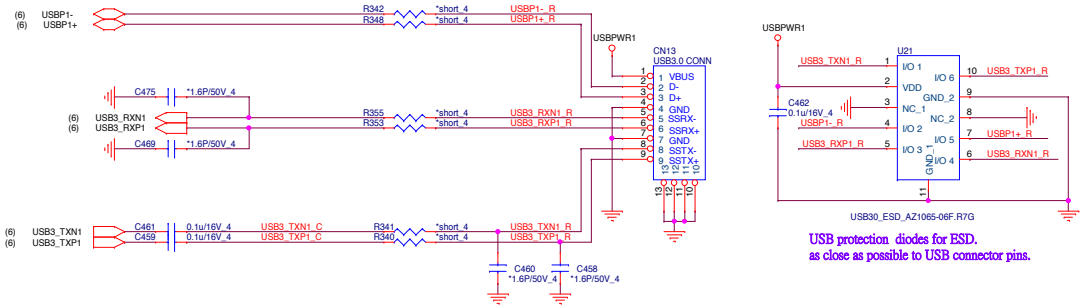
Rev:D change to shortpad



USB protection diodes for ESD.
as close as possible to USB connector pins.

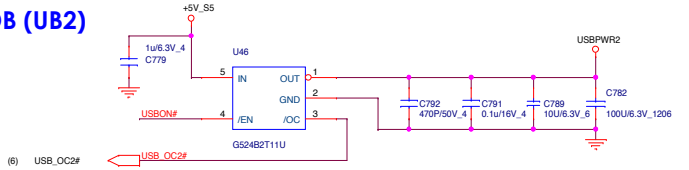


Enable: Low Active /2.5A
BCD:AL002822000
GMT:AL000524007

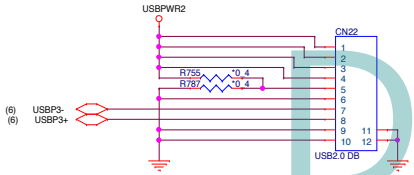


USB protection diodes for ESD.
as close as possible to USB connector pins.

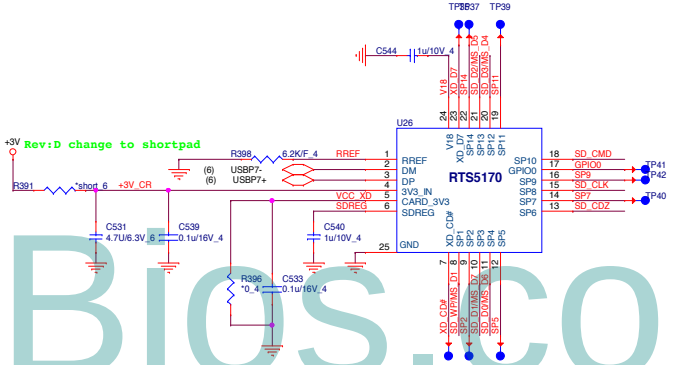
USB2.0 DB (UB2)

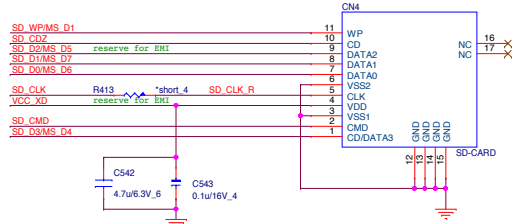


Enable: Low Active /2.5A
BCD:AL002822000
GMT:AL000524007



Card Reader (CRD)



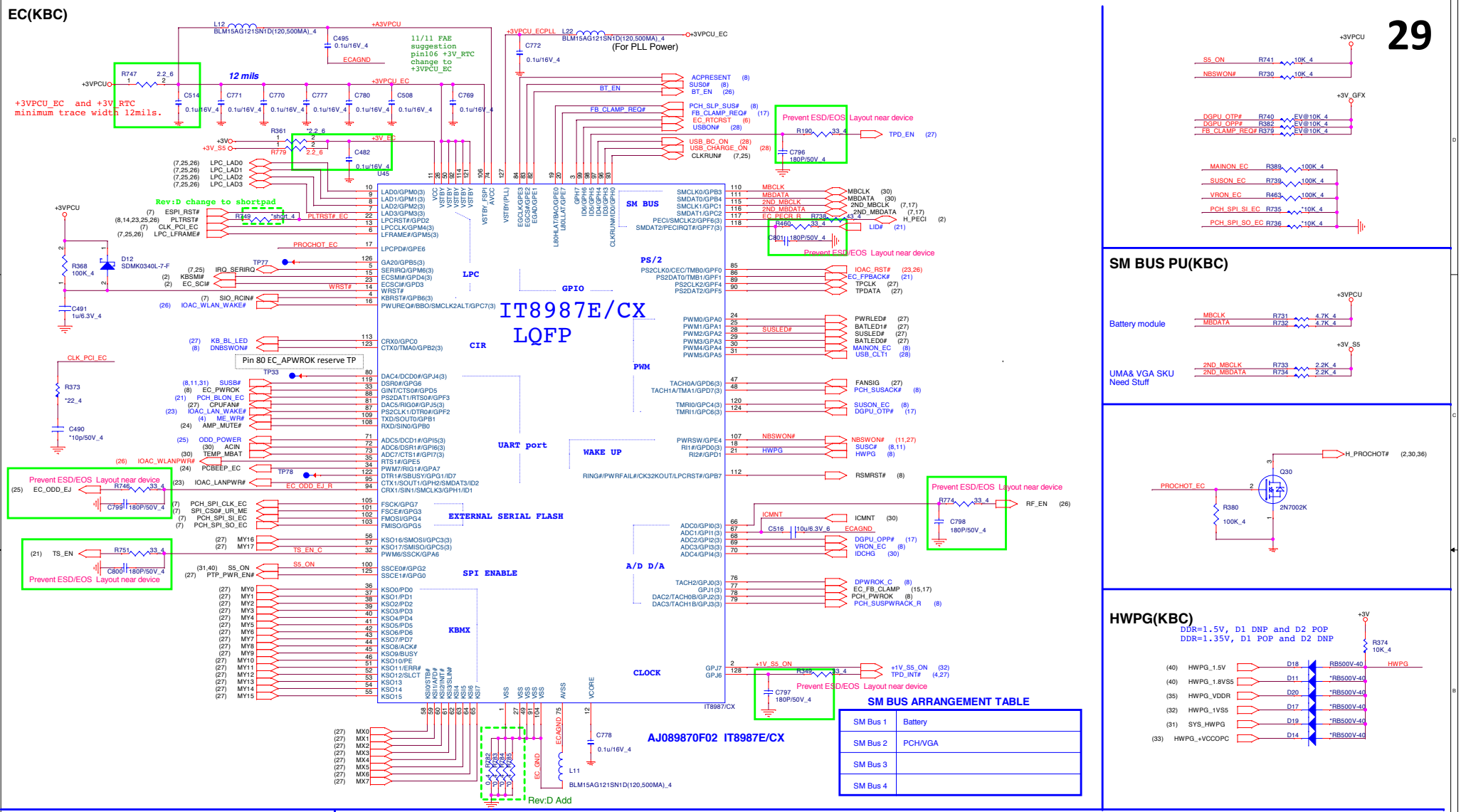


Rev:D change to shortpad

Quanta Computer Inc.
PROJECT : ZRW

Size	Document Number	Rev
	USB3/Charger/CR/USB2 DB	3A
Date: Monday, July 20, 2015	Sheet 28 of 48	

EC(KBC)



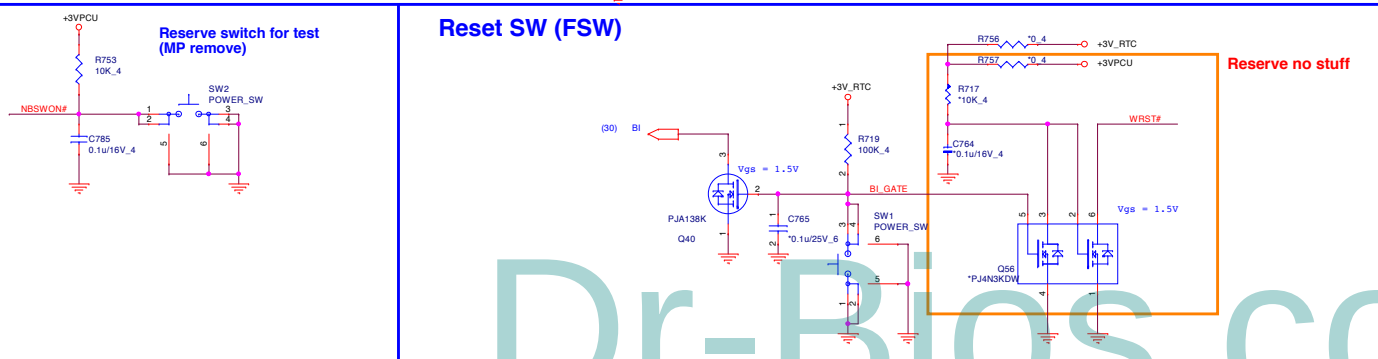
SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH/VGA
SM Bus 3	
SM Bus 4	

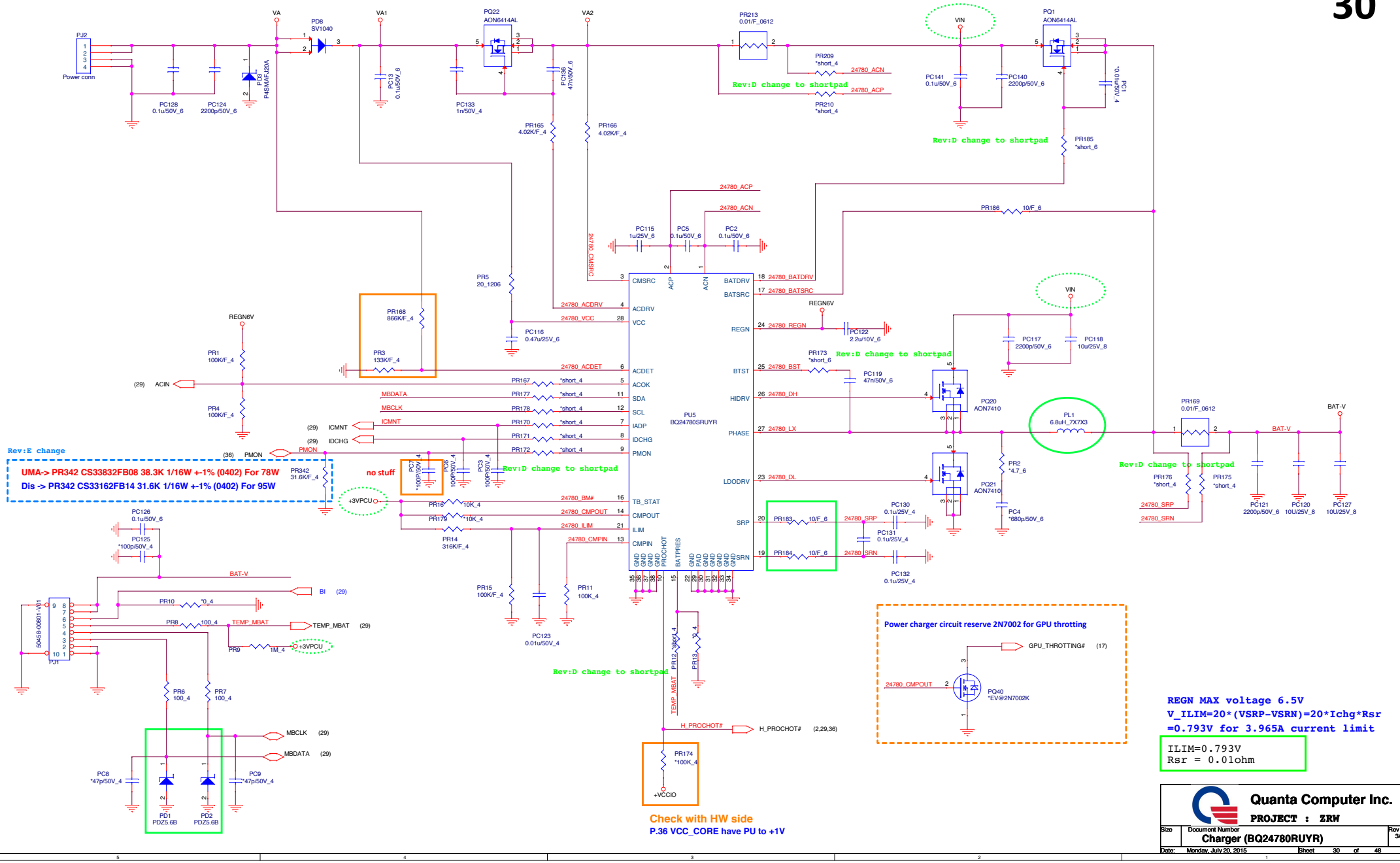
SM BUS PU(KBC)

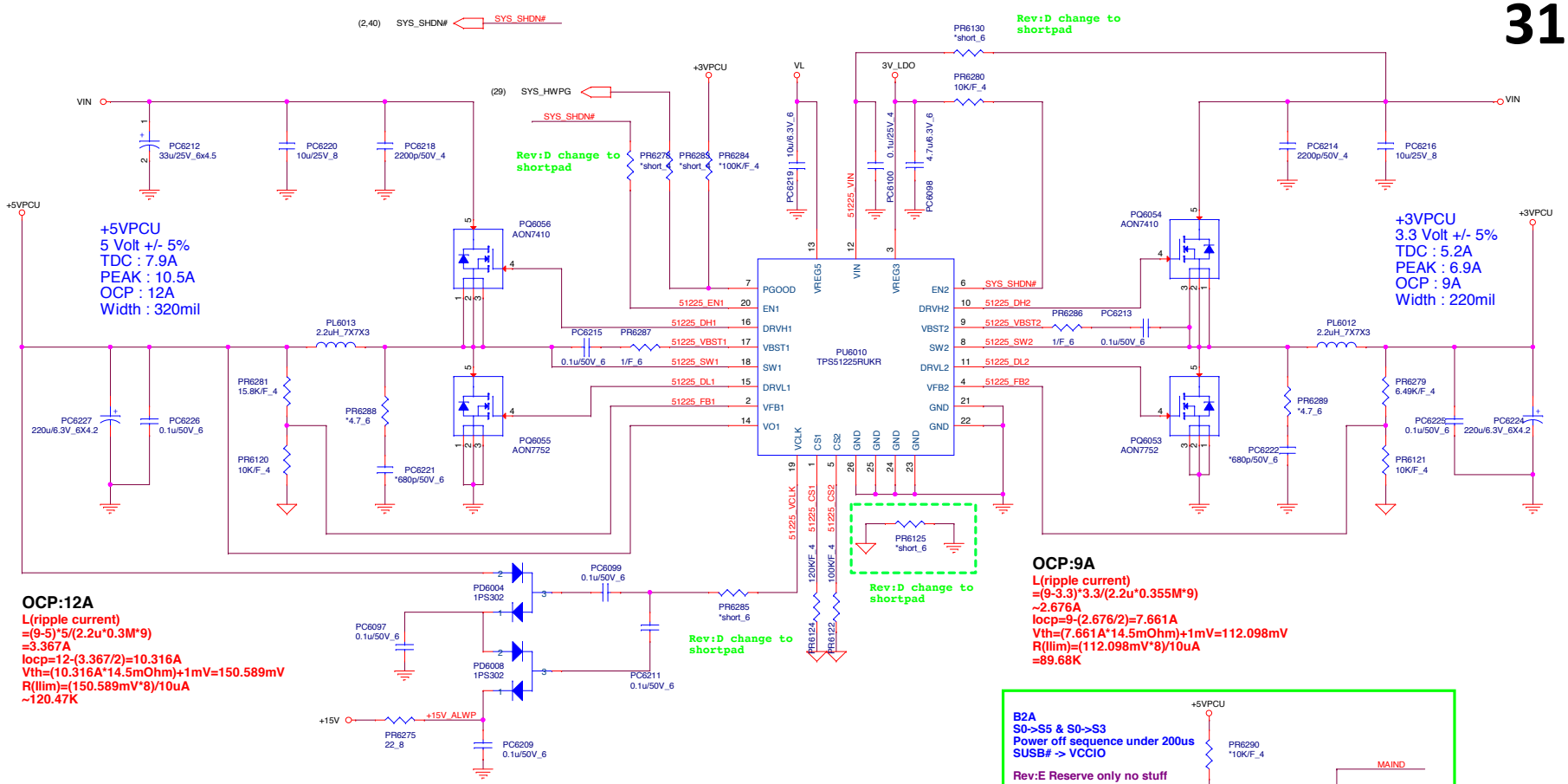
HWPG(KBC)

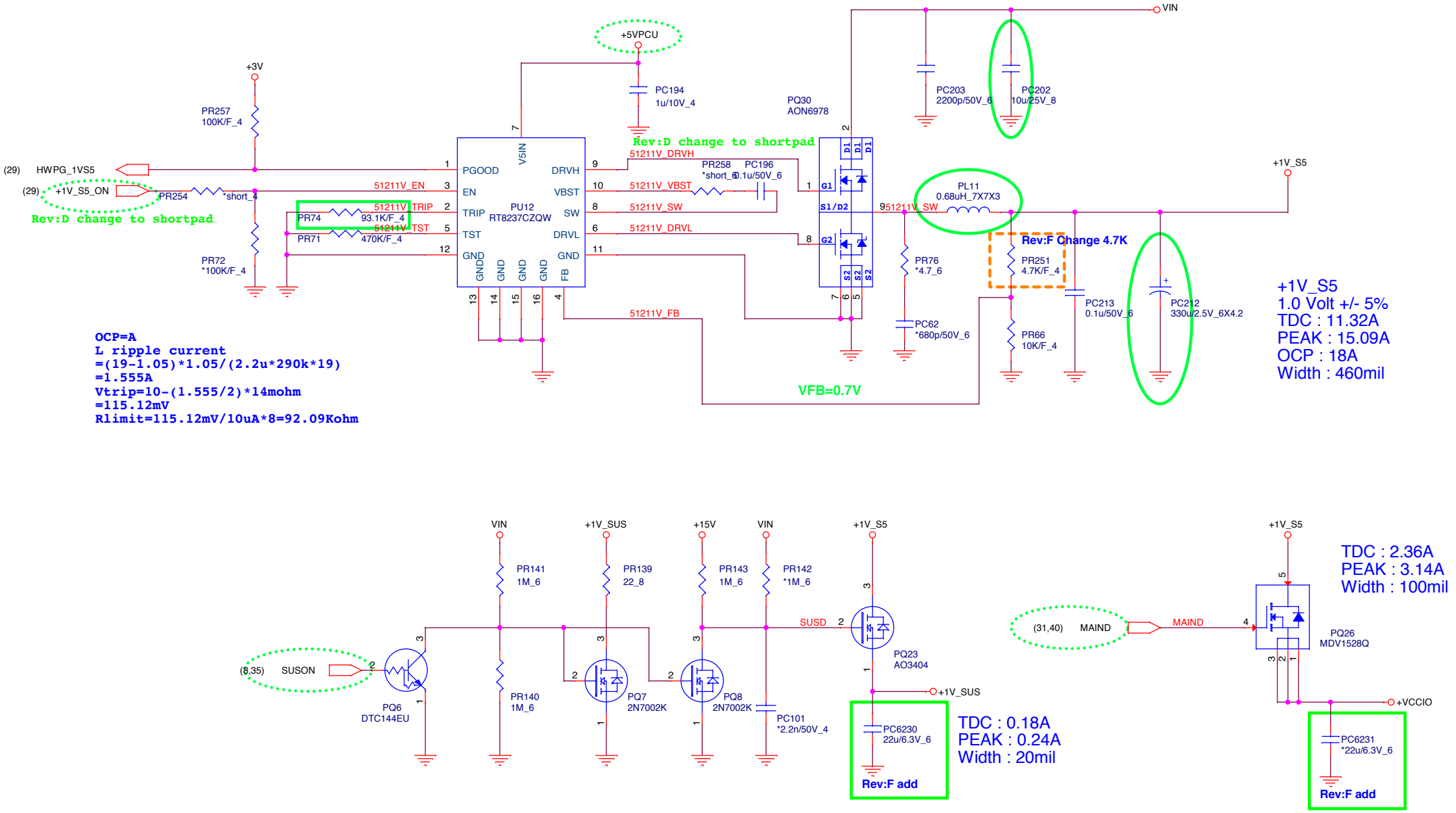
Reset SW (FSW)



Quanta Computer Inc.			
PROJECT : ZRW			
Size	Document Number	KBC IT8587	Rev 3A
Date: Monday, July 20, 2015	Sheet 29 of 48		


Power conn
PJ2
PD8 SV1040
PD3 P4SMAFL20A
PQ22 AON6414AL
PQ1 AON6414AL
PR213 0.01/F_0612
PR209 *short_4
PR210 *short_4
24780_ACN
24780_ACP
Rev:D change to shortpad
PC141 0.1u/50V_6
PC140 2200p/50V_6
PR185 *short_6
PR186 10/F_6
PC115 1u/25V_6
PC5 0.1u/50V_6
PC2 0.1u/50V_6
PR5 20_1206
PR165 4.02K/F_4
PR166 4.02K/F_4
PC116 0.47u/25V_6
PR168 866K/F_4
PR3 133K/F_4
PR1 100K/F_4
PR4 100K/F_4
REGN6V
ACIN
PU5 BQ24780SRUYR
CMSRC
ACDRV
VCC
ACDET
ACOK
SDA
SCL
IADP
IDCHG
PMON
TB_STAT
CMPOUT
ILIM
CMPIN
PROCHOT
BATPRES
BATDRV
BATSRC
REGN
BTST
HIDRV
PHASE
LDODRV
SRP
SRN
PQ20 AON7410
PQ21 AON7410
PL1 6.8uH_7X7X3
PR2 *4.7_6
PC4 *680p/50V_6
PR169 0.01/F_0612
BAT-V
PC121 2200p/50V_6
PC120 10U/25V_8
PC127 10U/25V_8
PR176 *short_4
PR175 *short_4
PR173 *short_6
PC122 2.2u/10V_6
PC117 2200p/50V_6
PC118 10u/25V_8
PC119 47n/50V_6
PC130 0.1u/25V_4
PC131 0.1u/25V_4
PC132 0.1u/25V_4
PR183 10/F_6
PR184 10/F_6
24780_SRP
24780_SRN
Rev:E change
UMA-> PR342 CS33832FB08 38.3K 1/16W +-1% (0402) For 78W
Dis -> PR342 CS33162FB14 31.6K 1/16W +-1% (0402) For 95W
PR342 31.6K/F_4
no stuff
PC7 *100P/50V_4
PC6 100P/50V_4
PC3 100P/50V_4
+3VPCU
PR16 10K_4
PR17 *10K_4
PR14 316K/F_4
PR15 100K/F_4
PR11 100K_4
PC123 0.01u/50V_4
PC126 0.1u/50V_6
PC125 *100p/50V_4
BAT-V
PR10 *0_4
PR8 100_4
TEMP_MBAT
PR9 1M_4
PJ1
PR6 100_4
PR7 100_4
MBCLK
MBDATA
PC8 *47p/50V_4
PC9 *47p/50V_4
PD1 PDZ5.6B
PD2 PDZ5.6B
PR12 *0_4
PR13 *0_4
H_PROCHOT#
PR174 *100K_4
+VCCIO
Check with HW side
P.36 VCC_CORE have PU to +1V
Power charger circuit reserve 2N7002 for GPU throtting
GPU_THROTTING#
PQ40 *EV@2N7002K
REGN MAX voltage 6.5V
V_ILIM=20*(VSRP-VSRN)=20*Ichg*Rsr
=0.793V for 3.965A current limit
ILIM=0.793V
Rsr = 0.01ohm
Quanta Computer Inc.
PROJECT : ZRW
Charger (BQ24780RUYR)
Rev 3A
Monday, July 20, 2015
Sheet 30 of 48

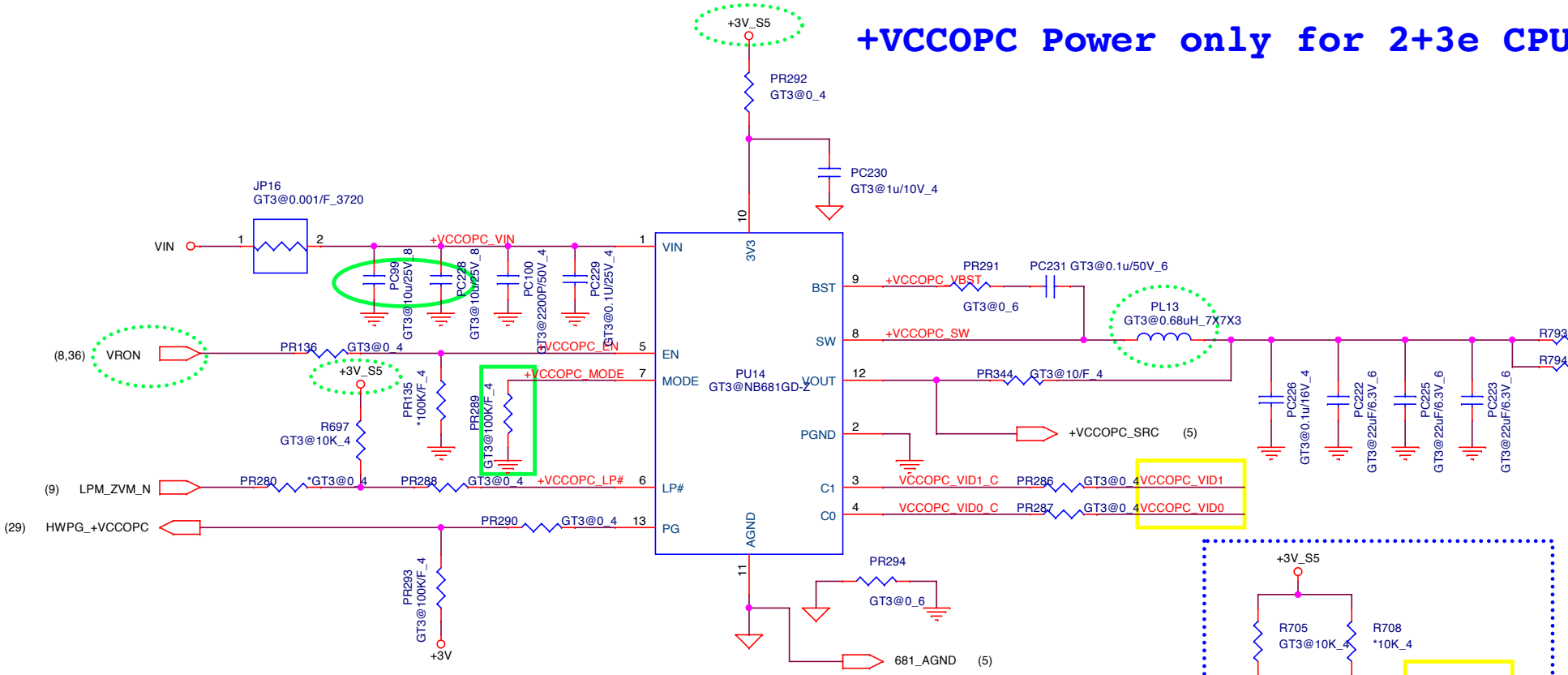

(2,40) SYS_SHDN# SYS_SHDN#
Rev:D change to shortpad
PR6130 *short_6
PR6280 10K/F_4
(29) SYS_HWPG
SYS_SHDN#
+3VPCU
VL
3V_LDO
VIN
PC6212 33u/25V_6x4.5
PC6220 10u/25V_8
PC6218 2200p/50V_4
PC6214 2200p/50V_4
PC6216 10u/25V_8
PR6278 *short_6
PR6285 *short_6
PR6284 *100K/F_4
PC6219 10u/6.3V_6
PC6100 0.1u/25V_4
PC6098 4.7u/6.3V_6
51225_VIN
+5VPCU
5 Volt +/- 5%
TDC : 7.9A
PEAK : 10.5A
OCP : 12A
Width : 320mil
PQ6056 AON7410
PQ6055 AON7752
PQ6054 AON7410
PQ6053 AON7752
PL6013 2.2uH_7X7X3
PL6012 2.2uH_7X7X3
PC6215 0.1u/50V_6
PR6287 1/F_6
PR6286 1/F_6
PC6213 0.1u/50V_6
PR6281 15.8K/F_4
PR6120 10K/F_4
PR6288 *4.7_6
PC6221 *680p/50V_6
PC6227 220u/6.3V_6X4.2
PC6226 0.1u/50V_6
PR6289 *4.7_6
PC6222 *680p/50V_6
PR6279 6.49K/F_4
PR6121 10K/F_4
PC6225 0.1u/50V_6
PC6224 220u/6.3V_6X4.2
PU6010 TPS51225RUKR
PGOOD
EN1
DRVH1
VBST1
SW1
DRVL1
VFB1
VO1
VREG5
VIN
VREG3
EN2
DRVH2
VBST2
SW2
DRVL2
VFB2
GND
VCLK
CS1
CS2
51225_EN1
51225_DH1
51225_VBST1
51225_SW1
51225_DL1
51225_FB1
51225_DH2
51225_VBST2
51225_SW2
51225_DL2
51225_FB2
51225_VCLK
51225_CS1
51225_CS2
PR6125 *short_6
Rev:D change to shortpad
+3VPCU
3.3 Volt +/- 5%
TDC : 5.2A
PEAK : 6.9A
OCP : 9A
Width : 220mil
OCP:12A
L(ripple current)
=(9-5)*5/(2.2u*0.3M*9)
=3.367A
Iocp=12-(3.367/2)=10.316A
Vth=(10.316A*14.5mOhm)+1mV=150.589mV
R(Ilim)=(150.589mV*8)/10uA
~120.47K
PD6004 1PS302
PD6008 1PS302
PC6099 0.1u/50V_6
PC6097 0.1u/50V_6
PC6211 0.1u/50V_6
PR6285 *short_6
PR6124 120K/F_4
PR6122 100K/F_4
+15V
+15V_ALWP
PR6275 22_8
PC6209 0.1u/50V_6
OCP:9A
L(ripple current)
=(9-3.3)*3.3/(2.2u*0.355M*9)
~2.676A
Iocp=9-(2.676/2)=7.661A
Vth=(7.661A*14.5mOhm)+1mV=112.098mV
R(Ilim)=(112.098mV*8)/10uA
=89.68K
MAIND
MAIND (32,40)
B2A
S0->S5 & S0->S3
Power off sequence under 200us
SUSB# -> VCCIO
Rev:E Reserve only no stuff
(8,11,29) SUSB#
PR6290 *10K/F_4
PQ6057 *2N7002K
PQ6058 *2N7002K
VIN
+3V_S5
+5V_S5
+15V
PR336 1M_6
PR338 22_8
PR339 22_8
PR334 1M_6
PR335 *1M_6
S5D
PQ34 MDV1528Q
+5V_S5
(29,40) S5_ON
PQ35 DTC144EU
PR337 1M_6
PQ36 2N7002K
PQ39 2N7002K
PQ33 2N7002K
PC282 *2.2n/50V_4
TDC : 3.38A
PEAK : 4.5A
Width : 140mil
PQ38 MDV1528Q
+5V
TDC : 3.6A
PEAK : 4.8A
Width : 160mil
PQ18 MDV1528Q
+3V
TDC : 2.05A
PEAK : 2.74A
Width : 100mil
PQ37 AO3404
TDC : 0.19A
PEAK : 0.25A
Width : 20mil
Rev E Add
C809 0.01u/50V_4
C810 0.01u/50V_4
Quanta Computer Inc.
PROJECT : ZRW
SYSTEM 5V/3V (NB680 & NB679)
Size
Document Number
Rev 3A
Date: Monday, July 20, 2015
Sheet 31 of 48

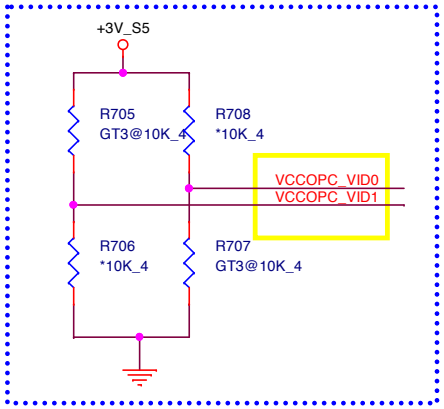


Quanta Computer Inc.		
PROJECT : ZRW		
Size	Document Number: +1V_S5 (RT8237CZQW)	Rev: 3A
Date: Monday, July 20, 2015	Sheet 32 of 48	

+VCCOPC Power only for 2+3e CPU

+VCCOPC
TDC : 4.5A
PEAK : 6A
Width : 200mil





Mode	VR Rail
0 ohm	VCCIO
Floating	PRIMCORE
100K	EDRAM/EOPIO
150K	Other

	LP#	C1	C0	Vo
VCCEDRAM	0	X	X	0V
	1	0	0	0.8V(MSM)
	1	0	1	0.95V
	1	1	0	1.0V
	1	1	1	1.05V

(5) +VCCOPC
(21,30,31,32,35,36,40,41,42) VIN
(2,4,6,7,8,9,12,13,14,15,16,21,22,23,24,25,27,28,31,32,35,36,40,41,42) +3V
(3,4,6,7,8,9,11,23,25,26,27,31,40,41) +3V_S5

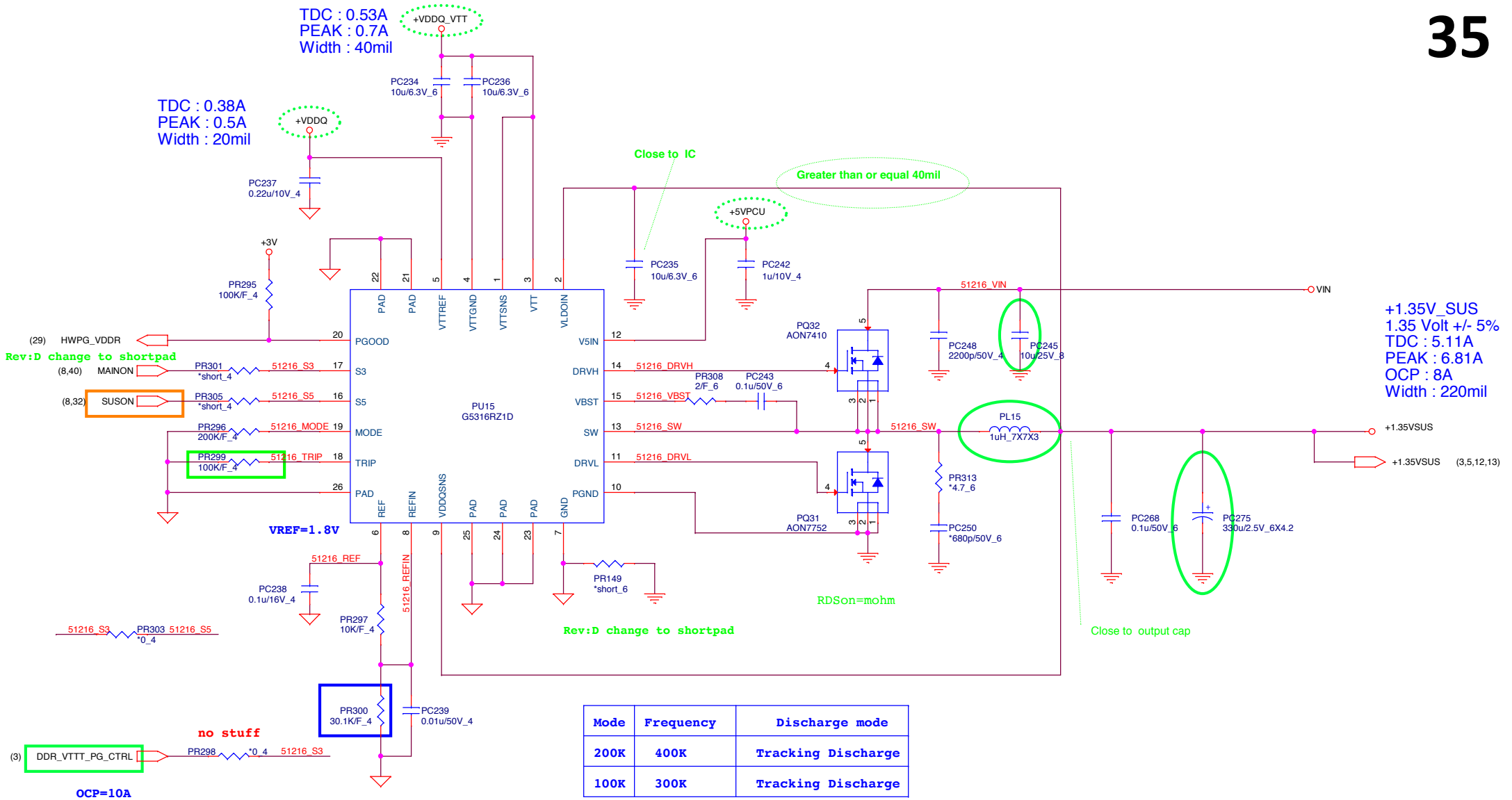
Quanta Computer Inc.
PROJECT : ZRW

Size	Document Number	Rev
	+VCCOPC (NB681GD-Z)	3A
Date: Monday, July 20, 2015	Sheet 33 of 48	

Quanta Computer Inc.

PROJECT : ZRW

Size	Document Number	Rev
	+VCCEOPIO (NB681GD-Z)	2A
Date: Thursday, June 25, 2015	Sheet 34 of 48	



Mode	Frequency	Discharge mode
200K	400K	Tracking Discharge
100K	300K	Tracking Discharge

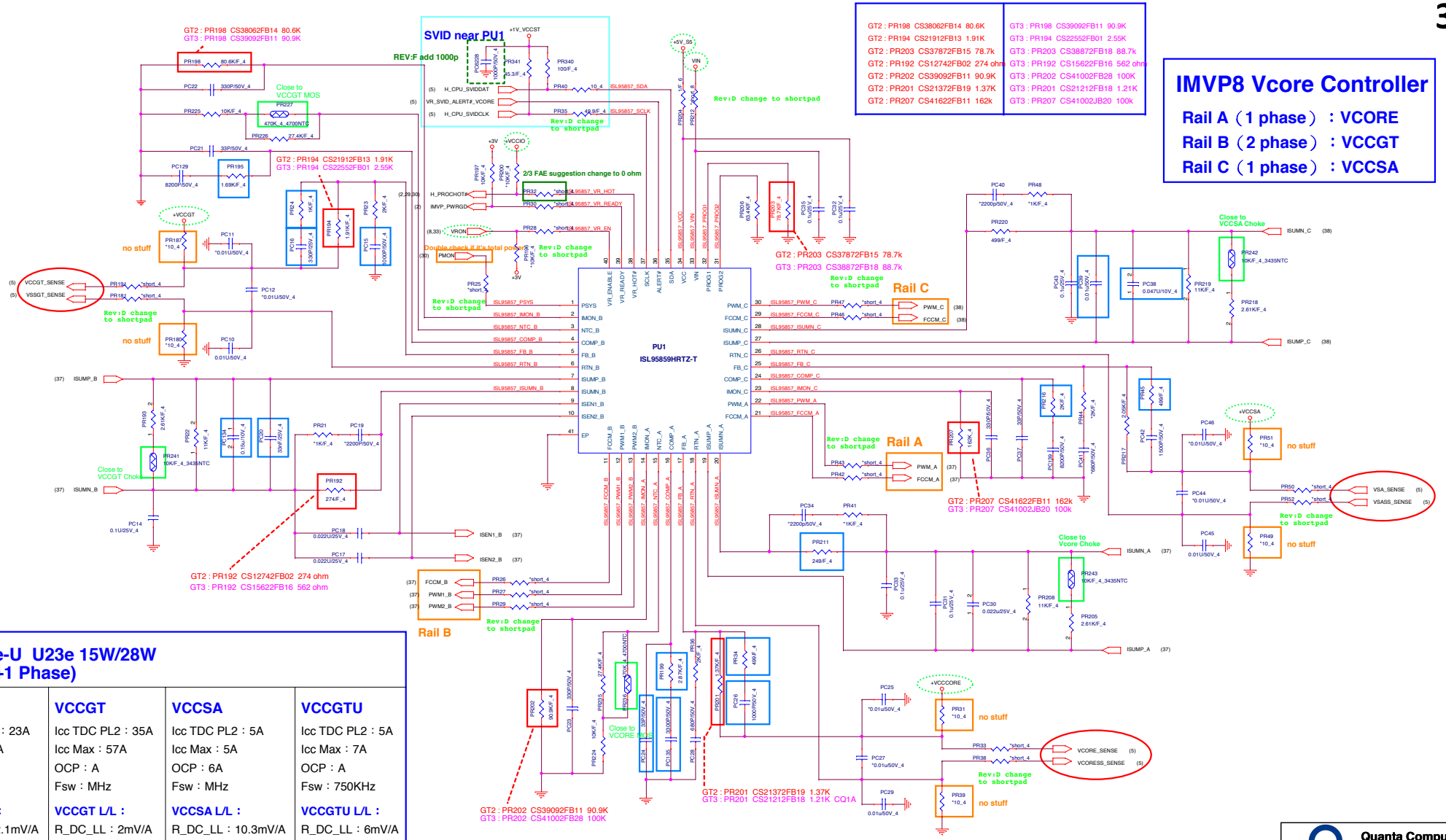
	S3	S5	+1.35VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

OCP=10A
L ripple current
=(19-1.35)*1.35/(2.2u*400k*19)
=1.425A
Vtrip=10-(1.425/2)*2.2mohm
=20.432mV
Rlimit=20.432mV/10uA*8=16.35Kohm

DDR=1.35V
PR84=10K/F_4
PR86=30.1K/F_4

Quanta Computer Inc.
PROJECT : ZRW

Size	Document Number	Rev
	DDR 1.35V (G5316RZ1D)	3A
Date: Monday, July 20, 2015	Sheet 35 of 48	



GT2 : PR198 CS38062FB14 80.6K	GT3 : PR198 CS39092FB11 90.9K
GT2 : PR194 CS21912FB13 1.91K	GT3 : PR194 CS22552FB01 2.55K
GT2 : PR203 CS37872FB15 78.7k	GT3 : PR203 CS38872FB18 88.7k
GT2 : PR192 CS12742FB02 274 ohm	GT3 : PR192 CS15622FB16 562 ohm
GT2 : PR202 CS39092FB11 90.9K	GT3 : PR202 CS41002FB28 100K
GT2 : PR201 CS21372FB19 1.37K	GT3 : PR201 CS21212FB18 1.21K
GT2 : PR207 CS41622FB11 162k	GT3 : PR207 CS41002JB20 100k

IMVP8 Vcore Controller

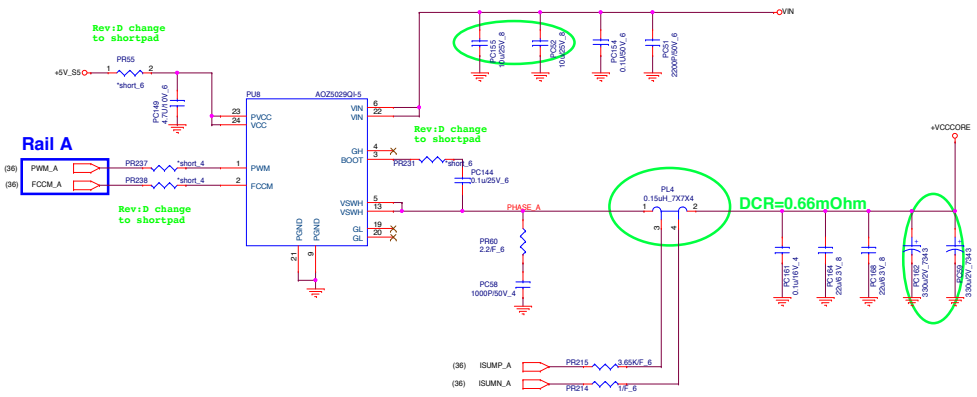
Rail A（1 phase）：VCORE
Rail B（2 phase）：VCCGT
Rail C（1 phase）：VCCSA

Skylake-U U23e 15W/28W (1+2+1+1 Phase)

VCORE	VCCGT	VCCSA	VCCGTU
Icc TDC PL2：23A	Icc TDC PL2：35A	Icc TDC PL2：5A	Icc TDC PL2：5A
Icc Max：29A	Icc Max：57A	Icc Max：5A	Icc Max：7A
OCP：35A	OCP：A	OCP：6A	OCP：A
Fsw：MHz	Fsw：MHz	Fsw：MHz	Fsw：750KHz
VCORE L/L：	**VCCGT L/L：**	**VCCSA L/L：**	**VCCGTU L/L：**
R_DC_LL：2.1mV/A	R_DC_LL：2mV/A	R_DC_LL：10.3mV/A	R_DC_LL：6mV/A
R_AC_LL：2.1mV/A	R_AC_LL：2mV/A	R_AC_LL：10.3mV/A	R_AC_LL：6mV/A

Quanta Computer Inc.
PROJECT : ZRW
Size | Document Number: CPU_CORE (ISL95857HRTZ-T) | Rev 3A
Date: Monday, July 20, 2015 | Sheet 36 of 48

VCORE



VCORE

Icc TDC PL2 : 23A

Icc Max : 29A

OCP : 35A

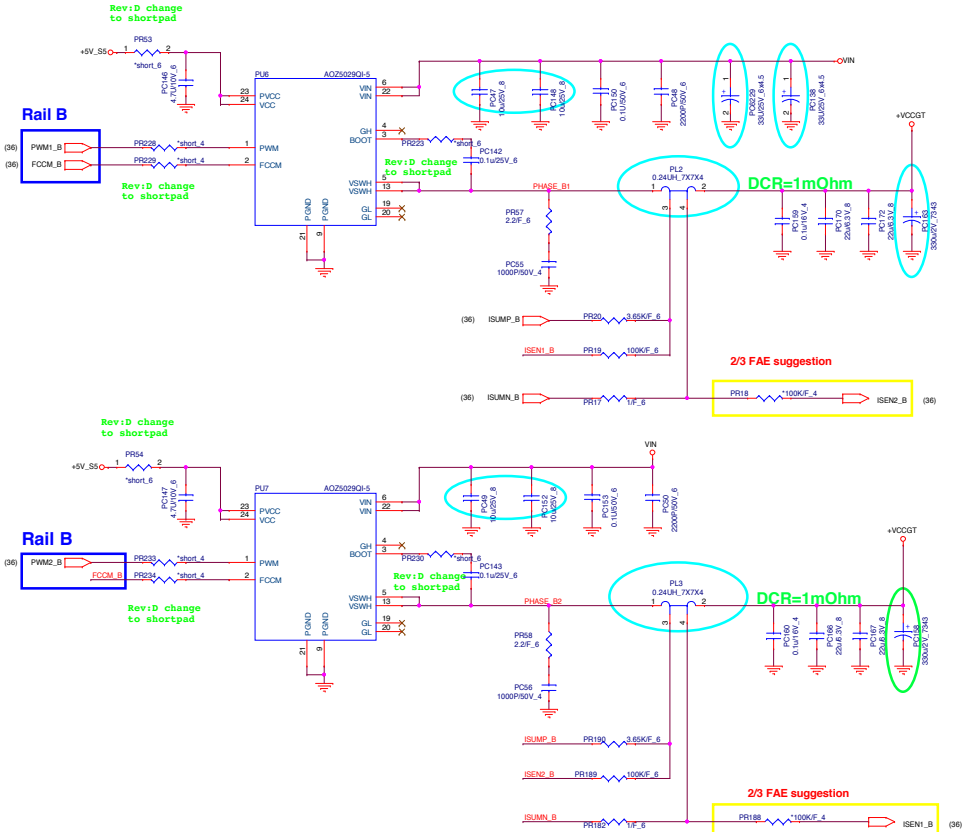
Fsw : 800KHz

VCORE L/L :

R_DC_LL : 2.1mV/A

R_AC_LL : 2.1mV/A

VCCGT



VCCGT

Icc TDC PL2 : 35A

Icc Max : 57A

OCP : A

Fsw : MHz

VCCGT L/L :

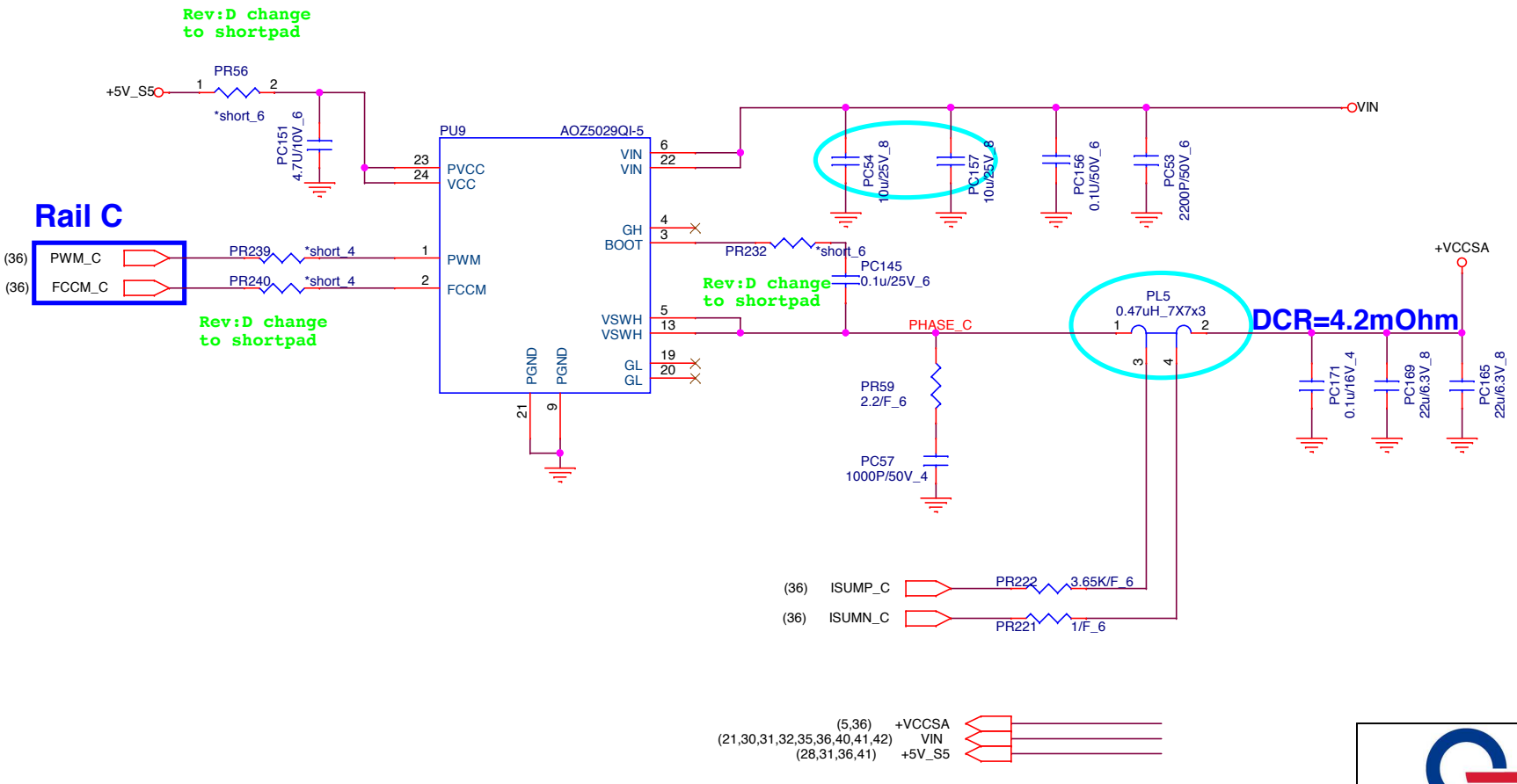
R_DC_LL : 2mV/A

R_AC_LL : 2mV/A

(5,36) +VCCORE
(21,30,31,32,35,36,40,41,42) VIN
(5,36) (28,31,36,41) +VCCGT +5V_S5

Quanta Computer Inc.
PROJECT : ZRW
Size | Document Number: VCORE/VCCGT (ISL95857HRTZ-T) | Rev: 3A
Date: Monday, July 20, 2015 | Sheet 37 of 48

VCCSA



VCCSA

Icc TDC PL2：5A

Icc Max：5A

OCP：6A

Fsw：800KHz

VCCSA L/L：

R_DC_LL：10.3mV/A

R_AC_LL：10.3mV/A

Quanta Computer Inc.

PROJECT : ZRW

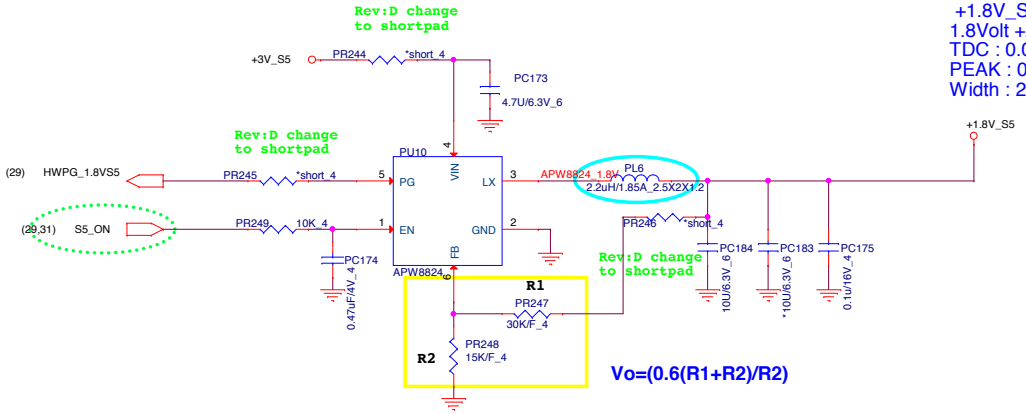
Size	Document Number	Rev
	VCCSA (ISL95857HRTZ-T)	3A
Date: Monday, July 20, 2015	Sheet 38 of 48	

Quanta Computer Inc.

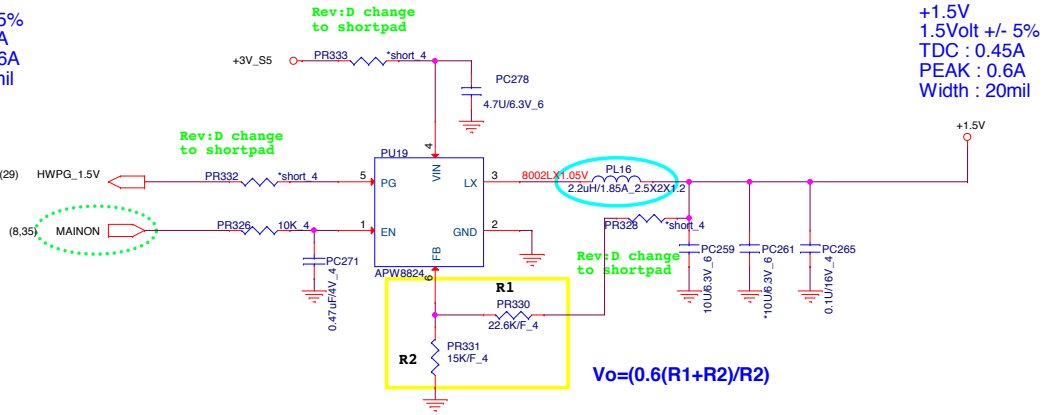
PROJECT : ZRW

Size	Document Number	Rev
	+VCCGTX (ISL95853HRZ-T)	2A

Date: Thursday, June 25, 2015 Sheet 39 of 48



+1.8V_S5
1.8Volt +/- 5%
TDC : 0.08A
PEAK : 0.06A
Width : 20mil

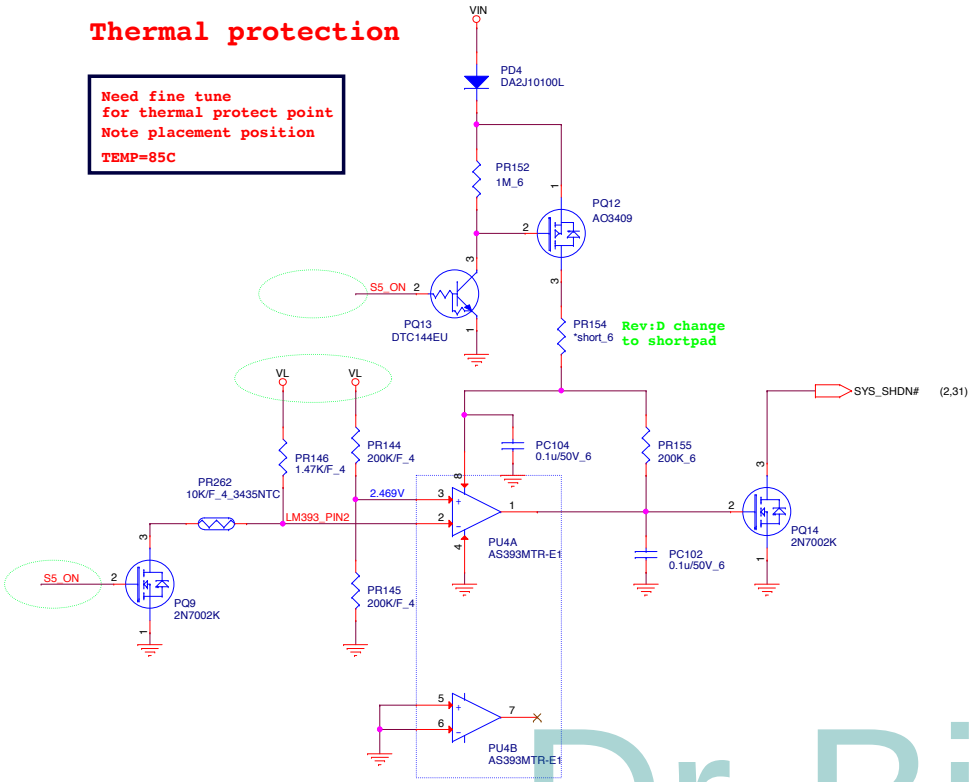


+1.5V
1.5Volt +/- 5%
TDC : 0.45A
PEAK : 0.6A
Width : 20mil

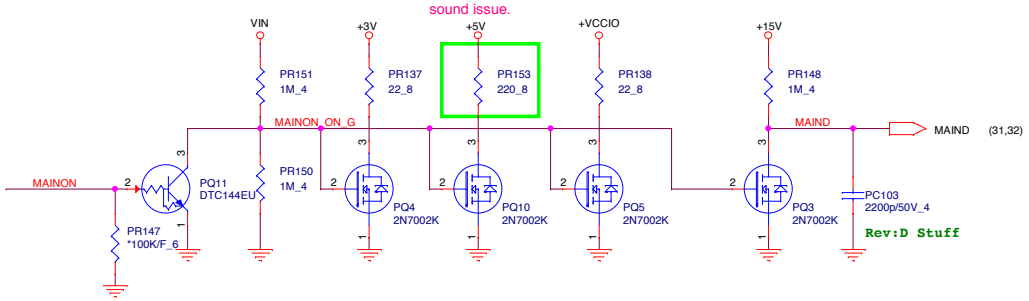
Thermal protection

Need fine tune
for thermal protect point
Note placement position

TEMP=85C



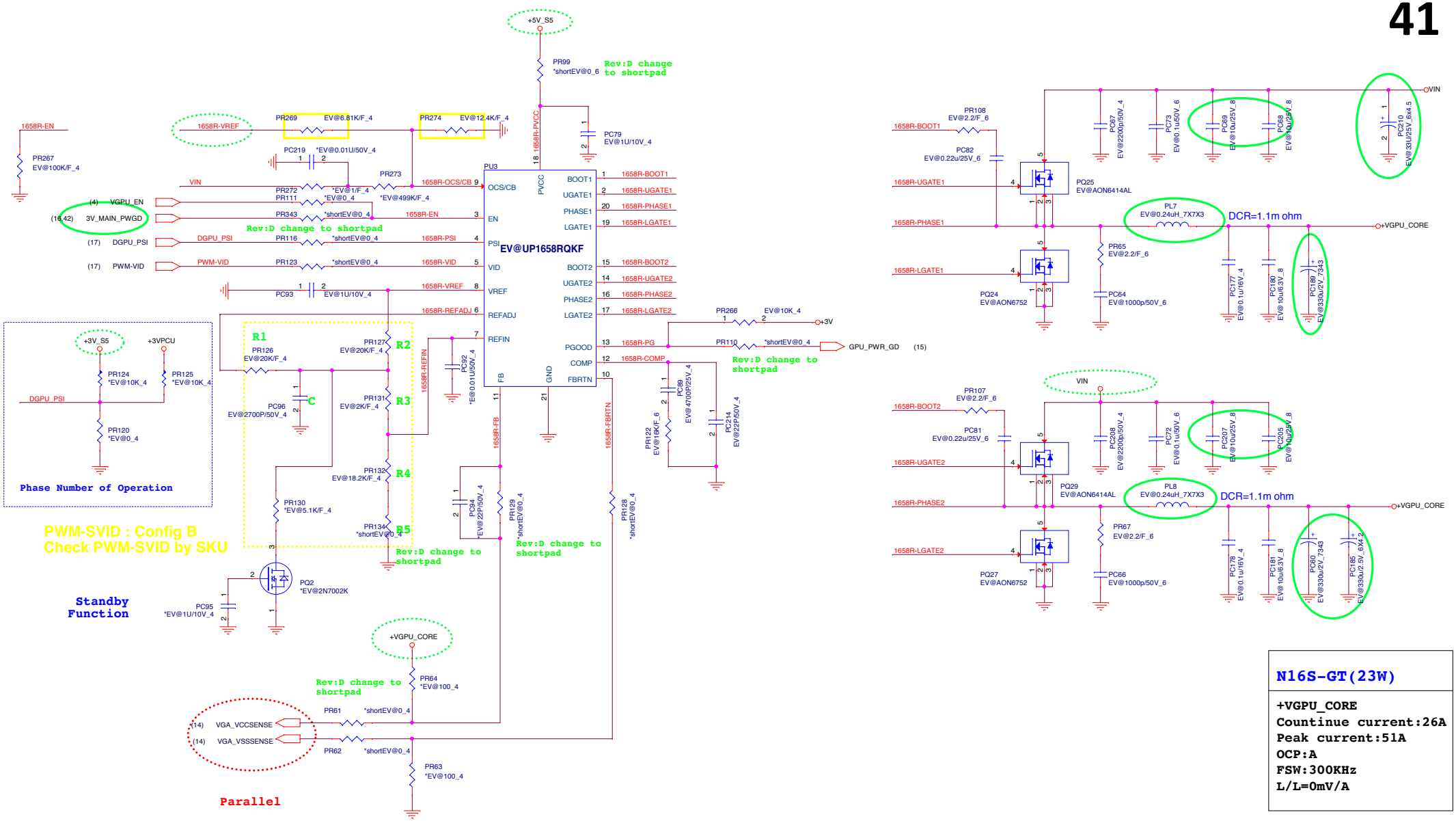
Rev:C change to 220 ohm
PR153 Change to
220 ohm for bo bo
sound issue.



For EC control thermal protection (output 3.3V)

Quanta Computer Inc.
PROJECT : ZRW

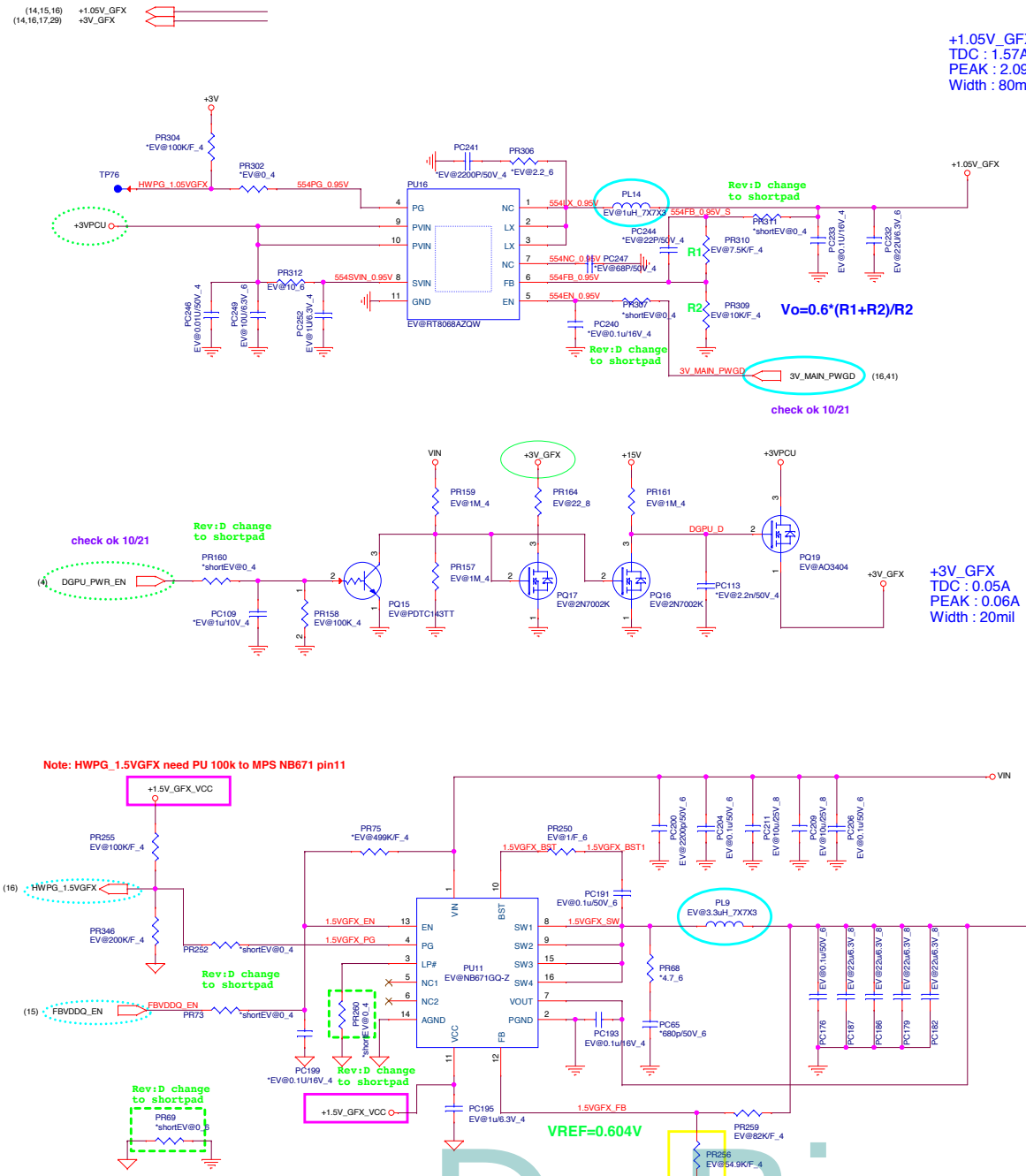
Size	Document Number	Rev
	+1.8V/+1.5V/Thermal Protect	3A
Date: Monday, July 20, 2015	Sheet 40 of 48	



N16S-GT(23W)

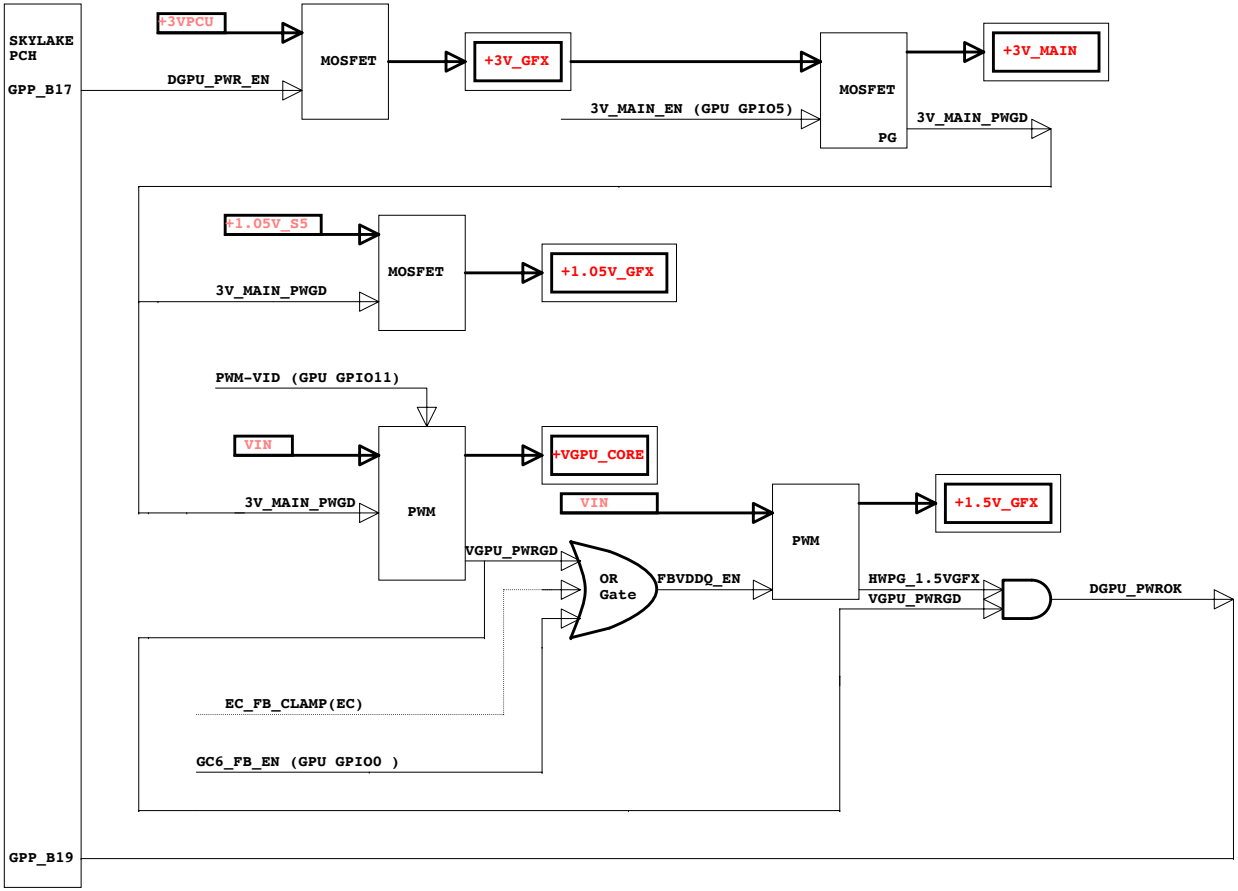
+VGPU_CORE
Countinue current:26A
Peak current:51A
OCP:A
FSW:300KHz
L/L=0mV/A

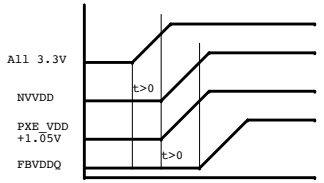
Quanta Computer Inc.		
PROJECT : ZRW		
Size	Document Number: +VGPU_CORE(UP1642PQAG)	Rev: 3A
Date: Monday, July 20, 2015	Sheet 41 of 48	



Quanta Computer Inc.			
PROJECT : ZRW			
Size	Document Number		Rev
	+1.5V_GFX/+1.05V_GFX/+3V_GFX		3A
Date: Monday, July 20, 2015	Sheet 42 of 48		

VGA power up sequence

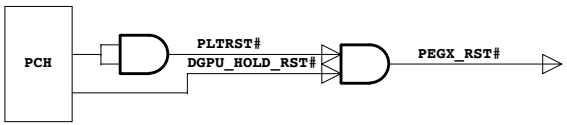




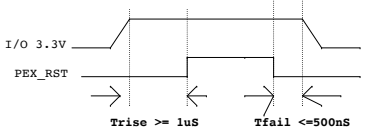
N15x Power on sequance

Notes: -All 3.3V includes all rails powered at 3.3V
-PEX_VDD 1.05V inculdes all rails that are shared

VGA Reset



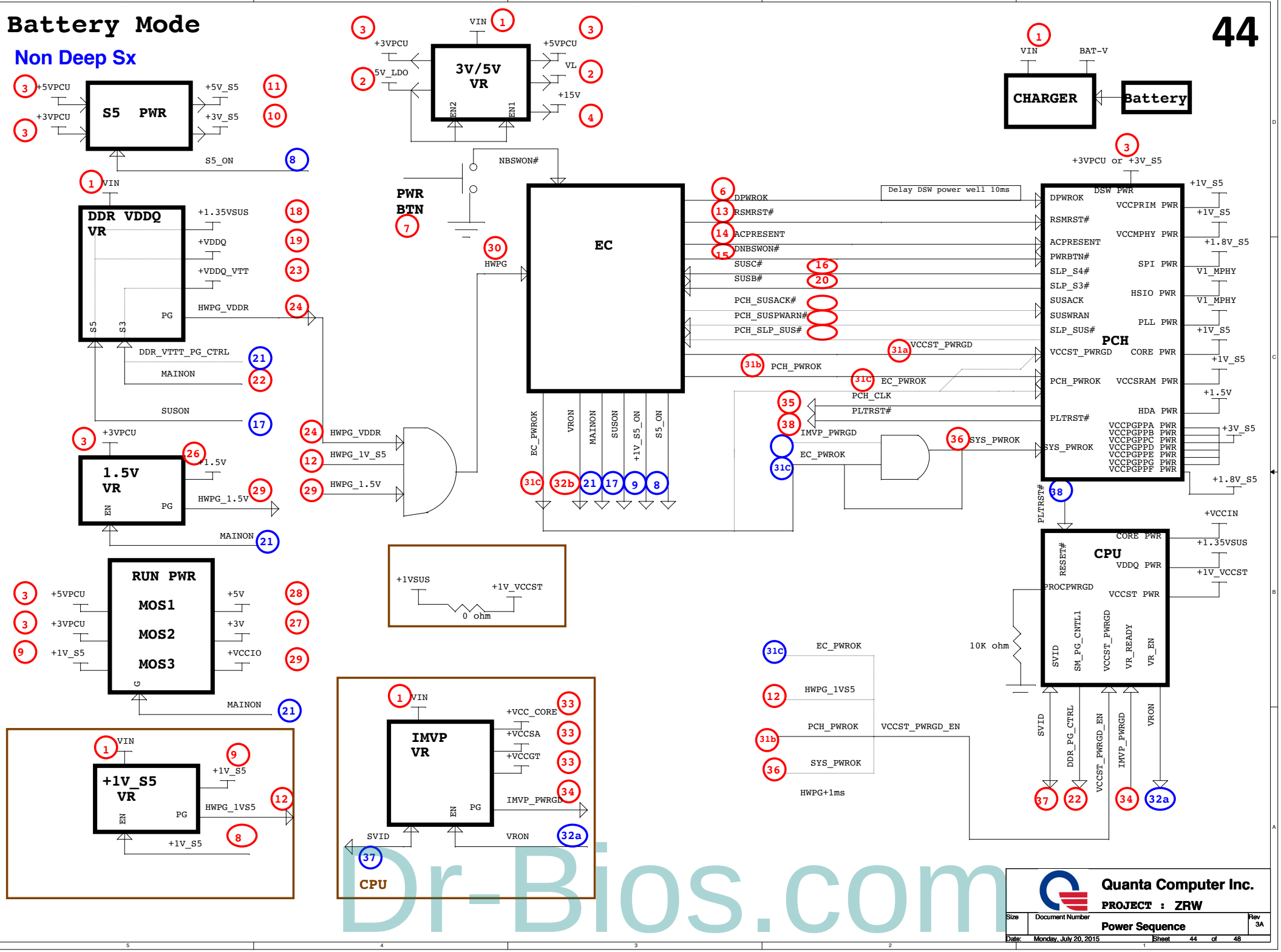
PEX_RST timing



Quanta Computer Inc.
PROJECT : ZRW
Size | Document Number: GPU PWR CRL | Rev 3A
Date: Monday, July 20, 2015 | Sheet 43 of 48

Battery Mode

Non Deep Sx



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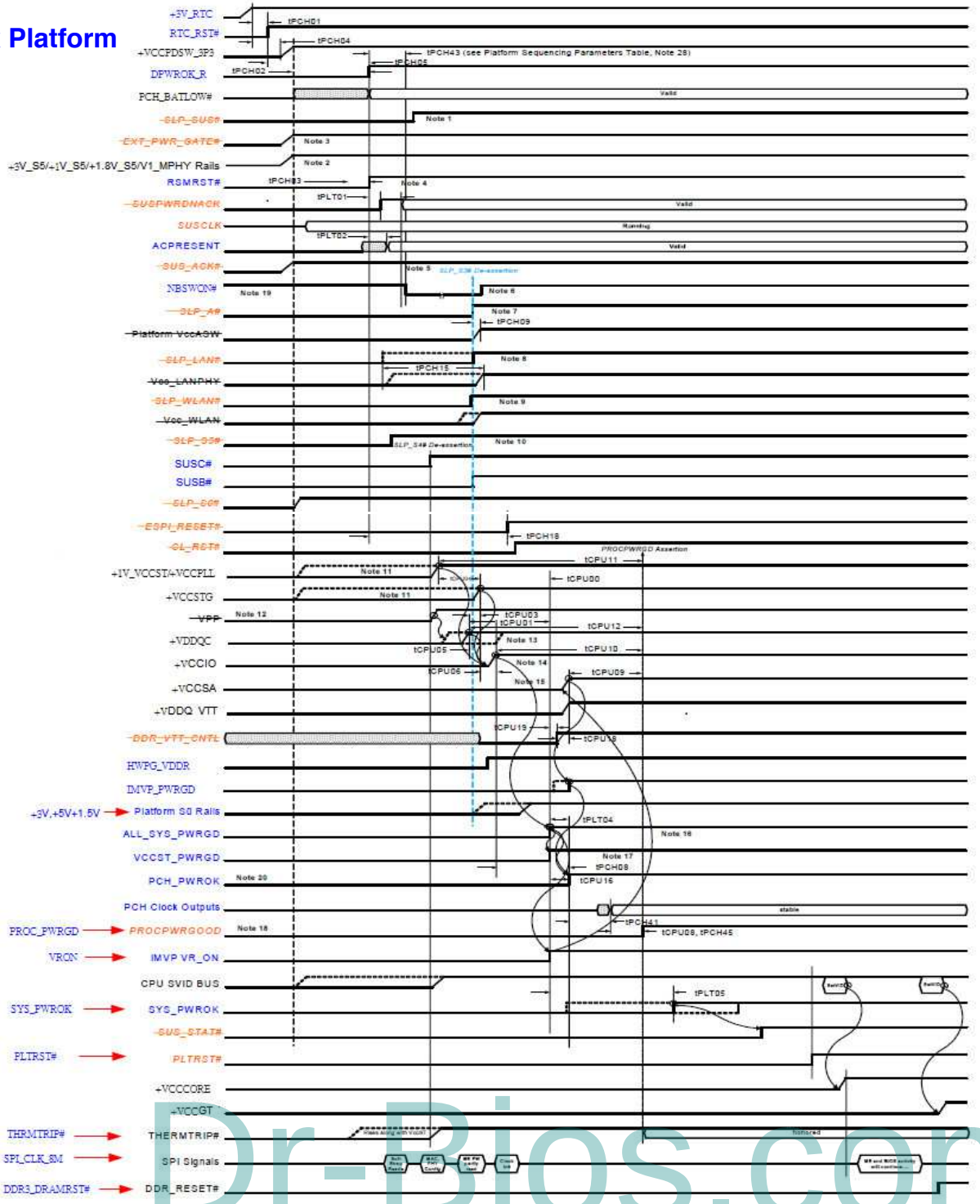
Skylake U Non-Deep Sx Platform Power on sequence



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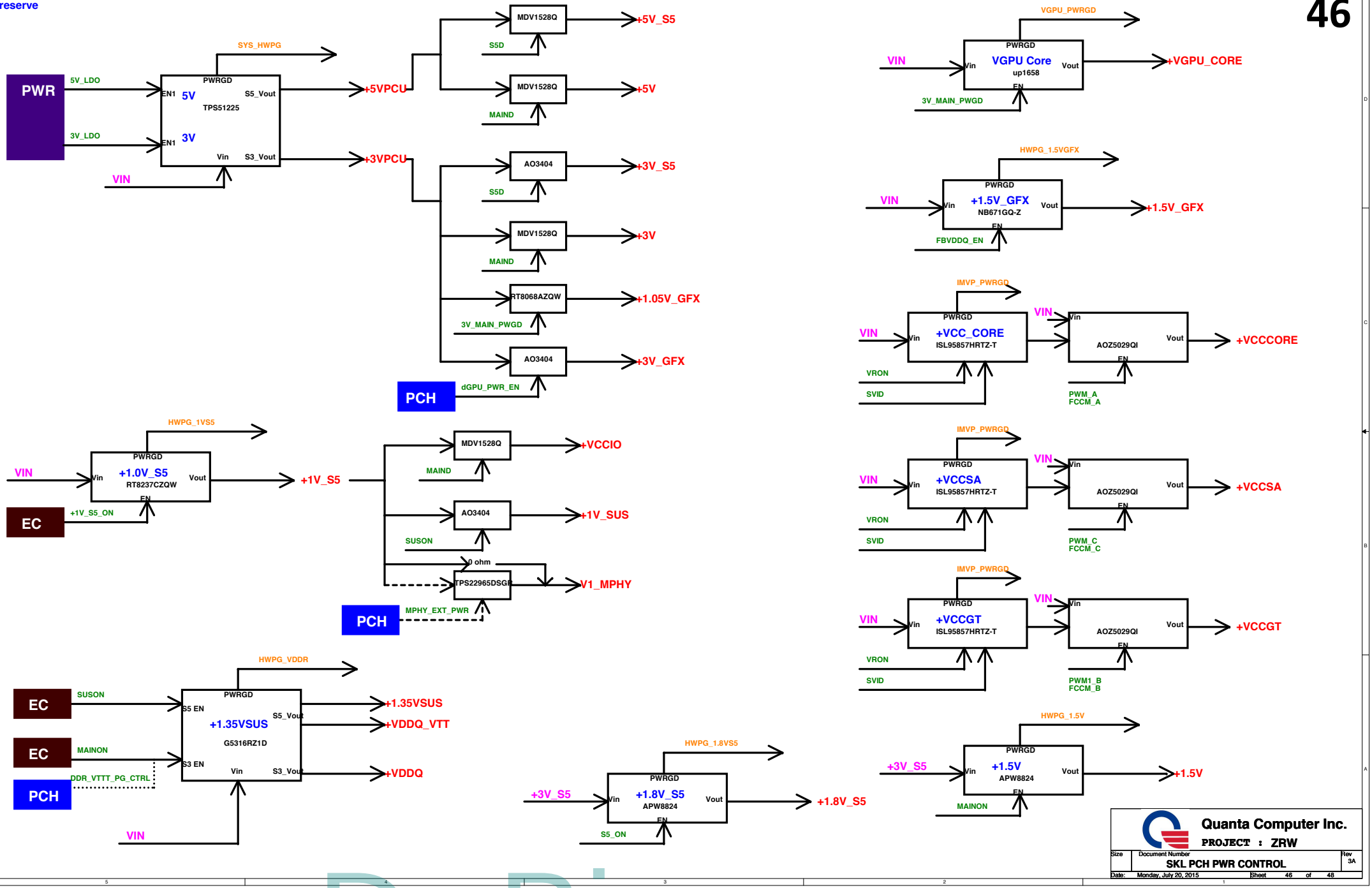
實線表defult
虛線表reserve



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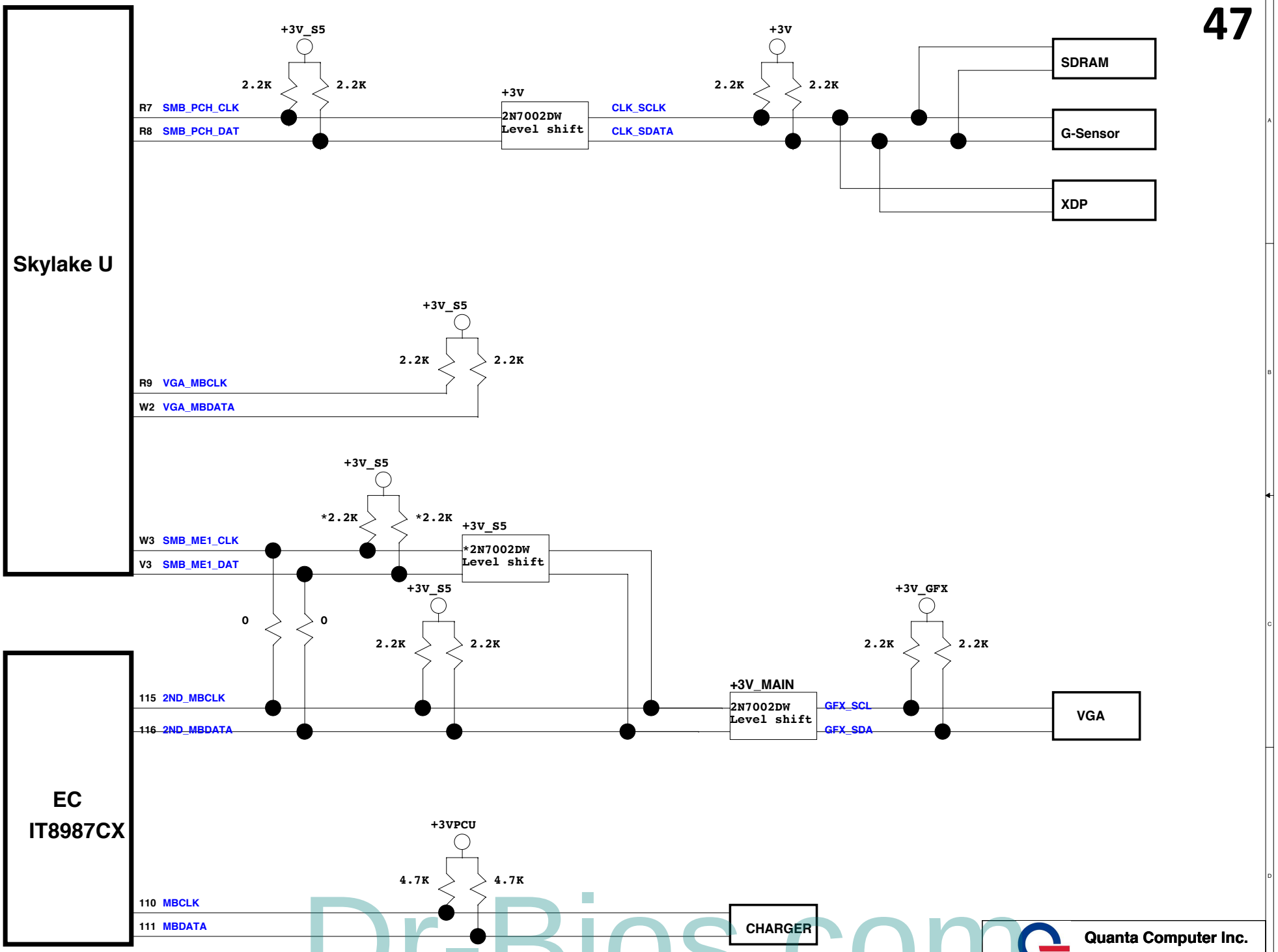

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Model	Date	CHANGE LIST
ZRW REV:A	1/20	1. FIRST RELEASED
ZRW REV:B	2/4	1. PU3#3 enable pin from VGPU_EN change to 3V_MAIN_PWGD control , add PR343 0ohm. (page 41) 2. U35#U11 #U12 connect to +1.8V_S5 for support Cannonlake-U PCH. (page 10) 3. U46#3 from net USB_OC1# change connect to USB_OC2# PCH. (page 28) 4. Add R776 33 0hm and C805 180 pf in NBSWON#. (page 27) 5. Change LAN WAKE# pin from CPU LAN_WAKE# to WAKE#(ball BB15) to support CPPM(PCIE LTR&OBFF&L1 off) (page 08) 6. add PR344 between PU14#12 & JP13. for GT3 CPU (page 33) 7. add PR345 between PU13#12 & JP12 for GT3 CPU (page 34)
	2/12	1. net ACCEL_INTA from U35#AD1 change to U35#AB1 [UART0_RX] net TP_INT_PCH from U35#AD2 change to U35#AB3 [UART0_CTS#] (page 04) 2. CN3 all pin from UART1 change connect to UART2 (page 04) 3. R587 from 0 ohm change to 1k pull down for USB2_ID (page 06) 4. add C806 for EMI request R748 0 ohm no stuff from EC site move at CPU site (page 07) 5. R293 stuff 4.7k , R294 from 4.99k change to 5.49k (page22) 6. XDP_TCK0,XDP_TCK1,XDP_TMS,XDP_TDI don't need pull up or pull down NO Stuff R515 , R558, R514, R537. (page 02)
	2/12	1. p.40 PR153 from 22 ohm change to 220 ohm for S3/S4/S5 bo bo sound issue.
	3/4	1. p.15 & p.16 L1 & L2 footprint from 0603 change to 0402 2. p.6 Delete UART1 4 pcs TP 3. p.25 EMI request add C807 33p for CLKRUN# 4. p.31 +3vpcu & +5vpcu from MPS NB679 change to TPS51225 5. p.24 R420 & R422 vendor suggest from 56 ohm change to 62 ohm [CS06202JB15]
ZRW REV:C1	4/30	1. p.2 Stuff 10k ohm_4 of R780 & R781. [KBSMI# & EC_SCI#] Pull up to +3V. 2. P.29 U45 EC pin 70 connect to p.30 PU5#8 IDCHG net 3. P.29 U45 EC pin 95 connect to net IOAC_LANPWR# 4. P.06 Add PQ6059 & PQ6060 for EC_RTCRST control reset RTC SRTC_RST# & RTC_RST#
	5/7	1. p.09 removed MPHY_EXT_PWR control power function. [Removed U11, R195, R197,C208,C253] 2. p.07 R576 & R572 from value 4.7k change to 2.2k
ZRW REV:C2	5/8	1. p.36 & p37 change new PU6,PU7,PU8,PU9 footprint AOZ5029QI-5 & partnumber AL005029001 2. p.28 Delete L8,L9,L10,L14,L15,17 EMI Choke footprint
	5/25	1. p.09 R762 [LPM_ZVM_N] & R763 [MSM#] No Stuff for GT3 2. p.09 add R789 0 ohm for VCCHDA p.24 R365 stuff 0 ohm connect to +3V , R363 0 ohm no stuff connect to +1.5v 3. p.34 delete +VCCEOPIO circuit 4. p.05 delete R141 , R133 , R547 for SVID data,Alert#,clk 5. p.39 delete VCCGTX circuit 6. p.37 delete PR77 & PR88 for VCCGT connect to VCCGTX
	5/28	1. p.03 Delete R656 & R189. DDR0_ALERT# & DDR1_ALERT# connect to GND 2. p.09 Delete R763 0 ohm for net MSM#.
ZRW REV:C3	6/18	1. p.05 Add C814 1000p/50v_4 connect +1V_VCCST and near R138 SVID. 2. p.36 Add PC6228 1000p/50v_4 connect +1V_VCCST and near RR341 SVID. 3. p.02 Add R795 , R796 , R797 0ohm for DCI USB 3.0 test fixture 4. p.11 delete XDP function connector U27 , U30 , CN1 5. p.09 Remove short Jumper for all +1V_S5. 1. R163 , R159 ,R581, R146 ,R149 , R157 , R173 , R151 , R170 , R136 2. R545 , R144 , R150 , R147 , R551 , R557, R584 [VCCCLK1~6] 3. R168 [+1_S5 -> V1_MPHY] 6. p.36 remove PR37 Shortpad for SVID_ALERT# 7. p.07 Delete Q33 , R579 ,R583 for SMBus(EC)
	6/23	1. p.02 Delete TP82 and Net [SKTOCC#] 2. p.05 reserve 5 pcs 1000 pF capacitor in +1V_VCCST [C815,C816,C817,C818,C819] , no stuff by default 3. p.09 Reserve test point TP95 for CPU AK13 ball 4. p.32 add PC6230 22u/6.3v_6 in connect to PQ23.1 [+1V_SUS]

Quanta Computer Inc. PROJECT : ZRW Size / Document Number / Rev 3A Change list Date: Monday, July 20, 2015 Sheet 48 of 48	DOC NO.	PROJECT MODEL : ZWA	APPROVED BY:	DATE:
		PART NUMBER:	DRAWING BY:	REVISON: