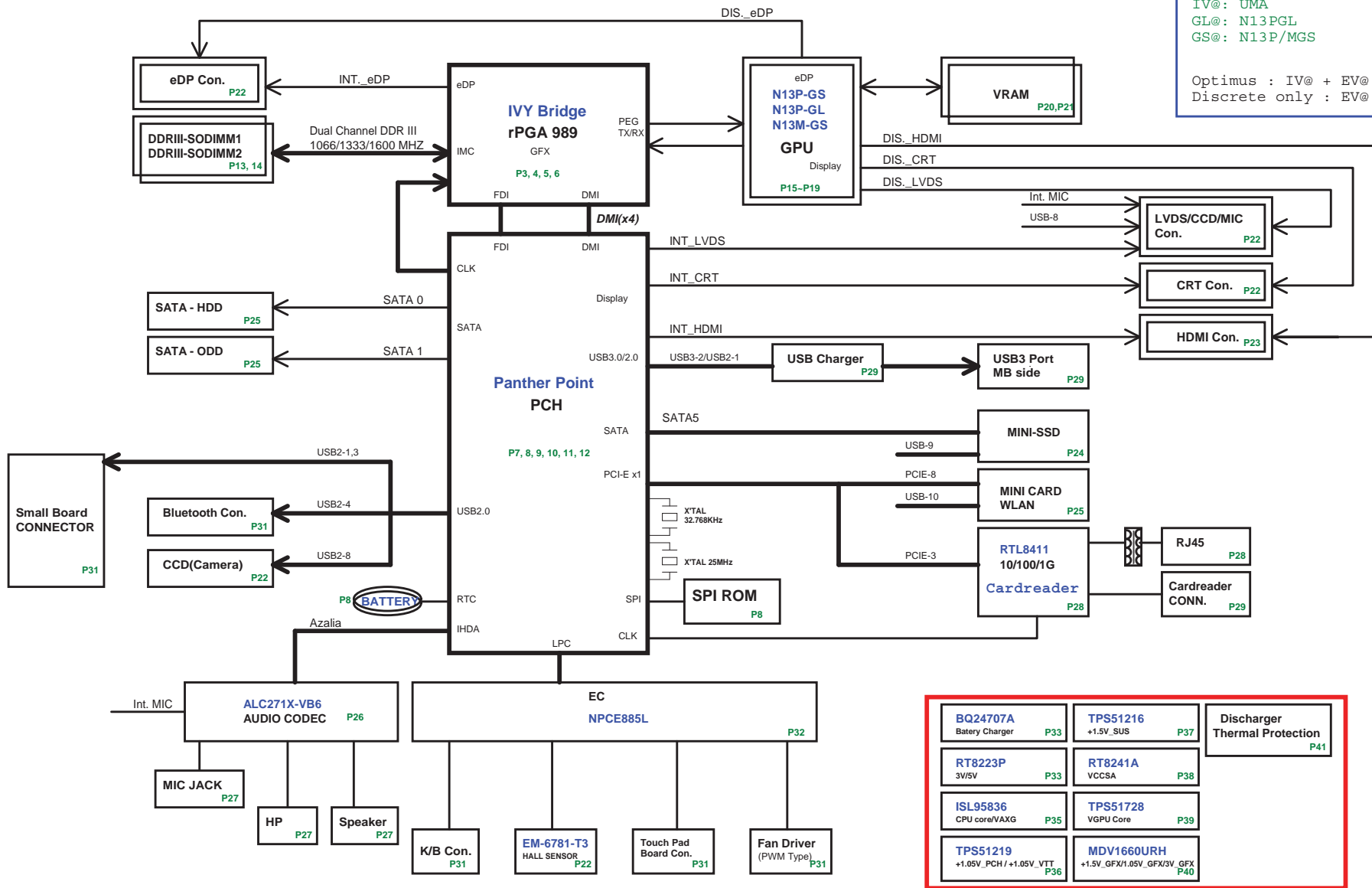


# ZQTA/ZQSA CRV SYSTEM BLOCK DIAGRAM

BOM

IV@ : iGPU  
 EV@ : dGPU  
 OP@ : Optimus  
 DO@ : Discrete only  
 SP@ : Special  
 SNP@ : N13PGS/GL  
 IV@ : UMA  
 GL@ : N13PGL  
 GS@ : N13P/MGS

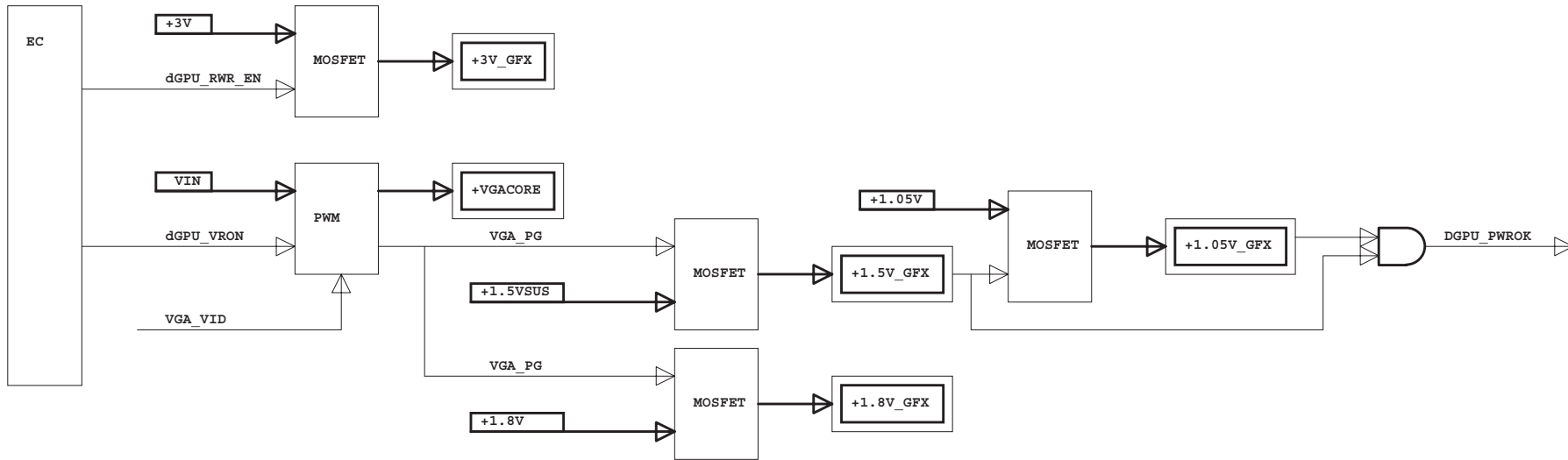
Optimus : IV@ + EV@ + OP@  
 Discrete only : EV@ + DO@



<b>BQ24707A</b> Battery Charger P33	<b>TPS51216</b> +1.5V_SUS P37	<b>Discharger Thermal Protection</b> P41
<b>RT8223P</b> 3V/5V P33	<b>RT8241A</b> VCCSA P38	
<b>ISL95836</b> CPU core/VAXG P35	<b>TPS51728</b> VGPU Core P39	
<b>TPS51219</b> +1.05V_PCH / +1.05V_VTT P36	<b>MDV1660URH</b> +1.5V_GFX/1.05V_GFX/3V_GFX P40	

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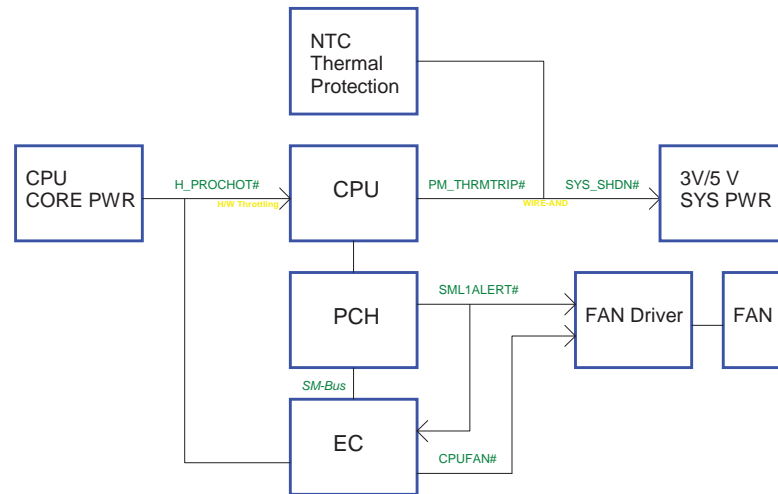
## VGA power up sequence



## Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+3V_RTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT/CIR POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.5VSUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+VGFX_AXG	variation	Internal GPU POWER	VRON	S0
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE POWER/IVY/SNB bridge VCCIO	MAINON	S0
+VCCSA	+0.9V	CPU POWER	HWPG_VTT	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
			MAINON	S0

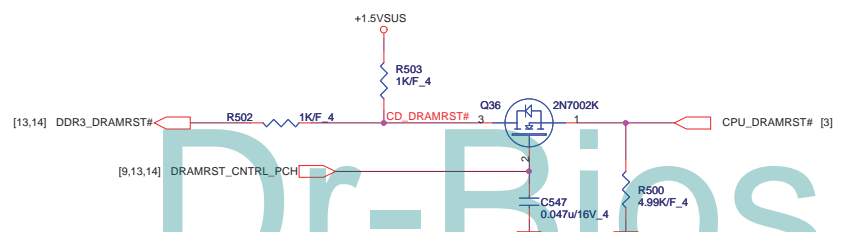
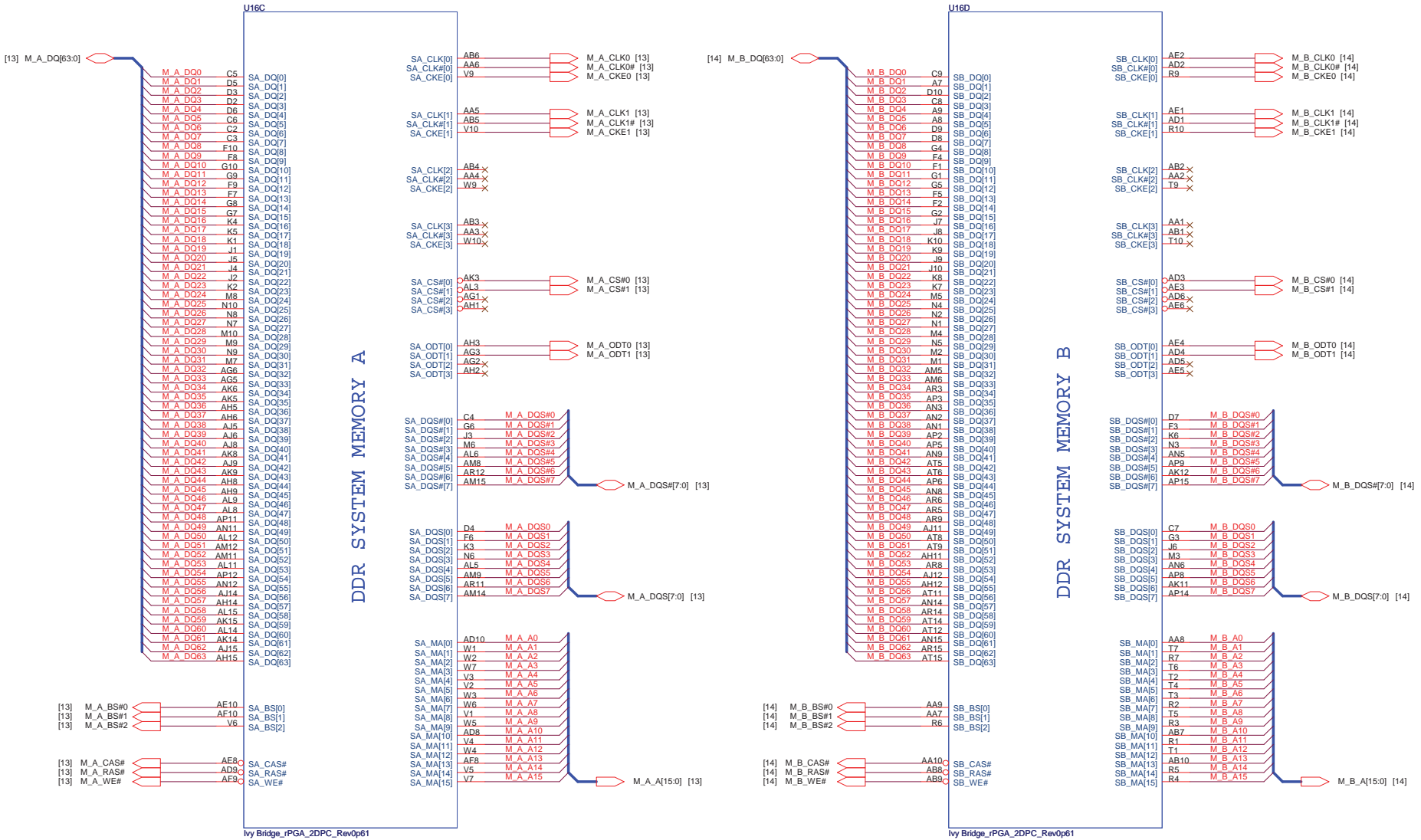
## Thermal Follow Chart



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# IVY Bridge Processor (DDR3)



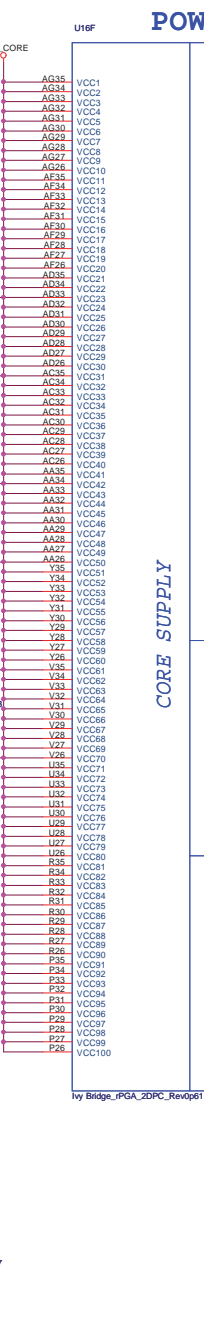
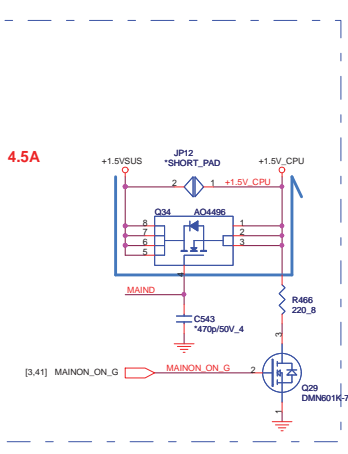
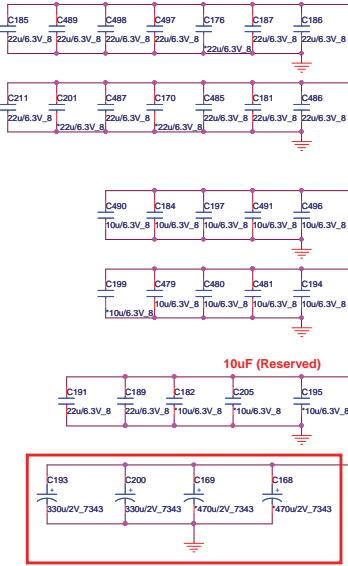
**Quanta Computer Inc.**  
PROJECT : ZQTA/ZQSA

Size	Document Number	Rev
	IVY Bridge 2/4	1A
Date:	Friday, November 11, 2011	Sheet 4 of 44

### IVY Processor (POWER)

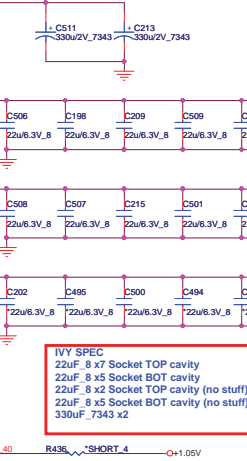
**CPU Core Power**  
 IVY 45W:TDC 52A  
 IVY SPEC  
 22uF\_8 x8 Socket TOP cavity  
 22uF\_8 x10 Socket BOT cavity  
 470uF\_7343 x4  
 total : 10uF x 10, RSVD x 1  
 total : 22uF x 16, RSVD x 3  
 total : 470u x 4, RSVD x2

**SNB : Spec**    **Cose down**  
 470uF/4mohm x 4    330uF x 2  
 22uF x 16            10uF x 4  
 10uF x 10            reserved x 5



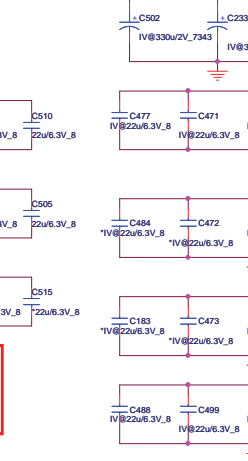
**CPU VTT**  
 IVY 45W:8.5A  
 SNB : Spec  
 330uF/6mohm x 2  
 22uF x 12  
 22uF x 7 (Non-stuff)

**Cose down**  
 330uF x1  
 22uF x 2  
 10uF x 10  
 reserved x 4

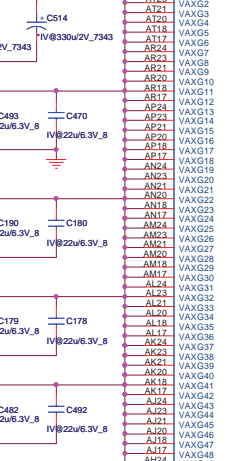


**CPU VGT**  
 IVY 45W:TDC 38A  
 Spec  
 470uF/4mohm x 2  
 22uF x 12

**Cose down**  
 330uF x1  
 22uF x 4  
 10uF x 10



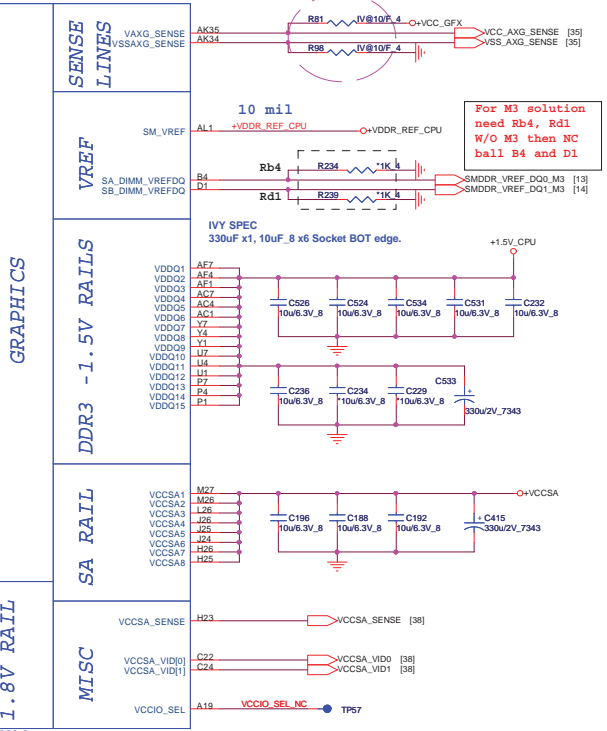
**IVY SPEC**  
 22uF\_8 x2 Socket TOP cavity  
 22uF\_8 x2 Socket BOT cavity  
 22uF\_8 x4 Socket TOP edge  
 22uF\_8 x4 Socket BOT edge  
 470uF\_7343 x2



### IVY Bridge Processor (GRAPHIC POWER)

#### POWER

0929 change value by CRB

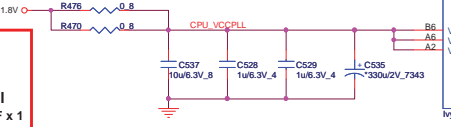


DIS. VGA	UMA / Optimus
Ra 0 ohm	NA

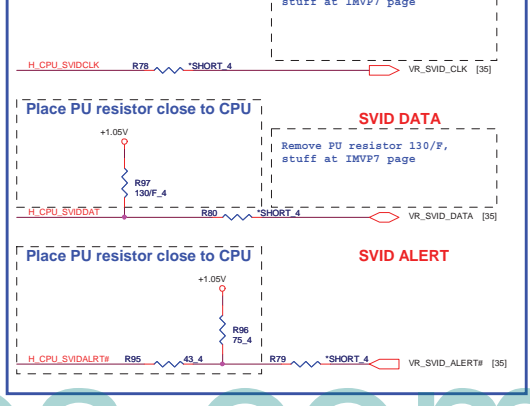
**CPU VCCPL**  
 IVY 45W:1.5A  
 Spec  
 330uF/7mohm x 1  
 10uF x 1  
 1uF x 2

**Real**  
 10uF x 1  
 1uF x 2

**IVY SPEC**  
 330uF x1, 10uF\_8 x1, 1uF\_4 x2  
 Socket BOT edge.

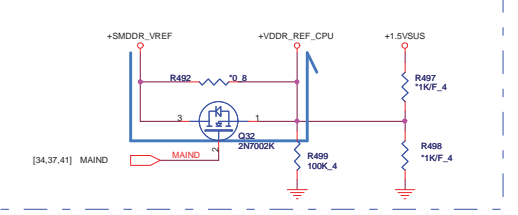


**Layout note: need routing together and ALERT need between CLK and DATA**



**IVY SPEC**  
 330uF x1, 10uF\_8 x1 Socket BOT edge,  
 10uF\_8 x2 Socket BOT cavity.

**CPU SA**  
 IVY 45W: 6A  
 Spec  
 330uF/7mohm x 1    10uF x 3  
 10uF x 3



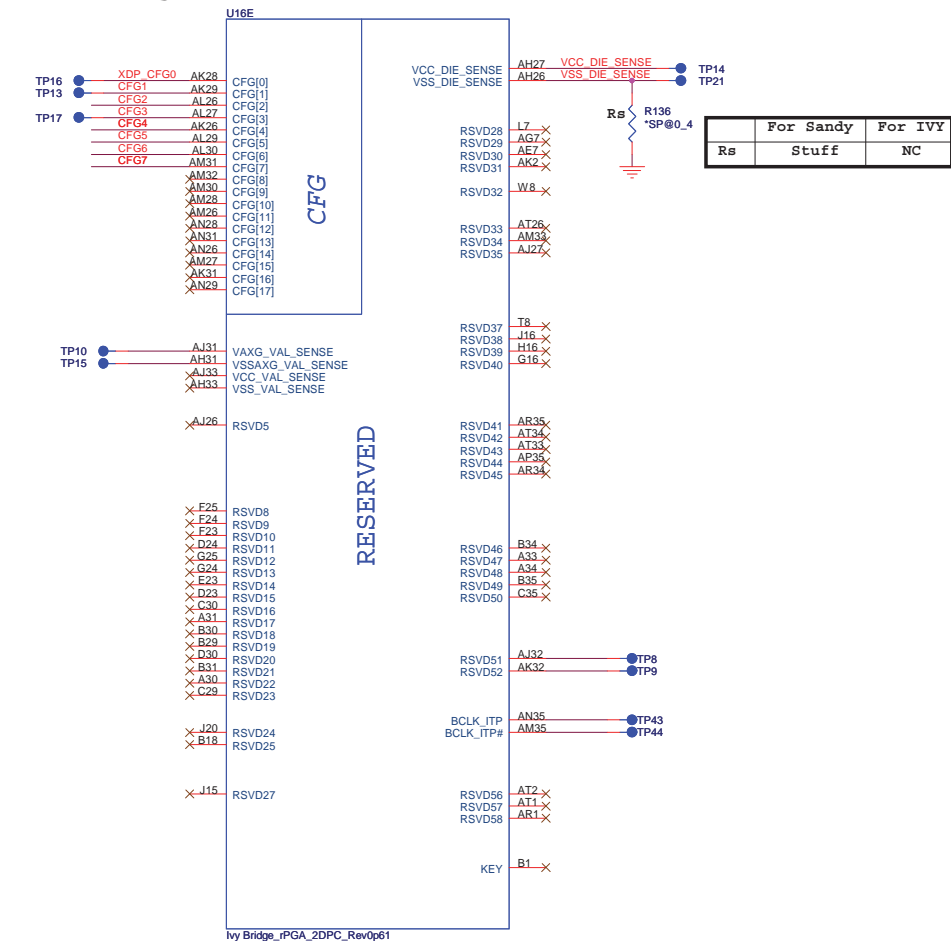
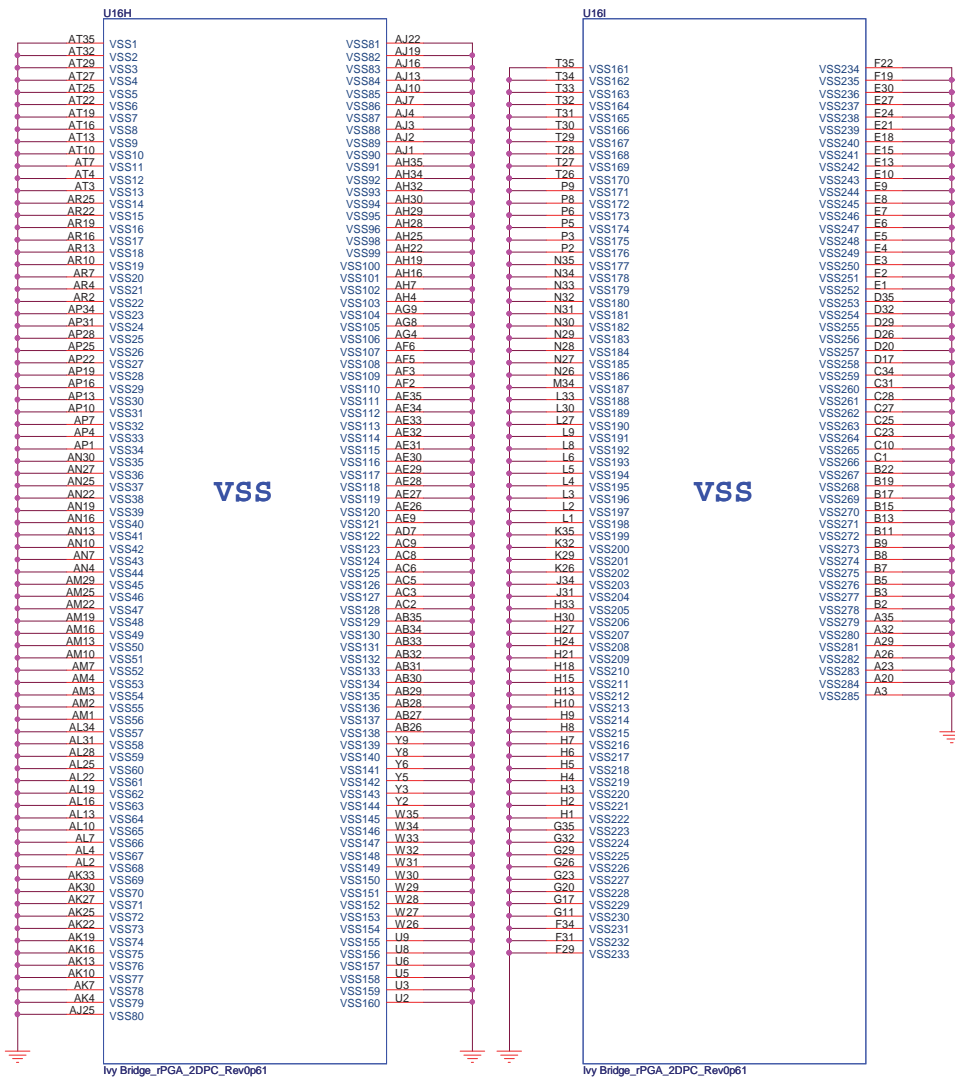
**CPU MCH**  
 IVY 45W: 5A  
 Spec  
 330uF/6mohm x 1  
 10uF x 6  
 Real  
 10uF x 8

Voltage selection for VCCIO:  
 | this pin must be pulled high on the motherboard  
 | On CRB  
 | H\_SNB\_IVB#\_PWRCTRL = low, 1.0V  
 | L\_SNB\_IVB#\_PWRCTRL = high/NC, 1.05V

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# IVY Bridge Processor (GND)

# IVY Bridge Processor (RESERVED, CFG)

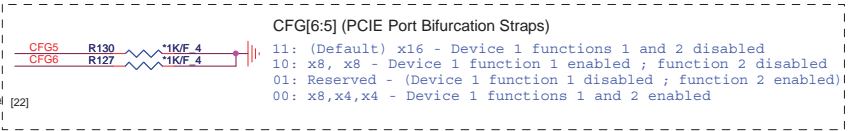
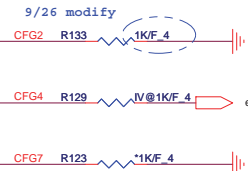


	For Sandy	For IVY
Rs	Stuff	NC

## Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



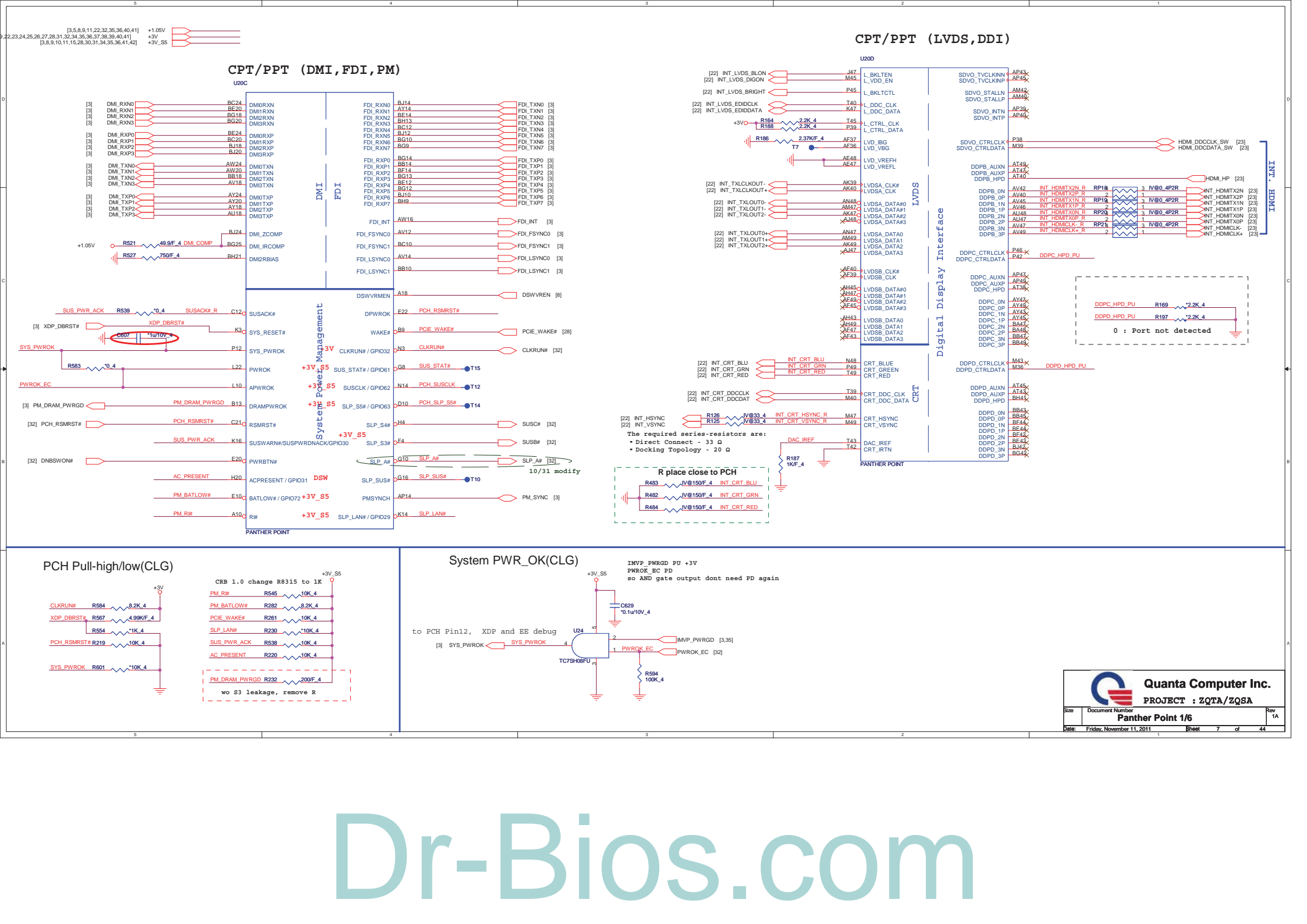
CFG[6:5] (PCIe Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled  
 10: x8, x8 - Device 1 function 1 enabled, function 2 disabled  
 01: Reserved - (Device 1 function 1 disabled; function 2 enabled)  
 00: x8, x4, x4 - Device 1 functions 1 and 2 enabled

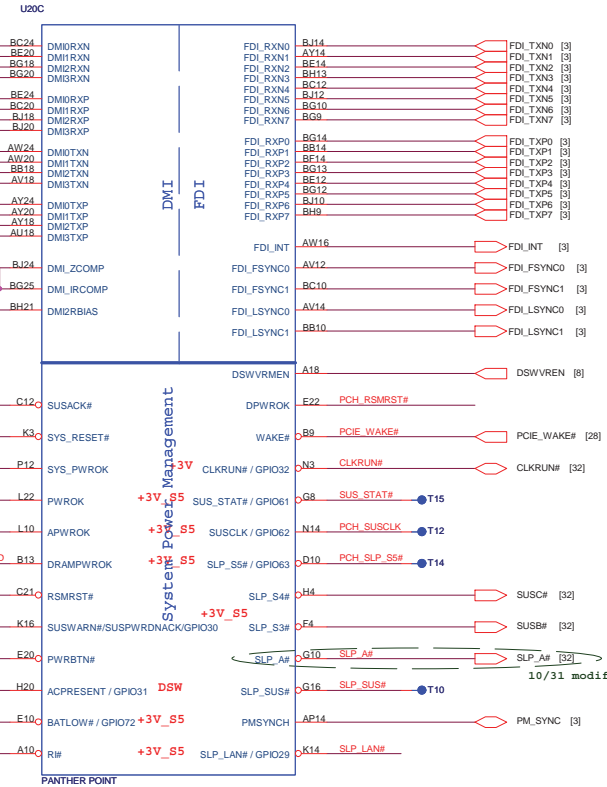


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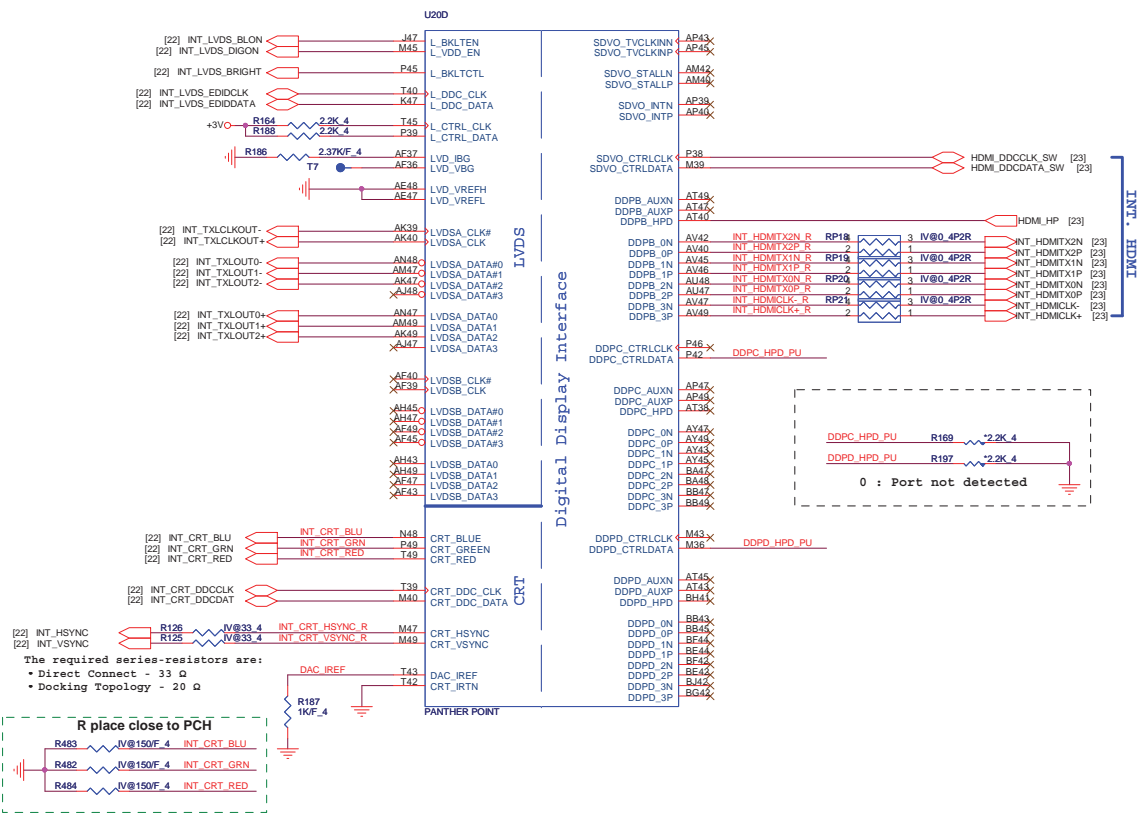
# Dr-Bios.com



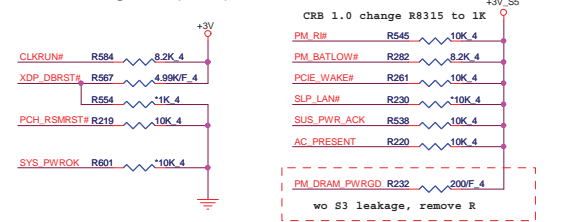
**CPT/PPT (DMI, FDI, PM)**



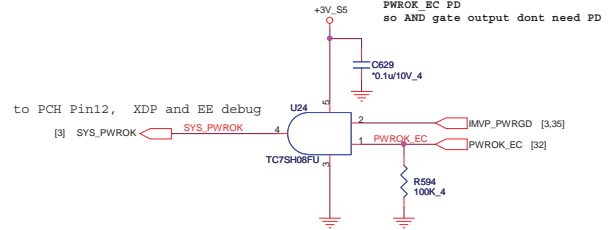
**CPT/PPT (LVDS, DDI)**



**PCH Pull-high/low (CLG)**



**System PWR\_OK (CLG)**



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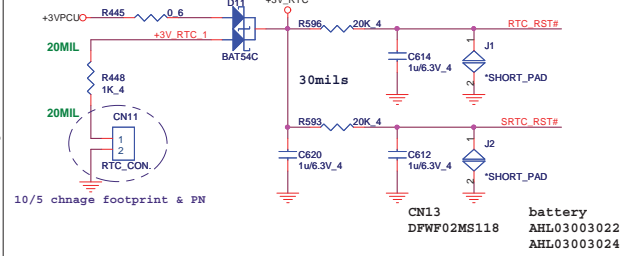
**PROJECT : ZQTA/ZQSA**

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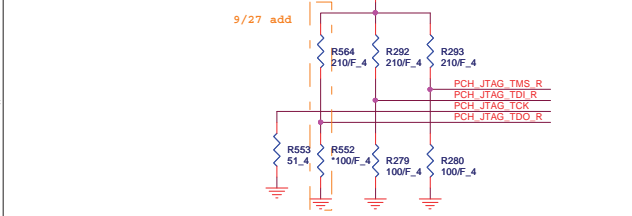
# RTC Circuitry(RTC)



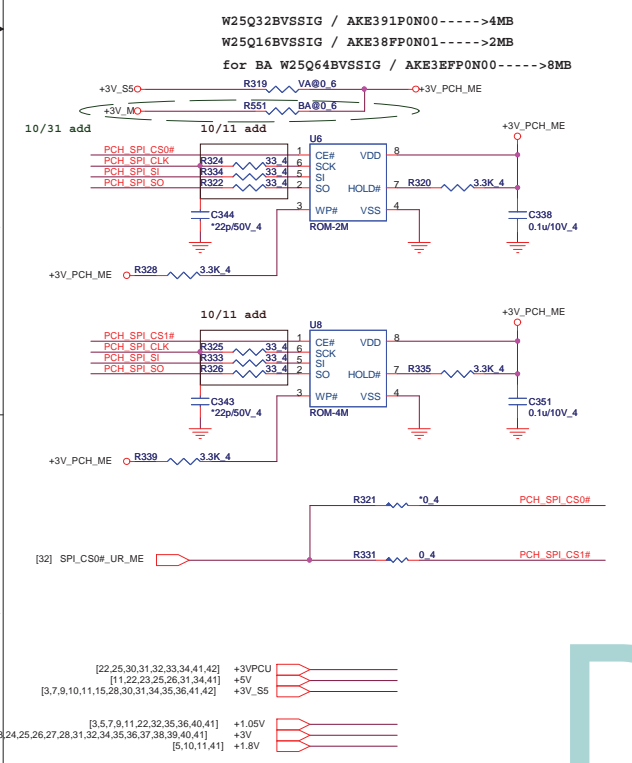
# HDA Bus(CLG)



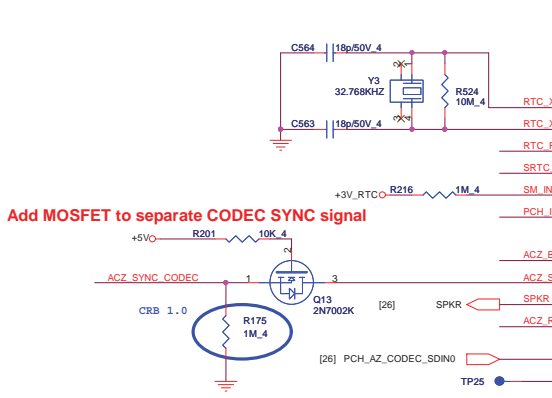
# PCH JTAG Debug (CLG)



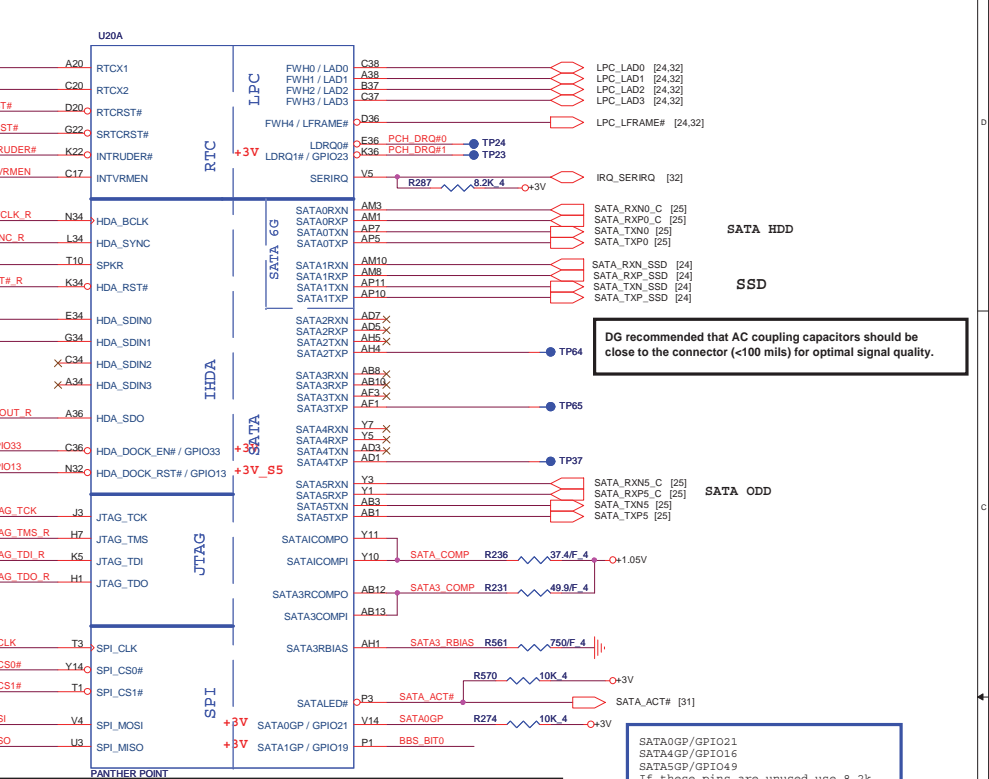
# PCH Dual SPI (CLG) (Default for WIN8)



# PCH2 (CLG)



# CPT/PPT (HDA, JTAG, SATA)



# PCH Strap Table

Pin Name	Strap description	Sampled	Configuration										
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V<sub>V</sub> R301 1K 4 SPKR									
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R171 1K 4 PCI_GNT3# [9]									
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC<sub>V</sub> R526 330K 4 PCH_INVRMEN									
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"> <thead> <tr> <th>GNT1#</th> <th>GNT0#</th> <th>Boot Location</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>1</td> <td>SPI *</td> </tr> <tr> <td>0</td> <td>0</td> <td>LPC</td> </tr> </tbody> </table>	GNT1#	GNT0#	Boot Location	1	1	SPI *	0	0	LPC	R473 1K 4 BBS_BIT1 [9]
GNT1#	GNT0#	Boot Location											
1	1	SPI *											
0	0	LPC											
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		R558 1K 4 BBS_BIT0									
HDA_SDO	Flash Descriptor Security	RSMRST	0 = effect (default)(weak pull-down 20K) 1 = overridden	[32] ME_WR R505 SHORT 4 ACZ_SDOUT_R									
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss (weak pull-down 20K) 1 = Set to Vcc	R548 2.2K 4 H_SNB_IVB# [3] R546 1K 4 DF_TVS [10] 0930									
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (weak pull-up 20K)	R277 1K 4 PLL_ODVR_EN [10]									
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3V_S5<sub>V</sub> R177 1K 4 ACZ_SYNC_R									
GPIO15	Intel ME Crypto Transport Layer Security (TLS) cipher suite internal PD	RSMRST	0 = Disable (Default) 1 = Enable	+3V_S5<sub>V</sub> R563 1K 4 PCH_GPIO15 [10]									
DSWVREN	DEEP S4/S5 well On Die DSW VR Enable	DSW	High = Enable (Default) Low = Disable	+3V_RTC<sub>V</sub> R530 330K 4 DSWVREN [7] R528 330K 4									
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)	+1.8V<sub>V</sub> R308 1K 4 NV_ALE [9]									

SATA0GP/GPIO21  
SATA4GP/GPIO16  
SATA5GP/GPIO49  
If these pins are unused use 8.2k to 10k pull-up to +Vcc3\_3 or 8.2k to 10k pull-down to ground

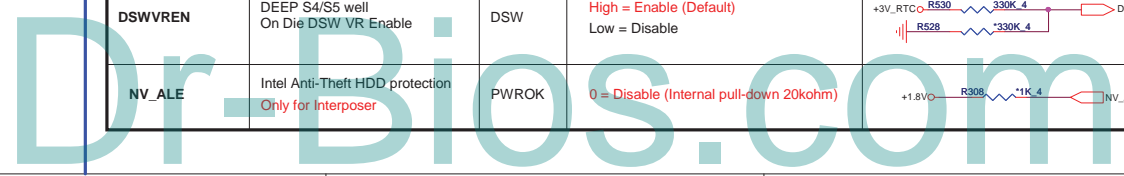
Used as GPIO only. at chklist 1.2

Default weak pull-up on GNT0/1#  
[Need external pull-down for LPC BIOS]

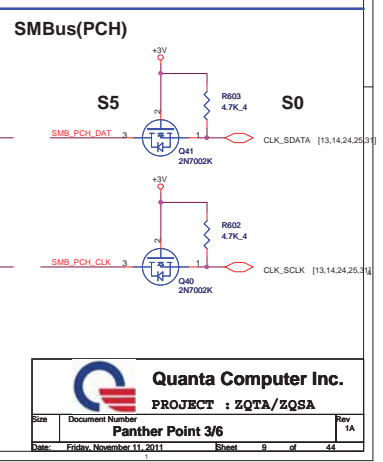
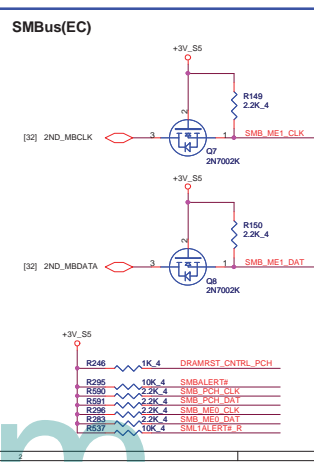
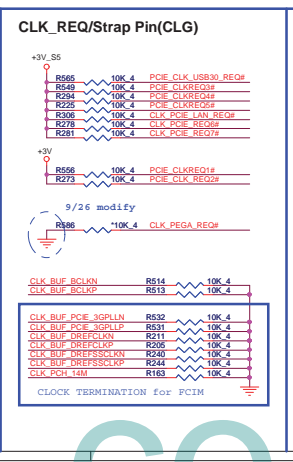
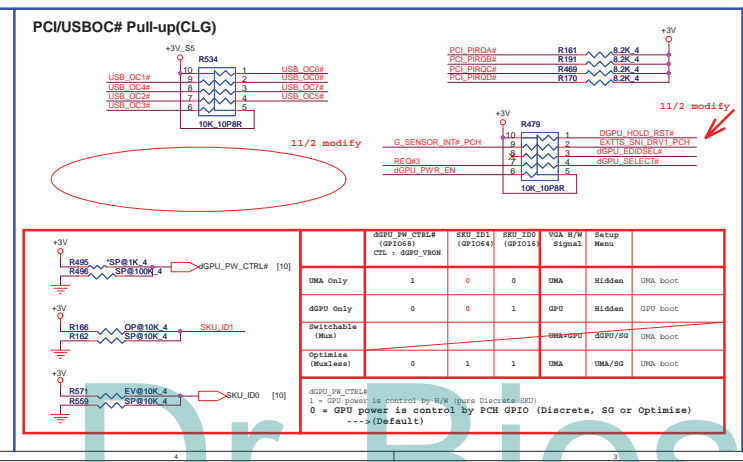
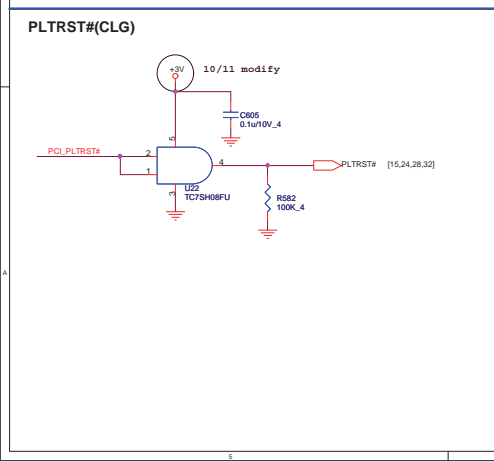
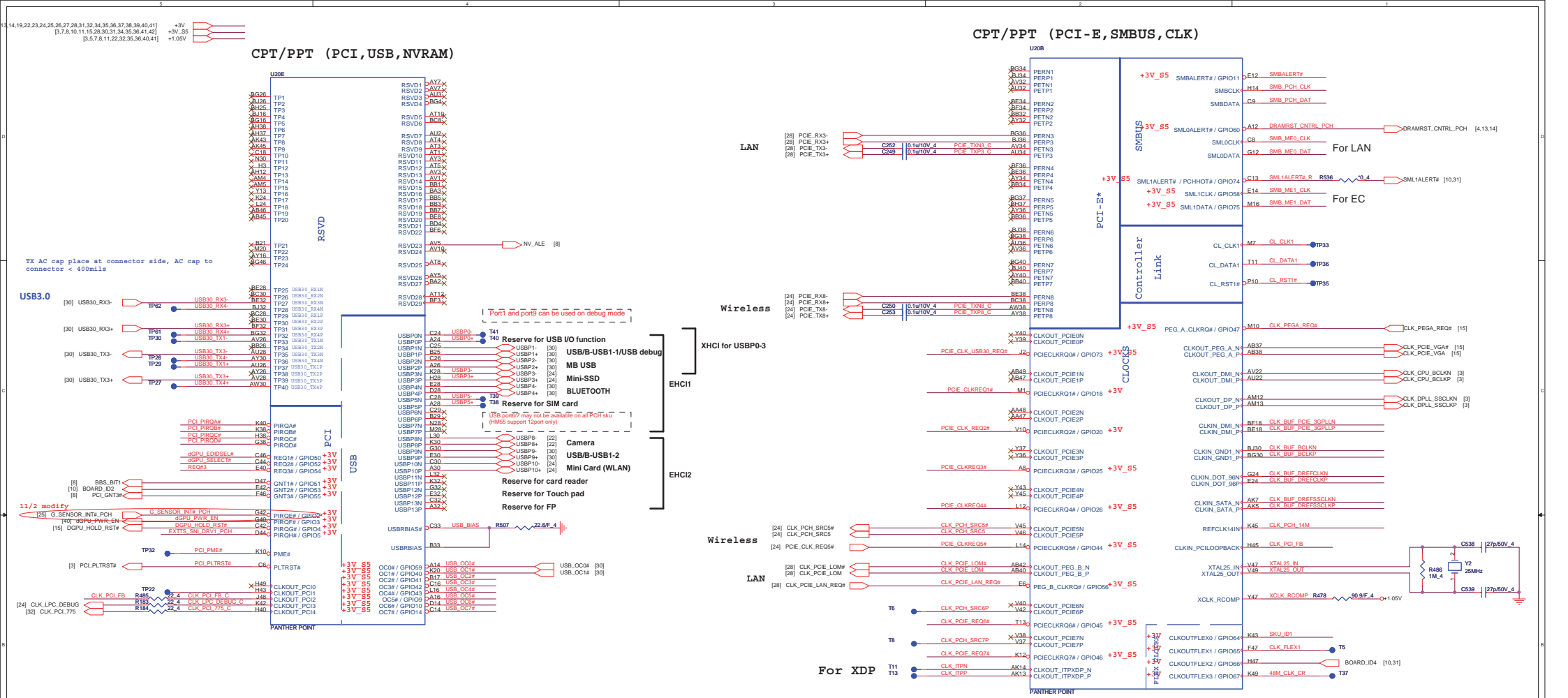
ME\_WR default EC setting folating

for future CPU, Sandy Bridge MC  
DF\_TVS needs to be pulled up to VccDFTERRM power rail through 2.2 kohm ±5% - R8361 change to 0 or not??

Needs to be pulled High for Huron River platform.  
chklist 1.2

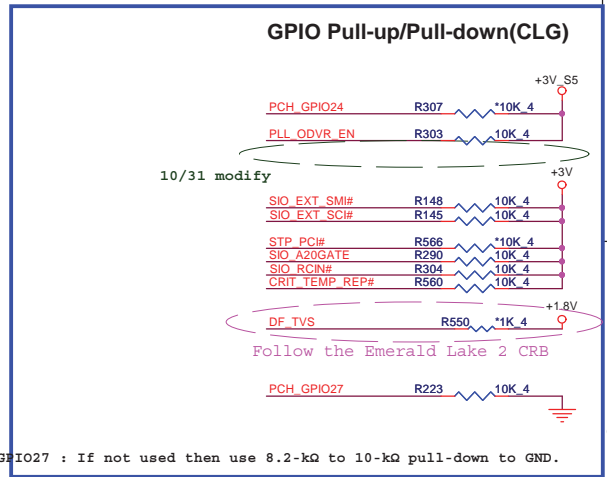
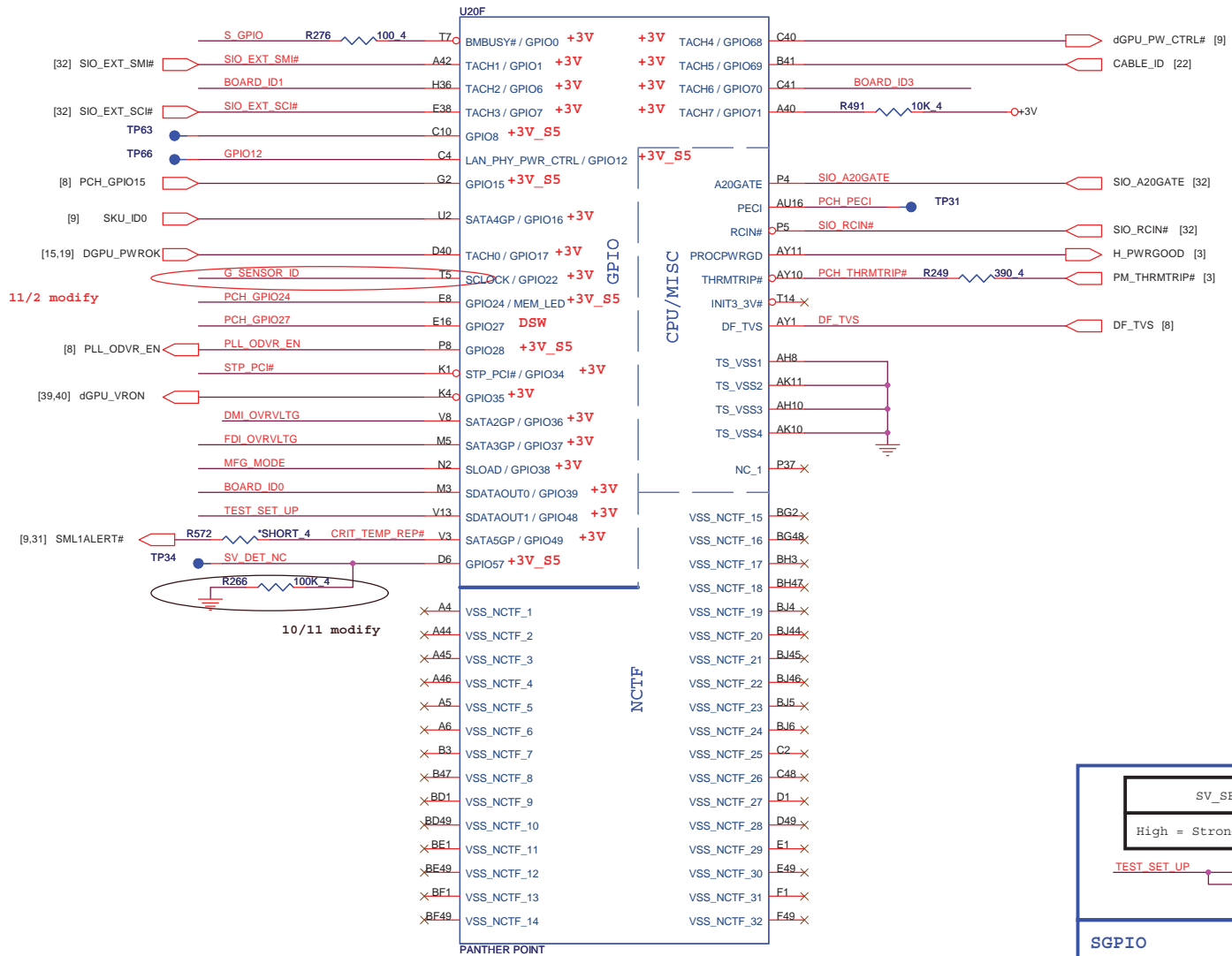




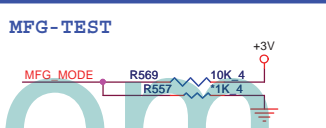
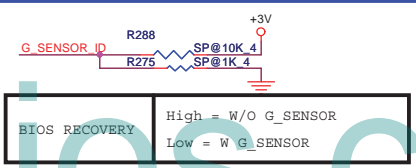
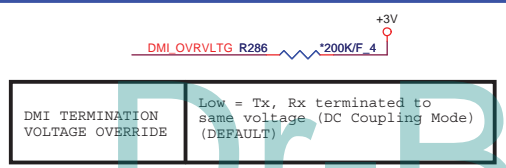
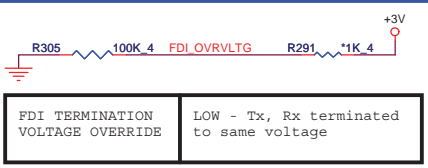
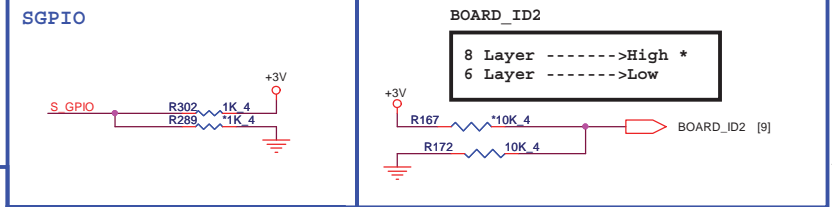
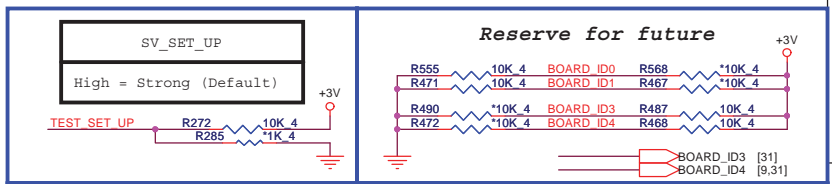


9,22,23,24,25,26,27,28,31,32,34,35,36,37,38,39,40,41] +3V  
 [3,7,8,9,11,15,28,30,31,34,35,36,41,42] +3V\_S5

### CPT/PPT (GPIO, VSS\_NCTF, RSVD)



SATA2GP : strap for reserved at chklist 1.2  
 SATA3GP : strap for reserved at chklist 1.2  
 NOTE: The internal pull-down is disabled after PLTRST# deasserts.  
 NOTE: This signal should not be pulled high when strap is sampled.



**PROJECT : ZQTA/ZQSA**

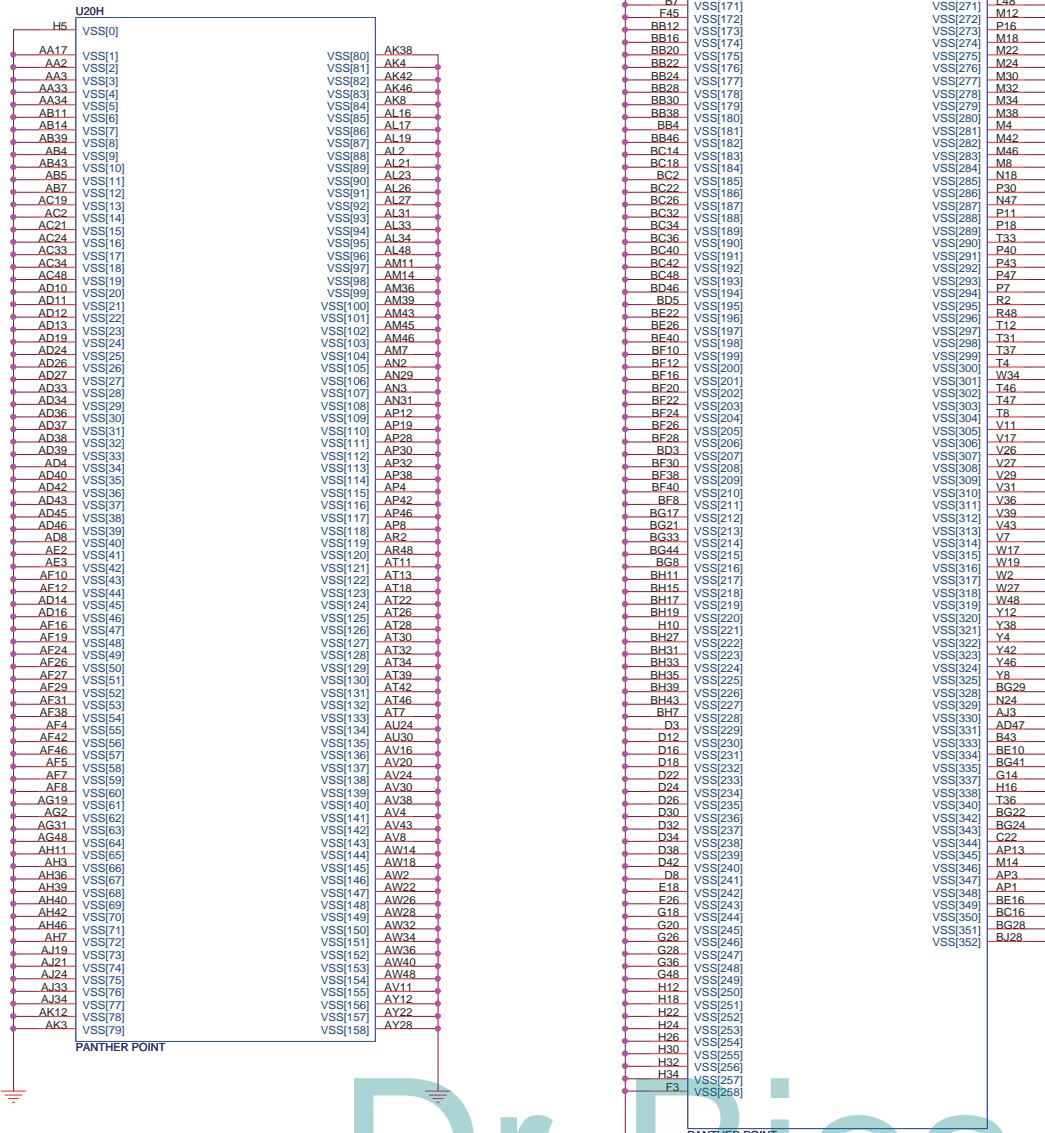
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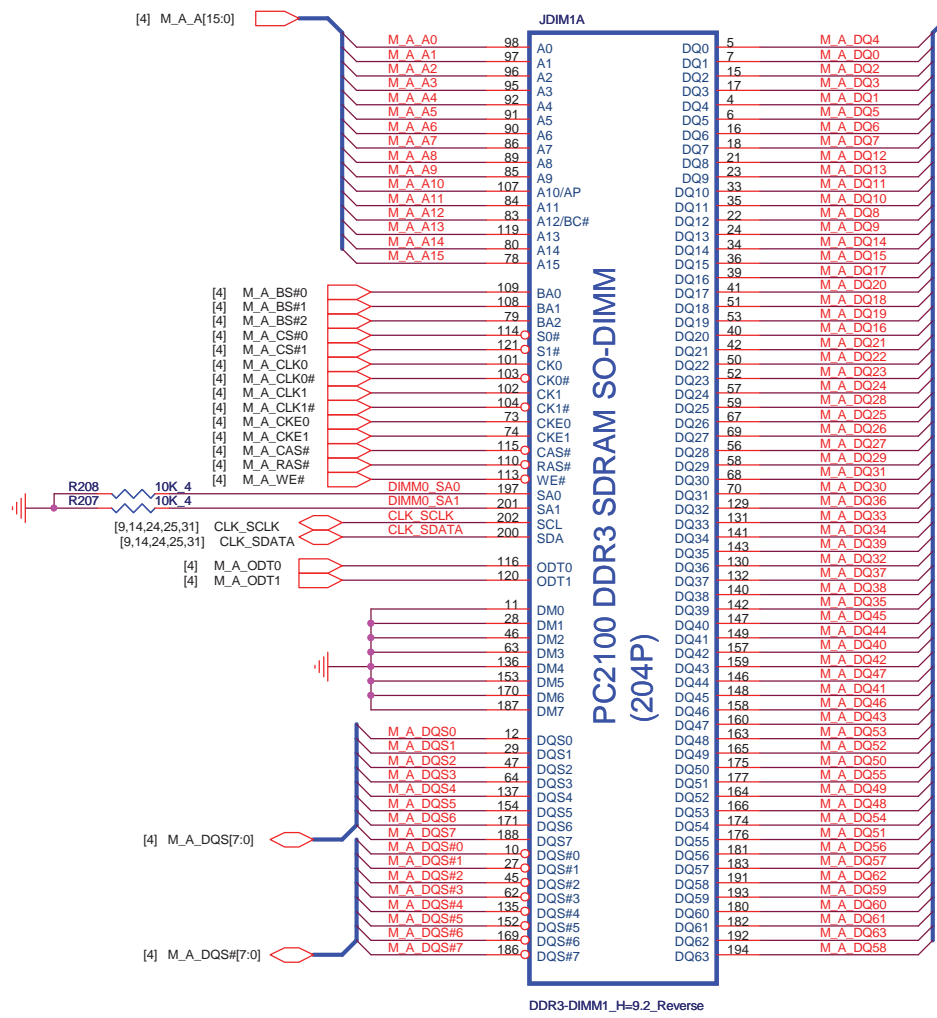


IBEX PEAK-M (GND)



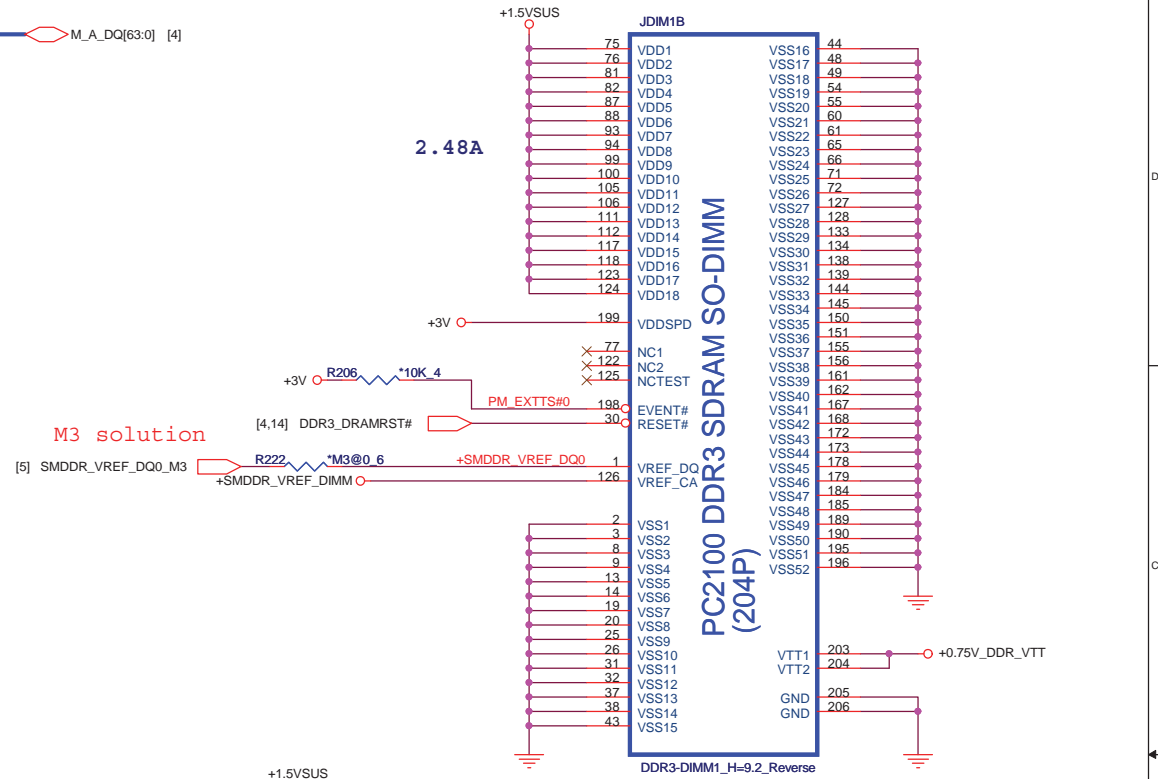
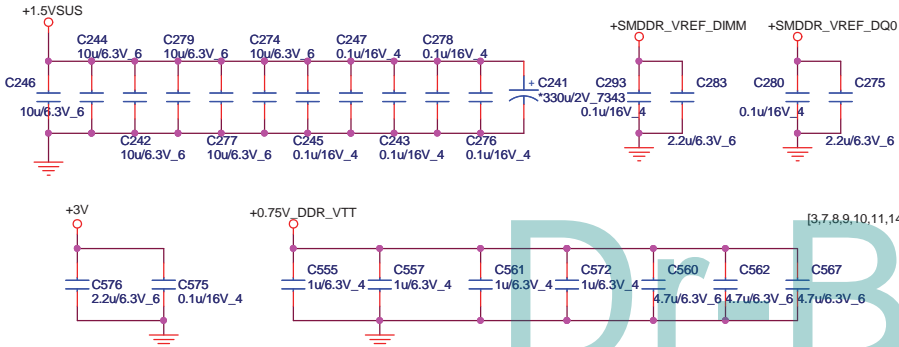
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**PROJECT : ZQTA/ZQSA**  
**Panther Point 6/6**

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		1A
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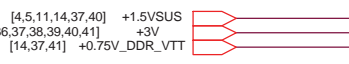
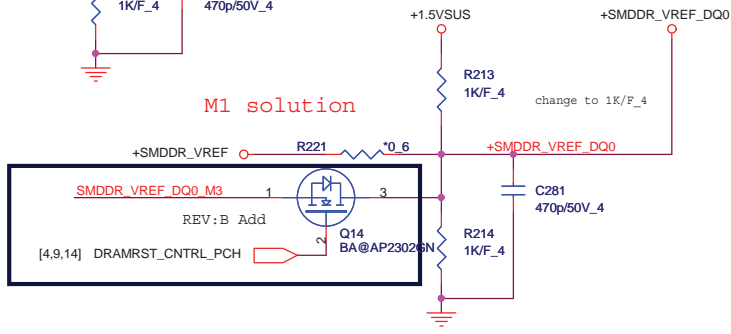
DDR3-DIMM1\_H=9.2\_Reverse

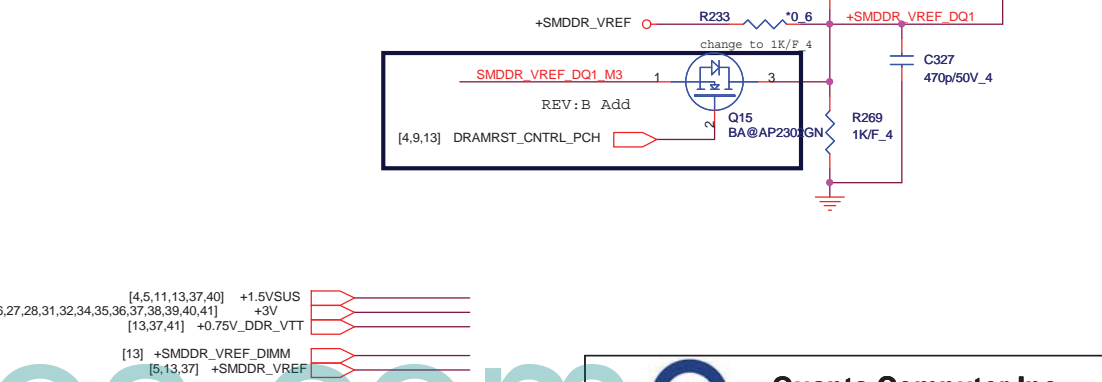
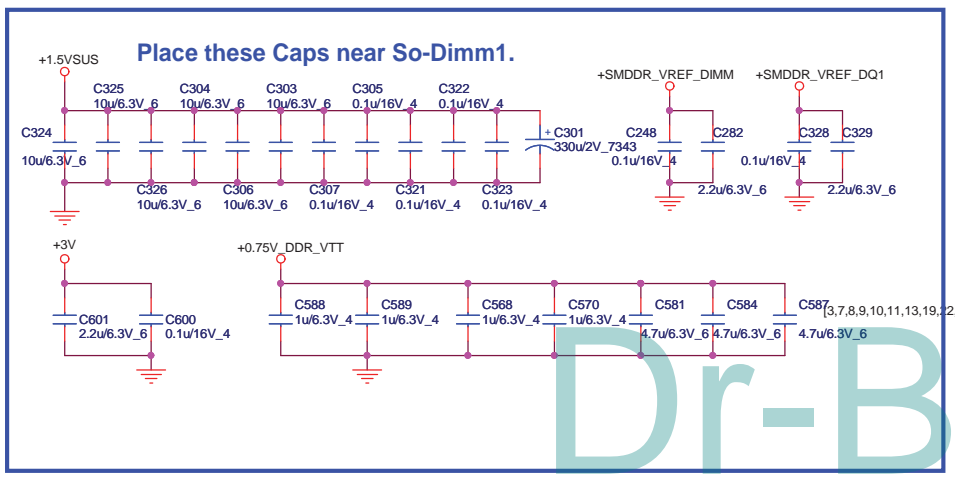
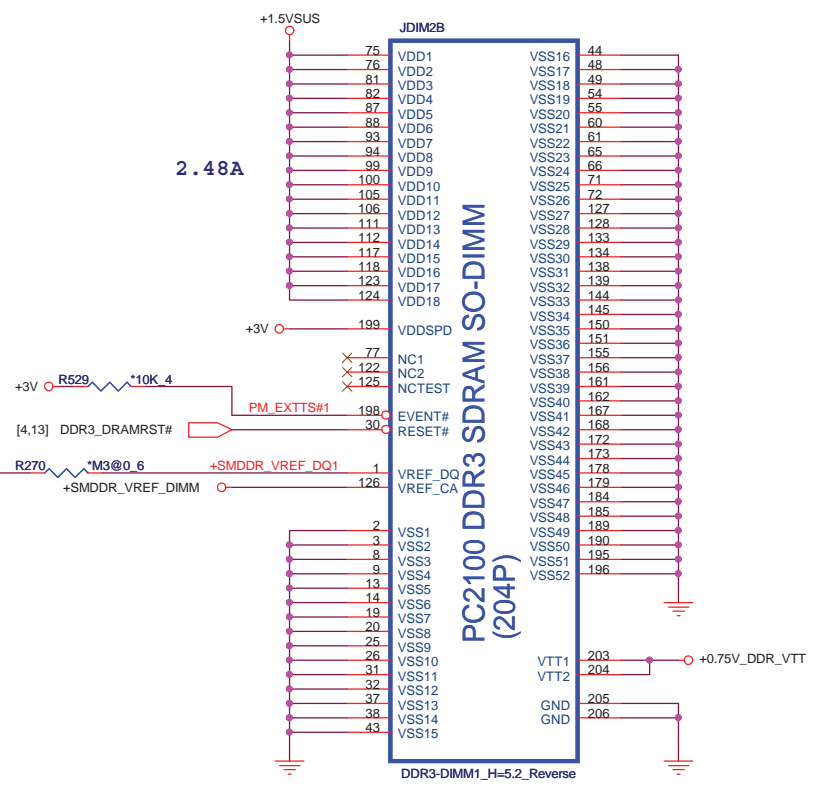
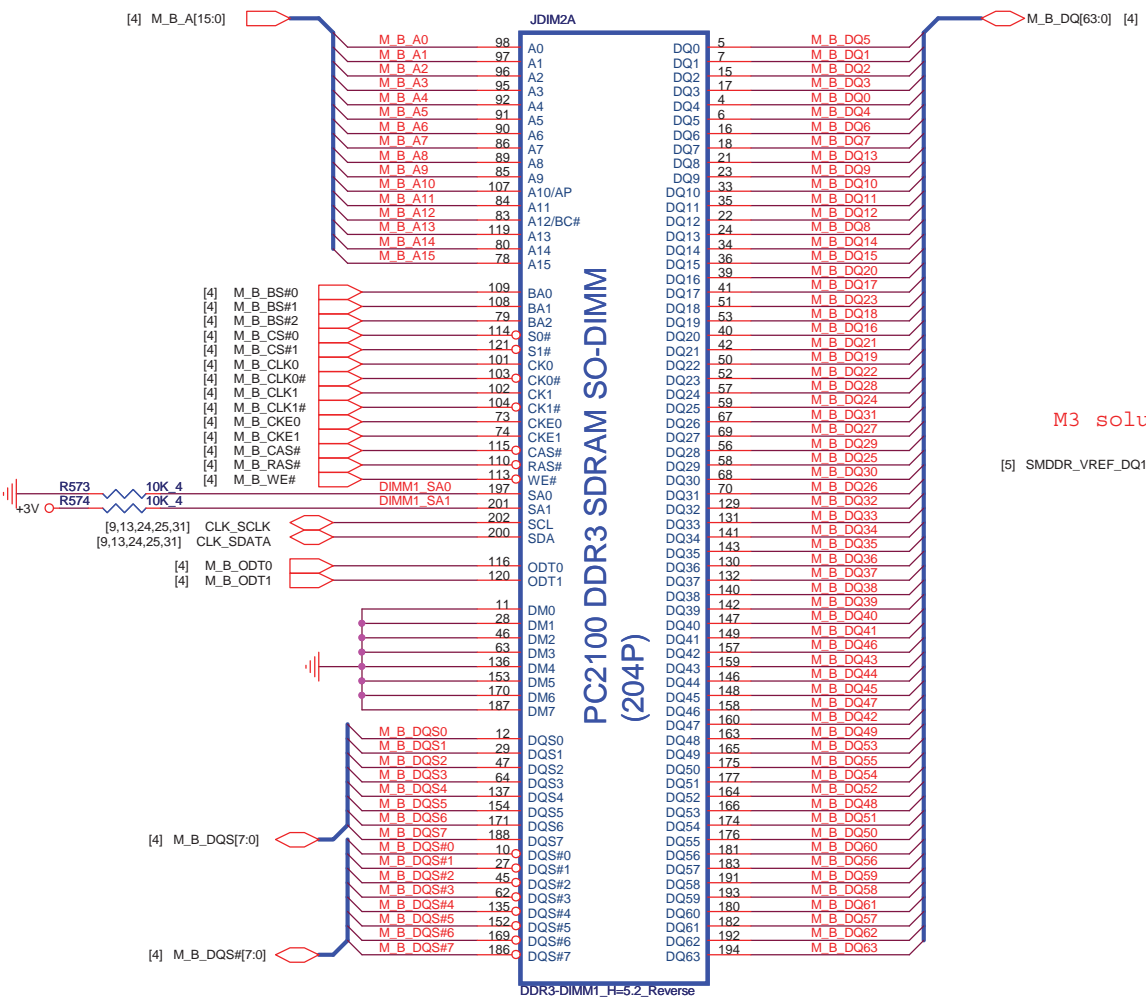
**Place these Caps near So-Dimm0.**



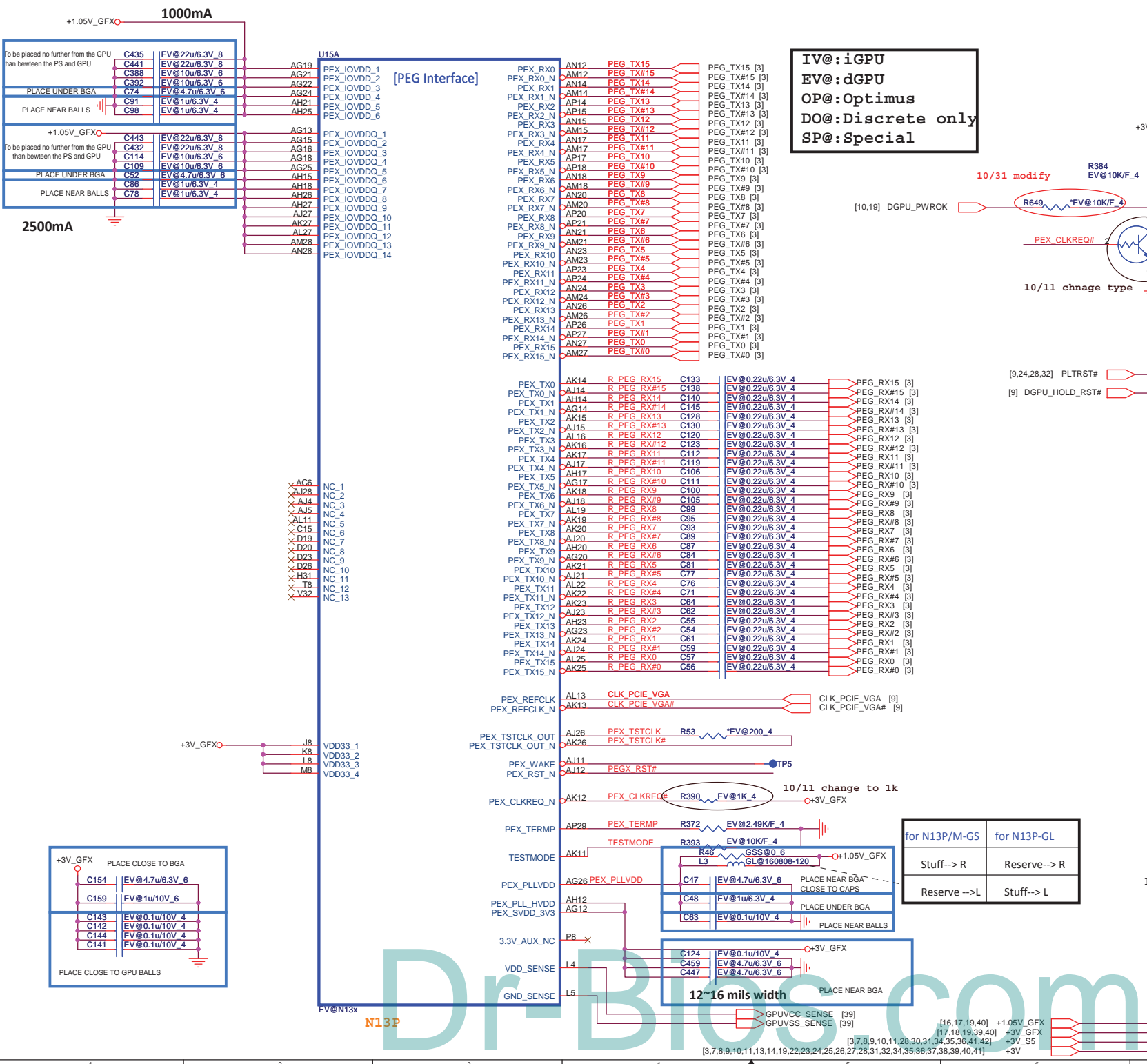
**M3 solution**

**M1 solution**





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N13P-GL	AJON13P0T02
N13P-GS	AJON13P0T07
N13M-GS	AJON13M0T08

**IV@:iGPU**  
**EV@:dGPU**  
**OP@:Optimus**  
**DO@:Discrete only**  
**SP@:Special**

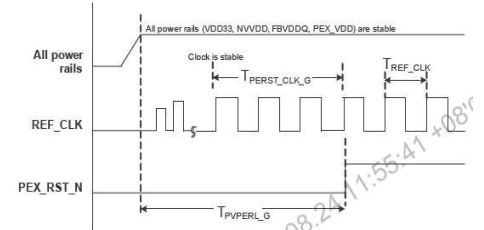
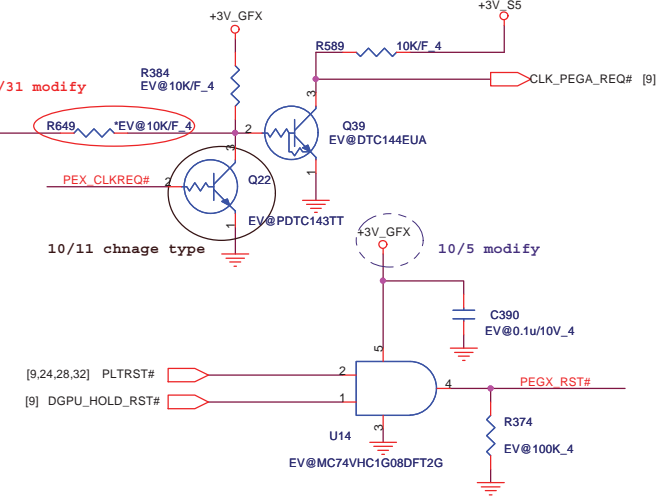
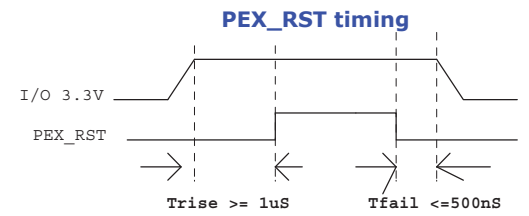
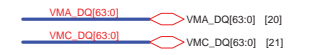
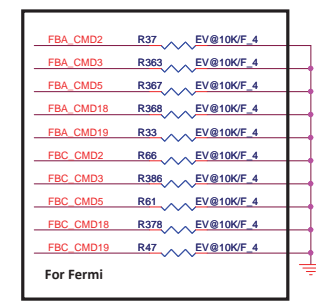
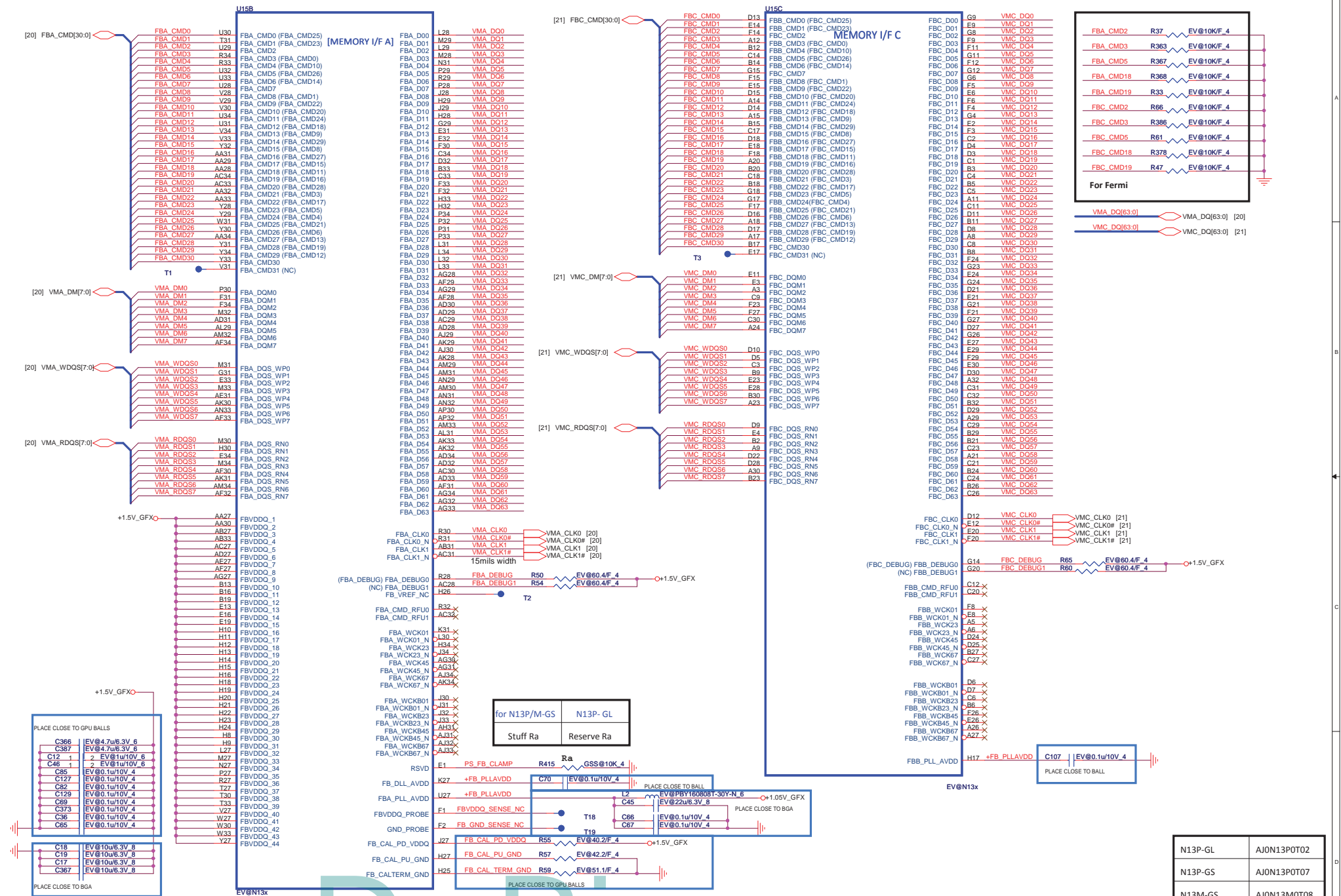


Figure 3-18. PEX\_RST\_N Timing for GPU  
 Table 3-8. N11x Reset Requirements for PCI Express 2.0

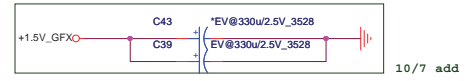
Constraint Parameter	Requirement	Notes
T <sub>P<sub>PERL_G</sub></sub>	T <sub>P<sub>PERL_G</sub></sub> ≥ 11ns	
T <sub>P<sub>ERST_CLK_G</sub></sub>	T <sub>P<sub>ERST_CLK_G</sub></sub> ≥ 1T <sub>REF_CLK</sub>	

	for N13P-M/G-S	for N13P-GL
Stuff--> R	Reserve--> R	
Reserve--> L	Stuff--> L	





N13P-GL	AJON13POT02
N13P-GS	AJON13POT07
N13M-GS	AJON13MOT08



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**PROJECT : ZQTA/ZQSA**

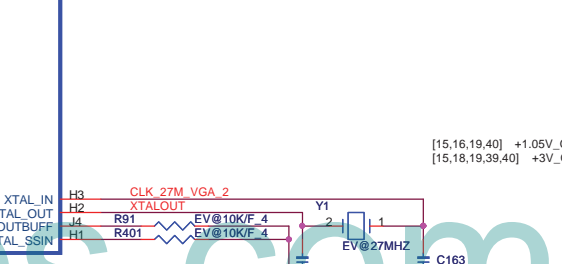
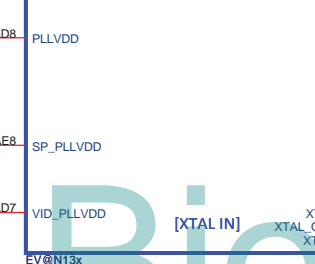
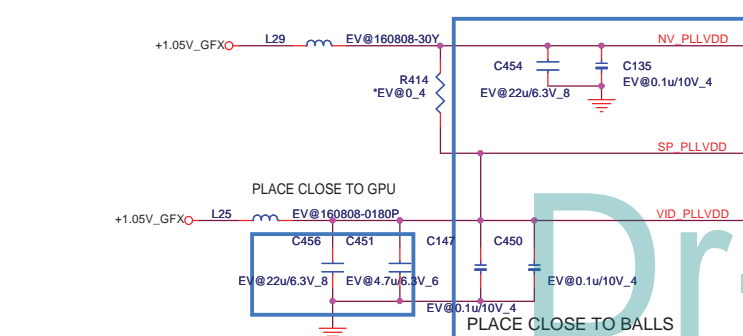
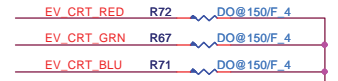
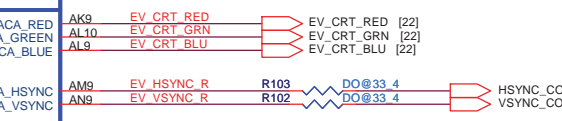
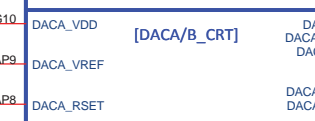
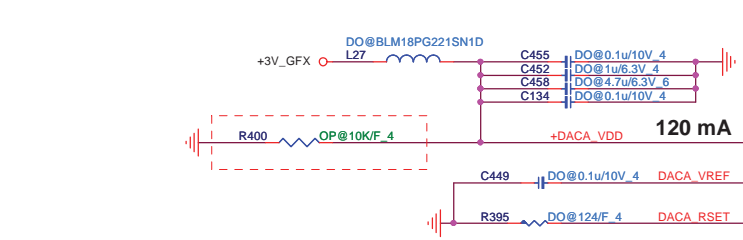
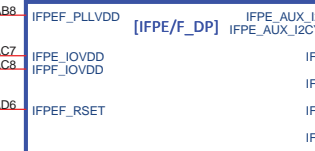
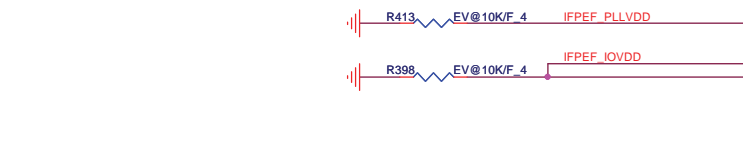
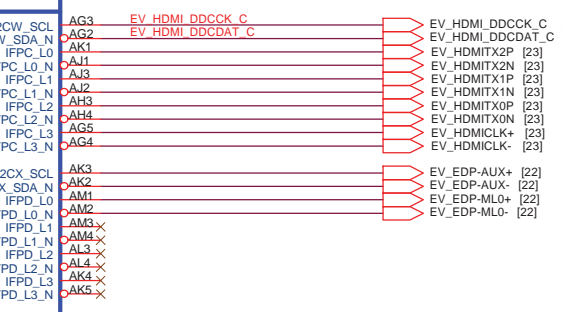
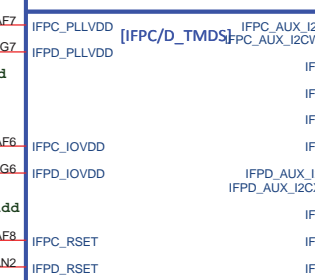
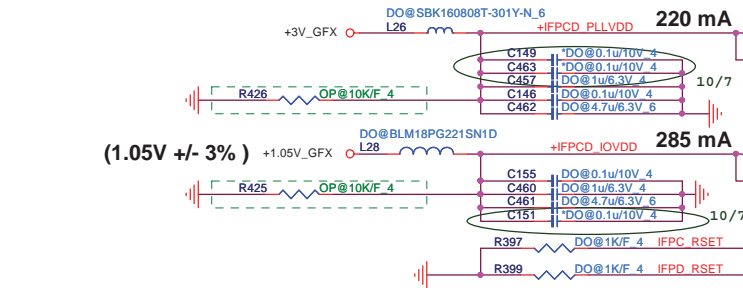
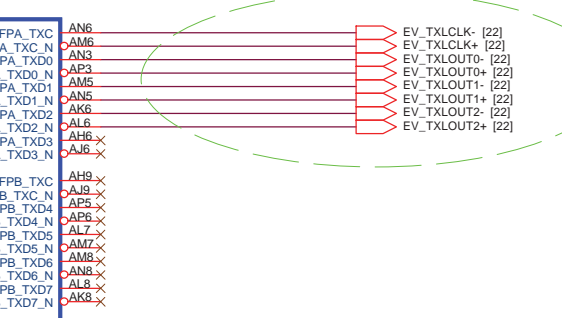
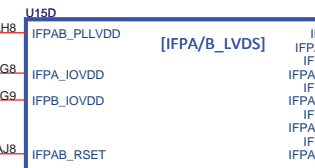
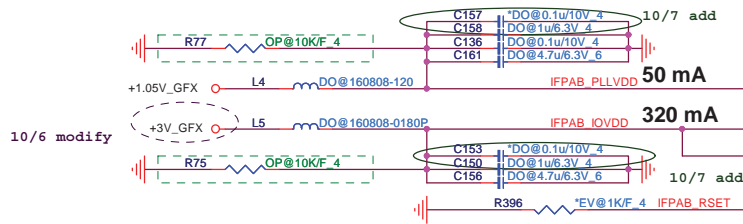
Size	Document Number	Rev
Date	DGPU Z/5 (Memory)	1A
Friday, November 11, 2011	Sheet	16 of 44



0929 Exchange + & - ; because symbol error

IV@:iGPU  
 EV@dGPU  
 OP@:Optimus  
 DO@:Discrete only  
 SP@:Special

N13P-GL	AJON13P0T02
N13P-GS	AJON13P0T07
N13M-GS	AJON13M0T08



[15,16,19,40] +1.05V\_GFX  
 [15,18,19,39,40] +3V\_GFX

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 PROJECT : ZQTA/ZQSA  
 Document Number: DGPU 3/5 (Display)  
 Date: Friday, November 11, 2011 Sheet 17 of 44

### Logical Strap Bit Mapping

	PU-VDD	PD
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

N13P-GL	AJON13P0T02
N13P-GS	AJ001070T00
N13M-GS	AJ001170T00

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	FB_1	FB_0	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM	1010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	1110
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	0010
STRAP4	RESERVED	PCI SPEED CHANGE GEN3	PCI_MAX SPEED	DP_PLL_VDD33	0011

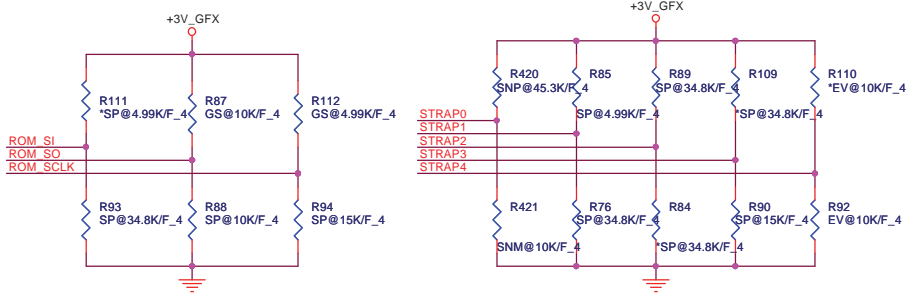
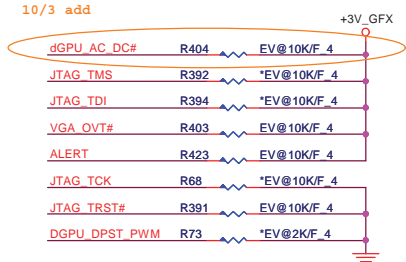
[15,17,19,39,40] +3V\_GFX

**STRAP2**  
N13P-GL (1001) --> 10k PU  
N13P-GS (1011) --> 20K PU

**STRAP1**  
N13P-GL (0111) --> 45.3k PD  
N13P-GS (0110) --> 34.8K PD

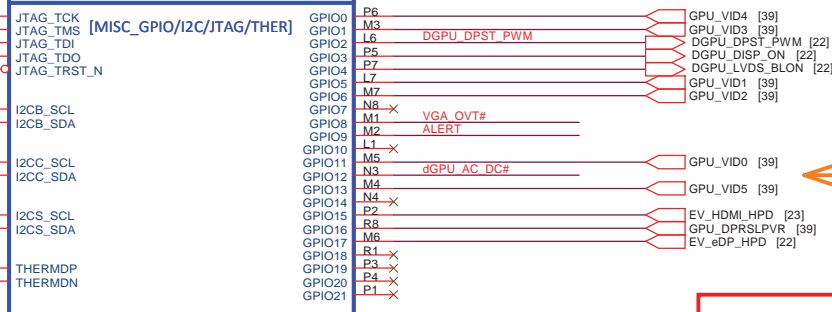
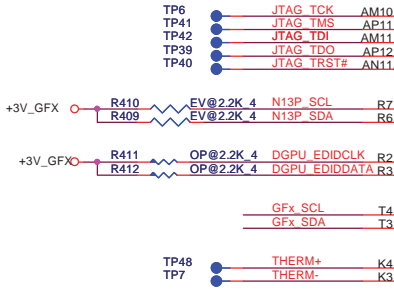
**STRAP3**  
Optimus --> 4.99k PD  
Discrete only --> 15K PD

**Resistor P/N**  
4.99K--> CS24992FB26  
10K --> CS31002FB26  
15K --> CS31502FB24  
20K --> CS32002FB29  
34.8K--> CS33482FB22  
45.3K --> CS34532FB18

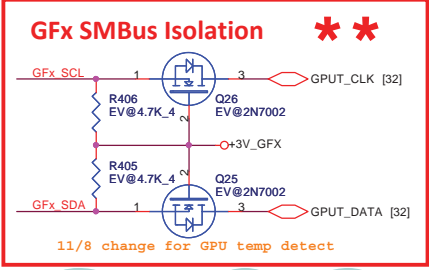
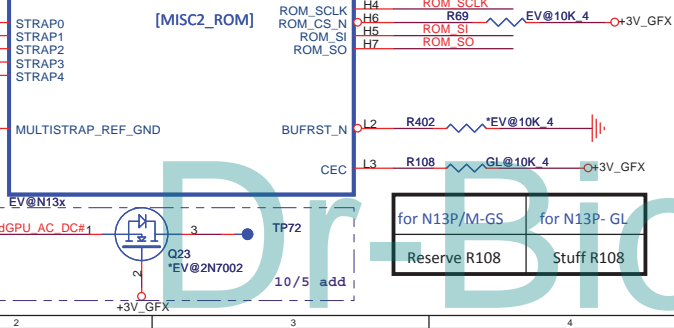
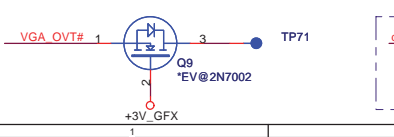


N13P-GS/-GL Strapping table

ROM_SI	1G Hynix 64Mx16 -->15K PD 1G Micron 64Mx16 -->20K PD 2G Hynix 128Mx16 -->35K PD (Default) 2G Micron 128Mx16 -->45K PD	ROM_SO	N13P-GL --> 10K PD N13P-GS --> 10K PU	ROM_SCLK	N13P-GL (0010) --> 15k PD N13P-GS (1000) --> 4.99K PU
--------	--	--------	--	----------	--



R422	
N13P-GS/GL	40.2K
N13M-GS	NC



N13M-GS Strapping table

Pin Name	Strap Mapping	Value
ROM_SCLK	SMB_ALT_ADDR	0
ROM_SI	SUB_VENDOR	0
ROM_SO	VGA_DEVICE	0
STRAP[3.0]	RAM_CFG[3.0]	0010(Hynix 64Mx16) 0110(Hynix 128Mx16)
STRAP[4]	PCIE_MAX_SPEED	0

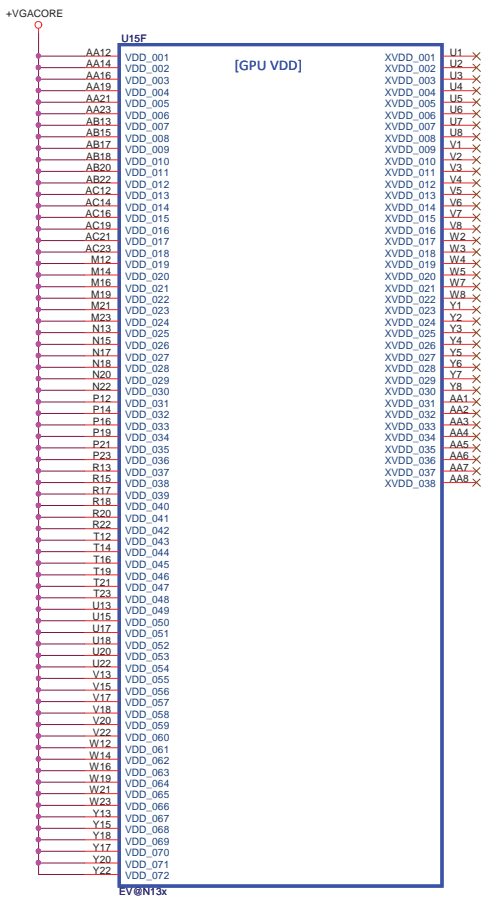
**Remark :**  
0 -> 10K PD  
1 -> 10K PU

for N13P/M-GS	for N13P-GL
Reserve R108	Stuff R108

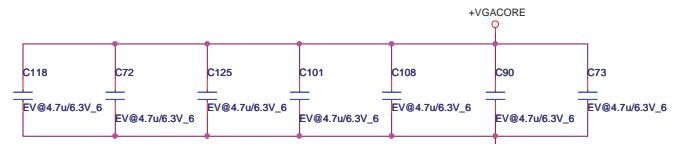
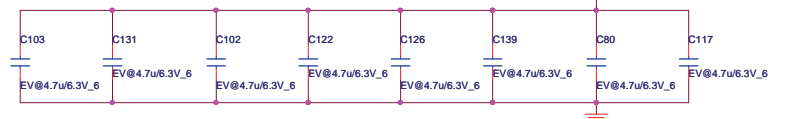
**Quanta Computer Inc.**  
PROJECT : ZQTA/ZQSA

Size	Document Number	Rev
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Date:	Friday, November 11, 2011	Sheet 18 of 44

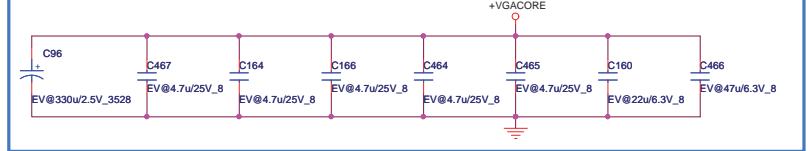
N13P-GL	AJON13POT02
N13P-GS	AJON13POT07
N13M-GS	AJON13MOT08



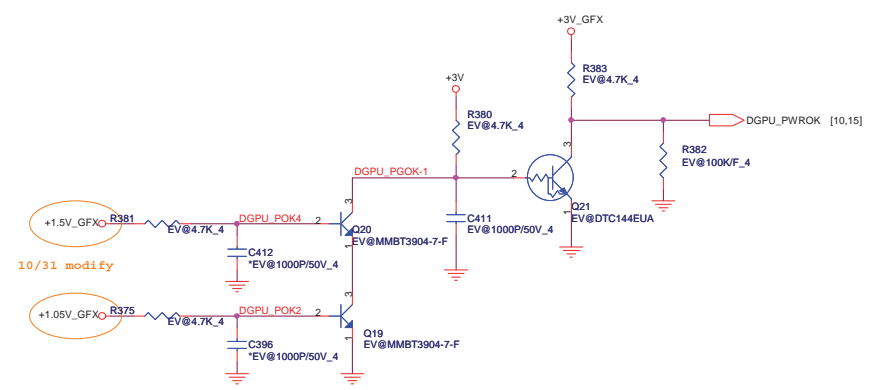
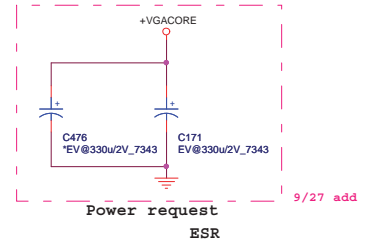
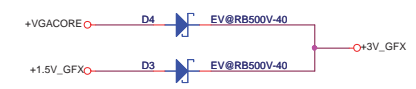
PLACE UNDER GPU



PLACE NEAR GPU



for meet Power down sequence for +3V\_GFX

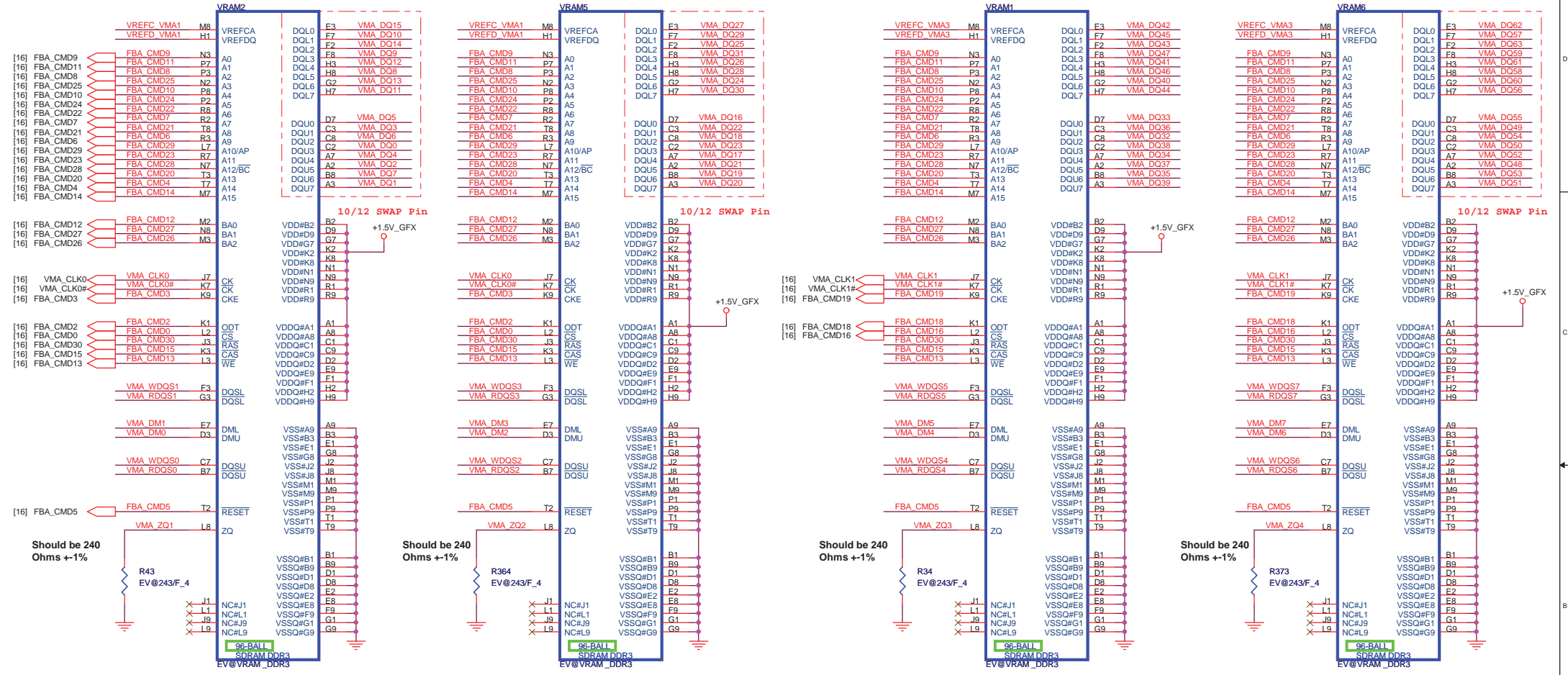


[31,39]	+VGACORE
[15,16,17,40]	+1.05V_GFX
[16,20,21,40]	+1.5V_GFX
[15,17,18,39,40]	+3V_GFX
[3,7,8,9,10,11,13,14,22,23,24,25,26,27,28,31,32,34,35,36,37,38,39,40,41]	+3V

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[16] VMA\_DQ[63..0]  
[16] VMA\_DM7..0  
[16] VMA\_WDQS7..0  
[16] VMA\_RDQS7..0

# CHANNEL A: 256MB/512MB DDR3

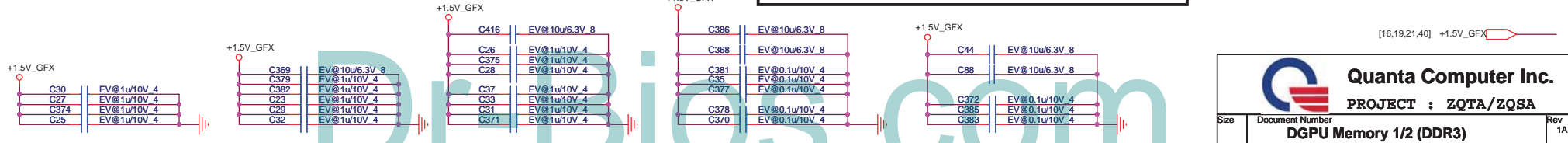


VMA\_CLK0  
R371 EV@162/F\_4

Fermi : Change to 160 ohm  
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5% (0402)  
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1% (0402)

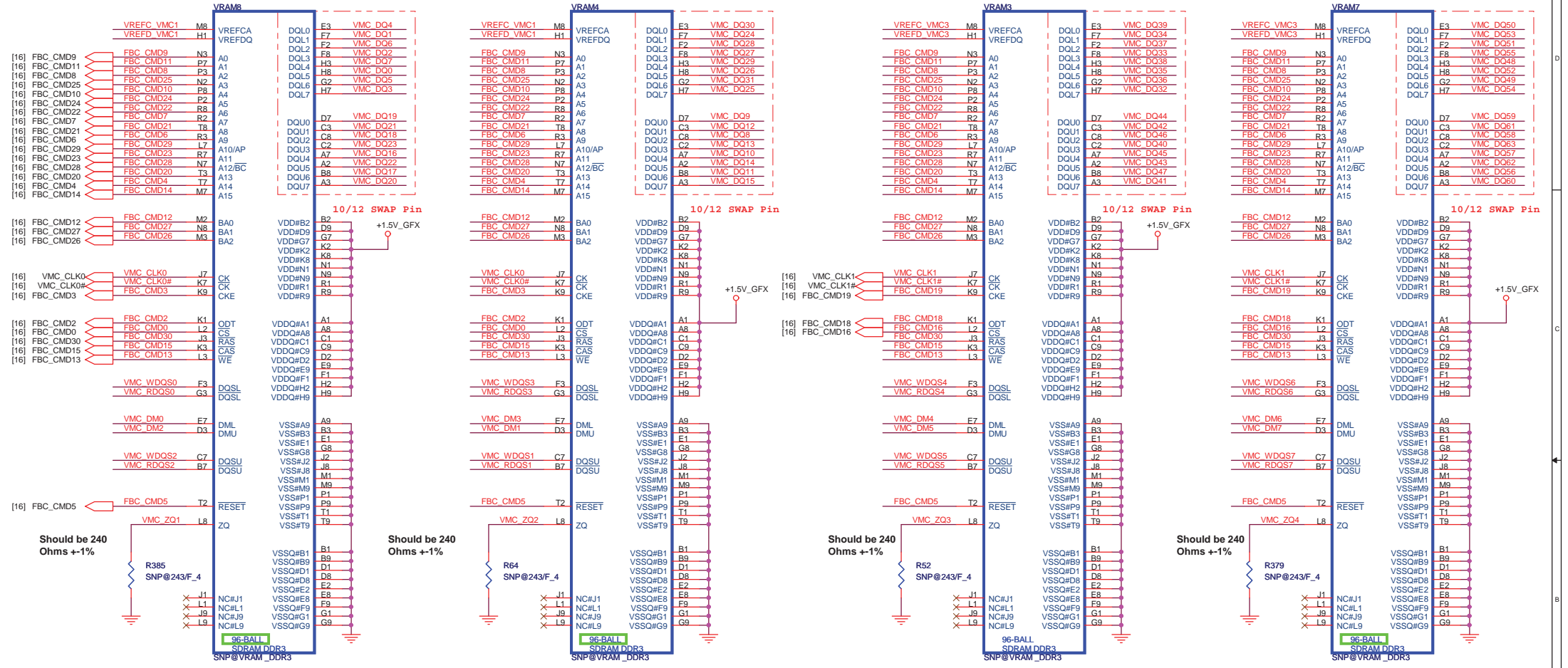
VMA\_CLK1  
R41 EV@162/F\_4

Fermi : Change to 160 ohm  
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5% (0402)  
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1% (0402)



[16] VMC\_DQ[63..0]  
[16] VMC\_DM[7..0]  
[16] VMC\_WDQS[7..0]  
[16] VMC\_RDQS[7..0]

# CHANNEL B: 256MB/512MB DDR3

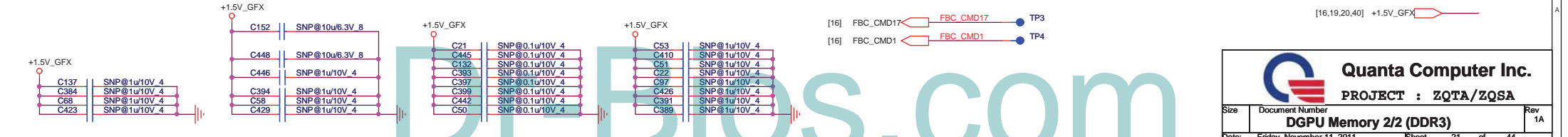


VMC\_CLK0  
R388 SNP@162/F\_4

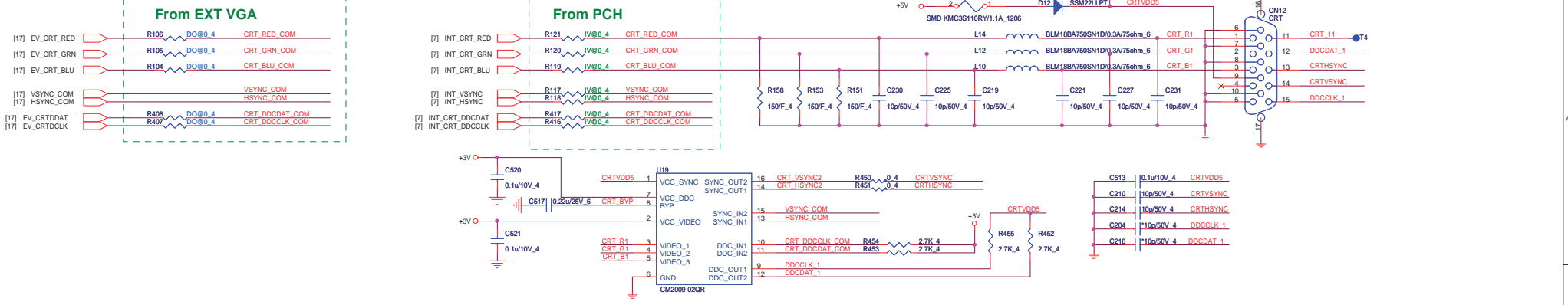
Fermi : Change to 160 ohm  
1 : CS11602JB00 ,RES CHIP 160 1/16W +5% (0402)  
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1% (0402)

VMC\_CLK1  
R49 SNP@162/F\_4

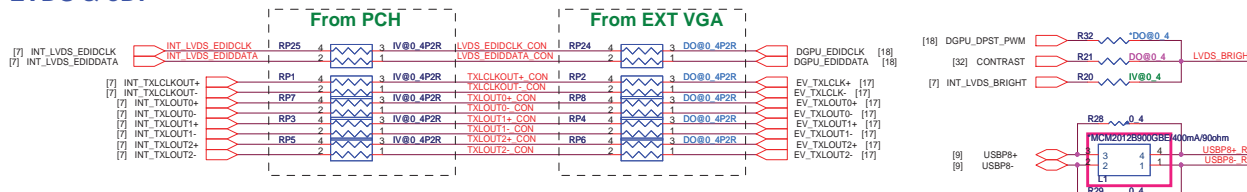
Fermi : Change to 160 ohm  
1 : CS11602JB00 ,RES CHIP 160 1/16W +5% (0402)  
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1% (0402)



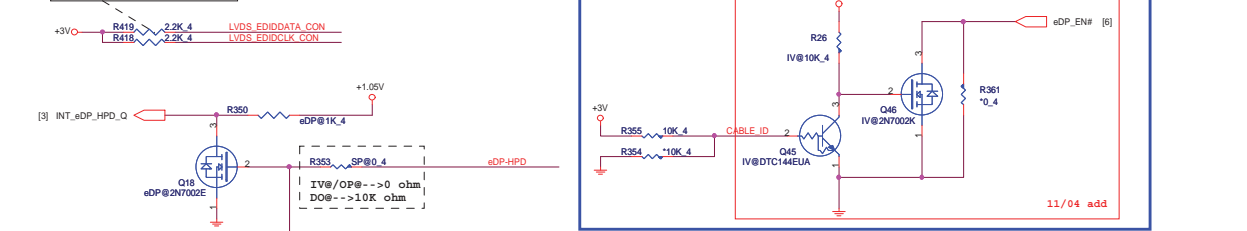
# CRT



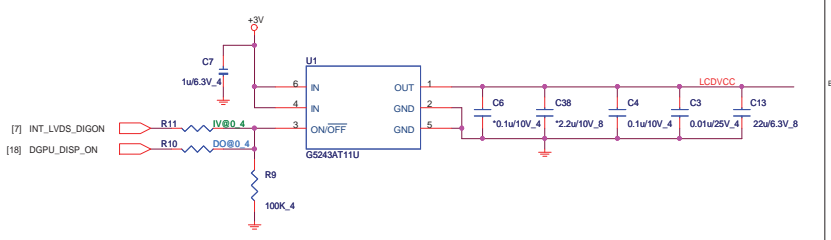
# LVDS & eDP



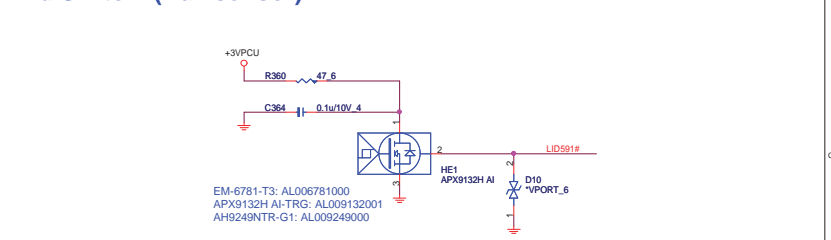
Enable/Disable LVDS  
Pull Up---->Enable  
NC-->Disable



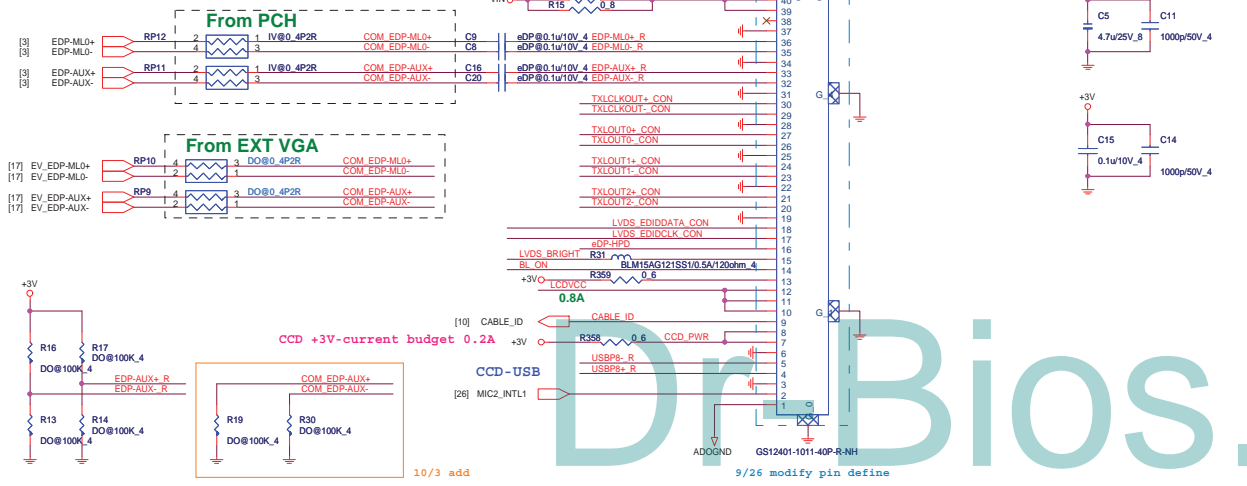
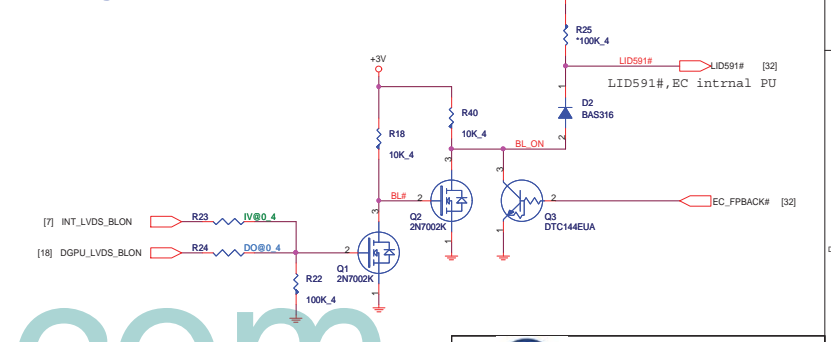
# LCD Power



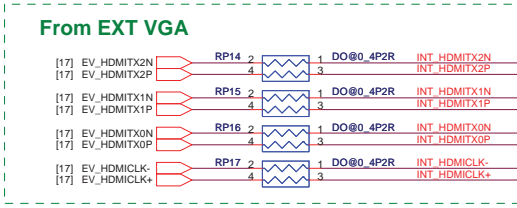
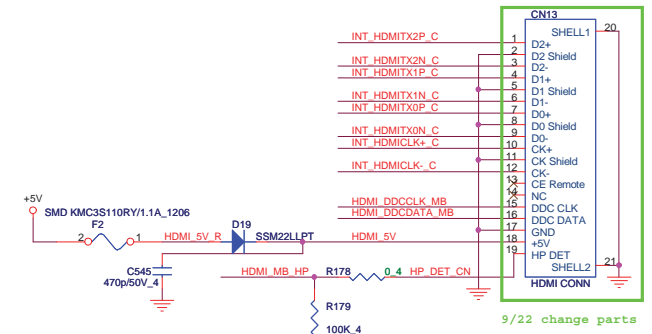
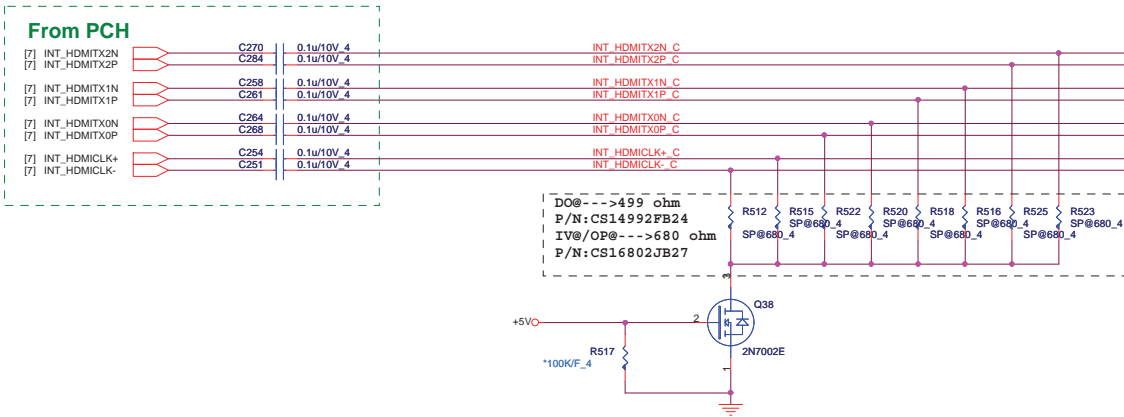
# Lid Switch (Hall sensor)



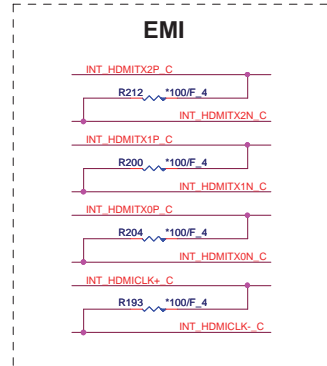
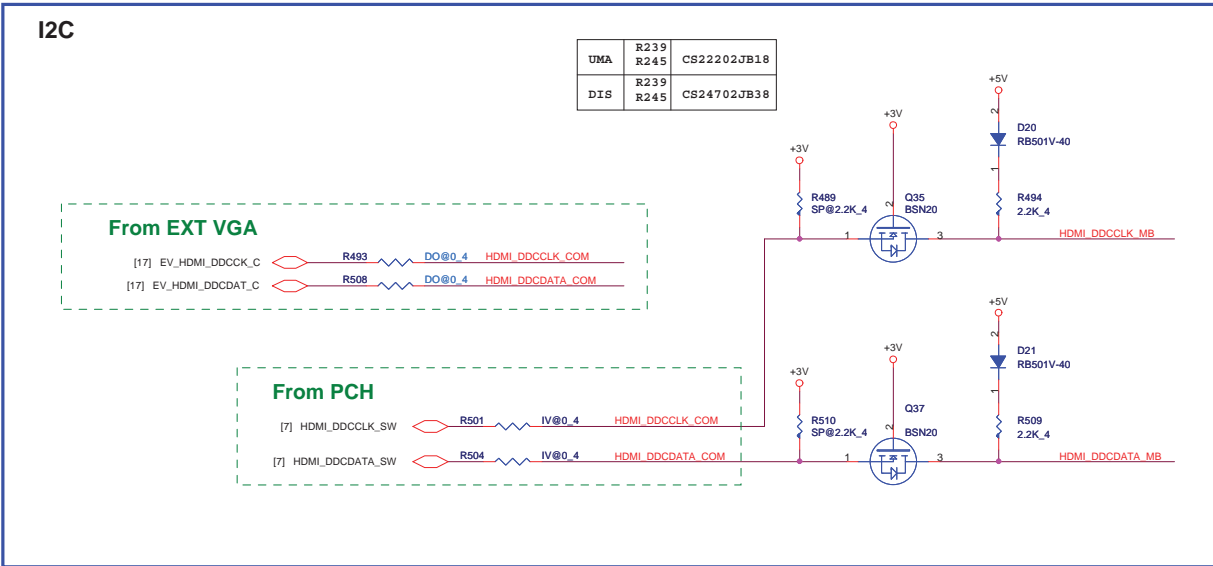
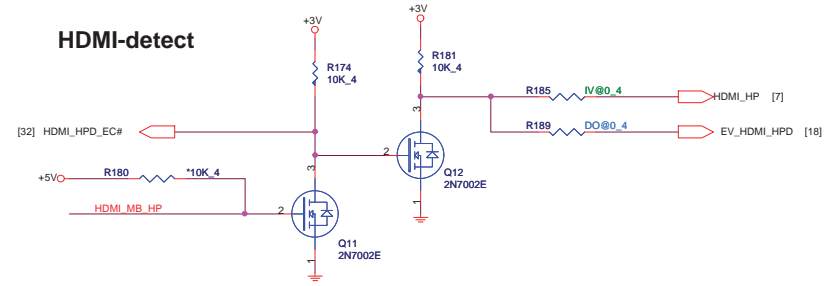
# Backlight Control



HDMI connector

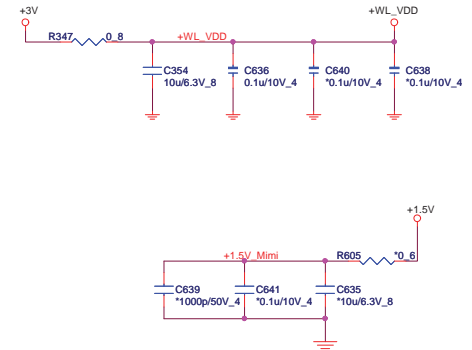
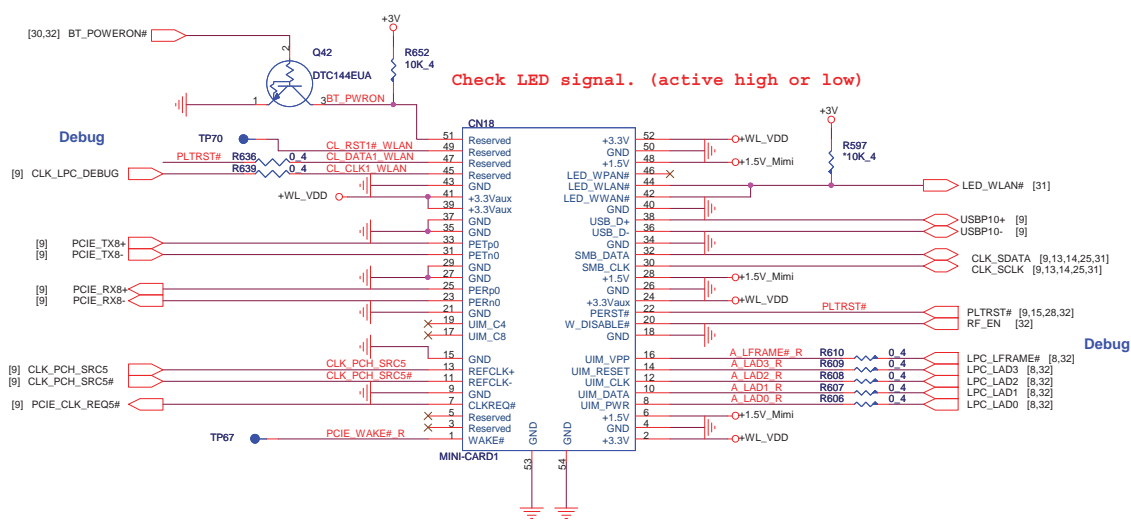


IV@:iGPU  
EV@:dGPU  
OP@:Optimus  
DO@:Discrete only  
SP@:Special

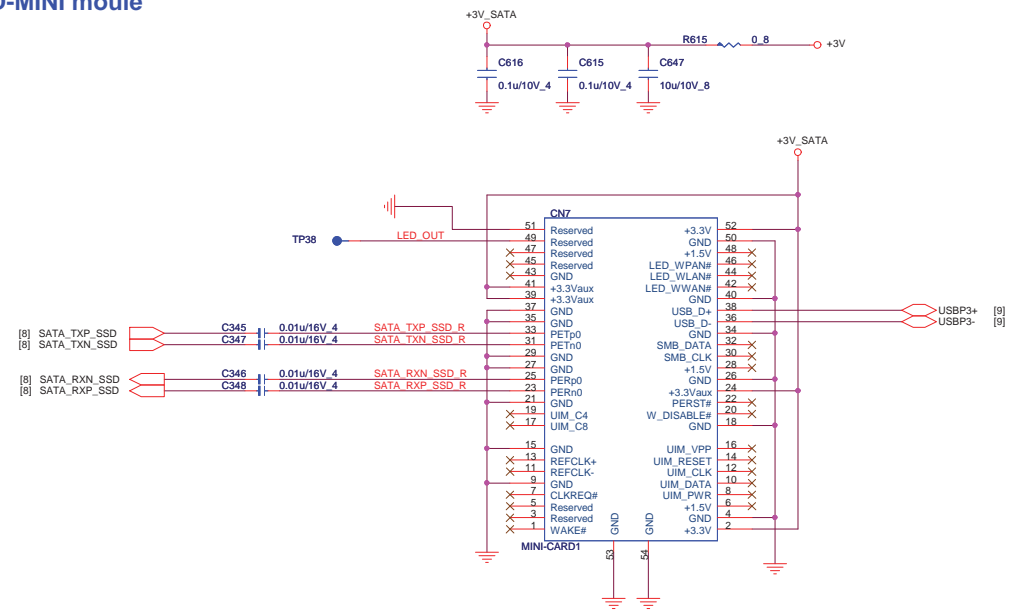


# MINI-CARD WLAN(MPC)

+3.3V: 1000mA  
 +3.3Vaux:330mA  
 +1.5V:500mA



# SSD-MINI moule

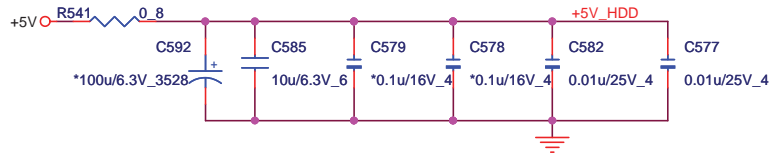
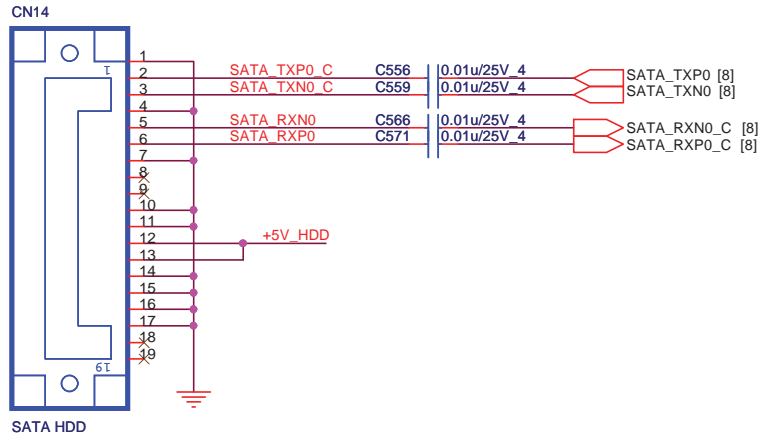


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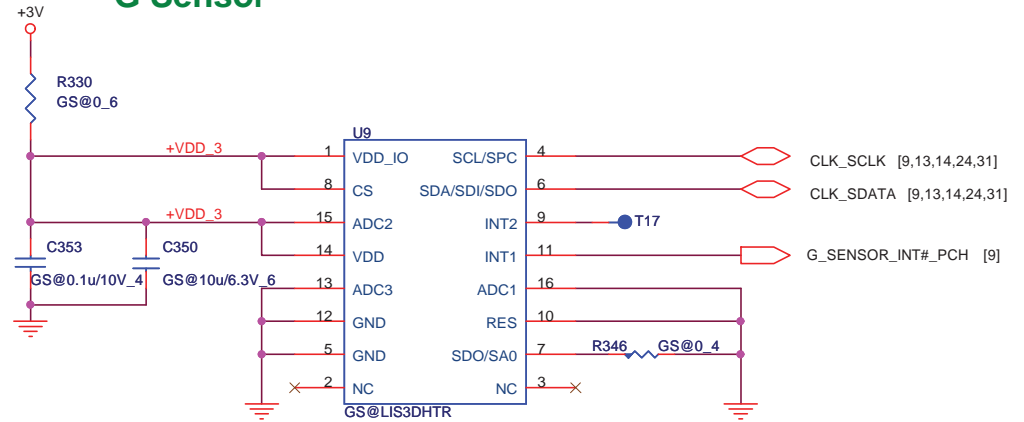
		<b>Quanta Computer Inc.</b> PROJECT : ZQTA/ZQSA	
		MINI PCI-E / SSD	Rev 1A
Size	Document Number	Date: Friday, November 11, 2011	Sheet 24 of 44



# MAIN SATA HDD(HDD)

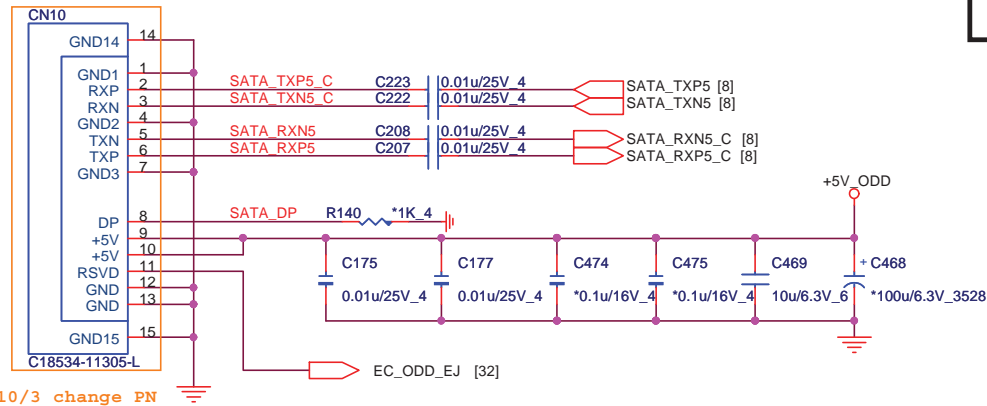


# G Sensor



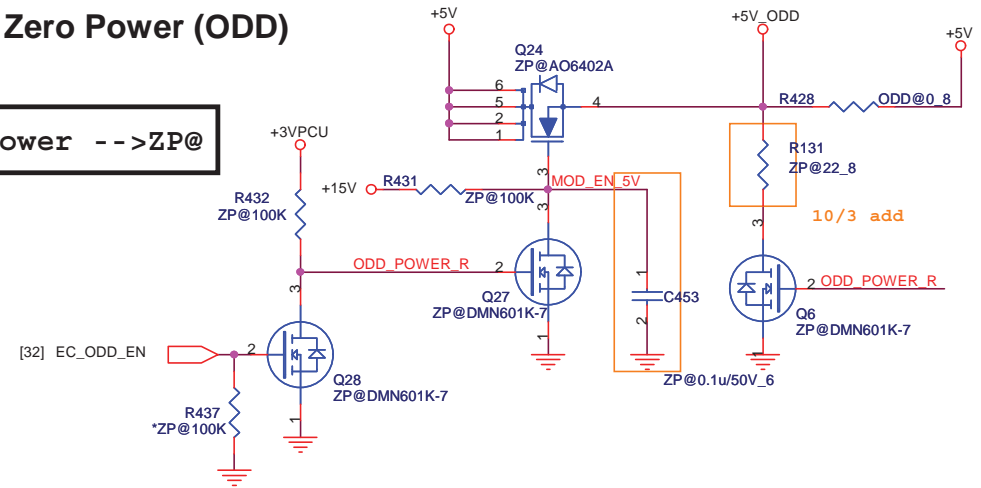
**G-Sensor -->GS@**

# ODD (ODD)



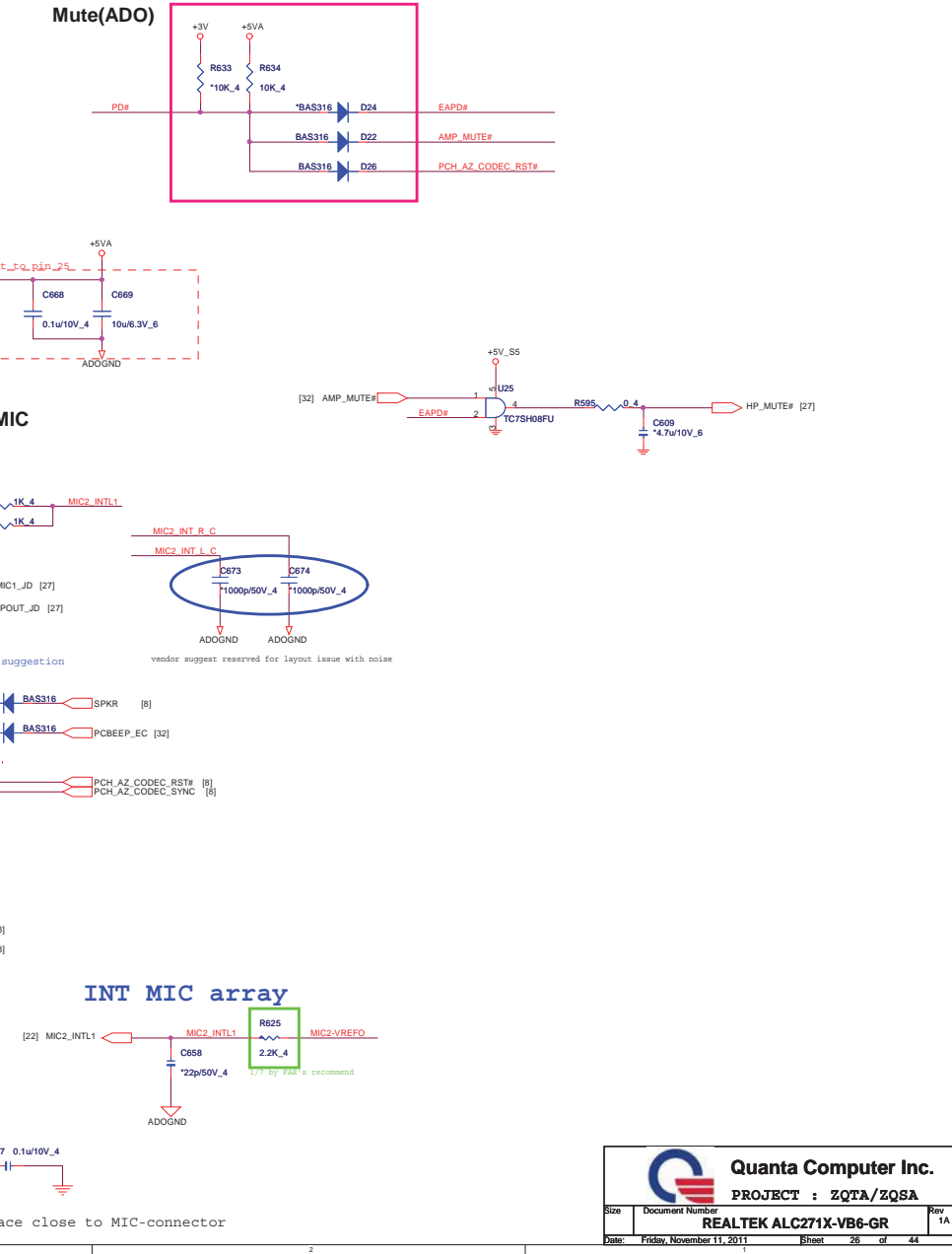
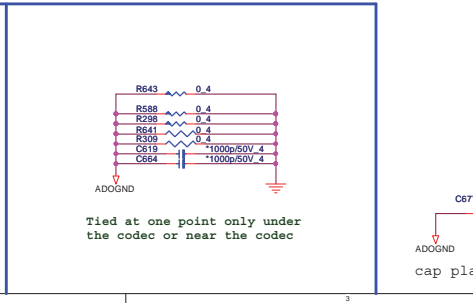
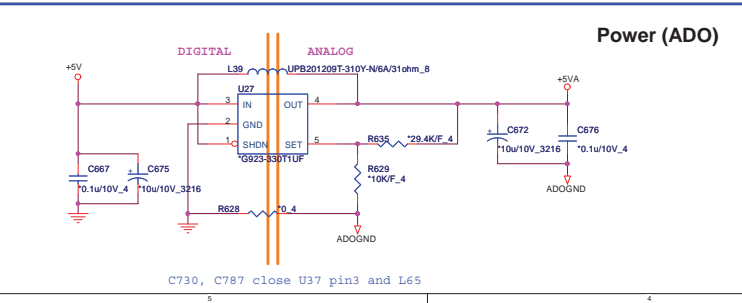
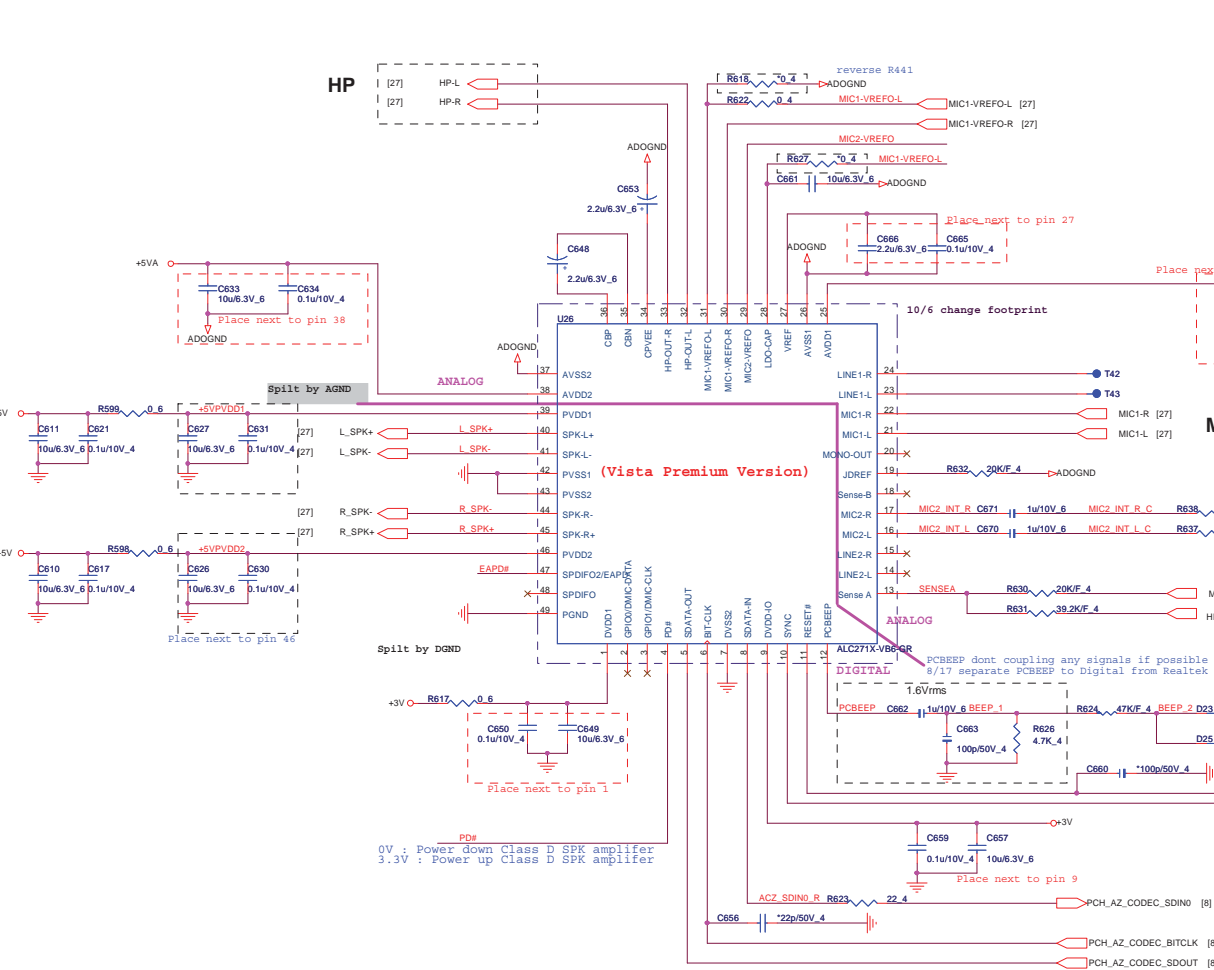
# Zero Power (ODD)

**Zero Power -->ZP@**

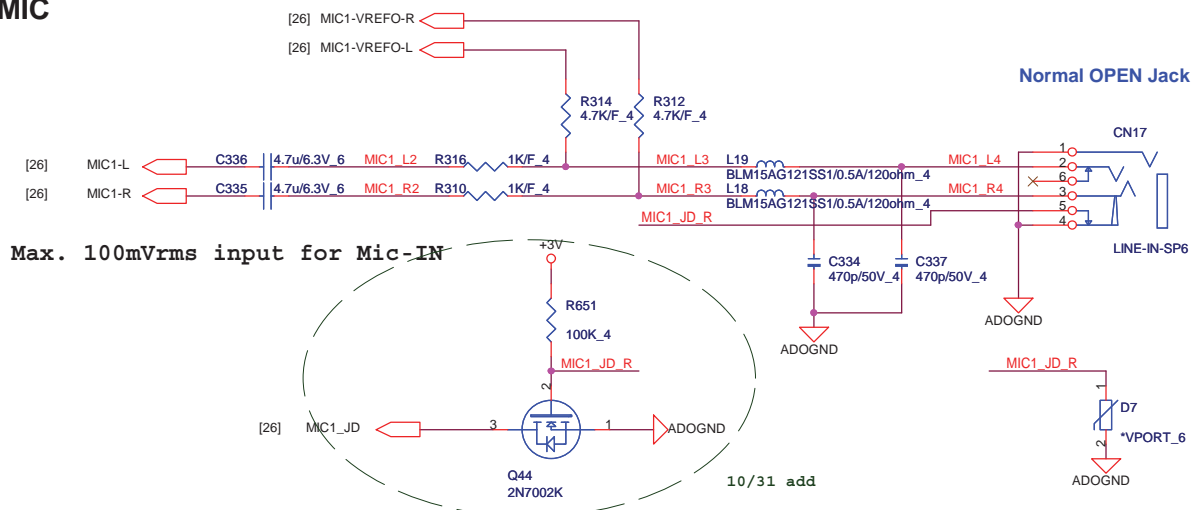


<b>Quanta Computer Inc.</b> <b>PROJECT : ZQTA/ZQSA</b>			
			Size
Date: Friday, November 11, 2011		Sheet 25 of 44	Rev 1A

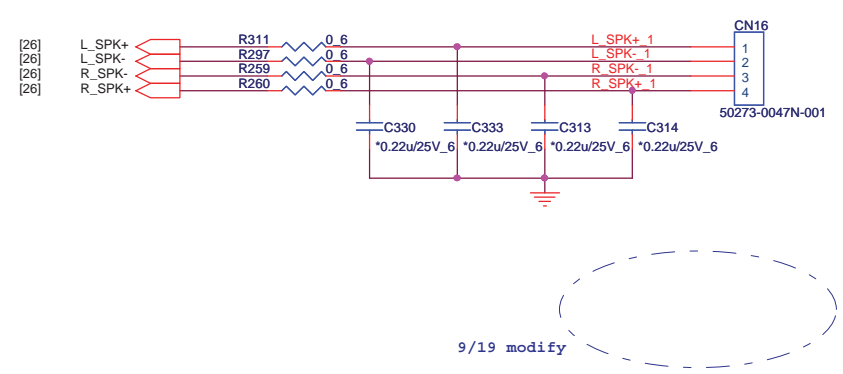
Codec(ADO)



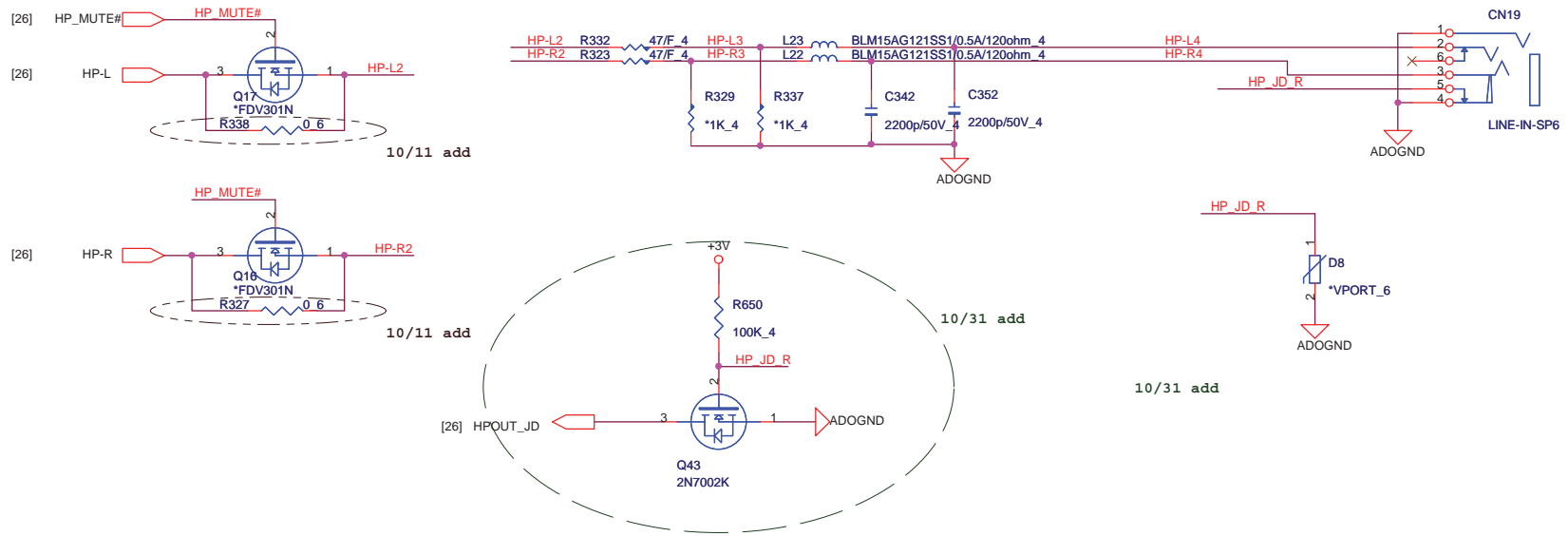
**MIC**



**Internal Speaker**

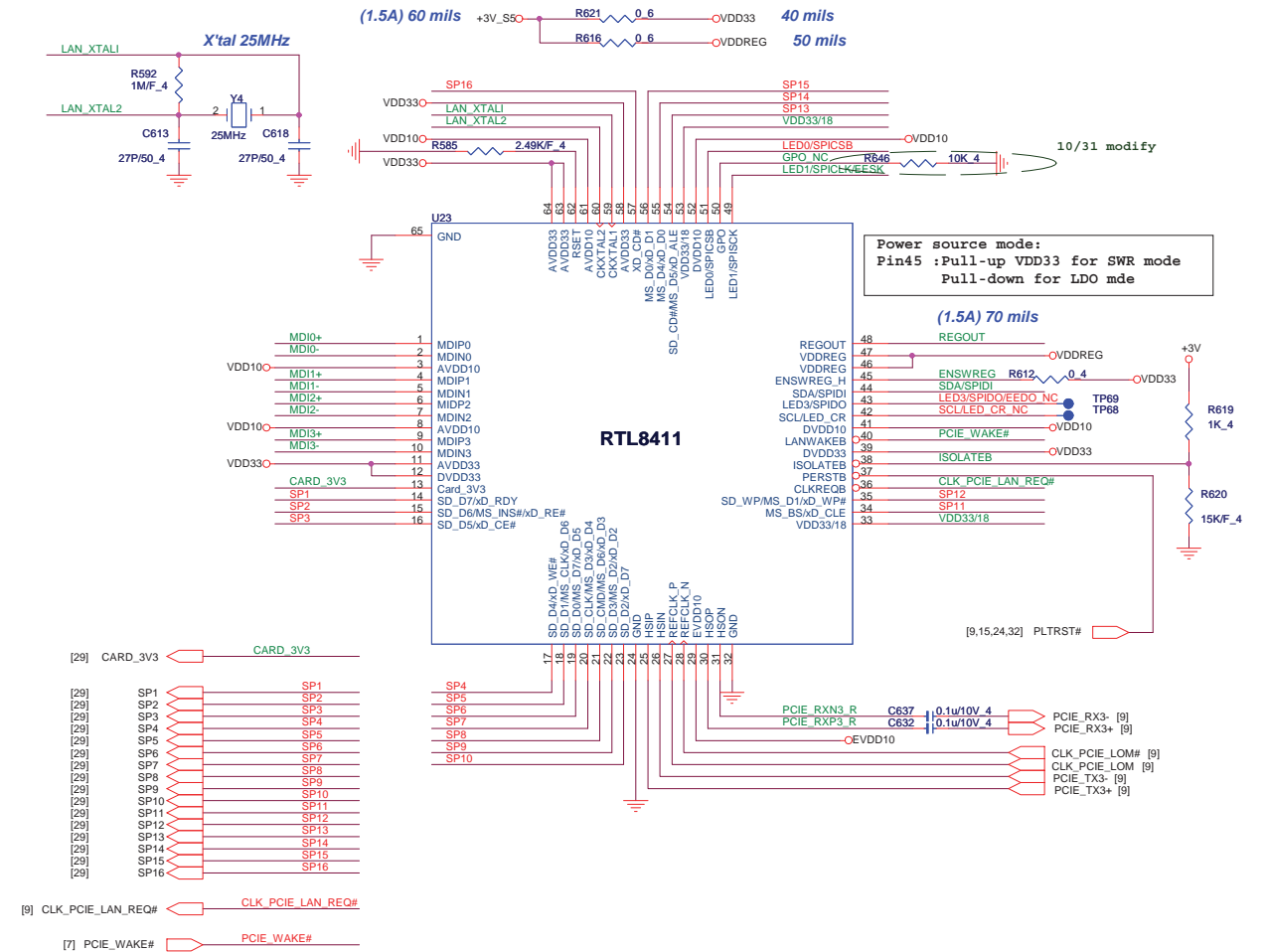


**HP**

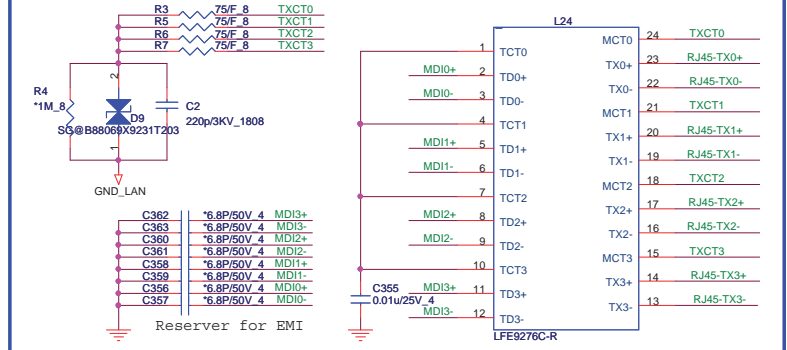


		<b>Quanta Computer Inc.</b> <b>PROJECT : ZQTA/ZQSA</b>	
		Date: Friday, November 11, 2011	Sheet 27 of 44

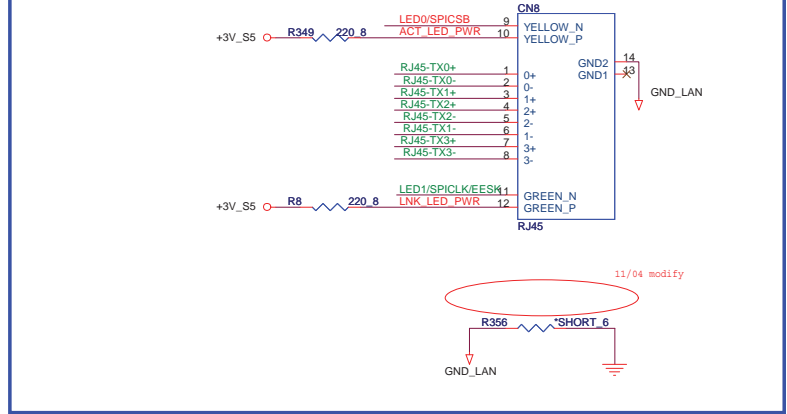
# LAN/Card reader



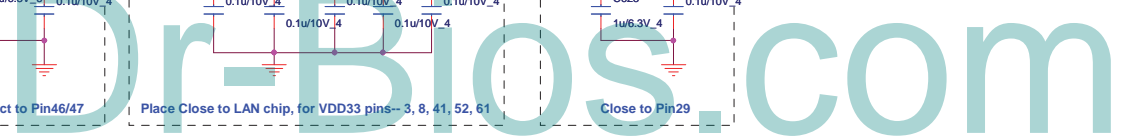
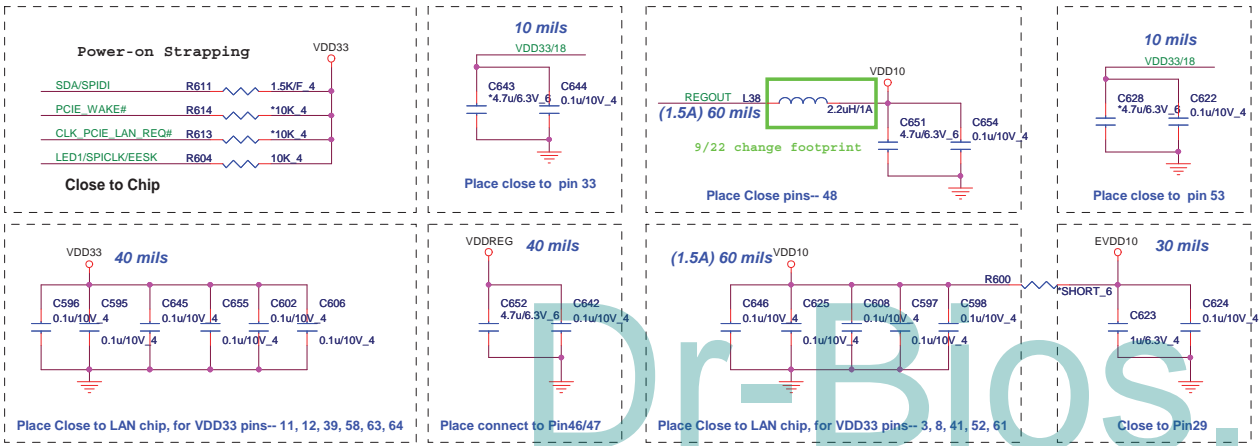
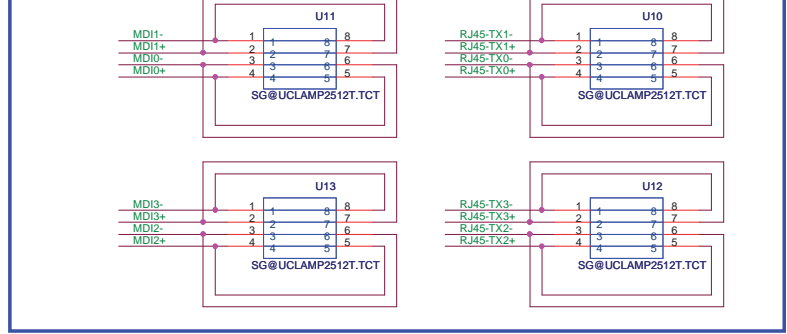
# Transformer



# RJ45



# SURGE



**Quanta Computer Inc.**

**PROJECT : ZQTA/ZQSA**

**LAN-RTL8411/CARD READER**

Size Document Number Rev 1A

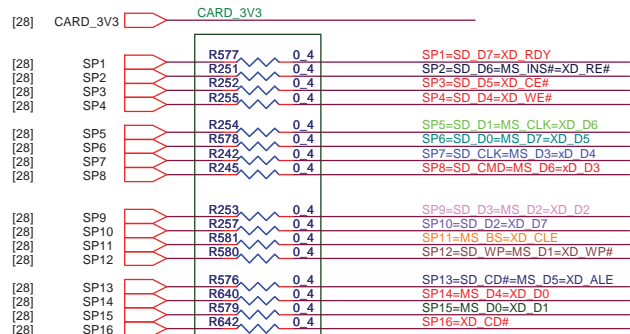
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# CARD READER CONNECTOR

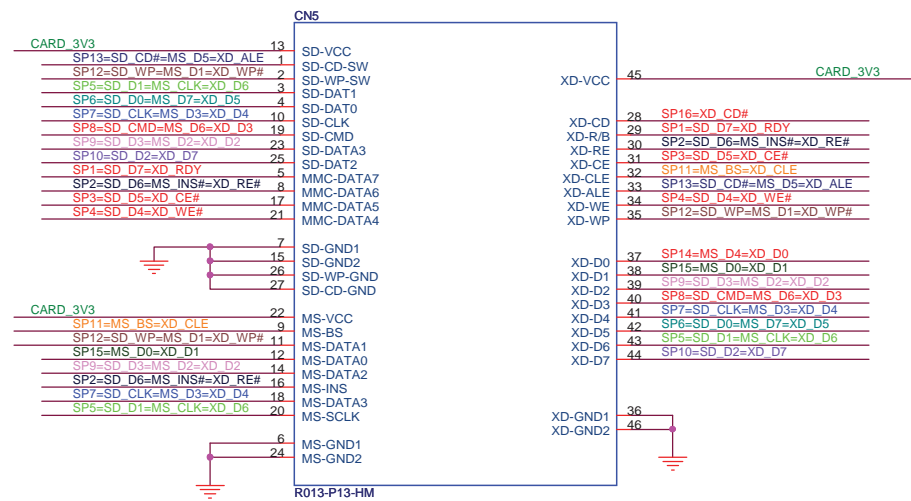
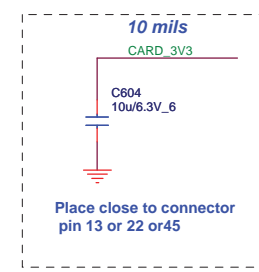
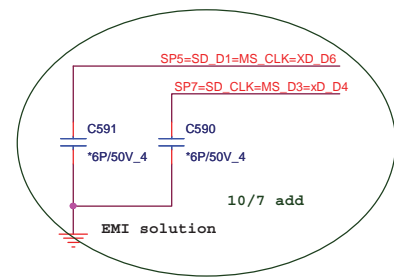
## Share Pin

SP1	SD_D7		xD_RDY
SP2	SD_D6	MS_INS#	xD_RE#
SP3	SD_D5		xD_CE#
SP4	SD_D4		xD_WE#
SP5	SD_D1	MS_CLK	xD_D6
SP6	SD_D0	MS_D7	xD_D5
SP7	SD_CLK	MS_D3	xD_D4
SP8	SD_CMD	MS_D6	xD_D3
SP9	SD_D3	MS_D2	xD_D2
SP10	SD_D2		xD_D7
SP11		MS_BS	xD_CLE
SP12	SD_WP	MS_D1	xD_WP#
SP13	SD_CD#	MS_D5	xD_ALE
SP14		MS_D4	xD_D0
SP15		MS_D0	xD_D1
SP16			xD_CD#

# XD,MMC 4.2/SD,MS/MSP 7 IN1 CARD READER

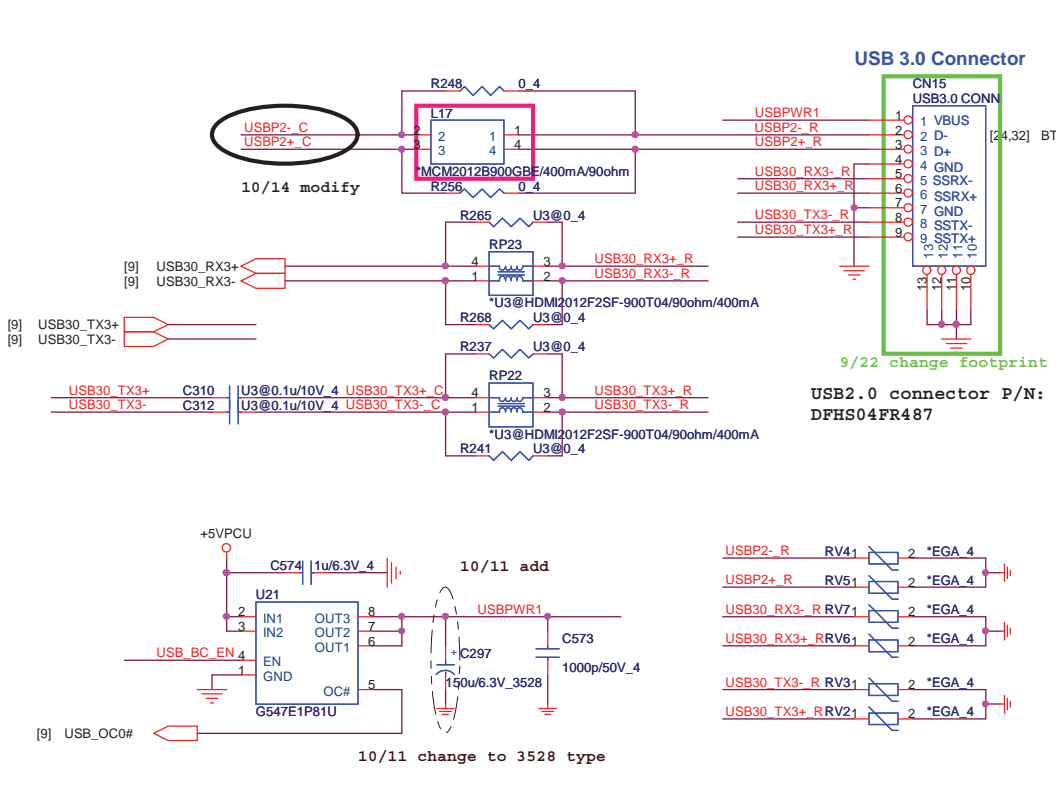


10/7 change 0 ohm

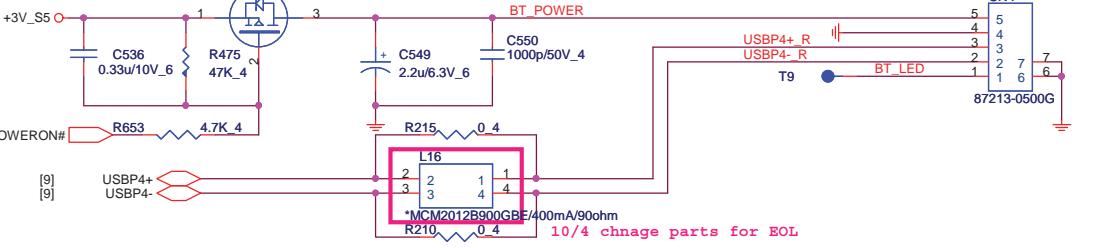


R013-P13-HM  
1 : DFHS44FR012  
2 : DFHS44FR014

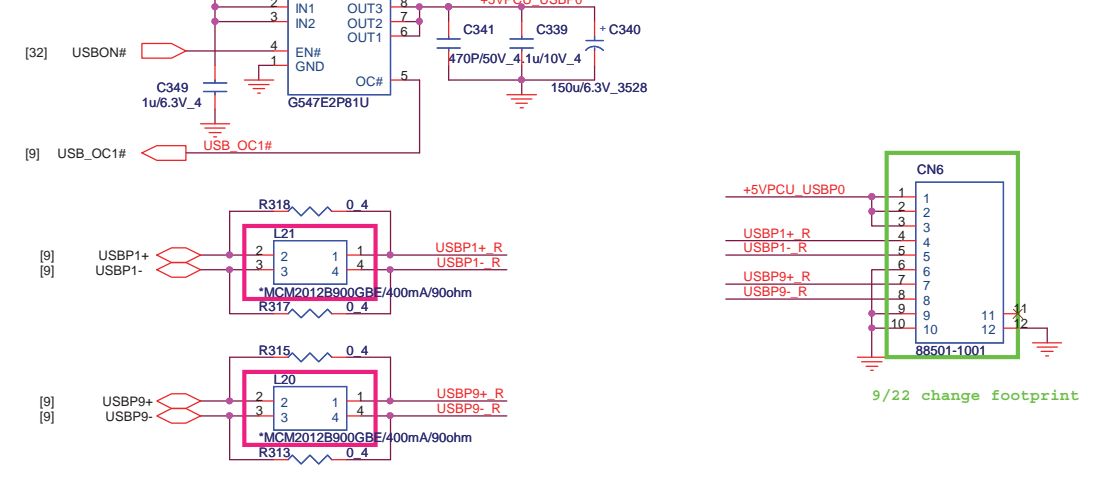
# USB3.0/2.0



# Bluetooth

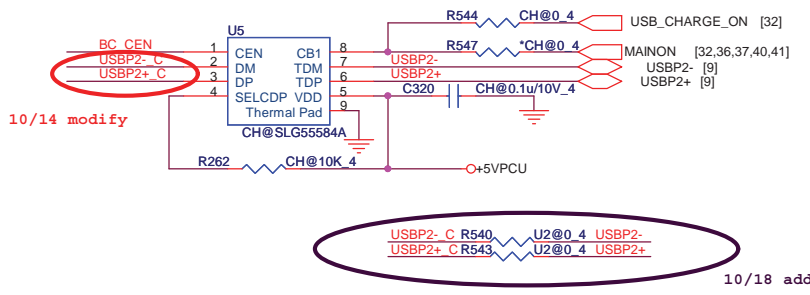


# USB/B

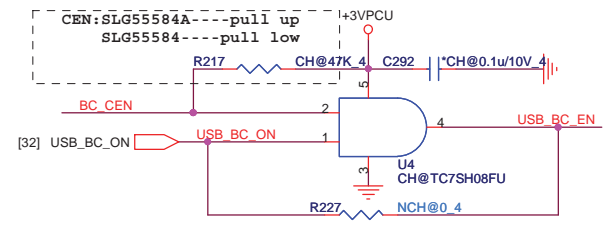


# USB Charger to 3.0

CB	SELCDP	Funcion
0	X	DCP autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP only
1	1	S0 charging with CDP or SDP only (depending on external device)

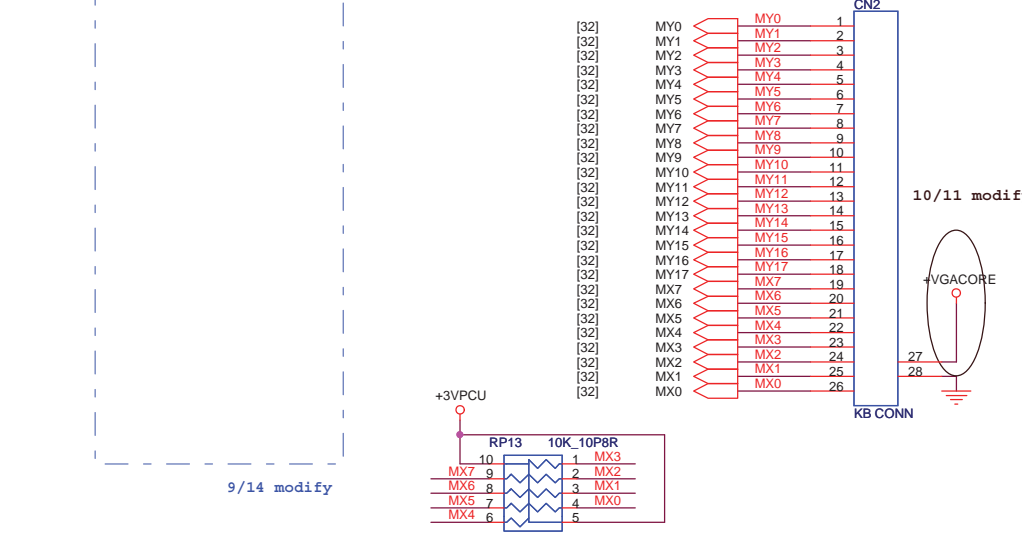


USB Charger -->CH@  
None Charger--> NCH@

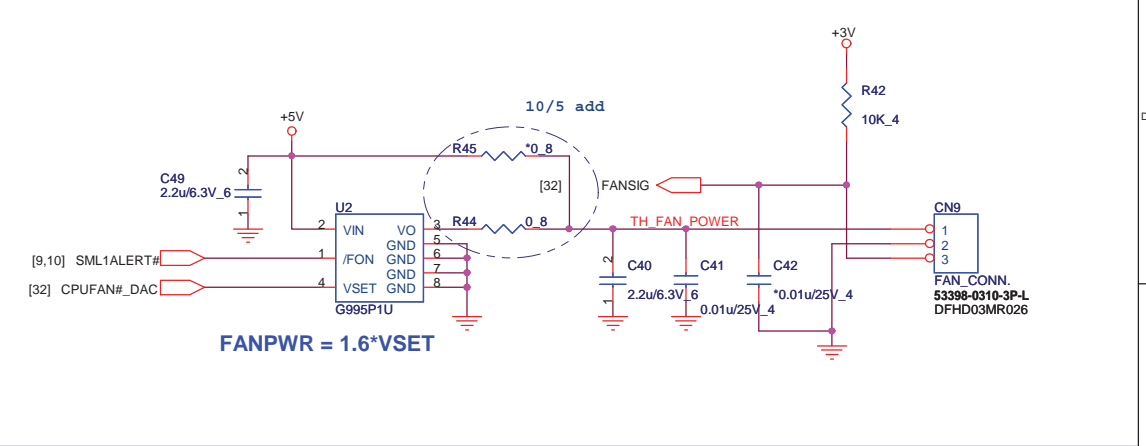


**Quanta Computer Inc.**  
PROJECT : ZQTA/ZQSA

Size	Document Number	Rev
	<b>USB/ BT/CHARGER</b>	1A
Date:	Friday, November 11, 2011	Sheet 30 of 44

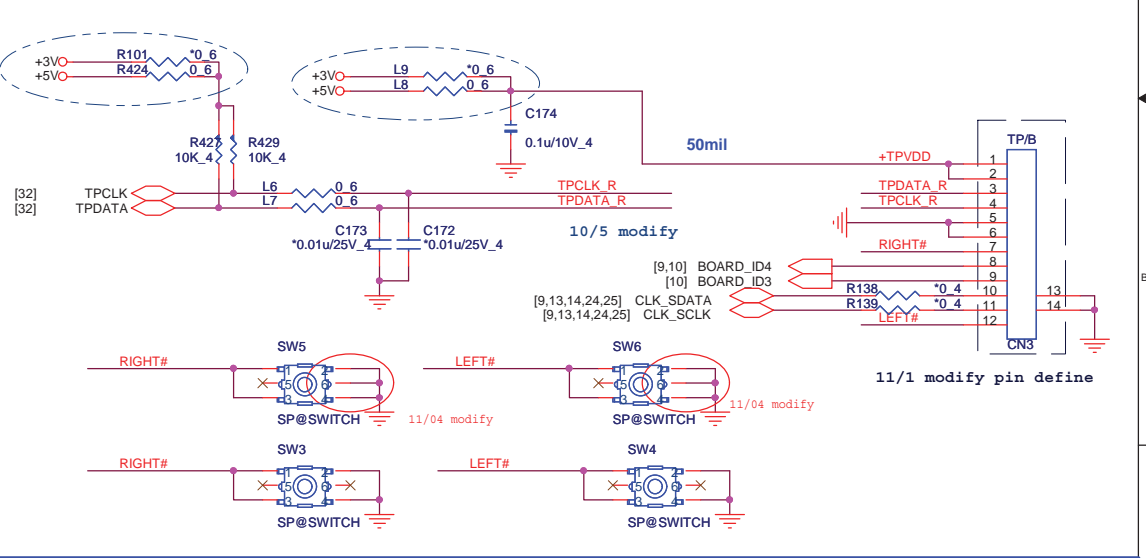


### CPU FAN

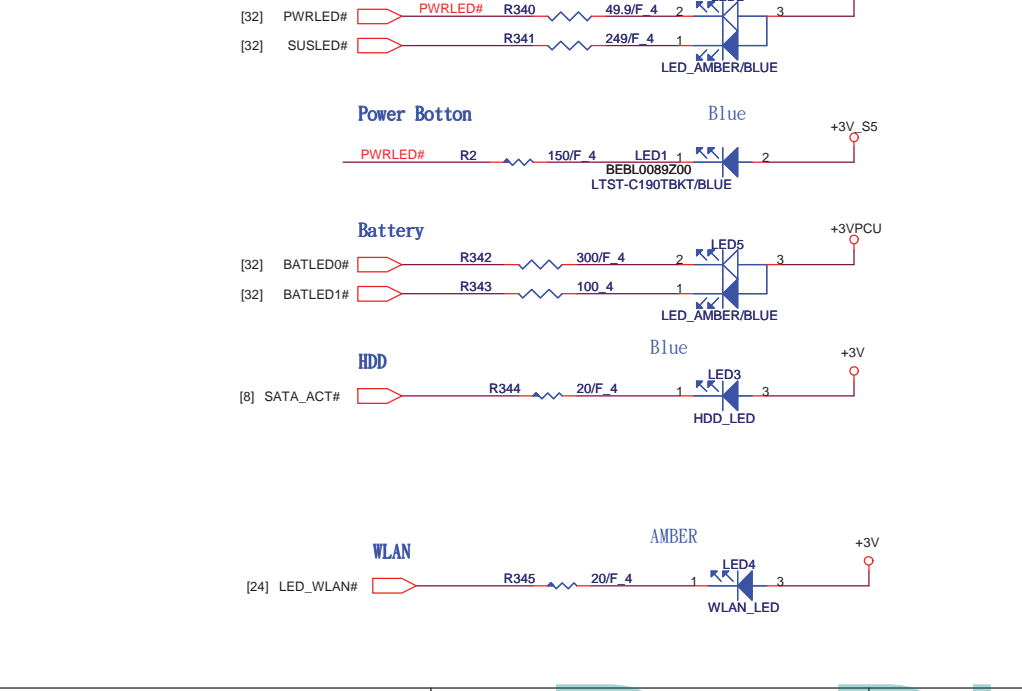


### TOUCHPAD & Switch CONN.

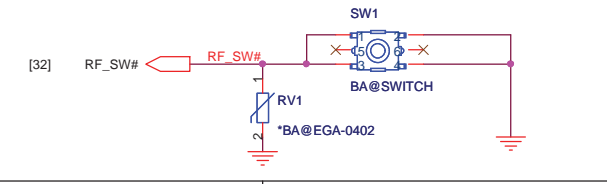
Model EA/EG/BA---->SW3, SW4  
VA/VG----->SW5, SW6



### LED



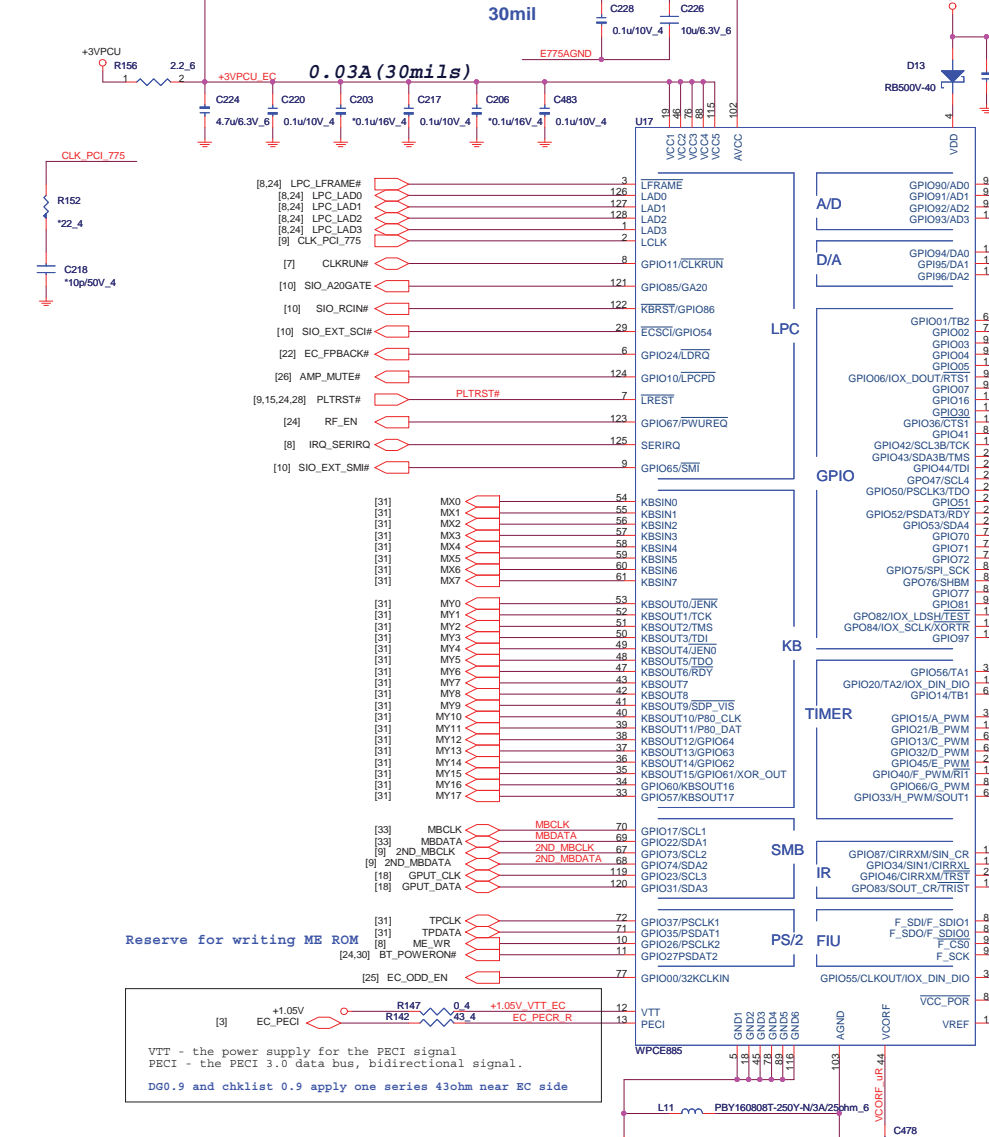
### For BA WLAN function



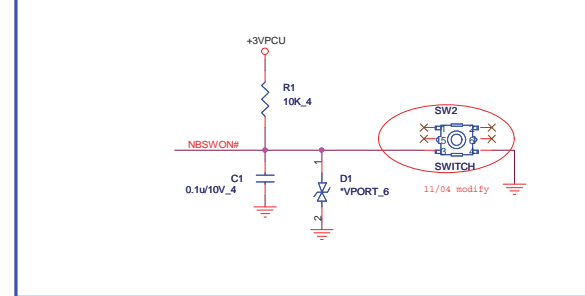
**Quanta Computer Inc.**  
PROJECT : ZQTA/ZQSA

Size	Document Number	Rev
	<b>KB/FAN/TP+FP/LED</b>	1A
Date:	Friday, November 11, 2011	Sheet 31 of 44

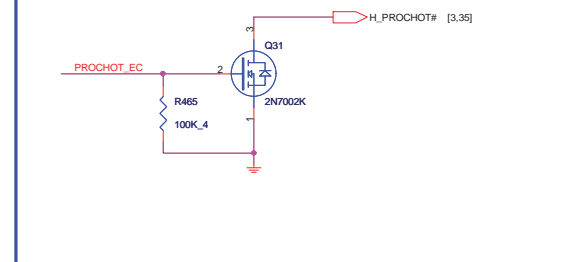
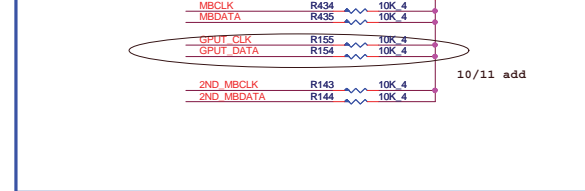
**EC(KBC)**



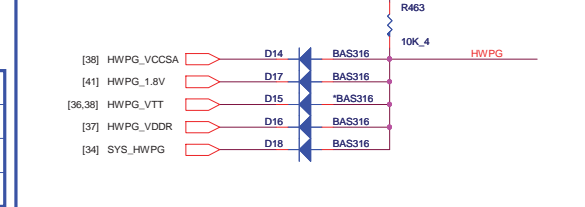
**Power on bottom**



**SM BUS PU(KBC)**



**HWPG(KBC)**



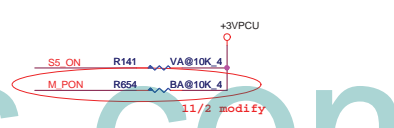
**SM BUS ARRANGEMENT TABLE**

SM Bus	Device
SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	VGA
SM Bus 4	HDMI

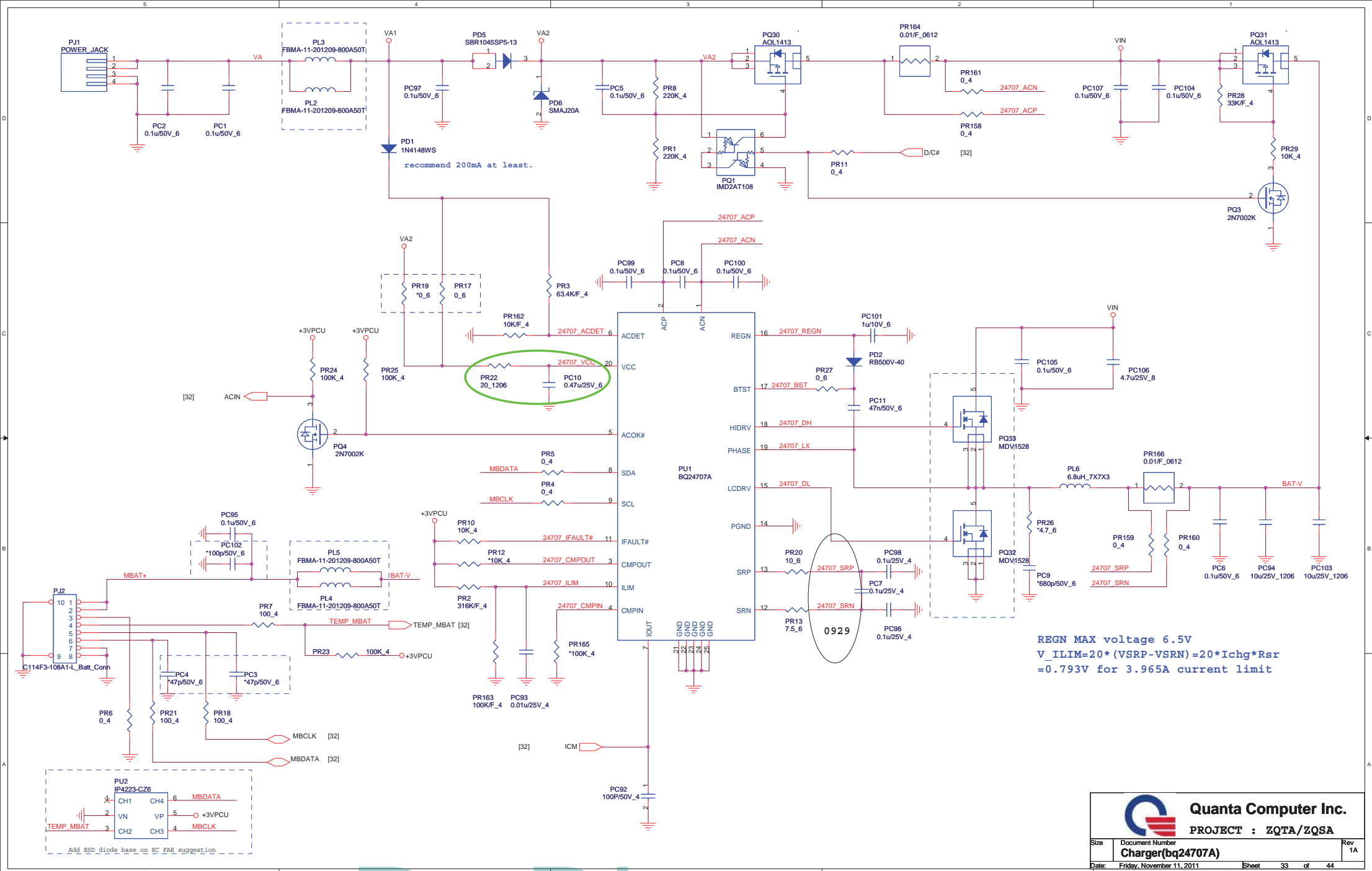
pin14 +VCC GFX  
pin22 +3V D for ATI  
pin24 +1V for ATI  
pin26 +1.8V GPU for ATI  
pin28 GPU\_RST#


pin13 GFX\_PWRGD  
pin21 dGPU\_VRON  
pin23 +VGPU\_CORE  
pin25 +1.5V GPU  
pin27 dGPU\_PWROK

VTT - the power supply for the Peci signal  
PECI - the Peci 3.0 data bus, bidirectional signal.  
Dg0.9 and chklst 0.9 apply one series 43ohm near EC side





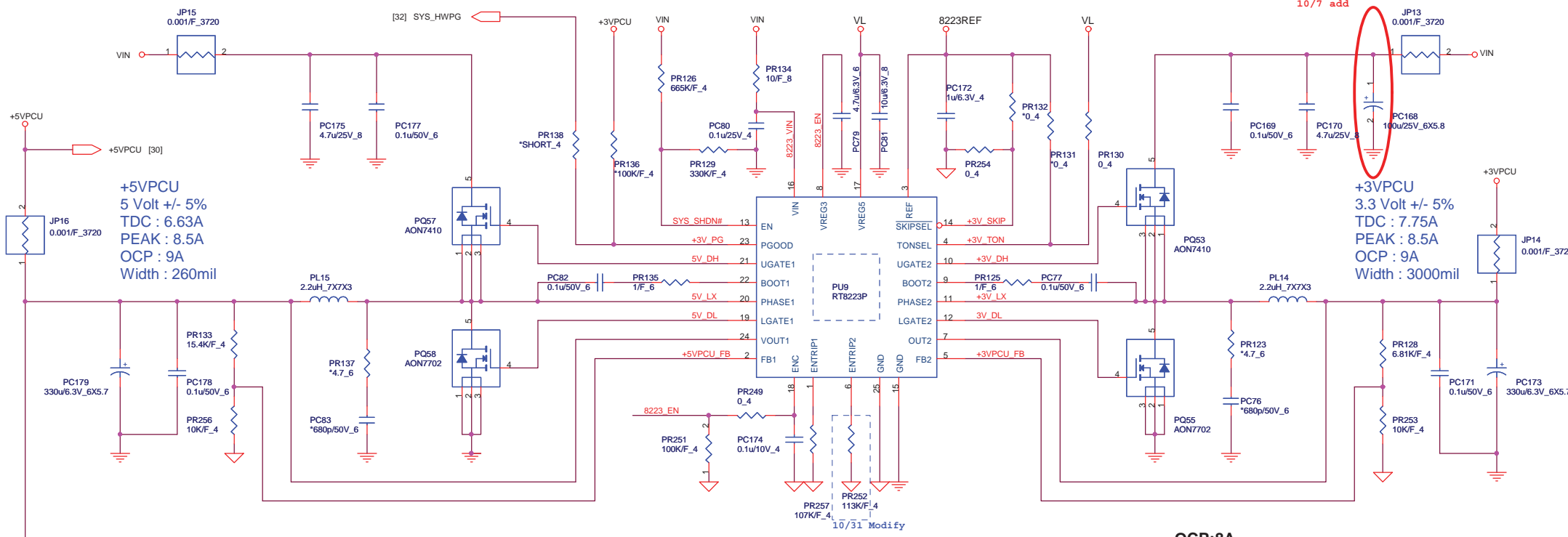


 <b>Quanta Computer Inc.</b> PROJECT : ZQTA/ZQSA		Rev
		1A
Size	Document Number	Sheet 33 of 44
<b>Charger(bq24707A)</b>		
Date:	Friday, November 11, 2011	

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MAIND [5,37,41]      SYS\_SHDN# [3,41]

Ven=7.23V

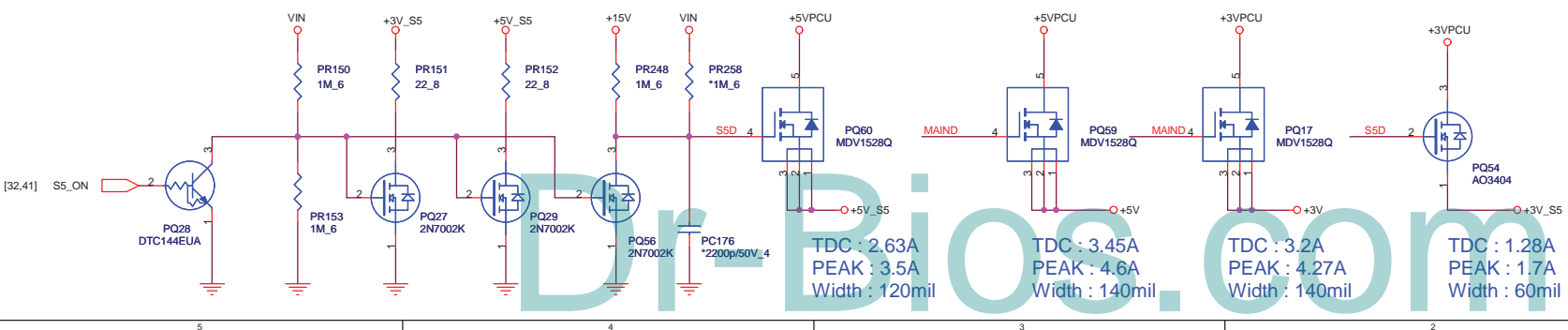
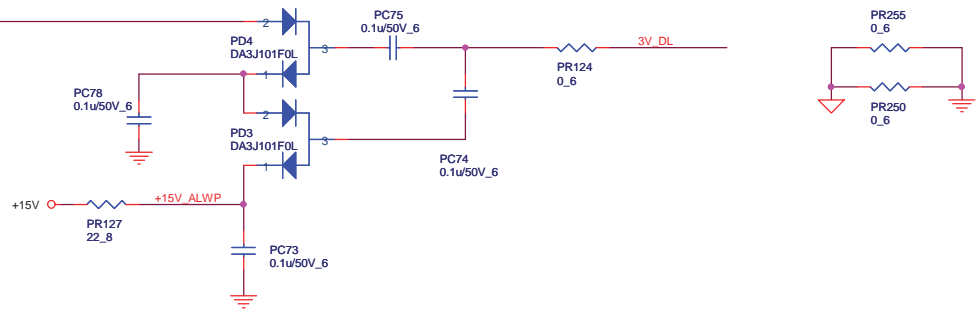


**+5VPCU**  
5 Volt +/- 5%  
TDC : 6.63A  
PEAK : 8.5A  
OCP : 9A  
Width : 260mil

**+3VPCU**  
3.3 Volt +/- 5%  
TDC : 7.75A  
PEAK : 8.5A  
OCP : 9A  
Width : 3000mil

**OCP:9A**  
L(ripple current)  
=(9-5)\*5/(2.2u\*0.4M\*9)  
=2.525A  
Iocp=9-(2.525/2)=7.74A  
Vth=7.74A\*14mOhm=0.10832mV  
R(IIim)=(108.32mV\*10)/10uA  
~107K

**OCP:8A**  
L(ripple current)  
=(9-3.3)\*3.3/(2.2u\*0.5M\*9)  
~1.9A  
Iocp=9-(1.9/2)=8.05A  
Vth=8.05A\*14mOhm=112.7mV  
R(IIim)=(112.7mV\*10)/10uA  
=112.7K




TDC : 2.63A  
PEAK : 3.5A  
Width : 120mil

TDC : 3.45A  
PEAK : 4.6A  
Width : 140mil

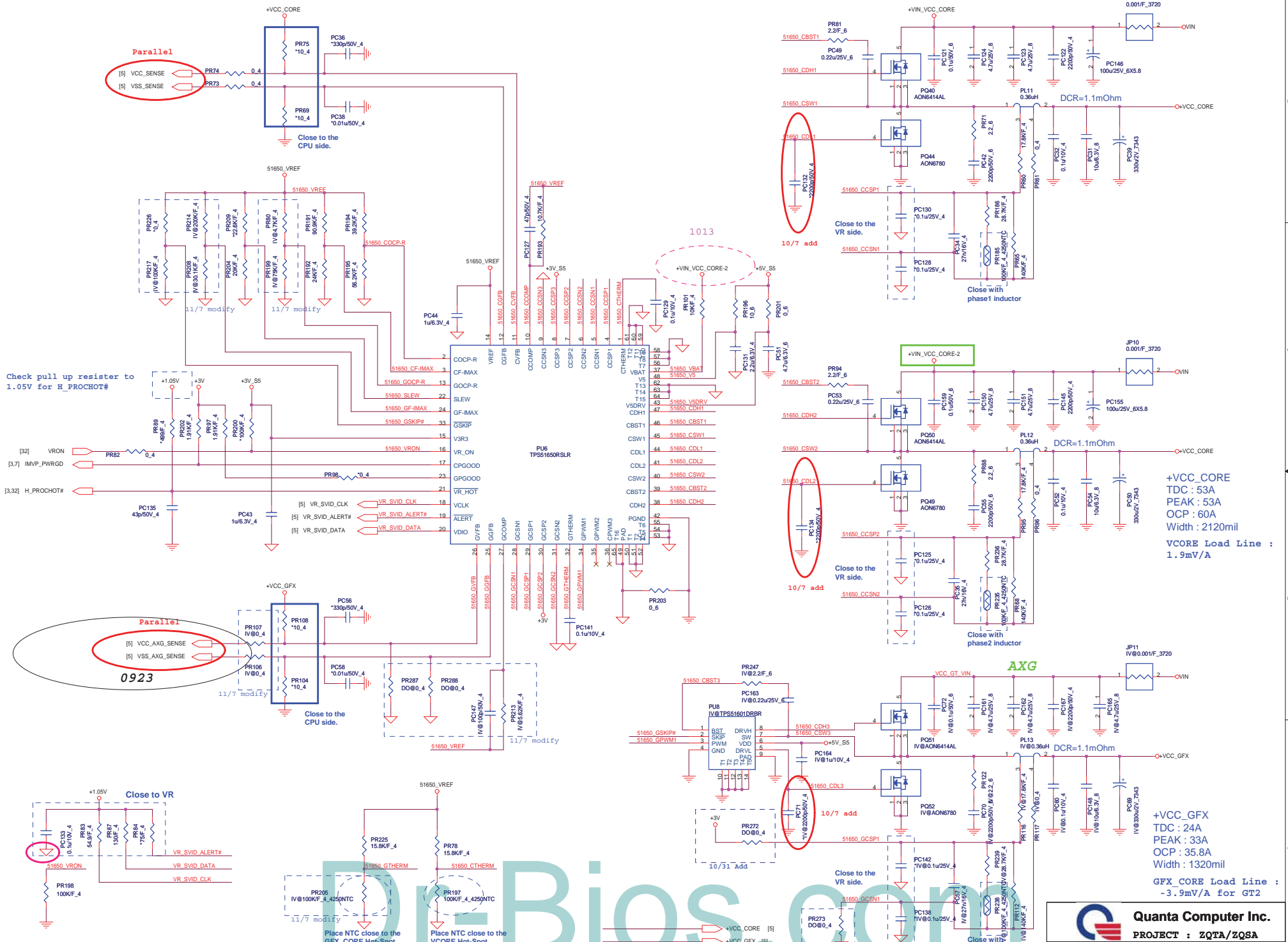
TDC : 3.2A  
PEAK : 4.27A  
Width : 140mil

TDC : 1.28A  
PEAK : 1.7A  
Width : 60mil



**Quanta Computer Inc.**  
**PROJECT : ZQTA/ZQSA**

Size	Document Number	Rev
<b>SYSTEM 5V/3V (RT8223P)</b>		1A
Date: Friday, November 11, 2011		Sheet 34 of 44



Parallel  
 [5] VCC\_SENSE  
 [5] VSS\_SENSE

Parallel  
 [5] VCC\_AXG\_SENSE  
 [5] VSS\_AXG\_SENSE

Check pull up resistor to 1.05V for H\_PROCHOT#

Close to the CPU side.

Close to the CPU side.

Close to VR

Place NTC close to the GFX\_CORE Hot-Spot.

Place NTC close to the VCORE Hot-Spot.

10/13

10/7 add

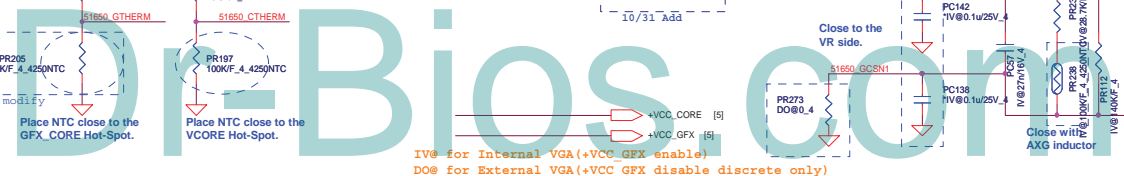
10/7 add

10/7 add

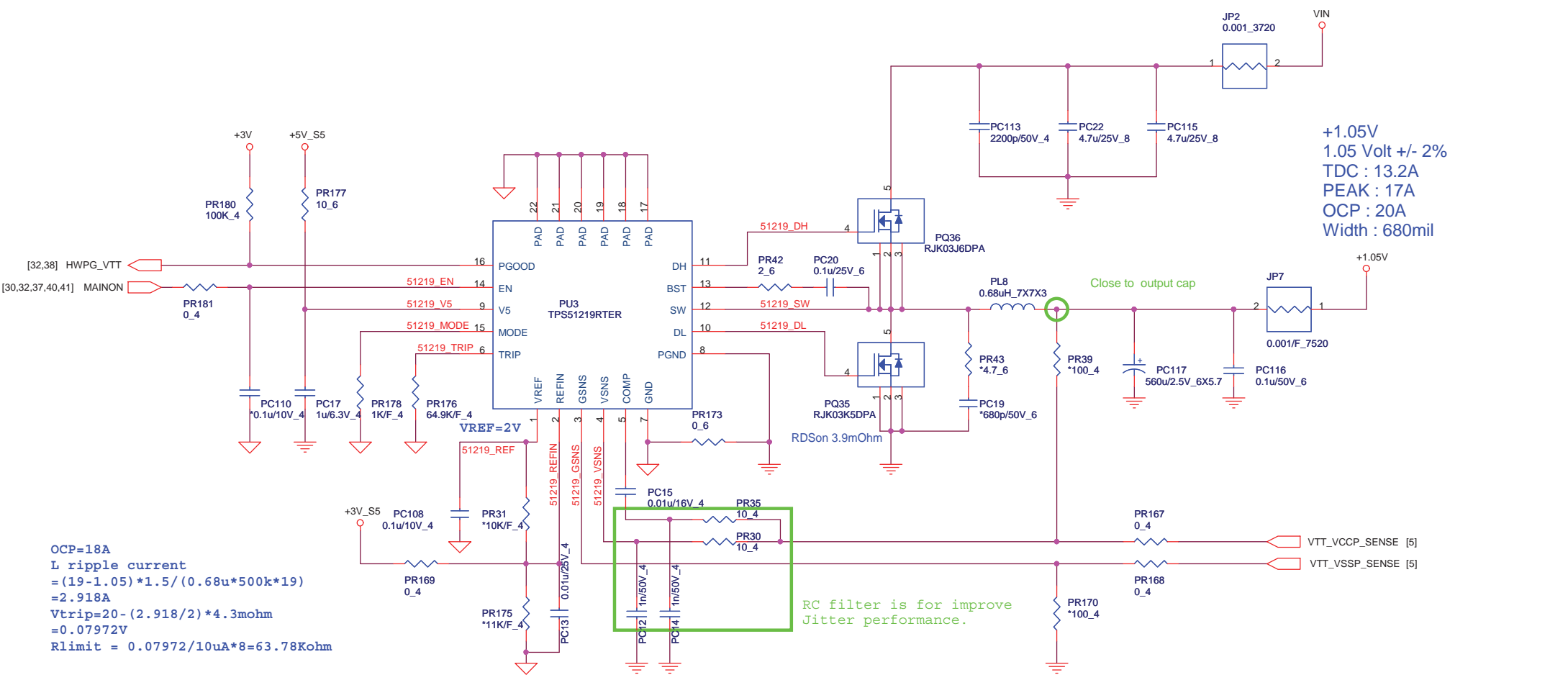
10/31 Add

+VCC\_CORE  
 TDC : 53A  
 PEAK : 53A  
 OCP : 60A  
 Width : 2120mil  
 VCORE Load Line : 1.9mV/A

+VCC\_GFX  
 TDC : 24A  
 PEAK : 33A  
 OCP : 35.8A  
 Width : 1320mil  
 GFX\_CORE Load Line : -3.9mV/A for GT2



IV@ for Internal VGA (+VCC\_GFX enable)  
 DO@ for External VGA (+VCC\_GFX disable discrete only)



+1.05V  
 1.05 Volt +/- 2%  
 TDC : 13.2A  
 PEAK : 17A  
 OCP : 20A  
 Width : 680mil

OCP=18A  
 L ripple current  
 = (19-1.05) \* 1.5 / (0.68u \* 500k \* 19)  
 = 2.918A  
 Vtrip = 20 - (2.918 / 2) \* 4.3mohm  
 = 0.07972V  
 Rlimit = 0.07972 / 10uA \* 8 = 63.78Kohm

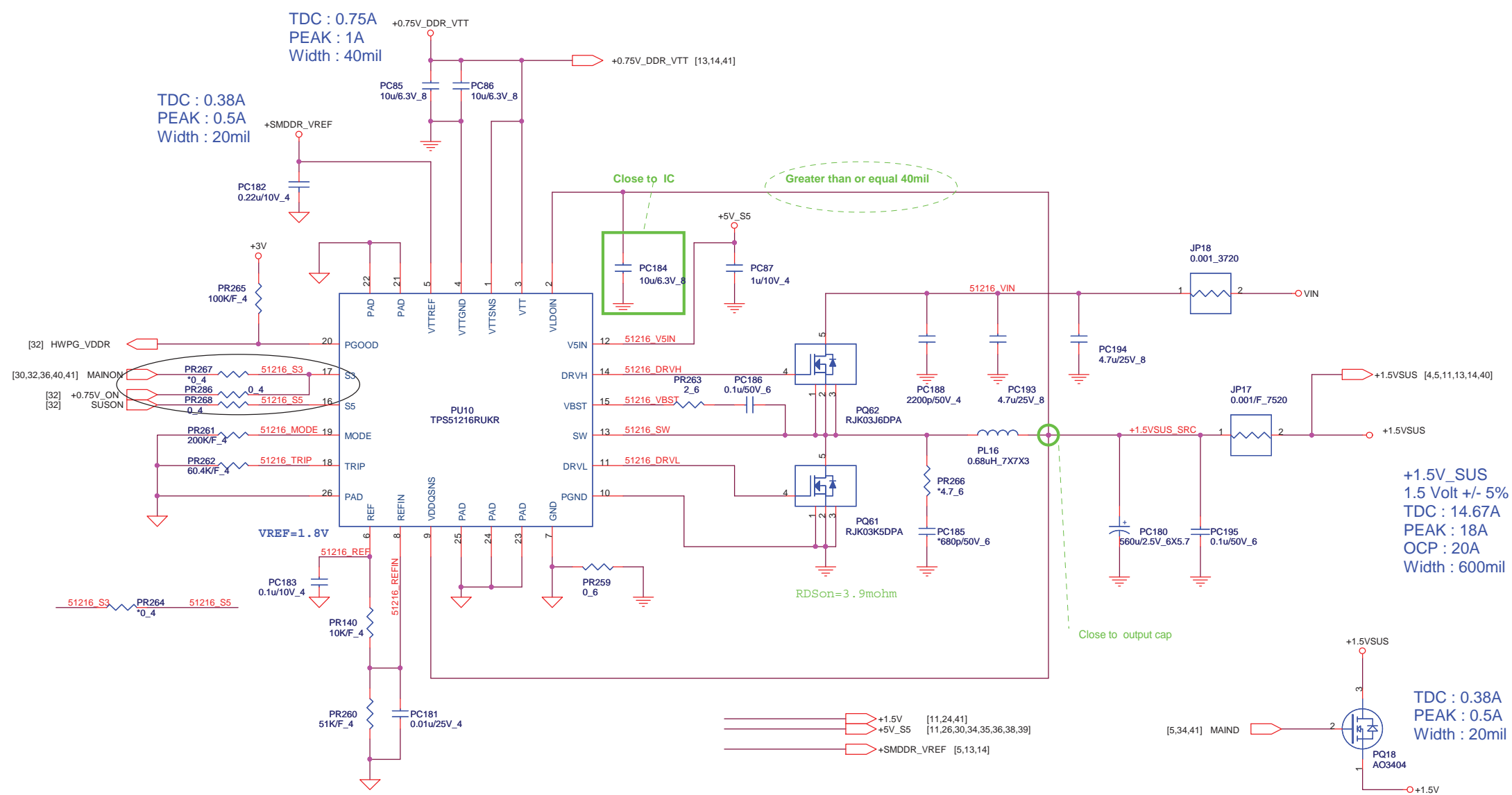
RC filter is for improve Jitter performance.

+3VPCU	[8,22,25,30,31,32,33,34,41,42]
+1.05V	[3,5,7,8,9,11,22,32,35,40,41]
+3V_S5	[3,7,8,9,10,11,15,28,30,31,34,35,41,42]
VIN	[22,33,34,35,37,38,39,40,41,42,43]
+5V_S5	[11,26,30,34,35,37,38,39]
+3V	[3,7,8,9,10,11,13,14,19,22,23,24,25,26,27,28,31,32,34,35,37,38,39,40,41]
+5VPCU	[30,34]

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 PROJECT : ZQTA/ZQSA

Size	Document Number	Rev
	<b>+1.05V (TPS51219)</b>	1A
Date:	Friday, November 11, 2011	Sheet 36 of 44



OCP=20A  
 I ripple current  
 $= (19-1.5) * 1.5 / (0.68 * 400k * 19)$   
 $= 5.079A$   
 $V_{trip} = 20 - (5.079 / 2) * 4.3mohm$   
 $= 0.07508V$   
 $R_{limit} = 0.07508 / 10uA * 8 = 60.063Kohm$

	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

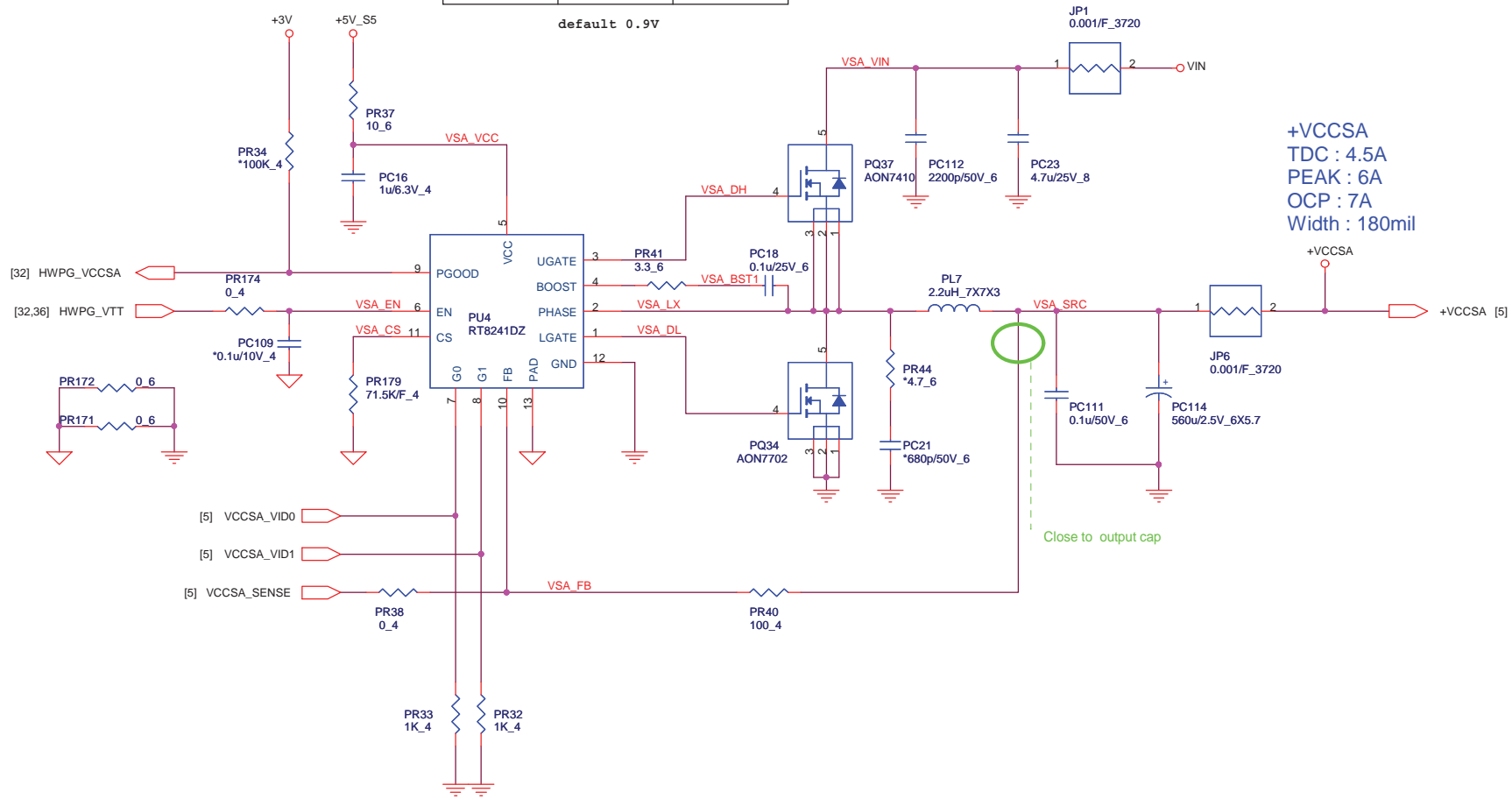
**Quanta Computer Inc.**  
 PROJECT : ZQTA/ZQSA

Size	Document Number	Rev
	<b>DDR 1.5V(TPS51216)</b>	1A

Date: Friday, November 11, 2011      Sheet 37 of 44

G0	G1	+VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

default 0.9V



+VCCSA  
TDC : 4.5A  
PEAK : 6A  
OCP : 7A  
Width : 180mil

Close to output cap

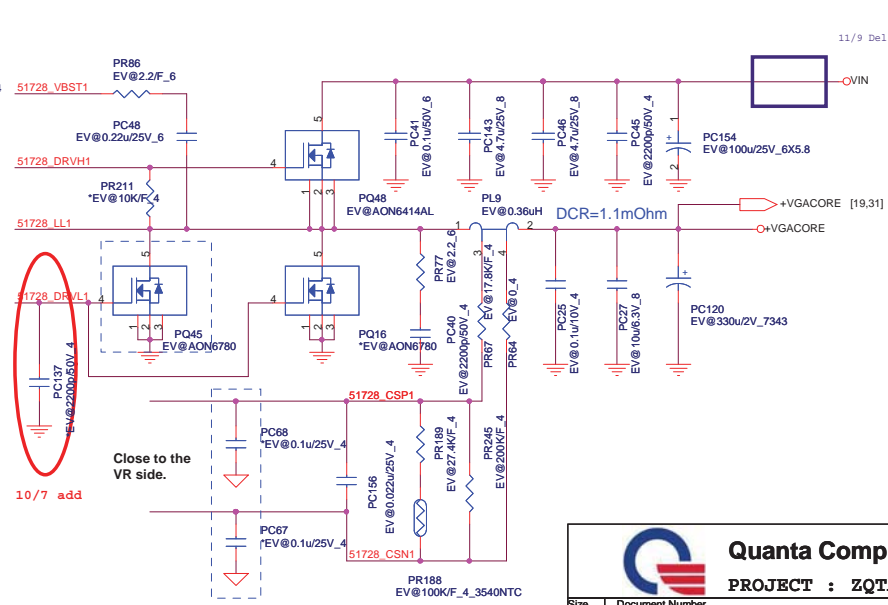
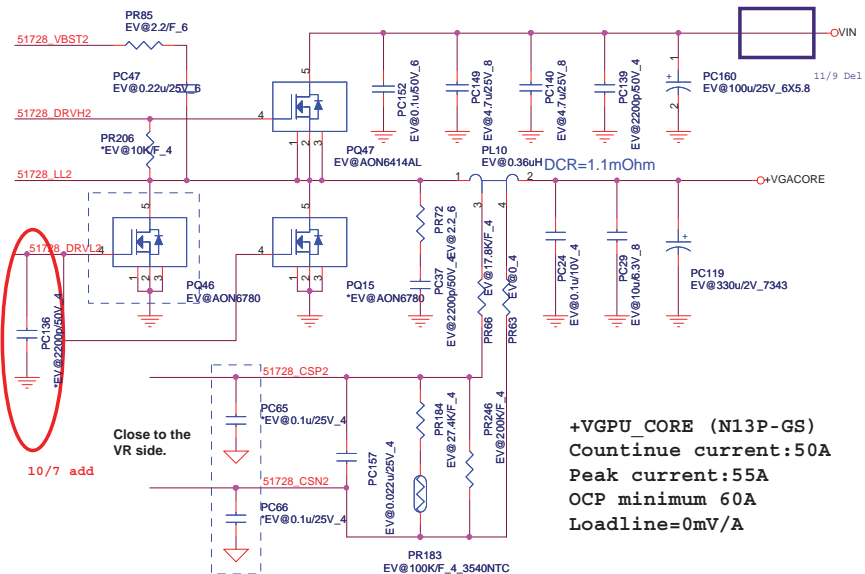
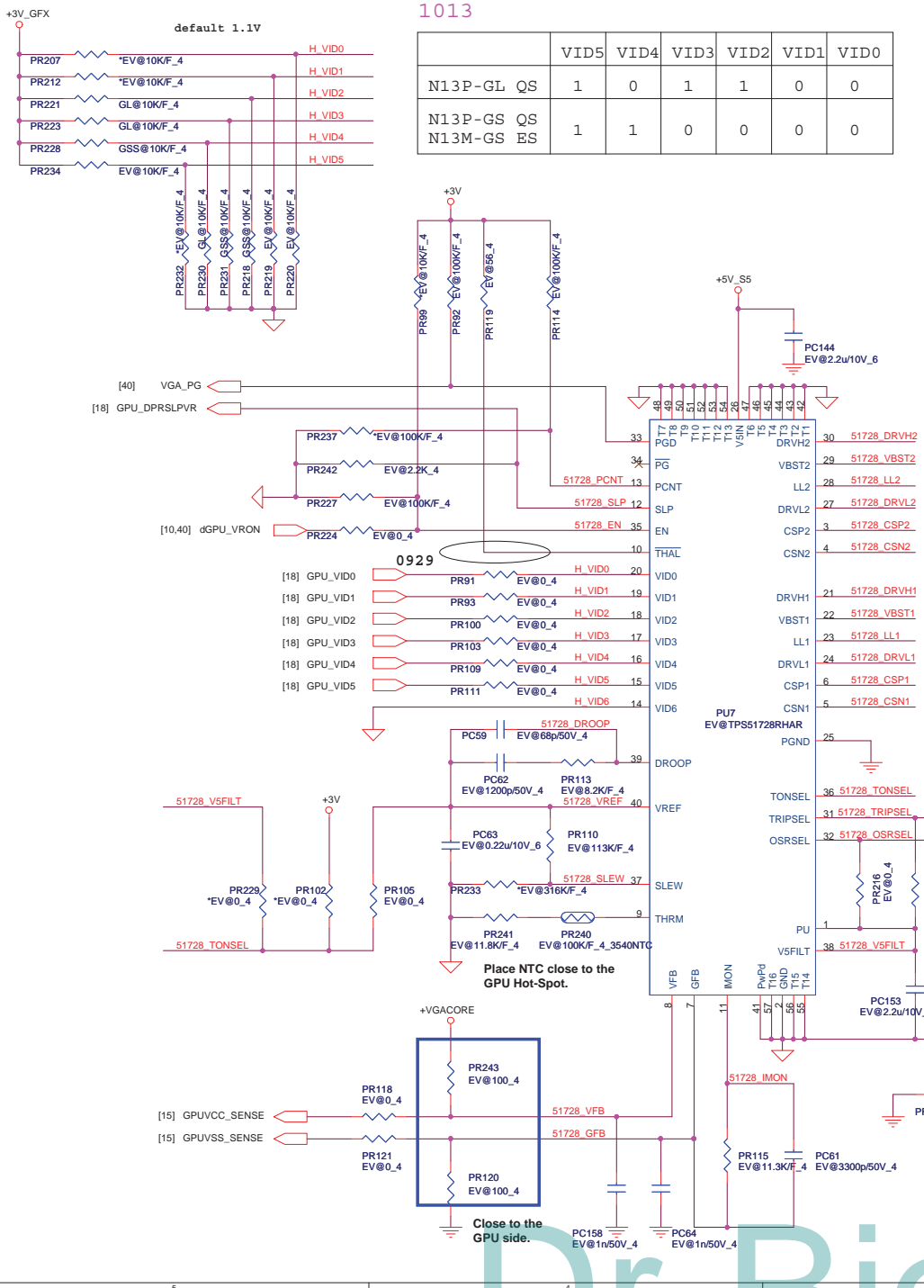
OCP=7A  
 $I_{ripple} = (19 - 0.9) * 0.9 / (2.2u * 300K * 19)$   
= 1.299A  
 $R_{th} = 14mohm * 8 * (7 - 0.65) / 10uA$   
= 71.125K  
Ipeak = 8.299A

**Quanta Computer Inc.**  
PROJECT : ZQTA/ZQSA

Size	Document Number	Rev
	VCCSA(RT8241DZ)	1A
Date:	Friday, November 11, 2011	Sheet 38 of 44

1013

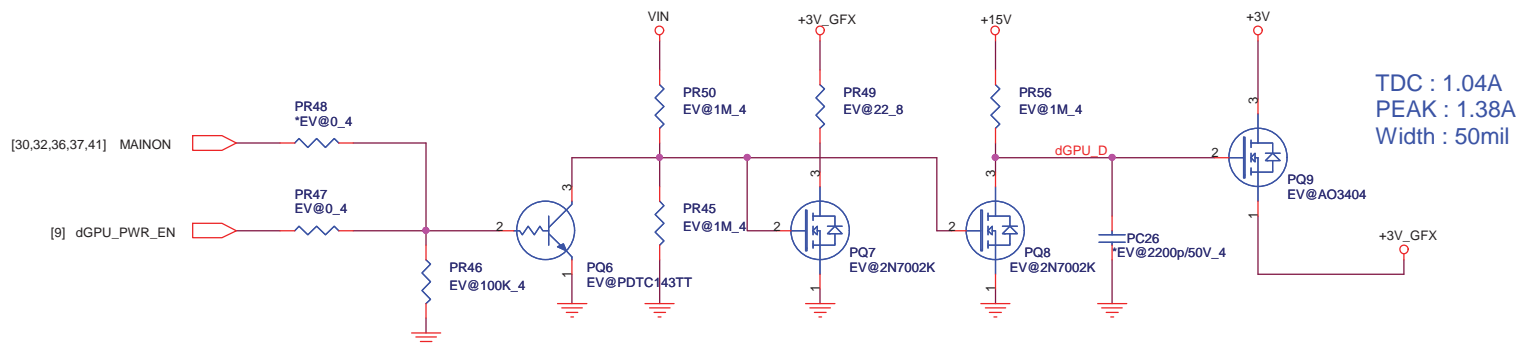
	VID5	VID4	VID3	VID2	VID1	VID0
N13P-GL QS	1	0	1	1	0	0
N13P-GS QS	1	1	0	0	0	0
N13M-GS ES						



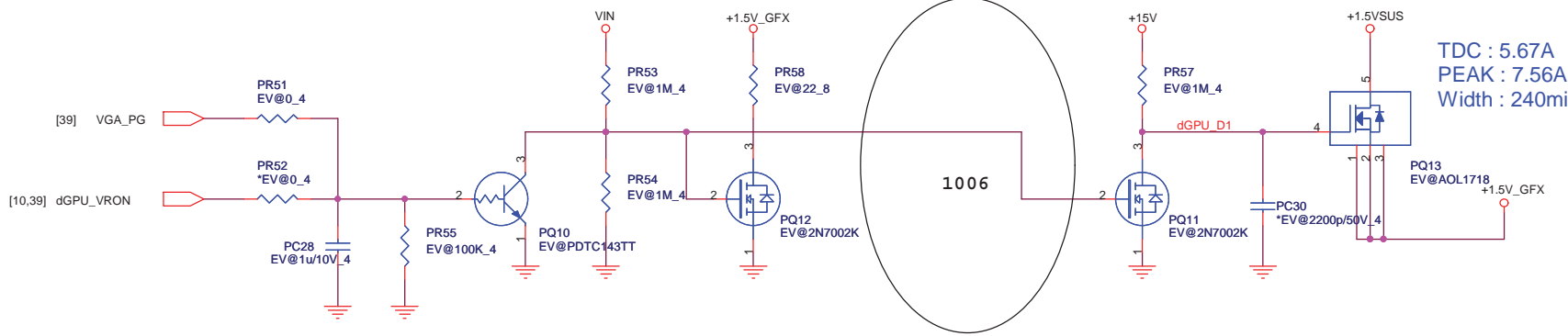
**Quanta Computer Inc.**  
**PROJECT : ZQTA/ZQSA**

Size	Document Number	Rev
	<b>VGPU Core (TPS51728)</b>	1A
Date	Friday, November 11, 2011	Sheet 39 of 44

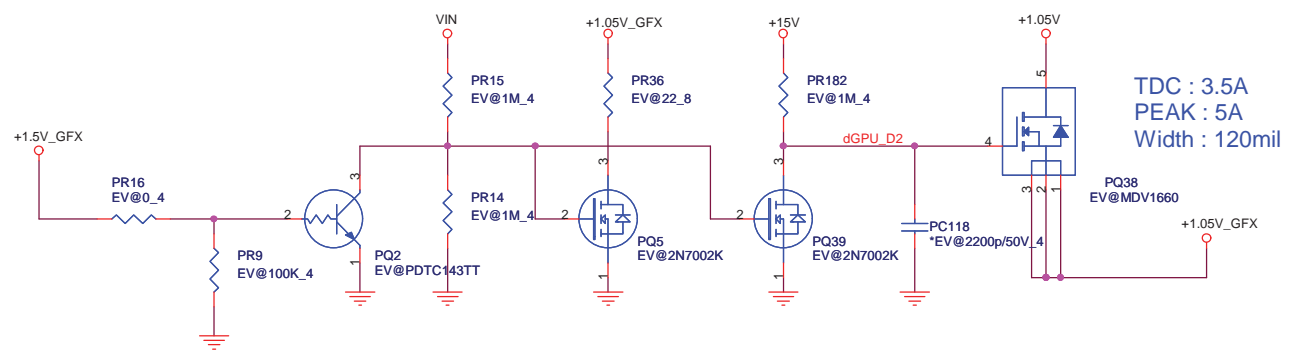
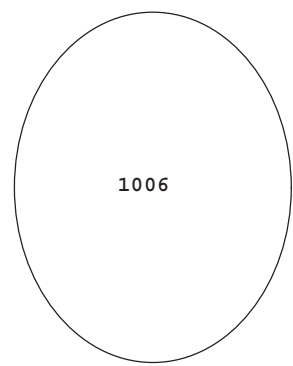
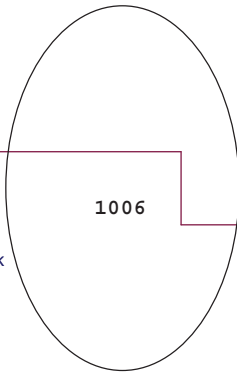
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TDC : 1.04A  
 PEAK : 1.38A  
 Width : 50mil




TDC : 5.67A  
 PEAK : 7.56A  
 Width : 240mil

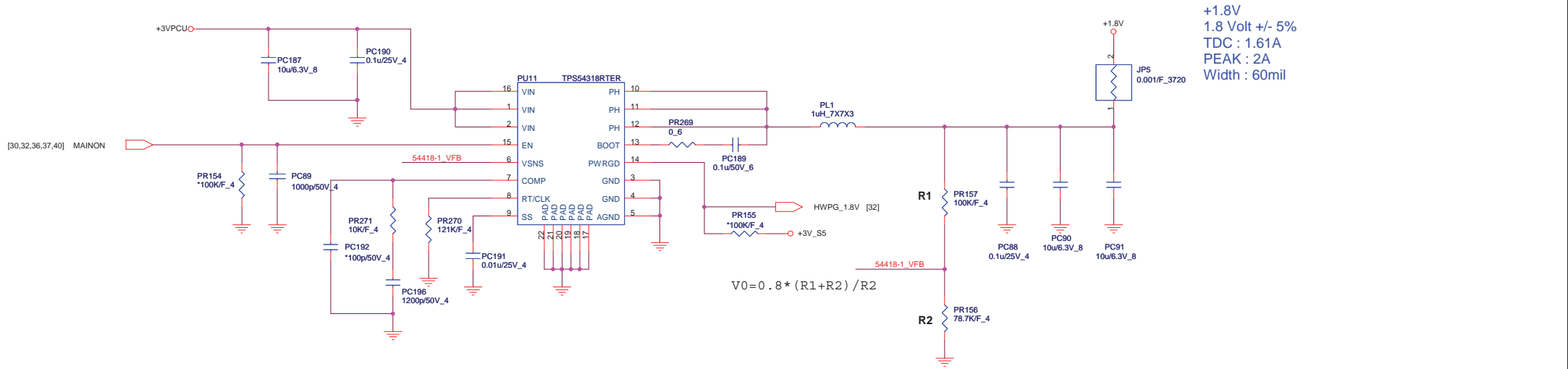


TDC : 3.5A  
 PEAK : 5A  
 Width : 120mil

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 <b>Quanta Computer Inc.</b> PROJECT : ZQTA/ZQSA		Rev
		1A
Size	Document Number	Date: Friday, November 11, 2011
GPU_PWR		Sheet 40 of 44

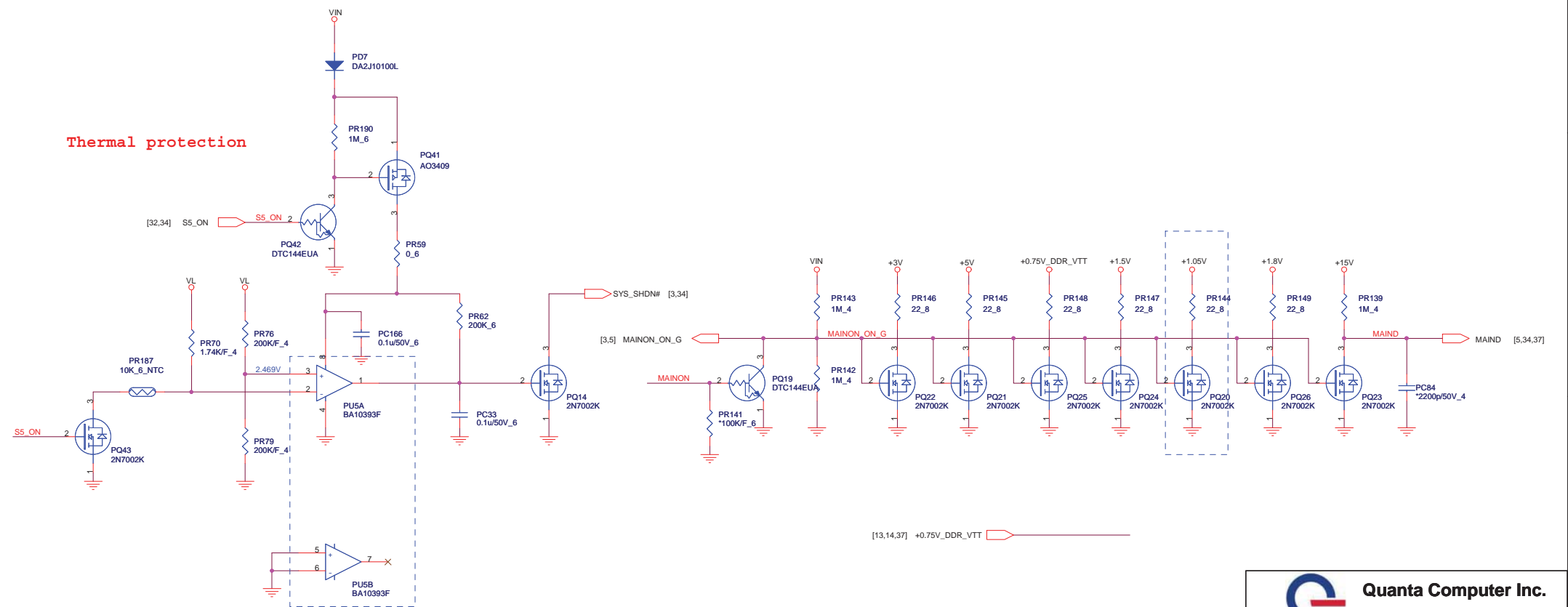





+1.8V  
 1.8 Volt +/- 5%  
 TDC : 1.61A  
 PEAK : 2A  
 Width : 60mil

$$V0 = 0.8 * (R1 + R2) / R2$$

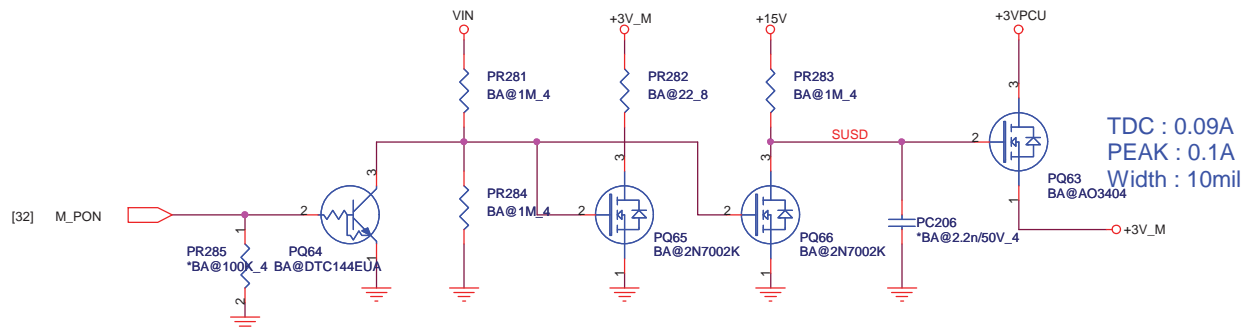
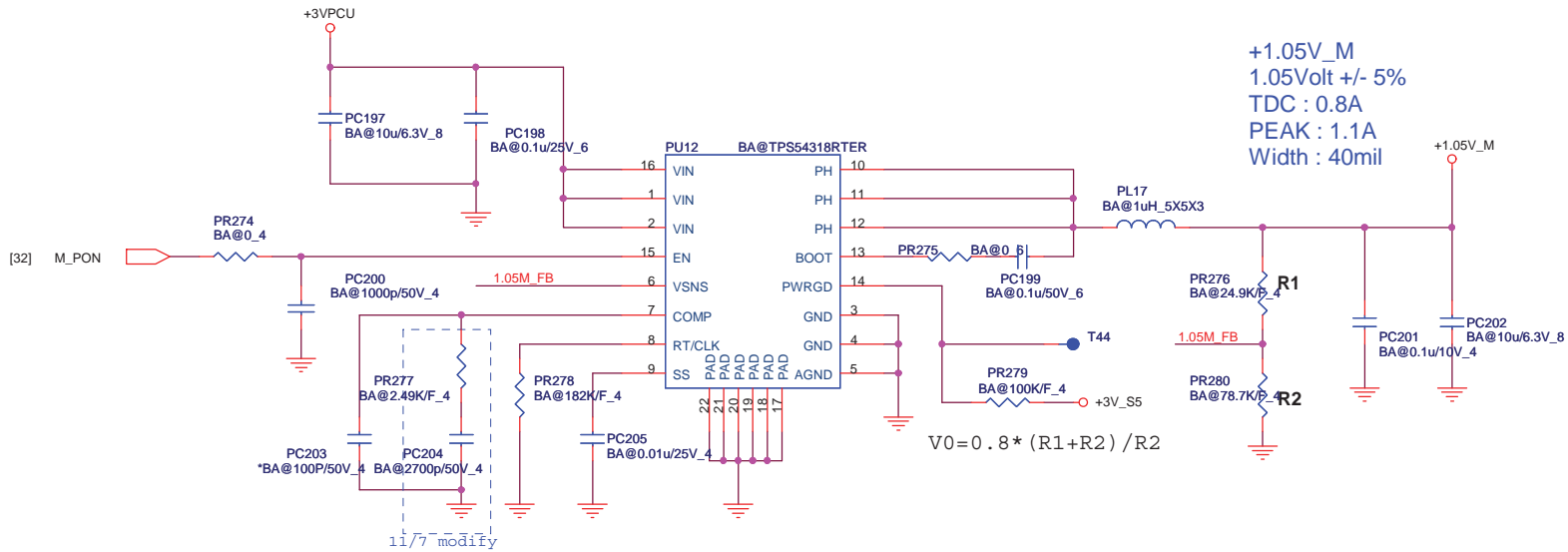
**Thermal protection**




For EC control thermal protection (output 3.3V)

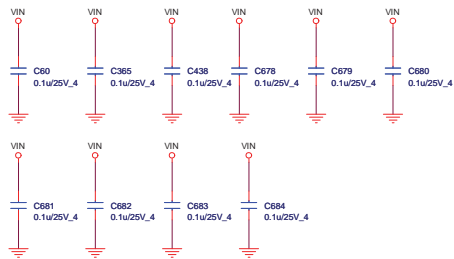
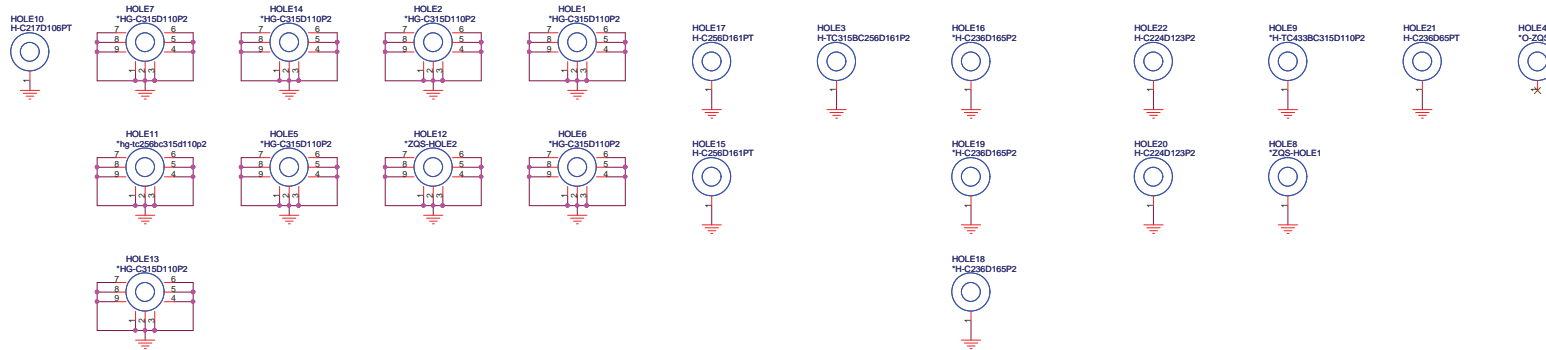
 <b>Quanta Computer Inc.</b> <b>PROJECT : ZQTA/ZQSA</b>			Rev
			1A
Size	Document Number		
	<b>+1.8V/Discharge/Thermal</b>		
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Model	date	CHANGE LIST
<b>ZASA/ZSQTA</b>	<b>9/26</b>	page3 : add R511,R525,R527,R528,R529 for Discrete Only &PCH_JTAG_TDO net change pull-up from +3V_S5 to +1.05 rail
	<b>9/27</b>	Update power circuit Page19 : add C3777,C3778
	<b>9/30</b>	Page18 : add Q3508 for U7 GPU_THERMAL_ALERT net Page31 : Del CN1
	<b>10/3</b>	Page18 : add dGPU_ACDC# net to U7 GPIO04 & add R347 Page22 : add R557,R554 to pull-down & R548,R547 stuff for Discrete only Page25 : add R3693,C116 for ODD zero power circuit
	<b>10/4</b>	Page31 : CN8 add board id3 & board id4 net for touch pad ID control
	<b>10/5</b>	Page31 : CN8.2,CN8.3 add CLK_SDATA & CLK_SCLK net for touch pad & add R278,R279 Page15 : U41 Power rail change to +3V_GFX Page24 : Del Q16 no't support wake up function Page18 : add Q3509 for dGPU_ACDC# net Page31 : add L35,R3694,R3695 for touch pad 5V & 3V option & add R297,R295 Fan PWR option
	<b>10/6</b>	Page17 : IFPAB_PLLVDD rail change from +1.8V_GFX to +3V_GFX Page27 : U6 change footprint Page39 : PWR engineer add PQ3006,PQ3005 Page40 : PWR engineer Del PR193,PQ51,PQ54
	<b>10/7</b>	Page16 :add C3779,C3780 Page29 :add C542,C530 for EMI solution & C544 change to 4.7u 0603 type Page35 :PWR engineer add PC3037,PC3038,PC3039 Page35 :PWR engineer add PC3035,PC3036
	<b>10/11</b>	Page8 :add R376,R381,R393,R407,R421,R434 for Dual SPI ROM Page9 :U13 power rail change to +3V Page10 :SV_DET_NC net add R250 to pull-down Page27 :add R133,R235 Page30 :C443 change to 3528 type & add C366,R340 Page31 :CN2.27 pin change to +VGACORE Page32 :add R330,R328 pull-up +3VPCU for GPUT_CLK,GPUT_DATA net
	<b>10/14</b>	Page20 :add C3781,C3782,R3569,R3570,R3571,R3576 Page21 :add C3783,C3784,R3577,R3578,R3579,R3581

 <b>Quanta Computer Inc.</b> <b>PROJECT : ZQTA/ZQSA</b>	<b>DOC NO.</b>	<b>PROJECT MODEL :</b> ZQTA/ZQSA	<b>APPROVED BY:</b>	<b>DATE:</b>
<b>Change list</b> Date: Friday, November 11, 2011 Sheet 44 of 44		<b>Rev</b> 1A	<b>PART NUMBER:</b>	<b>DRAWING BY:</b>

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