AMD KABINI EA/EG-40/50
PX /UMA Schematics Document
AMD FT3 APU
AMD GPU SUN XT M2/64bit

EAEG50 KB UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cover Page

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A4	KABINI	

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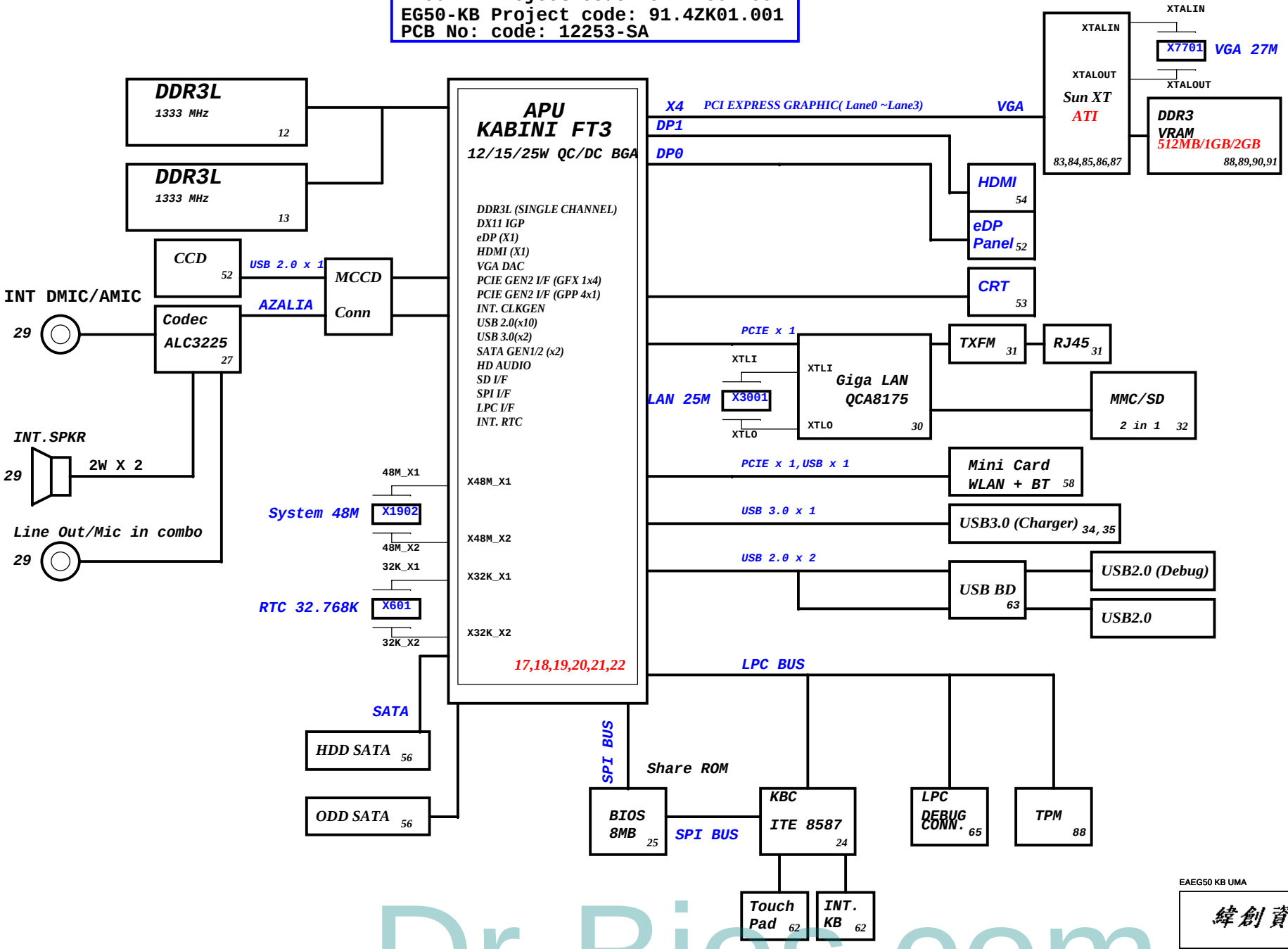
AMD KABINI

EA40-KB Project code: 91.4ZF01.001
PCB No: code: 12247-SA
EA50-KB Project code: 91.4YU01.001
EG50-KB Project code: 91.4ZK01.001
PCB No: code: 12253-SA



SYSTEM DC/DC TPS51225 45	
INPUTS	OUTPUTS
DCBATOUT	5V_CHARGER (6.52A) 3D3V_S5(5.05A)

SYSTEM DC/DC RT8207 49	
DCBATOUT	1D5V_S3(10.5A)
RT8207	
DCBATOUT	0D75_S0(1.2A)

SYSTEM DC/DC RT8068 50	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S5(3.05A
SY8208 48 , 51	
DCBATOUT	1D5V_S5(5.4A)
DCBATOUT	0D95V_S5(5.6A)

TPS22966 36	
5V_CHARGER	5V_S5(5.83A)
	5V_S0(3.5A)
TPS22966 36	
3D3V_S5	3D3V_S0(2.8A
1D5V_S5	1D5V_S0(0.6A
TPS22966 36	
1D8V_S5	1D8V_S0(1.5A
0D95V_S5	0D95V_S0(5.6A)

CHARGER BQ24737 44	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 5.5A

CPU DC/DC ISL6267 46,47	
INPUTS	OUTPUTS
DCBATOUT	APU_VDD 0.3~1.4V,21A APU_VDDNB 0.7~1.325V,17A

VGA DC/DC TPS51728 82	
DCBATOUT	VGA_CORE(35.5A)
TPS22966 83	
3D3V_S0	3D3V_VGA_S0
1D5V_S5	1D5V_VGA_S0
TPS22966 83	
1D8V_S5	1D8V_VGA_S0
0D95V_S5	0D95V_VGA_S0

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Title: Block Diagram
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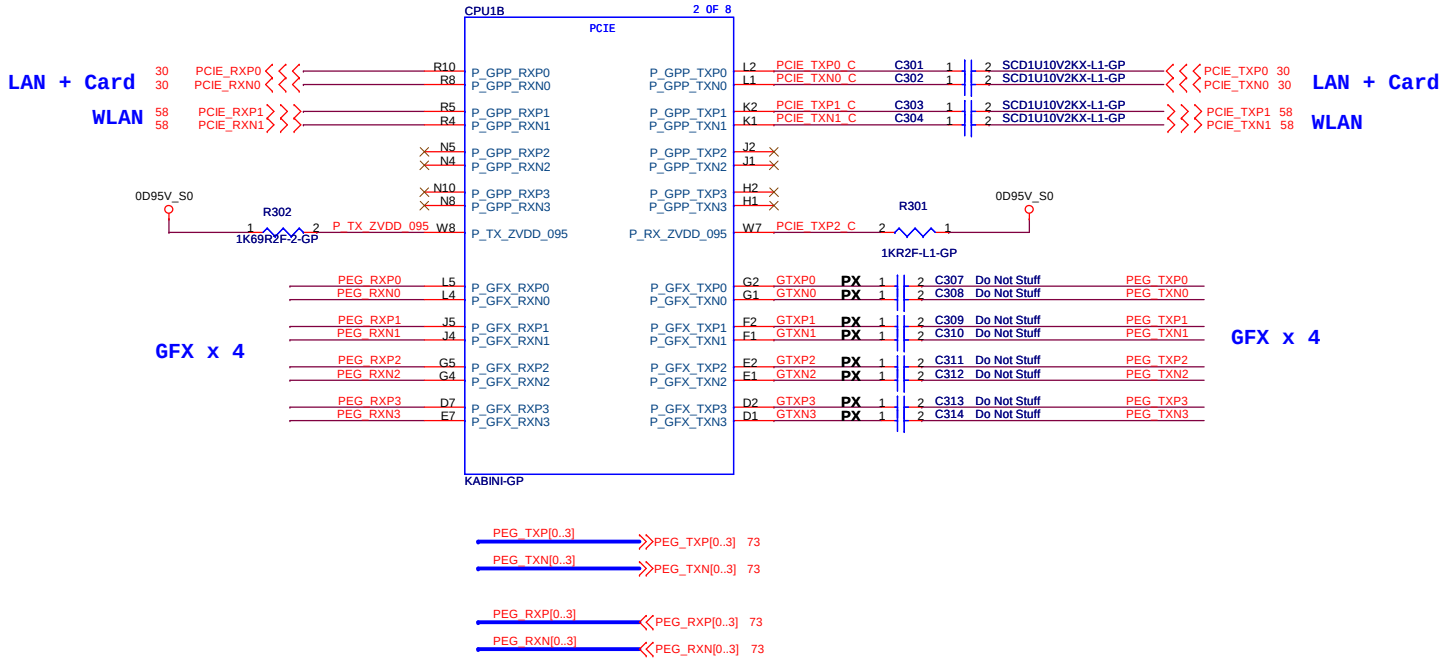

PCIE Table

0	LAN + Card
1	WLAN
2	NC
3	NC

71.KABIN.B0U IC CPU Kabini 4110 1.5GHz 15W4C FT3 ES2 BGA

71.KABIN.C0U IC CPU Kabini 5110 2.0GHz 25W4C FT3 ES2 BGA

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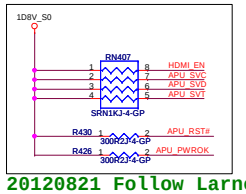
Title: CPU_PCIE

Size: A3 | Document Number: KABINI | Rev:

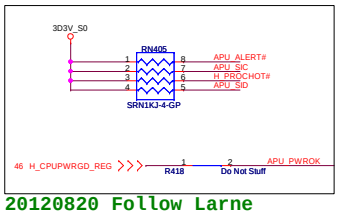
Date: Monday, February 04, 2013 | Sheet 3 of 102



20120821 Follow Larne

TABLE 6. PRE-PWROK METAL VID CODES

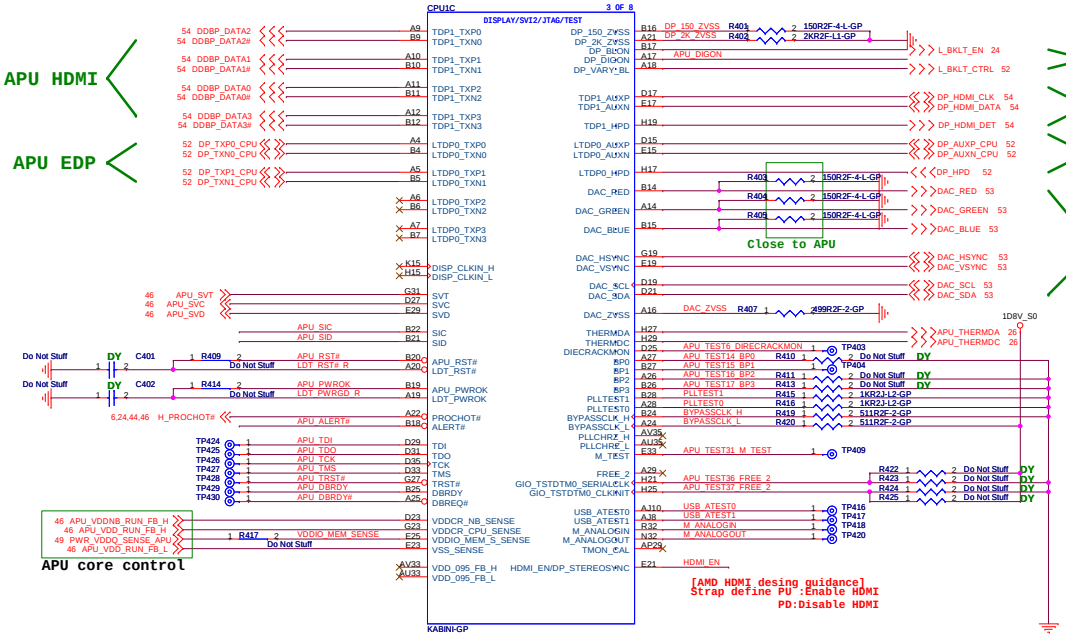
SVC	SVD	OUTPUT VOLTAGE (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8



20120820 Follow Larne

APU HDMI

APU EDP



APU EDP

APU HDMI SMB

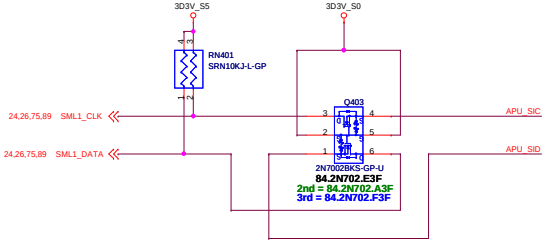
APU EDP

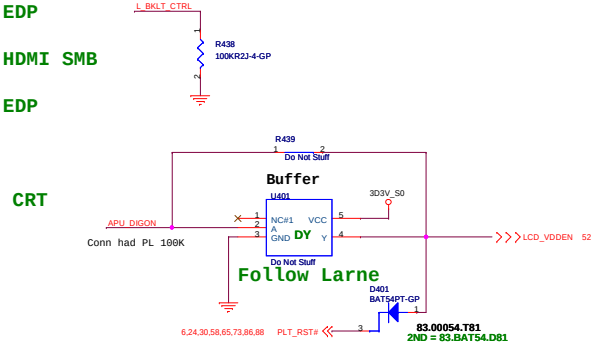
APU CRT

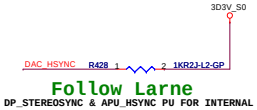
Close to APU

APU core control

[AMD HDMI desing guidance]
Strap define PU :Enable HDMI
PD:Disable HDMI







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Title: CPU_DISPLAY/CLK/MISC

Size: A2 | Document Number: KABINI | Rev:

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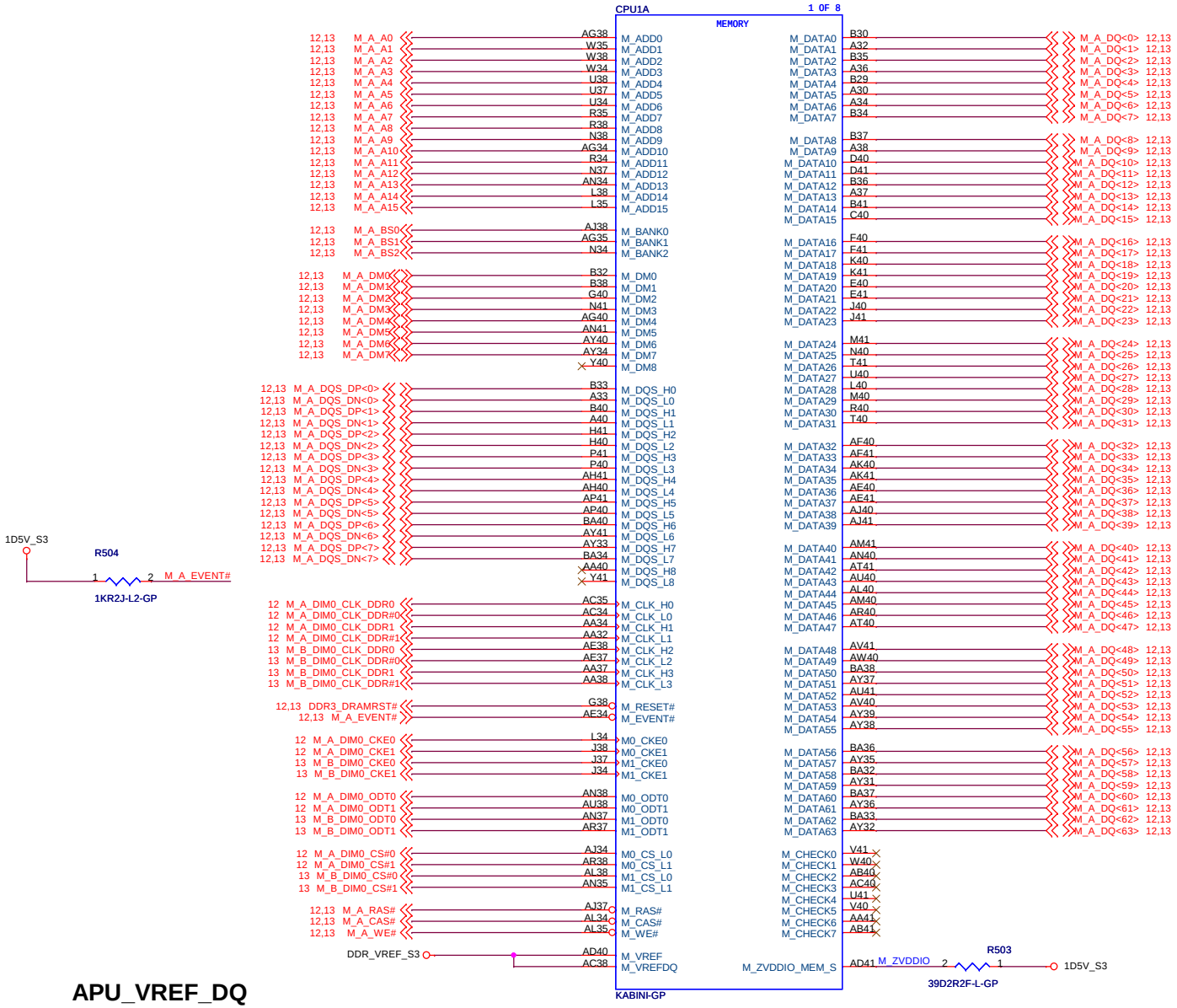
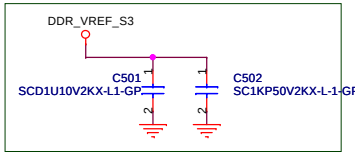


APU_VREF_DQ



LAYOUT: place them close to APU

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Title	CPU_DDR	
Size A3	Document Number KABINI	Rev
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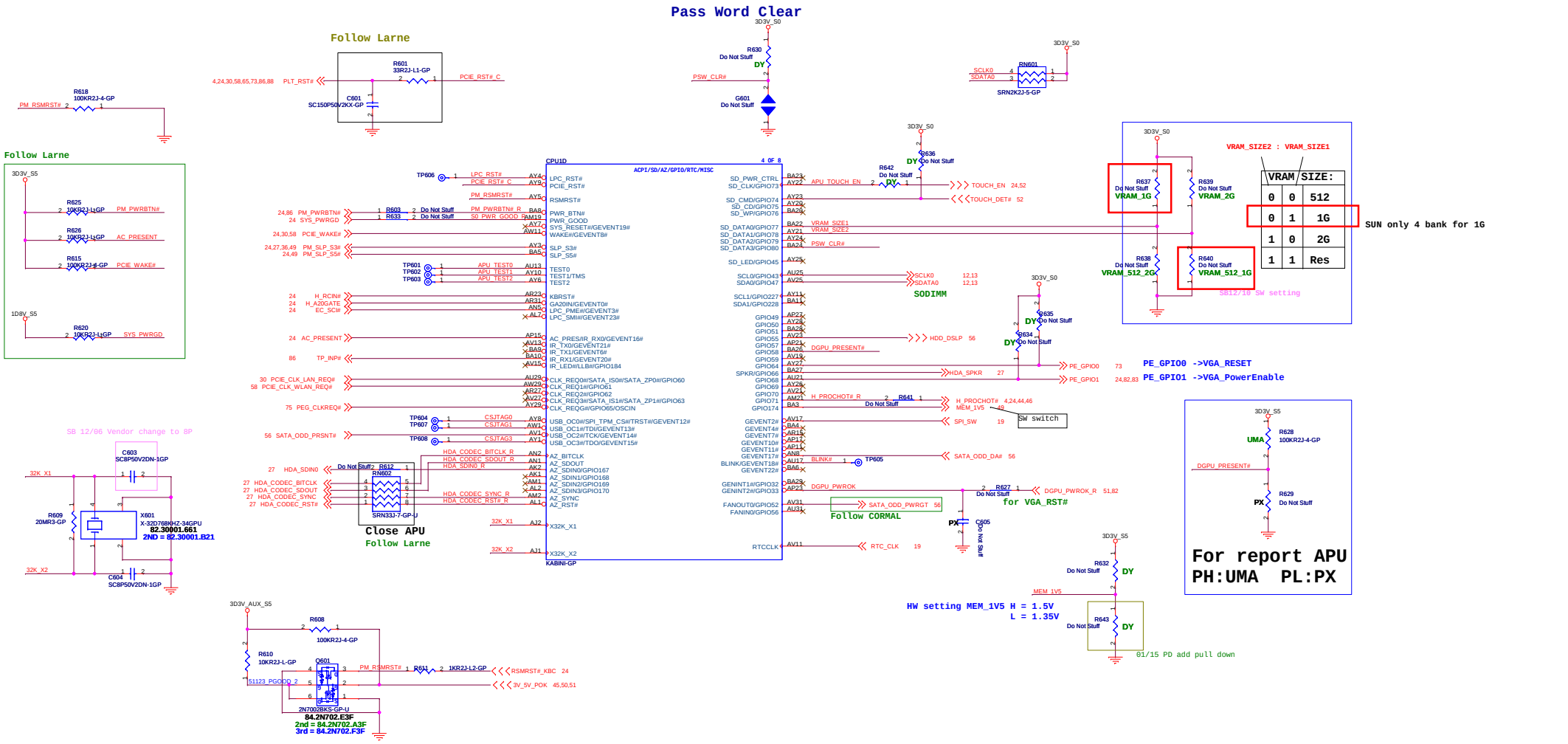

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Title: CPU (ACPI/SD/AZ/GPIO/RTC)

Size: Custom | Document Number: KABINI | Rev:

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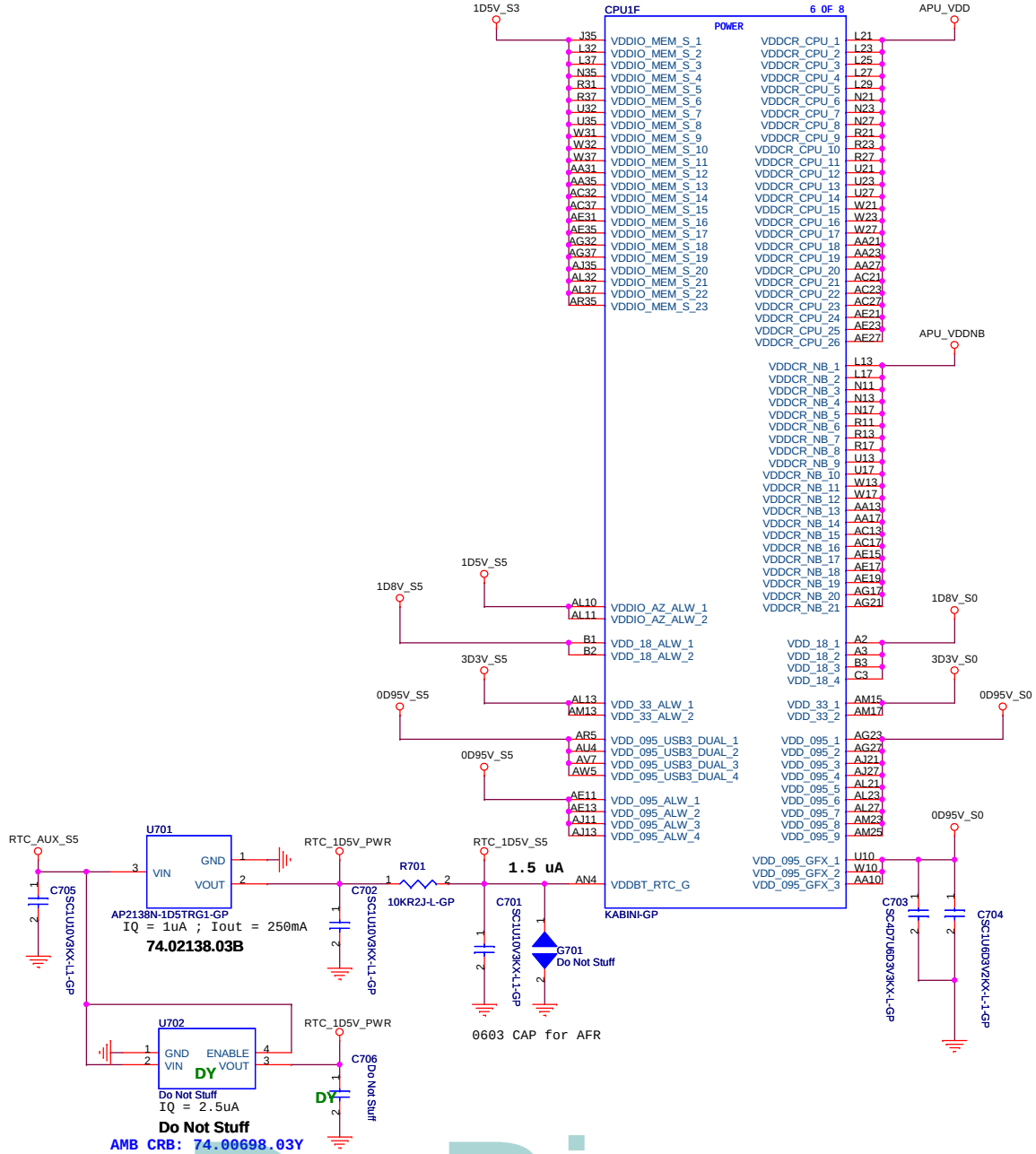

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Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_VCC CORE

Size: A3 | Document Number: KABINI | Rev:

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Title: CPU_VCC GFXCORE

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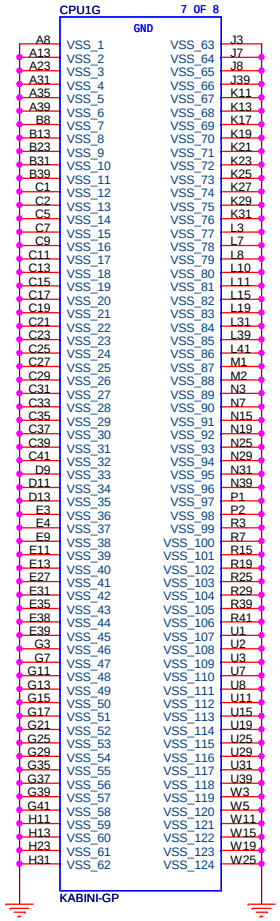

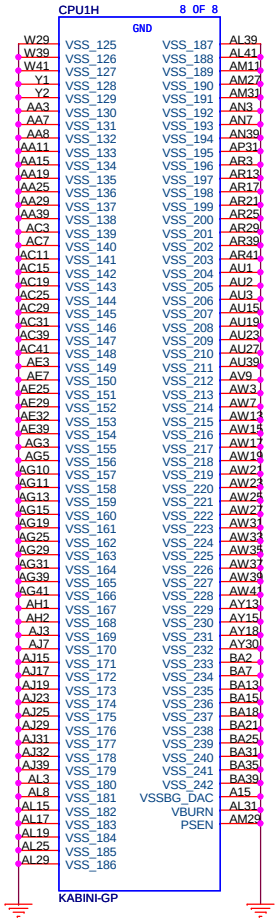

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Title: **CPU_VSS**

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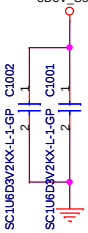
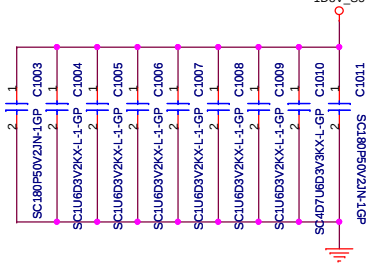
200mA

3D3V_S5



500mA

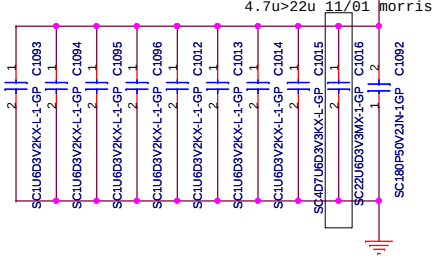
1D8V_S5



1000mA

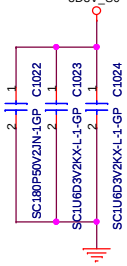
0D95V_S5

4.7u>22u 11/01 morris



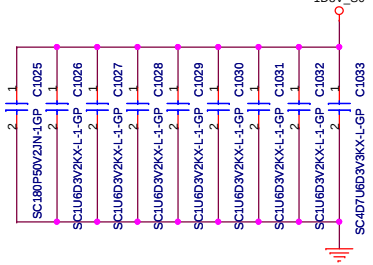
200mA

3D3V_S0



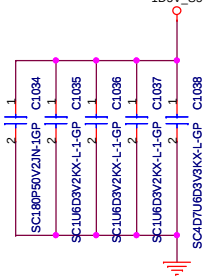
1500mA

1D8V_S0



100mA

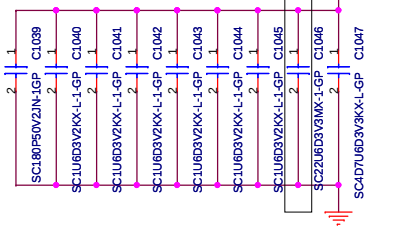
1D5V_S5



5600mA

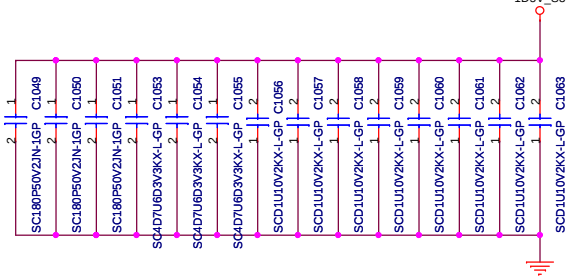
0D95V_S0

4.7u>22u 11/01 morris

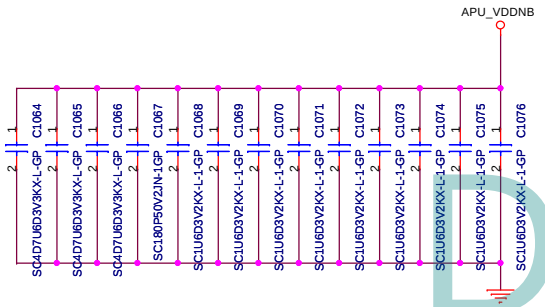


3000mA

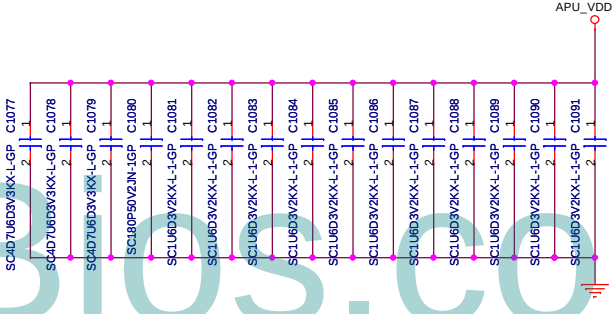
1D5V_S3



APU_VDDNB



APU_VDD



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緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: **CPU_POWER CAP1**

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Title

CPU_POWER CAP2

Size	Document Number	Rev
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01/14 PD change location name for factory issue

DM2

Intel HR DM tied to GND
AMD still following previous design

110110 for RF
Close to DM1

Place these caps close to VTT1 and VTT2.

Layout Note:
Place these Caps near SO-DIMMA.

SODIMM A DECOUPLING

DDR3-204P-123-GP
62.10017.761
2nd = 62.10024.M51
3rd = 62.10024.G11

Follow JE50-SB
H = 4mm

01/15 PD remove 62.10017.X31 for factory issue

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Title: DDR3 SODIMM 1

Size: A2 | Document Number: KABINI | Rev:

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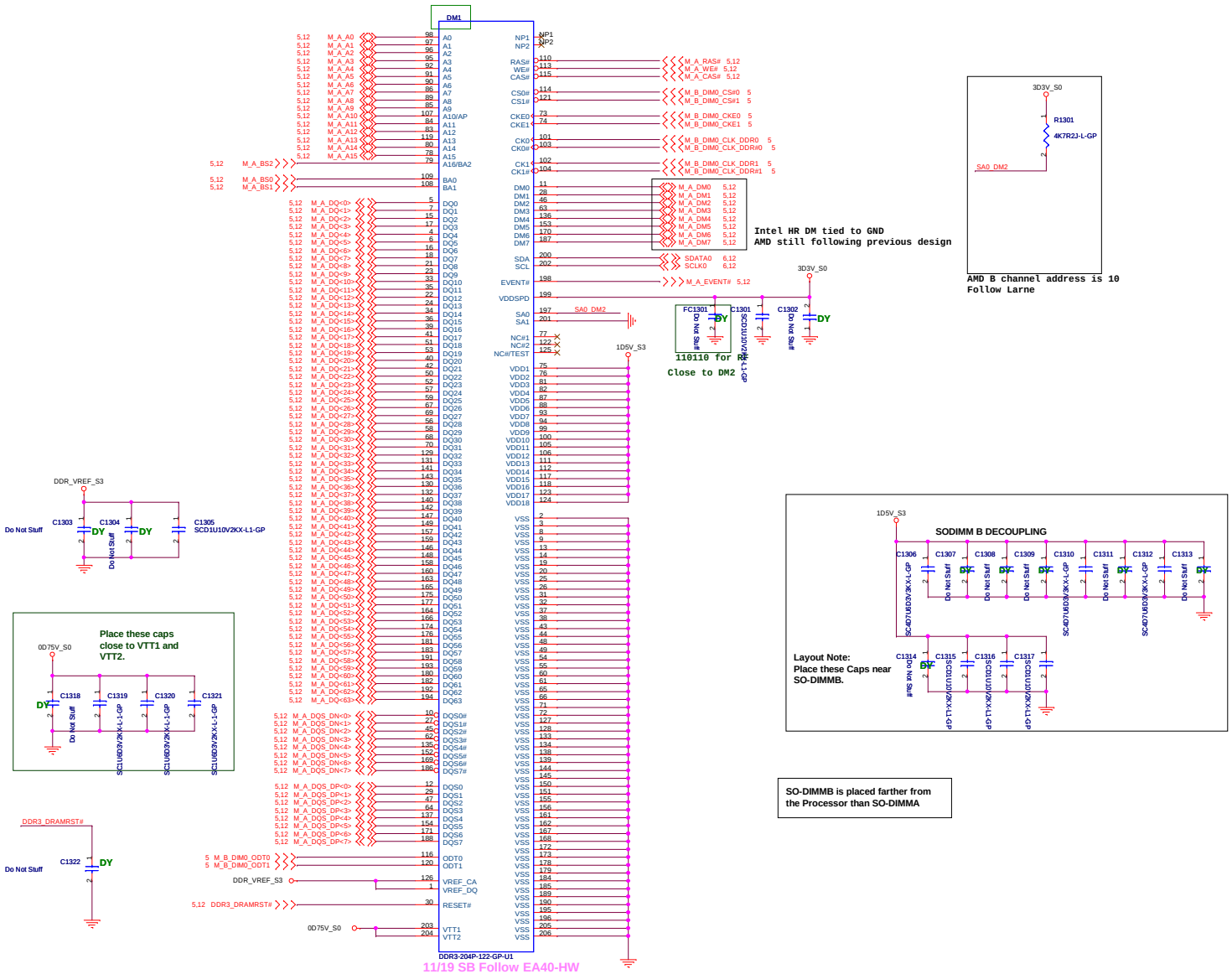
01/14 PD change location name for factory issue



62.10017.Z51

2nd = 62.10024.G21

3rd = 62.10024.M31

01/15 PD remove 62.10017.X41 for factory issue

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Title: DDR3 SODIMM 2

Size: A2 | Document Number: KABINI | Rev:

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Title: **CPU_PCIE/SMBUS/CLK/CL/SPI**

Size	Document Number	Rev
A	KABINI	

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SATA Table

0	HDD
1	ODD

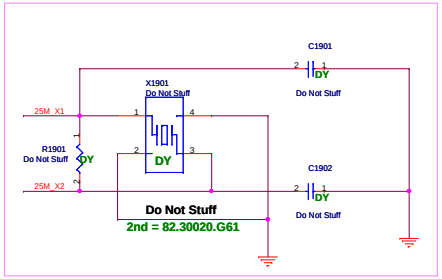
USB Table

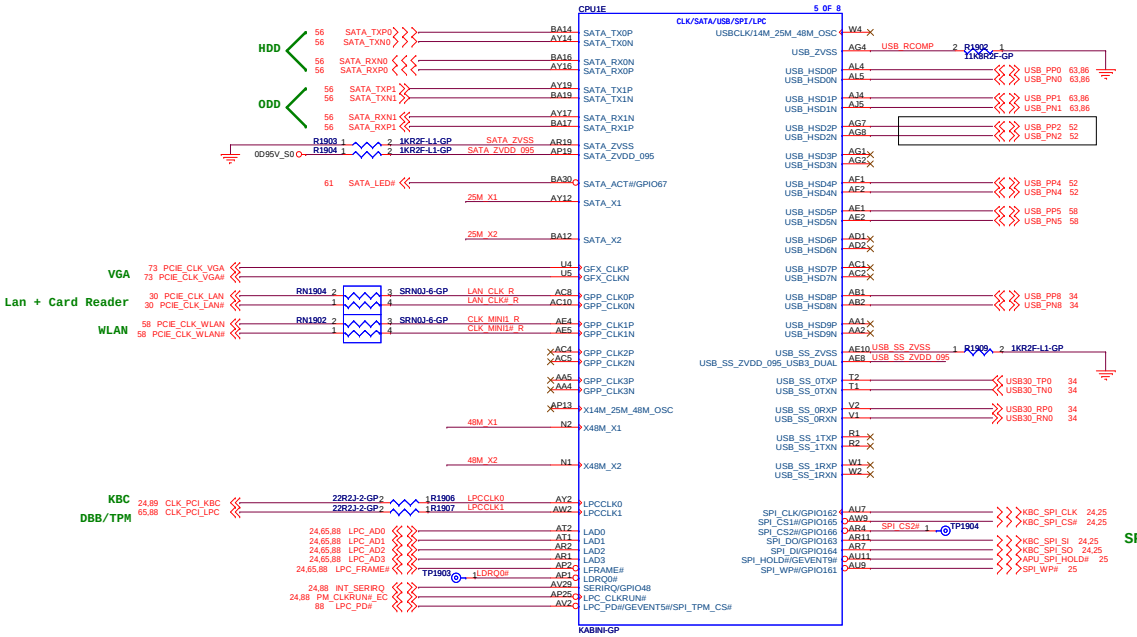
Pair	Device
0	USB2.0 Debug (DB Conn)
1	USB2.0 (DB Conn)
2	Touch Panel
3	
4	CCD (CCD Conn)
5	WLAN + BT (Mini PCI-E)
6	
7	
0/8	USB3.0 & USB 2.0 Charger (MB)
1/9	

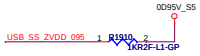
Xtal Table

		CLK
0	System & USB	48M
1	RTC	32.768K
2	SATA	25M
3	LAN	25M
4	VGA	27M

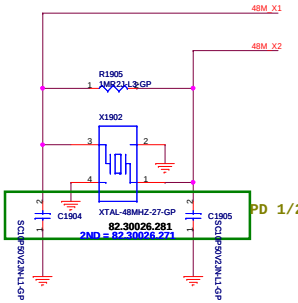
SB 11/27 25M XTAL Reserved for AMD





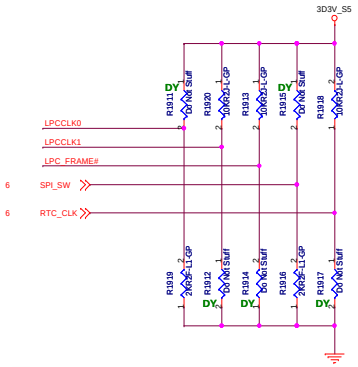


SPI SHARE ROM



PD 1/25 for USB3.0 SSC tuning

SYSTEM STRAPPINGS



	LPC_CLK0	LPC_CLK1	LFRAME_L	EXPCARD_PCIE_PWREN#	RTC_CLK
PULL HIGH	BOOT FAIL TIMER ENABLED	CLKGEN ENABLED (DEFAULT)	SPI ROM (DEFAULT)	1.8V SPI ROM (DEFAULT)	NORMAL POWR UP/RESET TIMING (DEFAULT)
PULL LOW	BOOT FAIL TIMER DISABLED (DEFAULT)	CLKGEN DISABLED	LPC ROM	3.3V SPI ROM	FAST POWER UP/RESET TIMING FOR SIMULATION

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Title: CPU_SATA/USB/LPC/SPI/CLK

Size: A2 | Document Number: KABINI | Rev:

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Title: CPU_GPIO/MISC

Size: A4 | Document Number: KABINI | Rev:

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Title: **CPU_POWER1**

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Title: **CPU_RSVD**

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Title: **CPU_VSS**

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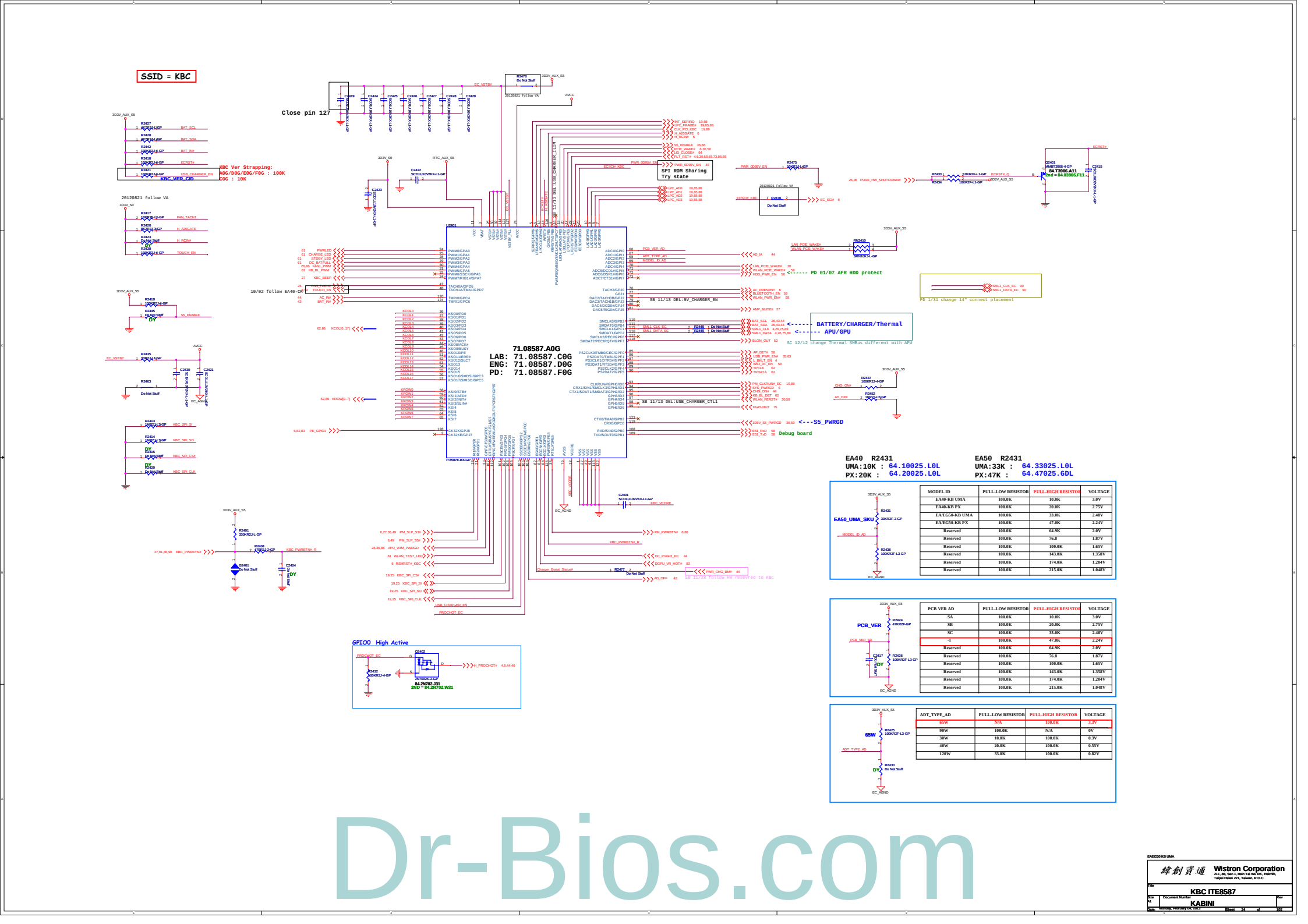


MODEL ID	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
EA40-KB UMA	100.0K	10.0K	3.0V
EA40-KB PX	100.0K	20.0K	2.75V
EA/EG50-KB UMA	100.0K	33.0K	2.48V
EA/EG50-KB PX	100.0K	47.0K	2.24V
Reserved	100.0K	64.9K	2.0V
Reserved	100.0K	76.8	1.87V
Reserved	100.0K	100.0K	1.65V
Reserved	100.0K	143.0K	1.358V
Reserved	100.0K	174.0K	1.204V
Reserved	100.0K	215.0K	1.048V

PCB VER AD	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.48V
-1	100.0K	47.0K	2.24V
Reserved	100.0K	64.9K	2.0V
Reserved	100.0K	76.8	1.87V
Reserved	100.0K	100.0K	1.65V
Reserved	100.0K	143.0K	1.358V
Reserved	100.0K	174.0K	1.204V
Reserved	100.0K	215.0K	1.048V

ADT_TYPE_AD	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
65W	N/A	100.0K	3.3V
90W	100.0K	N/A	0V
30W	10.0K	100.0K	0.3V
40W	20.0K	100.0K	0.55V
120W	33.0K	100.0K	0.82V

EA/EG50 KB UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC ITE8587

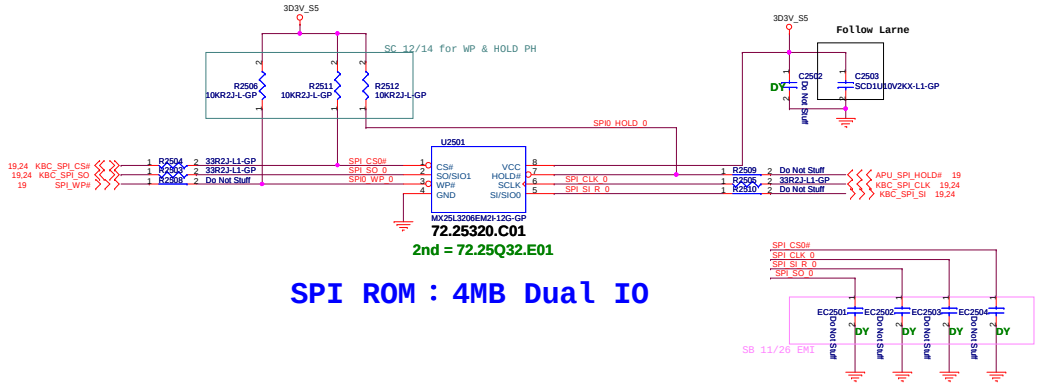
Size: A1 | Document Number: KABINI | Rev:

Date: Monday, February 04, 2013 | Sheet 24 of 52

SSID = Flash.ROM

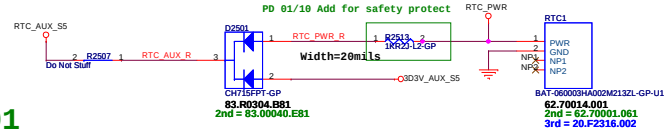
SPI FLASH ROM (4M byte) for KBC

PD 1/28 SPI ROM：4MB Dual IO
1st. MXIC : 72.25320.C01
2nd. WINBOND : 72.25Q32.E01
(手置件)請PCC移至DIP件



SPI ROM：4MB Dual IO

SSID = RBAT



CR2032額外備料:
1.KTS: 23.20068.001
2.DBV: 23.22065.001

EAEG50 KB UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash/RTC
Size: | Project Name: KABINI | Rev: SA
Date: Tuesday, February 19, 2013 | Sheet 25 of 102

SSID = Thermal

Thermal sensor NCT 7718W

Layout notice :
Both DXN and DXP routing 10 mil
trace width and 10 mil spacing.

3D3V_S0
R2601 Do Not Stuff 20120831
C2601 SCD1U10V2KX-L1-GP

Q2601 PMBS3904-1-GP
84.03904.L06
2nd = 84.03904.E11 PD 01/10 Add 2nd source
R2604 Do Not Stuff DY
C2604 SC470P50V3JN-2GP
C2605 SC2K2P50V2KX-L-GP
P2800_DXP
P2800_DXN
2.System Sensor, Put on palm rest

SC 12/12 for change Thermal SMBus with APU
U2601 NCT7718W-GP 74.07718.0B9
THERM_VDD
THERM_SYS_SHDN#
NCT_CLK
NCT_DATA
ALERT# SYS
T8-R5 R2605 18K7R2F-GP
1.H/W T8 Shutdown

SC for EA50 & EA40: 74.83771.ABG

3D3V_S0
RN2602 Do Not Stuff DY
APU-R5 R2611 Do Not Stuff DY
U2602
THERM_VDD
THERM_APU_SHDN#
NCT2_CLK
NCT2_DATA
ALERT# APU
APU_THERMDA
APU_THERMDC
C2607 Do Not Stuff DY
Do Not Stuff
2.APU H/W Shutdown

3D3V_S0
RN2601 SRN2K2J-5-GP
2N7002BKS-GP-U
Q2602 84.2N702.E3F
2nd = 84.2N702.A3F
3rd = 84.2N702.F3F
NCT_CLK
NCT_DATA
NCT_CLK_R
NCT_DATA_R
RN2603 DY Do Not Stuff
RN2604 SRN0J-6-GP
APU PU 3D3V_S5
SML1_CLK 4,24,75,89
SML1_DATA 4,24,75,89
BAT_SCL 24,43,44
BAT_SDA 24,43,44
SC 12/12 change Thermal SMBus different with APU

SC EA50 DY RN2604 , mount RN2603

5V_S0
D2601 CH551H-30PT-GP
83.R5003.C8F
2ND = 83.R5003.H8H
3rd = 83.5R003.08F
C2603 SC4D7U25V5KX-L2-GP
C2602 SCD1U10V2KX-L1-GP
20120904 to 0805

For AFTE
24,86 FAN1_PWM
86 FAN_TACH1_C
24 FAN_TACH1
FAN1 ETY-CON4-33-GP
20.F1579.004
2nd = 20.F1637.004
D2602 CH551H-30PT-GP
83.R5003.C8F
2ND = 83.R5003.H8H
3rd = 83.5R003.08F

For APU Remote Die THERMTRIP#
24,36 PURE_HW_SHUTDOWN#
R2608 Do Not Stuff DY
C2606 SCD1U10V2KX-L1-GP
Q2604 Do Not Stuff
2ND = 84.2N702.W31
APU-R7 R2607 Do Not Stuff DY
THERM_APU_SHDN#
APU_VRM_PWRGD 24,46,86
Q2603 2N7002K-2-GP 84.2N702.J31
2ND = 84.2N702.W31
T8-R7 R2606 2KR2F-L1-GP
THERM_SYS_SHDN#

ALERT# /T_CRIT#
Pull-up Resistor

R5 \ R7	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
2Kohm	77℃	87℃	97℃	107℃	117℃
7.5Kohm	79℃	89℃	99℃	109℃	119℃
10.5Kohm	81℃	91℃	101℃	111℃	121℃
14Kohm	83℃	93℃	103℃	113℃	123℃
18.7Kohm	85℃	95℃	105℃	115℃	125℃

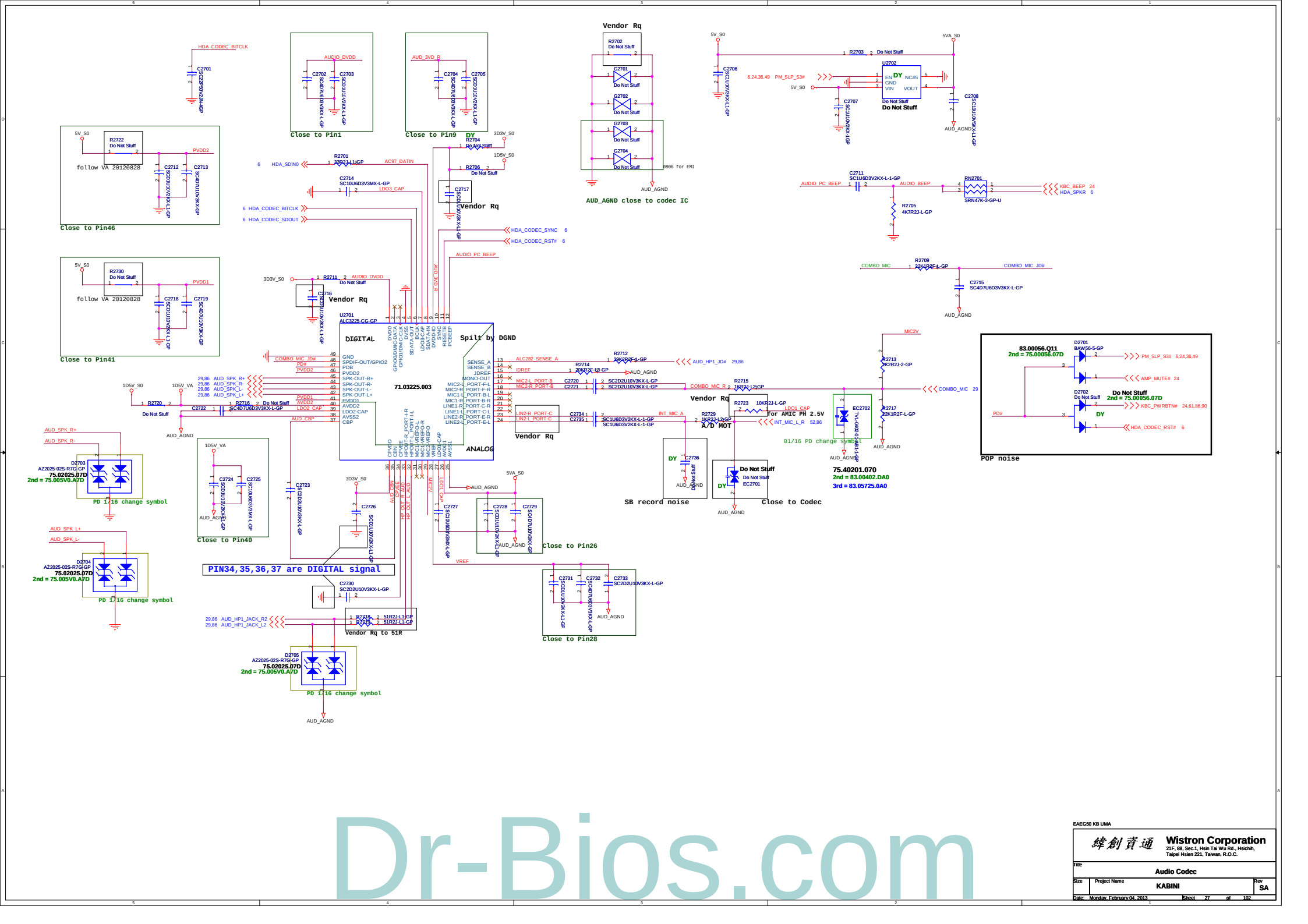
T_CRIT temperature strapping point

T8=85 degree
SYS=85 degree
APU=125 degree

EAEG50 KB UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal 7718/Fan Controllor P2793
Size | Project Name: KABINI | Rev: SA
Date: Monday, February 04, 2013 | Sheet 26 of 102



EAEG50 KB UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Codec

Size | Project Name: KABINI | Rev: SA

Date: Monday, February 04, 2013 | Sheet 27 of 102

EAEG50 KB UMA

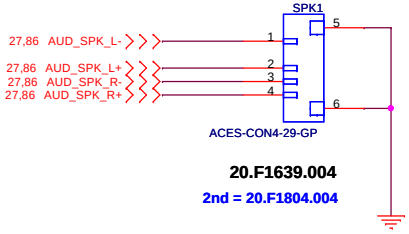
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

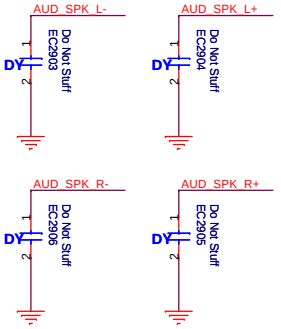
Title	AMP ALC1001	
Size	Project Name: KABINI	Rev: SA
Date: Friday, September 07, 2012	Sheet 28 of 102	

SSID = AUDIO

Speaker

2W 4ohm X 2 speaker

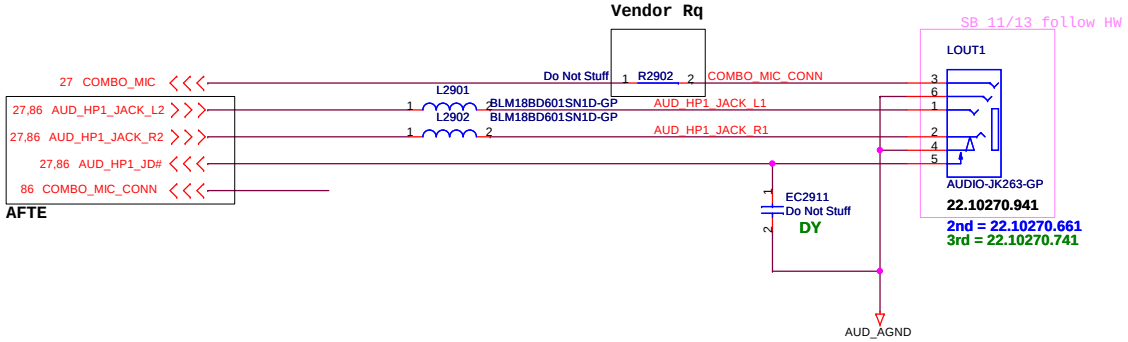




Layout Note:

Trace width=40mil

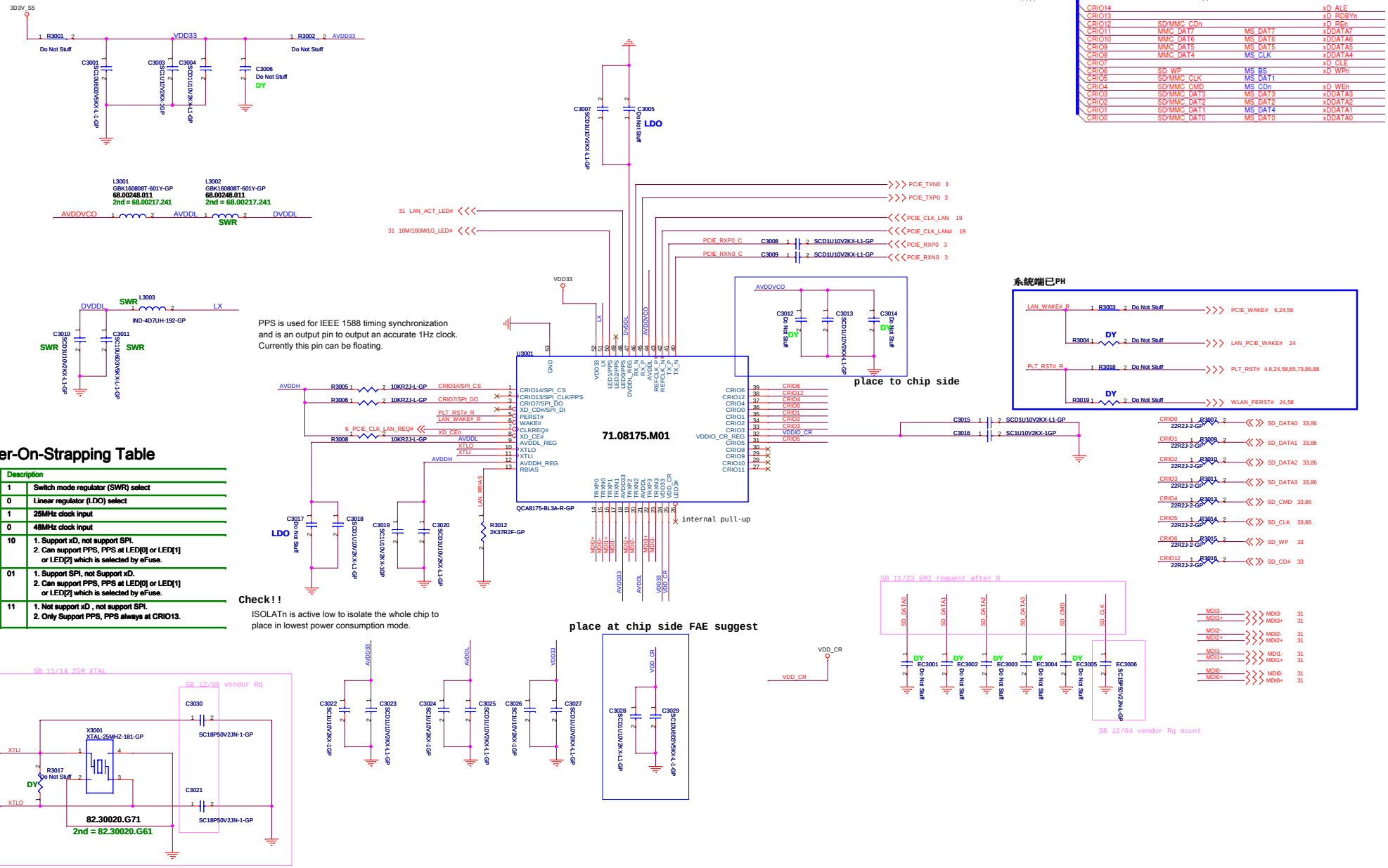
Combo Jack



EAEG50 KB UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Audio Jack	
Size	Project Name: KABINI	Rev: SA
Date: Monday, February 04, 2013	Sheet 29 of 102	



EAEG50 KB UMA

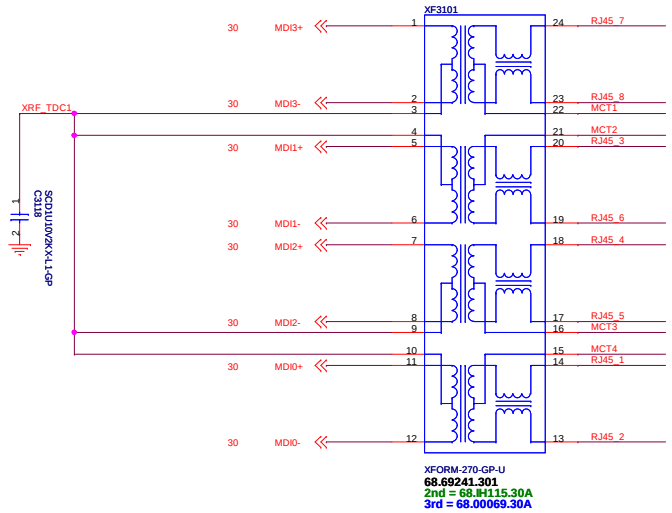
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

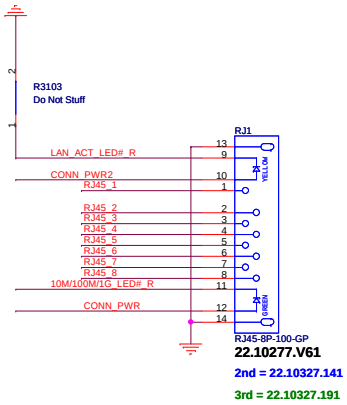
Title: RTL8411

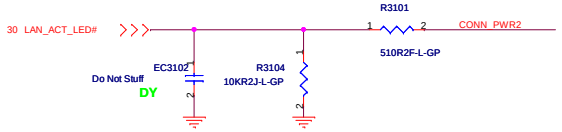
Size: | Project Name: KABINI | Rev: SA

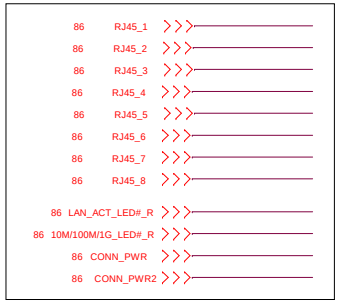
Date: Monday, February 04, 2013 | Sheet 30 of 102

SSID = LAN



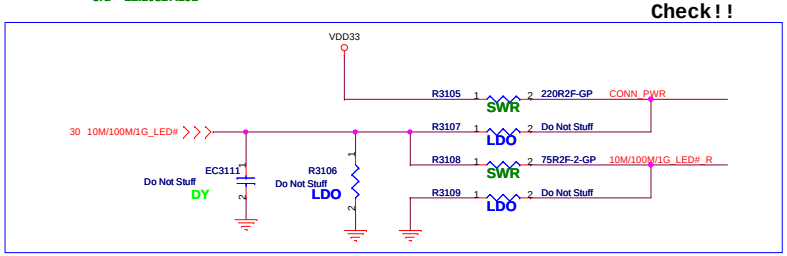


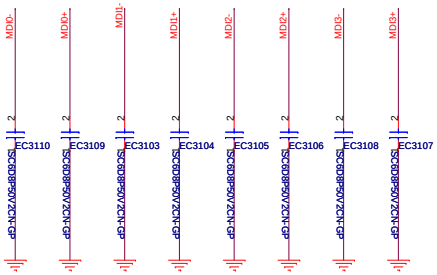


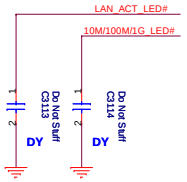


For AFTE

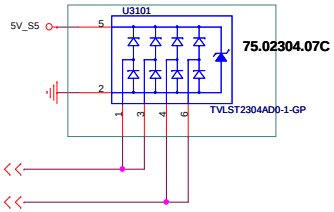
Check!!

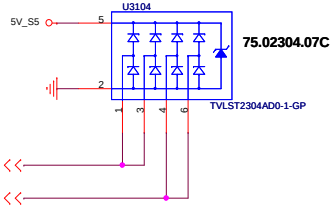


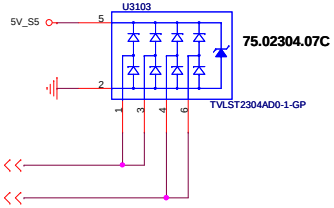


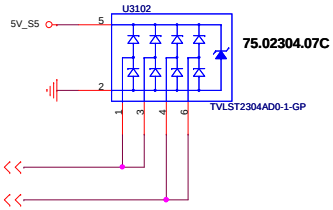


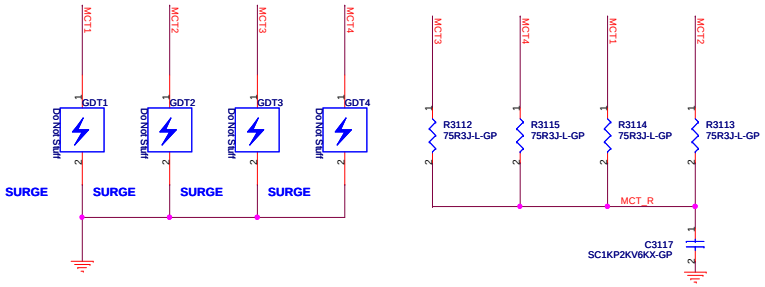
PD 1/17 soucer request to change PN for lock











EAEG50 KB UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	LAN CONNECTOR	
Size	Project Name: KABINI	Rev: SA
Date: Monday, February 04, 2013	Sheet 31 of 102	

EAEG50 KB UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

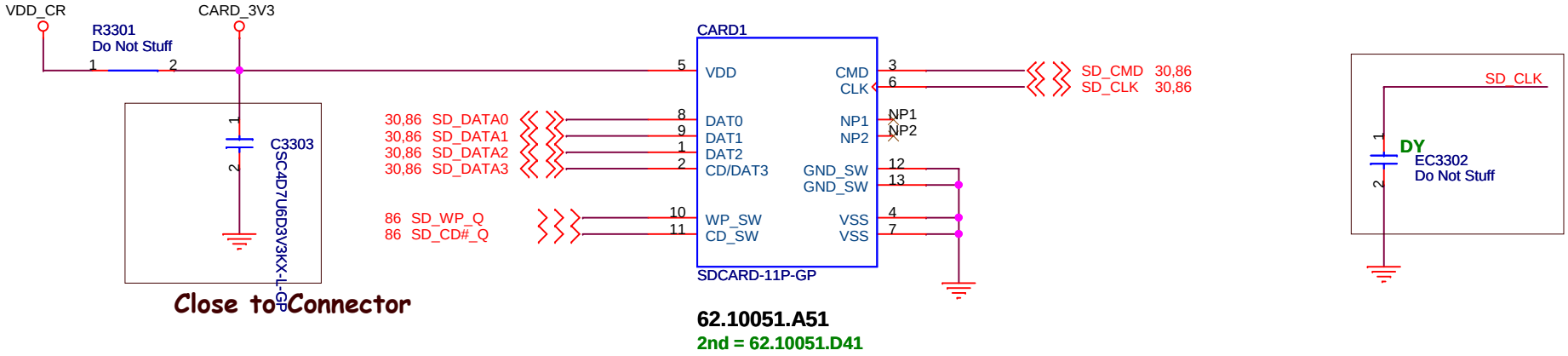
Title: **Card Reader IC**

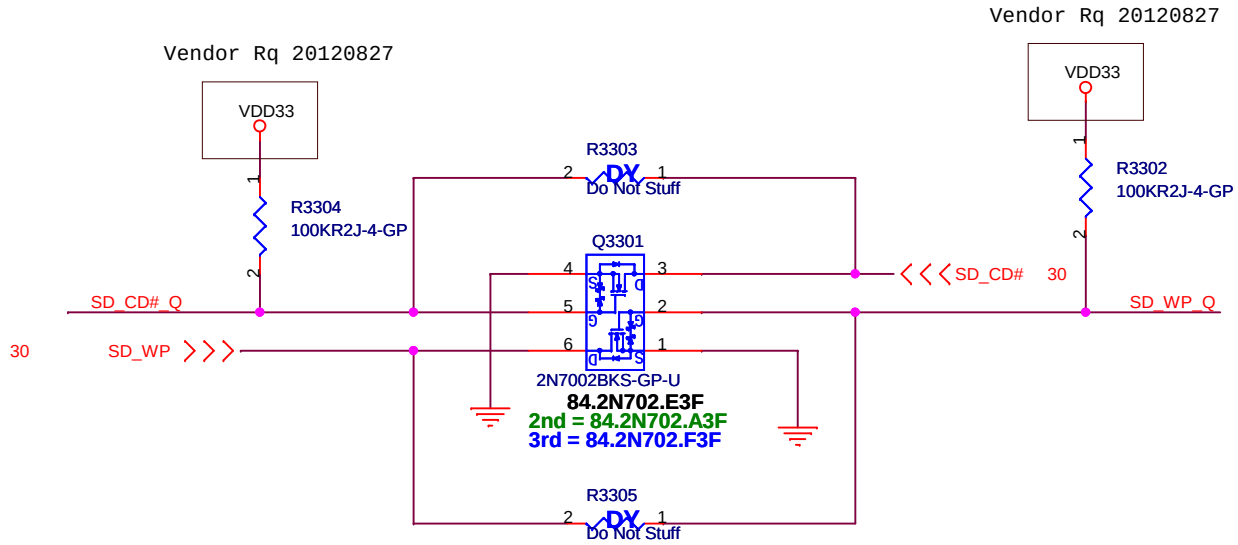
Size | Project Name: **KABINI** | Rev: **SA**

Date: Friday, September 07, 2012 | Sheet 32 of 102

SSID = SDIO

SD//MS Card Reader





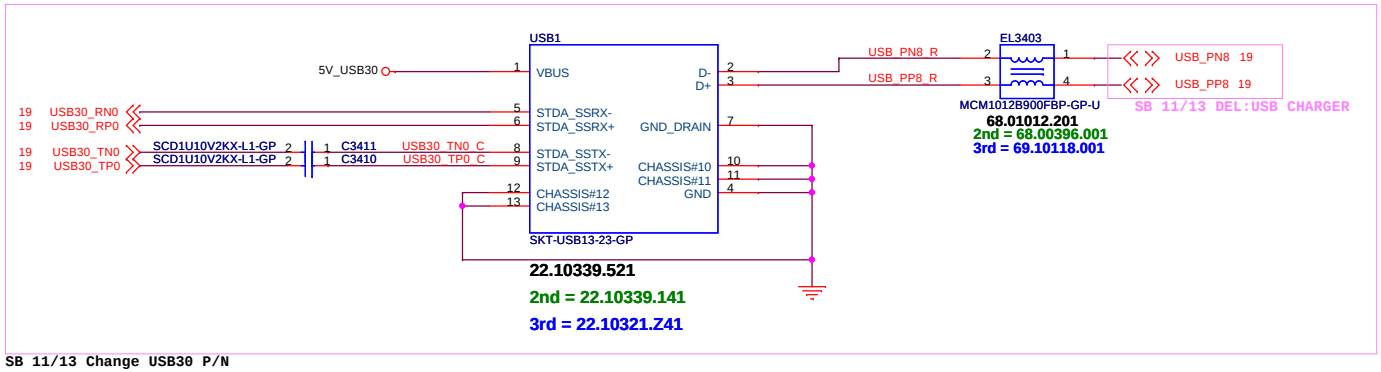
For CR conn normal colse type

EAEG50 KB UMA

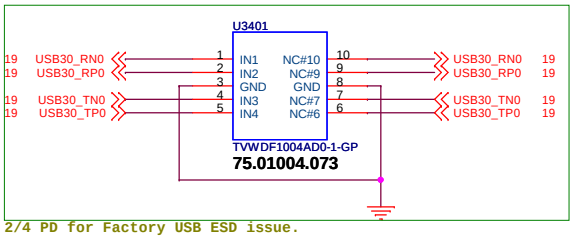
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CARD Reader CONN	
Size	Project Name: KABINI	Rev: SA
Date: Monday, February 04, 2013	Sheet 33 of 102	

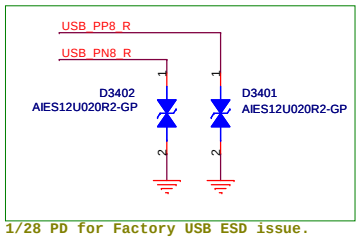
USB 2.0 CONTACT PIN		USB 3.0 CONTACT PIN	
PIN NO.	SIGNAL NAME	PIN NO.	SIGNAL NAME
1	VBUS	5	StdA_SSRX-
2	D-	6	StdA_SSRX+
3	D+	7	GND_DRAIN
4	GND	8	StdA_SSTX-
		9	StdA_SSTX+



SB 11/13 Change USB30 P/N



2/4 PD for Factory USB ESD issue.



1/28 PD for Factory USB ESD issue.

EAEG50 KB UMA

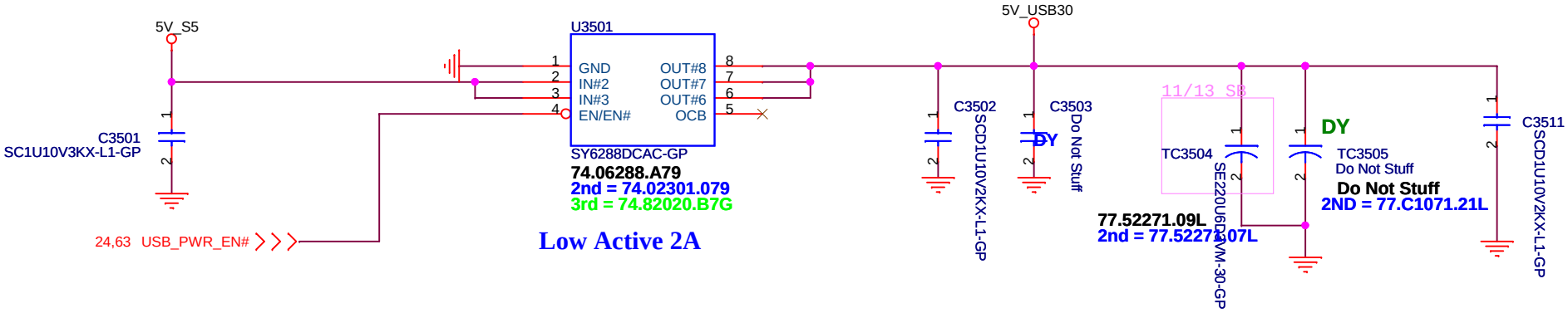
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB 3.0 Port

Size | Project Name: KABINI | Rev: SA

Date: Monday, February 04, 2013 | Sheet 34 of 102

SB 11/13 Change USB30

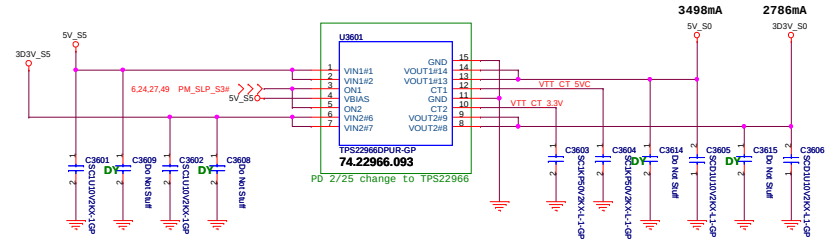


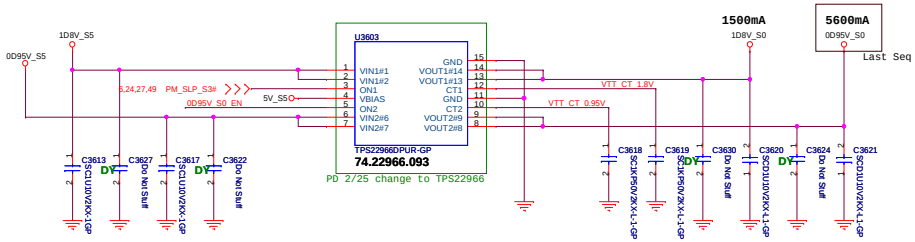
SC 12/20 EA50: Mount TC3504 , DY TC3505

EAEG50 KB UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	USB_Charger	
Size	Project Name: KABINI	Rev: SA
Date: Monday, February 04, 2013	Sheet 35 of 102	

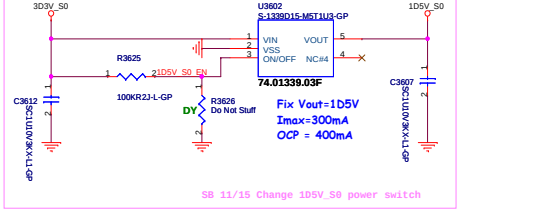
Power Sequence

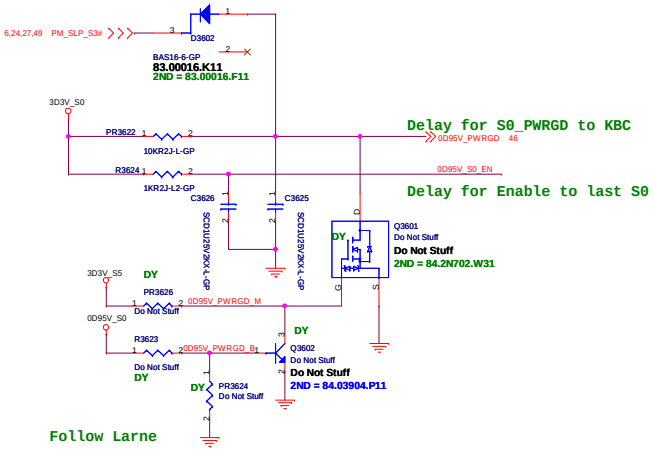


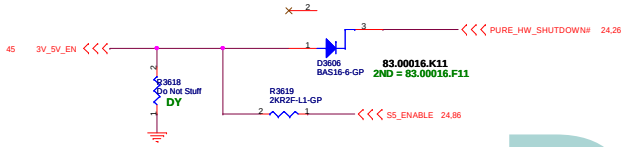


LDO for 1D5V_S0 (SB 11/15)

100mA for Audio chipset







EAEG50 KB UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable

Size | Project Name: KABINI | Rev: SA

Date: Monday, February 25, 2013 | Sheet 36 of 102

EAEG50 KB UMA

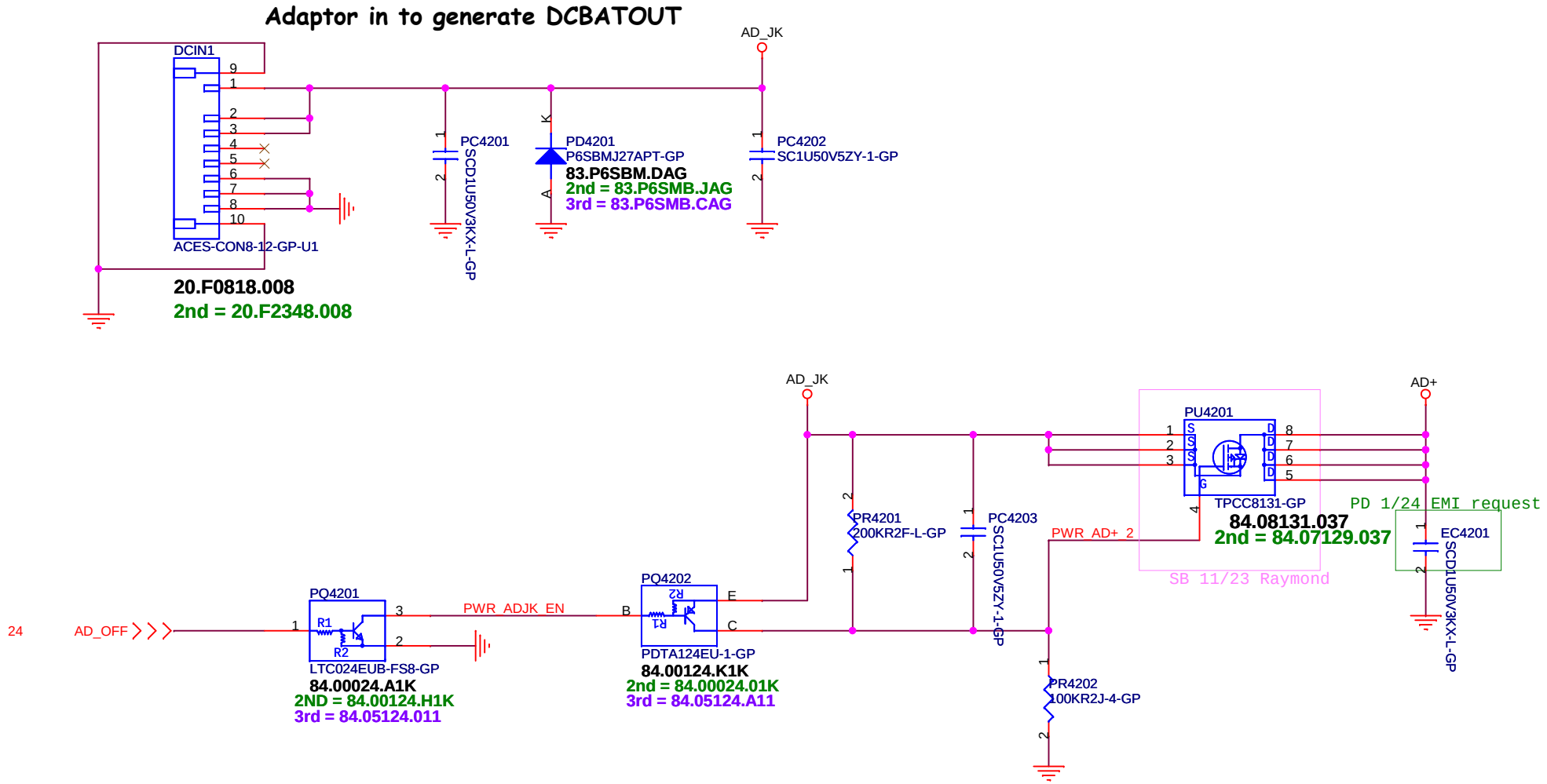
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size	Project Name	Rev
	KABINI	SA

Date: Friday, September 07, 2012 Sheet 41 of 102

ANNIE solution



EAEG50 KB UMA

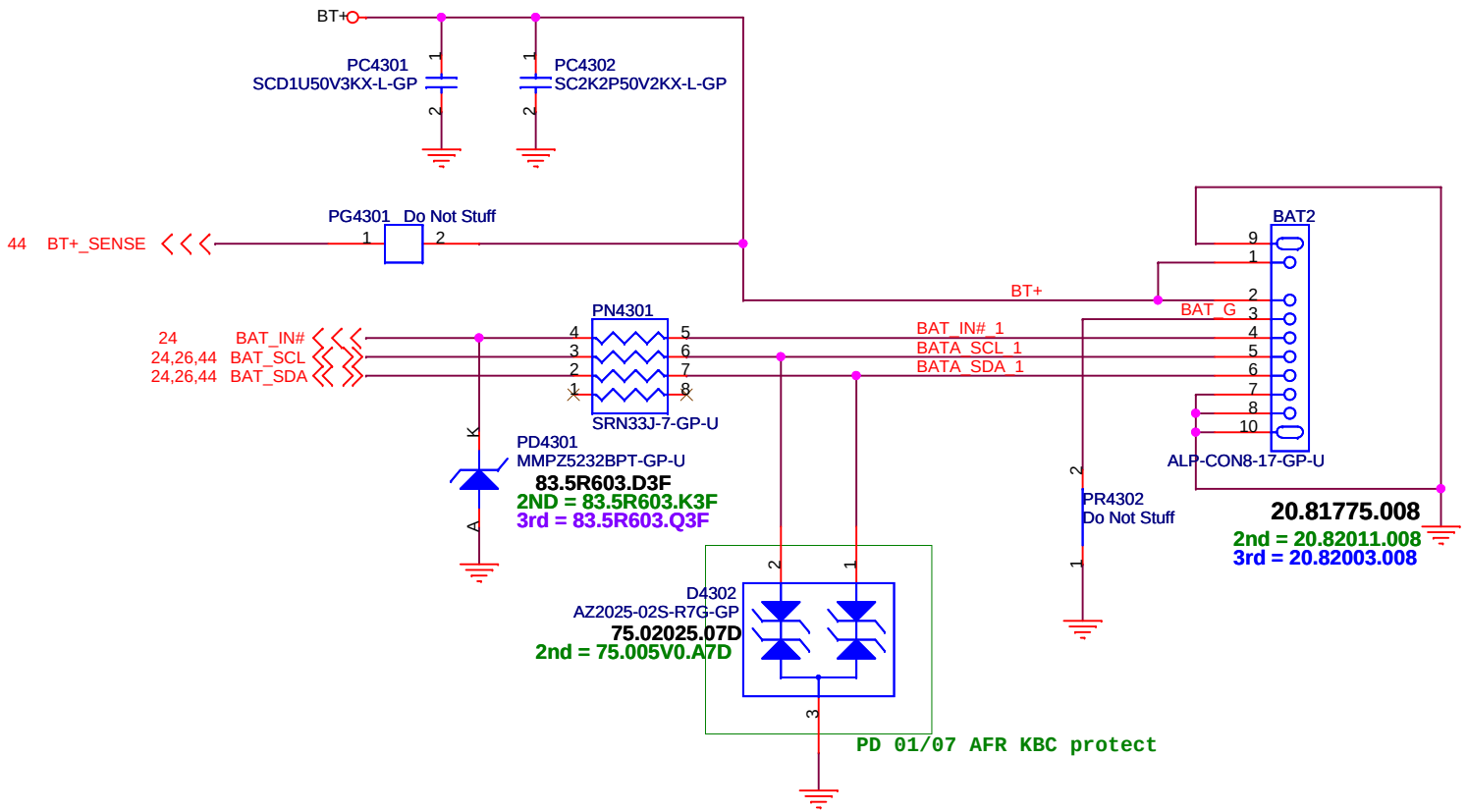
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	DCIN JACK	
Size	Project Name: KABINI	Rev: SA
Date: Tuesday, February 19, 2013	Sheet 42 of 102	

BATTERY CONNECTOR

86 BATA_SDA_1
86 BATA_SCL_1
86 BAT_IN#_1
86 BAT_G

For AFTE



EAEG50 KB UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

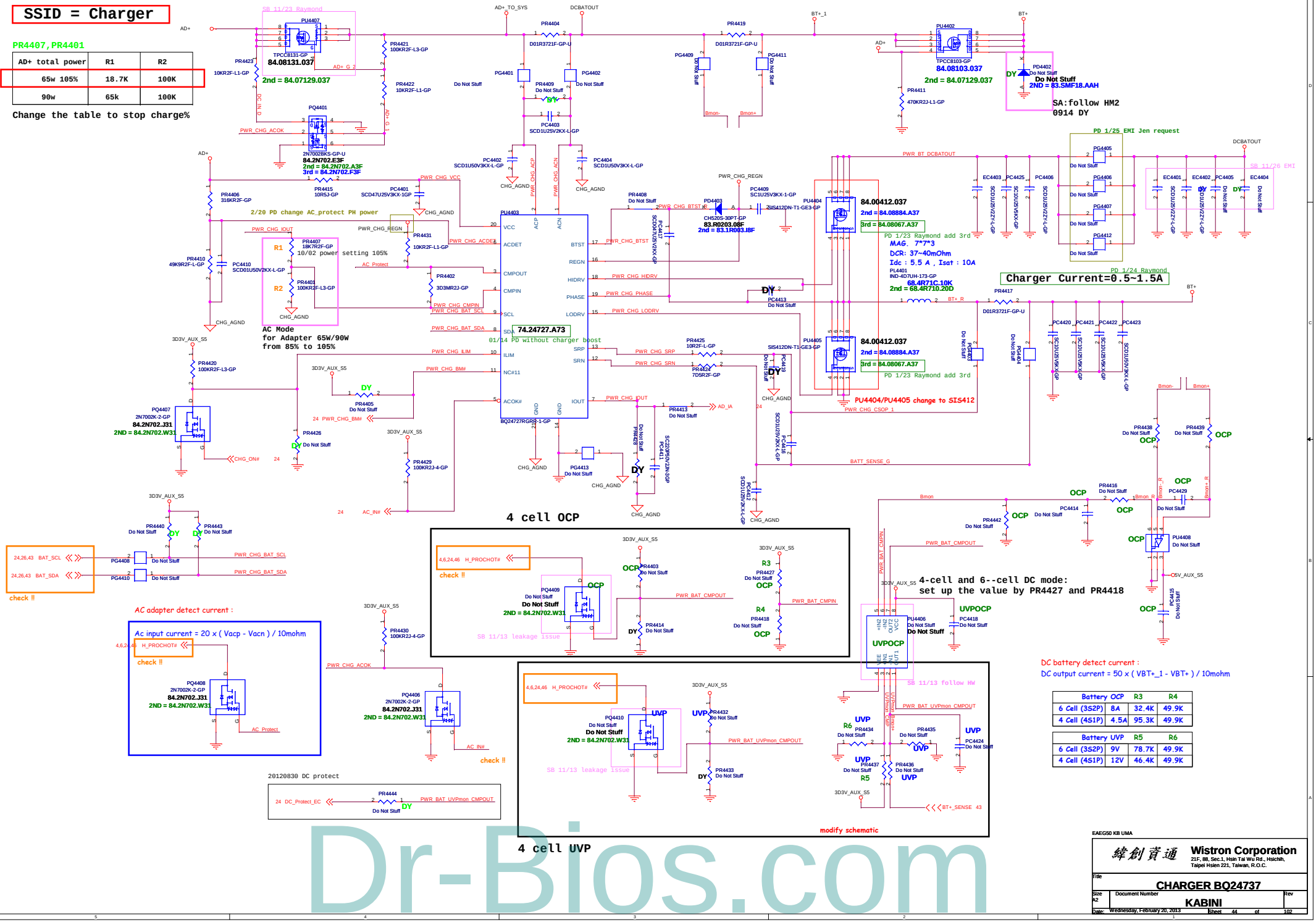
Title	BATT CONN	
Size	Project Name: KABINI	Rev: SA
Date: Wednesday, February 20, 2013	Sheet 43 of 102	

SSID = Charger

PR4407,PR4401

AD+ total power	R1	R2
65w 105%	18.7K	100K
90w	65k	100K

Change the table to stop charge%



Battery OCP	R3	R4
6 Cell (3S2P)	8A	32.4K	49.9K
4 Cell (4S1P)	4.5A	95.3K	49.9K

Battery UVP	R5	R6
6 Cell (3S2P)	9V	78.7K	49.9K
4 Cell (4S1P)	12V	46.4K	49.9K

EAEG50 KB UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER BQ24737

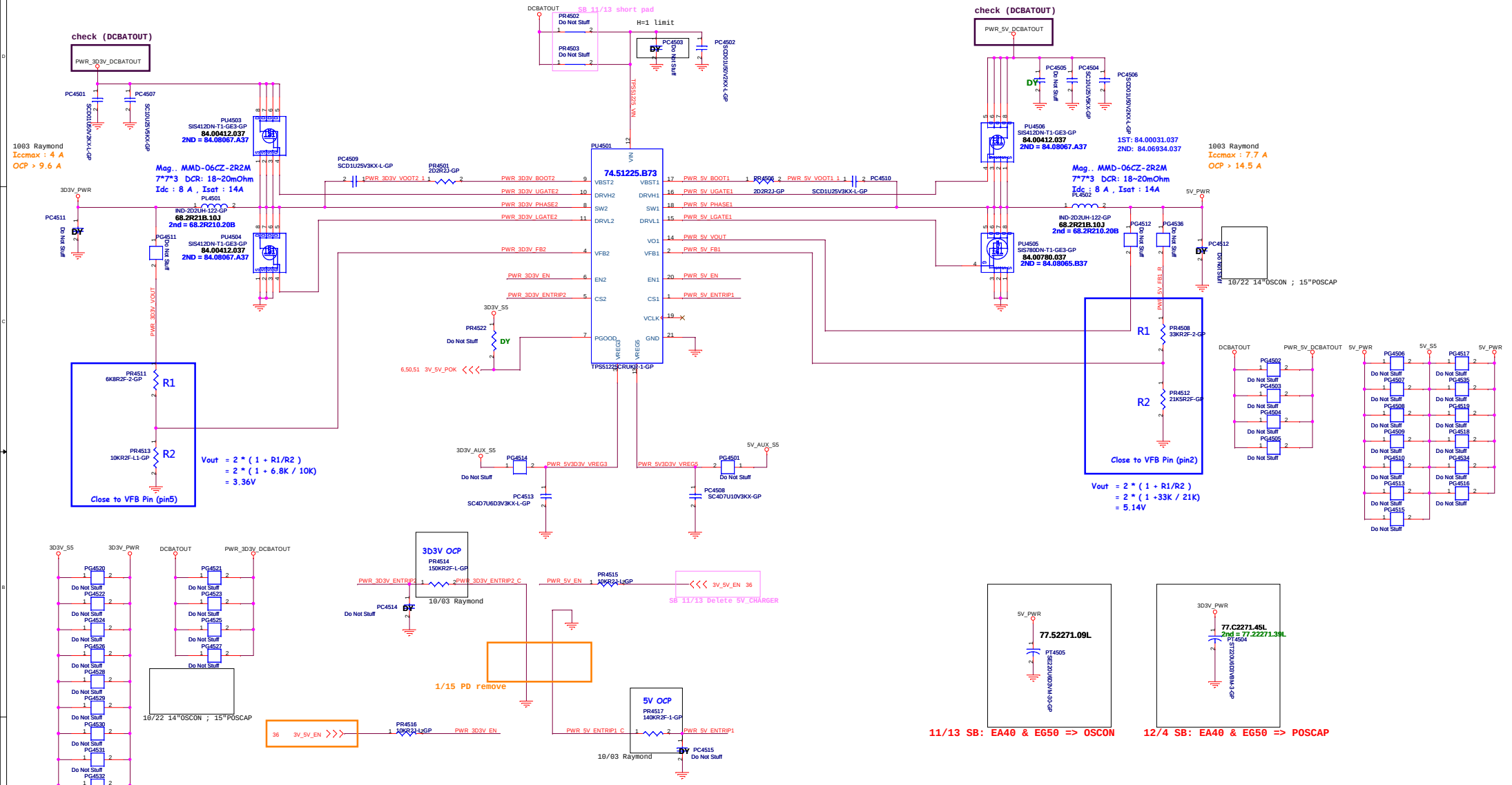
Size: A2 | Document Number: KABINI | Rev:

Date: Wednesday, February 20, 2013 | Sheet 44 of 102

SSID = PWR.Plane.Regulator_3p3v5v

Cut off itself

check (UVP)



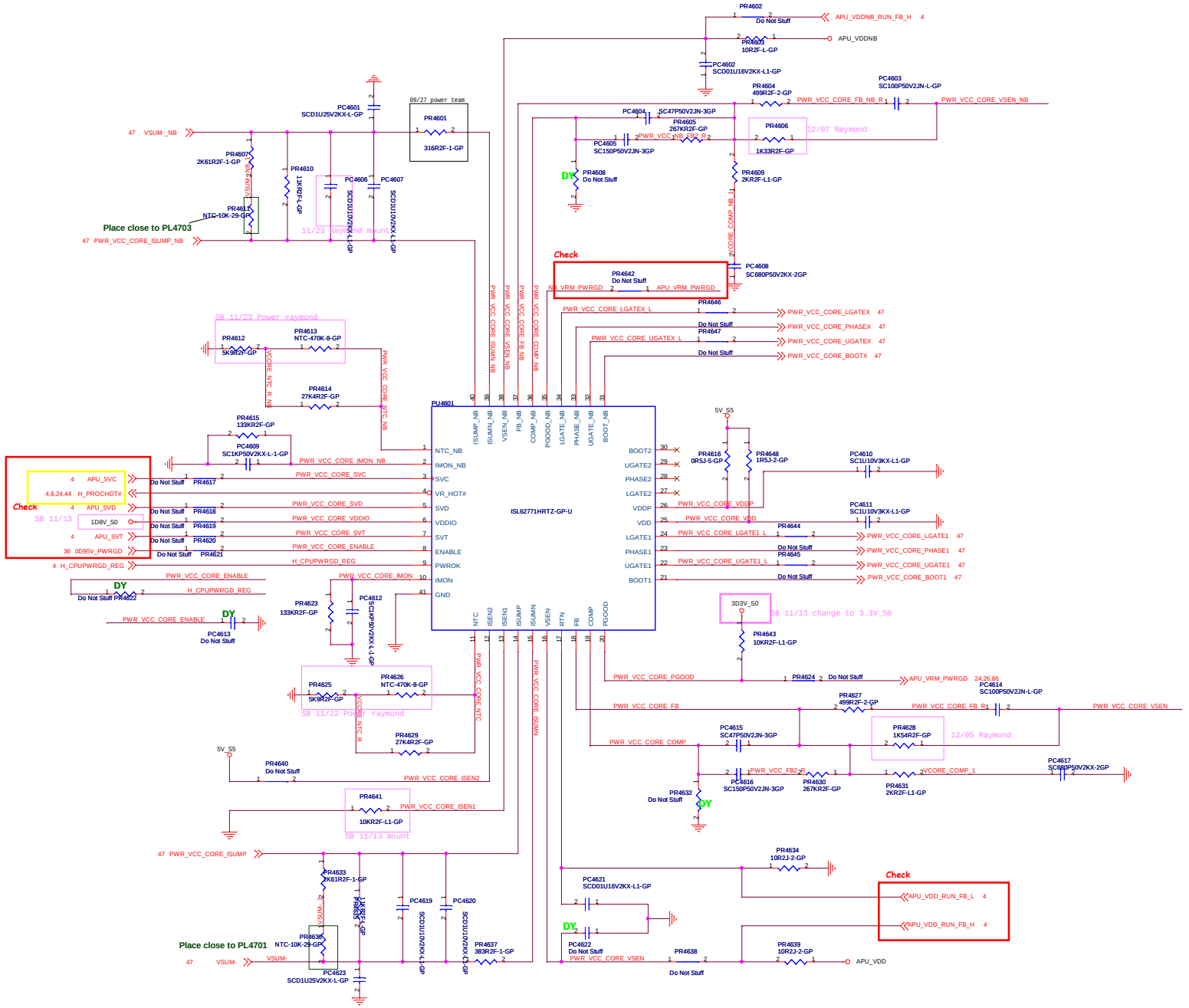
EAEG50 KB UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51225 5V/3D3V

Size: A2 | Document Number: KABINI | Rev:

Date: Monday, February 04, 2013 | Sheet 45 of 102



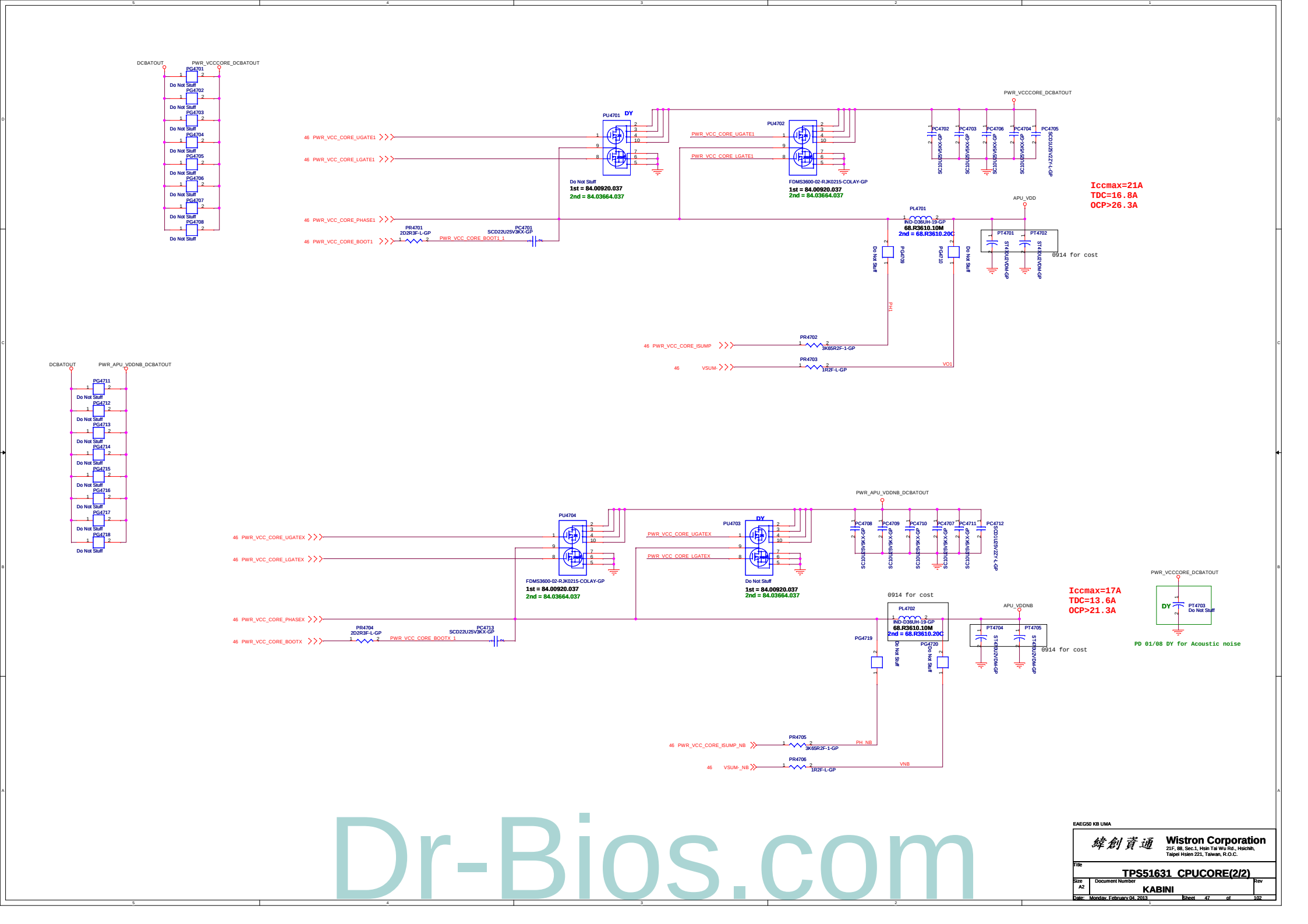
EAEG50 KB UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51631_CPUCORE(1/2)

Size: A2 | Document Number: KABINI | Rev:

Date: Monday, February 04, 2013 | Sheet 46 of 102



EAEG50 KB UMA

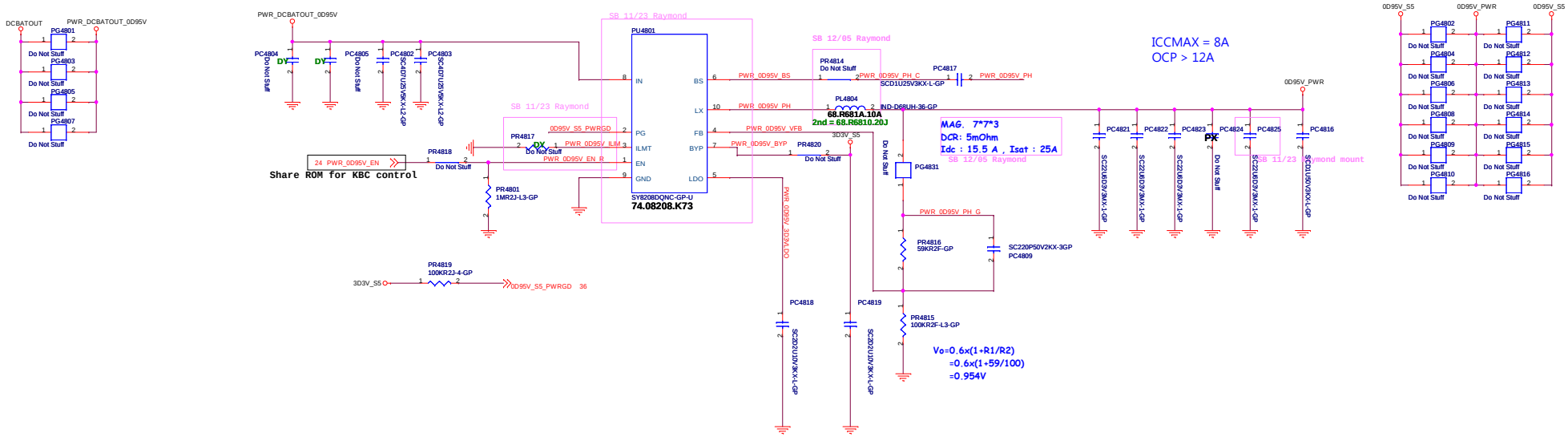
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51631_CPUCORE(2/2)

Size	Document Number	Rev
A2	KABINI	

Date: Monday, February 04, 2013 Sheet 47 of 102

SY8208D for 0D95V



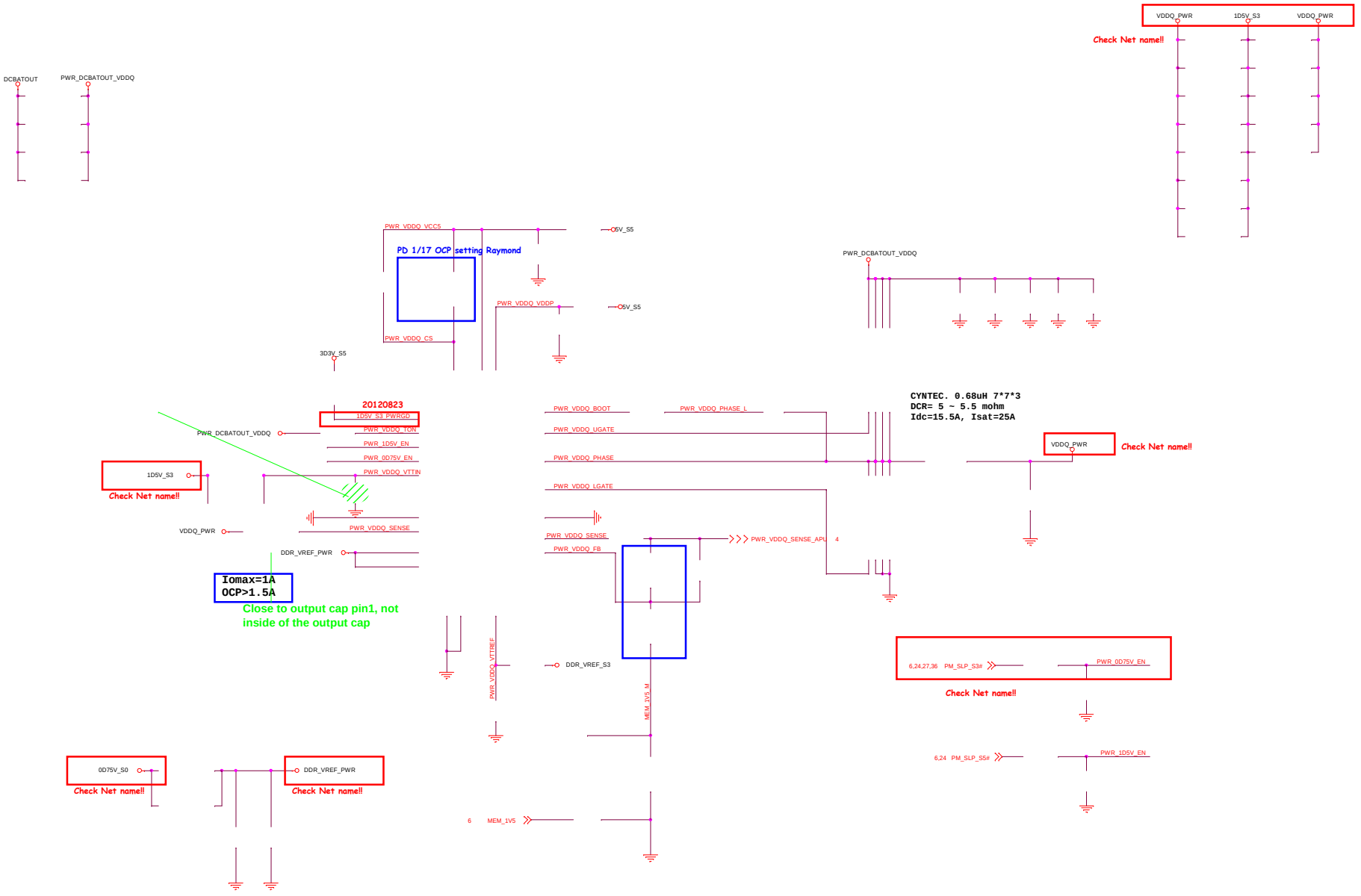
EAEG50 KB UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC to DC 0D95V(RT8237C)

Size: A2 | Document Number: KABINI | Rev:

Date: Tuesday, February 19, 2013 | Sheet 48 of 102



EAEG50 KB UMA

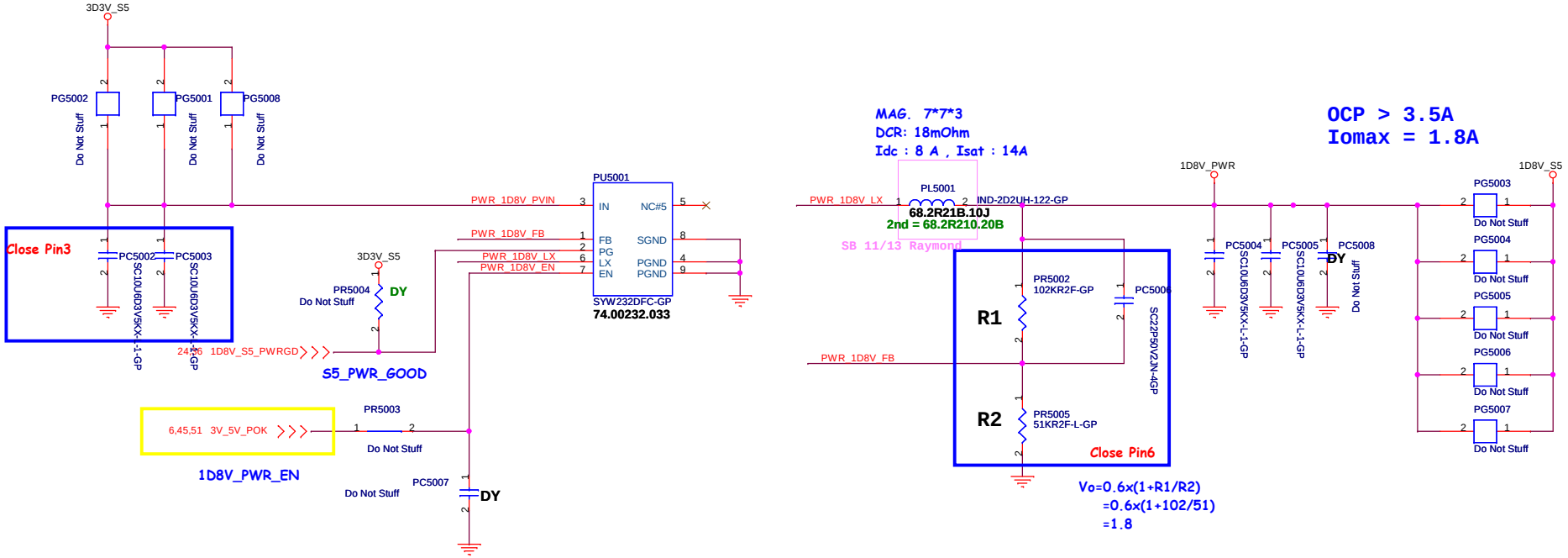
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8207

Size: A2 | Document Number: KABINI | Rev:

Date: Monday, February 04, 2013 | Sheet 49 of 102

SSID = PWR.Plane.Regulator_1p8v



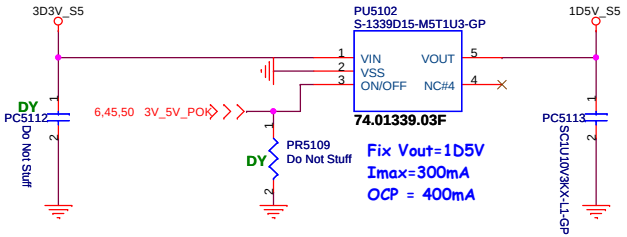
EAEG50 KB UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

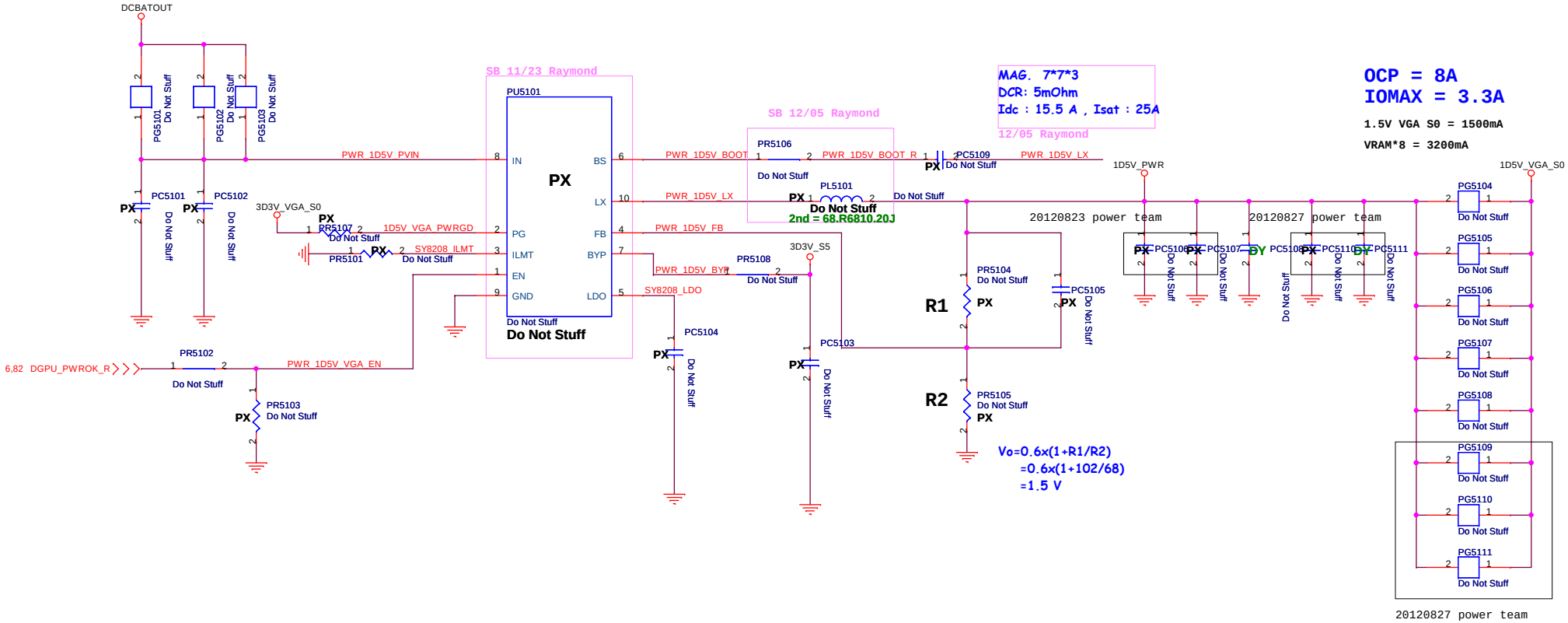
Title	1D8V_S0 SYW232	
Size A3	Document Number KABINI	Rev
Date: Monday, February 04, 2013	Sheet 50 of 102	

LDO for 1D5V_S5 (SB 11/13)

1.5V S0 = 100mA(VDDIO_AZ) + 100mA(Audio) + 600mA(Minicard DY) = 200mA



SY8208D for 1D5V_VGA_S0 (SB 11/13)

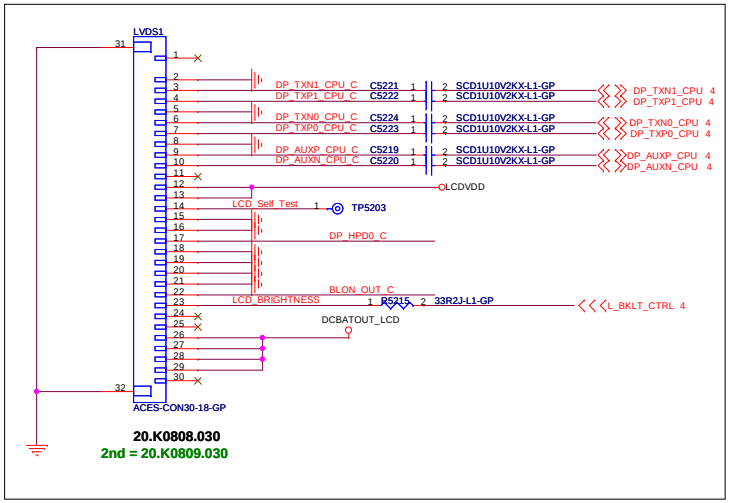


EAEG50 KB UMA

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	1D5V_S5 SY8208D	
Size A3	Document Number KABINI	Rev
Date: Tuesday, February 19, 2013	Sheet 51 of 102	

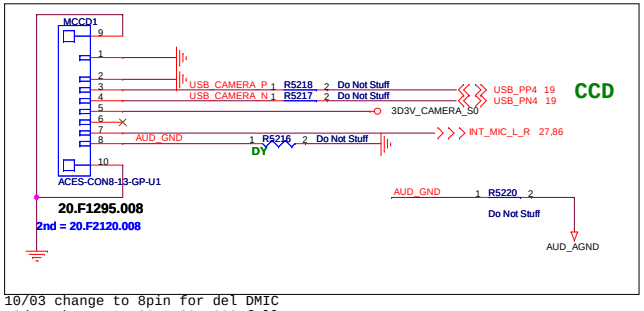
SSID = VIDEO

eDP Conn.



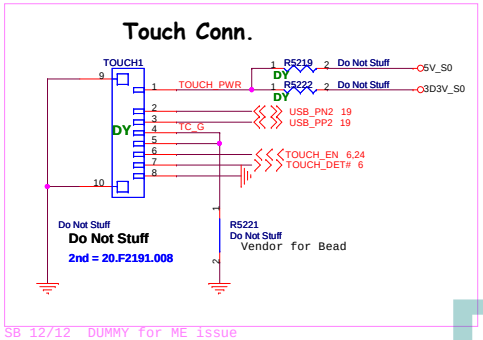
10/04 change to 20.K0808.030 for ME request

Camera+MIC Conn.



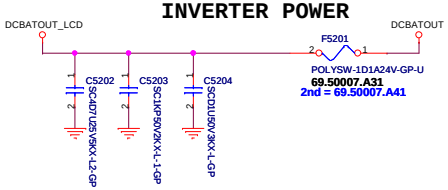
10/03 change to 8pin for del DMIC
10/15 change to 20.F1295.008 follow HW

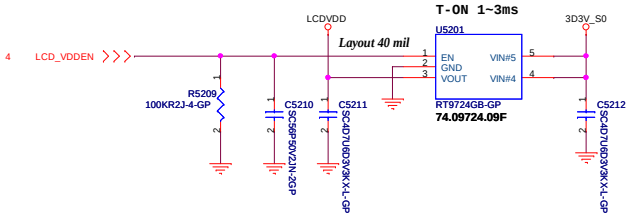
Touch Conn.

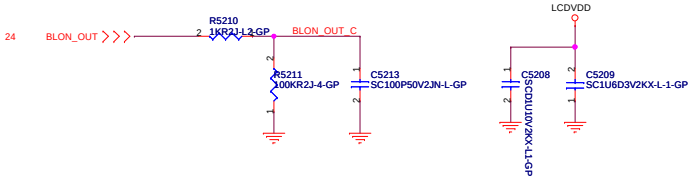


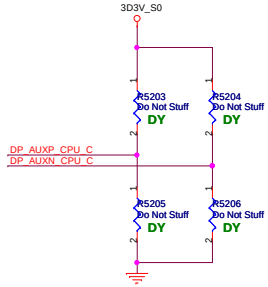
SB 12/12 DUMMY for ME issue
SC NO support

INVERTER POWER

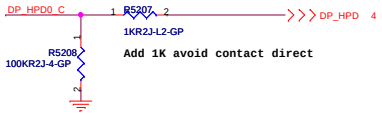




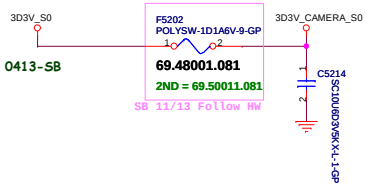


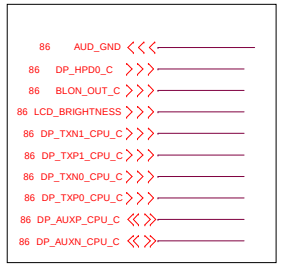


EDP HPD High active



Camera Power

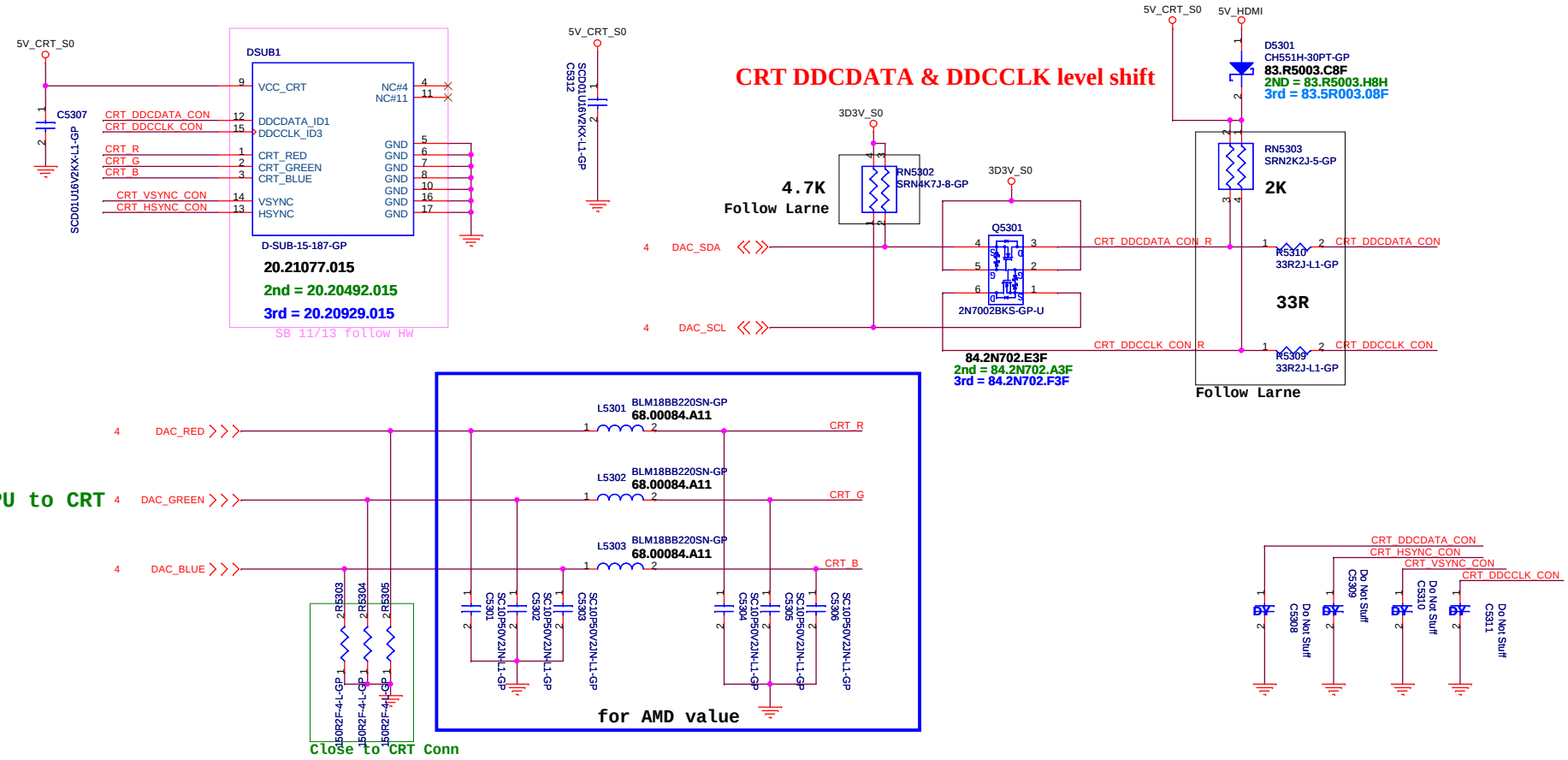




For AFTE

EAEG50 KB UMA

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	LCD Connector	
Size	Project Name: KABINI	Rev: SA
Date: Monday, February 25, 2013	Sheet 52 of 102	



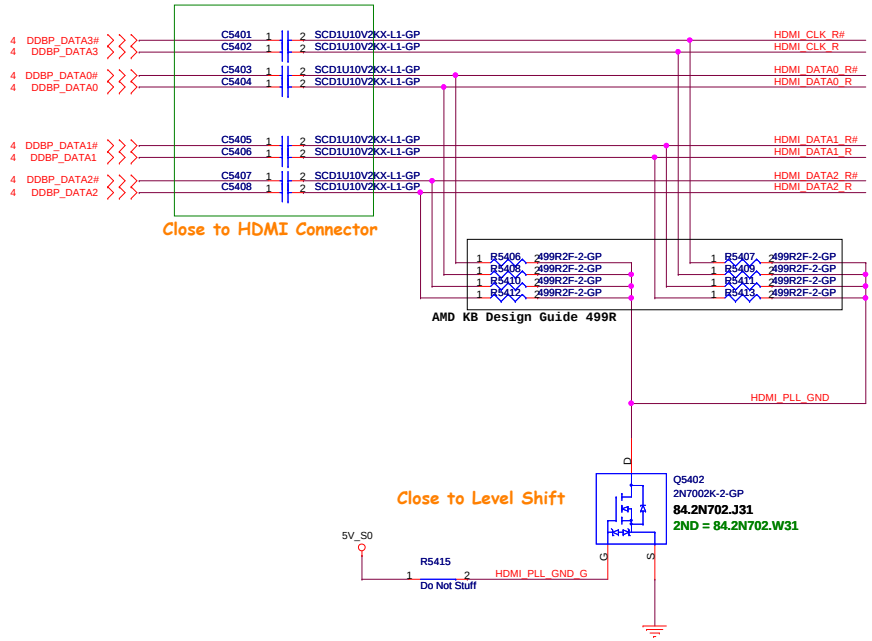
EAEG50 KB UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

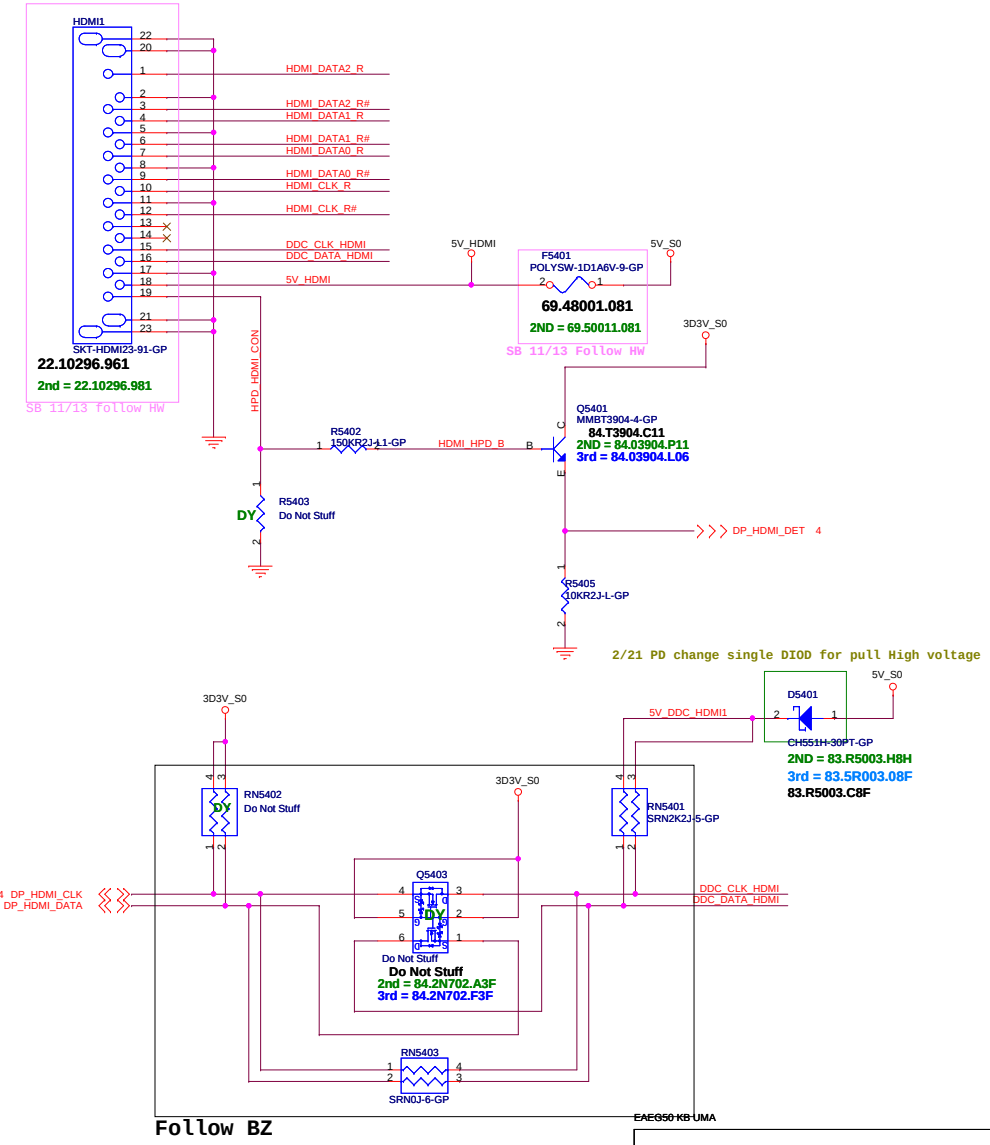
Title	CRT Board Connector	
Size	Project Name: KABINI	Rev: SA
Date: Monday, February 04, 2013	Sheet 53 of 102	

SSID = VIDEO

HDMI Level Shifter & CONNECTOR



HDMI CONN



緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: HDMI Level Shifter/Connector		
Size	Project Name: KABINI	Rev: SA
Date: Thursday, February 21, 2013	Sheet 54 of 102	

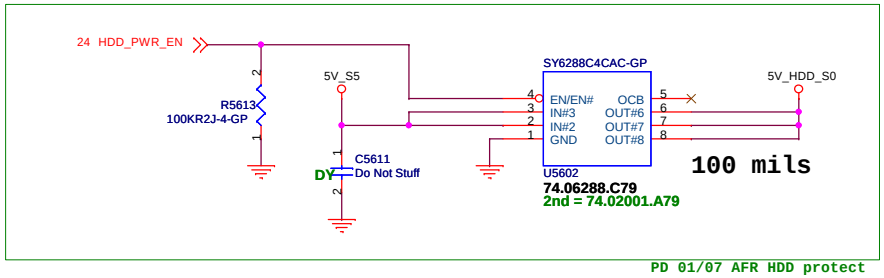
EAEG50 KB UMA

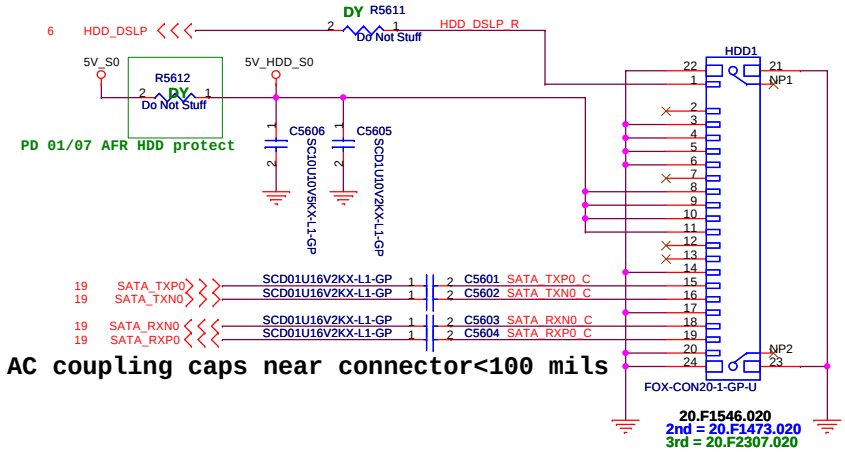
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	**Reserved**	
Size	Project Name **KABINI**	Rev **SA**
Date: Friday, September 07, 2012	Sheet 55 of 102	

SSID = SATA

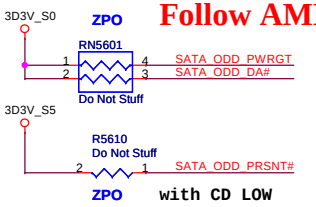
SATA HDD Connector

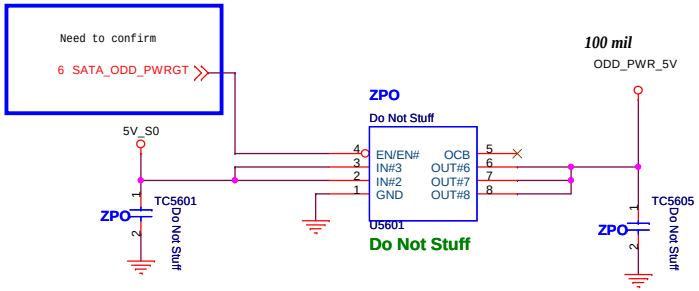


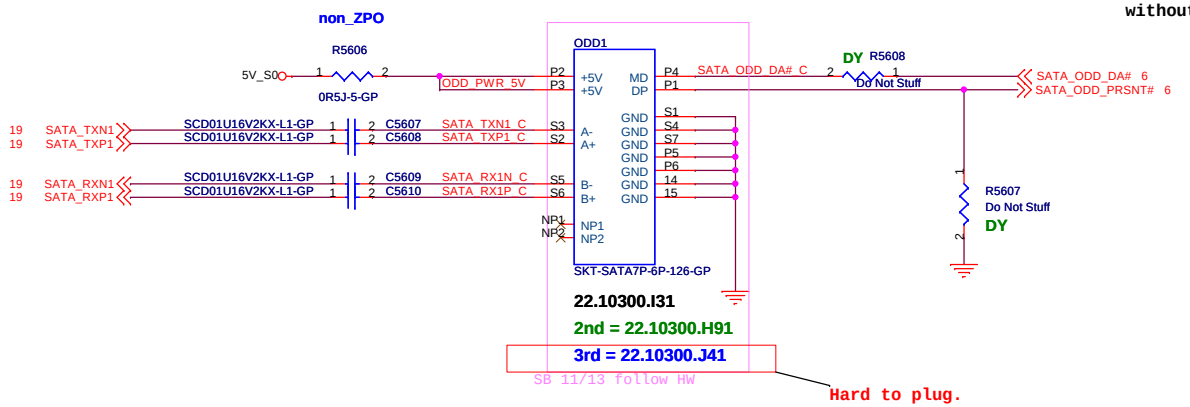


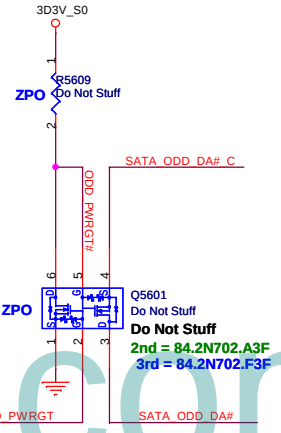
ODD Connector

SATA Zero Power ODD
Follow AMD Larne









Current limit Active High MIN =>2.01A

EAEG50 KB UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
HDD/ODD		
Size	Project Name	Rev
	KABINI	SA
Date: Monday, February 04, 2013	Sheet 56 of 102	

EAEG50 KB UMA

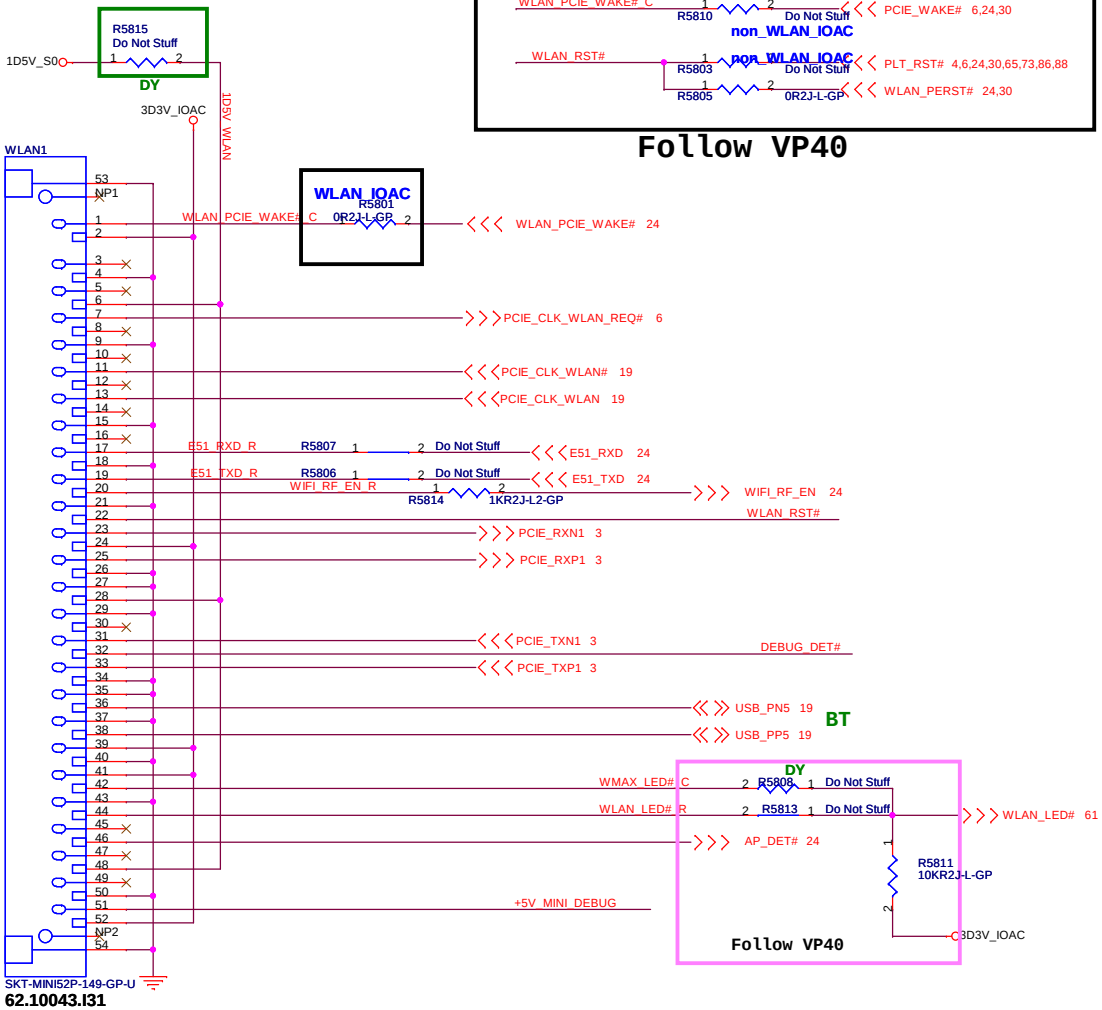
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

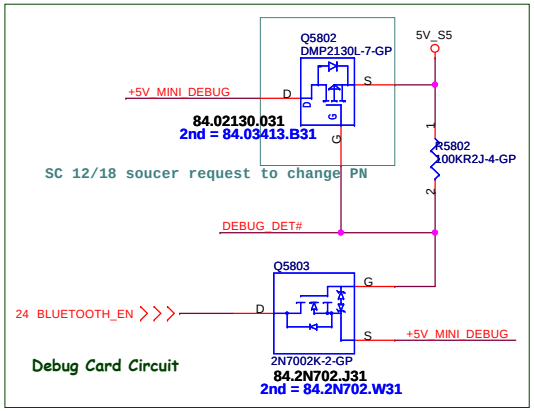
Title	**Reserved**		
Size	Project Name **KABINI**		Rev **SA**
Date: Friday, September 07, 2012		Sheet 57 of 102	

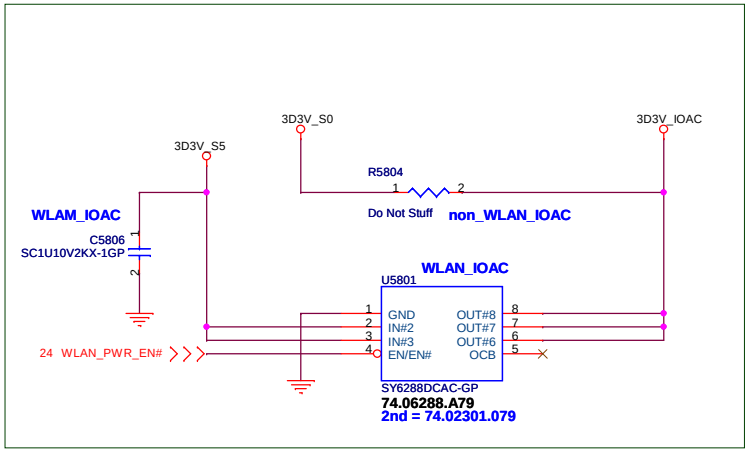
SSID = Wireless

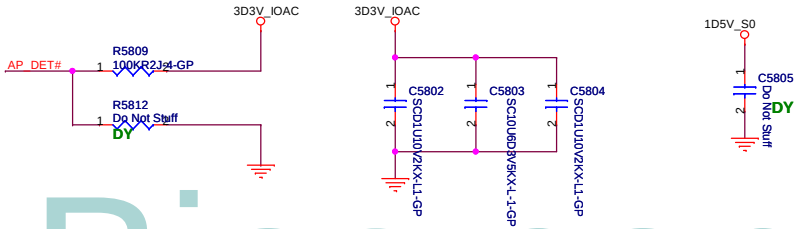
Mini Card Connector(802.11a/b/g/n)

10/15 follow EA40-HW









EAEG50 KB UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	MINICARD(WLAN)	
Size	Project Name: KABINI	Rev: SA
Date: Tuesday, February 19, 2013	Sheet 58 of 102	

SSID = Wireless

Mini Card Connector(WWAN)

EAEG50 KB UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	WWAN CONN	
Size	Project Name: KABINI	Rev: SA
Date: Friday, September 07, 2012	Sheet 59 of 102	

SSID = mSATA

Mini Card Connector(mSATA)

EAEG50 KB UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	mSATA Connector	
Size	Project Name: KABINI	Rev: SA
Date: Friday, September 07, 2012	Sheet 60 of 102	

SSID = User.Interface

System LED (BLU/ORG)

PD 1/24 LED tuning

STDBY_LED# Q — R6101 1K2R2F-1-GP — STDBY_LED# R

FRONT_PWRLED# Q — R6102 390R2F-2GP — FRONT_PWRLED# R

PLED1 LED-BO-22-GP → 5V_S5

11/21 EG50 LED fine tune

83.00326.M70

2nd = 83.01212.A70

Battery LED (BLU/ORG)

PD 1/24 LED tuning

CHARGE_LED# Q — R6103 1K2R2F-1-GP — CHARGE_LED# R

DC_BATFULL# Q — R6104 330R2F-GP — DC_BATFULL# R

CHLED1 LED-BO-22-GP → 5V_AUX_S5

11/21 EG50 LED fine tune

83.00326.M70

2nd = 83.01212.A70

SATA HDD LED (BLU)

SATA_LED# 1 — R6105 680R2F-GP — MEDIA_LED# R

HLED1 ZENER LED-B-162-GP → 5V_S0

11/21 EG50 LED fine tune

83.00320.B70

2nd = 83.01211.070

RF LED (ORG)

WLAN_LED# — R6106 560R2F-GP — WLAN_LED# EA

RFLED1 LED-O-36-GP-U → 3D3V_IOAC

11/21 EG50 LED fine tune

83.00270.D70

EA40 Power LED (BLU)

FRONT_PWRLED# Q — R6107 Do Not Stuff — FRONT_PWRLED# EA

PWLED1 → 5V_S5

14" R6107 / 14" Do Not Stuff

SB 11/19 for LED turning

Do Not Stuff

2nd = 83.19117.070

PWRLED

24 PWRLED — Q6101 LTC043ZUB-FS8-GP — FRONT_PWRLED# Q

84.00043.011

2nd = 84.00143.D1K

STDBY_LED

24 STDBY_LED — Q6103 LTC043ZUB-FS8-GP — STDBY_LED# Q

84.00043.011

2nd = 84.00143.D1K

DC_BATFULL

24 DC_BATFULL — Q6104 LTC043ZUB-FS8-GP — DC_BATFULL# Q

84.00043.011

2nd = 84.00143.D1K

SATA_LED

3D3V_S0 — Q6105 LTC043ZUB-FS8-GP — SATA_LED# 1 — SATA_LED# 19

84.00043.011

2nd = 84.00143.D1K

CHARGE_LED

24 CHARGE_LED — Q6106 LTC043ZUB-FS8-GP — CHARGE_LED# Q

84.00043.011

2nd = 84.00143.D1K

WLAN_LED

From module

WLAN_LED# 58 → Q6107 2N7002K-2-GP

84.2N702.J31

2ND = 84.2N702.W31

WLAN_TEST_LED 24

for factory test

5V_S5 — SB 11/26 EMI Close PBD1 — EC6101 SCD1U10W2KX-1-GP

PBD1 PTWO-CON6-13-GP

15" — KBC_PWRBTN# — FRONT_PWRLED# Q

20.K0397.006

2nd = 20.K0610.006

PW1 Do Not Stuff

14" Do Not Stuff

2nd = 62.40089.441

For EA-50

KBC_PWRBTN# → KBC_PWRBTN# 24,27,86,90

FRONT_PWRLED#_Q 90

For AFTE

EAEG50 KB UMA

緯創資通 Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: LED Bard/Power Button

Size | Project Name: KABINI | Rev: SA

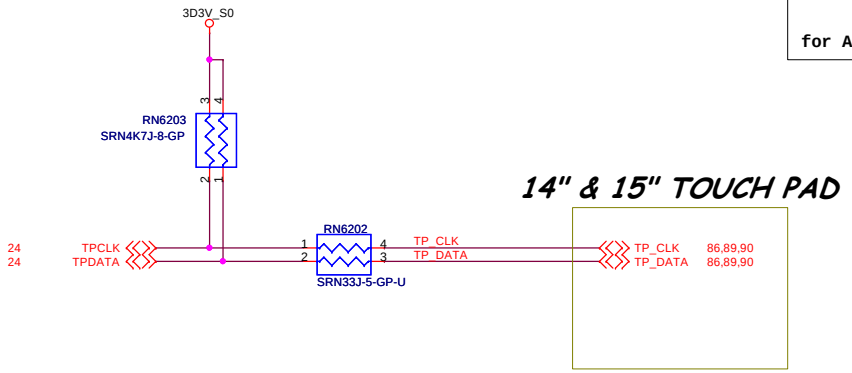
Date: Monday, February 04, 2013 | Sheet 61 of 102

SSID = KBC

Internal KeyBoard Connector

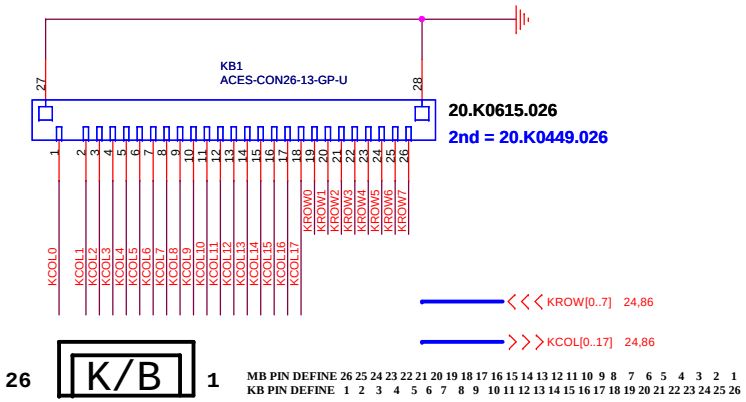
86,89,90 TP_DATA
86,89,90 TP_CLK
86,89,90 SWR
86,89,90 SWL

for AFTP



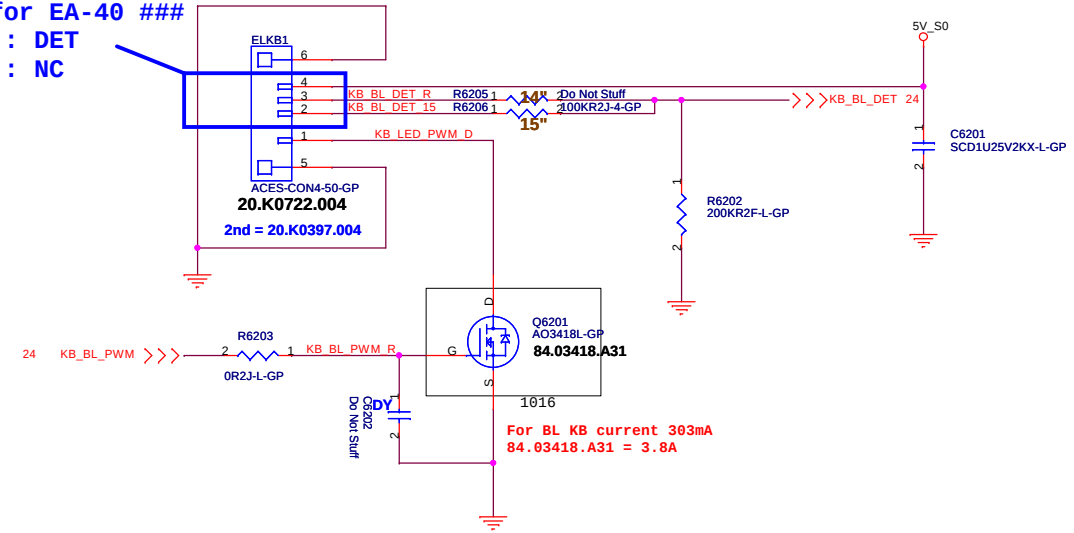
PD 1/14 Diffferent 14" & 15" TOUCH PAD reversion

14"& 15" use the same KB



for EA/EG-50
Pin3 : NC
Pin2 : DET

for EA-40
Pin3 : DET
Pin2 : NC

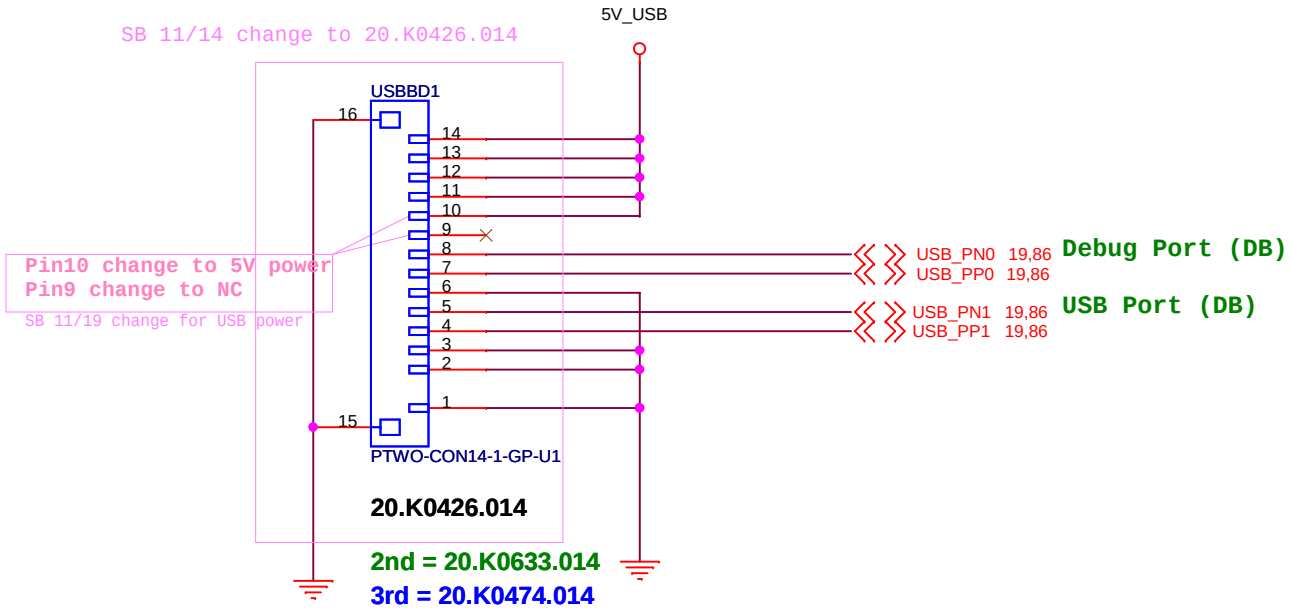


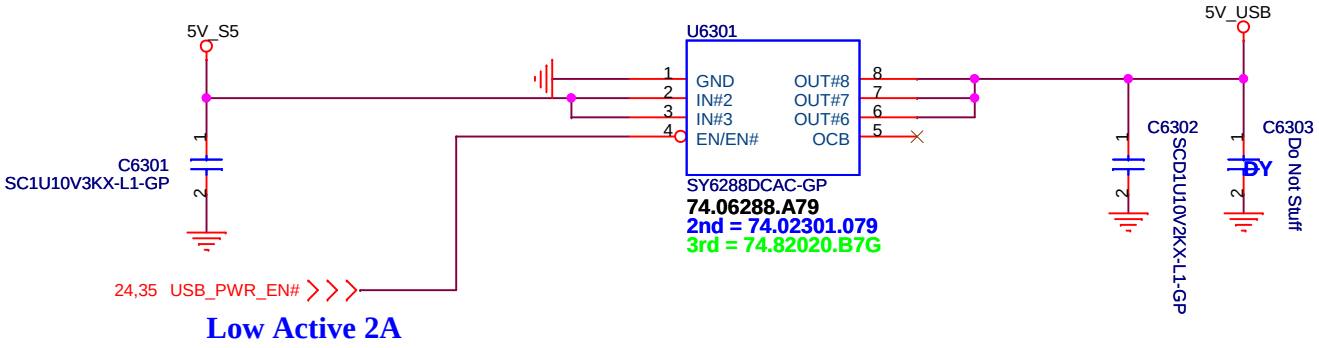
EAEG50 KB UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Key Board/Touch Pad	
Size	Project Name: KABINI	Rev: SA
Date: Tuesday, February 19, 2013	Sheet 62 of 102	

SB 11/14 change to 20.K0426.014

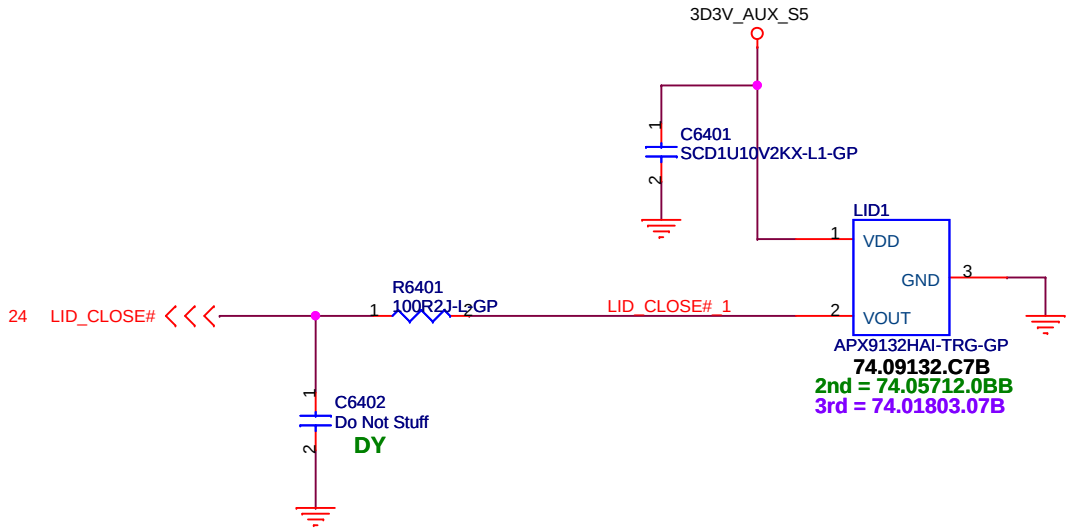




EAEG50 KB UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

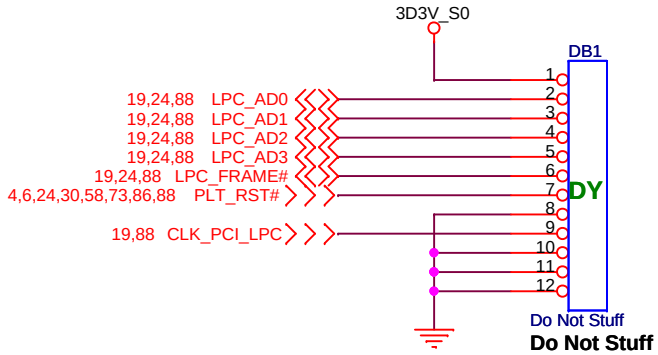
Title	IO Board Connector	
Size	Project Name: KABINI	Rev: SA
Date: Monday, February 04, 2013	Sheet 63 of 102	



EAEG50 KB UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Hall Sensor	
Size	Project Name: KABINI	Rev: SA
Date: Monday, February 04, 2013	Sheet 64 of 102	



EAEG50 KB UMA

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Dubug connector	
Size	Project Name: KABINI	Rev: SA
Date: Monday, February 04, 2013	Sheet 65 of 102	

(Blanking)

EAEG50 KB UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Reserved**		
Size	Project Name: **KABINI**	Rev: **SA**
Date: Friday, September 07, 2012	Sheet 66 of 102	

SSID = User.Interface

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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	G Sensor	
Size	Project Name: KABINI	Rev: SA
Date: Friday, September 07, 2012	Sheet 67 of 102	

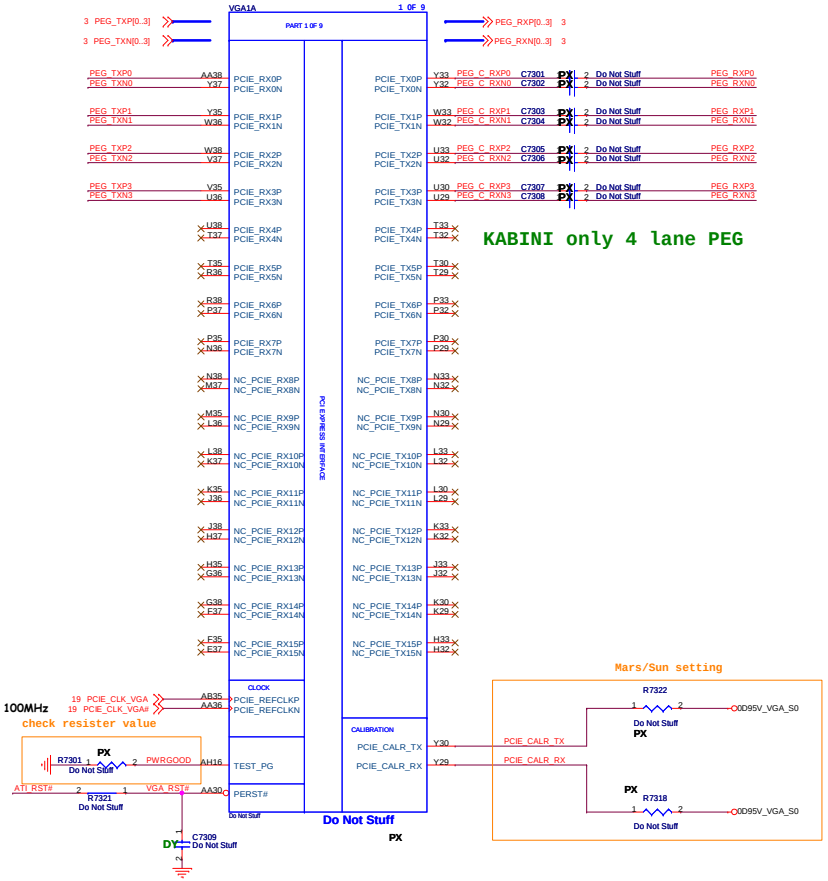
EAEG50 KB UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Thunderbolt (5/5)**

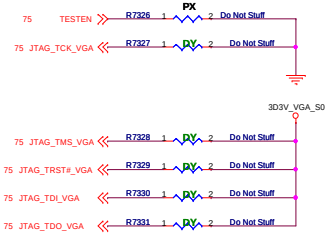
Size | Project Name: **KABINI** | Rev: **SA**

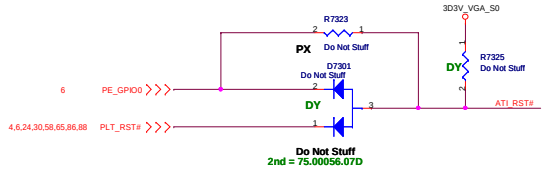
Date: Friday, September 07, 2012 | Sheet 72 of 102



JTAG SIGNAL OPTION

Signal	Normal mode	Debug mode	pilot run mode
TESTEN	"0"(PD)	"1"(PU)	"0"(PD)
JTAG_TRST#	"1"(PU)	"1"(PU)	NC
JTAG_TCK	"0"(PD)	"1"(PU)	NC
JTAG_TMS	"1"(PU)	"1"(PU)	NC





	PE_GPIO0
dGPU mode	H
IGPU	L
IGPU with BACO	H

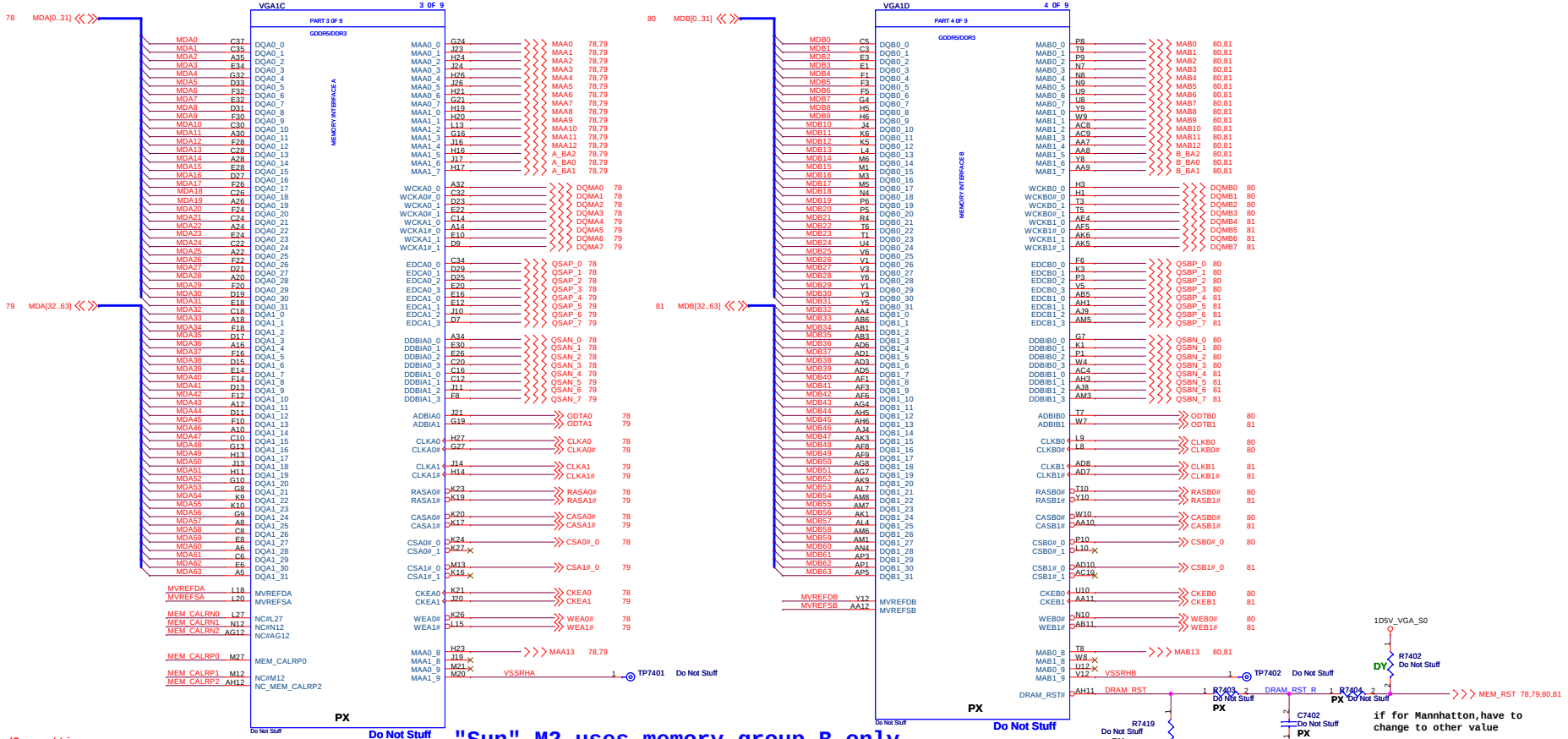
EAEG50 KB UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU PCIE/STRAPPING

Size | Project Name: KABINI | Rev: SA

Date: Monday, February 04, 2013 | Sheet 73 of 102



DDR3/GDDR3 Memory Stuff Option(Mad/Park)

	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

MEM_CALRN0	Whistler/Thames: Connect to VDDR1 through a 240Ω (±0.5%) resistor, Preferred resistor tolerance is 0.5%, but 1% is acceptable. Seymour: NC Heathrow/Chelsea :NC
MEM_CALRN1	Whistler/Thames: NC Seymour: Connect to VDDR1 through a 240Ω (±0.5%) resistor Heathrow/Chelsea :NC
MEM_CALRN2	Whistler/Thames: Connect to VDDR1 through a 240Ω (±0.5%) resistor Seymour: NC Heathrow/Chelsea :NC

MEM_CALRP0	Whistler/Thames: need a 240 Ω (1%) termination to ground Seymour: NC Heathrow/Chelsea: Need a 120Ω (1%) termination to ground
MEM_CALRP1	Whistler/Thames: NC Seymour: MEM_CALRP1—need a 240Ω (1%) termination to ground
MEM_CALRP2	Whistler/Thames: MEM_CALRP2—need a 240Ω (1%) termination to ground Seymour: NC Heathrow/Chelsea: Need a 120Ω (1%) termination to ground

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Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_Digitalout
Size: Project Name: KABINI
Rev: SA
Date: Monday, February 04, 2013 Sheet 74 of 102

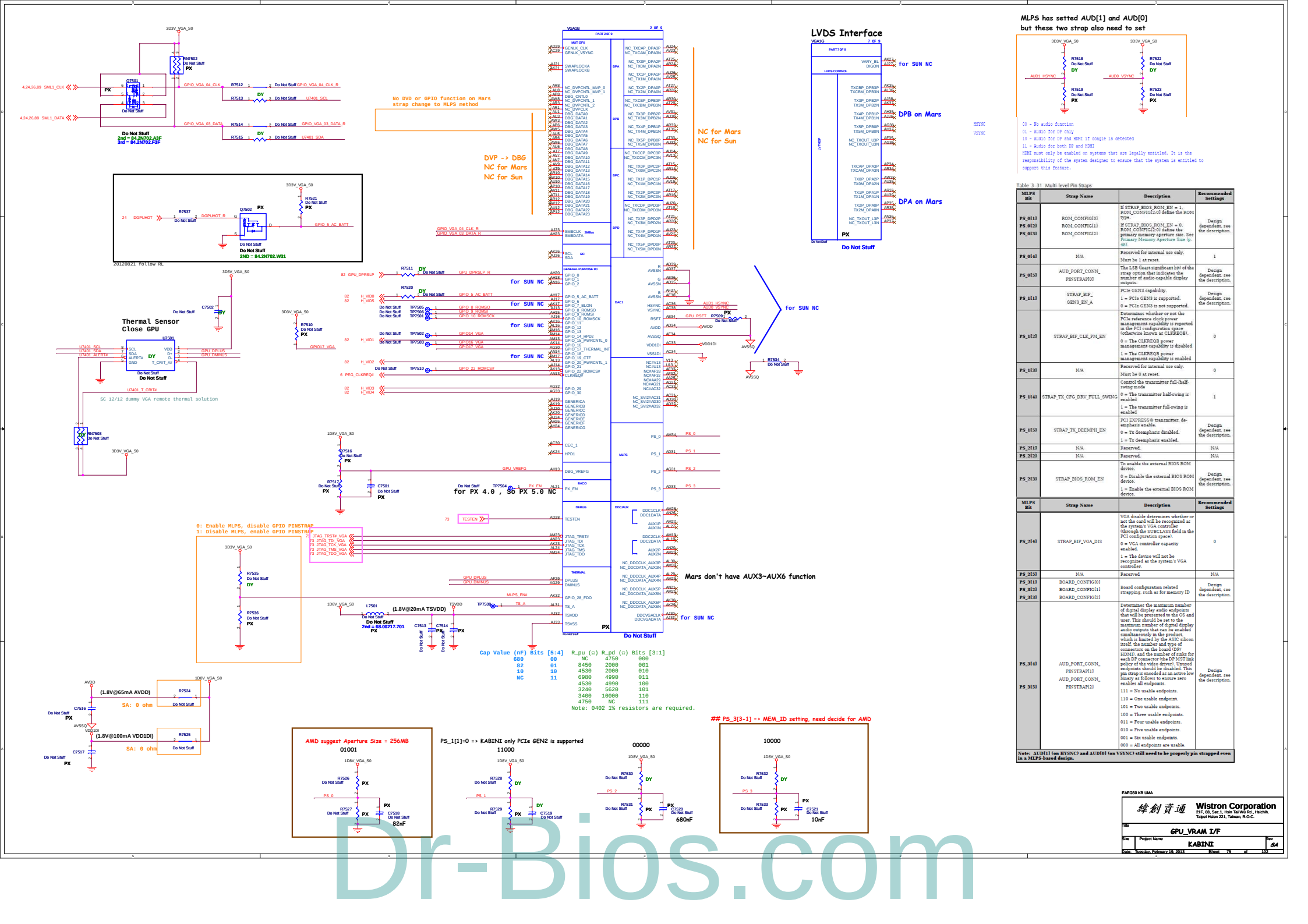


Table 3–31 Multi-level Pin Straps

MLPS Bit	Strap Name	Description	Recommended Settings
PS_0[1] PS_0[2] PS_0[3]	ROM_CONFIG[0] ROM_CONFIG[1] ROM_CONFIG[2]	If STRAP_BIOS_ROM_EN = 1, ROM_CONFIG[2:0] define the ROM type. If STRAP_BIOS_ROM_EN = 0, ROM_CONFIG[2:0] define the primary memory-aperture size. See Primary Memory Aperture Size (p. 48).	Design dependent, see the description.
PS_0[4]	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_0[5]	AUD_PORT_CONN_PINSTRAP[0]	The LSB (least significant bit) of the strap option that indicates the number of audio-capable display outputs.	Design dependent, see the description.
PS_1[1]	STRAP_BIF_GEN3_EN_A	PCIe GEN3 capability. 1 = PCIe GEN3 is supported. 0 = PCIe GEN3 is not supported.	Design dependent, see the description.
PS_1[2]	STRAP_BIF_CLK_PM_EN	Determines whether or not the PCIe reference clock power management capability is reported in the PCI configuration space (otherwise known as CLKREQ#). 0 = The CLKREQ# power management capability is disabled 1 = The CLKREQ# power management capability is enabled	0
PS_1[3]	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_1[4]	STRAP_TX_CFG_DRV_FULL_SWING	Control the transmitter full-/half-swing mode 0 = The transmitter half-swing is enabled 1 = The transmitter full-swing is enabled	1
PS_1[5]	STRAP_TX_DEEMPH_EN	PCI EXPRESS® transmitter, de-emphasis enable. 0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled.	Design dependent, see the description.
PS_2[1]	N/A	Reserved.	N/A
PS_2[2]	N/A	Reserved.	N/A
PS_2[3]	STRAP_BIOS_ROM_EN	To enable the external BIOS ROM device. 0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	Design dependent, see the description.

MLPS Bit	Strap Name	Description	Recommended Settings
PS_2[4]	STRAP_BIF_VGA_DIS	VGA disable determines whether or not the card will be recognized as the system's VGA controller (through the SUBCLASS field in the PCI configuration space). 0 = VGA controller capacity enabled. 1 = The device will not be recognized as the system's VGA controller.	0
PS_2[5]	N/A	Reserved	N/A
PS_3[1] PS_3[2] PS_3[3]	BOARD_CONFIG[0] BOARD_CONFIG[1] BOARD_CONFIG[2]	Board configuration related strapping, such as for memory ID	Design dependent, see the description.
PS_3[4] PS_3[5]	AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[2]	Determines the maximum number of digital display audio endpoints that will be presented to the OS and user. This should be set to the maximum number of digital display audio outputs that can be enabled simultaneously in the product, which is limited by the ASIC silicon itself, the number and type of connectors on the board (DP/ HDMI), and the number of sinks for each DP connector (the DP MST link policy of the video driver). Unused endpoints should be disabled. This pin strap is encoded as an active low binary as follows to ensure zero enables all endpoints. 111 = No usable endpoints. 110 = One usable endpoint. 101 = Two usable endpoints. 100 = Three usable endpoints. 011 = Four usable endpoints. 010 = Five usable endpoints. 001 = Six usable endpoints. 000 = All endpoints are usable.	Design dependent, see the description.

Note: AUD[1] (on HSYNC) and AUD[0] (on VSYNC) still need to be properly pin strapped even in a MLPS-based design.

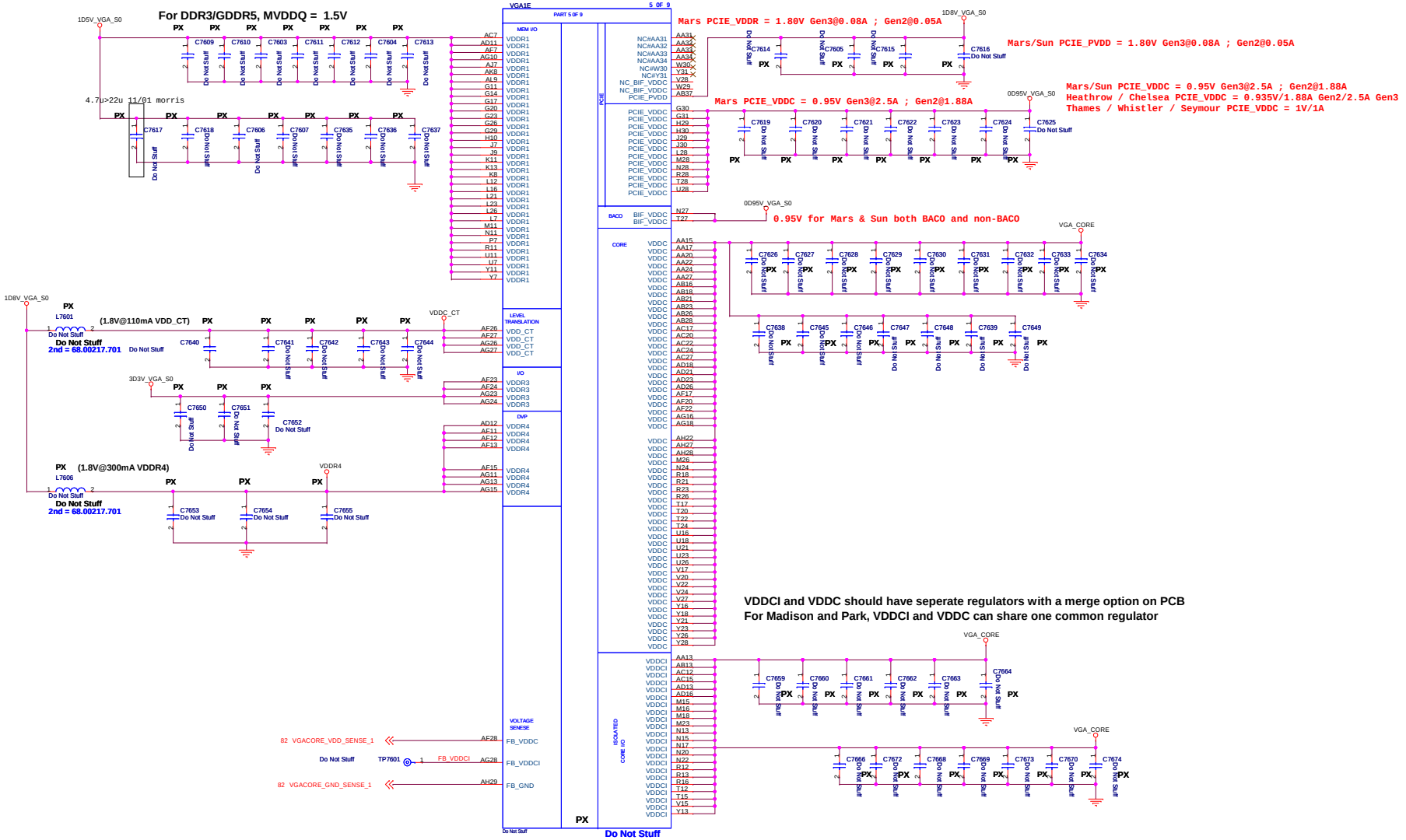
EAEG50 K8 UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_VRAM I/F

Size: Project Name: KABINI Rev: SA

Date: Tuesday, February 19, 2013 Sheet 75 of 102



EAEG50 KB UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_GPIO/STRAP

Size | Project Name: KABINI | Rev: SA

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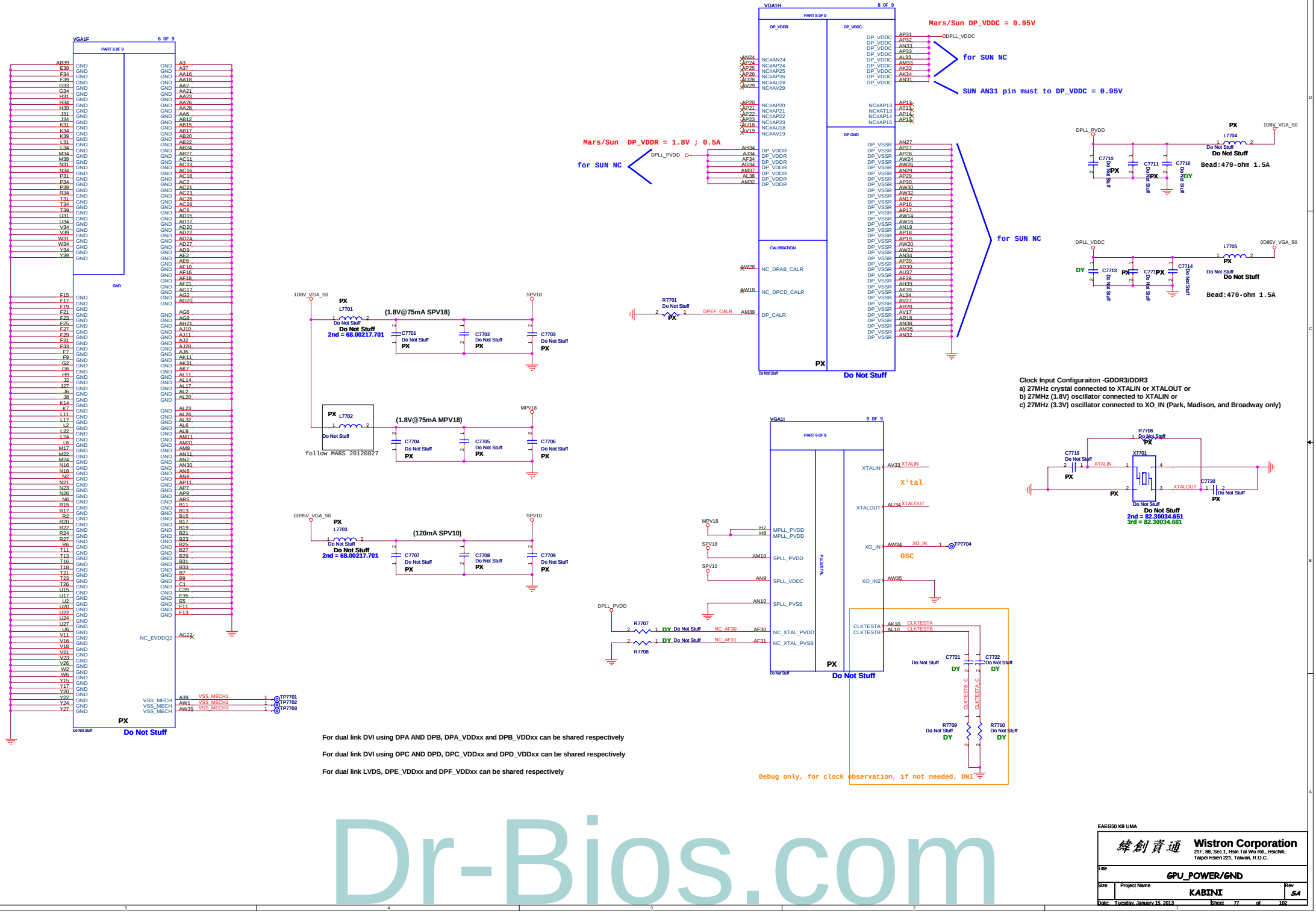


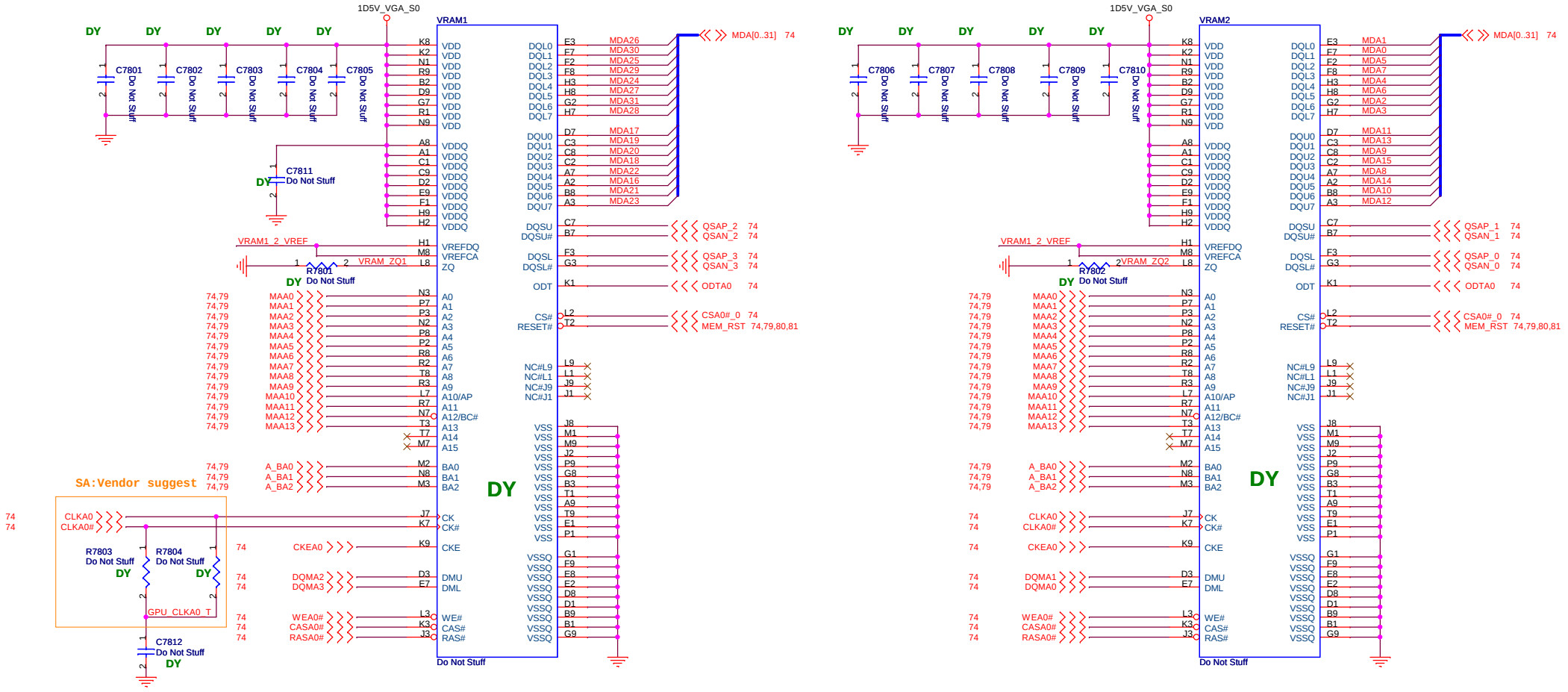
EAEG50 KB UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_POWER/GND

Size: | Project Name: KABINI | Rev: SA

Date: Tuesday, January 15, 2013 | Sheet 77 of 102



EAEG50 KB UMA

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	VRAM 1,2	
Size	Project Name: KABINI	Rev: SA
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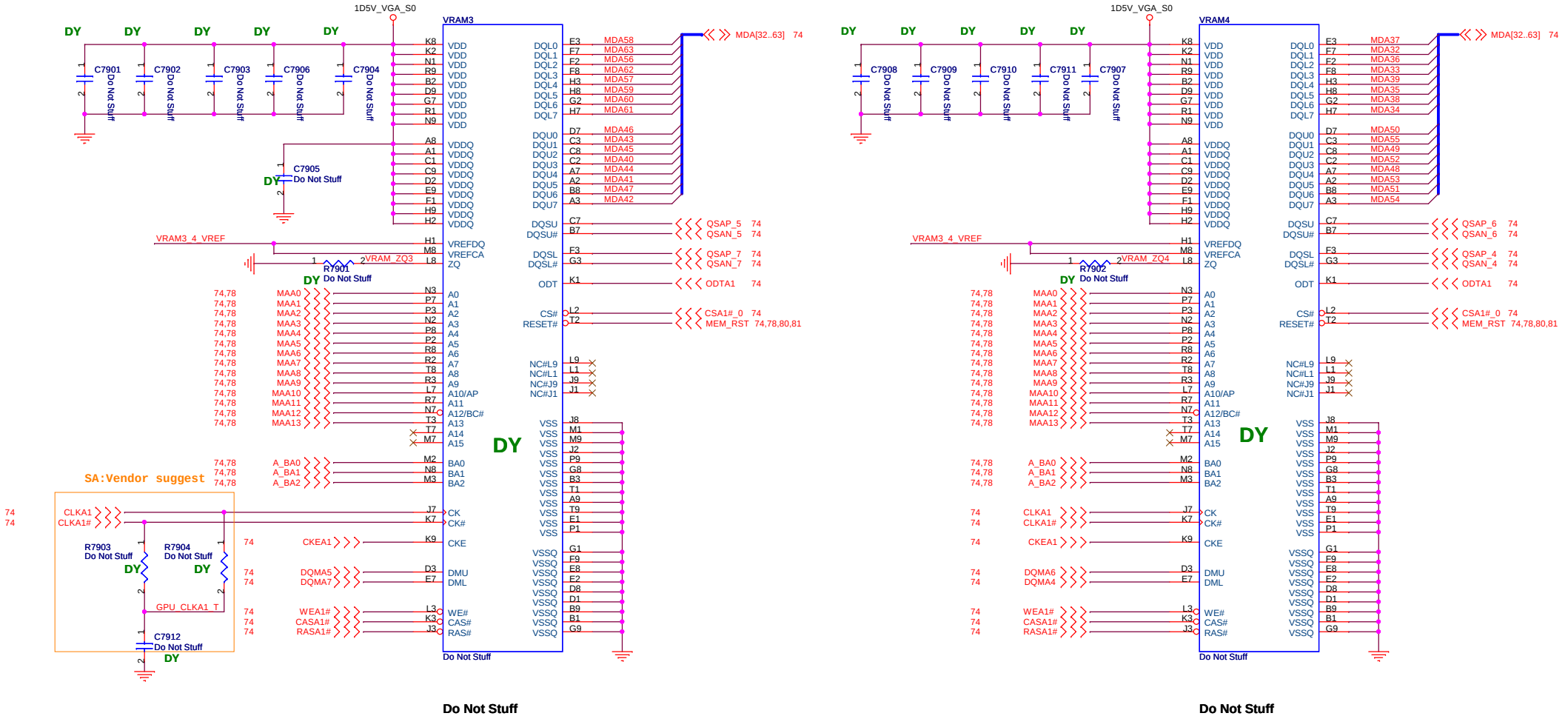
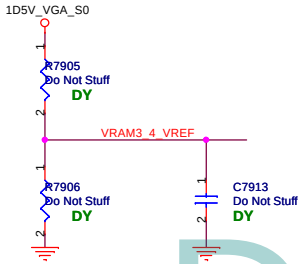


Do Not Stuff

Do Not Stuff



EAEG50 KB UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	VRAM 3,4	
Size	Project Name: KABINI	Rev: SA
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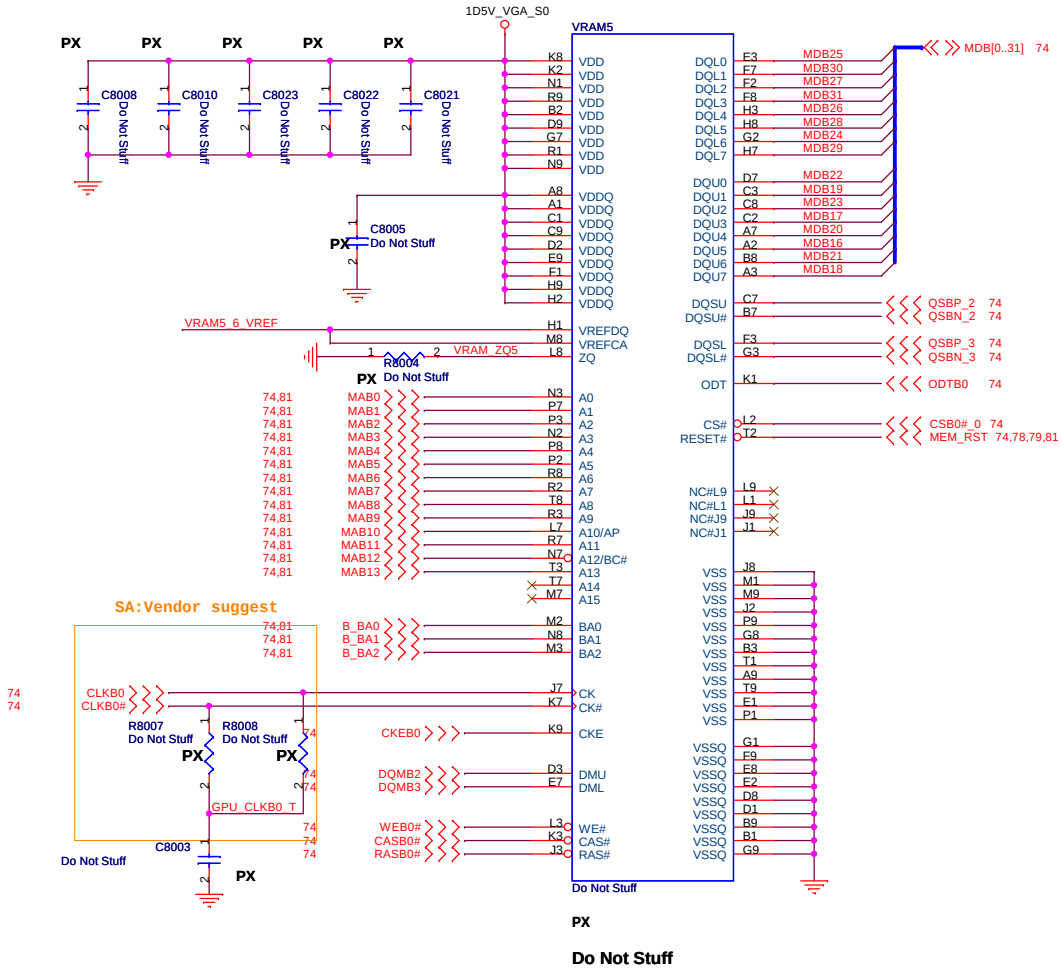
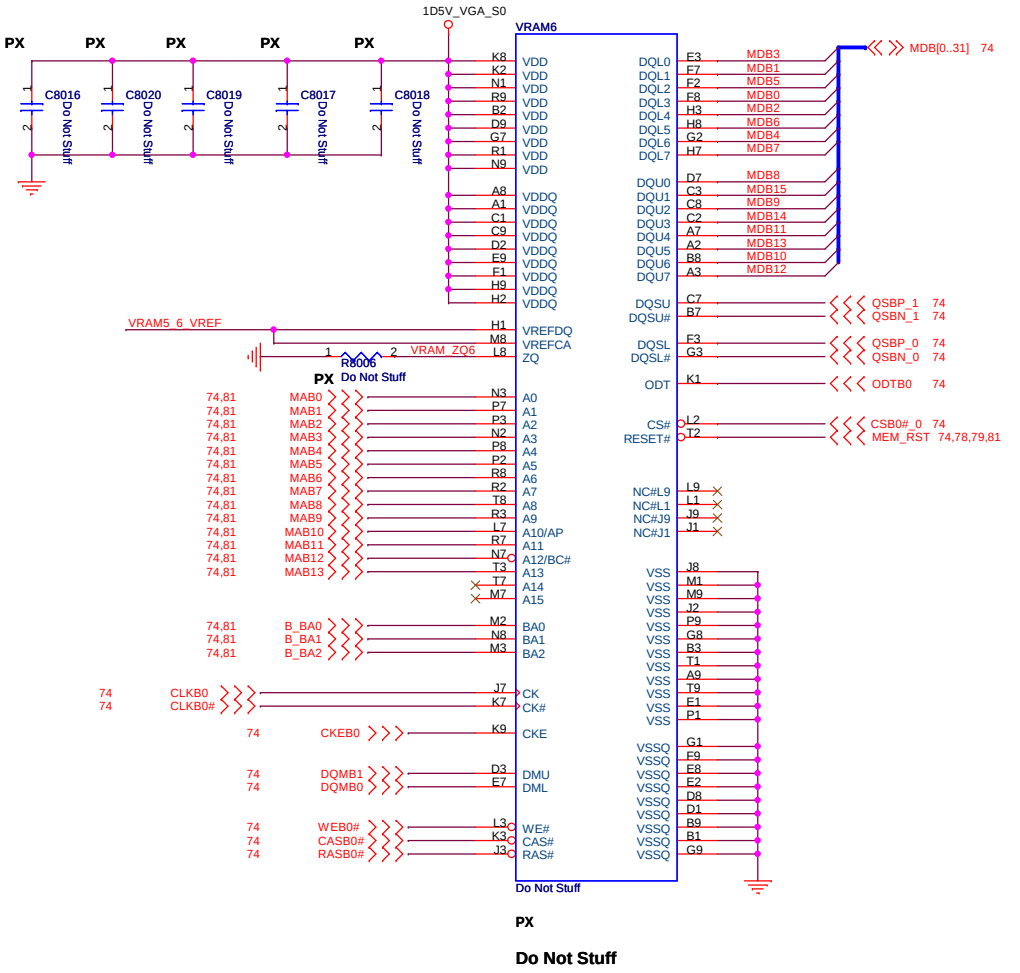
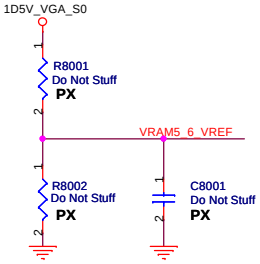




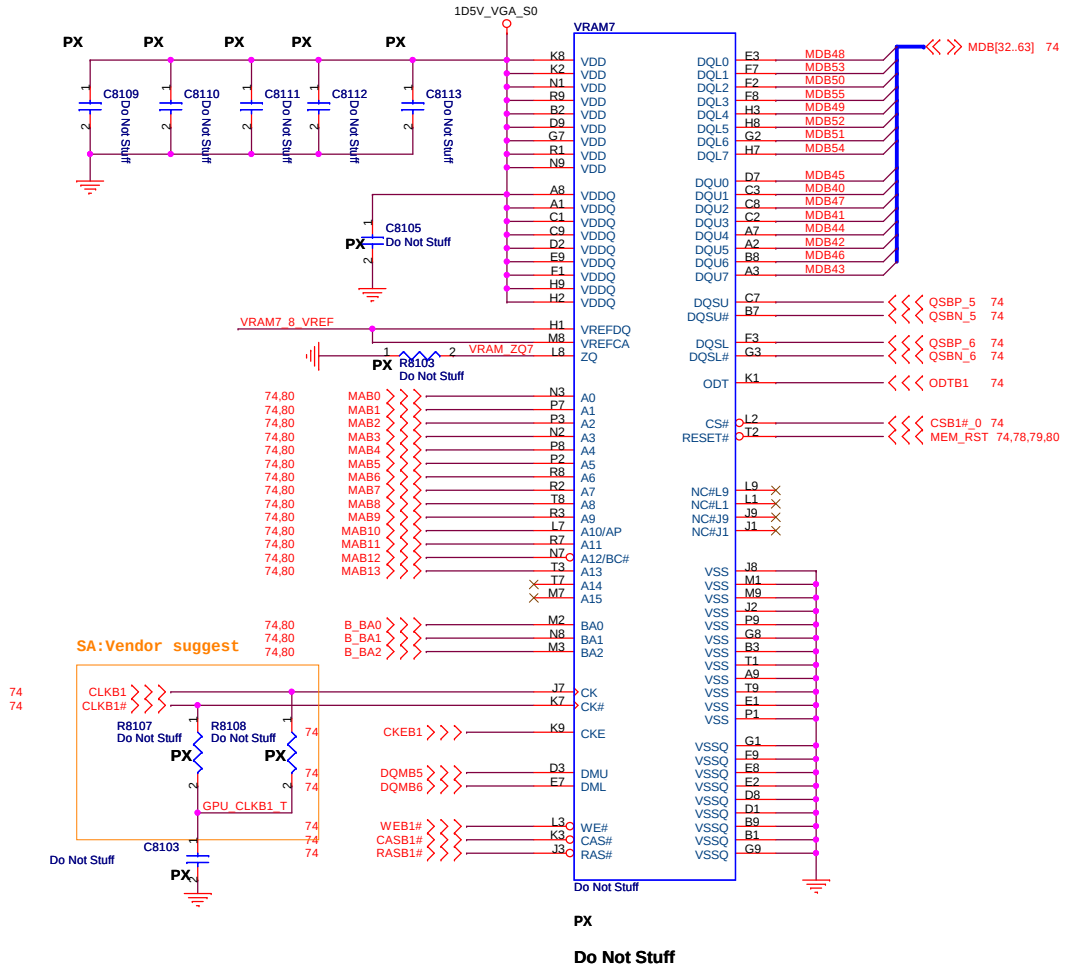


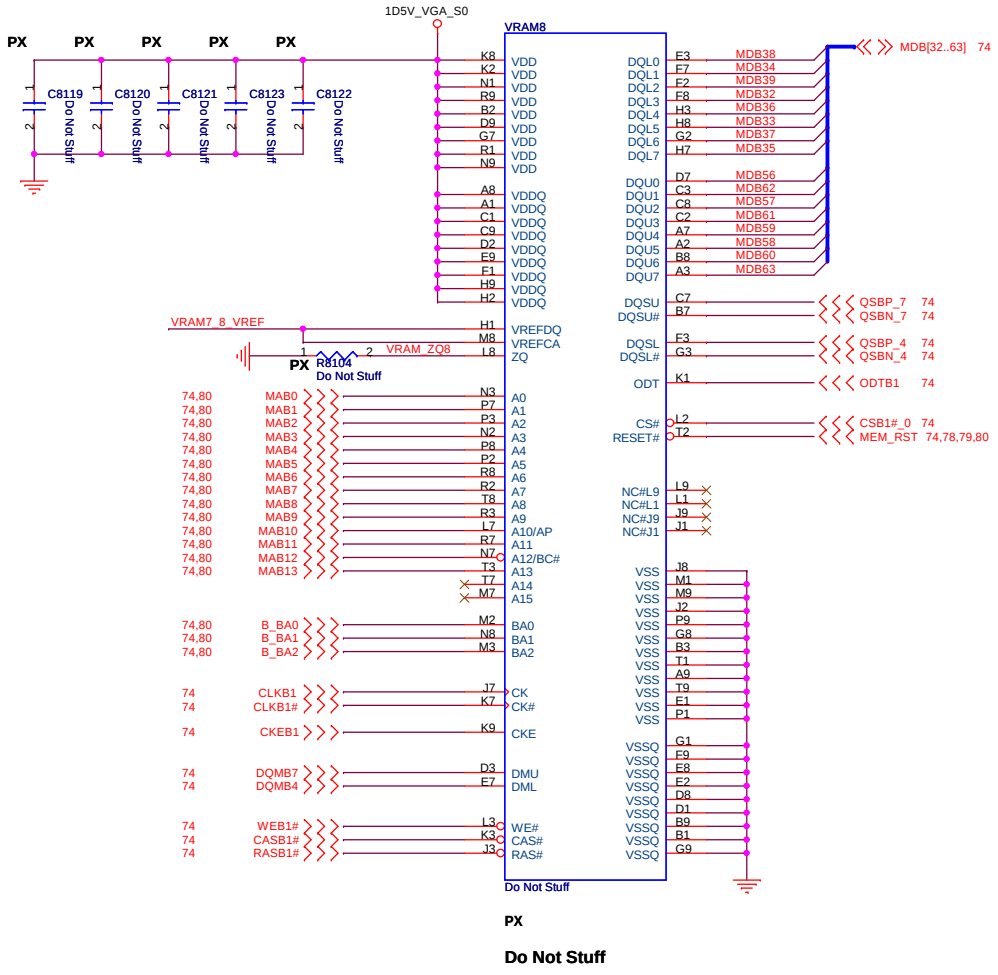
EG50 VRAM: 72.52G63.C0U (VR.2GB0G.005)
IC VRAM H5TQ2G63DFR-11C FBGA 96P 128M*16 x4

EAEG50 KB UMA

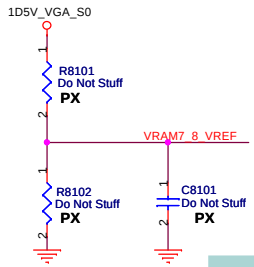
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	VRAM 5,6	
Size	Project Name: KABINI	Rev: SA
Date: Monday, February 04, 2013	Sheet 80 of 102	





Do Not Stuff



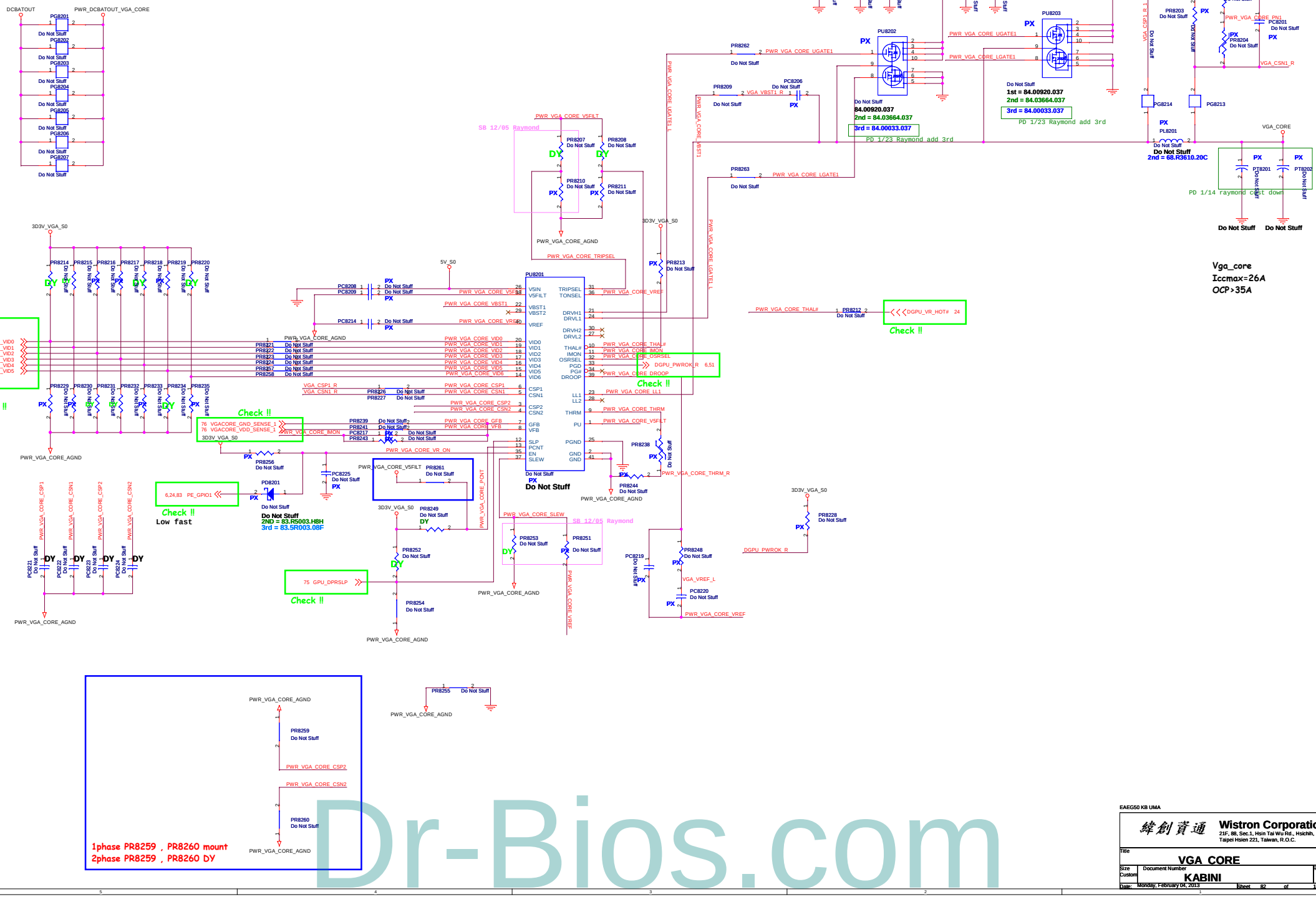
EG50 VRAM: 72.52G63.C0U (VR.2GB0G.005)
IC VRAM H5TQ2G63DFR-11C FBGA 96P 128M*16 x4

EAEG50 KB UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VRAM 7,8		
Size	Project Name: KABINI	Rev: SA
Date: Monday, February 04, 2013	Sheet 81 of 102	

SSID = PWR.Plane.Regulator_GFX



EAEG50 KB UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA_CORE

Size: Custom | Document Number: KABINI | Rev: SA

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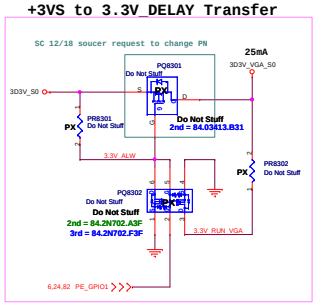
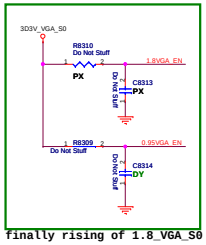
APL3523 for VGA_Power

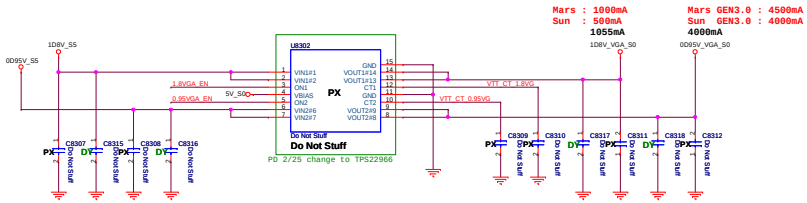
	PE_GPIO0	PE_GPIO1
dGPU mode	H	H
IGPU	L	L
IGPU with BACO	H	H

+3VS to 3.3V_DELAY Transfer





finally rising of 1.8_VGA_S0



EAEG50 KB LIMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DISCRETE VGA POWER

Size: Custom | Document Number: KABINI | Rev: SA

Date: Monday, February 25, 2013 | Sheet 83 of 103

EAEG50 KB UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Switch GFX	
Size	Project Name: KABINI	Rev: SA
Date: Friday, September 07, 2012	Sheet 84 of 102	

EAEG50 KB UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

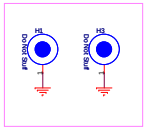
Title: **Switch VGA**

Size | Project Name: **KABINI** | Rev: **SA**

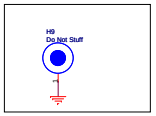
Date: Friday, September 07, 2012 | Sheet 85 of 102

ZZ.00PAD.2N1

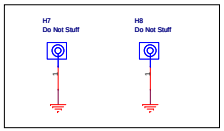
SB 11/14 follow HW for factory issue



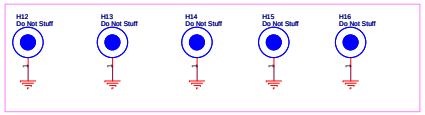
ZZ.00PAD.D01



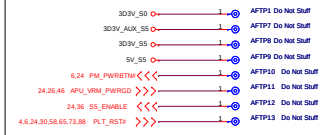
ZZ.00PAD.E01



SB 11/20 ZZ.00pad.2T1 for change BKT size

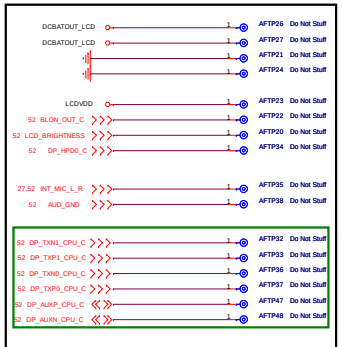


Check test point

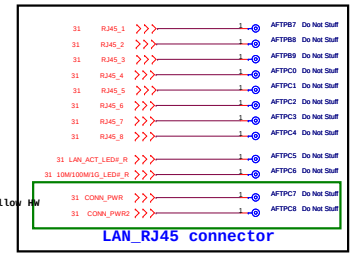


Test Point放在Dimm Door打開可量測處

10/15 follow HW

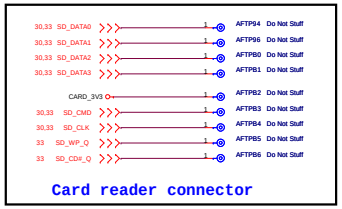


EDP + MIC connector

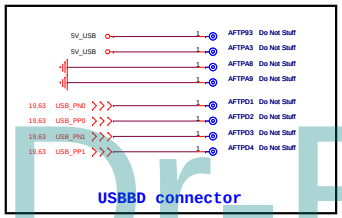


10/15 follow HW

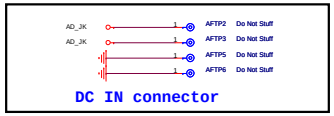
LAN_RJ45 connector



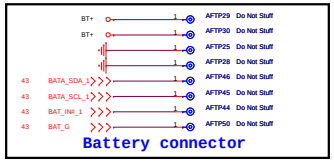
Card reader connector



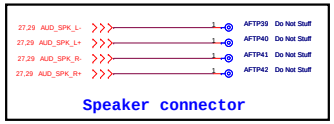
USBBD connector



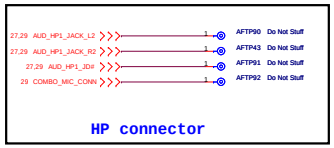
DC IN connector



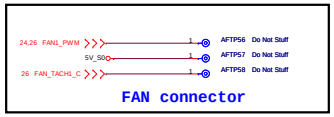
Battery connector



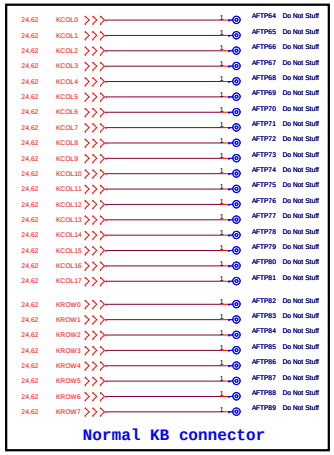
Speaker connector



HP connector



FAN connector



Normal KB connector

10/15 follow HW

Touch Pad connector

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Title: UNUSED PARTS/EMI Capacitors

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緯創資通

Wistron Corporation

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Title	NFC	
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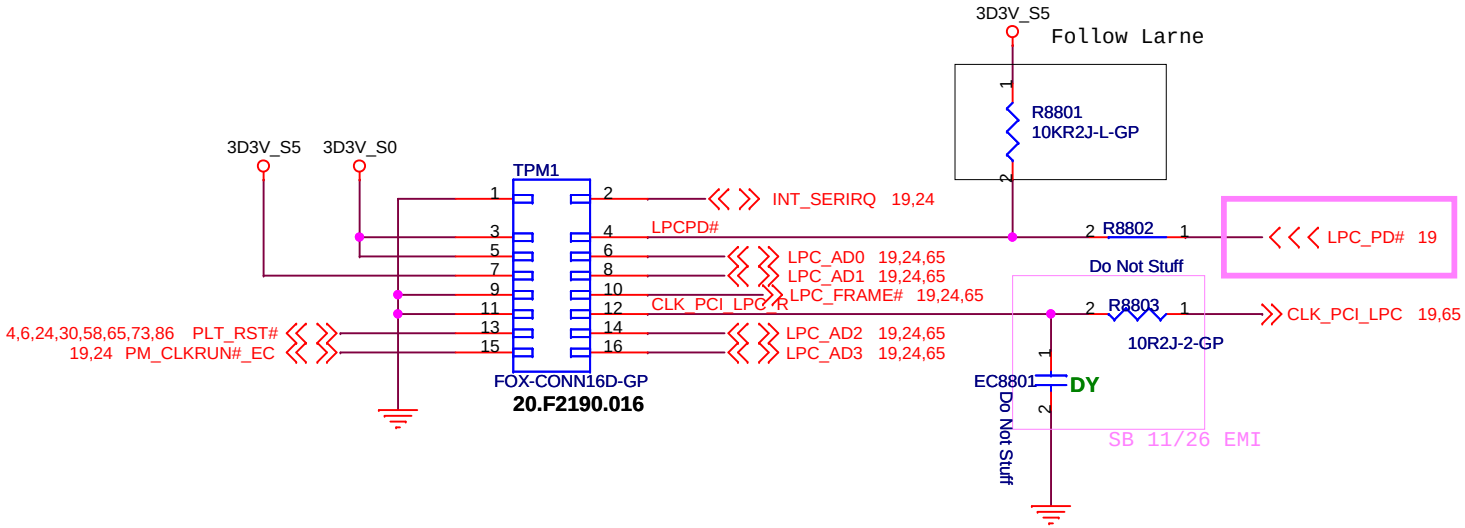

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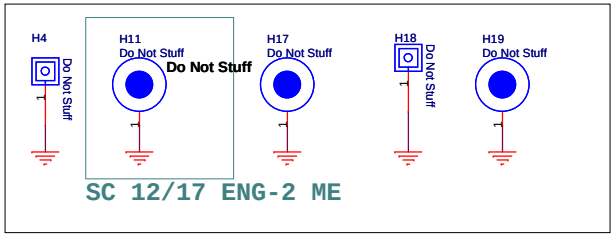
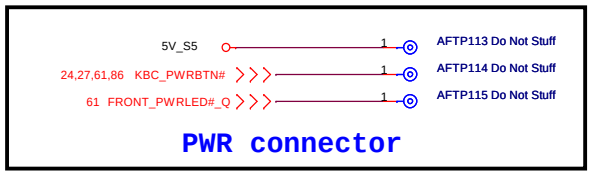
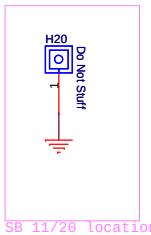
H4 & H11 & H17 & H18 & H19 for EG50



PWRBD AFTP for EG50

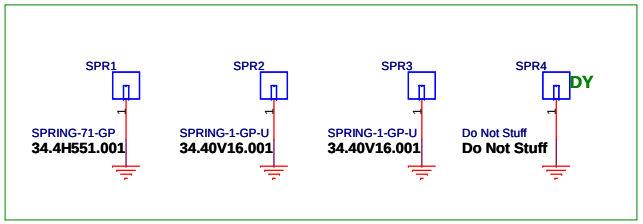


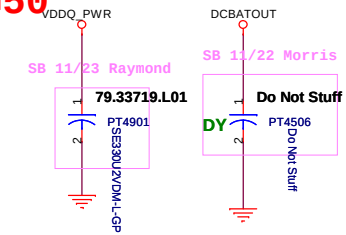
ZZ.00PAD.571



SB 11/20 location same with 14" H2

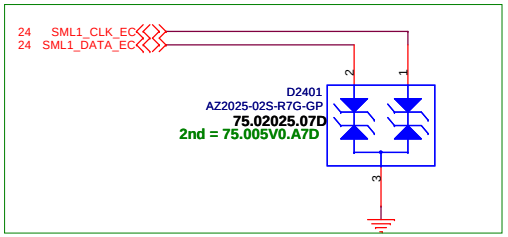
PD 1/23 EMI Jen

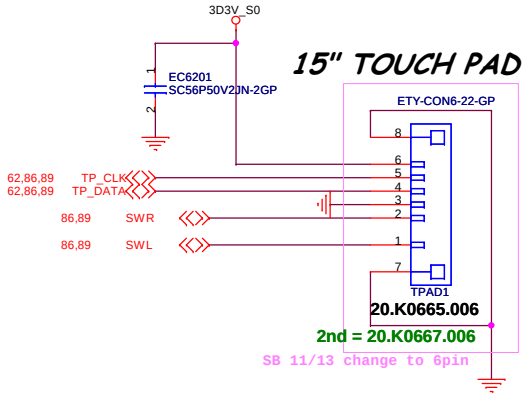


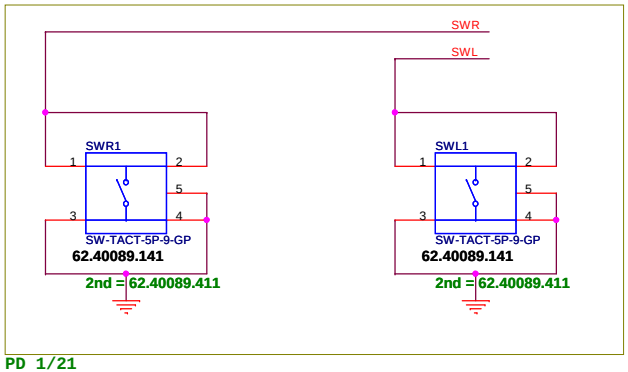


SB 11/23 3mm high limit in EG50

PD 01/31 Different Net name in 14" & 15" for placement







PD 1/21
SWL1 / SWR1 1st change to 62.40089.141,2nd change to 62.40089.411 ,
because 160kg change to 100kg.

For AFTE

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Title	15"	
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Title: table of content

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Title: **Change History**

Size | Project Name: **KABINI** | Rev: SA

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EAEC50 KB LMA

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Title: Power Sequence

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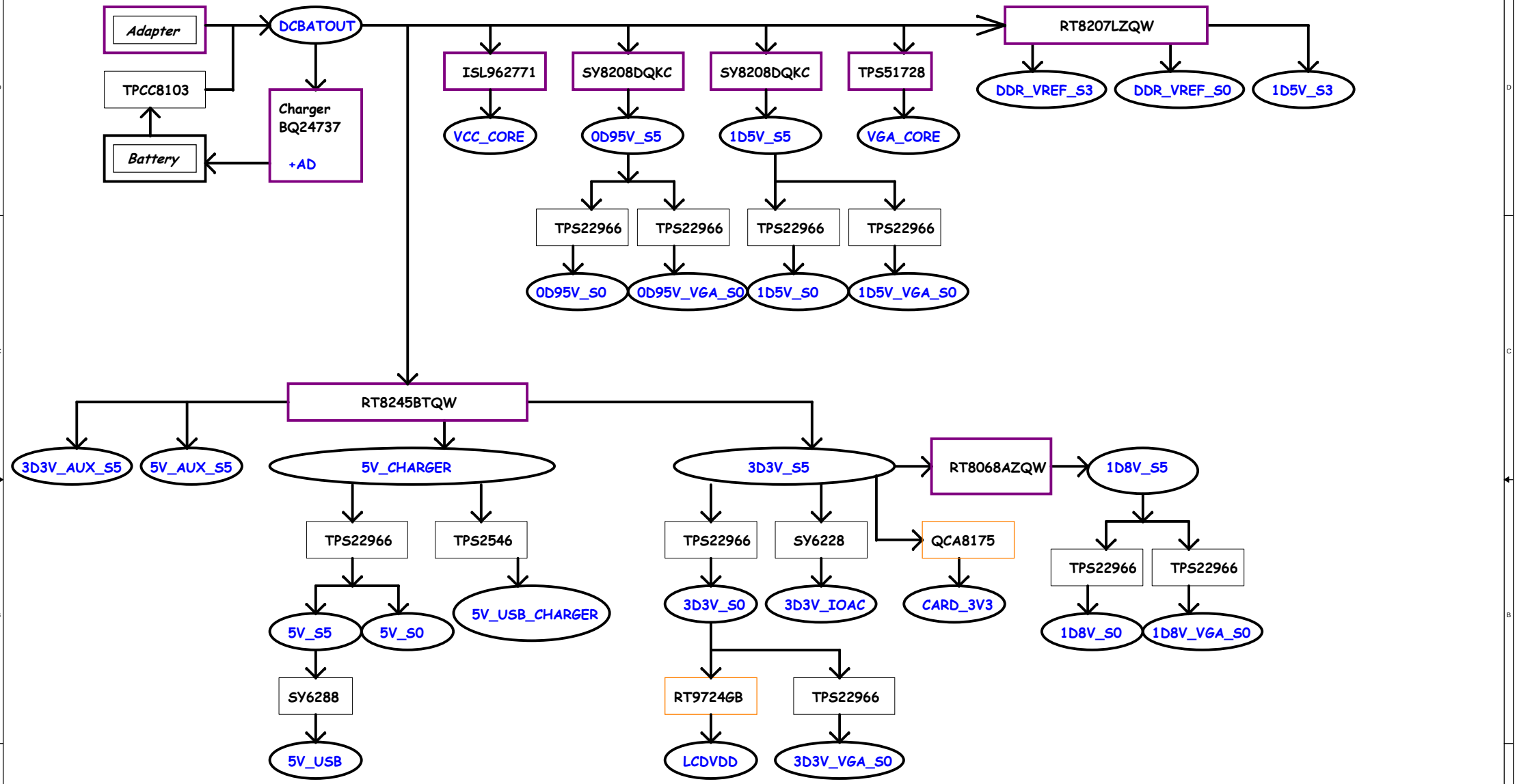

Power Shape

Regulator	LDO	Switch

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Title: **Power block Diagram**

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	KABINI	SA

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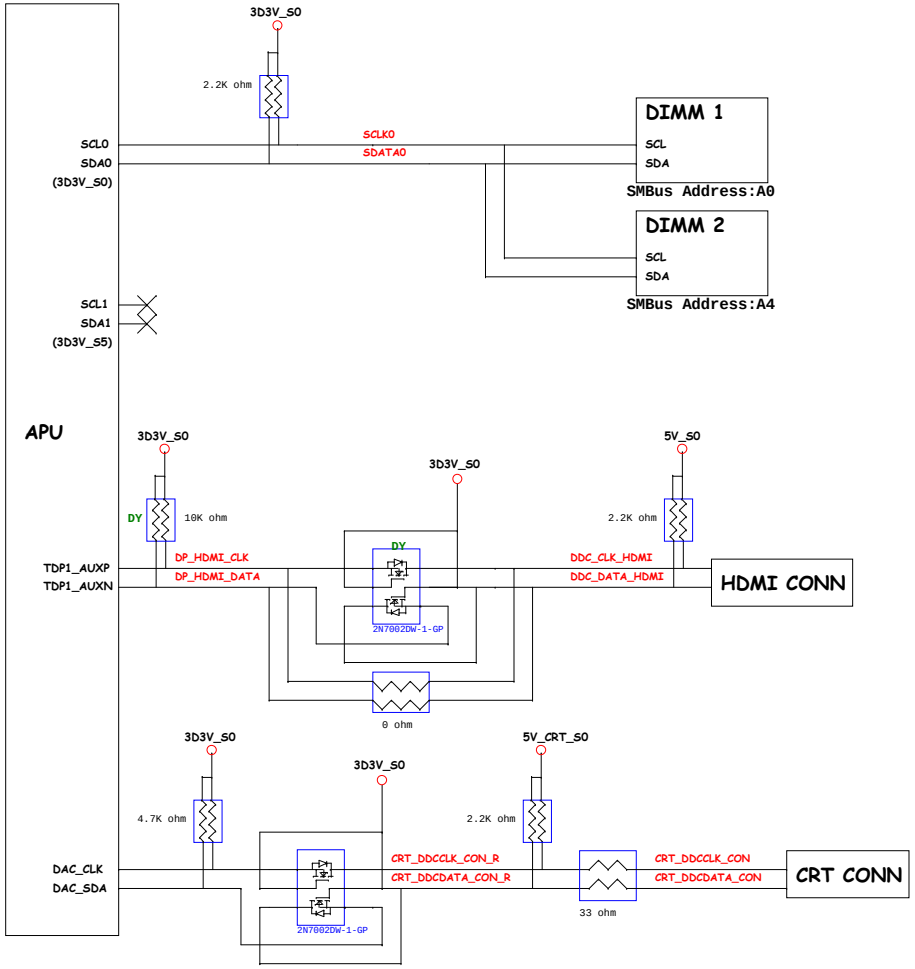
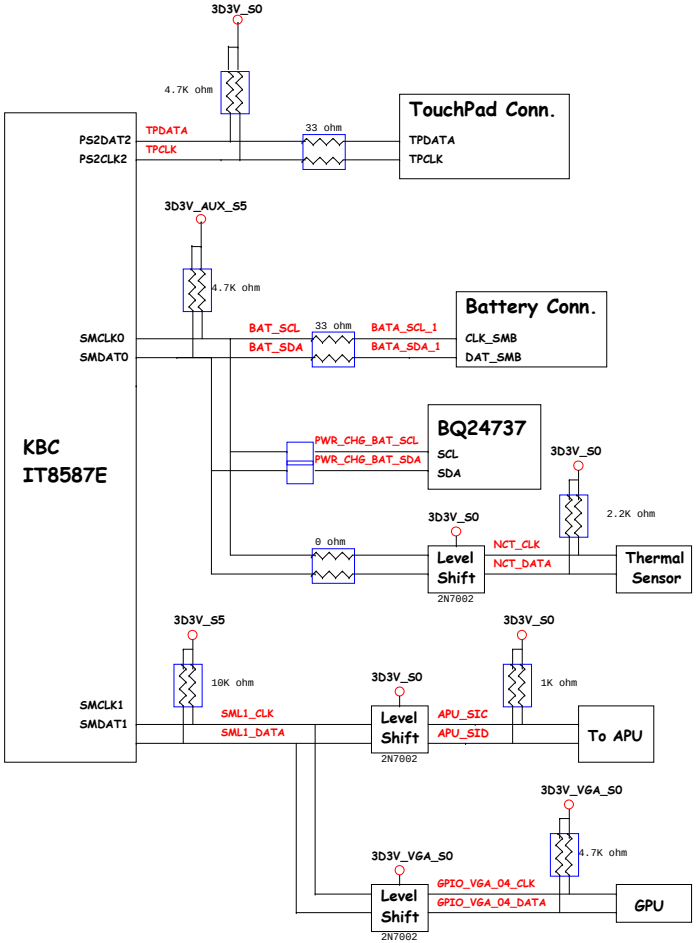
SMBus Block Diagram



KBC SMBus Block Diagram



EAEG50 KB UMA

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Title: SMBUS Block Diagram

Size	Project Name	Rev
	KABINI	SA

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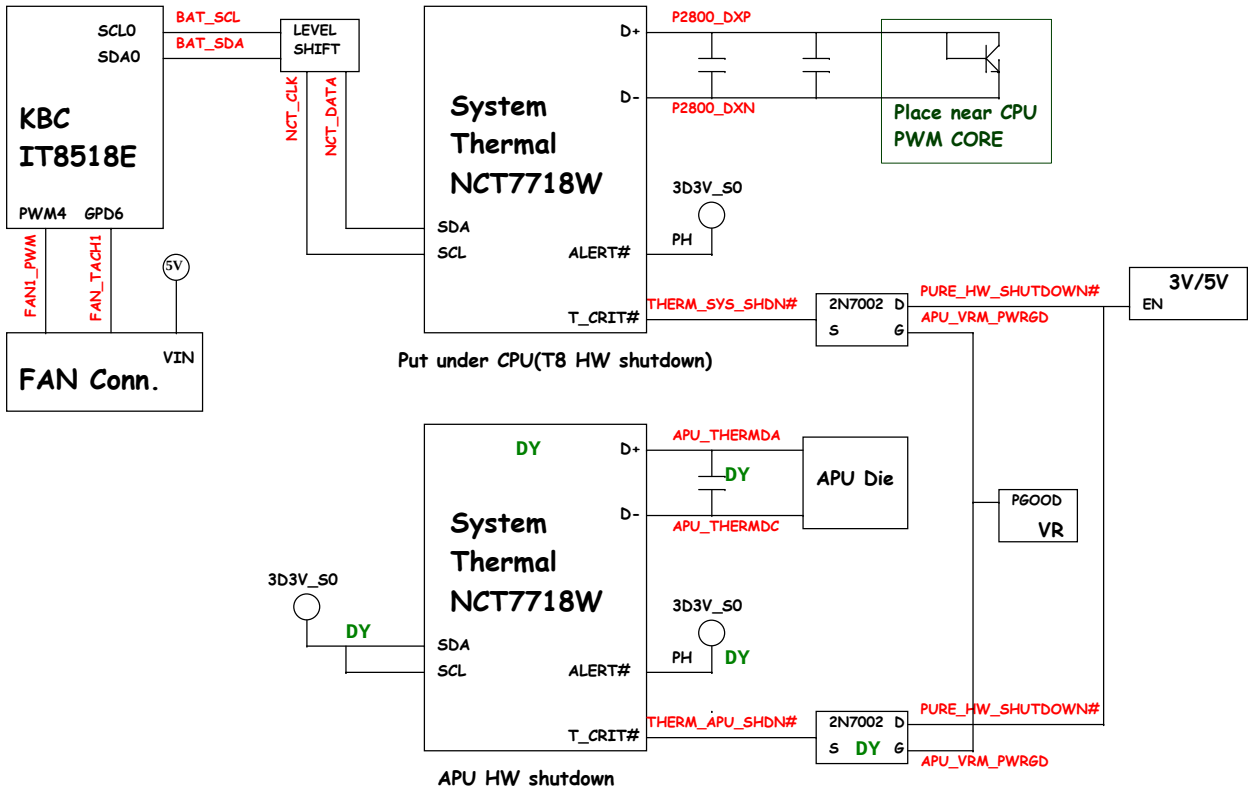
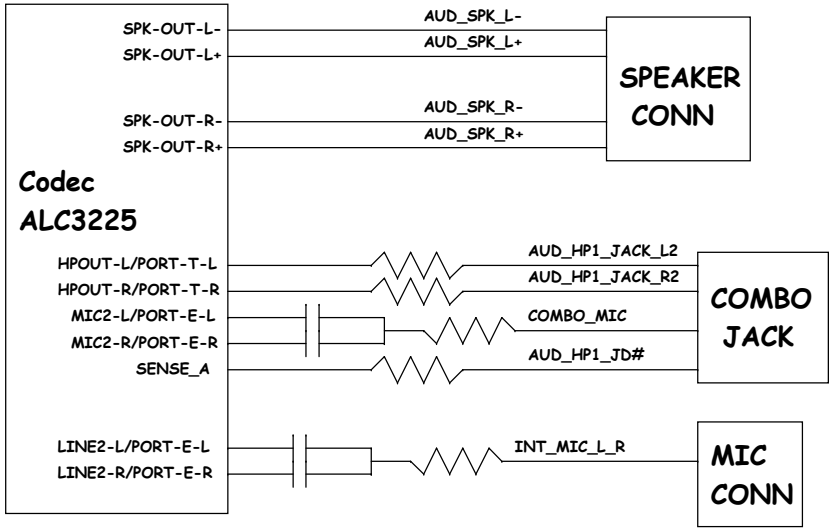
Thermal Block Diagram



Audio Block Diagram



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Title: Thermal/Audio Block Diagram

Size | Project Name: KABINI | Rev: SA

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