ZK2 SYSTEM BLOCK DIAGRAM

BOM MARK
I@: INT VGA
E@: STUFF FOR EXT VGA
ND@: STUFF FOR NON-DOCK
D@: DOCK
SP@: SPECIAL FOR EXT/INT VGA

DDR PWR TPS5116 P36 | CHARGER ISL6251 P32
THERMAL PROTECTION P37 | 3/5V SYS PWR ISL6237 P33
2.5V/ 1.5V PWR DISCHARGER P38 | CPU CORE PWR ISL6262A P34
POWER TREE P39 | +1.05V RT8202 P35

X'TAL 14.318MHz
CLOCK GENERATOR
ICS: ICS9LPRS365BGLFT
SELGO: SLG8SP512K05
P2

Penryn 479
uFCPGA
P3, P4

Thermal Sensor
(NS LM95245) P3

Fan Driver
(G991) P30

FSB
667/800/1067 Mhz

MXM (n-Vidia)
NB9M-GS
VRAM 512MB
P17

PCIE
EXT_LVDS
EXT_CRT
EXT_DVI

SWITCH CIRCUIT
P18

CRT P18
LVDS P18

DDRII
SO-DIMM 0
SO-DIMM 1
P16

Dual Channel DDR2
667/800 MHz

NB
Cantiga
(GM45/ PM45/ GL40)
P5, P6, P7, P8, P9, P10, P11

LVDS — INT_LVDS
RGB — INT_CRT

HDMI switch (PS8122) P19
HDMI P19
DOCKING/DVI P19

MP-Stage
31ZK2MB0000: ZK2 MB ASSY(GM/UMA)ASSY W/O CPU
31ZK2MB0010: ZK2 MB ASSY(PM/MXM)ASSY W/O CPU
31ZK2MB0020: ZK2 MB ASSY(PM/MXM) W/O CPU/E-SATA

X4 DMI interface

HDD (SATA) *2 P23
ODD (SATA) P23
SATA0
SATA4
SATA1
SATA5

eSATA Conn. USB1 P29
eSATA Buffer (PI2EQX3021) P29

USB Port x 3 USB0, 4, 7 P29
Bluetooth USB5 P21
CCD USB11 P18
FingerPrint USB9 P30
Wire Docking USB10 P30
USB 2.0

Azalia

SB
ICH9M
P12,P13,P14,P15

X'TAL 32.768KHz

PCI-Express
PCIE-1
New Card USB6 P26
USB6

PCIE-2&4
Mini Card WLAN / TV USB2 & 3 P22
USB2 & 3

USB8

PCIE-6
X'TAL 25MHz
ATHEROS Giga-LAN (AR8121) P20

Media Cardreader (RTS5158E) USB2 P27
Card Reader Connector P27

SPI
LPC

Audio CODEC (ALC888S) P24

HDCP ROM (Option) P13

EC (WPC775LDG) P31
X'TAL 32.768KHz

MDC 1.5 P24
RJ11 WIRE CONN.

SPI ROM P31
Touch Pad P30
MMB P28
K/B COON. P30
CIR P31

LAN SWITCH (PI3L500) P21
DOCK/LAN P30
Transformer P21
RJ45 P21

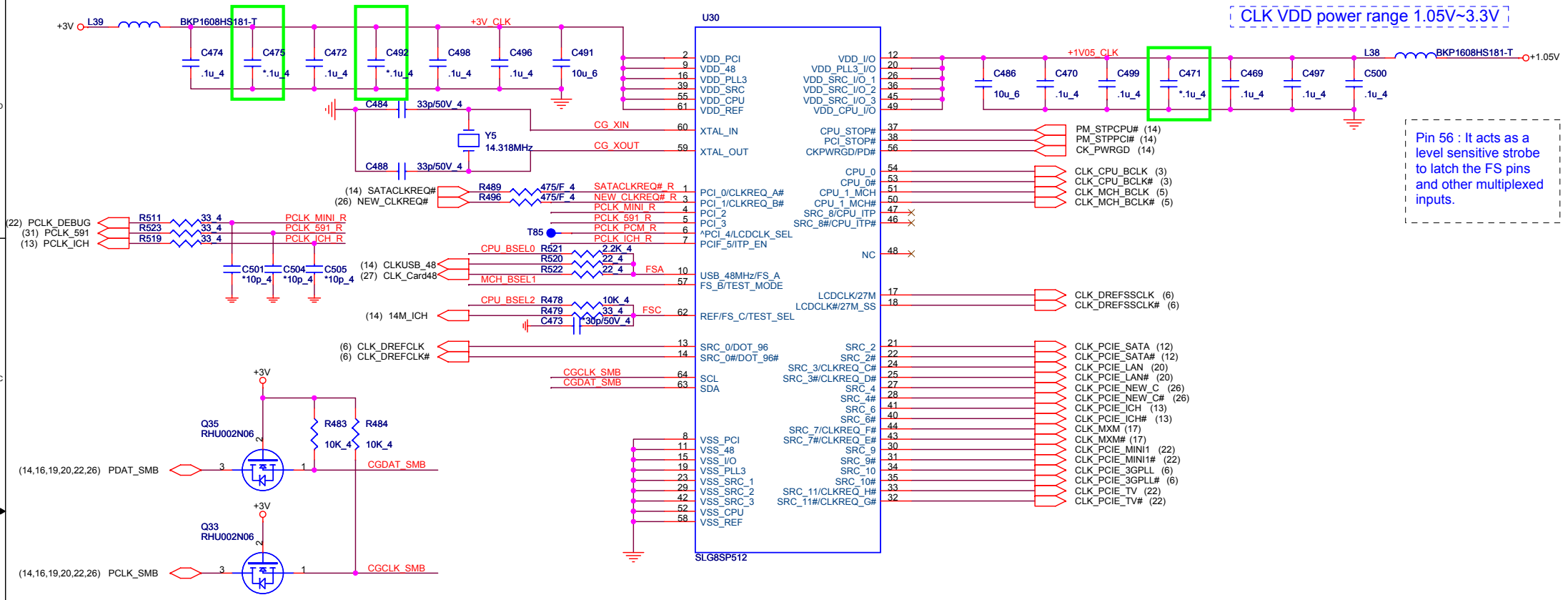
Audio Amplifier P24,P25
Sub-Amplifier (MAX9736B) P25

Speaker P25
S/PDIF P25
SUBWOOFER P25
Line in P25
MIC Jack P25
Int. D-MIC P18, P24

DA0ZK2MB6D0
DA0ZK2MB6C0
DA0ZK2MB6B0
DA0ZK2MB6A0

Quanta Computer Inc.
PROJECT : ZK2
Size | Document Number: Block Diagram | Rev 3B
Date: Friday, June 27, 2008 | Sheet 1 of 39

Clock Generator



CPU Clock select

Pin 10/57/62 : For Pin CPU frequency selection

(3) CPU_BSEL0 — CPU_BSEL0 R524 0_4 — MCH_BSEL0 (6)

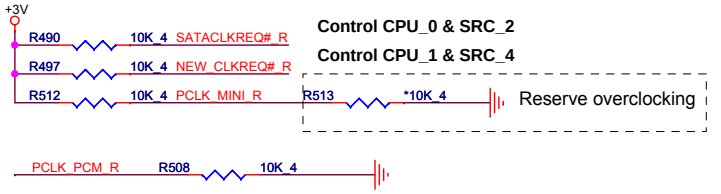
(3) CPU_BSEL1 — CPU_BSEL1 R480 0_4 — MCH_BSEL1 (6)

(3) CPU_BSEL2 — CPU_BSEL2 R476 0_4 — MCH_BSEL2 (6)

BSEL Frequency Select Table

FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz

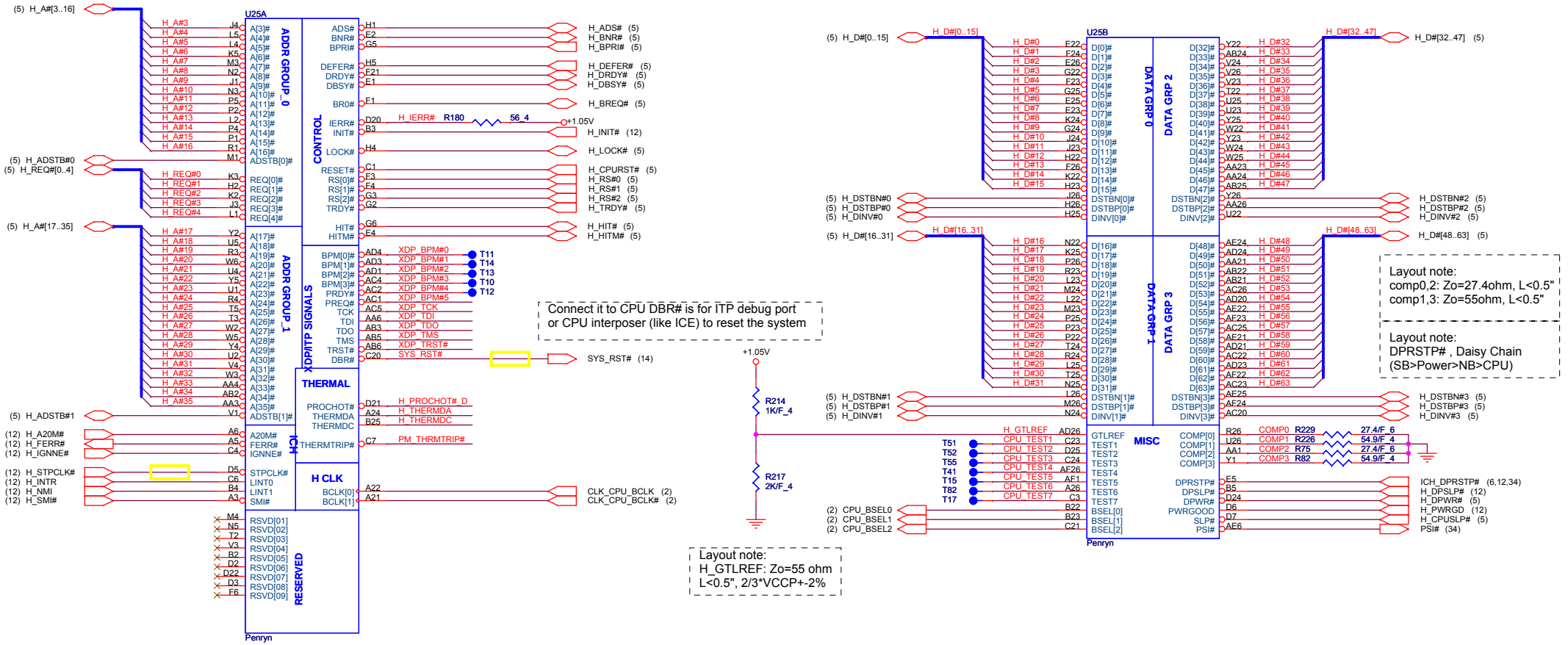
Strap table



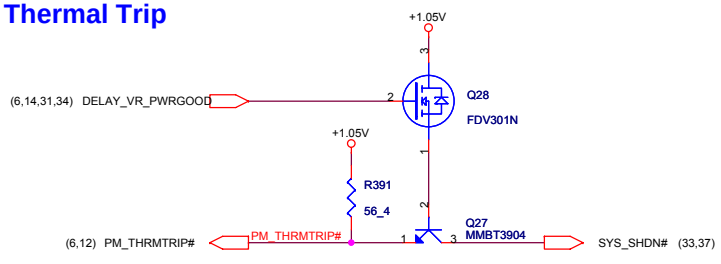
CLOCK GENERATOR

Quanta Computer Inc.
PROJECT : ZK2

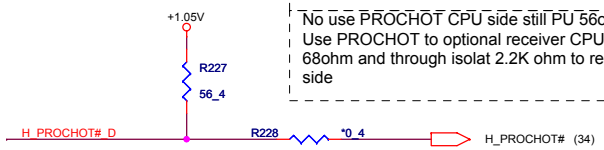
Size	Document Number	Rev
	CLOCK GENERATOR	3B
Date: Wednesday, July 09, 2008	Sheet 2 of 39	



Thermal Trip



Processor hot

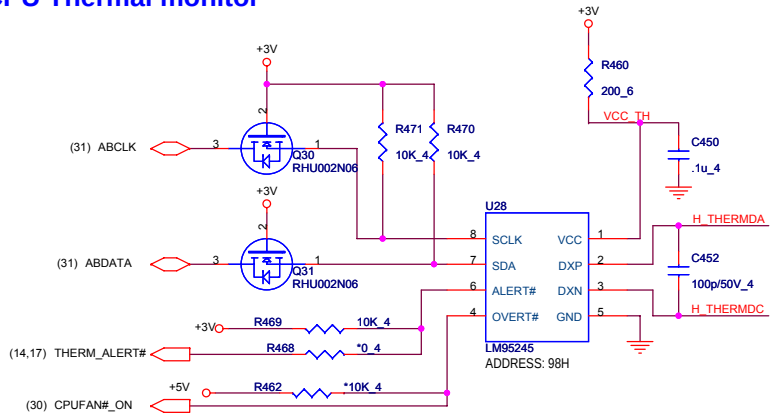


No use Thermal trip CPU side still PU 56ohm.
Use Thermal trip can share PU at SB side

No use PROCHOT CPU side still PU 56ohm.
Use PROCHOT to optional receiver CPU side PU 68ohm and through isolat 2.2K ohm to receiver side

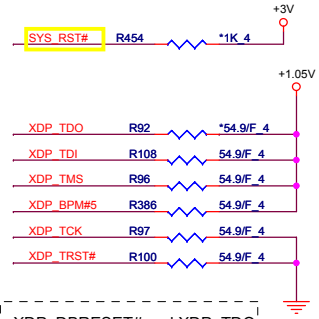
CPU 1/2

CPU Thermal monitor



NS	AL095245000
WINDBOND	AL83L771000

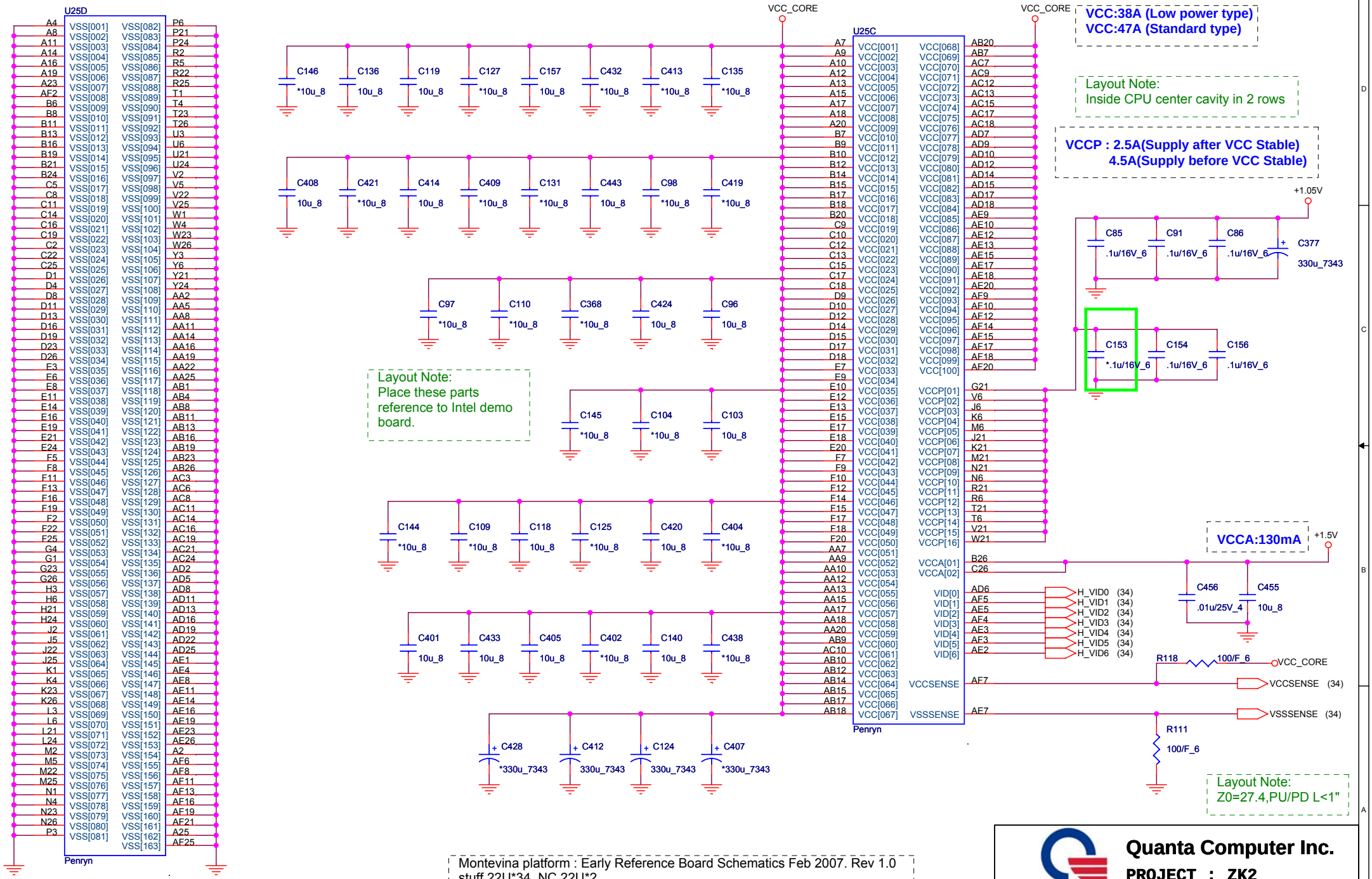
XDP PU/PD



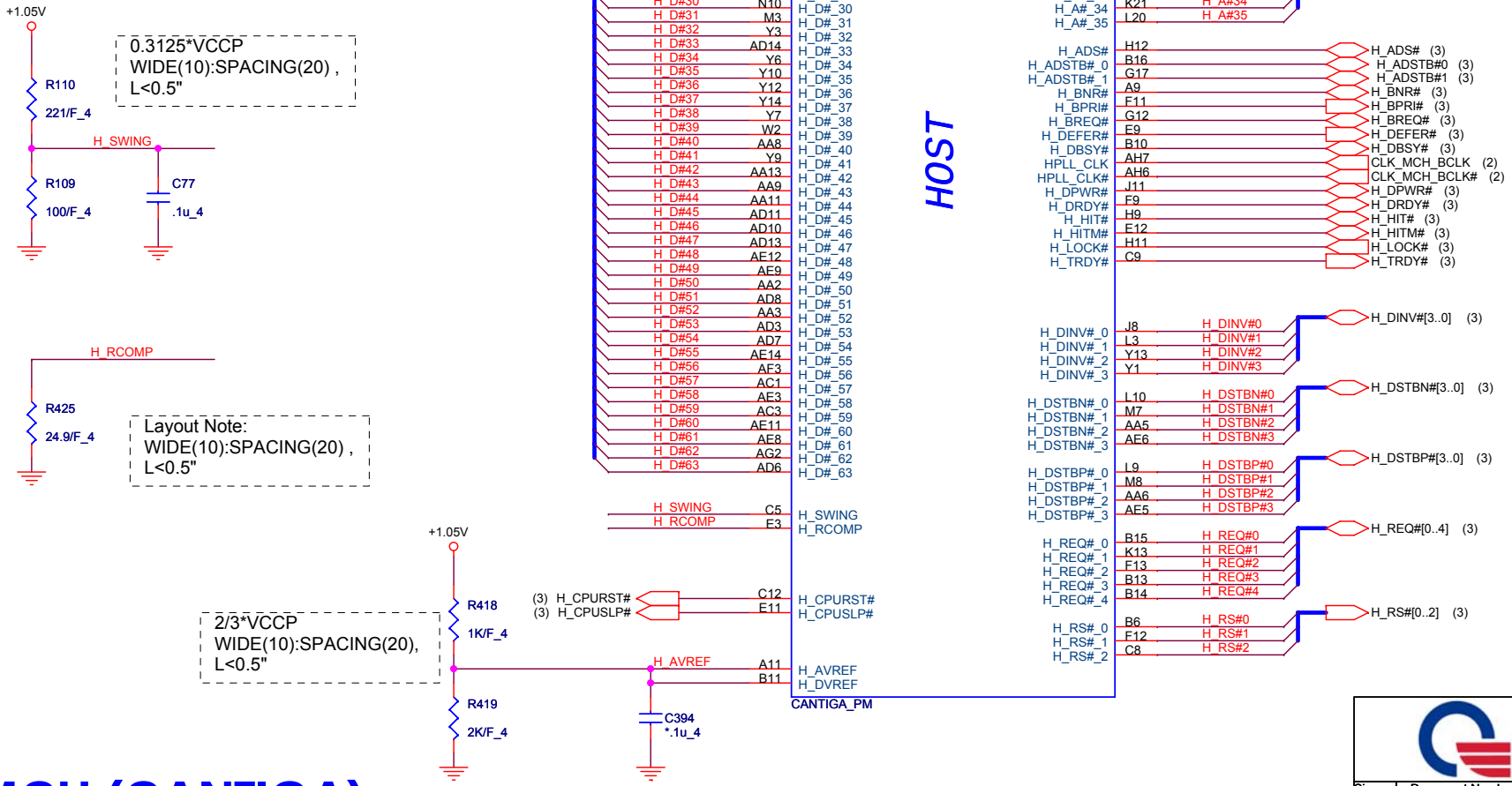
XDP_DBRESET# and XDP_TDO reserve for XDP

Quanta Computer Inc.
PROJECT : ZK2

Size	Document Number	Rev
	CPU Host Bus	3B
Date: Wednesday, July 09, 2008	Sheet 3 of 39	


U25D
Penryn
U25C
Penryn
VCC_CORE
VCC_CORE
VCC:38A (Low power type)
VCC:47A (Standard type)
Layout Note:
Inside CPU center cavity in 2 rows
VCCP : 2.5A(Supply after VCC Stable)
4.5A(Supply before VCC Stable)
+1.05V
Layout Note:
Place these parts
reference to Intel demo
board.
VCCA:130mA
+1.5V
Layout Note:
Z0=27.4,PU/PD L<1"
R118 100/F_6
R111 100/F_6
VCCSENSE (34)
VSSSENSE (34)
H_VID0 (34)
H_VID1 (34)
H_VID2 (34)
H_VID3 (34)
H_VID4 (34)
H_VID5 (34)
H_VID6 (34)
Montevina platform : Early Reference Board Schematics Feb 2007. Rev 1.0
stuff 22U*34, NC 22U*2
stuff 330U*2, NC330U*2
CPU 2/2
Quanta Computer Inc.
PROJECT : ZK2
Size
Document Number
CPU Power
Rev
3B
Date: Friday, June 27, 2008
Sheet 4 of 39

	QCI P/N
Intel Cantiga (G)M	**AJSLB940T04**
Intel Cantiga (P)M	AJSLB970T06



GMCH (CANTIGA)

Quanta Computer Inc.

PROJECT : ZK2

Size	Document Number	Rev
	GMCH HOST	3B

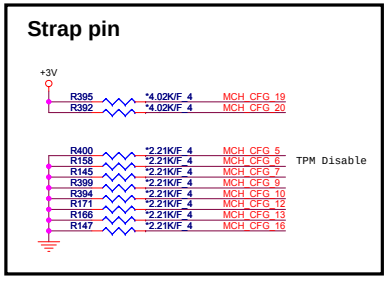
Date: Friday, June 27, 2008 Sheet 5 of 39

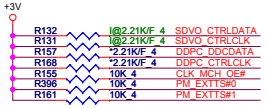
IV@
EV@

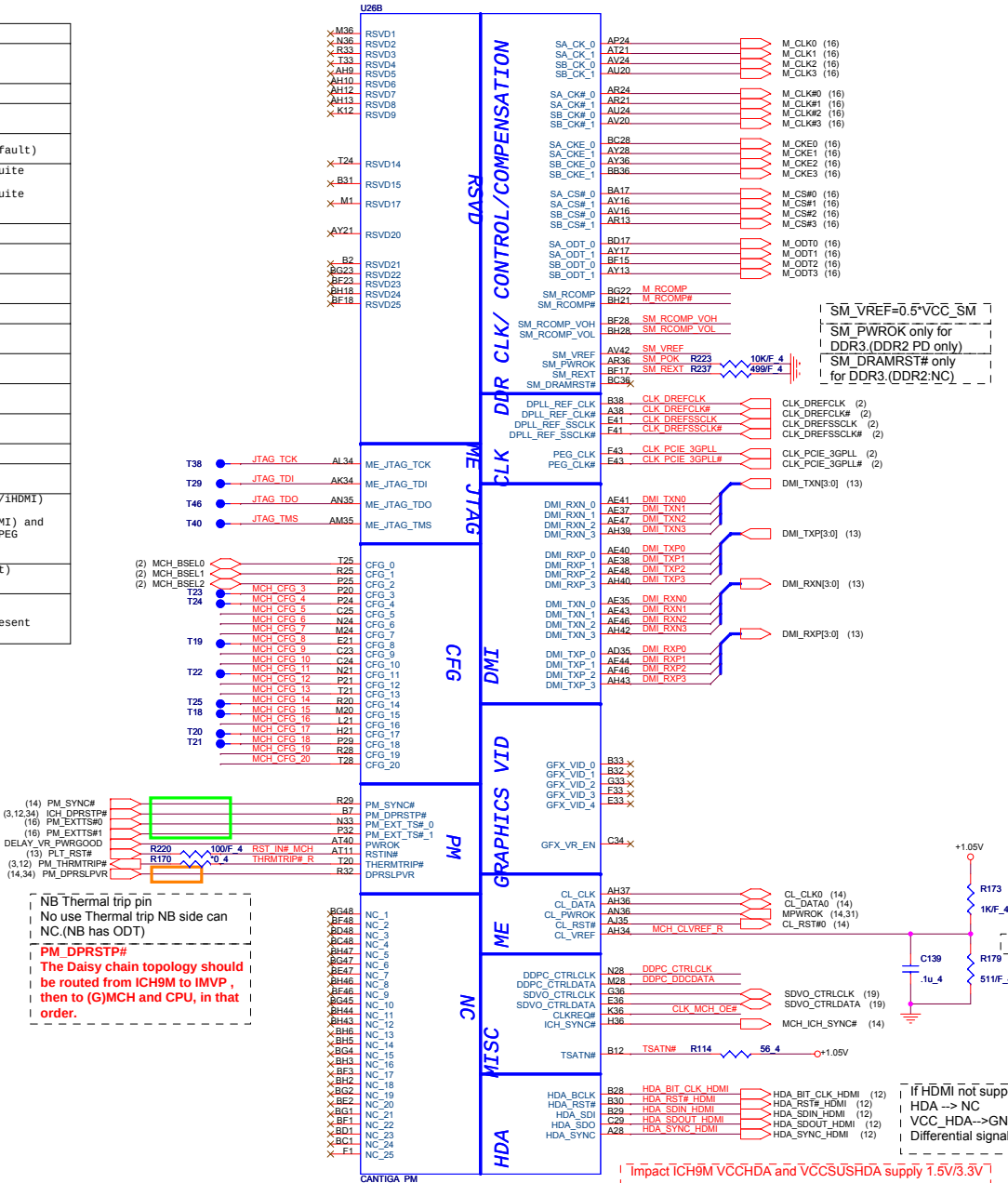
Strap table

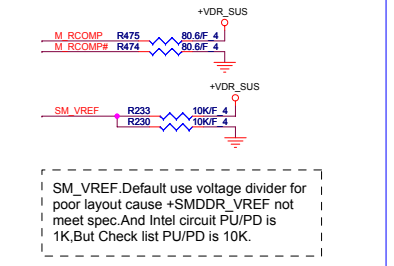
Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	000= FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	iTPM Host Interface	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is disabled(Default)
CFG7	ME TLS Confidentiality	0 = AMT Firmware will use TLS cipher suite with no confidentiality 1 = AMT Firmware will use TLS cipher suite with confidentiality(Default)
CFG8	Reserved	
CFG9	PCIE Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG10	PCIE Loopback enable	0 = Enabled 1 = Disabled (Default)
CFG11	Reserved	
CFG12	ALLZ	0 = ALLZ mode enable 1 = disable(Default)
CFG13	XOR	0 = XOR mode enable 1 = disable(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal (Default) 1 = Lanes Reversed
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display port (SDVO/DP/iHDMI) or PCIE is operational (Default) 1 = Digital Display port (SDVO/DP/iHDMI) and PCIE are operating simultaneously via PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO/HDMI Device Present(Default) 1 = SDVO/HDMI Device present
DDPC_CTRLDATA	Digital Display Present	0 = Digital display(HDMI/DP) device absent(Default) 1 = Digital display(HDMI/DP) device present

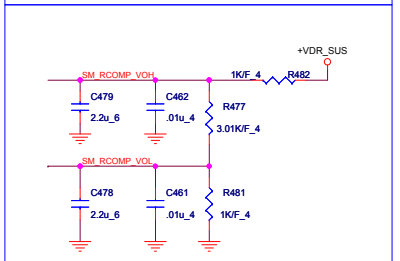
Strap pin

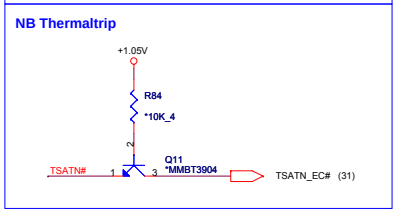












GMCH (CANTIGA)

Quanta Computer Inc.
PROJECT : ZK2
Size | Document Number | Rev
GMCH DMI | 3B
Date: Friday, June 27, 2008 | Sheet 6 of 39

IV@
EV@
SP@

IV&EV Dis/Enable setting
If LVDS no use,all signal can NC

U26C

(18) L_BKLT_CTRL
(18) INT_LVDS_BLON
R154 I@10K_4 L_CTRL_CLK
+3V
R401 I@10K_4 L_CTRL_DATA
(18) INT_LVDS_EDIDCLK
(18) INT_LVDS_EDIDDATA
(18) INT_LVDS_DIGON
R121 I@2.37K/F_4

L32 L_BKLT_CTRL
G32 L_BKLT_EN
M32 L_CTRL_CLK
M33 L_CTRL_DATA
K33 L_DDC_CLK
J33 L_DDC_DATA
M29 L_VDD_EN
C44 LVDS_IBG
B43 LVDS_VBG
E37 LVDS_VREFH
E38 LVDS_VREFL
C41 LVDSA_CLK#
C40 LVDSA_CLK
B37 LVDSB_CLK#
A37 LVDSB_CLK

(17) INT_TXLCLKOUT-
(17) INT_TXLCLKOUT+
(17) INT_TXUCLKOUT-
(17) INT_TXUCLKOUT+
INT_TXLCLKOUT-
INT_TXLCLKOUT+
INT_TXUCLKOUT-
INT_TXUCLKOUT+

(17) INT_TXLOUT0-
(17) INT_TXLOUT1-
(17) INT_TXLOUT2-
INT_TXLOUT0-
INT_TXLOUT1-
INT_TXLOUT2-
H47 LVDSA_DATA#_0
E46 LVDSA_DATA#_1
G40 LVDSA_DATA#_2
A40 LVDSA_DATA#_3

(17) INT_TXLOUT0+
(17) INT_TXLOUT1+
(17) INT_TXLOUT2+
INT_TXLOUT0+
INT_TXLOUT1+
INT_TXLOUT2+
H48 LVDSA_DATA_0
D45 LVDSA_DATA_1
F40 LVDSA_DATA_2
B40 LVDSA_DATA_3

(17) INT_TXUOUT0-
(17) INT_TXUOUT1-
(17) INT_TXUOUT2-
INT_TXUOUT0-
INT_TXUOUT1-
INT_TXUOUT2-
A41 LVDSB_DATA#_0
H38 LVDSB_DATA#_1
G37 LVDSB_DATA#_2
J37 LVDSB_DATA#_3

(17) INT_TXUOUT0+
(17) INT_TXUOUT1+
(17) INT_TXUOUT2+
INT_TXUOUT0+
INT_TXUOUT1+
INT_TXUOUT2+
B42 LVDSB_DATA_0
G38 LVDSB_DATA_1
F37 LVDSB_DATA_2
K37 LVDSB_DATA_3

LVDS

R137 75_4 INT_TV_COMP
R143 75_4 INT_TV_Y/G
R156 75_4 INT_TV_C/R
F25 TVA_DAC
H25 TVB_DAC
K25 TVC_DAC
H24 TV_RTN
C31 TV_DCONSEL_0
E32 TV_DCONSEL_1

TV

(17) INT_CRT_BLU
(17) INT_CRT_GRN
(17) INT_CRT_RED
INT_CRT_BLU E28 CRT_BLUE
INT_CRT_GRN G28 CRT_GREEN
INT_CRT_RED J28 CRT_RED
G29 CRT_IRTN

(17) INT_CRT_DDCCLK
(17) INT_CRT_DDCDAT
(17) INT_HSYNC
(17) INT_VSYNC
R416 I@30.1_4 HSYNC_G
CRTIREF E29
R415 I@30.1_4 VSYNC_G
H32 CRT_DDC_CLK
J32 CRT_DDC_DATA
J29 CRT_HSYNC
L29 CRT_VSYNC

VGA

HSYNC/VSYNC serial R place close to NB

CRTIREF pull down
for IV cantiga 1.02k ohm/F

CANTIGA_PM

PCI-EXPRESS GRAPHICS

L<0.5" , If PCIE not support
still connect to +VCC_PEG

+1.05V
T37 EXP_A_COMPX R165 49.9/F_4
T36
PEG_COMPI
PEG_COMPO

PEG_RX#_0 H44 PEG_RXN0
PEG_RX#_1 J46 PEG_RXN1
PEG_RX#_2 L44 PEG_RXN2
PEG_RX#_3 L40 PEG_RXN3
PEG_RX#_4 N41 PEG_RXN4
PEG_RX#_5 P48 PEG_RXN5
PEG_RX#_6 N44 PEG_RXN6
PEG_RX#_7 T43 PEG_RXN7
PEG_RX#_8 U43 PEG_RXN8
PEG_RX#_9 Y43 PEG_RXN9
PEG_RX#_10 Y48 PEG_RXN10
PEG_RX#_11 Y36 PEG_RXN11
PEG_RX#_12 AA43 PEG_RXN12
PEG_RX#_13 AD37 PEG_RXN13
PEG_RX#_14 AC47 PEG_RXN14
PEG_RX#_15 AD39 PEG_RXN15
PEG_RXN[15:0] (17)

Can support reversal routing.If CFG9=1, PCI Express is normal operation. If CFG9=0, then PEG_TXP0 becomes PEG_TXP15, PEG_TXP1 becomes PEG_TXP14, PEG_TXP2 becomes PEG_TXP13, etc. similarly for PEG_RXP[15:0] and PEG_RXN[15:0]

PEG_RX_0 H43 PEG_RXP0
PEG_RX_1 J44 PEG_RXP1
PEG_RX_2 L43 PEG_RXP2
PEG_RX_3 L41 PEG_RXP3
PEG_RX_4 N40 PEG_RXP4
PEG_RX_5 P47 PEG_RXP5
PEG_RX_6 N43 PEG_RXP6
PEG_RX_7 T42 PEG_RXP7
PEG_RX_8 U42 PEG_RXP8
PEG_RX_9 Y42 PEG_RXP9
PEG_RX_10 W47 PEG_RXP10
PEG_RX_11 Y37 PEG_RXP11
PEG_RX_12 AA42 PEG_RXP12
PEG_RX_13 AD36 PEG_RXP13
PEG_RX_14 AC48 PEG_RXP14
PEG_RX_15 AD40 PEG_RXP15
PEG_RXP[15:0] (17)

PEG_TX#_0 J41 C_PEG_TXN0 C88 .1u_4 PEG_TXN0
PEG_TX#_1 M46 C_PEG_TXN1 C80 .1u_4 PEG_TXN1
PEG_TX#_2 M47 C_PEG_TXN2 C90 .1u_4 PEG_TXN2
PEG_TX#_3 M40 C_PEG_TXN3 C100 .1u_4 PEG_TXN3
PEG_TX#_4 M42 C_PEG_TXN4 C102 *E@.1u_4 PEG_TXN4
PEG_TX#_5 R48 C_PEG_TXN5 C107 *E@.1u_4 PEG_TXN5
PEG_TX#_6 N38 C_PEG_TXN6 C111 *E@.1u_4 PEG_TXN6
PEG_TX#_7 T40 C_PEG_TXN7 C122 *E@.1u_4 PEG_TXN7
PEG_TX#_8 U37 C_PEG_TXN8 C123 *E@.1u_4 PEG_TXN8
PEG_TX#_9 U40 C_PEG_TXN9 C142 *E@.1u_4 PEG_TXN9
PEG_TX#_10 Y40 C_PEG_TXN10 C152 *E@.1u_4 PEG_TXN10
PEG_TX#_11 AA46 C_PEG_TXN11 C134 *E@.1u_4 PEG_TXN11
PEG_TX#_12 AA37 C_PEG_TXN12 C155 *E@.1u_4 PEG_TXN12
PEG_TX#_13 AA40 C_PEG_TXN13 C176 *E@.1u_4 PEG_TXN13
PEG_TX#_14 AD43 C_PEG_TXN14 C216 *E@.1u_4 PEG_TXN14
PEG_TX#_15 AC46 C_PEG_TXN15 C172 *E@.1u_4 PEG_TXN15
PEG_TXN[15:0] (17)

PEG_TX_0 J42 C_PEG_TXP0 C89 .1u_4 PEG_TXP0
PEG_TX_1 L46 C_PEG_TXP1 C75 .1u_4 PEG_TXP1
PEG_TX_2 M48 C_PEG_TXP2 C82 .1u_4 PEG_TXP2
PEG_TX_3 M39 C_PEG_TXP3 C94 .1u_4 PEG_TXP3
PEG_TX_4 M43 C_PEG_TXP4 C101 *E@.1u_4 PEG_TXP4
PEG_TX_5 R47 C_PEG_TXP5 C105 *E@.1u_4 PEG_TXP5
PEG_TX_6 N37 C_PEG_TXP6 C108 *E@.1u_4 PEG_TXP6
PEG_TX_7 T39 C_PEG_TXP7 C115 *E@.1u_4 PEG_TXP7
PEG_TX_8 U36 C_PEG_TXP8 C120 *E@.1u_4 PEG_TXP8
PEG_TX_9 U39 C_PEG_TXP9 C138 *E@.1u_4 PEG_TXP9
PEG_TX_10 Y39 C_PEG_TXP10 C151 *E@.1u_4 PEG_TXP10
PEG_TX_11 Y46 C_PEG_TXP11 C128 *E@.1u_4 PEG_TXP11
PEG_TX_12 AA36 C_PEG_TXP12 C148 *E@.1u_4 PEG_TXP12
PEG_TX_13 AA39 C_PEG_TXP13 C175 *E@.1u_4 PEG_TXP13
PEG_TX_14 AD42 C_PEG_TXP14 C219 *E@.1u_4 PEG_TXP14
PEG_TX_15 AD46 C_PEG_TXP15 C171 *E@.1u_4 PEG_TXP15
PEG_TXP[15:0] (17)

MXM STUFFED.
HSYNC_G
VSYNC_G
R417 *E@0_4
R414 *E@0_4

IV&EV Dis/Enable setting
<5/31>Montevina_Schematics_Checklist_Rev0_8
a)For TVOUT Disabled, TV_DCONSEL[1:0] Connect to GND. But design guide Rev0.7 show NC.What is correct.
b)For CRT DAC Disable, CRT_DDC_CLK, CRT_DDC_DATA . CRT_HSYNC, CRT_VSYNCThese signals should be connected to GND. But design guide Rev0.7 show NC, Intel suggest follow Design guide.

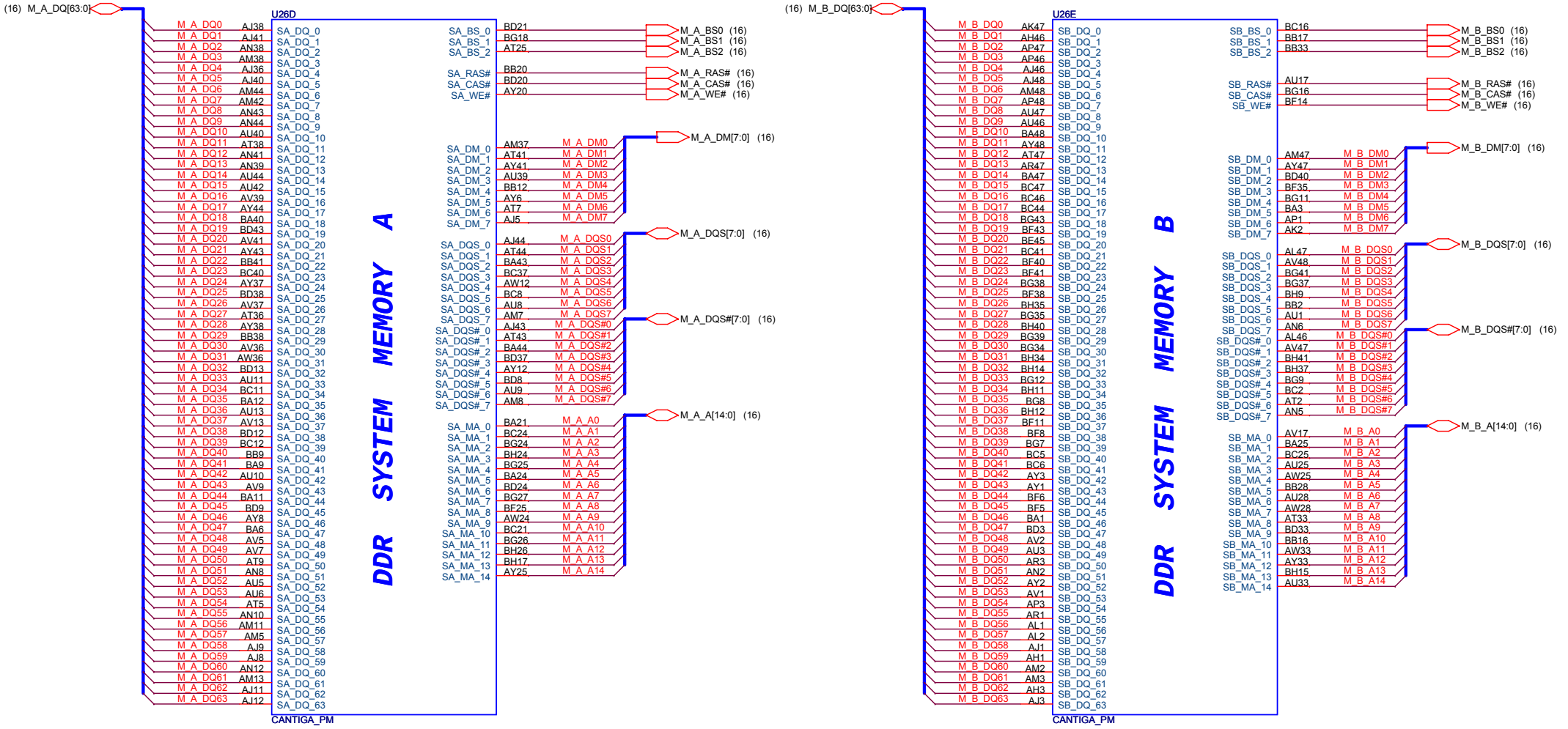
<check list>	<check list>
For EV@	For IV@
CRT R/G/B 0ohm to GND	CRT R/G/B 150ohm to GND
CRTIREF 0ohm to GND	CRTIREF 1.02Kohm to GND

CRTIREF
For IV: 1.02Kohm
For EV:0ohm
R115 SP@1.02K/F_4 CRTIREF

SP@
CRT_R/G/B
For IV: 150ohm
For EV:0ohm
R127 SP@150_4 INT_CRT_BLU
R138 SP@150_4 INT_CRT_GRN
R146 SP@150_4 INT_CRT_RED

Quanta Computer Inc.
PROJECT : ZK2

Size	Document Number	Rev
	GMCH VGA	3B
Date: Wednesday, July 09, 2008	Sheet 7 of 39	



GMCH (CANTIGA)

Quanta Computer Inc.
PROJECT : ZK2

Size	Document Number	Rev
	GMCH DDRII	3B
Date: Friday, June 27, 2008	Sheet 8 of 39	

IV@

SP@

Power consumption reference to Intel
644135 Cantiga chipset EDS Volume1.
Section 10

GM TDP 10.5~12W
GS TDP 7~8W
PM TDP 7W

Intel check list(Rev 0.8)
No description for VCC_SM bulk CAP
Intel CRB(Rev 0.7)
330U*1 Reserve near to power
330U*1 near to NB

Intel check list(Rev 0.8)
270U*1 near to power(+V1.05M).
270U*2 near to NB
Intel CRB(Rev 0.7)
270U*3 near to power(+V1.05M).
270U*1 near to NB
ESR=12m ohm

+VDR_SUS

C464 22u_8 C465 22u_8 C191 .1u_4 C477 330u_7343

U26G

VCC_SM(1.8V)
DDR2(800M)
3000mA_S0 , 1mA_S3
DDR2(667M) : 2600mA_S0
DDR3(1067M) : 4140mA_S0

VCC SM POWER

AP33 AN33 BH32 BG32 BF32 BD32 BC32 BB32 BA32 AY32 AW32 AV32 AU32 AT32 AR32 AP32 AN32 BH31 BG31 BF31 BG30 BH29 BG29 BF29 BD29 BC29 BB29 BA29 AY29 AW29 AV29 AU29 AT29 AR29 AP29 — VCC_SM_1 … VCC_SM_35

BA36 BB24 BD16 BB21 AW16 AW13 AT13 — VCC_SM_36/NC … VCC_SM_42/NC

+1.05V_AXG

1.05V
Graphics core
VCC_AXG
VCC_AXG_NCTF
6326.84mA

Y26 AE25 AB25 AA25 AE24 AC24 AA24 Y24 AE23 AC23 AB23 AA23 AJ21 AG21 AE21 AC21 AA21 Y21 AH20 AF20 AE20 AC20 AB20 AA20 T17 T16 AM15 AL15 AE15 AJ15 AH15 AG15 AF15 AB15 AA15 Y15 V15 U15 AN14 AM14 U14 T14 — VCC_AXG_1 … VCC_AXG_42

VCC GFX

VCC GFX NCTF

W28 V28 W26 V26 W25 V25 W24 V24 W23 V23 AM21 AL21 AK21 W21 V21 U21 AM20 AK20 W20 U20 AM19 AL19 AK19 AJ19 AH19 AG19 AF19 AE19 AB19 AA19 Y19 W19 V19 U19 AM17 AK17 AH17 AG17 AF17 AE17 AC17 AB17 Y17 W17 V17 AM16 AL16 AK16 AJ16 AH16 AG16 AF16 AE16 AC16 AB16 AA16 Y16 W16 V16 U16 — VCC_AXG_NCTF_1 … VCC_AXG_NCTF_60

Voltage regulator is shared between
the Graphics Core Rail,
VCCA_HPLL,VCCA_MPLL,VCCA_PEG_PLLVCCD_PEG_PLL,
VCCA_SM_CK, VCCA_DPLLA, VCCA_DPLLB, VCCD_HPLL,
VCCA_SM, VCC_AXF

+1.05V_AXG

IV@ R197 I@10/F_4 R191 I@10/F_4

AJ14 AH14 — VCC_AXG_SENSE VSS_AXG_SENSE

1. Route VCC_AXG_SENSE and VSS_AXG_SENSE differentially
2. VCC_AXG_SENSE PU to +VGFX_CORE_INT with 10ohm
and VSS_AXG_SENSE PD with 10ohm for Intel suggest

CANTIGA_PM

VCC SM LF

VCC_SM_LF1 … VCC_SM_LF7 — AV44 BA37 AM40 AV21 AY5 AM10 BB13

1.8V
Internal connect to power

C227 1u_4 C185 .1u_4 C211 .22u_4 C204 .22u_4 C184 .47u_4 C218 1u_4 C208 1u_4

+1.05V

C177 .1u_4 C166 .22u_4 C167 .22u_4 C143 22u_8 C418 330u_7343

Place close to
the GMCH

U26F

AG34 AC34 AB34 AA34 Y34 V34 U34 AM33 AK33 AJ33 AG33 AF33 — VCC_1 … VCC_12

AE33 AC33 AA33 Y33 W33 V33 U33 AH28 AF28 AC28 AA28 AJ26 AG26 AE26 AC26 AH25 AG25 AF25 AG24 AJ23 AH23 AF23 — VCC_13 … VCC_34

T32 — VCC_35

VCC CORE

POWER

VCC NCTF

AM32 AJ32 AK32 AJ32 AH32 AG32 AE32 AC32 AA32 Y32 W32 U32 AM30 AL30 AK30 AH30 AG30 AF30 AE30 AC30 AB30 AA30 Y30 W30 V30 U30 AL29 AK29 AJ29 AH29 AG29 AE29 AC29 AA29 Y29 W29 V29 AL28 AK28 AL26 AK26 AK25 AK24 AK23 — VCC_NCTF_1 … VCC_NCTF_44

VCC
VCC_NCTF
1210.34mA_EV
1930.4mA_IV
ME Engine
508.12mA
Total Max=2438.52mA

+1.05V_AXG

IV@ R172 I@0_8 R435 I@0_8 R449 I@0_8

IV&EV Dis/Enable setting
Design guide(Table 72)
For INT VGA diasble.VCC_AXG power can connect to GND

+C444 I@330u_7343 +C454 I@330u_7343 C159 I@.47u_4 C186 SP@1u_6 C141 I@10u_8 C133 I@22u_8 C137 I@.1u_4 C193 I@.1u_4 C130 I@.1u_4

SP@

SP@:IV Sutff 1uf
EVstuff 0 ohm

Place close to the GMCH

Cavity Capacitors

Intel check list(Rev 0.8)
220U*2 near to NB(ESR=15m ohm)
Intel CRB(Rev 0.7)
270U*4 near to power(+V1.05S).
330U*2 near to NB

CANTIGA_PM

GMCH (CANTIGA)

Quanta Computer Inc.
PROJECT : ZK2

Size	Document Number	Rev
	GMCH VCC,NCTF	3B

Date: Friday, June 27, 2008 Sheet 9 of 39

Power consumption reference to Intel
Cantiga chipset EDS Volume1. Section 10

IV@
EV@
SP@

External Graphics
(GMCH Integrated Graphics Disable)

VCCSYNC_CRT	GND
VCCA_CRT_DAC	GND
VCCD_LVDS	GND
VCC_TX_LVDS	GND
VCCA_LVDS	GND
VCCA_TVDAC	GND
VCCD_QDAC	GND
VCCA_DAC_BG	GND
VCC_AXG	GND
VCC_AXG_NCTF	GND

IV&EV Dis/Enable setting

+3V_CRT_TV_DAC R397 I@0_6 +3V_VCCA_CRT_DAC
C386 I@.1u_4 C387 SP@.01u_4 C393 I@10u_8
SP@:INT use 0.01U EXT use 0 ohm

R403 I@0_6 +3V_A_DAC_BG
C398 I@.1u_4 C392 SP@.01u_4 C665 I@10u_8
3.3V 73mA

3.3V 5mA

USE same GND plane

VCCA_DPLLA/B always keep to +1.05V
(If no use IV dynamic core power)

1210 10UH, 10%
0.45A DCR_max = 0.39

+1.05V L28 I@10uh_8
C378 I@220u_7343 ESR=15 m C382 SP@.1u_4
1.05V 64.8mA for DPLL_A/B

1210 10UH, 10%
0.45A DCR_max = 0.39

+1.05V L33 I@10uh_8
C399 I@220u_7343 C403 SP@.1u_4
ESR=15 m
1.05V 24mA

+1.05V R202 0_6
C169 4.7u_6 C164 .1u_4
1.05V 139.2mA

L16 BLM18PG181SN1D_6
1210 0.1uH, 20%, 1A,
DCR_max=0.078Ω

+1.05VM_MPLL_RC R182 0.5/F_6
C168 22u_8 C160 .1u_4

3.3V
24.15mA for VCCA_TVA_DAC
39.48mA for VCCA_TVB_DAC
24.15mA for VCCA_TVC_DAC
Total 87.78mA

FB 180@100 MHz, 25% 1.5A
DCR_max=90 m
3.3V 79mA
+3V L32 I@BLM18PG181SN1D_6
C384 I@10u_8 C391 I@.1u_4 C397 SP@.01u_4
IV&EV Dis/Enable setting
SP@:INT use 0.01U EXT use 0 ohm

CRB no 10U
Check list need min 10U~100U for VCCA_TV_DAC
1.5V 50mA

+1.5V R389 I@0_6
C76 SP@.1u_4
SP@:INT use 0.1U EXT use 0 ohm

VCCD_TVDAC always keep 0.1U/0.022U/10U to +1.5V
1.5V 35mA
+1.5V R112 0_6
C99 .1u_4 C93 .01u/25V_4

1.5V 48.363mA for CRT
5mA for TV

FB 180@100 MHz, 25% 1.5A
DCR_max=90 m
1.5V 0.5mA
L27 I@BLM18PG181SN1D_6
C380 10u_8 C92 I@.1u_4 C84 SP@.01u_4
CRB no 10U
Check list need min 10U~100U
for VCCA_QDAC
SP@:INT use 0.01U EXT use 0 ohm
IV&EV Dis/Enable setting

FB 220 @100 MHz, 25%, 2A
1.05V 50mA
+1.05V L34 BLM18PG181SN1D_6
C415 .1u_4 C434 .1u_4
+1.05VM_PEGPLL_RC R430 1/F_4
C431 10u_6
ESR=60m ohm

+VDR_SUS R162 I@0_6
1.8V 60.31mA
IV&EV Dis/Enable setting
+1.8VSUS_DLVDS
SP@:INT use 1 U EXT use 0 ohm
C114 SP@1u_4

VCCD_QDAC share to TV and CRT
+1.5V_QDAC L28
+1.05V R212 0_6
1.05V 157.2mA
C181 .1u_4
+1.05VM_MCH_PLL2 AF1
+1.05VM_PEGPLL AA47
VCCD_TVDAC M25
VCCD_QDAC
VCCD_HPLL
VCCD_PEG_PLL
VCCD_LVDS_1 M38
VCCD_LVDS_2 L37

+1.05VM_DPLLA F47
+1.05VM_DPLLB L48
+1.05VM_HPLL AD1
+1.05VM_MPLL AE1
+1.8VSUS_TXLVDS J48
VCCA_LVDS J47
VSSA_LVDS

1.8V 13.2mA
C390 I@1000p/50V_4
1.5V 414uA

+1.5V R453 0_8 +VCCA_PEG_BG AD48
C442 .1u_4
1.05V 50mA
+1.05VM_PEGPLL AA48
VCCA_PEG_PLL
+1.25V for Teenah use(100mA)

3.9 nH, 0.2 nH, 1A
DCR_max=32 m
1.05V DDR2-800 720mA
+1.05V R192 0_6 +1.05VM_A_SM
C195 22u_8 C194 4.7u_6 C187 1u_4

1.05V DDR2-800 26mA
+1.05V R193 0_6 +1.05VM_A_SM_CK
C188 *2.2u_6 C182 22u_8 C189 .1u_4
CRB : 0 ohm
Check list : 2.2nH

+3V_CRT_TV_DAC B24
VCCA_TV_DAC_1
VCCA_TV_DAC_2 A24
VCC_HDA A32
+1.5V_TVDAC

VCCA_CRT_DAC_1 R27
VCCA_CRT_DAC_2 A26
VCCA_DAC_BG A25
VSSA_DAC_BG B25
VCCA_DPLLA F48
VCCA_DPLLB L48
VCCA_HPLL AD1
VCCA_MPLL AE1
VCCA_LVDS J48
VSSA_LVDS J47
VCCA_PEG_BG AD48
VCCA_PEG_PLL AA48
VCCA_SM_1 AR20
VCCA_SM_2 AP20
VCCA_SM_3 AN20
VCCA_SM_4 AR17
VCCA_SM_5 AP17
VCCA_SM_6 AN17
VCCA_SM_7 AT16
VCCA_SM_8 AR16
VCCA_SM_9 AP16
VCCA_SM_CK_1 AP28
VCCA_SM_CK_2 AN28
VCCA_SM_CK_3 AP25
VCCA_SM_CK_4 AN25
VCCA_SM_CK_5 AN24
VCCA_SM_CK_NCTF_1 AM28
VCCA_SM_CK_NCTF_2 AM26
VCCA_SM_CK_NCTF_3 AM25
VCCA_SM_CK_NCTF_4 AL25
VCCA_SM_CK_NCTF_5 AM24
VCCA_SM_CK_NCTF_6 AL24
VCCA_SM_CK_NCTF_7 AM23
VCCA_SM_CK_NCTF_8 AL23

CRT PLL LVDS PEG SM A CK TV HDA TV/CRT LVDS

U26H
CANTIGA_PM

POWER

VTT
VTT_1 U13
VTT_2 T13
VTT_3 U12
VTT_4 T12
VTT_5 U11
VTT_6 T11
VTT_7 U10
VTT_8 T10
VTT_9 U9
VTT_10 T9
VTT_11 U8
VTT_12 T8
VTT_13 U7
VTT_14 T7
VTT_15 U6
VTT_16 T6
VTT_17 U5
VTT_18 T5
VTT_19 V3
VTT_20 U3
VTT_21 V2
VTT_22 U2
VTT_23 T2
VTT_24 V1
VTT_25 U1

1.05V FSB-1067 852mA
+1.05V
C149 .47u_4 C132 2.2u_6 C129 4.7u_6 C126 4.7u_6 C383 330u_7343
ESR= 12m ohm

Check list : 0.1UH
CRB : 0 ohm
1210 0.1 ?H, 20% 1A
DCR max = 78 m

1.05V 321.35mA
+1.05VM_AXF
C396 1u_4 C389 *10u_8
ESR = 60 m
L31 0.1uh_8 +1.05V

1.8V DDR2-800 124mA
0805 1UH , Rdc = 0.14 - 0.26.
Max rated current = 220 mA
+1.8VSUS_VCC_SM_CK
L37 1uh_8 +VDR_SUS
C463 .1u_4
1/F_4 R473 +1.8VSUS_SMCK_RC C466 10u_6

IV&EV Dis/Enable setting
1.8V 118.8mA
0805 100 nH, DCR=160 m
+1.8VSUS_TXLVDS
L30 I@0.1uh_6 +VDR_SUS
SP@:INT use 1000pf EXT use 0 ohm
C385 SP@1000p/50V_4 C388 I@22u_8

VCC_AXF_1 B22
VCC_AXF_2 B21
VCC_AXF_3 A21
AXF

VCC_SM_CK_1 BF21
VCC_SM_CK_2 BH20
VCC_SM_CK_3 BG20
VCC_SM_CK_4 BF20
SM CK

3.3V 105.3mA
+3V
R384 10_4 +1.05V_SD D22 1 2 CH751 +1.05V
C83 .1u_4

VCC_TX_LVDS K47
VCC_HV_1 C35
VCC_HV_2 B35
VCC_HV_3 A35
HV

1.05V 1782mA
+1.05V
C449 4.7u_6 C453 22u_8 C374 220u_7343

VCC_PEG_1 V48
VCC_PEG_2 U48
VCC_PEG_3 V47
VCC_PEG_4 U47
VCC_PEG_5 U46
PEG

1.05V 456mA
C447 .1u_4

VCC_DMI_1 AH48
VCC_DMI_2 AF48
VCC_DMI_3 AH47
VCC_DMI_4 AG47
DMI

VTTLF1 A8
VTTLF2 L1
VTTLF3 AB2
VTTLF
C429 .47u_4 C406 .47u_4 C395 .47u_4

1.05V
Internal connect to power

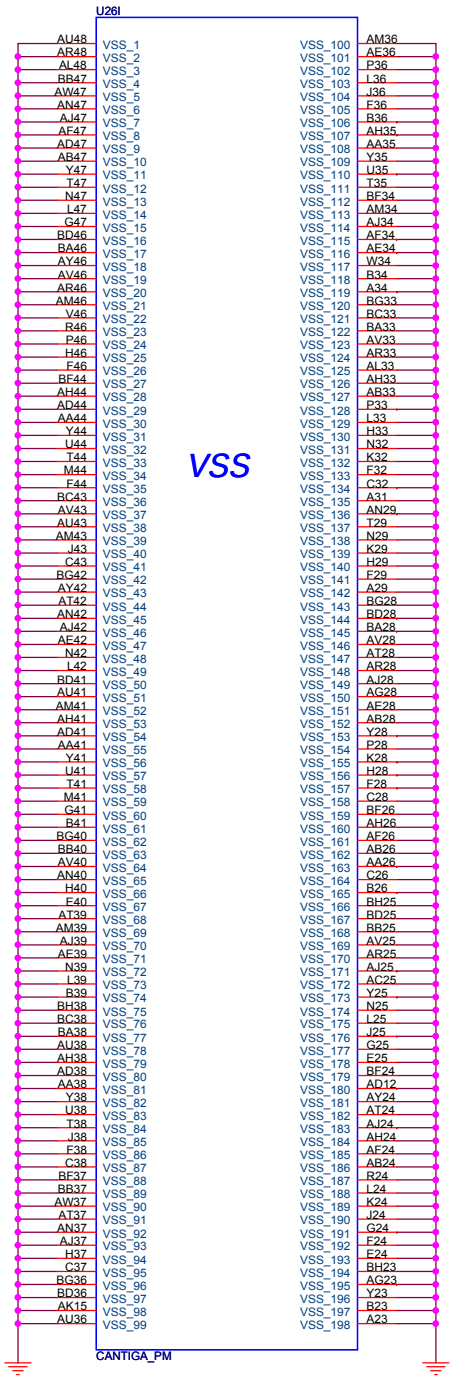
Power Net Name	Cantiga(V)
VCC_AXG_# VCC_AXG_NCTF_#	1.05V
VCCA_PEG_BG	1.5V
VCCA_DPLLA	1.05V
VCCA_DPLLB	1.05V
VCCA_SM_#	1.05V
VCCA_HPLL	1.05V
VCCA_MPLL	1.05V
VCCA_SM_CK_#	1.05V
VCCA_PEG_PLL	1.05V
VCC_AXF_#	1.05V
VCCD_HPLL	1.05V
VCCD_PEG_PLL	1.05V

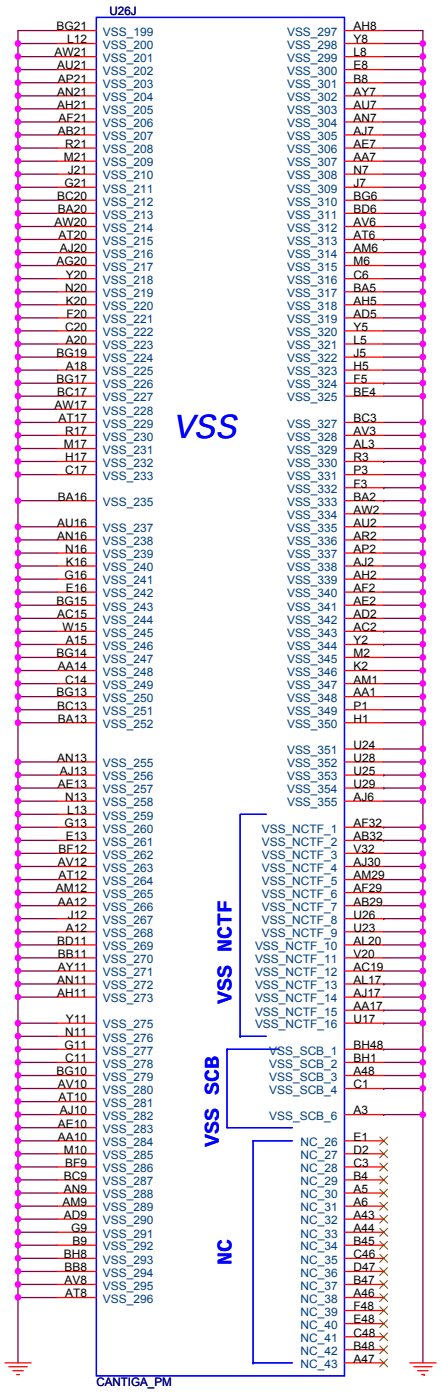
GMCH (CANTIGA)

Quanta Computer Inc.
PROJECT : ZK2

Size	Document Number	Rev
	GMCH POWER	3B

Date: Friday, June 27, 2008 Sheet 10 of 39





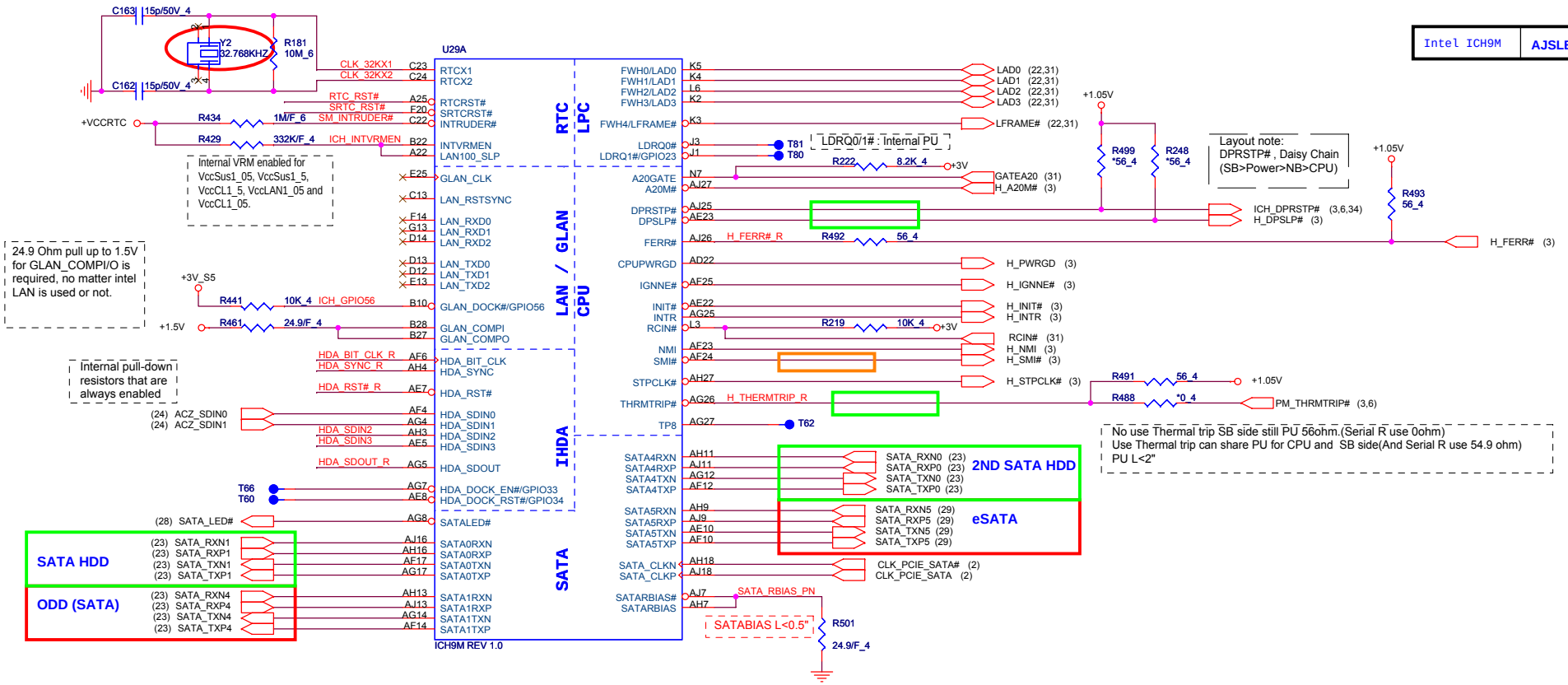
GMCH (CANTIGA)

Quanta Computer Inc.		
PROJECT : ZK2		
Size	Document Number: GMCH VSS	Rev: 3B
Date: Friday, June 27, 2008	Sheet 11 of 39	

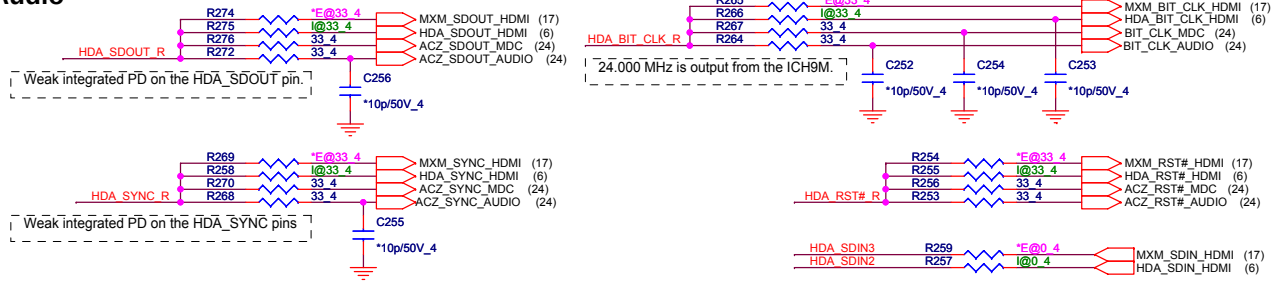
ICH9M

IV@

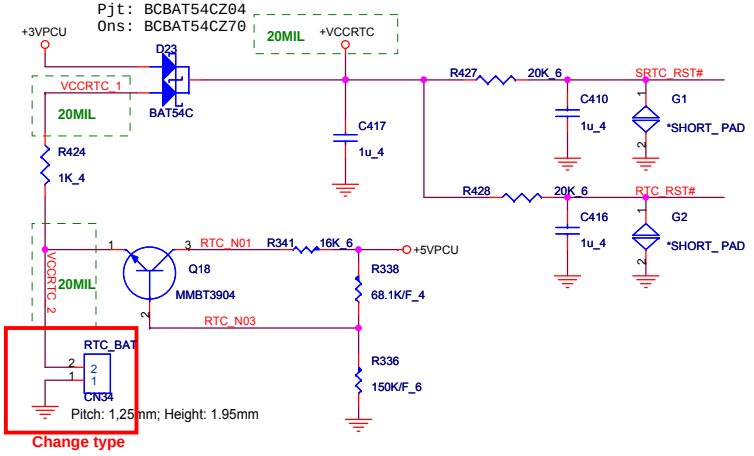
EV@



HD Audio



RTC



South Bridge Strap Pin (1/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_DOCK_EN/ GPIO33	Flash Descriptor Security Override Strap	PWROK	0 = The Flash Descriptor Security will be overridden. 1 = The security measures defined in the Flash Descriptor will be in effect	This strap should only be enabled in manufacturing environments using an external pull-up resistor.
SATALED#	PCI Express Lane Reversal (Lanes 1-4)	PWROK	Internal PU	
TP3	XOR Chain Entrance	PWROK	ICH_TP3 / HDA_SDOUT: 0/0 RSVD; 0/1 Enter XOR Chain; 1/0 Normal opration(Default); 1/1 Set PCIE port config bit 1	(14) ICH_TP3 — ICH_TP3 — R451 *1K_4
HDA_SDOUT	XOR Chain Entrance /PCI Express* Port Config 1 bit 1(Port 1-4)	PWROK		HDA_SDOUT_R — R273 *1K_4 — +3V

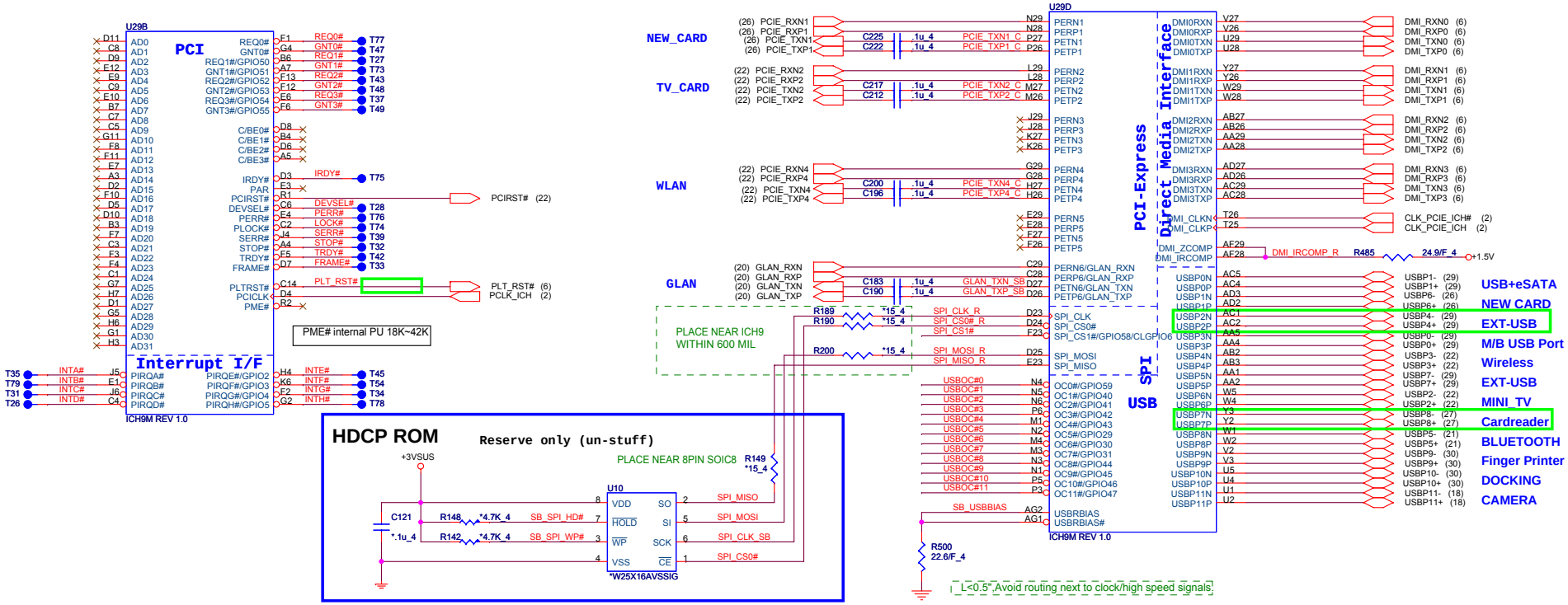
Intel ICH9M	AJSLB8Q0T03

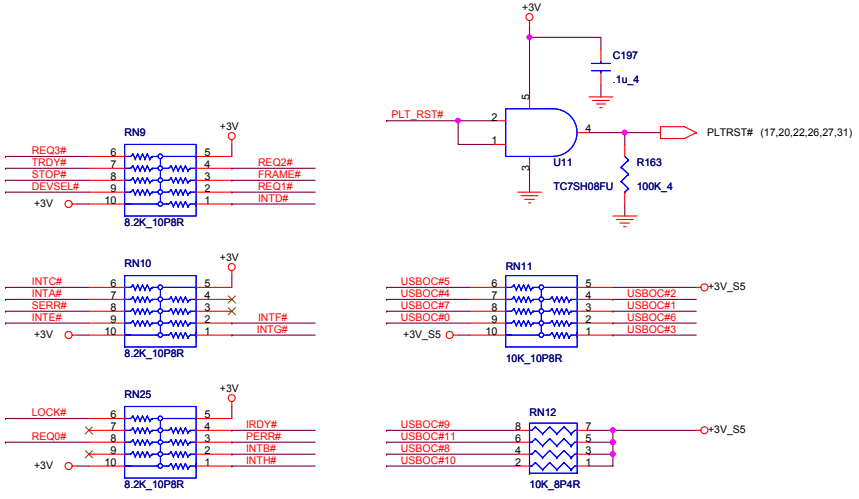
Quanta Computer Inc.

PROJECT : ZK2

Size	Document Number	Rev
	ICH9M HOST	3B
Date: Wednesday, July 09, 2008	Sheet 12 of 39	

ICH9M

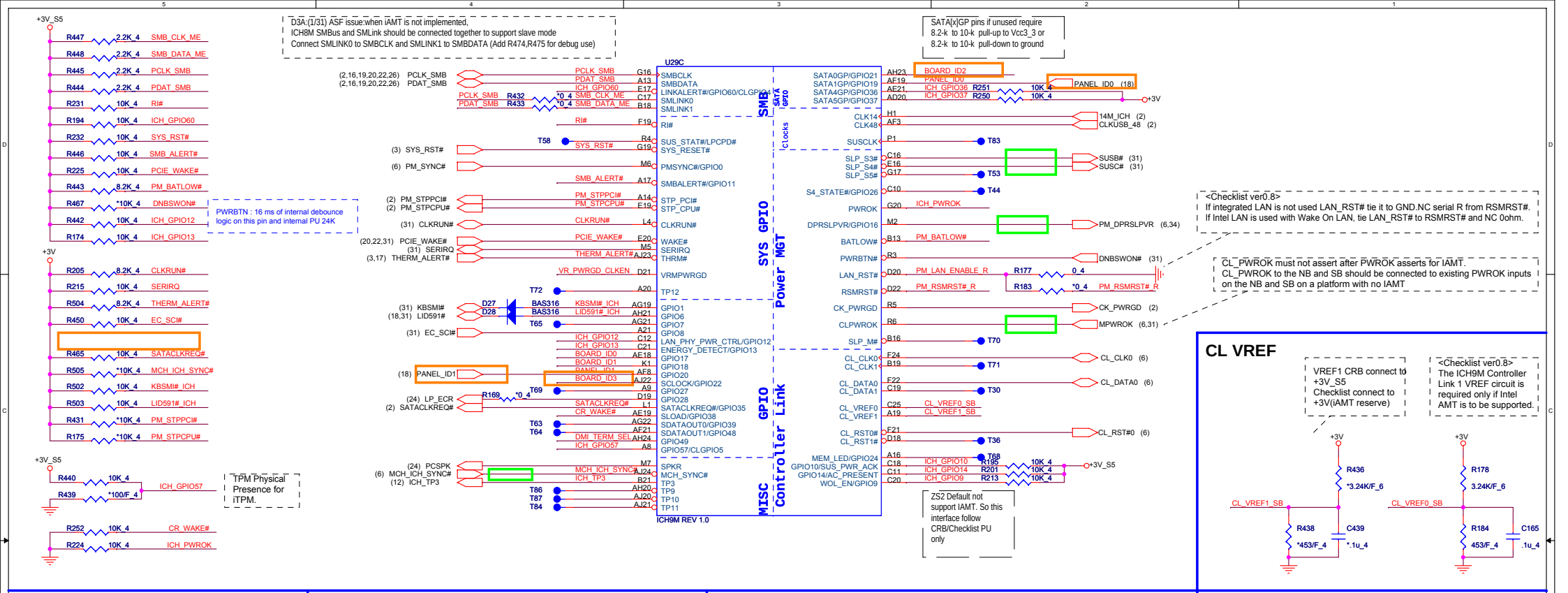




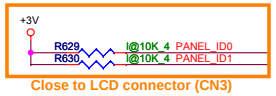
South Bridge Strap Pin (2/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0	
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default	
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default	
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default	GNT3# R204 *1K_4
SPI_MOSI	Integrated TPM Enable	CLPWROK	0 = INT TPM disable(Default) 1 = INT TPM enable	SPI_MOSI R199 *10K_4 +3V_S5
GNT0#	Boot BIOS Selection 0	PWROK	PCI_GNT#0 / SPI_CS#1 / Boot Location 0 / 1 / SPI	GNT0# R221 *1K_4
SPI_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK	1 / 0 / PCI 1 / 1 / **LPC(Default)**	SPI_CS1# R216 *1K_4

Quanta Computer Inc.
PROJECT : ZK2
Size | Document Number: ICH9M PCIE / PCI / USB | Rev 3B
Date: Friday, June 27, 2008 | Sheet 13 of 39

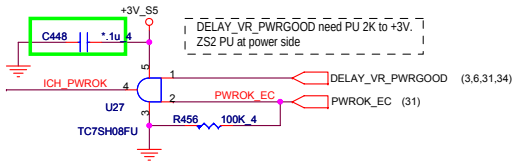


Panel ID (UMA only)

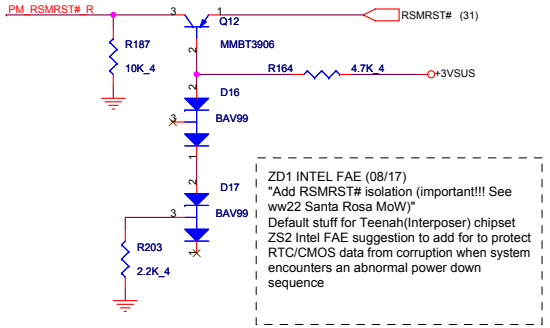


P_ID1 (GPIO20)	P_ID0 (GPIO19)	Resolution
0	0	1366x768
0	1	1920x1080
1	0	Reserved
1	1	Reserved

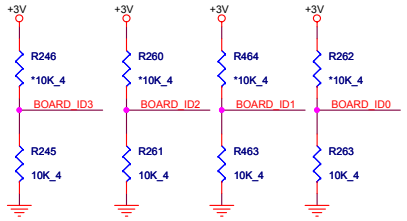
ICH PWROK



Resume RST



M/B ID

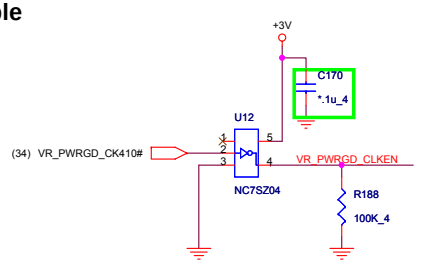


Board ID	ID3	ID2	ID1	ID0
default	0	0	0	0
	0	0	0	1
	0	0	1	0
	0	0	1	1
	0	1	0	0

South Bridge Strap Pin (3/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
GPIO20	Reserved	PWROK		
SPKR	No Reboot	PWROK	0 = Default 1 = No Reboot mode	PCSPK R236 *1K_4 +3V
GPIO49	DMI Termination Voltage	PWROK	0 = for desktop applications 1 = for mobile applications Internal PU	DMI_TERM_SEL R507 *1K_4

CLK Enable



Quanta Computer Inc.
PROJECT : ZK2
Size | Document Number | Rev 3B
ICH9M GPIO
Date: Friday, June 27, 2008 | Sheet 14 of 39

ICH9M

IV@

EV@

Power consumption reference to Intel ICH9 Family EDS Rev 1.6

PER INTEL SUGGESTION: CHANGE TO 100OHM & 1UF

2~3.456v 3.6uA_G3

5V 2mA

5V S0:2mA S3/4/5:1mA

1.5V 646mA

330 Ohms@ 100 MHz , 0805

1.5V 47mA

VCC1_5_A 1.5V 1342mA

1.5V 11mA

1.05V , Powered by VCC1_05 in S0

3.3V S0:19mA S3/4/5:78mA

If use SB MAC for LAN function. And support wake up need connect to relation power.

1.5V 23mA

1.5V 80mA

3.3V 1mA

1.05V 1634mA

1.5V 23mA

1.05V 50mA

1.05V 2mA

3.3V 308mA

3.3V S0:212mA S3/4/5:53mA

3.3V S0:19mA S3/4/5:73mA

If use SB MAC for LAN function. And support wake up need connect to relation power.

VCCUS1_05 power by VCC1_05 in S0 / VCCSUS3_3 in S3/S4/S5

VCCUS1_5 power by VCC1_5_A in S0 / VCCSUS3_3 in S3/S4/S5

VCCCL1_05 power by VCC1_05_A in S0

VCCCL1_5 power by VCC1_5_A in S0

Impact ICH9M VCCHDA and VCCSUSHDA supply 1.5V/3.3V

Support INT HDMI HDA interface. These power only support 1.5V.Device must to meet.

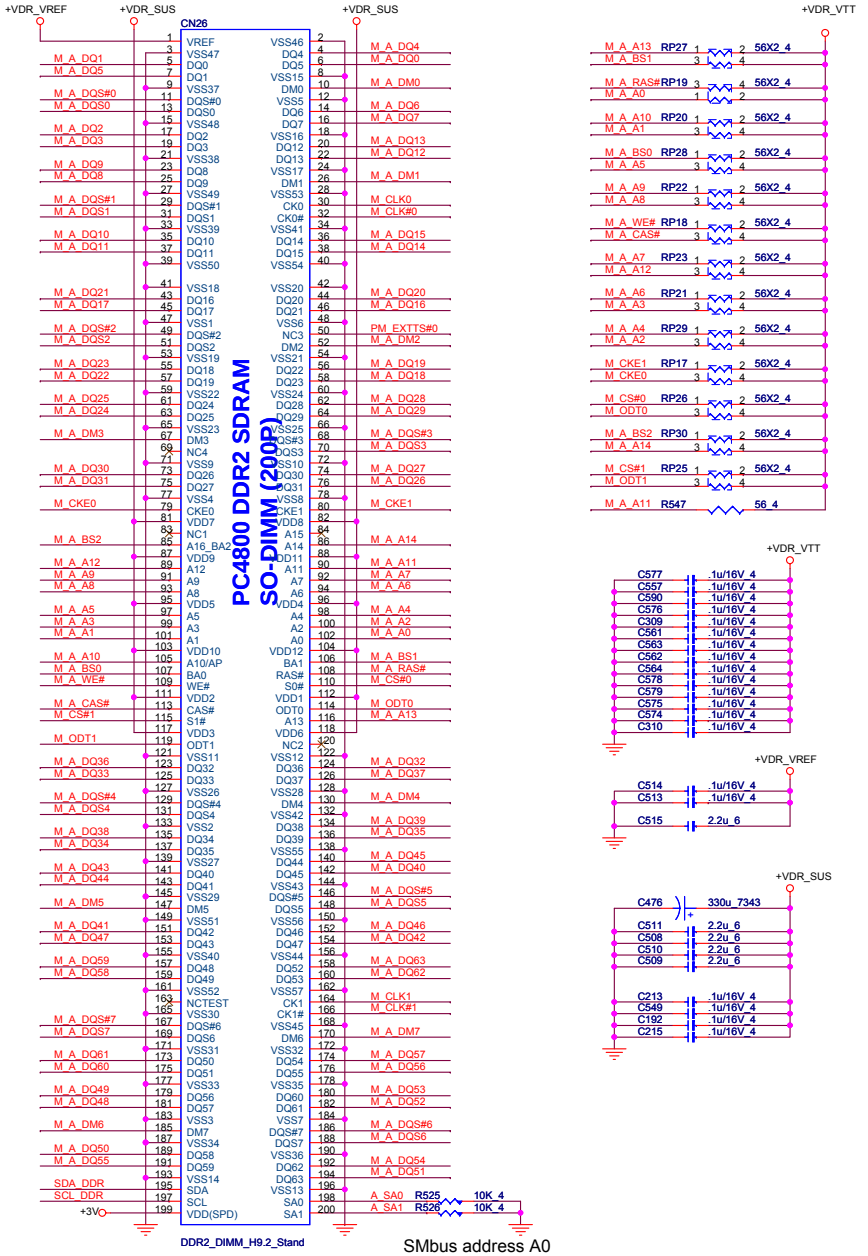
1.5v / 3.3V 11mA

1.5v / 3.3V S0:11mA S3/4/5:1mA

NOTE:
If (G)MCH's HD Audio signals are connected to ICH9M for iHDMI, VCCHDA and VCCSUSHDA on ICH9M should be only on 1.5V. These power pins on ICH9M can be supplied with 3.3V if and only if (G)MCH's HDA is not connected to ICH9M. Consequently, only 1.5V audio/modem codecs can be used on the platform.

Quanta Computer Inc.		
PROJECT : ZK2		
Size	Document Number	Rev
	ICH9 POWER	3B
Date: Friday, June 27, 2008	Sheet 15 of 39	

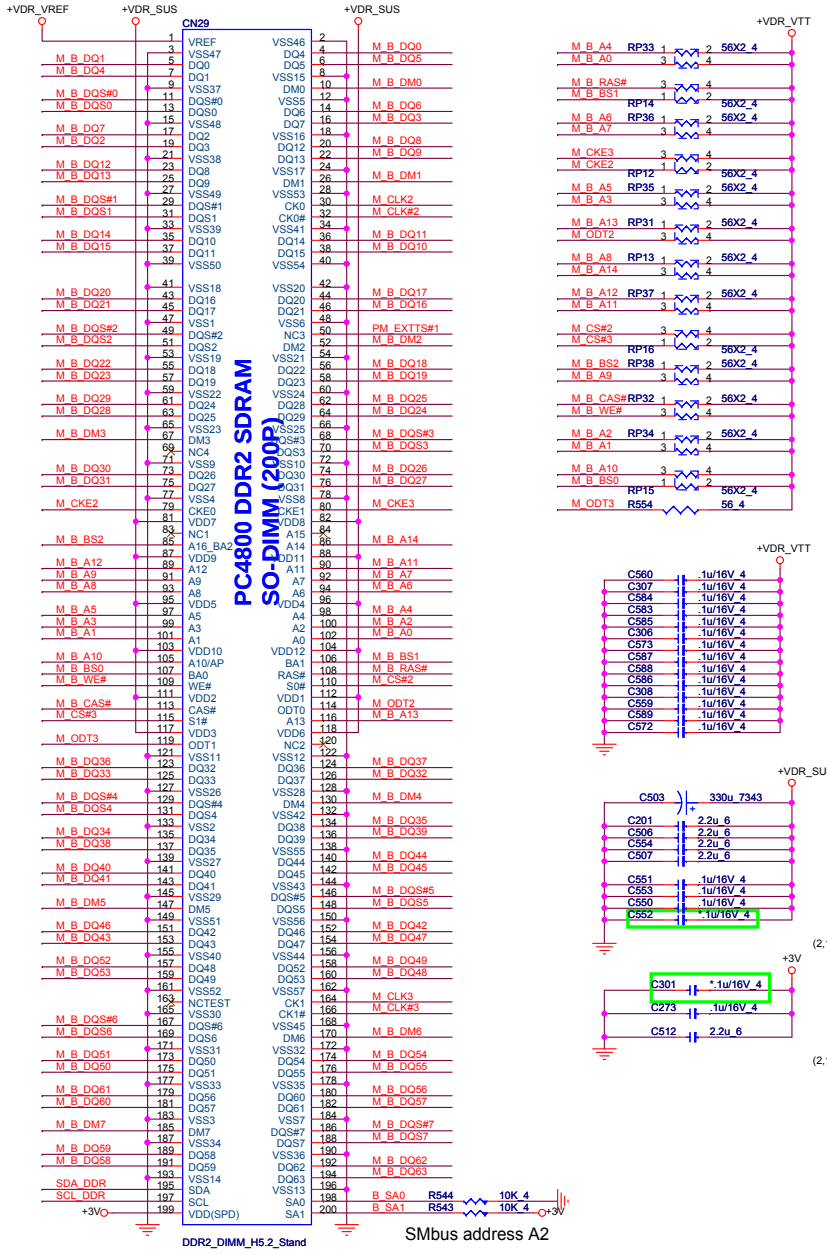
DDR2 Module



IN2-Layer

CLOCK 0,1

NOTE:Place one cap close to every 2 pull-up resistors terminated to +SMDDR_VTERM



IN1-Layer

CLOCK 2,3

Quanta Computer Inc.			
PROJECT : ZK2			
Size	Document Number		Rev
	DDRII SO-DIMM		3B
Date: Friday, June 27, 2008		Sheet 16 of 39	

MXM Module

IV@
EV@

4Amp
0.5Amp
1.5Amp
0.5Amp
3.5Amp

CN21A

CN21B

*E@MXM CONNECTOR_2

*E@MXM CONNECTOR_2

For ATI only

CRT

LVDS

iHDMI

Quanta Computer Inc.
PROJECT : ZK2

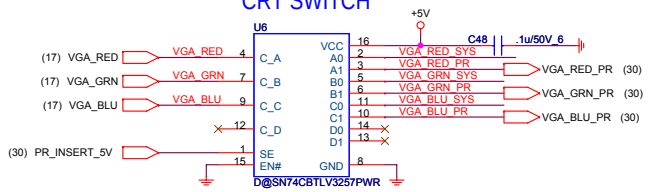
Size	Document Number	Rev
	MXM	3B

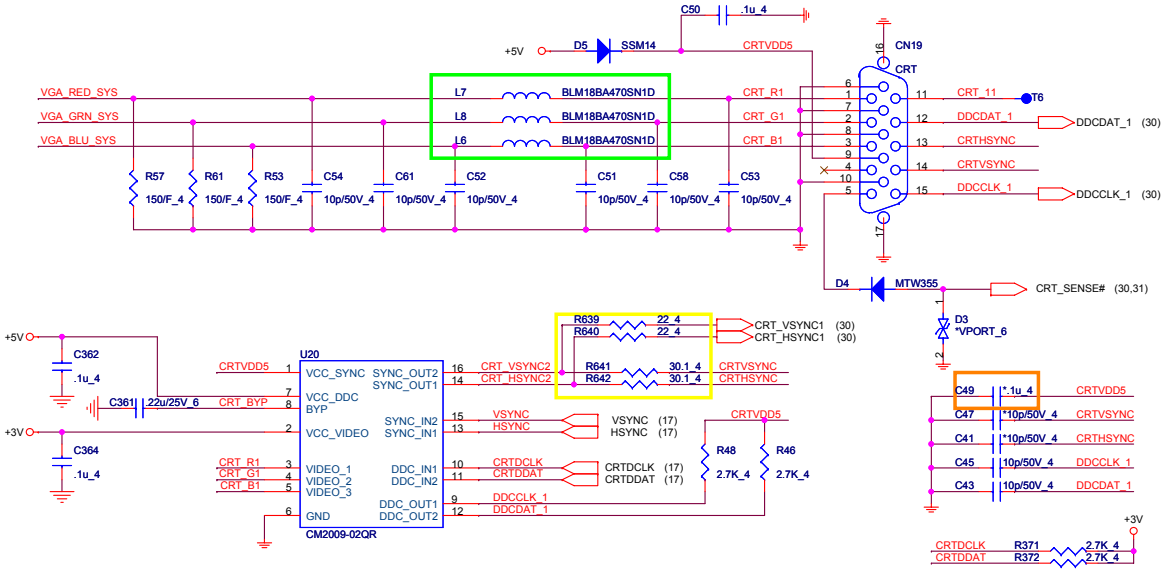
Date: Friday, June 27, 2008 Sheet 17 of 39

CRT

IV@
EV@

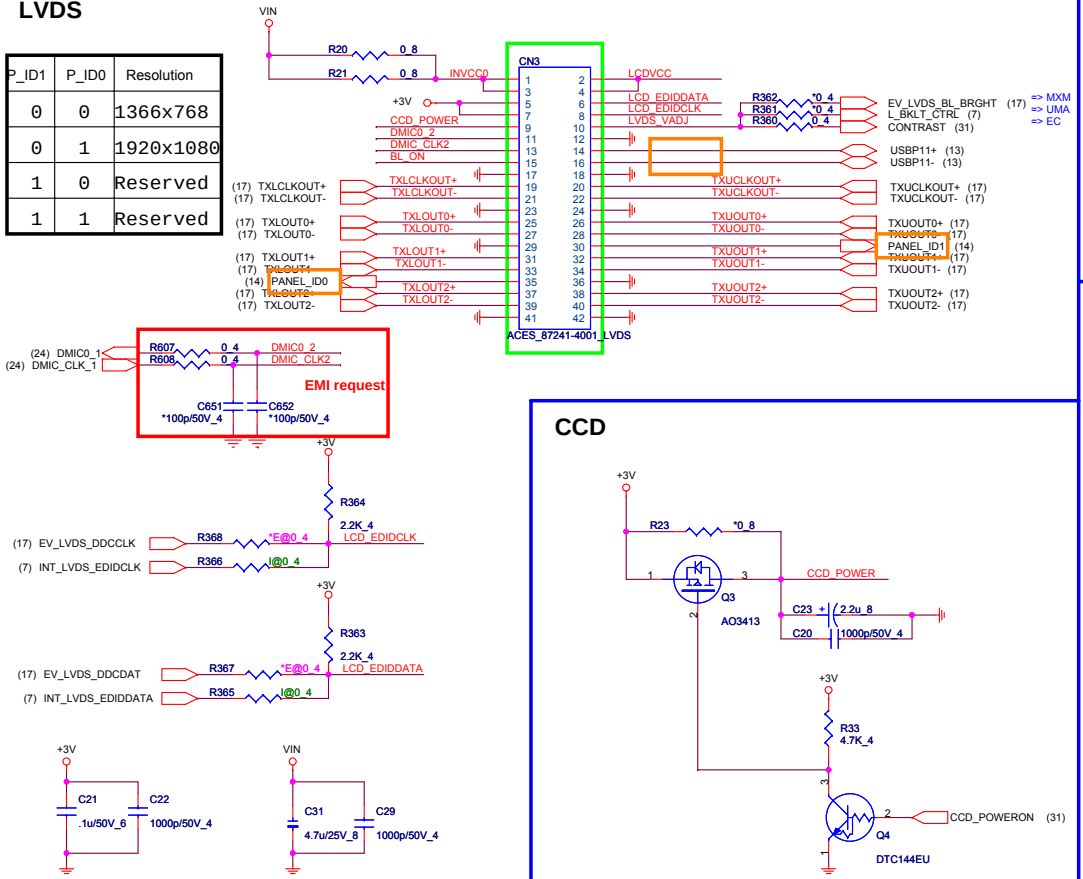
CRT SWITCH





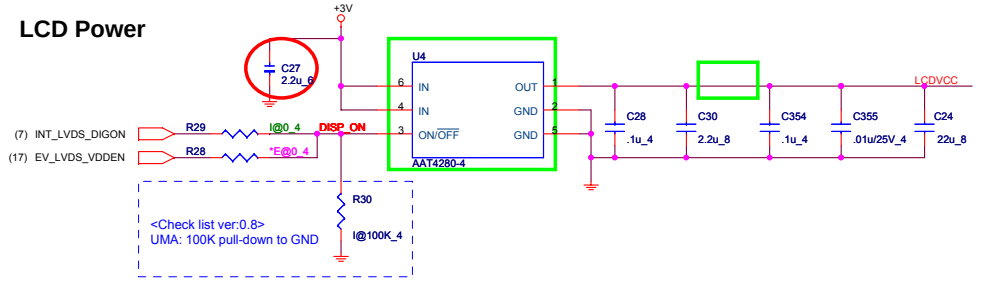
LVDS

P_ID1	P_ID0	Resolution
0	0	1366x768
0	1	1920x1080
1	0	Reserved
1	1	Reserved

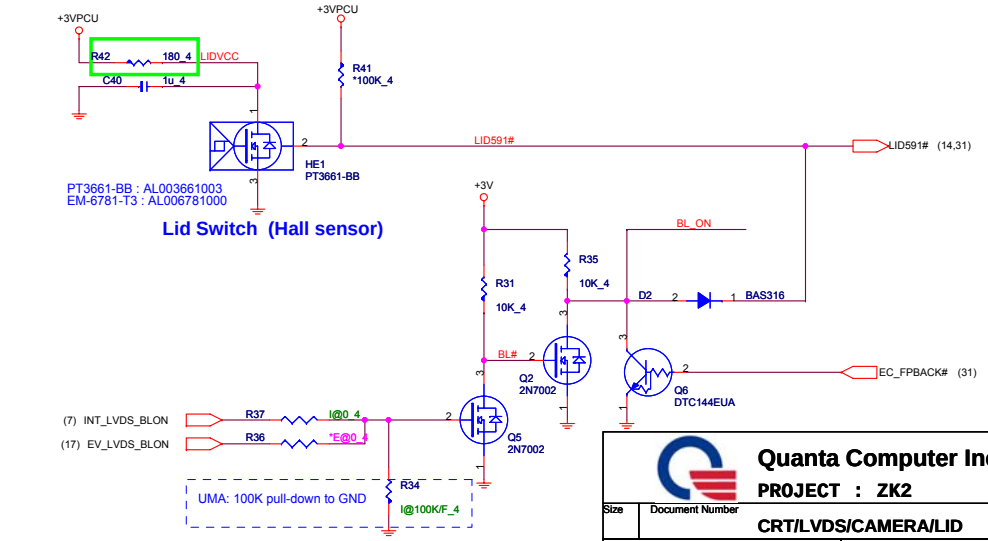


CCD

LCD Power



Backlight Control & LID



Quanta Computer Inc.
PROJECT : ZK2

Size	Document Number	Rev
	CRT/LVDS/CAMERA/LID	3B

Date: Wednesday, July 09, 2008 Sheet 18 of 39

HDMI Switch

IV@
EV@
SP@

BIAS	FUNCTION
H	MXM (DC-coupled)
L	UMA(AC-coupled)

From GMCH

(17) INT_HDMITXP0 / (17) INT_HDMITXN0 — RN26 — I@0_4P2R — HDMITX0P / HDMITX0N
(17) INT_HDMITXP1 / (17) INT_HDMITXN1 — RN27 — I@0_4P2R — HDMITX1P / HDMITX1N
(17) INT_HDMITXP2 / (17) INT_HDMITXN2 — RN28 — I@0_4P2R — HDMITX2P / HDMITX2N
(17) INT_HDMITXP3 / (17) INT_HDMITXN3 — RN29 — I@0_4P2R — HDMICLK+ / HDMICLK-

From MXM

(17) HDMI_TX0P / (17) HDMI_TX0N — RN1 — *E@0_4P2R — HDMITX0P / HDMITX0N
(17) HDMI_TX1P / (17) HDMI_TX1N — RN2 — *E@0_4P2R — HDMITX1P / HDMITX1N
(17) HDMI_TX2P / (17) HDMI_TX2N — RN3 — *E@0_4P2R — HDMITX2P / HDMITX2N
(17) HDMI_CLK+ / (17) HDMI_CLK- — RN4 — *E@0_4P2R — HDMICLK+ / HDMICLK-

+5V — R604 D@1.5K_4 HDMI_DDCDATA_MB
R603 D@1.5K_4 HDMI_DDCCLK_MB
R606 D@1.5K_4 HDMI_DDCCLK_DK
R605 D@1.5K_4 HDMI_DDCDATA_DK

+3V — R595 I@0_4 — R596 *E@0_4 — C645 D@2.2u_6 — BIAS

HDMITX2P / HDMITX2N
HDMITX1P / HDMITX1N
HDMITX0P / HDMITX0N
HDMICLK+ / HDMICLK-
HDMI_DDCCLK_SW
HDMI_DDCDATA_SW
HDMI_HP_SW
HDMI_REXT — R598 D@499/F_4

U7 — D@PS8122 (I2C Control Mode)

IN2p IN2n VCC IN3p IN3n GND IN4p IN4n SCL_SRC SDA_SRC HPD_SRC REXT GND
SDA_CTL SCL_CTL I2C_CTL_EN HPD1 AUX1p AUX1n SCL1_AUX1p VCC OUT1D4n OUT1D4p GND OUT1D3n OUT1D3p
IN1n IN1p VBIAS REXT OUT2D1p OUT2D1n GND OUT2D2p OUT2D2n VCC OUT2D3p OUT2D3n
OUT2D4p OUT2D4n GND SCL2_AUX2p SDA2_AUX2n HPD2 I2C_ADDR OUT1D1p OUT1D1n VCC OUT1D2p OUT1D2n

HDMIDATA / HDMICLK / I2C_EN — R599 D@4.7K_4 — +3V
HDMI_MB_HP
HDMI_DDCDATA_MB
HDMI_DDCCLK_MB

R597 D@4.7K_4 — +3V
MB_HDMITX2P / MB_HDMITX2N
MB_HDMITX1P / MB_HDMITX1N
MB_HDMITX0P / MB_HDMITX0N
MB_HDMICLK+ / MB_HDMICLK-

I2C_ADDR	Address
H	BE/BF
L	9E/9F (internal PD)

To Dock

D_DVITX2+ / D_DVITX2- — D_DVITX2+ (30) / D_DVITX2- (30)
D_DVITX1+ / D_DVITX1- — D_DVITX1+ (30) / D_DVITX1- (30)
D_DVITX0+ / D_DVITX0- — D_DVITX0+ (30) / D_DVITX0- (30)
D_DVICLK+ / D_DVICLK- — D_DVICLK+ (30) / D_DVICLK- (30)
HDMI_DDCCLK_DK — HDMI_DDCCLK_DK (30)
HDMI_DDCDATA_DK — HDMI_DDCDATA_DK (30)
HDMI_HP_DK — HDMI_HP_DK (30)

To M/B

MB_HDMITX0P / MB_HDMITX0N
MB_HDMICLK+ / MB_HDMICLK-

+3V — C646 D@2.2u_6 — C647 D@.1u/16V_4 — C648 D@.1u/16V_4 — C649 D@.1u/16V_4 — C650 D@.1u/16V_4

EMI reserve

MB_HDMITX2P — R634 *100/F_4 — MB_HDMITX2N
MB_HDMITX1P — R635 *100/F_4 — MB_HDMITX1N
MB_HDMITX0P — R636 *100/F_4 — MB_HDMITX0N
MB_HDMICLK+ — R637 *100/F_4 — MB_HDMICLK-

D_DVITX2+ — R619 100/F_4 — C656 1p_4 — D_DVITX2-
D_DVITX1+ — R620 100/F_4 — C657 1p_4 — D_DVITX1-
D_DVITX0+ — R621 100/F_4 — C658 1p_4 — D_DVITX0-
D_DVICLK+ — R622 100/F_4 — C659 1p_4 — D_DVICLK-

Close Docking side

SDVO I2C Control

NV suggestion near HDMI connector

(6) SDVO_CTRLCLK — R119 *2K/F_4 — Q43 *RHU002N06 — R627 I@0_4 — HDMI_DDCCLK_1 — L11 BLM18AG601_6 — HDMI_DDCCLK_SW — C78 *.1u_4
(17) HDMI_DDCCLK — R601 *E@0_4

(6) SDVO_CTRLDATA — R126 *2K/F_4 — Q44 *RHU002N06 — R628 I@0_4 — HDMI_DDCDATA_1 — L10 BLM18AG601_6 — HDMI_DDCDATA_SW — C70 *.1u_4
(17) HDMI_DDCDATA — R602 *E@0_4

HP-detect

To GMCH

(17) TMDS_HPD# — R458 I@20K/F_6 — R455 I@7.5K/F_4 — Q29 I@RHU002N06 — HDMI_HP_SW — R133 *100K_4

To MXM

(17) HDMI_HP_EV — R600 *E@0_4

SMBUS

(2,14,16,20,22,26) PDAT_SMB / (17,28,31) MXM_SMCLK — R58 *0_4 — Q10 D@RHU002N06 — R66 D@1.5K_4 — R65 D@1.5K_4 — HDMICLK

(2,14,16,20,22,26) PCLK_SMB / (17,28,31) MXM_SMDATA — R56 *0_4 — Q9 D@RHU002N06 — HDMIDATA

ESD Protect

U39 *RClamp0514M_AG
MB_HDMICLK+ / MB_HDMICLK- — HDMI_DDCCLK_MB / HDMI_DDCDATA_MB

U40 *RClamp0514M_AG
MB_HDMITX2P / MB_HDMITX2N — MB_HDMITX1P / MB_HDMITX1N

U41 *RClamp0514M_AG
MB_HDMITX0P / MB_HDMITX0N — HDMI_MB_HP

HDMI connector

Change footprint

CN20 — HDMI
D2+ D2 Shield D2- D1+ D1 Shield D1- D0+ D0 Shield D0- CK+ CK Shield CK- CE Remote NC DDC CLK DDC DATA GND +5V HP DET
SHELL1 SHELL2 GND GND

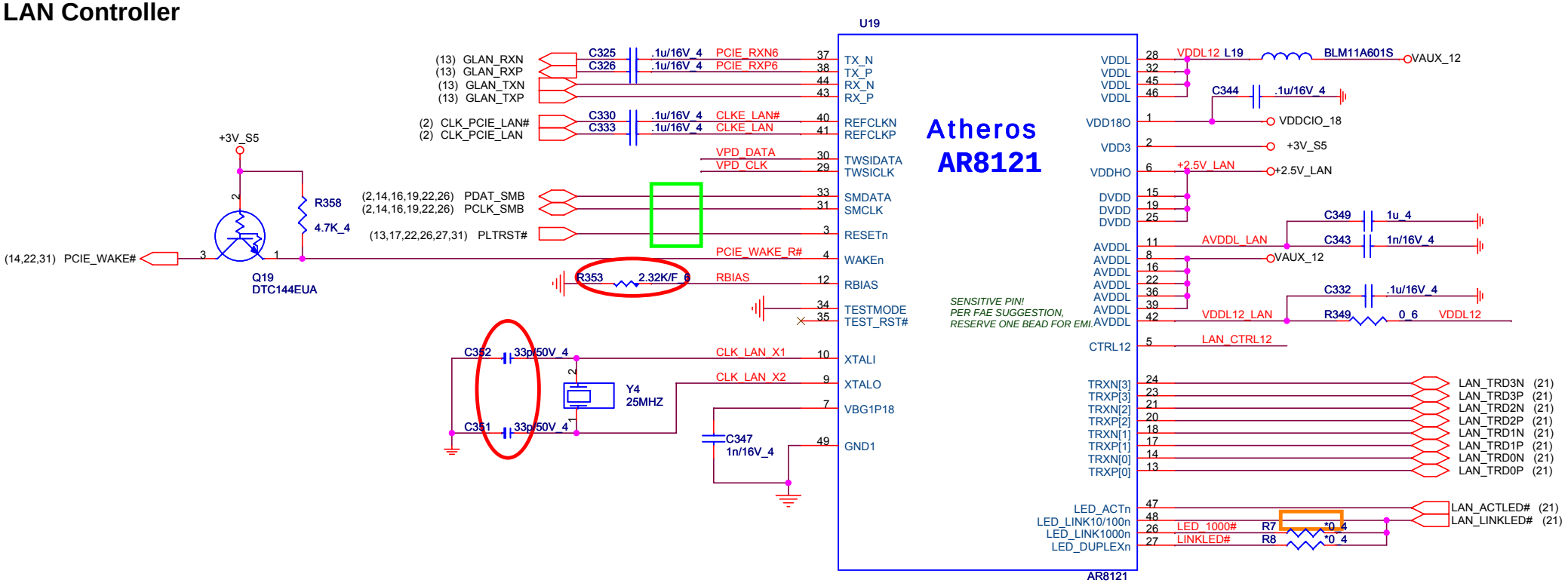
MB_HDMITX2P / MB_HDMITX2N / MB_HDMITX1P / MB_HDMITX1N / MB_HDMITX0P / MB_HDMITX0N / MB_HDMICLK+ / MB_HDMICLK-
HDMI_DDCCLK_MB / HDMI_DDCDATA_MB
HDMI_MB_HP — R107 0_4 — +5V — HP_DET
C662 *.1u/16V_4
+5V — C95 .1u/16V_4

Quanta Computer Inc.
PROJECT : ZK2

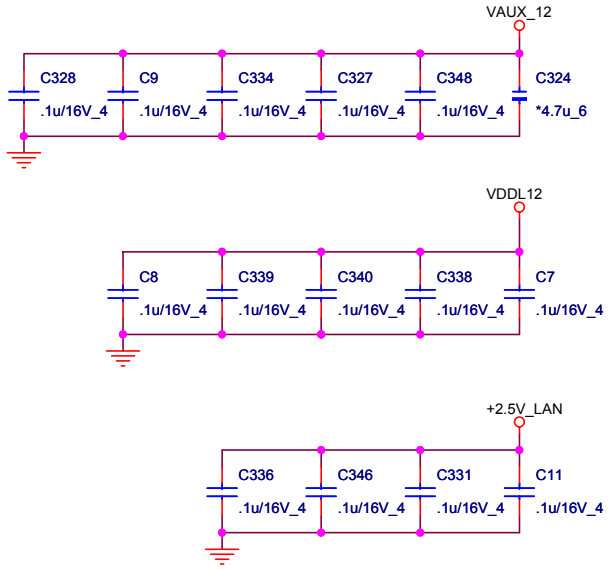
Size	Document Number	Rev
	LVDS/HDMI/CAMERA/LID	3B

Date: Friday, June 27, 2008 Sheet 19 of 39

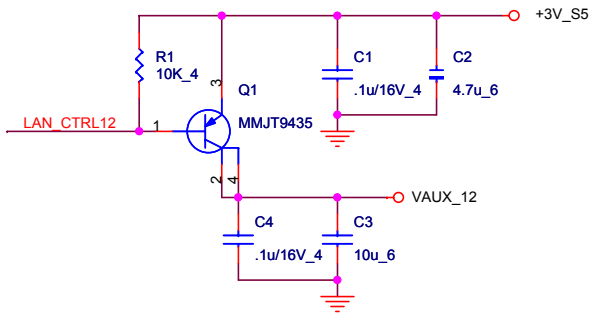
LAN Controller



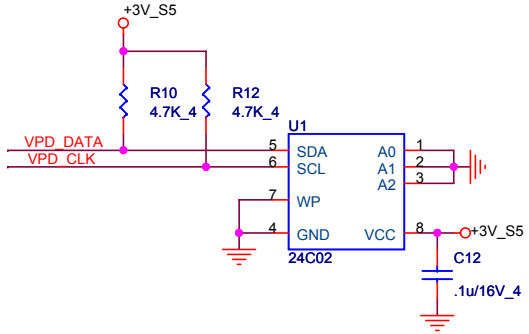
Decoupling CAP



Regulator(1.2V)



EEPROM

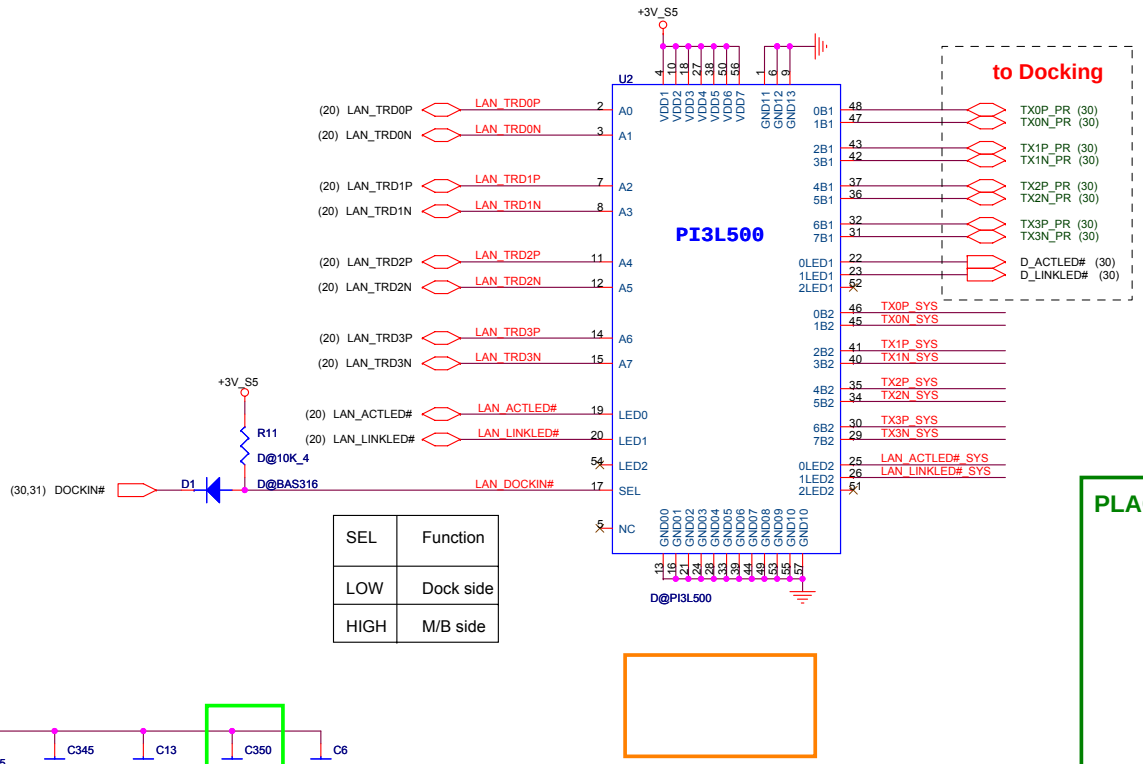


Quanta Computer Inc.

PROJECT : ZK2

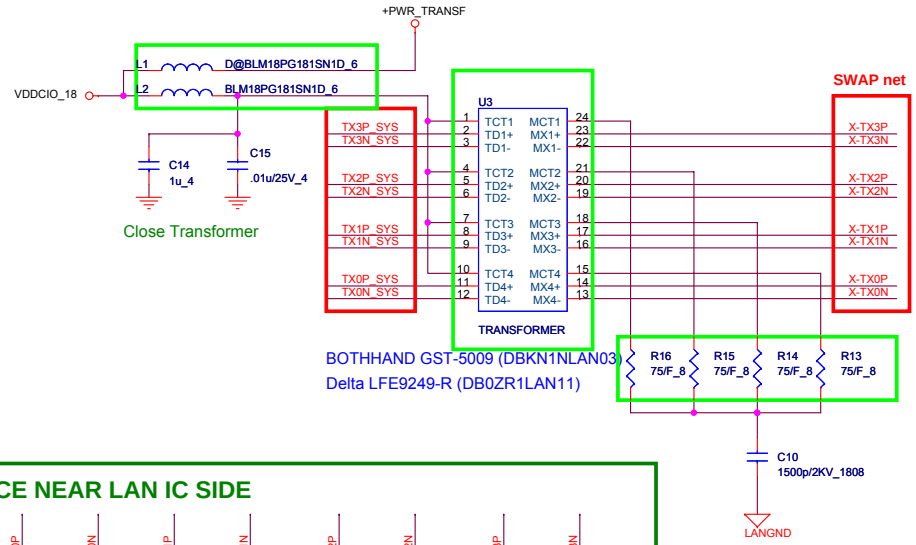
Size	Document Number	Rev
	AR8121 LAN	3B
Date: Friday, June 27, 2008	Sheet 20 of 39	

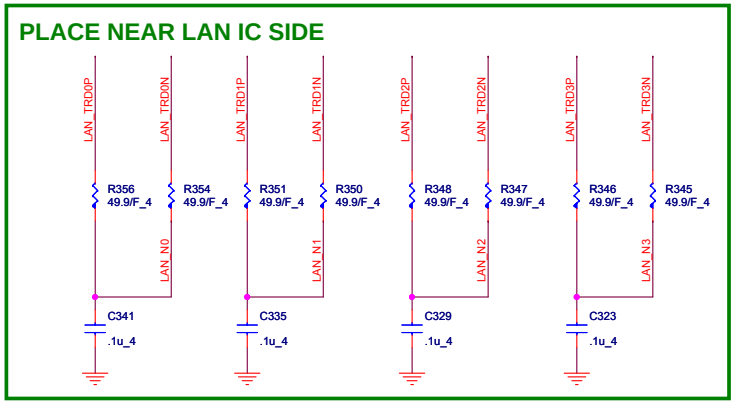
LAN SWITCH



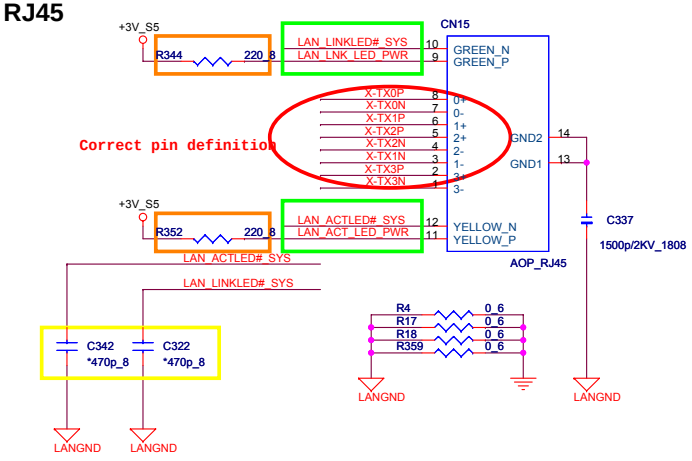
SEL	Function
LOW	Dock side
HIGH	M/B side

TRANSFORMER

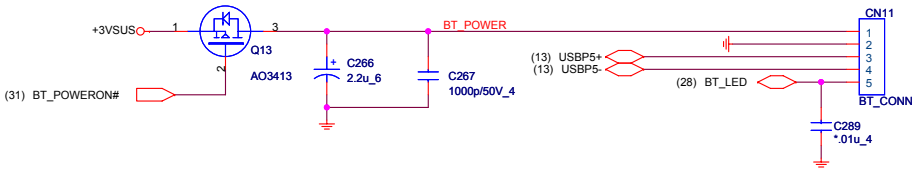




RJ45



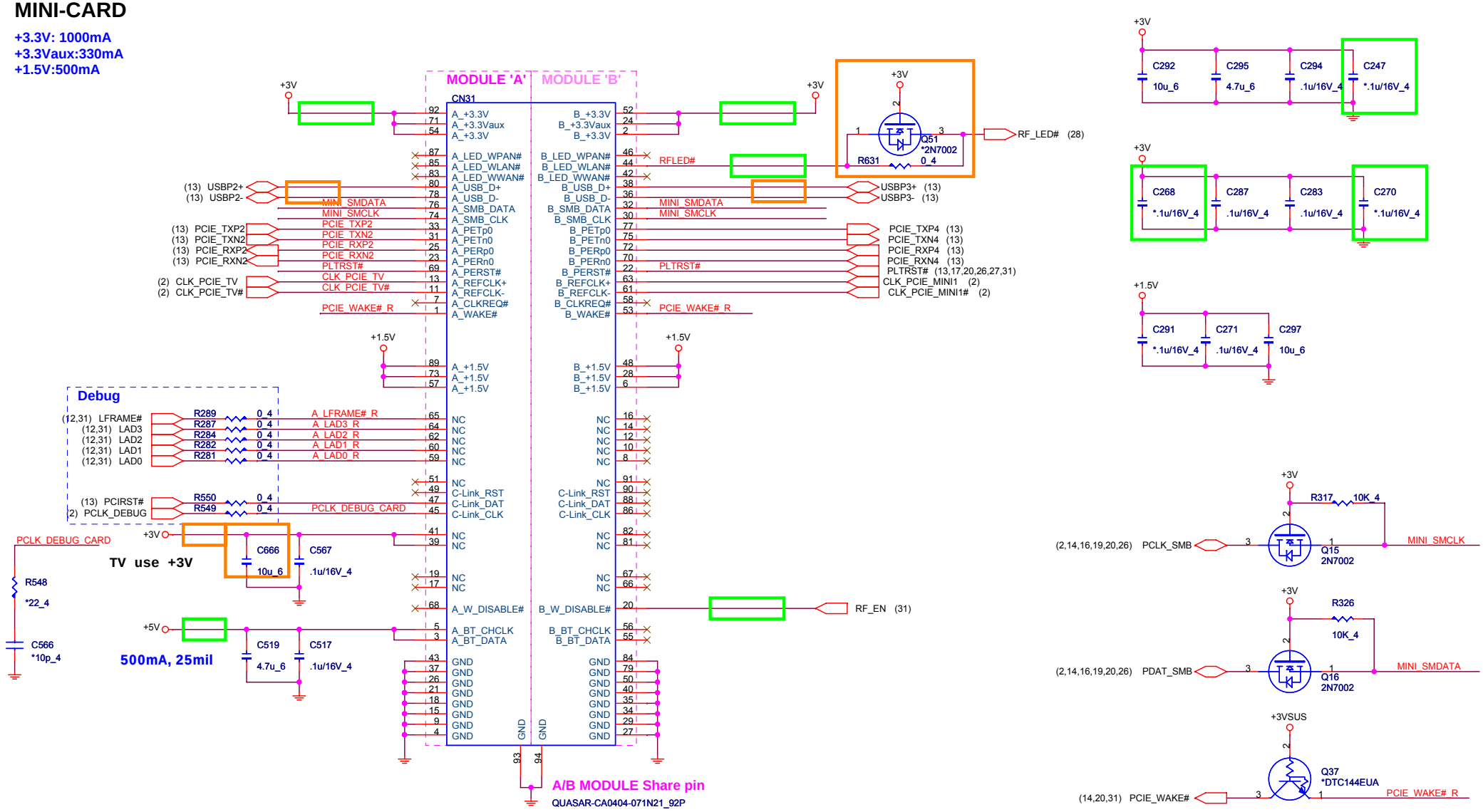
BLUETOOTH CONNECTOR



Quanta Computer Inc. PROJECT : ZK2			
Size	Document Number: LAN SWITCH/TRANSFORMER/RJ45/BT		Rev 3B
Date: Wednesday, July 09, 2008		Sheet 21 of 39	

MINI-CARD

+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA



MODULE 'A' TV card

MODULE 'B' Wireless card

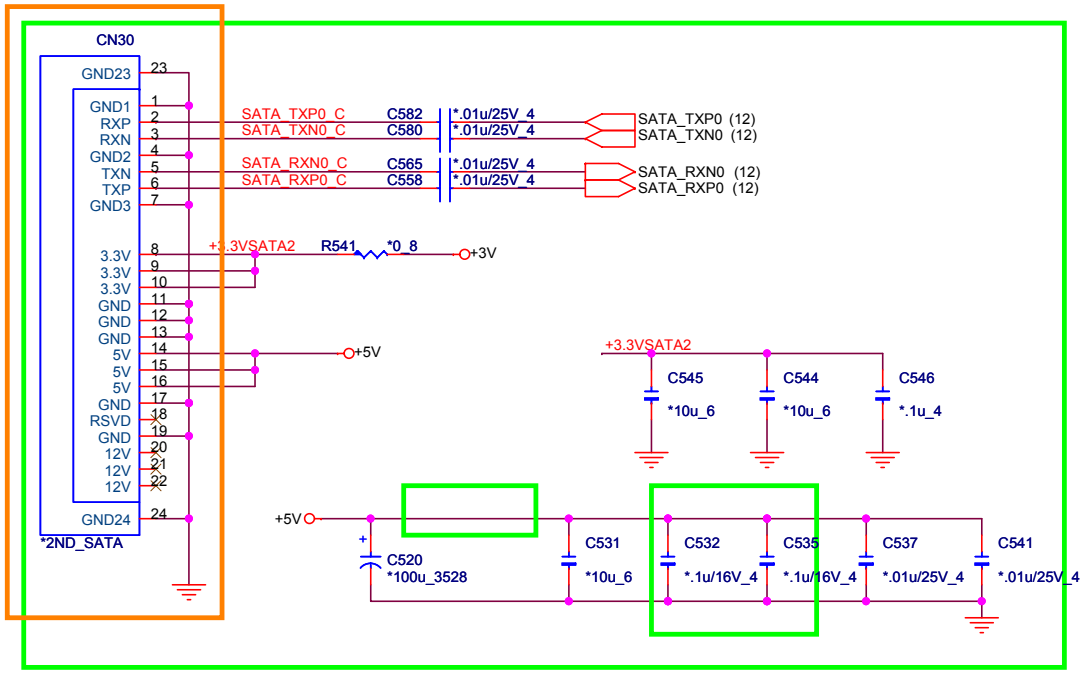
Double Stack MINI CARD

Quanta Computer Inc.

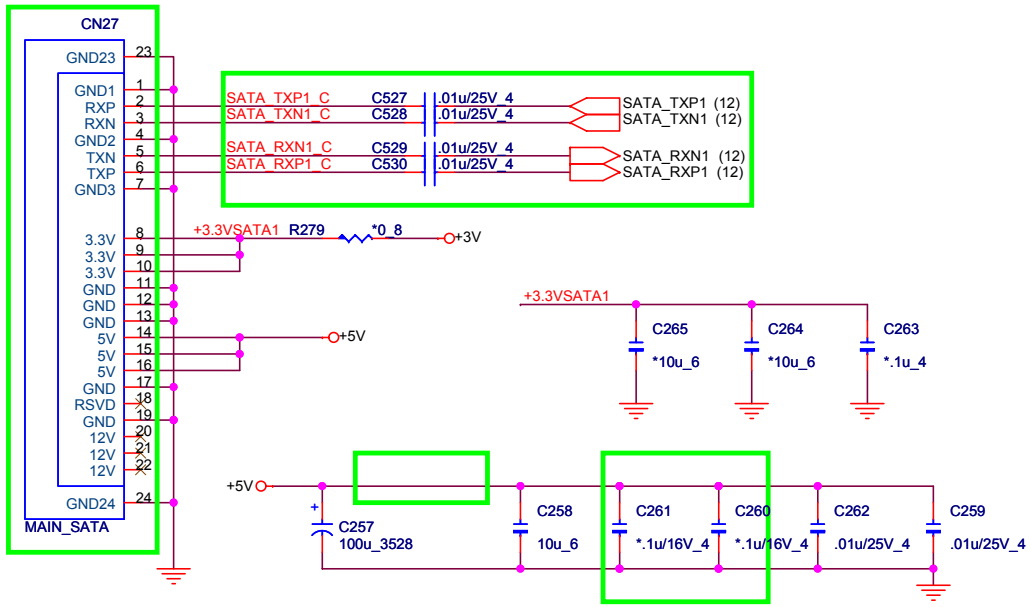
PROJECT : ZK2

Size	Document Number	Rev
	MINI PCI-E card/TV	3B
Date: Friday, June 27, 2008	Sheet 22 of 39	

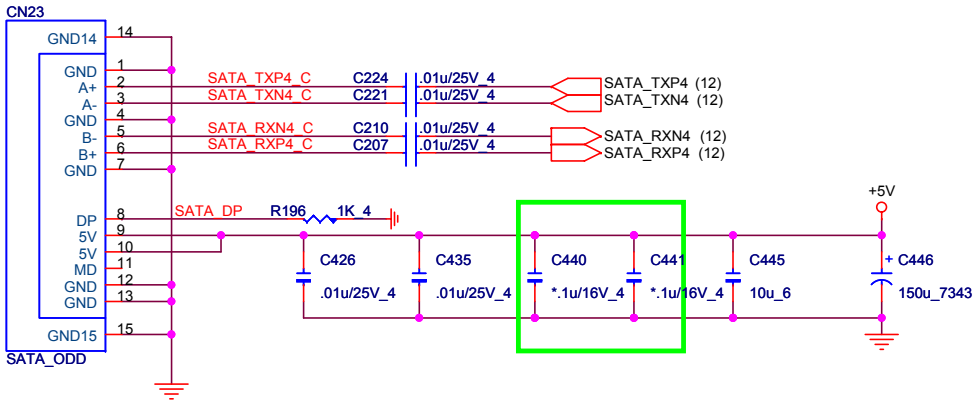
2nd SATA HDD (edge of board)



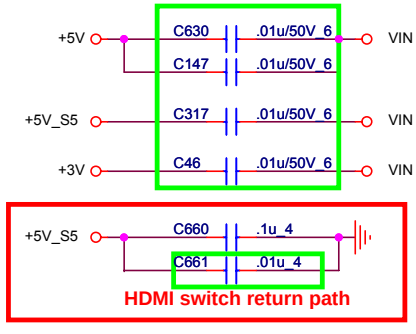
MAIN SATA HDD

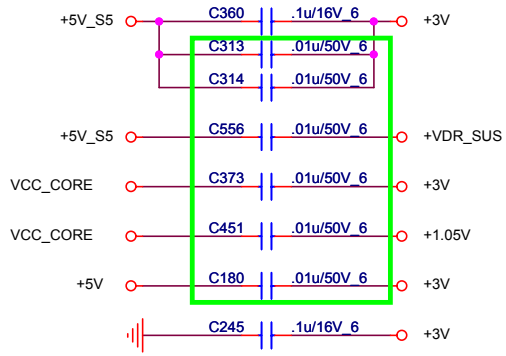


ODD (SATA)



EE RETURN-PATH CAPACITORS





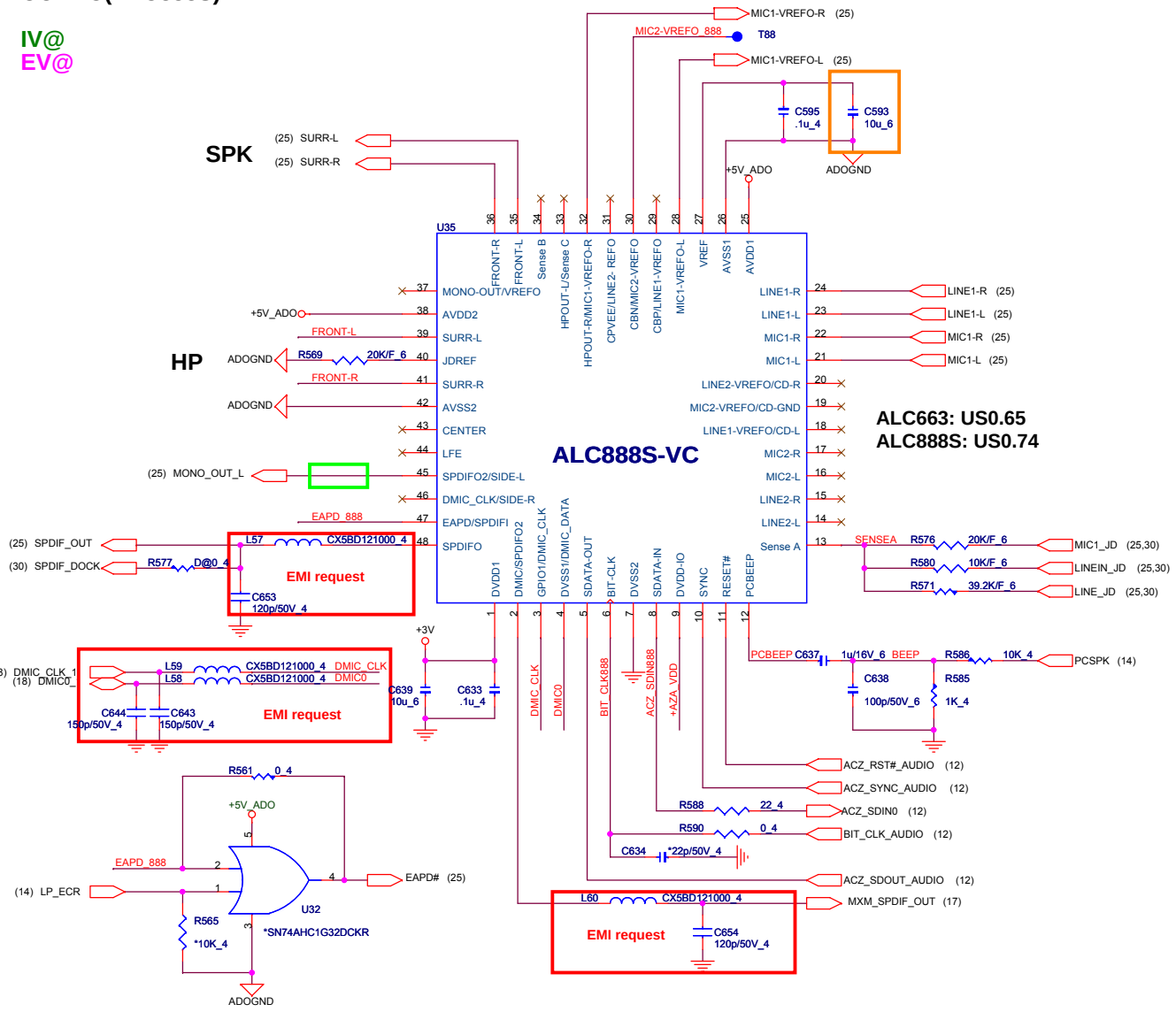
Quanta Computer Inc.

PROJECT : ZK2

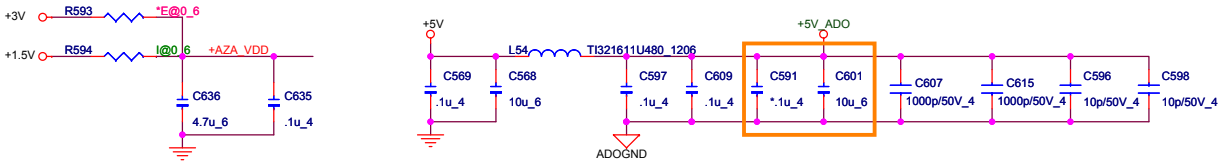
Size	Document Number	Rev
	SATA-HDD/ODD/USB-ESATA	3B
Date: Friday, June 27, 2008	Sheet 23 of 39	

CODEC(ALC888S)

IV@
EV@

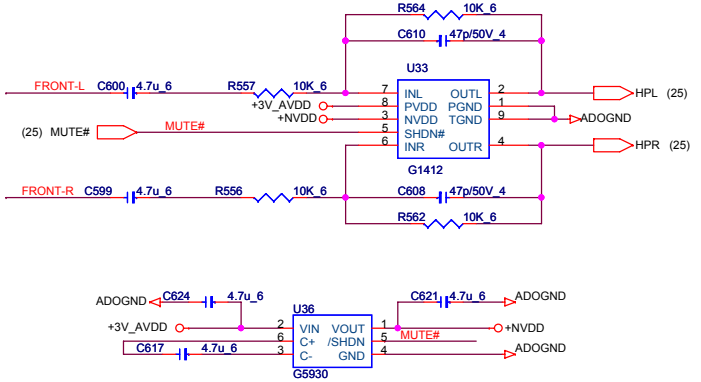


Codec Power

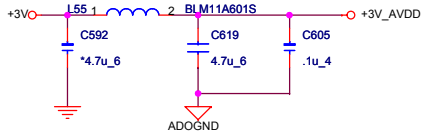


CODEC & MDC

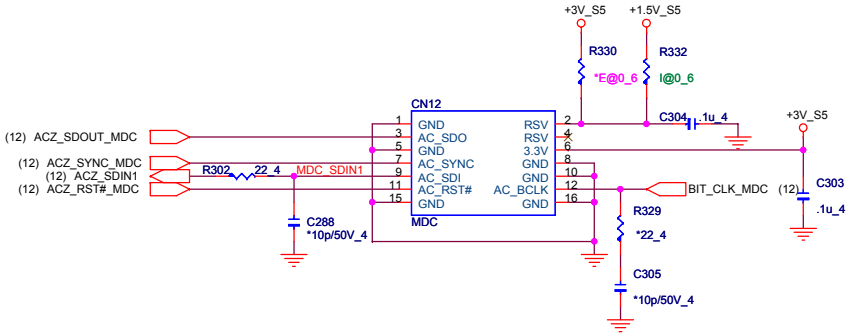
LINE-Out Amplifier



LINE-Out Amplifier Power



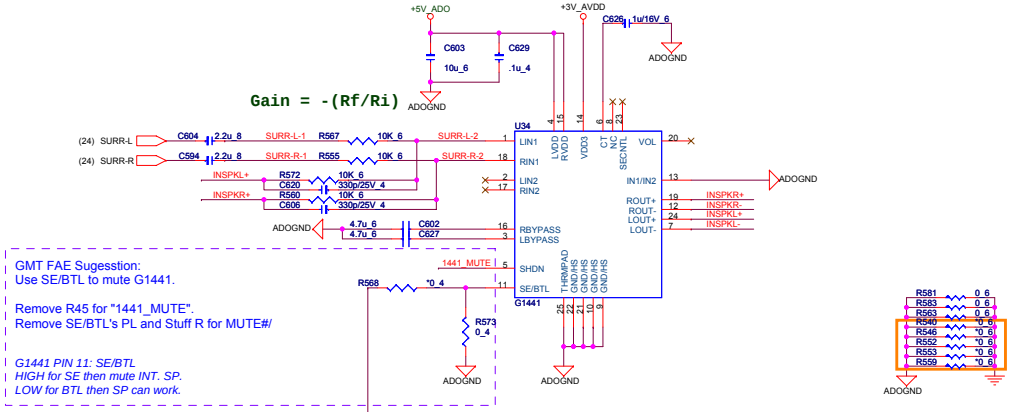
MDC



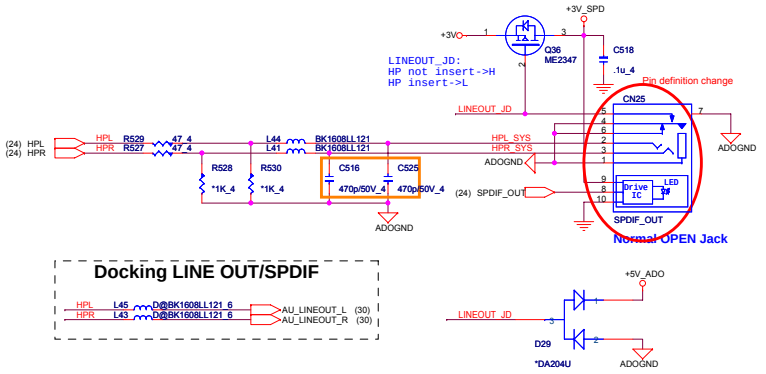
Quanta Computer Inc.
PROJECT : ZK2

Size	Document Number	Rev
	REALTEK ALC663&888/MDC	3B
Date: Friday, June 27, 2008	Sheet 24 of 39	

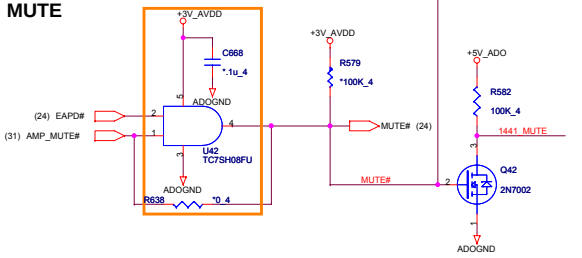
SPEAKER AMP.



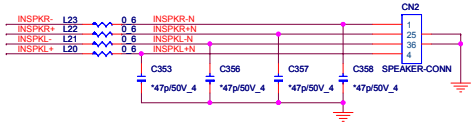
LINE-OUT/SPDIFO

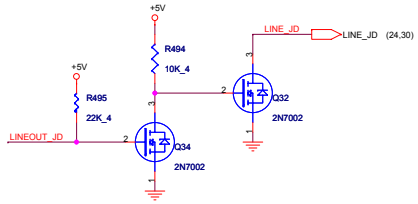


MUTE

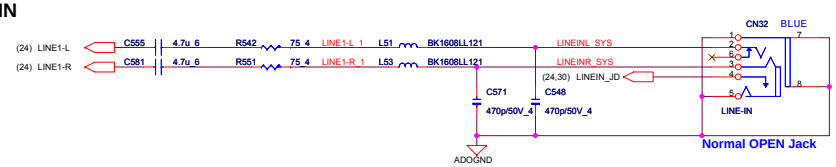


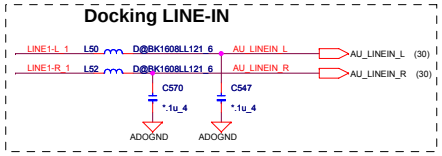
SPEAKER

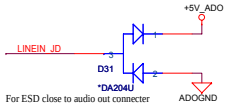




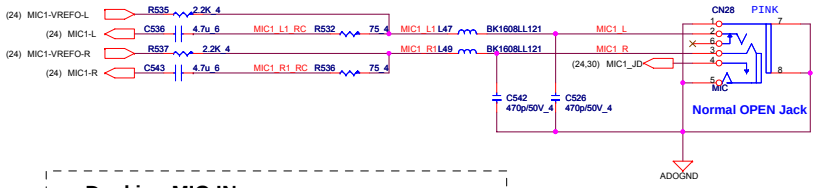
LINE IN

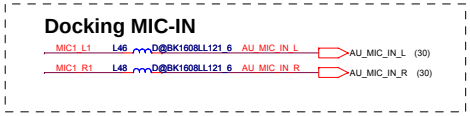


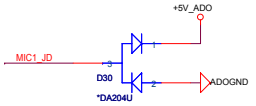




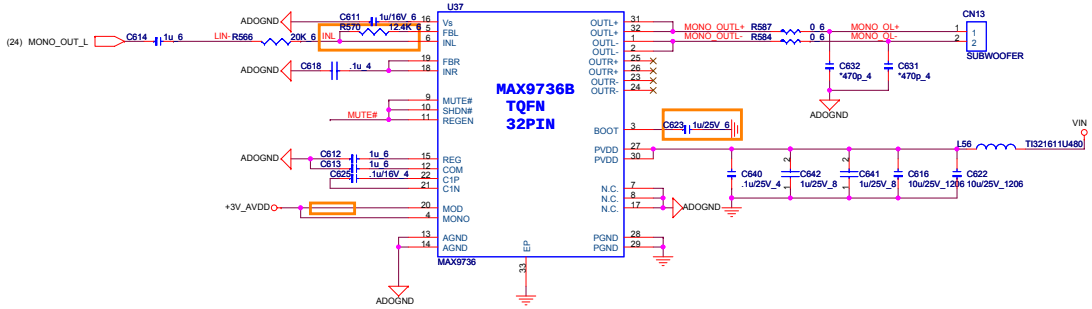
MIC







SUBWOOFER



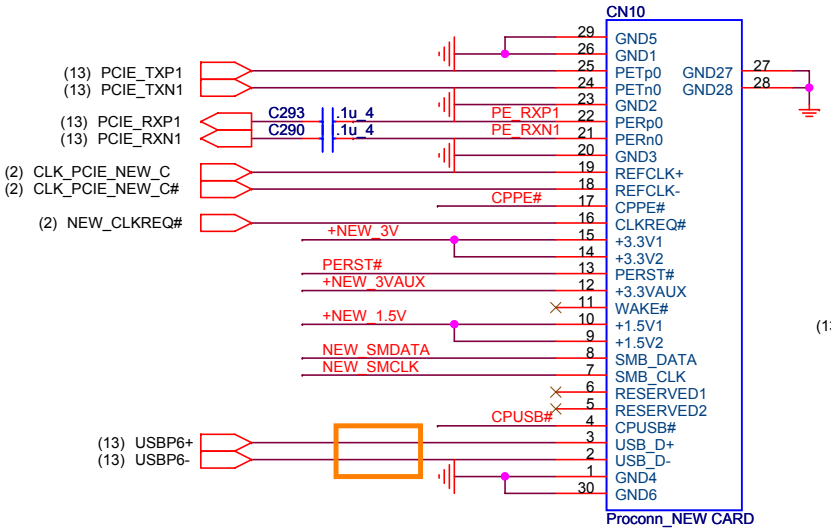
AMP& PHONE JACK & SUBWOOFER

Quanta Computer Inc.
PROJECT : ZK2

Size	Document Number	Rev
	AMP /AUDIO JACK CONN	3B

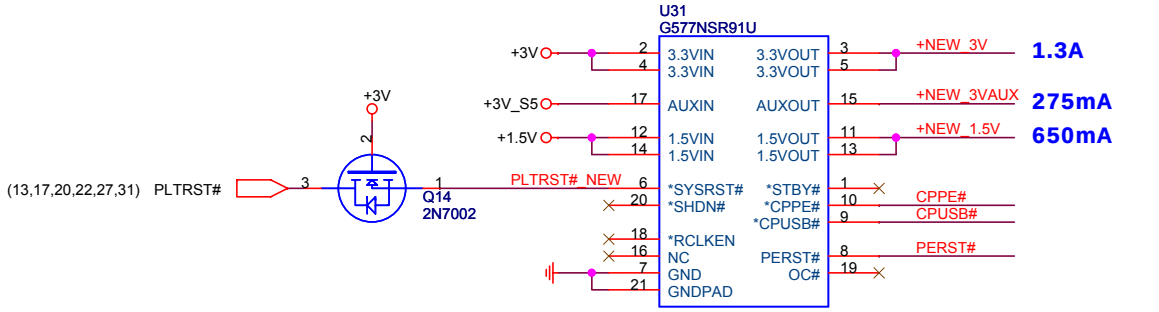
Date: Friday, June 27, 2008 Sheet 25 of 39

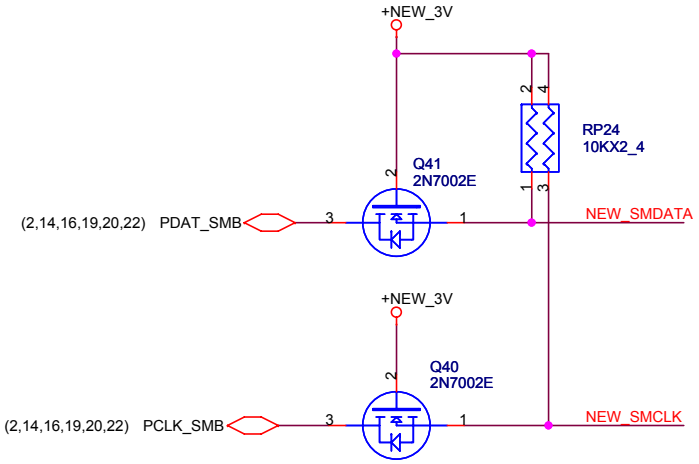
NEW CARD

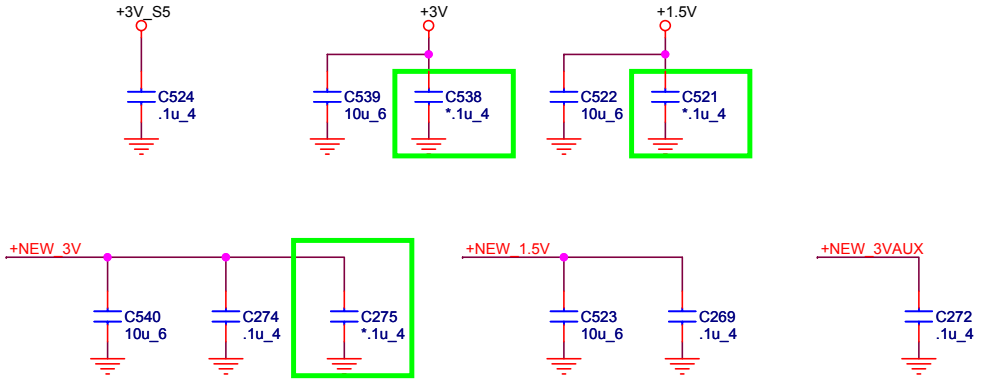


NEW CARD'S POWER SWITCH

TI: AL002231000
GMT: AL000577002



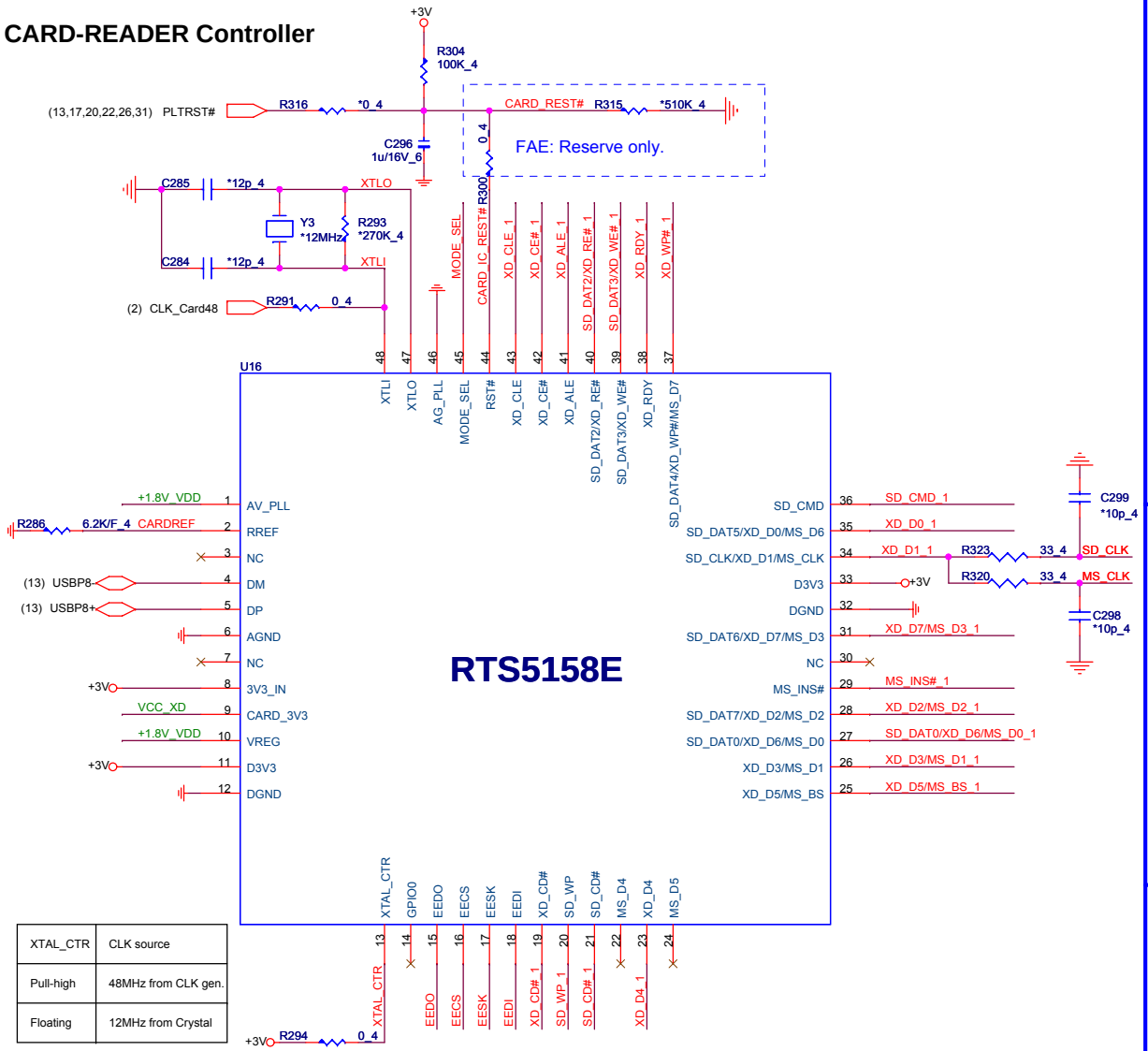




Quanta Computer Inc.
PROJECT : ZK2

Size	Document Number	Rev
	NEW CARD	3B
Date: Friday, June 27, 2008	Sheet 26 of 39	

CARD-READER Controller

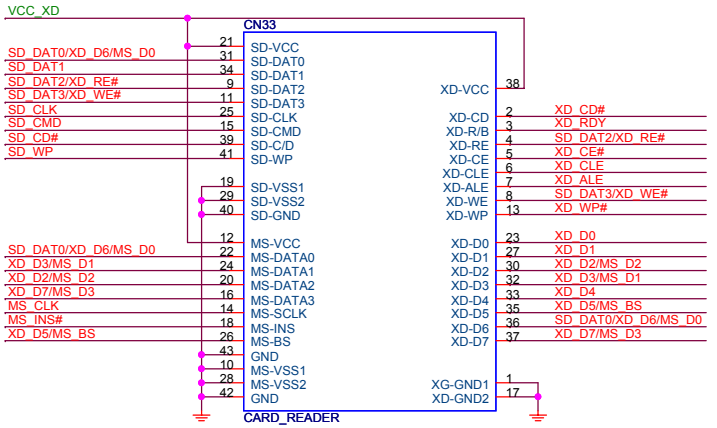


XTAL_CTR	CLK source
Pull-high	48MHz from CLK gen.
Floating	12MHz from Crystal

pin 19	XD_CD#_1	R299 33_4	XD_CD#
pin 20	SD_WP_1	R303 33_4	SD_WP
pin 21	SD_CD#_1	R306 33_4	SD_CD#
pin 23	XD_D4_1	R308 33_4	XD_D4
pin 25	XD_D5/MS_BS_1	R313 33_4	XD_D5/MS_BS
pin 26	XD_D3/MS_D1_1	R314 33_4	XD_D3/MS_D1
pin 27	SD_DAT0/XD_D6/MS_D0_1	R312 33_4	SD_DAT0/XD_D6/MS_D0
pin 28	XD_D2/MS_D2_1	R311 33_4	XD_D2/MS_D2
pin 29	MS_INS#_1	R327 33_4	MS_INS#
pin 31	XD_D7/MS_D3_1	R324 33_4	XD_D7/MS_D3

pin 34	XD_D1_1	R325 33_4	XD_D1
pin 35	XD_D0_1	R321 33_4	XD_D0
pin 36	SD_CMD_1	R322 33_4	SD_CMD
pin 37	XD_WP#_1	R318 33_4	XD_WP#
pin 38	XD_RDY_1	R319 33_4	XD_RDY
pin 39	SD_DAT3/XD_WE#_1	R309 33_4	SD_DAT3/XD_WE#
pin 40	SD_DAT2/XD_RE#_1	R307 33_4	SD_DAT2/XD_RE#
pin 41	XD_ALE_1	R310 33_4	XD_ALE
pin 42	XD_CE#_1	R305 33_4	XD_CE#
pin 43	XD_CLE_1	R301 33_4	XD_CLE

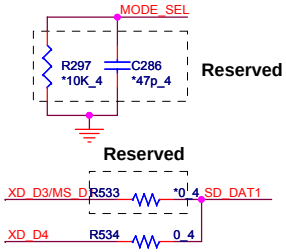
4 IN 1 CARD READER



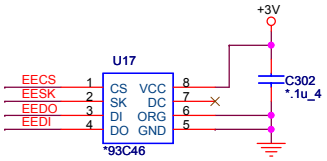
Model_Select

R6256/C860=NC/NC (R6258:ON)=> SD_D1 from pin23

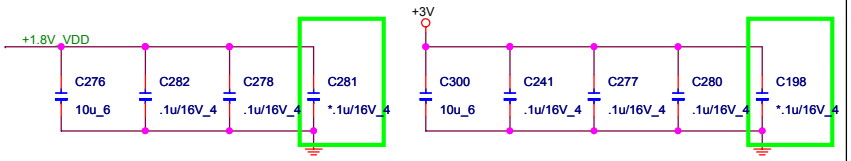
R6256/C860=10K/47pF(R6257:ON)=>SD_D1 from pin26

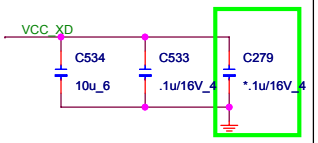


EEPROM(Reserved)



Decoupling CAP





	SD/MMC	MS	XD
SP1		XD_CD#	
SP2	SD_WP		
SP3	SD_CD#		
SP4		XD_D4	
SP5		XD_D5	MS_BS
SP6		XD_D3	MS_D1
SP7	SD_DAT0	XD_D6	MS_D0
SP8	SD_DAT7	XD_D2	MS_D2
SP9			MS_INS#
SP10	SD_DAT6	XD_D7	MS_D3
SP11		XD_D1	
SP12	SD_DAT5	XD_D0	MS_D6
SP13	SD_DAT4	XD_WP#	MS_D7
SP14		XD_RDY	
SP15	SD_DAT3	XD_WE#	
SP16	SD_DAT2	XD_RE#	
SP17		XD_ALE	
SP18		XD_CE#	
SP19		XD_CLE	
		MS_D4	
		MS_D5	

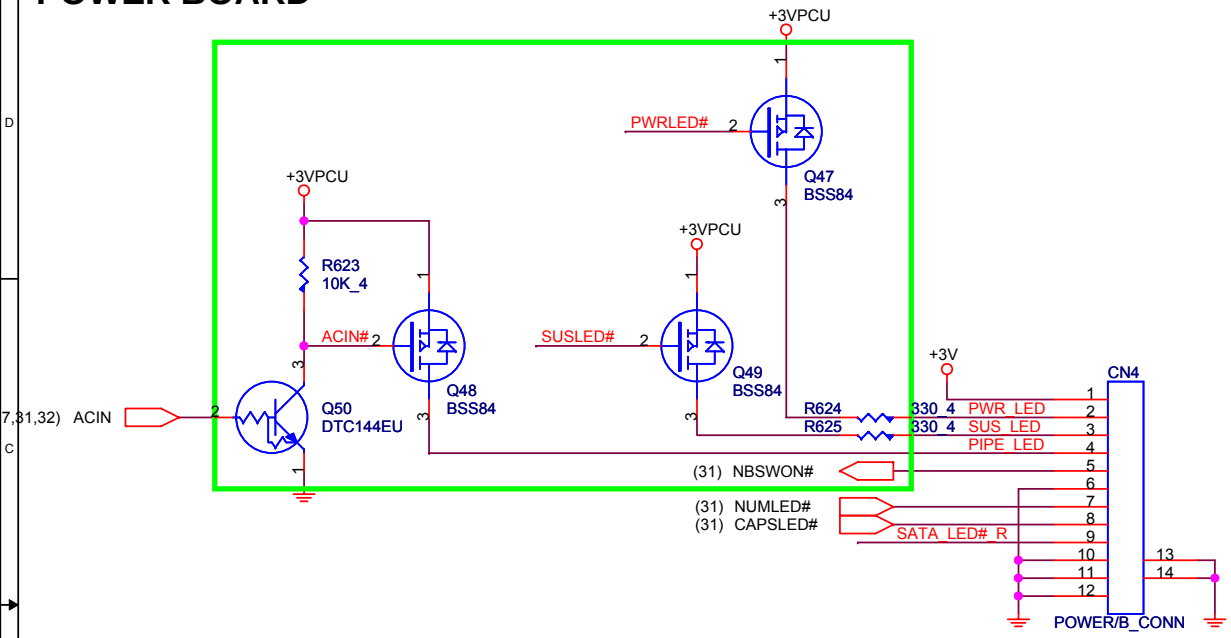
Quanta Computer Inc.

PROJECT : ZK2

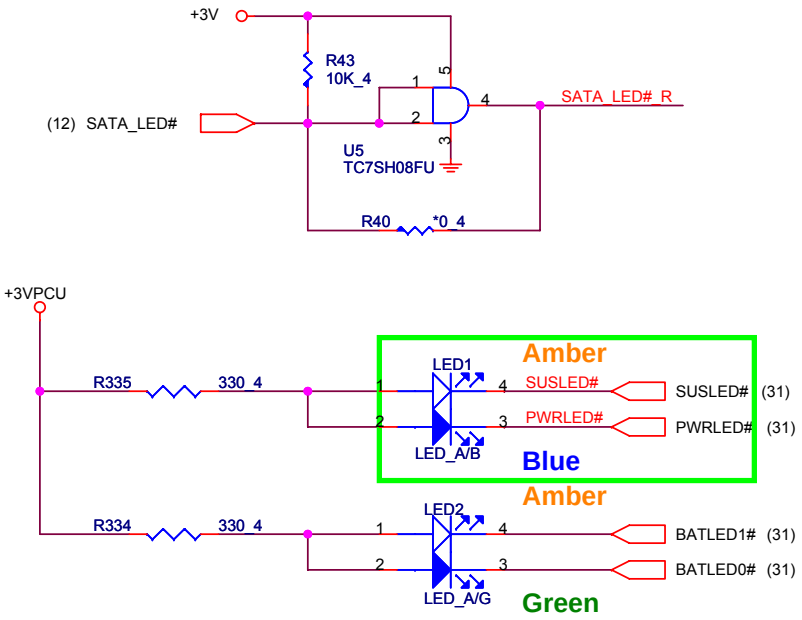
Size	Document Number	Rev
	CARD READER RTS5158E	3B

Date: Friday, June 27, 2008 Sheet 27 of 39

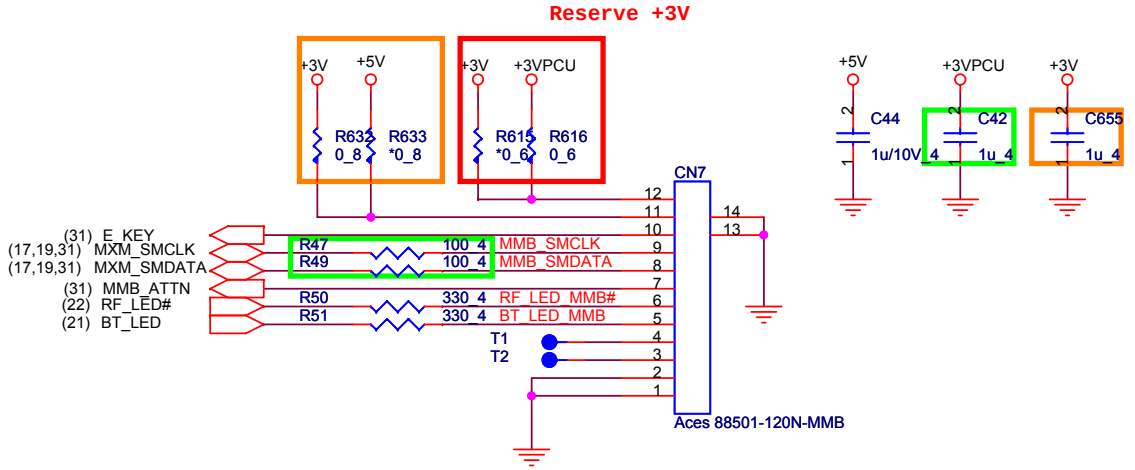
POWER BOARD



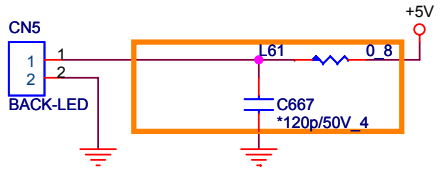
LED



MMB

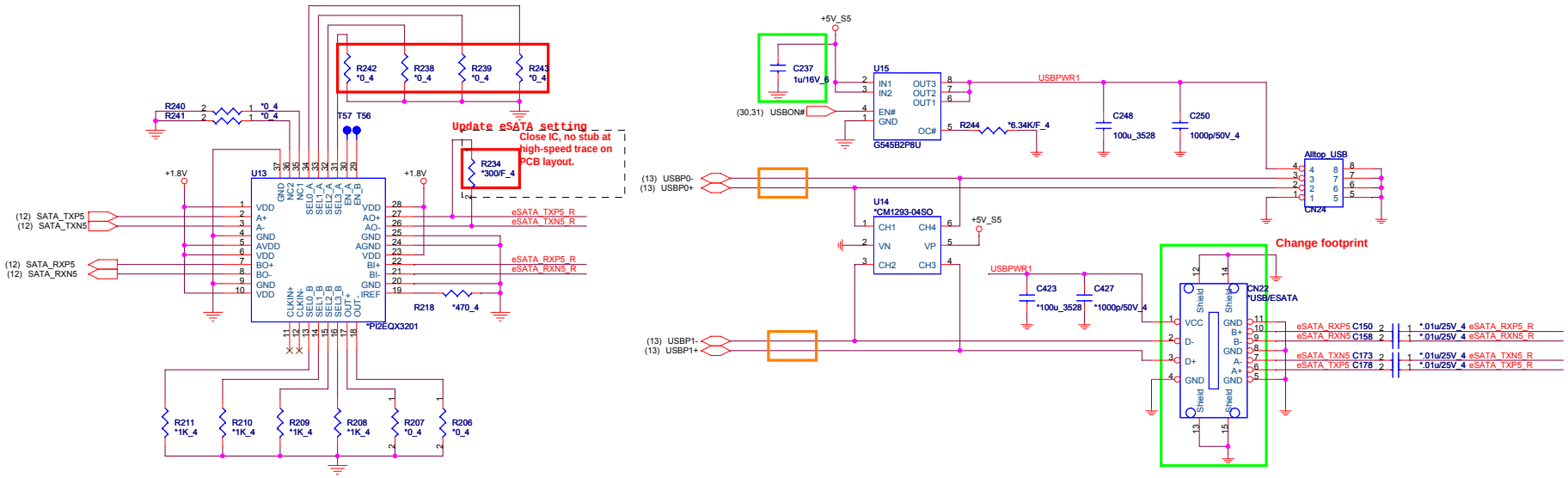


Backlight Logo LED



Quanta Computer Inc.		
PROJECT : ZK2		
Size	Document Number: POWER/MMB/LAUNCH/LED	Rev: 3B
Date: Friday, June 27, 2008	Sheet 28 of 39	

USB & ESATA

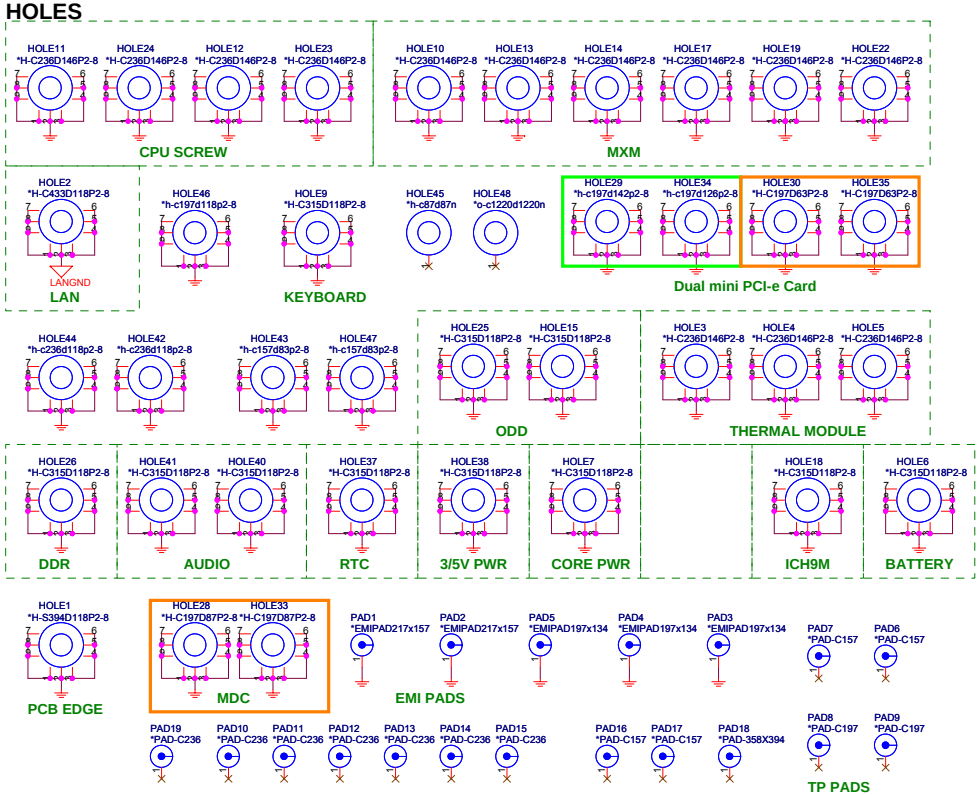


SEL0_X	SEL1_X	Eq
0	0	0dB
0	1	2.5dB
1	0	4.5dB
1	1	6.5dB

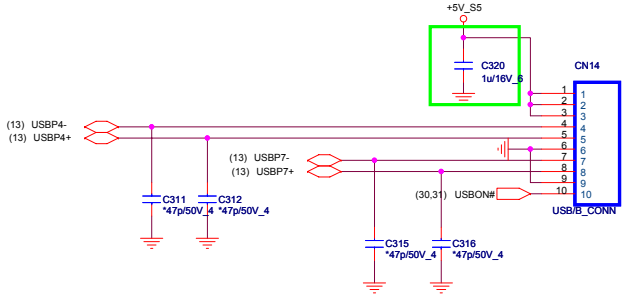
SEL2_X	Swing
0	1.0X
1	1.2X

SEL3_X	De-Emphasis
0	0dB
1	-3.5dB

HOLES



USB/B



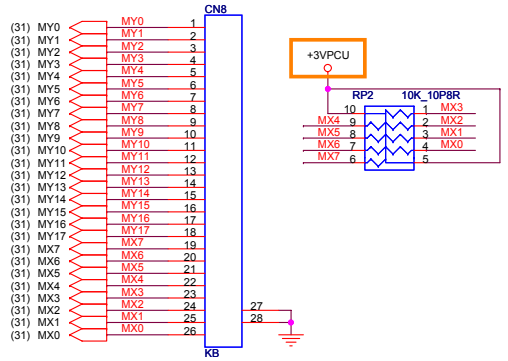
Quanta Computer Inc.

PROJECT : ZK2

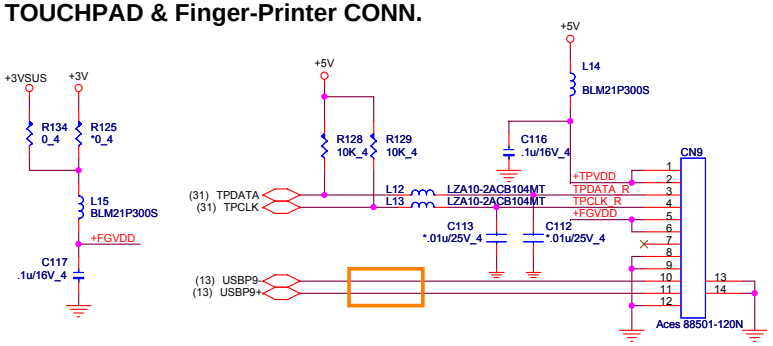
Size	Document Number	Rev
	USB	3B

Date: Friday, June 27, 2008 Sheet 29 of 39

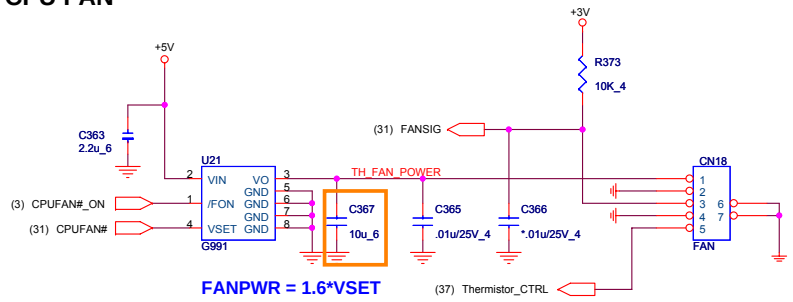
INT K/B



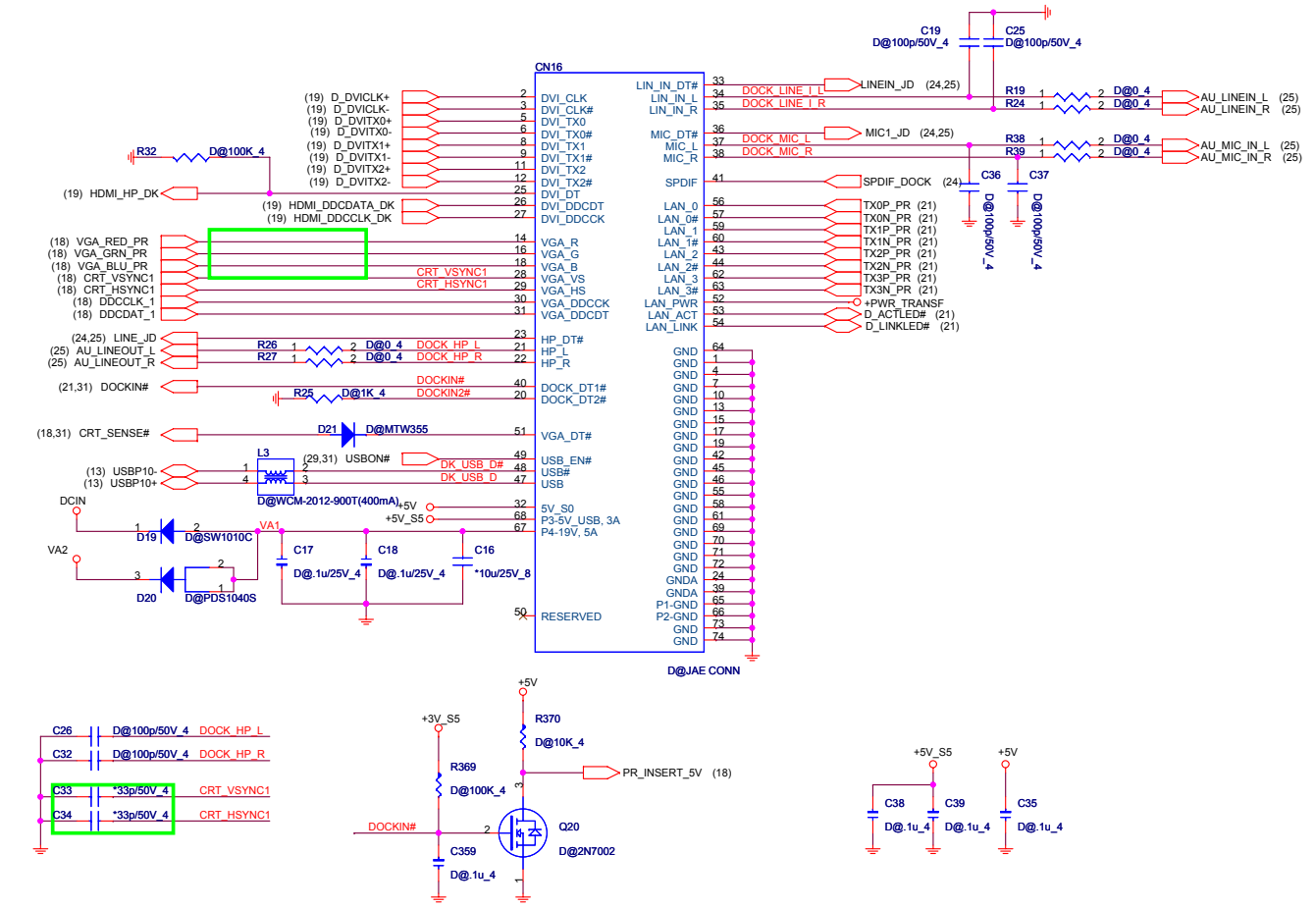
TOUCHPAD & Finger-Printer CONN.



CPU FAN

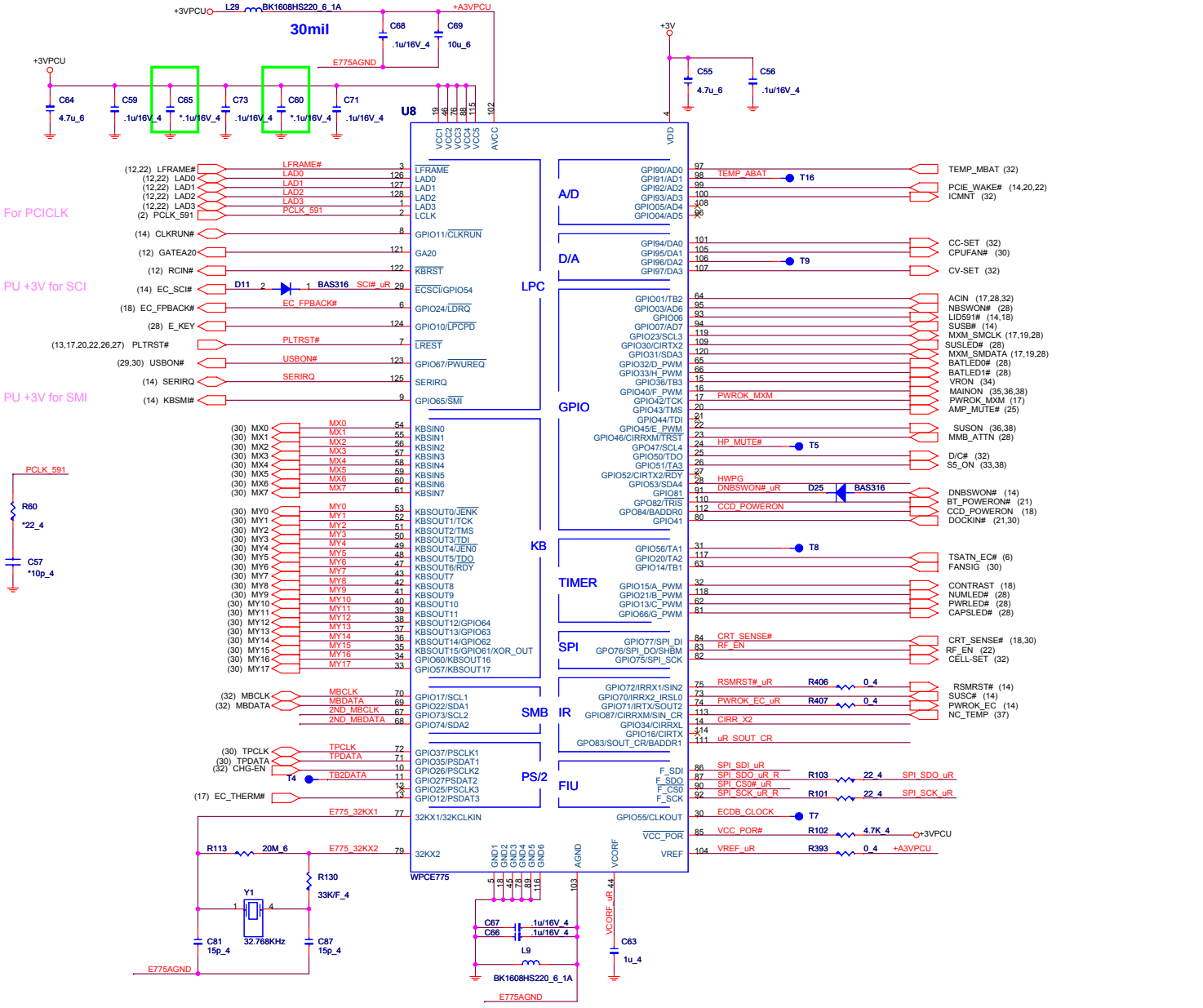


CABLE DOCK



Quanta Computer Inc.			
PROJECT : ZK2			
Size	Document Number	KB/FAN/TP+FP/DOCK	Rev 3B
Date: Wednesday, July 09, 2008		Sheet 30 of 39	

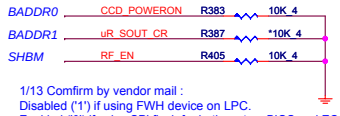
EC



I/O ADDRESS SETTING

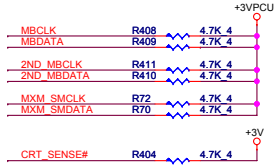
BADDR1-0	I/O Address	
	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

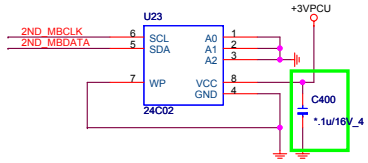


1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

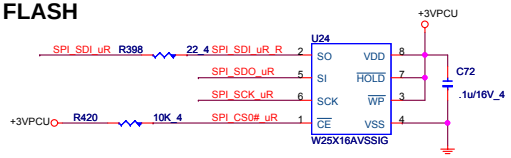
SM BUS PU



ACER ID

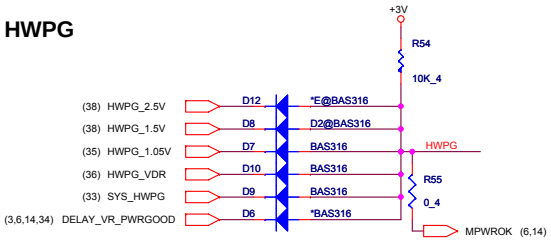


SPI FLASH

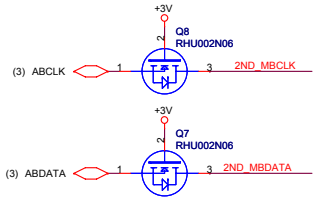


1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

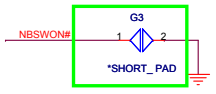
HWPG



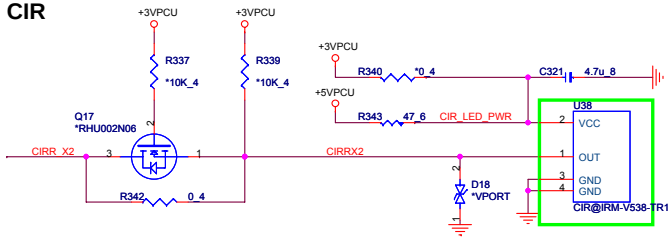
SMBus



POWER-ON PAD

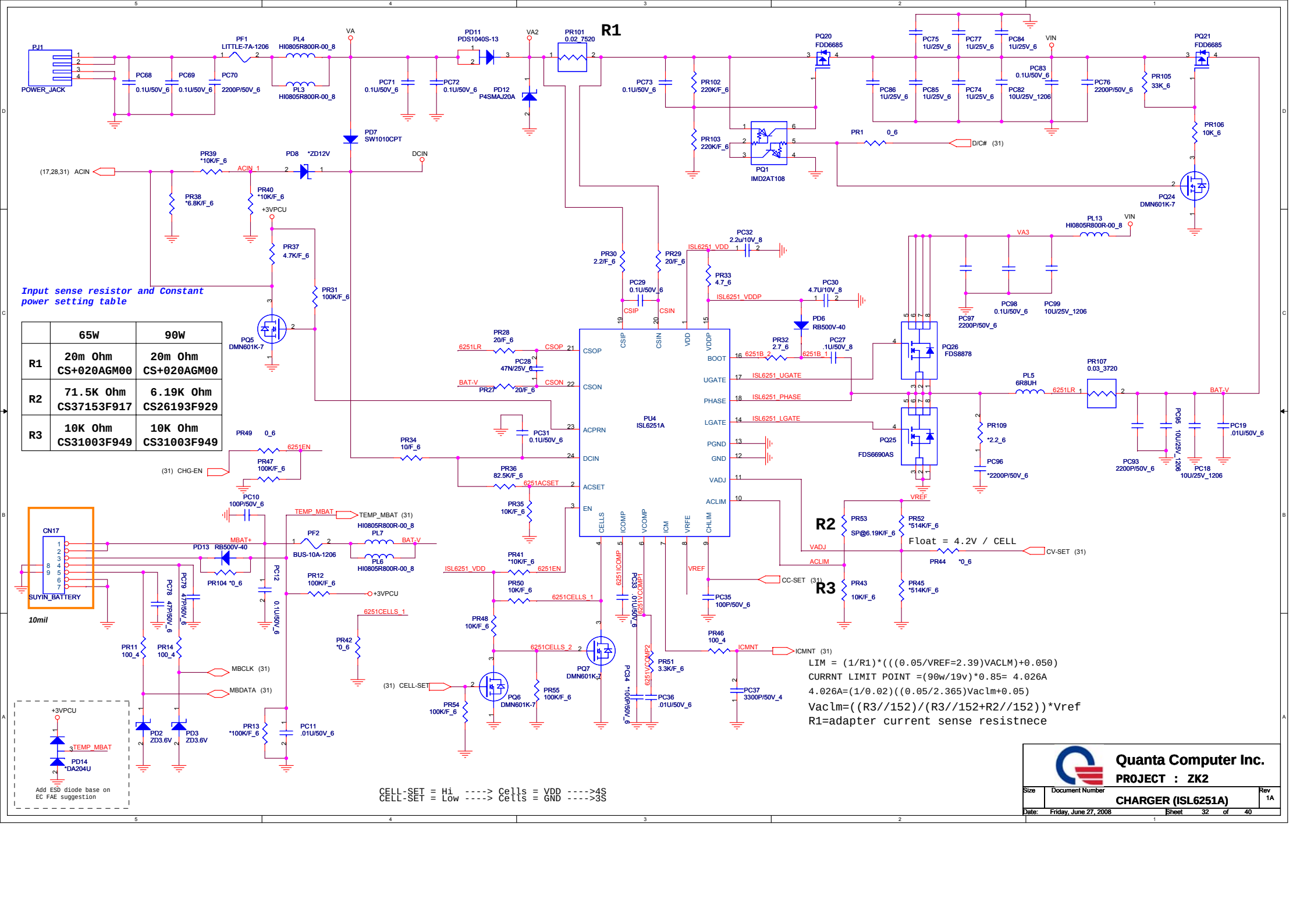


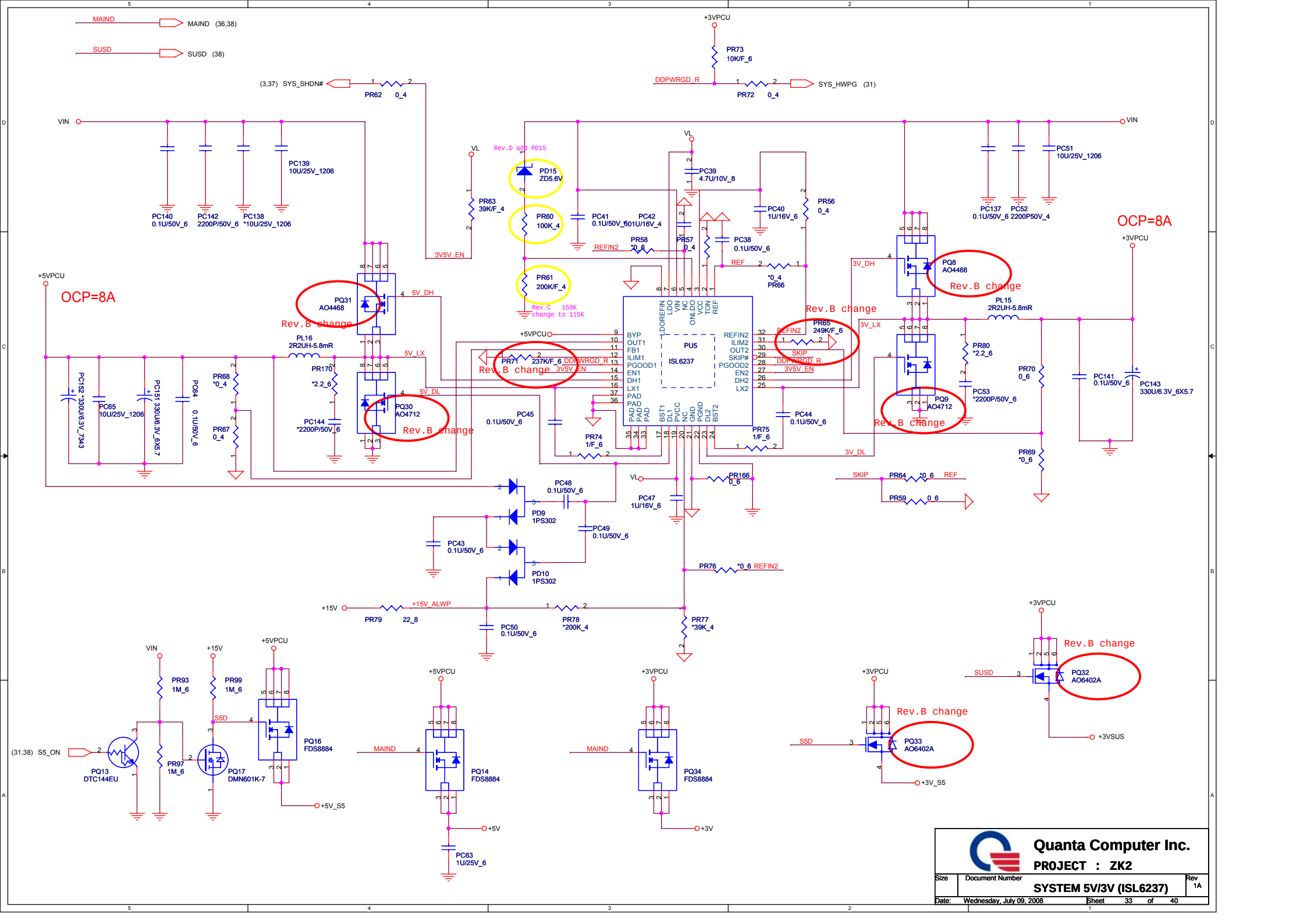
CIR

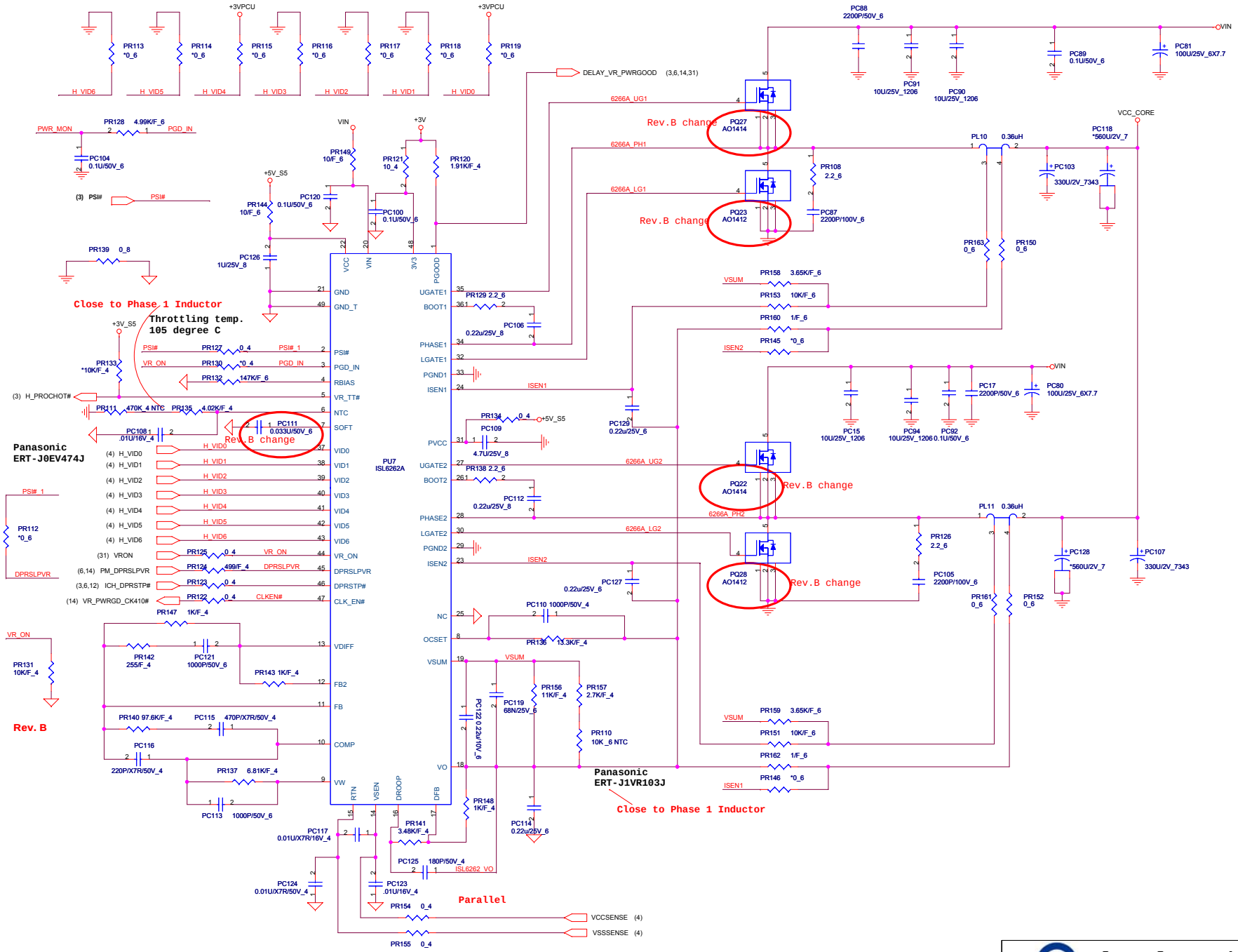


INTERNAL KEYBOARD STRIP SET

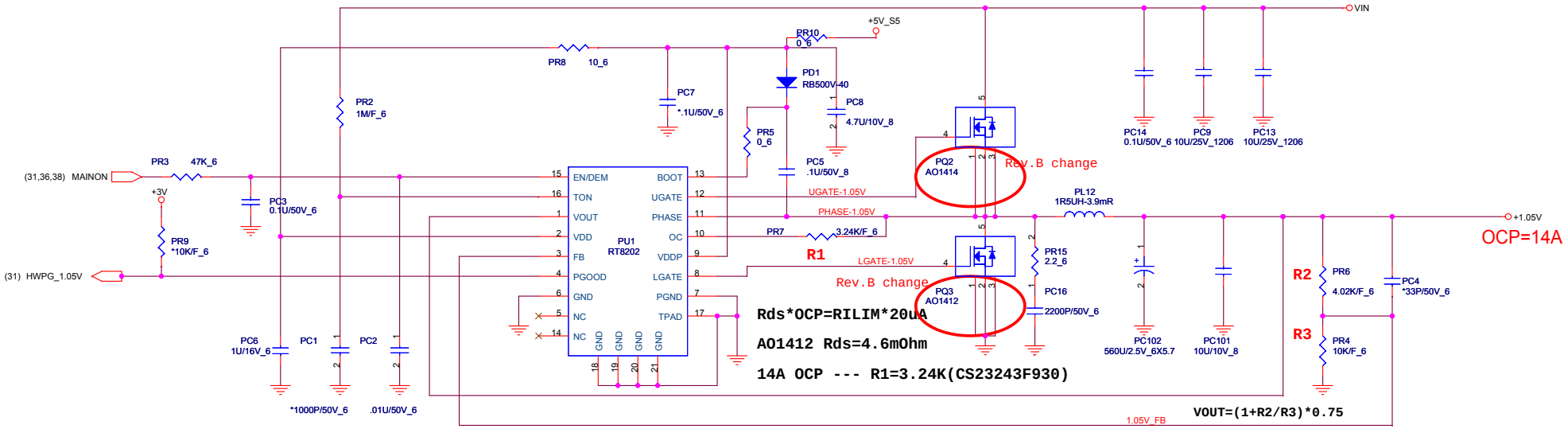
Quanta Computer Inc.			
PROJECT : ZK2			
Size	Document Number		Rev
	WPCE775C_0DG & FLASH		3B
Date: Friday, June 27, 2008		Sheet 31 of 39	


R1
R2
R3
PU4 ISL6251A
Input sense resistor and Constant power setting table
65W
90W
R1
20m Ohm CS+020AGM00
20m Ohm CS+020AGM00
R2
71.5K Ohm CS37153F917
6.19K Ohm CS26193F929
R3
10K Ohm CS31003F949
10K Ohm CS31003F949
Float = 4.2V / CELL
LIM = (1/R1)*(((0.05/VREF=2.39)VACLM)+0.050)
CURRNT LIMIT POINT =(90w/19v)*0.85= 4.026A
4.026A=(1/0.02)((0.05/2.365)Vaclm+0.05)
Vaclm=((R3//152)/(R3//152+R2//152))*Vref
R1=adapter current sense resistnece
CELL-SET = Hi ----> Cells = VDD ---->4S
CELL-SET = Low ----> Cells = GND ---->3S
Add ESD diode base on EC FAE suggestion
Quanta Computer Inc.
PROJECT : ZK2
CHARGER (ISL6251A)
Rev 1A
Friday, June 27, 2008
Sheet 32 of 40


MAIND
MAIND (36,38)
SUSD
SUSD (38)
(3,37) SYS_SHDN#
PR62 0_4
+3VPCU
PR73 10K/F_6
DDPWRGD_R
PR72 0_4
SYS_HWPG (31)
VIN
PC139 10U/25V_1206
PC140 0.1U/50V_6
PC142 2200P/50V_6
PC138 *10U/25V_1206
VL
Rev.D add PD15
PD15 ZD5.6V
PR63 39K/F_4
PR60 100K_4
PR61 200K/F_4
Rev.C 150K change to 115K
3V5V_EN
PC41 0.1U/50V_6
PC42 01U/16V_4
PC39 4.7U/10V_8
PC40 1U/16V_6
PR56 0_4
PR57 0_4
PC38 0.1U/50V_6
PR58 *0_6
REFIN2
REF
*0_4 PR66
PC137 0.1U/50V_6
PC52 2200P50V_4
PC51 10U/25V_1206
OCP=8A
+5VPCU
PQ31 AO4468
5V_DH
Rev.B change
PL16 2R2UH-5.8mR
5V_LX
PR71 237K/F_6
DDPWRGD_R
3V5V_EN
PU5 ISL6237
BYP
OUT1
FB1
ILIM1
PGOOD1
EN1
DH1
LX1
PAD
PAD
PAD
PAD
PAD
BST1
DL1
PVCC
NC
PGND
DL2
BST2
LDOREFIN
LDO
VIN
NC
ONLOC
VCC
TON
REF
REFIN2
ILIM2
OUT2
SKIP#
PGOOD2
EN2
DH2
LX2
PR65 249K/F_6
SKIP
PQ30 AO4712
5V_DL
PC45 0.1U/50V_6
PR74 1/F_6
PR75 1/F_6
PC44 0.1U/50V_6
3V_DH
3V_LX
3V_DL
PQ8 AO4468
PQ9 AO4712
PL15 2R2UH-5.8mR
PR80 *2.2_6
PC53 *2200P/50V_6
PR70 0_6
PR69 *0_6
PC141 0.1U/50V_6
PC143 330U/6.3V_6X5.7
PC152 *330U/6.3V_7343
PC65 10U/25V_1206
PC151 330U/6.3V_6X5.7
PC64 0.1U/50V_6
PR68 *0_4
PR67 0_4
PR170 *2.2_6
PC144 *2200P/50V_6
PC48 0.1U/50V_6
PD9 1PS302
PC49 0.1U/50V_6
PC43 0.1U/50V_6
PD10 1PS302
PC47 1U/16V_6
PR166 0_6
PR64 *0_6
PR59 0_6
PR76 *0_6
REFIN2
+15V
+15V_ALWP
PR79 22_8
PR78 *200K_4
PC50 0.1U/50V_6
PR77 *39K_4
PR93 1M_6
PR99 1M_6
S5D
(31,38) S5_ON
PQ13 DTC144EU
PR97 1M_6
PQ17 DMN601K-7
PQ16 FDS8884
+5V_S5
MAIND
PQ14 FDS8884
PC63 1U/25V_6
+5V
PQ34 FDS8884
+3V
PQ33 AO6402A
+3V_S5
PQ32 AO6402A
+3VSUS
Quanta Computer Inc.
PROJECT : ZK2
Size
Document Number
SYSTEM 5V/3V (ISL6237)
Rev 1A
Date: Wednesday, July 09, 2008
Sheet 33 of 40



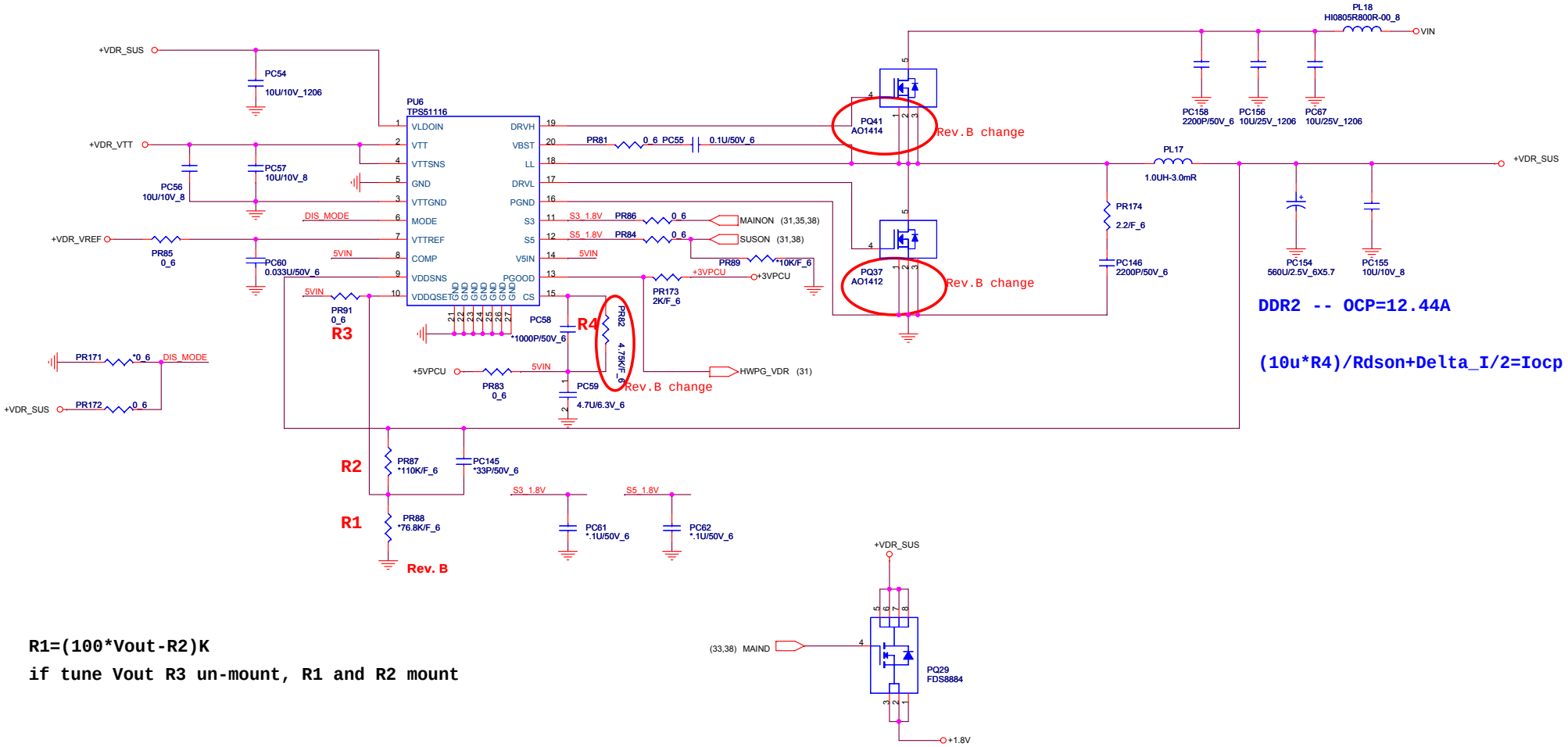
Quanta Computer Inc.			
PROJECT : ZK2			
Size	Document Number	CPU CORE(ISL6266)	Rev 1A
Date: Friday, June 27, 2008		Sheet 34 of 40	



TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

Quanta Computer Inc.		
PROJECT : ZK2		
Size	Document Number	Rev
	VTT 1.05V (RT8202)	1A
Date: Friday, June 27, 2008	Sheet 35 of 40	

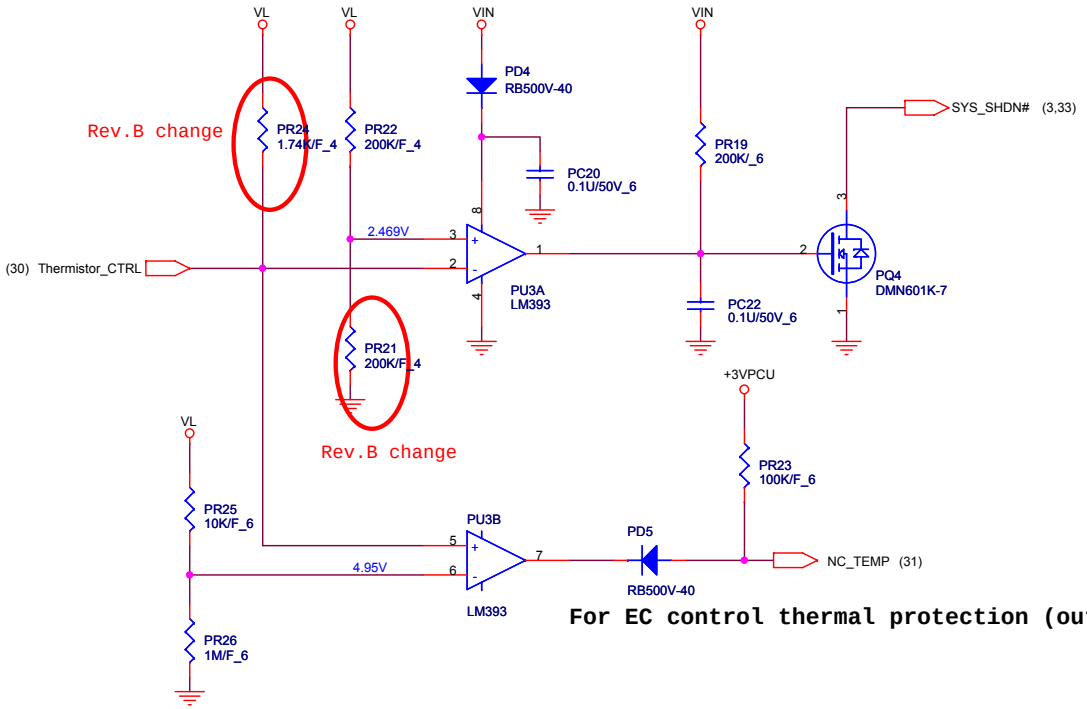


R1=(100*Vout-R2)K

if tune Vout R3 un-mount, R1 and R2 mount

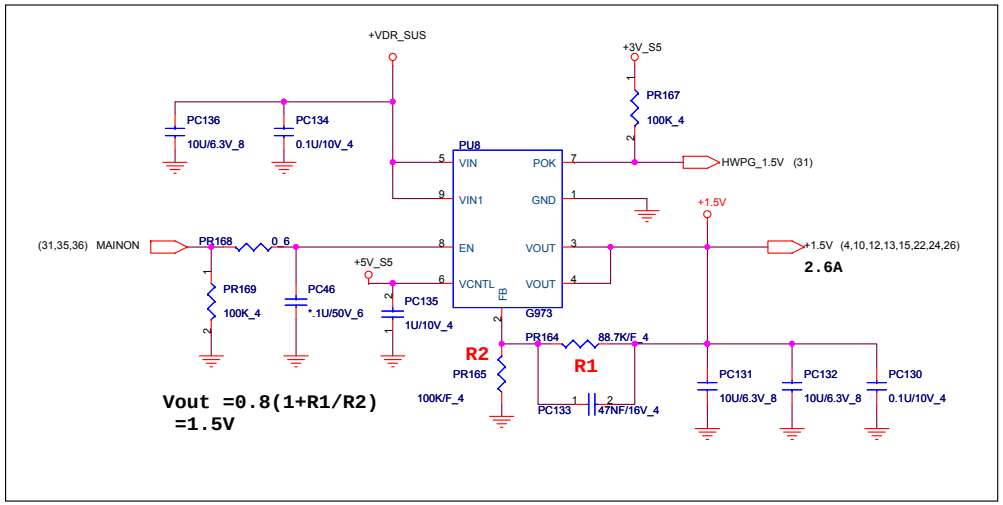
Quanta Computer Inc.		
PROJECT : ZK2		
Size	Document Number	Rev
	VDR (TPS51116)	1A
Date: Friday, June 27, 2008	Sheet 36 of 40	

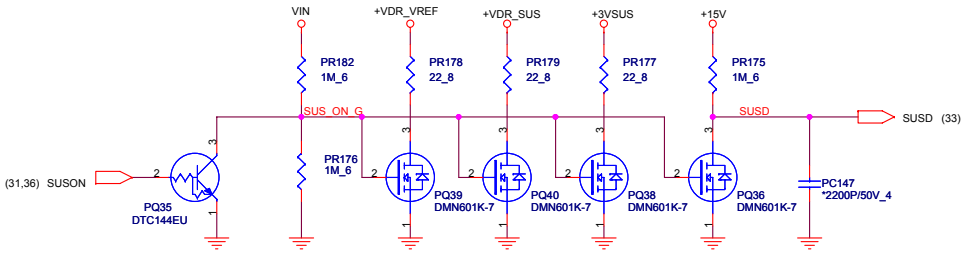
thermal protection

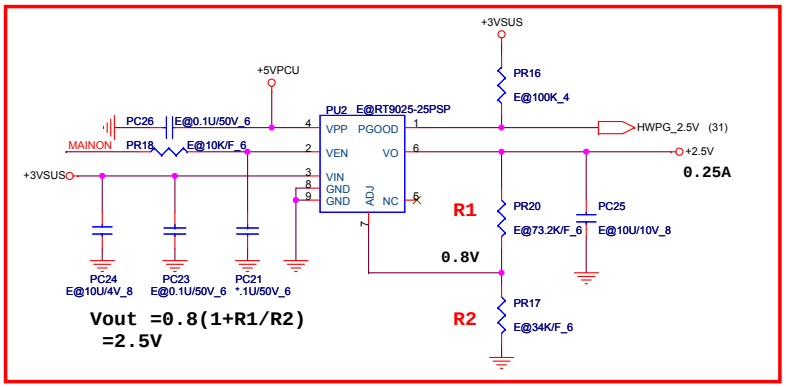


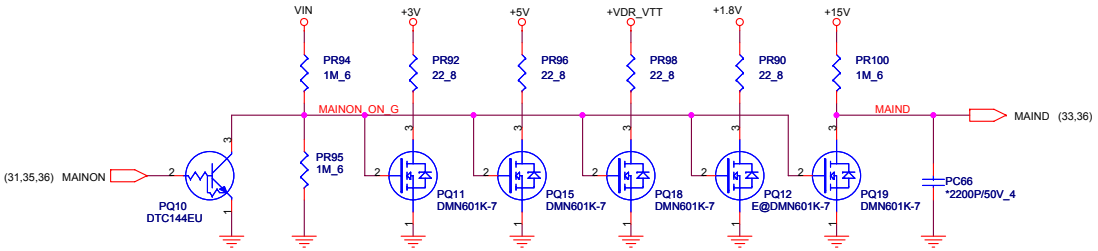
For EC control thermal protection (output 3.3V)

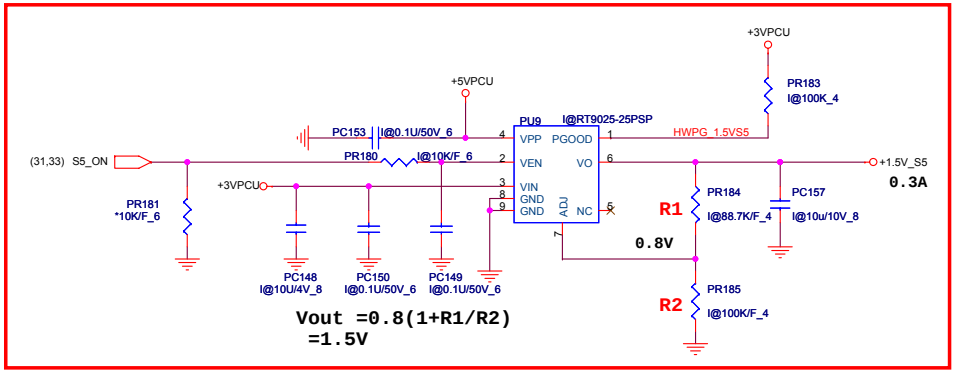
Quanta Computer Inc.		
PROJECT : ZK2		
Size	Document Number: Thermal protect	Rev 1A
Date: Friday, June 27, 2008	Sheet 37 of 40	











Quanta Computer Inc.

PROJECT : ZK2

Size	Document Number	Rev
	Discharge (2.5V/1.5V)	1A

Date: Friday, June 27, 2008 Sheet 38 of 40

Model	REV	CHANGE LIST	MODEL	ZK2	
				FROM	To
ZK2 MB	1A	FIRST RELEASED: E200803-5424 (PCB: DA0ZK2MB6A0)		X	1A
				X	1A
	2A	Page10 : Correct LVDS power of NorthBridge to +VDD_SUS		1A	2A
		Page12 : Change 32.768KHz (Y2) to normal type(H15)		1A	2A
		Change RTC battery connector type (CN34) to DFHD02MR311		1A	2A
		Swap SATA port between port-1 (ODD) and port-4 (2ND HDD)		1A	2A
		Page17 : Remove power short-pad for MXM		1A	2A
		Page18 : Change LCD power input capacitor (C27) to 2.2uf		1A	2A
		Change array Resistor (RP1) to two resistor (R617/R618) for EMI		1A	2A
		Page19 : Change all HDMI switch solution to Parade (PS8122), and connector type to DIP type		1A	2A
		Page20 : Correct LAN Rbias (R353) to 2.32Kohm to improve performance and signal quality		1A	2A
		Correct X'tal capacitor (C351/C352) to 33pF for 25MHz		1A	2A
		Page21 : Change LAN tranformer for EMI and correct RJ45 connector pin definition for wrong connect		1A	2A
		Page22 : Change L42 to 0ohm resistor		1A	2A
		Page23 : Add two 0.1uf return-path capacitor (C660/C661) for HDMI switch		1A	2A
		Page24 : Change L&C solution for SPDIF and DMIC EMI issue		1A	2A
		Page25 : Correct SPDIF (CN25) pin definition		1A	2A
		Page28 : Change power/B power source to +3V only		1A	2A
		Reserve +3V power source for MMB function		1A	2A
		Page29 : Modify eSATA controller (U13) swing/EQ/de-emphasis setting for signal quality, and correct eSATA connector type		1A	2A
		Move USB power switch to USB/B		1A	2A
		Page29 : Change finger-printer power source to +3VSUS		1A	2A
		Power change items		1A	2A
		Page32 : [PR53] 6.19Kohm(CS26193F929) for MXM(90W ADP)		1A	2A
		71.5Kohm(CS37153F917) for UMA(60W ADP)		1A	2A
		Page33 : 1. Change PQ31/PQ8 from FDS8878(BAM88780020) to AO4468(BAM44680003)		1A	2A
		2. Change PQ30/PQ9 from FDS6690AS(BAM66900022) to AO4712 (BAM47120000)		1A	2A
		3. Change PQ32/PQ33 from FDC653 (BAM653N0Z03) to AO6402A (BAM64020000)		1A	2A
		4. Change PR61 from 150K/F_4(CS41502FB18) to 150K/K_4(CS41502JB10)		1A	2A
		5. Change PR71 from 178K/F_6 (CS41783F918) to 237K/F_6 (CS42373F911)		1A	2A
		6. Change PR65 from 196K/F_6 (CS41963F916) to 249K/F_6 (CS42493F914)		1A	2A
		Page34 : 1. Change PQ27/PQ22 from TPCA8023-H(BAM80230000) to AO1414 (BAM14140001)		1A	2A
		2. Change PQ28/PQ23 from TPCA8019-H (BAM80190000) to AO1412 (BAM14120000)		1A	2A
		3. Change PC111 from 0.022U/50V_6 (CH3226K1901) to 0.033U/50V_6 (CH3336J1900)		1A	2A
		Page35 : 1. Change PQ2 from TPCA8023-H (BAM80230000) to AO1414 (BAM14140001)		1A	2A
		2. Change PQ3 from TPCA8019-H (BAM80190000) to AO1412 (BAM14120000)		1A	2A
		Page36 : 1. Change PQ41 fromTPCA8023-H (BAM80230000) to AO1414 (BAM14140001)		1A	2A
		2. Change PQ37 from TPCA8019-H (BAM80190000) to AO1412 (BAM14120000)		1A	2A
		3. Change PR82 from 5.62K/F_6 (CS25623F914) to 4.75K/F_6 (CS24753F919)		1A	2A
		Page37 : 1. Change PR21 from 196K/F_4 (CS41962FB01) to 200K/F_4 (CS42002FB12)		1A	2A
		2. Change PR24 from 1.43K/F_4 (CS21432FB00) to 1.74K/F_4 (CS21742FB00)		1A	2A
	3A	Page2 : no mount 0.1uf (C475/C492/C471)		2A	3A
		Page4 : no mount 0.1uf (C152)		2A	3A
		Page6 : remove 0 ohm (R160/R390/R402/R159), and connect them directly		2A	3A
		Page12 : remove 0 ohm (R498/R249/R487), and connect them directly		2A	3A
		Swap Main HDD to port-0, and 2nd HDD to port-4		2A	3A
		Page13 : remove 0 ohm (R198), and connect them directly		2A	3A
		Swap USB port2 to external USB, and port-7 to Cardreader		2A	3A
		Page14 : remove 0 ohm (R186/R185/R466/R235/R506), and connect them directly.		2A	3A
		no mount 0.1uf (C170/C448)		2A	3A
		Page16 : no mount 0.1uf (C301/C552)		2A	3A
		Page17 : reserve 0 ohm (R626) from MXM to EC (EC_THERM#)		2A	3A
		no mount 0.1uf (C489)		2A	3A
		no mount Q21/Q24 and bypass from 0ohm (R378/R381), pull-up 2K ohm to +3V for MXM sku		2A	3A
		Page18 : Change L6/7/8 to BLM18BA470SN1D		2A	3A
		Change U4 to AL004280001 (AAT4280-4) part		2A	3A
		Remove 0 ohm (R22), and connect directly		2A	3A
		Change CN3 to DFWF40MR000 for SMT request		2A	3A
		Change R42 from 330 ohm to 180 ohm (CS11802JB15)		2A	3A
		Page19 : Use 100 ohm (R619/R620/R621/R622) and 1pf (C656/C657/C658/C659) for HDMI EMI request		2A	3A
		Reserve C662/Q43/Q44/R119/R126, and bypass 0ohm (R627/R628)		2A	3A
		Page20 : remove 0ohm (R5/R9/R357) and connect directly		2A	3A
		Page21 : Change L1/L2 (BLM18PG181SN1D) to increase current rating		2A	3A
		Change transformer to GST-5009		2A	3A
		Change R13~R16 from 75ohm 0402 to 0805 size		2A	3A
		no mount 0.1uf (C350)		2A	3A
		Swap LAN LED color connect (green: linking/orange:active)		2A	3A
		Page22 : Remove R296/R292/R328/L42/R298 and connect directly		2A	3A
		no mount 0.1uf (C247/C270/C268)		2A	3A
		Page23 : Change main (CN27) and 2nd (CN30) HDD footprint for M/E request		2A	3A
		no mount 0.1uf (C532/C535/C260/C261/C440/C441)		2A	3A
		Change 0.1uf to 0.01uf (C630/C147/C317/C46/C661/C663/C313/C314/C556/C373/C451/C180)		2A	3A
		Page24 : remove 0ohm (R574) and connect directly		2A	3A
		Page26 : no mount 0.1uf (C538/C537/C275)		2A	3A
		Page27 : no mount 0.1uf (C281/C198/C279)		2A	3A
		Page28 : Add AC-IN LED-Oh function (Q48/Q50)		2A	3A
		Add PWRLED/SUSLED function on Power/B (Q47/Q49/R624/R625)		2A	3A
		Change R47/R49 from 0ohm to 100ohm for synaptic MMB		2A	3A
		Change LED1 from Green/Amber to Blue/Amber		2A	3A
		Page29 : Change C537/C528 from 470P 10uF to 1uF for power team suggestion		2A	3A
		Change e-SATA connecotr (CN22)		2A	3A
		Update incorrect hole29/hoe34 footprint		2A	3A
		Page30 : no mount 33pf (C33/C34)		2A	3A
		Remove L24/L25/L26 and connect directly		2A	3A
		Page31 : no mount 0.1uf (C60/C65/C400)		2A	3A
		Change SW1 to short-pad (G3) for easy power-on		2A	3A
		Change U38 to everlight part (IRM-V538-TR1)		2A	3A
	3B	Page5 : update NB p/n to AJSLB940T04 (GM45), AJSLB070T06 (PM45)		3A	3B
		Page6 : remove 0 ohm (R167), and connect them directly		3A	3B
		Page10 : Add 10uf capacitor (C665/C393) for CRT flicker issue		3A	3B
		Page12 : remove 0 ohm (R247), and connect them directly		3A	3B
		update SB p/n to AJSLB0Q0T03		3A	3B
		Page14 : Add panle_ID0 (GPIO19)/1 (GPIO20) on SB, and pull-up 10Kohm (R629/R630) to +3V near LCD connector (CN3)		3A	3B
		Change Board_ID2 to GPIO21, and Board_ID3 to GPIO22		3A	3B
		Remove R516		3A	3B
		Page17 : no mount 4.7uf capacitor (C481)		3A	3B
		remove 0 ohm (R176/R472), and connect directly		3A	3B
		Page18 : delete no-dock CRT resistor, no mount 0.1uf (C49)		3A	3B
		remove 0 ohm (R617/618), and connect directly for USB		3A	3B
		Add panel_ID0 (CN3.35) and panel_ID1 (CN3.30)		3A	3B
		Page19 : reserve 100 ohm (R634/R635/R636/R637)		3A	3B
		Remove 0 ohm (R59/R64) and connect directly		3A	3B
		Page20 : remove 0ohm (R355) and connect directly		3A	3B
		Page21 : delete no-dock LAN resistor		3A	3B
		Change R344/R352 to 220 0805 size for RMA request		3A	3B
		Page22 : Remove RP11/RP10/R545 and connect directly		3A	3B
		Reserve Q51 and bypass 0ohm (R631)		3A	3B
		Add 10uf (C666) for TV		3A	3B
		Page23 : Update new footprint (CN30) library issue		3A	3B
		Page24 : no mount 0.1uf (C591) and add 10uf (C593)		3A	3B
		Change C601 from 4.7uf to 10uf		3A	3B
		Page25 : Change MUTE# function circuit to AND gate (U42), and reserve bypass 0ohm (R638)		3A	3B
		remove 0 ohm bridge resistor (R540/R546/R552/R553/R559) to reduce noise		3A	3B
		Change R570 from 20Kohm to 12.4Kohm for subwoofer gain issue		3A	3B
		remove 0ohm (R575) and connect directly		3A	3B
		Change C623 from ADOGND to GND		3A	3B
		Change C518/C525 from 47pf to 470pf		3A	3B
		Page26 : Remove 0ohm (R271/R277) and connect directly		3A	3B
		Page28 : Use +3V power (R632) for MMB and Reserve +5V (R633)		3A	3B
		Add 1uf (C655) for +3V power		3A	3B
		Remove R45 and connect directly, reserve L61/C667 for EMI request		3A	3B
		Page29 : Remove 0ohm (R609/R610/R611/R612) and connect directly		3A	3B
		Increase 0.1mm width for Hole28/33/30/35		3A	3B
		Page30 : Change RP2 from +3VSUS to +3VPCU for EC engineer suggestion		3A	3B
		Remove 0ohm (RP7) and connect directly		3A	3B
		Change 2.2uf to 10uf (C367)		3A	3B
				3A	3B

Quanta Computer Inc.
PROJECT : ZK2

Size	Document Number	Rev
	Change list	3B

Date: Friday, June 27, 2008 Sheet 39 of 51

DOC NO.	PROJECT MODEL :	ZK2	APPROVED BY:		DATE:	2008/06/27
	PART NUMBER:		DRAWING BY:		REVISON:	3B