

# Compal Confidential

## NEW71/91 M/B Schematics Document

### Intel Arrandale Processor with DDRIII + Ixex Peak-M NV N11P-GV2H

2009-12-23

REV : 0 . 1

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2009/08/01	Deciphered Date	2010/08/01	Title Cover Page		
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				Custom	NEW71/91 M/B LA-5893P Schematic	0.1
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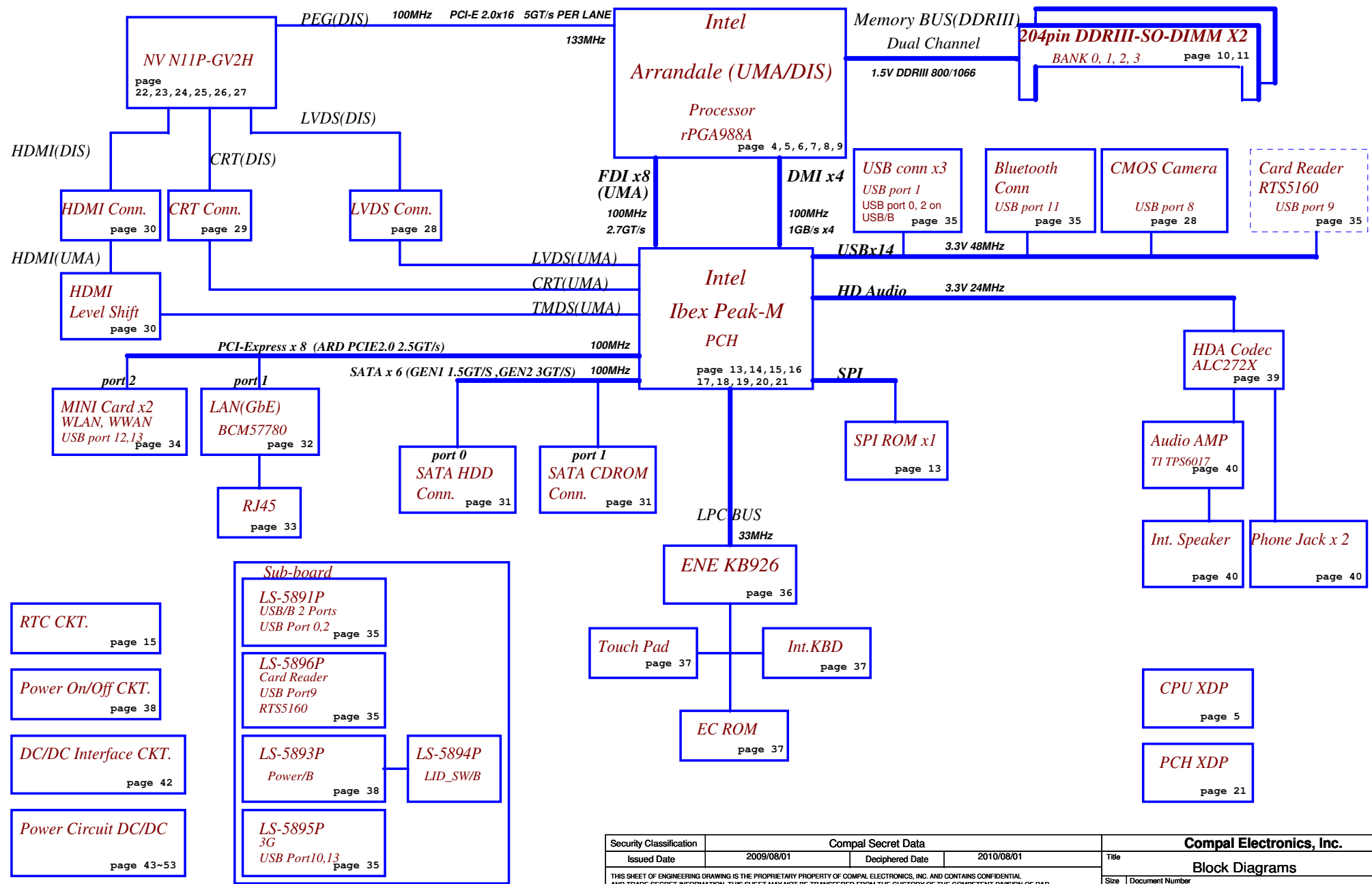
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Model Name : NEW71/91

File Name : LA5893P

Fan Control  
page 41

Clock Generator  
IDT: 9LVS3199AKLFT  
Realtek: RTM890N-631-VB-GRT  
133/120/100/96/14.318MHZ to PCH  
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## Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for Arrandale GPU (only for arrandaleCPU)	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.0VSDGPU	+1.0VSDGPU to +1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VTTP to +1.05VS_VTT switched power rail for ARD CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VTT to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VS to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+3V_LAN	+3VALW to +3V_LAN power rail for LAN	ON	ON	ON*
+3V	+3VALW to +3V power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5V	+5VALW to +5V switched power rail for PCH (Short resistor)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

## EC SM Bus1 address

## EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011Xb		

## PCH SM Bus address

Device	Address
Clock Generator (9LVS3199AKLFT, RTM890N-631-VB-GRT)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

BOM Config	
<b>NEW71 SKU DISCTETE ONLY</b>	BT@,3G@,DIS@,DIS ONLY@,NonSG@,71@,X7621@,XDP@
<b>NEW91 SKU DISCTETE ONLY</b>	BT@,3G@,DIS@,DIS ONLY@,NonSG@,91@,X7621@,XDP@

### VRAM BOM Config

**X7621@:** X76198BOL21 ALT. GROUP PARTS 1G SAM

**X7622@:** X76198BOL22 ALT. GROUP PARTS 1G HYN

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

## Board ID / SKU ID Table for AD channel

Board ID	Rb / Rd / Rf	V <sub>AD_BID min</sub>	V <sub>AD_BID typ</sub>	V <sub>AD_BID max</sub>
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

## BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

## BTO Option Table

BTO Item	BOM Structure
UMA	UMA@
UMA Only	UMA ONLY@
Discrete	DIS@
Discrete Only	DIS ONLY@
VRAM	X76@
Switchable	SG@
Connector	CONN@
3G	3G@
Blue Tooth	BT@
Unpop	@
XDP	XDP@
NonSG	NonSG@
NEW71	71@
NEW91	91@

### VRAM P/N:

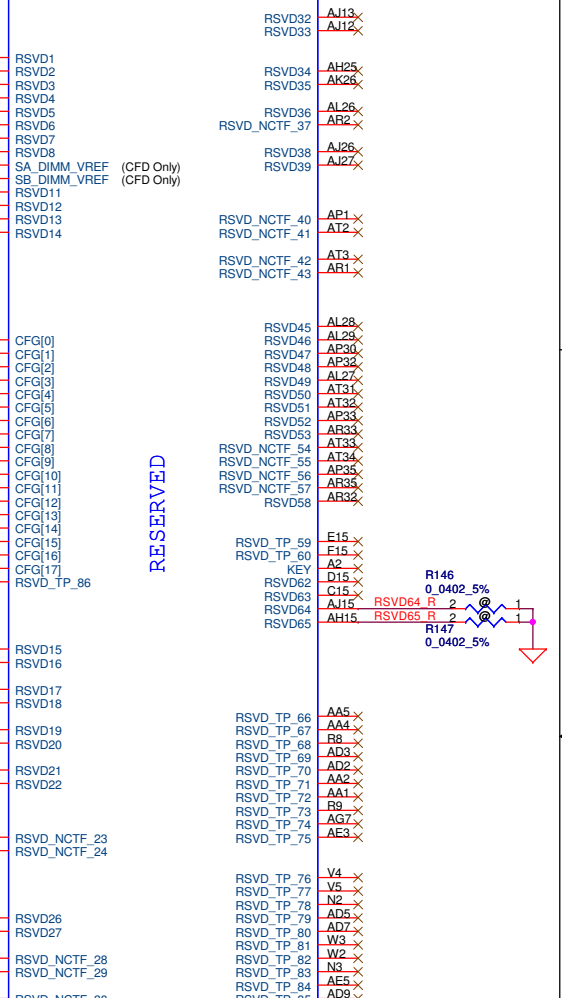
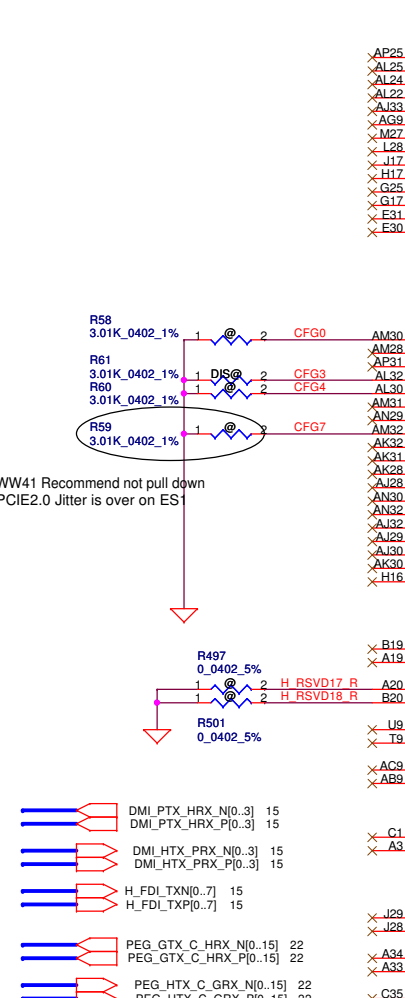
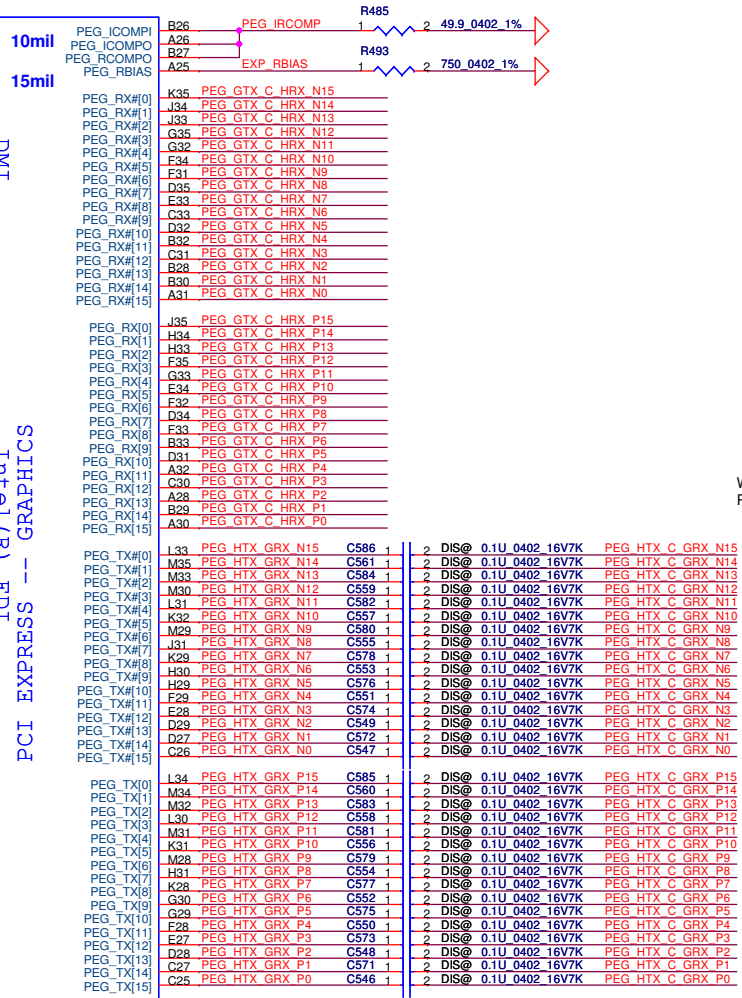
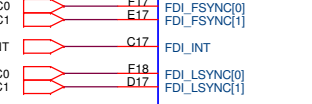
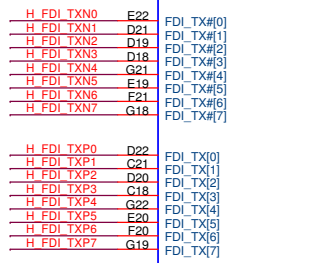
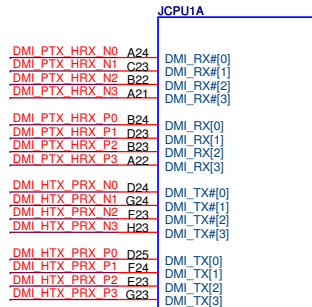
Samsung : SA000035720 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA ABO!)

Hynix : SA000032420 (S IC D3 64MX16 H5TG1G63BFR-12C FBGA ABO!)

## USB Port Table

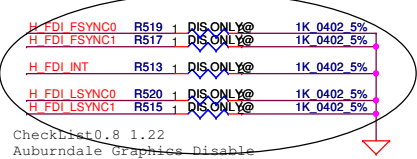
USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB/B (Right Side)
		1	USB Port (Left Side)
	UHCI1	2	USB/B (Right Side)
		3	
		4	
	UHCI2	5	
		6	
EHCI2	UHCI3	7	
		8	Camera
	UHCI4	9	Card Reader
		10	SIM Card
	UHCI5	11	Blue Tooth
		12	Mini Card(WLAN)
		13	Mini Card(GPS)

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### eDP Signals Mapping

eDP Signal	PEG Singals	Lane Reversal
eDP_TX0	PEG HTX_C_GRX_P15	PEG HTX_C_GRX_P0
eDP_TX#0	PEG HTX_C_GRX_N15	PEG HTX_C_GRX_N0
eDP_TX1	PEG HTX_C_GRX_P14	PEG HTX_C_GRX_P1
eDP_TX#1	PEG HTX_C_GRX_N14	PEG HTX_C_GRX_N1
eDP_TX2	PEG HTX_C_GRX_P13	PEG HTX_C_GRX_P2
eDP_TX#2	PEG HTX_C_GRX_N13	PEG HTX_C_GRX_N2
eDP_TX3	PEG HTX_C_GRX_P12	PEG HTX_C_GRX_P3
eDP_TX#3	PEG HTX_C_GRX_N12	PEG HTX_C_GRX_N3
eDP_AUX	PEG GTX_C_HRX_P13	PEG GTX_C_HRX_P2
eDP_AUX#	PEG GTX_C_HRX_N13	PEG GTX_C_HRX_N2
eDP_HPD#	PEG GTX_C_HRX_P12	PEG GTX_C_HRX_P3



**CFG0 - PCI-Express Configuration Select**

\*1: Single PEG  
0: Bifurcation enabled

**CFG3 - PCI-Express Static Lane Reversal**

\*1: Normal Operation  
0: Lane Numbers Reversed  
15 > 0, 14 > 1, ...

**CFG4 - Display Port Presence**

\*1: Disabled; No Physical Display Port attached to Embedded Display Port  
0: Enabled; An external Display Port device is connected to the Embedded Display Port

\*: Default

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10 DDR\_A\_D[0..63]  
 10 DDR\_A\_DM[0..7]  
 10 DDR\_A\_DQS[0..7]  
 10 DDR\_A\_DQS[0..7]  
 10 DDR\_A\_MA[0..15]

JCPU1C

DDR A D0 A10  
 DDR A D1 C10  
 DDR A D2 C7  
 DDR A D3 A7  
 DDR A D4 B10  
 DDR A D5 D10  
 DDR A D6 E10  
 DDR A D7 A8  
 DDR A D8 D8  
 DDR A D9 F10  
 DDR A D10 E9  
 DDR A D11 E2  
 DDR A D12 E9  
 DDR A D13 B7  
 DDR A D14 E7  
 DDR A D15 C6  
 DDR A D16 H9  
 DDR A D17 G8  
 DDR A D18 K7  
 DDR A D19 J8  
 DDR A D20 G7  
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 DDR A D23 J10  
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DDR SYSTEM MEMORY A

SA\_CK[0] AA6  
 SA\_CK#0 AA7  
 SA\_CKE[0] P7  
 SA\_CK[1] Y6  
 SA\_CK#1 Y5  
 SA\_CKE[1] P6  
 SA\_CS#0 CAE2  
 SA\_CS#1 CAE8  
 SA\_ODT[0] AD8  
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 SA\_DM[1] D7  
 SA\_DM[2] LH7  
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 SA\_DM[6] AN10  
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 SA\_DQS#1 C8  
 SA\_DQS#2 C9  
 SA\_DQS#3 CAH7  
 SA\_DQS#4 CAK9  
 SA\_DQS#5 CAP11  
 SA\_DQS#6 CAP11  
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 SA\_MA[2] AA8  
 SA\_MA[3] AA3  
 SA\_MA[4] V1  
 SA\_MA[5] AA9  
 SA\_MA[6] V8  
 SA\_MA[7] T1  
 SA\_MA[8] Y9  
 SA\_MA[9] U6  
 SA\_MA[10] AD4  
 SA\_MA[11] T2  
 SA\_MA[12] U3  
 SA\_MA[13] AG8  
 SA\_MA[14] T3  
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IC\_AUB\_CFD\_rPGA,R1P0  
 CONN@

11 DDR\_B\_D[0..63]  
 11 DDR\_B\_DM[0..7]  
 11 DDR\_B\_DQS[0..7]  
 11 DDR\_B\_DQS[0..7]  
 11 DDR\_B\_MA[0..15]

JCPU1D

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DDR SYSTEM MEMORY - B

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 SB\_CKE[0] M3  
 SB\_CK[1] V7  
 SB\_CK#1 V6  
 SB\_CKE[1] M2  
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 DDR B\_CLK0 11  
 DDR B\_CLK0# 11  
 DDR B\_CLK1 11  
 DDR B\_CLK1# 11  
 DDR B\_CKE0 11  
 DDR B\_CKE1 11  
 DDR B\_CS0# 11  
 DDR B\_CS1# 11  
 DDR B\_ODT0 11  
 DDR B\_ODT1 11  
 DDR B\_DM0  
 DDR B\_DM1  
 DDR B\_DM2  
 DDR B\_DM3  
 DDR B\_DM4  
 DDR B\_DM5  
 DDR B\_DM6  
 DDR B\_DM7  
 DDR B\_DQS#0  
 DDR B\_DQS#1  
 DDR B\_DQS#2  
 DDR B\_DQS#3  
 DDR B\_DQS#4  
 DDR B\_DQS#5  
 DDR B\_DQS#6  
 DDR B\_DQS#7  
 DDR B\_DQS0  
 DDR B\_DQS1  
 DDR B\_DQS2  
 DDR B\_DQS3  
 DDR B\_DQS4  
 DDR B\_DQS5  
 DDR B\_DQS6  
 DDR B\_DQS7  
 DDR B\_MA0  
 DDR B\_MA1  
 DDR B\_MA2  
 DDR B\_MA3  
 DDR B\_MA4  
 DDR B\_MA5  
 DDR B\_MA6  
 DDR B\_MA7  
 DDR B\_MA8  
 DDR B\_MA9  
 DDR B\_MA10  
 DDR B\_MA11  
 DDR B\_MA12  
 DDR B\_MA13  
 DDR B\_MA14  
 DDR B\_MA15

IC\_AUB\_CFD\_rPGA,R1P0  
 CONN@

10 DDR\_A\_BS0  
 10 DDR\_A\_BS1  
 10 DDR\_A\_BS2

DDR A BS0 AC3  
 DDR A BS1 AB2  
 DDR A BS2 U7

SA\_BS[0]  
 SA\_BS[1]  
 SA\_BS[2]

10 DDR\_A\_CAS#  
 10 DDR\_A\_RAS#  
 10 DDR\_A\_WE#

DDR A CAS# AE1C  
 DDR A RAS# AB3C  
 DDR A WE# AE9C

SA\_CAS#  
 SA\_RAS#  
 SA\_WE#

11 DDR\_B\_BS0  
 11 DDR\_B\_BS1  
 11 DDR\_B\_BS2

DDR B BS0 AB1  
 DDR B BS1 W5  
 DDR B BS2 R7

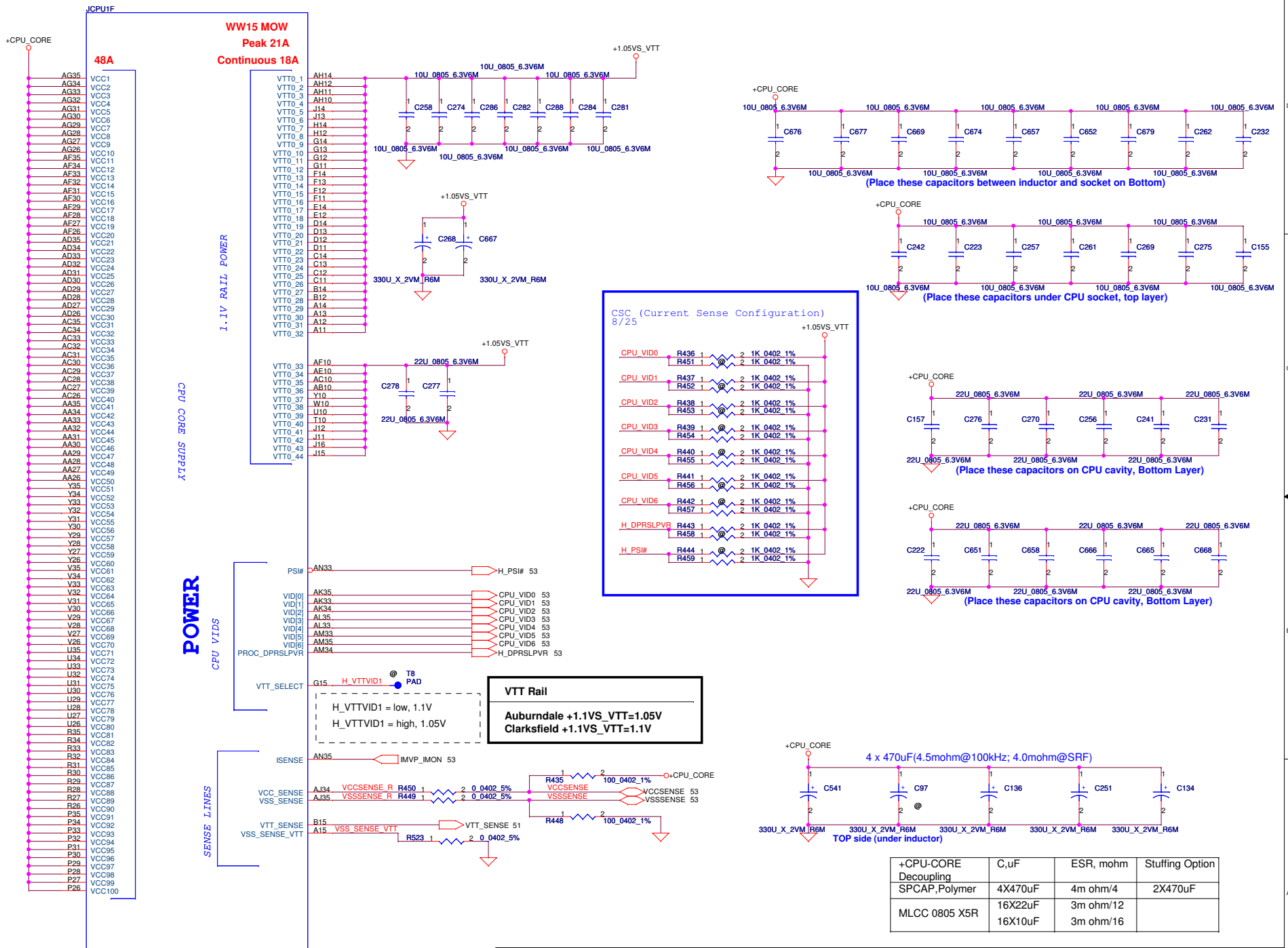
SB\_BS[0]  
 SB\_BS[1]  
 SB\_BS[2]

11 DDR\_B\_CAS#  
 11 DDR\_B\_RAS#  
 11 DDR\_B\_WE#

DDR B CAS# AC5C  
 DDR B RAS# Y7C  
 DDR B WE# AC6C

SB\_CAS#  
 SB\_RAS#  
 SB\_WE#

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Date:	Tuesday, December 22, 2009	Sheet	6	of	56



**CSC (Current Sense Configuration) 8/25**

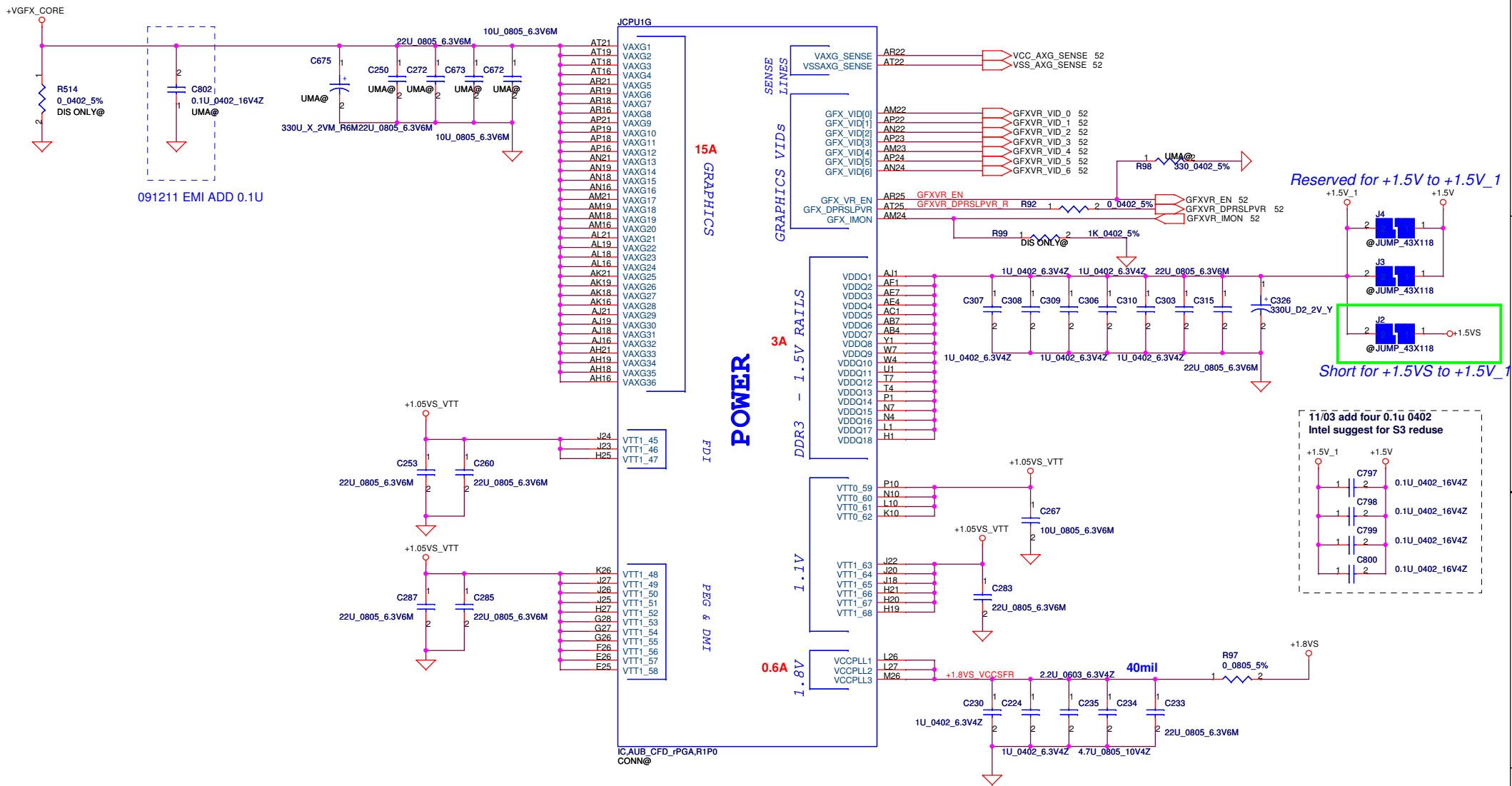
CPU_VID0	R436	1	2	1K	0402	1%
	R451	1	2	1K	0402	1%
CPU_VID1	R437	1	2	1K	0402	1%
	R452	1	2	1K	0402	1%
CPU_VID2	R438	1	2	1K	0402	1%
	R453	1	2	1K	0402	1%
CPU_VID3	R439	1	2	1K	0402	1%
	R454	1	2	1K	0402	1%
CPU_VID4	R440	1	2	1K	0402	1%
	R455	1	2	1K	0402	1%
CPU_VID5	R441	1	2	1K	0402	1%
	R456	1	2	1K	0402	1%
CPU_VID6	R442	1	2	1K	0402	1%
	R457	1	2	1K	0402	1%
H_DPRSLPVR	R443	1	2	1K	0402	1%
	R458	1	2	1K	0402	1%
H_PSI#	R444	1	2	1K	0402	1%
	R459	1	2	1K	0402	1%

**VTT Rail**

Auburdale +1.1VS\_VTT=1.05V  
 Clarksfield +1.1VS\_VTT=1.1V

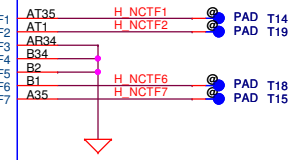
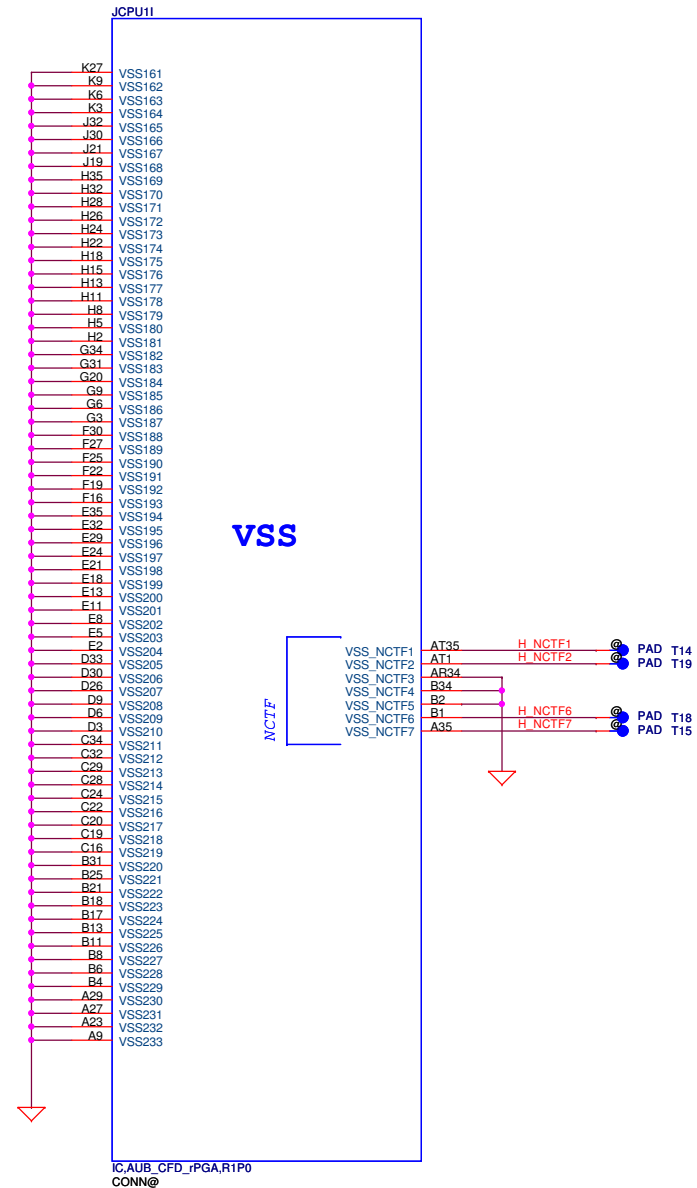
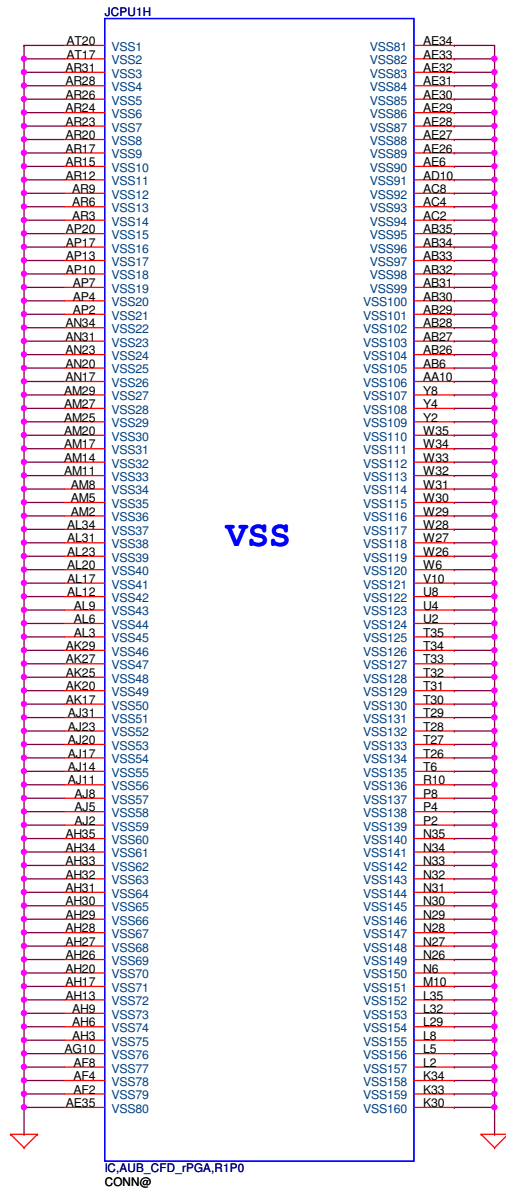
+CPU-CORE Decoupling	C, uF	ESR, mohm	Stuffing Option
SPCAP, Polymer	4X470uF	4m ohm/4	2X470uF
MLCC 0805 X5R	16X22uF	3m ohm/12	
	16X10uF	3m ohm/16	

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Size	Document Number	Customer		Rev	
Date:	NEW71/91 M/B LA-5893P Schematic	Date:		0.1	
Tuesday, December 22, 2009		Tuesday, December 22, 2009		Sheet 8 of 56	



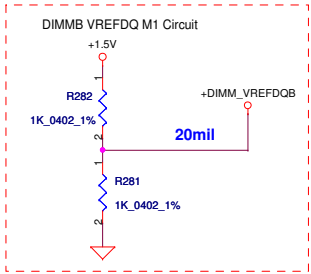
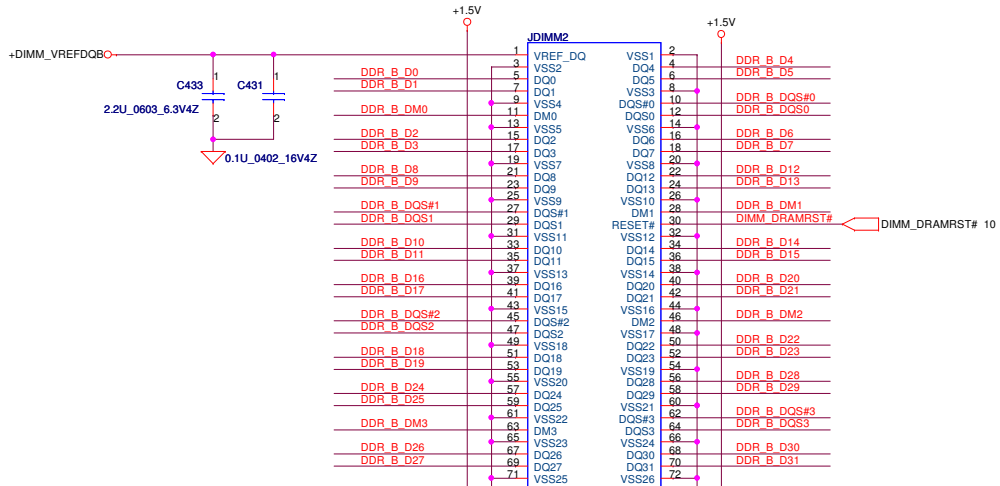


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Size	Document Number	Customer		Rev	
	NEW71/91	M/B LA-5893P Schematic		0.1	
Date:	Friday, December 18, 2009	Sheet	9	of 56	



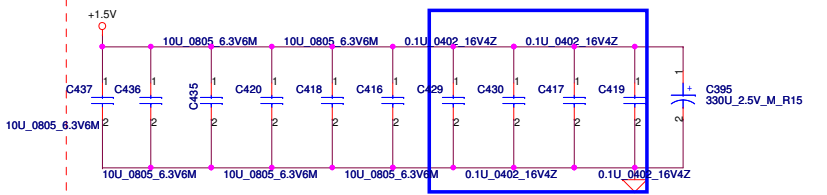
- 6 DDR\_B\_DQS#0[0..7]
- 6 DDR\_B\_D0[0..63]
- 6 DDR\_B\_DM[0..7]
- 6 DDR\_B\_DQS#0[0..7]
- 6 DDR\_B\_MA[0..15]

2008/9/8 #400755  
 Calpella Clarkstead  
 DDR3 SO-DIMM  
 VREFDQ Platform  
 Design Guide Change Details

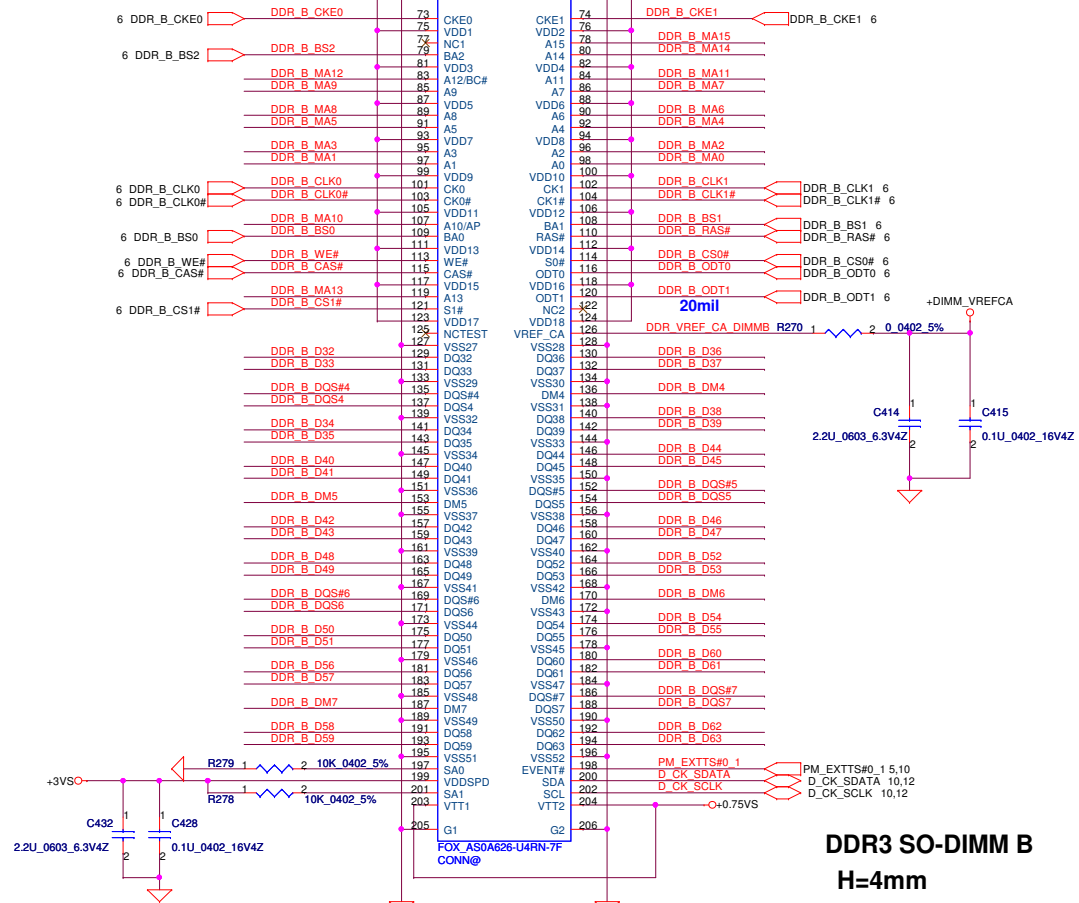
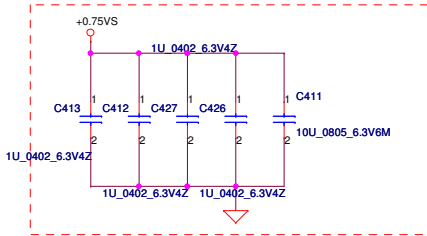


**Layout Note:**  
Place near JDIMM2

**Layout Note:** Place these 4 Caps near Command and Control signals of DIMMB



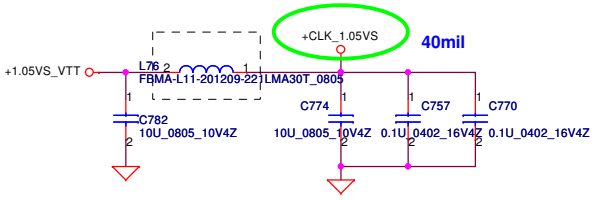
**Layout Note:**  
Place near JDIMM2.203 & JDIMM2.204



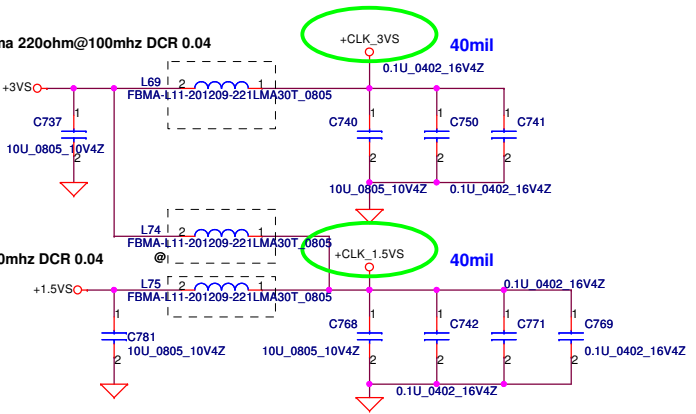
**DDR3 SO-DIMM B  
H=4mm**

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Issued Date	2009/08/01	Deciphered Date	2010/08/01	DDRIII-SODIMM SLOT2
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Customer	NEW71/91 M/B LA-5893P Schematic	Size	Document Number	Rev
Date	Tuesday, December 22, 2009	Sheet	11	of 56

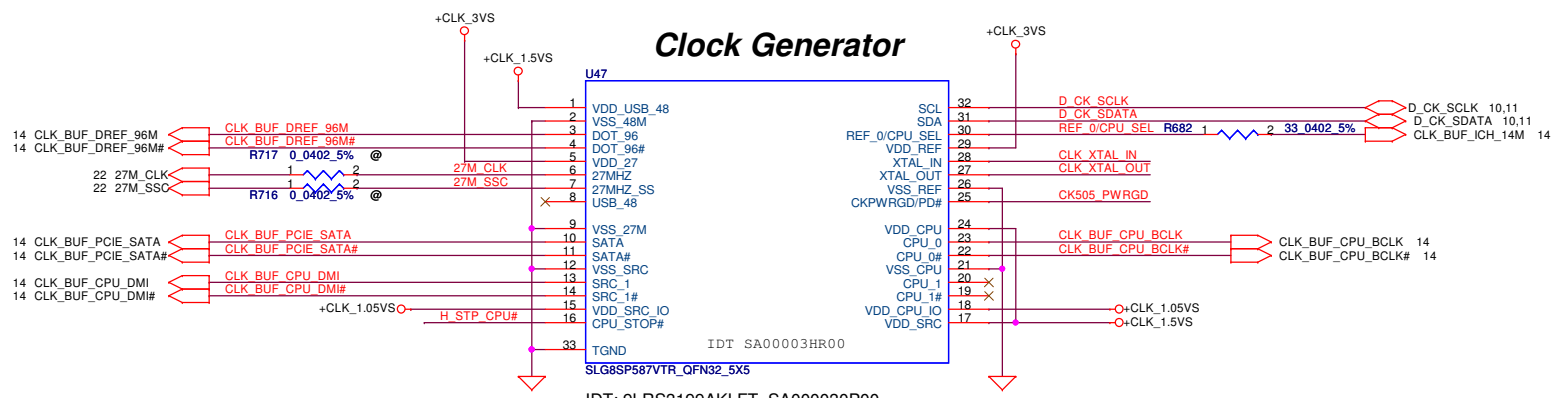
SM010014520 3000ma 220ohm@100mhz DCR 0.04



SM010014520 3000ma 220ohm@100mhz DCR 0.04



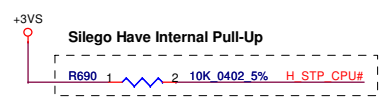
SM010014520 3000ma 220ohm@100mhz DCR 0.04



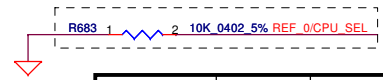
**Clock Generator**

IDT: 9LRS3199AKLFT, SA00003P00  
 SILEGO: SLG8SP587V(WF), SA00002XY10  
 Low Power:  
 IDT: 9LVS3199AKLFT, SA00003HR00  
 Realtek: RTM890N-631-VB-GRT, SA00003HQ10

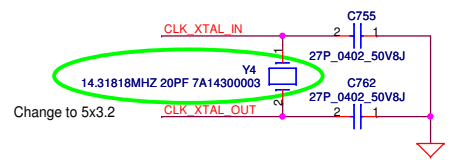
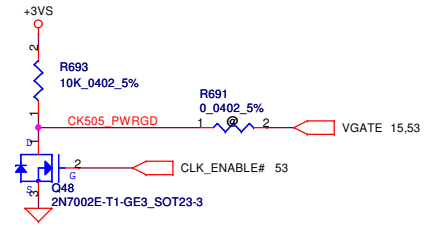
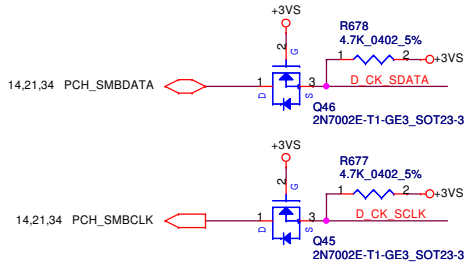
IDT 9LVS3199AKLFT NC



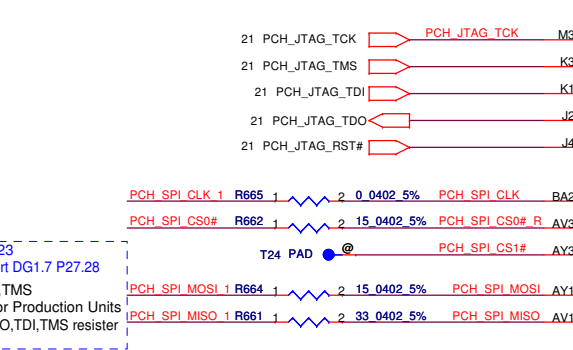
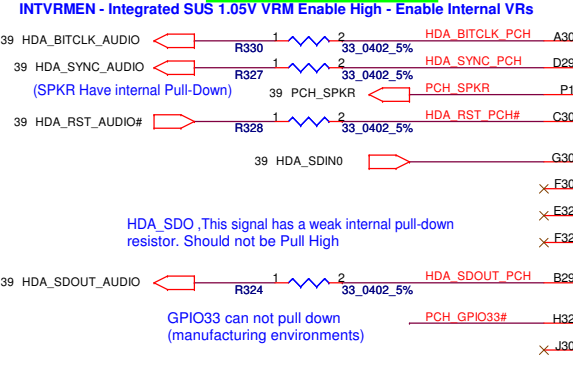
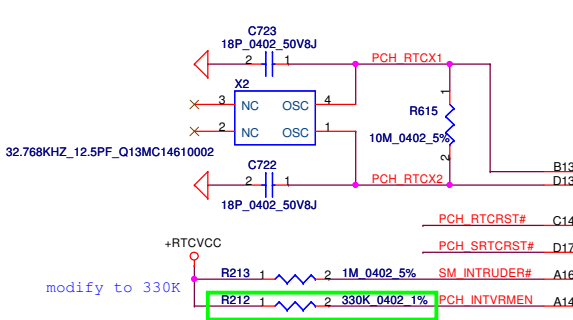
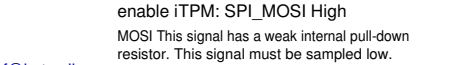
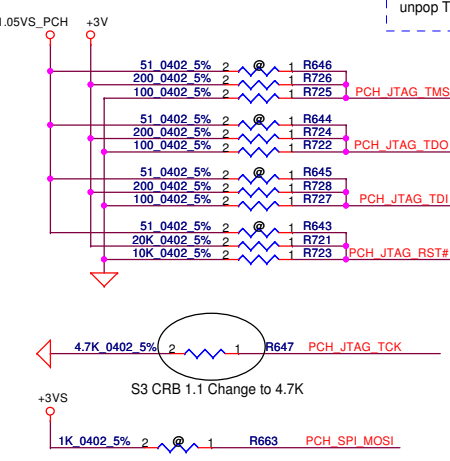
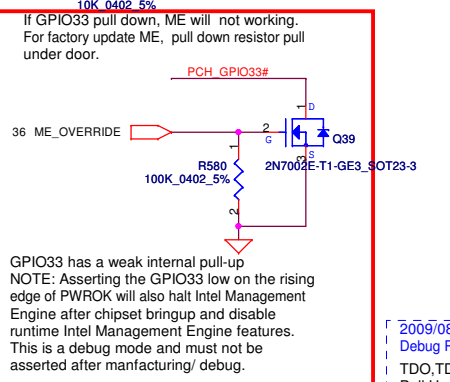
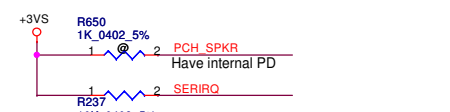
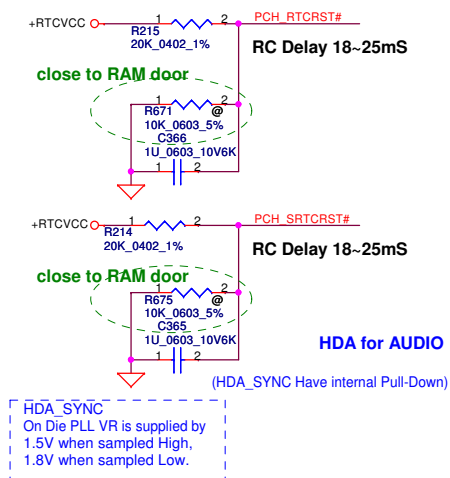
IDT Have Internal Pull-Down  
 FOR Realtek



PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

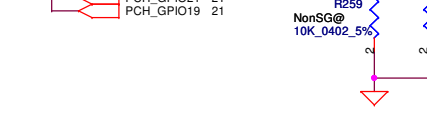
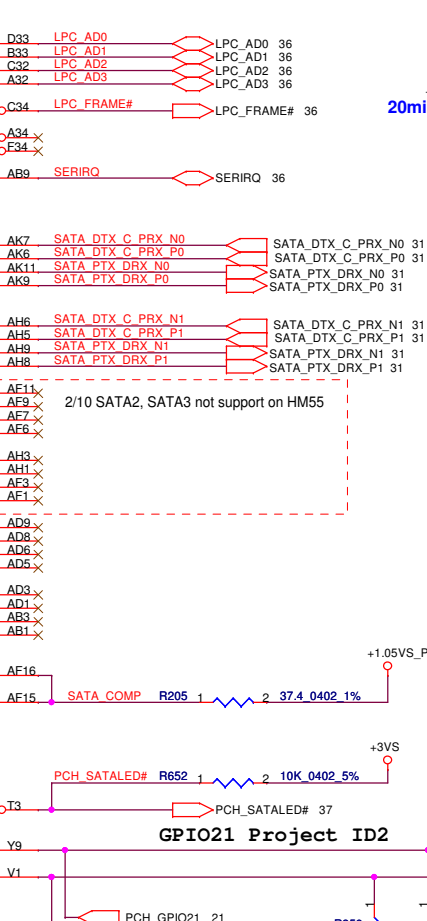
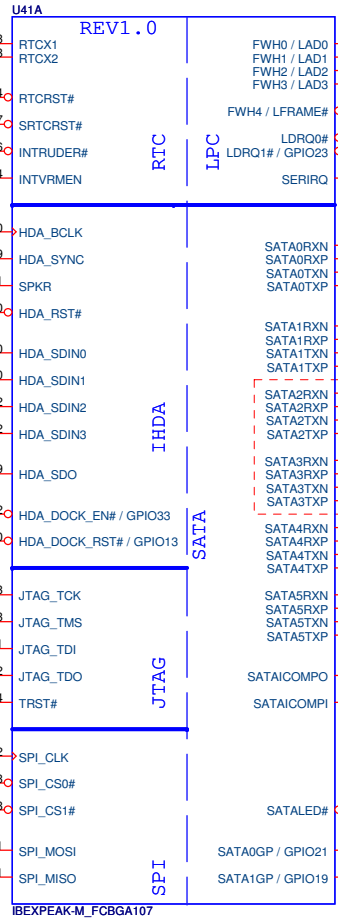


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Size	Document Number	Customer		Rev	
Date	NEW71/91 M/B LA-5893P Schematic	Date		0.1	
Tuesday, December 22, 2009		Sheet		12 of 56	

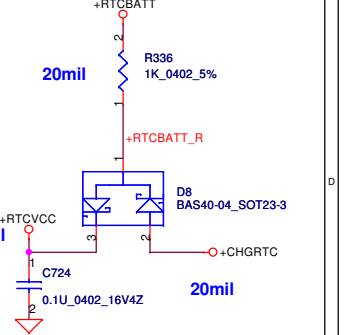


2008 Intel MOW36/MOW50  
TDO:  
Reserved on ES1 Sample  
Mount R724, R722 on ES2 Sample

MP mount R646, R644,  
R645, R643 and remove  
others



	GPIO19	GPIO37
	PCH_GPIO19	VGA_PRSNT_L#
dGPU	0	0
iGPU	0	1
SG	1	X



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Size	Document Number	Date	Sheet	Rev	
Customer	NEW71/91 M/B LA-5893P Schematic	Tuesday, December 22, 2009	13	0.1	
			Sheet	of	
			13	56	

For PCIE LAN

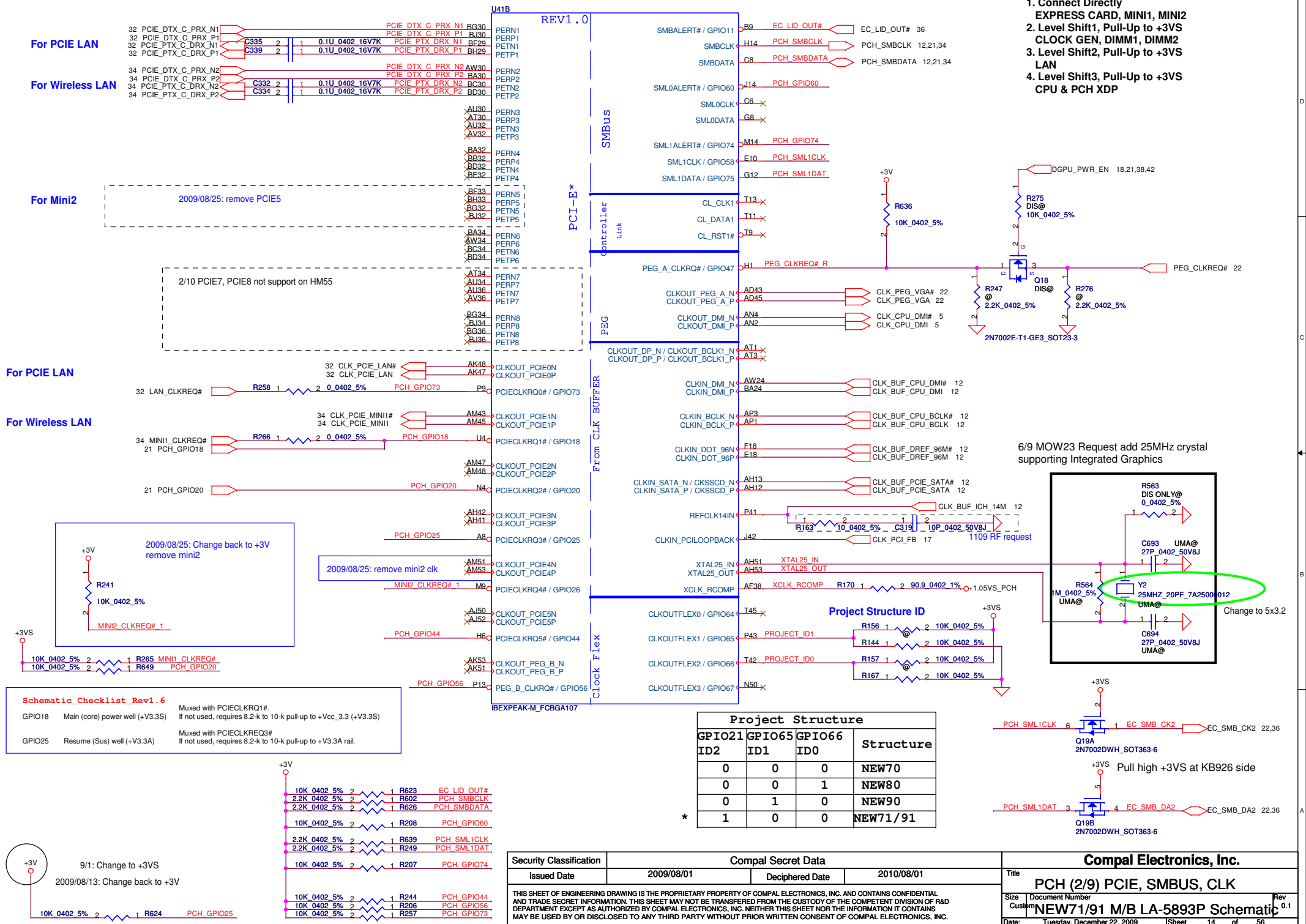
For Wireless LAN

For Mini2

For PCIE LAN

For Wireless LAN

1. Connect Directly EXPRESS CARD, MINI1, MINI2
2. Level Shift1, Pull-Up to +3VS CLOCK GEN, DIMM1, DIMM2
3. Level Shift2, Pull-Up to +3VS LAN
4. Level Shift3, Pull-Up to +3VS CPU & PCH XDP



**Schematic Checklist\_Rev1.6**

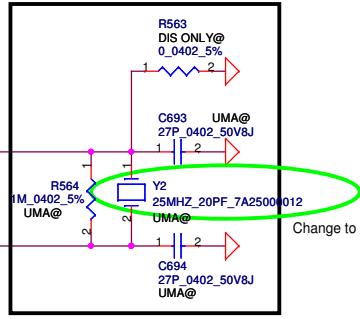
GPIO18 Main (core) power well (+V3.3S) Mixed with PCIECLKRQ1#. If not used, requires 8.2-k to 10-k pull-up to +Vcc\_3.3 (+V3.3S)

GPIO25 Resume (Sus) well (+V3.3A) Mixed with PCIECLKRQ3#. If not used, requires 8.2-k to 10-k pull-up to +V3.3A rail.

**Project Structure**

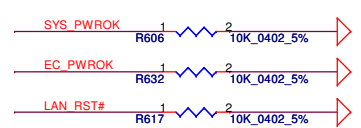
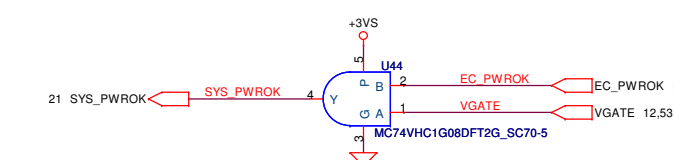
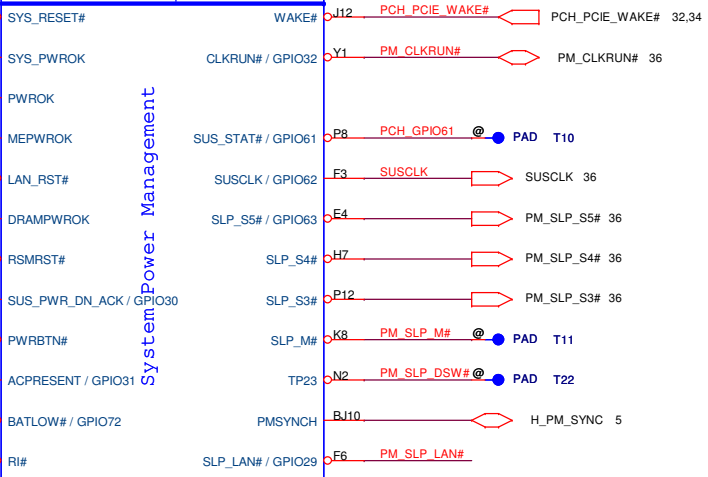
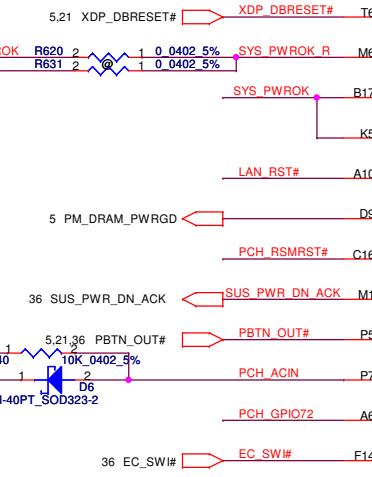
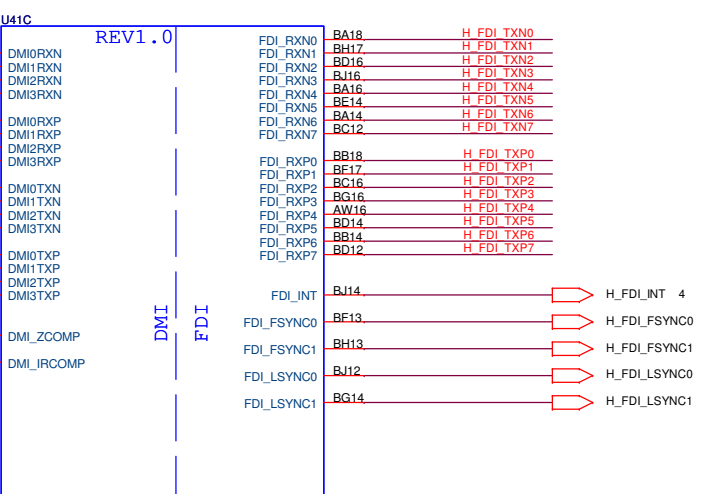
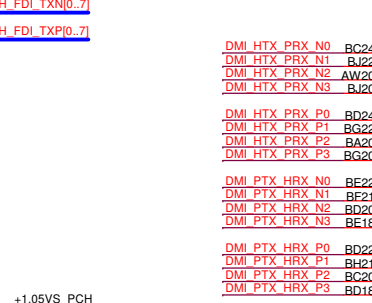
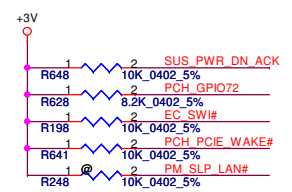
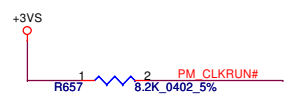
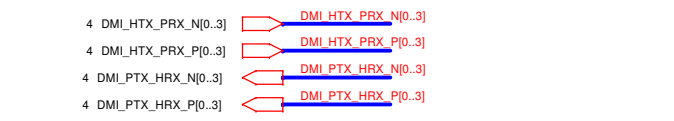
GPIO21 ID2	GPIO65 ID1	GPIO66 ID0	Structure
0	0	0	NEW70
0	0	1	NEW80
0	1	0	NEW90
1	0	0	NEW71/91

6/9 MOW23 Request add 25MHz crystal supporting Integrated Graphics

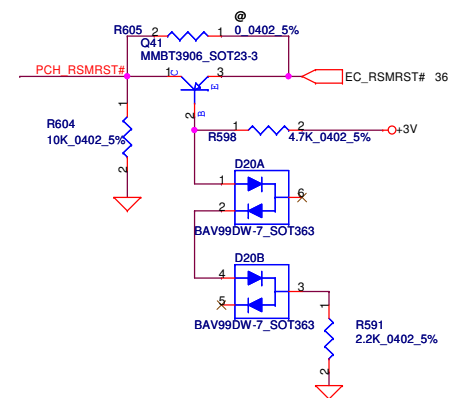


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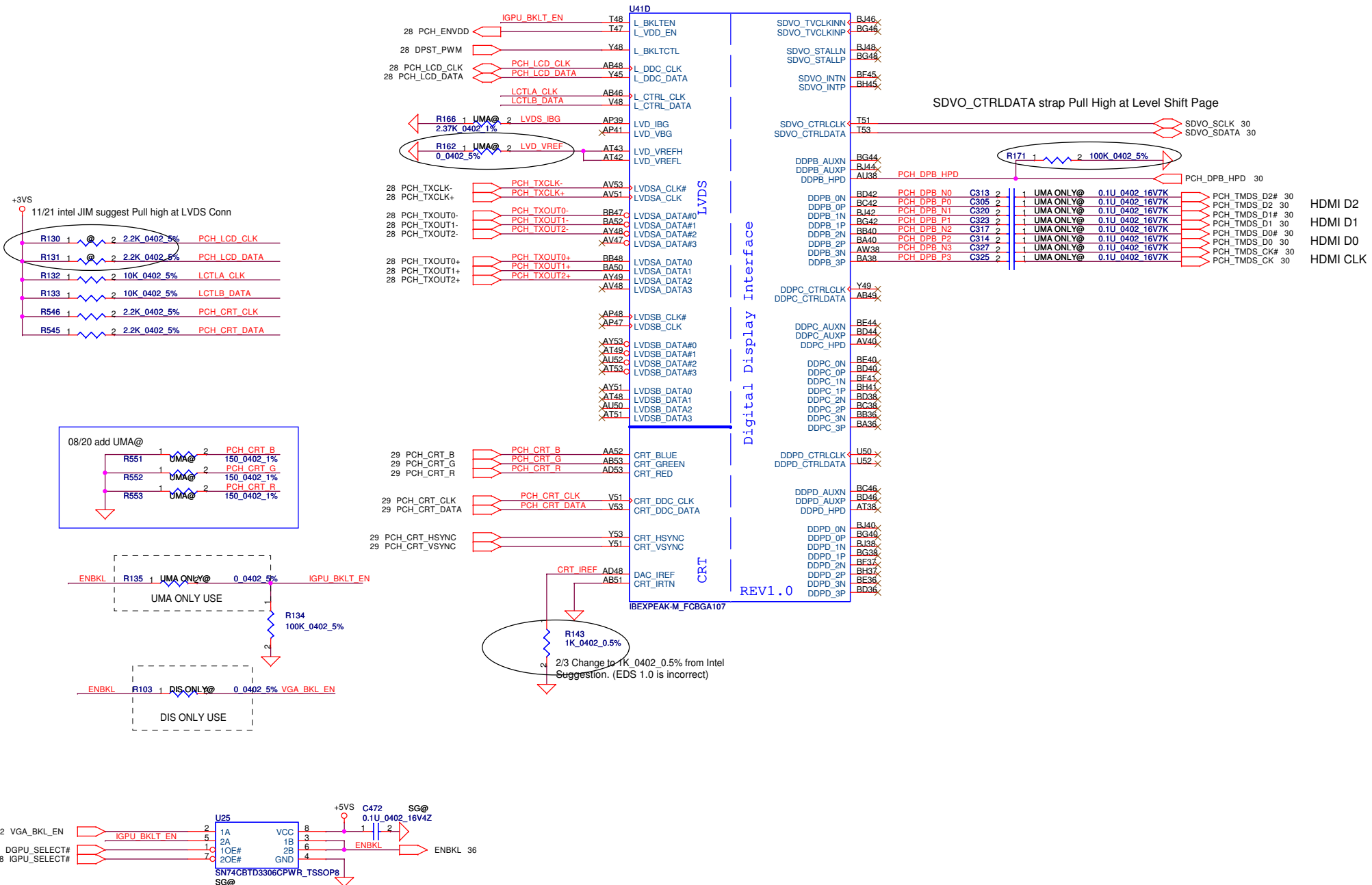
Compal Electronics, Inc.			
Title: PCH (2/9) PCIE, SMBUS, CLK			
Size	Document Number	Rev	
Customer	NEW71/91 M/B LA-5893P Schematic	0.1	
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No used Integrated LAN,  
 connecting LAN\_RST# to GND

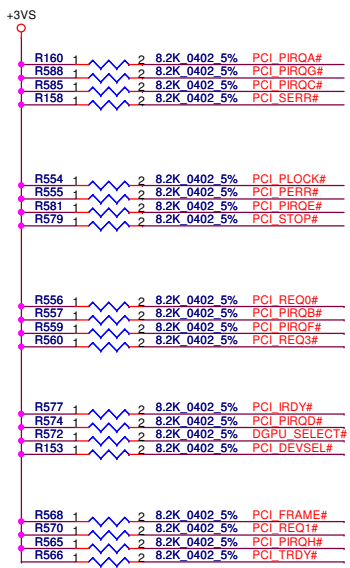


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Date:	Tuesday, December 22, 2009	Sheet	15	of	56



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Size	Document Number	Customer		Rev	
Date	NEW71/91 M/B LA-5893P Schematic	Date		0.1	
Tuesday, December 22, 2009		Sheet		16 of 56	





PCI\_GNT0#, PCI\_GNT1#, PCI\_GNT2#, PCI\_GNT3# has a weak internal pull-up

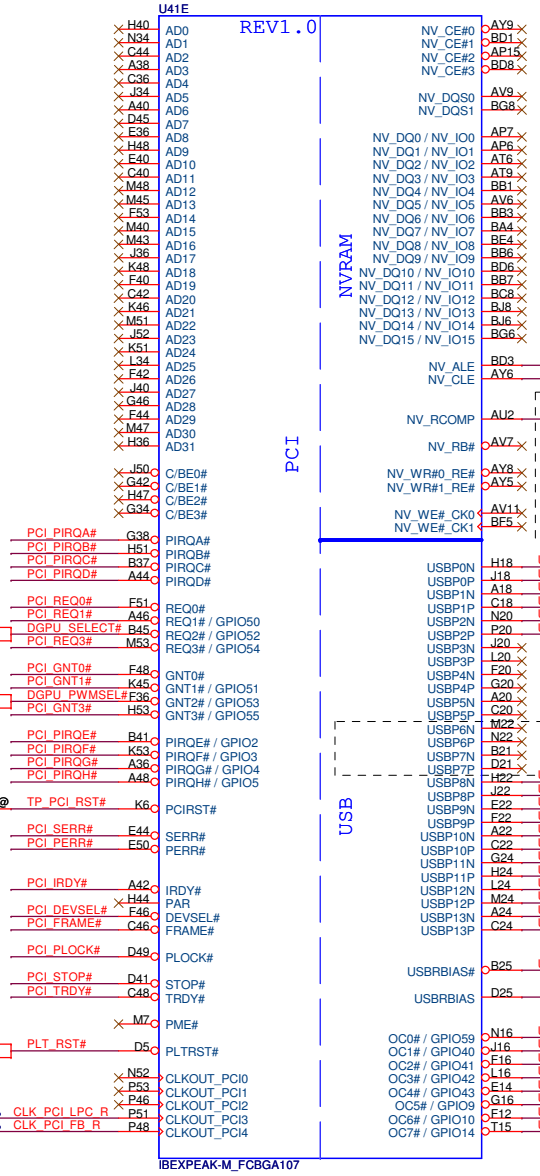
PCI\_GNT2# ESI Strap (Server Only) this signal should not be pulled low

2008/1/6 2009MOW01 change to 22 ohm

PCI_GNT#0	PCI_GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

A16 swap override Strap/Top-Block Swap Override jumper

Low=A16 swap override/Top-Block Swap Override enabled  
High=Default \*

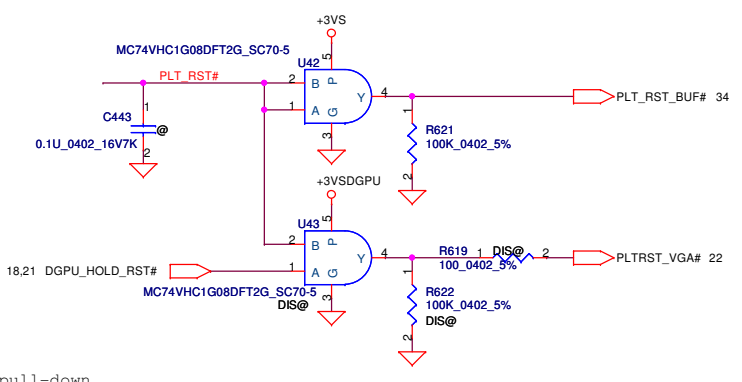


Design Guide 1.5 Ver: 3.26.13 Terminating Unused Braidwood Interface

If not implemented, the dual channel NAND interface signals, including NV\_RCOMP, can be left as No Connect.

USB/B (Right Side)  
USB Port (Left Side)  
USB/B (Right Side)

CMOS Camera (LVDS)  
Card Reader  
Mini Card(SIM Card)  
Bluetooth  
Mini Card(WLAN)  
Mini Card(WWAN)



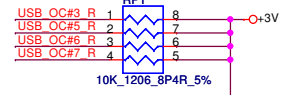
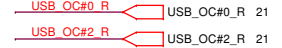
Intel Anti-Theft Technology	
NV_ALE	High=Enabled
NV_CLE	Low=Disable(floating) *

DMI Termination Voltage	
NV_CLE	Set to Vcc when HIGH
NV_CLE	Set to Vss when LOW

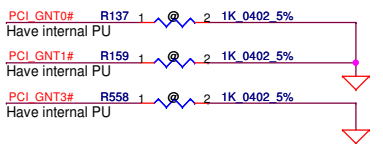
NV\_ALE Enable Intel Anti-Theft Technology : 8.2K PU to +3VS

Disable Intel Anti-Theft Technology : floating(internal PD)

NV\_CLE DMI termination voltage. weak internal PU, don't PD



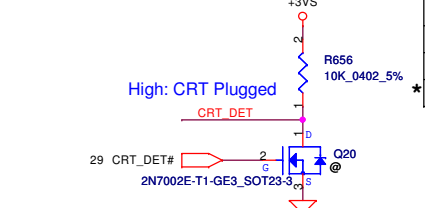
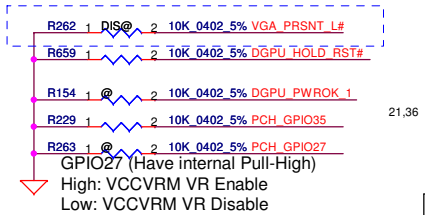
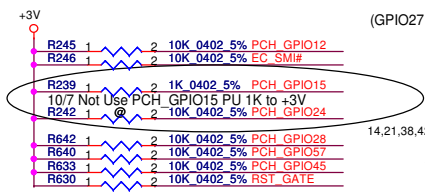
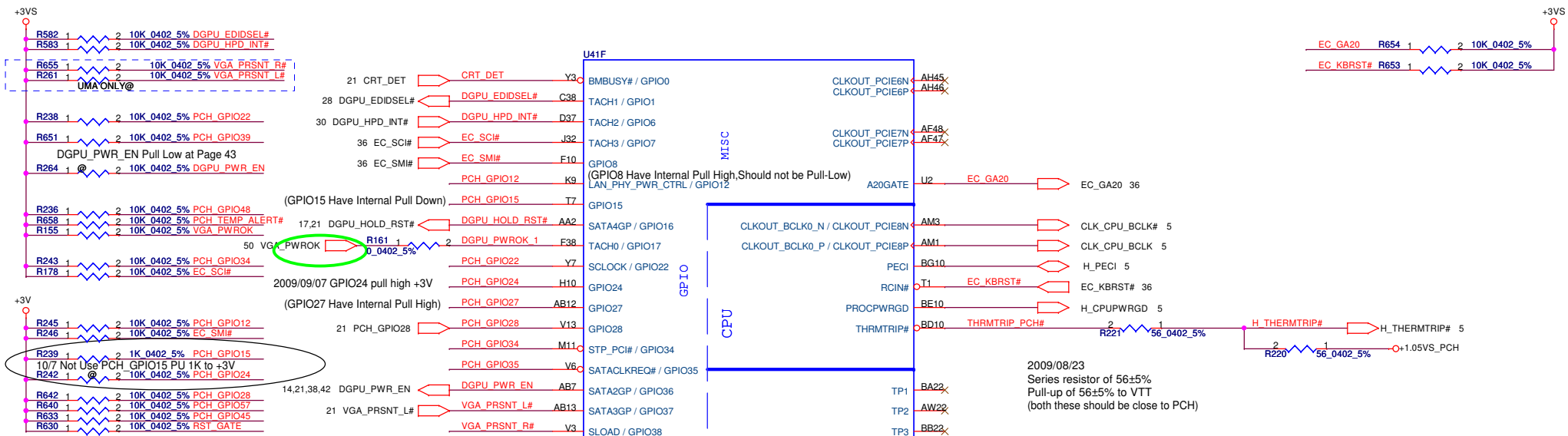
OC[0..3] use for EHCI 1  
OC[4..7] use for EHCI 2



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Compal Electronics, Inc.			
Title <b>PCH (5/9) PCI, USB, VRAM</b>			
Size	Document Number	Rev	
Customer	NEW71/91 M/B LA-5893P Schematic	0.1	
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**GPIO8**  
This signal has a weak internal pull up can't Pull low

**GPIO27**  
On-Die PLL Voltage Regulator  
This signal has a weak internal pull up

- H : On-Die voltage regulator enable
- L : On-Die PLL Voltage Regulator disable

Note: the internal pull-up is disabled after RSMRST# de-asserts.  
The On-Die PLL voltage regulator is enabled when sampled high. When sampled low the On-Die PLL Voltage Regulator is disabled.

**GPIO15**

- L : Intel ME Crypto Transport Layer Security(TLS) chiper suite with no confidentiality
- H : Intel ME Crypto Transport Layer Security(TLS) chiper suite with confidentiality

CRB has a 1-k pull-up on this signal to +3.3VA rail.

	GPIO19 PCH_GPIO19	GPIO37 VGA_PRSN_T_L#
dGPU	0	0
iGPU	0	1
SG	1	0

- ✕ A4 VSS\_NCTF\_1
- ✕ A49 VSS\_NCTF\_2
- ✕ A5 VSS\_NCTF\_3
- ✕ A50 VSS\_NCTF\_4
- ✕ A52 VSS\_NCTF\_5
- ✕ A53 VSS\_NCTF\_6
- ✕ B2 VSS\_NCTF\_7
- ✕ B4 VSS\_NCTF\_8
- ✕ B52 VSS\_NCTF\_9
- ✕ B53 VSS\_NCTF\_10
- ✕ BE1 VSS\_NCTF\_11
- ✕ BE53 VSS\_NCTF\_12
- ✕ BF1 VSS\_NCTF\_13
- ✕ BF53 VSS\_NCTF\_14
- ✕ BH1 VSS\_NCTF\_15
- ✕ BH2 VSS\_NCTF\_16
- ✕ BH52 VSS\_NCTF\_17
- ✕ BJ1 VSS\_NCTF\_18
- ✕ BJ2 VSS\_NCTF\_19
- ✕ BJ4 VSS\_NCTF\_20
- ✕ BJ49 VSS\_NCTF\_21
- ✕ BJ5 VSS\_NCTF\_22
- ✕ BJ50 VSS\_NCTF\_23
- ✕ BJ52 VSS\_NCTF\_24
- ✕ BJ53 VSS\_NCTF\_25
- ✕ BJ54 VSS\_NCTF\_26
- ✕ D1 VSS\_NCTF\_27
- ✕ D2 VSS\_NCTF\_28
- ✕ D53 VSS\_NCTF\_29
- ✕ E1 VSS\_NCTF\_30
- ✕ E53 VSS\_NCTF\_31

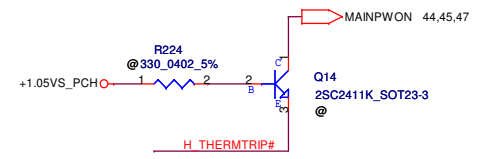
IBEXPEAK-M\_FCBGA107

REV1.0

2009/08/23  
(Have internal PH, Do not pull down)

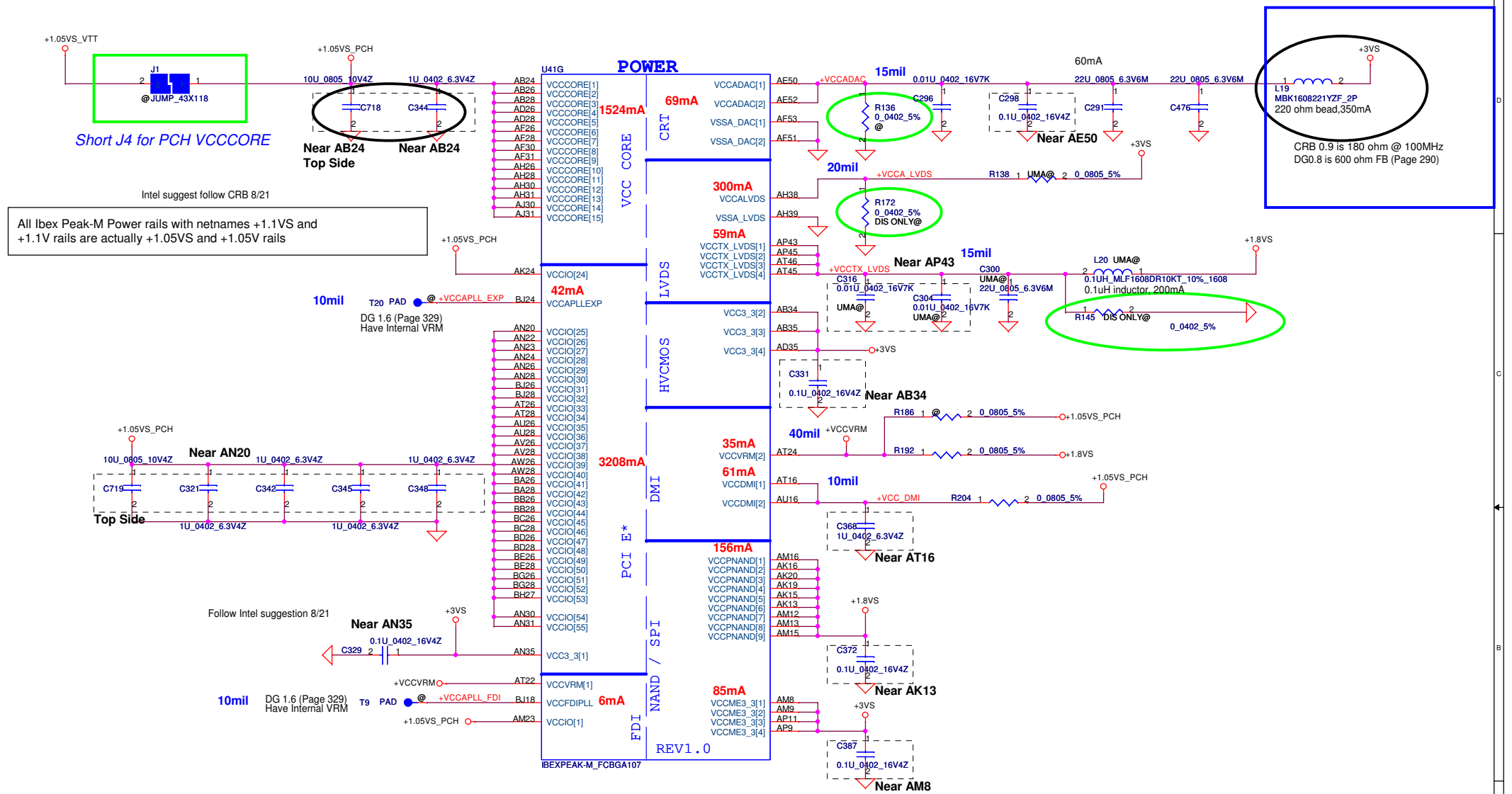
**INIT3\_3V**  
This signal has weak internal PH, can't pull low

2009/08/23  
Series resistor of 56±5%  
Pull-up of 56±5% to VTT  
(both these should be close to PCH)



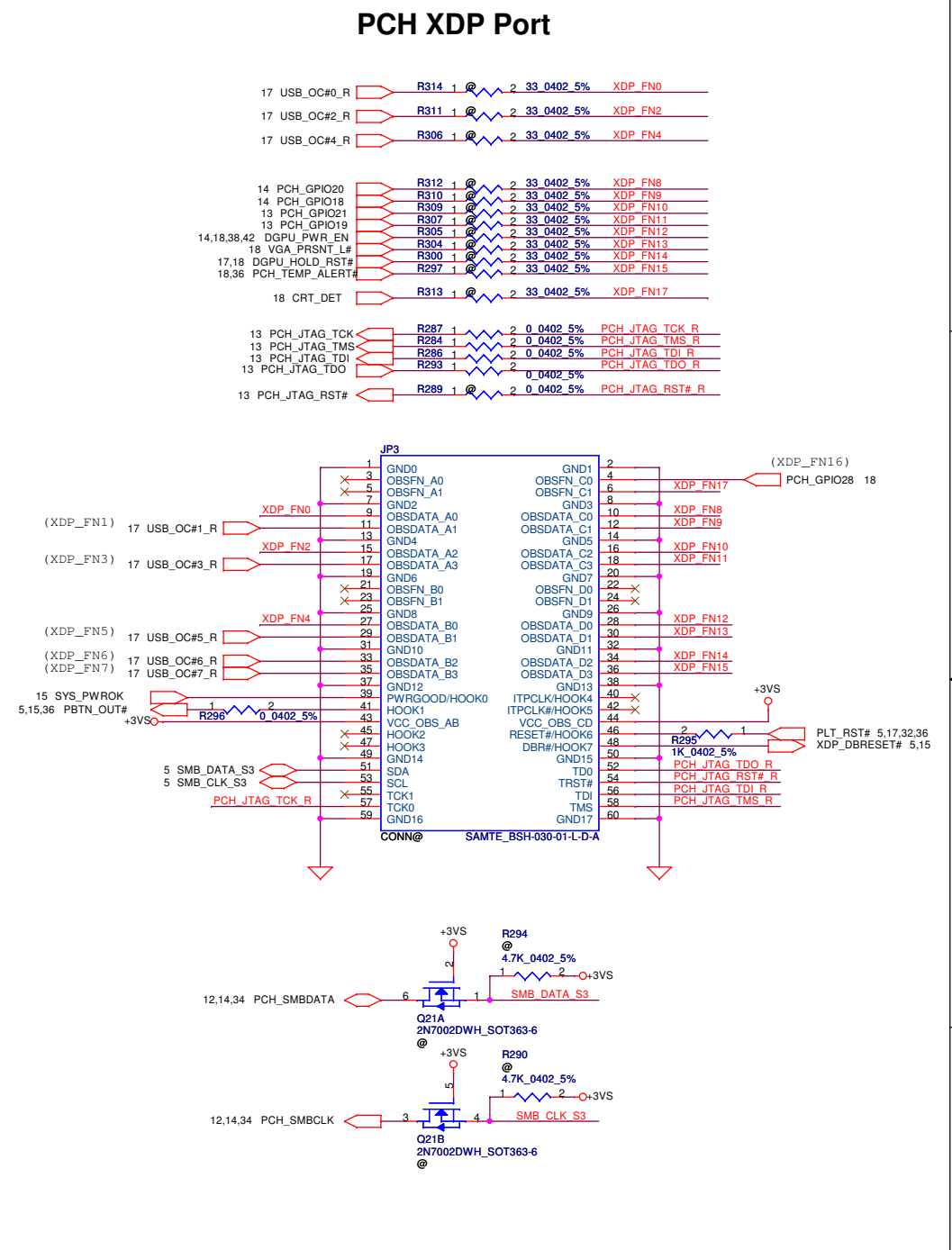
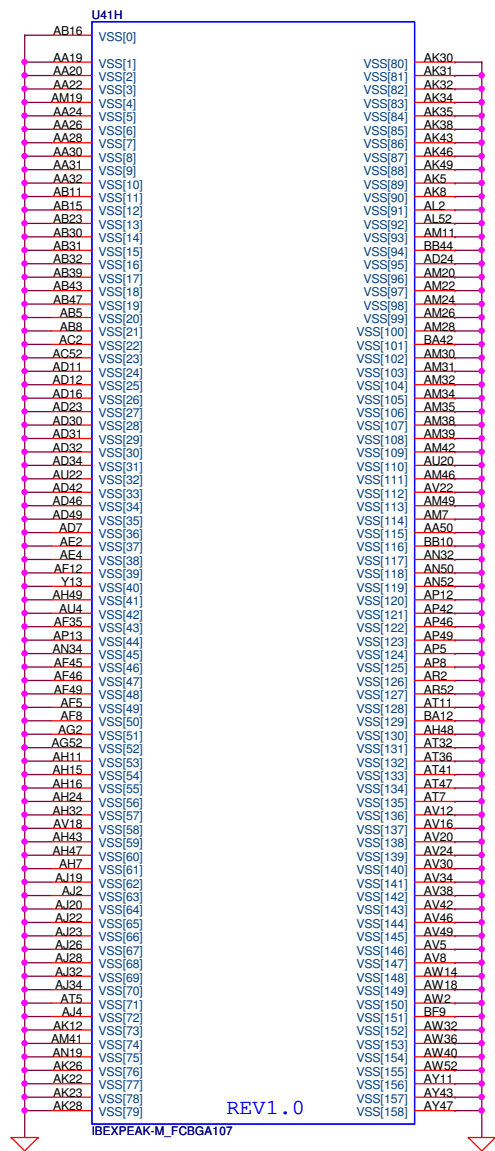
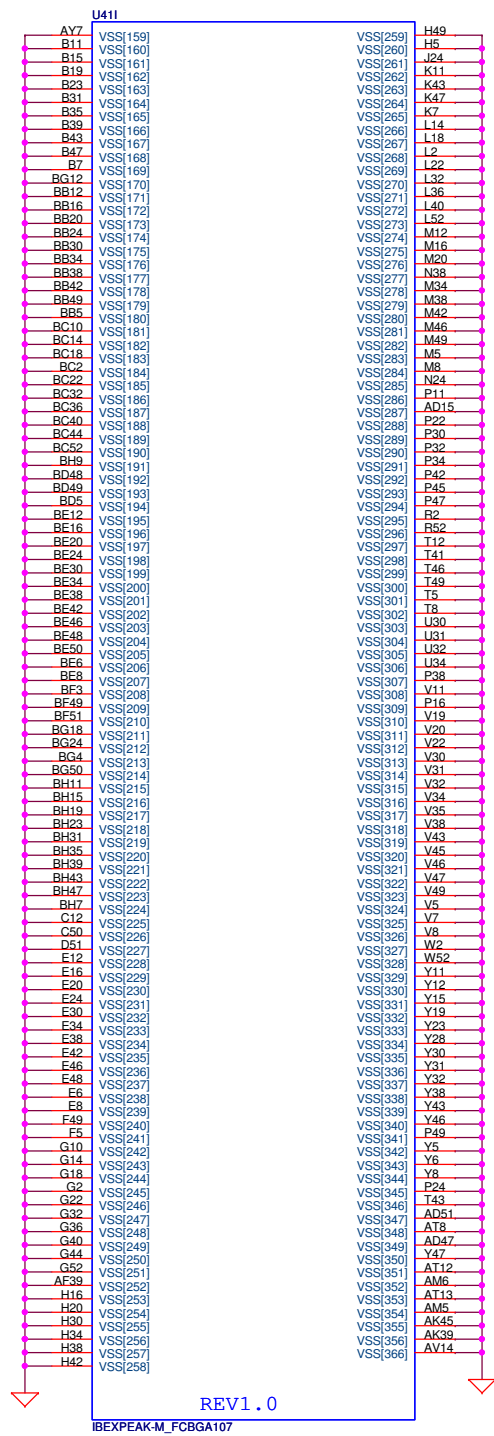
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Issued Date	2009/08/01	Deciphered Date	2010/08/01	PCH (6/9) GPIO, CPU, MISC	
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Need Modify  
180 ohm @  
100MHz Bead



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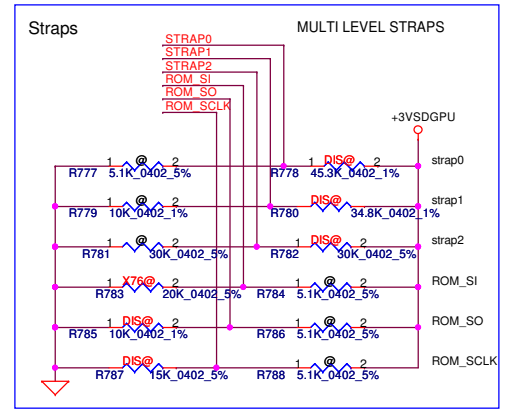
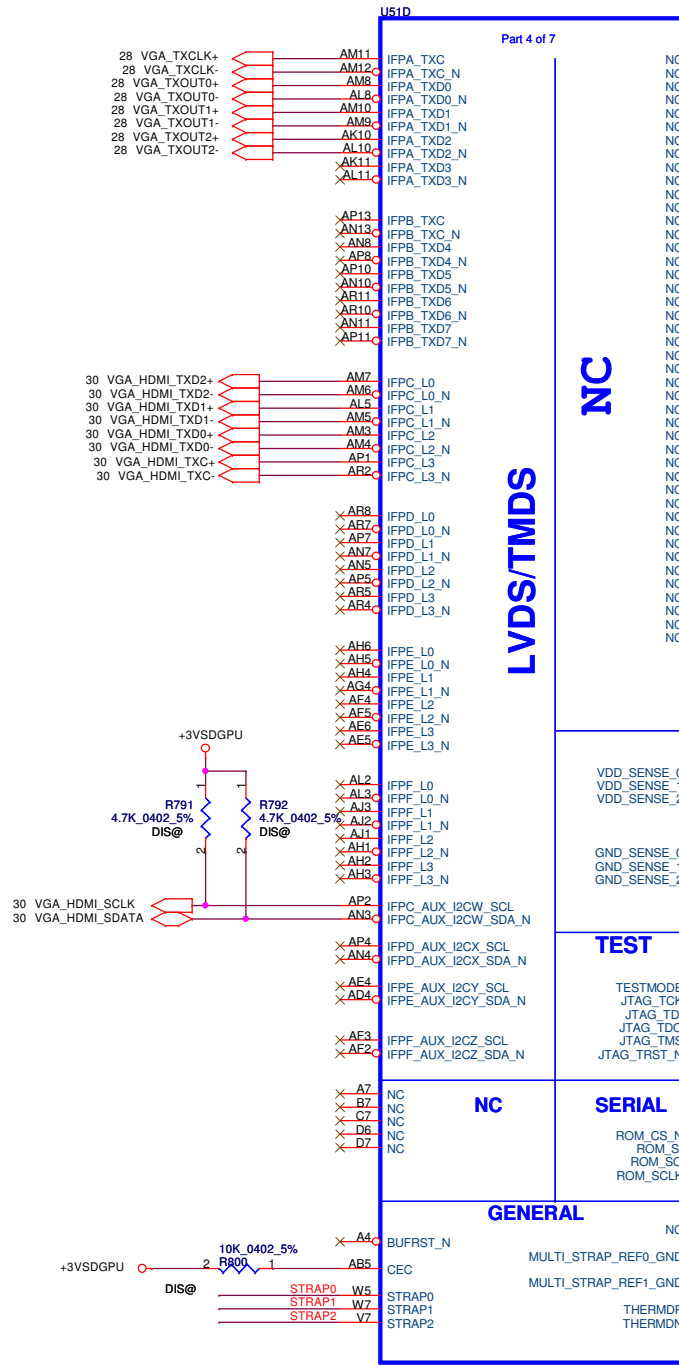


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Size	Document Number	Date	Tuesday, December 22, 2009	Sheet	21 of 56
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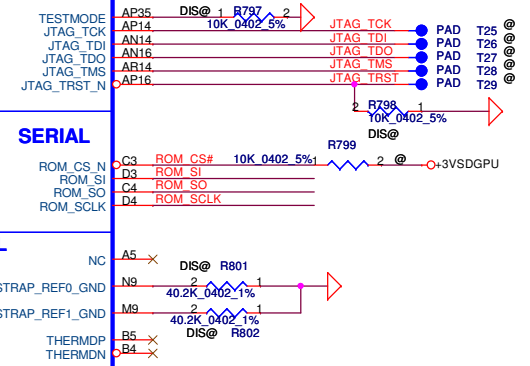
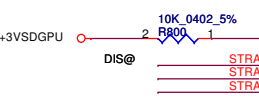
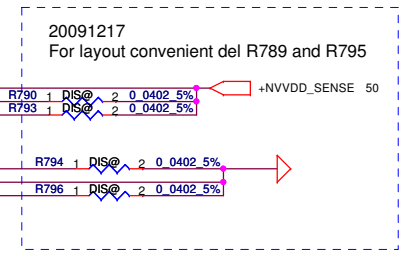


Mode E Command Mapping GB2-128 Package Femi	Mode C Command Mapping GB1-128 Package	Data Bit	0..31	32..63
FBx_CMD3	FBx_CMD0	CKE_L		
FBx_CMD8	FBx_CMD1	A8		A8
FBx_CMD2	FBx_CMD2	CS0_L*		
FBx_CMD21	FBx_CMD3	A7		A6
FBx_CMD24	FBx_CMD4	A2		A1
FBx_CMD23	FBx_CMD5	A11		A9
FBx_CMD26	FBx_CMD6	A5		A4
FBx_CMD7	FBx_CMD7	A0		A12
FBx_CMD15	FBx_CMD8	CAS*		CAS*
FBx_CMD13	FBx_CMD9	BA1		A3
FBx_CMD4	FBx_CMD10	A9		A11
FBx_CMD18	FBx_CMD11			CS0_H
FBx_CMD29	FBx_CMD12	BA0		BA0
FBx_CMD27	FBx_CMD13	BA2		A15
FBx_CMD6	FBx_CMD14	A3		BA1
FBx_CMD17	FBx_CMD15			CS1_H
FBx_CMD19	FBx_CMD16			ODT_H
FBx_CMD22	FBx_CMD17	A4		A5
FBx_CMD12	FBx_CMD18	A13		A14
FBx_CMD28	FBx_CMD19	WE*		A10
FBx_CMD10	FBx_CMD20	A1		A2
FBx_CMD25	FBx_CMD21	A10		WE*
FBx_CMD9	FBx_CMD22	A12		A0
FBx_CMD1	FBx_CMD23	CS1_L*		
FBx_CMD11	FBx_CMD24	RAS*		RAS*
FBx_CMD0	FBx_CMD25	ODT_L		
FBx_CMD5	FBx_CMD26	A6		A7
FBx_CMD16	FBx_CMD27			CKE_H
FBx_CMD20	FBx_CMD28	RST		RST
FBx_CMD14	FBx_CMD29	A14		A13
FBx_CMD30	FBx_CMD30	A15		BA2
FBx_CMD31				

LOW HIGH



20091214 Modify	strap0	strap1	strap2	ROM_SI	ROM_SO	ROM_SCLK
64MX16 Samsung SA000035720	H 45K	H 35K	H 30K	L 20K	L 10K	L 15K
64MX16 Hynix SA000032420	H 45K	H 35K	H 30K	L 15K	L 10K	L 15K

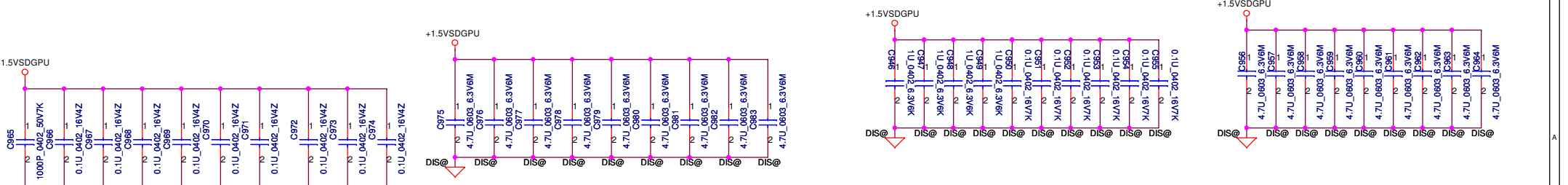
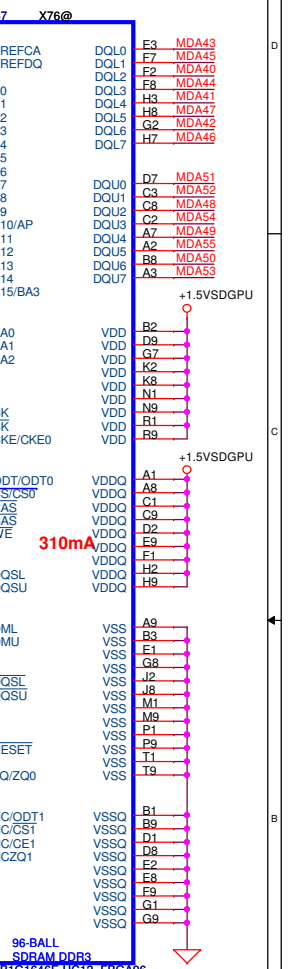
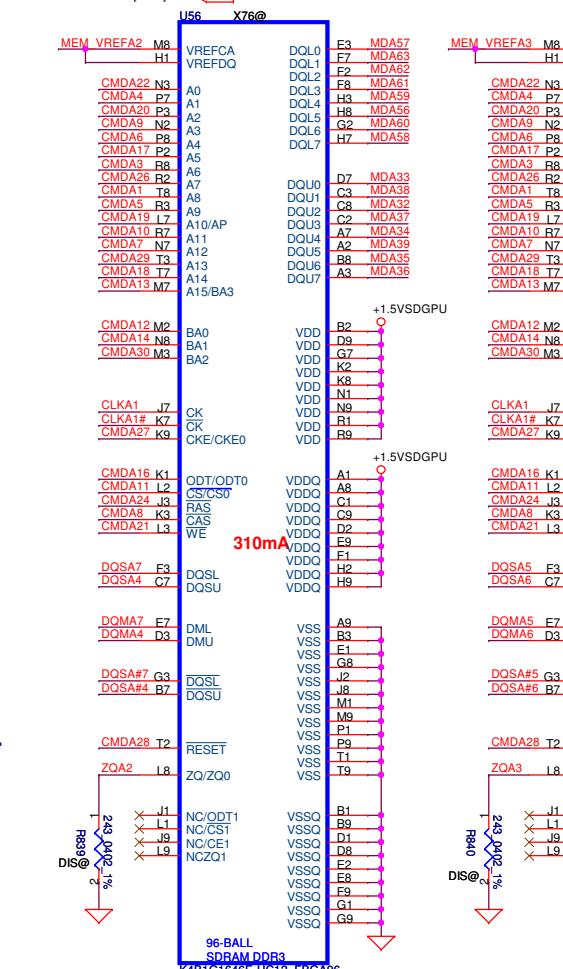
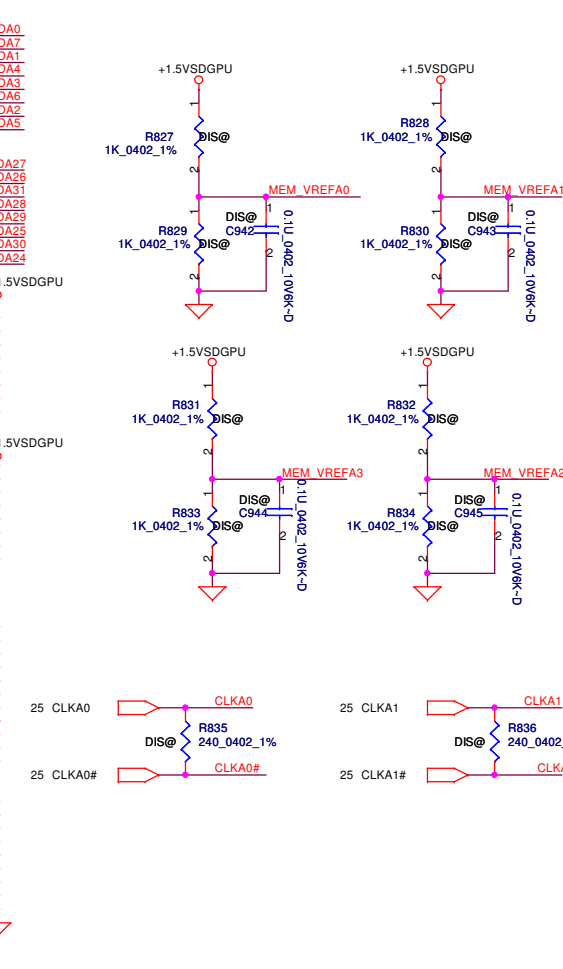
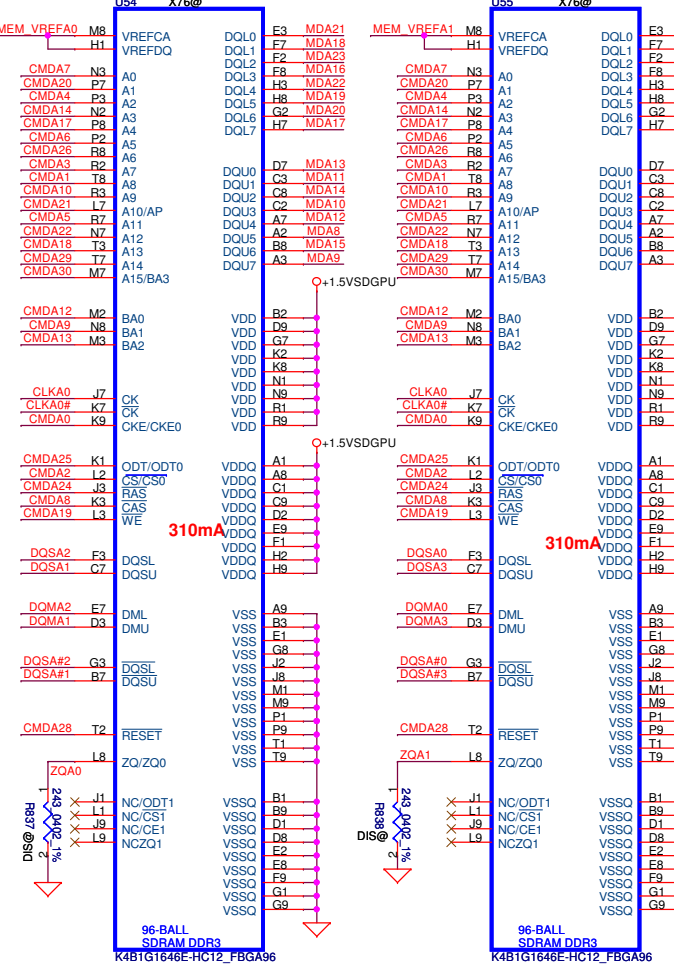
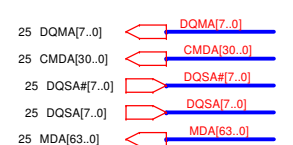
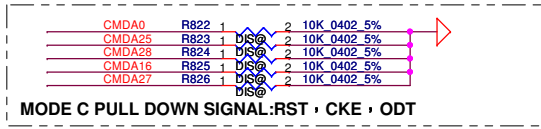
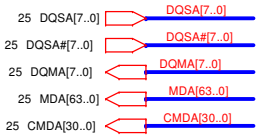


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Size	Document Number	Customer		Rev	
Date:	Tuesday, December 22, 2009	Sheet		23 of 56	

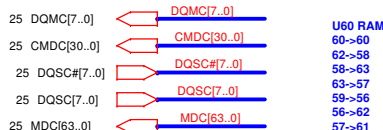
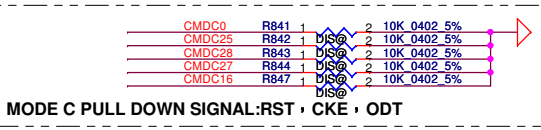
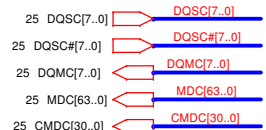




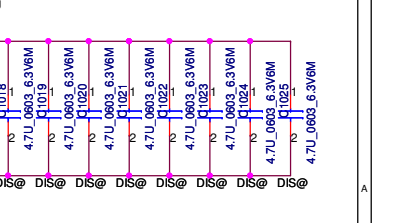
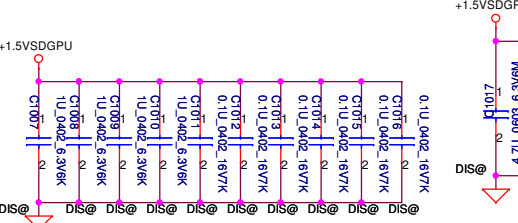
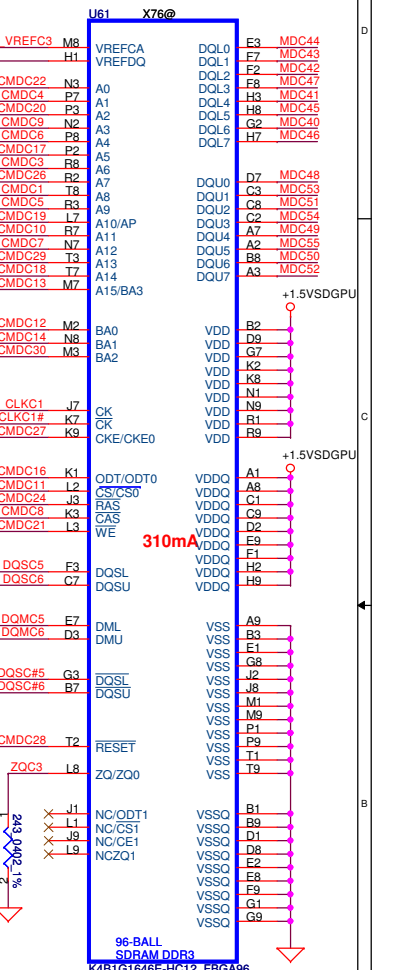
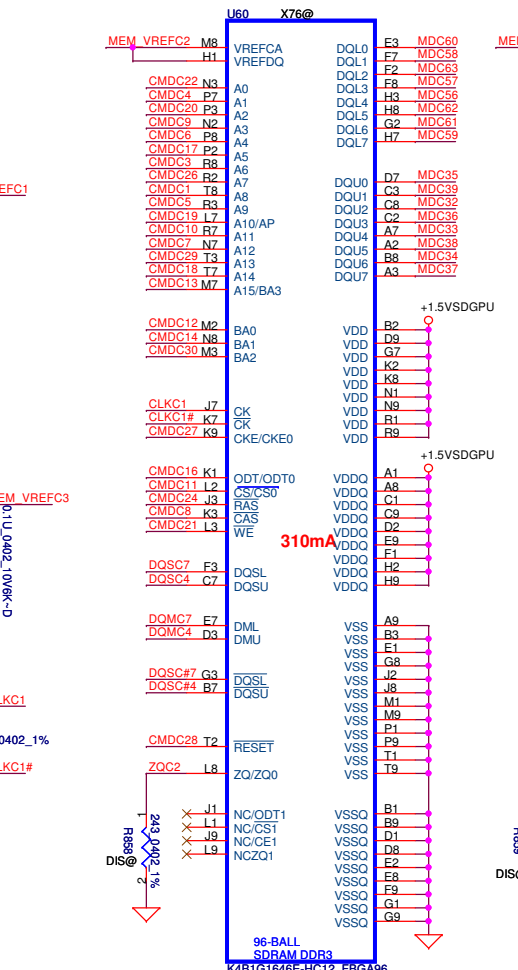
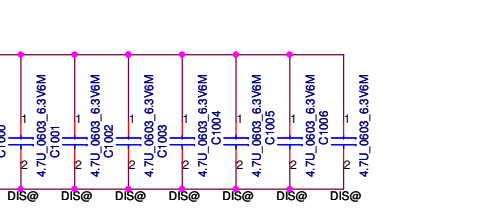
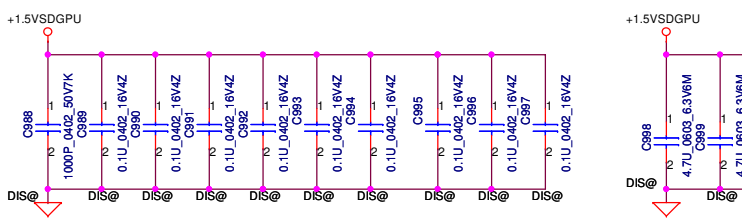
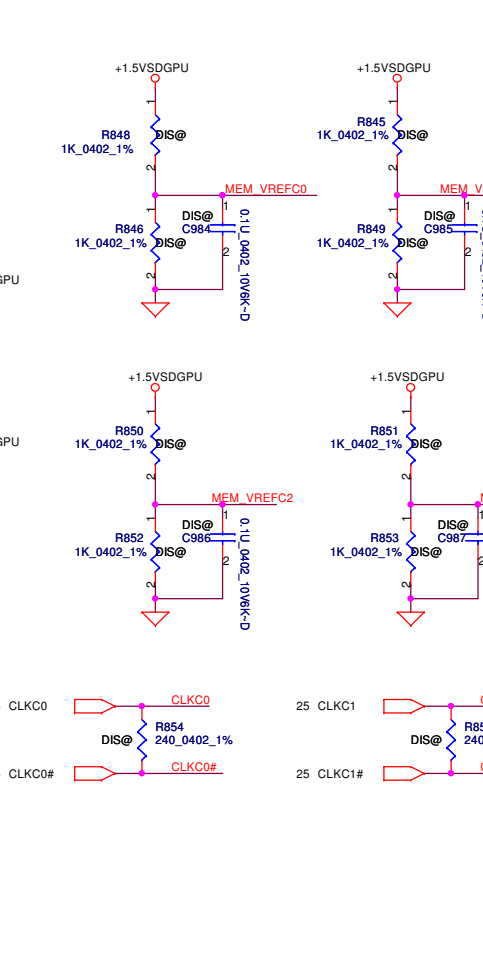
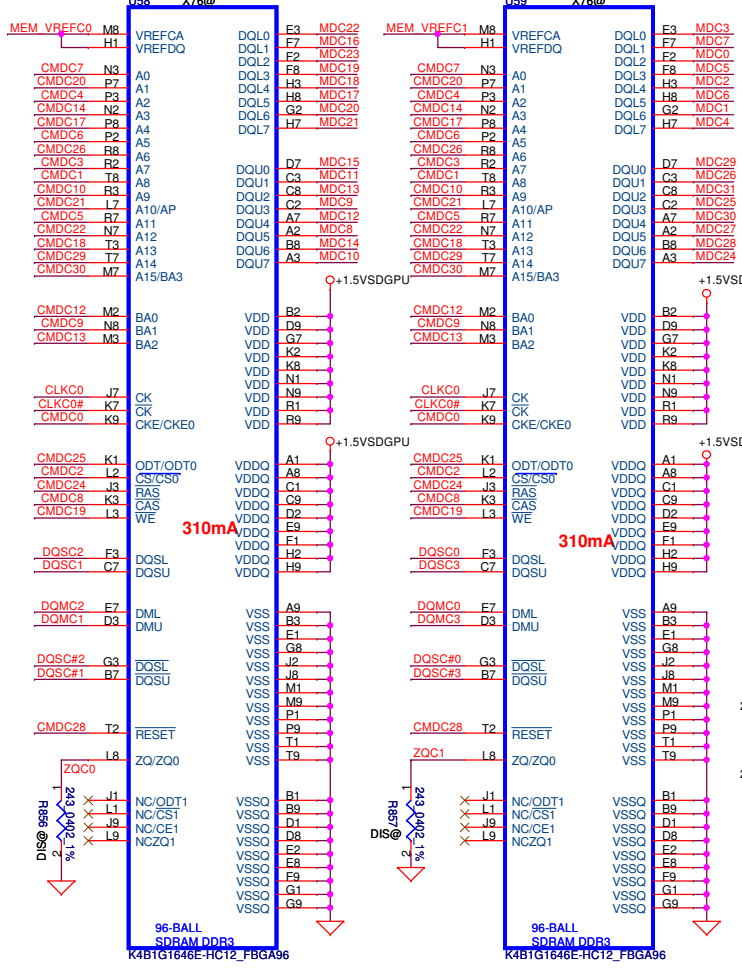




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Customer	NEW71/91 M/B LA-5893P Schematic				
Date:	Tuesday, December 22, 2009	Sheet	26	of	56

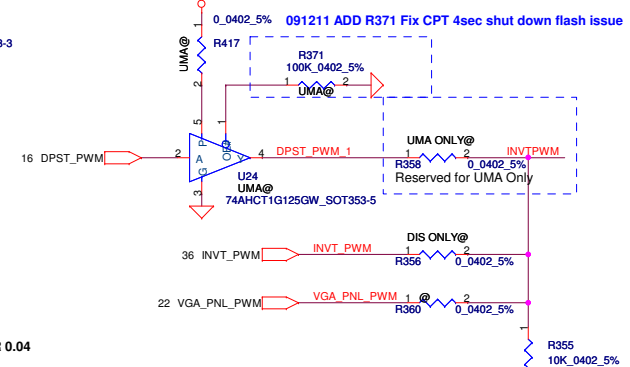
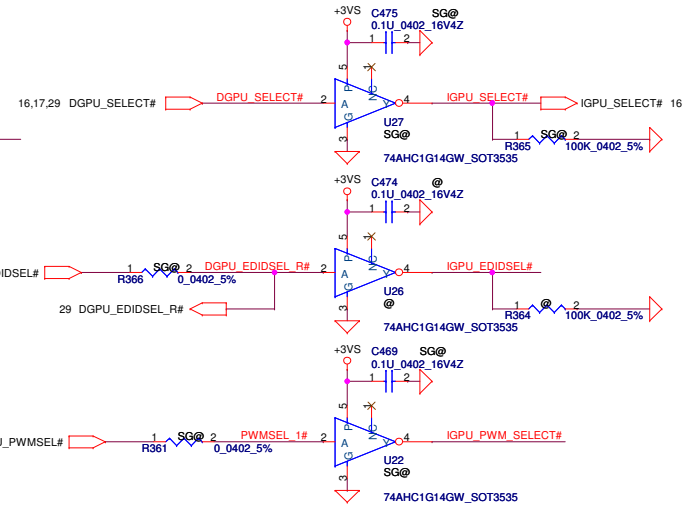
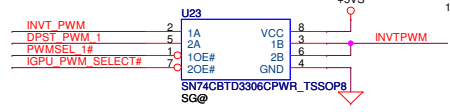
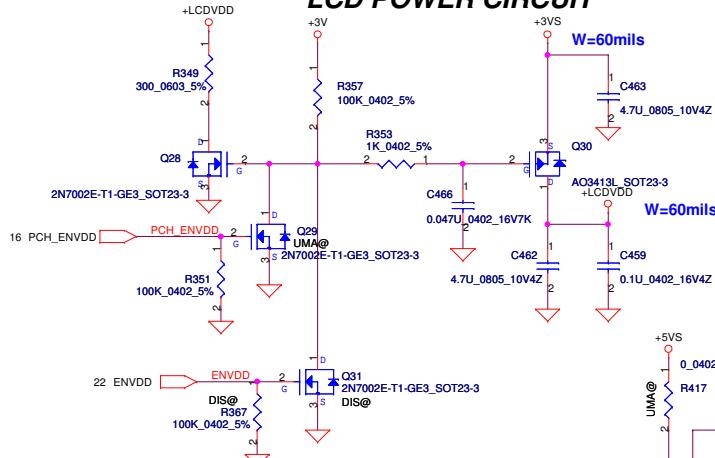


U60 RAM BIT SWAP 20091211  
 60-60  
 62-58  
 58-63  
 63-57  
 59-56  
 56-62  
 57-61  
 61-59

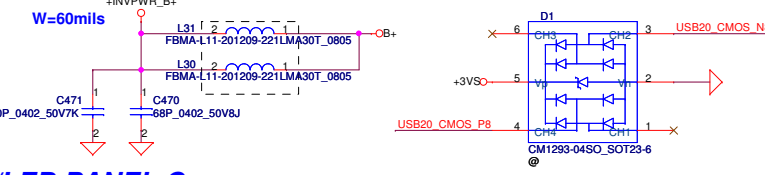


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NEW71/91	M/B LA-5893P Schematic	Tuesday, December 22, 2009		27	0.1

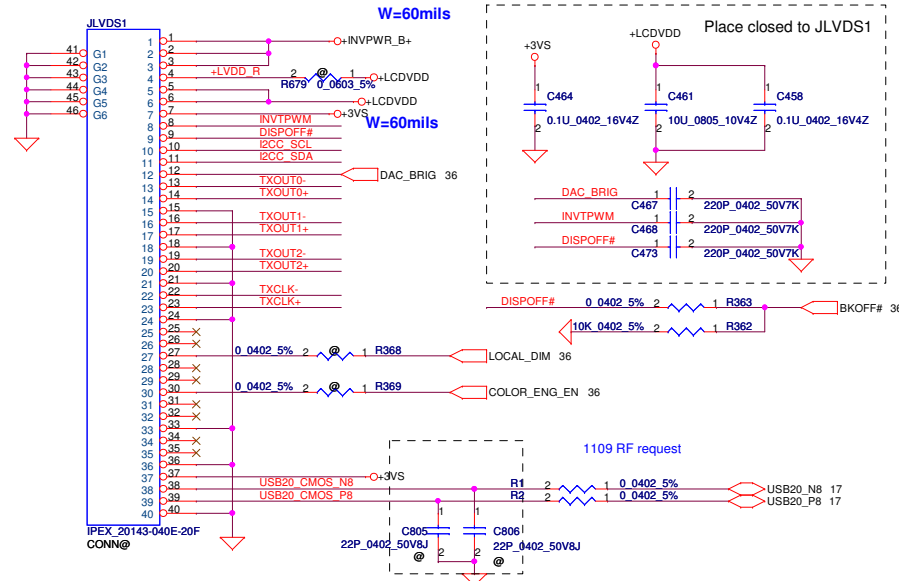
# LCD POWER CIRCUIT



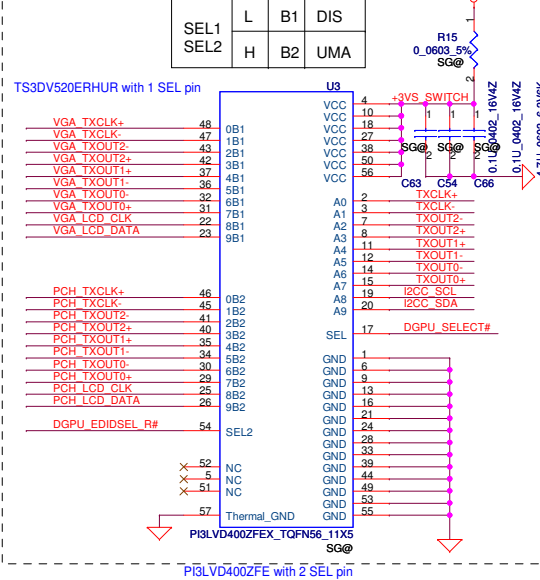
SM010014520 3000ma 220ohm@100mhz DCR 0.04



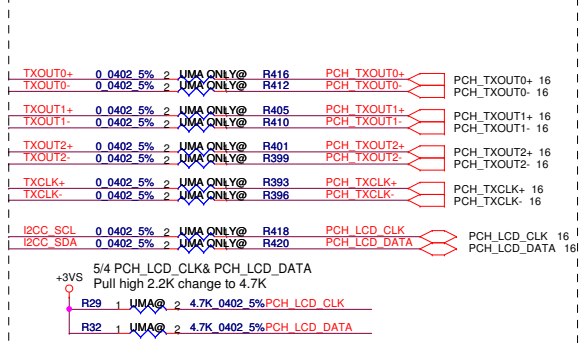
## LCD/LED PANEL Conn.



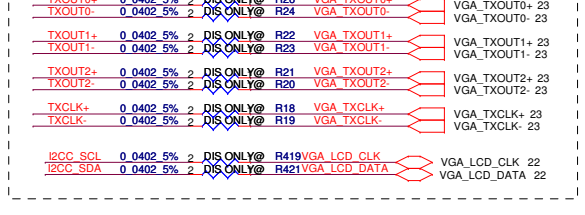
## SWITCHABLE



## UMA ONLY



## Discrete ONLY

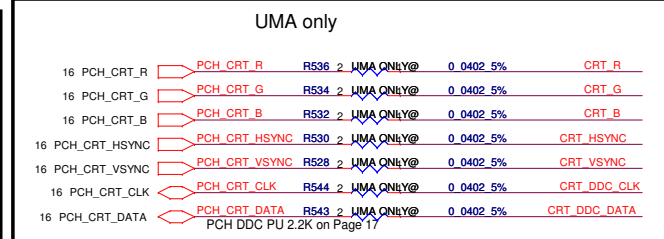
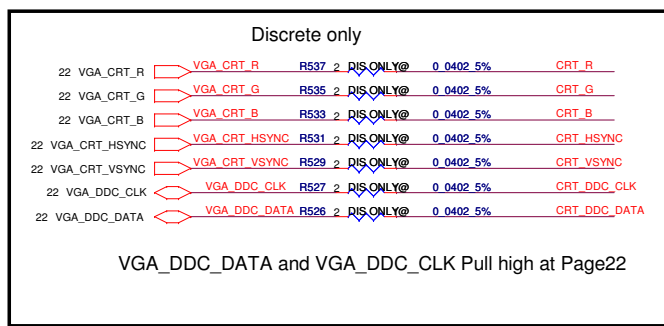
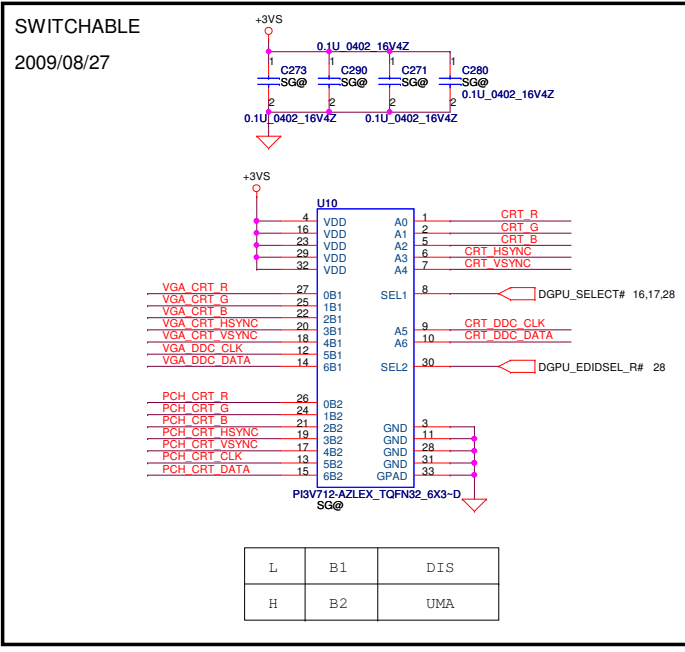
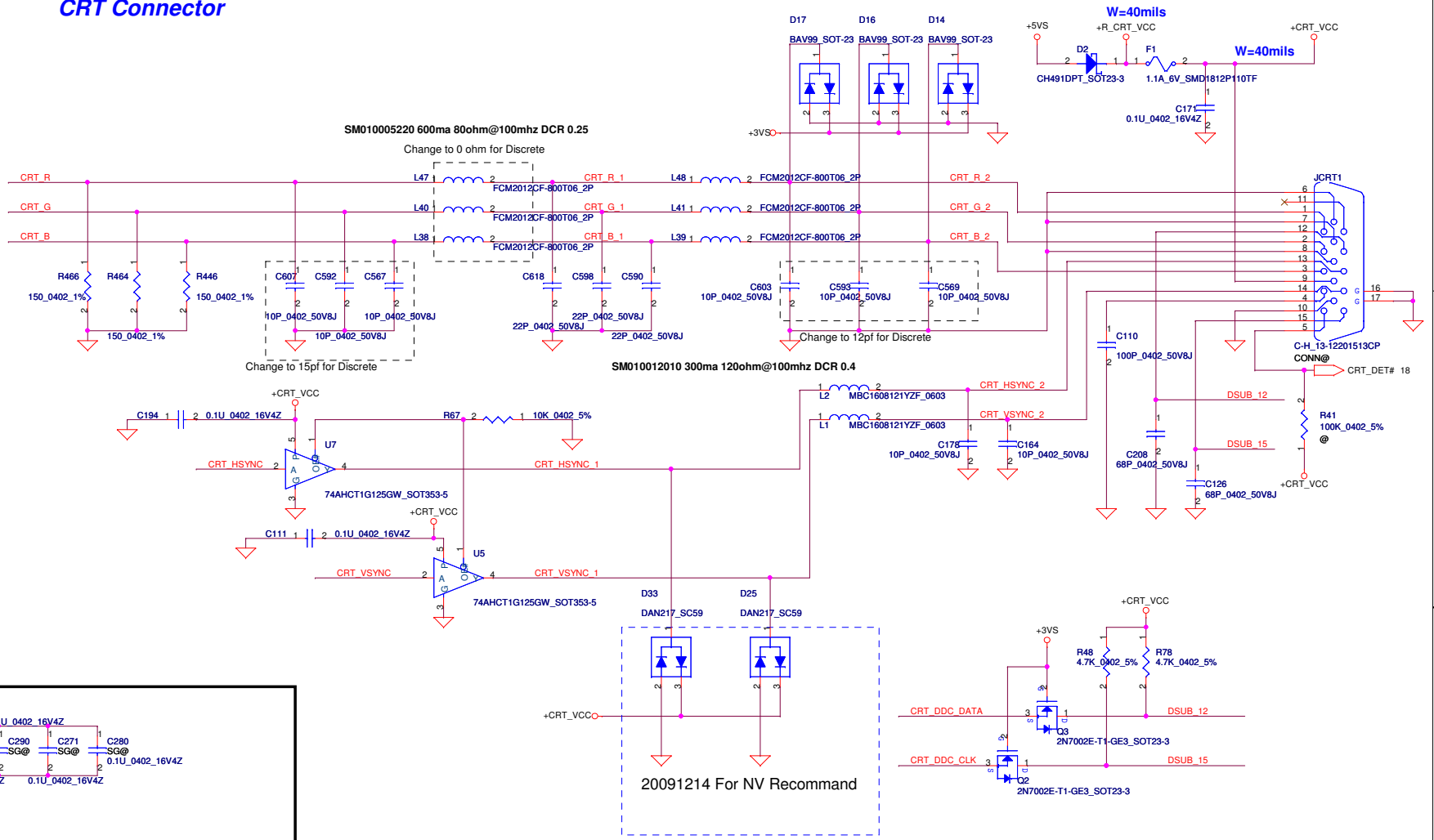


Security Classification	Compal Secret Data	
Issued Date	2009/08/01	Deciphered Date
		2010/08/01

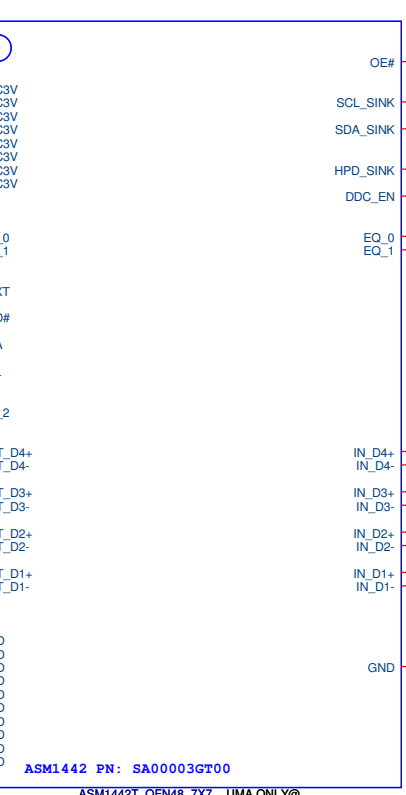
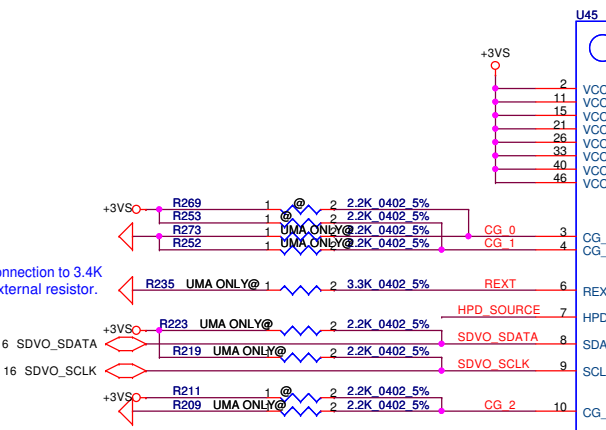
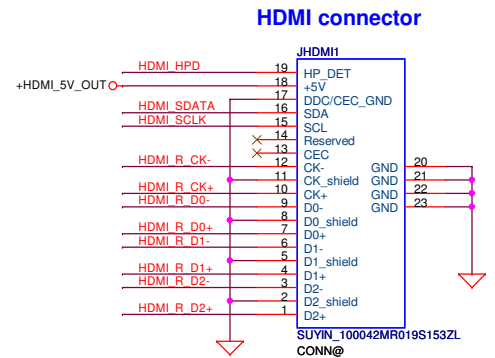
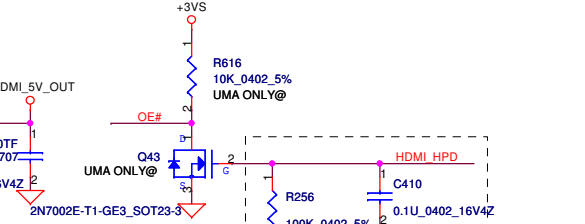
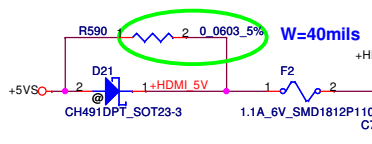
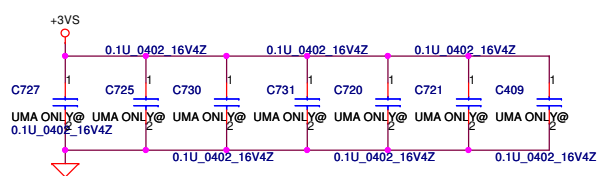
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Compal Electronics, Inc.		
LVDS Connector		
Title	Document Number	Rev
	NEW71/91 M/B LA-5893P Schematic	0.1
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# CRT Connector

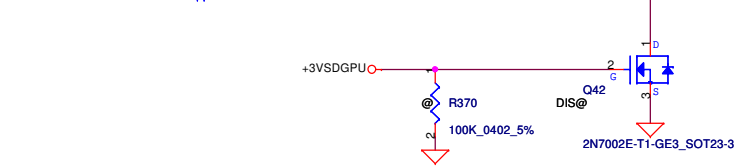
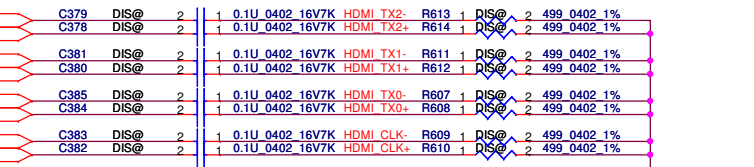
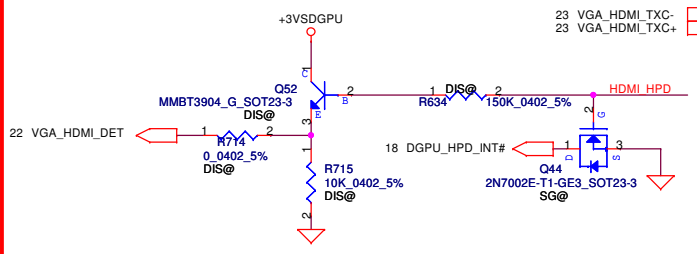
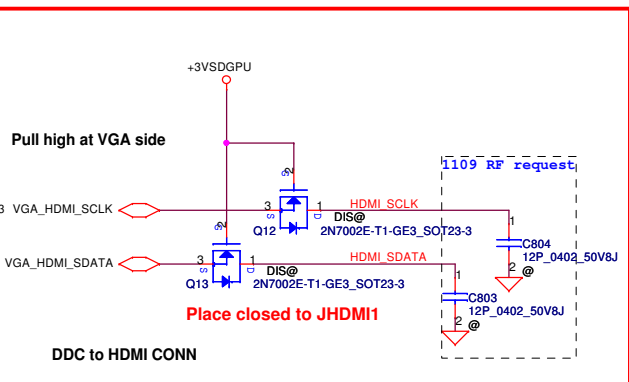
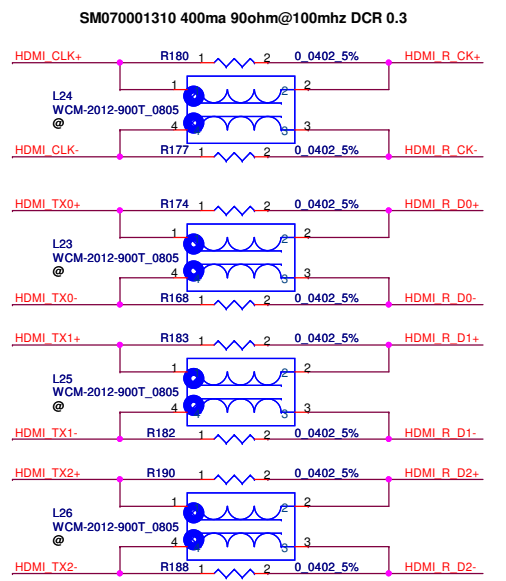
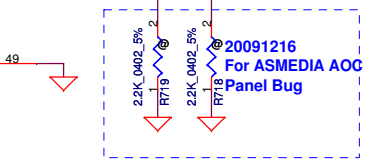
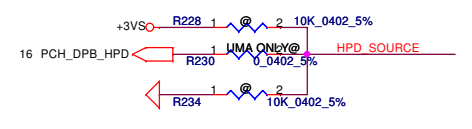


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Issued Date	2009/08/01	Deciphered Date	2010/08/01	CRT Connector	
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				Date:	Tuesday, December 22, 2009
				Sheet	29 of 56



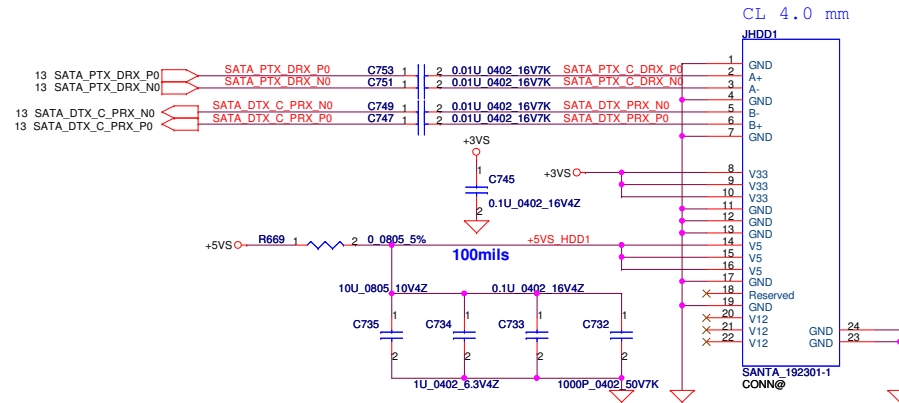
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0	0	12dB
0	1	9dB
1	0	6dB
1	1	3dB (default)

CG0	CG1	CG2	Swing	Pre-amp	Slew-rate
0	0	0	450	0	0
0	0	1	420	0	-3db
0	1	0	450	0	-3db (default)
0	1	1	460	0	-4db
1	0	0	340	0	0
1	0	1	400	2db	0
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1	1	1	420	0	0

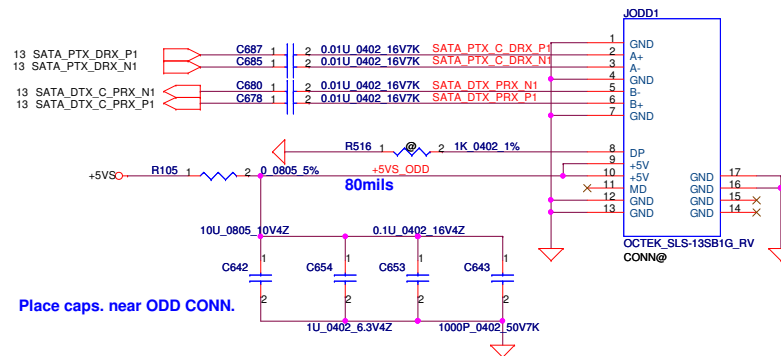


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Size	Document Number	Date		Rev	
Custom	NEW71/91 M/B LA-5893P Schematic	Tuesday, December 22, 2009		Sheet 30 of 56	

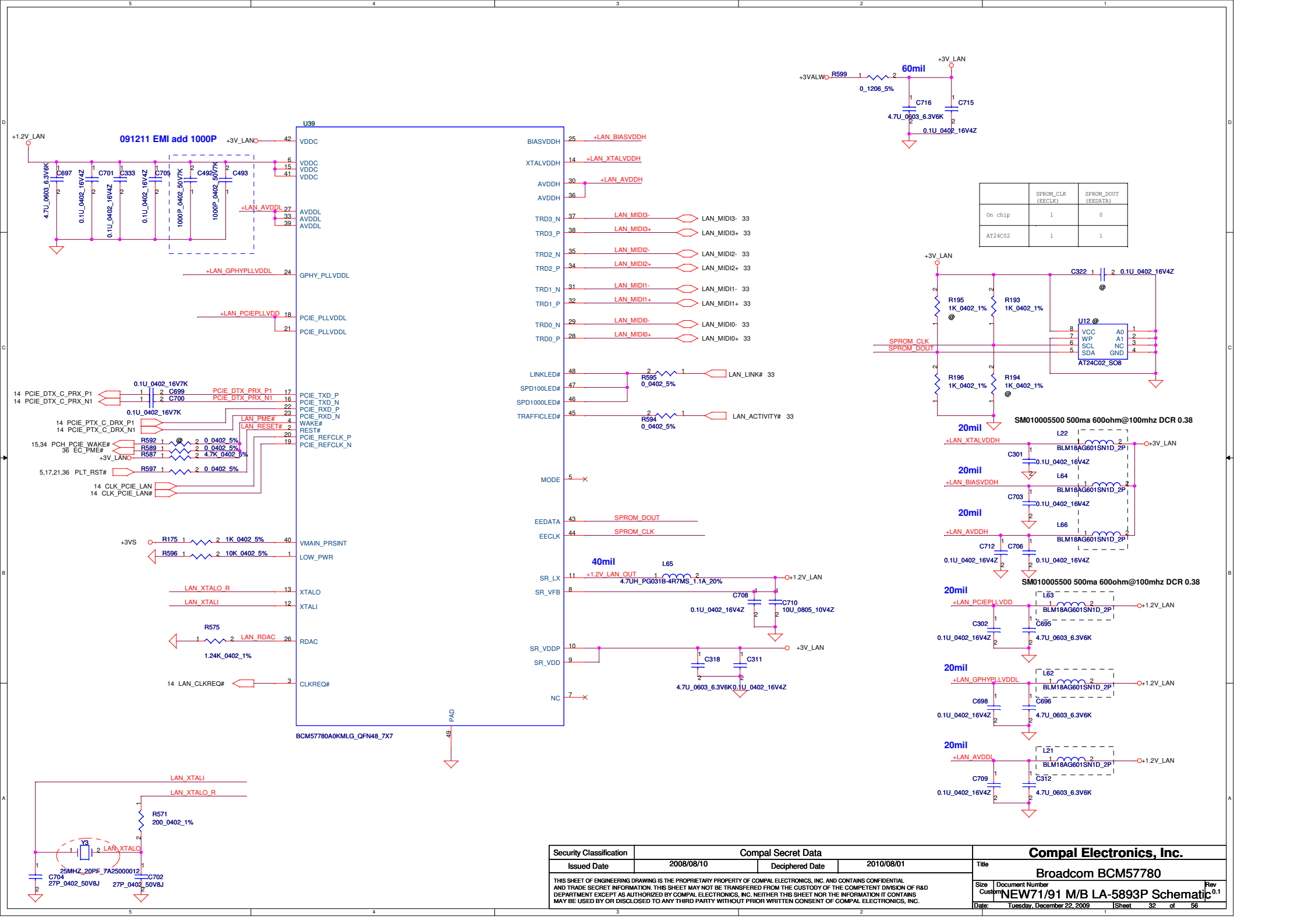
### SATA HDD1 Conn.



### SATA ODD Conn.



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Issued Date	2008/08/10	Deciphered Date	2010/08/01	Title HDD & ODD Connector		
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	SPMR_CLK (EECLK)	SPMR_DOUT (EEDATA)
On chip	1	0
AT24C02	1	1

SM010005500 500ma 600ohm@100mhz DCR 0.38

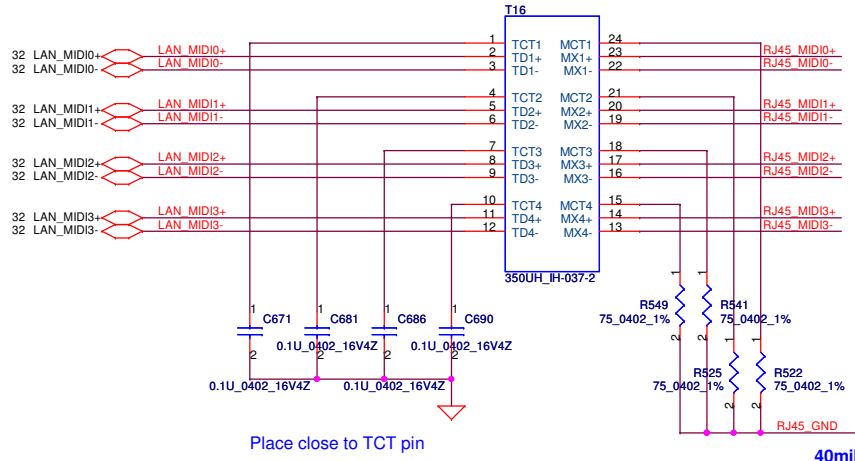
SM010005500 500ma 600ohm@100mhz DCR 0.38

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Issued Date	2008/08/10	Deciphered Date	2010/08/01
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Compal Electronics, Inc.			
Broadcom BCM57780			
Title	Document Number	Rev	
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Date:	Tuesday, December 22, 2009	Sheet	32 of 56



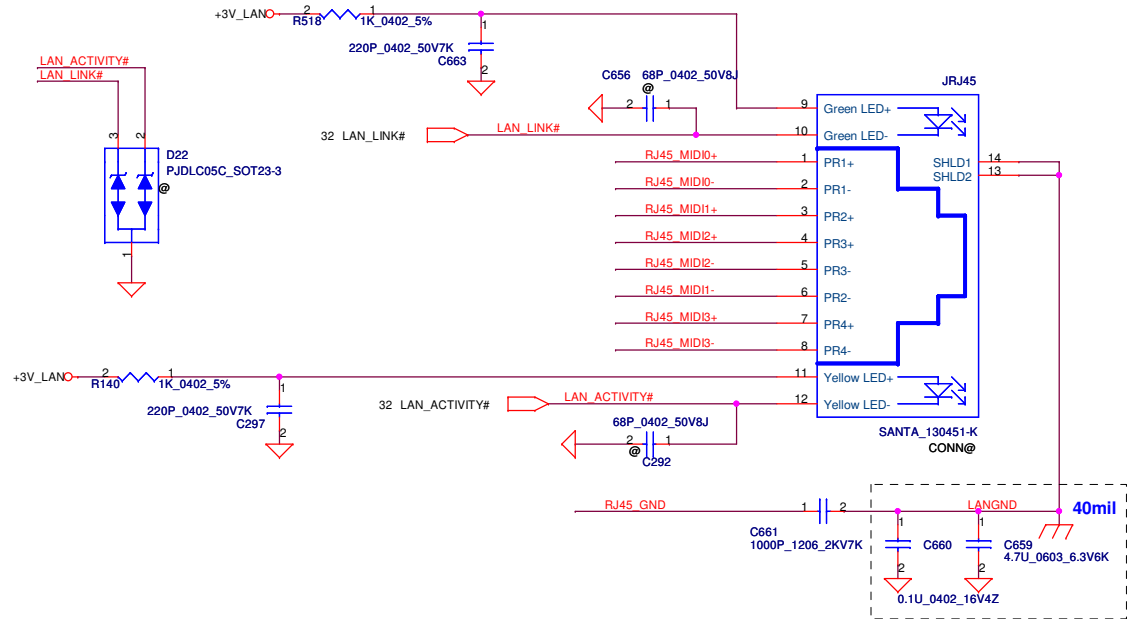
# LAN Connector



Place close to TCT pin

BOTHHAND: S X'FORM\_GST5009-D LF LAN, SP050006B00  
 TIMAG:S X'FORM\_IH-160 LAN , SP050006F00

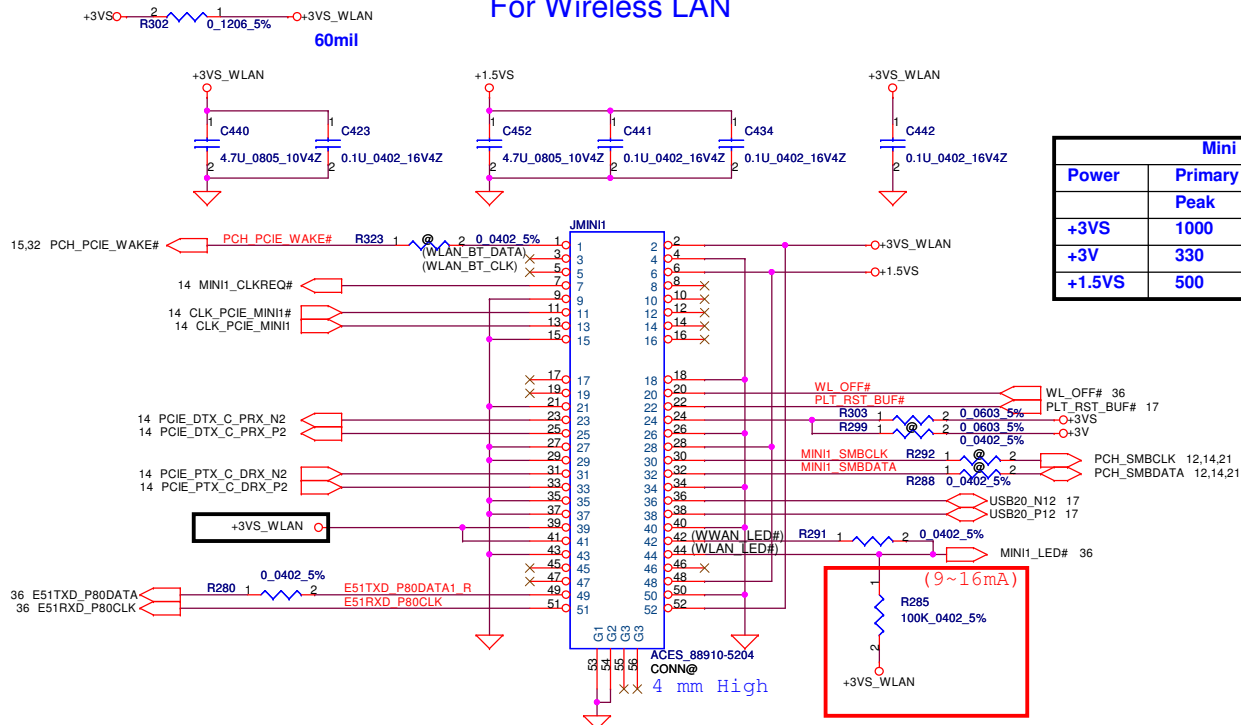
40mil



40mil

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Size	Document Number	Date		Rev	0.1
Customer	NEW71/91 M/B LA-5893P Schematic	Tuesday, December 22, 2009		Sheet	33 of 56

# For Wireless LAN

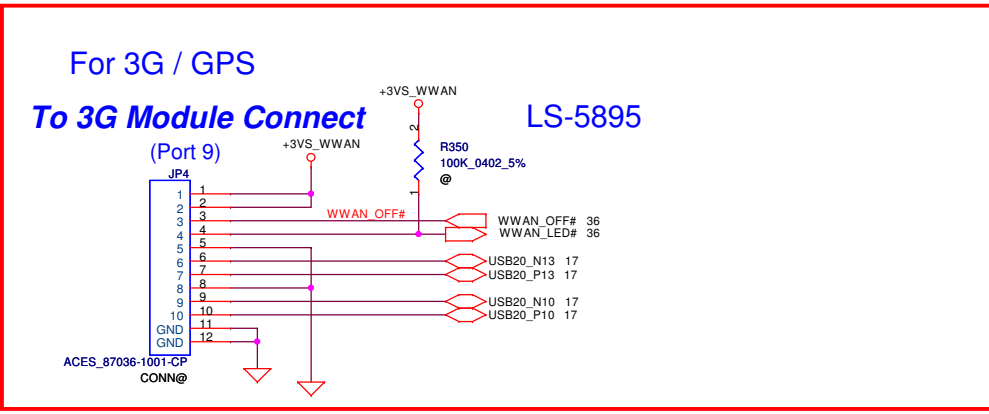
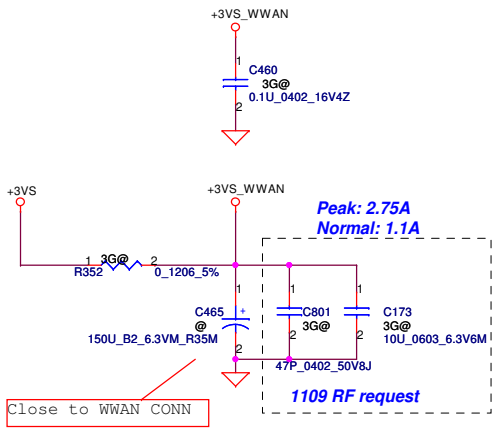


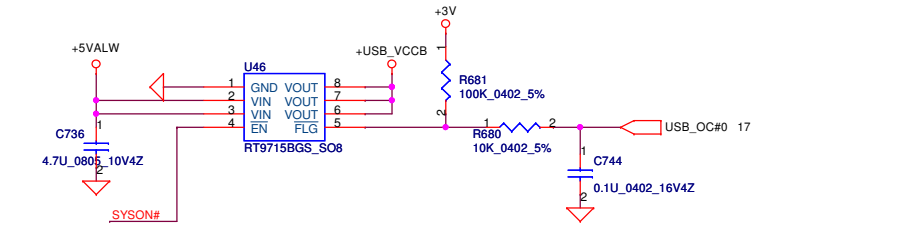
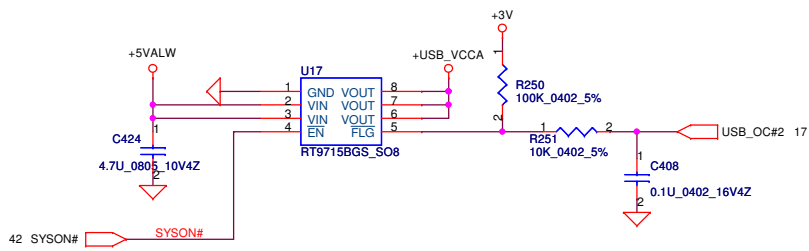
Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

# For 3G / GPS

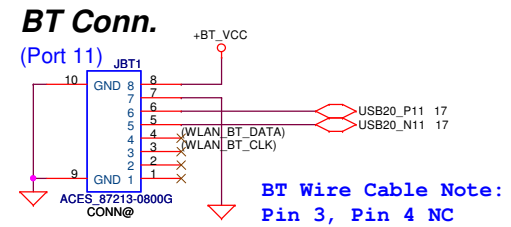
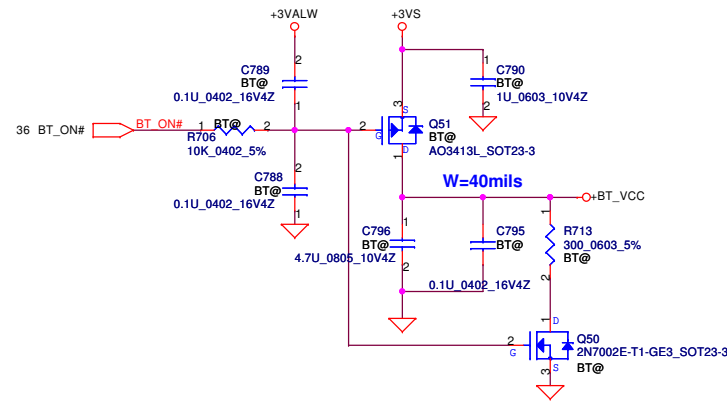
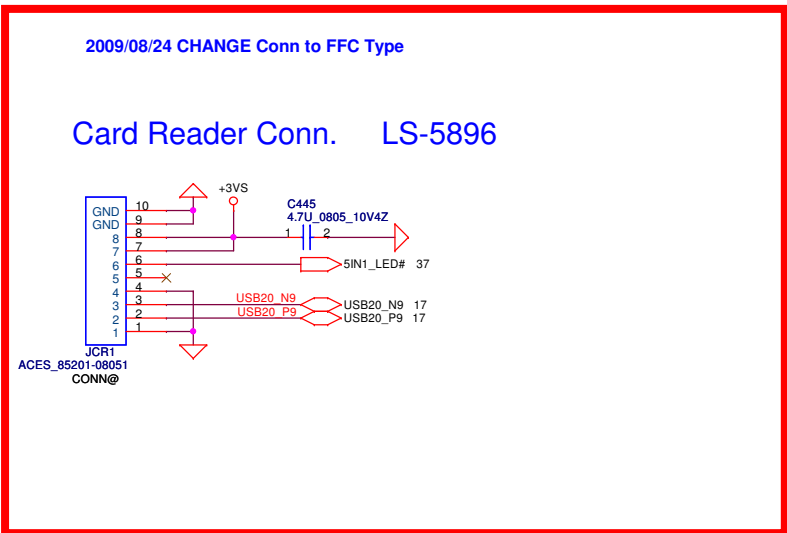
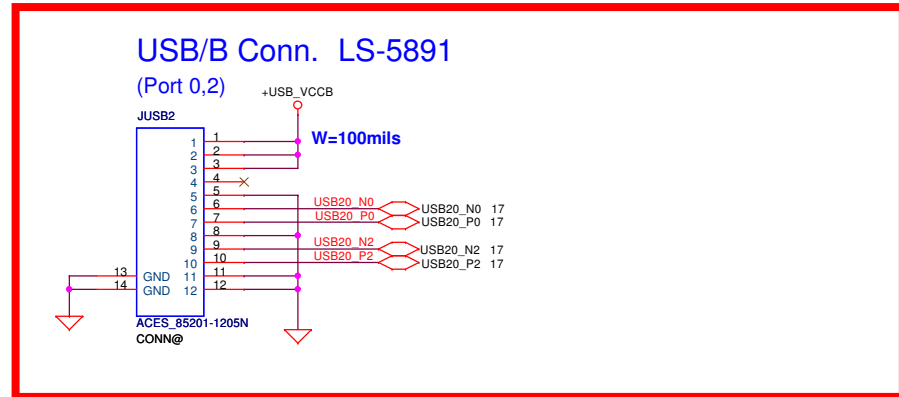
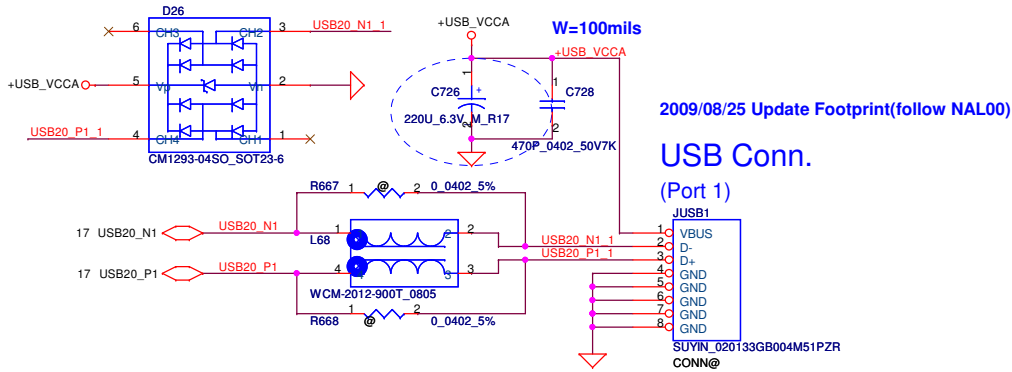
## To 3G Module Connect

LS-5895

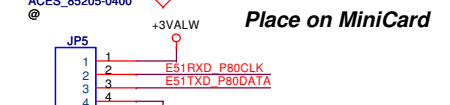
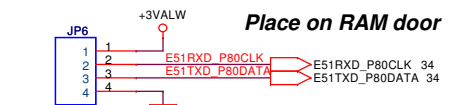
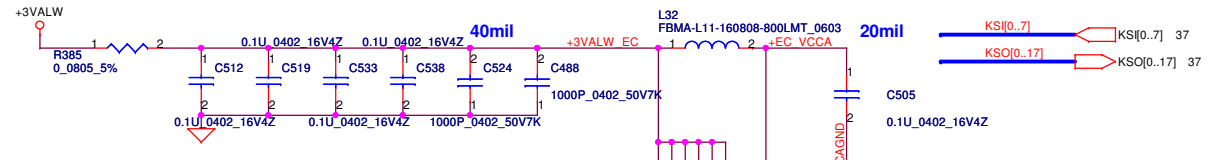




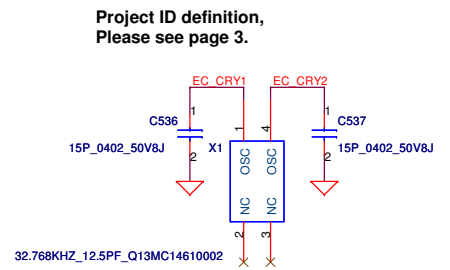
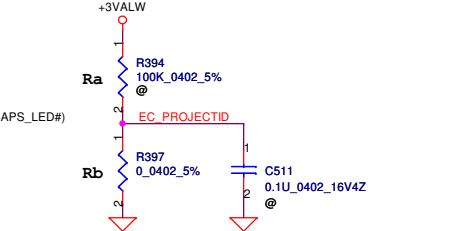
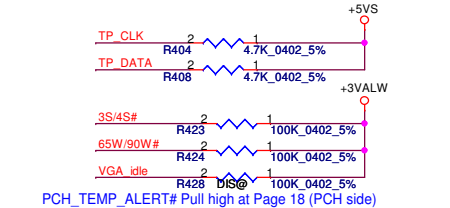
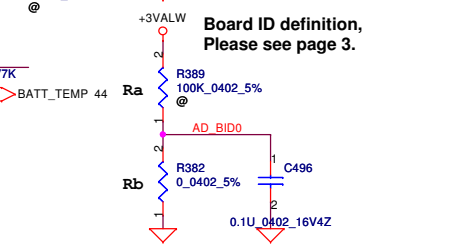
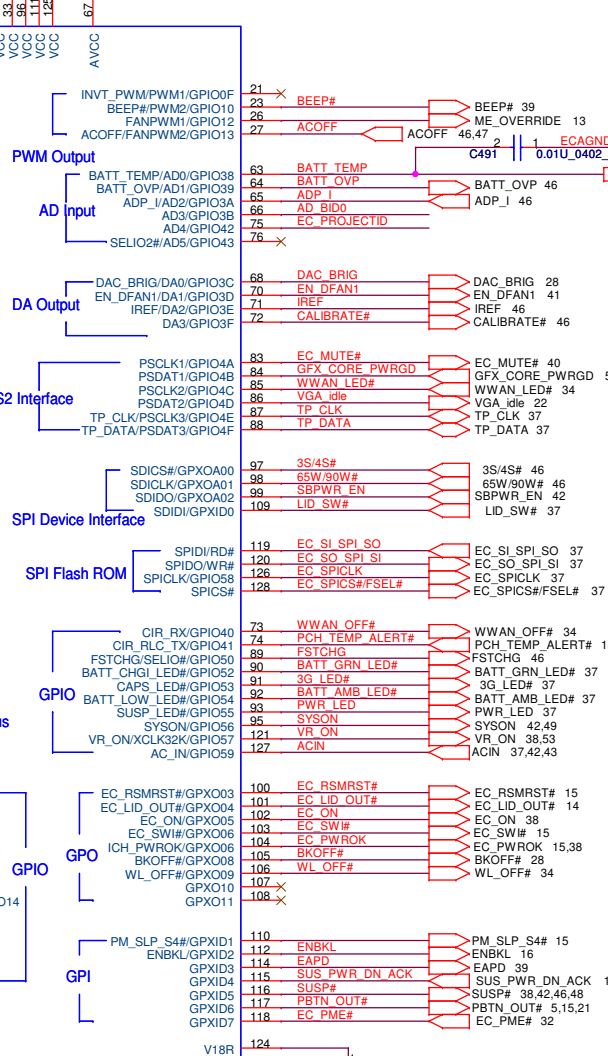
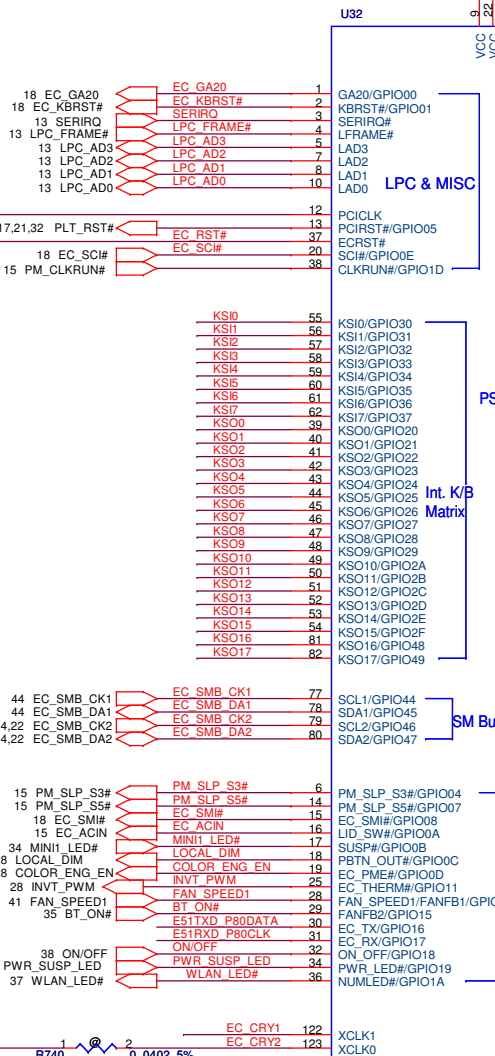
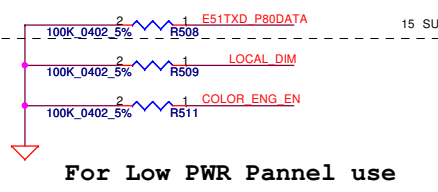
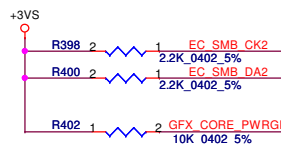
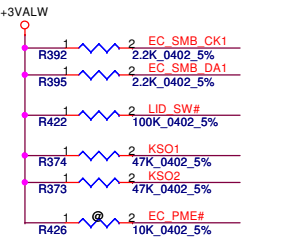
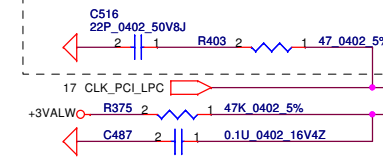
2009/08/14 CHANGE cap



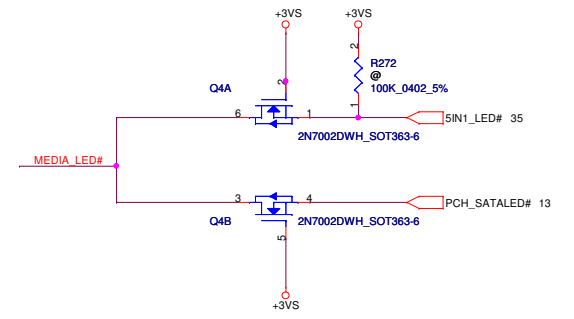
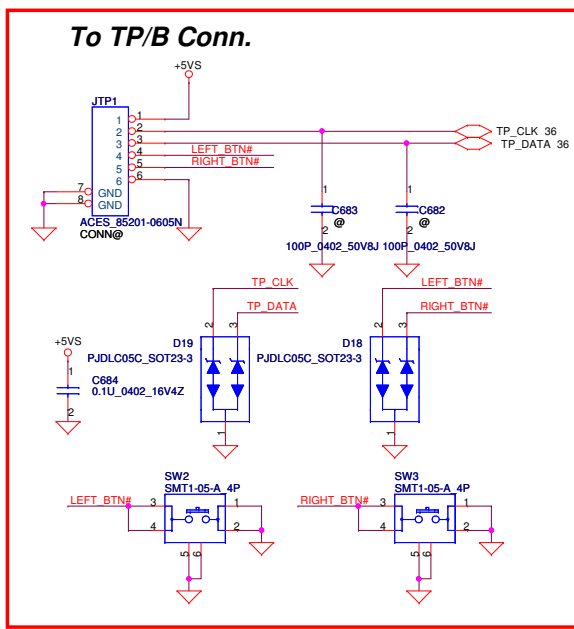
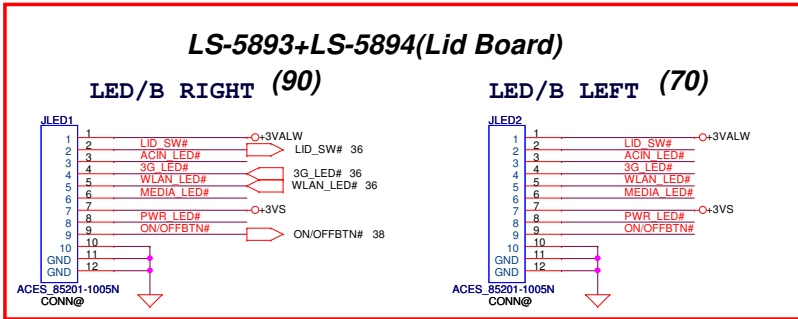
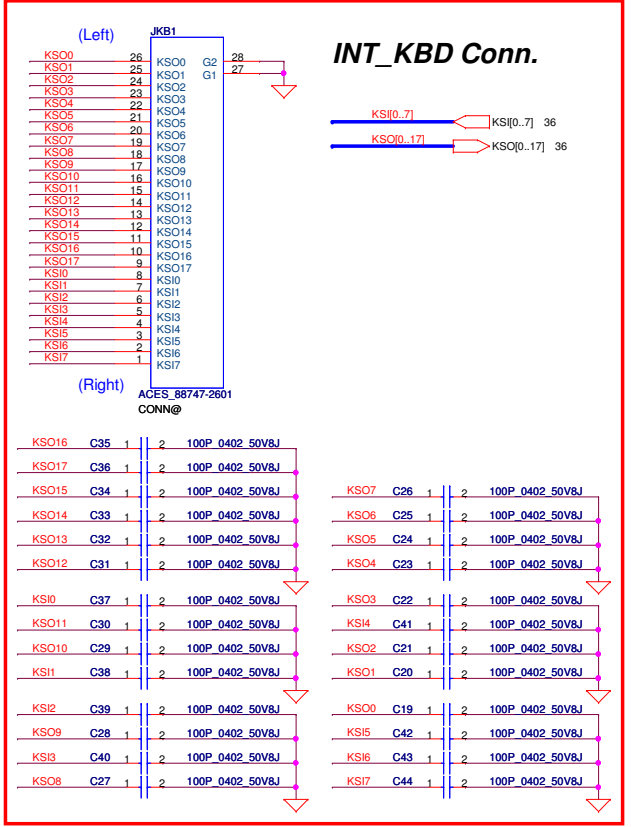
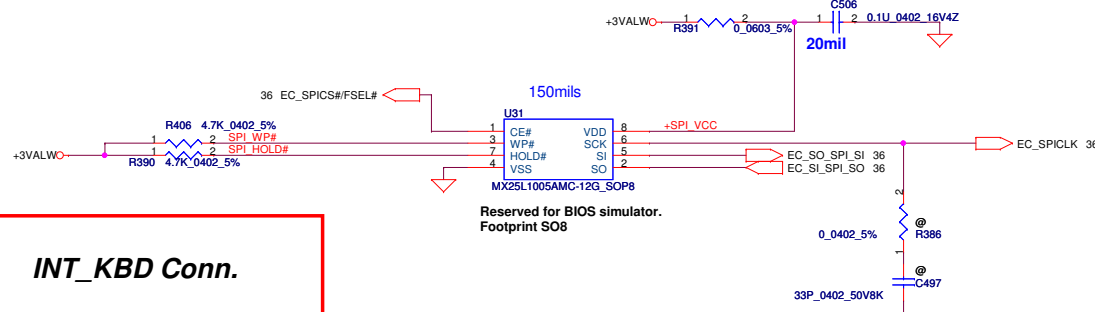
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Issued Date	2008/08/10	Deciphered Date	2010/08/01	Title	
				USB / BT / USBB	
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Size	Document Number			Rev	0.1
Customer	NEW71/91 M/B LA-5893P Schematic				
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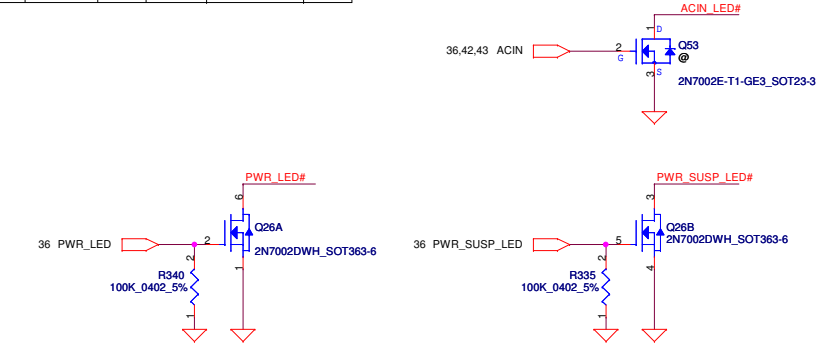
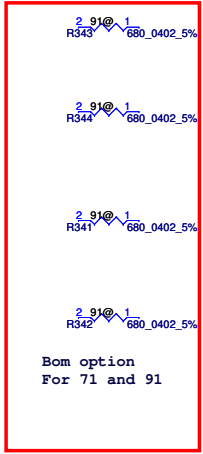
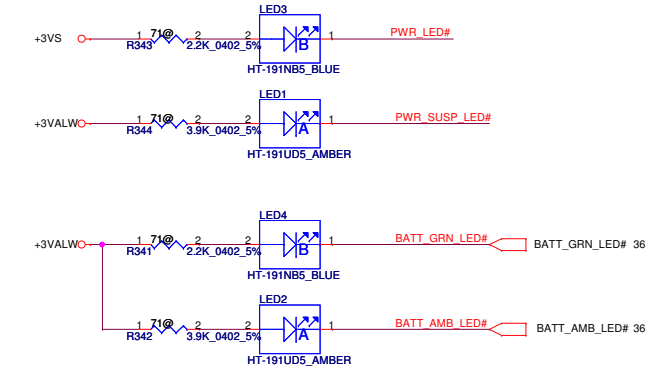
1109 RF request



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Size	Document Number	Date		Rev	
B	NEW71/91 M/B LA-5893P Schematic	Tuesday, December 22, 2009		0.1	
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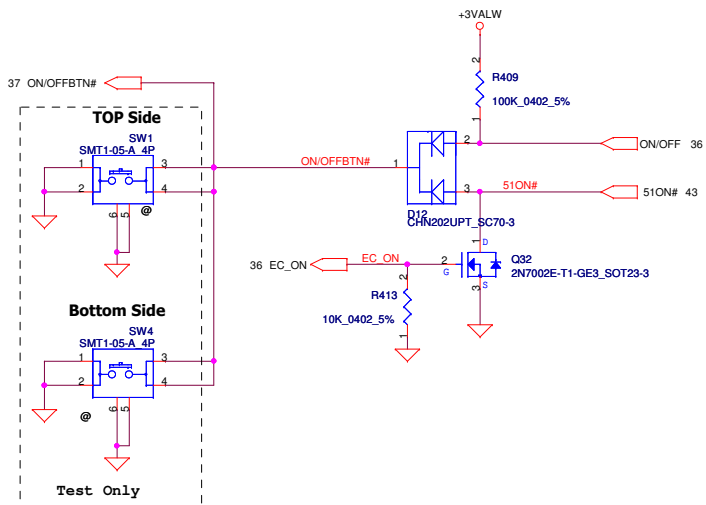
LED Status	Power/SUS		Battery		3G/WLAN		BlueTooth	ACIN
	ON	SUS	Full	Charge	3G	WLAN		
NEW70/80/90	Blue	Amber	Blue	Amber	Blue	Amber		



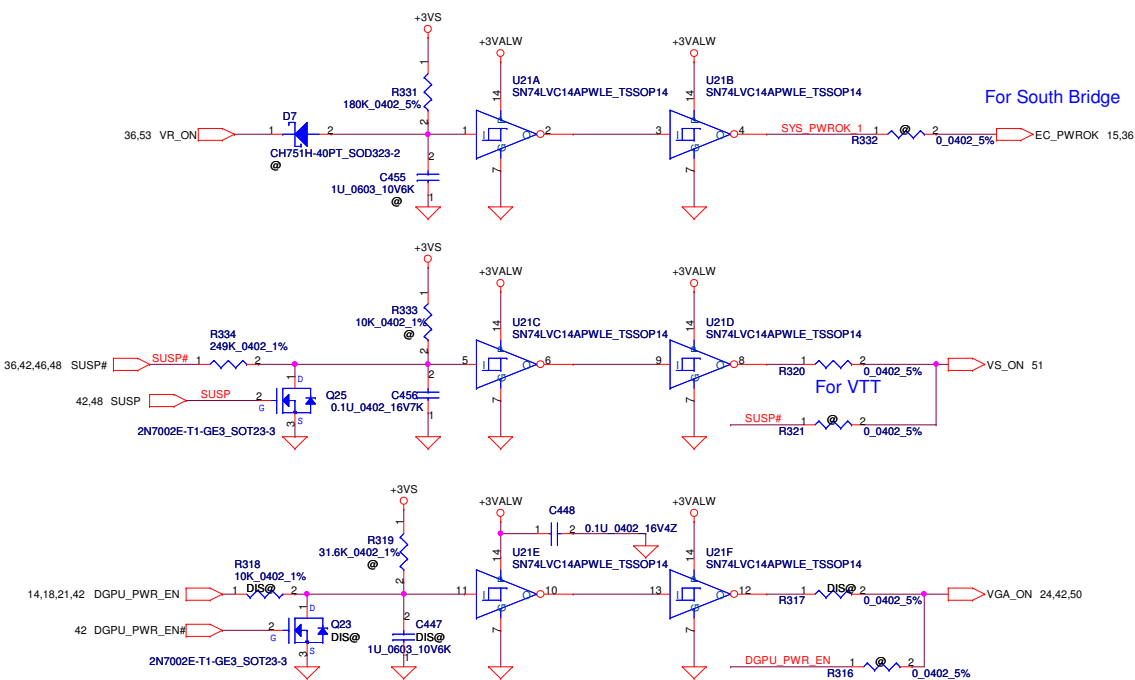
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/08/10	Deciphered Date	2010/08/01	Title
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Size	Document Number	Rev		
B	NEW71/91 M/B LA-5893P Schematic	0.1		
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# Power Button

ON/OFF switch



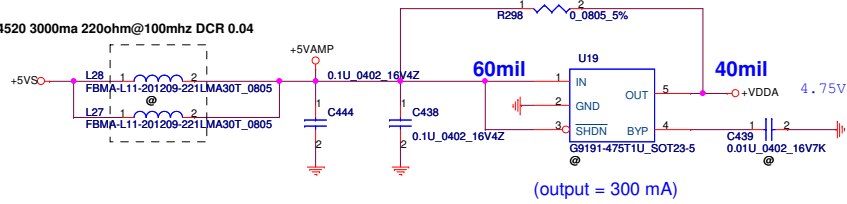
# Power ON Circuit



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/08/10	Deciphered Date	2010/08/01	Title	
				Power OK	
Size	Document Number			Rev	
B	NEW71/91 M/B LA-5893P Schematic			0.1	
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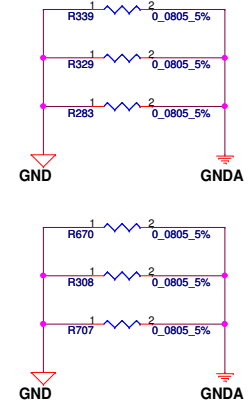
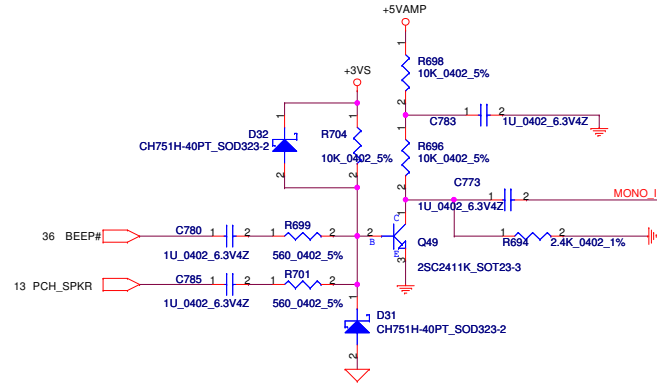
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SM010014520 3000ma 220ohm@100mhz DCR 0.04

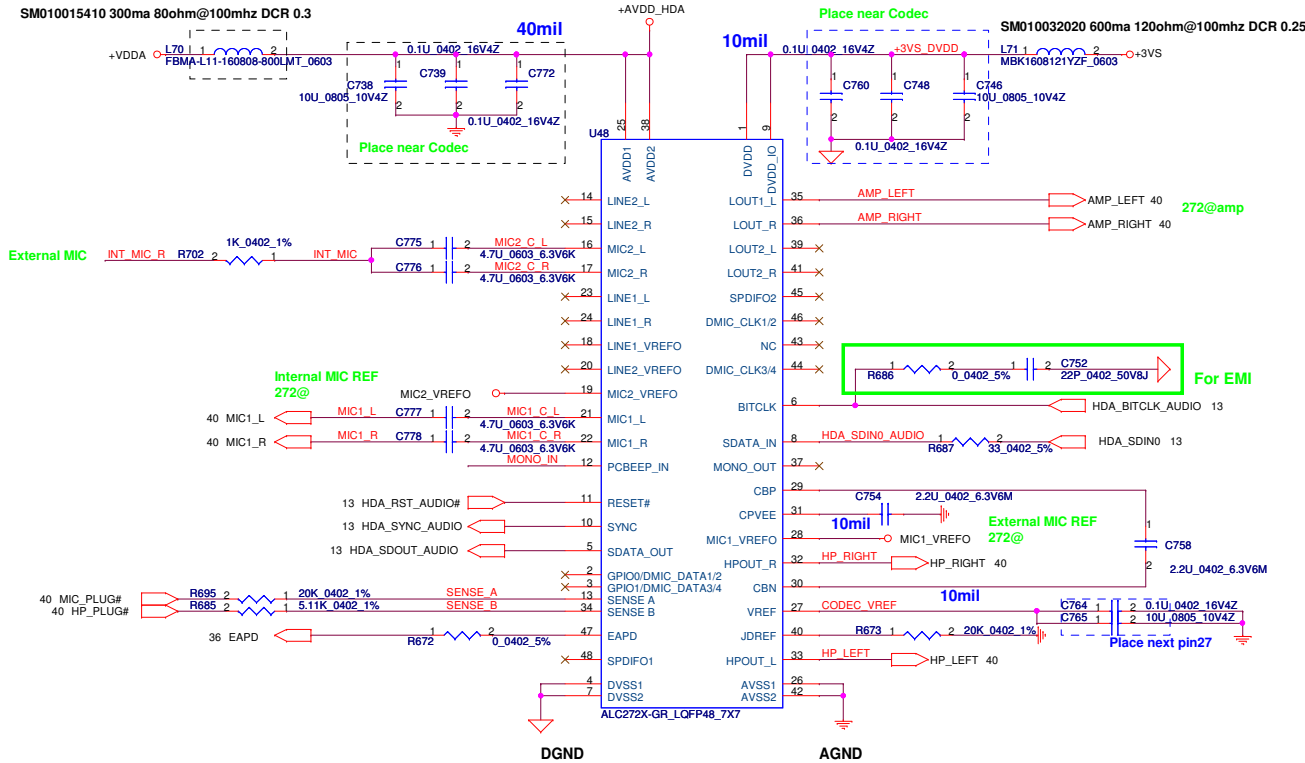


(output = 300 mA)

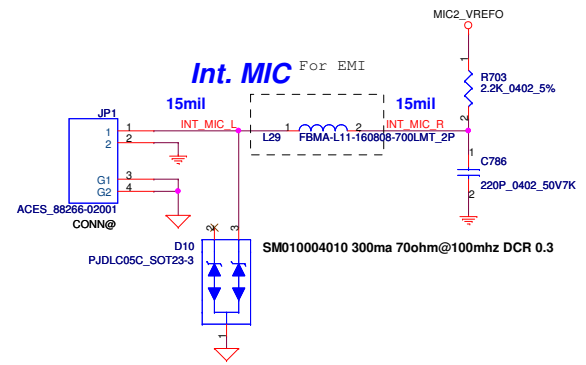
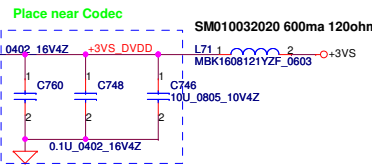
### HD Audio Codec



SM010015410 300ma 80ohm@100mhz DCR 0.3

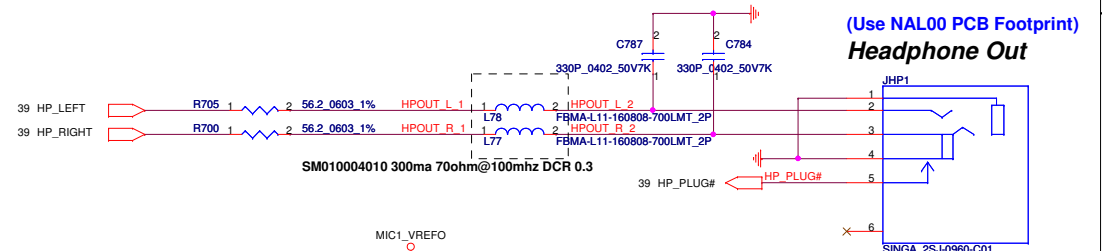
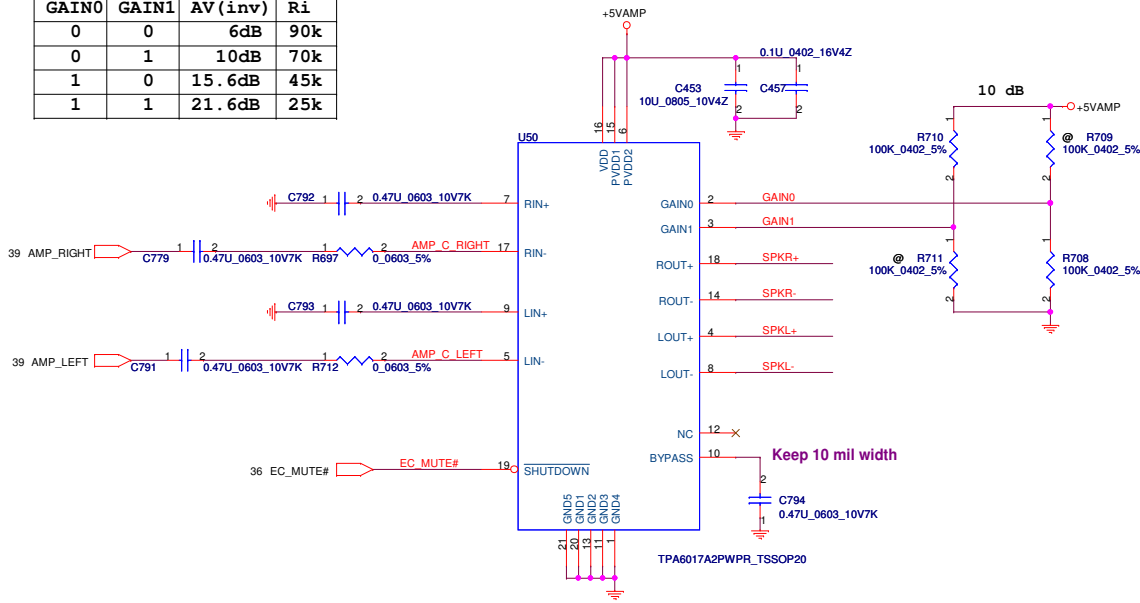


SM010032020 600ma 120ohm@100mhz DCR 0.25



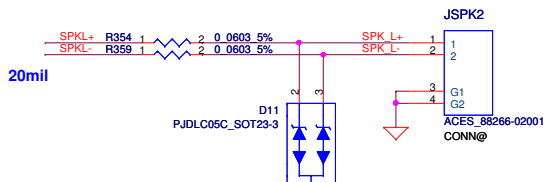
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Issued Date	2008/08/10	Deciphered Date	2010/08/01	Title		
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GAIN0	GAIN1	AV (inv)	Ri
0	0	6dB	90k
0	1	10dB	70k
1	0	15.6dB	45k
1	1	21.6dB	25k

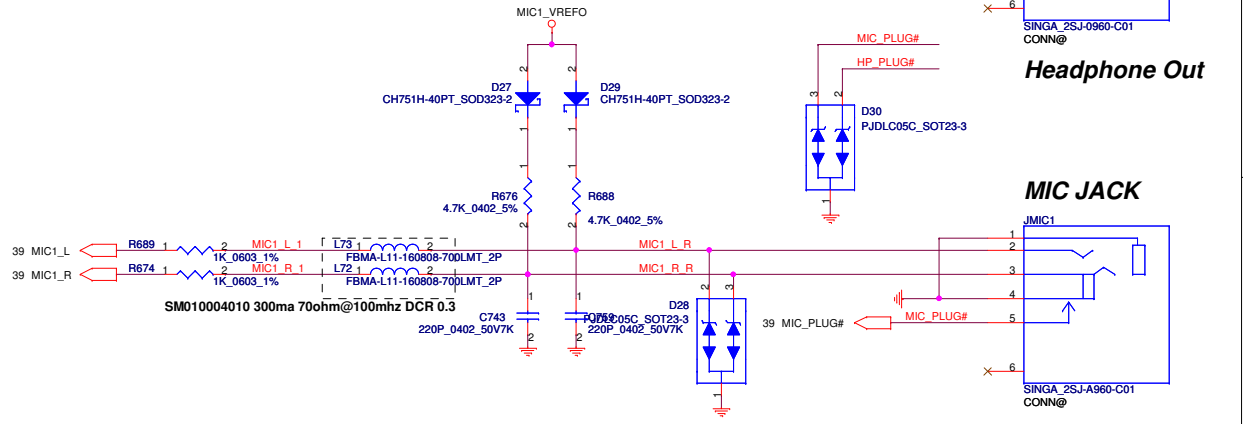
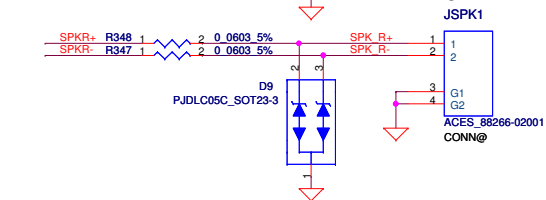


**Int. Speaker Conn.**

Left Side



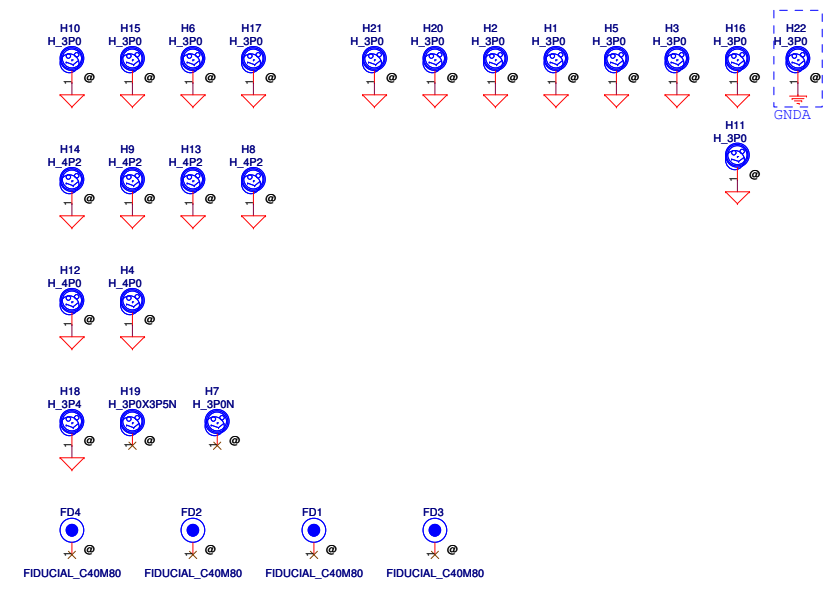
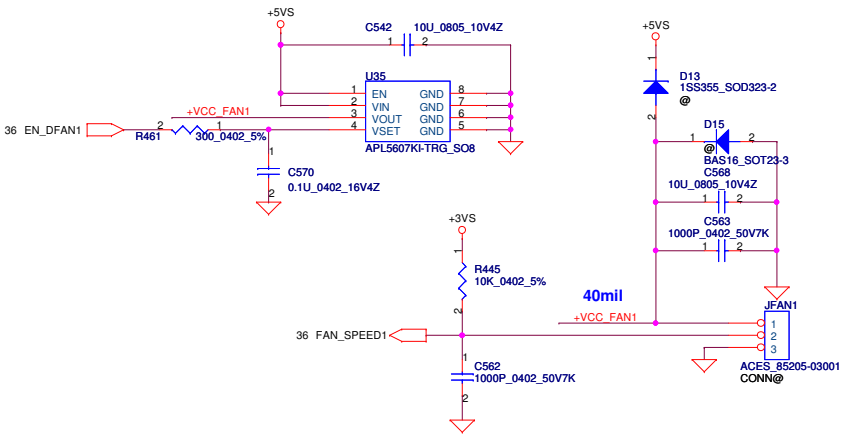
Right Side



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				Amplifier & Audio Jack	
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				Customer	NEW71/91 M/B LA-5893P Schematic 0.1
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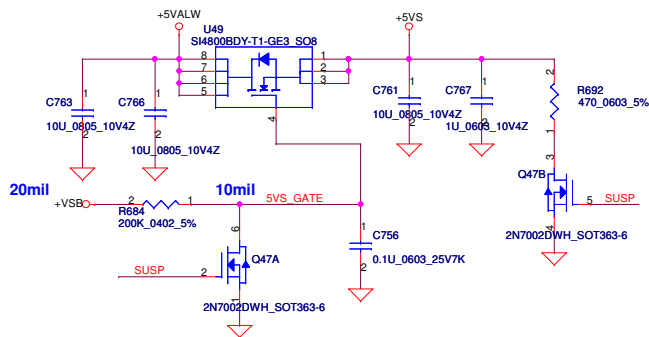


### FAN1 Conn

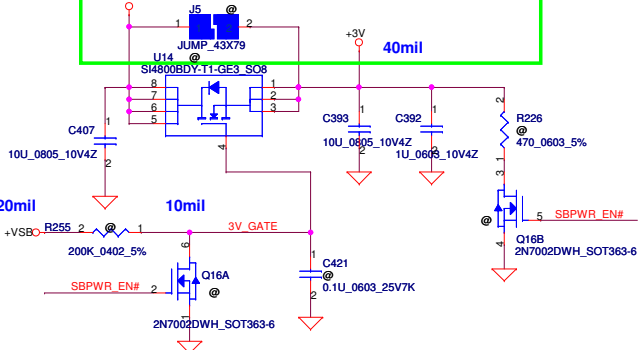


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Size	Document Number	Rev		
B	NEW71/91 M/B LA-5893P Schematic	0.1		
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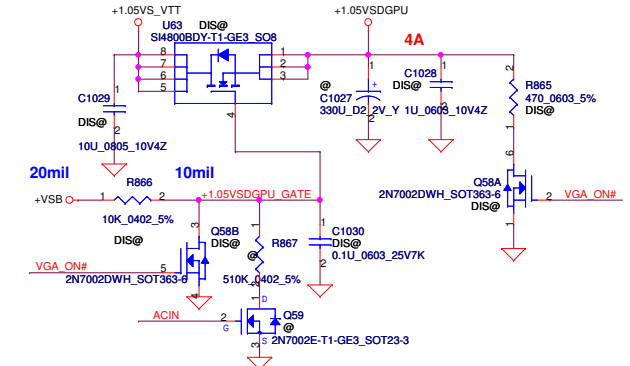
**+5VALW TO +5VS**



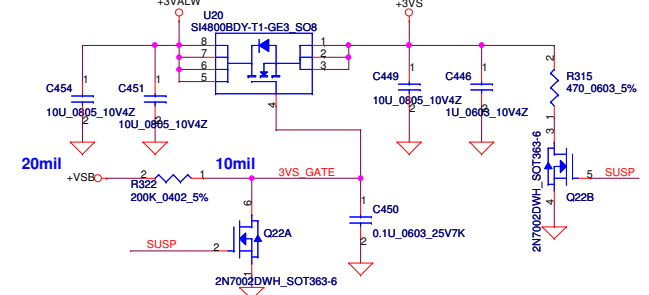
**+3VALW TO +3V(PCH AUX SUS3.3)**



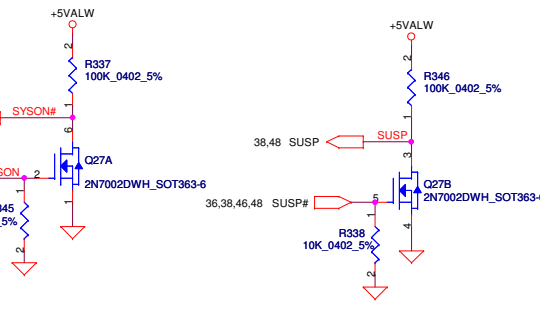
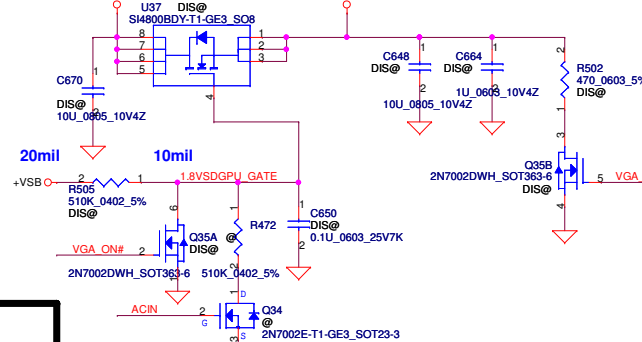
**+1.05VS\_VTT to +1.05VSDGPU for GPU**



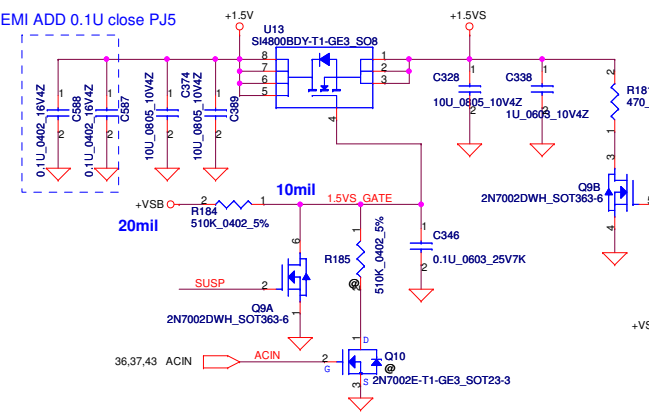
**+3VALW TO +3VS**



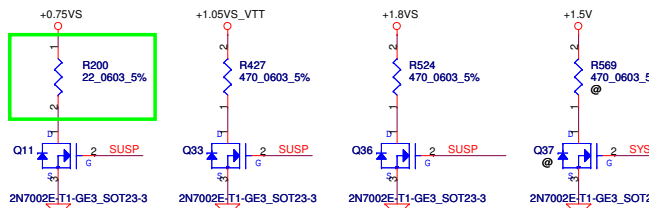
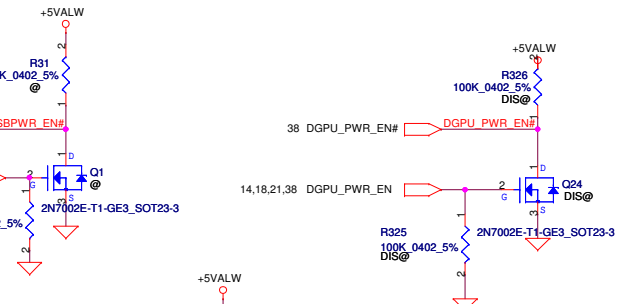
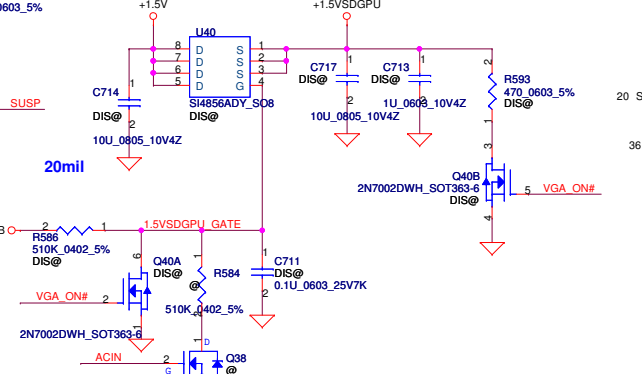
**+1.8VS to +1.8VSDGPU for GPU**



**+1.5V to +1.5V**

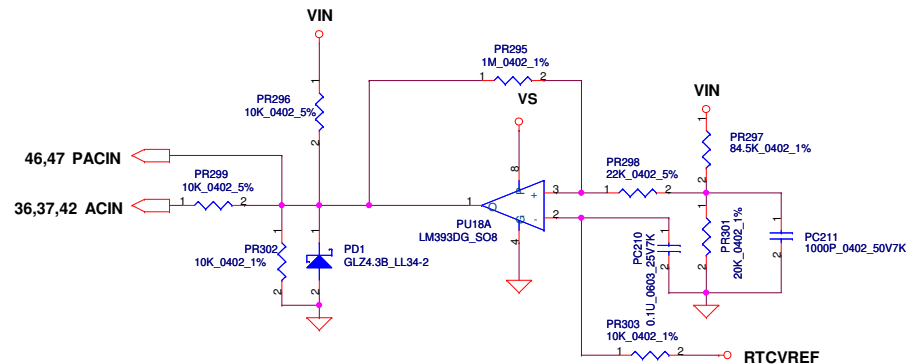
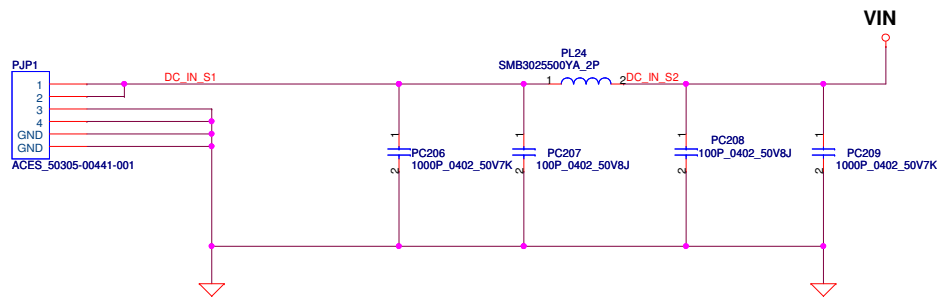


**+1.5V to +1.5VSDGPU for GPU**

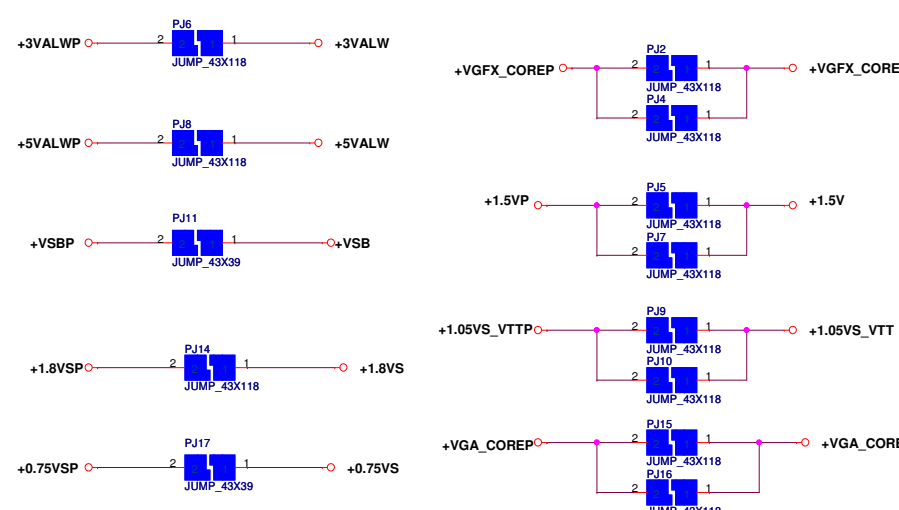
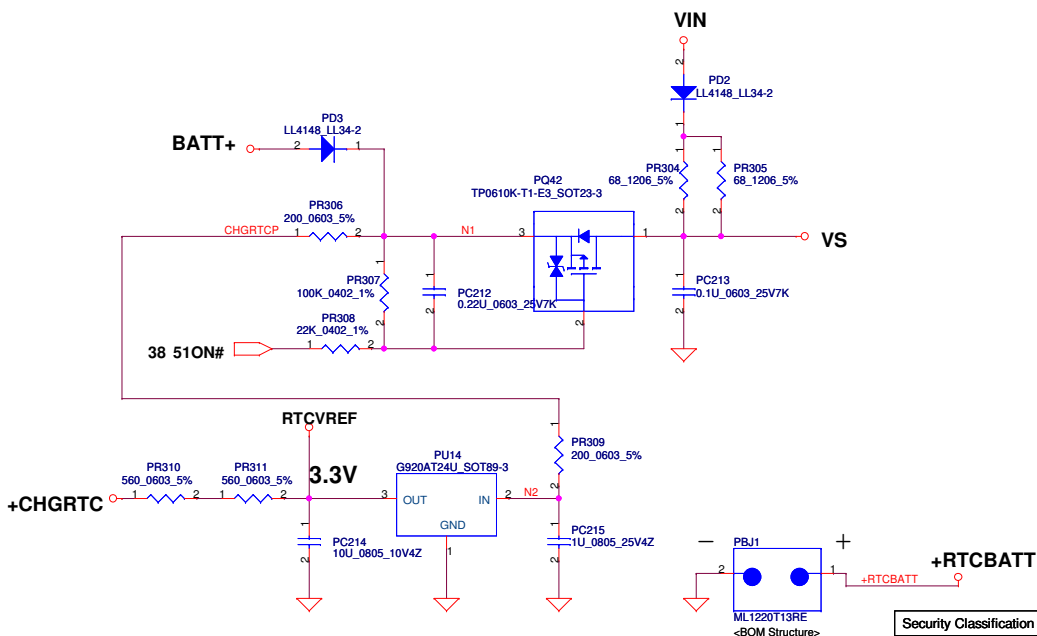


2009/08/14  
 CP\_S3PowerReduction  
 WhitePaper\_Rev0.9  
 0.75VS speed up discharge

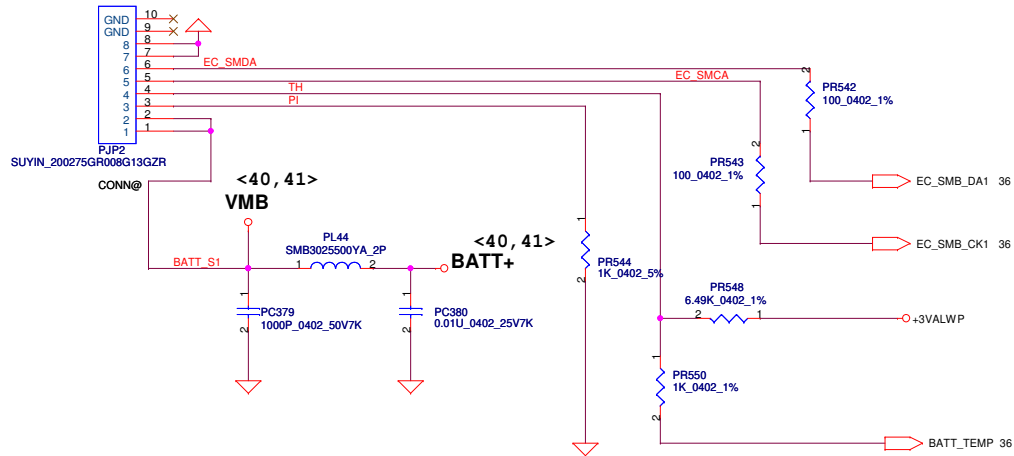
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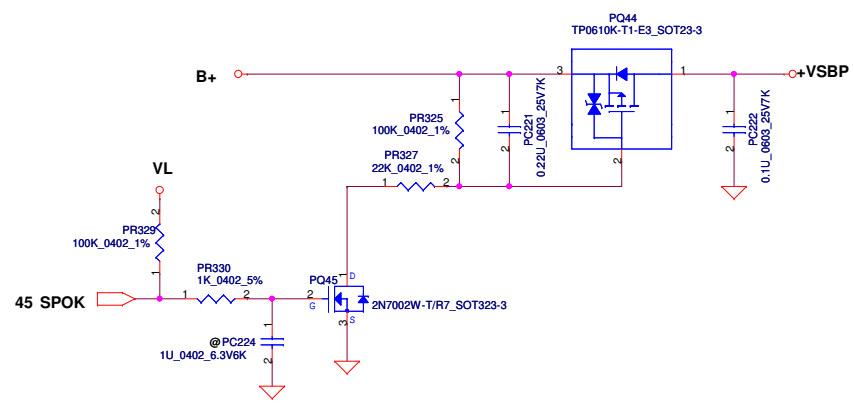
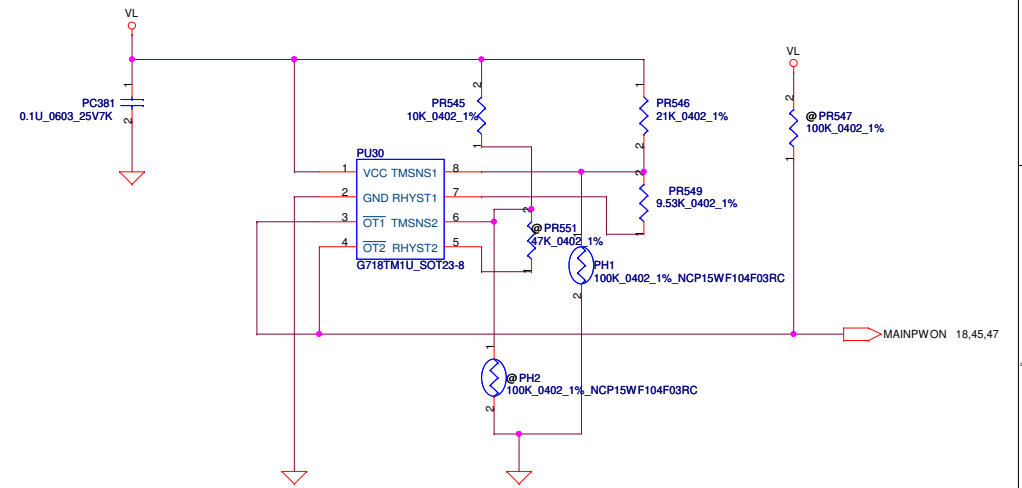
Vin Dectector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V



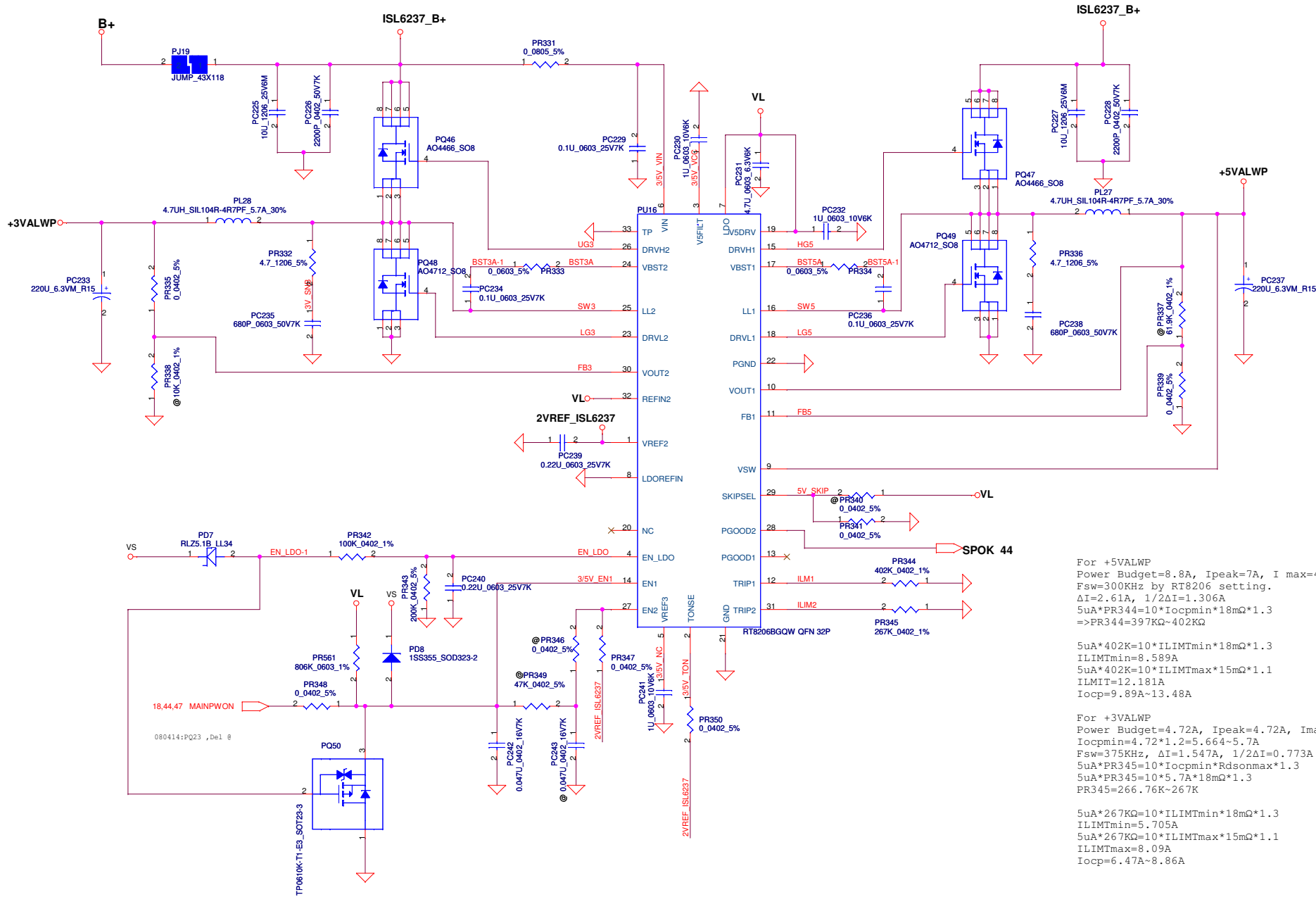
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Issued Date	2007/09/20	Deciphered Date	2010/08/01	Title <b>DCIN &amp; DETECTOR</b>				
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PH1 under CPU botten side :  
CPU thermal protection at 92 degree C



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For +5VALWP  
 Power Budget=8.8A, Ipeak=7A, I max=4.9A  
 Fsw=300KHz by RT8206 setting.  
 $\Delta I=2.61A$ ,  $1/2\Delta I=1.306A$   
 $5uA*PR344=10*Iocpmin*18m\Omega*1.3$   
 $\Rightarrow PR344=397K\Omega-402K\Omega$

$5uA*402K=10*ILIMITmin*18m\Omega*1.3$   
 $ILIMITmin=8.589A$   
 $5uA*402K=10*ILIMITmax*15m\Omega*1.1$   
 $ILIMIT=12.181A$   
 $Iocp=9.89A-13.48A$

For +3VALWP  
 Power Budget=4.72A, Ipeak=4.72A, I max=4A  
 $Iocpmin=4.72*1.2=5.664\sim 5.7A$   
 $Fsw=375KHz$ ,  $\Delta I=1.547A$ ,  $1/2\Delta I=0.773A$   
 $5uA*PR345=10*Iocpmin*18m\Omega*1.3$   
 $5uA*PR345=10*5.7A*18m\Omega*1.3$   
 $PR345=266.76K\sim 267K$

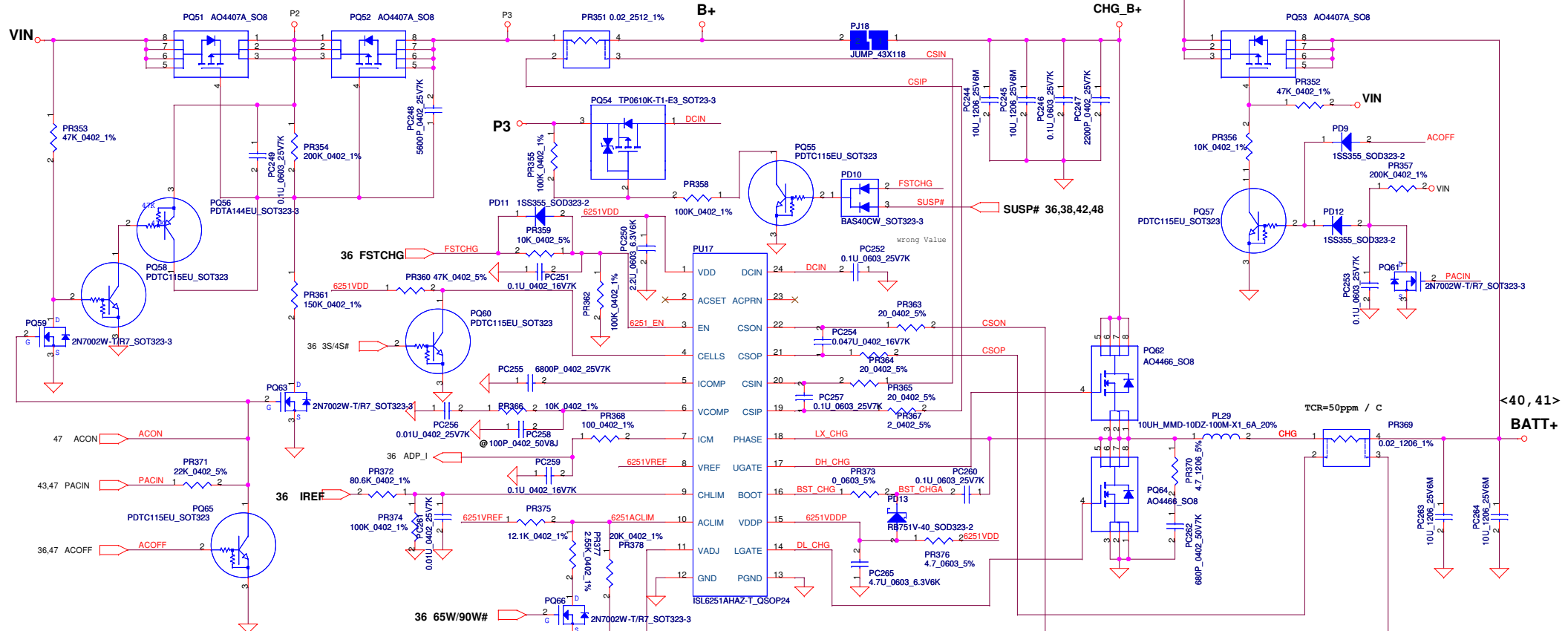
$5uA*267K=10*ILIMITmin*18m\Omega*1.3$   
 $ILIMITmin=5.705A$   
 $5uA*267K=10*ILIMITmax*15m\Omega*1.1$   
 $ILIMITmax=8.09A$   
 $Iocp=6.47A-8.86A$

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Custom	NEW71	0.1		

Iada=0~4.74A (90W/19V=4.736A)  
 Iada=0~3.42A (90W/19V=3.421A)

ADP\_I = 19.9\*Iadapter\*Rsense

CP = 85%\*Iada ; CP = 4.07A  
 CP = 85%\*Iada ; CP = 2.91A



**CP mode**  
 $I_{input} = (1/0.02) (0.05 * V_{ac1m} / 2.39 + 0.05)$   
 where  $V_{ac1m} = 1.502V$ ,  $I_{input} = 4.07A$

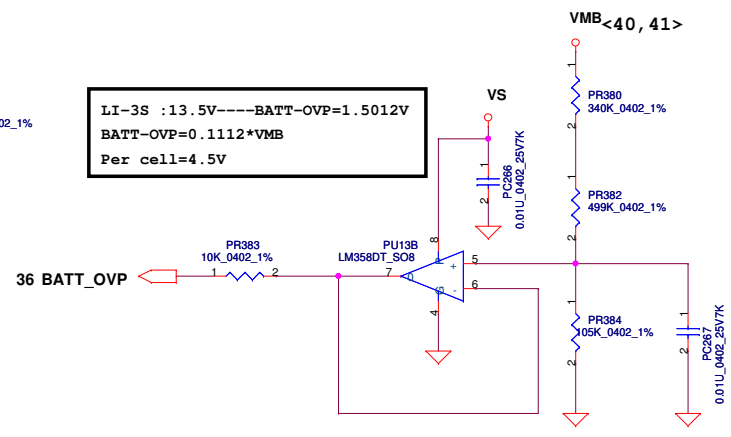
**CC=0.6~4.48A**  
 $I_{ref} = 0.7224 * I_{charge}$   
 $kI = 0.7224$   
 $I_{REF} = 0.43V \sim 3.24V$

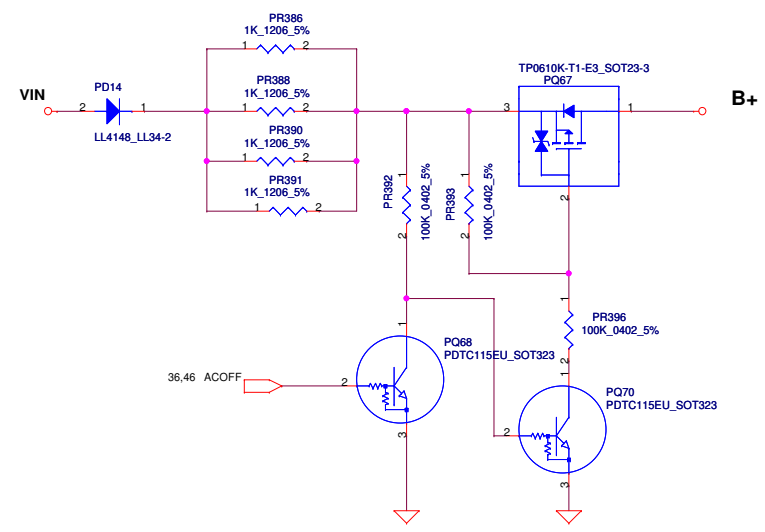
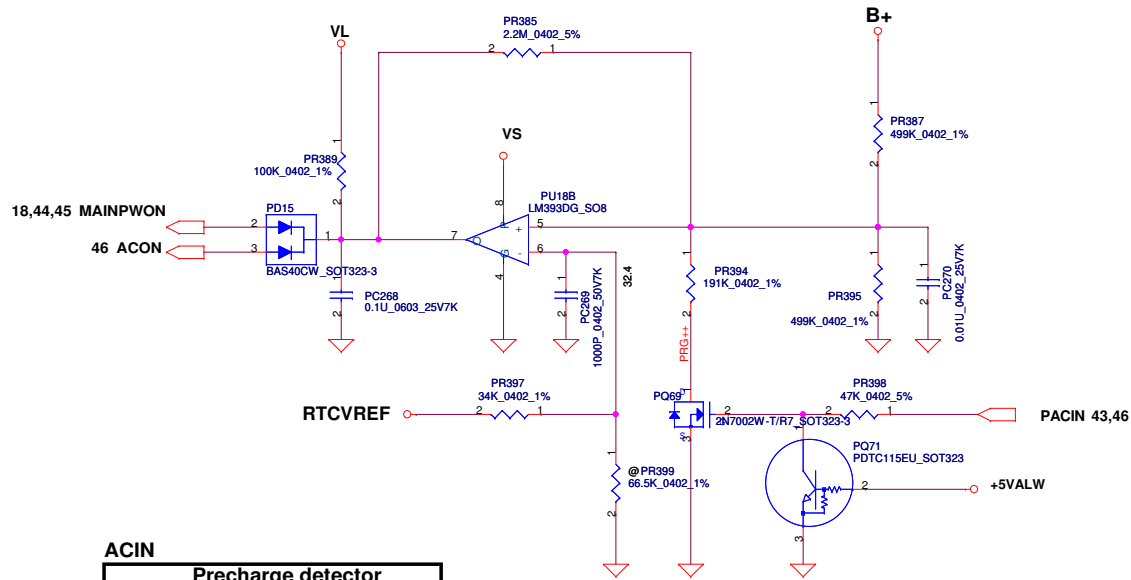
K1  
 $V_{ch1m} = I_{ref} * (PR374 / (PR372 + PR374))$   
 $= I_{ref} * (100K / (80.6K + 100K))$   
 $= I_{ref} * 0.5537$   
 $I_{charge} = (165mV / PR369) * (V_{ch1m} / 3.3V)$   
 $= (165m / 20m) * (1/3.3V) * I_{ref} * 0.5537$   
 $= 1.3842 * I_{ref}$   
 $I_{ref} = 0.7224 * I_{charge} \Rightarrow kI = 0.7224$

Kv  
 $R_{internal} = 514K$   $R_{ec} = 3K$   $R1 = PR379 = 15.4K$   $R2 = PR381 = 31.6K$   
 $R = 514K // 31.6K // (15.4K + 3K) = 1.372K$   
 $r = 514K // 514K // 31.6K = 28.14K$   
 $V_{cell} = 0.175 * V_{adj} + 3.99V$   
 $4.2V = 0.175 * V_{adj} + 3.99V \Rightarrow V_{adj} = 1.2V$   
 $V_{adj} = V_{ref} * (R / (R + 514K)) + CALIBRATE * (r / (r + 514K))$   
 $1.1463 = CALIBRATE * 0.6048 \Rightarrow CALIBRATE = 1.899$   
 $1.899 = (4.2 - (V_{cell} * 0.175)) * Kv \Rightarrow Kv = (4.2 - (4.2 * 0.175)) * Kv$   
 $A = V_{ref} * (R / (R + 514K)) = 0.052$   
 $Kv = 9.451$

**LI-3S : 1.3.5V --- BATT-OVP=1.5012V**  
 $BATT-OVP = 0.1112 * V_{MB}$   
 Per cell = 4.5V

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V





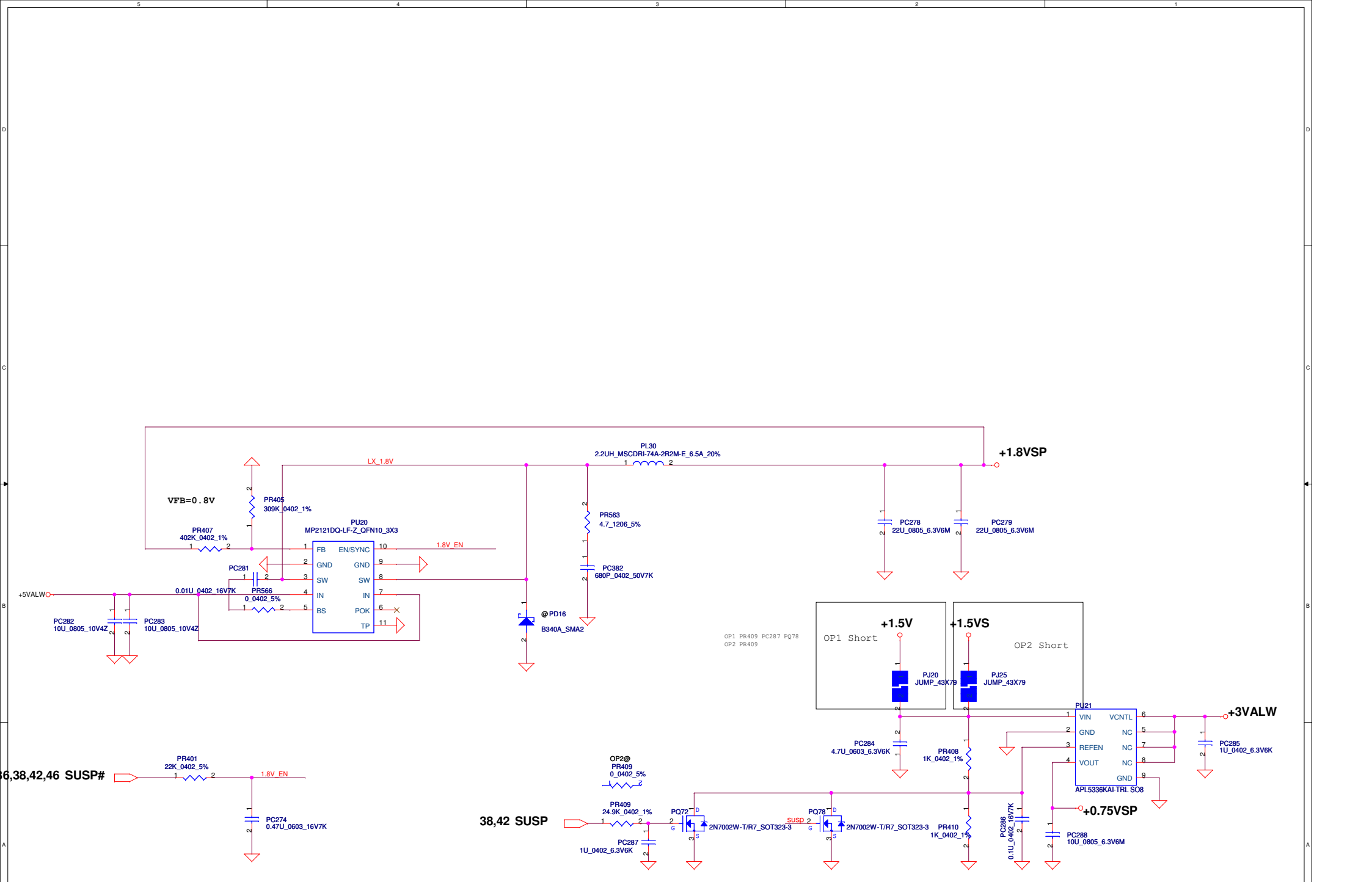
**ACIN**

Precharge detector			
	Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

**BATT ONLY**

Precharge detector			
	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

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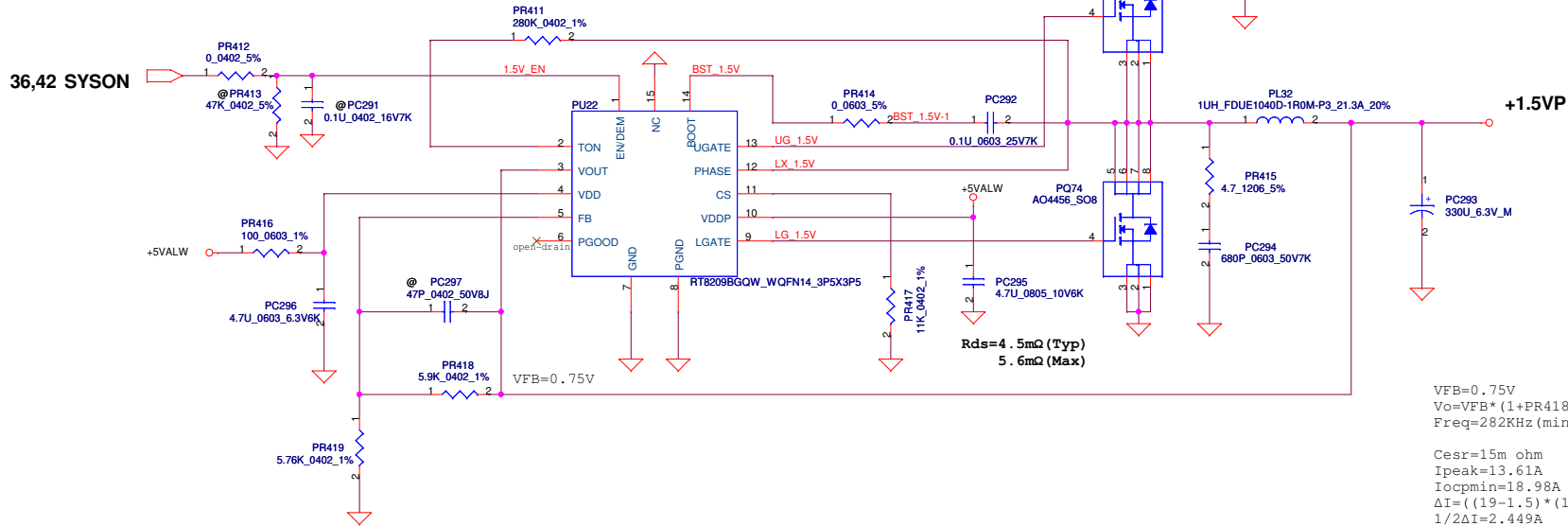


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- EN\_PSV  
 1. GND=>Disable SMPS  
 2. FLOAT=>PWM\_only mode  
 3. HIGH=>Auto\_skip mode

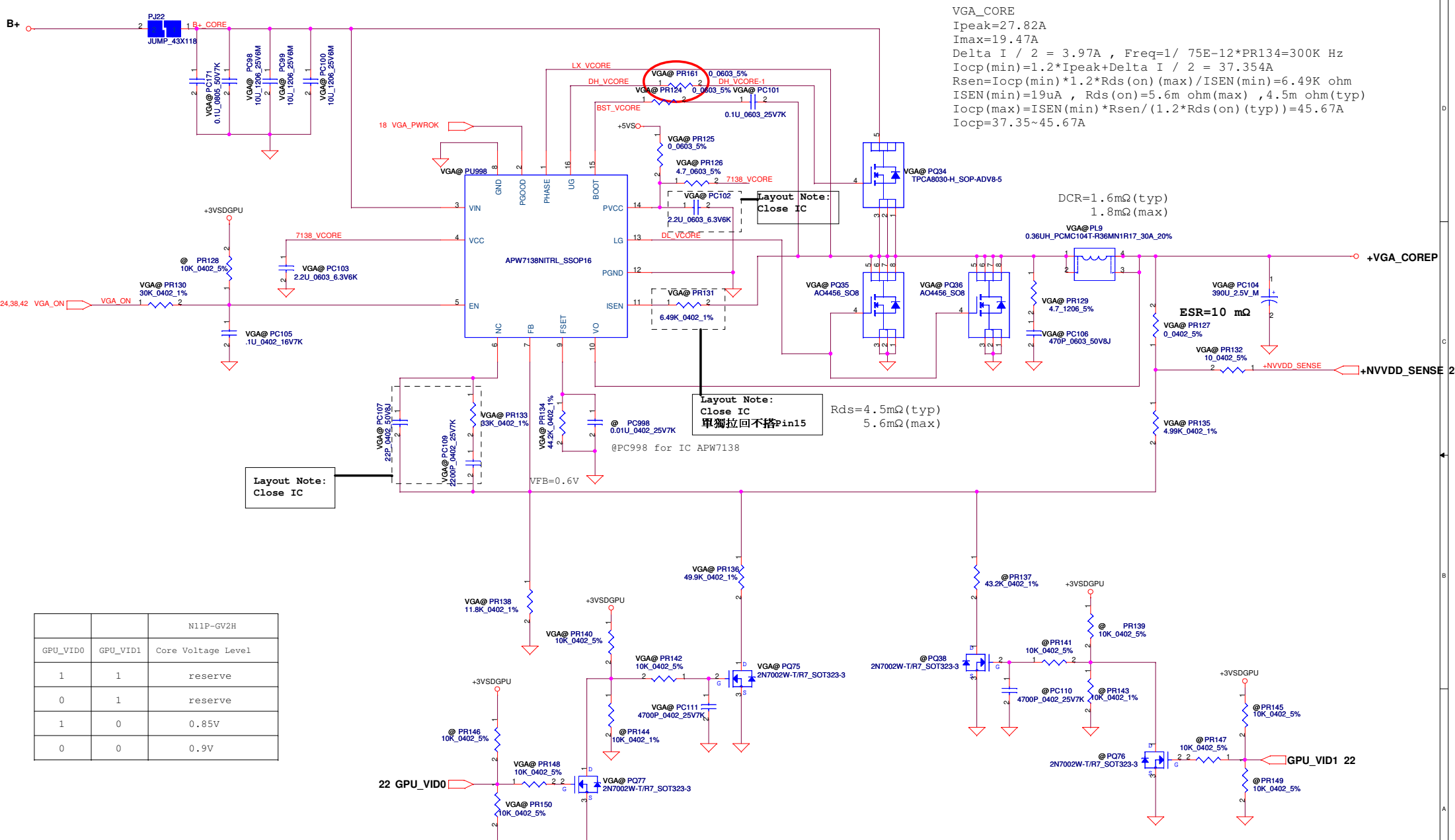
Because +1.5VSP has 17.74A power budget, it includes DDR3, VGA chip, VRAM, so must use molding choke.



R<sub>ds</sub> = 4.5mΩ (Typ)  
 5.6mΩ (Max)

VFB=0.75V  
 Vo=VFB\*(1+PR418/PR419)=1.52V  
 Freq=282KHz(min) , 300KHz(typ)  
 C<sub>esr</sub>=15m ohm  
 I<sub>peak</sub>=13.61A  
 I<sub>ocpmin</sub>=18.98A  
 $\Delta I = ((19-1.5) * (1.5/19)) / (L * Freq) = 4.899A$   
 $1/2 \Delta I = 2.449A$   
 I<sub>ocp</sub> = 18.09A ~ 29.13A

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Custom		0.1		Date: Tuesday, December 22, 2009   Sheet 49 of 56	



VGA\_CORE  
 Ipeak=27.82A  
 Imax=19.47A  
 $\Delta I / 2 = 3.97A$  , Freq=1/75E-12\*PR134=300K Hz  
 $I_{ocp}(min)=1.2 * I_{peak} + \Delta I / 2 = 37.354A$   
 $R_{sen}=I_{ocp}(min) * 1.2 * R_{ds}(on)(max) / I_{SEN}(min)=6.49K \text{ ohm}$   
 $I_{ocp}(max)=I_{SEN}(min) * R_{sen} / (1.2 * R_{ds}(on)(typ))=45.67A$   
 $I_{ocp}=37.35 \sim 45.67A$

DCR=1.6mΩ (typ)  
 1.8mΩ (max)

VGA@PL9  
 0.36UH\_PCMC104T-R36MN1R17\_30A\_20%

ESR=10 mΩ

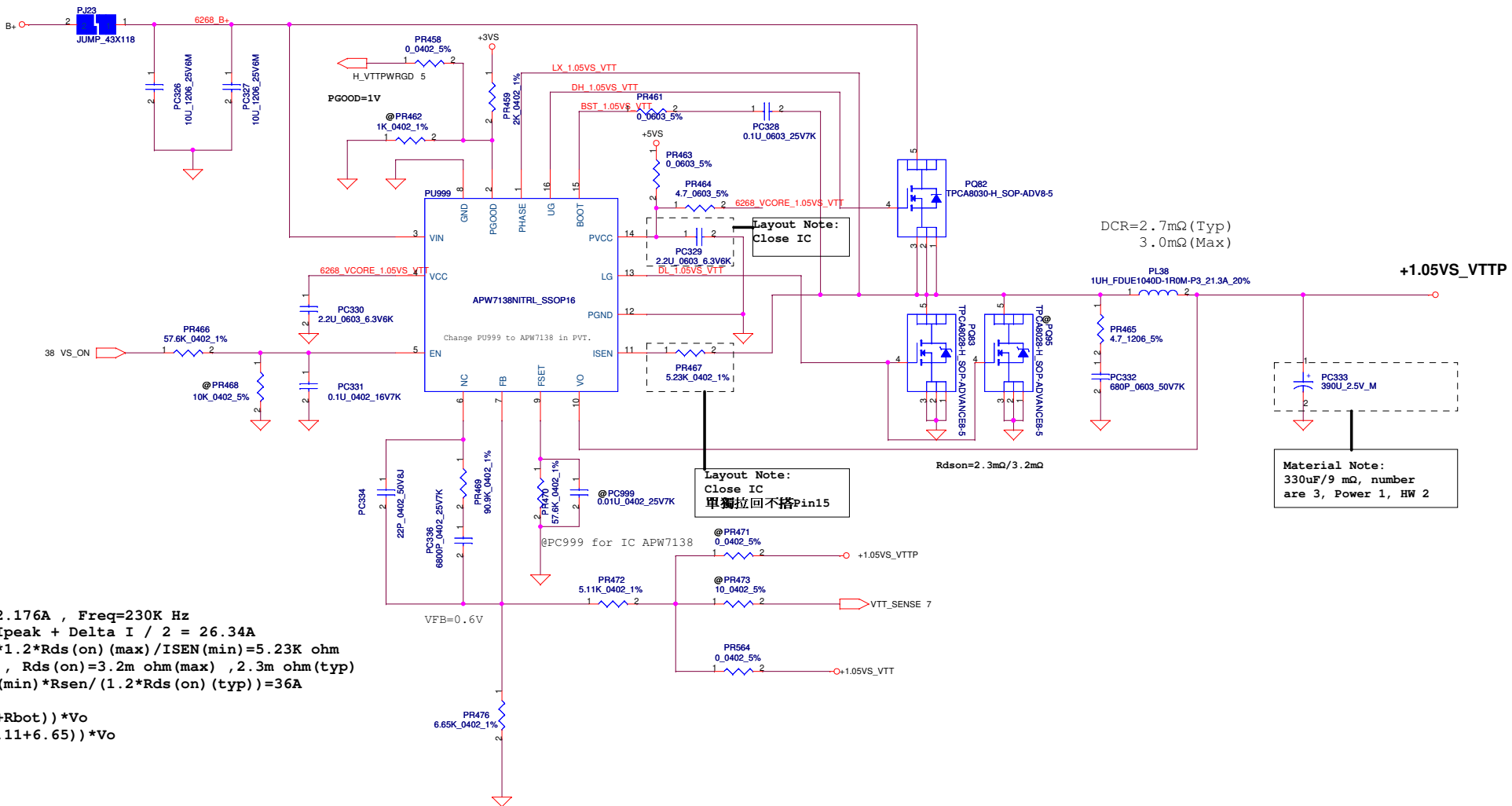
Rds=4.5mΩ (typ)  
 5.6mΩ (max)

Layout Note:  
 Close IC

Layout Note:  
 Close IC  
 單獨拉回不搭Pin15

GPU_VID0	GPU_VID1	Core Voltage Level
1	1	reserve
0	1	reserve
1	0	0.85V
0	0	0.9V

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Issued Date	2009/08/25	Deciphered Date	2010/08/25	VGA COREP	
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**+1.05VS\_VTTP**  
**Ipeak=20.14A**  
**I<sub>max</sub>=14.10A**  
**Delta I / 2 = 2.176A , Freq=230K Hz**  
**I<sub>ocp</sub>(min)=1.2\*I<sub>peak</sub> + Delta I / 2 = 26.34A**  
**R<sub>sen</sub>=I<sub>ocp</sub>(min) \* 1.2 \* R<sub>ds</sub>(on) / I<sub>SEN</sub>(min) = 5.23K ohm**  
**I<sub>SEN</sub>(min)=19uA , R<sub>ds</sub>(on)=3.2m ohm(max) , 2.3m ohm(typ)**  
**I<sub>ocp</sub>(max)=I<sub>SEN</sub>(min) \* R<sub>sen</sub> / (1.2 \* R<sub>ds</sub>(on) (typ)) = 36A**  
**I<sub>ocp</sub>=26.34~36A**  
**V<sub>ref</sub>=(R<sub>b</sub> / (R<sub>top</sub>+R<sub>bot</sub>)) \* V<sub>o</sub>**  
**=>0.6=(6.65 / (5.11+6.65)) \* V<sub>o</sub>**  
**V<sub>o</sub>=1.061V**

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	For BOM unique.	For BOM unique.	0.1	46	Change PD8 from SC1SS355003(S DIO 1SS355) to SC100001K00( DIO 1SS355 SOD323 T/R-5K)	2009-1021	to DVT
2	For BOM unique.	For BOM unique.	0.1	54	Delete PQ86/PQ91 SB00000HL00(S TR TPCA8030-H 1N SOP). Add PQ87/PQ90 SB00000HL00(S TR TPCA8030-H 1N SOP).	2009-1021	to DVT
3	For UMA Arrandale CPU commond design.	For UMA Arrandale CPU, we just only pop 1 HS MOS and 1 LS MOS.	0.1	54	Delete PQ89/PQ93 SB00000GL00(S TR TPCA8028-H 1N SOP)	2009-1021	to DVT
4	For VTT Power rail commond design.	For VTT Power rail commond design, we pop 1 HS MOS and 1LS MOS.	0.1	52	Delete PQ95 SB00000GL00(S TR TPCA8028-H 1N SOP)	2009-1021	to DVT
5	CIS link error.	CIS link error.	0.1	54	Change PR500 from SD028100A00(S RES 1/16W 10 +-5% 0402) to SD028100A80(S RES 1/16W 10 +-5% 0402)	2009-1021	to DVT
6	BOM unique.	BOM unique.	0.1	47	Chnage PC265 from SE107475M80(S CER CAP 4.7U 6.3V M X5R 0603 to SE107475K80(S CER CAP 4.7U 6.3V K X5R 0603)	2009-1021	to DVT
7	BOM unique.	BOM unique.	0.1	49	Chnage PC284 from SE107475M80(S CER CAP 4.7U 6.3V M X5R 0603 to SE107475K80(S CER CAP 4.7U 6.3V K X5R 0603)	2009-1021	to DVT
8	BOM unique.	BOM unique.	0.1	54	Chnage PC350 from SE107475M80(S CER CAP 4.7U 6.3V M X5R 0603 to SE107475K80(S CER CAP 4.7U 6.3V K X5R 0603)	2009-1021	to DVT
9	BOM unique.(For Madison/Park SKU)	BOM unique.(For Madison/Park SKU)	0.1	52	Chnage PC367 from SE107475M80(S CER CAP 4.7U 6.3V M X5R 0603 to SE107475K80(S CER CAP 4.7U 6.3V K X5R 0603)	2009-1021	to DVT
10	BOM unique.	BOM unique.	0.1	46	Change PC225/PC227 from SE153106K80(S CER CAP 10U 25V K X6S 1206) to SE142106M80 (S CER CAP 10U 25V M X5R 1206)	2009-1021	to DVT
11	BOM unique.	BOM unique.	0.1	54	Change PC339/PC341 from SE153106K80(S CER CAP 10U 25V K X6S 1206) to SE142106M80 (S CER CAP 10U 25V M X5R 1206) Change PC354/PC355 from SE153106K80(S CER CAP 10U 25V K X6S 1206) to SE142106M80 (S CER CAP 10U 25V M X5R 1206)	2009-1021	to DVT
12	+1.05VS_VTTP Cost down 1 LS MOS. HW request.	+1.05VS_VTTP Cost down 1 LS MOS. Because +1.05VS_VTT has voltage drop issue, HW request, remote sense to close to PCH.	0.2	52	Delete PQ95 SB00000GL00(S TR TPCA8028-H 1N SOP ) Delete PR471 SD028000080(S RES 0 0402 5%) Delete PR473 from SD034100A80(S RES 10 0402 5%) Add PR564 SD028000080(S RES 1/16W 0 0402 5%)	2009-1029	to DVT
13	Adjust +1.05VS_VTTP OCP.	Because we remove a LS MOS, so OCP must adjust.	0.2	52	Change PR467 from SD000004080(S RES 1/16W 2.2K +-1% 0402) to SD034499180(S RES 1/16W 4.99K 0402 1%)	2009-1029	to DVT
14	+1.8VSP2, Using MP2121 for 1.8V only.	No need to use LDO for +1.8V. Delete all PU19 circiut.	0.2	49	Delete PU19 SA00001NC00 (S IC APL5913-KAC-TRL SO 8P)	2009-1029	to DVT
15	+1.8VSP2, Using MP2121 for 1.8V only.	No need to use LDO for +1.8V. Delete all PU19 circiut.	0.2	49	Delete PR402 SD034150280, PR404 SD034120280.	2009-1029	to DVT
16	+1.8VSP2, Using MP2121 for 1.8V only.	No need to use LDO for +1.8V. Delete all PU19 circiut.	0.2	49	Delete PC273 SE075103K80 PC275 SE000000I10 Delete PC272 SE107475K80, PC271 SE107105M80	2009-1029	to DVT
17	+VGA_COREP, efficiency issue.	Increase Freq, decrease choke, to improve efficiency.	0.2	51	Delete PR401 and PR403 SD028220280, PC274 SE026474K80 Change PR196 from SD034442280 to SD034365280.	2009-1029	to DVT
18	+VGA_COREP, OVP issue.	Becasue if PR199/PR202 pop 0ohm, it will cause OVP when VID change from 00 to 11)	0.2	51	Change PL14 from SL200000V00 to SH000005680 Change PR199/PR202 from SD028000080 to SD028100280 (S RES 1/16W 10K 0402 5%)	2009-1029	to DVT
19	+VGA_COREP, cost issue.	Cost down.	0.2	51	Change PQ75/PQ78 from SB00000GL00(S TR TPCA8028-H 1N SOP) to SB000009F80(S TR AO4456 1N S08)	2009-1029	to DVT
20	+VGA_COREP, satndard design.	+VGA_COREP, satndard design, pop 1HS MOS and 2LS MOS, so remove one HS MOS PQ79.	0.2	51	Delete PQ79 SB000008L80 (S TR SI7866DP-T1-E3 1N POWERPAK S08 )	2009-1029	to DVT
21	+GFX_COREP, spike issue.	Because +GFX_COREP has spike voltage issue, add schottky diode across GFXVR_EN and VS_ON to solve it.	0.2	51	Add PD17 SCS00000200 (S SCH DIO RB751V-40 SOD-323 )	2009-1029	to DVT
22	+VGA_COREP, OCP caaculation erroe issue.	Because VGA_CORE has 2 LS MOS, APW7138 detect LS Rdson, so when caculate OCP, Rdson must reduce 1/2.	0.2	51	Change PR190 from SD034649180 to SD034511180 (S RES 1/16W 5.11K 0402 1%)	2009-1029	to DVT

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PCB

ZZZ



LA-5893P REV0 M/B

ZZZ1



X76198BOL21

ALT. GROUP PARTS 1G SAM

ZZZ2



X76198BOL22

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