

# Compal Confidential

## PAWF5/F6 M/B Schematics Document

### Intel Penryn Processor with Cantiga + DDRIII + ICH9M

2010-02-03

REV: 0.1

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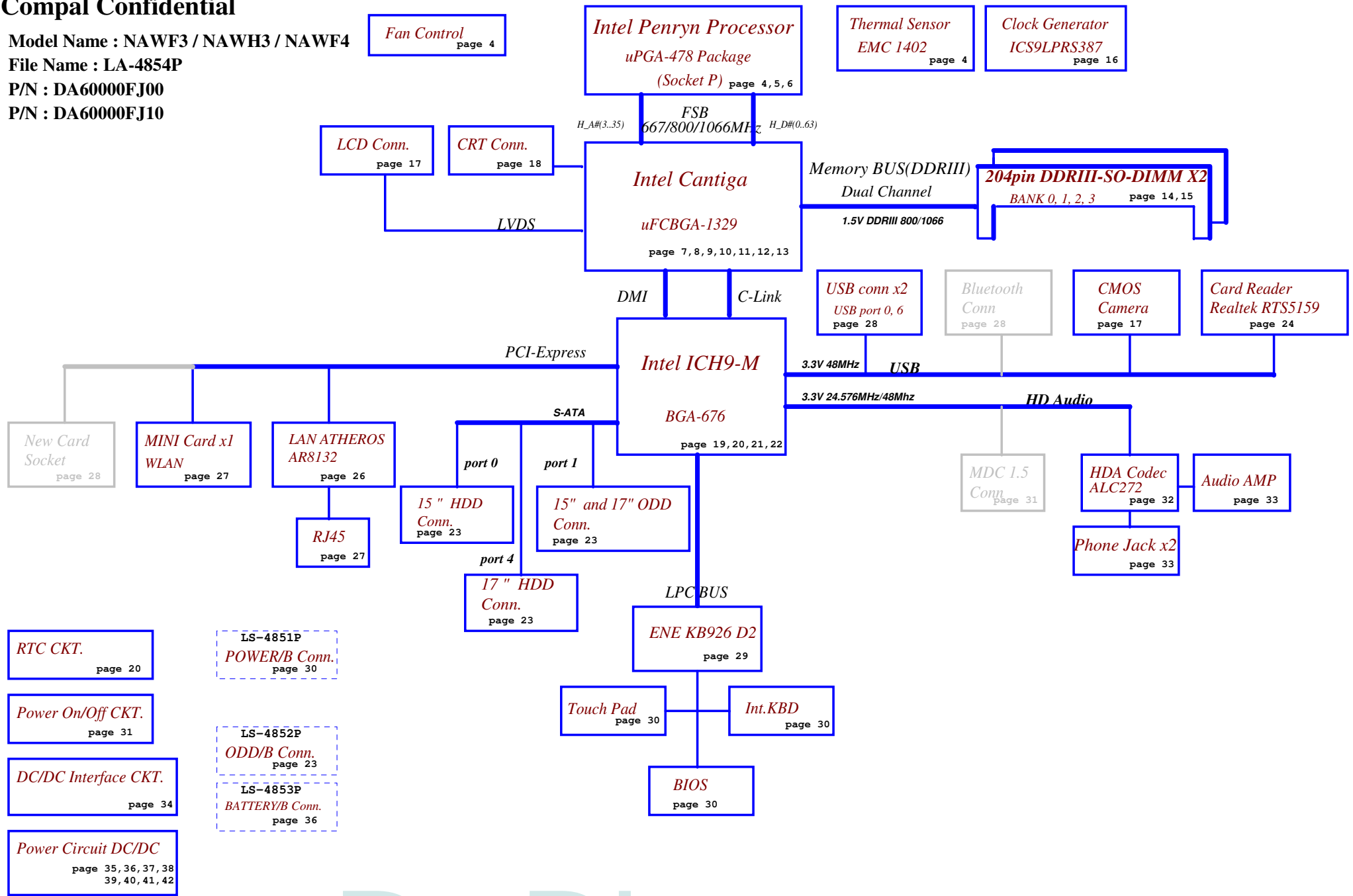
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Model Name : NAWF3 / NAWH3 / NAWF4

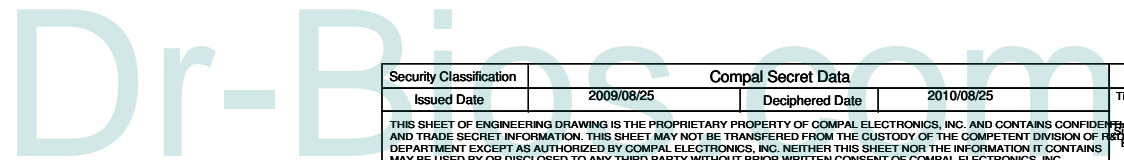
File Name : LA-4854P

P/N : DA60000FJ00

P/N : DA60000FJ10



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## Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.75VS	0.75V power rail for DDR	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for DDR	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for LVDS	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail for SB	ON	ON	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

## External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

## EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADI ADT7421	1001 100X b
EEPROM(24C16/02)	1010 000X b		
GMT G781-1	1001 101X b		

## EC SM Bus2 address

## ICH9M SM Bus address

Device	Address
Clock Generator (ICS9LPRS387, SLG8SP556V)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

## Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0		0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

## BOARD ID Table

Board ID	PCB Revision
0	
1	
2	
3	
4	
5	0.1 (PVT)
6	
7	

## BTO Option Table

BTO Item	BOM Structure
GM45	GM@
GL40	GL@
PAWF5	F5@
PAWF7	F7@
8114	8114@
8132	8132@

## PCIE table

PCIE port1	Express Card(Reserved)
PCIE port2	Wireless Card
PCIE port3	PCIE LAN
PCIE port4	
PCIE port5	
PCIE port6	

## USB table

	UHCI1	Port0	MB USB Conn.
EHCI1	UHCI2	Port1	
		Port2	
		Port3	CMOS Camera
EHCI2	UHCI3	Port4	Card Reader
		Port5	New Card(Reserved)
		Port6	MB USB Conn.
		Port7	
		Port8	Blue Tooth
EHCI2	UHCI5	Port9	
		Port10	Wireless Card
		Port11	

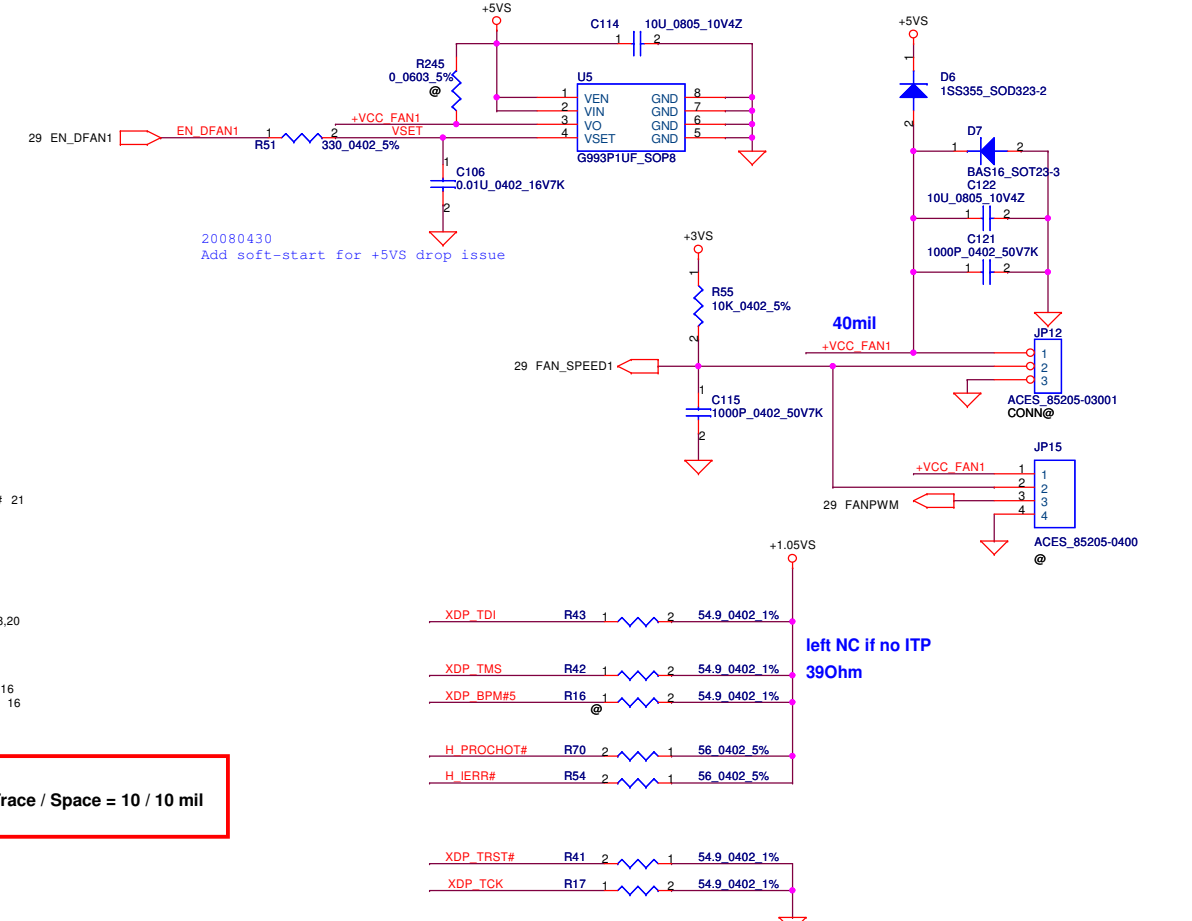
## SATA table

SATA port0	HDD
SATA port1	ODD
SATA port2	
SATA port3	
SATA port4	for 17" 2nd HDD
SATA port5	

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- 7 H\_A#[3..35]  $\rightarrow$  H\_A#[3..35]
- 7 H\_REQ#[0..4]  $\rightarrow$  H\_REQ#[0..4]
- 7 H\_RS#[0..2]  $\rightarrow$  H\_RS#[0..2]

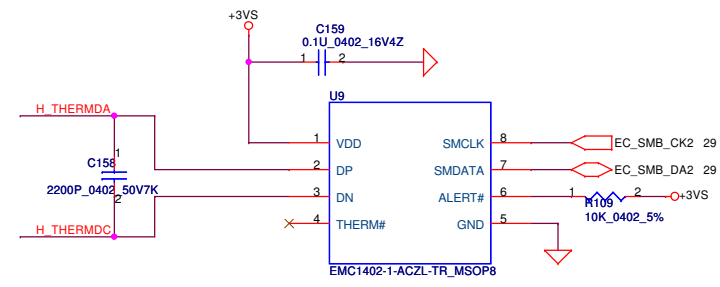
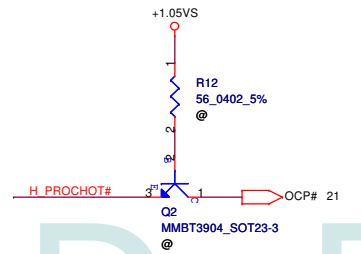
### FAN1 Conn

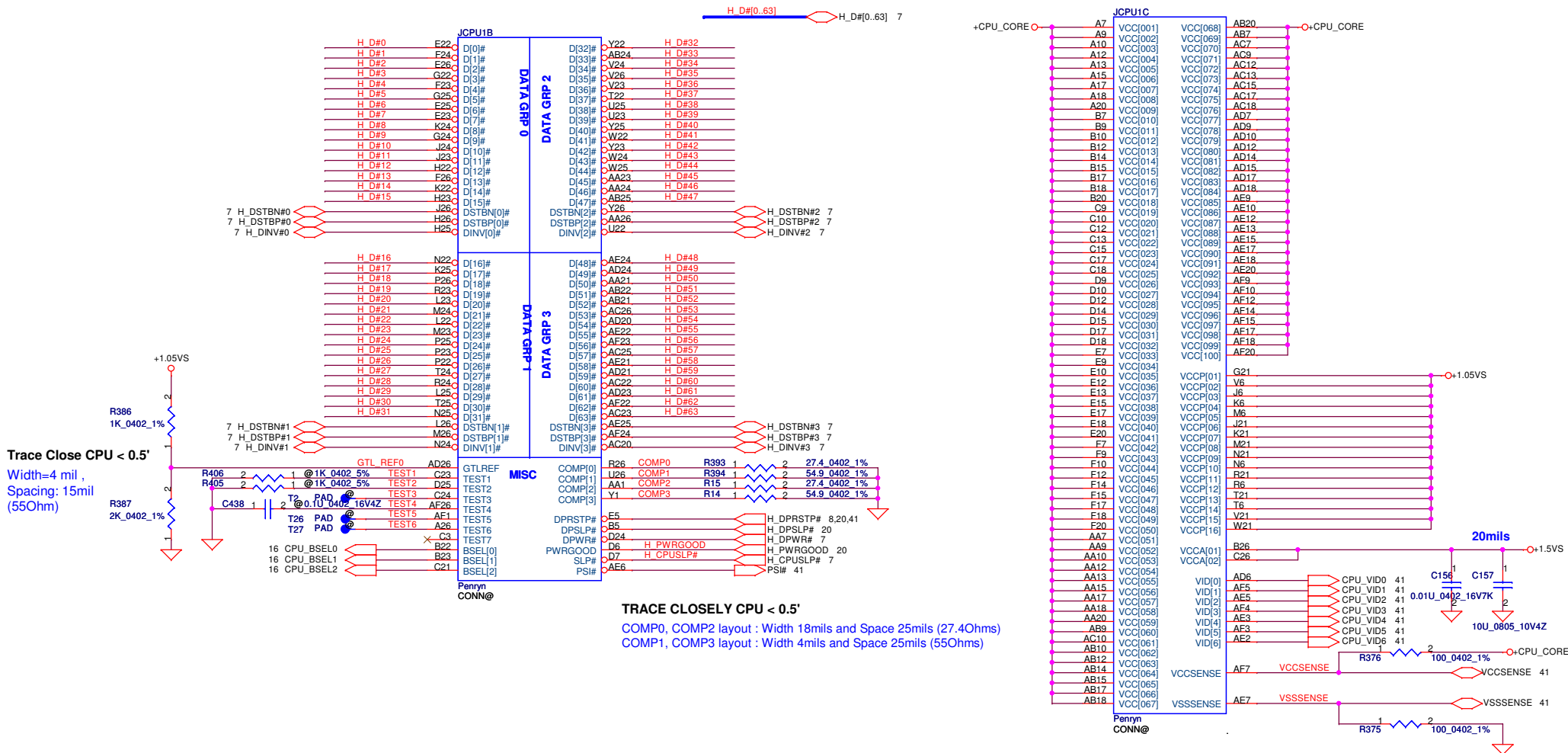


20080430  
Add soft-start for +5VS drop issue

**Layout Note:**  
H\_THERMDA&H\_THERMDC Trace / Space = 10 / 10 mil

BSEL2	BSEL1	BSEL0	BCLK
0	0	0	266
0	1	0	200
0	1	1	166

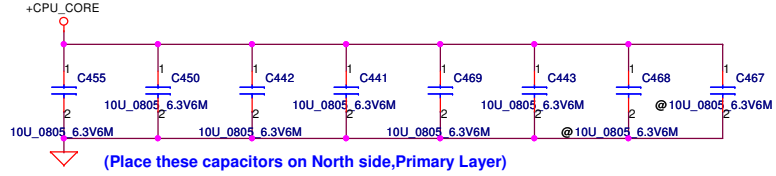
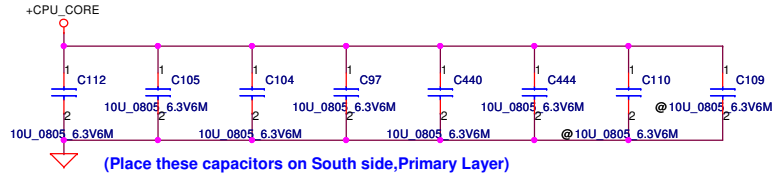
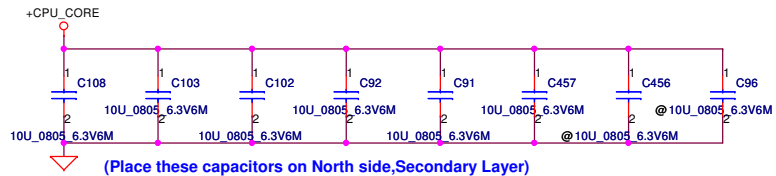
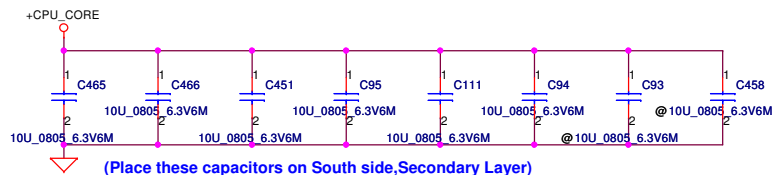
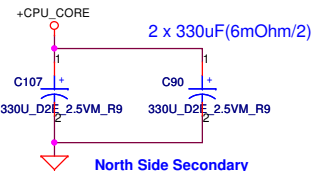
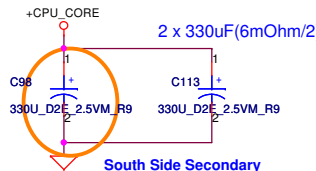




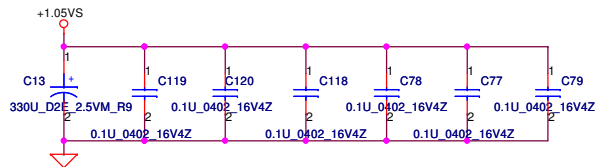
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JCPUID		
A4	VSSJ001	VSSJ082
A8	VSSJ002	VSSJ083
A11	VSSJ003	VSSJ084
A14	VSSJ004	VSSJ085
A16	VSSJ005	VSSJ086
A19	VSSJ006	VSSJ087
A23	VSSJ007	VSSJ088
AF2	VSSJ008	VSSJ089
B6	VSSJ009	VSSJ090
B8	VSSJ010	VSSJ091
B11	VSSJ011	VSSJ092
B13	VSSJ012	VSSJ093
B16	VSSJ013	VSSJ094
B19	VSSJ014	VSSJ095
B21	VSSJ015	VSSJ096
B24	VSSJ016	VSSJ097
C5	VSSJ017	VSSJ098
C8	VSSJ018	VSSJ099
C11	VSSJ019	VSSJ100
C14	VSSJ020	VSSJ101
C16	VSSJ021	VSSJ102
C19	VSSJ022	VSSJ103
C2	VSSJ023	VSSJ104
C22	VSSJ024	VSSJ105
C25	VSSJ025	VSSJ106
D1	VSSJ026	VSSJ107
D4	VSSJ027	VSSJ108
D8	VSSJ028	VSSJ109
D11	VSSJ029	VSSJ110
D13	VSSJ030	VSSJ111
D16	VSSJ031	VSSJ112
D19	VSSJ032	VSSJ113
D23	VSSJ033	VSSJ114
D26	VSSJ034	VSSJ115
E3	VSSJ035	VSSJ116
E6	VSSJ036	VSSJ117
E8	VSSJ037	VSSJ118
E11	VSSJ038	VSSJ119
E14	VSSJ039	VSSJ120
E16	VSSJ040	VSSJ121
E19	VSSJ041	VSSJ122
E21	VSSJ042	VSSJ123
E24	VSSJ043	VSSJ124
F5	VSSJ044	VSSJ125
F8	VSSJ045	VSSJ126
F11	VSSJ046	VSSJ127
F13	VSSJ047	VSSJ128
F16	VSSJ048	VSSJ129
F19	VSSJ049	VSSJ130
F2	VSSJ050	VSSJ131
F22	VSSJ051	VSSJ132
F25	VSSJ052	VSSJ133
G4	VSSJ053	VSSJ134
G1	VSSJ054	VSSJ135
G23	VSSJ055	VSSJ136
G26	VSSJ056	VSSJ137
H3	VSSJ057	VSSJ138
H6	VSSJ058	VSSJ139
H21	VSSJ059	VSSJ140
H24	VSSJ060	VSSJ141
J2	VSSJ061	VSSJ142
J22	VSSJ062	VSSJ143
J25	VSSJ063	VSSJ144
J25	VSSJ064	VSSJ145
K1	VSSJ065	VSSJ146
K4	VSSJ066	VSSJ147
K23	VSSJ067	VSSJ148
K26	VSSJ068	VSSJ149
L3	VSSJ069	VSSJ150
L6	VSSJ070	VSSJ151
L21	VSSJ071	VSSJ152
L24	VSSJ072	VSSJ153
M2	VSSJ073	VSSJ154
M5	VSSJ074	VSSJ155
M22	VSSJ075	VSSJ156
M25	VSSJ076	VSSJ157
N1	VSSJ077	VSSJ158
N4	VSSJ078	VSSJ159
N23	VSSJ079	VSSJ160
N26	VSSJ080	VSSJ161
P3	VSSJ081	VSSJ162
		VSSJ163
		AE1
		AE4
		AE8
		AE11
		AE14
		AE16
		AE19
		AE23
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		AF19
		AF21
		A25
		AE25

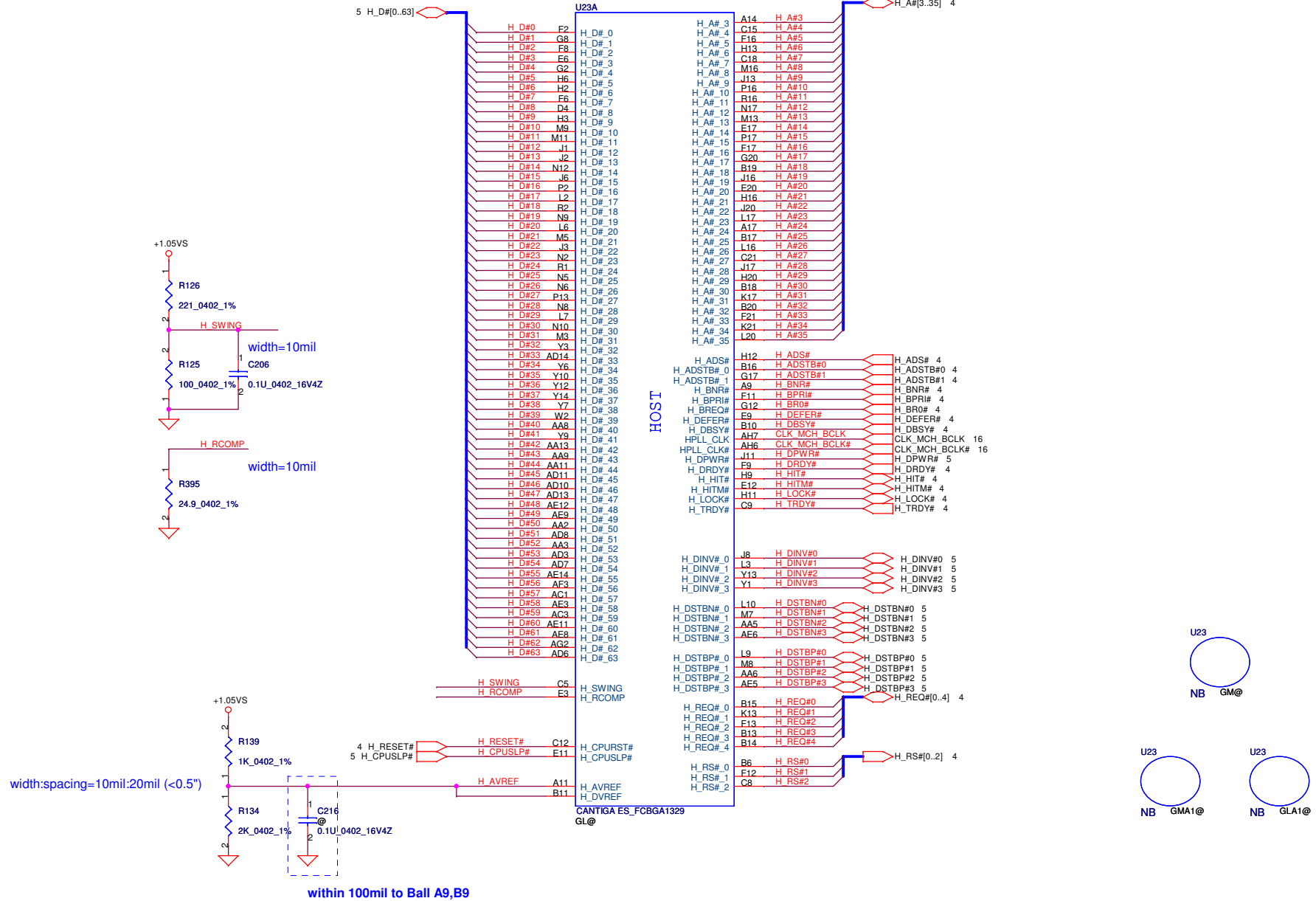
Penryn  
CONN@



+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP, Polymer	4X330uF	6m ohm/4	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32
	32X10uF	3m ohm/32	0.6nH/32



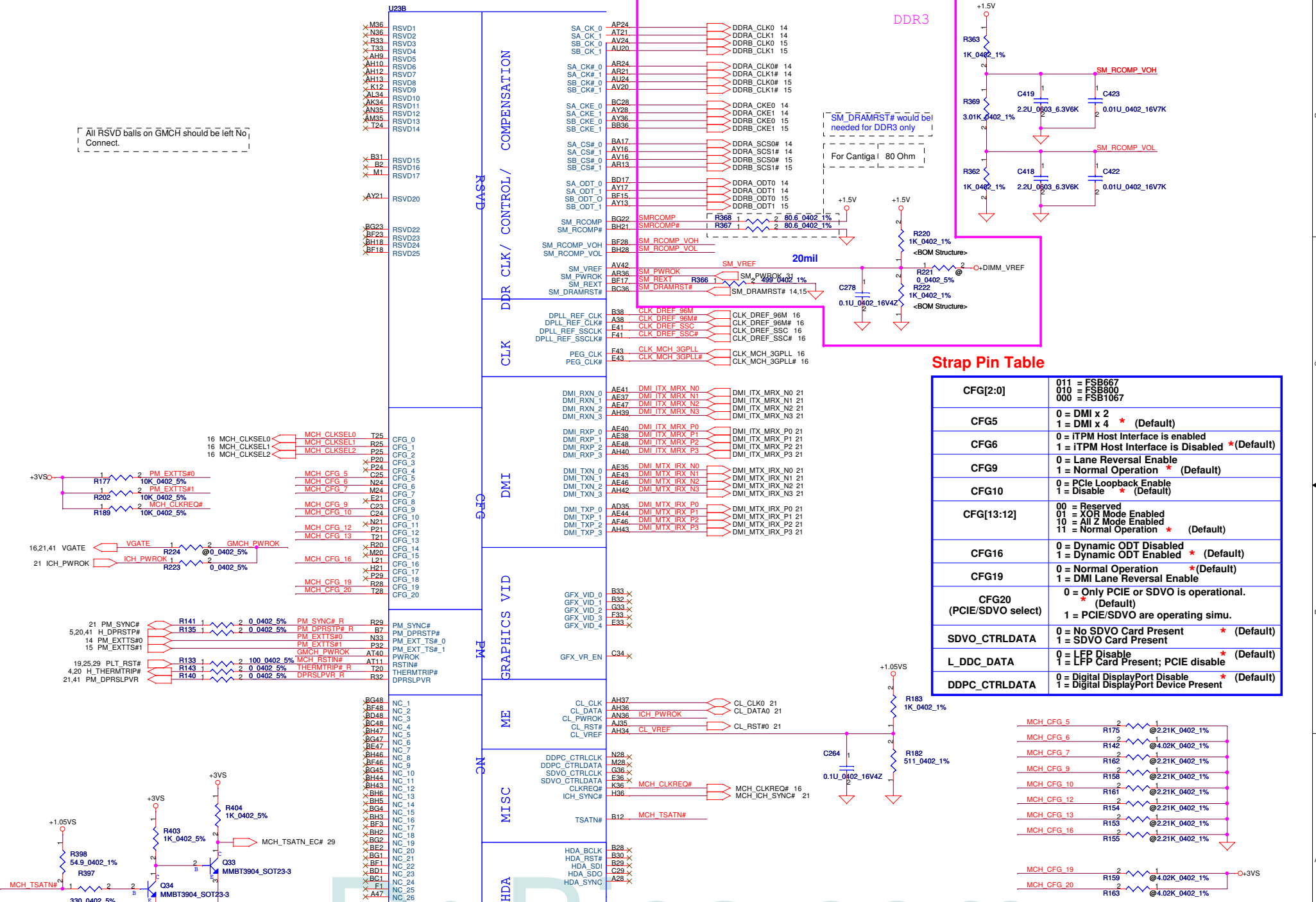
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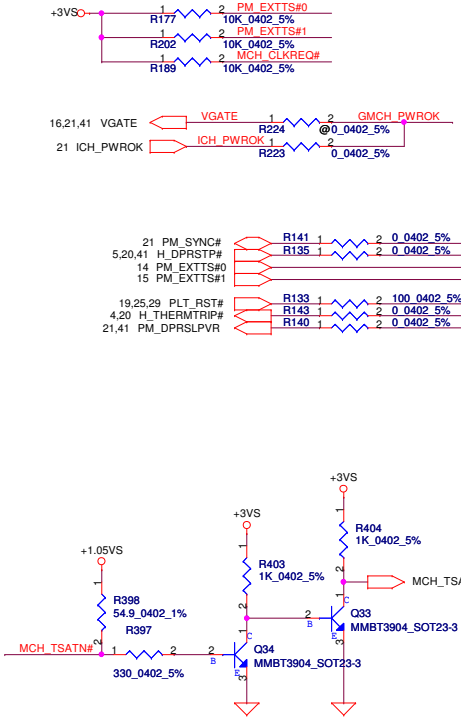
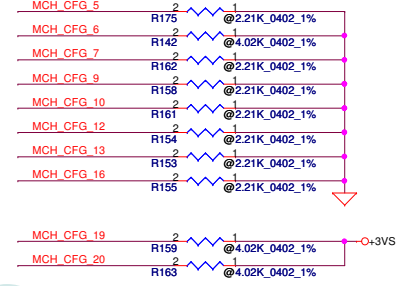
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All RSVD balls on GMCH should be left No Connect.



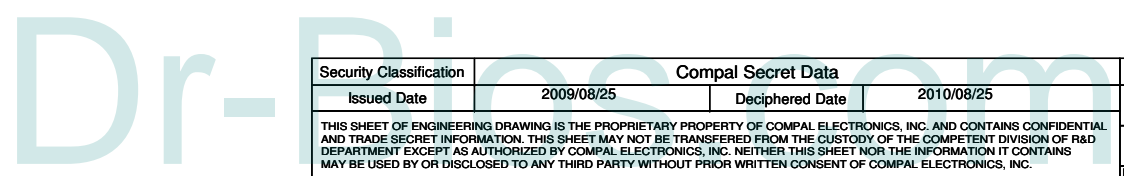
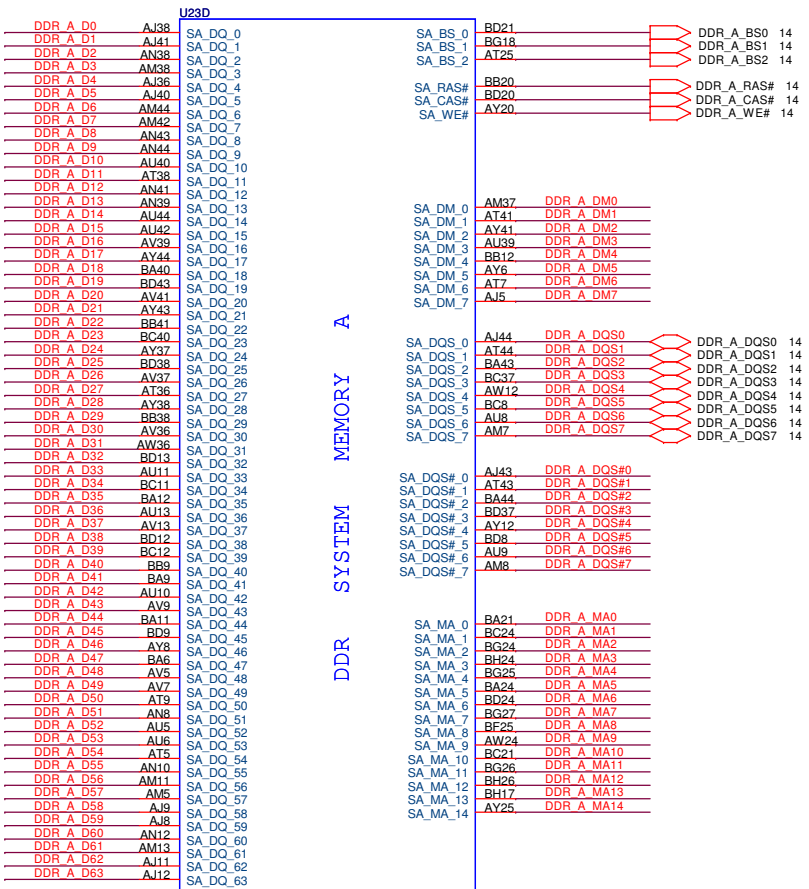
Strap Pin Table

CFG[2:0]	011 = FSB667 010 = FSB800 000 = FSB1067
CFG5	0 = DMI x 2 1 = DMI x 4 * (Default)
CFG6	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is Disabled * (Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation * (Default)
CFG10	0 = PCIe Loopback Enable 1 = Disable * (Default)
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation * (Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled * (Default)
CFG19	0 = Normal Operation * (Default) 1 = DMI Lane Reversal Enable
CFG20 (PCIe/SDVO select)	0 = Only PCIe or SDVO is operational. (Default) 1 = PCIe/SDVO are operating simu.
SDVO_CTRLDATA	0 = No SDVO Card Present * (Default) 1 = SDVO Card Present
L_DDC_DATA	0 = LFP Disable 1 = LFP Card Present; PCIe disable * (Default)
DDPC_CTRLDATA	0 = Digital DisplayPort Disable 1 = Digital DisplayPort Device Present * (Default)



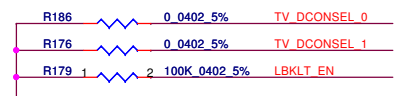
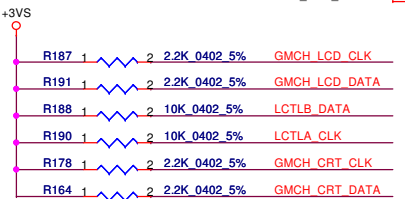
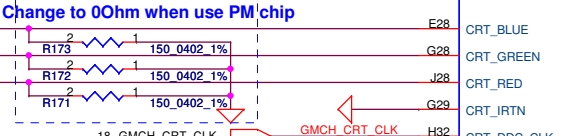
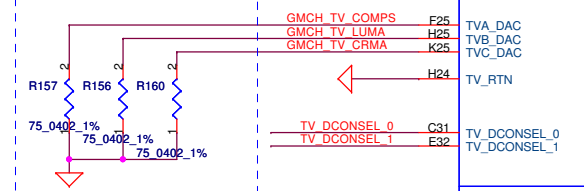
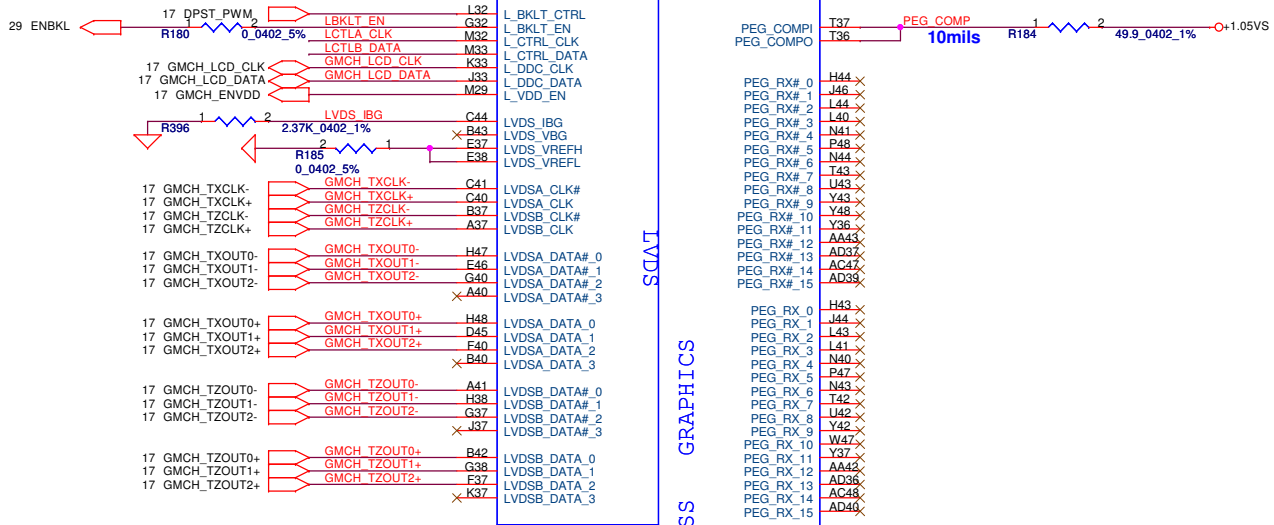
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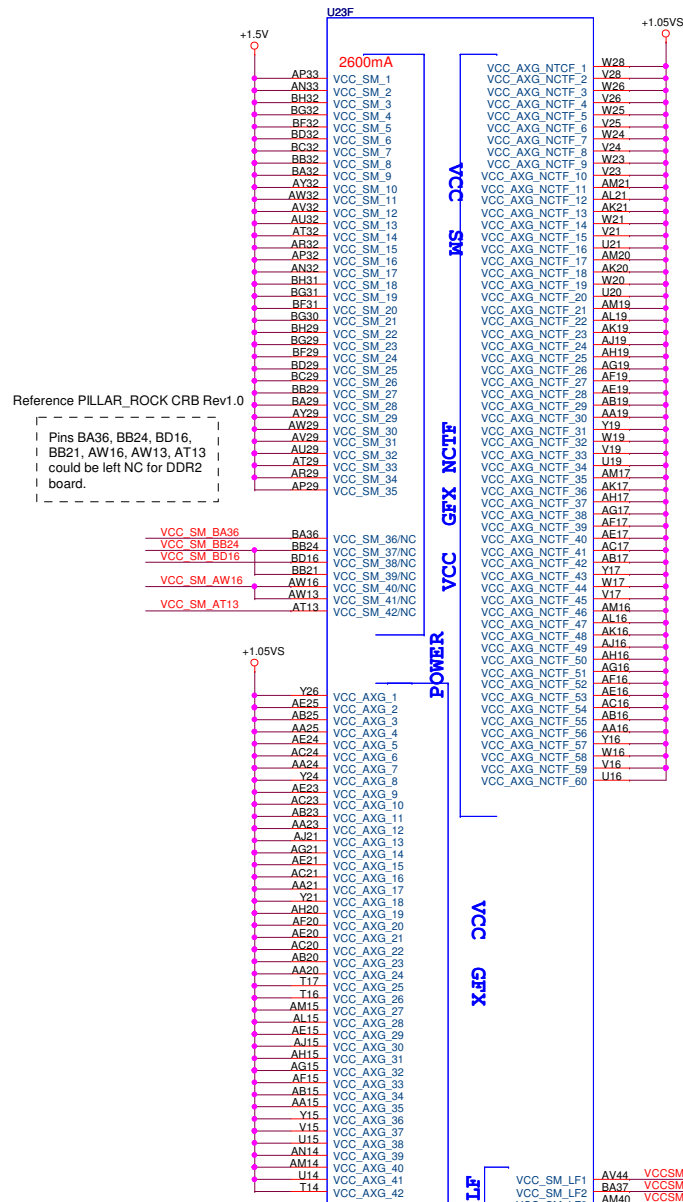
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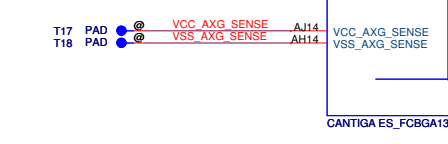
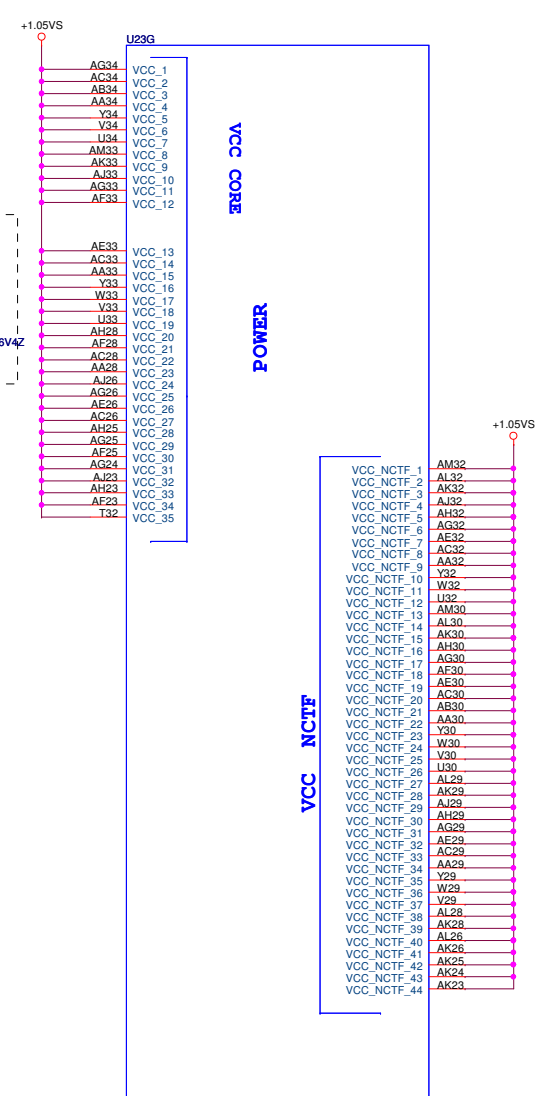
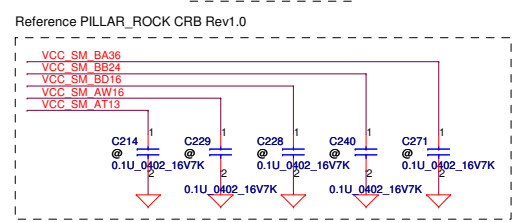
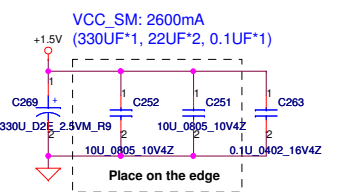
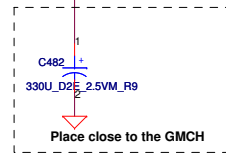
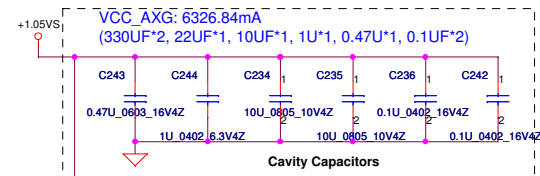
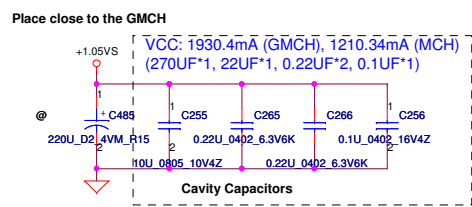


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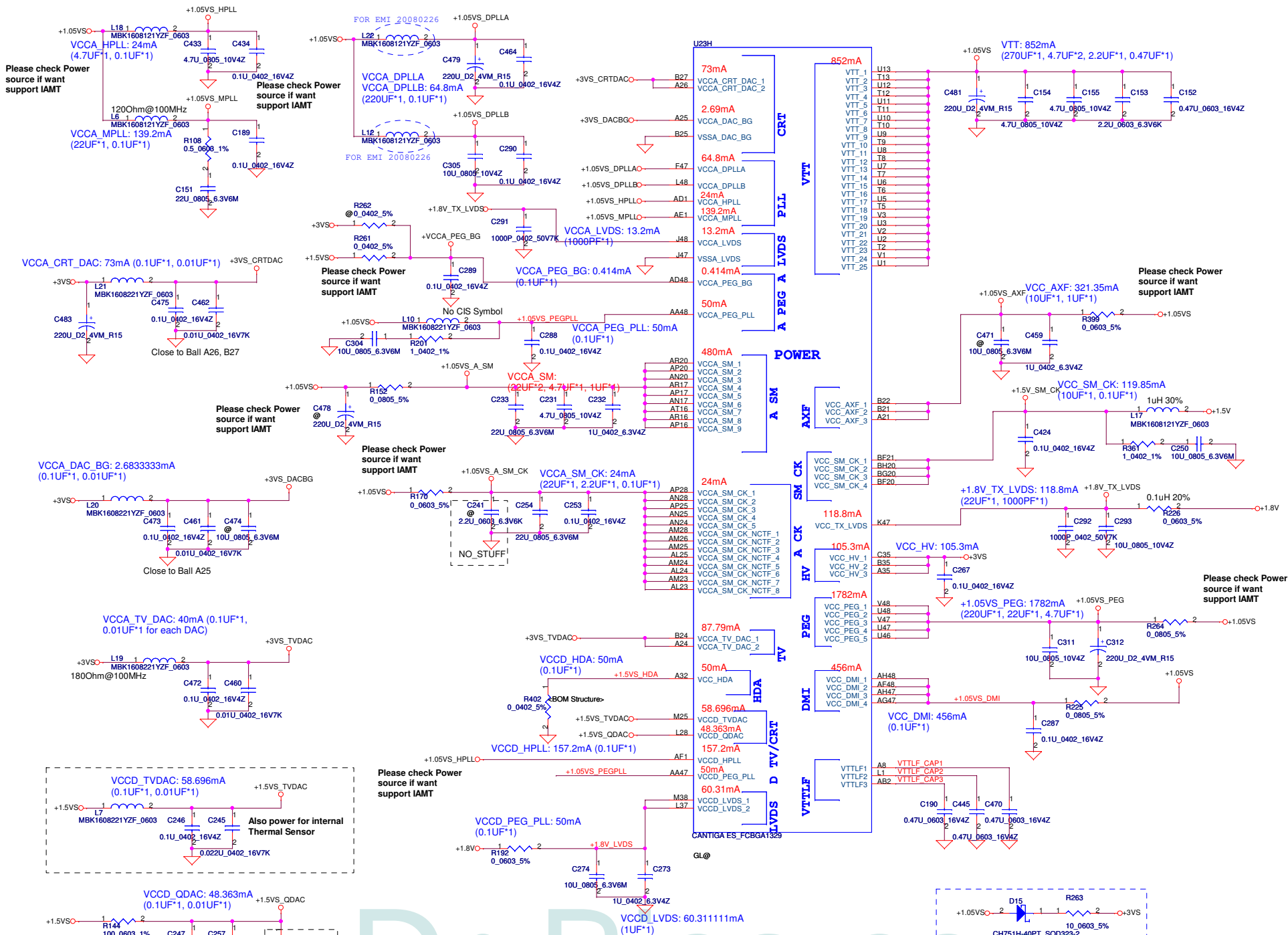
Compal Electronics, Inc.			
Title Cantiga GMCH(4/7)-VGA/LVDS/TV			
Size	Document Number	Rev	1.0
Custpm	NAWF3 M/B LA-4854P Schematic		
Date:	Wednesday, March 03, 2010	Sheet	10 of 45



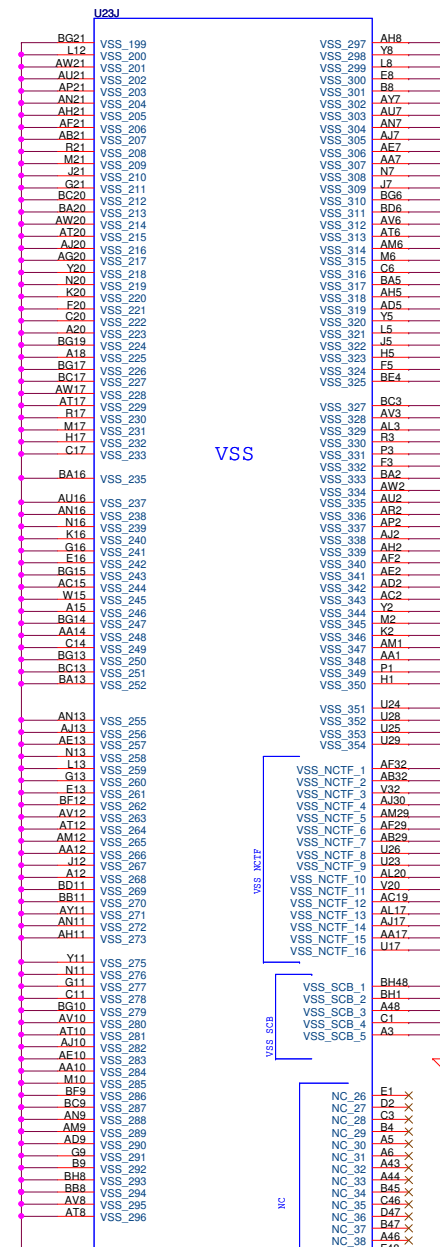
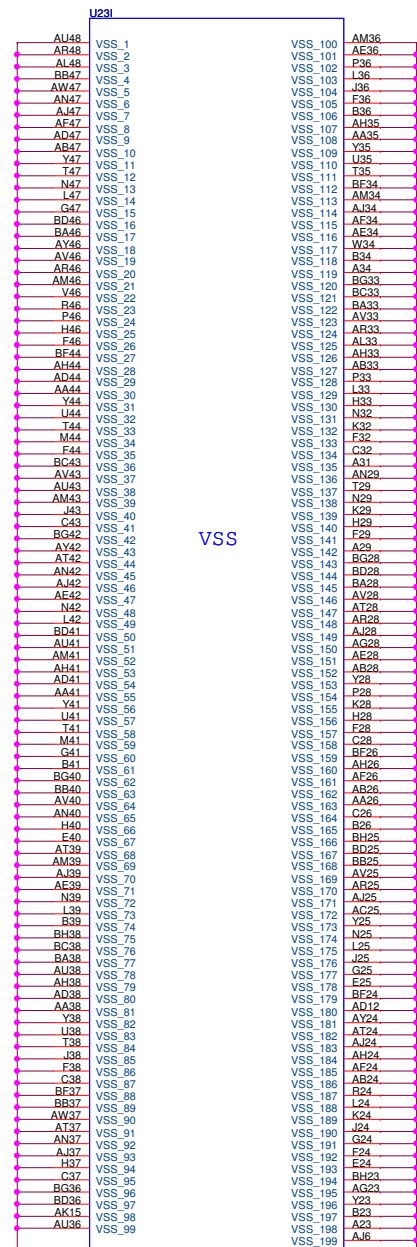
Reference PILLAR\_ROCK CRB Rev1.0  
Pins BA36, BB24, BD16, BB21, AW16, AW13, AT13 could be left NC for DDR2 board.



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Issued Date	2009/08/25	Deciphered Date	2010/08/25	Compal Electronics, Inc.
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NAWF3 M/B LA-4854P Schematic				Rev 1.0
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				Customer	NAWF3 M/B LA-4854P Schematic
Date	Wednesday, February 03, 2010	Sheet	12	Rev	1.0



CANTIGA ES\_FCBGA1329

CANTIGA ES\_FCBGA1329

GL@

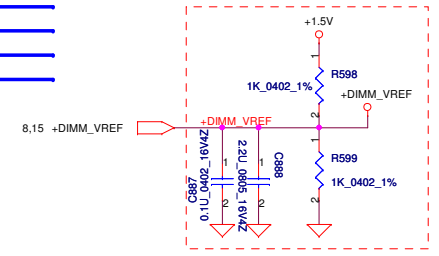
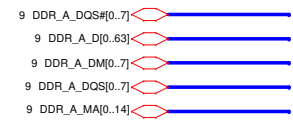
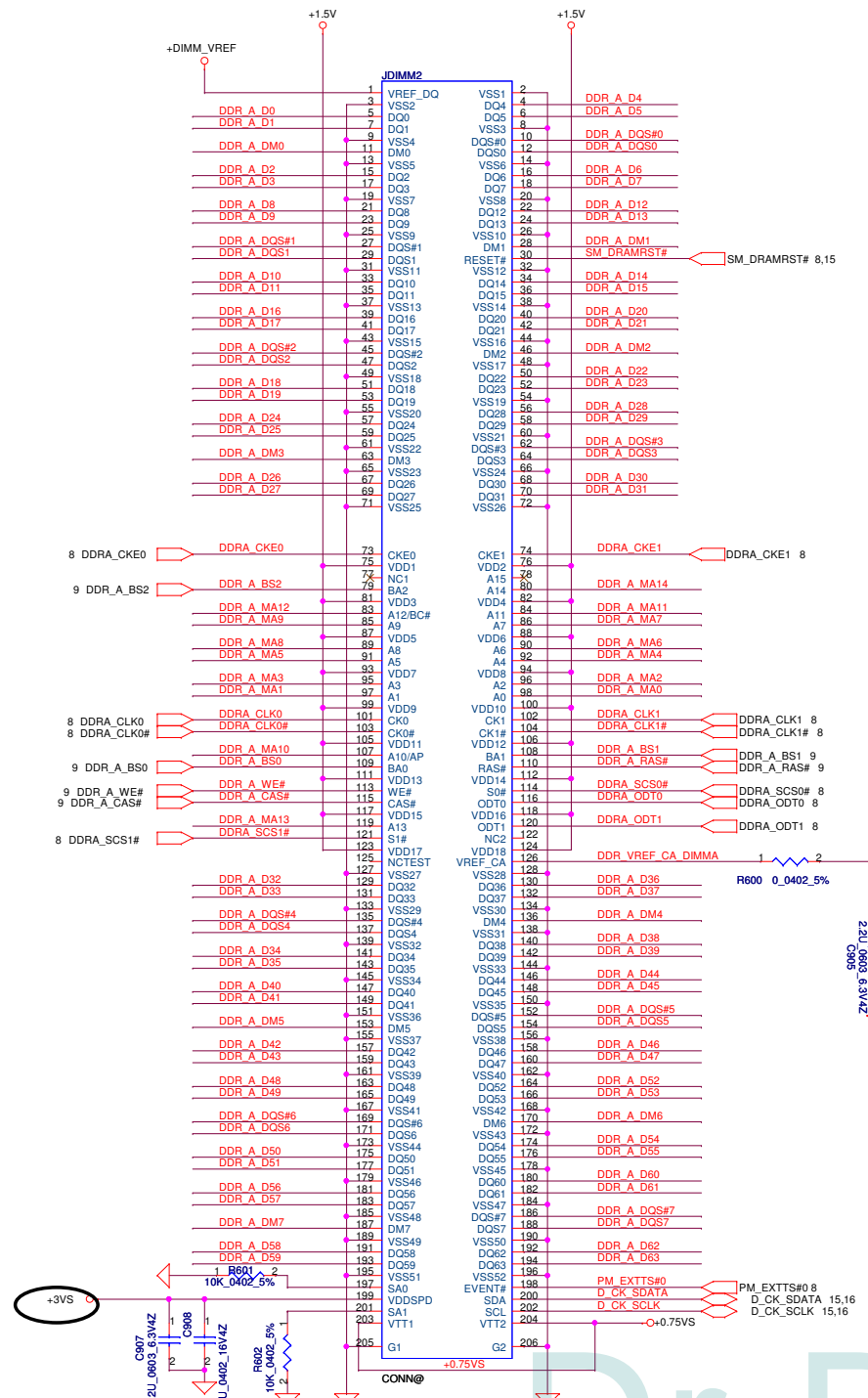
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Issued Date	2009/08/25	Deciphered Date
		2010/08/25

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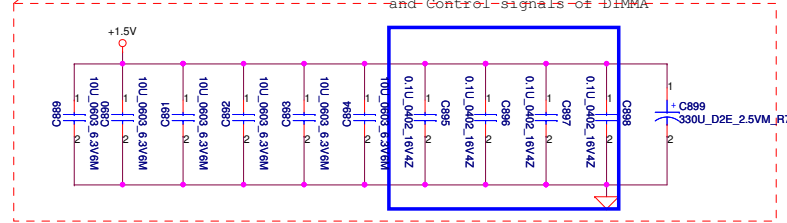
Compal Electronics, Inc.	
Title	Cantiga GMCH(1/7)-GTL
Document Number	NAWF3 M/B LA-4854P Schematic
Date	Wednesday, February 03, 2010
Sheet	13 of 45

Rev 1.0

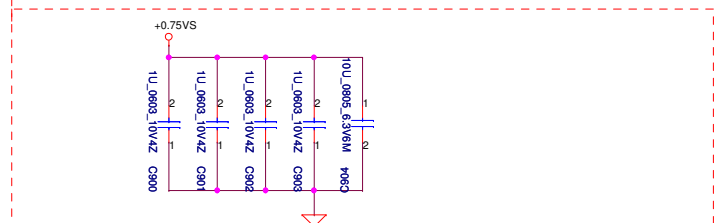


**Layout Note:**  
Place near JDIMM2

Layout Note: Place these 4 Caps near Command and Control signals of DIMM

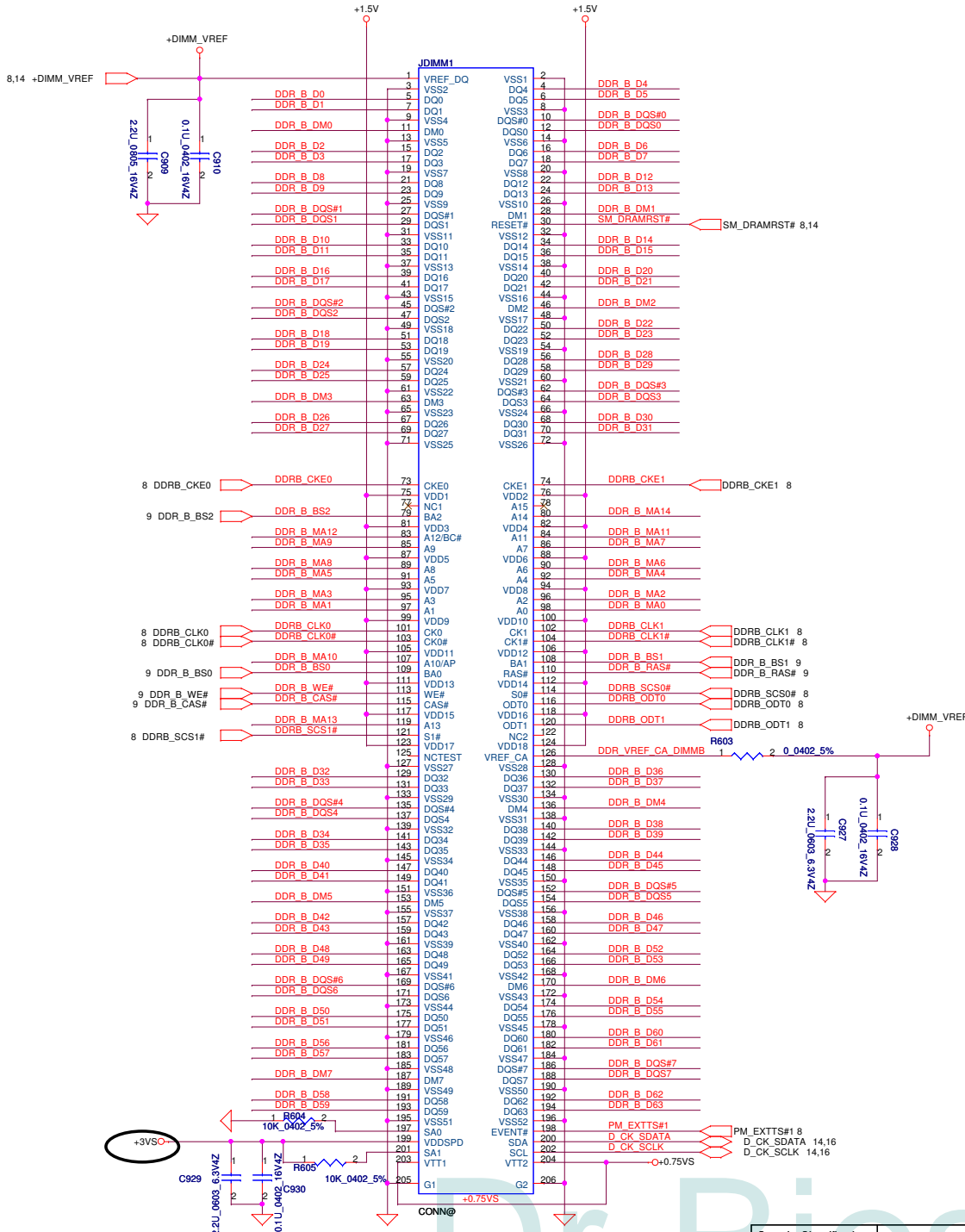


**Layout Note:**  
Place near JDIMM2.203 & JDIMM2.204

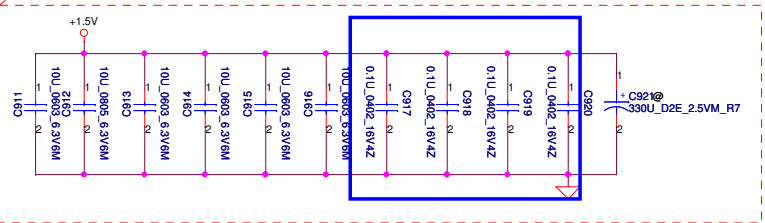


**DIMM0 REV H:5.2mm (BOT)**

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				NAWF3 M/B LA-4854P Schematic	
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				Sheet	14 of 45

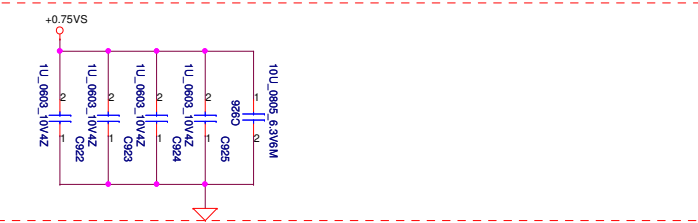


**Layout Note:**  
Place near JDIMM1



Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

**Layout Note:**  
Place near JDIMM1.203 & JDIMM1.204



DIMM1 REV H:9.2mm (BOT)

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Issued Date	2009/08/25	Deciphered Date
		2010/08/25

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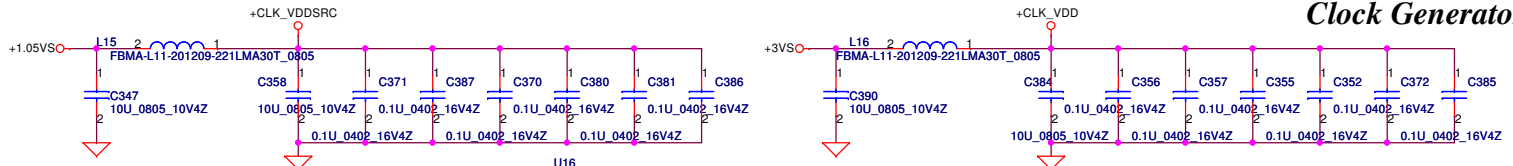
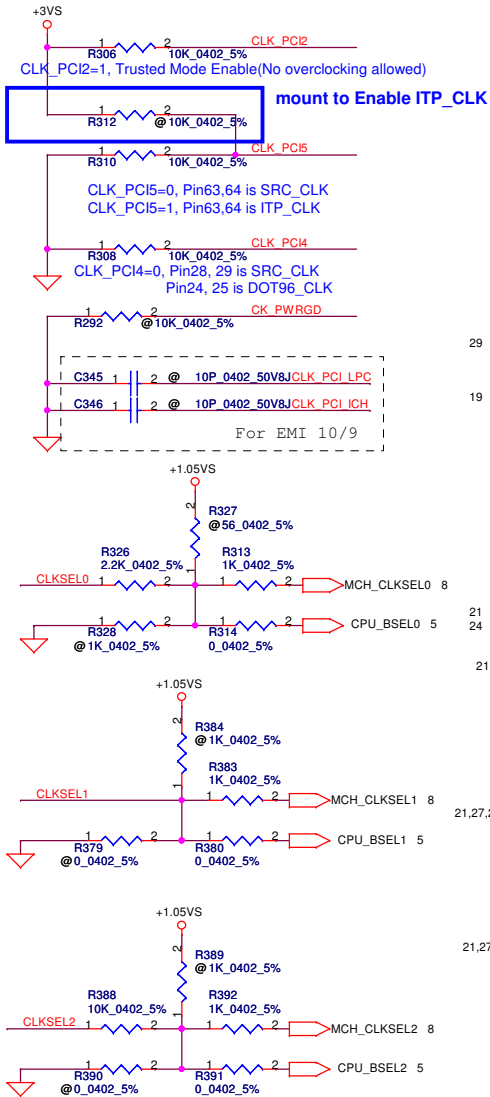
Compal Electronics, Inc.	
Title	DDRIII-SODIMM1
Document Number	NAWF3 M/B LA-4854P Schematic
Date	Wednesday, March 03, 2010
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FSLC	FSLB	FSLA	CPU MHz	SRC MHz	PCI MHz
0	0	0	266	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3

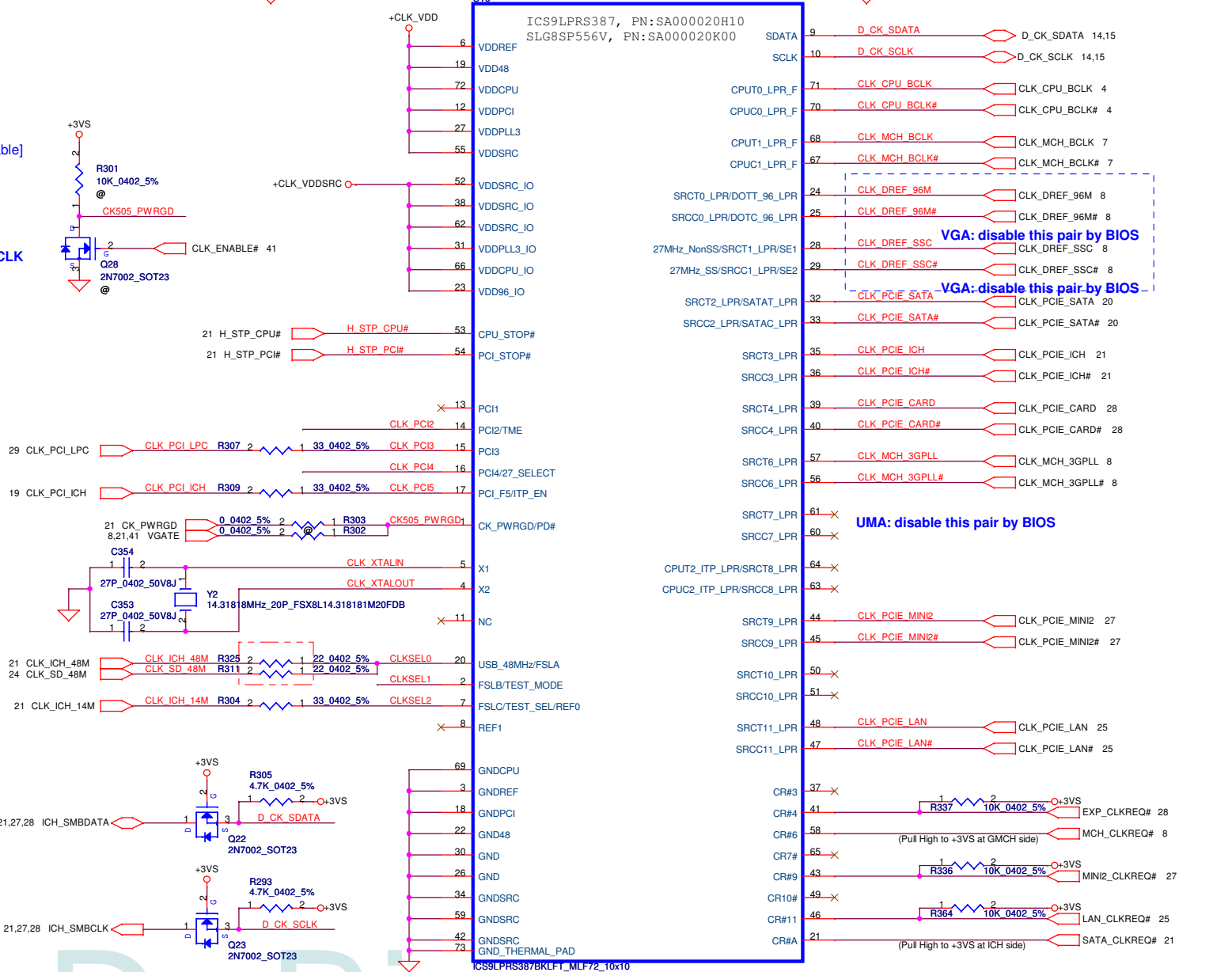
Table : ICS9LPRS387

CLK_REQ#	Control	Free-Run
CR#_10(WLAN)	PCIEX10	PCIEX0
CR#_6(MCH)	PCIEX6	PCIEX1
CR#_4(NEW CARD)	PCIEX4	
CR#_9(MINI CARDII)	PCIEX9	

SRC7(VGA\_CLK): Discrete VGA[Enable] UMA[Disable]



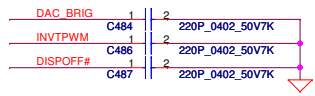
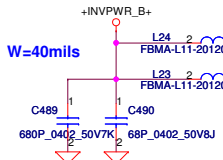
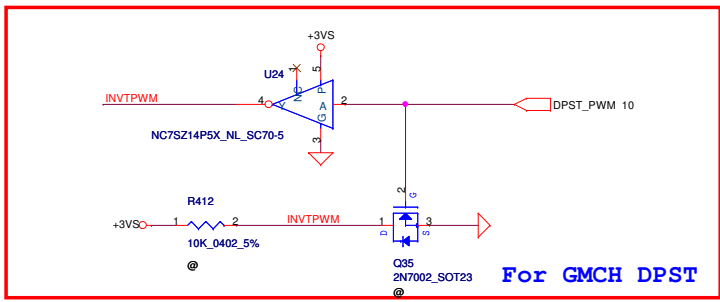
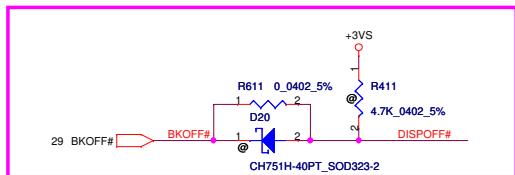
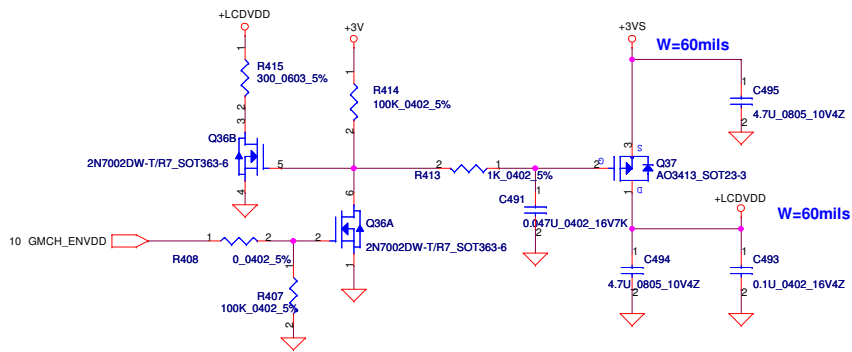
### Clock Generator



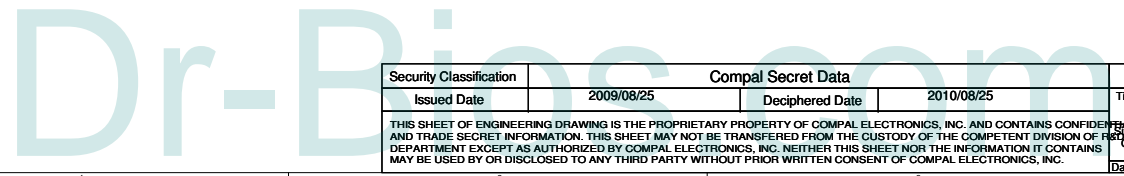
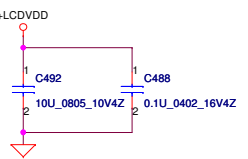
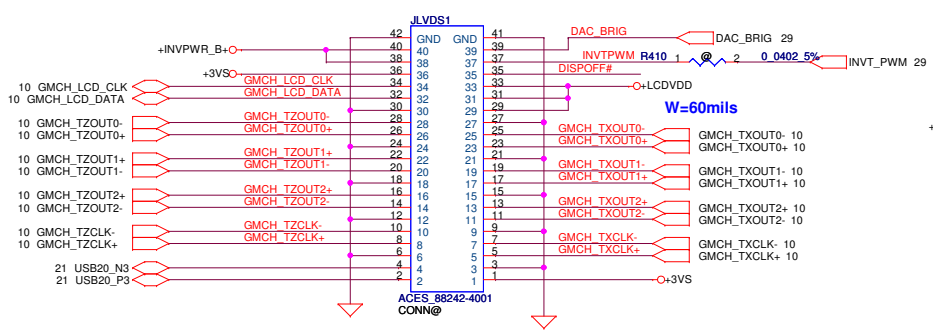
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/08/25	Deciphered Date	2010/08/25	Title Clock Generator (CK505)	
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Size	Document Number	Customer		Rev	1.0
Date:	Wednesday, March 03, 2010	Sheet	16	of 45	



# LCD POWER CIRCUIT

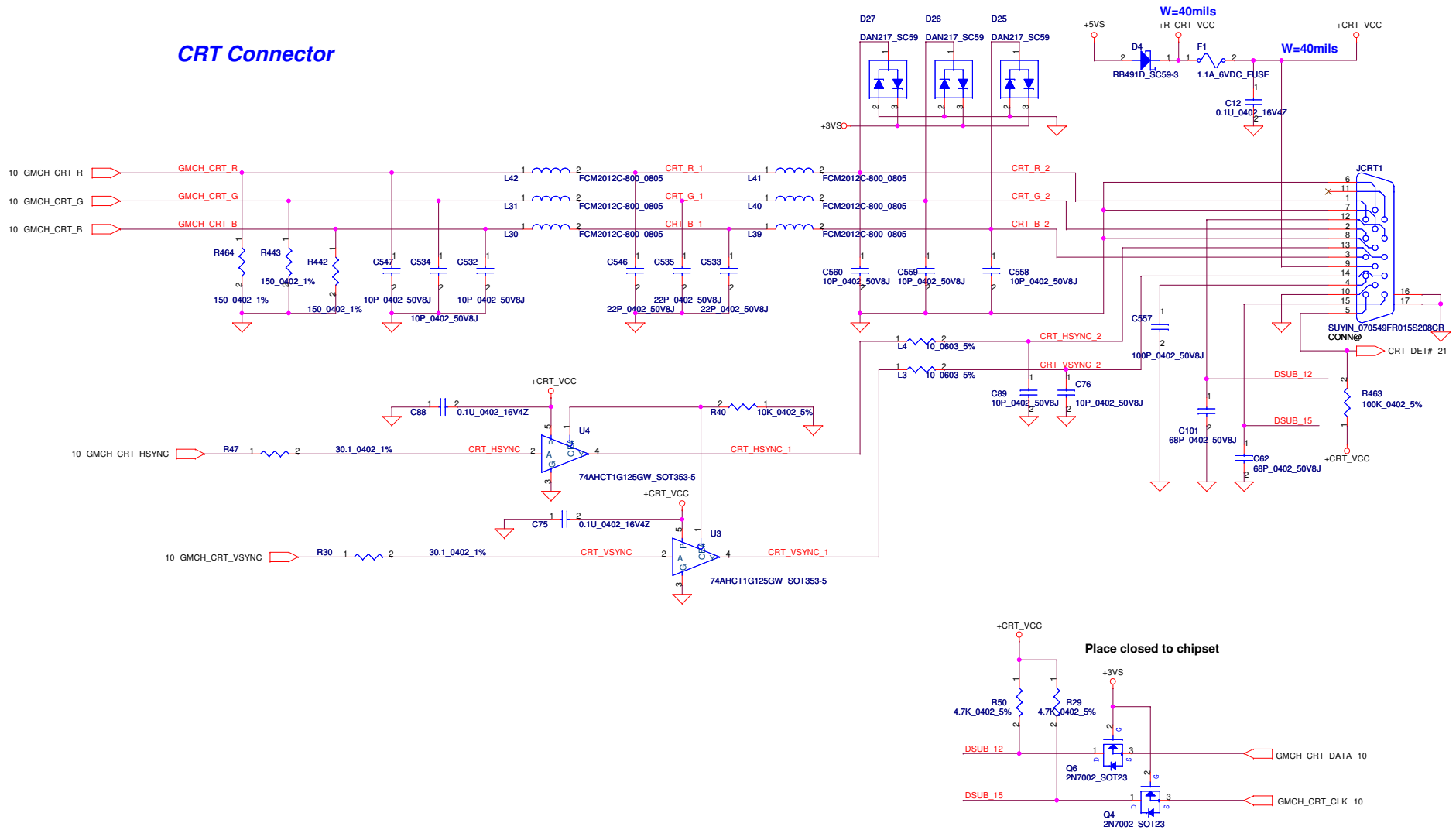


## LCD/PANEL BD. Conn.

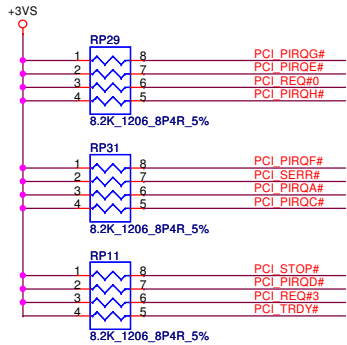
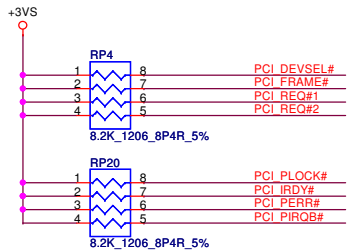


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				NAWF3 M/B LA-4854P Schematic
				Rev 1.0
				Date: Wednesday, March 03, 2010   Sheet 17 of 45

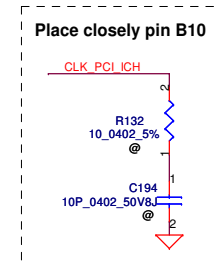
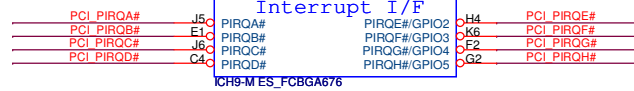
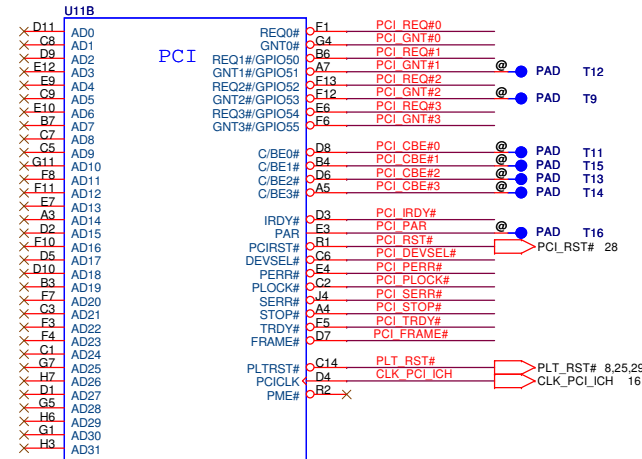
# CRT Connector



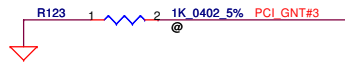
Security Classification		Compal Secret Data		Title	
Issued Date	2009/08/25	Deciphered Date	2010/08/25	Compal Electronics, Inc.	
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				NAWF3 M/B LA-4854P Schematic	1.0
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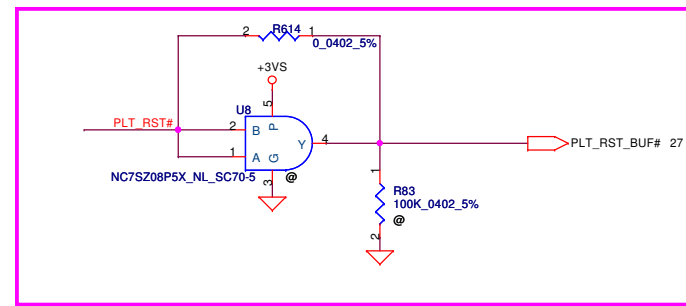
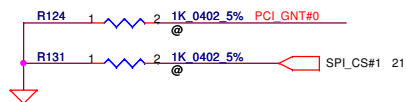
**DMI for ESI-compatible operation**  
**PCI\_GNT#1** Low= DMI for ESI-compatible operation  
 High= Default\* (Internal pull-up)



**A16 Swap Override Strap**  
**PCI\_GNT#3** Low= A16 swap override Enable  
 High= Default\*

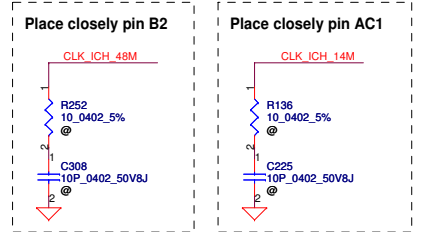
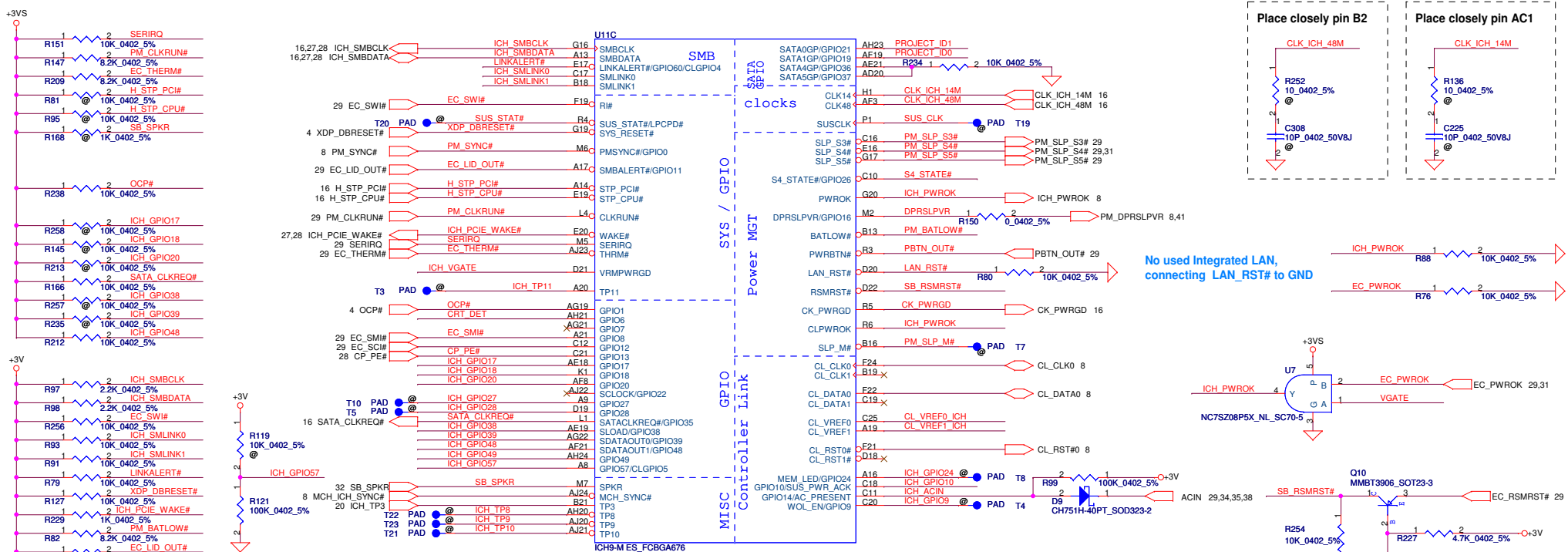


Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*

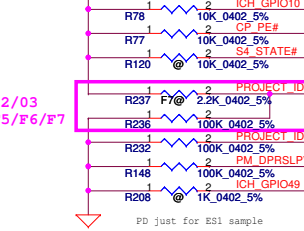
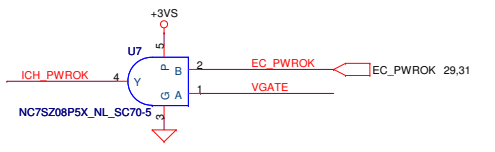


PVT2 8/24





No used Integrated LAN, connecting LAN\_RST# to GND



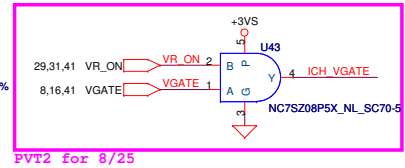
02/03 F5/F6/F7

For Express Card

For MINI\_CARD1

For PCIE LAN

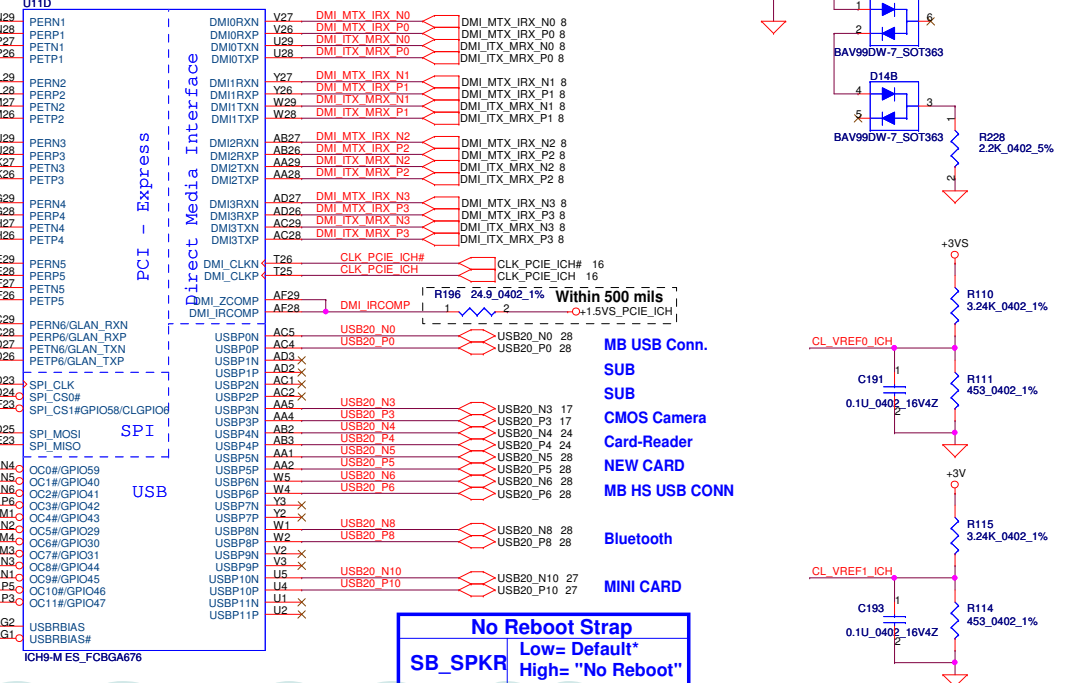
2010/02/24 Add PU Res. High: CRT Det



PVT2 for 8/25

	Project_ID0	Project_ID1	Project_ID2	Board_ID (EC)
PAWF6	0	0	0	5
PAWF5	0	0	1	5
PAWF7	1	0	0	5

02/03 F5/F6/F7



No Reboot Strap  
SB\_SPKR Low= Default High= "No Reboot"

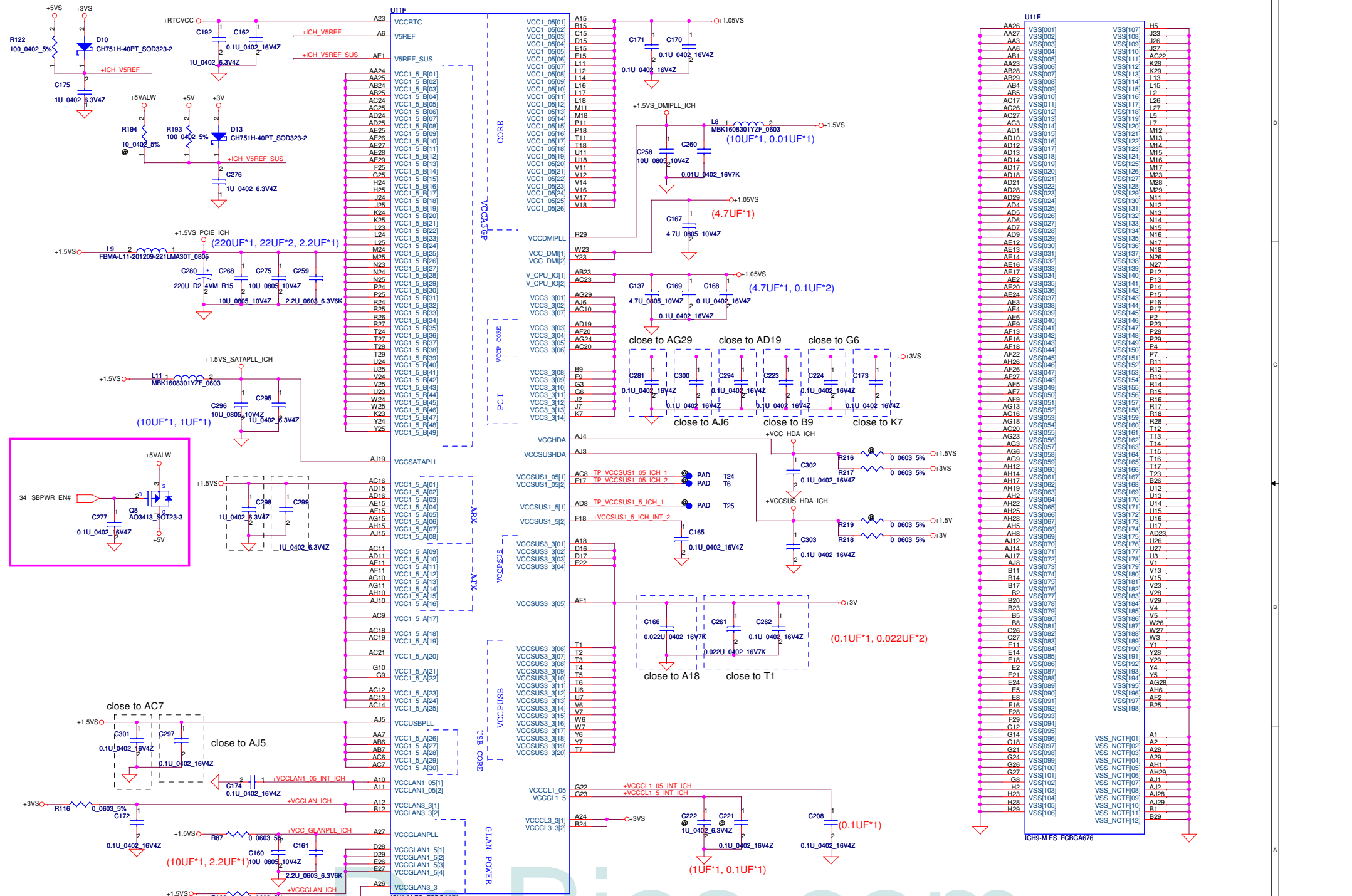
**Internal TPM Strap**  
Low= Disable\*  
High= ITPM enable by MCH strap

**DMI Termination Voltage**  
Low= Desktop used  
High= Mobile\* (Internal pull-up)

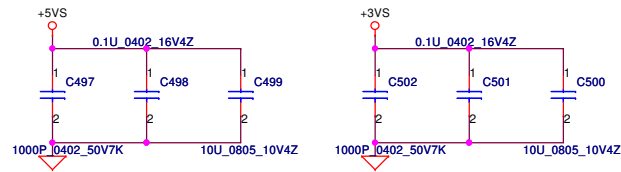
Security Classification	Compal Secret Data
Issued Date	2009/08/25
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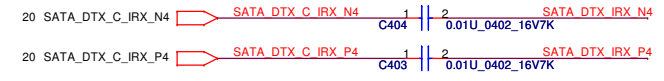
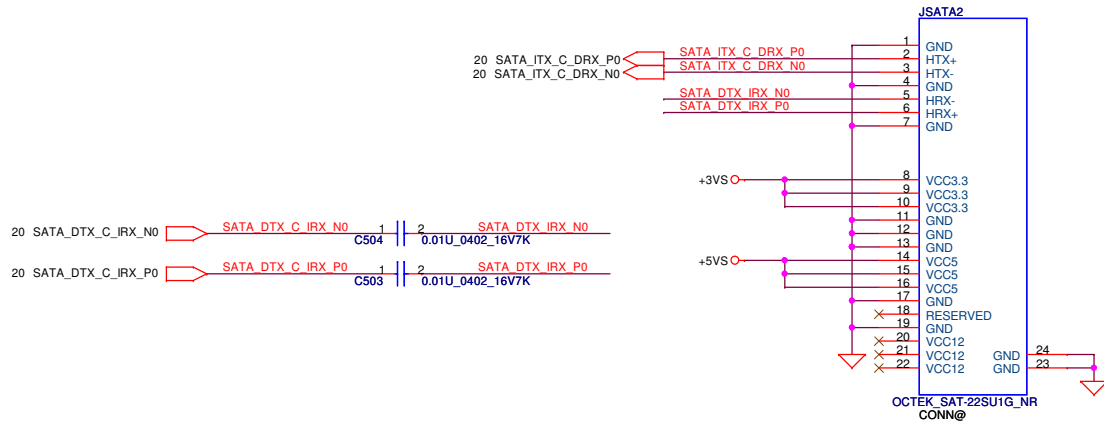
Compal Electronics, Inc.	
ICH9M(3/4)-USB,GPIO,PCIE	
Document Number	NAWF3 M/B LA-4854P Schematic
Date	Wednesday, March 03, 2010
Sheet	21 of 45



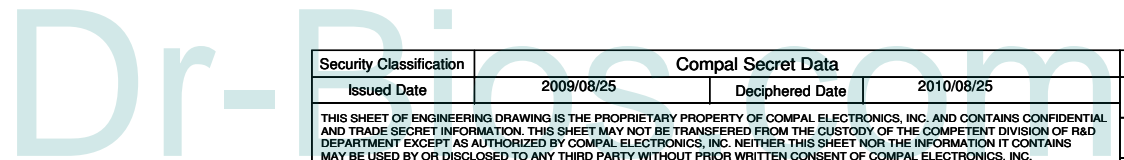
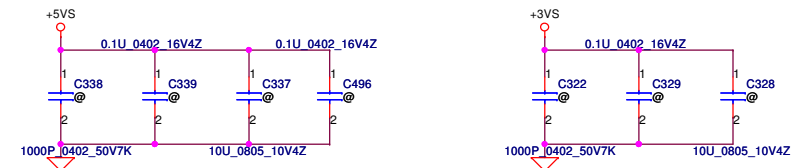
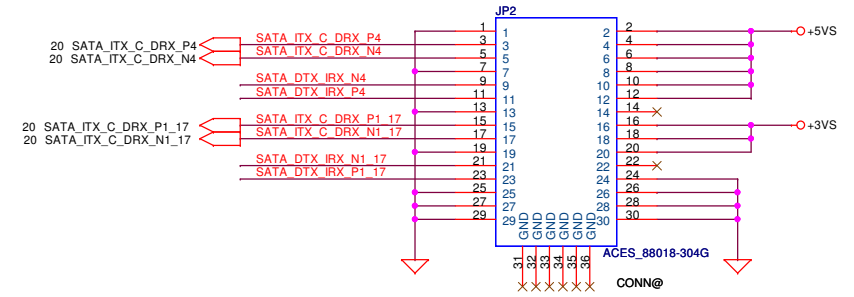
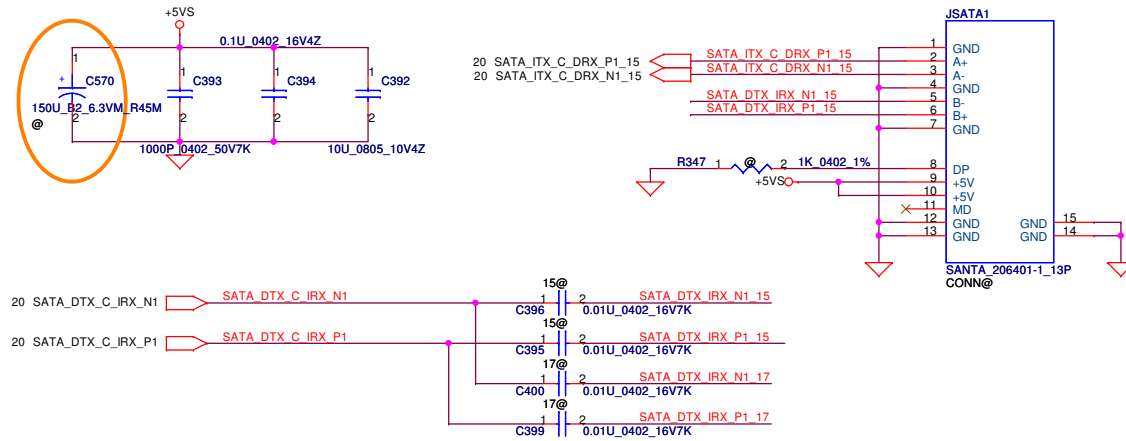
Security Classification	Compal Secret Data		Title	ICh9M(4/4)-POWER&GND	
Issued Date	2009/08/25	Deciphered Date	2010/08/25	Size	Document Number
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			Date	Wednesday, March 03, 2010	Rev 1.0
			Sheet 22 of 45		



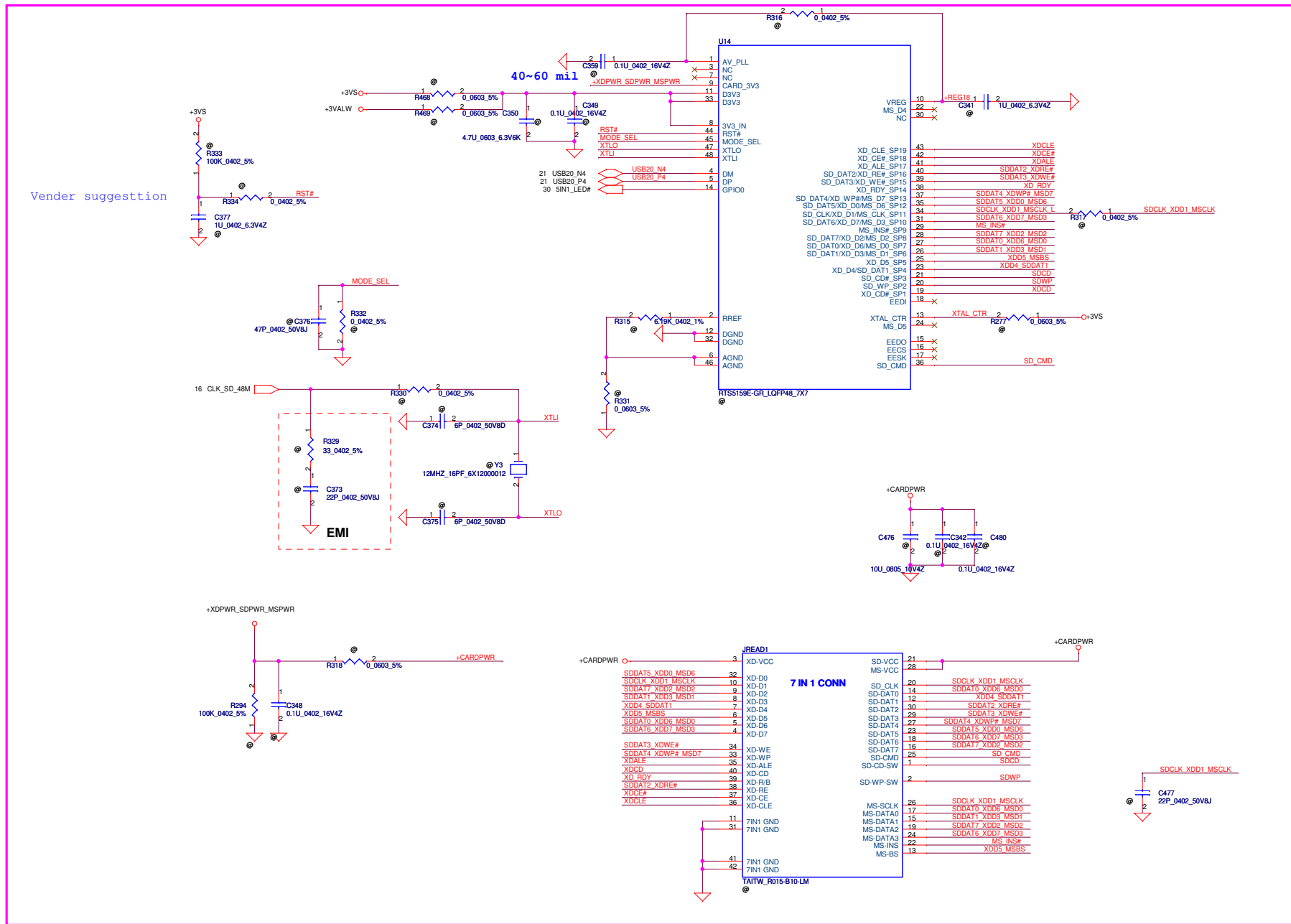
### SATA HDD Conn.



### SATA ODD Conn.



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/08/25	Deciphered Date	2010/08/25	Title	
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Size	Document Number	Customer		Rev	
	NAWF3 M/B LA-4854P Schematic			1.0	
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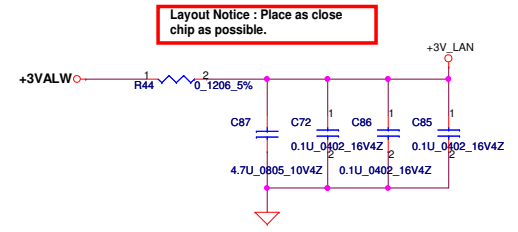
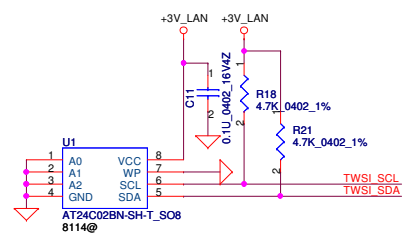
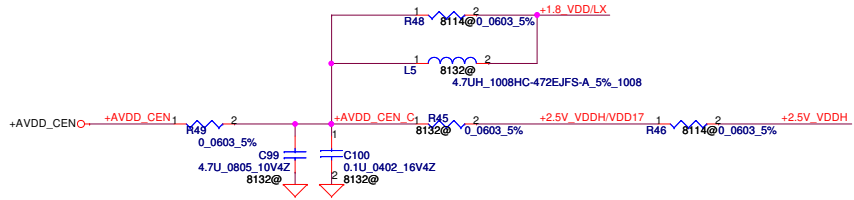


02/03 F5/F6/F7  
remove Card reader

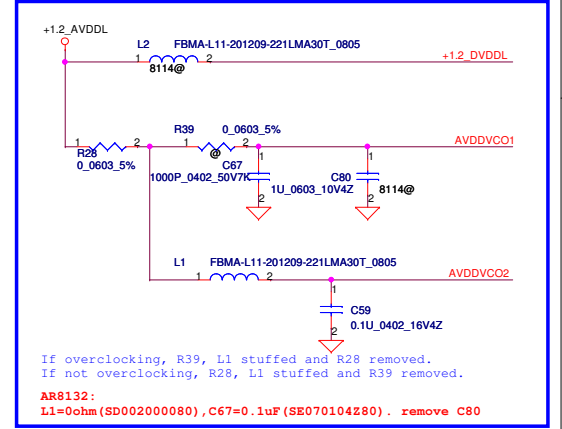
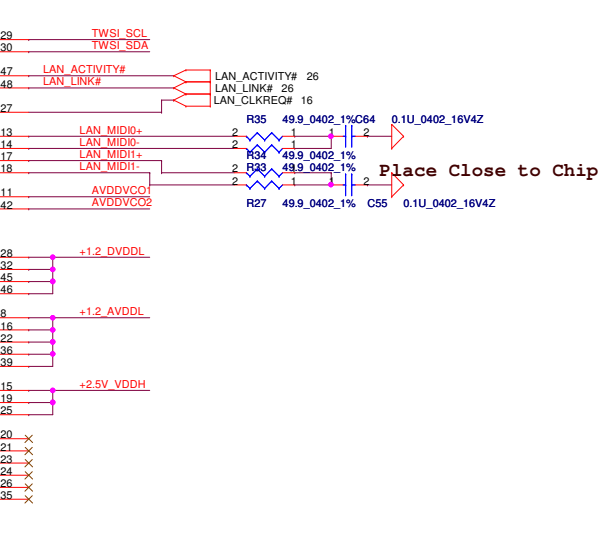
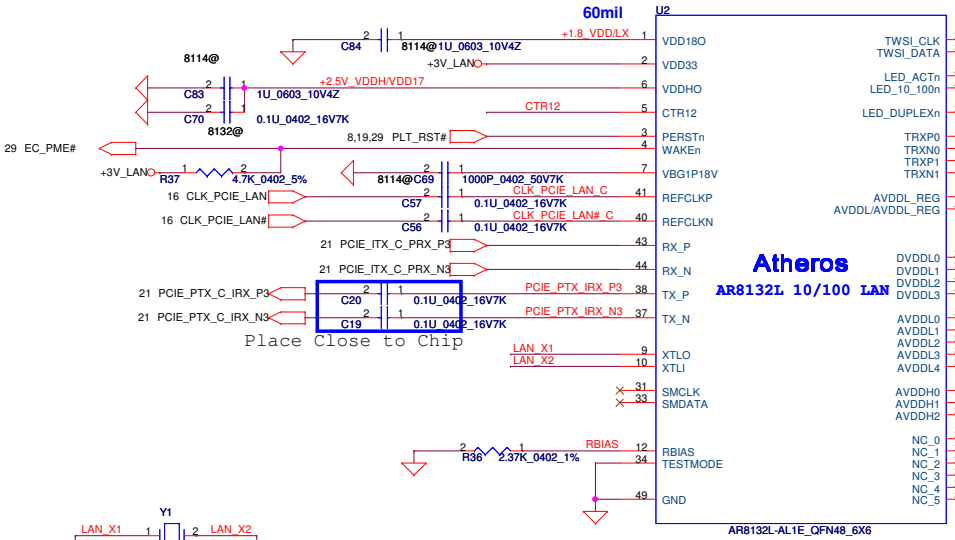


Security Classification		Compal Secret Data		Title	
Issued Date	2009/08/25	Deciphered Date	2010/08/25	5 in 1 Card reader	
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				Customer	1.0
				Date	Wednesday, March 03, 2010
				Sheet	24 of 45

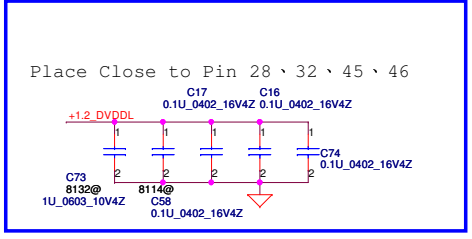




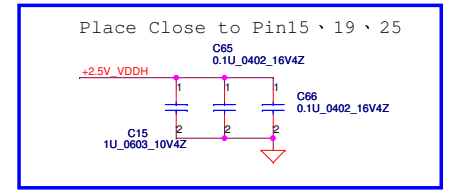
Layout Notice : Place as close chip as possible.



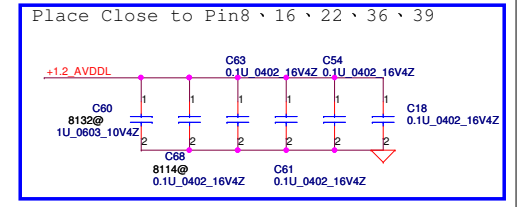
If overclocking, R39, L1 stuffed and R28 removed.  
If not overclocking, R28, L1 stuffed and R39 removed.  
AR8132:  
L1=0ohm(SD00200080), C67=0.1uF(SE070104Z80) . remove C80



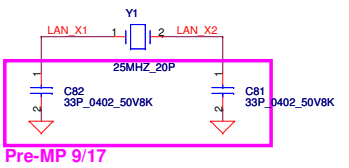
Place Close to Pin 28、32、45、46



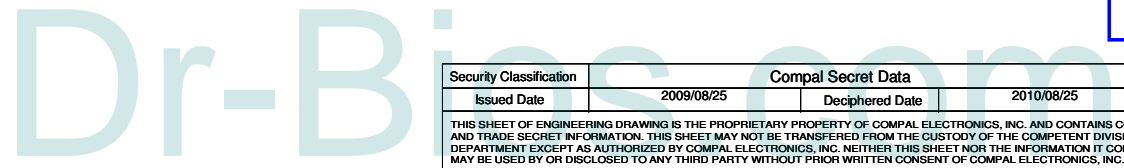
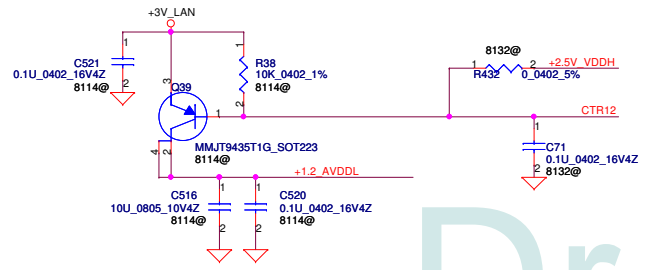
Place Close to Pin15、19、25



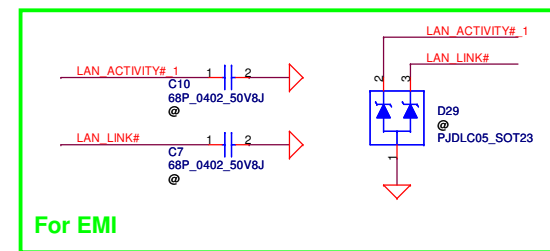
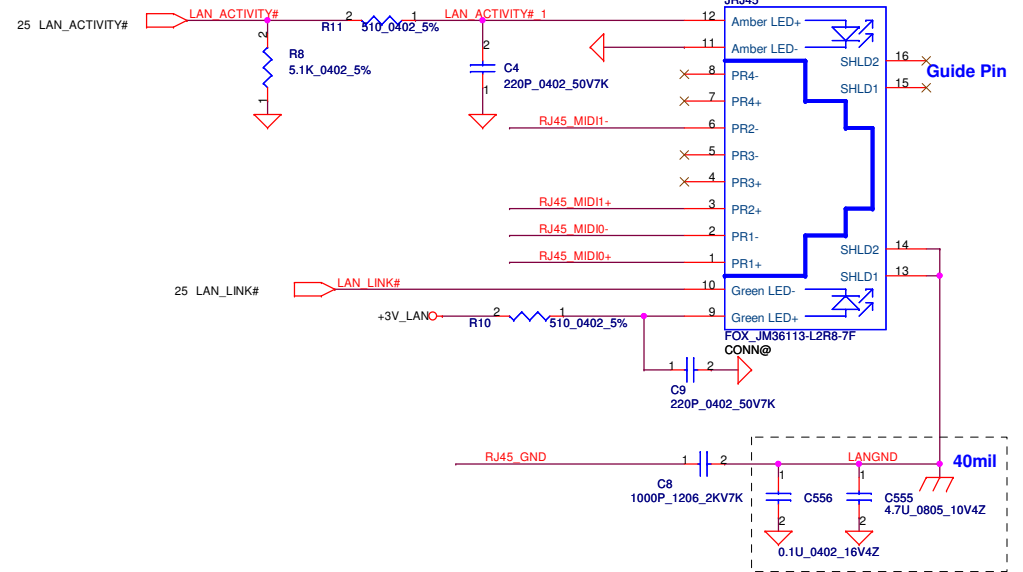
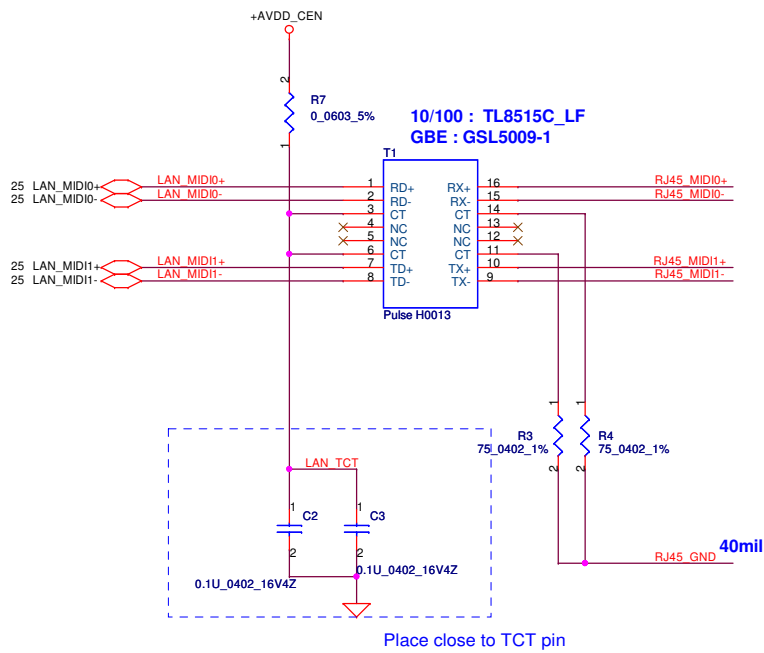
Place Close to Pin8、16、22、36、39



Pre-MP 9/17



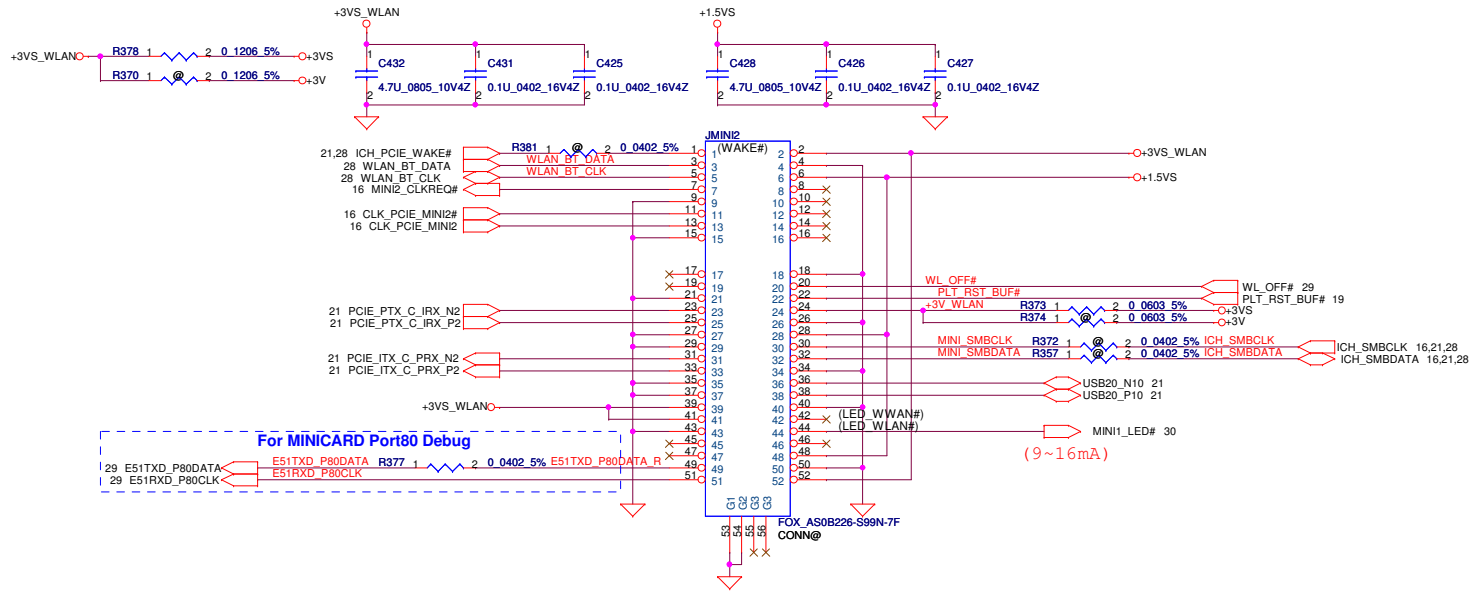
Security Classification	Compal Secret Data		Title	
Issued Date	2009/08/25	Deciphered Date	2010/08/25	AR8114
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Date: Wednesday, March 03, 2010			Sheet 25 of 45	



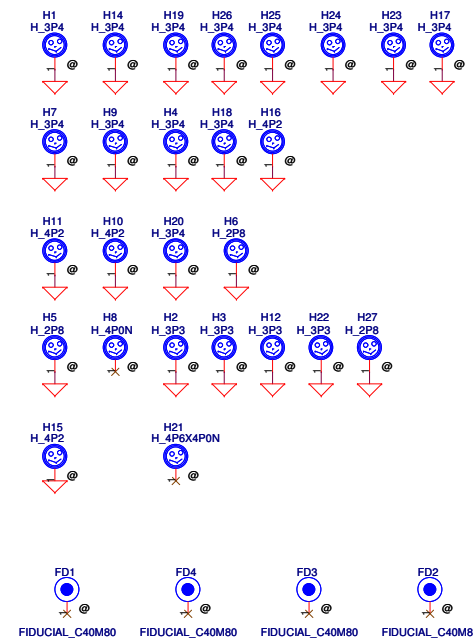
Dr-Print.com

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Size	Document Number			Rev	
B	NAWF3 M/B LA-4854P Schematic			1.0	
Date:	Wednesday, March 03, 2010	Sheet	26	of 45	

# For Wireless LAN



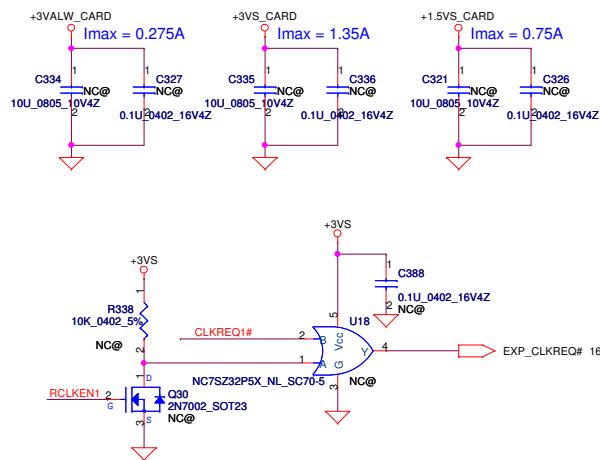
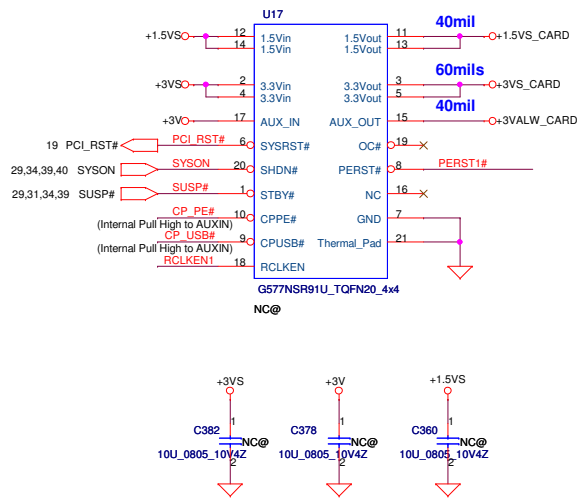
Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)



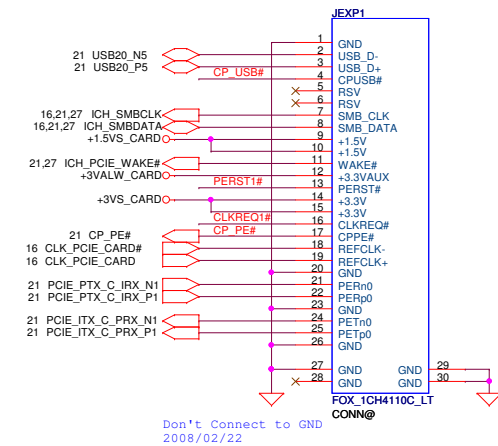
Dr-Bios.com

Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/08/25	Deciphered Date	2010/08/25	Title
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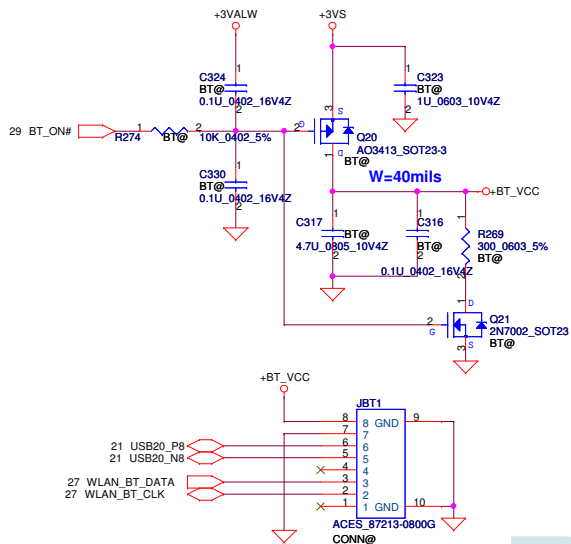
### New Card Power Switch



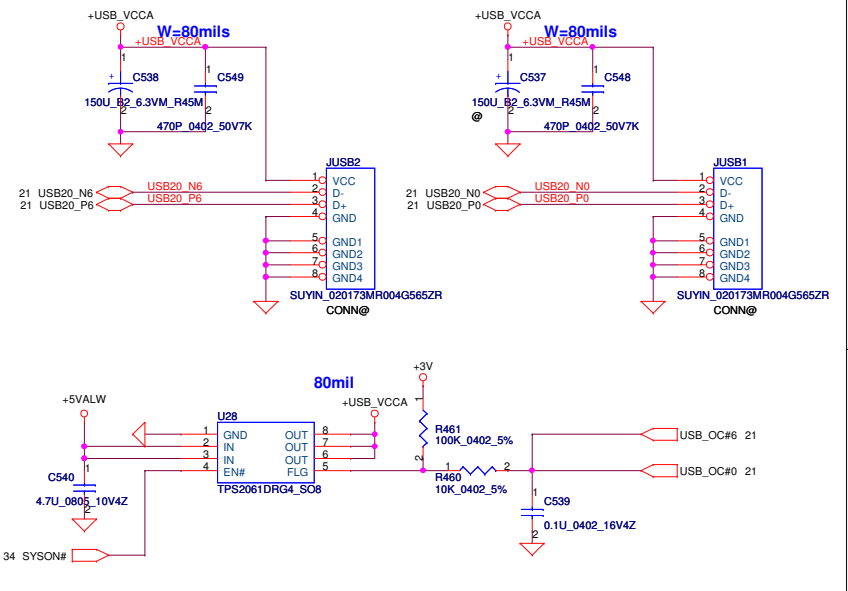
### New Card Socket (Left/TOP)



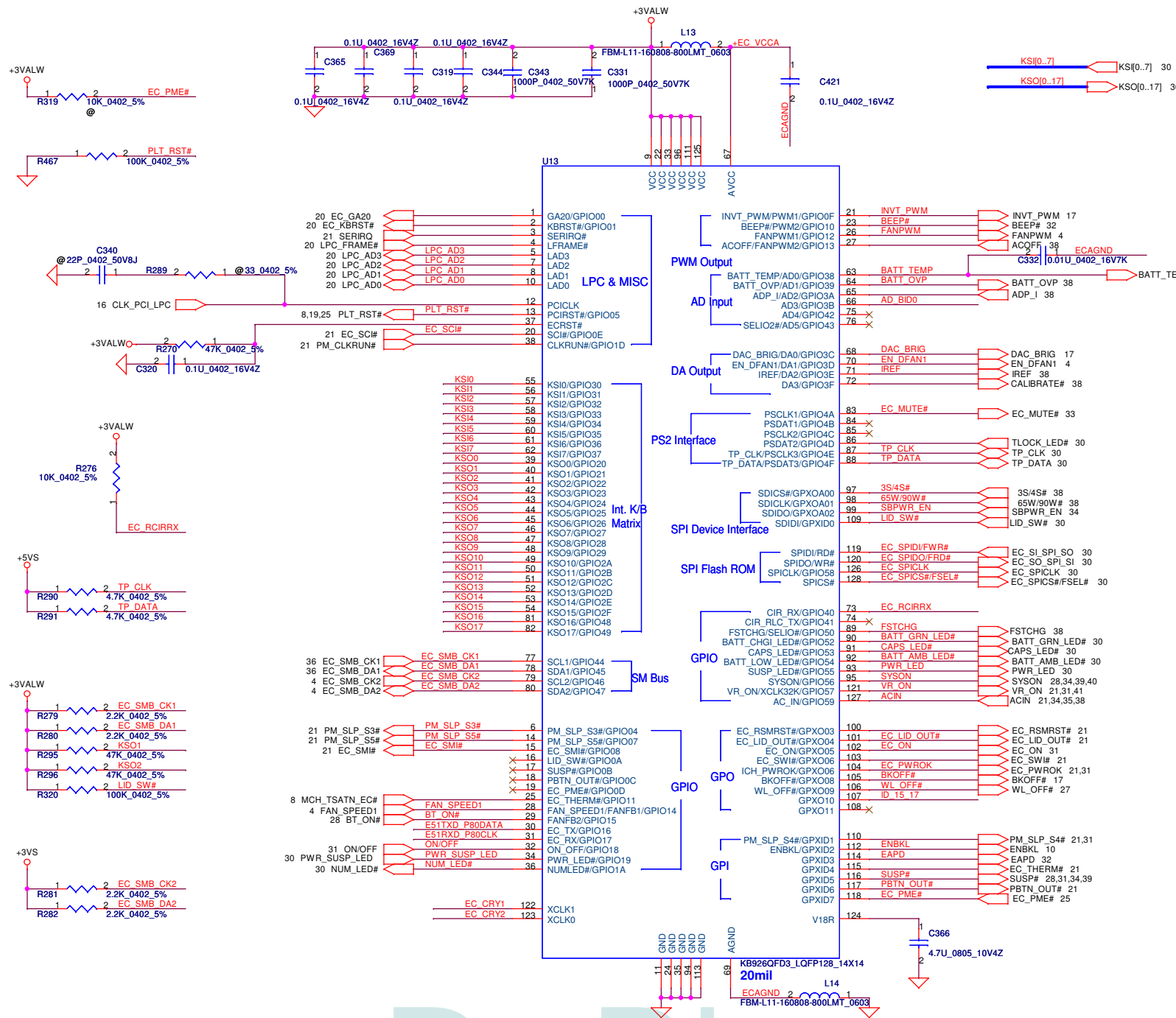
### Bluetooth Conn.



### USB CONN.

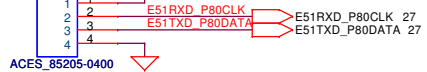


Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2009/08/25	Deciphered Date	2010/08/25	Title	
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				NAWF3 M/B LA-4854P Schematic	
				Date: Wednesday, March 03, 2010	
				Sheet 28 of 45	

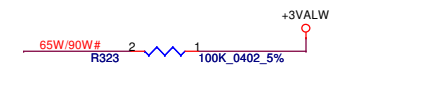
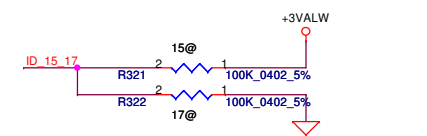
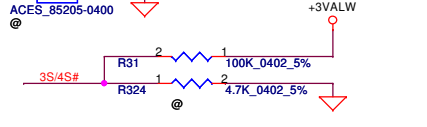
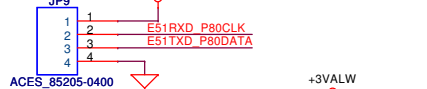


**For EC Tools**

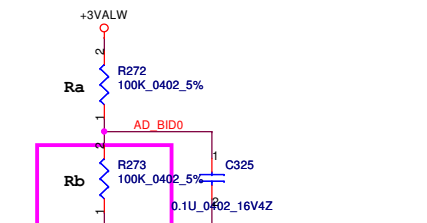
Place on RAM door



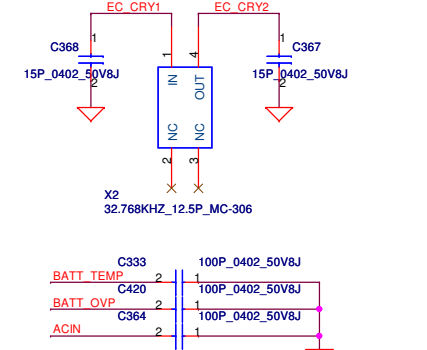
Place on MiniCard



Analog Board ID definition, Please see page 3.



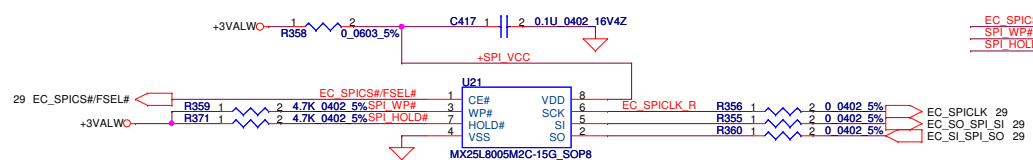
02/03 F5/F6/F7 modify



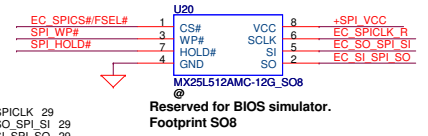
Dr-PCB.com

<BOM Structure>

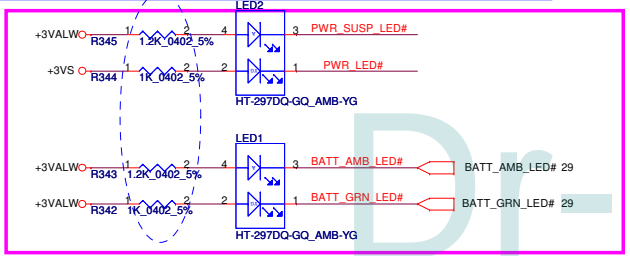
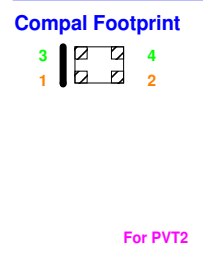
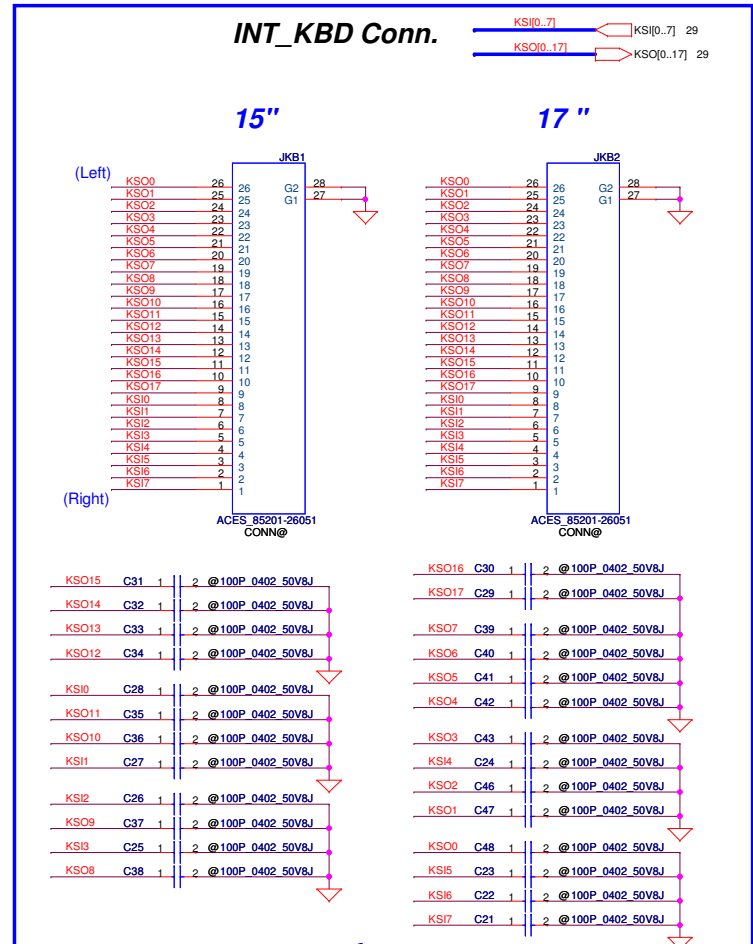
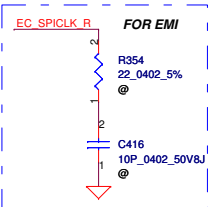
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Size	Document Number			Rev	
B	NAWF3 M/B LA-4854P Schematic			1.0	
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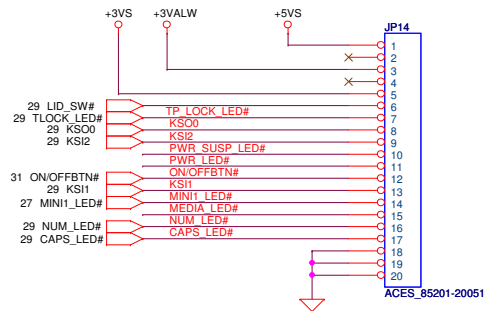
ENE suggestion SPI Frequency over 66MHz  
 SST: 50MHz  
 MXIC: 70MHz  
 ST: 40MHz



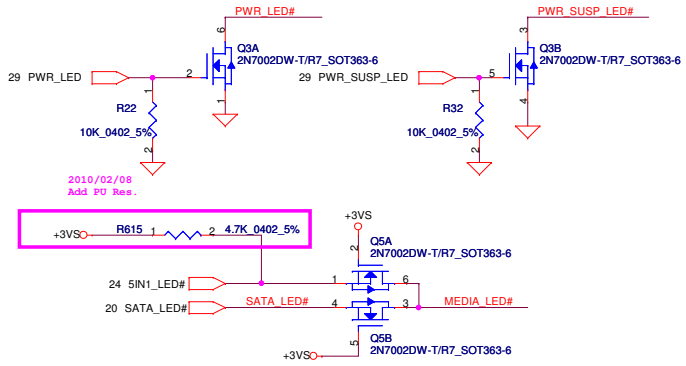
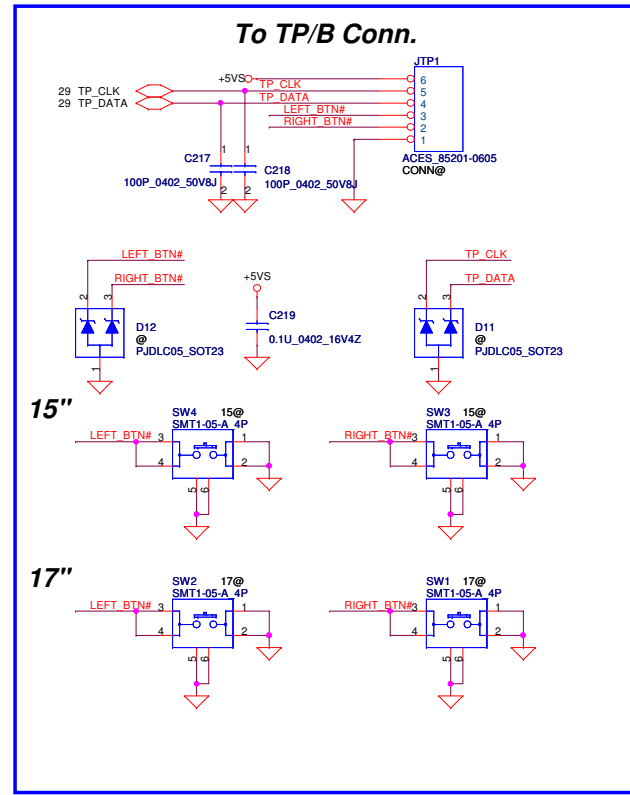
Reserved for BIOS simulator.  
 Footprint S08



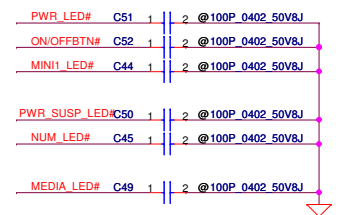
To POWER/B



	KSO0
KSI1	WL_BTN#
KSI2	TLOCK_BTN#
KSI3	
KSI4	
KSI5	



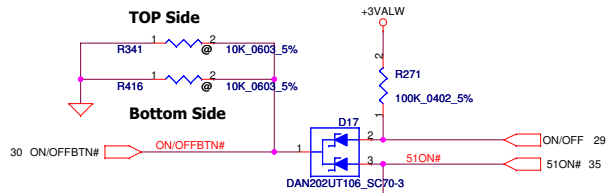
FOR EMI



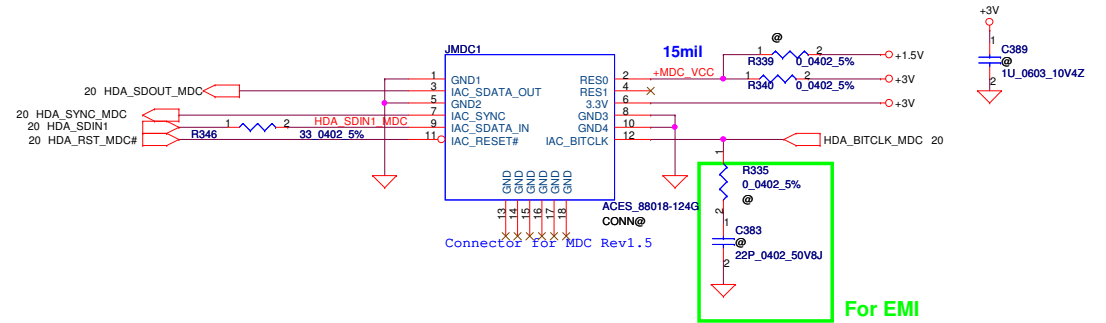
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Issued Date	2009/08/25	Deciphered Date	2010/08/25	Title
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				NAWF3 M/B LA-4854P Schematic
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# Power Button

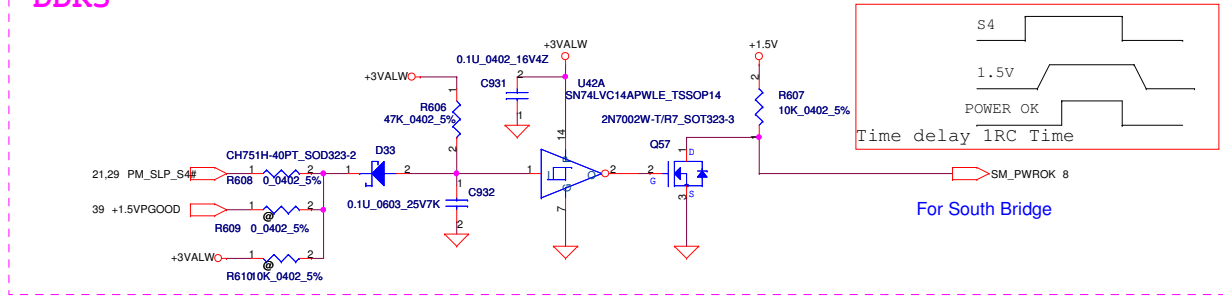
ON/OFF switch



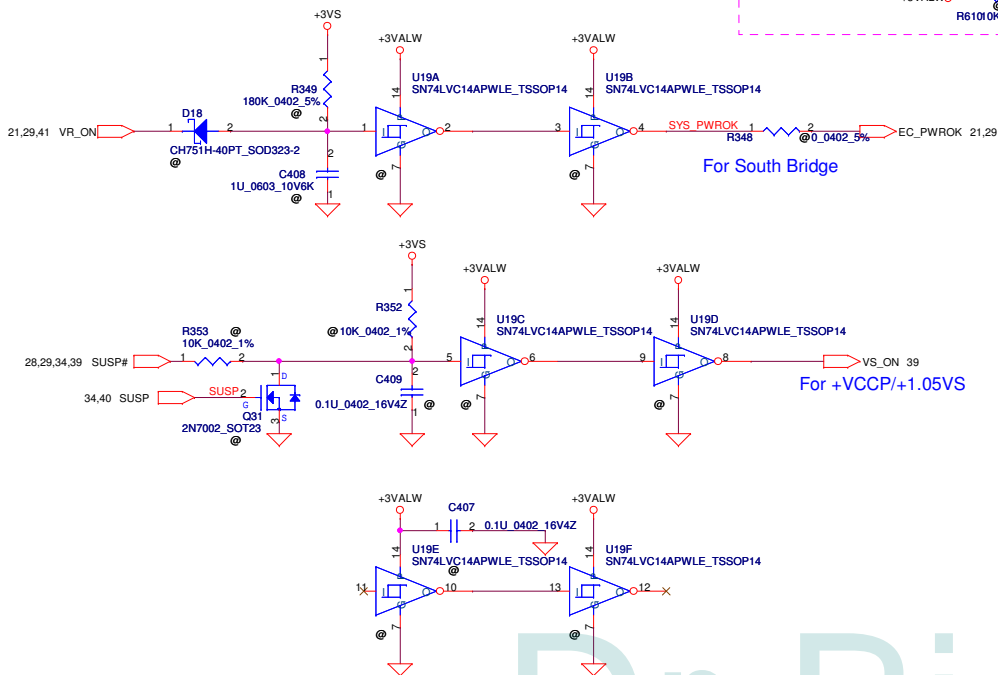
# HDA MDC Conn.



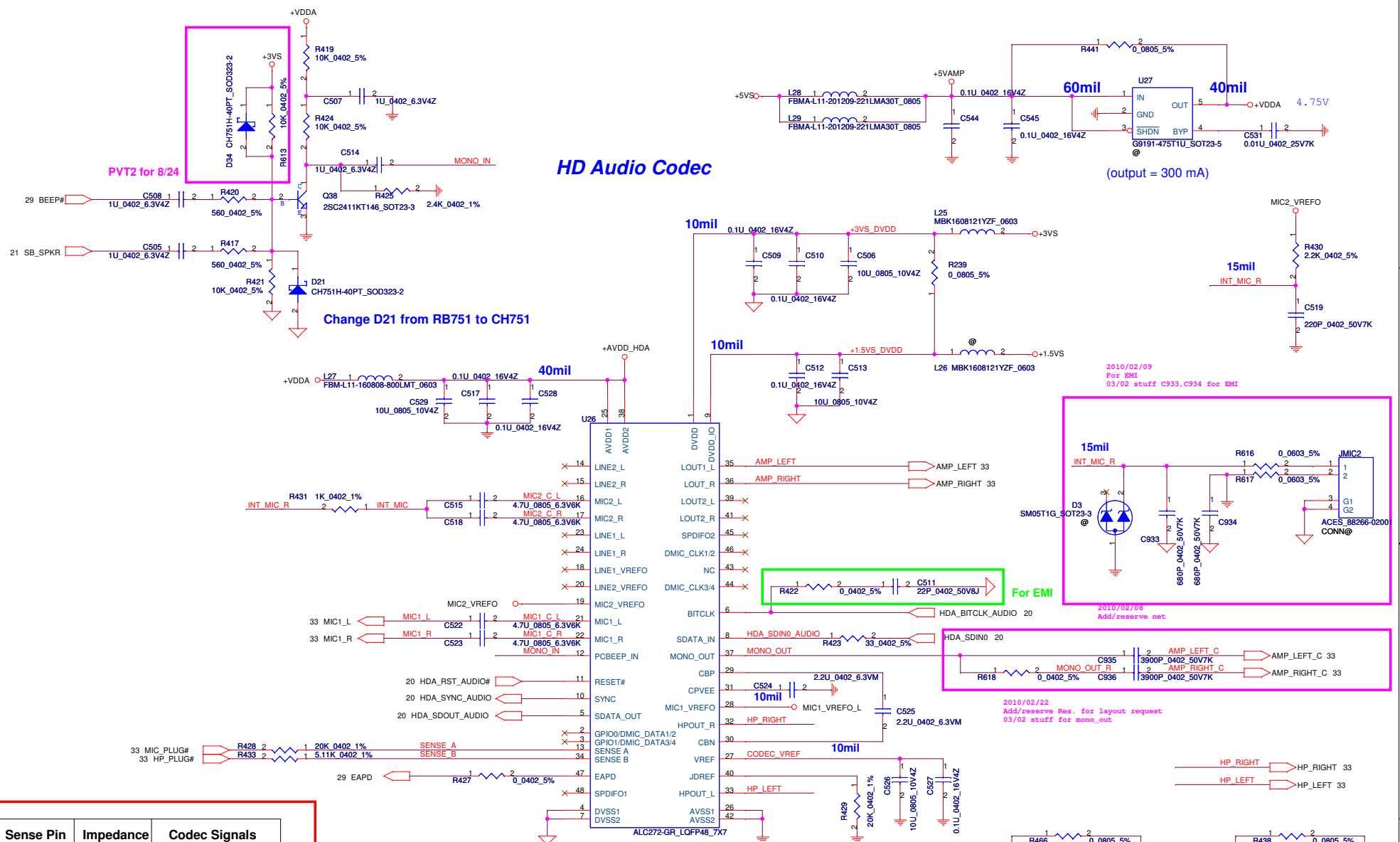
# DDR3



# Power ON Circuit



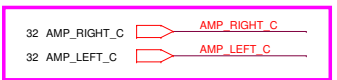
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Issued Date	2009/08/25	Deciphered Date	2010/08/25	Title
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				NAWF3 M/B LA-4854P Schematic
				Rev 1.0
				Date: Wednesday, March 03, 2010   Sheet 31 of 45



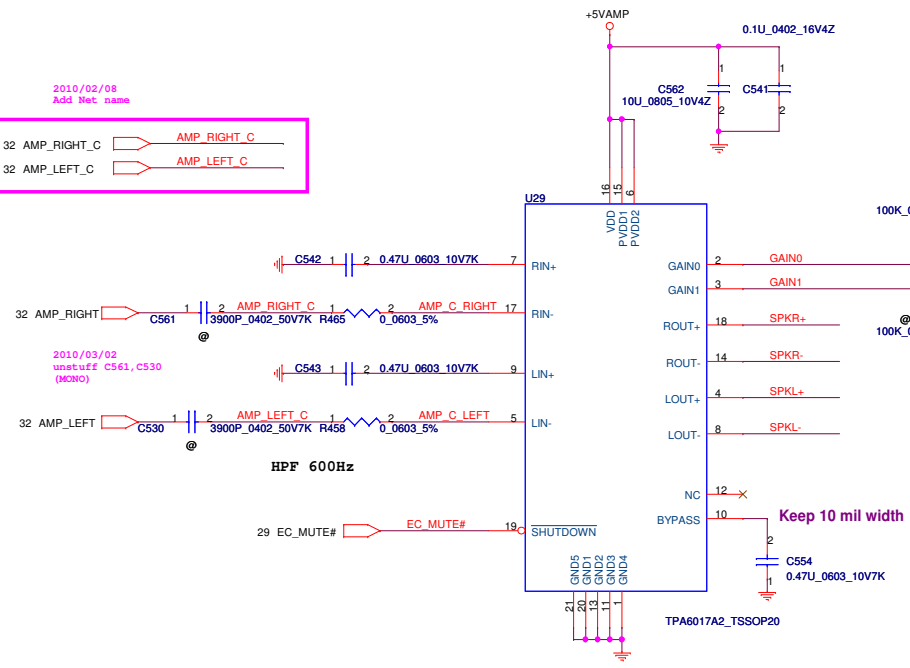
Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	
	20K	PORT-B (PIN 21, 22)
	10K	
	5.1K	
SENSE B	39.2K	
	20K	
	10K	
	5.1K	PORT-H (PIN 32,33)



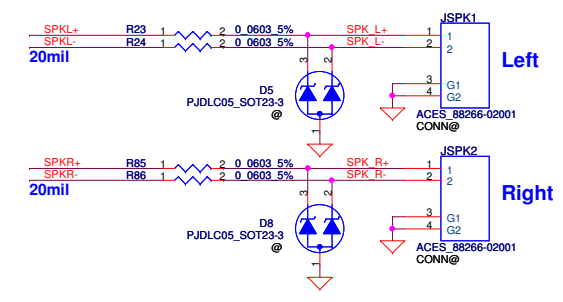
2010/02/08  
Add Net name



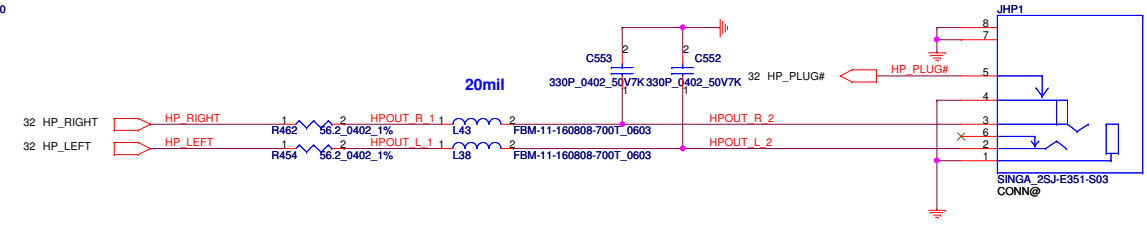
2010/03/02  
unstuff C561, C530  
(MONO)



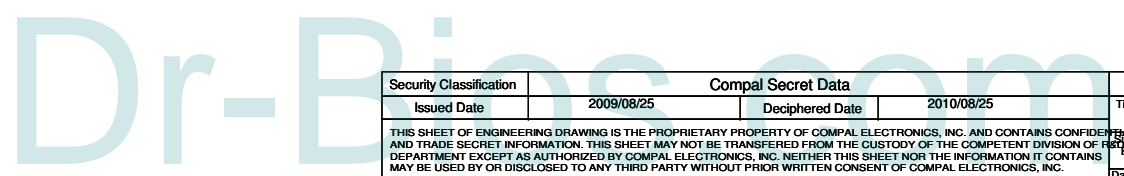
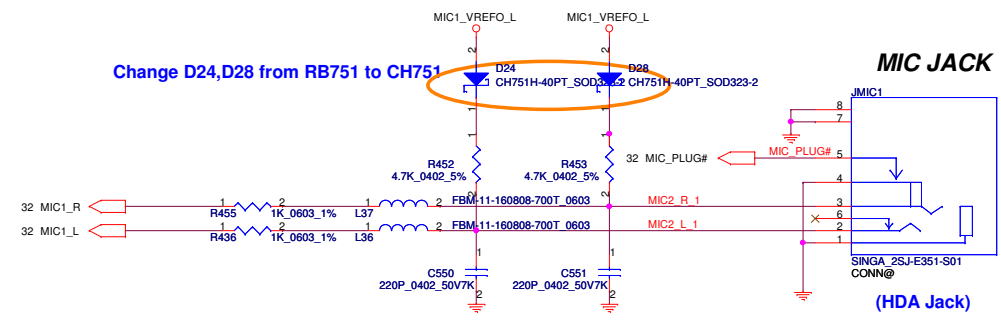
### Int. Speaker Conn.



### LINE Out/Headphone Out



Change D24, D28 from RB751 to CH751



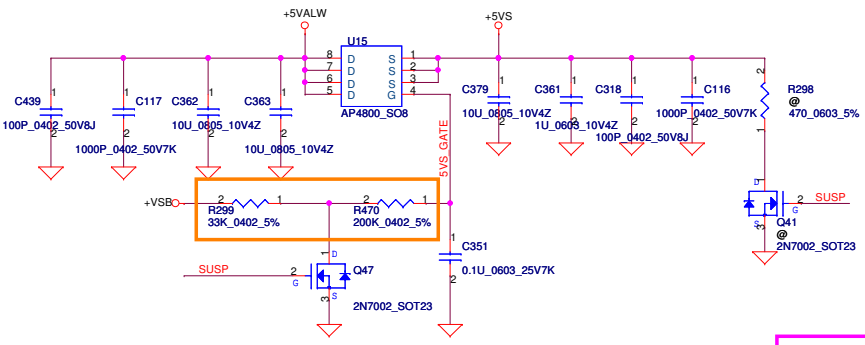
Security Classification	Compal Secret Data		Title	
Issued Date	2009/08/25	Deciphered Date	2010/08/25	Document Number
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Date: Wednesday, March 03, 2010				Sheet 33 of 45

Compal Electronics, Inc.

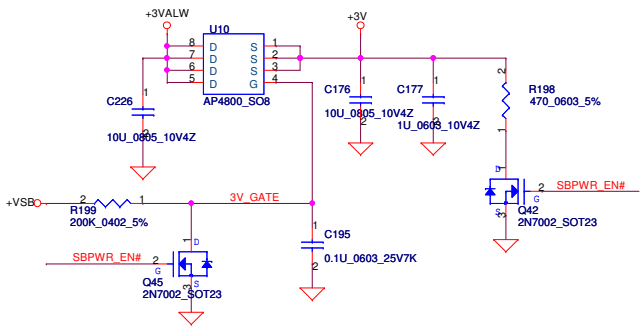
Amplifier & Audio Jack

NAWF3 M/B LA-4854P Schematic

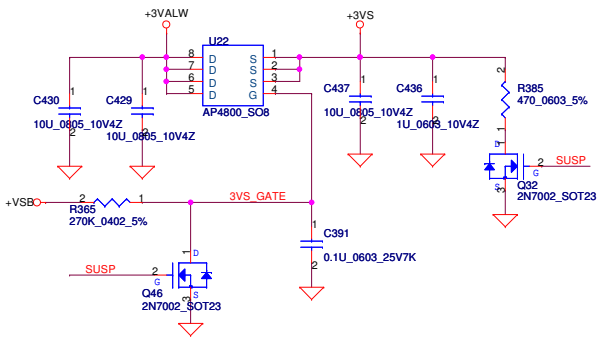
**+5VALW TO +5VS**



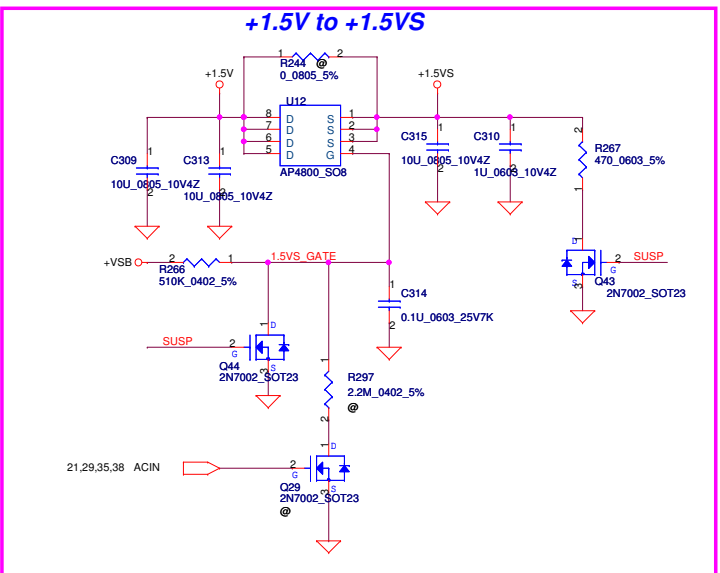
**+3VALW TO +3V\_SB(ICH8M AUX Power)**



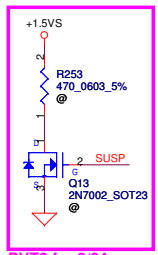
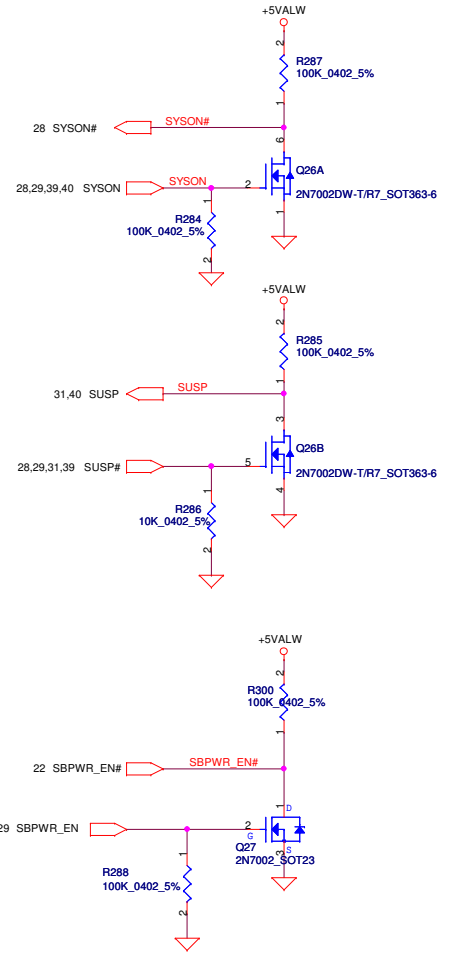
**+3VALW TO +3VS**



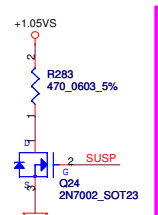
**+1.5V to +1.5VS**



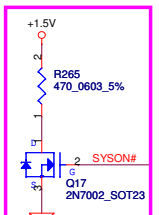
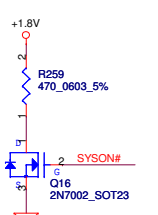
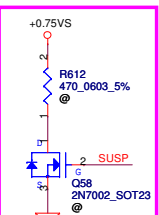
PVT2 for 8/24



PVT2 for 8/24

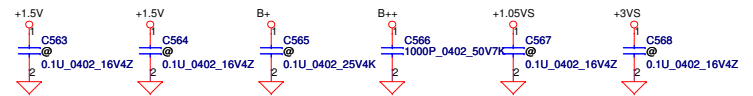


PVT2 for 8/24

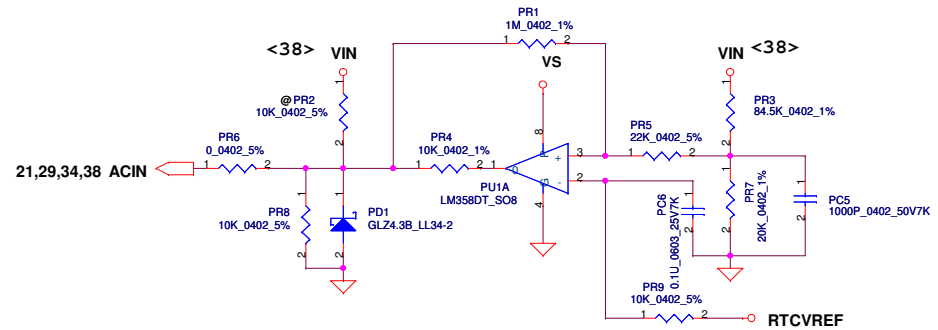
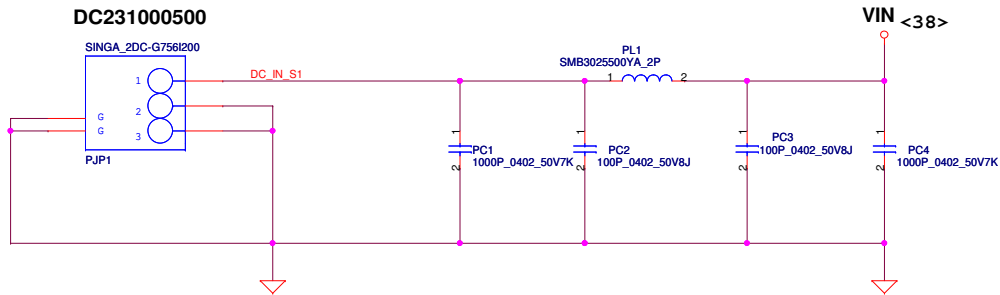


PVT2 for 8/24

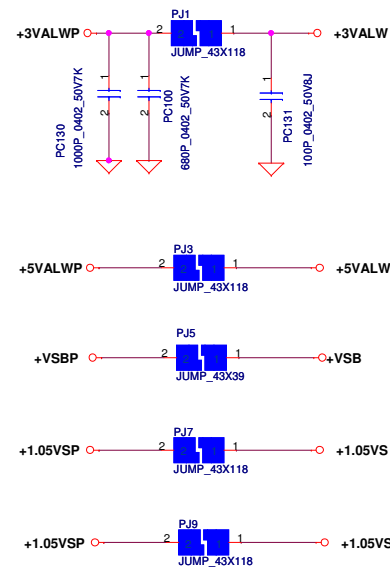
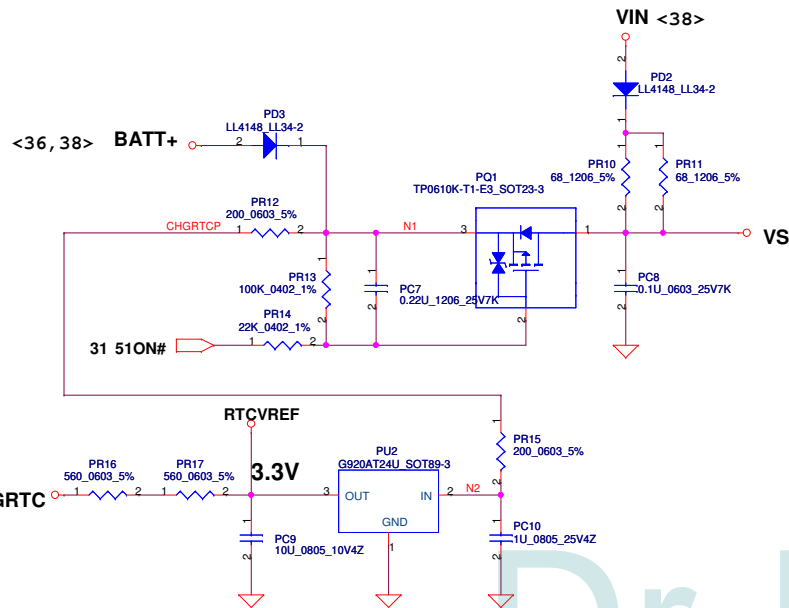
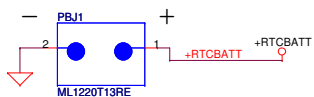
**Reserve for EMI request**



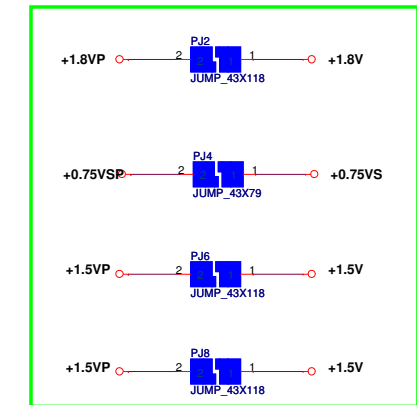
Security Classification	Compal Secret Data		Title	
Issued Date	2009/08/25	Deciphered Date	2010/08/25	DC Interface
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Date: Wednesday, March 03, 2010				Rev 1.0



Vin Dectector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V



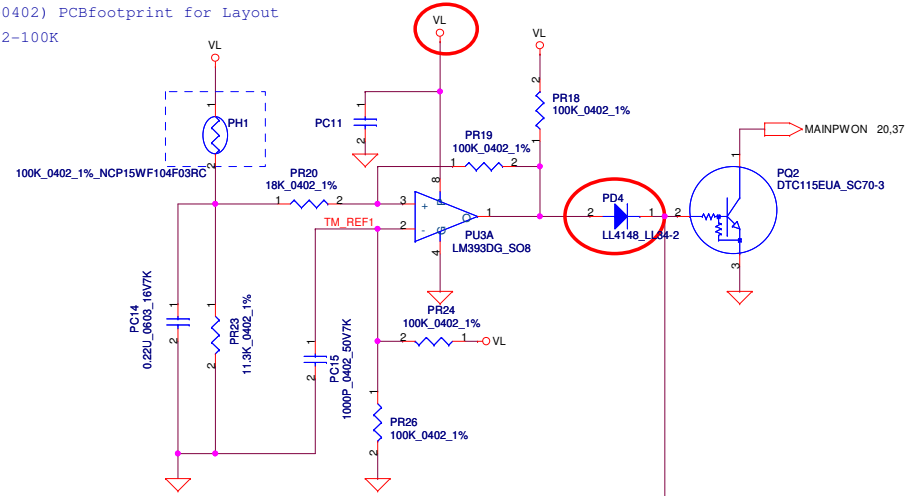
Delete (PJ16/PJ17/PJ18)  
1.1VILDO + VGA\_CORE JUMPER



**PH1 under CPU botten side :**

CPU thermal protection at 90 degree C  
Recovery at 70 degree C

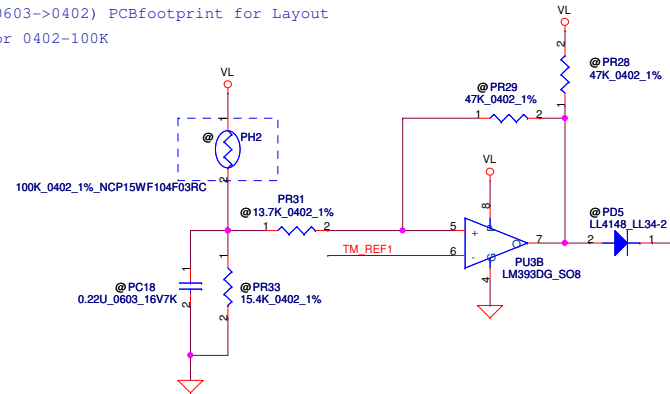
2009\_08\_06 (0603->0402) PCBfootprint for Layout  
Change P/N for 0402-100K



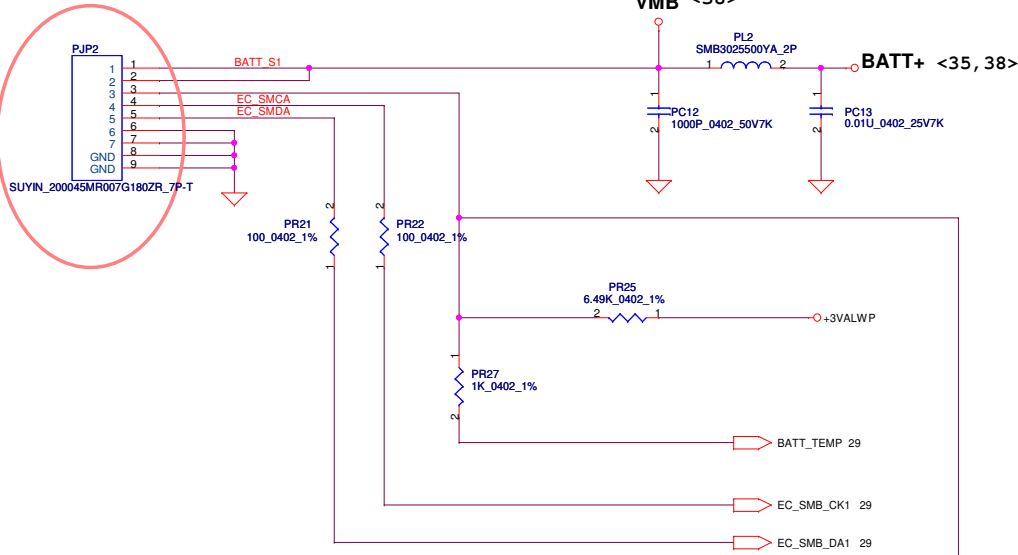
**PH2 near main Battery CONN :**

BAT. thermal protection at 90 degree C  
Recovery at 70 degree C

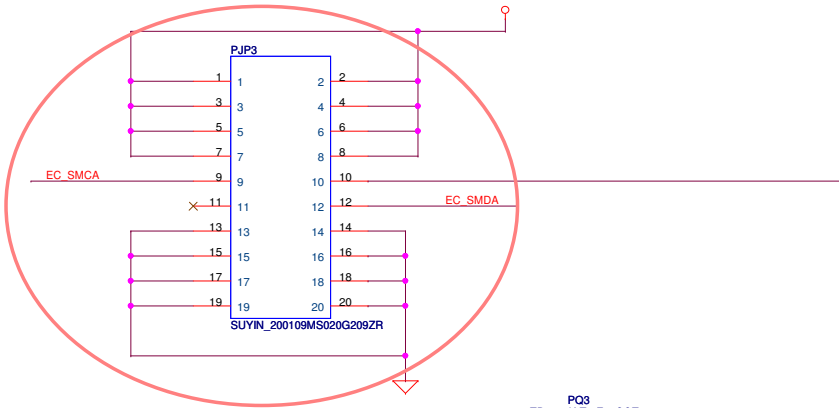
2009\_08\_06 (0603->0402) PCBfootprint for Layout  
Change P/N for 0402-100K



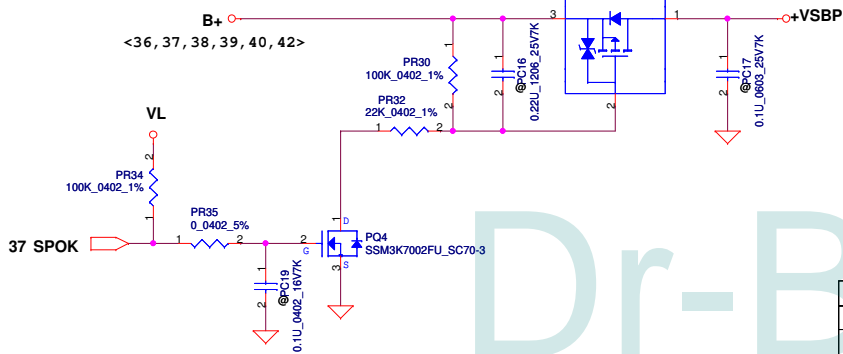
**VMB <38>**



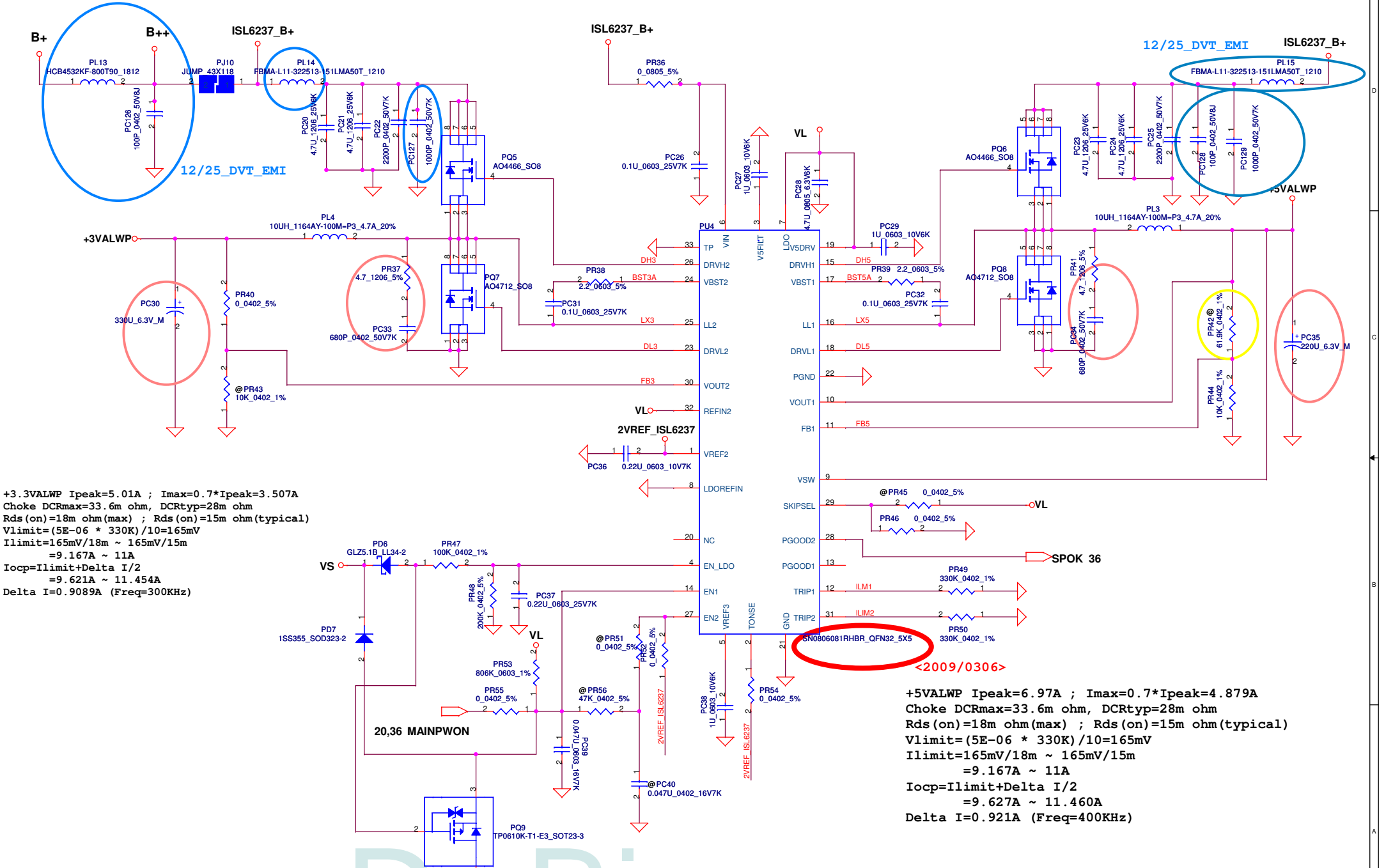
**VMB <38>**



**PQ3 TP0610K-T1-E3\_SOT23-3**



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Size	Document Number	Rev	1.0		
Custom	NAWF3 M/B LA-4854P Schematic	Date:	Wednesday, March 03, 2010	Sheet	36 of 45



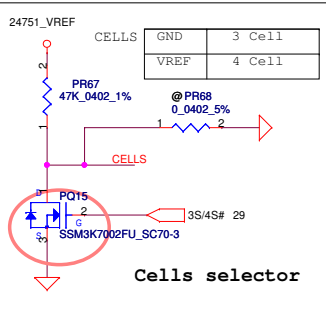
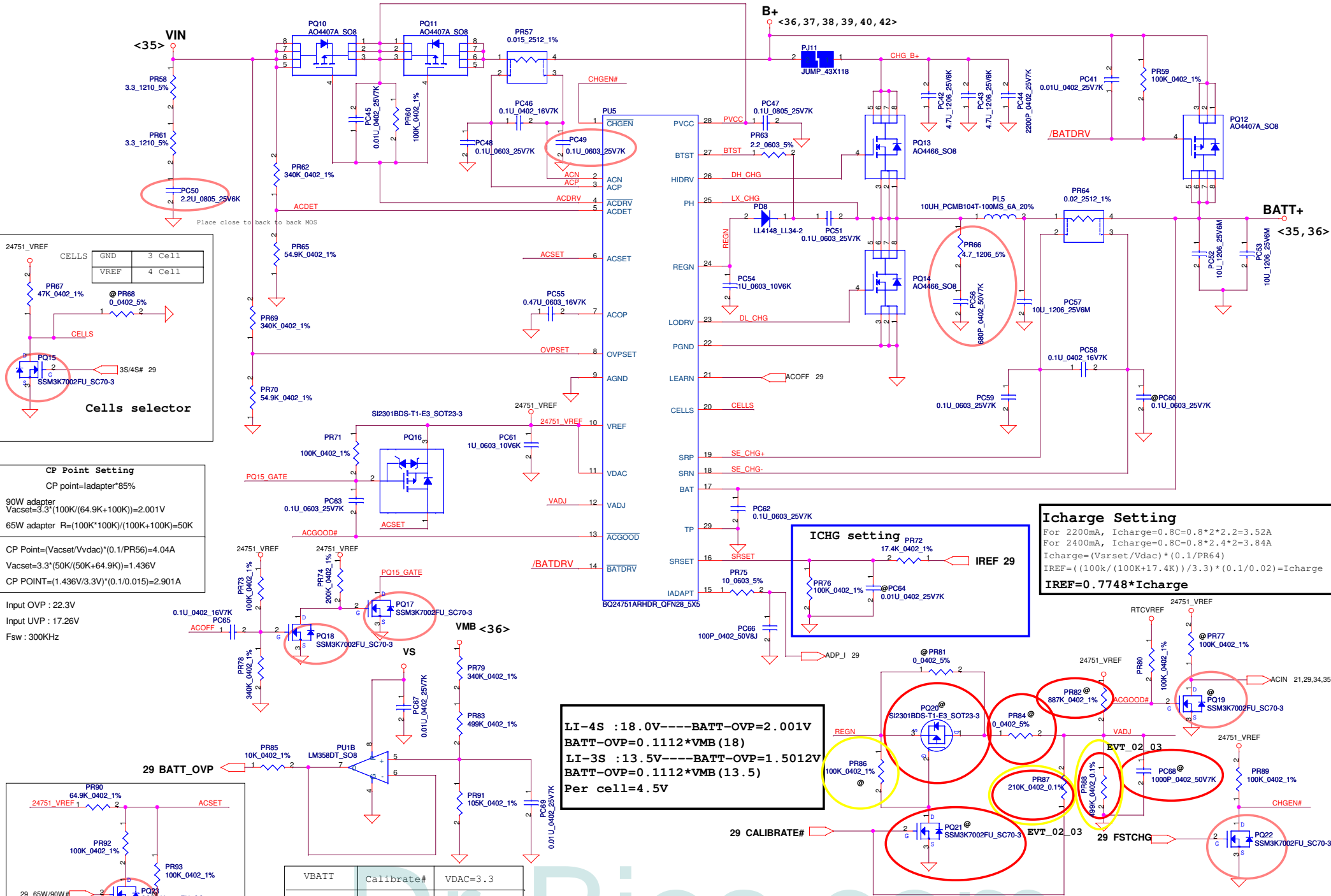
+3.3VALWP Ipeak=5.01A ; Imax=0.7\*Ipeak=3.507A  
 Choke DCRmax=33.6m ohm, DCRtyp=28m ohm  
 Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)  
 Vlimit=(5E-06 \* 330K)/10=165mV  
 Ilimit=165mV/18m ~ 165mV/15m  
 =9.167A ~ 11A  
 Iocp=Ilimit+Delta I/2  
 =9.621A ~ 11.454A  
 Delta I=0.9089A (Freq=300KHz)

20,36 MAINPWON

+5VALWP Ipeak=6.97A ; Imax=0.7\*Ipeak=4.879A  
 Choke DCRmax=33.6m ohm, DCRtyp=28m ohm  
 Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)  
 Vlimit=(5E-06 \* 330K)/10=165mV  
 Ilimit=165mV/18m ~ 165mV/15m  
 =9.167A ~ 11A  
 Iocp=Ilimit+Delta I/2  
 =9.627A ~ 11.460A  
 Delta I=0.921A (Freq=400KHz)

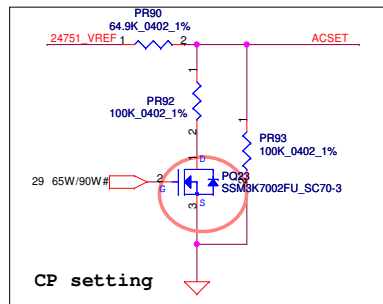
SN0806081RHBR\_QFN32\_5X5  
 <2009/0306>

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Size	Document Number	Date		Rev	
Customer	NAWF3 M/B LA-4854P Schematic	Wednesday, March 03, 2010		1.0	
				Sheet	37 of 45



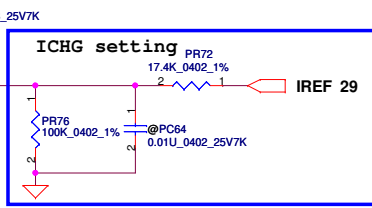
**CP Point Setting**  
 CP point=ladapter\*85%  
 90W adapter  
 $V_{acset} = 3.3 * (100K / (64.9K + 100K)) = 2.001V$   
 65W adapter  $R = (100K * 100K) / (100K + 100K) = 50K$   
 $CP\ Point = (V_{acset} / V_{vdac}) * (0.1 / PR56) = 4.04A$   
 $V_{acset} = 3.3 * (50K / (50K + 64.9K)) = 1.436V$   
 $CP\ POINT = (1.436V / 3.3V) * (0.1 / 0.015) = 2.901A$

Input OVP : 22.3V  
 Input UVP : 17.26V  
 Fsw : 300KHz



VBATT	Calibrate#	VDAC=3.3
4.0V	L=0	
4.2V	1.8755V	
4.3V	2.8132V	
4.35V	H=3.3	

**LI-3S : 18.0V --- BATT-OVP=2.001V**  
**BATT-OVP=0.1112 \* VMB (18)**  
**LI-3S : 13.5V --- BATT-OVP=1.5012V**  
**BATT-OVP=0.1112 \* VMB (13.5)**  
**Per cell=4.5V**



**Icharge Setting**  
 For 2200mA,  $I_{charge} = 0.8C = 0.8 * 2 * 2.2 = 3.52A$   
 For 2400mA,  $I_{charge} = 0.8C = 0.8 * 2.4 * 2 = 3.84A$   
 $I_{charge} = (V_{srset} / V_{dac}) * (0.1 / PR64)$   
 $IREF = (100k / (100K + 17.4K)) / 3.3 * (0.1 / 0.02) = I_{charge}$   
**IREF=0.7748 \* Icharge**

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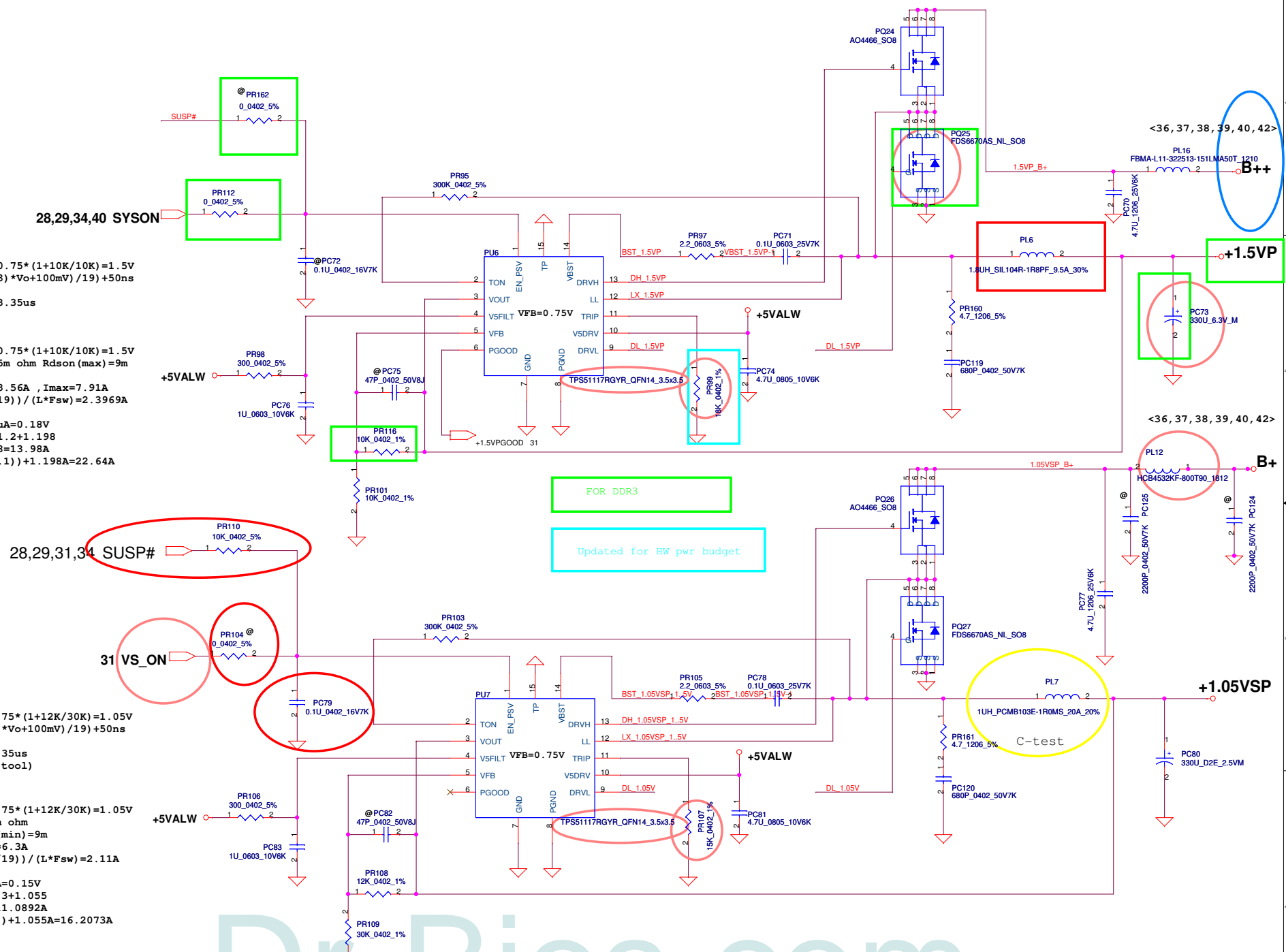
Compal Electronics, Inc.			
<b>CHARGER</b>			
Title	Document Number	Rev	1.0
	<b>NAWF3 M/B LA-4854P Schematic</b>		
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VFB=0.75V  
 $V_o = VFB * (1 + PR116 / PR117) = 0.75 * (1 + 10K / 10K) = 1.5V$   
 $Ton = 19 * e^{-12 * 143000 * ((2/3) * V_o + 100mV) / 19} + 50ns = 2.645e-7 us$   
 $=> V_o / Vin = D = Ton / Ts => Ts = 3.35us$   
 $Fsw = 262KHz$

<Vo=1.5V> VFB=0.75V  
 $V_o = VFB * (1 + PR116 / PR117) = 0.75 * (1 + 10K / 10K) = 1.5V$   
 $Fsw = 262KHz$  Cout ESR=15m ohm Rsdson(max)=9m Rsdson(min)=11.5m  
 $I_{peak} = 1.3A$ ,  $I_{2I_{peak}} = 13.56A$ ,  $I_{max} = 7.91A$   
 $\Delta I = ((19 - 1.5) * (1.5 / 19)) / (L * Fsw) = 2.3969A$   
 $=> 1/2 \Delta I = 1.198A$   
 $V_{trip} = R_{trip} * I_{0uA} = 18K * 10uA = 0.18V$   
 $I_{ocpmin} = V_{trip} / R_{sdsonmax} * 1.2 + 1.198 = 0.075 / (0.018 * 1.3) + 1.198 = 13.98A$   
 $I_{ocpmax} = (0.075 / (0.015 * 1.1)) + 1.198A = 22.64A$   
 $I_{ocp} = 13.98 \sim 22.64A$

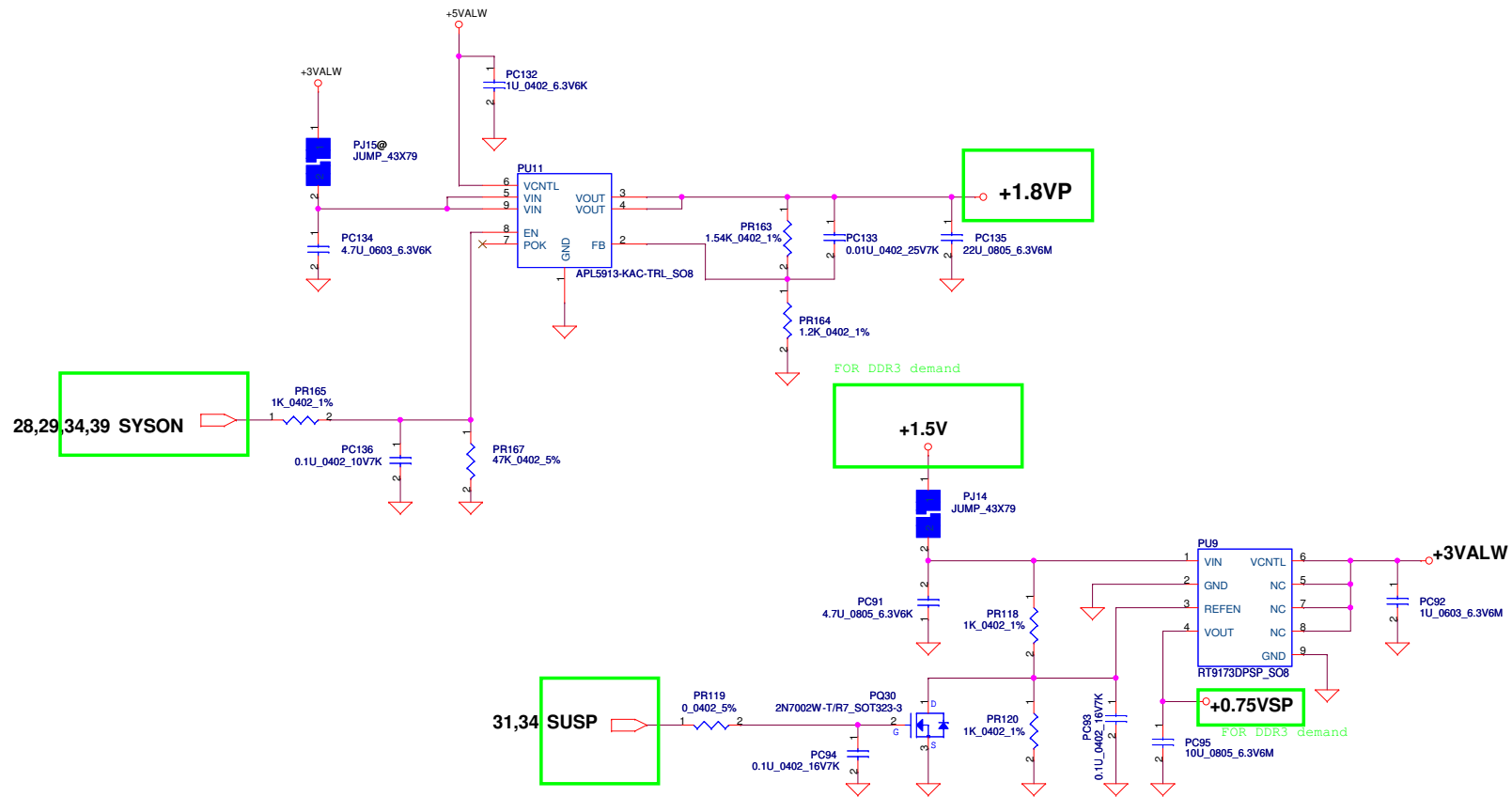
VFB=0.75V  
 $V_o = VFB * (1 + PR108 / PR109) = 0.75 * (1 + 12K / 30K) = 1.05V$   
 $Ton = 19 * e^{-12 * 143000 * ((2/3) * V_o + 100mV) / 19} + 50ns = 2.645e-7 us$   
 $=> V_o / Vin = D = Ton / Ts => Ts = 3.35us$   
 $Fsw = 261KHz$  (by caculation tool)

<Vo=1.05V> VFB=0.75V  
 $V_o = VFB * (1 + PR108 / PR109) = 0.75 * (1 + 12K / 30K) = 1.05V$   
 $Fsw = 261KHz$  Cout ESR=15m ohm Rsdson(max.)=11.5m Rsdson(min)=9m  
 $I_{peak} = 9A$ ,  $I_{max} = I_{peak} * 0.7 = 6.3A$   
 $\Delta I = ((19 - 1.05) * (1.05 / 19)) / (L * Fsw) = 2.11A$   
 $=> 1/2 \Delta I = 1.055A$   
 $V_{trip} = R_{trip} * I_{0uA} = 15K * 10uA = 0.15V$   
 $I_{ocpmin} = V_{trip} / R_{sdsonmax} * 1.3 + 1.055 = 0.15 / (0.011 * 1.3) + 1.055 = 11.0892A$   
 $I_{ocpmax} = (0.15 / (0.009 * 1.1)) + 1.055A = 16.2073A$   
 $I_{ocp} = 11.0892A \sim 16.2073A$



FOR DDR3  
 Updated for HW pwr budget

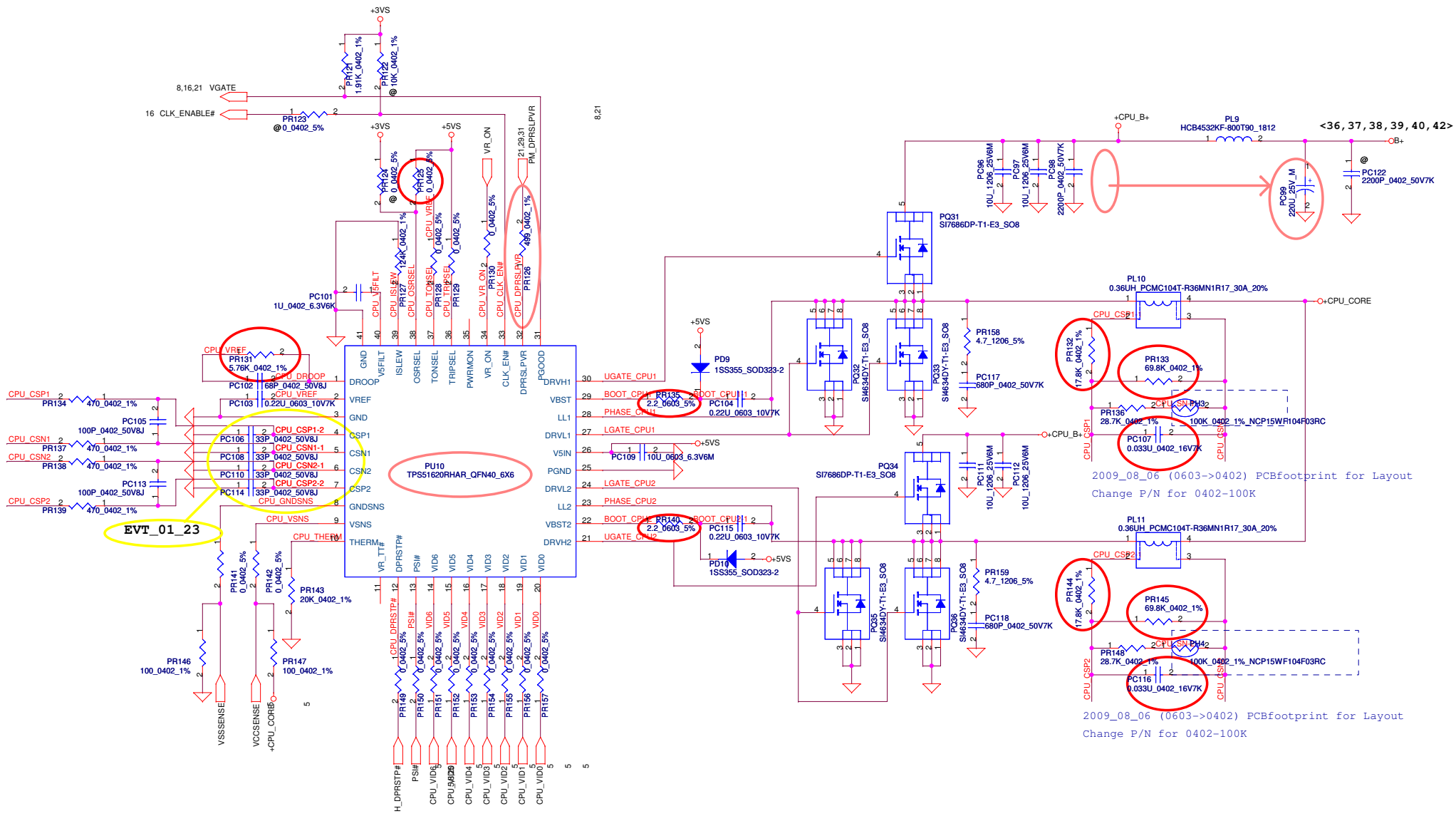
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				+1.5VP	
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				+CPU CORE
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	NAWF3 M/B LA-4854P Schematic		1.0	
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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		Add PC57 :10U_1206_25V_6M	0.1	38	Add PC57 :10U_1206_25V_6M	20080902	EVT
2		Add snubber for EMI	0.1	42	Add snubber for EMI	20080915	EVT
3		Shift PC99 from +cpu_B+ to B+	0.1	42	Shift PC99 from +cpu_B+ to B+	20080915	EVT
4		Add PJ15 to B+	0.1	39	Add PJ15 to B+	20080915	EVT
5		PR135 and PR140 change to 0_0603_5%	0.1	42	PR135 and PR140 change to 0_0603_5%	20080915	EVT
6	Charger feedback trace too long	ADD PC49	0.2	38	ADD PC49	20081124	DVT
7	Power sequence error	+1.5VP: enable pin change from SUSP# to SYSON +0.9VSP: enable pin change from SUSP# to SUSP	0.2	40	+1.5VP: enable pin change from SUSP# to SYSON +0.9VSP: enable pin change from SUSP# to SUSP	20081124	DVT
8	Load line over spec	PR131: change to 5.76K_0402_1%	0.2	42	PR131: change to 5.76K_0402_1%	20081124	DVT
9	3D hang	Charger PR63:change to 2.2_0603_5% PR66:Add 4.7_1206_5% PC56:Add 680P_0402_50V7K	0.2	38	Charger PR63:change to 2.2_0603_5% PR66:Add 4.7_1206_5% PC56:Add 680P_0402_50V7K	20081124	DVT
10	3D hang	+1.8VP PR97:change to 2.2_0603_5% PR160:Add 4.7_1206_5% PC119:Add 680P_0402_50V7K	0.2	39	+1.8VP PR97:change to 2.2_0603_5% PR160:Add 4.7_1206_5% PC119:Add 680P_0402_50V7K	20081124	DVT
11	3D hang	+1.05VSP PR105:change to 2.2_0603_5% PR161:Add 4.7_1206_5% PC120:Add 680P_0402_50V7K Add bead between B+ and 1.05VSP_B+	0.2	39	+1.05VSP PR105:change to 2.2_0603_5% PR161:Add 4.7_1206_5% PC120:Add 680P_0402_50V7K Add bead between B+ and 1.05VSP_B+	20081124	DVT
12	EMI solution	+5VALW/+3VALW PR37: Add 4.7_1206_5% PR41: Add 4.7_1206_5% PC33: Add 680P_0402_50V7K PC34: Add 680P_0402_50V7K PR38: change to 2.2_0603_5% PR39: change to 2.2_0603_5%	0.2	37	+5VALW/+3VALW PR37: Add 4.7_1206_5% PR41: Add 4.7_1206_5% PC33: Add 680P_0402_50V7K PC34: Add 680P_0402_50V7K PR38: change to 2.2_0603_5% PR39: change to 2.2_0603_5%	20081124	DVT
13	EMI solution	+CPU CORE PR158: Add 4.7_1206_5% PR159: Add 4.7_1206_5% PC117: Add 680P_0402_50V7K PC118: Add 680P_0402_50V7K PR135: change to 2.2_0603_5% PR140: change to 2.2_0603_5%	0.2	42	+CPU CORE PR158: Add 4.7_1206_5% PR159: Add 4.7_1206_5% PC117: Add 680P_0402_50V7K PC118: Add 680P_0402_50V7K PR135: change to 2.2_0603_5% PR140: change to 2.2_0603_5%	20081124	DVT
16	EMI solution	+CPU CORE PC122: Reserve 2200P_0402_50V7K on B+	0.2	42	+CPU CORE PC122: Reserve 2200P_0402_50V7K on B+	20081124	DVT
17	EMI solution	+1.05VSP PR105 : change to 2.2_0603_5% PL12 : Add HCB4532KF-800T90_1812 PC124: Reserve 2200P_0402_50V7K on B+ PC125: Reserve 2200P_0402_50V7K on B+	0.2	39	+1.05VSP PR105 : change to 2.2_0603_5% PL12 : Add HCB4532KF-800T90_1812 PC124: Reserve 2200P_0402_50V7K on B+ PC125: Reserve 2200P_0402_50V7K on B+	20081124	DVT

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
18	Battery & HW solution	Charger PQ20:Reserve(@)SI2301BDS-T1-E3_SOT23-3 PQ21:Reserve(@)SSM3K7002FU_SC70-3 PR82:Reserve(@)887K_0402_1% PR84:Reserve(@)0_0402_5% PC68:Reserve(@)1000P_0402_50V7K PR87:change to 210K_0402_1% PR88:change to 499K_0402_1%  +1.05VSP PR104: Reserve(@)0_0402_5% PR110: change to 10K_0402_5% PR79 : Add 0.1U_0402_16V7K  +1.5VP PR112: Reserve(@) 0_0402_5%	0.2	38 39 40	Charger PQ20:Reserve(@)SI2301BDS-T1-E3_SOT23-3 PQ21:Reserve(@)SSM3K7002FU_SC70-3 PR82:Reserve(@)887K_0402_1% PR84:Reserve(@)0_0402_5% PC68:Reserve(@)1000P_0402_50V7K PR87:change to 210K_0402_1% PR88:change to 499K_0402_1%  +1.05VSP PR104: Reserve(@)0_0402_5% PR110: change to 10K_0402_5% PR79 : Add 0.1U_0402_16V7K  +1.5VP PR112: Reserve(@) 0_0402_5%	20081124	DVT
19	EMI soultion	+3VALWP/+3VALW PC100: 680P_0402_50V7K PC130: 1000P_0402_50V_7K PC131: 1000P_0402_50V_8J +1.5VP ADD PR113: 2.2_0603_5% ADD PR163: 4.7_1206_5% ADD PC121: 680P_0402_50V7K ADD PL16 :FBMA-L11-322513-151LMA50T_1210	0.3	35 40	+3VALWP/+3VALW PC100: 680P_0402_50V7K PC130: 1000P_0402_50V_7K PC131: 1000P_0402_50V_8J +1.5VP ADD PR113: 2.2_0603_5% ADD PR163: 4.7_1206_5% ADD PC121: 680P_0402_50V7K ADD PL16 :FBMA-L11-322513-151LMA50T_1210	20081224	PVT
20	POWER Solution	+3VALWP/+5VALWP  RT8206- Fix output 5V for HW no HDMI	0.3	37	+3VALWP/+5VALWP PR42: Reserve 61.9K_0402_1%	20090111	PVT

COMPAL ELECTRONICS			
Title PIR POWER2			
Size	Document Number	Rev	
	KAWF0 M/B LA-4431P Schematic	0.2	
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Item	Fixed Issue	Reason for change	Rev	PG#	Modify List	Date	Phase
21	EMI solution	Reduce the Noise	0.3	37	Add PL 13 ( HCB4532KF-800T90_1812) Add PL 14 ( FBMA-L11-322513-151LMA50T_1210) Add PL 15 ( FBMA-L11-322513-151LMA50T_1210) Add PC126 ( 100P_0402_50V8J) Add PC128 ( 100P_0402_50V8J) Add PC129 ( 1000P_0402_50V7K)	20090112	PVT
22	Battery solution	Adjust battery voltage	0.3	38	Reserve PR86 ( 100K_0402_1%)	20090112	PVT
23	Saturation current	1.8u choke saturation current too small	0.3	39	change PL7 to 1UH_PCMB103E-1R0MS_20A_20%	20090113	PVT
24	GP BOM	Tolerance: K:+-10% ; J:+-5%	0.4	42	Change PC106 to 33P_0402_50V8J Change PC108 to 33P_0402_50V8J Change PC110 to 33P_0402_50V8J Change PC114 to 33P_0402_50V8J	20090123	PVT



COMPAL ELECTRONICS			
Title		<Title> PIR POWER3	
Size	Document Number	Rev	
A	KAWF0 M/B LA-4431P Schematic	0.2	
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**09/01 Change DDR2 as DDR3 PIR**

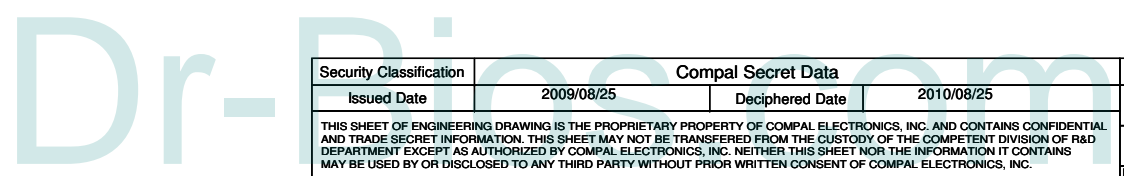
1. P.8 Remove R181 ; Stuff R220, R222 ; Unstuff R221
2. P.14 Remove RP28, RP27, RP19, RP18, RP10, RP9, RP3, RP25, RP26, RP17, RP16, RP8, RP7, R138, R200, R195, R350, R351  
Remove C148, C186, C185, C134, C202, C415, C412, C413, C414, C187, C149, C146,C183, C188, C147, C203, C150, C135  
Remove C201, C204, C184, C200, C285, C411, C410  
Change JDIMM2 P/N  
Add R598~R602 ; C887~C908
3. P.15 Remove RP30, RP24, RP23, RP15, RP14, RP6, RP2, RP22, RP21, RP13, RP12, RP5, RP1, R137, R52, R53  
Remove C283, C284, C197, C181, C143, C198, C144, C182, C210, C180, C142, C131, C212, C133, C179  
Remove C211, C196, C199, C132, C209, C141, C140, C178, C145  
Change JDIMM1 P/N  
Add R603~R605 ; C909~C930
4. P.31 Add R608, R607, R606, C931, C932, D33, U42, Q57
5. P.34 Unstuff R244, R253, Q13 ; Stuff C309, C313, C310, C314, R266, R267, Q43, Q44, U12, R265, Q17

**09/01 Other PIR**

1. P.17 Unstuff D20, R411 ; Add R611 for DISPOFF#
2. P.19 Unstuff U8, R83 ; Add R614 for PLT\_RST#
3. P.21 Add U43 ; Remove R75 for ICH\_VGATE
4. P.23 Unstuff C570
5. P.30 Change LED1, LED2 P/N
6. P.32 Add D34, R613 for Audio BEEP#

**09/17**

1. P.25 Change C81, C82 27pF as 33pF for Xtal 25MHz(TXC suggest value)
2. P.20 Change C163, C164 18pF as 15pF for Xtal 32.768kHz (TXC suggest value)
3. P.29 Change R273 8.2k ohm as 18k ohm for Board ID



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