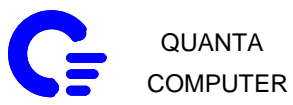


MODEL	REV	CHANGE LIST	Model		
			Page	ZL8	MB
				FM	TO
ZL9	1A	Preliminary Release	1	1A	
	2A	<p>Page 4 : Add C573 4.7pf for Signal quanlity</p> <p>Page 6 : Add R460 0om for UMA.</p> <p>Page 11 : seprate SATALED# for IDE interrupt.</p> <p>Page 14 :add R45 0ohm for M52-T.</p> <p>Page 19 : enlarge H22,H23 to 6mm for VGA sink Nut.</p> <p>Page 24 : Add 459 10Kohm for keep the GPIO normal Low.</p> <p>Page 25 : Add R239 0ohm for Po Po sound.</p> <p>Page 27 : Add R458 , Q25 for SATALED#.</p> <p>Page 28 : PL14->0.6uH,PR122->680ohm,PR120->680ohm,PR118->470ohm,PC55->220P,PR38->160K for power efficiency.</p> <p>Page 30 : PR40->20K,PD11->CH551,PC39->.22U,PC46->2.2n,PL11->1.5UH,PR59->221K for power efficiency.</p> <p>Page 30 : PC176->1000P,PC182->1000P,PC179->1000P,PC180->100P,PC181->100P,PC177->1000P for EMI.</p> <p>Page 31 : PR142->0 , PR94->100K,PR95->0,PR93->100K for battery charger modify ,PC178->1000P for EMI.</p> <p>Page 32 : PR15->6.65K , PL6->1.0UH for power efficiency.</p>	2	1A	
			3	1A	
			4	2A	
			5	1A	
			6	2A	
			7	1A	
			8	1A	
			9	1A	
			10	1A	
			11	2A	
			12	1A	
			13	1A	
			14	2A	
			15	1A	
			16	1A	
			17	1A	
			18	1A	
			19	2A	
			20	2A	
			21	1A	
	22	1A			
	23	1A			
	24	2A			
	25	2A	3A		
	26	1A			
	27	2A	3A		
	28	2A			
	29	1A			
	30	2A			
	31	2A			
	32	2A			
3A	<p>Page 25 : R250->100Kohm, Q13->2N7002,Q23->2N7002,Add Q24 AO3403 for SPDIF on/off LED.</p> <p>Page 27 :Del R458 , Q25 for HDD LED can't light issue.</p>				



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ZL9

CPU CORE
SENTECH
SC4511TSTR
 Page: 28

SYSTEM 3V/5V
MAXIM
MAX1999
 +3VPCU
 +3V_S5/+3VSUS
 +3V
 +5VPCU
 +5VSUS
 +5V
 +15V
 Page: 29

+1.8VSUS
 +1.8V
 +0.9VSUS
 +0.9V ON NCP5214
 +1.5V SENTECH SC1470
 +1.5V_S5 SI9183-AD
 +2.5V SENTECH SC1565
 +1.05V SENTECH SC4215
 Page: 30
 +1.2V SENTECH SC4215
 +NVVDD SENTECH SC1470
 Page: 32

BATTERY CHARGER
MAXIM
MAX8724
 Page: 31

CLOCK GEN
ICS954206
(RTM865T-433)
 Page: 4

CELERON-M/PENTIUM-M
 INTEL Mobile_479 CPU
 Page: 2, 3

DDR-II SODIMM1
 Page: 10

DDR-II SODIMM2
 Page: 10

NB
INTEL
ALVISO 915PM/GM
 Page: 5, 6, 7, 8

ATi
M52-T
 Page: 14, 15, 16, 17

CRT
 Page: 19

LVDS
 Page: 19

SATA HDD
 Page: 20

PATA HDD
 Page: 20

IDE-ODD
 Page: 20

SB
INTEL
ICH6-M
 Page: 11, 12, 13

MINI-PCIE slot
Wireless LAN
 (Option)
 Page: 21

TI PCMCIA
PCI1510
 AD17
 REQ1# / GNT1#
 INTC#
 Page: 23

TYPE II
SLOT
 Page: 23

AUDIO CODEC
Realtek
ALC883 (ALC260)
 Page: 24

AMP
MAX9755
 Page: 25

MODEM
 Page: 24

KBC
NS
PC97551/541V
 Page: 26

MIC IN
 Page: 24

SPEAKER
 Page: 25

LINE OUT
 Page: 25

RJ11
 Page: 22

Touchpad
 Page: 27

Keyboard
 Page: 27

FLASH
 Page: 26

FAN
 Page: 27

SYSTEM
USB PORT *3
USB2, 3, 5
 Page: 21

Bluetooth
USB interface
USB4
 Page: 21

MINI-PCI
Wireless LAN
AD20
 REQ2# / GNT2#
 INTB# , INTD#
 Page: 21

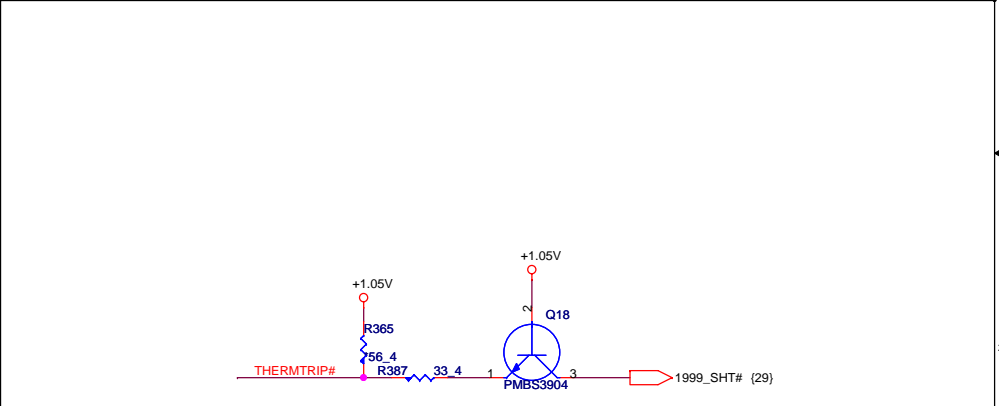
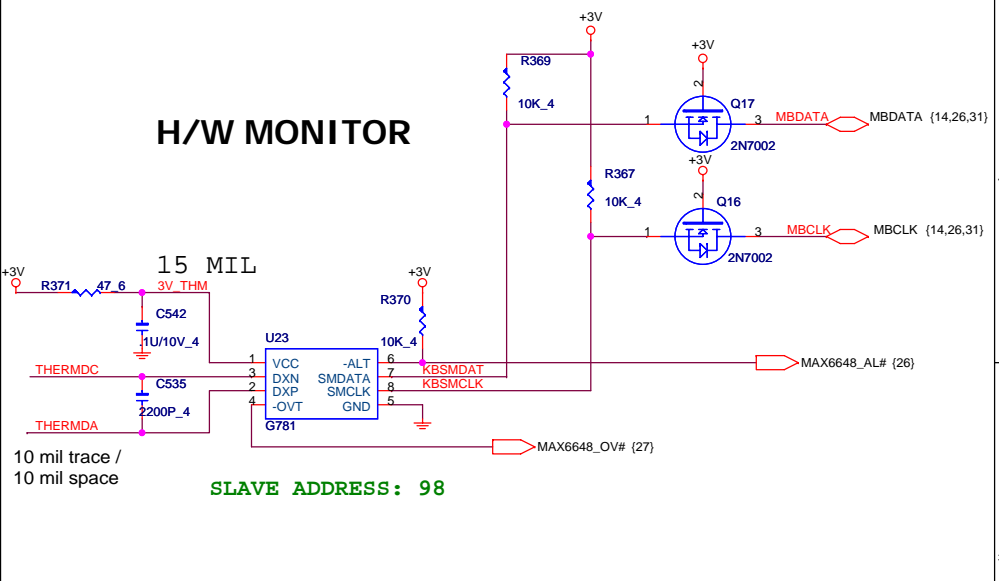
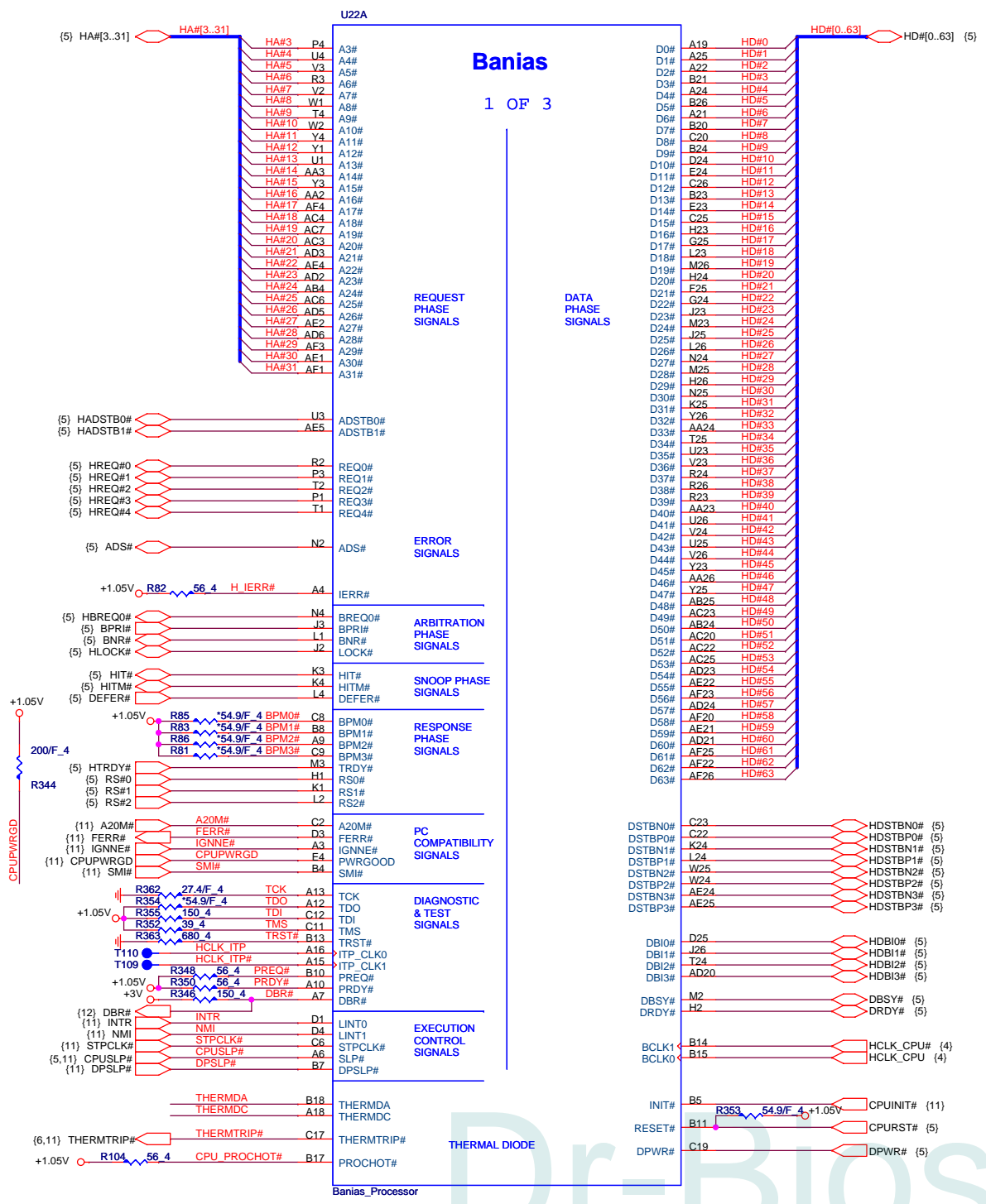
REALTEK
RTL8100CL
AD24
 REQ0# / GNT0#
 INTA#
 Page: 22

RJ45
 Page: 22

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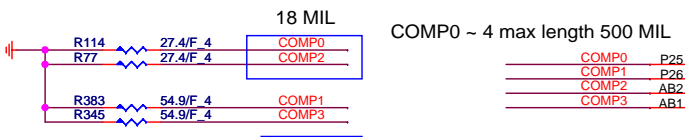
PROJECT : ZL9
Quanta Computer Inc.

Size	Document Number	Rev
	BLOCK DIAGRAM	3A
Date:	Monday, December 19, 2005	Sheet 1 of 32



PROJECT : ZL9
Quanta Computer Inc.

Size	Document Number	Rev
	CPU (HOST BUS)-1	3A
Date:	Monday, December 19, 2005	Sheet 2 of 32



18 MIL

COMP0 ~ 4 max length 500 MIL

GTLREF0

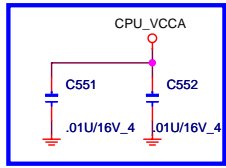
0.5" max

6.5 MIL

(11) DPRSLP#

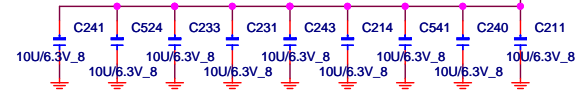
A0 : STUFF

A1 : NC

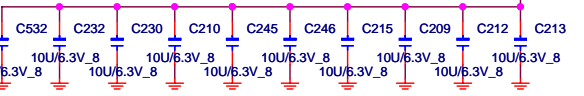


PLACE one 10U & one 0.01U for each VCCA pin

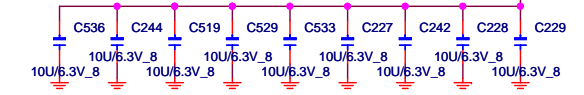
10U/6.3V/X5R(CC0805) *30



VCC_CORE



VCC_CORE



VCC_CORE

COMP0	P25	A2	VSS	A5	VCCP0	W23	VSS
COMP1	P26	A8	VSS	A6	VCCP1	W26	VSS
COMP2	AB2	A11	VSS	A9	VCCP2	Y2	VSS
COMP3	AB1	A14	VSS	A10	VCCP3	Y5	VSS
		A17	VSS	A13	VCCP4	Y24	VSS
		A20	VSS	A16	VCCP5	AA1	VSS
		A23	VSS	A19	VCCP6	AA4	VSS
		A26	VSS	A22	VCCP7	AA6	VSS
		B3	VSS	A25	VCCP8	AA8	VSS
		B6	VSS	A28	VCCP9	AA10	VSS
		B9	VSS	A31	VCCP10	AA12	VSS
		B12	VSS	A34	VCCP11	AA14	VSS
		B15	VSS	A37	VCCP12	AA16	VSS
		B18	VSS	A40	VCCP13	AA18	VSS
		B21	VSS	A43	VCCP14	AA20	VSS
		B24	VSS	A46	VCCP15	AA22	VSS
		B27	VSS	A49	VCCP16	AA25	VSS
		C1	VSS	A52	VCCP17	AB3	VSS
		C4	VSS	A55	VCCP18	AB5	VSS
		C7	VSS	A58	VCCP19	AB7	VSS
		C10	VSS	A61	VCCP20	AB9	VSS
		C13	VSS	A64	VCCP21	AB11	VSS
		C15	VSS	A67	VCCP22	AB13	VSS
		C18	VSS	A70	VCCP23	AB15	VSS
		C21	VSS	A73	VCCP24	AB17	VSS
		C24	VSS	A76	VCCP25	AB19	VSS
		D2	VSS	A79	VCCP26	AB21	VSS
		D5	VSS	A82		AB23	VSS
		D7	VSS	A85		AB26	VSS
		D9	VSS	A88		AC2	VSS
		D11	VSS	A91		AC5	VSS
		D13	VSS	A94		AC8	VSS
		D15	VSS	A97		AC10	VSS
		D17	VSS	A100		AC12	VSS
		D19	VSS	A103		AC14	VSS
		D21	VSS	A106		AC16	VSS
		D23	VSS	A109		AC18	VSS
		D26	VSS	A112		AC21	VSS
		E3	VSS	A115		AC24	VSS
		E6	VSS	A118		AD1	VSS
		E8	VSS	A121		AD4	VSS
		E10	VSS	A124		AD7	VSS
		E12	VSS	A127		AD9	VSS
		E14	VSS	A130		AD11	VSS
		E16	VSS	A133		AD13	VSS
		E18	VSS	A136		AD15	VSS
		E20	VSS	A139		AD17	VSS
		E22	VSS	A142		AD19	VSS
		E25	VSS	A145		AD22	VSS
		F1	VSS	A148		AD25	VSS
		F4	VSS	A151		AE3	VSS
		F5	VSS	A154		AE6	VSS
		F7	VSS	A157		AE8	VSS
		F9	VSS	A160		AE10	VSS
		F11	VSS	A163		AE12	VSS
		F13	VSS	A166		AE14	VSS
		F15	VSS	A169		AE16	VSS
		F17	VSS	A172		AE18	VSS
		F19	VSS	A175		AE20	VSS
		F21	VSS	A178		AE23	VSS
		F24	VSS	A181		AE26	VSS
		G2	VSS	A184		AF2	VSS
		G6	VSS	A187		AF5	VSS
		G22	VSS	A190		AF9	VSS
		G23	VSS	A193		AF11	VSS
		G26	VSS	A196		AF13	VSS
		H3	VSS	A199		AF15	VSS
		H5	VSS	A202		AF16	VSS
		H6	VSS	A205		AF17	VSS
		H21	VSS	A208		AF19	VSS
		H25	VSS	A211		AF21	VSS
		J1	VSS	A214		AF24	VSS
		J4	VSS	A217			
		J6	VSS	A220			
		J22	VSS	A223			
		J24	VSS	A226			
		K2	VSS	A229			
		K5	VSS	A232			
		K6	VSS	A235			
		K21	VSS	A238			
		K23	VSS	A241			
		K26	VSS	A244			
		L3	VSS	A247			
		L6	VSS	A250			
		L22	VSS	A253			
		L25	VSS	A256			
		M1	VSS	A259			
		M4	VSS	A262			
		M5	VSS	A265			
		M6	VSS	A268			
		M21	VSS	A271			
		M24	VSS	A274			
		N3	VSS	A277			
		N6	VSS	A280			
		N22	VSS	A283			
		N23	VSS	A286			
		N26	VSS	A289			
		P2	VSS	A292			
		P5	VSS	A295			
		P21	VSS	A298			
		P24	VSS	A301			
		R1	VSS	A304			
		R4	VSS	A307			
		VCC71	VSS	A310			

Banias

2 OF 3

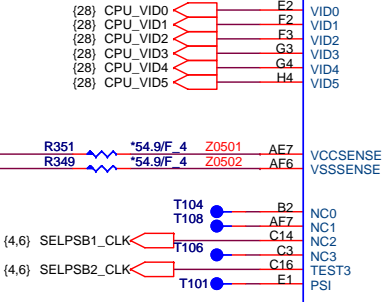
POWER, GROUND, RESERVED SIGNALS

Banias

3 OF 3

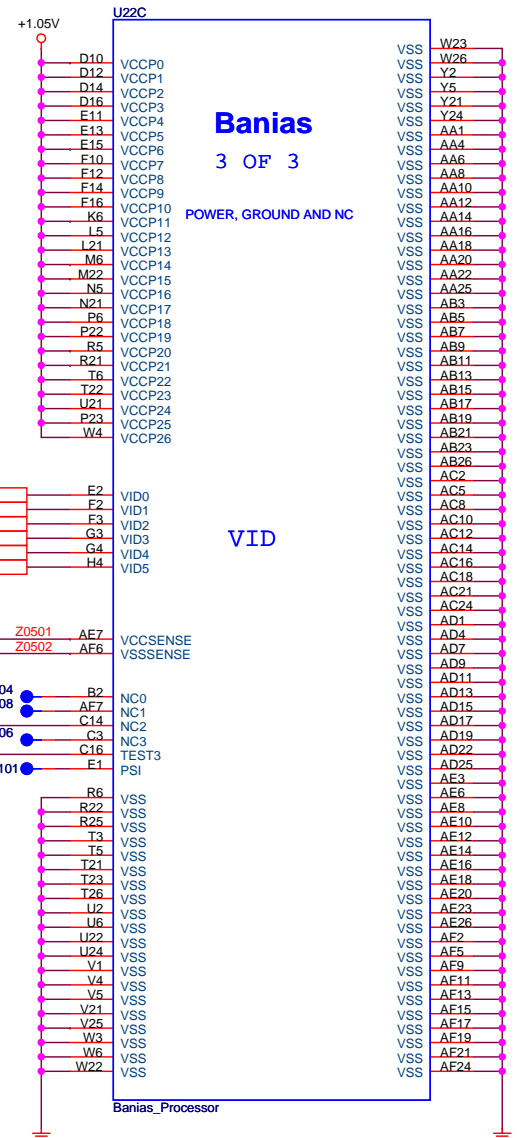
POWER, GROUND AND NC

VID

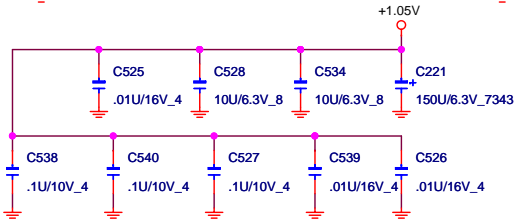


(28) CPU_VID0
(28) CPU_VID1
(28) CPU_VID2
(28) CPU_VID3
(28) CPU_VID4
(28) CPU_VID5

(4,6) SELPSB1_CLK
(4,6) SELPSB2_CLK



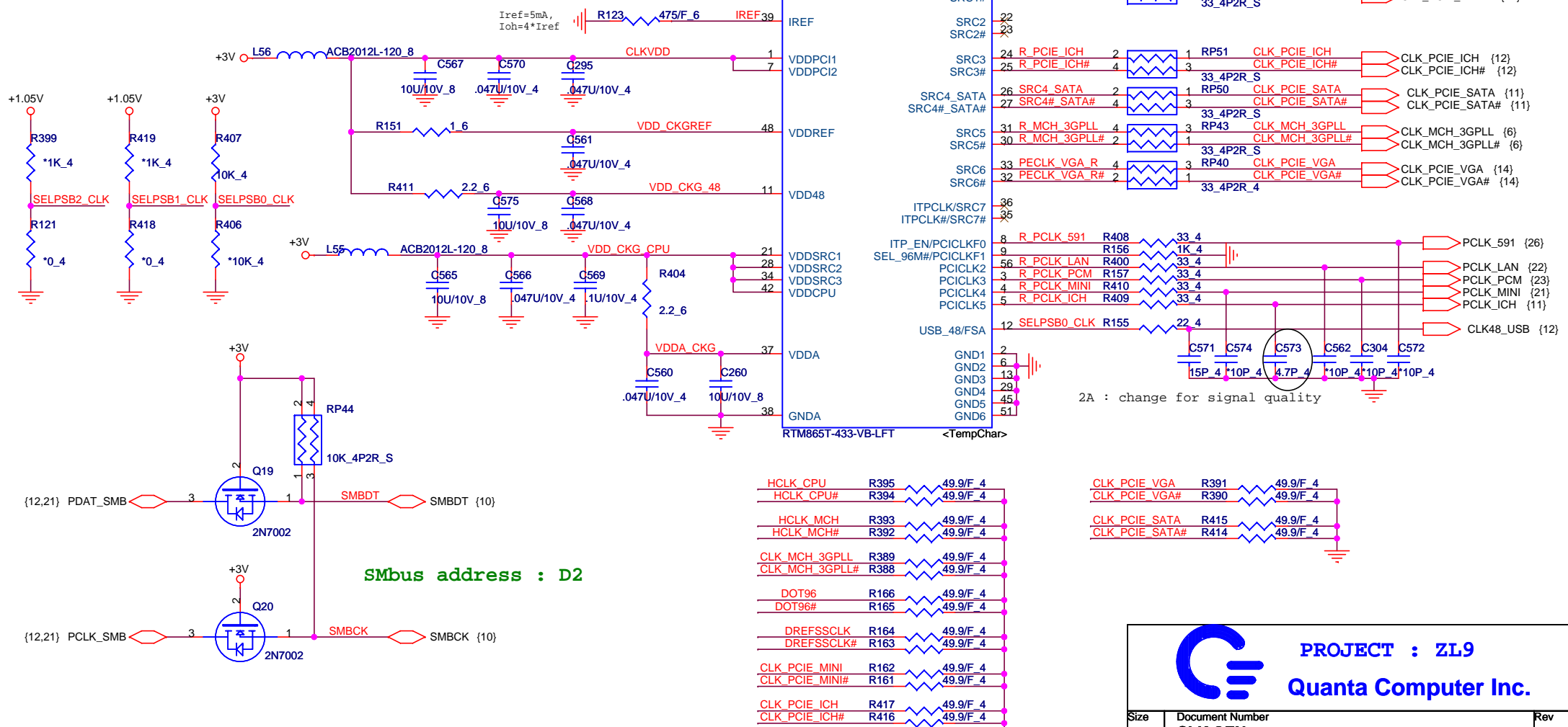
Banias_Processor



PROJECT : ZL9
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FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

DOTHAN-A 400
DOTHAN-A 533



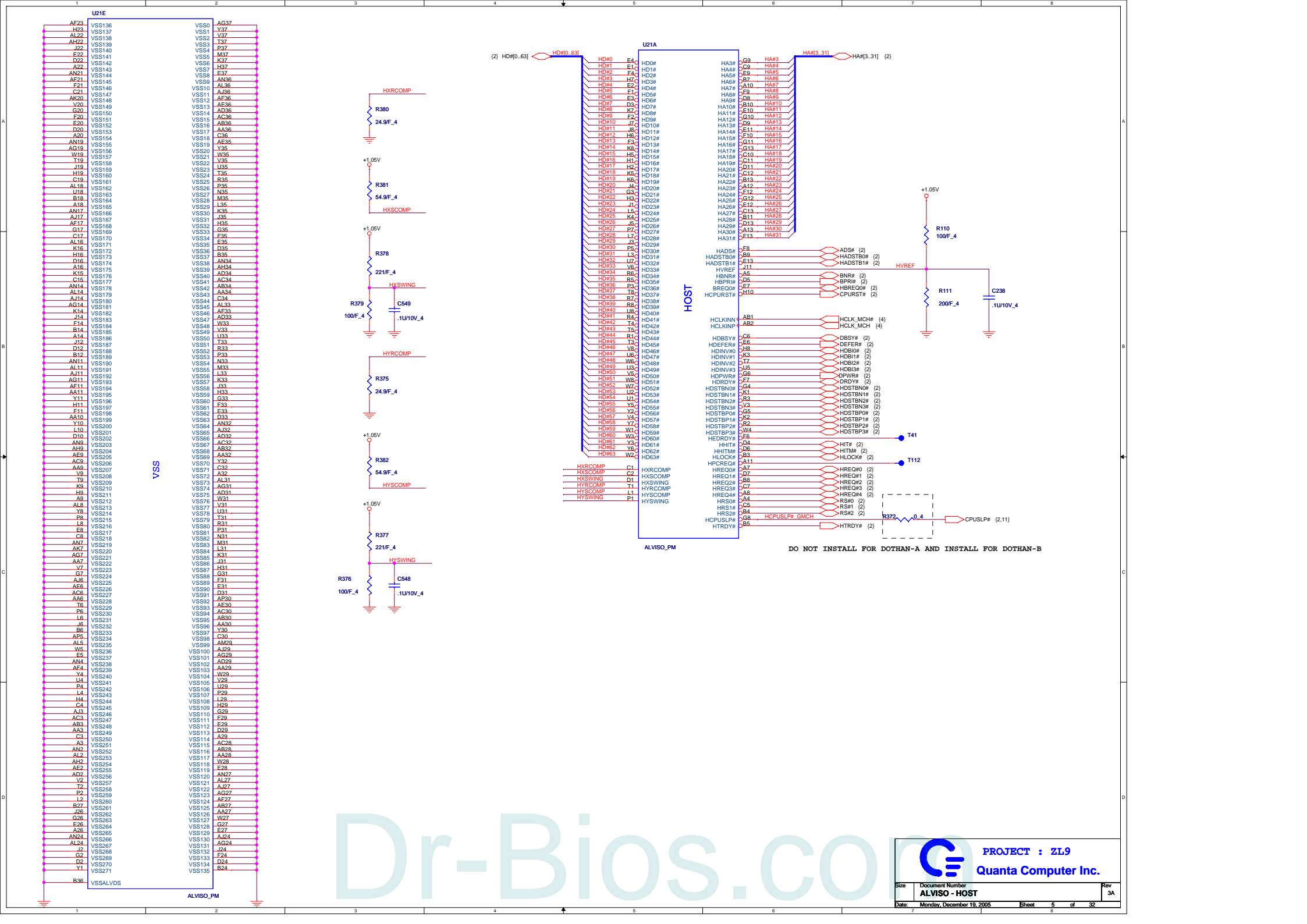
SMBus address : D2

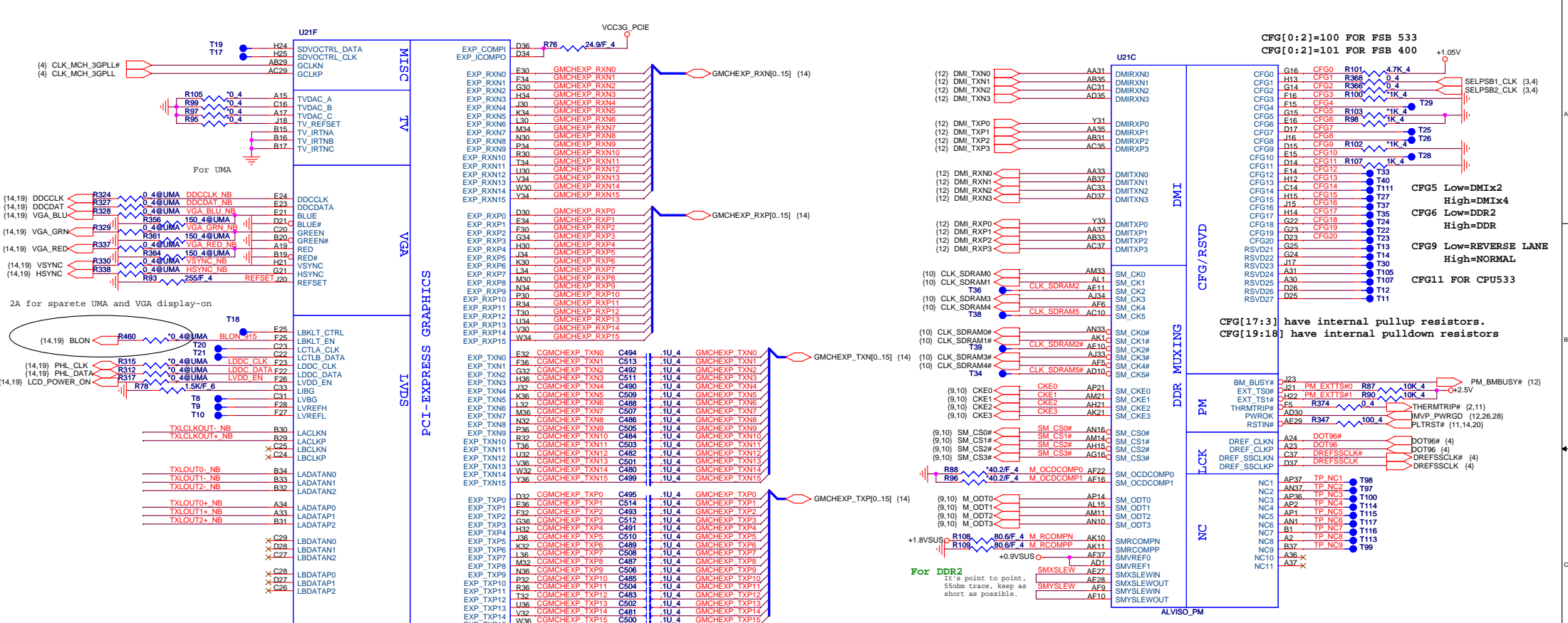
- HCLK_CPU R395 49.9/F 4
- HCLK_CPU# R394 49.9/F 4
- HCLK_MCH R393 49.9/F 4
- HCLK_MCH# R392 49.9/F 4
- CLK_MCH_3GPLL R389 49.9/F 4
- CLK_MCH_3GPLL# R388 49.9/F 4
- DOT96 R166 49.9/F 4
- DOT96# R165 49.9/F 4
- DREFSSCLK R164 49.9/F 4
- DREFSSCLK# R163 49.9/F 4
- CLK_PCIE_MINI R162 49.9/F 4
- CLK_PCIE_MINI# R161 49.9/F 4
- CLK_PCIE_ICH R417 49.9/F 4
- CLK_PCIE_ICH# R416 49.9/F 4

- CLK_PCIE_VGA R391 49.9/F 4
- CLK_PCIE_VGA# R390 49.9/F 4
- CLK_PCIE_SATA R415 49.9/F 4
- CLK_PCIE_SATA# R414 49.9/F 4

PROJECT : ZL9
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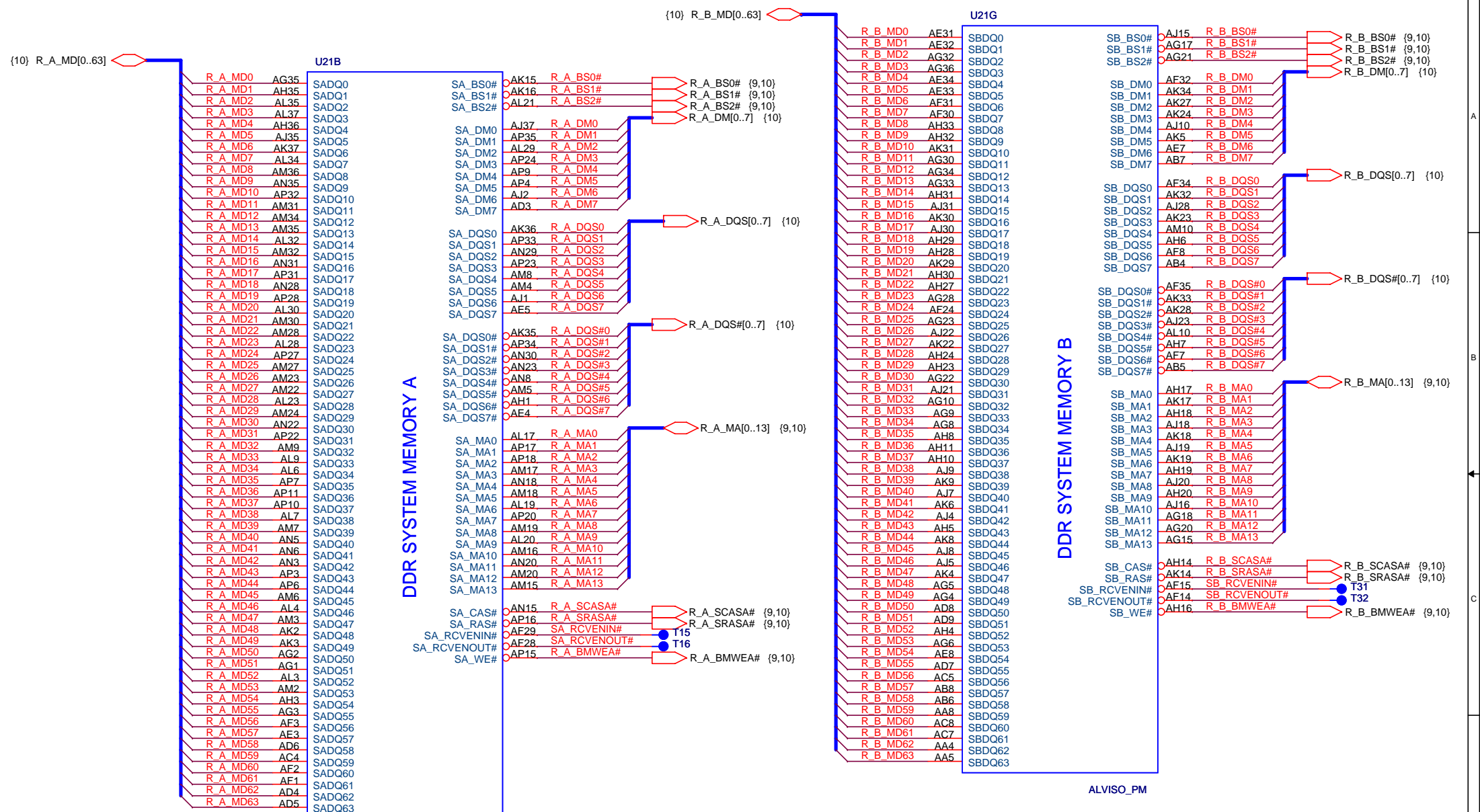
Size	Document Number	Rev
	CLK GEN	3A
Date:	Monday, December 19, 2005	Sheet 4 of 32





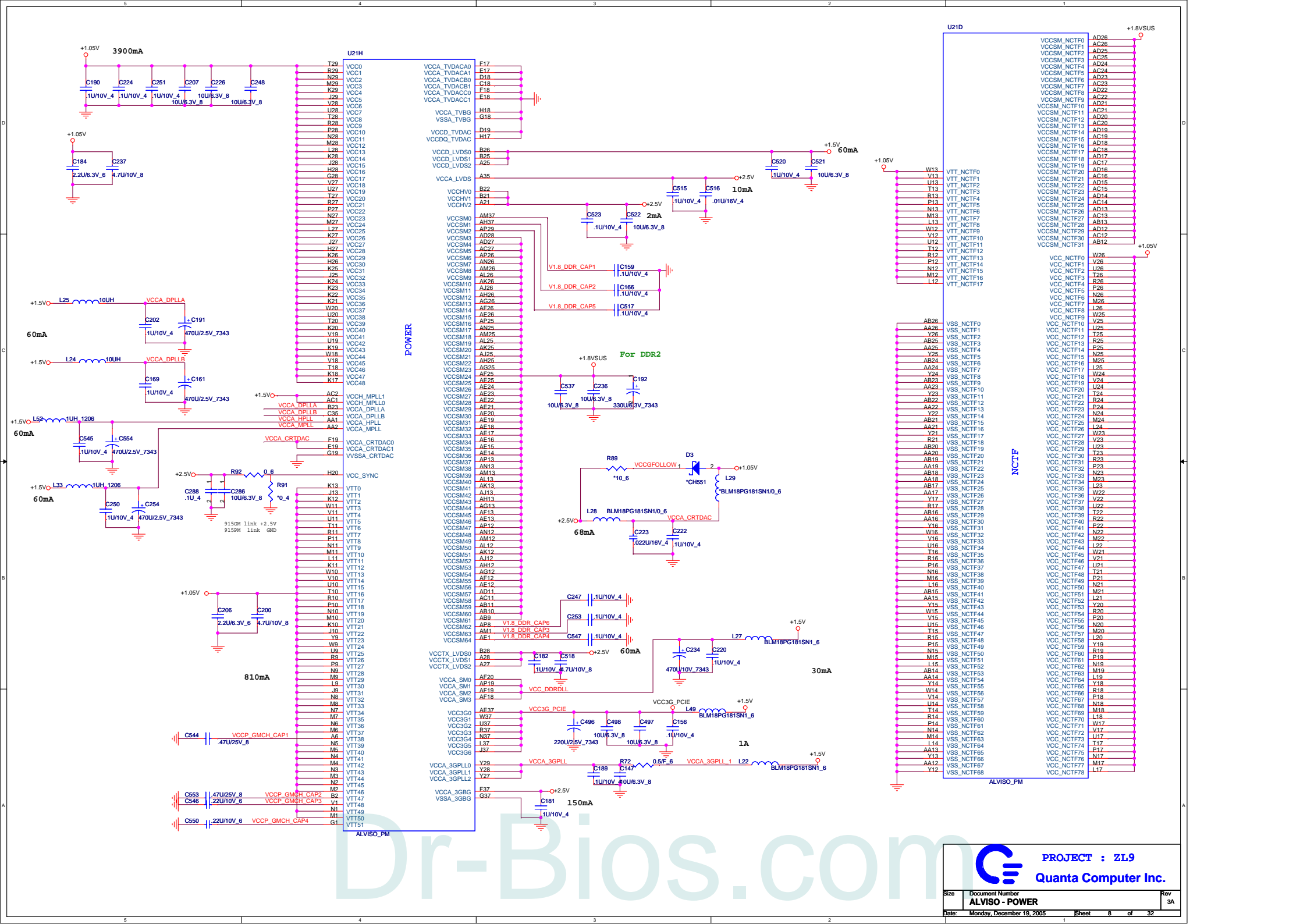
PROJECT : ZL9
Quanta Computer Inc.

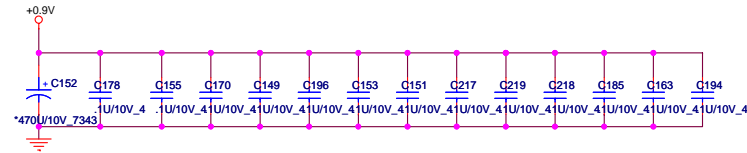
Size	Document Number	Rev
	ALVISO - DMI / VGA	3A
Date:	Monday, December 19, 2005	Sheet 6 of 32



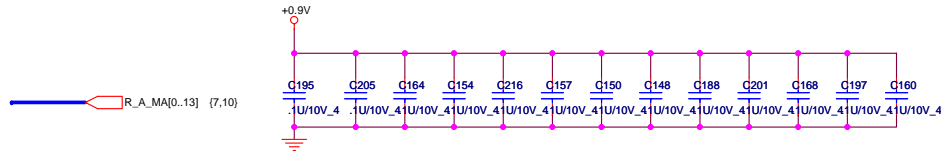
PROJECT : ZL9
Quanta Computer Inc.

Size	Document Number ALVISO - DDRII	Rev 3A
Date:	Monday, December 19, 2005	Sheet 7 of 32

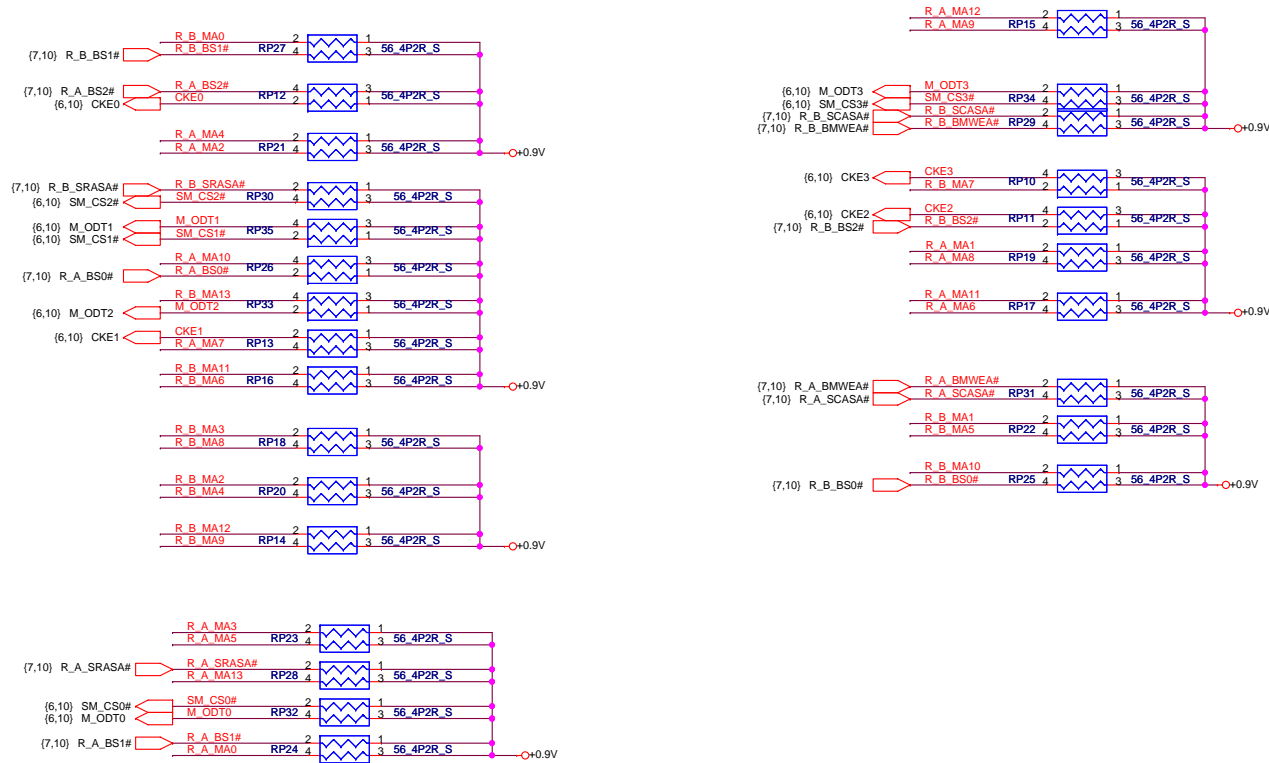




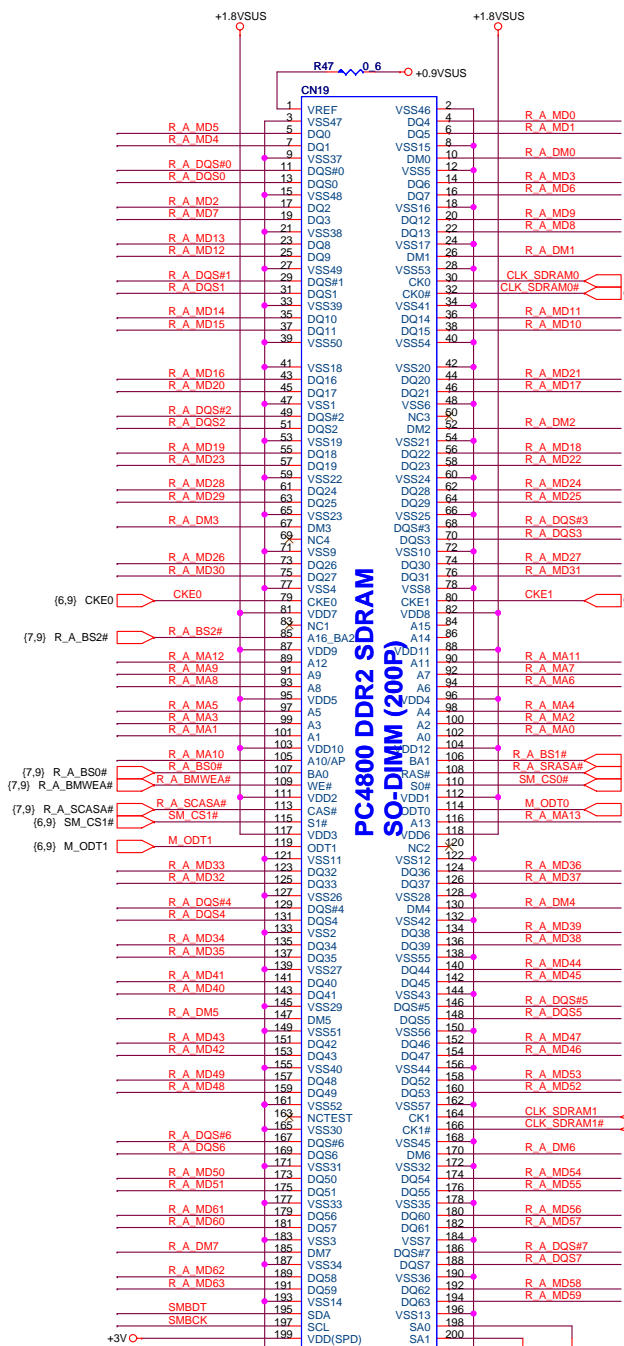
Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9V



Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9V

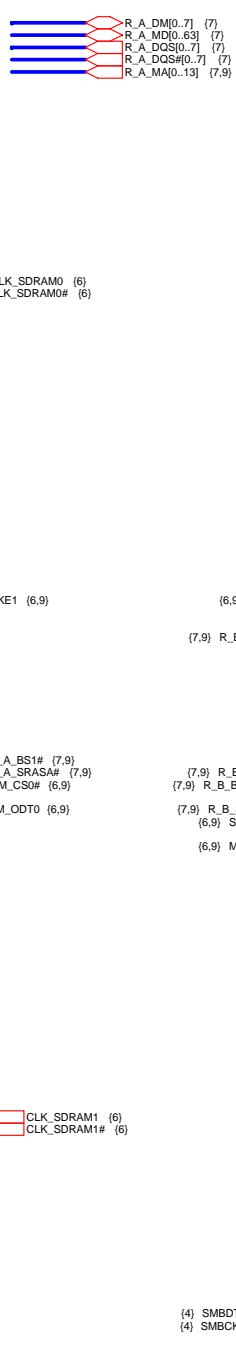


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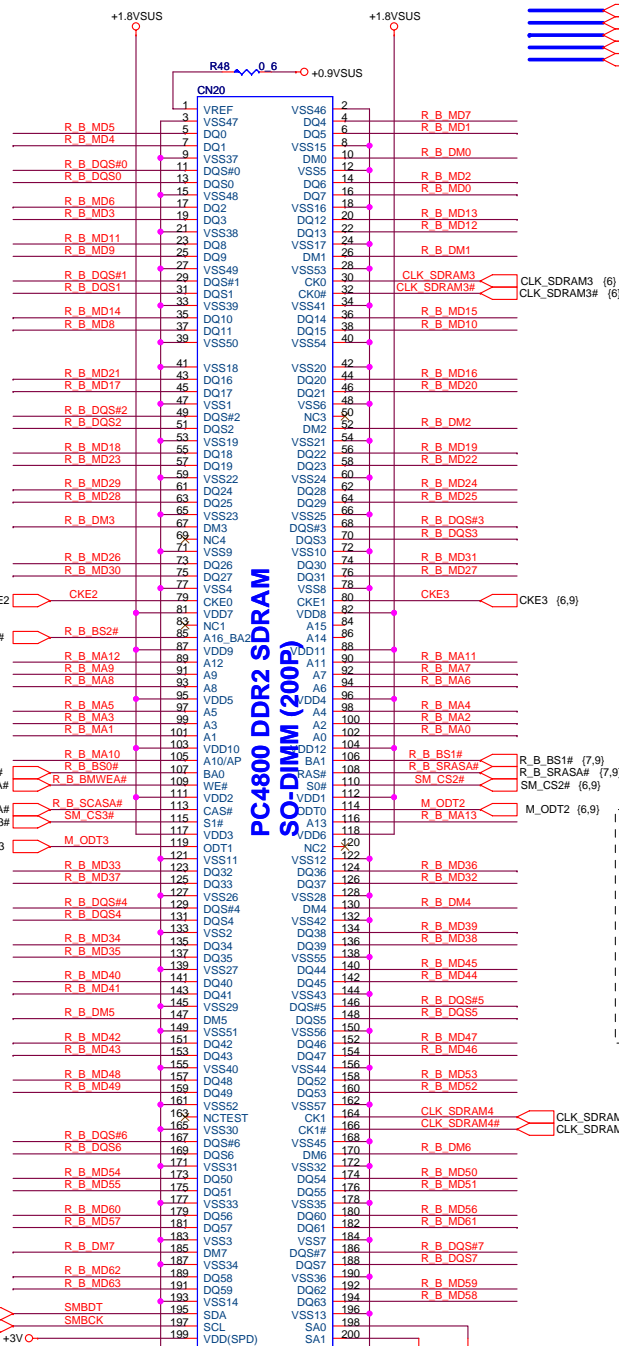
**PC4800 DDR2 SDRAM
SO-DIMM (200P)**

SMBus address A0
PC4800_DDR2_4.0MM_STD
**CLOCK 0,1,2
CKE 0,1**



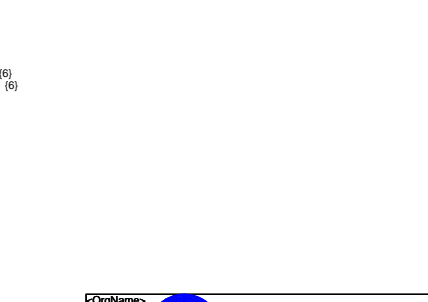
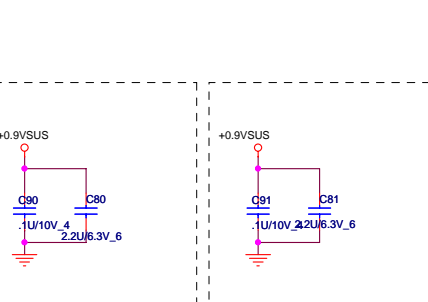
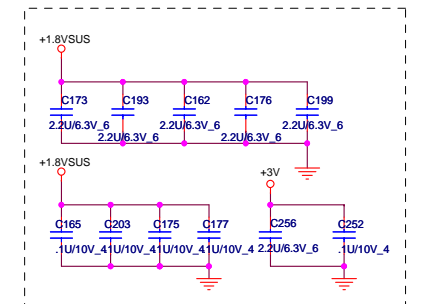
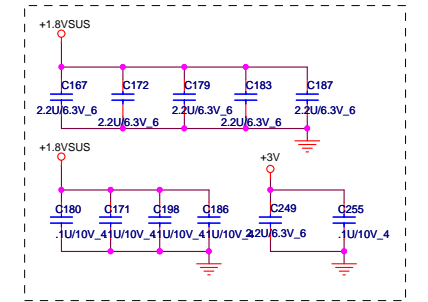
**PC4800 DDR2 SDRAM
SO-DIMM (200P)**

SMBus address A1
PC4800_DDR2_8.0MM_STD
**CLOCK 3,4,5
CKE 2,3**



**PC4800 DDR2 SDRAM
SO-DIMM (200P)**

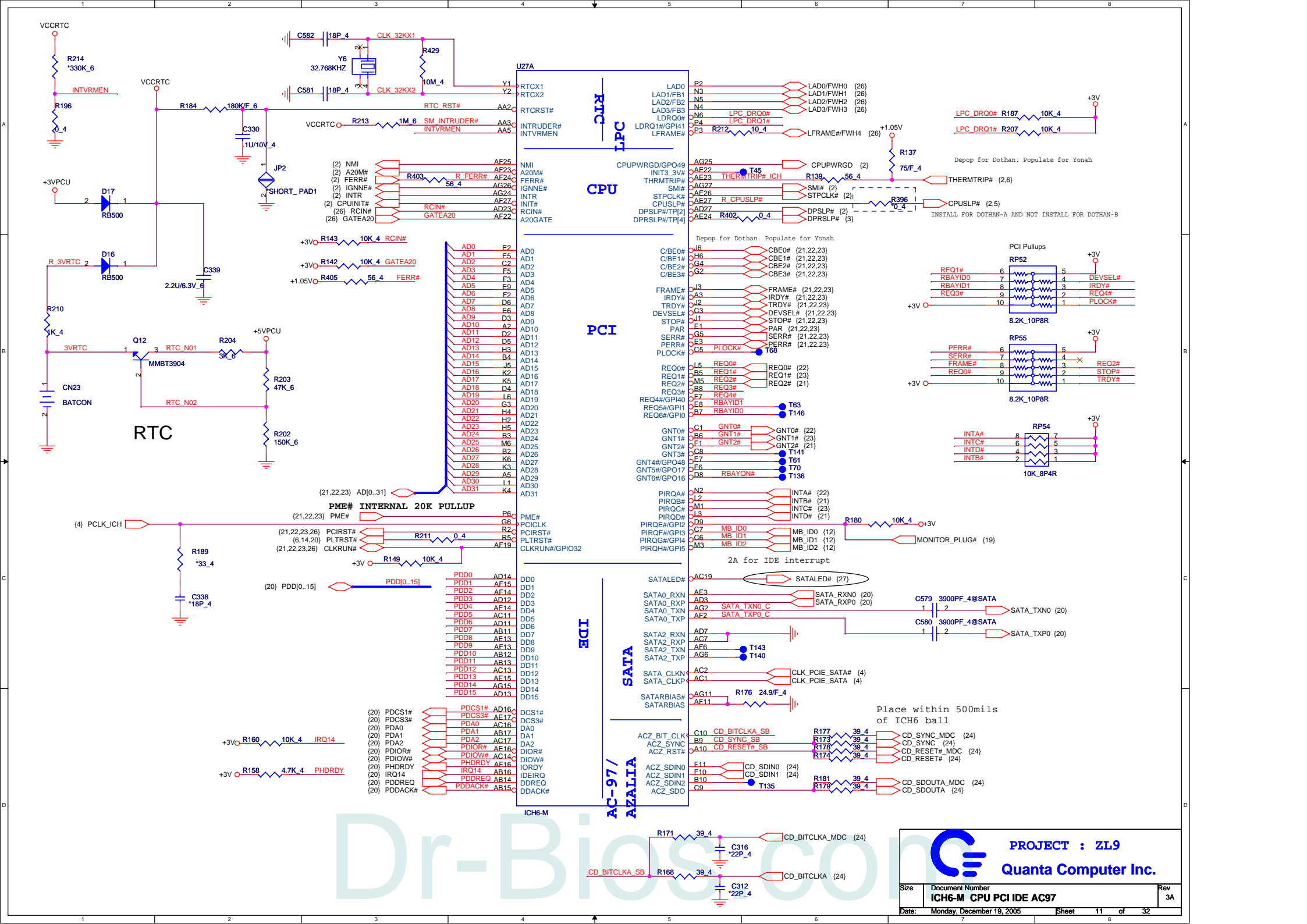
SMBus address A2
PC4800_DDR2_8.0MM_STD
**CLOCK 6,7,8
CKE 4,5,6**

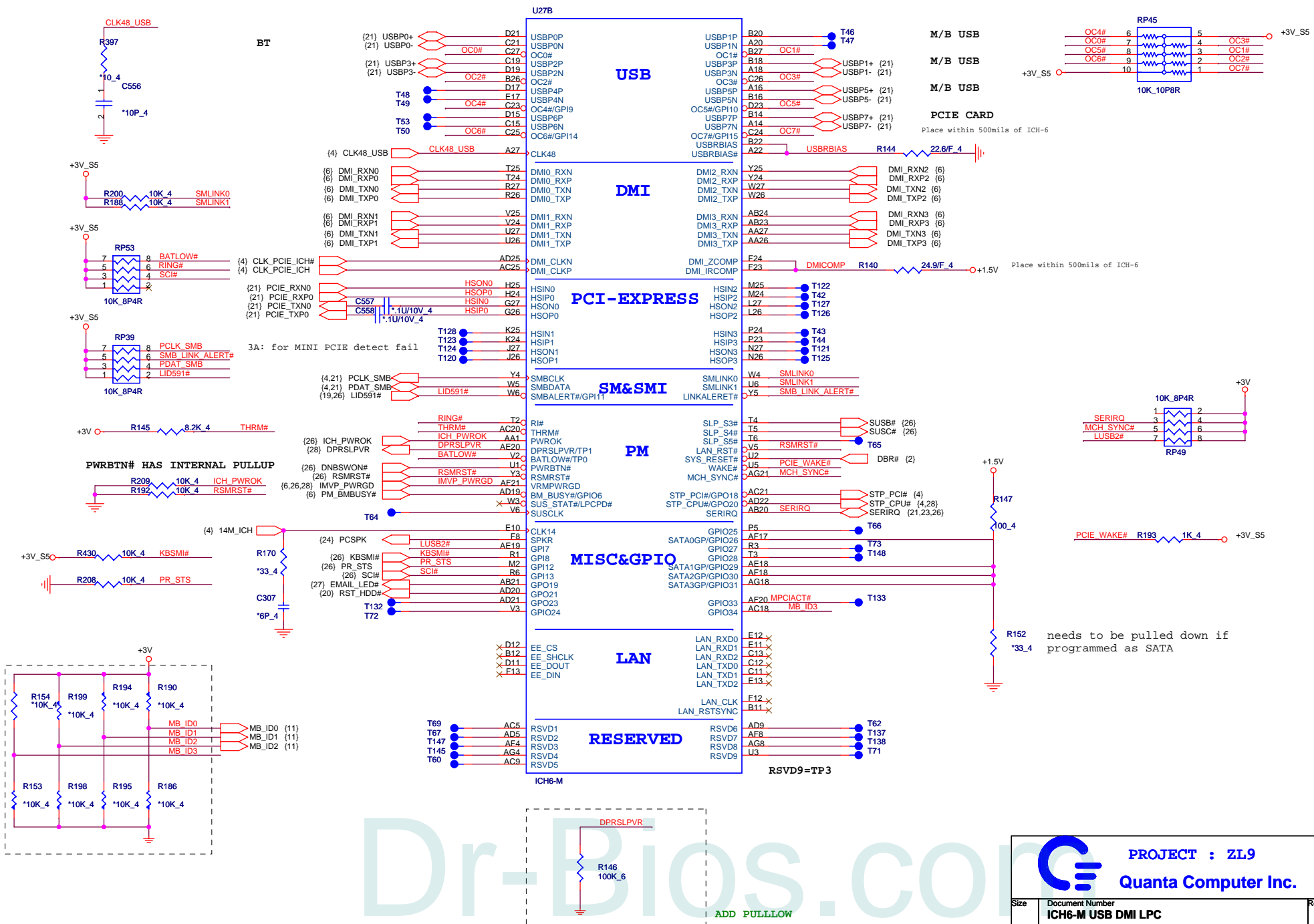


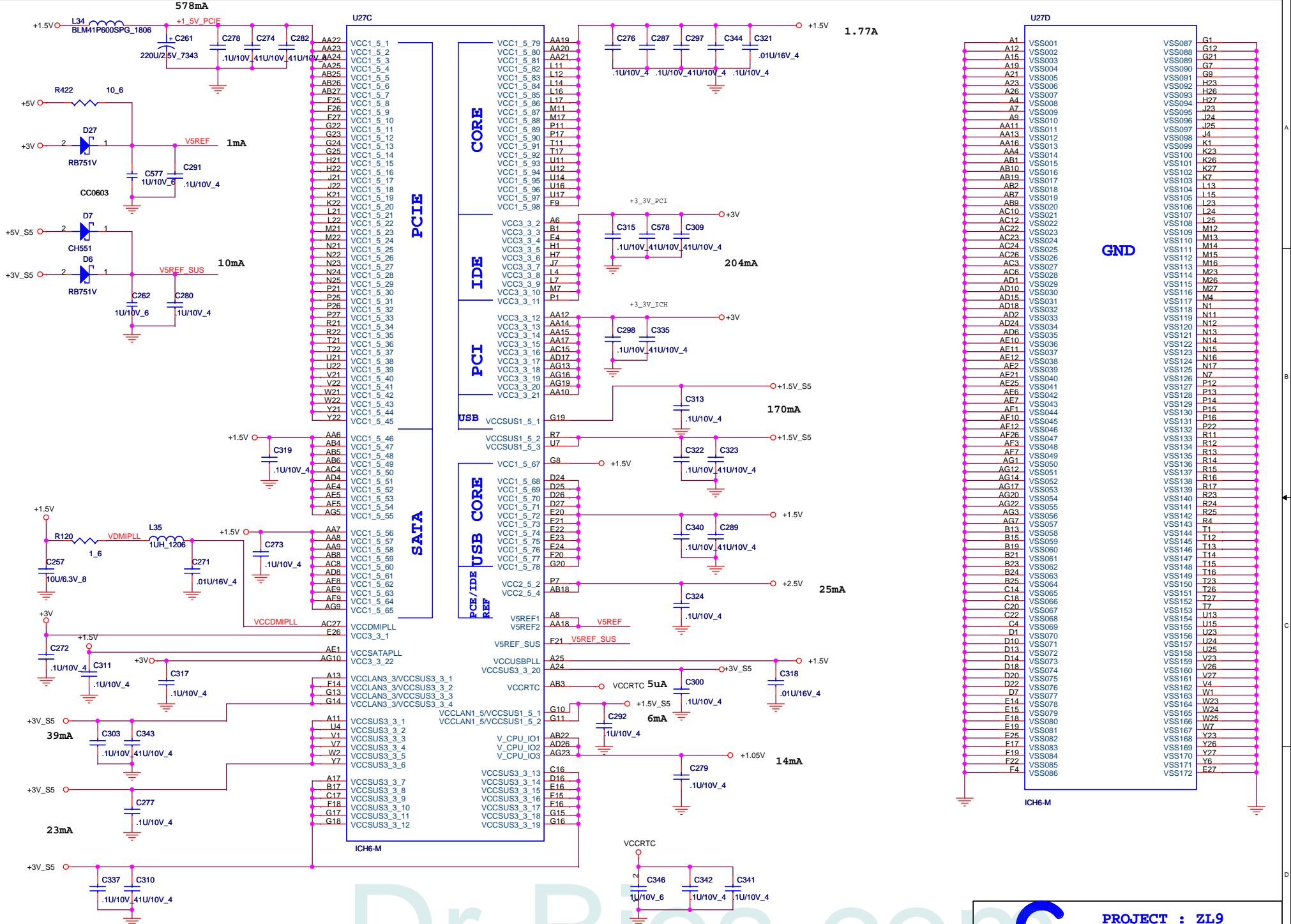
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 <OrgAddr1>
 <OrgAddr2>
 <OrgAddr3>
 <OrgAddr4>

PROJECT : ZL9
Quanta Computer Inc.

Size	Document Number	Rev
	DDR2 SO-DIMM (200P)	3A
Date:	Monday, December 19, 2005	Sheet 10 of 32

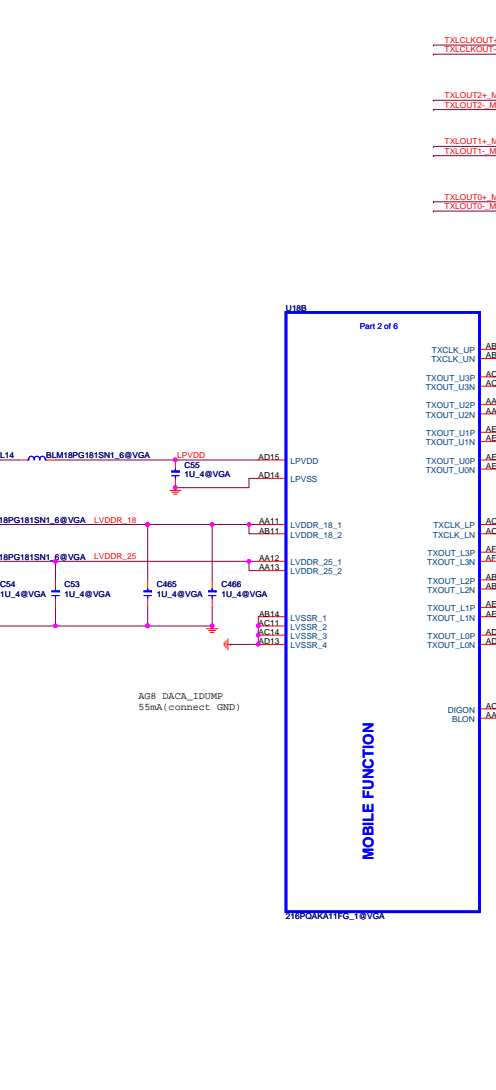
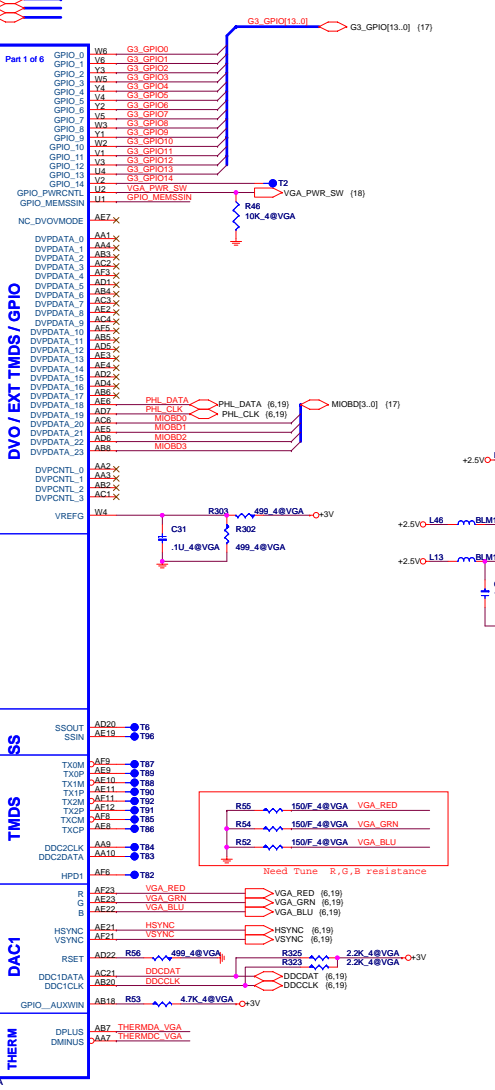
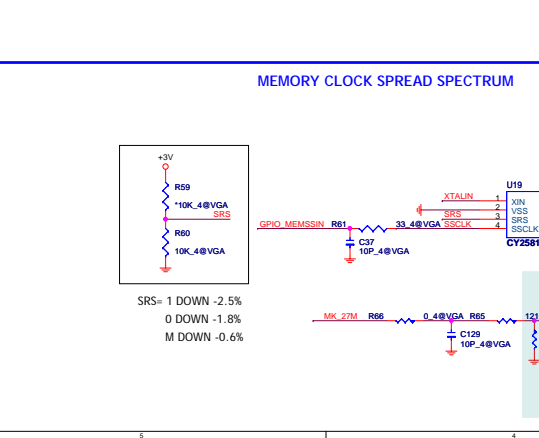
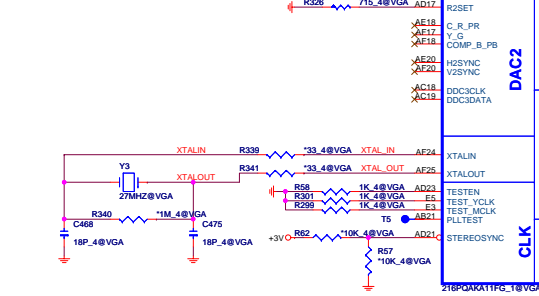
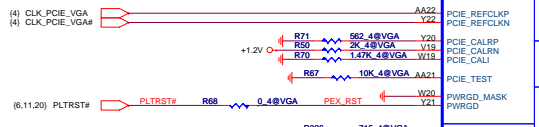
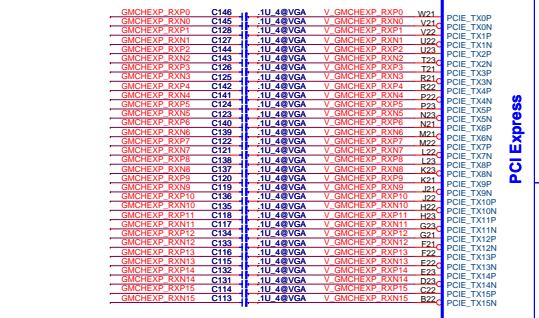
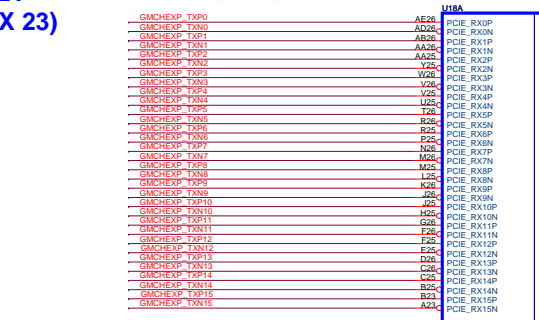




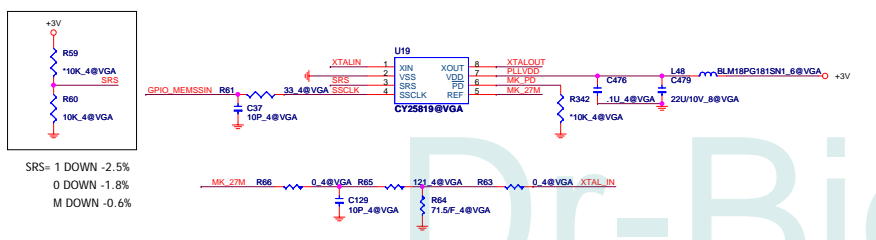


0.1u Capacitors place at last 1/3 of trace

- (8) GMCHEXP_TXP0..15
- (8) GMCHEXP_TXN0..15
- (6) GMCHEXP_RXP0..15
- (6) GMCHEXP_RXN0..15

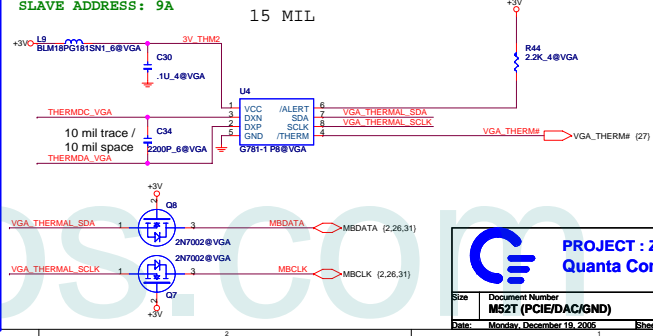


MEMORY CLOCK SPREAD SPECTRUM



SRS= 1 DOWN -2.5%
 0 DOWN -1.8%
 M DOWN -0.6%

Thermal Sensor for Graphic



PROJECT : ZL9
 Quanta Computer Inc.

{18} VMA_DQ[63.0]

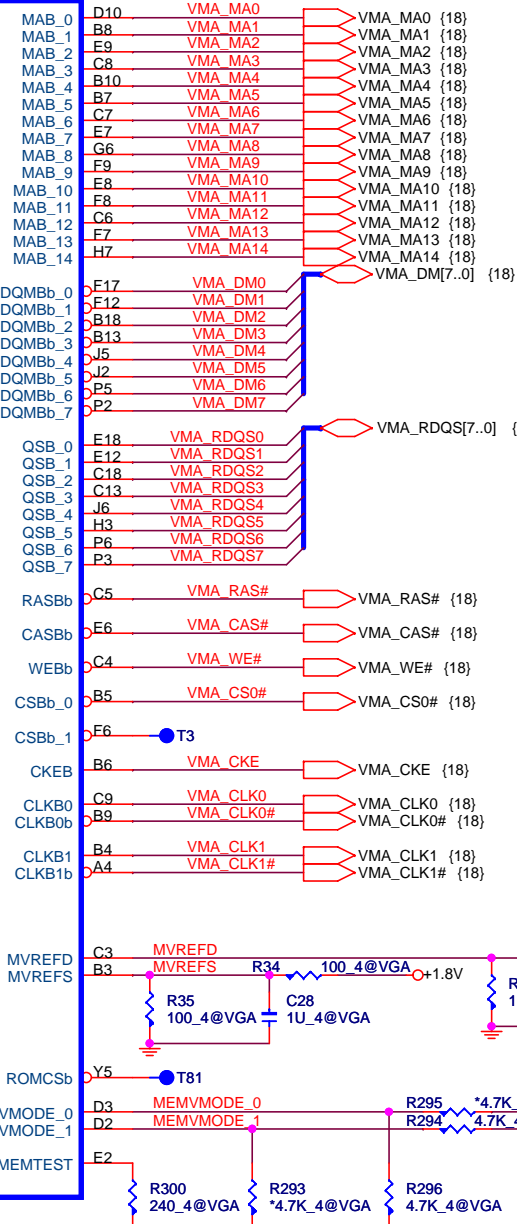
- VMA_DQ0 F16
- VMA_DQ1 E20
- VMA_DQ2 E16
- VMA_DQ3 E19
- VMA_DQ4 F19
- VMA_DQ5 E17
- VMA_DQ6 E15
- VMA_DQ7 F18
- VMA_DQ8 F14
- VMA_DQ9 F13
- VMA_DQ10 E14
- VMA_DQ11 E13
- VMA_DQ12 F10
- VMA_DQ13 E10
- VMA_DQ14 F11
- VMA_DQ15 E11
- VMA_DQ16 C20
- VMA_DQ17 B19
- VMA_DQ18 B20
- VMA_DQ19 C19
- VMA_DQ20 C16
- VMA_DQ21 C17
- VMA_DQ22 B16
- VMA_DQ23 B17
- VMA_DQ24 B12
- VMA_DQ25 C15
- VMA_DQ26 C11
- VMA_DQ27 B15
- VMA_DQ28 C14
- VMA_DQ29 B11
- VMA_DQ30 B14
- VMA_DQ31 C12
- VMA_DQ32 F5
- VMA_DQ33 G5
- VMA_DQ34 H6
- VMA_DQ35 H5
- VMA_DQ36 K6
- VMA_DQ37 K5
- VMA_DQ38 L6
- VMA_DQ39 L5
- VMA_DQ40 F2
- VMA_DQ41 G2
- VMA_DQ42 H2
- VMA_DQ43 G3
- VMA_DQ44 K2
- VMA_DQ45 L2
- VMA_DQ46 J3
- VMA_DQ47 K3
- VMA_DQ48 M5
- VMA_DQ49 M6
- VMA_DQ50 N6
- VMA_DQ51 N5
- VMA_DQ52 R6
- VMA_DQ53 U5
- VMA_DQ54 R5
- VMA_DQ55 T5
- VMA_DQ56 M2
- VMA_DQ57 M3
- VMA_DQ58 N2
- VMA_DQ59 N3
- VMA_DQ60 R2
- VMA_DQ61 R3
- VMA_DQ62 T2
- VMA_DQ63 T3

U18C

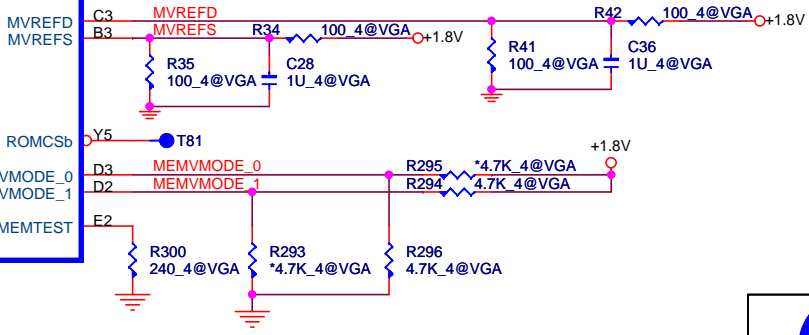
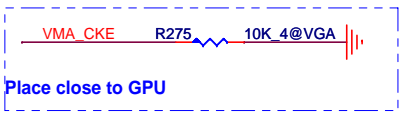
Part 3 of 6

MEMORY INTERFACE

216PQAKA11FG_1@VGA



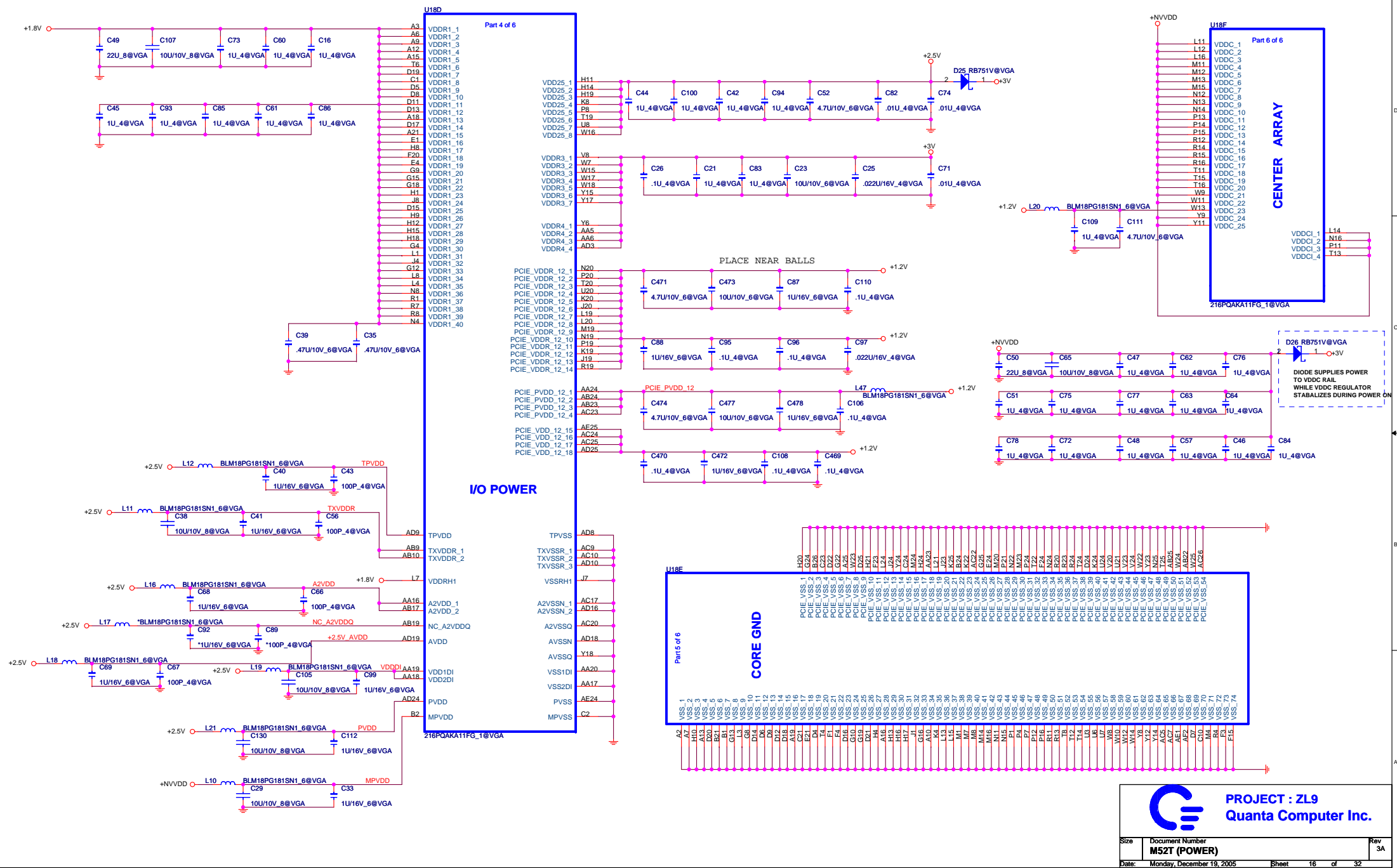
VDDR1	MEMVMODE_0	MEMVMODE_1
1.8V	GND	+VDDC_CT
2.5V	+VDDC_CT	GND
2.8V	+VDDC_CT	+VDDC_CT



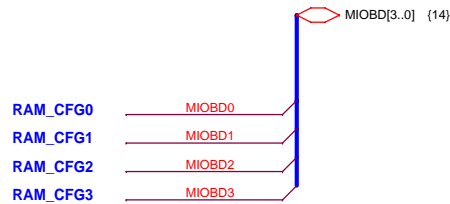
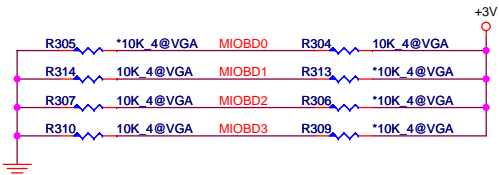
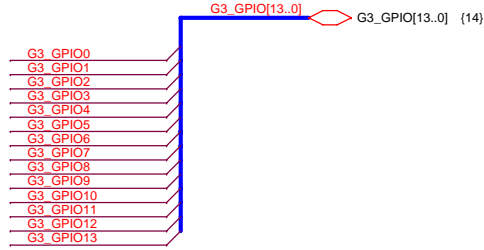
PROJECT : ZL9
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Size	Document Number	Rev
	M52T (MEMORY A/B)	3A
Date:	Monday, December 19, 2005	Sheet 15 of 32

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M52T VRAM Configuration Table

RAM_CFG[3:0]	DESCRIPTION
0000	DDR2 , 16Mx16 , 2pcs (64M)
0001	DDR2 , 16Mx16 , 4pcs (128M)
0010	DDR2 , 32Mx16 , 2pcs (128M)
0011	DDR2 , 32Mx16 , 4pcs (256M)
others	Reserved

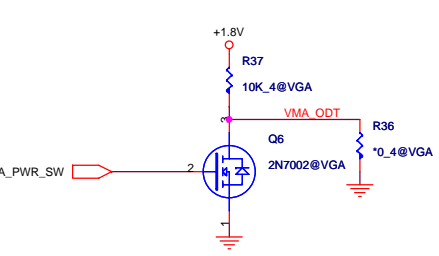
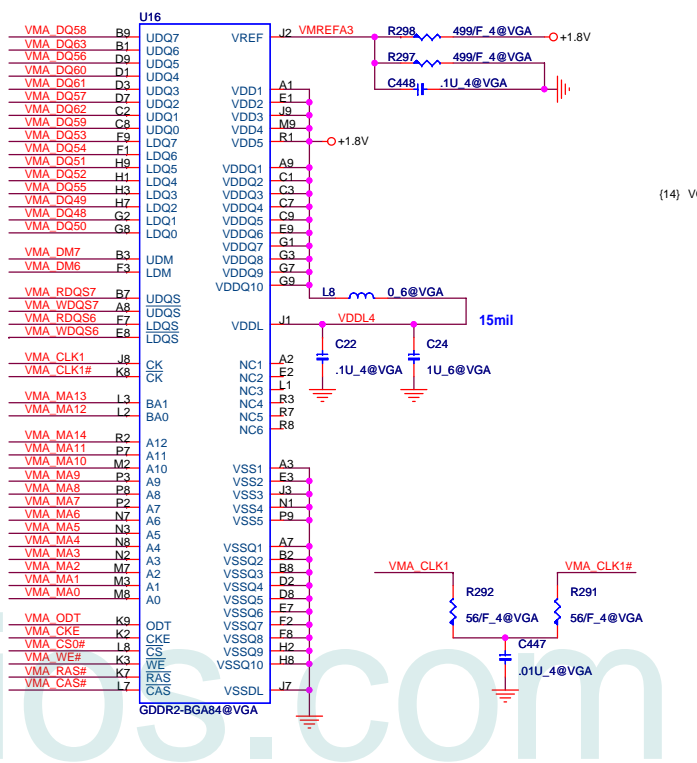
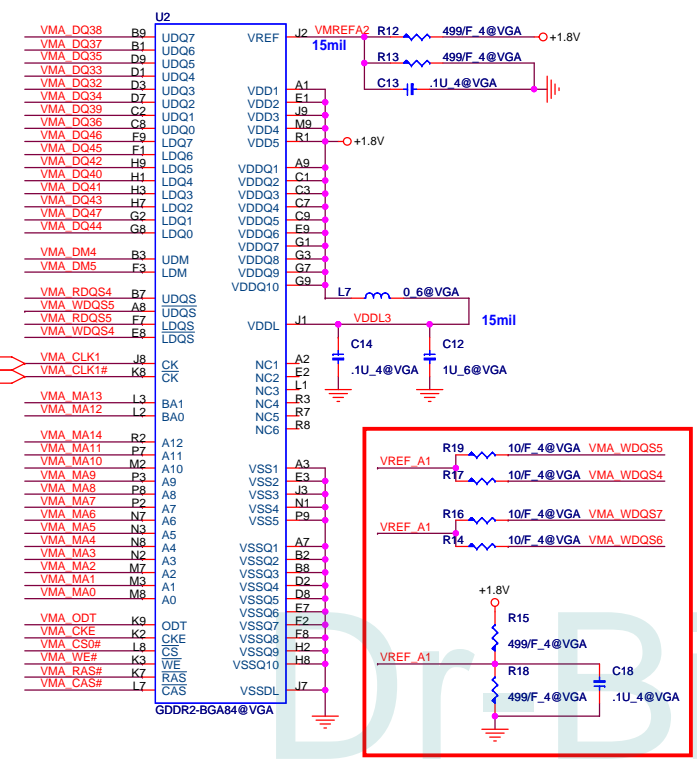
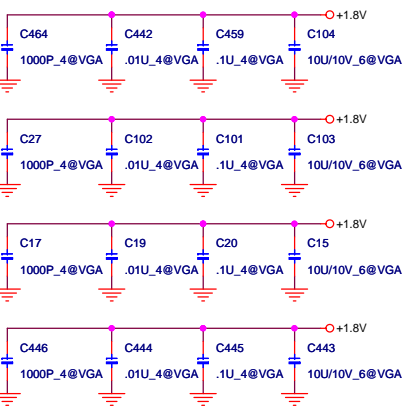
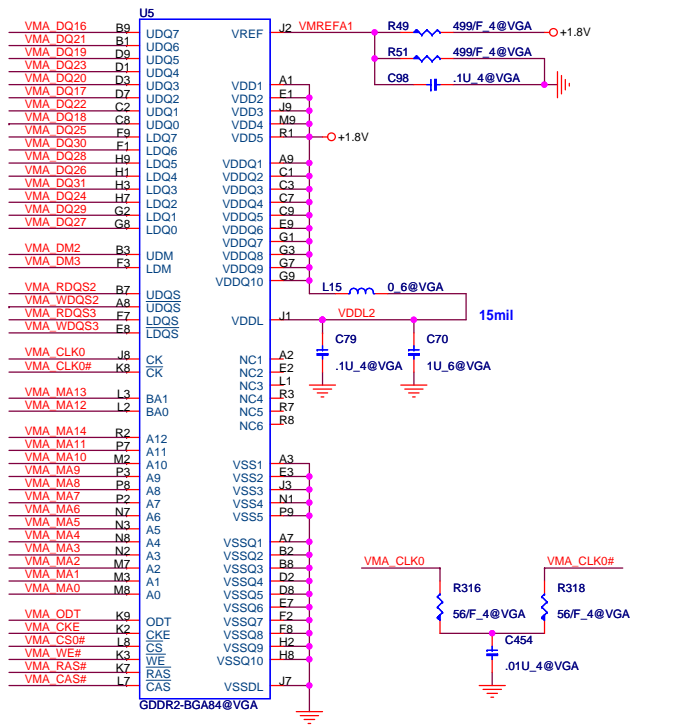
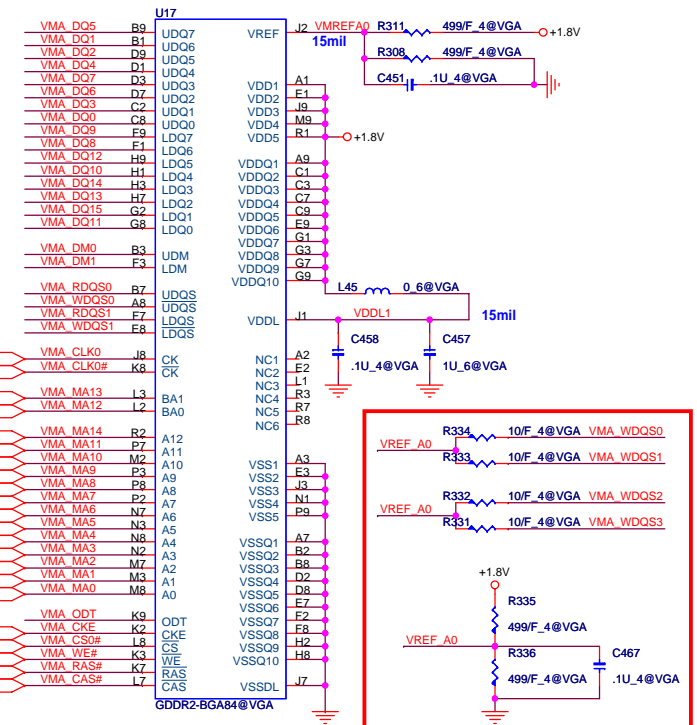
STRAPS	PIN	DESCRIPTION	ASIC DEFAULT
TX_PWRS_ENB	G3_GPIO0	FULL SWING	1
TX_DEEMPH_EN	G3_GPIO1	TRANSMITTER DE-EMPHASIS ENABLE - TX DE-EMPHASIS DISABLED FOR MOBILE	0
DEBUG_ACCESS	G3_GPIO4	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible.	0
FORCE COMPLIANCE	G3_GPIO8	Force chip to get to compliance state quickly for tester purposes	0
ROMIDCFG(3:0)	G3_GPIO(9,13,12,11)	<p>128M</p> <p>256M</p> <p>64M</p> <p>Reserved</p>	<p>0000</p> <p>0010</p> <p>0100</p> <p>0110</p>

MULTIFUNC(1:0)	LCDDATA(17:16)	Multi-function device select 00 - single function device. 01 - two function device. No AGP in either function 10 - two function device. AGP only in function 0 11 - two function device. AGP in both functions If BUSCFG pin based straps are set to PCI, then AGP will not be enabled in any function.	00
VIP_DEVICE	LCDDATA(20)	Indicates if any slave VIP host devices drove this low during reset. 0 - Slave VIP host port devices present 1 - No slave VIP host port devices reporting presence during reset	0
DWNGRD	LCDDATA(21)	0 - Device remain a workstation grade part. 1 - Part is downgraded to a Normal part	0 (internal pull-down)



- (15) VMA_DQ[63..0]
- (15) VMA_DM[7..0]
- (15) VMA_RDQS[7..0]

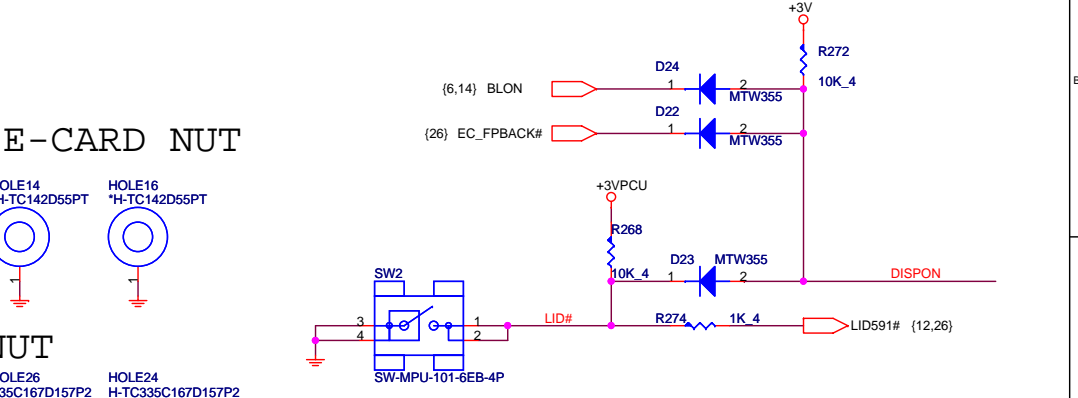
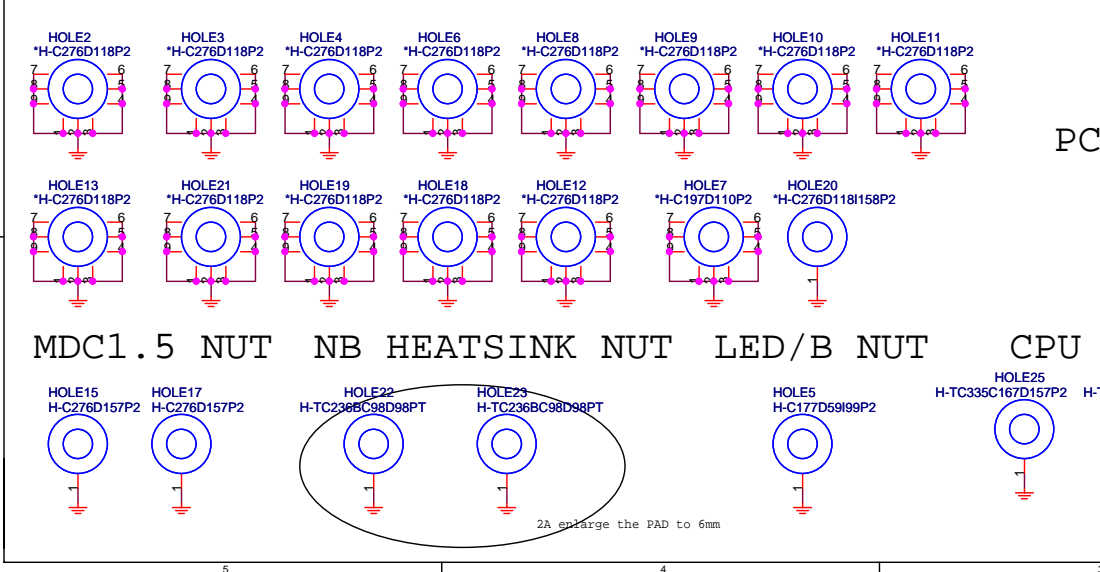
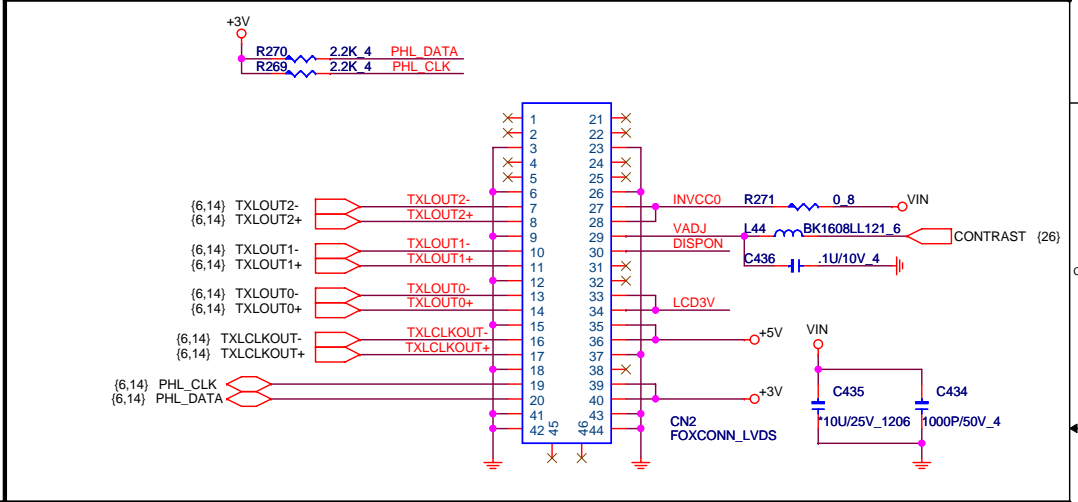
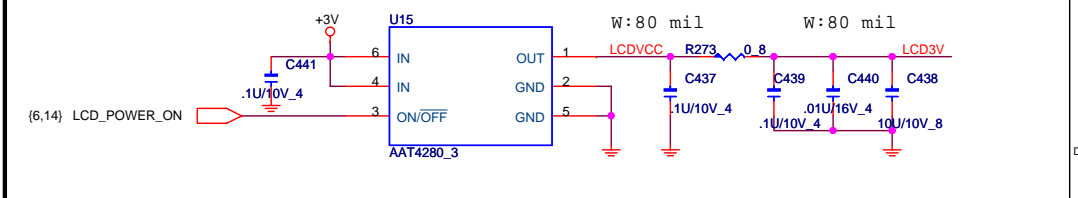
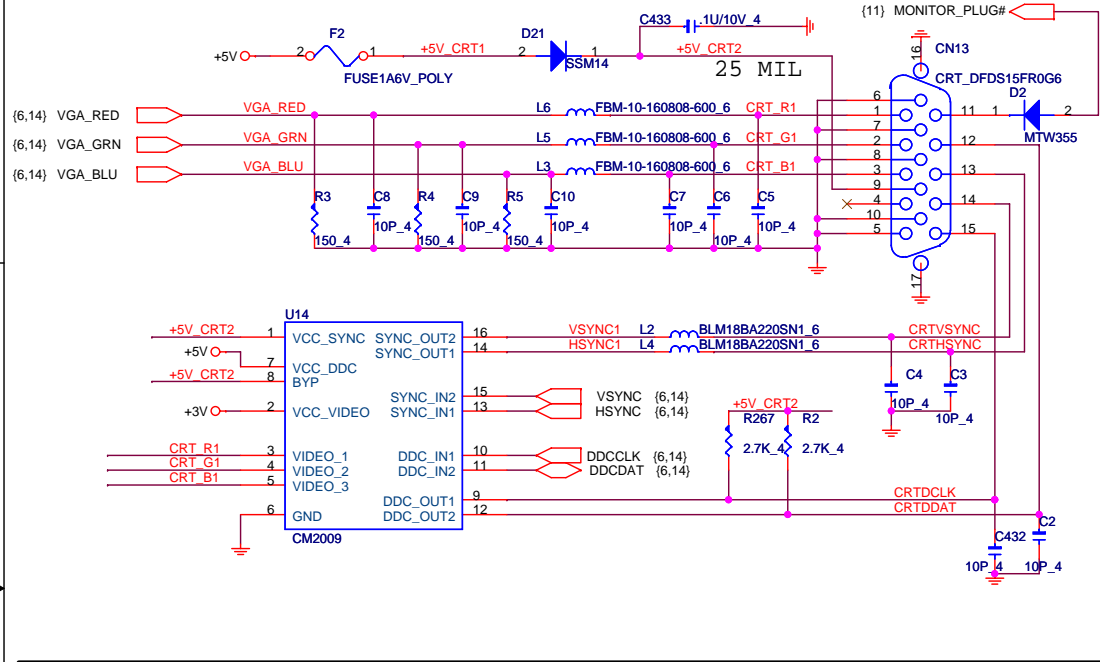
256Mb : AKD5JGAT*05
512Mb : AKD59G-T*01




PROJECT : ZL9
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Size	Document Number	Rev
	VRAM (GDDR2)	3A
Date:	Monday, December 19, 2005	Sheet 18 of 32

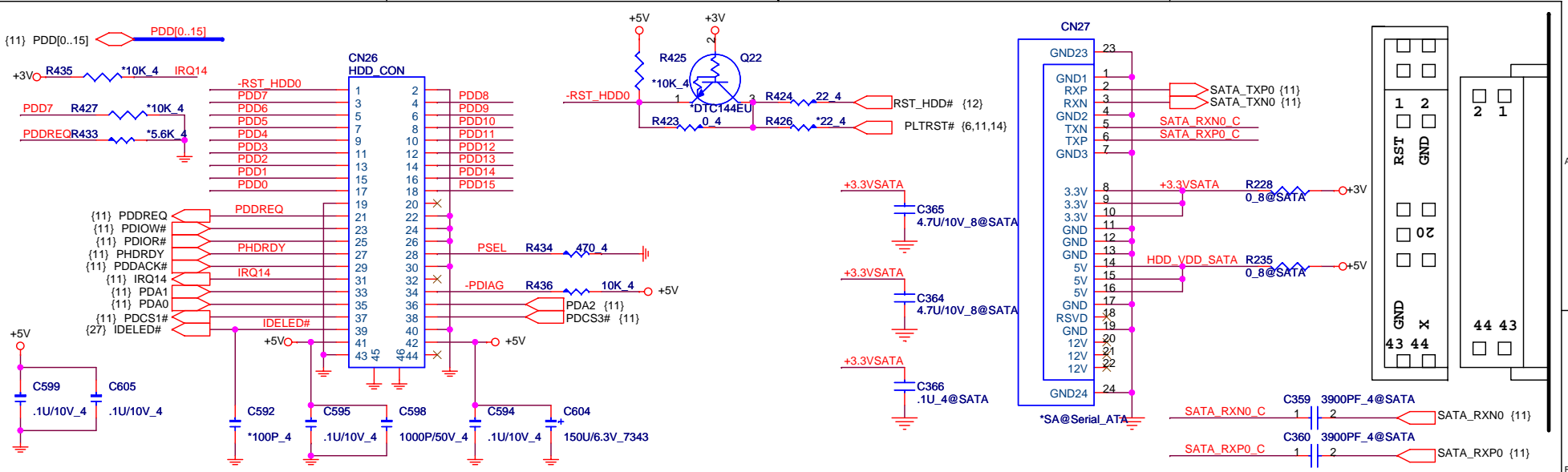
CRT PORT



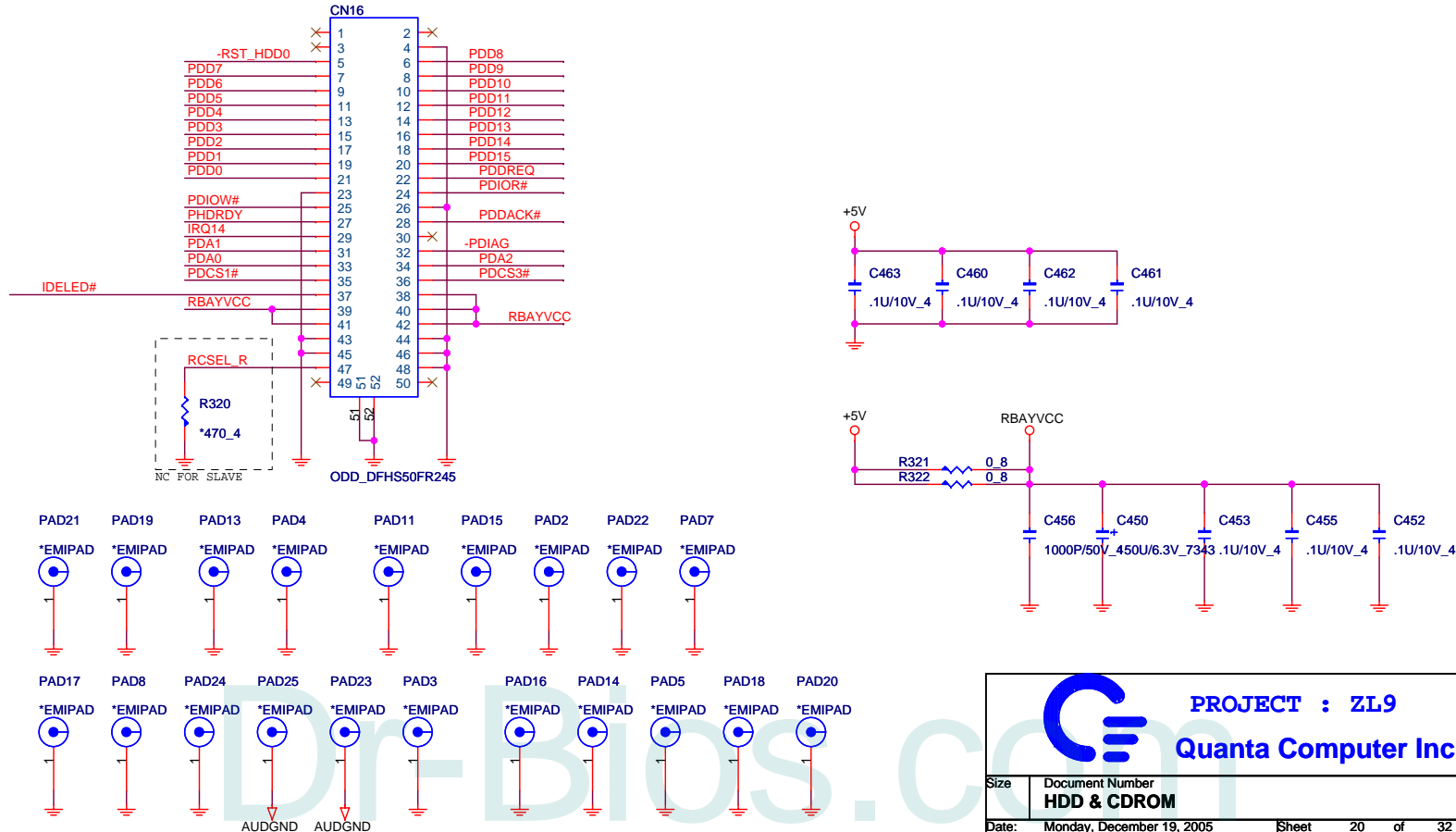


PROJECT : ZL9
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Size	Document Number	Rev
	LVDS,VGA Ports, LID, & HOLES	3A
Date:	Monday, December 19, 2005	Sheet 19 of 32



ODD Connector

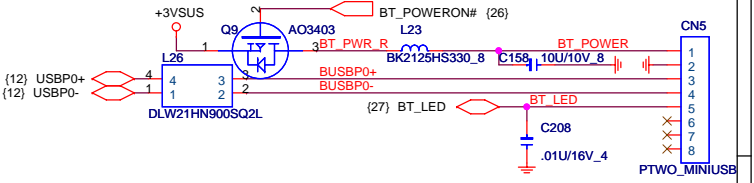
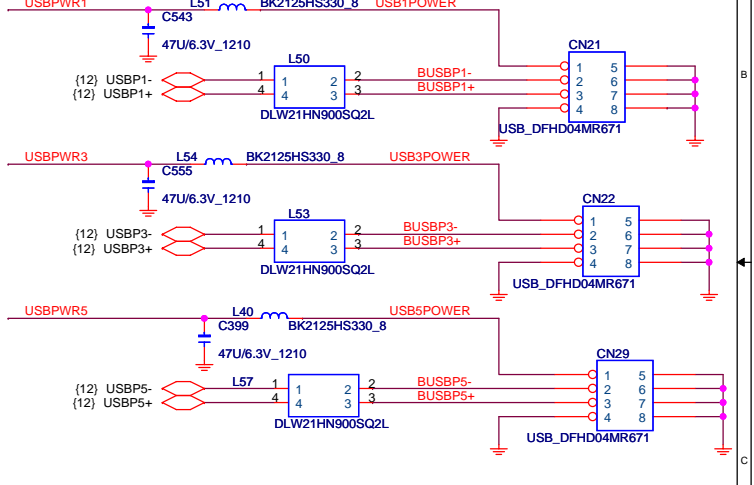
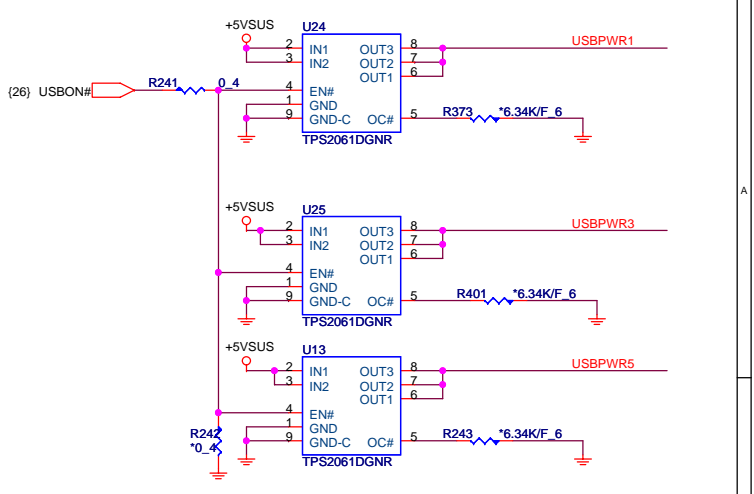
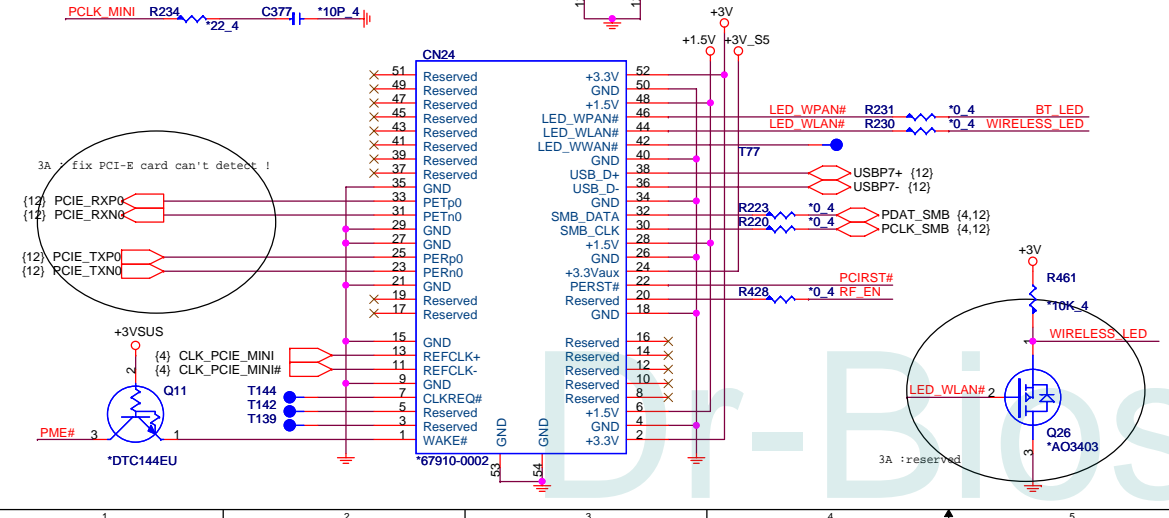
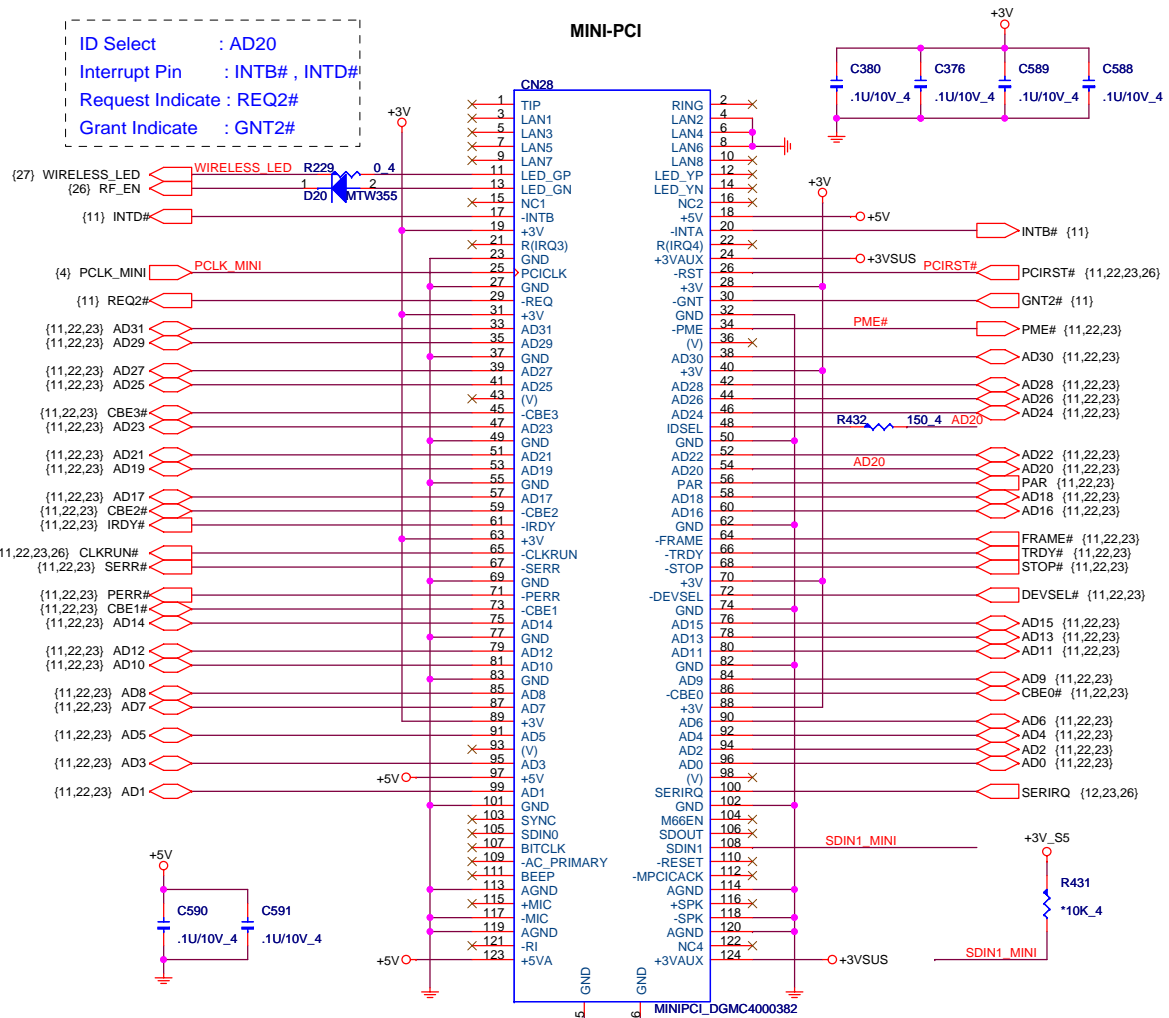



PROJECT : ZL9
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Size	Document Number	Rev
	HDD & CDROM	3A
Date:	Monday, December 19, 2005	Sheet 20 of 32

ID Select : AD20
 Interrupt Pin : INTB# , INTD#
 Request Indicate : REQ2#
 Grant Indicate : GNT2#

MINI-PCI

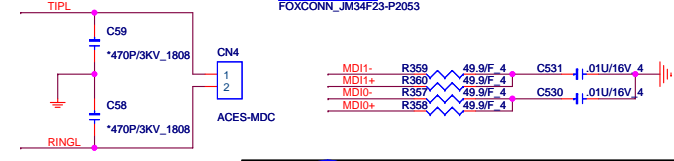
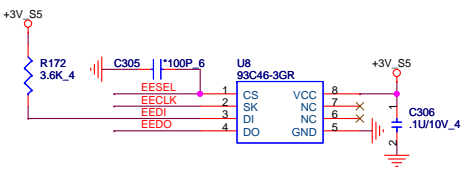
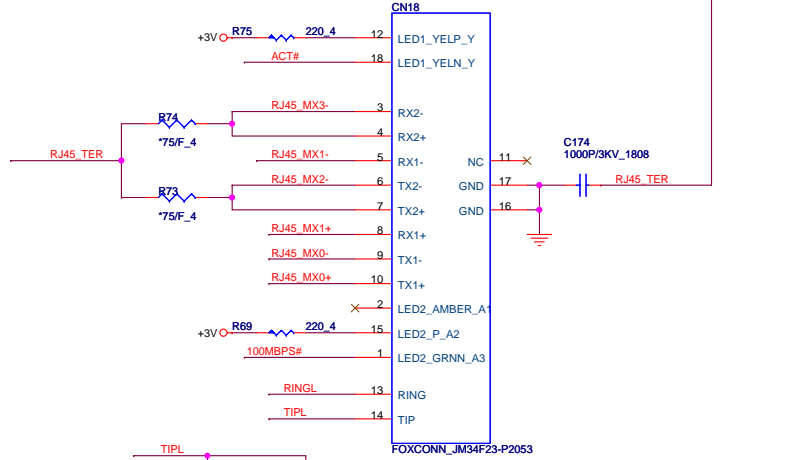
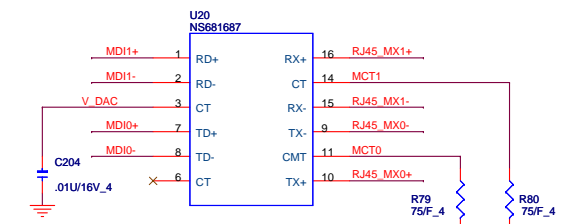
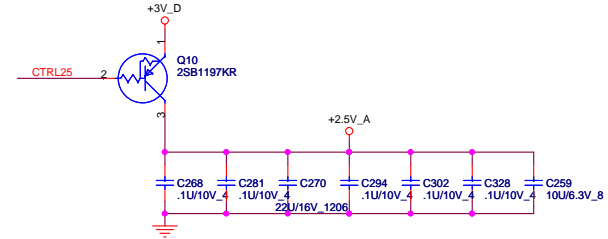
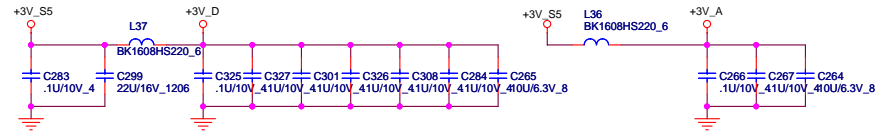
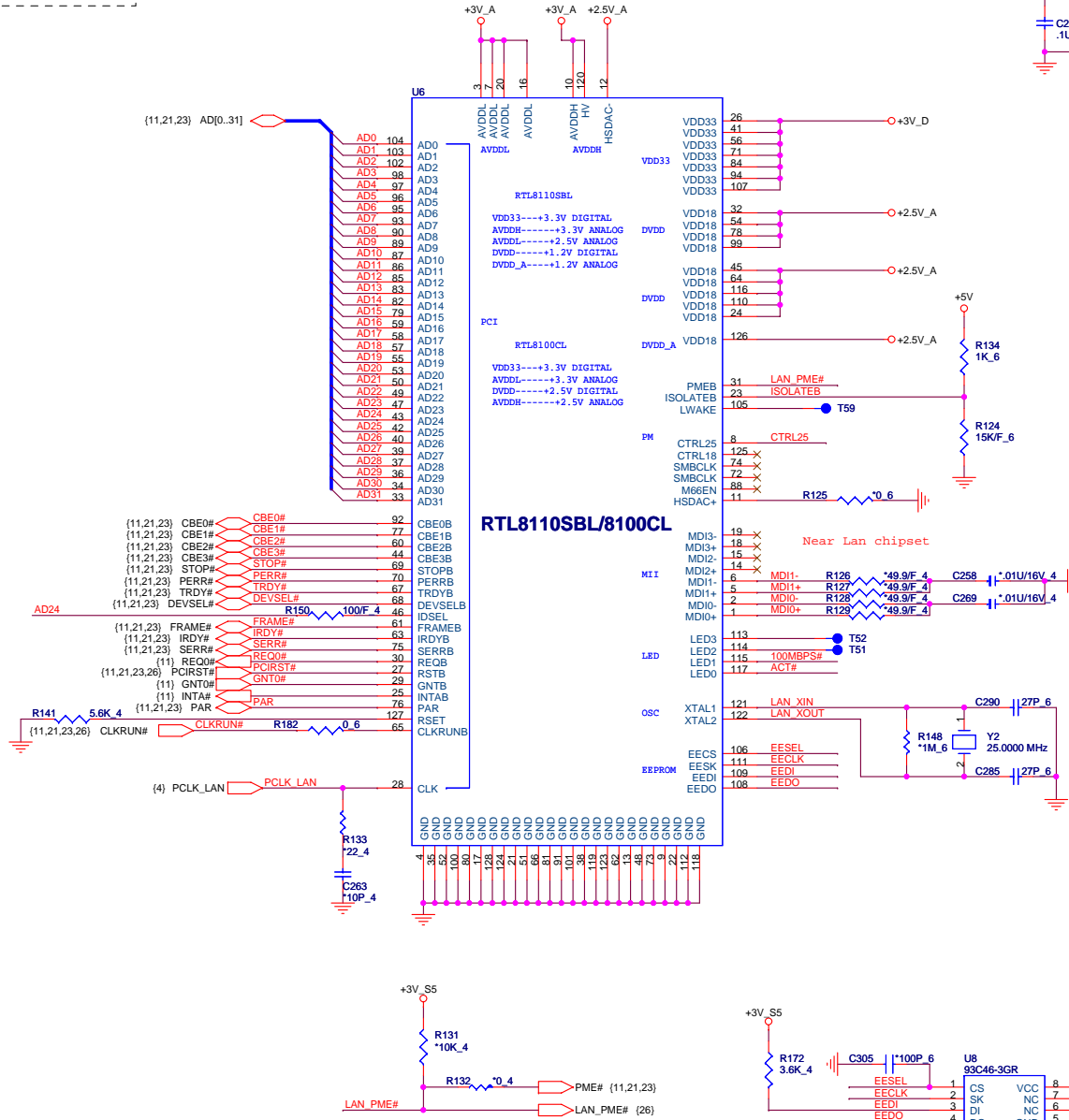




PROJECT : ZL9
Quanta Computer Inc.

Size	Document Number	Rev
	MINI PCI,USB	3A
Date:	Monday, December 19, 2005	Sheet 21 of 32

ID Select : AD24
 Interrupt Pin : INTA#
 Request Indicate : REQ0#
 Grant Indicate : GNT0#



2A : modify for ESD issue

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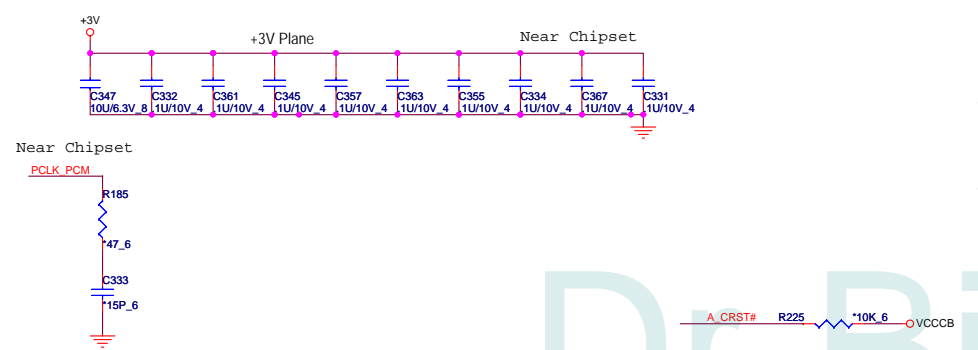
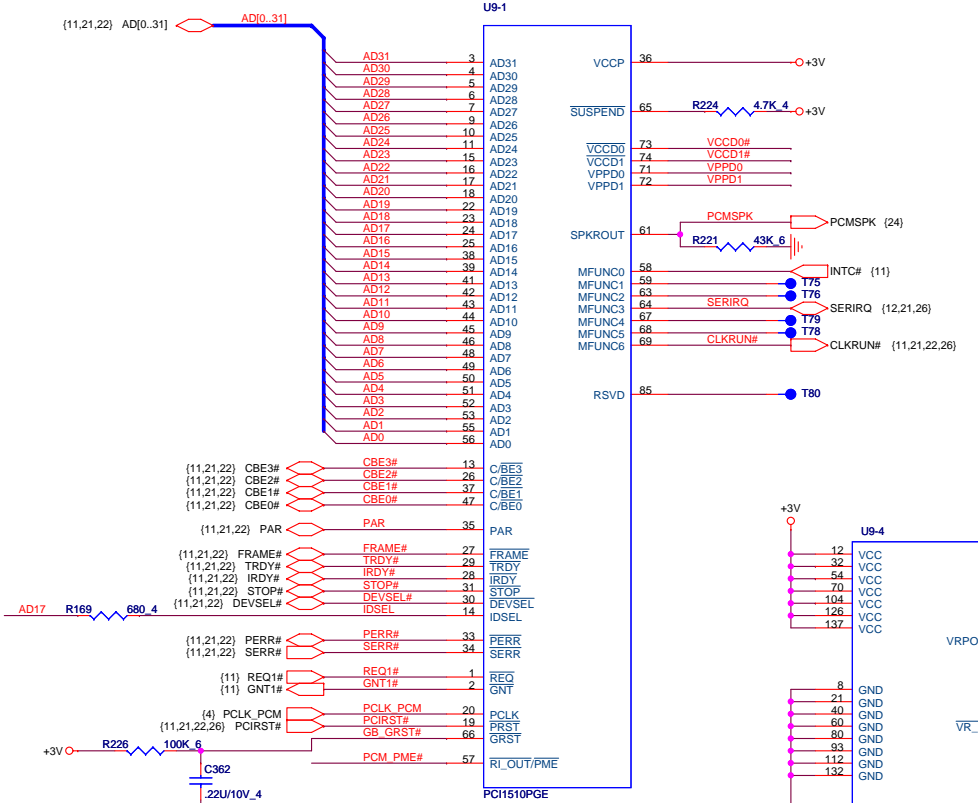
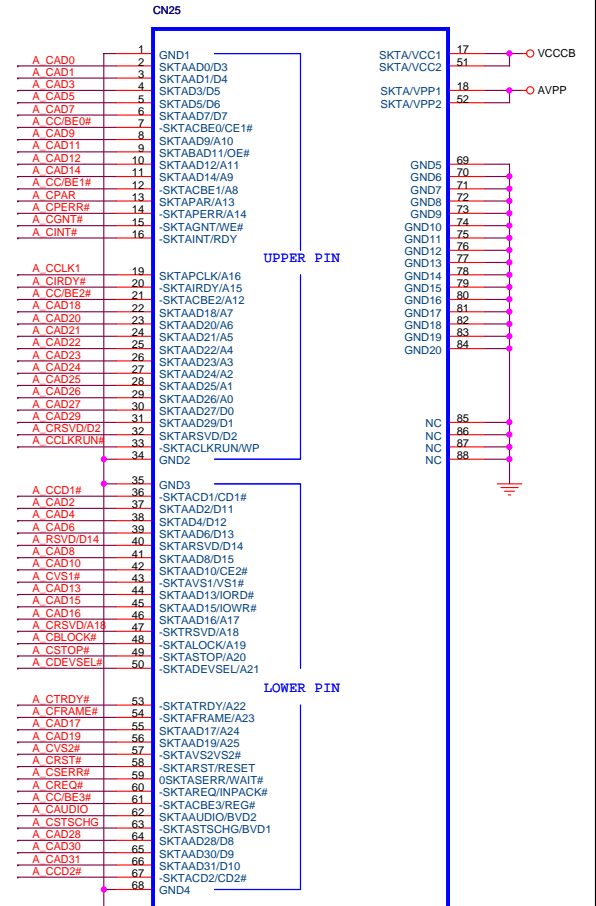
PROJECT : ZL9
 Quanta Computer Inc.

Size	Document Number	Rev
	LAN RTL810SBL/8100CL	3A
Date:	Monday, December 19, 2005	Sheet 22 of 32

ID Select : AD17
 Interrupt Pin : INTC#
 Request Indicate : REQ1#
 Grant Indicate : GNT1#

U9-2		
VCCCB	109	VCCB R R227 0 8 -VCCCB
CAD31/D10	144	A CAD31
CAD30/D9	142	A CAD30
CAD29/D1	141	A CAD29
CAD28/D8	140	A CAD28
CAD27/D0	139	A CAD27
CAD26/A0	129	A CAD26
CAD25/A1	128	A CAD25
CAD24/A2	127	A CAD24
CAD23/A3	123	A CAD23
CAD22/A4	121	A CAD22
CAD21/A5	120	A CAD21
CAD20/A6	118	A CAD20
CAD19/A7	116	A CAD19
CAD18/A17	115	A CAD18
CAD17/A24	114	A CAD17
CAD16/A17	97	A CAD16
CAD15/IOWR	96	A CAD15
CAD14/A9	94	A CAD13
CAD13/IORD	92	A CAD12
CAD12/A11	90	A CAD11
CAD11/0E	89	A CAD10
CAD10/CE2	87	A CAD9
CAD9/A10	87	A CAD8
CAD8/D15	86	A CAD7
CAD7/D17	82	A CAD6
CAD6/D13	83	A CAD5
CAD5/D6	79	A CAD4
CAD4/D12	81	A CAD3
CAD3/D5	77	A CAD2
CAD2/D11	78	A CAD1
CAD1/D4	76	A CAD0
CAD0/D3		
CC/BE3/REG	124	A CC/BE3#
CC/BE2/A12	113	A CC/BE2#
CC/BE1/A8	98	A CC/BE1#
CC/BE0/CET	88	A CC/BE0#
CPAR/A13	100	A CPAR
CFRAME/A23	111	A CFRAME#
CTRDY/A22	108	A CTRDY#
CIRDY/A15	110	A CIRDY#
CSTOP/A20	103	A CSTOP#
CDEVSEL/A21	106	A CDEVSEL#
CBLOCK/A19	101	A CBLOCK#
CPERR/A14	102	A CPERR#
CSERR/WAIT	133	A CSERR#
CREQ/INPACK	122	A CREQ#
CGNT/WE	105	A CGNT#
CSTSCHG/STSCHE	135	A CSTSCHG
CCLKRUNIOIS16	136	A CCLKRUN#
CCLK/A16	107	R232 47.6 A CCLK1
CINT/IREQ	131	A CINT#
CRST/RESET	119	A CRST#
CAUDIO/SPKR	134	A CAUDIO
CCD1/CDT	75	A CCD1#
CCD2/CD2	138	A CCD2#
CVS1/V51	130	A CVS1#
CVS2/V52	117	A CVS2#
RSVD/D14	84	A RSVD/D14
RSVD/D12	143	A RSVD/D12
RSVD/A18	99	A RSVD/A18

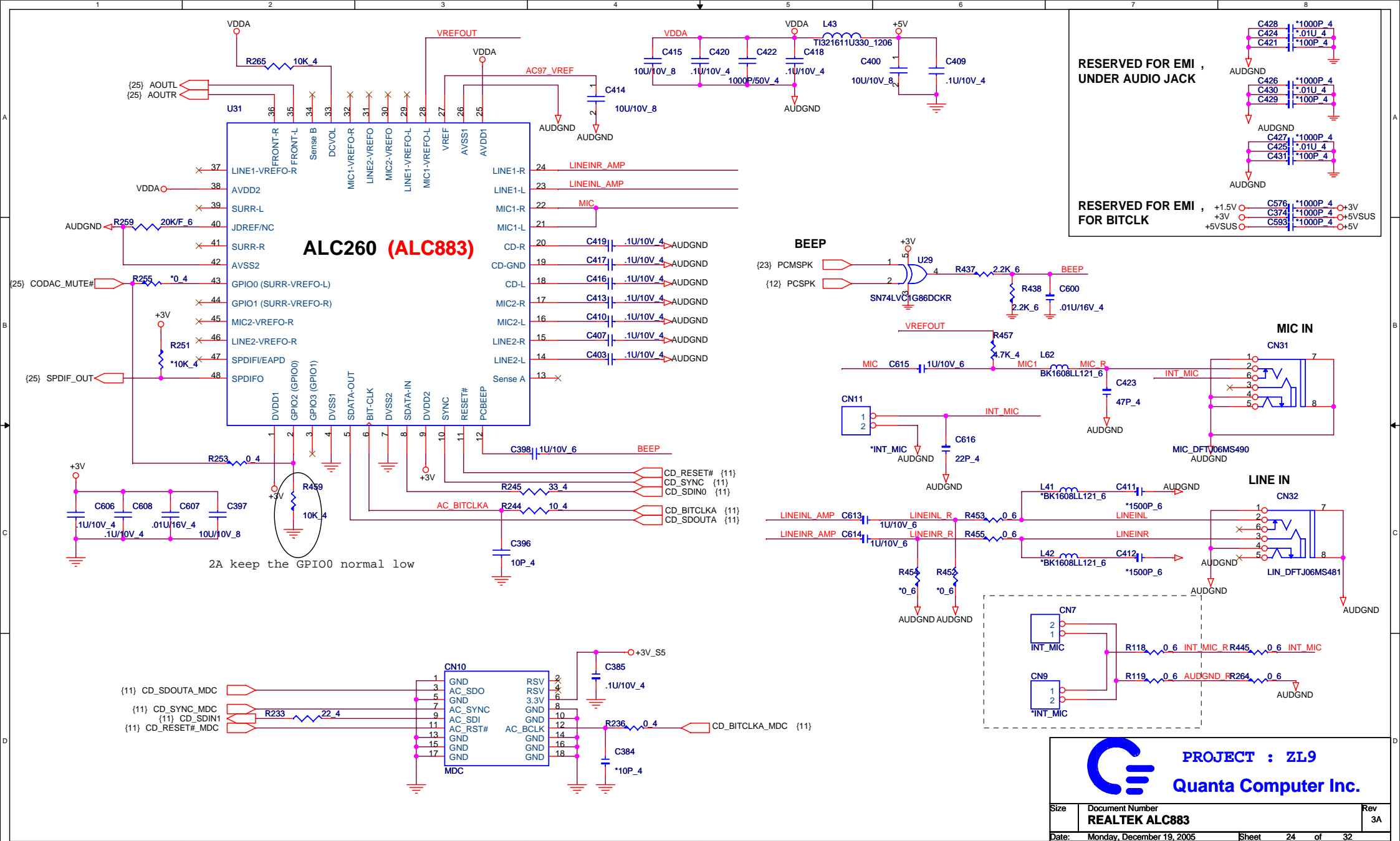
CARDBUS SLOT



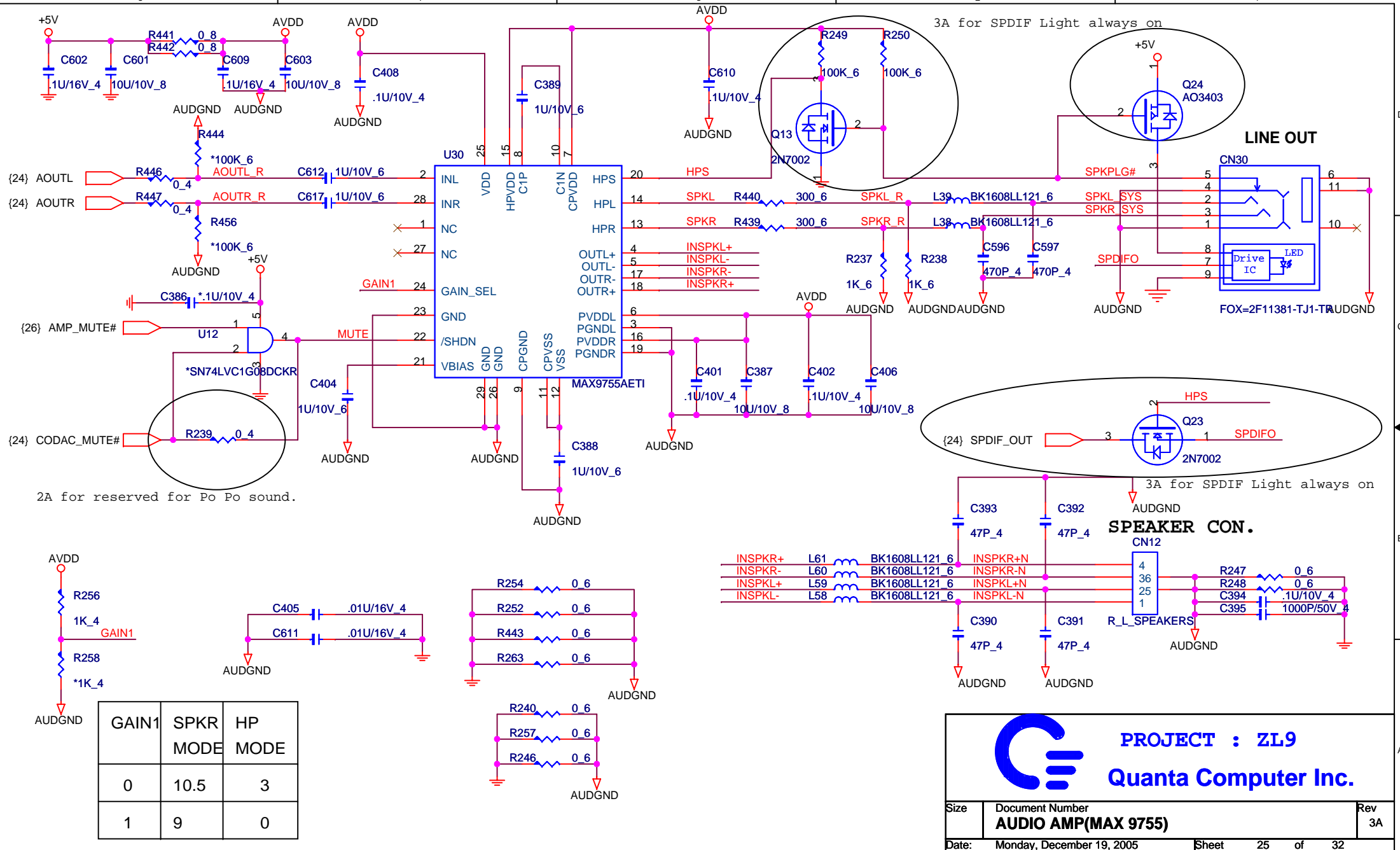
Near Slot

PROJECT : ZL9
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Size	Document Number	Rev
	PCMCIA CONTROLLER	3A
Date:	Monday, December 19, 2005	Sheet 23 of 32




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2A for reserved for Po Po sound.

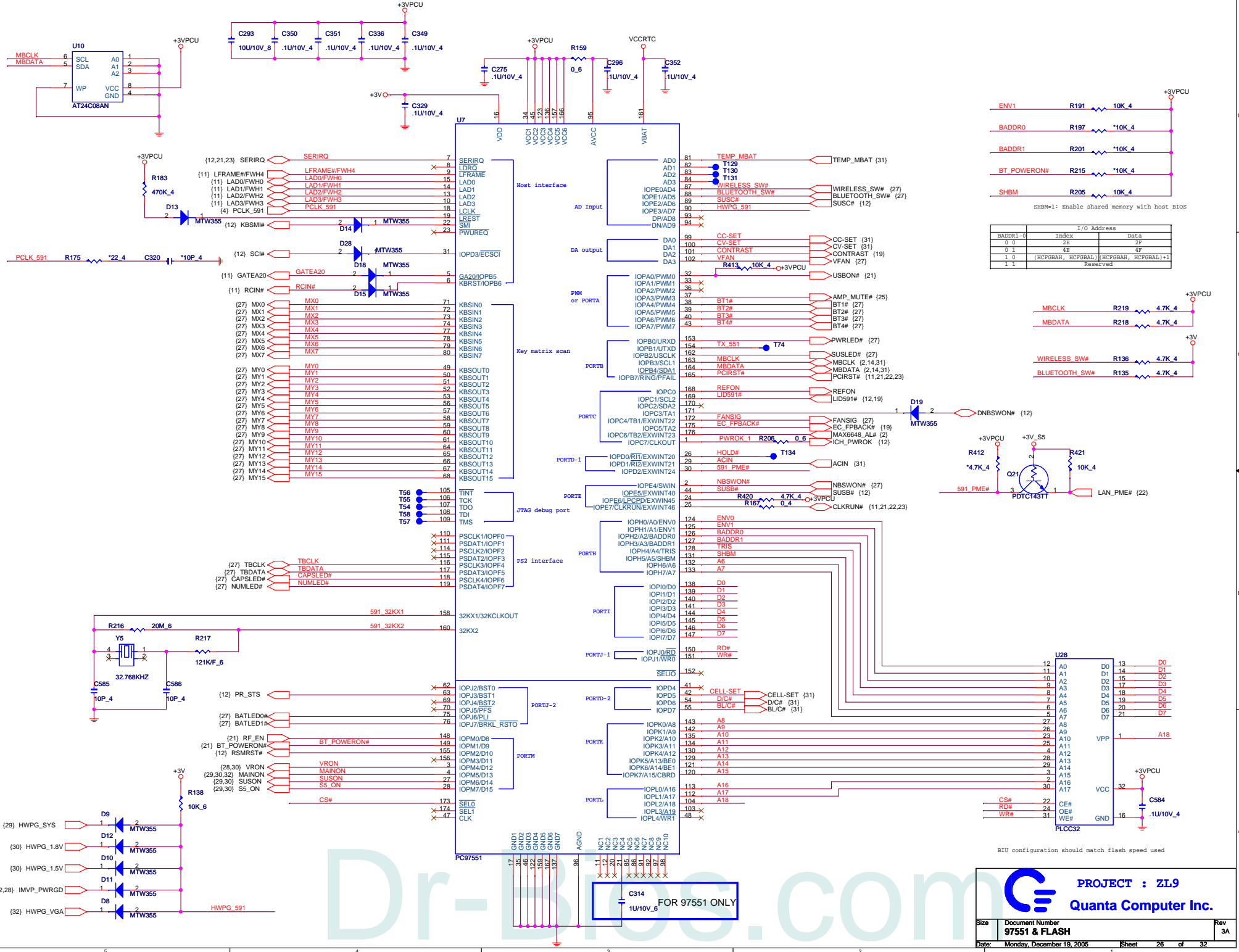
3A for SPDIF Light always on

GAIN1	SPKR MODE	HP MODE
0	10.5	3
1	9	0



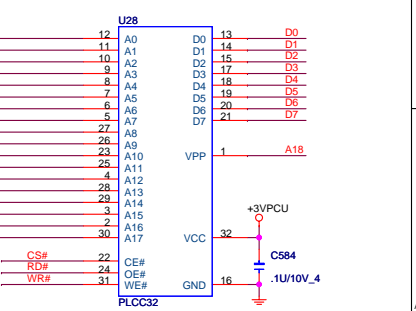
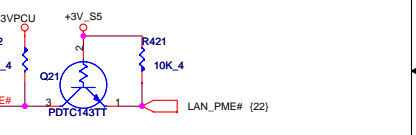
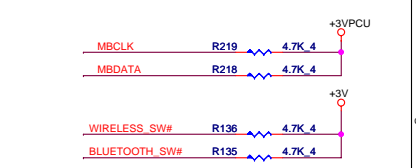
PROJECT : ZL9
Quanta Computer Inc.

Size	Document Number	Rev
	AUDIO AMP(MAX 9755)	3A
Date:	Monday, December 19, 2005	Sheet 25 of 32



SHBM=1: Enable shared memory with host BIOS

BADDR1-0	Index	Data
0 0	2E	2F
0 1	4E	4F
1 0	{HCFGBAH, HCFGBAL}	{HCFGBAH, HCFGBAL}+1
1 1		Reserved

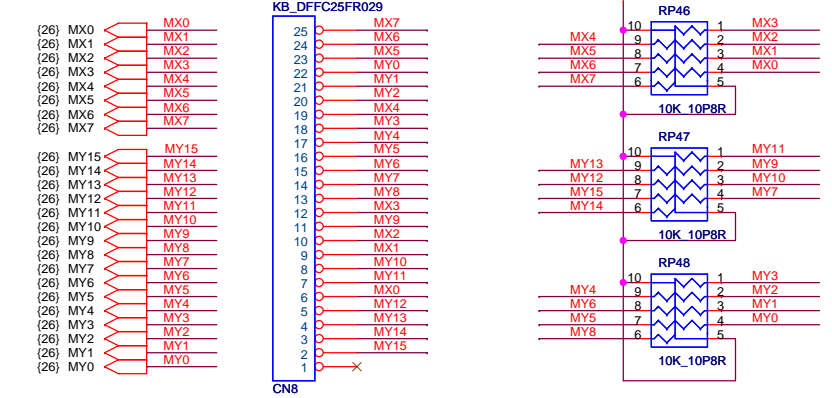


BIU configuration should match flash speed used

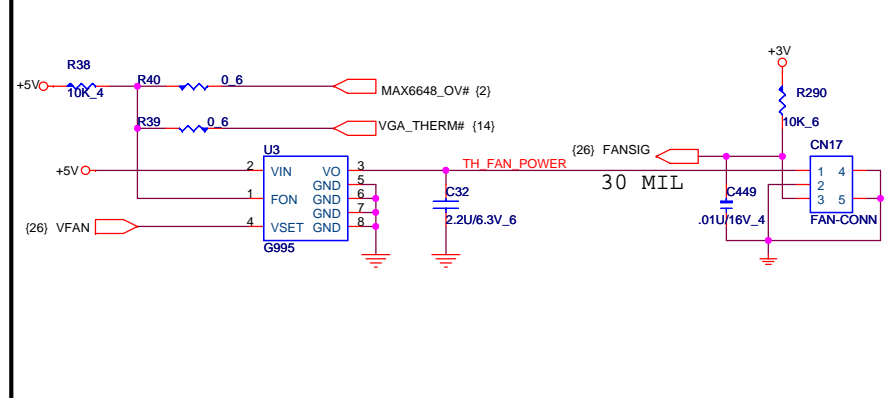
PROJECT : ZL9
Quanta Computer Inc.

Size	Document Number	Rev
	97551 & FLASH	3A
Date:	Monday, December 19, 2005	Sheet 26 of 32

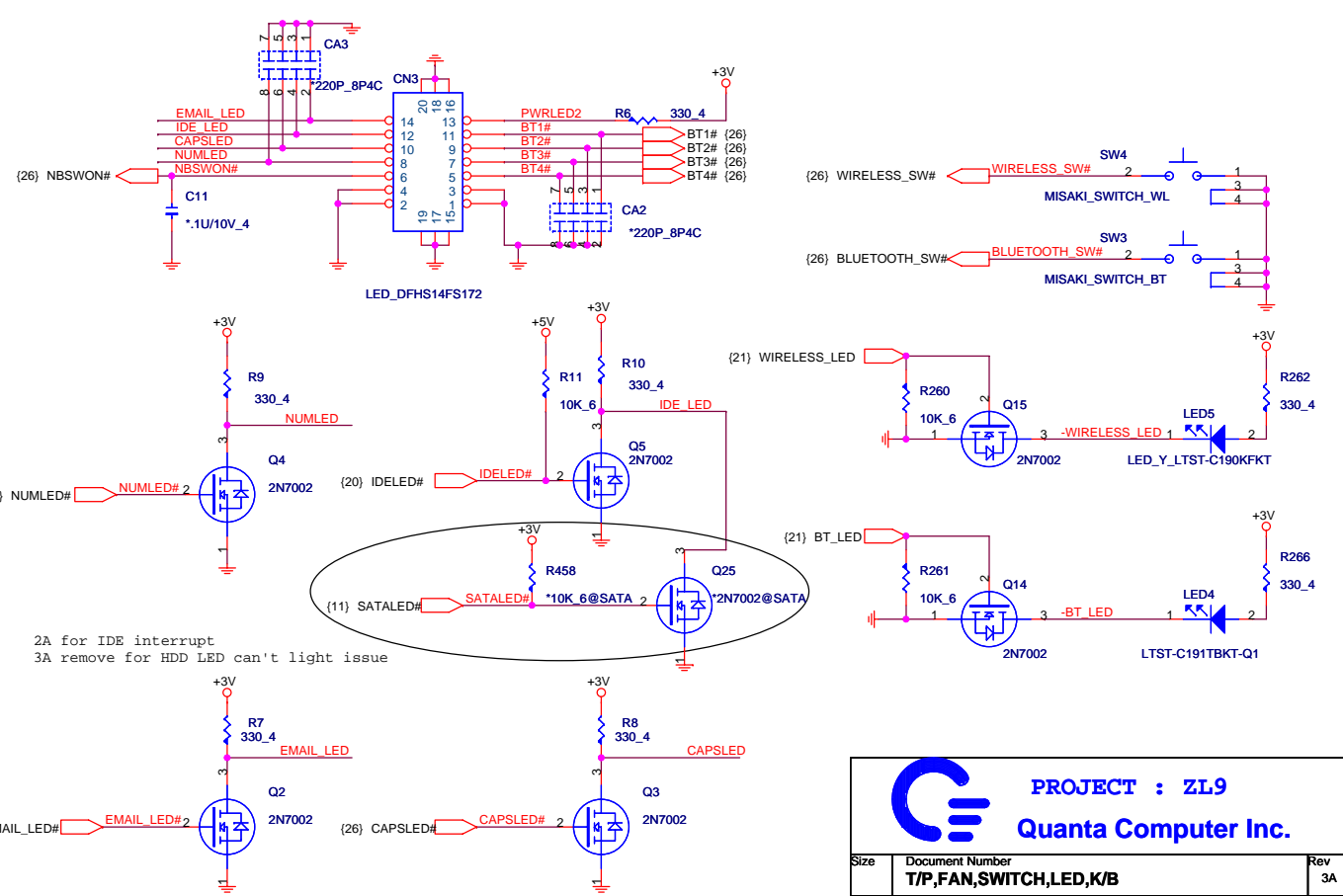
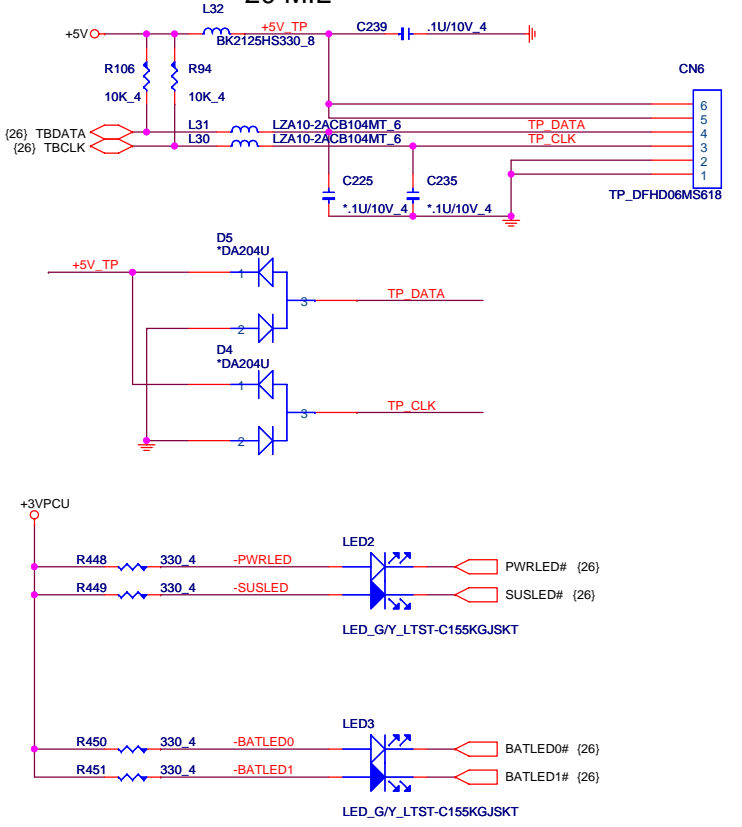
INT K/B



FAN CONTROL



TOUCH PAD

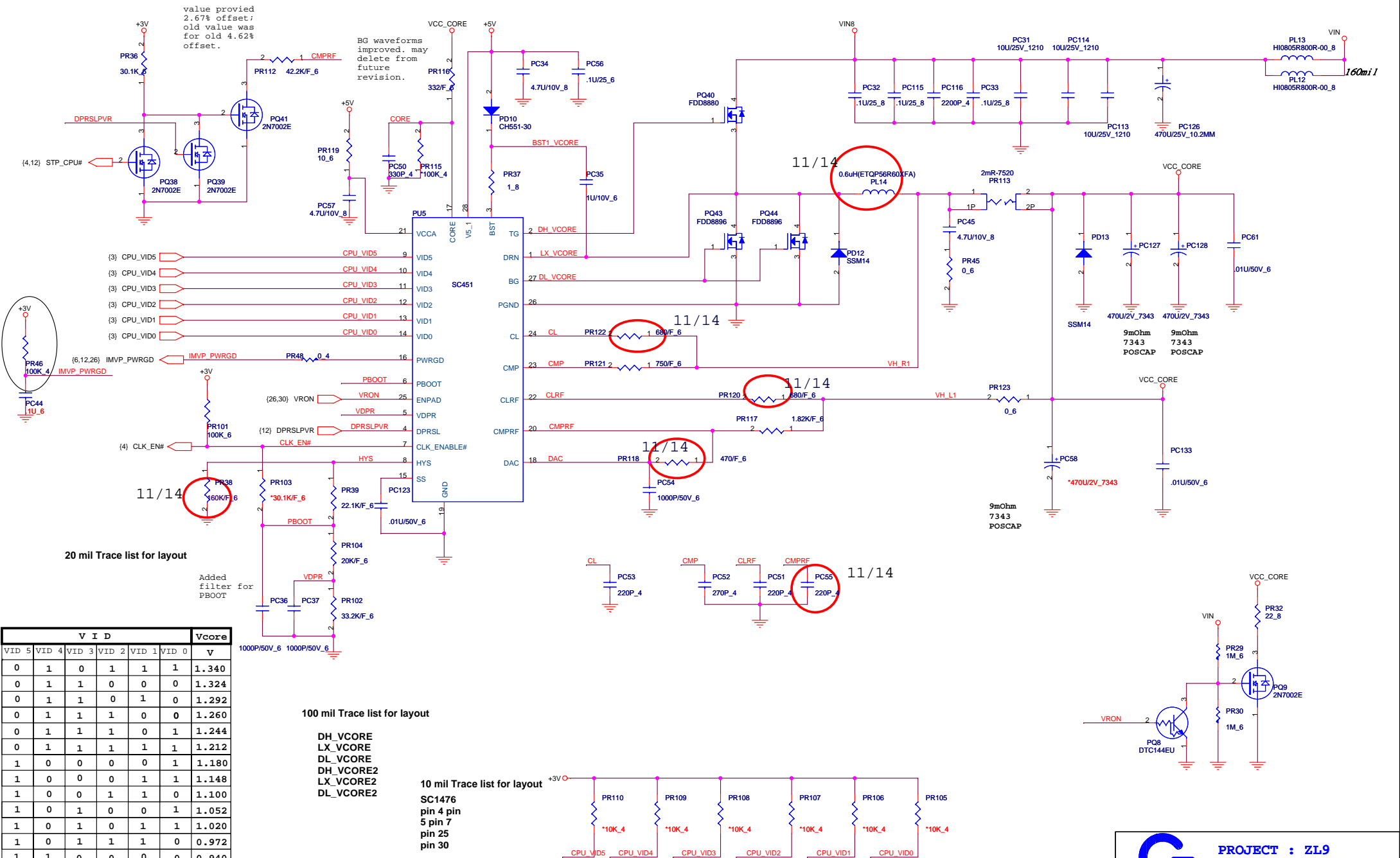


PROJECT : ZL9
Quanta Computer Inc.

Size	Document Number	Rev
	T/P,FAN,SWITCH,LED,K/B	3A
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value provided
2.67% offset;
old value was
for old 4.62%
offset.

BG waveforms
improved may
delete from
future
revision.



20 mil Trace list for layout

Added filter for PBOOT

V I D							Vcore
VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	v	
0	1	0	1	1	1	1.340	
0	1	1	0	0	0	1.324	
0	1	1	0	1	0	1.292	
0	1	1	1	0	0	1.260	
0	1	1	1	0	1	1.244	
0	1	1	1	1	1	1.212	
1	0	0	0	0	1	1.180	
1	0	0	0	1	1	1.148	
1	0	0	1	1	0	1.100	
1	0	1	0	0	1	1.052	
1	0	1	0	1	1	1.020	
1	0	1	1	1	0	0.972	
1	1	0	0	0	0	0.940	

100 mil Trace list for layout

- DH_VCORE
- LX_VCORE
- DL_VCORE
- DH_VCORE2
- LX_VCORE2
- DL_VCORE2

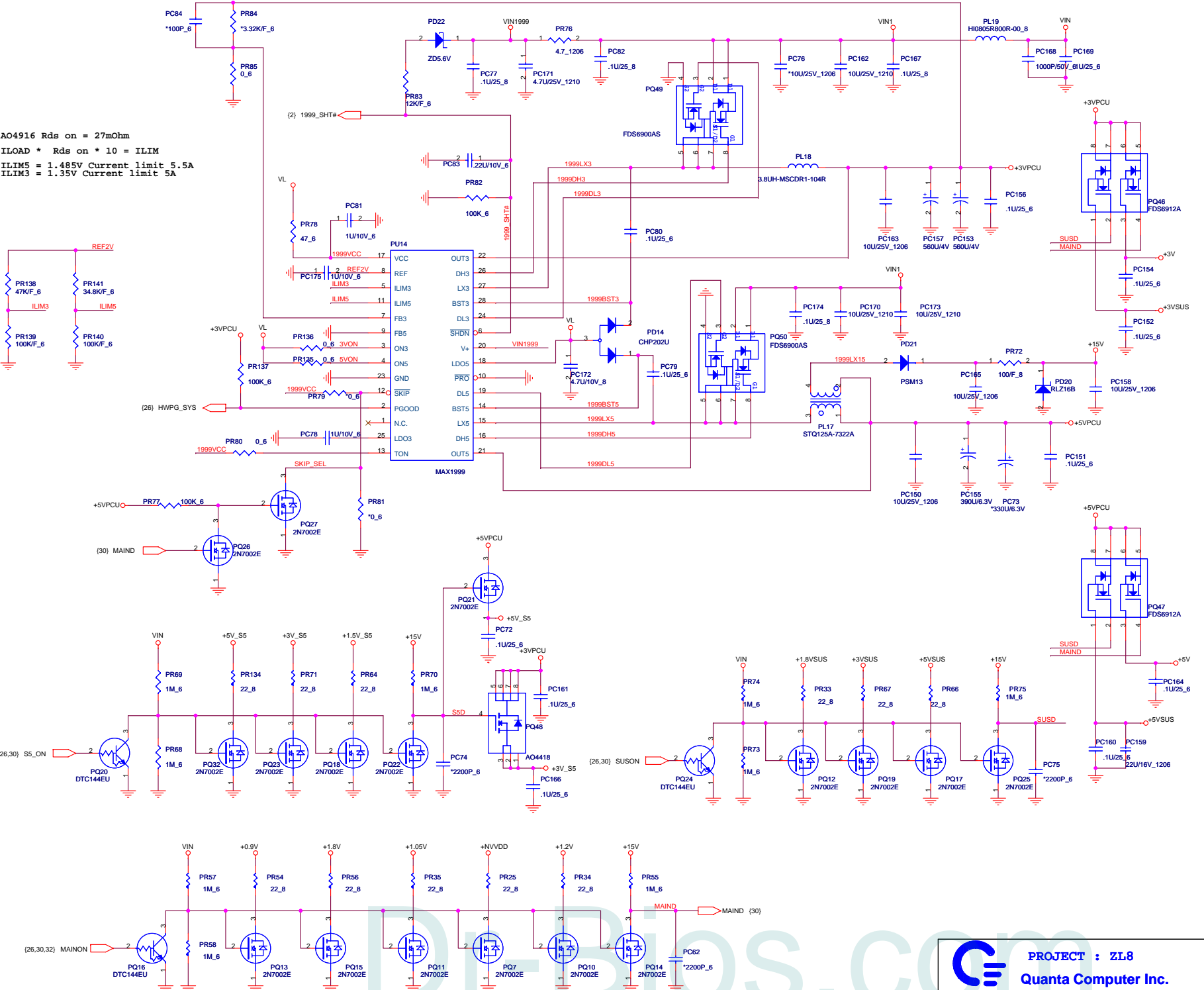
10 mil Trace list for layout

- SC1476
- pin 4 pin
- 5 pin 7
- pin 25
- pin 30

PROJECT : ZL9
Quanta Computer Inc.

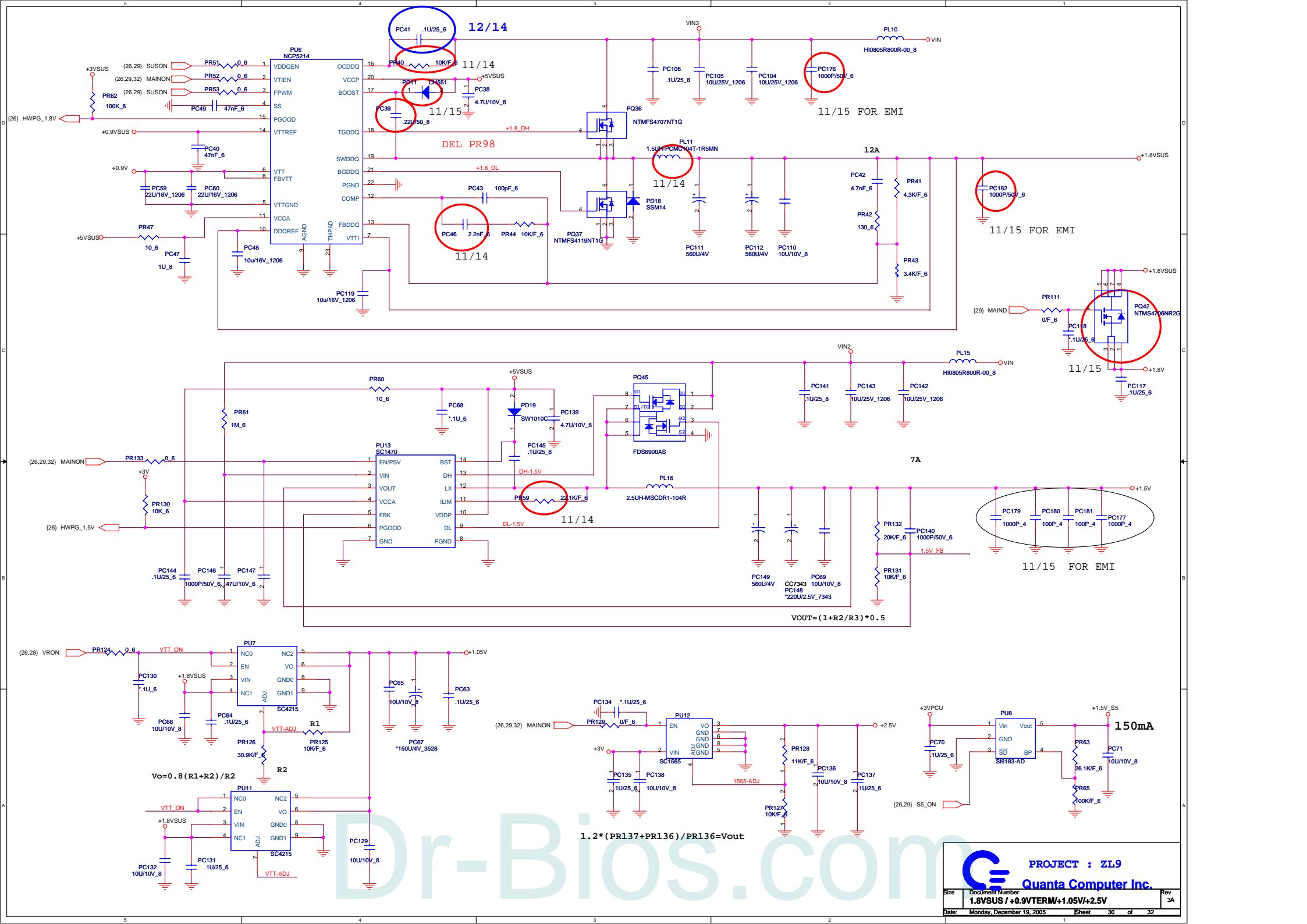
Size	Document Number	Rev
	CPU CORE (SC451)	3A
Date:	Monday, December 19, 2005	Sheet 28 of 32

AO4916 Rds on = 27mOhm
 ILOAD * Rds on * 10 = ILIM
 ILIM5 = 1.485V Current limit 5.5A
 ILIM3 = 1.35V Current limit 5A



PROJECT : ZL8
Quanta Computer Inc.

Size	Document Number	Rev
	5V/3.3V (MAX1999)	3A
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12/14

11/15 FOR EMI

11/15 FOR EMI

11/15

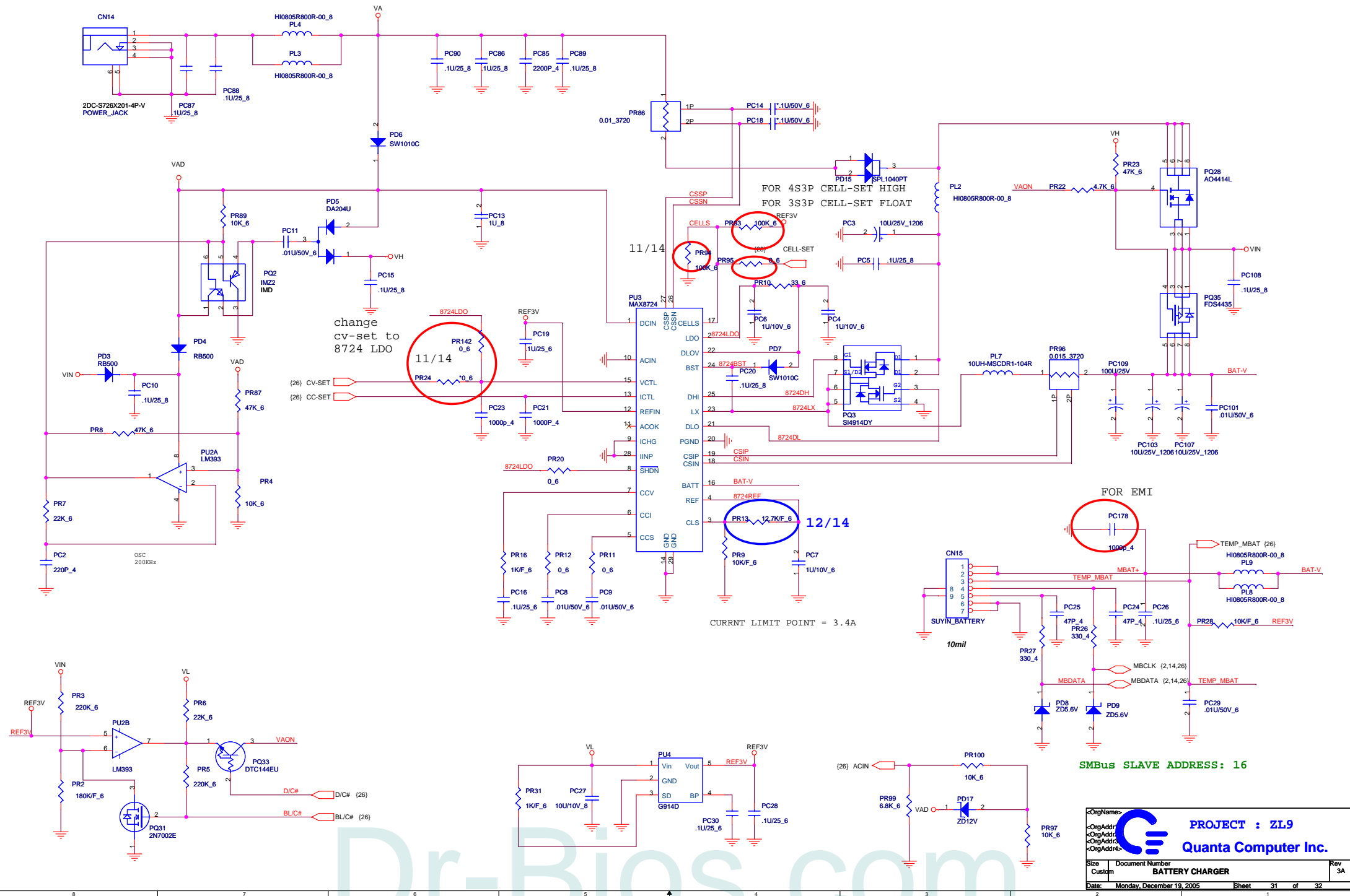
11/15 FOR EMI

$$V_o = 0.8 \cdot (R1 + R2) / R2$$

$$1.2 \cdot (PR137 + PR136) / PR136 = V_{out}$$

PROJECT : ZL9
Quanta Computer Inc.

Size	Document Number	Rev
	1.8VSUS / +0.9VTERM/+1.05V/+2.5V	3A
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change cv-set to 8724 LDO

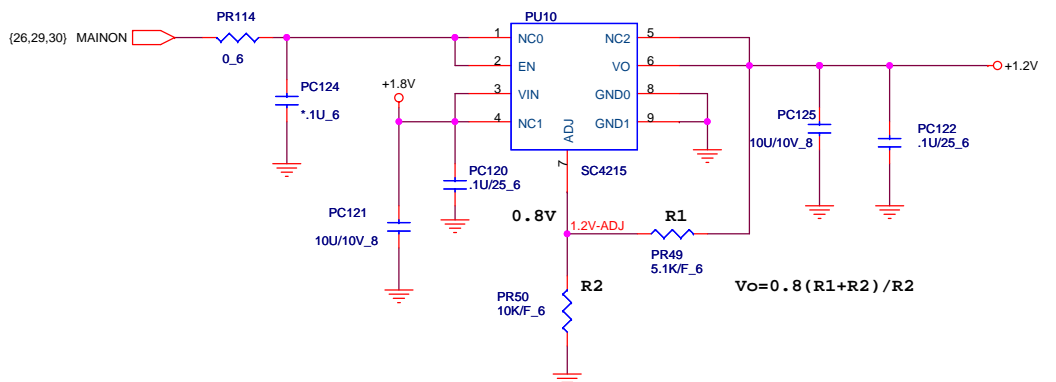
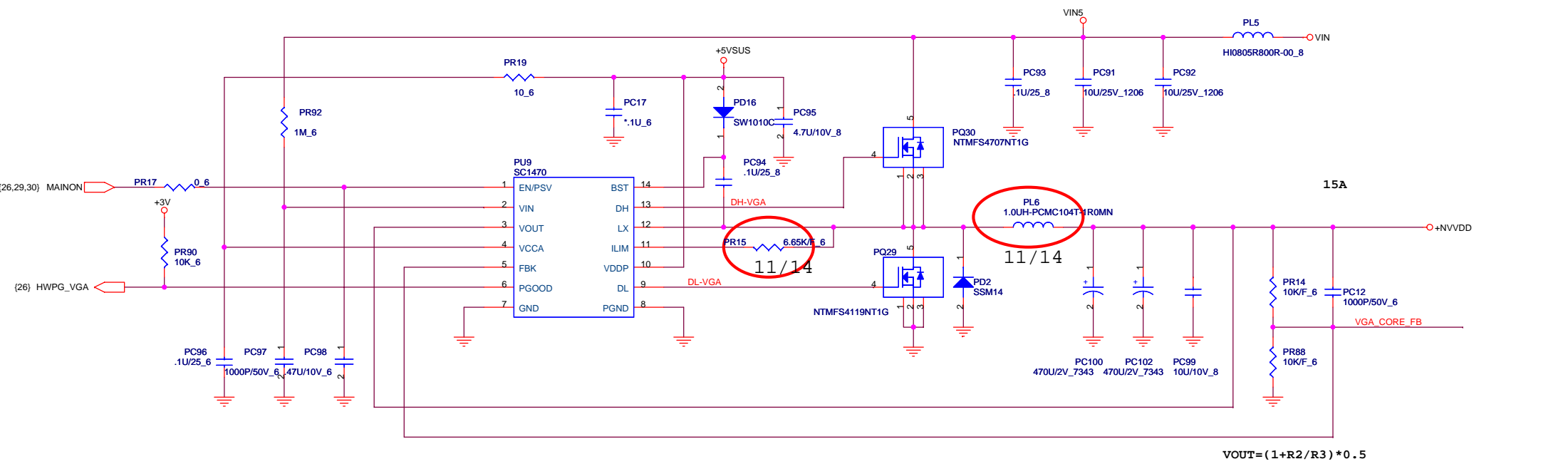
FOR 4S3P CELL-SET HIGH
FOR 3S3P CELL-SET FLOAT

CURRENT LIMIT POINT = 3.4A

FOR EMI

SMBus SLAVE ADDRESS: 16

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