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NAL00 Schematics Document

AMD L310/L110 Processor with RS780MN/SB710/M92-S2/S3 LP

2009-04-24

REV:0.2

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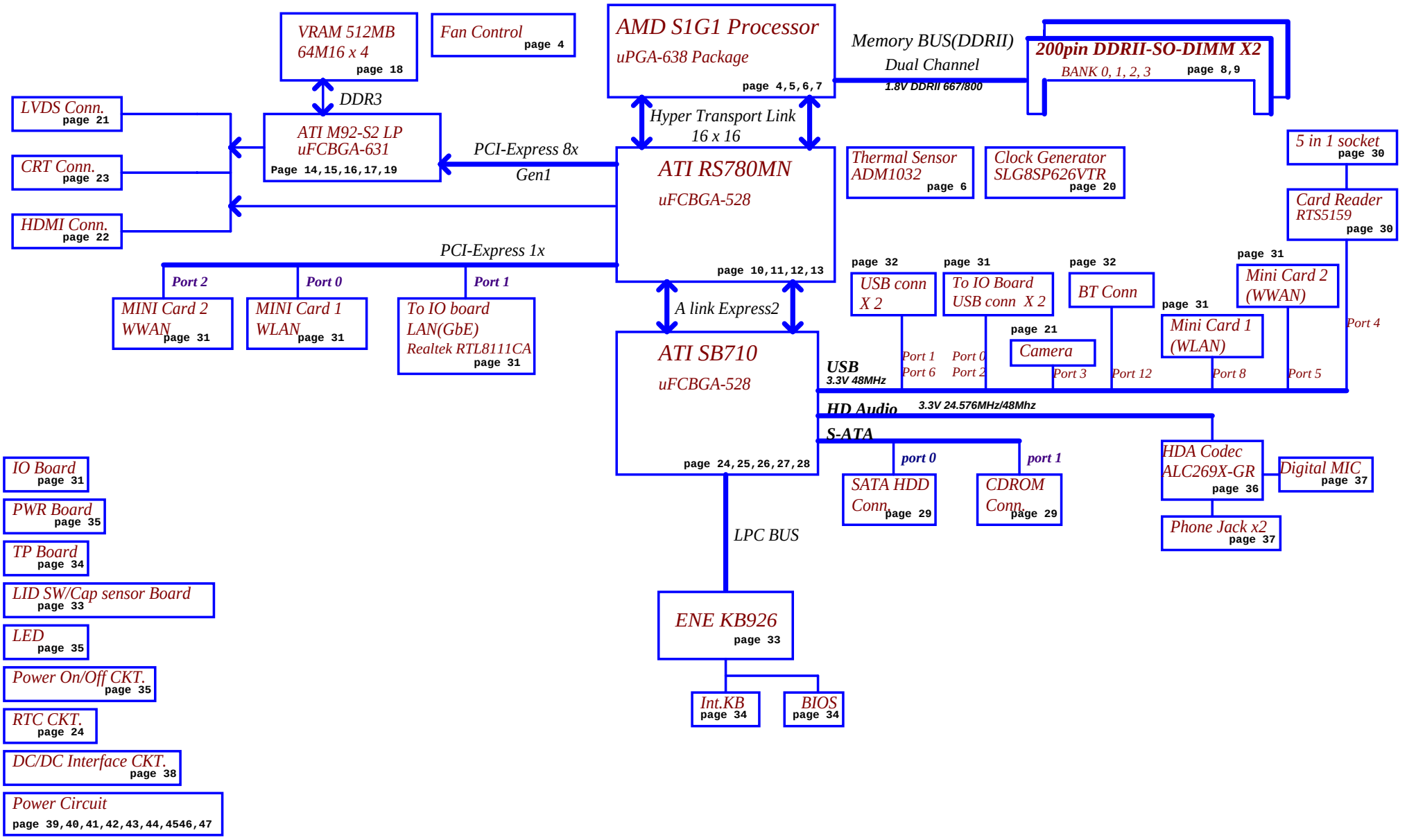
Model Name : NAL00



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+NB_CORE	1.0V switched power rail	ON	OFF	OFF
+0.9V	0.9V switched power rail for DDR terminator	ON	ON	OFF
+1.1VS	1.1V switched power rail for NB VDDC & VGA	ON	OFF	OFF
+1.2V_HT	1.2V switched power rail	ON	OFF	OFF
+VGA_CORE	0.90-0.95V switched power rail	ON	OFF	OFF
+1.5VS	1.5V power rail for PCIE Card	ON	OFF	OFF
+1.8V	1.8V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address	HEX
Smart Battery	0001 011X b	16H

EC SM Bus2 address

Device	Address	HEX
ADI ADM1032 (CPU)	1001 100X b	98H
SB-Temp Sensor		9CH

SB710 SM Bus 0 address

Device	Address	HEX
Clock Generator (SILEGO SLG8SP626)	1101 001Xb	D2
DDR DIMM1	1001 000Xb	90
DDR DIMM2	1001 010Xb	94
Mini card		

SB700 SM Bus 1 address

Device	Address
New card	

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
Discrete	VGA@
UMA	UMA@
UMA_HDMI	UMA_H@
Side port	SP@
JM51	JM@
HM52	HM@

	SB700	SB700	RS780MN	DISPLAY OUTPUT
	PX_GPIO0	PX_GPIO1	PX_GPIO2	
Function Description	dGPU_Reset	dGPU_PWR_Enable	PX Mode Switch	
IGP only mode	X	X	X	
PowerXpress mode	H : Enable	H : Enable	L : iGPU(DC) / H : dGPU(AC)	LVDS / CRT

	KB926					
	PX_GPIO1	PX_GPIO2	PX_+3VS	PX_+1.8VS	PX_+VGA_CORE	PX_GPIO2_NB
Function Description	Enable +1.1VS_PX	PX MODE SWITCH	Enable +3VS_DELAY	Enable +1.8VS_PX	Enable +VGA_CORE	Trigger from SB
IGP only mode	X	X	X	X	X	X
PowerXpress mode	H : Enable	Reserved	H : Enable	H : Enable	H : Enable	Reserved

	KB926
	PX_GPIO1_SB
Function Description	Trigger from SB to Enable (PX_GPIO1/PX_+3VS/PX_+1.8VS/PX_+VGA_CORE)
IGP only mode	X
PowerXpress mode	H : Enable

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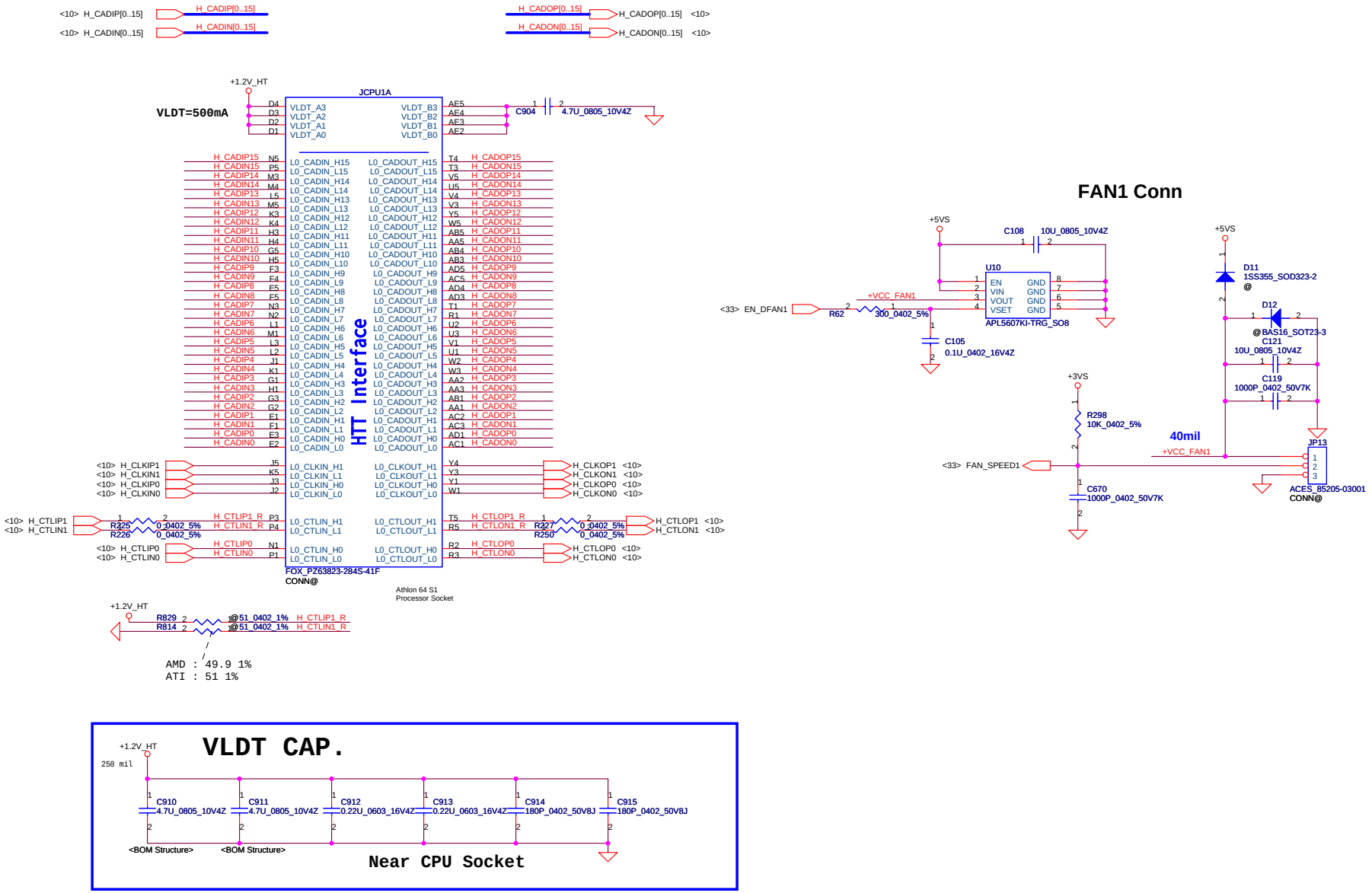

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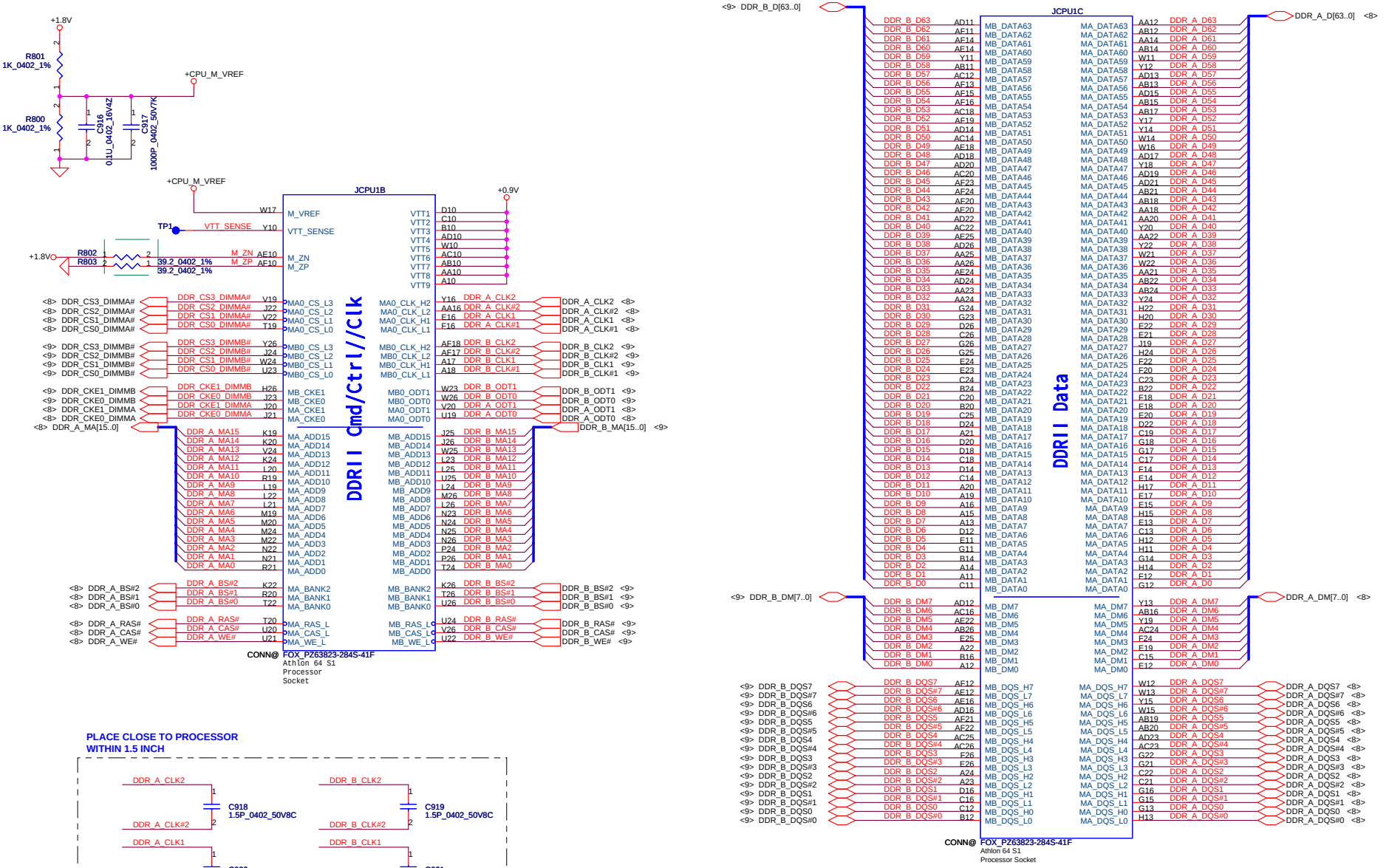
Processor DDR2 Memory Interface



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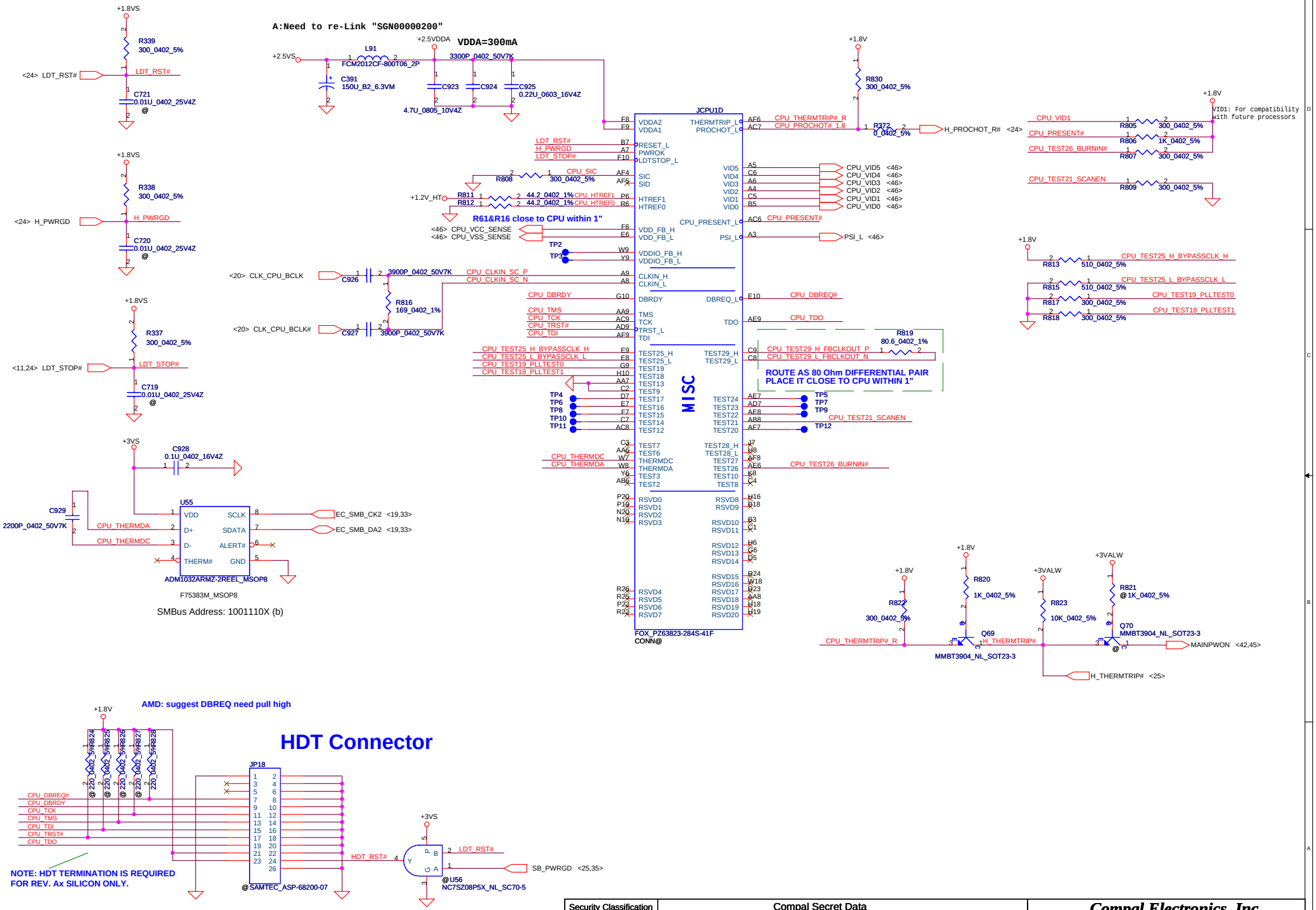

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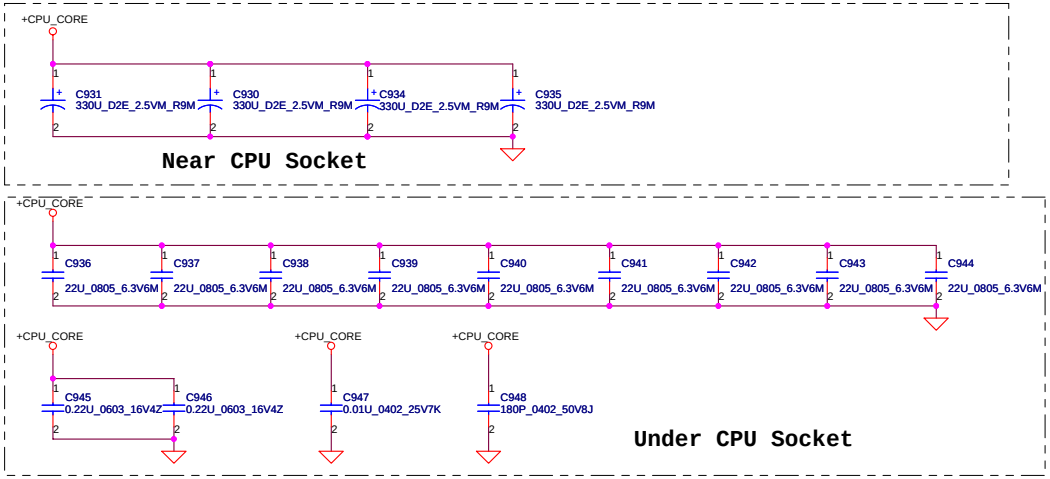
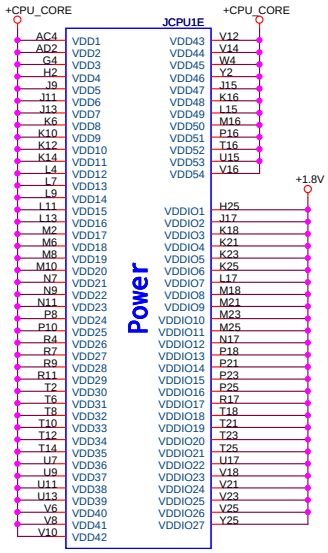
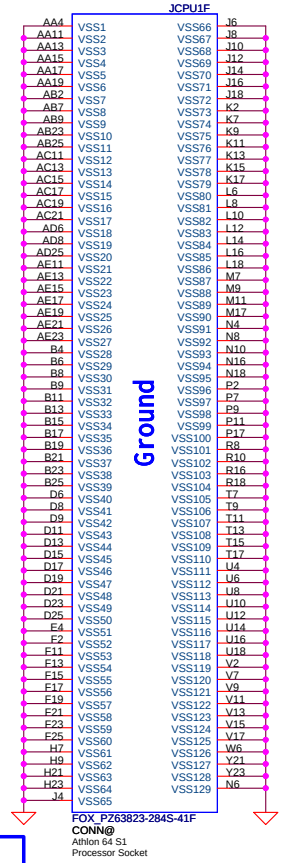
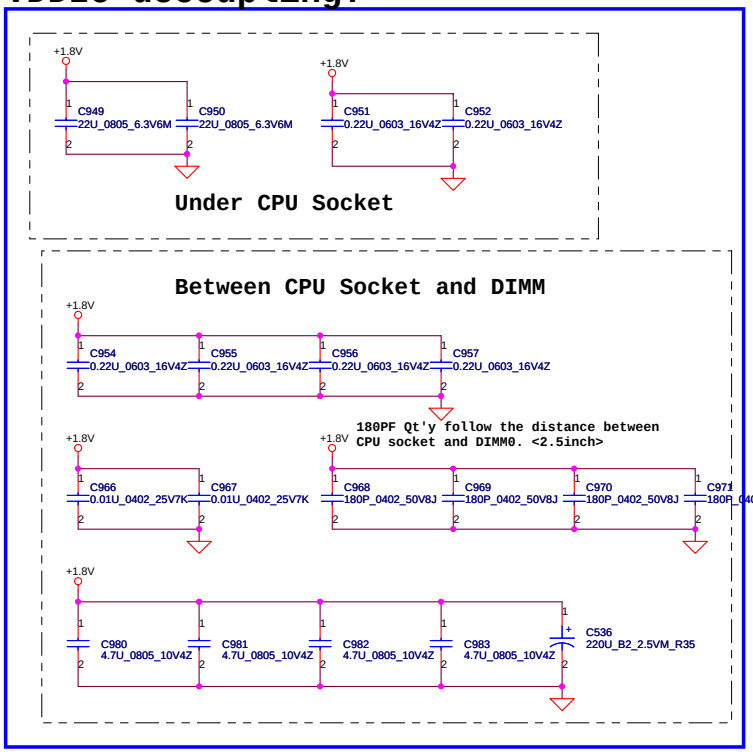
VDD(+CPU_CORE) decoupling.



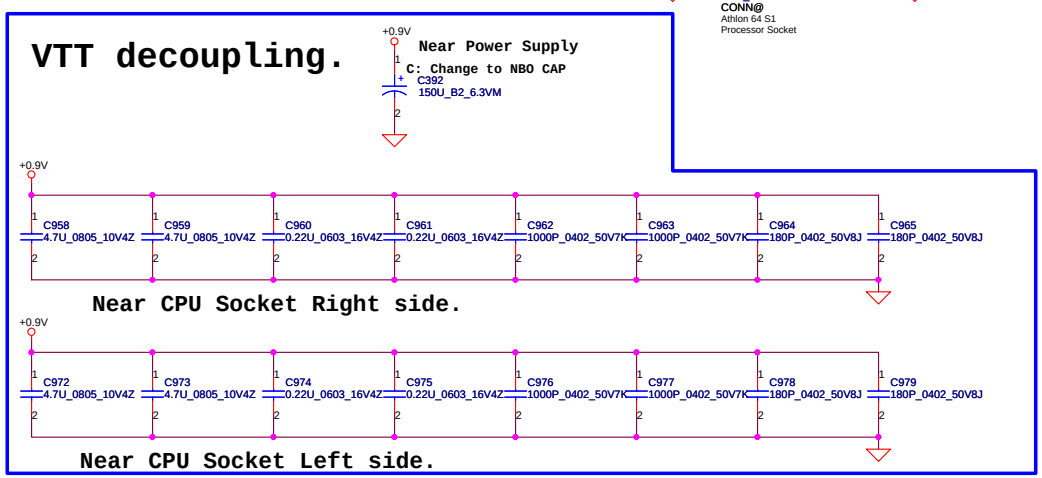




VDDIO decoupling.



VTT decoupling.



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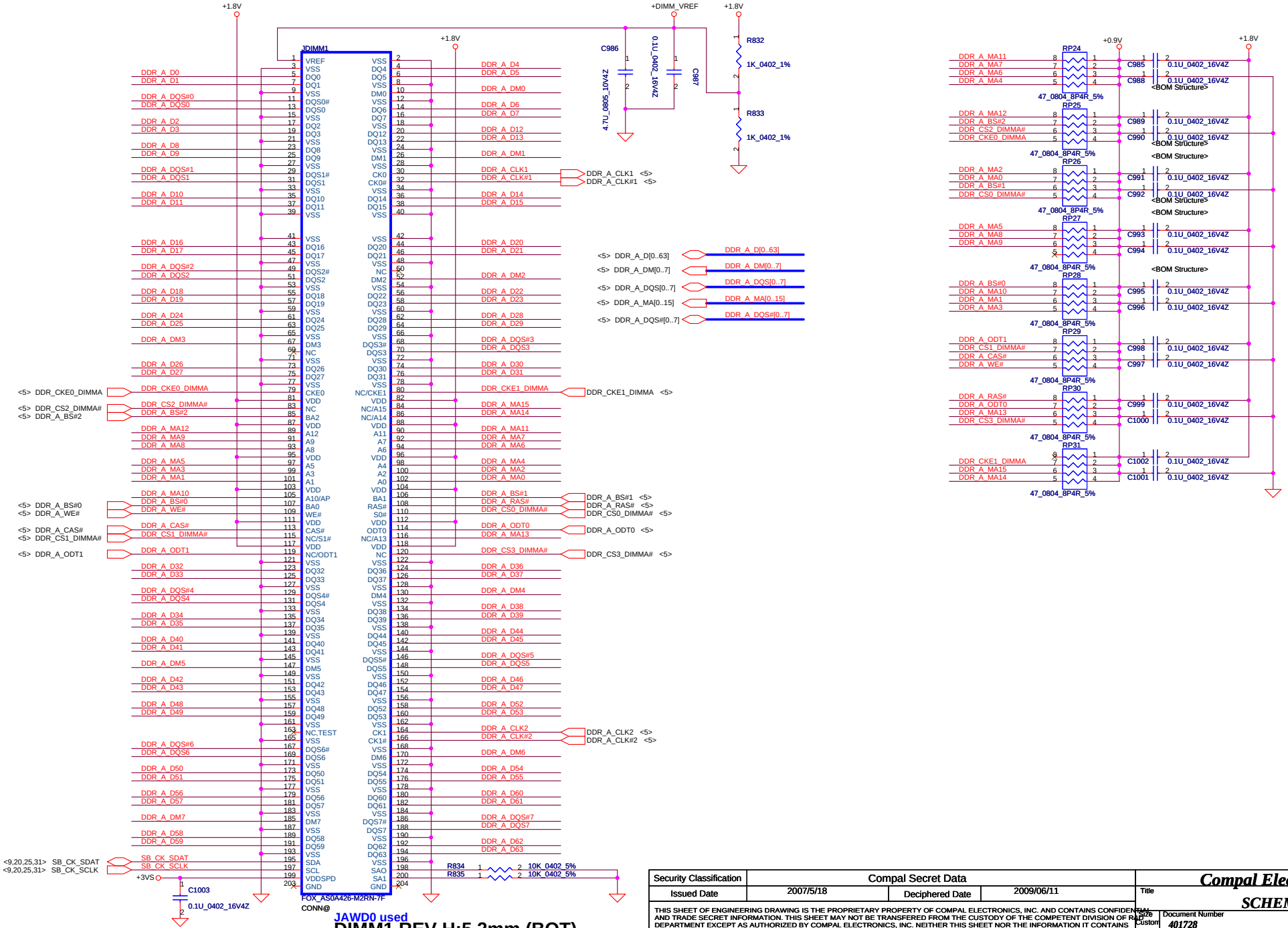

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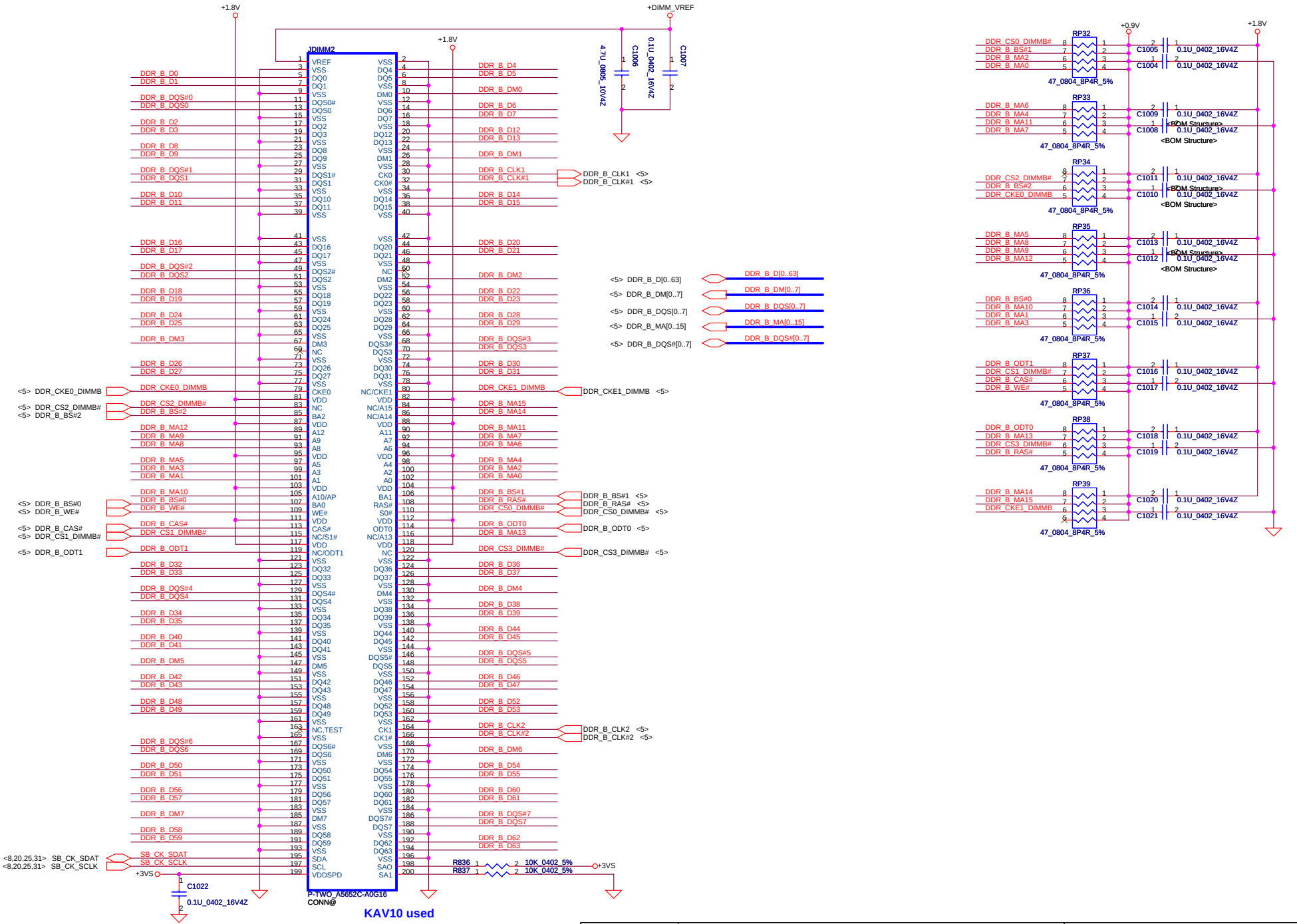

KAV10 used

DIMM2 H:5.2mm (BOT)

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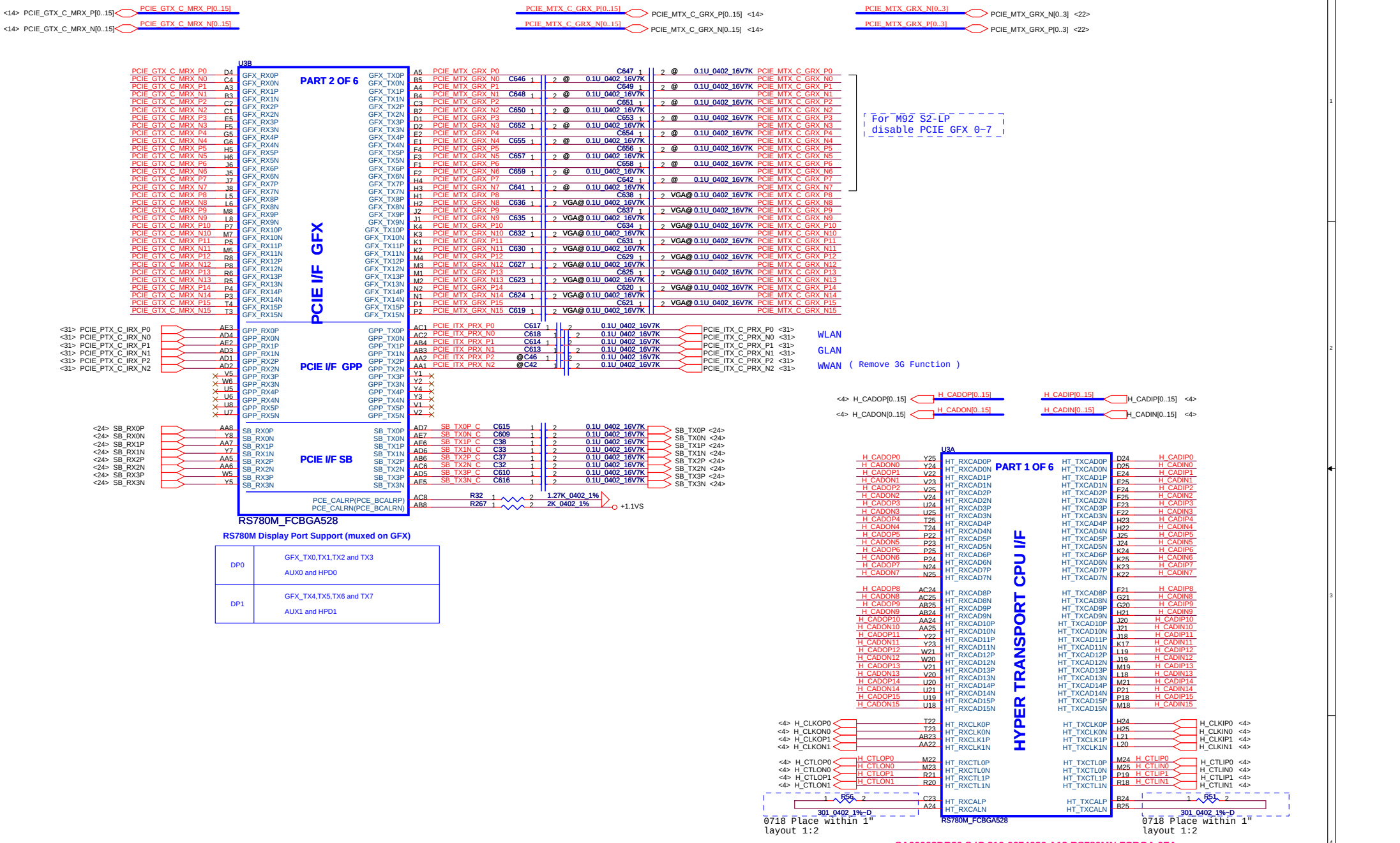

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For RS780M A13
RED: Connected to GND through two separate 140ohm 1% resistor

UMA@ R45 140_0402_1% GMCH_CRT_R
UMA@ R49 150_0402_1% GMCH_CRT_G
UMA@ R50 150_0402_1% GMCH_CRT_B

PLLVDD=65mA
+1.1VS L59 MBK2012221YZF 0805 +NB_PLLVDD
C645 2.2U_0603_6.3V4Z
C663 1U_0402_6.3V4Z

PLLVDD18=20mA
+1.8VS L13 MBK2012221YZF 0805 +NB_HTPVDD
C93 2.2U_0603_6.3V4Z
C84 1U_0402_6.3V4Z

VDDA18HTPLL=20mA
+1.8VS L9 MBK2012221YZF 0805 +VDDA18HTPLL
C66 2.2U_0603_6.3V4Z
C72 1U_0402_6.3V4Z

VDDA18PCIEPLL=0.12A
+1.8VS L14 MBK2012221YZF 0805 +VDDA18PCIEPLL
C87 2.2U_0603_6.3V4Z
C86 1U_0402_6.3V4Z

AVDD=0.11A
+3VS L15 FBM-L11-201209-300LMA30T_0805 +AVDD1
C94 2.2U_0603_6.3V4Z

AVDDDI=20mA
+1.8VS L10 FBM-L11-201209-300LMA30T_0805 +AVDD2
C74 0.1U_0402_16V4Z

AVDDQ=4mA
+1.8VS L8 FBM-L11-201209-300LMA30T_0805 +AVDDQ
C61 2.2U_0603_6.3V4Z

U3C
PART 3 OF 6
RS780M_FCBGA528

CRT/TVOUT
AVDD1(NC) F12
AVDD2(NC) E12
AVDDDI(NC) F14
AVSSDI(NC) G15
AVDDQ(NC) H15
AVSSQ(NC) H14
C_Pr(DFT_GPIO5) E17
Y(DFT_GPIO2) F17
COMP_Pb(DFT_GPIO4) F15
RED(DFT_GPIO0) G18
REDb(NC) G17
GREEN(DFT_GPIO1) E18
GREENb(NC) F18
BLUE(DFT_GPIO3) E19
BLUEb(NC) F19
DAC_HSYNC(PWM_GPIO4) A11
DAC_VSYNC(PWM_GPIO6) B11
DAC_SCL(PCE_RCALRN) E8
DAC_SDA(PCE_TCALRN) E8
DAC_RSET(PWM_GPIO1) G14
TXOUT_L0P(NC) A22
TXOUT_L0N(NC) B22
TXOUT_L1P(NC) A21
TXOUT_L1N(NC) B21
TXOUT_L2P(NC) B20
TXOUT_L2N(DBG_GPIO0) A20
TXOUT_L3P(NC) A19
TXOUT_L3N(DBG_GPIO2) B19
TXOUT_U0P(NC) B18
TXOUT_U0N(NC) A18
TXOUT_U1P(PCIE_RESET_GPIO3) A17
TXOUT_U1N(PCIE_RESET_GPIO2) B17
TXOUT_U2P(NC) D20
TXOUT_U2N(NC) D21
TXOUT_U3P(PCIE_RESET_GPIO5) D18
TXOUT_U3N(NC) D19
TXCLK_LP(DBG_GPIO1) B16
TXCLK_LN(DBG_GPIO3) A16
TXCLK_UP(PCIE_RESET_GPIO4) D16
TXCLK_UN(PCIE_RESET_GPIO1) D17

PLL PWR
PLLVDD(NC) A12
PLLVDD18(NC) D14
PLLVSS(NC) B12
VDDA18HTPLL H17
VDDA18PCIEPLL1 D7
VDDA18PCIEPLL2 E7

LVTM
VDDLTP18(NC) A13
VSSLTP18(NC) B13
VDDLT18_1(NC) A15
VDDLT18_2(NC) B15
VDDLT33_1(NC) A14
VDDLT33_2(NC) B14
VSSLT1(VSS) C14
VSSLT2(VSS) D15
VSSLT3(VSS) C16
VSSLT4(VSS) C18
VSSLT5(VSS) C20
VSSLT6(VSS) E20
VSSLT7(VSS) C22

PM
SYSRESETb D8
POWERGOOD A10
LDTSTOPb C10
ALLOW_LDTSTOP C12

CLOCKS
HT_REFCLKP C25
HT_REFCLKN C24
REFCLK_P/OSCIN(OSCIN) E11
REFCLK_N(PWM_GPIO3) F11
GFX_REFCLKP T2
GFX_REFCLKN T1
GPP_REFCLKP U1
GPP_REFCLKN U2
GPPSB_REFCLKP(SB_REFCLKP) V4
GPPSB_REFCLKN(SB_REFCLKN) V3
LVDS_DIGON(PCE_TCALRP) E9
LVDS_BLON(PCE_RCALRP) F7
LVDS_ENA_BL(PWM_GPIO2) G12

MIS.
I2C_CLK B9
I2C_DATA A9
DDC_DATA0/AUX0N(NC) B8
DDC_CLK0/AUX0P(NC) A8
DDC_CLK1/AUX1P(NC) B7
DDC_DATA1/AUX1N(NC) A7
STRP_DATA B10
RSVD G11
AUX_CAL(NC) C8
TMDS_HPD(NC) D9
HPD(NC) D10
SUS_STAT#(PWM_GPIO5) D12
THERMALDIODE_P AE8
THERMALDIODE_N AD8
TESTMODE D13

<23> GMCH_CRT_R
<23> GMCH_CRT_G
<23> GMCH_CRT_B
<13,23> GMCH_CRT_HSYNC
<13,23> GMCH_CRT_VSYNC
<23> GMCH_CRT_CLK
<23> GMCH_CRT_DATA
R42 715_0402_1%
+NB_PLLVDD
+NB_HTPVDD
+VDDA18HTPLL
+VDDA18PCIEPLL
<13,14,24,31,33> PLT_RST#
<25> NB_PWRGD
R298 0_0402_5%
NB_RESET#
NB_LDTSTOP#
NB_ALLOW_LDTSTOP
+1.8VS R283 300_0402_5%
<20> CLK_NBHT
<20> CLK_NBHT#
<20> CLK_NB_14.318M
CLK_NB_14.318M
<20> CLK_NBGFX
<20> CLK_NBGFX#
<20> CLK_SBLINK_BCLK
<20> CLK_SBLINK_BCLK#
<21> GMCH_LCD_CLK
<21> GMCH_LCD_DATA
GMCH_LCD_CLK
GMCH_LCD_DATA
GMCH_HDMI_DATA_R2
GMCH_HDMI_CLK_R2
GMCH_HDMI_CLK_R1
GMCH_HDMI_DATA_R1
DVT
+3VS R288 @ 10K_0402_5%
<43> POWER_SEL
POWER_SEL
<13> AUX_CAL
Strap pin

CLK_NB_14.318M
R477 100_0402_5% @
C854 100P_0402_25V8K @
+1.1VS R293 4.7K_0402_5%
R290 4.7K_0402_5%

	POWER_SEL
HIGH	1.0V
LOW	1.1V

+3VS R295 4.7K_0402_5% GMCH_LCD_CLK
R289 4.7K_0402_5% GMCH_LCD_DATA

Un-stuff for Tigris
Change as 1K_5% ohm for Tigris
+1.8VS R60 300_0402_5%
<24> ALLOW_LDTSTOP R59 0_0402_5% NB_ALLOW_LDTSTOP

DVT
R491 @ 0_0402_5% GMCH_HDMI_CLK_R2
<22> GMCH_HDMI_CLK
<22> GMCH_HDMI_DATA
GMCH_HDMI_CLK
GMCH_HDMI_DATA
R488 UMA@ 0_0402_5% GMCH_HDMI_CLK_R1
R489 UMA@ 0_0402_5% GMCH_HDMI_DATA_R1
R492 @ 0_0402_5% GMCH_HDMI_DATA_R2

<6,24> LDT_STOP# 0_0402_5% R280 NB_LDTSTOP#

<21> GMCH_TXOUT0+
<21> GMCH_TXOUT0-
<21> GMCH_TXOUT1+
<21> GMCH_TXOUT1-
<21> GMCH_TXOUT2+
<21> GMCH_TXOUT2-
<21> GMCH_TZOUT0+
<21> GMCH_TZOUT0-
<21> GMCH_TZOUT1+
<21> GMCH_TZOUT1-
<21> GMCH_TZOUT2+
<21> GMCH_TZOUT2-
<21> GMCH_TXCLK+
<21> GMCH_TXCLK-
<21> GMCH_TZCLK+
<21> GMCH_TZCLK-

VDDLTP18=15mA
+VDDLTP18 L56 MBC1608121YZF_0603 +1.8VS
C665 1U_0402_6.3V4Z
C644 2.2U_0603_6.3V4Z

VDDLT18=0.3A
+VDDLT18 L12 MBC1608121YZF_0603 +1.8VS
C90 0.1U_0402_16V4Z
C95 4.7U_0805_10V4Z

+VDDLTP18
+VDDLT18

UMA_ENVDD
UMA_ENBKL <21>
UMA_DPST
R469 1.27K_0402_1% @
R294 1.27K_0402_1%
R295 1.27K_0402_1%
UMA@
DVT

AMD Vari bright function
UMA_DPST R758 @0_0402_5% ENBKL

HDMI_DET <15,22>
SUS_STAT# <25>
SUS_STAT_R# <13> Strap pin
R297 0_0402_5%
R279 1.8K_0402_5%

R744 0_0402_5%
+3VS
C857 0.1U_0402_16V4Z
UMA_ENVDD
U48 NC7SZ08P5X_NL_SC70-5 @
UMA_ENVDD_R <21>
NB_PWRGD
UMA_ENBKL
U49 NC7SZ08P5X_NL_SC70-5 UMA@
ENBKL <33>

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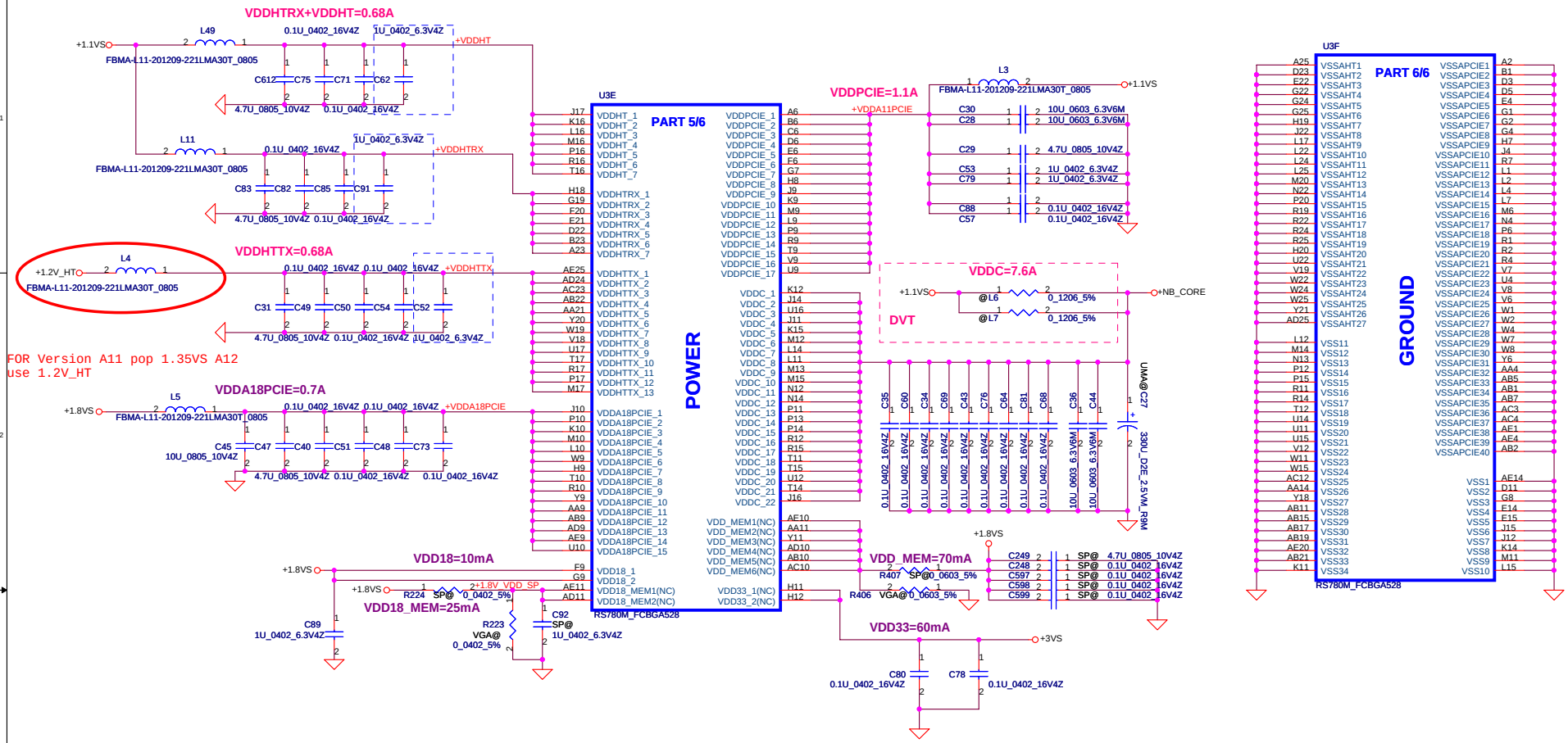

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DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO. (VSYNC)
1 : Disable (RS780)
0 : Enable (Rs780)

<11,23> GMCH_CRT_VSYNC — R286 3K_0402_5% — +3VS
R287 @ 3K_0402_5%

DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected
RS740/RX780: DFT_GPIO1 RS780:SUS_STAT

<11> AUX_CAL — @R284 150_0402_1%
RS780 DFT_GPIO1
D29 @ CH751H-40_SC76
<11> SUS_STAT_R# — PLT_RST# <11,14,24,31,33>
R299 @ 3K_0402_5%

RS780 use HSYNC to enable SIDE PORT

RS740/RS780: Enables Side port memory (RS780 use HSYNC#)
0. Enable (RS780)
1 : Disable(RS780)

RS780 use HSYNC to enable SIDE PORT

<11,23> GMCH_CRT_HSYNC — R281 VGA@ 3K_0402_5% — +3VS
R282 SP@ 3K_0402_5%

U61
MEM_BA0 MEM_BA1 MEM_A12 MEM_A11 MEM_A10 MEM_A9 MEM_A8 MEM_A7 MEM_A6 MEM_A5 MEM_A4 MEM_A3 MEM_A2 MEM_A1 MEM_A0
BA0 BA1 A12 A11 A10/AP A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
DQ15 DQ14 DQ13 DQ12 DQ11 DQ10 DQ9 DQ8 DQ7 DQ6 DQ5 DQ4 DQ3 DQ2 DQ1 DQ0
MEM_DQ12 MEM_DQ13 MEM_DQ9 MEM_DQ14 MEM_DQ15 MEM_DQ8 MEM_DQ10 MEM_DQ11 MEM_DQ5 MEM_DQ2 MEM_DQ6 MEM_DQ1 MEM_DQ0 MEM_DQ4 MEM_DQ3 MEM_DQ7
MEM_CLKN MEM_CLKP R135 SP@ 100_0402_1%
CK CK CKE MEM_CKE
CS MEM_CS# WE MEM_WE# RAS MEM_RAS# CAS MEM_CAS#
LDM MEM_DM0 UDM MEM_DM1 ODT MEM_ODT
LDQS MEM_DQS_P0 LDQS MEM_DQS_N0 UDQS MEM_DQS_P1 UDQS MEM_DQS_N1
VREF +MEM_VREF
NC MEM_BA2
VDDQ +1.8V_MEM_VDDQ
VDDL VSSDL — SP@ L23 FBMA-L11-160808-221LMT 0603 — +1.8V_MEM_VDDQ
C184 SP@ 1U_0402_6.3V4Z
Layout Note: 50 mil for VSSDL
VSSQ VSS
HY5PS561621AFP-25_FBGA84
Support 8M x 16bit x 8 bank side port

03/16 SA000031O00 S IC D2 64M16/500 K4N1G164QE-HC20 FBGA84
03/16 SA00002UH00 S IC D2 64M16/500 H5PS1G63EFR-20L FBGA84

U3D
PAR 4 OF 6
SBD_MEM/DVO_I/F
MEM_A0 MEM_A1 MEM_A2 MEM_A3 MEM_A4 MEM_A5 MEM_A6 MEM_A7 MEM_A8 MEM_A9 MEM_A10 MEM_A11 MEM_A12
MEM_BA0 MEM_BA1 MEM_BA2
MEM_RAS# MEM_CAS# MEM_WE# MEM_CS# MEM_CKE MEM_ODT
MEM_CLKP MEM_CLKN
MEM_COMP_P MEM_COMP_N
MEM_DQ0/DVO_VSYNC(NC) MEM_DQ1/DVO_HSYNC(NC) MEM_DQ2/DVO_DE(NC) MEM_DQ3/DVO_D0(NC) MEM_DQ4(NC) MEM_DQ5/DVO_D1(NC) MEM_DQ6/DVO_D2(NC) MEM_DQ7/DVO_D4(NC) MEM_DQ8/DVO_D3(NC) MEM_DQ9/DVO_D5(NC) MEM_DQ10/DVO_D6(NC) MEM_DQ11/DVO_D7(NC) MEM_DQ12(NC) MEM_DQ13/DVO_D9(NC) MEM_DQ14/DVO_D10(NC) MEM_DQ15/DVO_D11(NC)
MEM_DQS0P/DVO_IDCKP(NC) MEM_DQS0N/DVO_IDCKN(NC) MEM_DQS1P(NC) MEM_DQS1N(NC)
MEM_DM0(NC) MEM_DM1/DVO_D8(NC)
IOPLLVDD18(NC) IOPLLVDD(NC) IOPLLVSS(NC) MEM_VREF(NC)
MEM_DQ0 MEM_DQ1 MEM_DQ2 MEM_DQ3 MEM_DQ4 MEM_DQ5 MEM_DQ6 MEM_DQ7 MEM_DQ8 MEM_DQ9 MEM_DQ10 MEM_DQ11 MEM_DQ12 MEM_DQ13 MEM_DQ14 MEM_DQ15
MEM_DQS_P0 MEM_DQS_N0 MEM_DQS_P1 MEM_DQS_N1
MEM_DM0 MEM_DM1
RS780M_FCBGA528
+1.8VS=W/S=20/10mil For Memory PLL power
+1.1VS=W/S=20/10mil For Memory PLL power
15mA
26mA
FBMA-L11-160808-221LMT 0603 L22 +1.1VS1
L21 FBMA-L11-160808-221LMT 0603 +1.8VS
C185 SP@ 2.2U_0603_6.3V4Z
C183 SP@ 2.2U_0603_6.3V4Z
+1.8V_MEM_VDDQ R140 SP@ 40.2_0402_1% MEM_COMP_P
+1.8V_MEM_VDDQ R136 SP@ 40.2_0402_1% MEM_COMP_N

220 ohm @ 100MHz,2A
+1.8V_MEM_VDDQ +1.8VS L16 SP@ 0_0805_5%
C628 SP@ 1U_0402_6.3V4Z
C626 SP@ 1U_0402_6.3V4Z
C201 SP@ 1U_0402_16V4Z
C206 SP@ 0.1U_0402_16V4Z
C208 SP@ 0.1U_0402_16V4Z
C202 SP@ 22U_0805_6.3V6M

+1.8V_MEM_VDDQ
C195 SP@ 0.1U_0402_16V4Z
R118 SP@ 1K_0402_1%
+MEM_VREF
C207 SP@ 0.1U_0402_16V4Z
R119 SP@ 1K_0402_1%

+1.8V_MEM_VDDQ
C197 SP@ 0.1U_0402_16V4Z
R117 SP@ 1K_0402_1%
+MEM_VREF1
C200 SP@ 0.1U_0402_16V4Z
R120 SP@ 1K_0402_1%

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Issued Date	2008/10/06	Deciphered Date	2009/10/06

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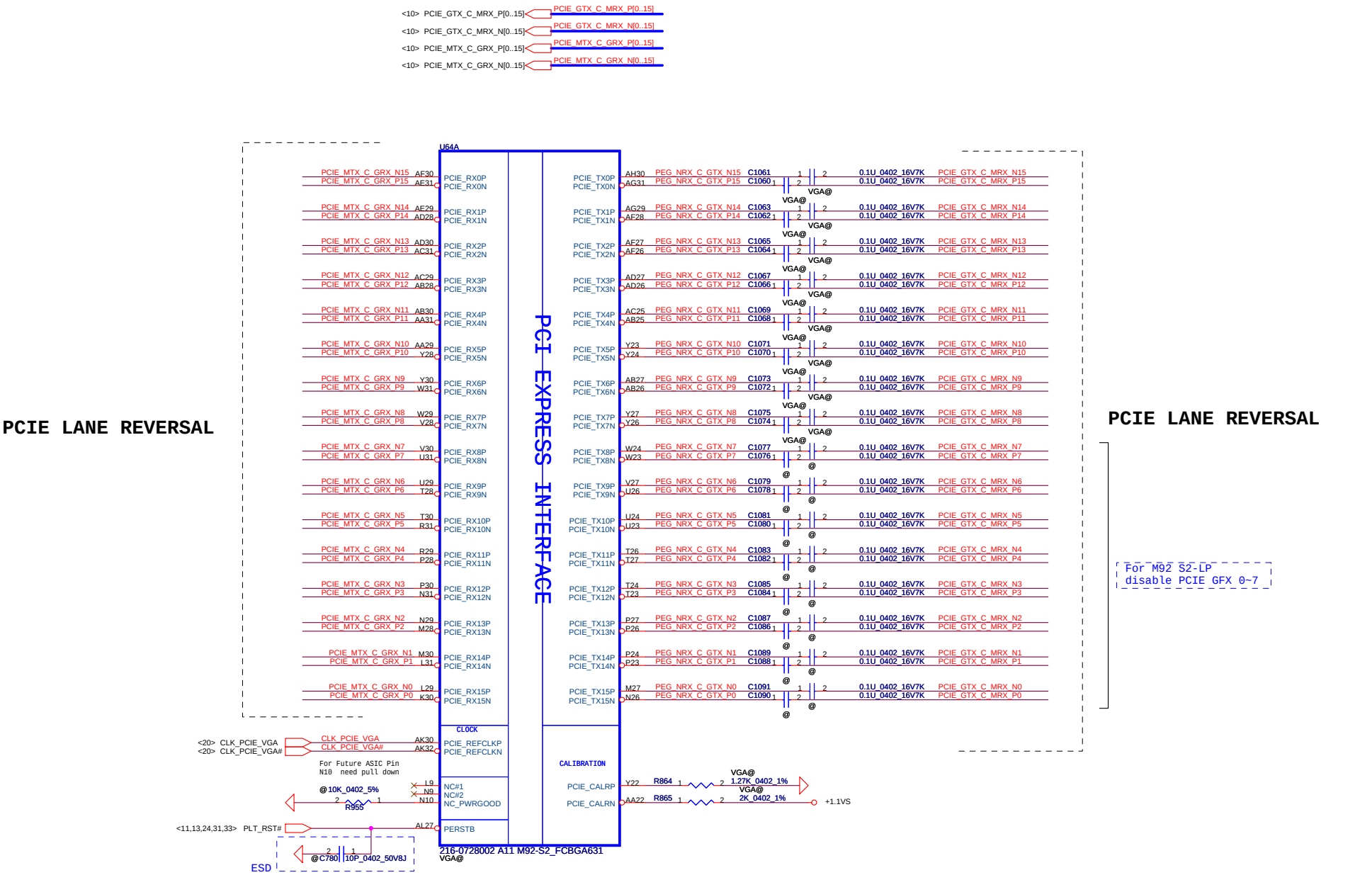

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Issued Date	2007/10/11	Deciphered Date	200810/11

Compal Electronics, Inc.			
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Size	Document Number: 401728		Rev: A
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For M92-S2: DO NOT Install any Component in this Box.

LCD

10/24 Reference AMD REF136-1

Do not use Back Bais than pull high to +VDDC

CRT

HDMI

DO NOT INSTALL for M93-S3

Close to M92

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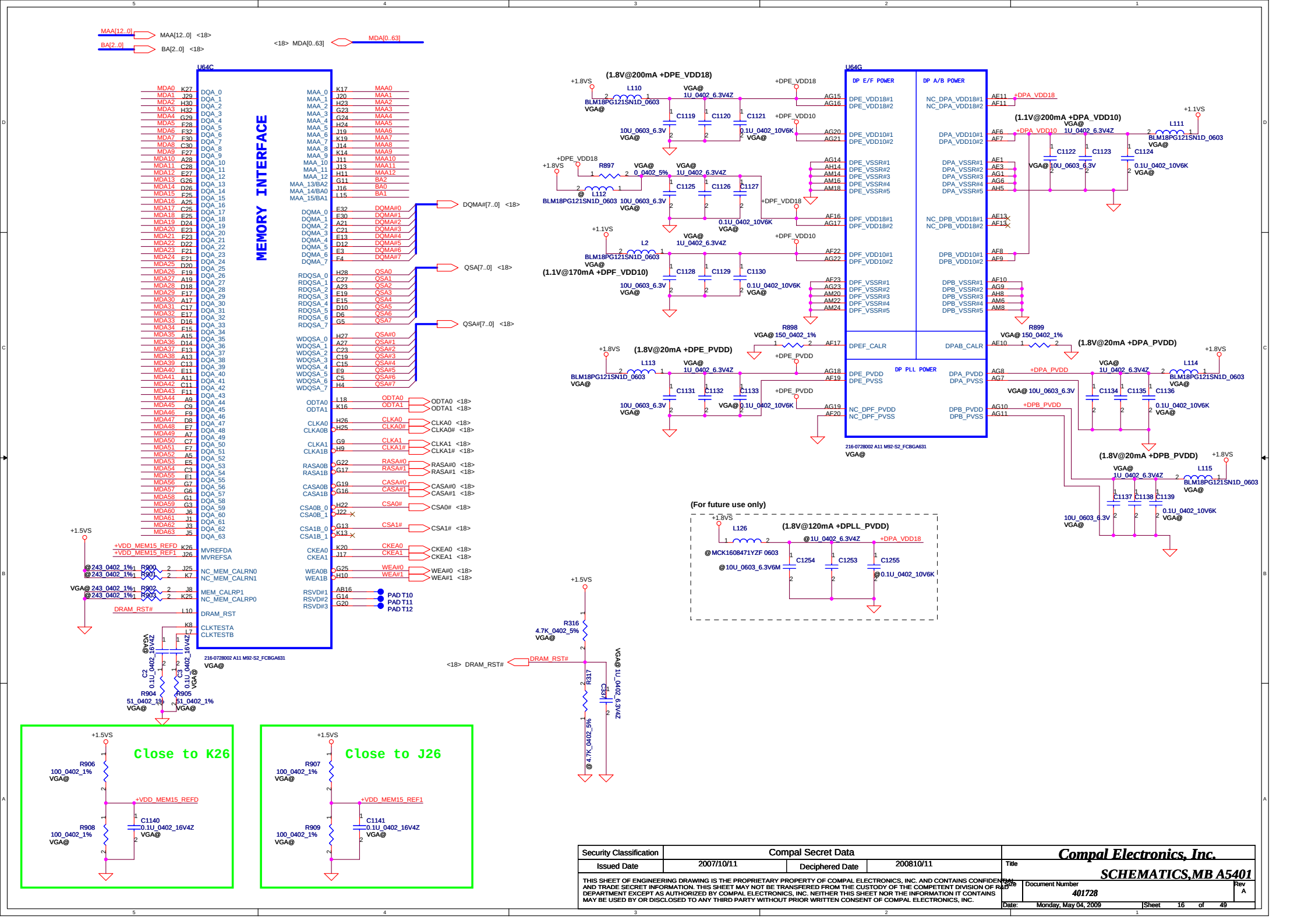
MAA[12..0]
MAA[12..0] <18>
BA[2..0]
BA[2..0] <18>
<18> MDA[0..63]
MDA[0..63]
U64C
MEMORY INTERFACE
DQMA#[7..0] <18>
QSA[7..0] <18>
QSA#[7..0] <18>
ODTA0 <18>
ODTA1 <18>
CLKA0 <18>
CLKA0# <18>
CLKA1 <18>
CLKA1# <18>
RASA#0 <18>
RASA#1 <18>
CASA#0 <18>
CASA#1 <18>
CSA0# <18>
CSA1# <18>
CKEA0 <18>
CKEA1 <18>
WEA#0 <18>
WEA#1 <18>
PAD T10
PAD T11
PAD T12
+1.5VS
+VDD_MEM15_REFD
+VDD_MEM15_REF1
DRAM_RST#
<18> DRAM_RST#
216-0728002 A11 M92-S2_FCBGA631
VGA@
(1.8V@200mA +DPE_VDD18)
(1.1V@170mA +DPF_VDD10)
(1.8V@20mA +DPE_PVDD)
(1.1V@200mA +DPA_VDD10)
(1.8V@20mA +DPA_PVDD)
(1.8V@20mA +DPB_PVDD)
(For future use only)
(1.8V@120mA +DPLL_PVDD)
Close to K26
Close to J26
Security Classification
Compal Secret Data
Issued Date
2007/10/11
Deciphered Date
200810/11
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Rev
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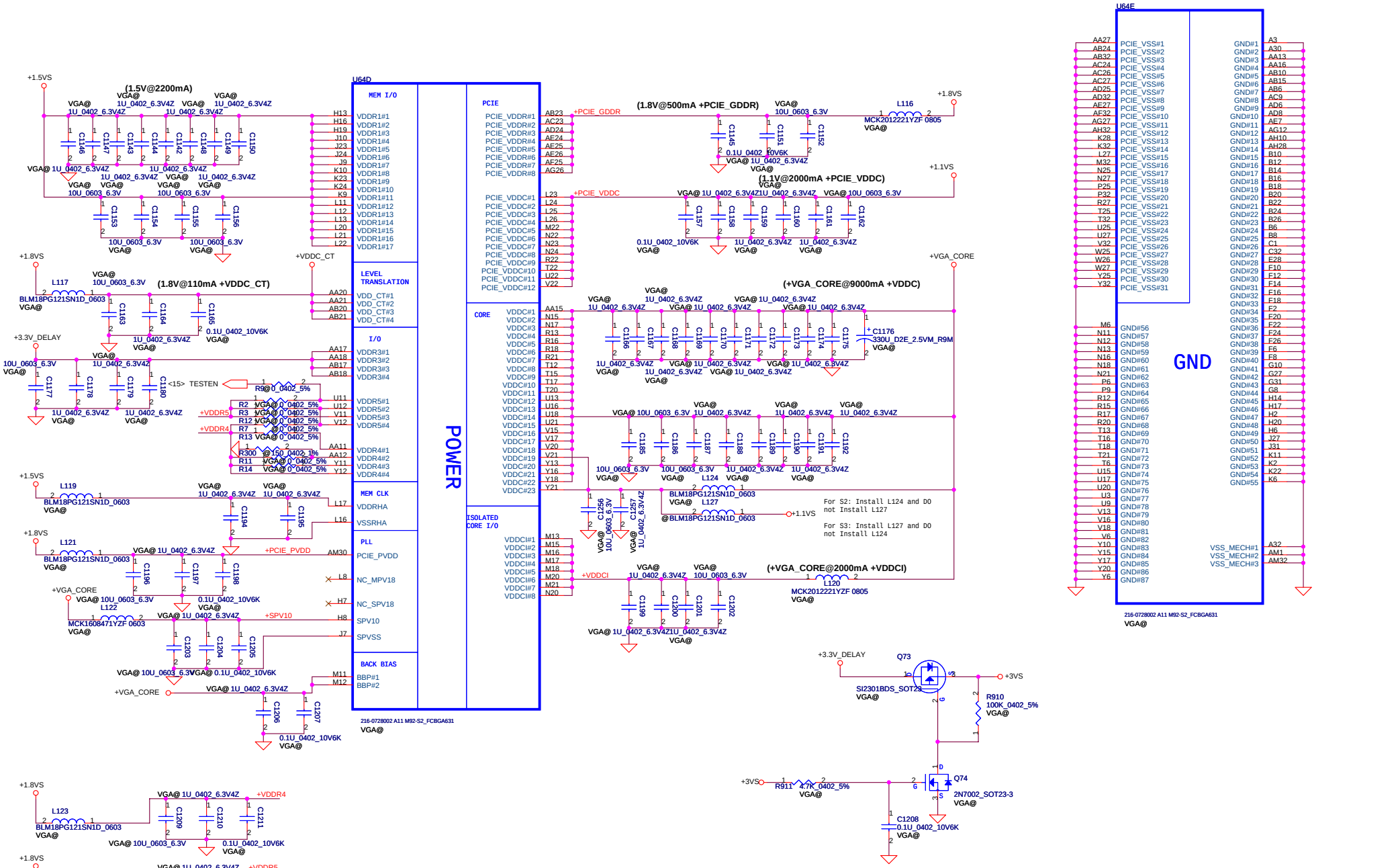

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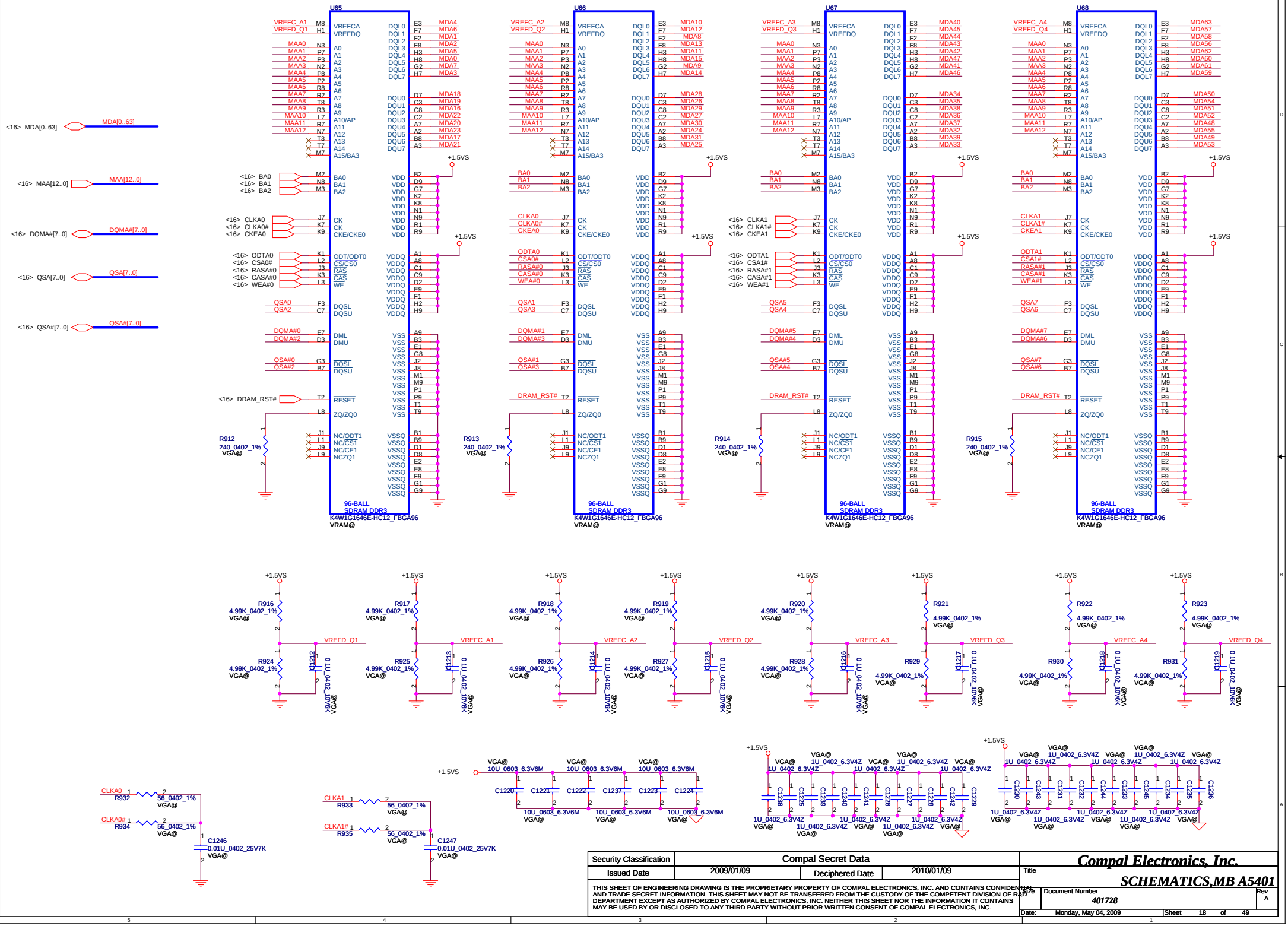

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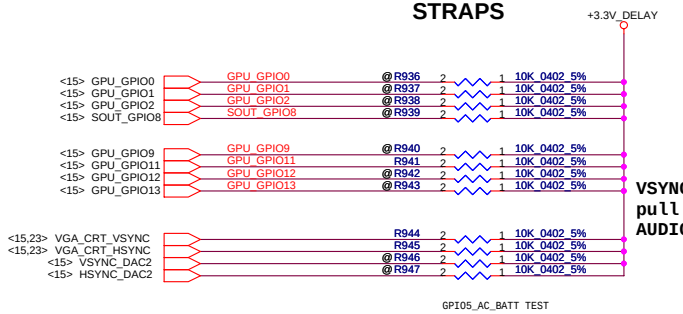
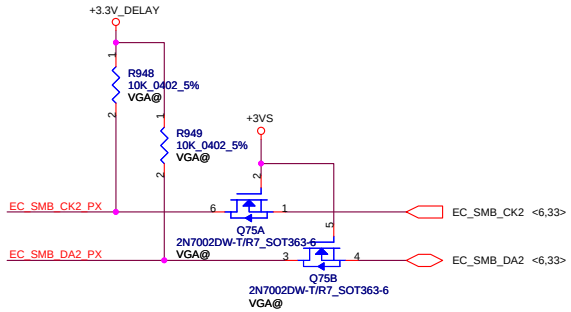
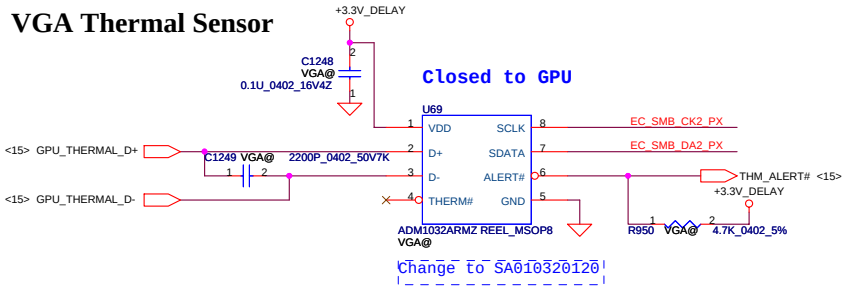
STRAPS



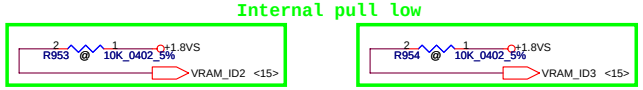
VSYNC_DAC1 and HSYNC_DAC1 pull up to HDMI & DISPLAYPORT AUDIO funciton



VGA Thermal Sensor



Internal pull low



CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	1
BIF_GEN2_EN_A	GPIO2	PCIE GNE2 ENABLED	1
BIF_CLK_PM_EN	GPIO8	BIF_CLK_PM_EN	0
BIF_VGA DIS	GPIO9	VGA ENABLED	0
BIF_RX_PLL_CALIB_BP	GPIO21		0
BIOS_ROM_EN	GPIO_22_ROMCSB		1
ROMIDCFG(2:0)	GPIO[13:11]	BIF_RX_PLL_CALIB_BP	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	ENABLE EXTERNAL BIOS ROM	0
SMS_EN_HARD	H2SYNC	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0
CCBYPASS	GENERICC	IGNORE VIP DEVICE STRAPS	0
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	X X

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO_28_TDO GPIO21_BB_EN

VRAM_ID0=VRAM_ID0_0
VRAM_ID1=VRAM_ID1_1
VRAM_ID2=VRAM_ID2_2
VRAM_ID3=VRAM_ID3_3

STRAPS	PIN	GPU	Project	VRAM size	Vendor Part Number#	Compal Part Number#	VRAM_ID 3,2,1,0
VRAM_ID[3:0]	DVPDATA (3,2,1,0)	M92 S2-LP	JM51_PU	512MB(x4)	Samsung 64Mx16 1.5V	SA000035700	0 0 0 0
							0 0 0 1
			JM51_PU	512MB(x4)	Hynix 64Mx16 1.5V	SA000032400	0 0 1 0
							0 0 1 1
							0 1 0 0
							0 1 0 1

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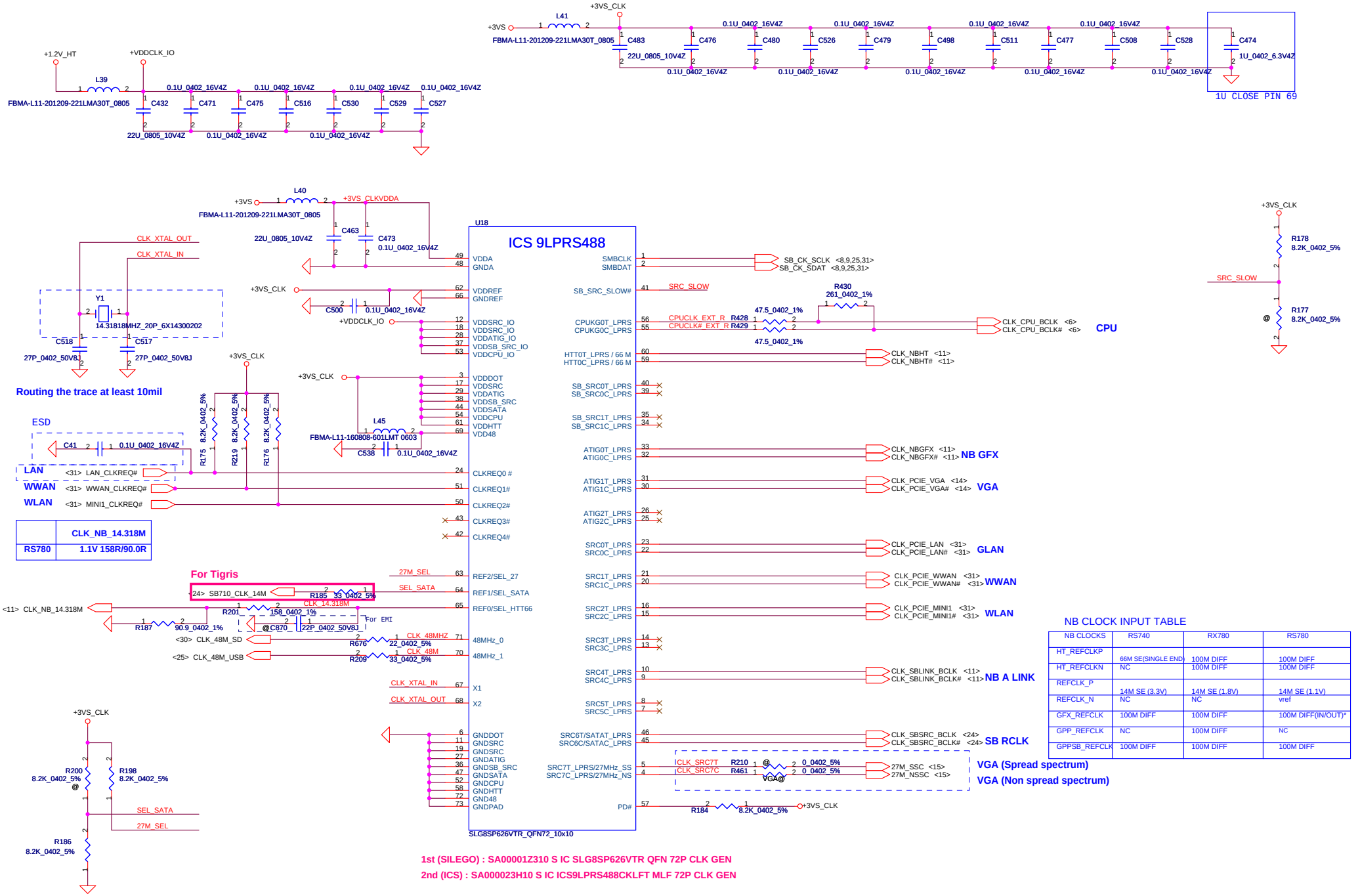

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	NC	100M DIFF	NC
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

SEL_HTT66		
	1	single-ended 66MHz HTT output
	0*	differential 100MHz HTT output

SEL_SATA		
	1*	NON SPREAD 100M_SATA SRC6 output
	0	SPREAD 100M_SATA SRC6 output

* default

27M_SEL		
	1 *	NON SPREAD 27M and SPREAD 27M output
	0	differential spread SRC_7 output

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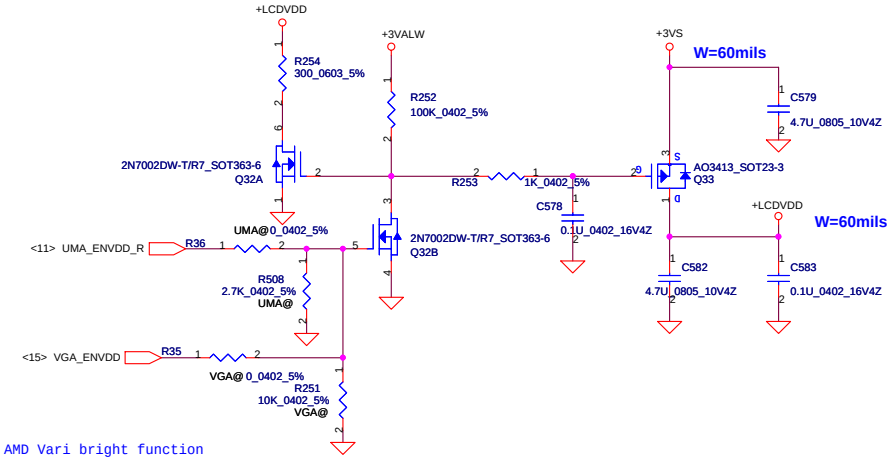
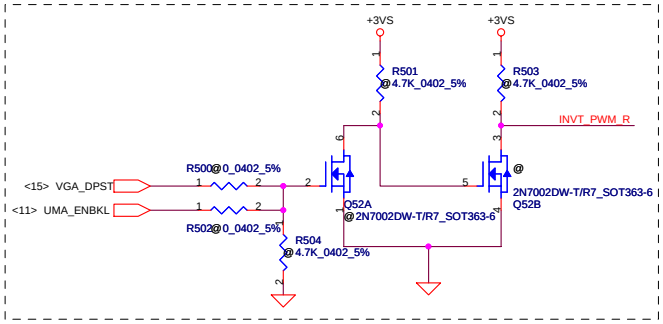
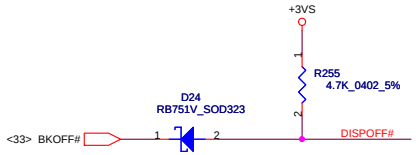
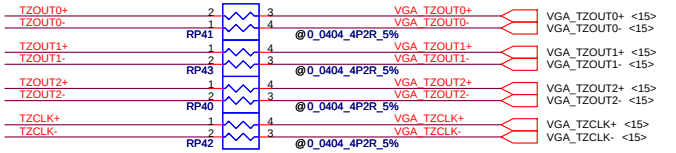
LCD POWER CIRCUIT

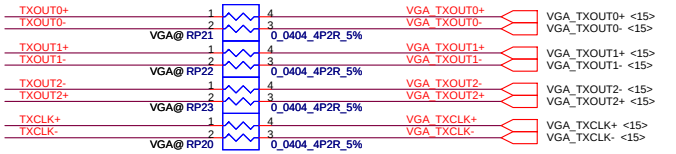


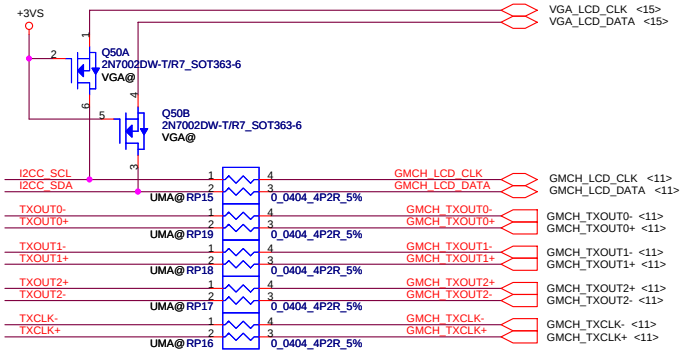
AMD Vari bright function

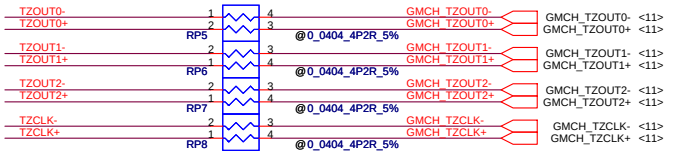




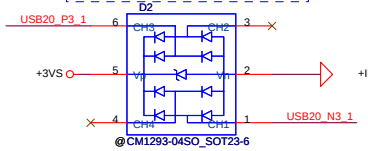




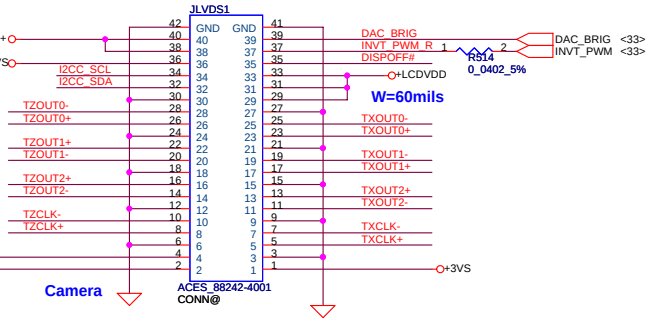




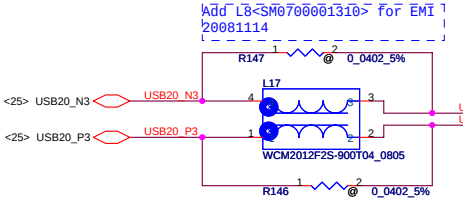
Add D2<SC300000B00> for ESD
20081114

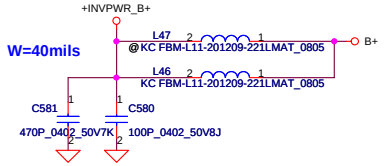


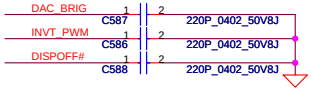
LCD/PANEL BD. Conn.



Add L8<SM0700001310> for EMI
20081114







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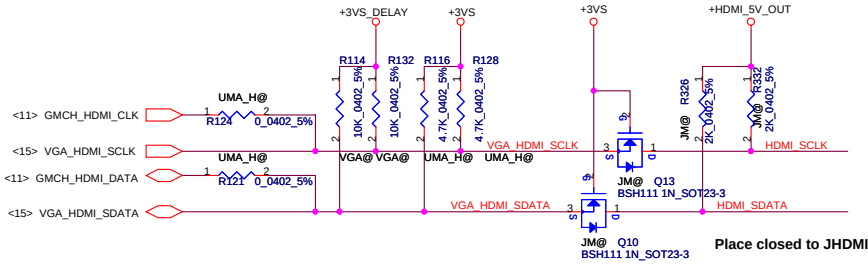
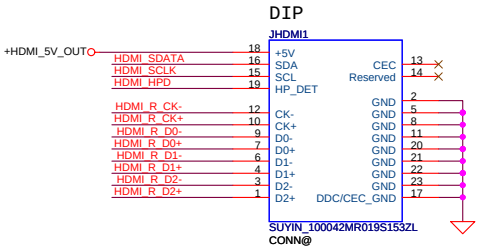
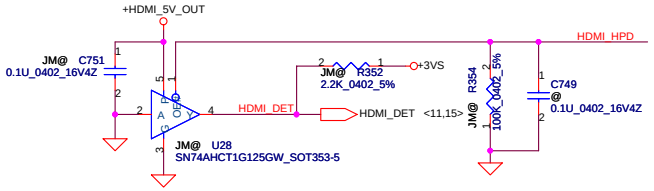
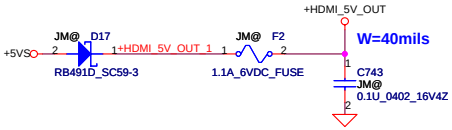
DDC to HDMI CONN



Place closed to JHDMI1



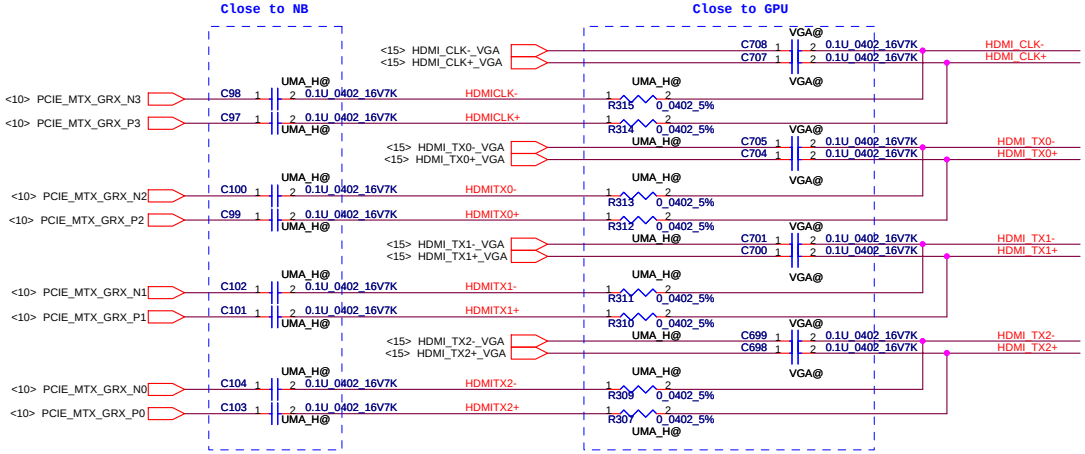


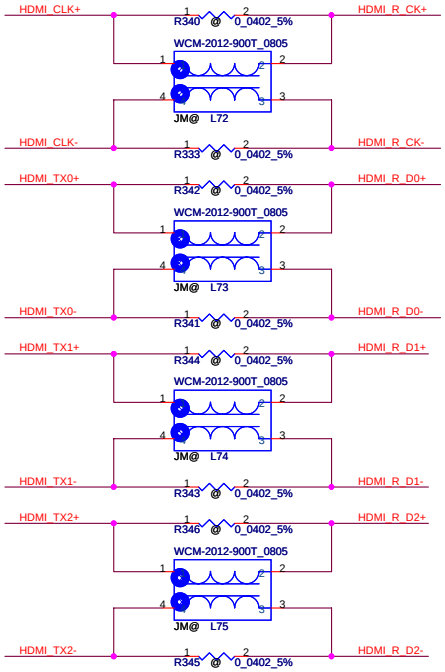


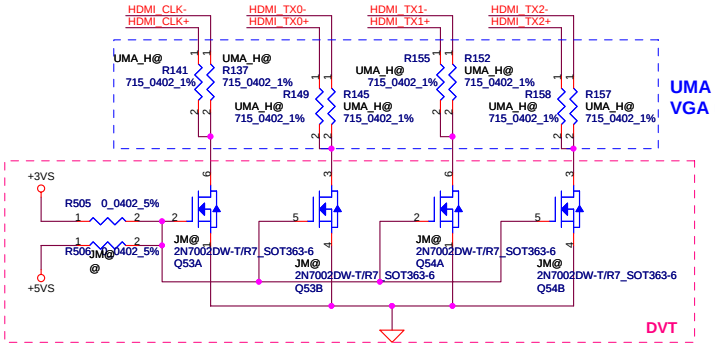
W=40mils

Close to NB

Close to GPU







Update (For Puma / Tigris default value)

UMA use 715 ohm
VGA use 499 ohm

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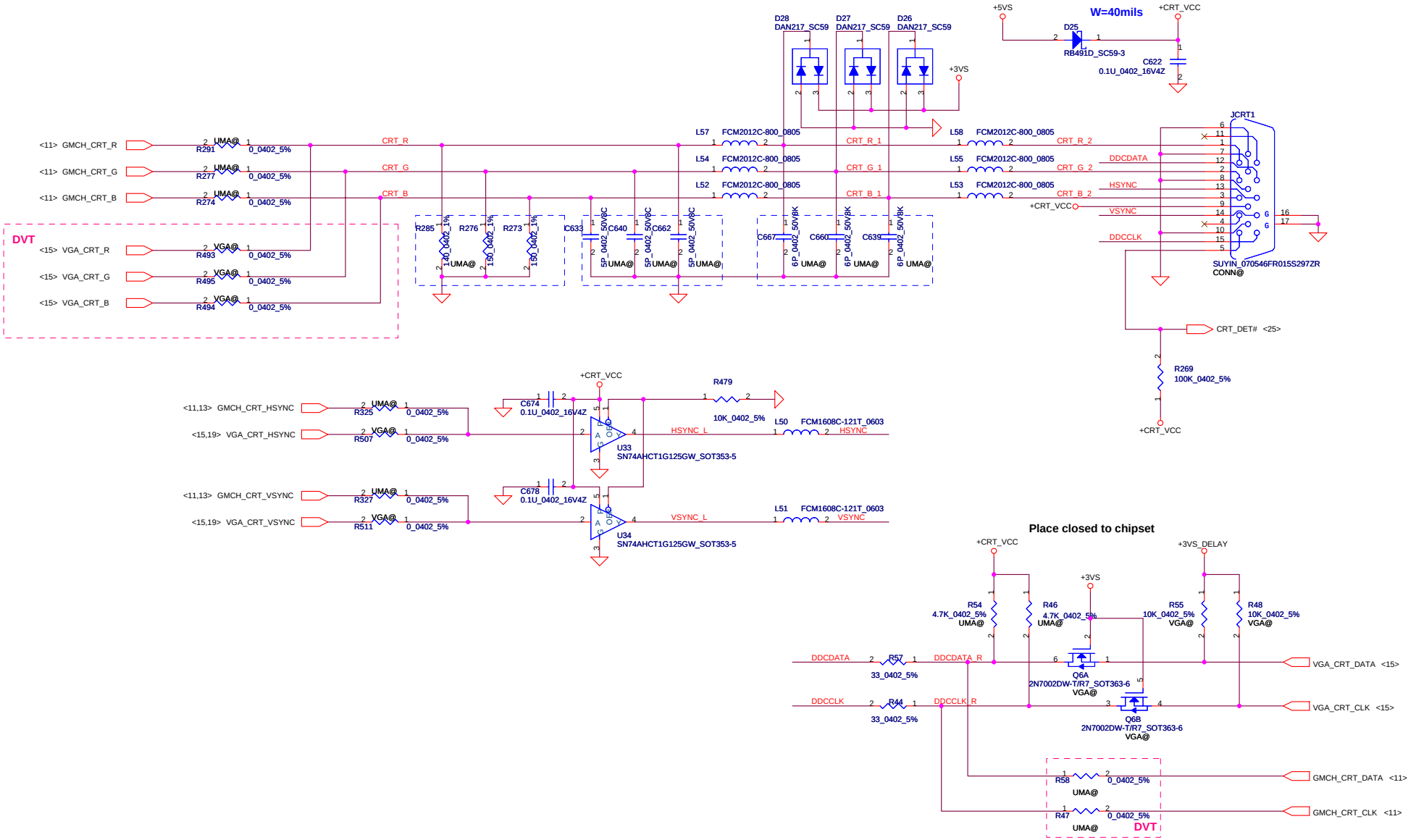
CRT CONNECTOR



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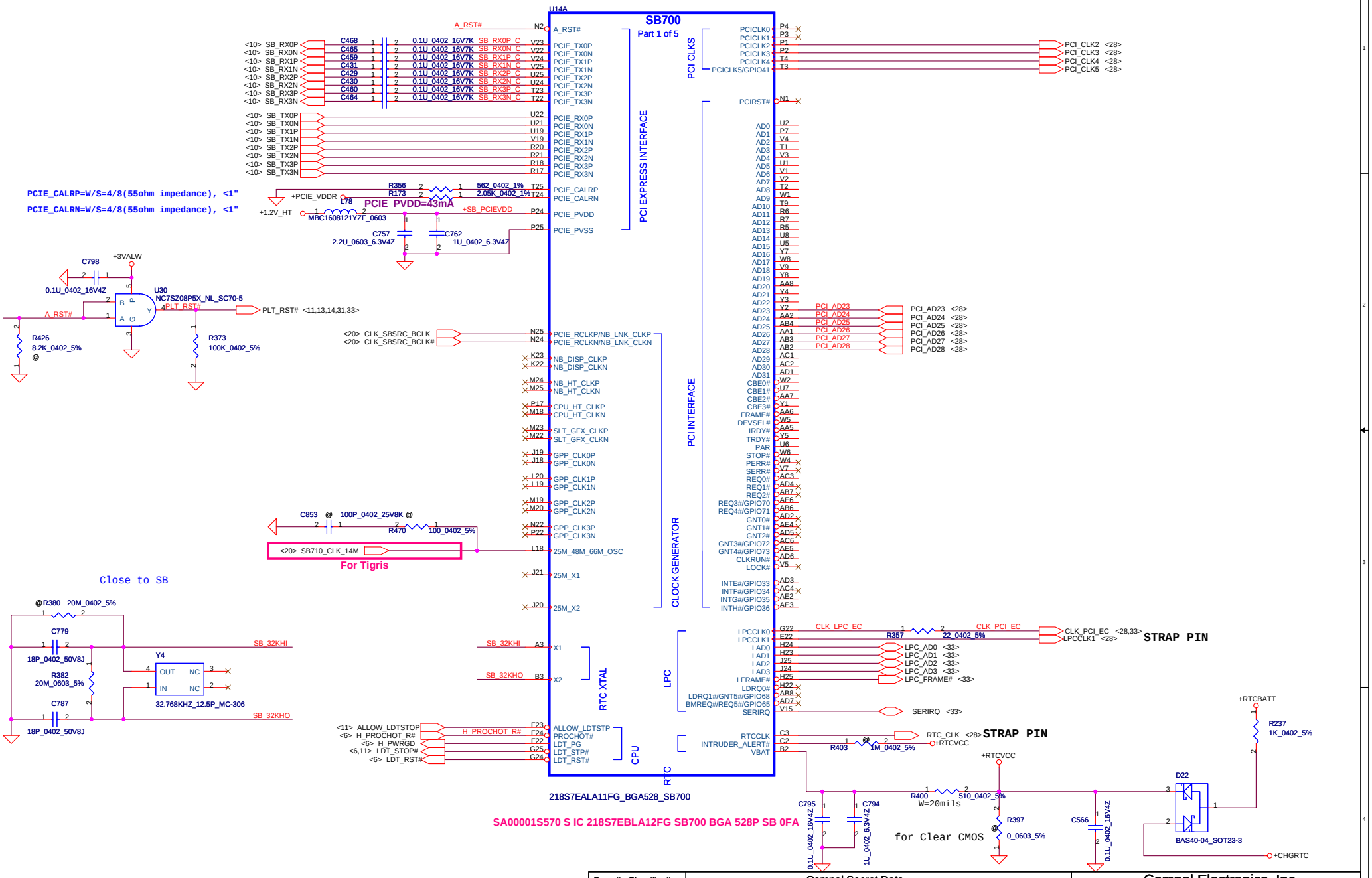

Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

Compal Electronics, Inc.	
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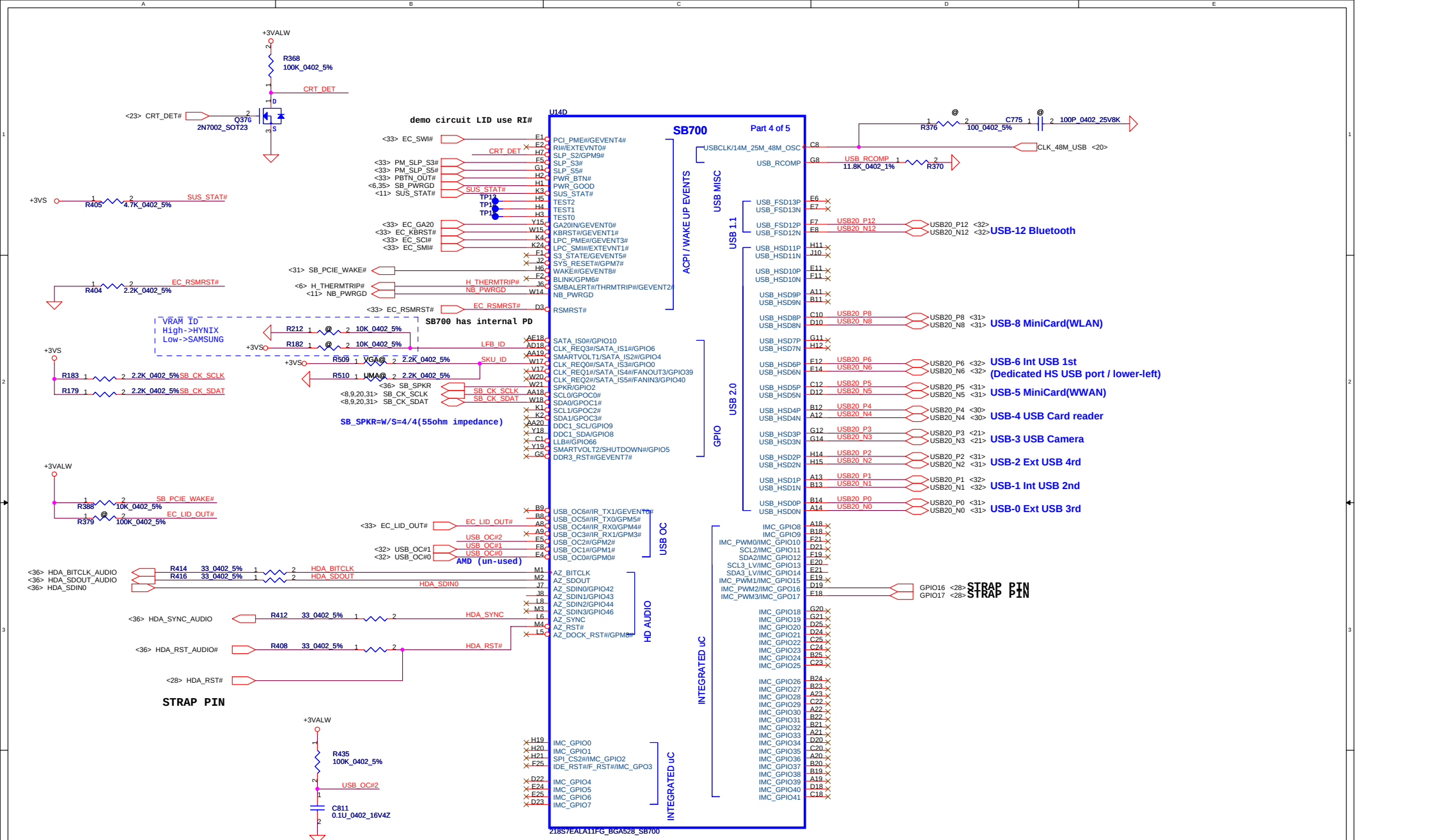

Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2009/10/06

Compal Electronics, Inc.

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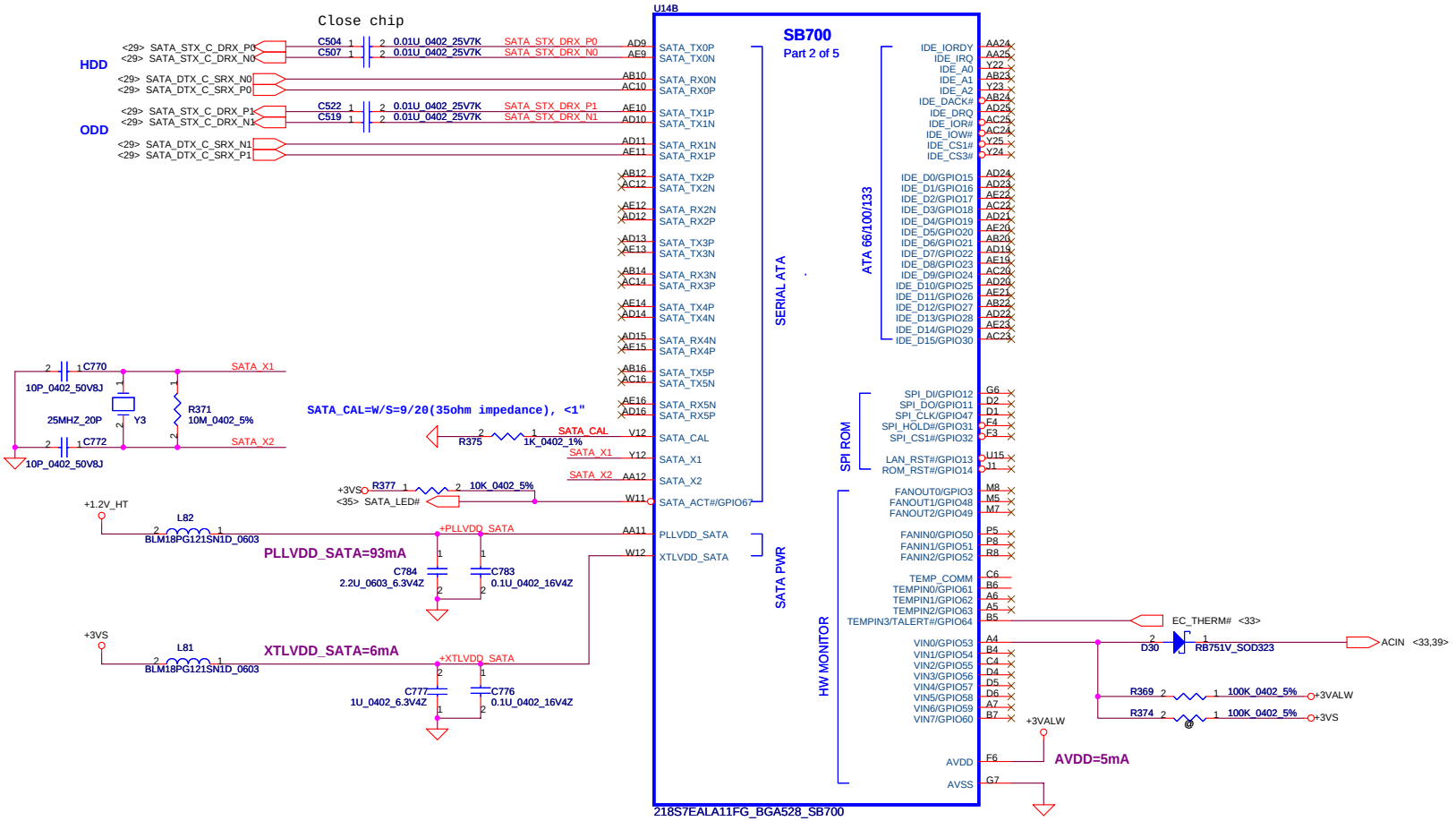

Port Number	Pri/SEC,Mas/Slave assignment	SATA drive controlled by
Port 0	Primary master	SATA controler
Port 1	Secondary master	SATA controler
Port 2	Primary slave	SATA controler
Port 3	Secondary slave	SATA controler
Port 4	Primary (Secondary) master	PATA controler
Port 5	Primary (Secondary) slave	PATA controler

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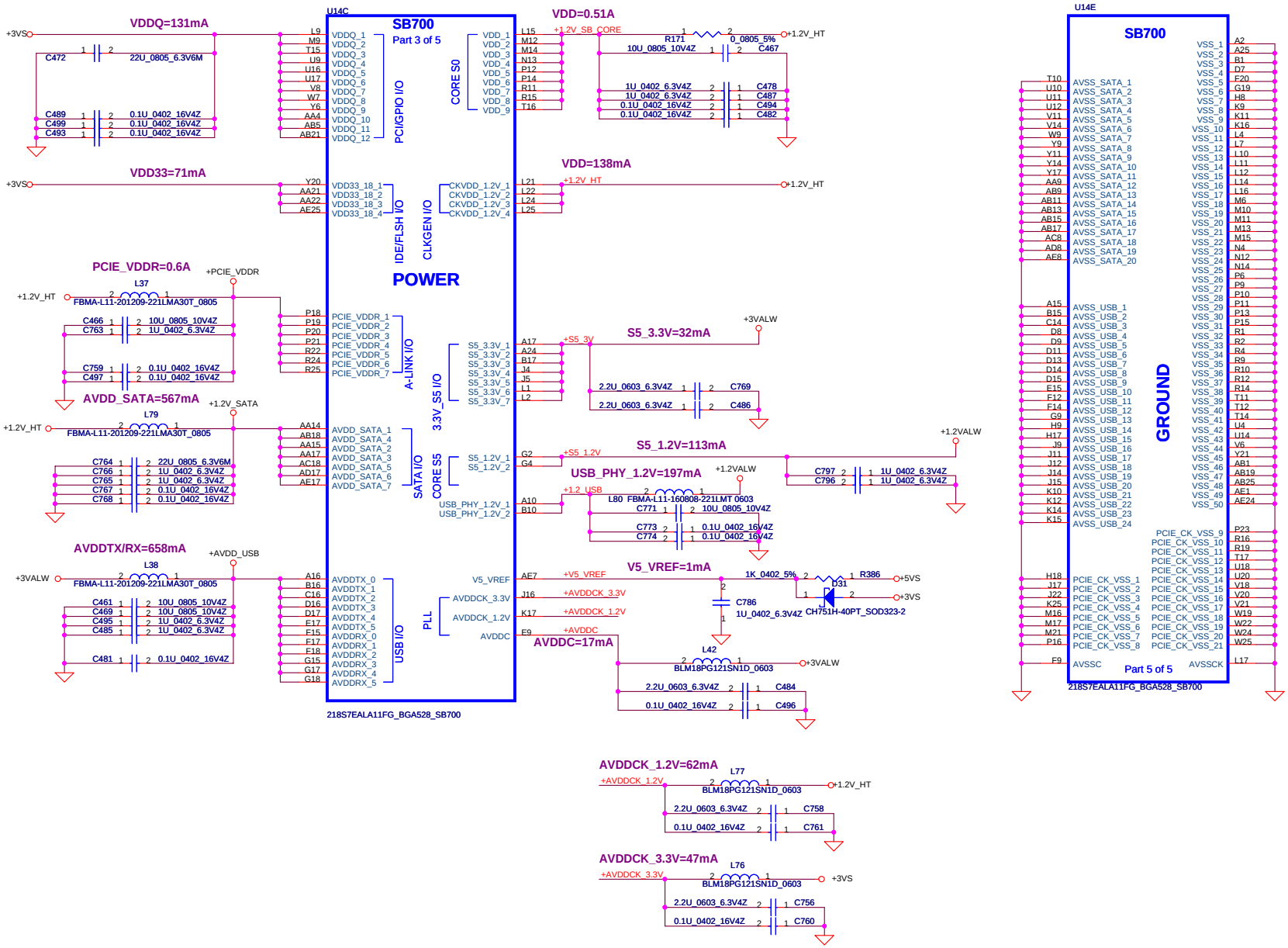

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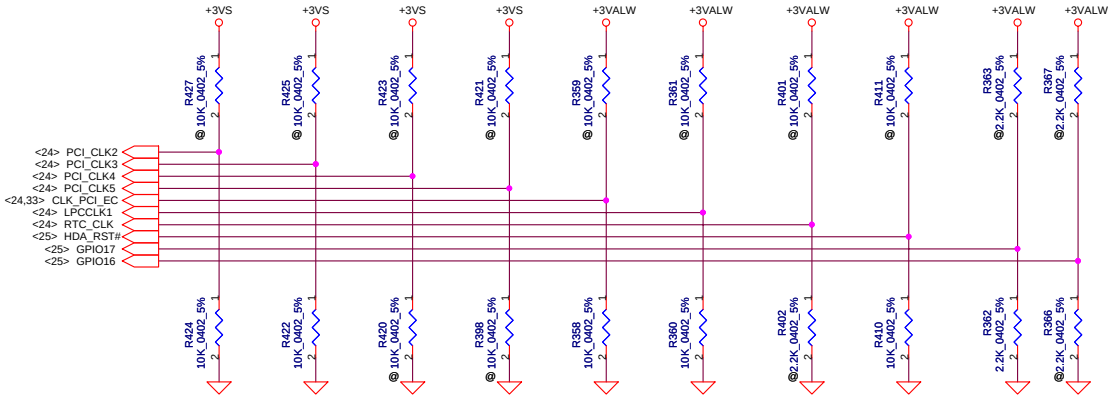
REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

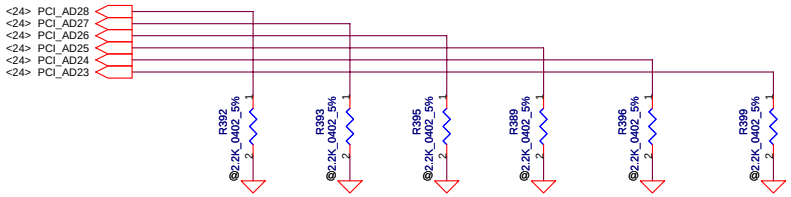
	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0 CLK_PCI_EC	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17 GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	**INTERNAL RTC** DEFAULT	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM L,L = FWH ROM
PULL LOW	**BOOTFAIL TIMER DISABLED** DEFAULT	**IGNORE DEBUG STRAPS** DEFAULT			**DISABLE PCI MEM BOOT** DEFAULT	**CLKGEN DISABLED** DEFAULT	**EXT. RTC** (PD on X1, apply 32KHz to RTC_CLK)	**EC DISABLED** DEFAULT	**L,H = LPC ROM (SB700)** **L,NC = LPC ROM (SB710)**



DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	**USE LONG RESET** DEFAULT	**USE PCI PLL** DEFAULT	**USE ACPI BCLK** DEFAULT	**USE IDE PLL** DEFAULT	**USE DEFAULT PCIE STRAPS** DEFAULT	**RESERVED**
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



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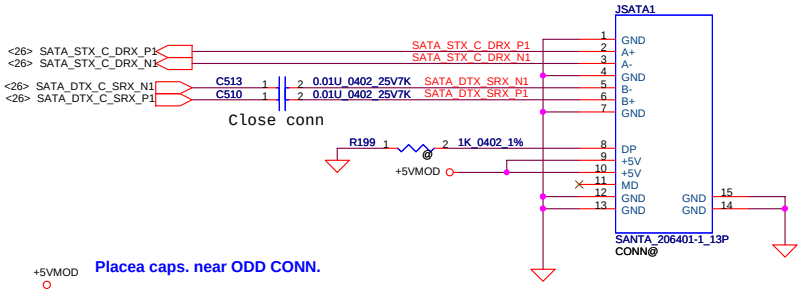
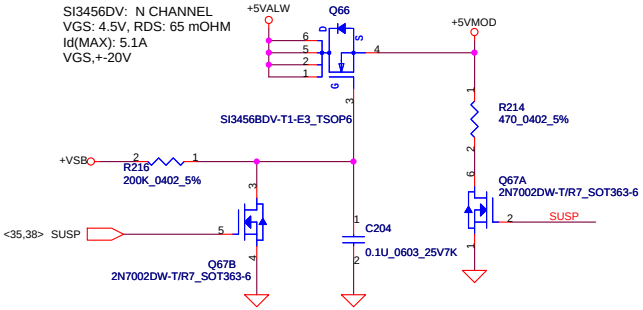
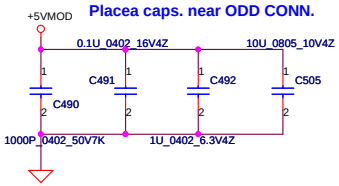
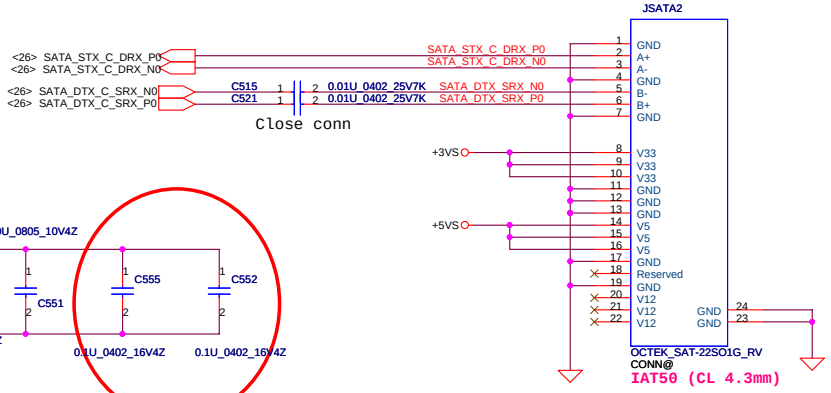
SATA ODD Conn.

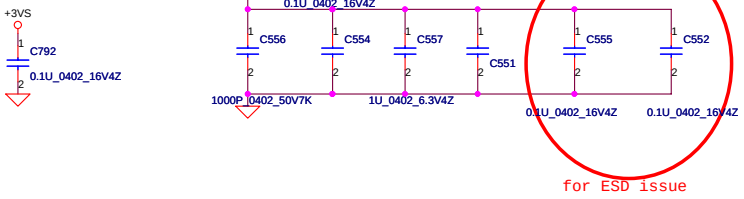






SATA HDD Conn.





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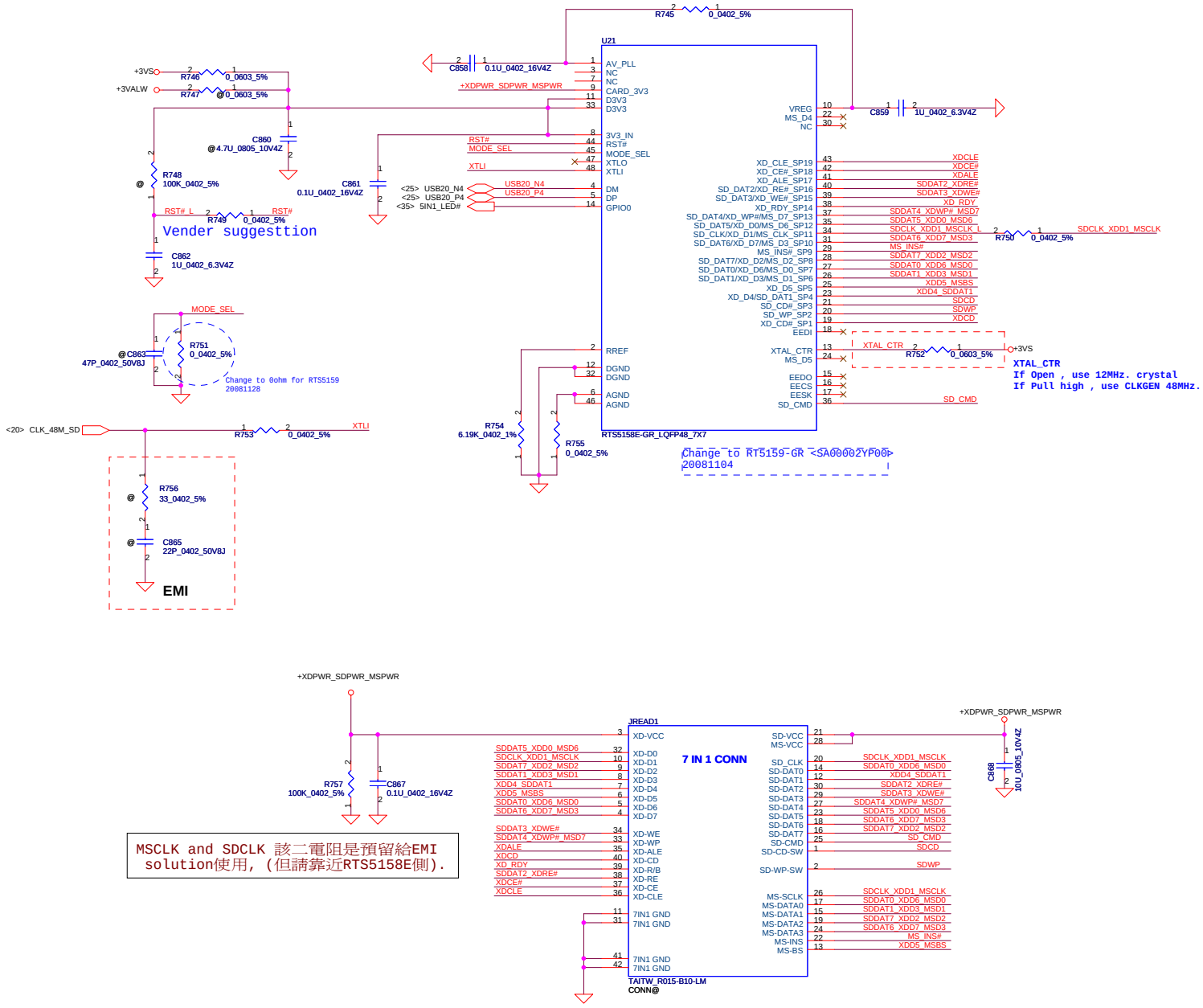

Security Classification	Compal Secret Data		
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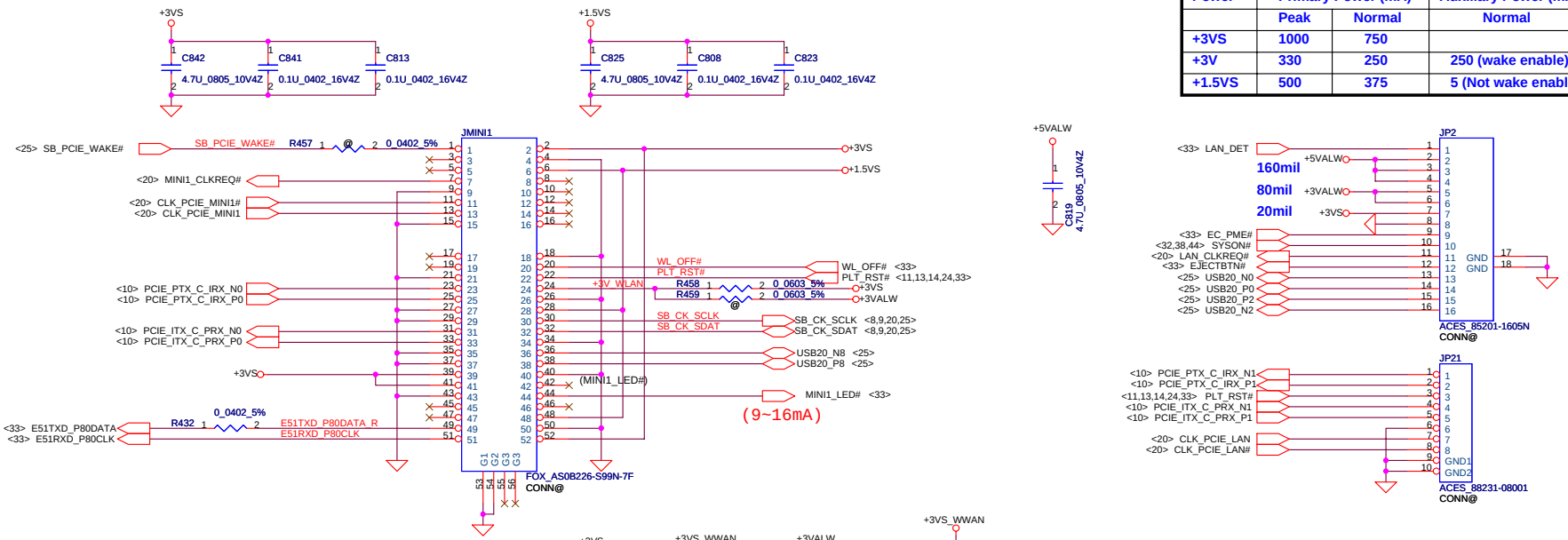
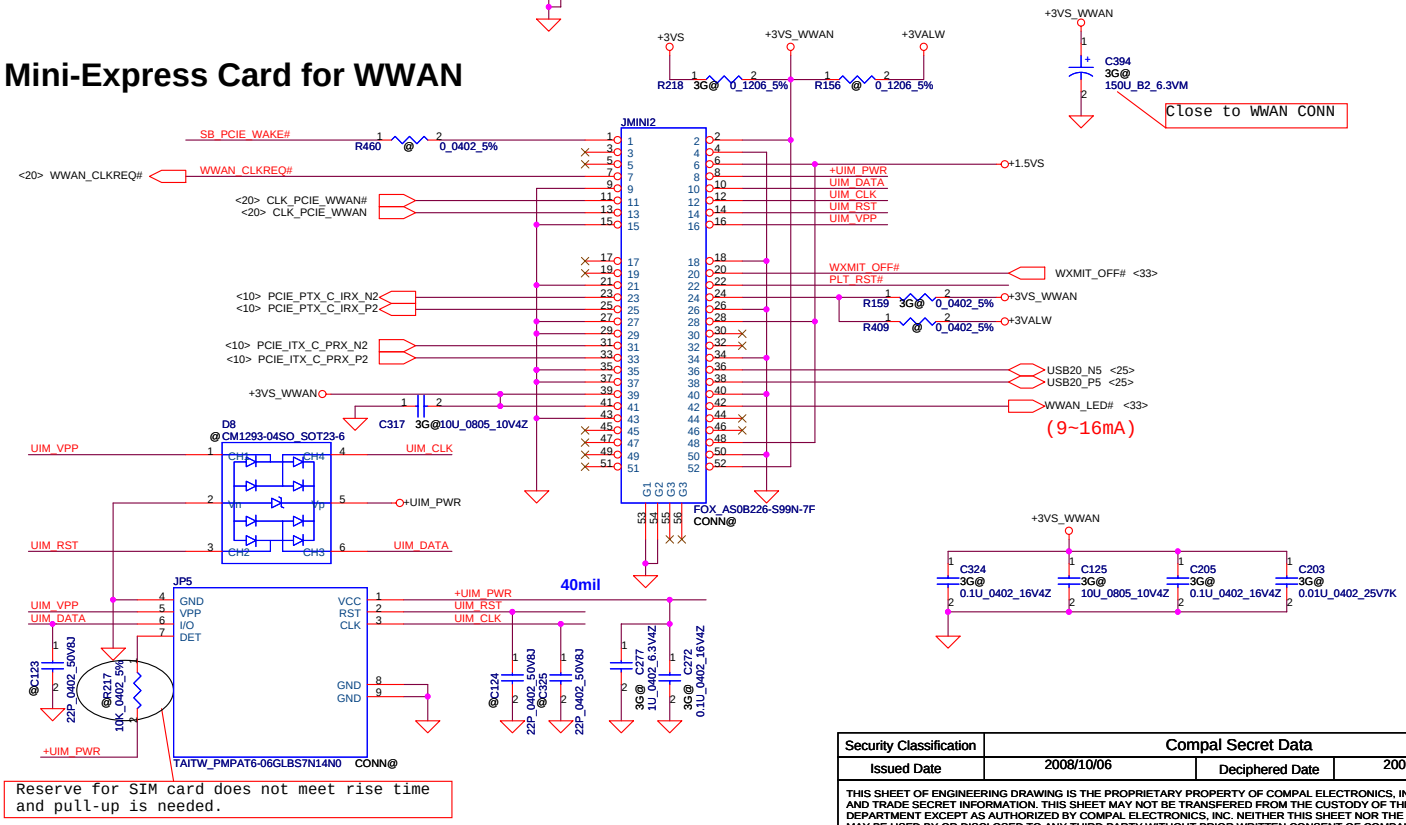
For Wireless LAN

Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)



Mini-Express Card for WWAN



Reserve for SIM card does not meet rise time and pull-up is needed.

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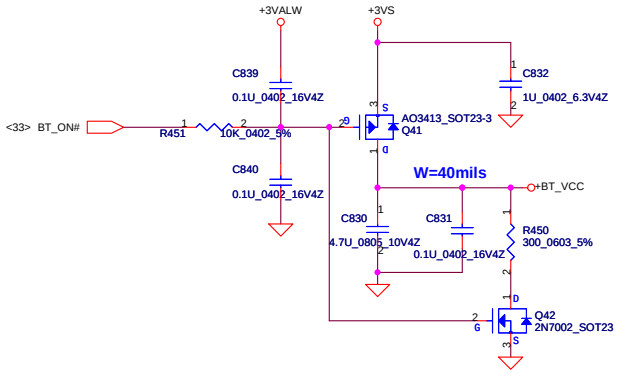
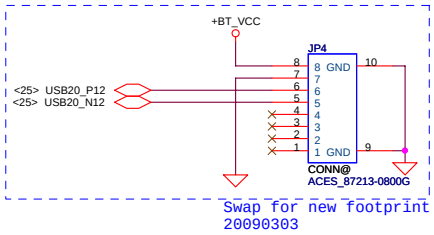
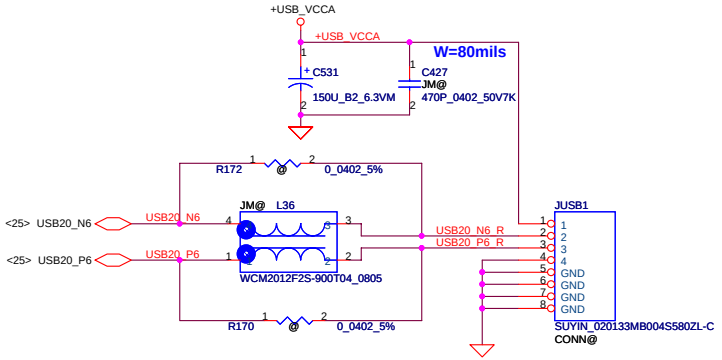
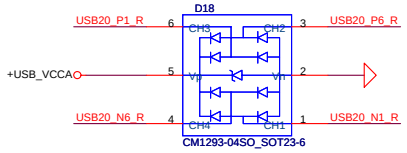
Bluetooth Conn.

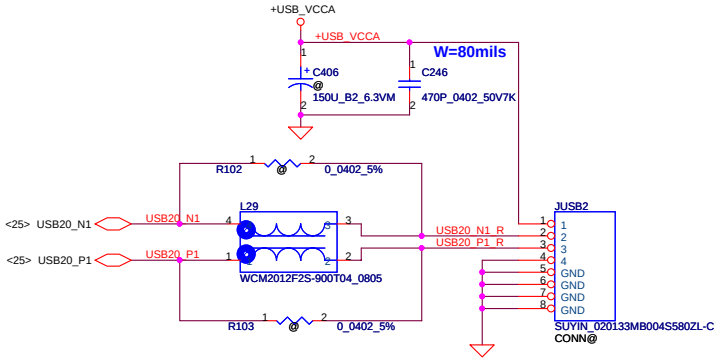


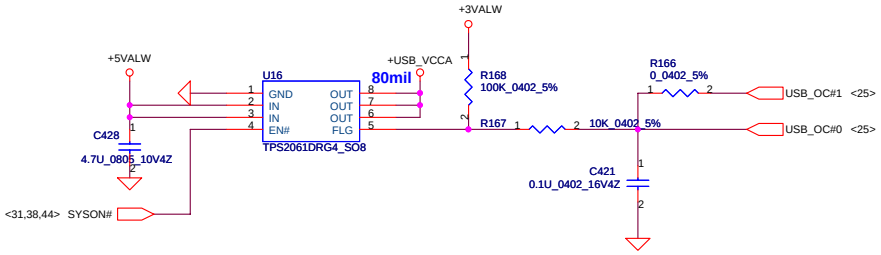


USB PORT x 2









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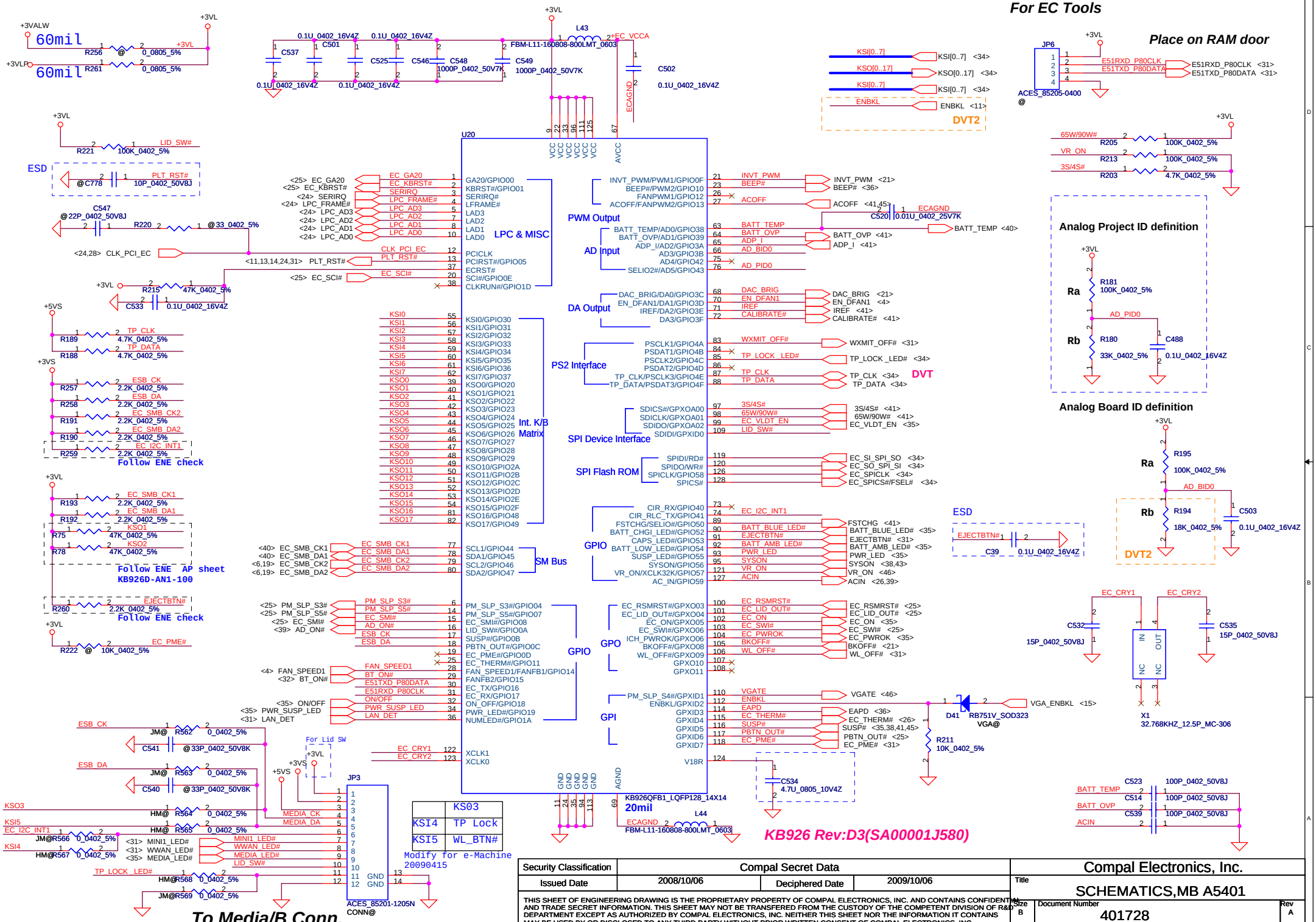
For EC Tools
Place on RAM door
U20
KB926QFB1_LQFP128_14X14
20mil
KB926 Rev:D3(SA00001J580)
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
GPIO
SM Bus
GPO
GPI
DVT
DVT2
ESD
Analog Project ID definition
Analog Board ID definition
Follow ENE check
Follow ENE AP sheet KB926D-AN1-100
To Media/B Conn.
Modify for e-Machine 20090415
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Issued Date
2008/10/06
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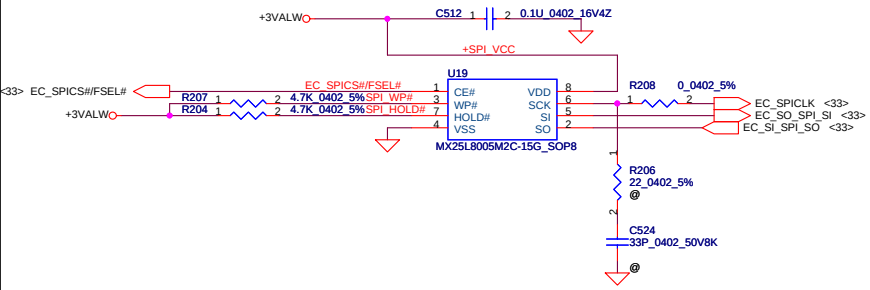
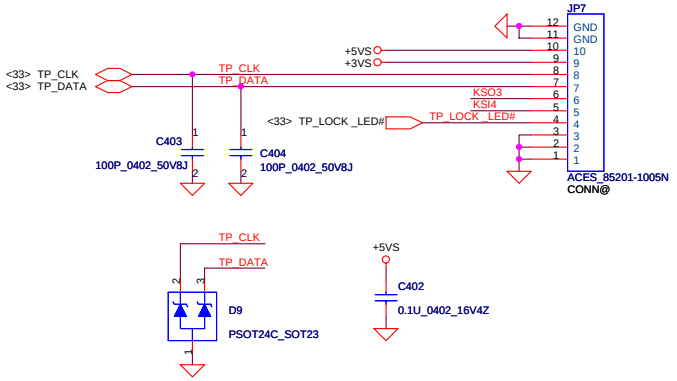
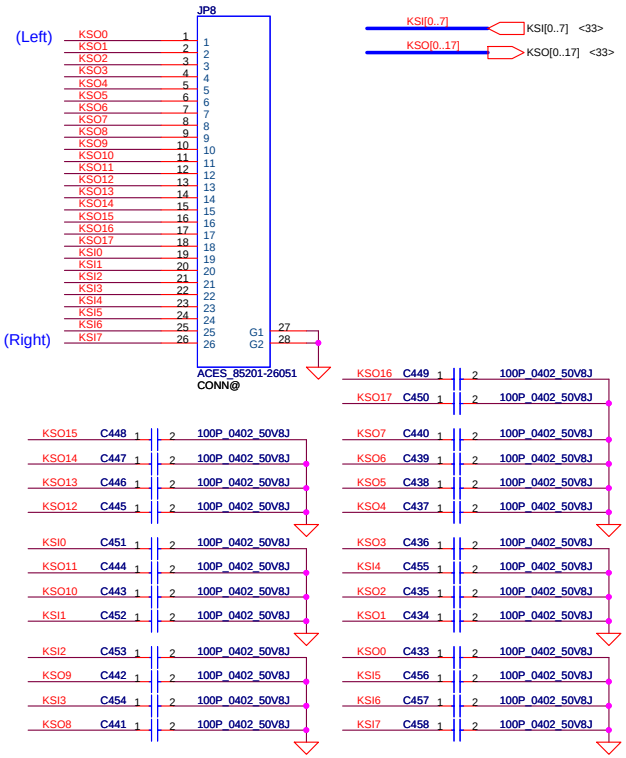
BIOS(SYS / EC / VGA)



To TP/B Conn.



INT_KBD Conn.



	KSO4	KSO2	KSO3
KSI5	WL_BTN#	Volume Down	Back Up
KSI6	BT_BTN#	Volume Up	Program (KBLG0) Battery (KALG0)
KSI4			T/P lock

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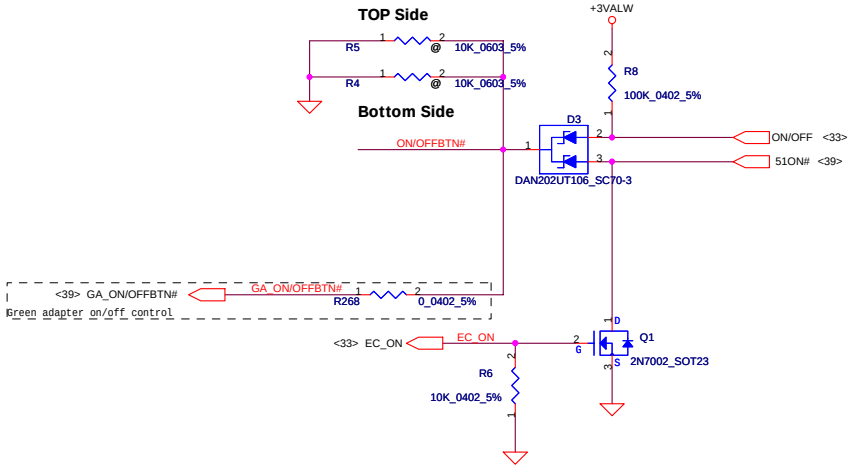
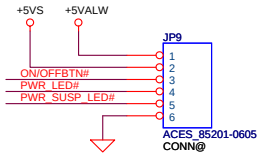
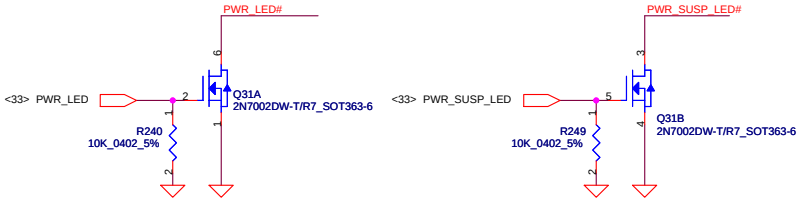
Power Button

ON/OFF switch

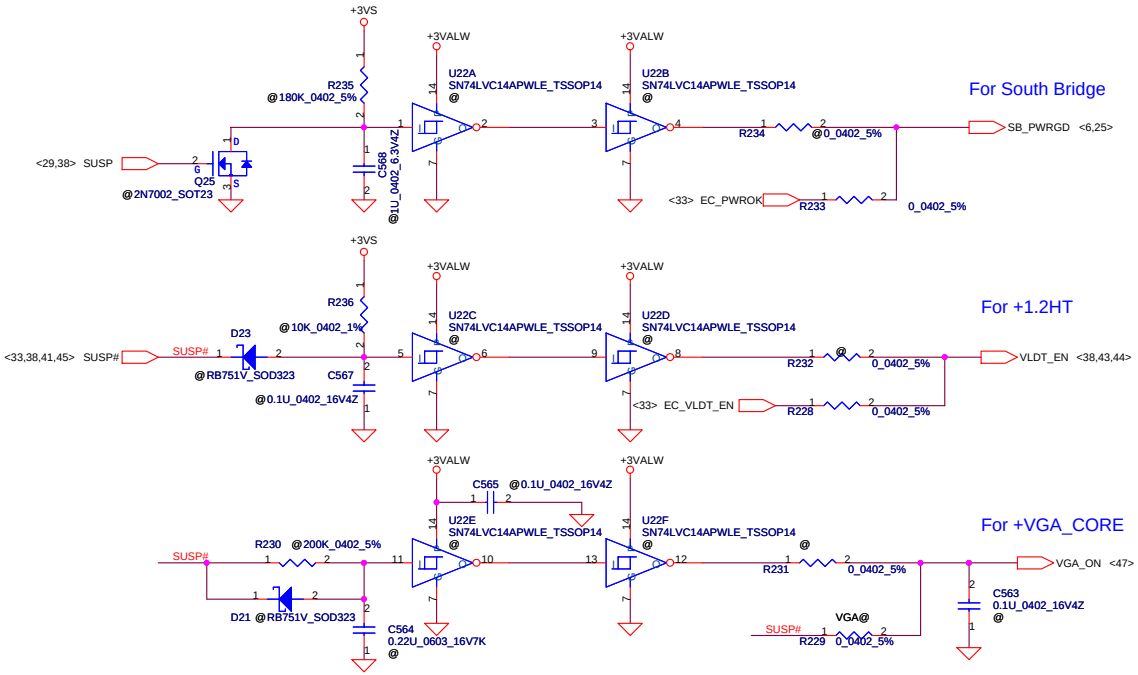


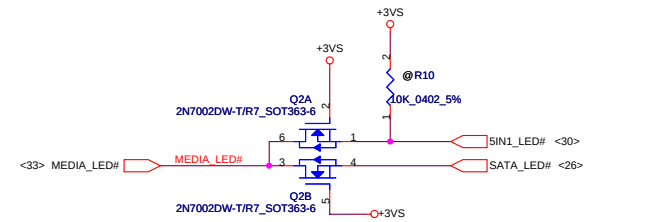
To PWR/B Conn.

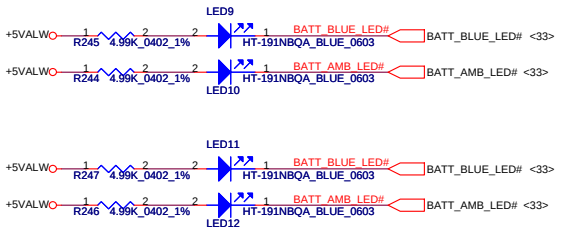




Power ON Circuit







BLUE / AMBER

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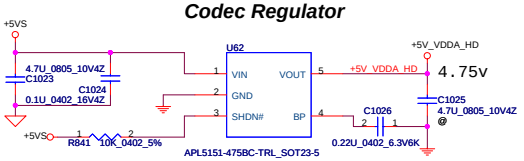
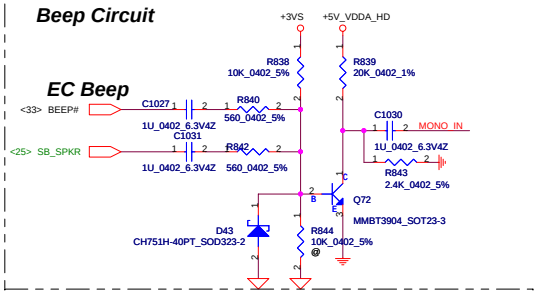
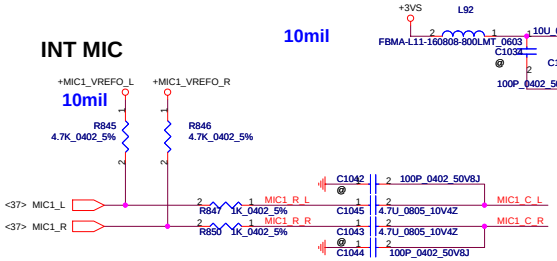
Codec Regulator

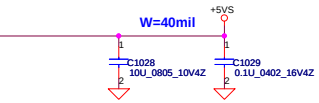


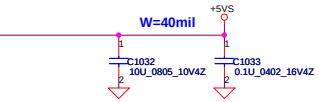
Beep Circuit

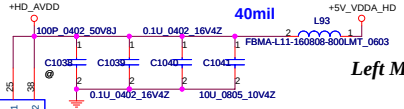


INT MIC

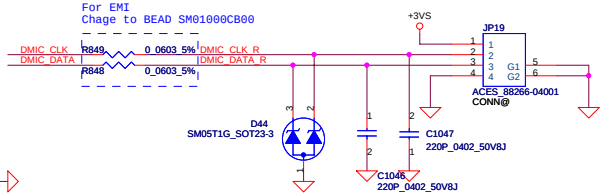


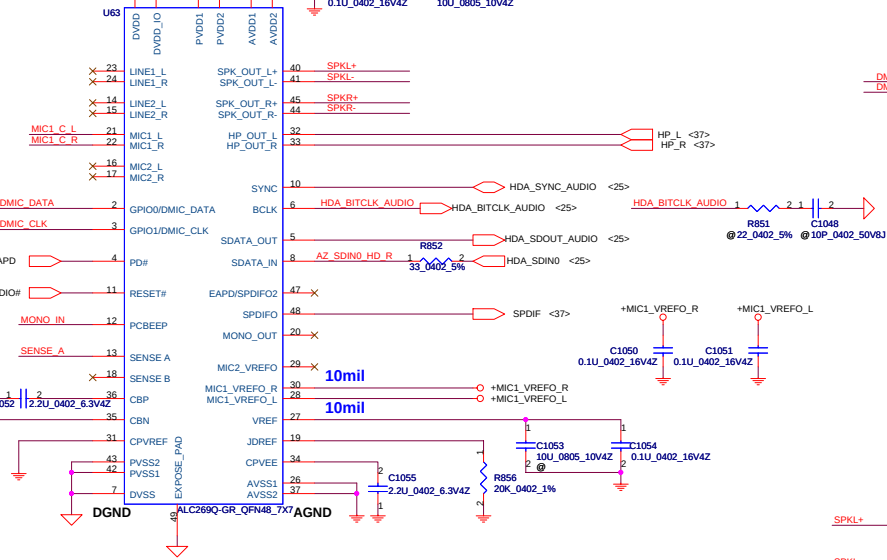


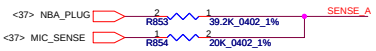




Left Main Speaker Connector

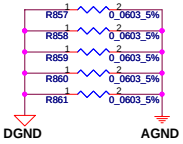




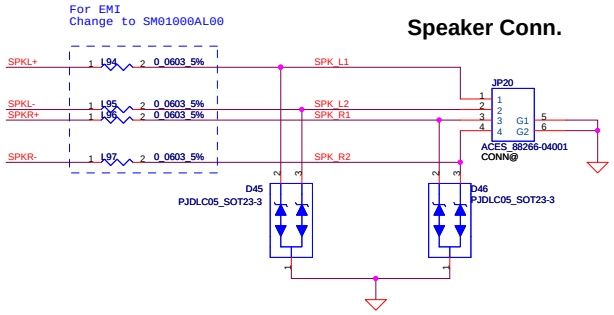


Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 32, 33)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 48)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 20)
	5.1K	PORT-H (PIN 47)

DGND To AGND Bypass



Speaker Conn.



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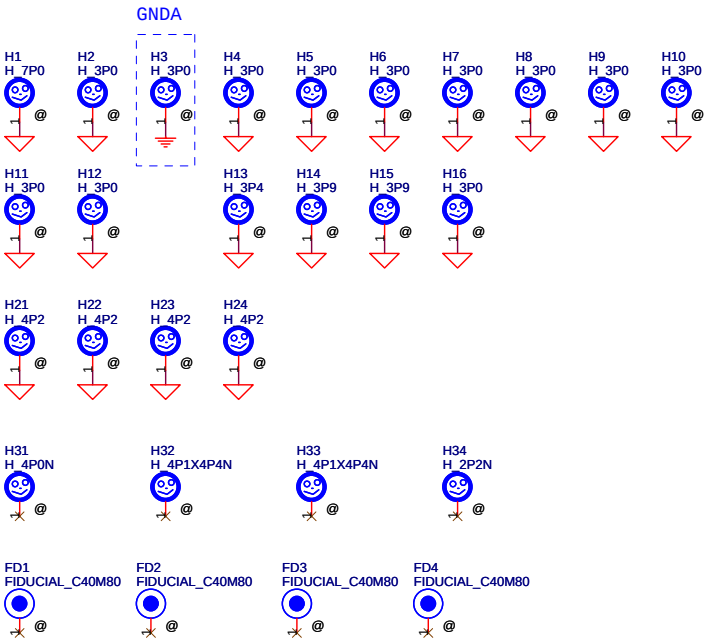
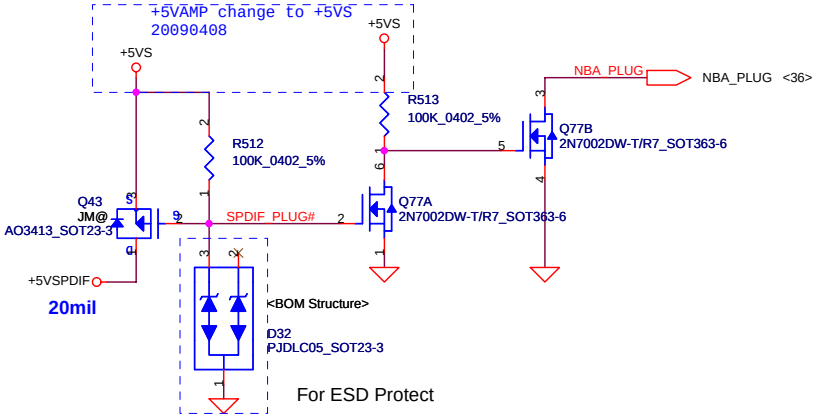
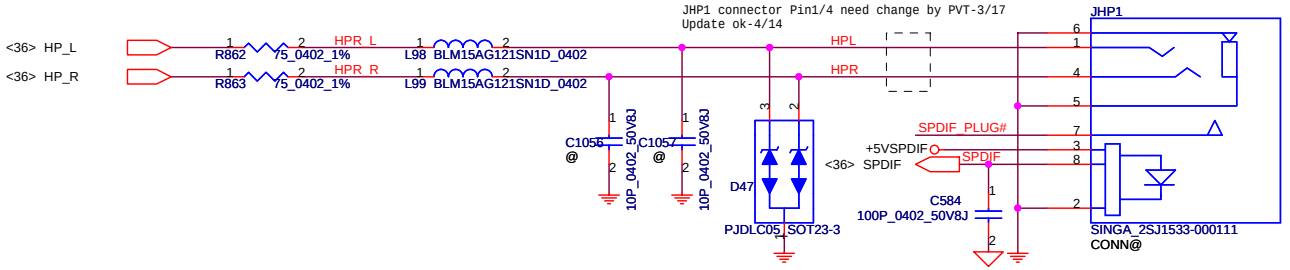
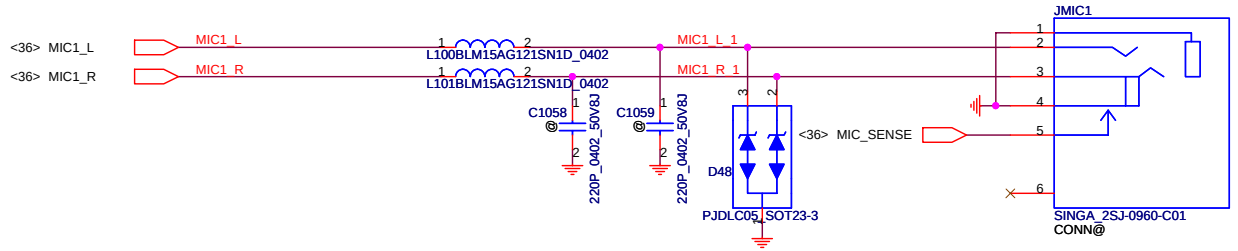




HeadPhone JACK



Ext.MIC JACK



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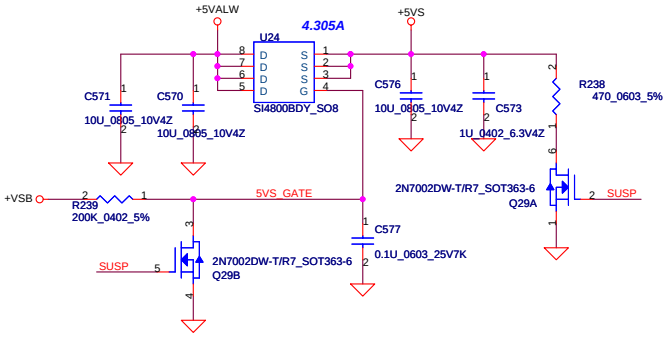
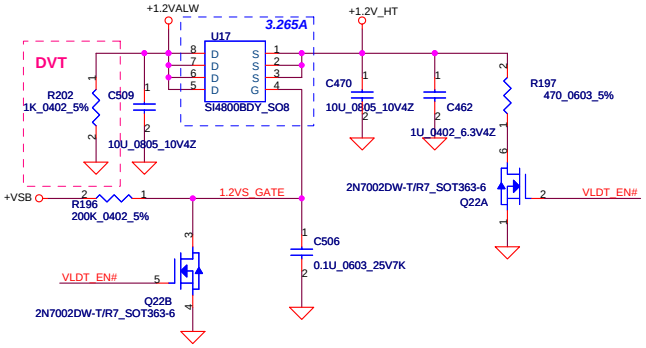
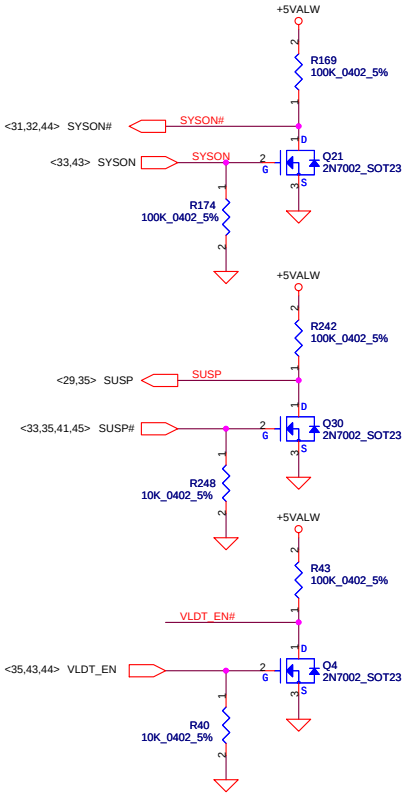
+5VALW TO +5VS

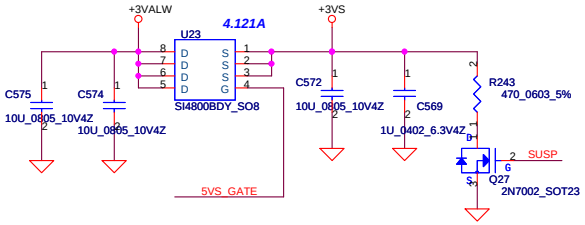


+1.2VALW TO +1.2V_HT

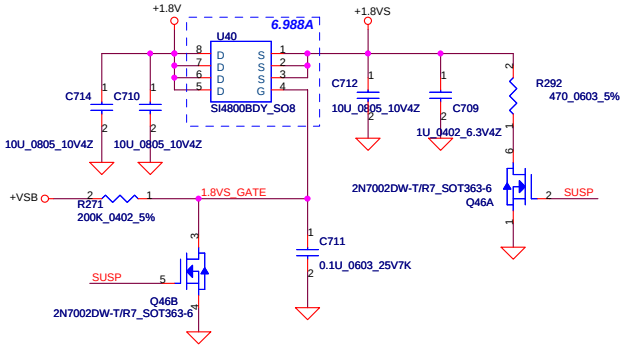


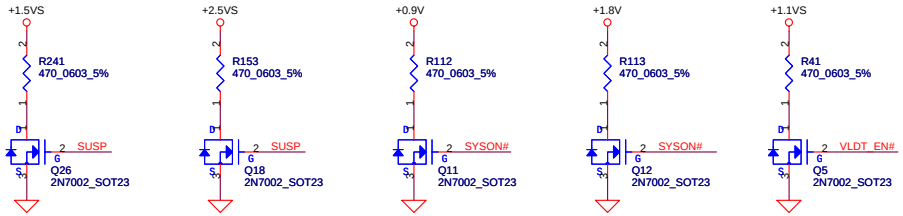


+3VALW TO +3VS



+1.8V to +1.8VS





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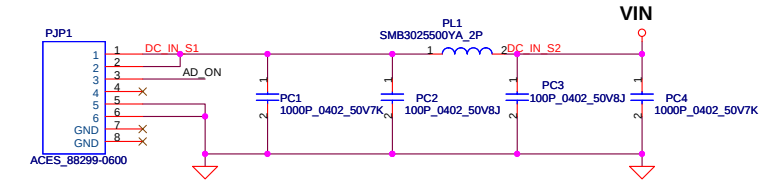
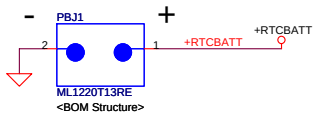
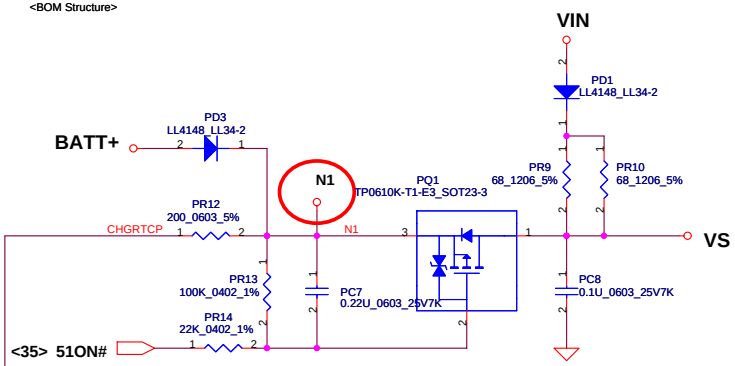
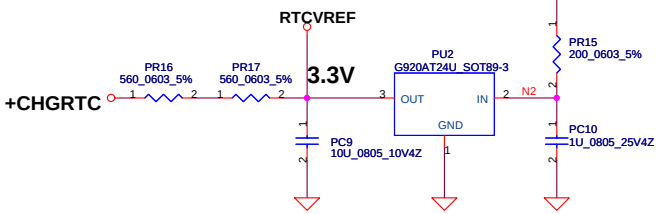
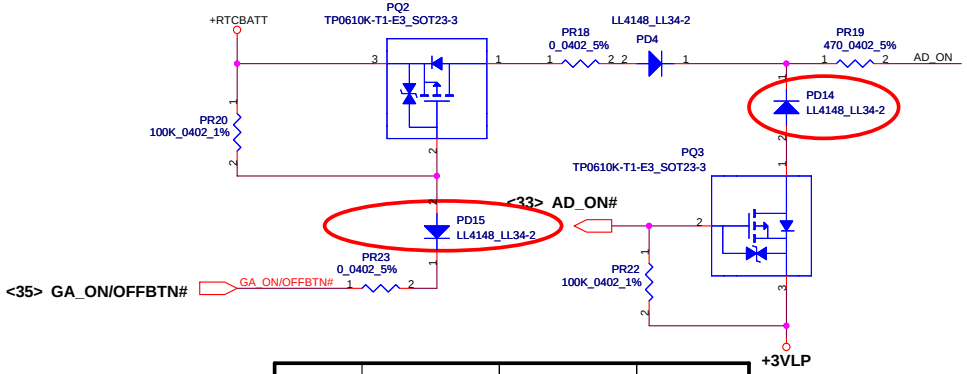
03/05 change footprint (refer to the JAL70)







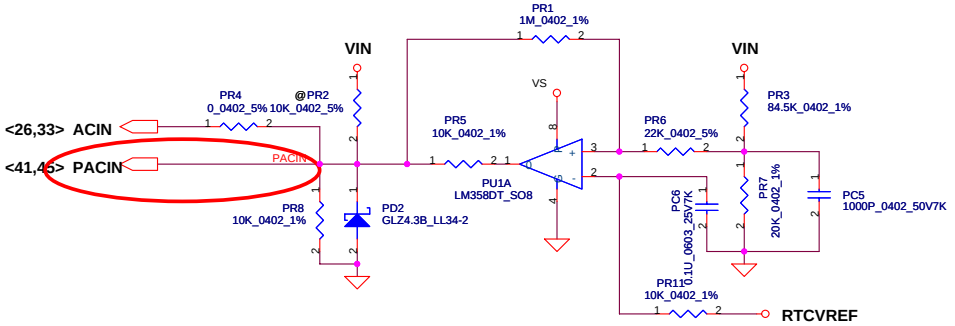


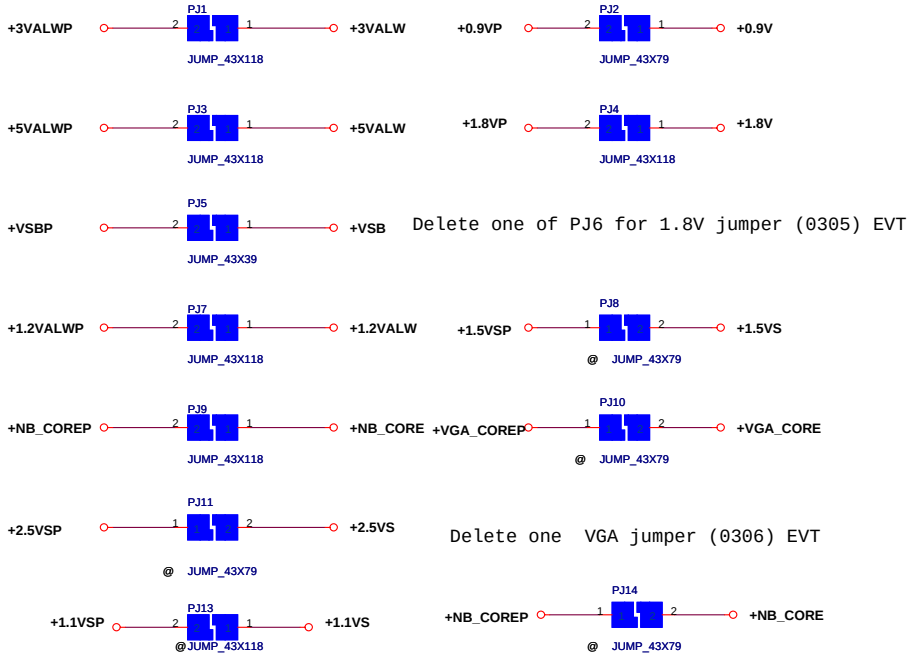


	S5 W/O WOL	S5 W WOL	S3/S0
AD_ON#	H	L	L

Vin Dectector

	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V





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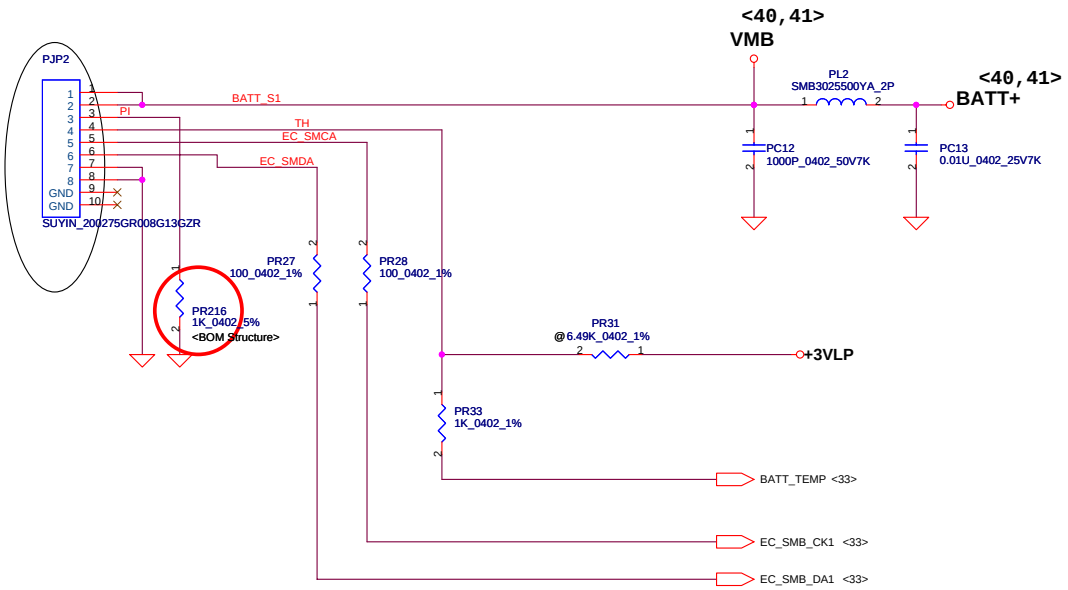
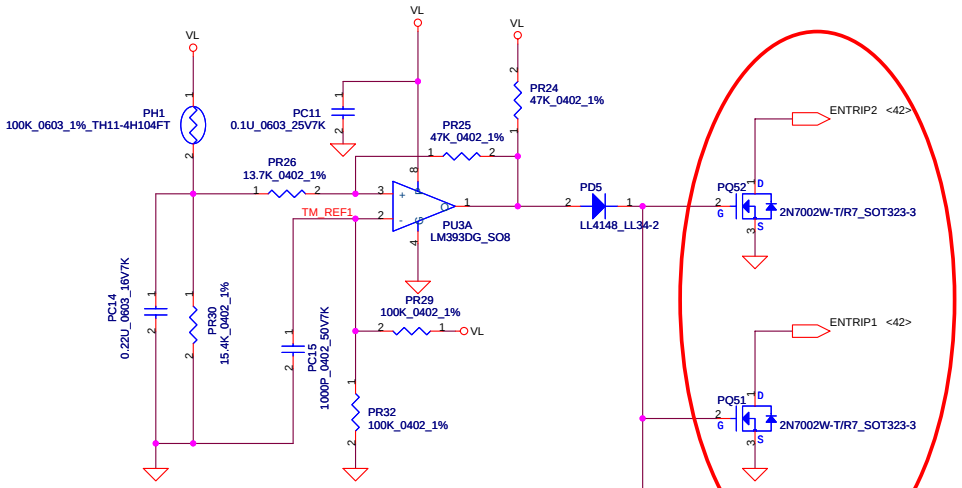
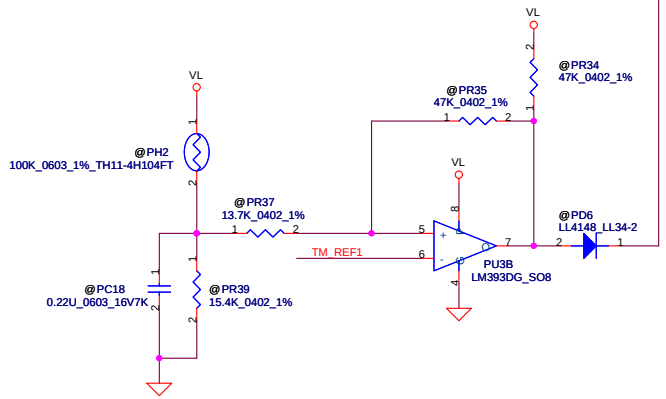
--03/05--OK->add OLB to Library)
--03/09--PJP1 mirror to correct location (update OK)

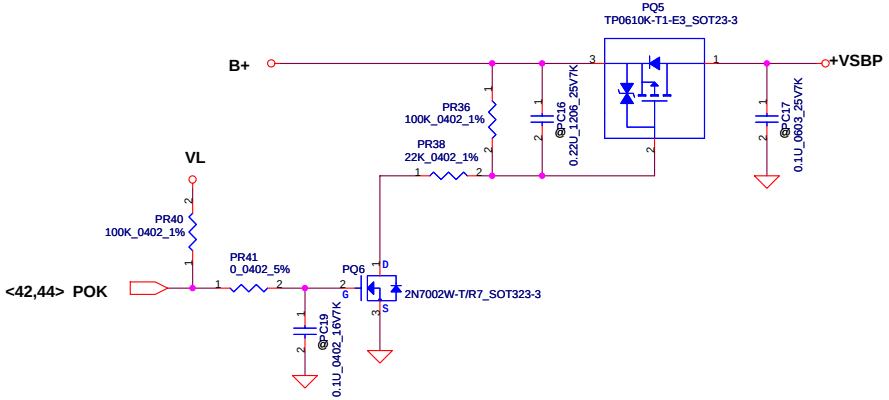


PH1 under CPU botten side :
CPU thermal protection at 93 degree C
Recovery at 57 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 79 degree C
Recovery at 47 degree C





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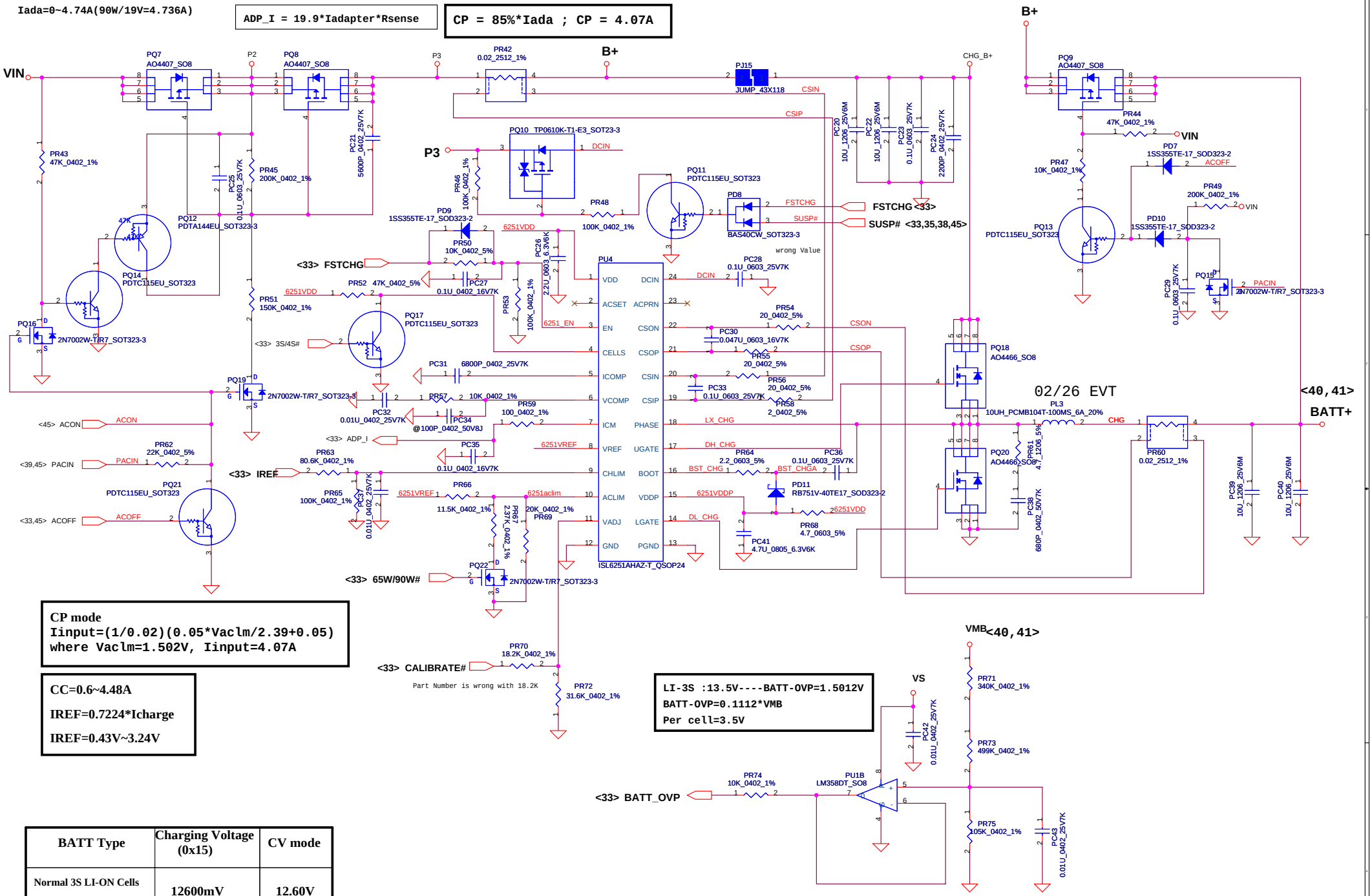
Iada=0~4.74A(90W/19V=4.736A)

ADP_I = 19.9*Iadapter*Rsense

CP = 85%*Iada ; CP = 4.07A



CP mode
Iinput=(1/0.02)(0.05*Vaclm/2.39+0.05)
where Vaclm=1.502V, Iinput=4.07A

CC=0.6~4.48A

IREF=0.7224*Icharge

IREF=0.43V~3.24V

LI-3S :13.5V----BATT-OVP=1.5012V
BATT-OVP=0.1112*VMB
Per cell=3.5V

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

-

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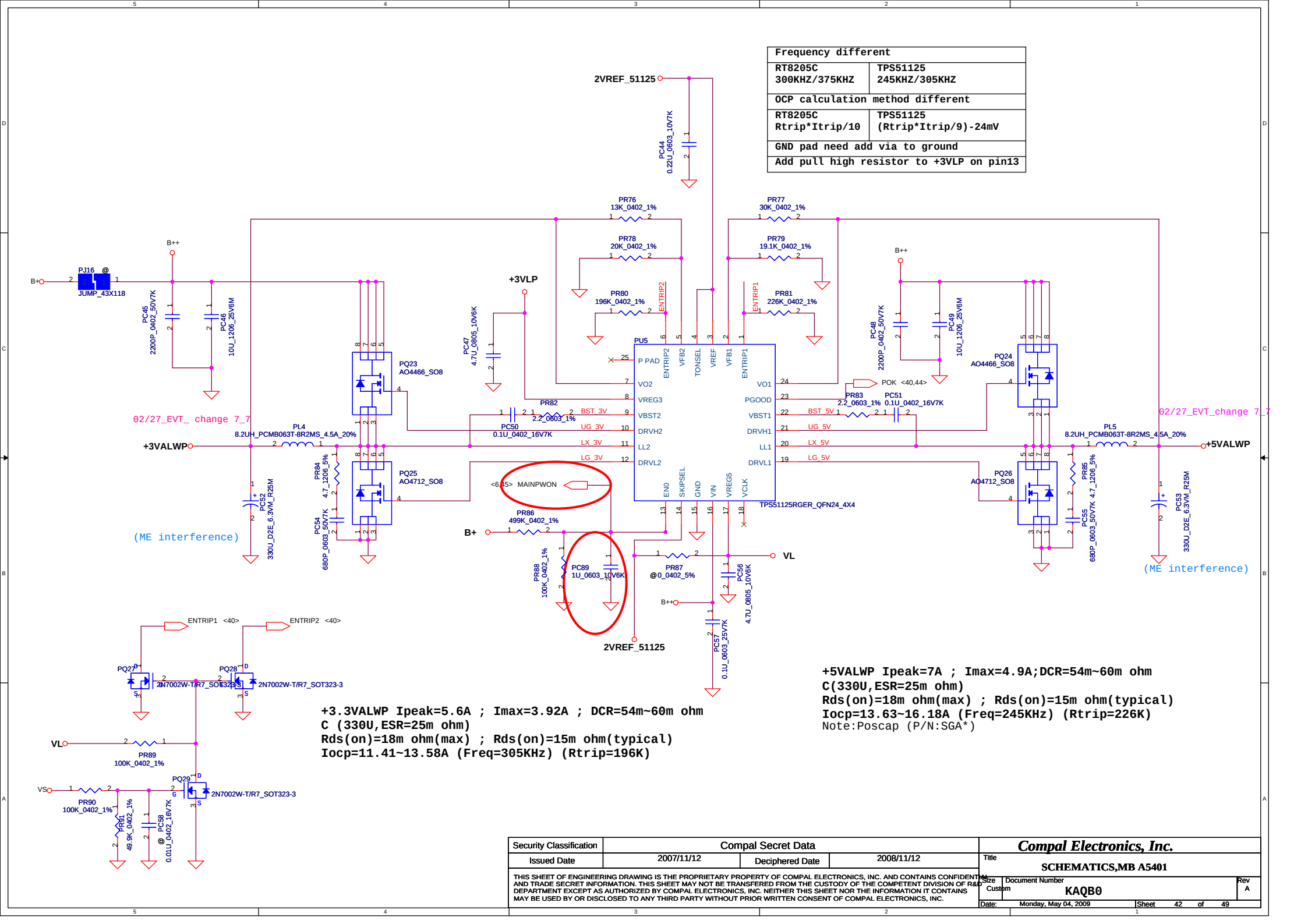

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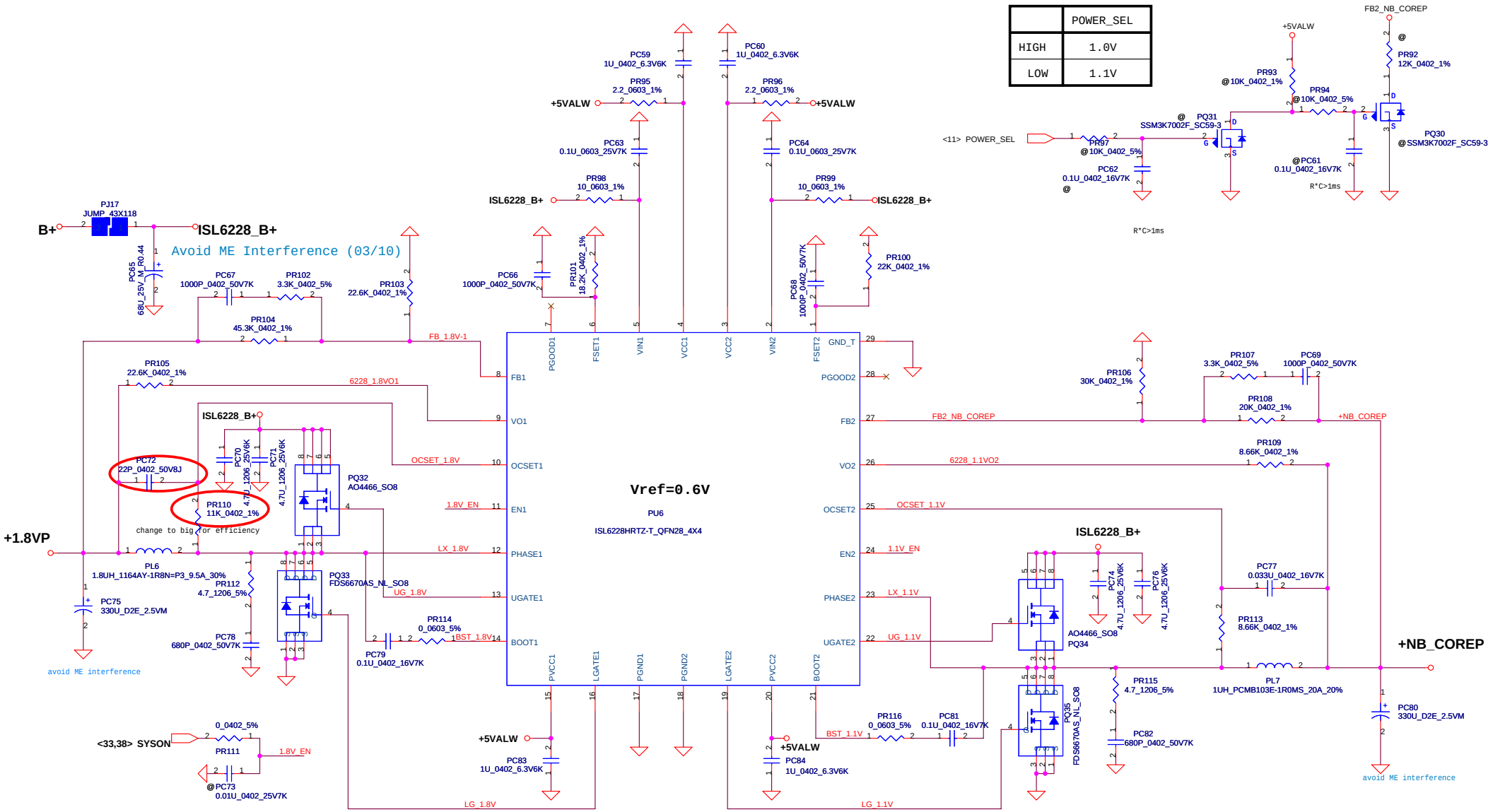
Confirm :UMA (pop-->o/p:adjustable) Discrete(unpop-->o/p:fix)

	POWER_SEL
HIGH	1.0V
LOW	1.1V



DCR=7.5m ohm /tolerance :30%/(L=1.8uH)
C(330U,ESR=15m ohm)
1.8VP Ipeak=9.023A, Imax=6.316A, Iocp=1.2*Ipeak=10.8276A
Fsw=1/1.5E-10*18.2k =366K
Vo=Vref*((PR97+PR99)/PR97)
Roset=change to 11k ohm (remember)
Csen=change to 0.022UF=22PF (remember)
Iocp=11.282A

DCR=3.5m ohm /tolerance :20%/(L=1uH)
C(330U,ESR=15m ohm)
1.8VP Ipeak=11.93A, Imax=8.351A, Iocp=1.2*Ipeak=14.316A
Fsw=1/1.5E-10*22k =303K
Vo=Vref*((PR97+PR99)/PR97)
Roset=change to 8.66k ohm (remember)
Csen=change to 0.033UF=33PF (remember)
Iocp=20.619A

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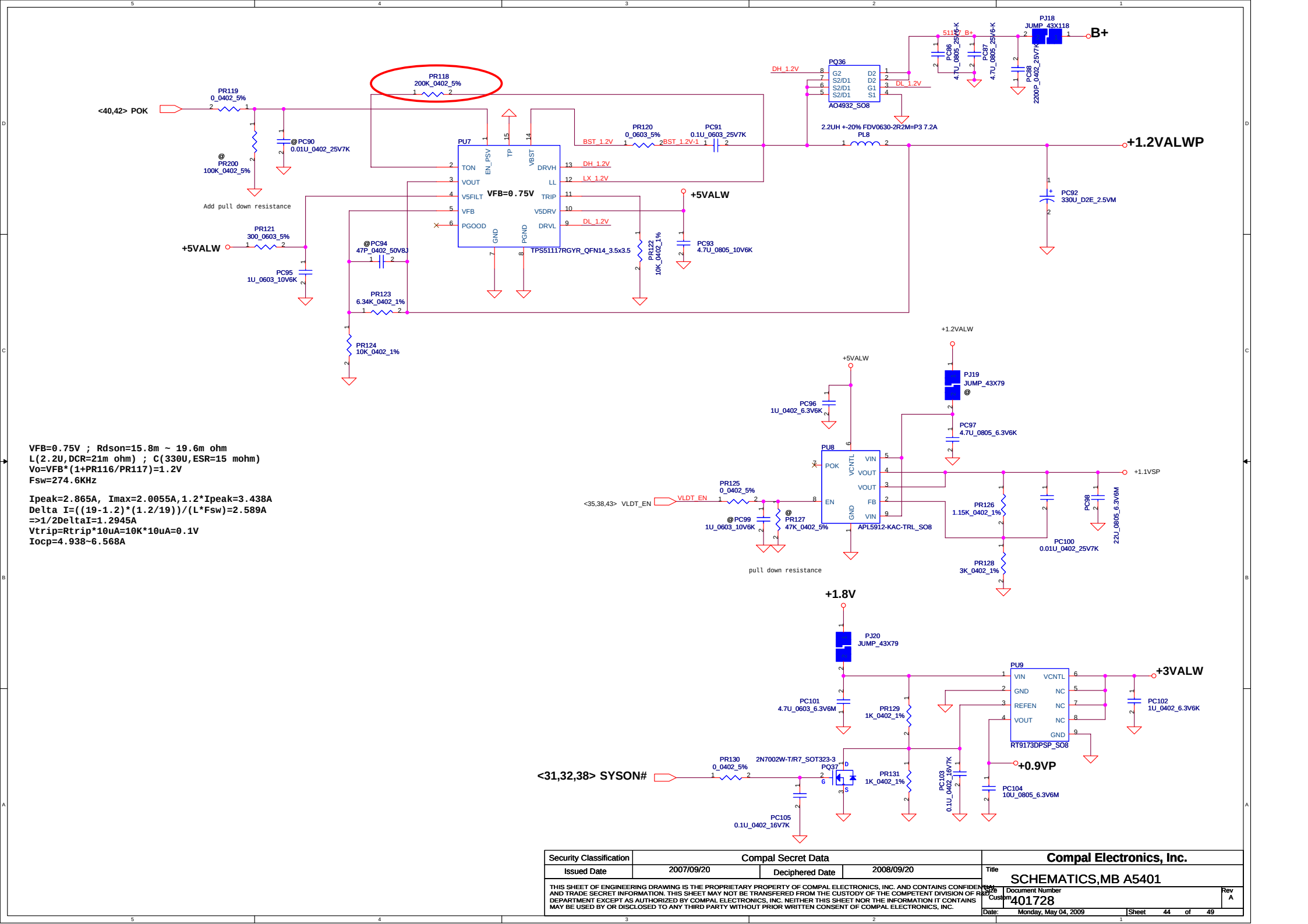

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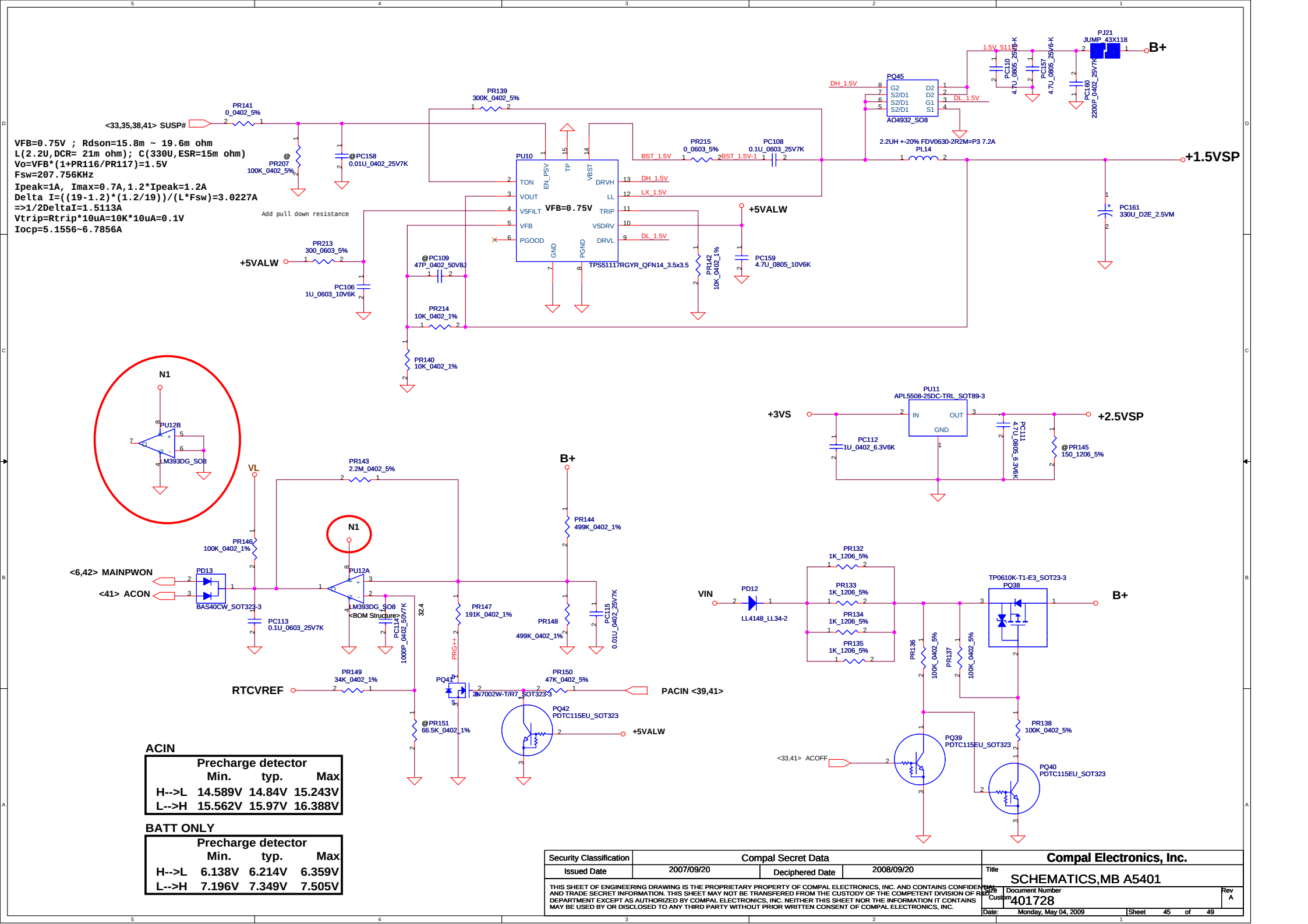

ACIN

Precharge detector	Min.	typ.	Max
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

Precharge detector	Min.	typ.	Max
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

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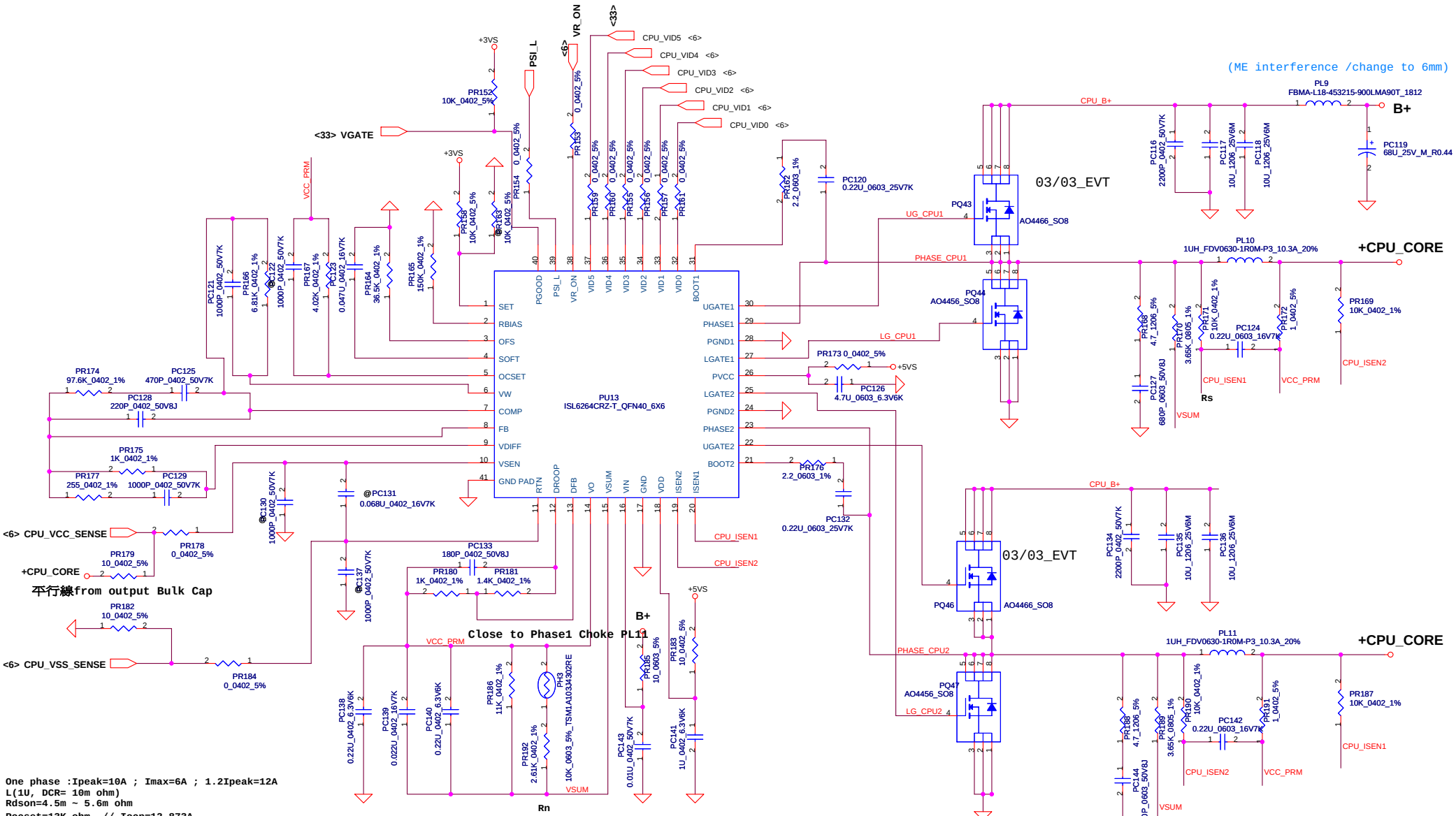

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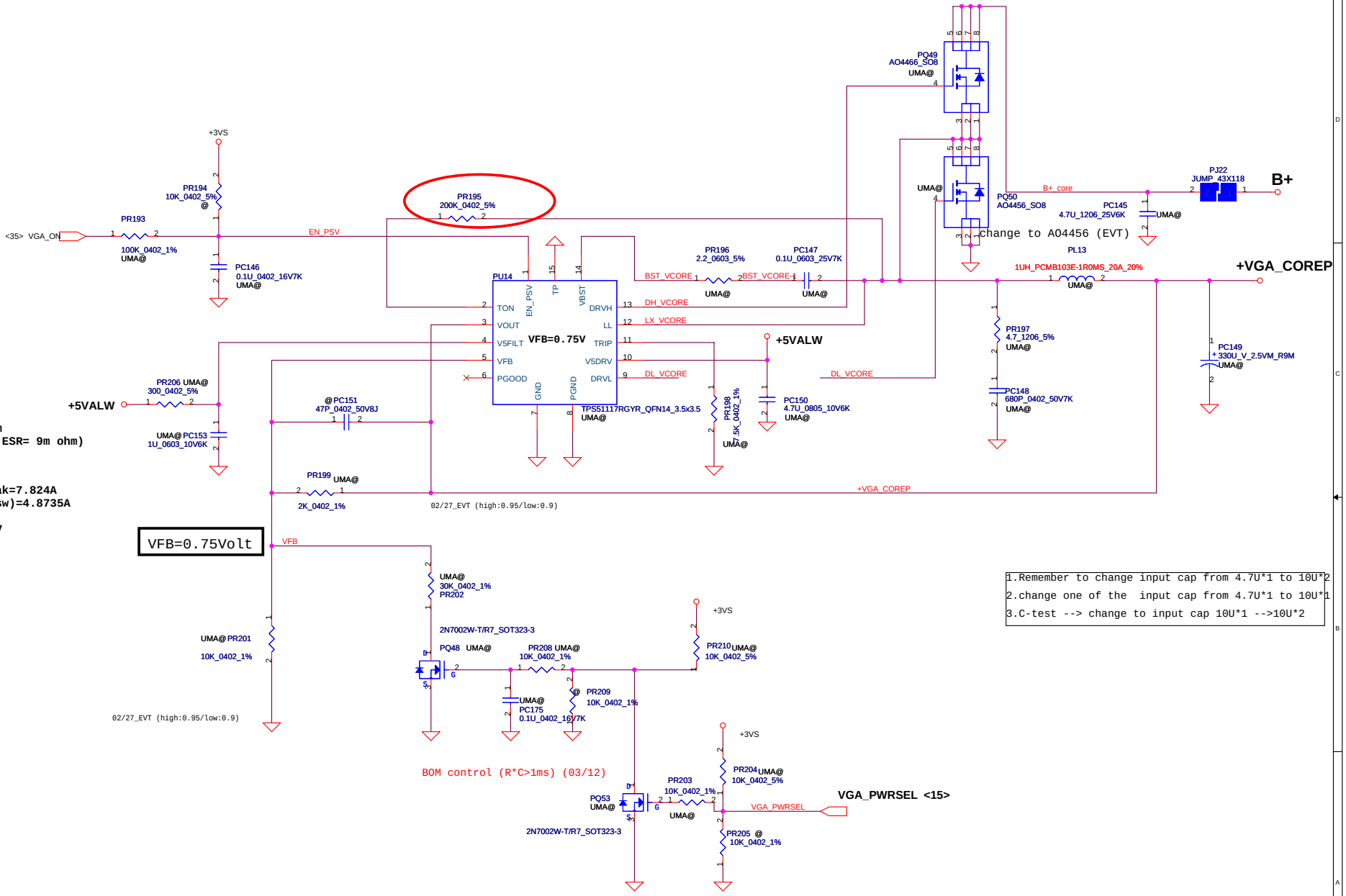

VFB=0.75V ; Rdson=4.6m ~ 5.6m ohm
L(1U,DCR= 2.7~3.0m ohm); C(330 U,ESR= 9m ohm)
Vo=VFB*(1+PR116/PR117)=0.95V
Fsw=254.237KHz

Ipeak=6.52A, Imax=4.564A,1.2*Ipeak=7.824A
Delta I=((19-1.2)*(1.2/19))/(L*Fsw)=4.8735A
=>1/2DeltaI=2.4367A
Vtrip=Rtrip*10uA=7.5K*10uA=0.075V
Iocp=12.0031~16.0237A

	M92-M2 XT
VGA_PWRSEL	Core Voltage Level
0	0.95V
1	0.9V

1.Remember to change input cap from 4.7U*1 to 10U*2
2.change one of the input cap from 4.7U*1 to 10U*1
3.C-test --> change to input cap 10U*1 -->10U*2

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Version change list (P.I.R. List)

for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	ADD circuit	Switch NB_core voltage	0.1	50	ADD PC107, PC105, PR121, PR123, PR122, PR102, PQ25, PQ28 at UMA Sku	2009/01/04	DVT
2	ADD circuit	Switch NB_core voltage	0.1	51	ADD PC110, PC111, PC108, PC109, PC1113, PR1128, PR194, PR129, PR127 at UMA Sku	2009/01/04	DVT
3	ADD snubber	EMI requestmrnt	0.1	50	Add PR104 4.7 ohm and PC83 680p	2009/01/04	DVT
4	ADD snubber	EMI requestmrnt	0.1	50	Add PR108 4.7 ohm and PC89 680p	2009/01/04	DVT
5	ADD CPU boot	EMI requestmrnt	0.1	53	Add PR229 2.2 ohm	2009/01/04	DVT
6	ADD CPU boot	EMI requestmrnt	0.1	53	Add PR243 2.2 ohm	2009/01/04	DVT
7	Change resistance value	Switch NB_core voltage	0.1	50	Change PR95 from 51 Kohm to 39.2 Kohm	2009/01/04	DVT
8	Change resistance value	Switch NB_core voltage	0.1	50	Change PR122 from 12 Kohm to 226 Kohm	2009/01/04	DVT
9	Change resistance value	soft start of Switch NB_core voltage	0.1	50	Change PR123 from 0 ohm to 10 Kohm	2009/01/04	DVT
10	Change capacitor value	soft start of Switch NB_core voltage	0.1	50	Change PC105 from 0.01 uF to o.1 uF	2009/01/04	DVT
11	Change IC part number	Change IC part number	0.1	48	Change PU4 part number to SA00002V400	2009/01/04	DVT
12							
13							
14							
15							
16							
17							
18							
19							
20							
21							
22							
23							

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PHASE	PAGE	Modification list	PURPOSE
PVT	P.29	Delete Q24 and modify ODD power circuit	Modify ODD power circuit to follow up SUSP#
	P.36	Change L94~L97 to bead , delete C1184/C1193	Follow Realtek suggest
	P.37	Change SPDIF detec power +5VAMP to +5VS	
		C45、C466 Change to 10U	
	P.33	Add R566、R567 for e-machine	
	4/20	Add H34	For FAN
	4/21	Add LAN_DET function	For FAN
		IO/B PLT_RST# change to JP21	For ESD
	4/22	Add R212	For VRAM ID
		Update USB footprint -FOX_UB511AC-RABA7-7F_4P-T	
		C536 Change to 220U	
	4/23	Add C39、C41、C778、C780	For ESD
	4/24	Change Lid SW power to +3VL	

For Discrete

CRT

R285 VGA@ 150_0402_1%

R54 VGA@ 2.2K_0402_5%

R46 VGA@ 2.2K_0402_5%

C633 VGA@ 3.3P_0402_50V8J

C640 VGA@ 3.3P_0402_50V8J

C662 VGA@ 3.3P_0402_50V8J

C667 VGA@ 8P_0402_50V8J

C660 VGA@ 8P_0402_50V8J

C639 VGA@ 8P_0402_50V8J

HDMI

R141 VGA@ 499_0402_1%

R137 VGA@ 499_0402_1%

R149 VGA@ 499_0402_1%

R145 VGA@ 499_0402_1%

R155 VGA@ 499_0402_1%

R152 VGA@ 499_0402_1%

R158 VGA@ 499_0402_1%

R157 VGA@ 499_0402_1%

For E-Machine disable side port

R281 HM@ 3K_0402_5%

R223 HM@ 0_0402_5%

R406 HM@ 0_0603_5%

PCB

zzz

PCB 06F LA-5401P REV0 M/B

LA5401P MB Rev0: DA80000ET00

LA5401P MB Rev1: DA80000ET10

LA5401P MB with Sub/B Rev1: DAZ~

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