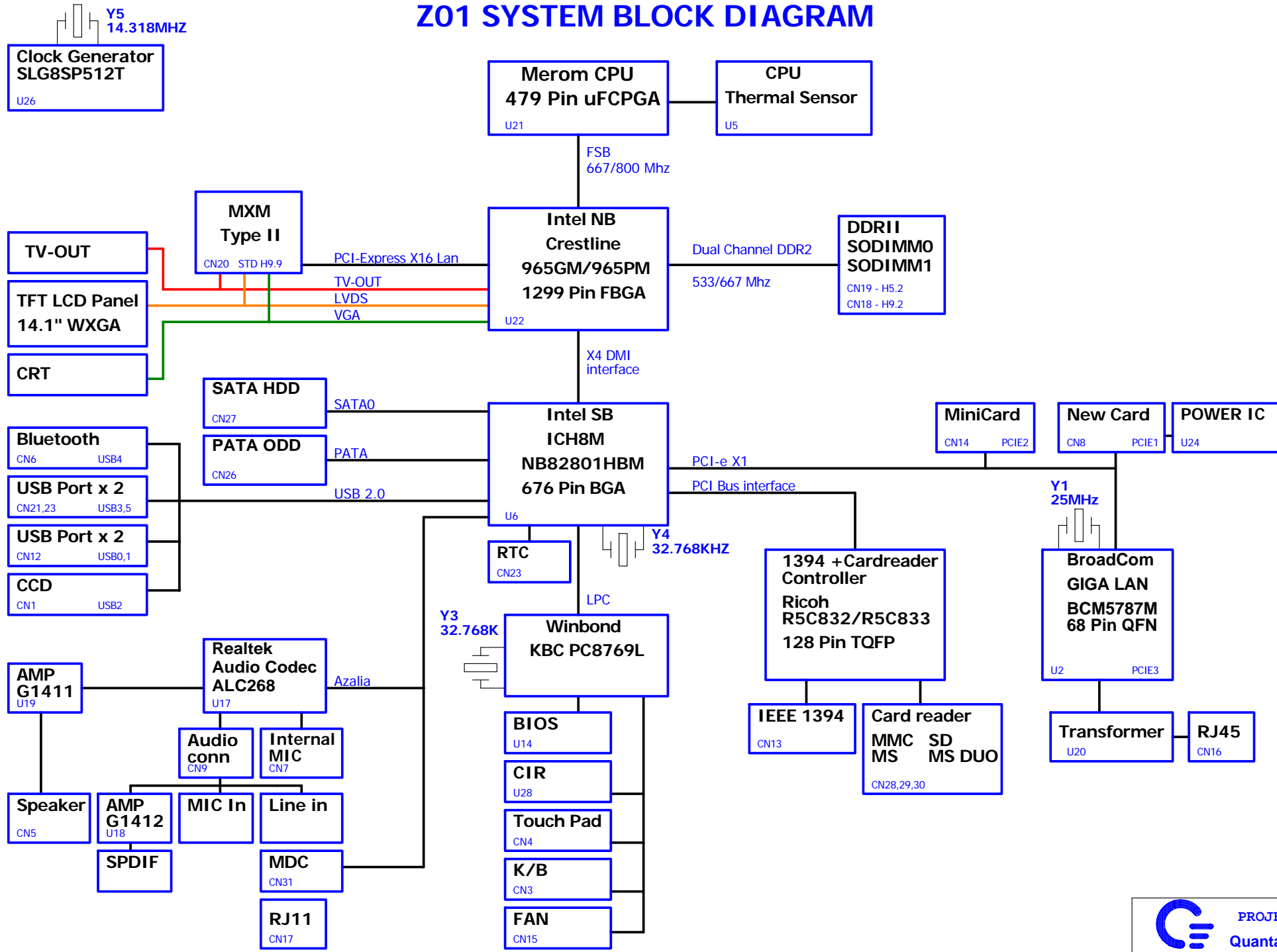


MODEL :	REV :	CHANGE LIST :	MODEL : Z01 MB
Z01 MotherBoard	1A	FIRST RELEASE	
	1B	PAGE02. 1. R447,455,456 MODIFY to EP P/N:CS14752FB11 PAGE03. 1. STUFF HOLE6 P/N:FBZ01007010 2. STUFF HOLE7,8,15 P/N:FBED8001016 , 3. STUFF HOLE5 P/N:FBZ01006010 PAGE03. 1. STUFF HOLE23,25 P/N:FBZ01003010 2. STUFF HOLE18 P/N:FBZ01004010 3. STUFF HOLE31 P/N:FBZ01005010 PAGE05. 1. U22 MODIFY to GM965 P/N:AJ00N120T04 , 2. R193,194 MODIFY to EP P/N:CS03902FB11 PAGE06. 1. R242 MODIFY to EP P/N:CS33002JB23 PAGE08. 1. L52,53 MODIFY to EP P/N:CV01004KNO0 PAGE11. 1. R332 MODIFY to EP P/N:CS23243F930 , 2. U6 MODIFY to ICH8 P/N:AJ00M740T03 PAGE12. 1. R244,R347,R353 MODIFY to EP P/N:CS00004JA40 , 2. L28 MODIFY to P/N:CV-1005MZ01 PAGE13. 1. CN10 MODIFY to CRT P/N:DFDS15FR611 PAGE15. 1. R467 MODIFY to EP P/N:CS00004JA40,2. R50 MODIFY to EP P/N:CS31003J941,3.CN27 MODIFY to SATA P/N:DFHS22FR005 PAGE16. 1. CN16 MODIFY to RJ45/11 P/N:DFTJ15FR057 PAGE18. 1. R317,323 MODIFY to 0603 P/N:CS31003F949 , 2. R310 MODIFY to EP P/N:CS31003J941 PAGE20. 1. PR100 MODIFY to EP P/N:CS51002FB11 PAGE21. 1. PR86 MODIFY to EP P/N:CS24022FB13 , 2. PR38,82 MODIFY to 1% P/N:CS31002FB26 , 3. PR83 MODIFY to EP P/N:CS00004JA40 PAGE22. 1. PR100 MODIFY to EP P/N:CS32002FB29 , 2. PR6 MODIFY to 1% P/N:CS51003F934 PAGE23. 1. PR106 MODIFY to 0 ohm P/N:CS00002JB38 , 2. UN-STUFF PR107,PC111 PAGE24. 1. PR29 MODIFY to EP P/N:CS31003J941 2. PJ1 MODIFY to BATTERY P/N:DFHD07MR006 PAGE25. 1. PR70 MODIFY to EP P/N:CS32002FB29	PAGE FROM TO 1 1A 2 2B 3 2B 4 2B 5 2B 6 2B 7 2B 8 2B 9 2A
	2A	PAGE02. 1. Connect VDDIO CLK to +1.25V 2. un-stuff R292;R445;R308 3. stuff C575,C574,C576,C578,C573,C546 for EMI issue PAGE06. 1. Connect ICH PWROK SIGNAL TO NB CLPWROK 2.un-stuff R242;R235;R422;R222;R421;R423 3. R360,R361 only stuff for UMA PAGE07. 1. MODIFY 22u to 10u PAGE08. 1. R489 MODIFY to 0805 2. Stuff L50;R182;C238 for EV@ (MXM) PAGE09. 1. Add PU for SMA MA14 ; SMB MA14 PAGE10. 1. un-stuff R337,C115,C127,C129,C298,C302,C294,C283,C291 PAGE11. 1. Q18 MODIFY to P/N:AL07SZ04C27 2.R395 connect to VCCRTC 3.R336;R251;R419;R255 un-stuff 4.R226 connect to +3V_S5 5.ICH_PWROK to SB CLPWROK PAGE11. 1. stuff C500,C509,C300,C513 33pF P/N:CH03306JB04 2. C507,C508 10pF change to 15pF P/N:CH01506JB06 , 3. stuff R238,R392,C2989 for Contr-LINK PAGE12. 1. VCCSDA & VCCSUSDA change to 3V PAGE13. 1. Add CRT DDC IN PU 2. R8, L9, L10 P/N change to 0.47UH for MXM , 3. C22,C24,C25,C27,C31,C32 P/N change to 47pF for MXM PAGE14. 1. CN6 MODIFY CONN. to 5 PIN P/N:DFHD05MRD98 PAGE15. 1. MODIFY SWITCH BOARD PIN DEFINE 2. Modify FAN circuit , 2. MR1 P/N change to AL000268000 PAGE16. 1. C46,C47 27pF change to 33pF P/N:CH03306JB04 2. stuff C104,C105,C119,C112 0.1uF P/N:CH41003ZB35 PAGE17. 1. CARD READER COLAY TO CN28, DEL CN30 2. C311 change to 27pF P/N:CH02706JB06 3. stuff R209 4. un-stff R213,C325,U11 PAGE18. 1. CHANGE MDC & CODEC to 3V 2.Delete D12 3. stuff R314,R483,C393,C595 PAGE19. 1. SWAP NBSWON# & ACIN 2. C363,C364 5.6pF change to 18pF P/N:CH01806JB07 PAGE20. 1. Modify PQ19 P/N PAGE21. 1. Modify Capacitor P/N to meet ME height limit PAGE22. 1. stuff PR74,PC69 2. Remove JP Pad PAGE23. 1. stuff PR126,PC131,PC137 2. Remove JP Pad 3. un-stuff +1.8V PAGE25. 1. un-stuff PR101,PQ21,PR22,PQ2,PR26,PR9,PR5,PC33,PC38,PC39,PC19,PC22,PU2	10 3A 3B 11 2B 12 2B 13 3A 3B 14 3A 15 3A 3B 16 3A 3B 17 2A 18 2B 3A 19 3A 3B 20 2B
	2B	PAGE02. 1. Change R293 to 2.2K for meet Intel Design checklist PAGE03. 1. Change XDP PU/PD resistors value to meet Intel Design checklist PAGE04. 1. Un-stuff C28,C457 PAGE05. 1. Add LVDS VREF strap PAGE06. 1. Add SDVO I2C strap PAGE07. 1. Remove NB resistors to GND PAGE08. 1. Remove DIODE for D27 2. Remove VCCA_DPLLA&B for external VGA PAGE10. 1. Add CRT & LVDS I2C Strap PAGE11. 1. Un-stuff Control Link Vref1 PAGE12. 1. Remove reserve ICH8 HDA 1.5V power rail PAGE13. 1. Modify LCD_VCC enable power rail 2. Add LVDS INV I2C Strap PAGE14. 1. Add EMI solution for debug port PCI clock PAGE15. 1. Change Q33,Q34 to MOSFET PAGE16. 1. Add PIN 59 & 3 PAGE18. 1. Change CN31 pin2 to +3V_S5 for Modem can't wake up from S3 PAGE19. 1. Add GPIO46 , 47 PAGE20~25. 1. Add EMI solution 2. Update Power component P/N	21 3A 22 3A 23 3A 3B 24 3A 25 3A 3B
	3A	PAGE10. 1. Add +2.5V & +1.8V capacitors for nVIDIA MXM card PAGE11. 1. Change C507,C508 to 15pF for RTC PAGE13. 1. Add C609 & C610 to meet CM2009 specification PAGE14. 1. Reserve +5VPCU & Add Q40,R540 for CIR PAGE15. 1. Add C611 for PLC hall IC 2. Stuff R60 for G995 PAGE19. 1. CN44 un-stuff 2. D322,D332 reserve for ESD PAGE21. 1. Modify PC85 value PAGE22. 1. Modify PR4,PC13 value for sequence PAGE23. 1. Add PQ22 for nVIDIA MXM +1.8V PAGE24. 1. Modify PF1 P/N PAGE25. 1. Add PU2 for nVIDIA MXM +2.5V	
	3B	PAGE10. 1. Remove R337 & Add R542,Q41,Q42 for Nvidia ACIN function PAGE13. 1. Add D34-D36,D40 for ESD solution PAGE15. 1. R484,R485,R486 from 330 change to 220 ohm for LED light issue 2. Add D41,D42,D43 for ESD 3. Stuff Q39 PAGE16. 1. Add C621,C622 for EMI solution 2. C112,C119 change to 100pF/50V for EMI PAGE18. 1. Un-stuff L55, stuff U16,R470,R471 for internal Mic. issue PAGE19. 1. Modify D32,D33 package to 0402 for ESD PAGE23. 1. Add PR140,PR141 for +1.8V vltage PAGE25. 1. Stuff PR22,PR101,PQ2,PQ21 for nVIDIA MXM +1.8V & +2.5V Discharge	

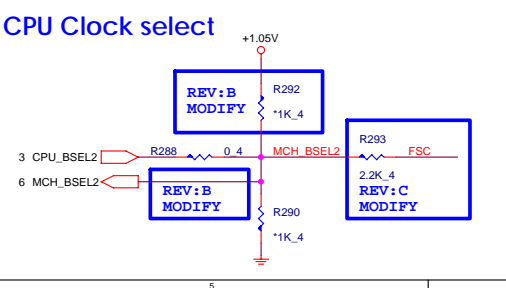
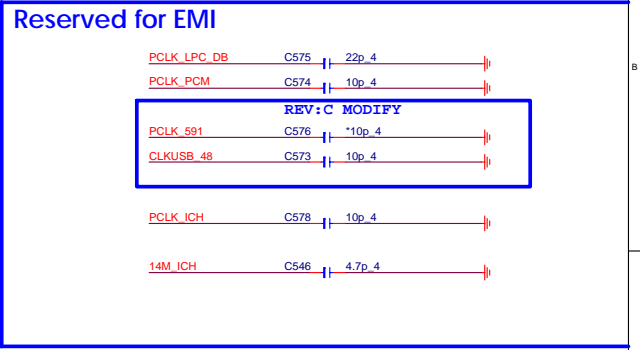
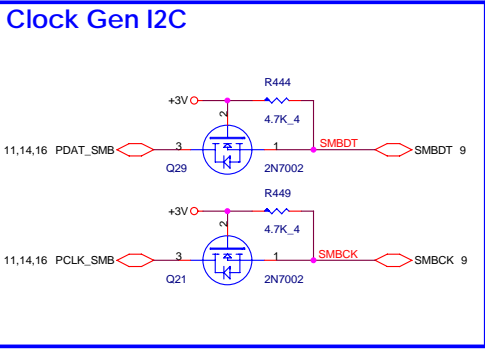
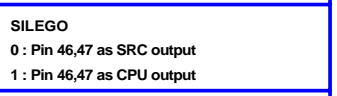
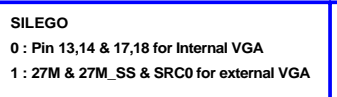
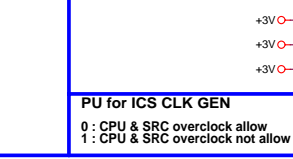
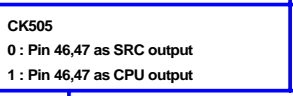
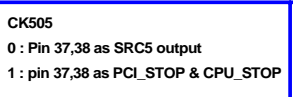
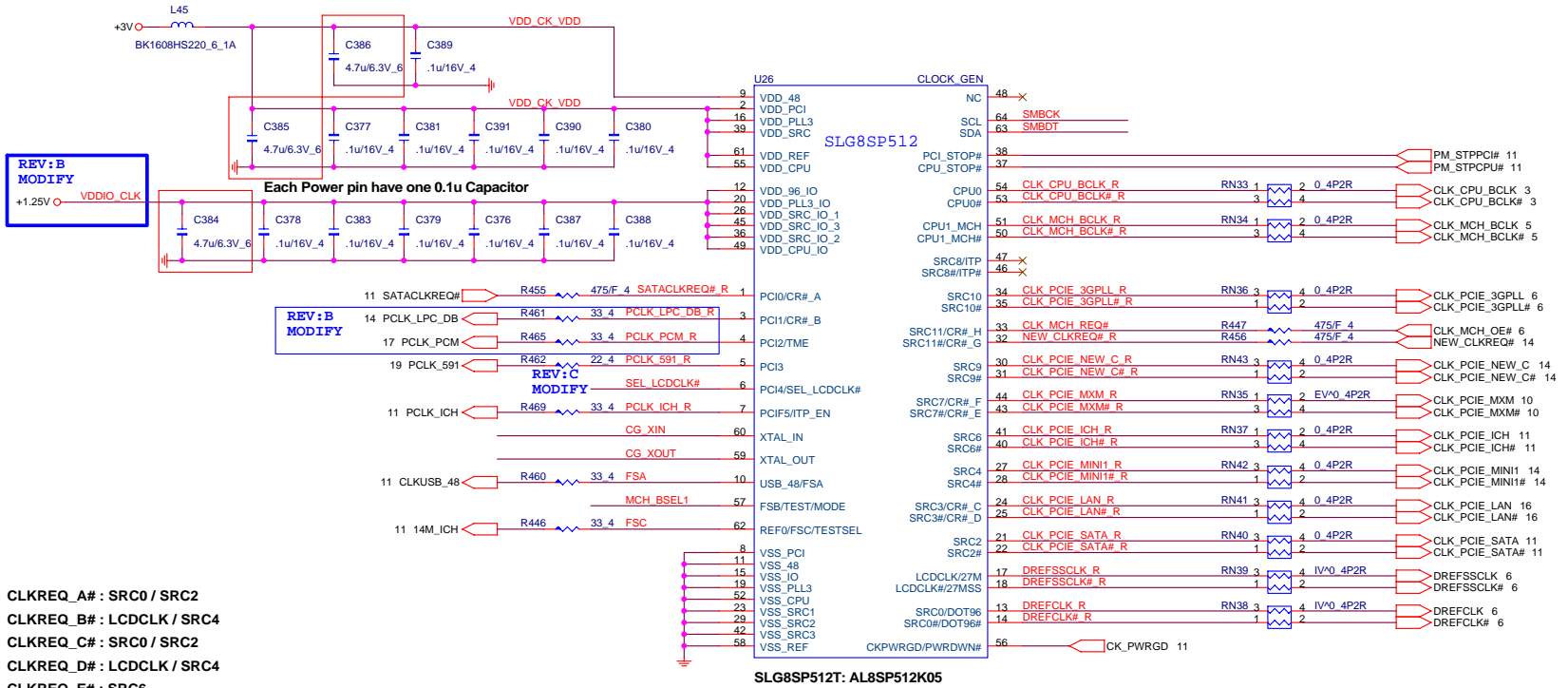


PROJECT : Z01	APPROVE BY: JIM HSU	DRAWING BY:JACKY CHENG	REV 3A
MB ASSY'S P/N : 31Z01MB00XX	PROJECT LEADER: JIM HSU	DOCUMENT NO: 204	DATE :2007/04/14

# Z01 SYSTEM BLOCK DIAGRAM



# Clock Generator



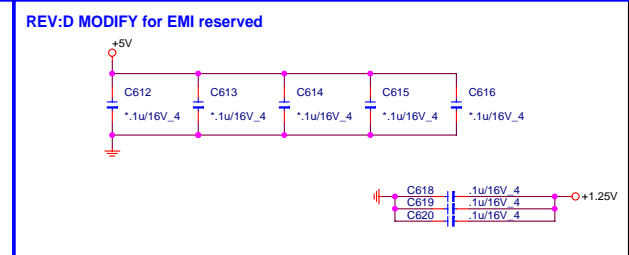
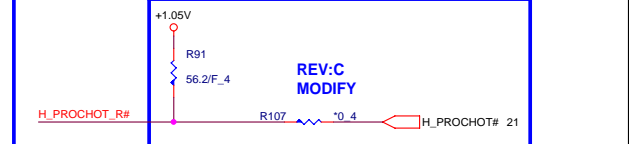
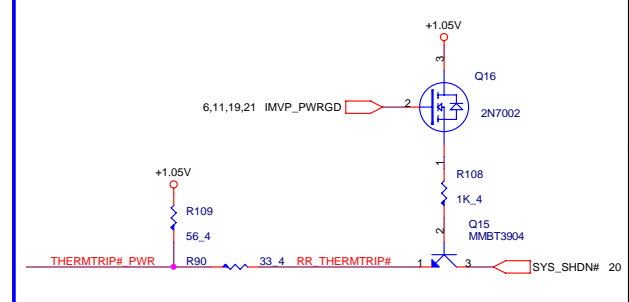
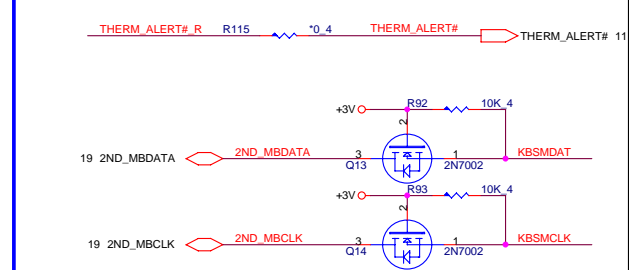
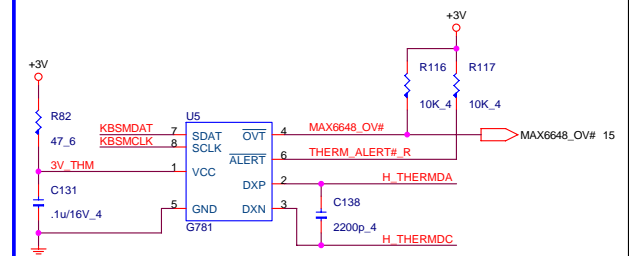
**BSEL Frequency Select Table**

FSC	FSA	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	0	200Mhz
0	1	1	166Mhz
1	0	0	333Mhz
1	0	1	100Mhz
1	1	0	400Mhz
1	1	1	Reserved

**PROJECT : ZO1**  
**Quanta Computer Inc.**

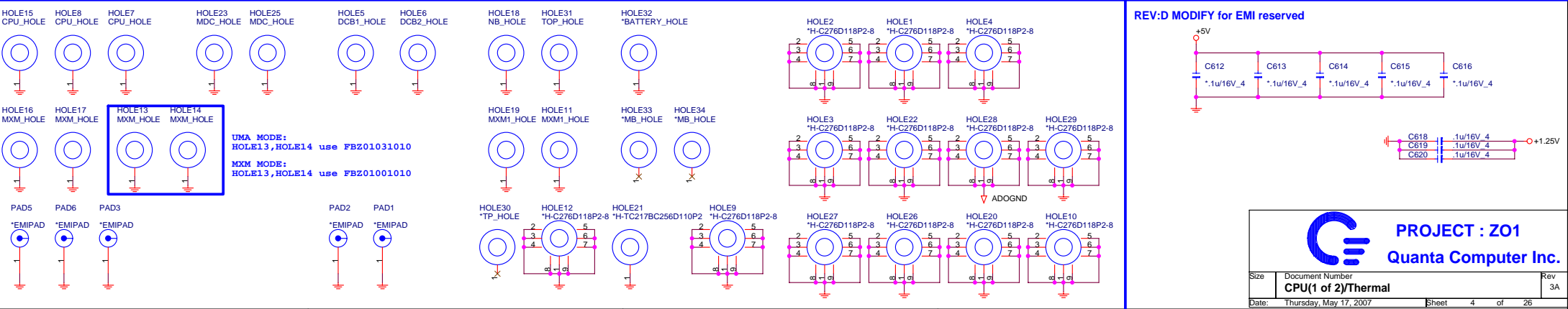
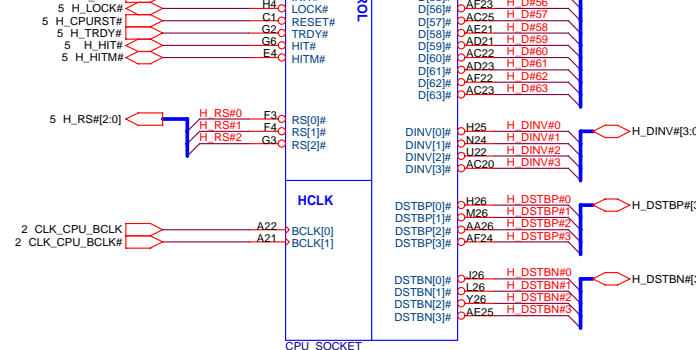
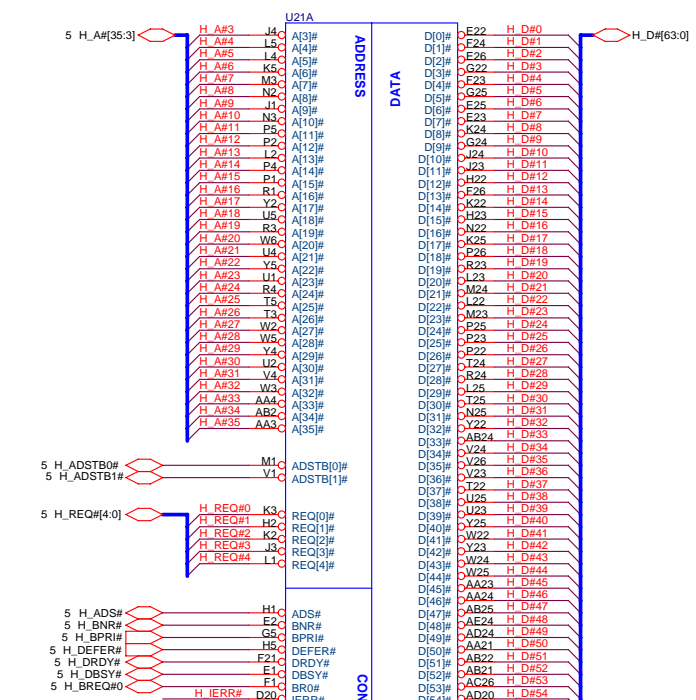
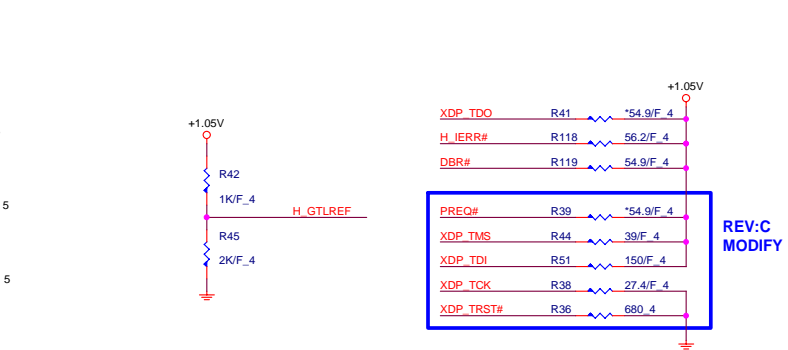
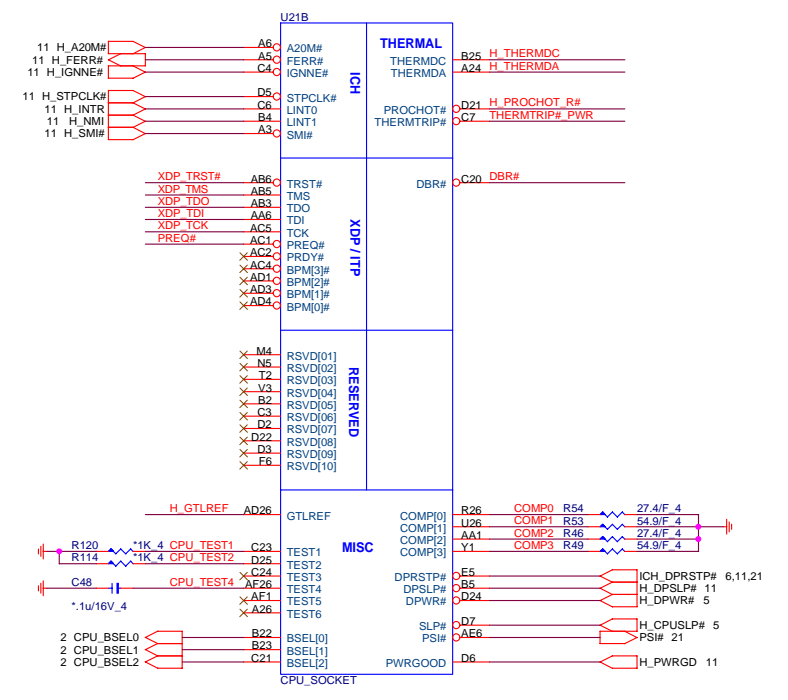
Size Document Number  
**CLOCK GENERATOR CK505 W/REGULATOR** Rev 2B  
Date: Thursday, May 17, 2007 Sheet 3 of 26

SMBUS Address : 98

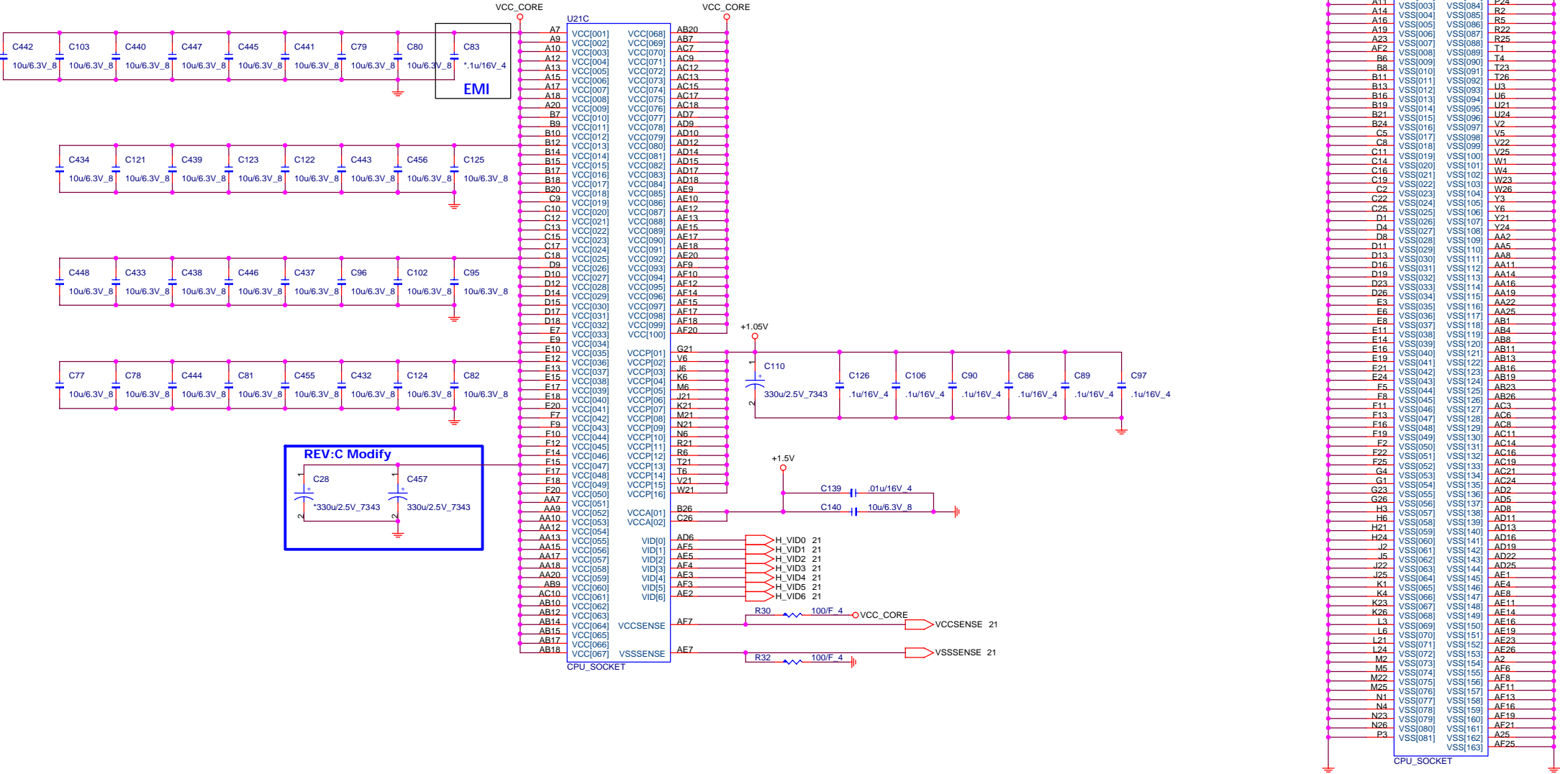



**PROJECT : ZO1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>CPU(1 of 2)/Thermal</b>	3A
Date:	Thursday, May 17, 2007	Sheet 4 of 26



# CPU(Power)



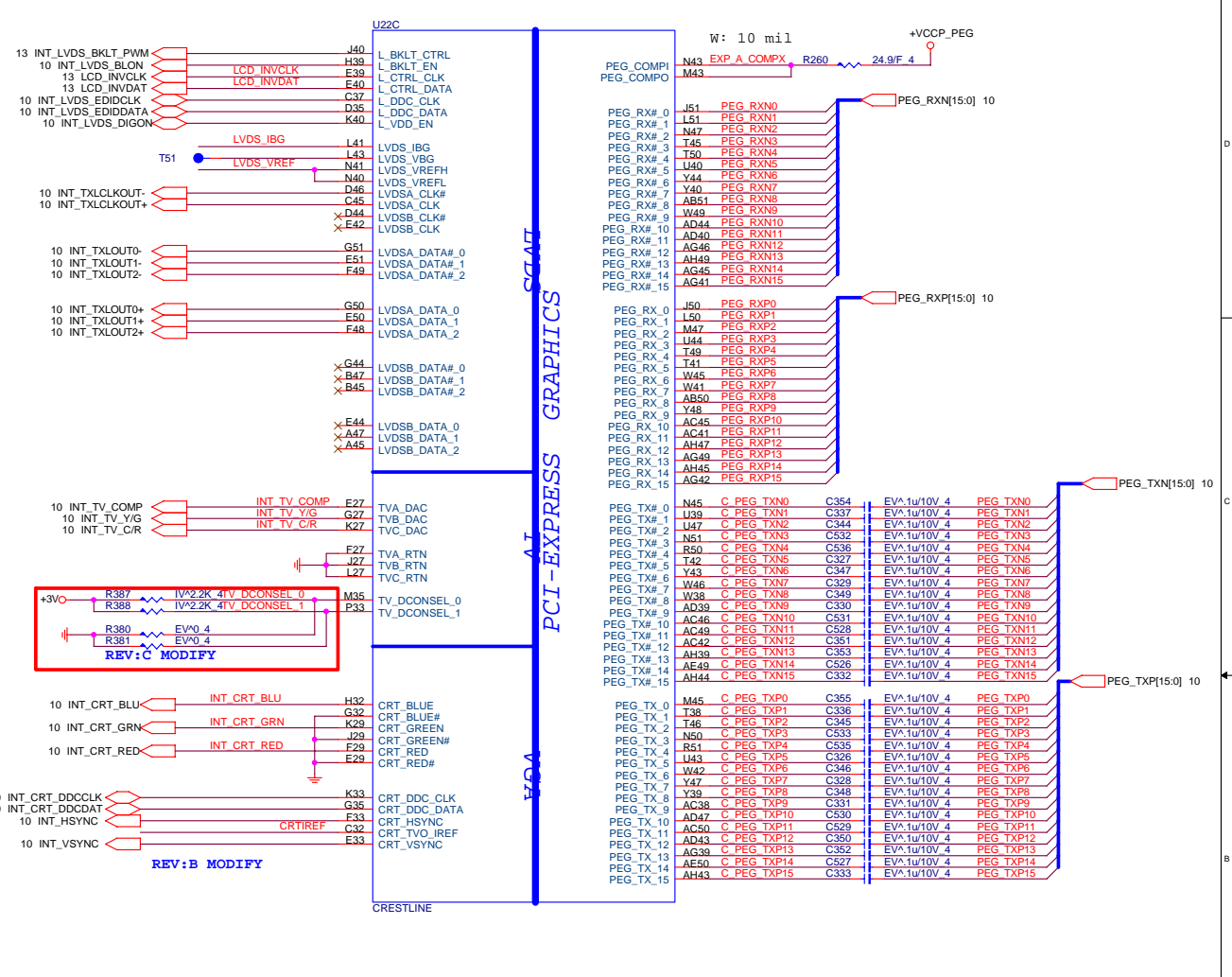
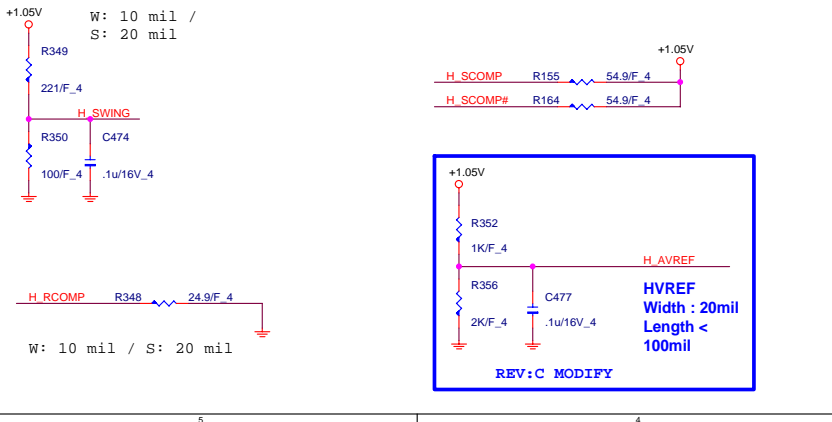
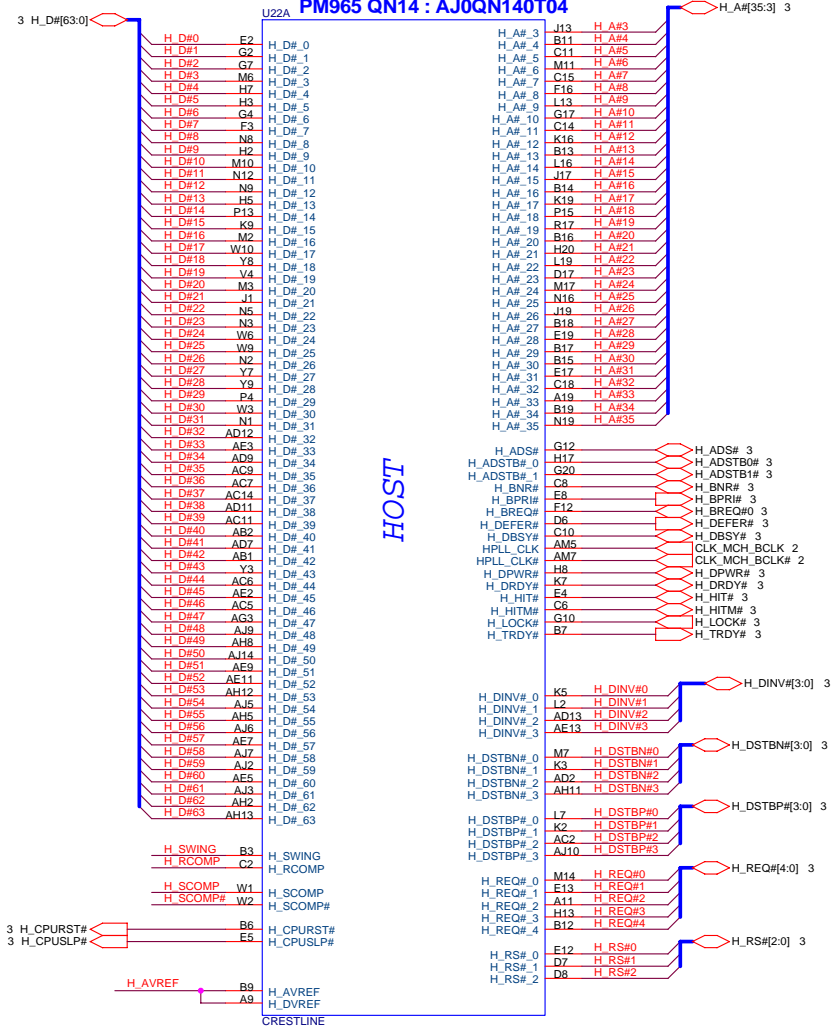


**PROJECT : Z01**  
Quanta Computer Inc.

Size	Document Number	Rev
	<b>CPU(2 of 2)Power</b>	2B
Date:	Thursday, May 17, 2007	Sheet 5 of 26



GM965 QN12 : AJ0QN120T04  
PM965 QN14 : AJ0QN140T04



**<check list>**  
For EV @  
Connect to GND  
CRT R/G/B  
TV A/B/C  
HSYNC/VSNC

**<check list>**  
For IV @  
Connect to 150ohm:  
CRT R/G/B  
TV A/B/C  
Connect to 30ohm:  
HSYNC/VSNC

**<check list & CRB> REV: C MODIFY**  
For Calero : 1.5K  
For Cresline:2.4K

**OHM (PD) FOR EV (TV)**

R205 EV#0.4 INT\_HSYNC  
R206 EV#0.4 INT\_VSYNC

R197 0.4 INT\_TV\_COMP  
R198 0.4 INT\_TV\_YIG  
R199 0.4 INT\_TV\_C/R

**OHM (PD) FOR EV (RGB)**

R214 0.4 INT\_CRT\_BLU  
R216 0.4 INT\_CRT\_GRN  
R204 0.4 INT\_CRT\_RED

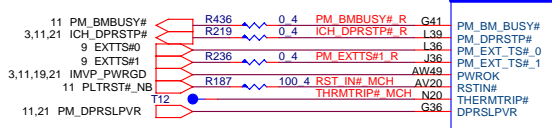
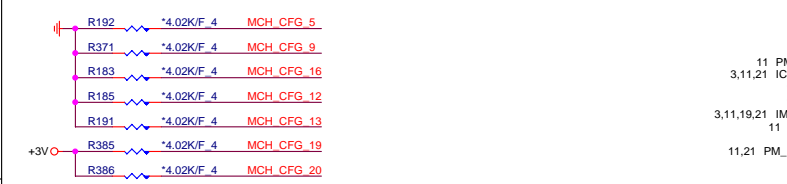
**IV&EV Dis/Enable setting**

**<check list & CRB>**  
For Calero : 255 <-FAE>  
For Cresline:1.3K/F  
For external VGA.0

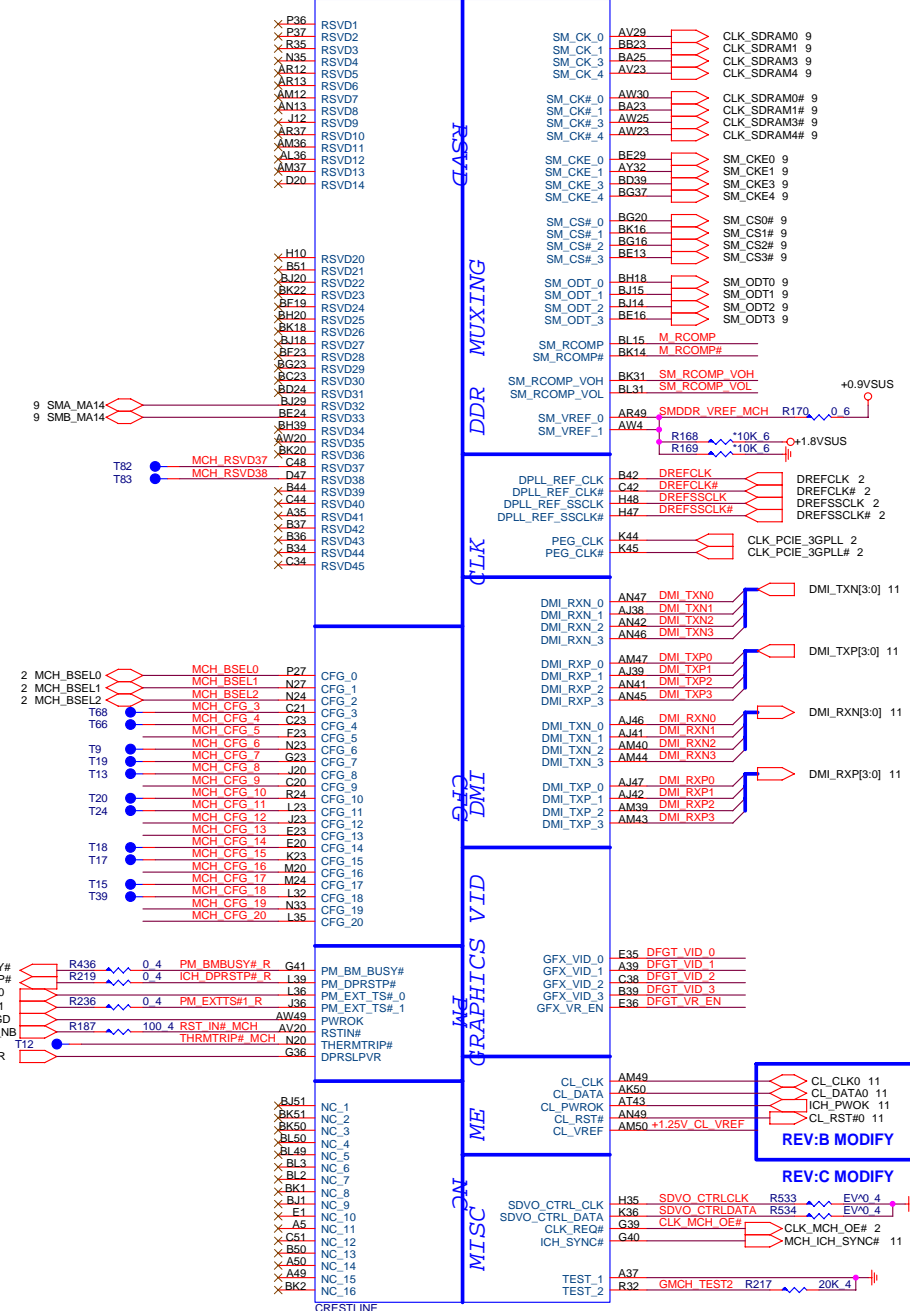
R211 0.4 CRTIREF

All strap are sampled with respect to the leading edge of the GMCH PWROK signal  
 CFG[17:3] Have internal Pull-up  
 CFG[18:19] Have internal Pull-down  
 Any CFG signal strapping option not list below should be left NC Pin

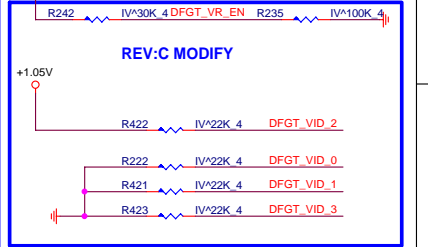
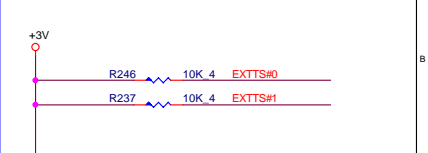
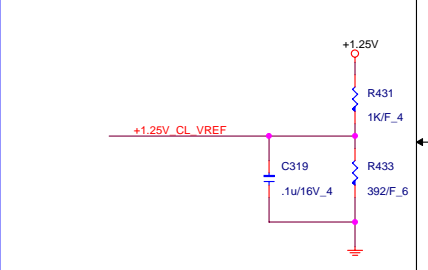
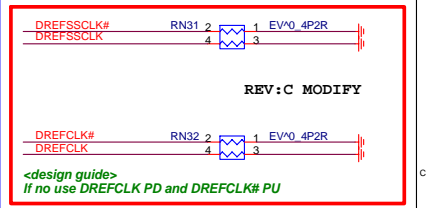
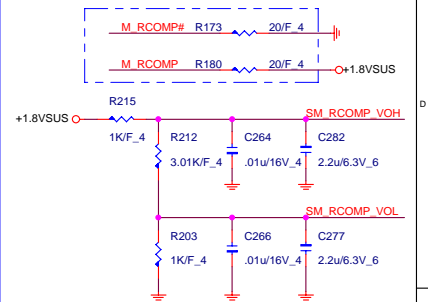
CFG[2:0]	FSB Frequency Select	001 = FSB 533 MHz 010 = FSB 800 MHz 011 = FSB 667 MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU(Default)
CFG8	Low power PCI Express	0 = Normal mode 1 = Low Power mode
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALLZ	00 = Reserved 01 = XOR Mode Enable 10 = All-Z Mode Enabled 11 = Normal operation(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
CFG18	VCC select	0 = 1.05V (Default) 1 = 1.5V
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present(Default) 1 = SDVO Card Present
CFG19	DMI Lane Reversal	0 = Normal operation(Default) 1 = Reverse Lanes
CFG20	SDVO/PCIE concurrent	0 = Only SDVO or PCIE x1 is operation(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port



GM965 QN12 : AJQN120T04  
 PM965 QN14 : AJQN140T04



Width : 20mil  
 Length < 500mil  
 <check list & CRB>  
 R Value select  
 For Calero : 80.6ohm  
 For Crestline:20ohm  
 But check list use 80.6ohm

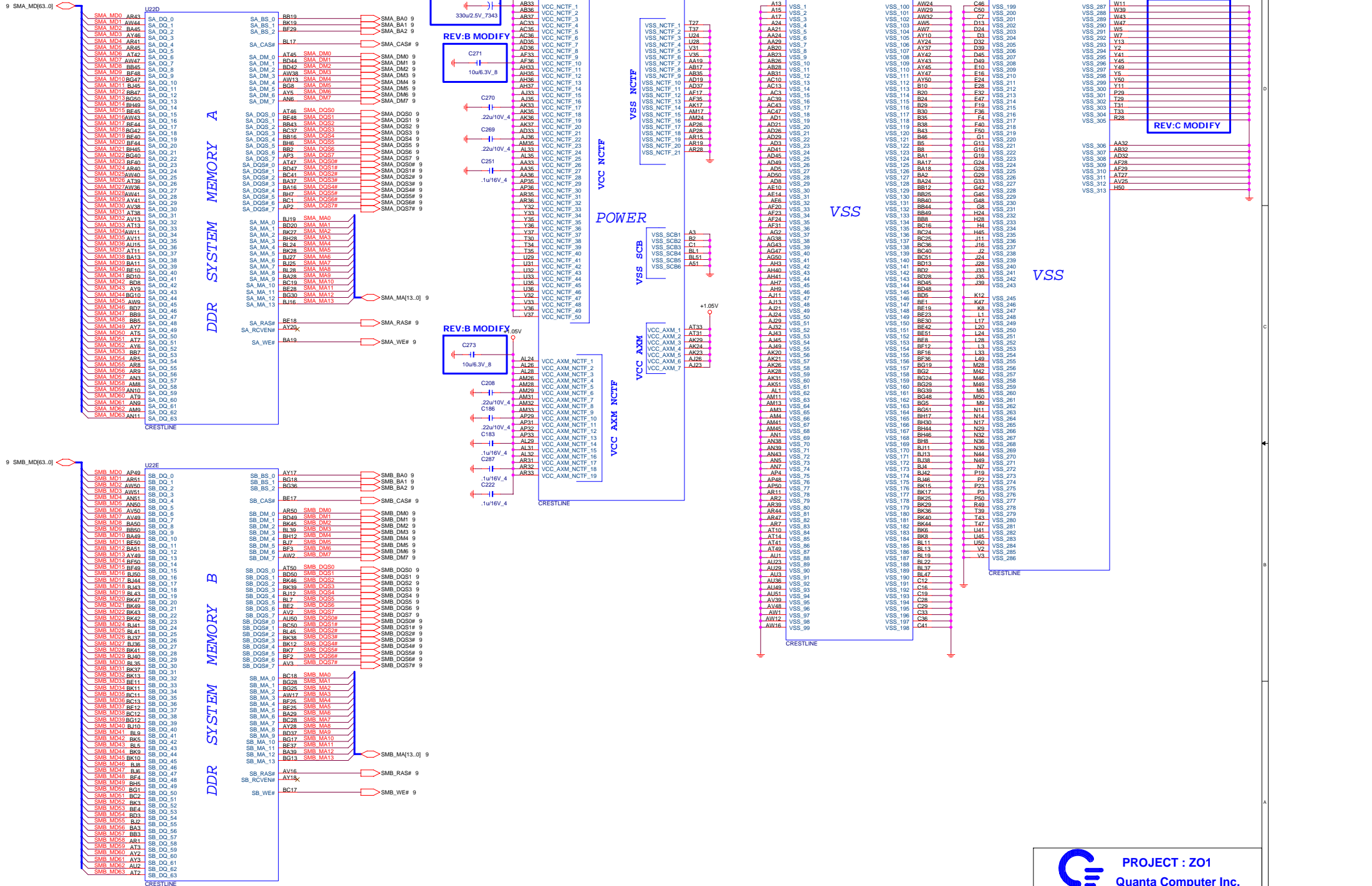


**PROJECT : ZO1**  
**Quanta Computer Inc.**

Size Document Number Rev 2B  
**GMCH DMI & STRAP**

Date: Thursday, May 17, 2007 Sheet 7 of 26

GM965 QN12 : AJQ0N120T04  
PM965 QN14 : AJQ0N140T04





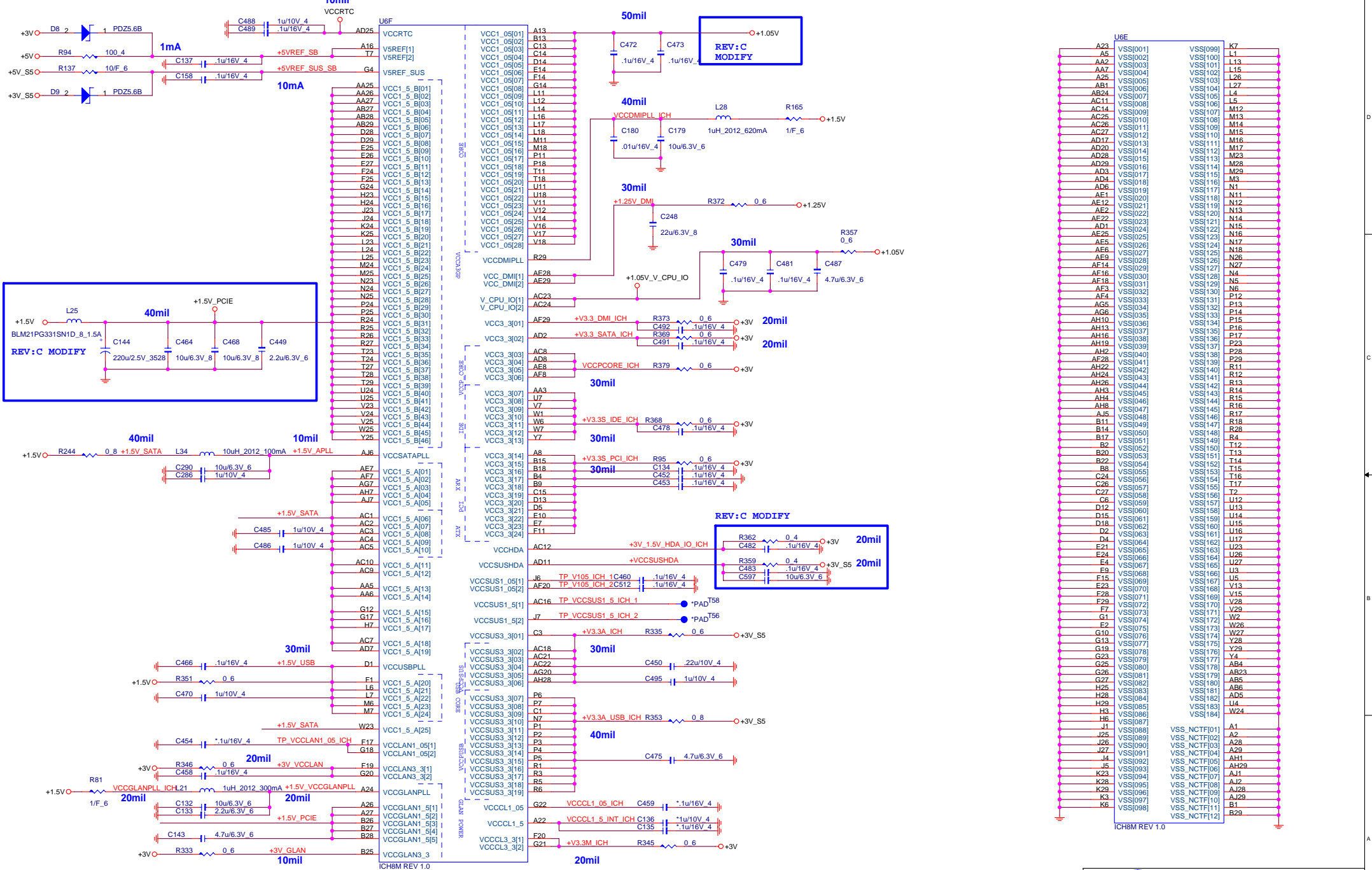










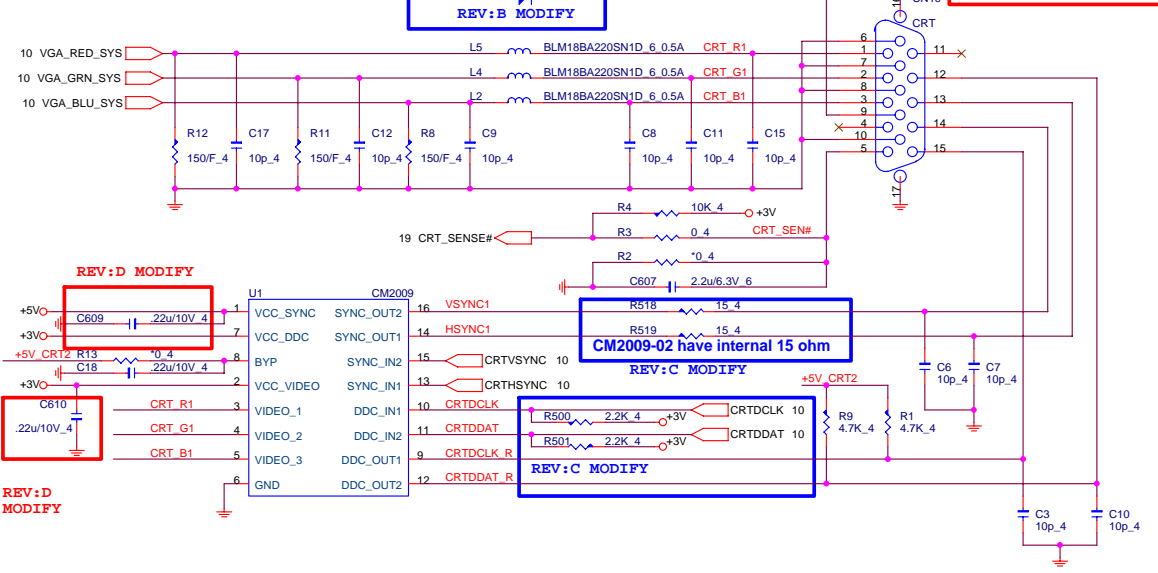


U6E		U6E	
A23	VSS[001]	VSS[099]	K7
A5	VSS[002]	VSS[100]	L1
AA2	VSS[003]	VSS[101]	L13
AA7	VSS[004]	VSS[102]	L15
A25	VSS[005]	VSS[106]	L26
AB1	VSS[006]	VSS[107]	L27
AB24	VSS[007]	VSS[108]	L4
AC11	VSS[008]	VSS[109]	L5
AC14	VSS[009]	VSS[110]	M12
AC26	VSS[010]	VSS[111]	M13
AC27	VSS[012]	VSS[112]	M14
AD17	VSS[013]	VSS[113]	M15
AD21	VSS[014]	VSS[114]	M16
AD28	VSS[015]	VSS[117]	M17
AD29	VSS[016]	VSS[118]	M23
AD4	VSS[017]	VSS[119]	M28
AD6	VSS[018]	VSS[120]	M29
AE1	VSS[019]	VSS[121]	N1
AE12	VSS[021]	VSS[122]	N11
AE2	VSS[022]	VSS[123]	N12
AE22	VSS[023]	VSS[124]	N13
AD1	VSS[024]	VSS[125]	N14
AE25	VSS[026]	VSS[126]	N15
AE5	VSS[027]	VSS[127]	N16
AE6	VSS[028]	VSS[128]	N17
AE14	VSS[029]	VSS[129]	N18
AF16	VSS[030]	VSS[130]	N26
AF18	VSS[031]	VSS[131]	N27
AG5	VSS[032]	VSS[132]	N4
AG6	VSS[033]	VSS[133]	N5
AH10	VSS[034]	VSS[134]	N6
AH11	VSS[035]	VSS[135]	P12
AH12	VSS[036]	VSS[136]	P13
AH16	VSS[037]	VSS[137]	P14
AH19	VSS[038]	VSS[138]	P15
AH2	VSS[039]	VSS[139]	P16
AH22	VSS[040]	VSS[140]	P21
AH24	VSS[043]	VSS[141]	P22
AH26	VSS[044]	VSS[142]	P28
AH3	VSS[045]	VSS[143]	P29
AH4	VSS[046]	VSS[144]	R12
AH8	VSS[047]	VSS[145]	R13
AJ5	VSS[048]	VSS[146]	R16
B11	VSS[049]	VSS[147]	R17
B17	VSS[050]	VSS[148]	R18
B2	VSS[051]	VSS[149]	R4
B20	VSS[052]	VSS[150]	T12
B25	VSS[053]	VSS[151]	T13
B6	VSS[054]	VSS[152]	T14
C24	VSS[055]	VSS[153]	T15
C26	VSS[056]	VSS[154]	T16
C27	VSS[057]	VSS[155]	T2
D12	VSS[058]	VSS[156]	T17
D15	VSS[059]	VSS[157]	T18
D18	VSS[060]	VSS[158]	T19
D2	VSS[061]	VSS[159]	T20
D4	VSS[062]	VSS[160]	T21
E21	VSS[063]	VSS[161]	T22
E24	VSS[064]	VSS[162]	U23
E4	VSS[065]	VSS[163]	U26
E5	VSS[066]	VSS[164]	U27
F15	VSS[067]	VSS[165]	U3
F23	VSS[068]	VSS[166]	U13
F28	VSS[069]	VSS[167]	U16
F7	VSS[070]	VSS[168]	U18
G1	VSS[071]	VSS[169]	U19
G2	VSS[072]	VSS[170]	U28
G10	VSS[073]	VSS[171]	U29
G19	VSS[074]	VSS[172]	Y2
G23	VSS[075]	VSS[173]	Y26
G26	VSS[076]	VSS[174]	Y27
G27	VSS[077]	VSS[175]	Y28
H25	VSS[078]	VSS[176]	Y4
H28	VSS[079]	VSS[177]	Y4
H3	VSS[080]	VSS[178]	Y29
H6	VSS[081]	VSS[179]	Y30
J1	VSS[082]	VSS[180]	AB23
J25	VSS[083]	VSS[181]	AB5
J28	VSS[084]	VSS[182]	AB6
J27	VSS[085]	VSS[183]	AD5
J4	VSS[086]	VSS[184]	L14
J5	VSS[087]	VSS[184]	W24
J6	VSS[088]	VSS[184]	W24
J22	VSS[088]	VSS[184]	W24
J23	VSS[089]	VSS[184]	W24
J27	VSS[090]	VSS[184]	W24
J4	VSS[091]	VSS[184]	W24
J5	VSS[092]	VSS[184]	W24
K23	VSS[093]	VSS[184]	W24
K28	VSS[094]	VSS[184]	W24
K29	VSS[095]	VSS[184]	W24
K3	VSS[096]	VSS[184]	W24
K6	VSS[097]	VSS[184]	W24
K8	VSS[098]	VSS[184]	W24
VSS_NCTFF[01]	VSS_NCTFF[01]	VSS_NCTFF[12]	A1
VSS_NCTFF[02]	VSS_NCTFF[02]	VSS_NCTFF[12]	A2
VSS_NCTFF[03]	VSS_NCTFF[03]	VSS_NCTFF[12]	A29
VSS_NCTFF[04]	VSS_NCTFF[04]	VSS_NCTFF[12]	A11
VSS_NCTFF[05]	VSS_NCTFF[05]	VSS_NCTFF[12]	AH29
VSS_NCTFF[06]	VSS_NCTFF[06]	VSS_NCTFF[12]	A12
VSS_NCTFF[07]	VSS_NCTFF[07]	VSS_NCTFF[12]	A128
VSS_NCTFF[08]	VSS_NCTFF[08]	VSS_NCTFF[12]	A129
VSS_NCTFF[09]	VSS_NCTFF[09]	VSS_NCTFF[12]	B1
VSS_NCTFF[10]	VSS_NCTFF[10]	VSS_NCTFF[12]	B29
VSS_NCTFF[11]	VSS_NCTFF[11]	VSS_NCTFF[12]	B29
VSS_NCTFF[12]	VSS_NCTFF[12]	VSS_NCTFF[12]	B29



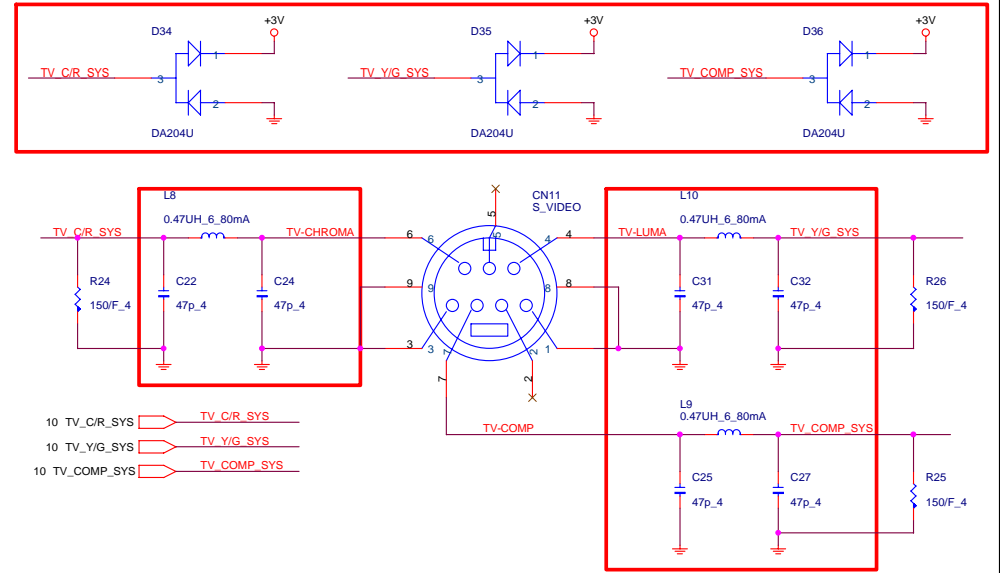
# CRT

**UMA mode**  
 1. C8,9,11,12,15,17 use 4.7pF CH-4716TB06  
 2. L2,L4,L5 use CX8BA470003

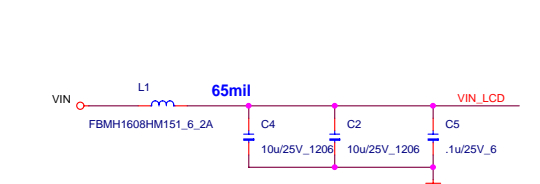
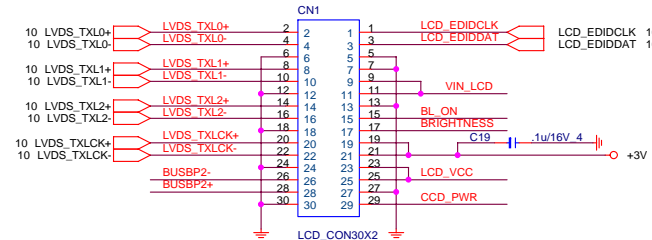


# S-VIDEO

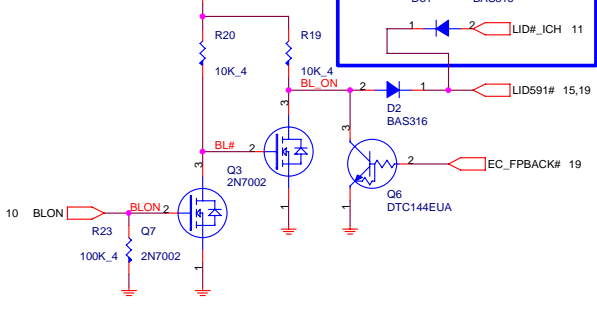
**UMA mode**  
 1. C22,C24,C25,C27,C31,C32 use 6pF CH00606TB04  
 2. L8,L9,L10 use CX8LL121002



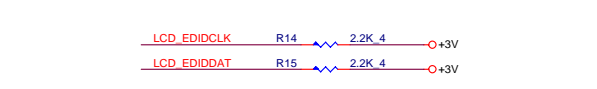
# LVDS



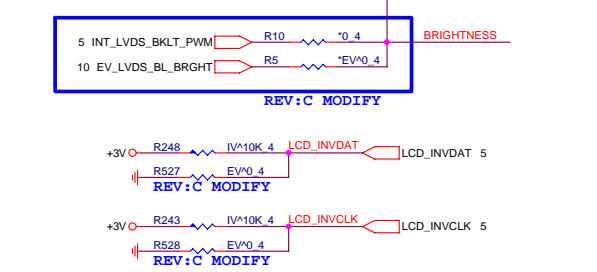
# Backlight Control



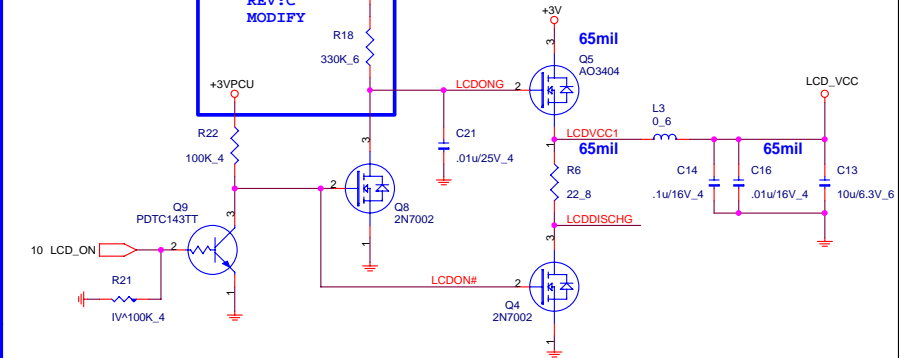
# LCD EDID SMBus Pu



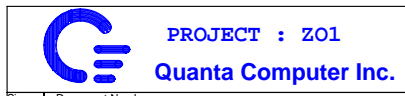
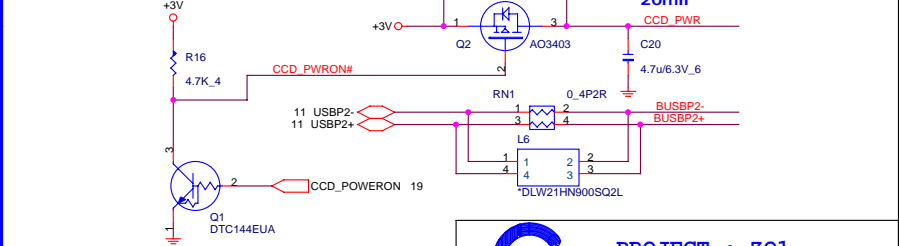
# DPST



# LCD\_ON

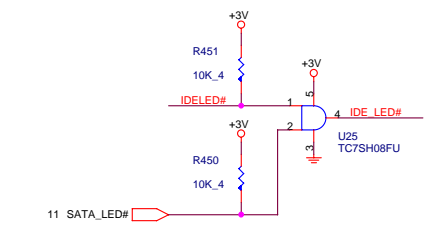
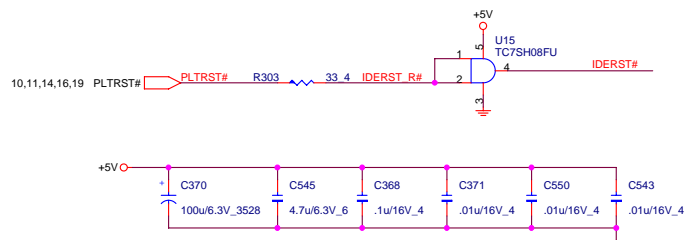
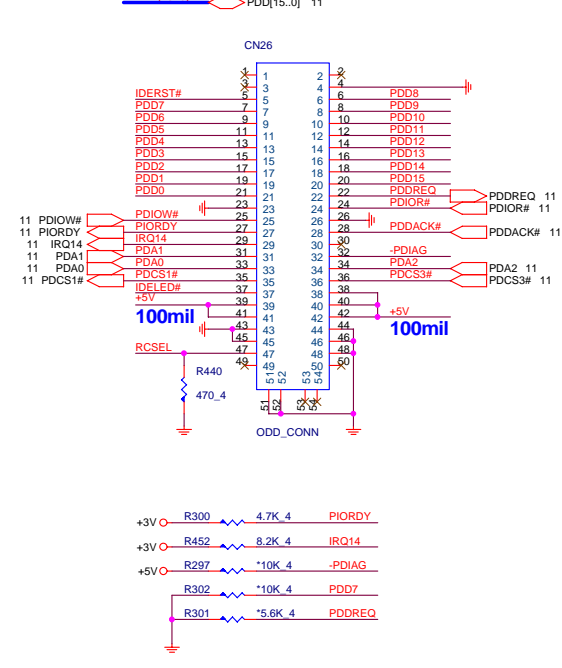


# Camera

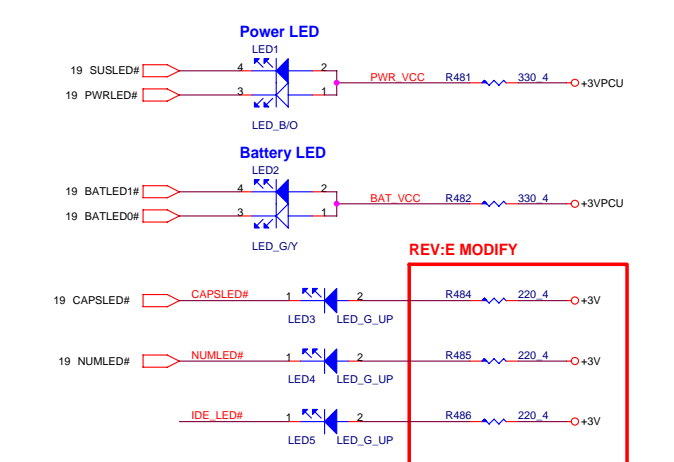




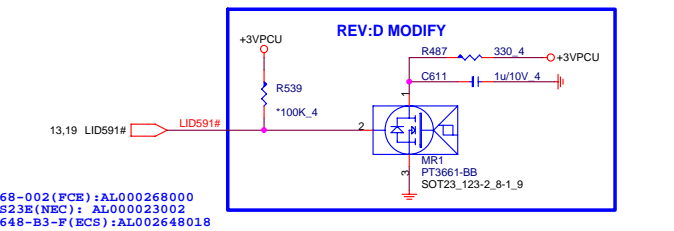
# ODD



# LED

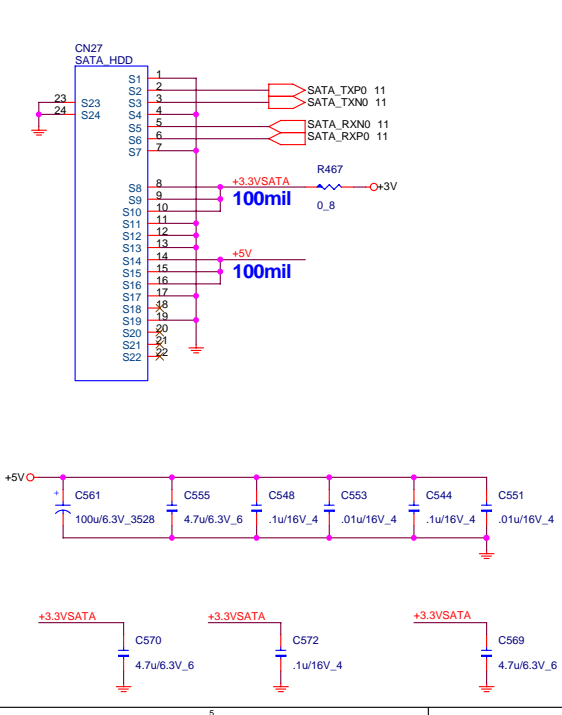


# LID

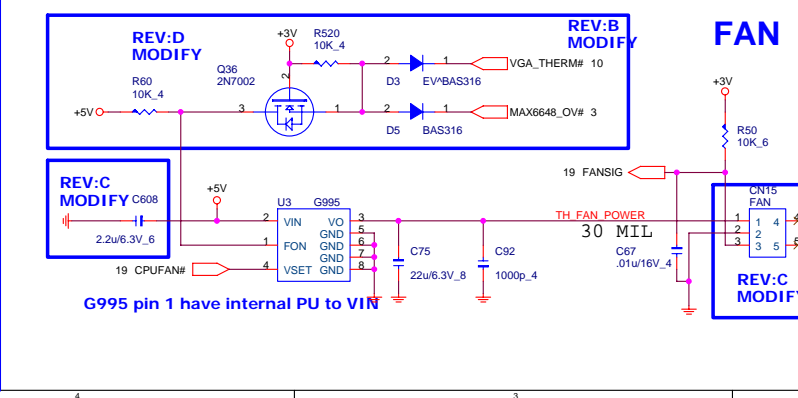
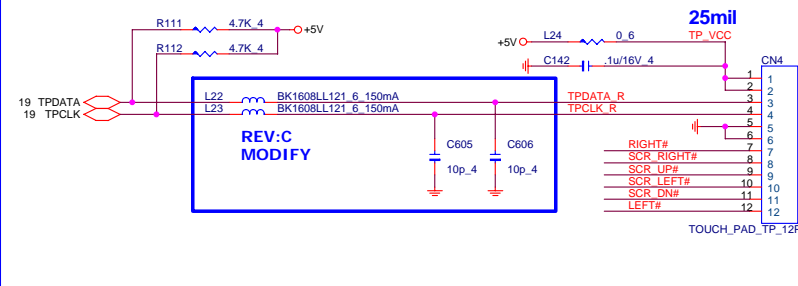


ME268-002 (FCE) : AL000268000  
 MRS2323E (NEC) : AL000023002  
 EC2648-B3-F (ECS) : AL002648018

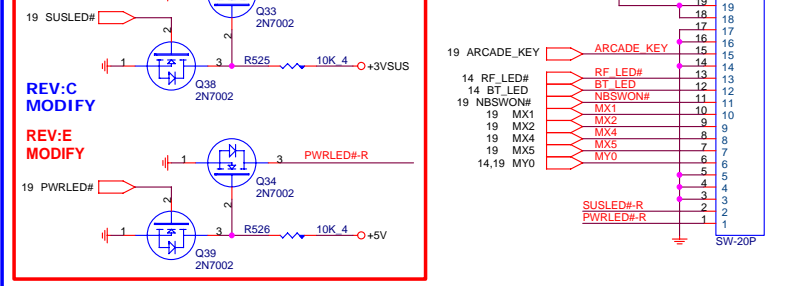
# SATA



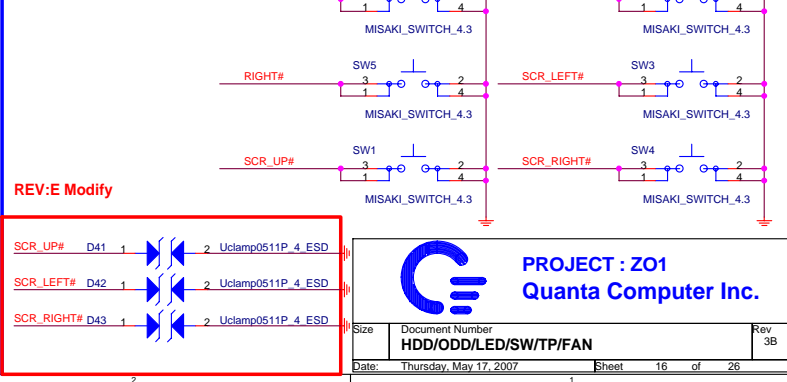
# TP CONN



# TO SW/B



# TP SWITCH

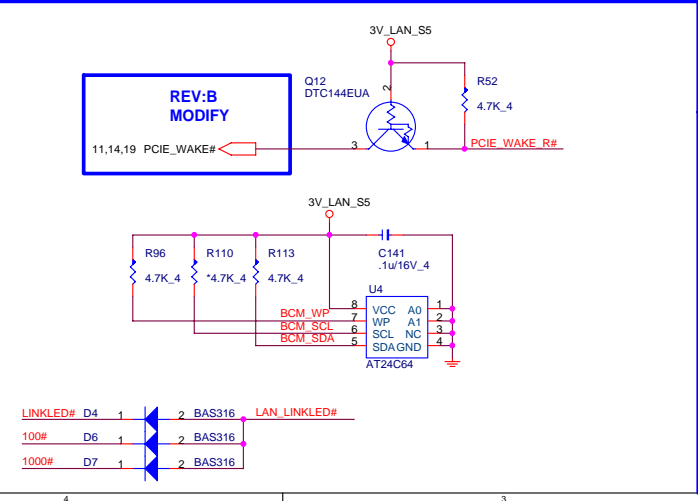
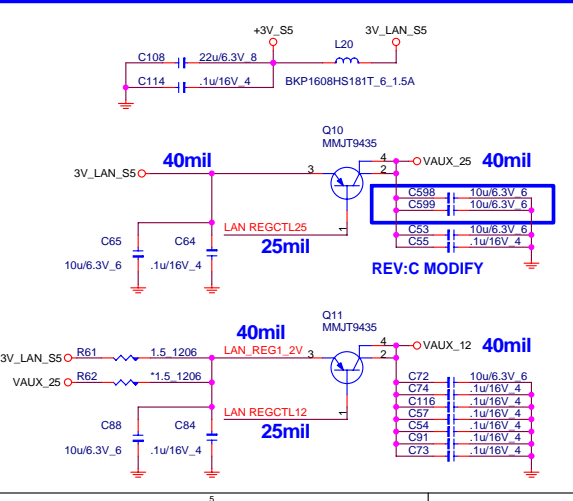
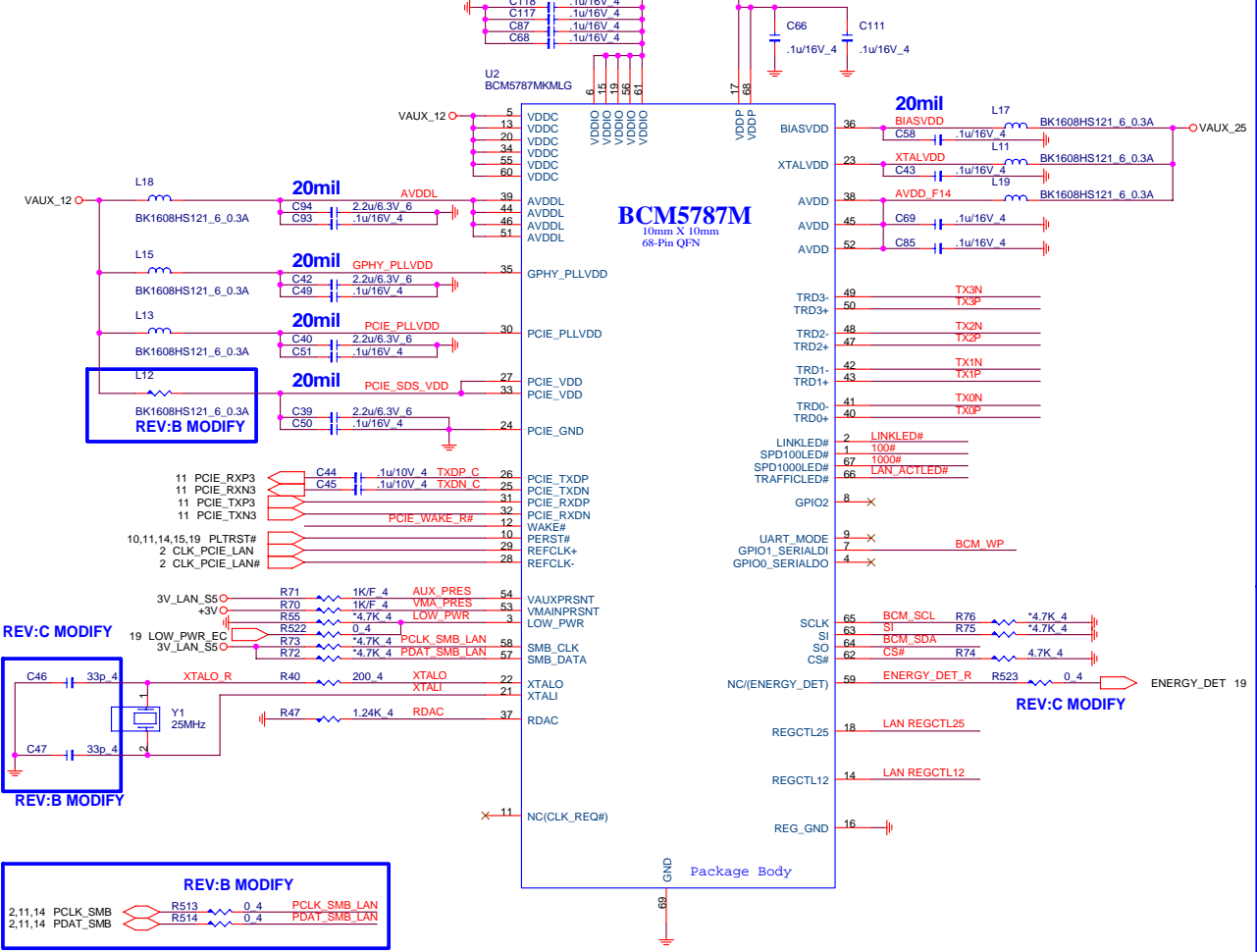


**PROJECT : Z01**  
**Quanta Computer Inc.**

Size: Document Number  
**HDD/ODD/LED/SW/TP/FAN**

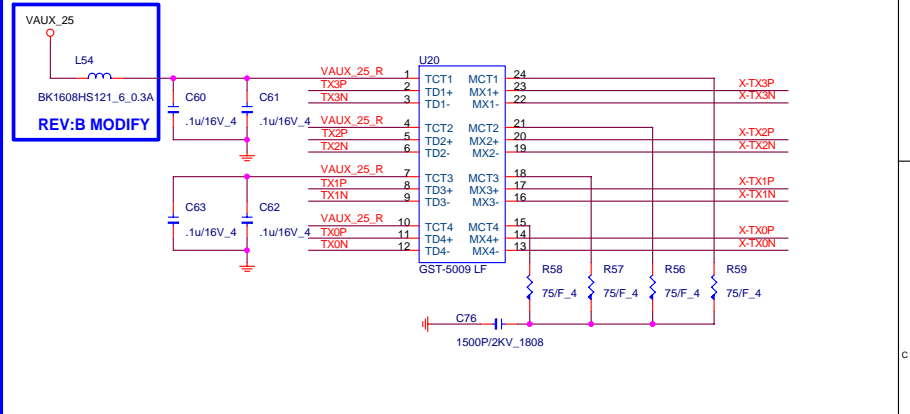
Date: Thursday, May 17, 2007 Sheet 16 of 26 Rev 3B

# Giga LAN BCN5785M

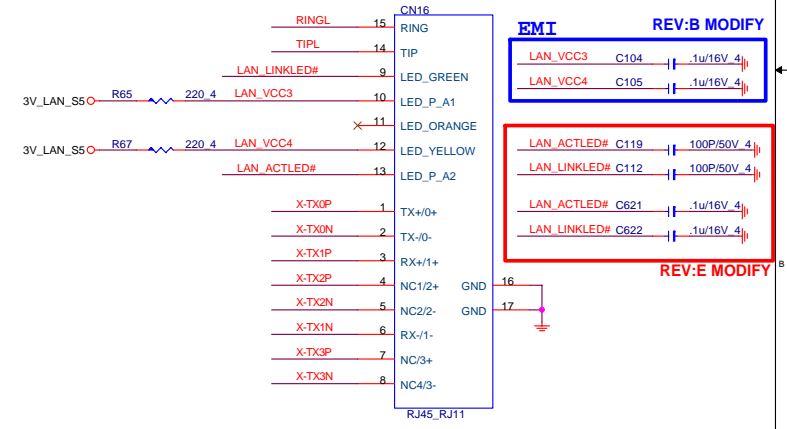


# Transformer

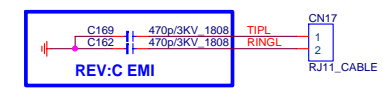
- Source 1: DELTA LFE9249 DBOZR1LAN11
- Source 2: Bothand GST5009 DBKN1NLAN03
- Source 3: FCE NS892402 DBOZH1LAN06



# RJ45 & RJ11 connector



# RJ11 cable



**PROJECT : ZO1**  
**Quanta Computer Inc.**

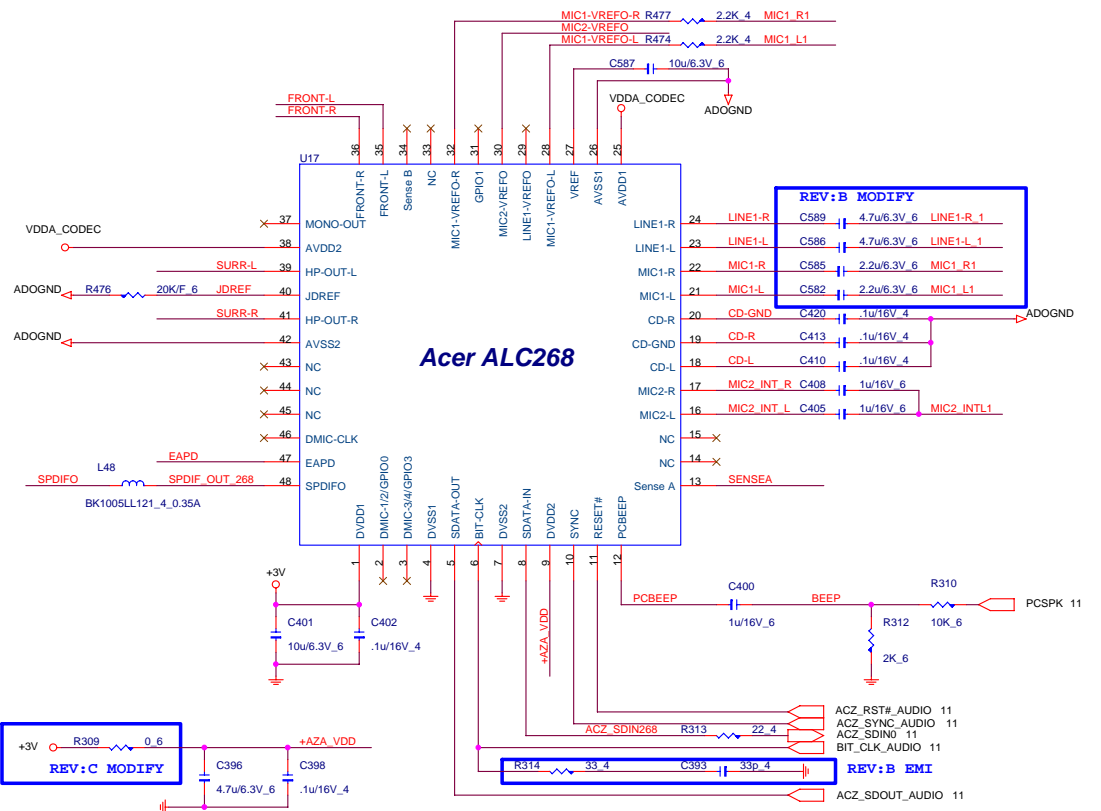
Size: Document Number  
**GigaLAN BCM5787M & RJ45/11** Rev 3A

Date: Thursday, May 17, 2007 Sheet 17 of 26



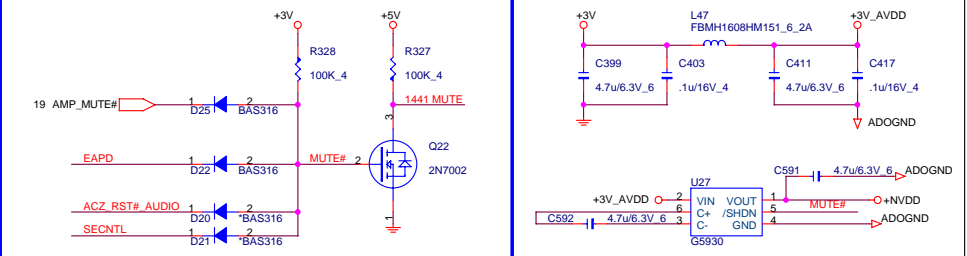
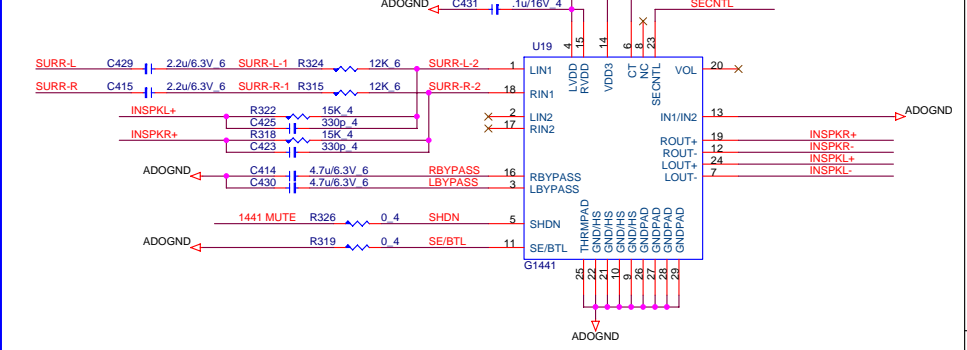


# CODEC(ALC268)

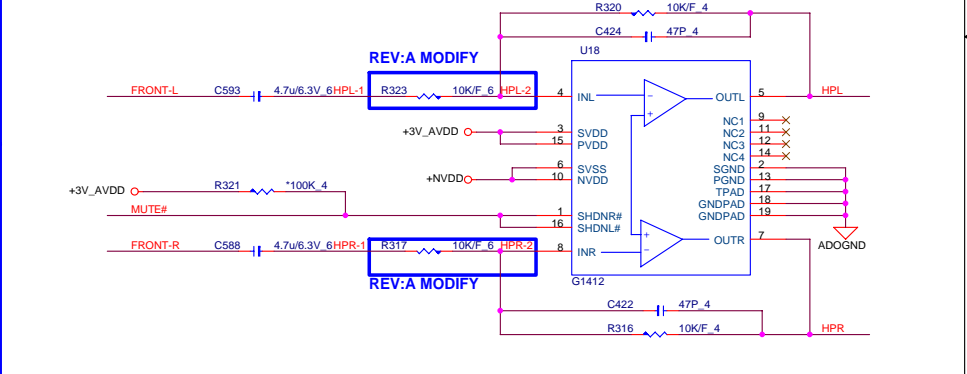


## Acer ALC268

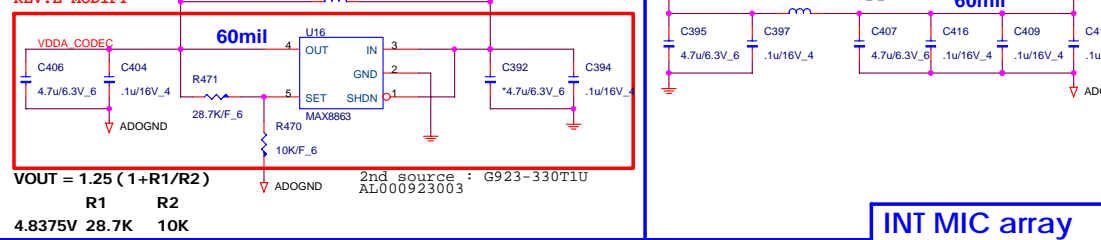
# Speaker Amplifier



# LINE OUT Amplifier



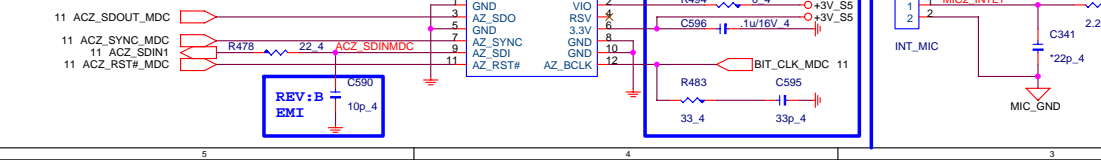
# Codec Power



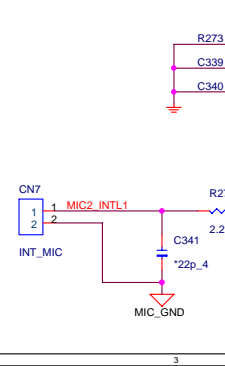
# SPEAKER



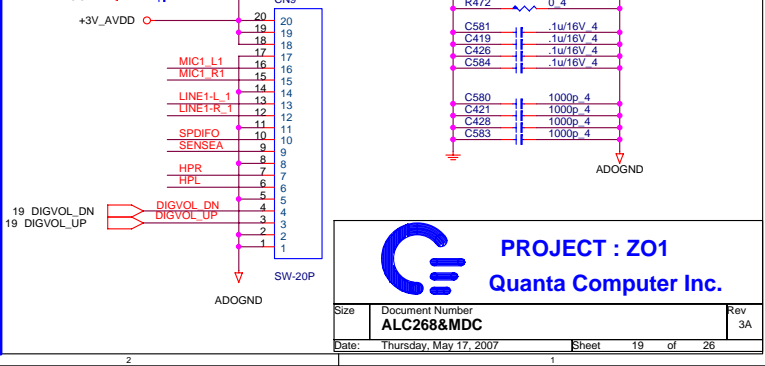
# MDC

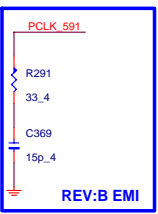
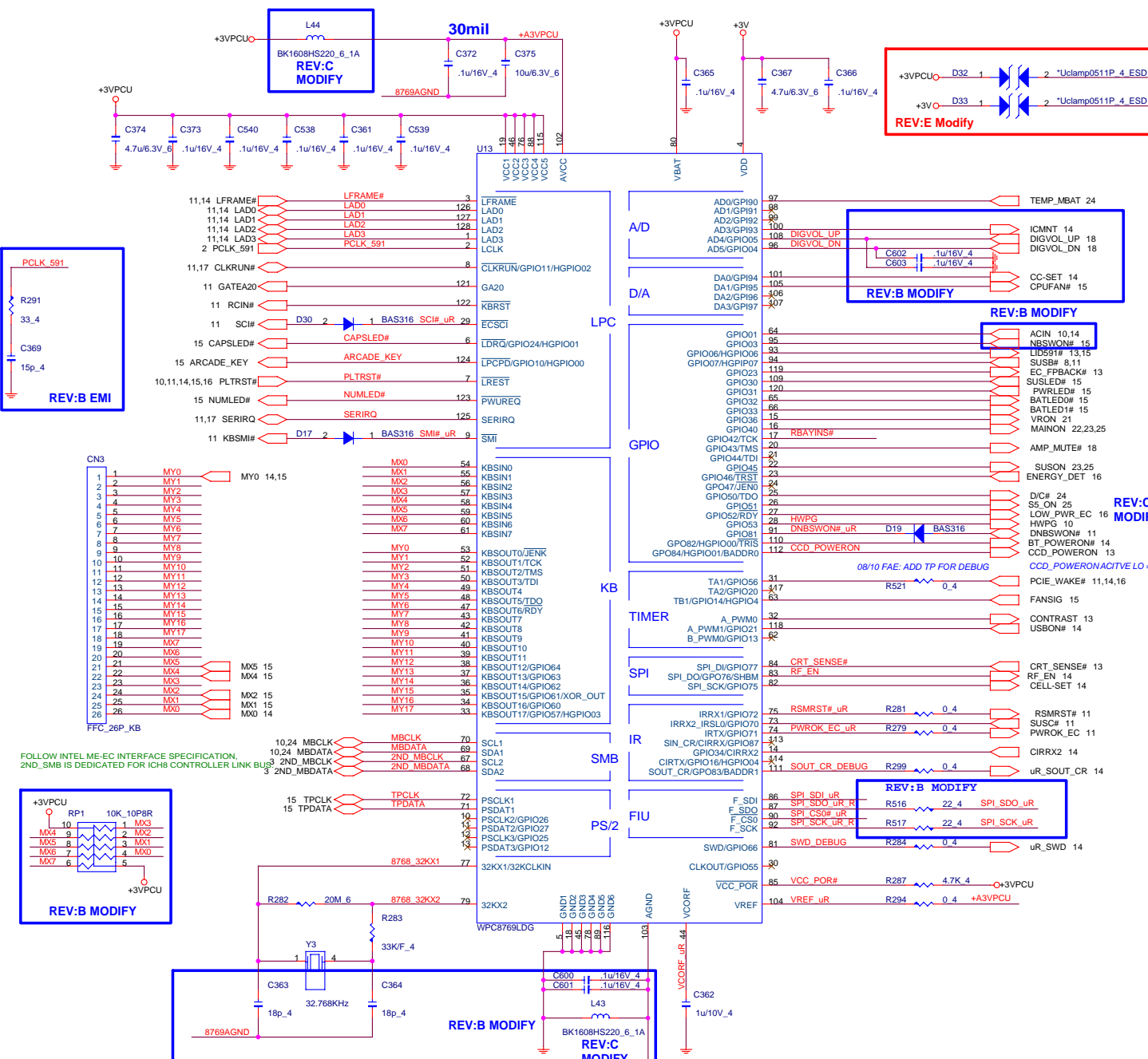


# INT MIC array

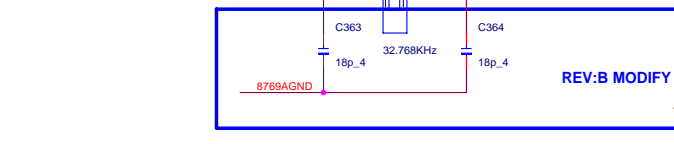
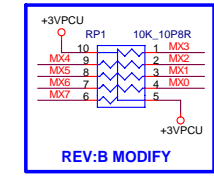


# AUDIO/B

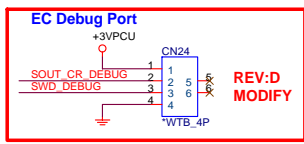




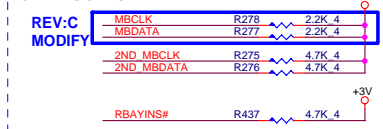
FOLLOW INTEL ME-EC INTERFACE SPECIFICATION.  
2ND\_SMB IS DEDICATED FOR ICH8 CONTROLLER LINK BUS



08/10 FAE:  
L83 CAN CHANGE FROM BEAD TO SHORT.  
BUT, PLEASE PUT AGND & 32K CAP & AVCC CAP AT ONE POINT.  
ZS1 STILL USE BEAD FOR SAFE.



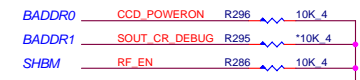
### SM BUS PU



### I/O ADDRESS SETTING

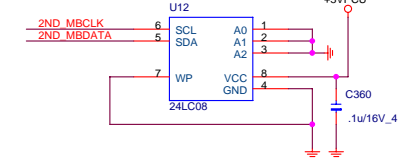
I/O Address	
BADDR1-0	Data
0 0	XOR TREE TEST MODE
0 1	CORE DEFINED
1 0	2Eh 2Fh
1 1	164Eh 164Fh

SHBM=0: Enable shared memory with host BIOS

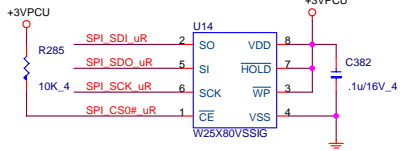


1/13 Confirm by vendor mail :  
Disabled ('1') if using FWH device on LPC.  
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

### ACER ID

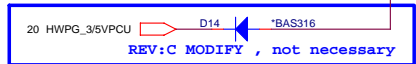
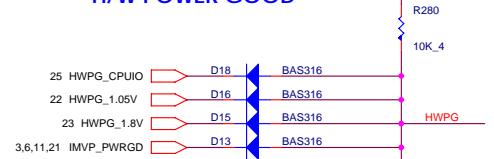


### SPI FLASH

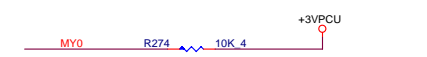


1/13 Confirm by vendor mail :  
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

### H/W POWER GOOD



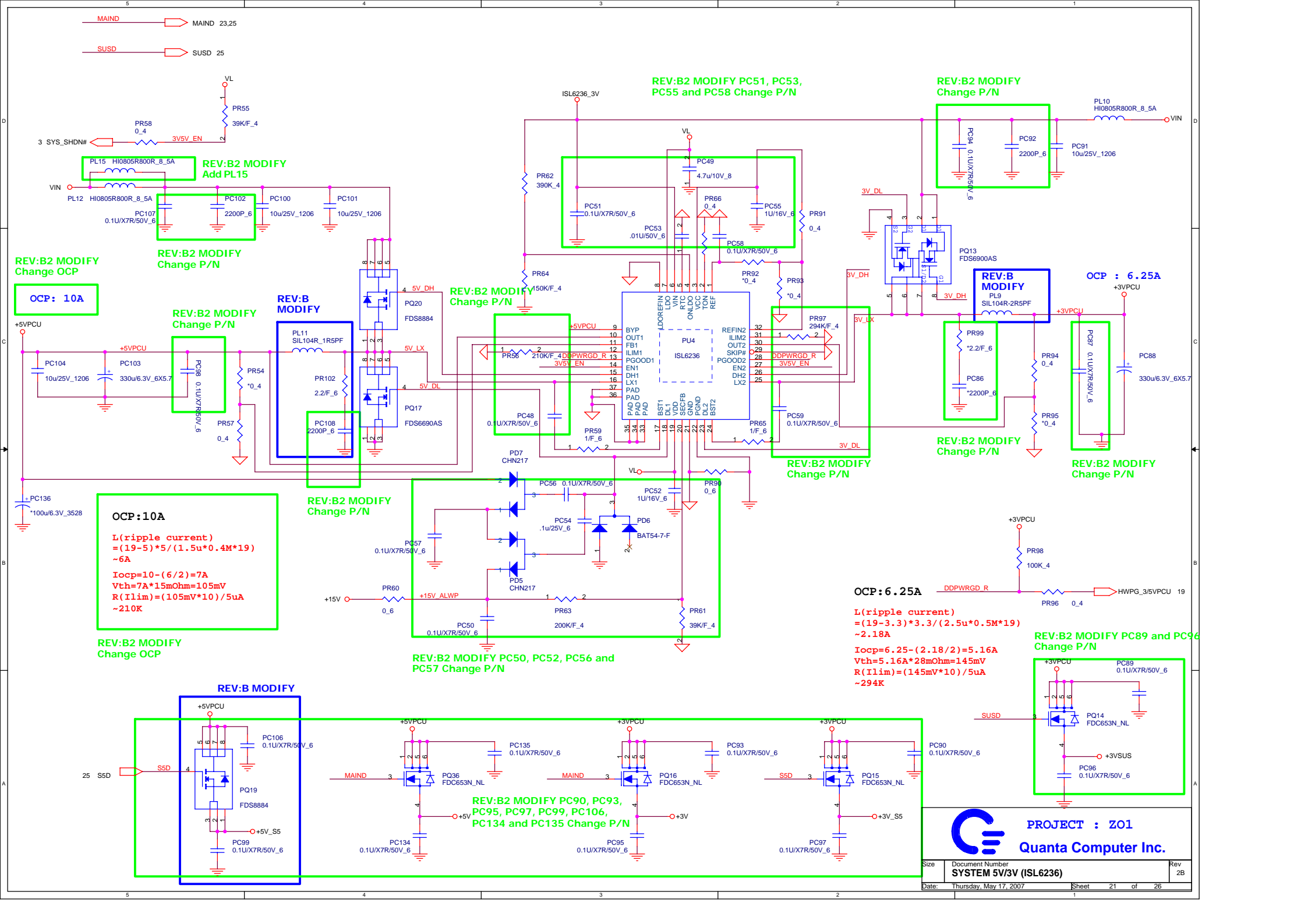
### INTERNAL KEYBOARD STRIP SET



## PROJECT : Z01

### Quanta Computer Inc.

Size	Document Number	Rev
	<b>PC8769L &amp; FLASH</b>	3B
Date:	Thursday, May 17, 2007	Sheet 20 of 26



**REV:B2 MODIFY**  
Change OCP  
**OCP: 10A**

**REV:B2 MODIFY**  
Add PL15

**REV:B2 MODIFY**  
Change P/N

**REV:B2 MODIFY**  
Change P/N

**REV:B MODIFY**

**REV:B2 MODIFY**  
Change P/N

**REV:B2 MODIFY**  
PC51, PC53,  
PC55 and PC58 Change P/N

**REV:B2 MODIFY**  
Change P/N

**OCP:10A**  
 $L(\text{ripple current}) = (19-5) * 5 / (1.5u * 0.4M * 19) \sim 6A$   
 $I_{ocp} = 10 - (6/2) = 7A$   
 $V_{th} = 7A * 15m\Omega = 105mV$   
 $R(I_{lim}) = (105mV * 10) / 5uA \sim 210K$

**REV:B2 MODIFY**  
Change OCP

**REV:B2 MODIFY**  
PC50, PC52, PC56 and  
PC57 Change P/N

**OCP: 6.25A**  
 $L(\text{ripple current}) = (19-3.3) * 3.3 / (2.5u * 0.5M * 19) \sim 2.18A$   
 $I_{ocp} = 6.25 - (2.18/2) = 5.16A$   
 $V_{th} = 5.16A * 28m\Omega = 145mV$   
 $R(I_{lim}) = (145mV * 10) / 5uA \sim 294K$

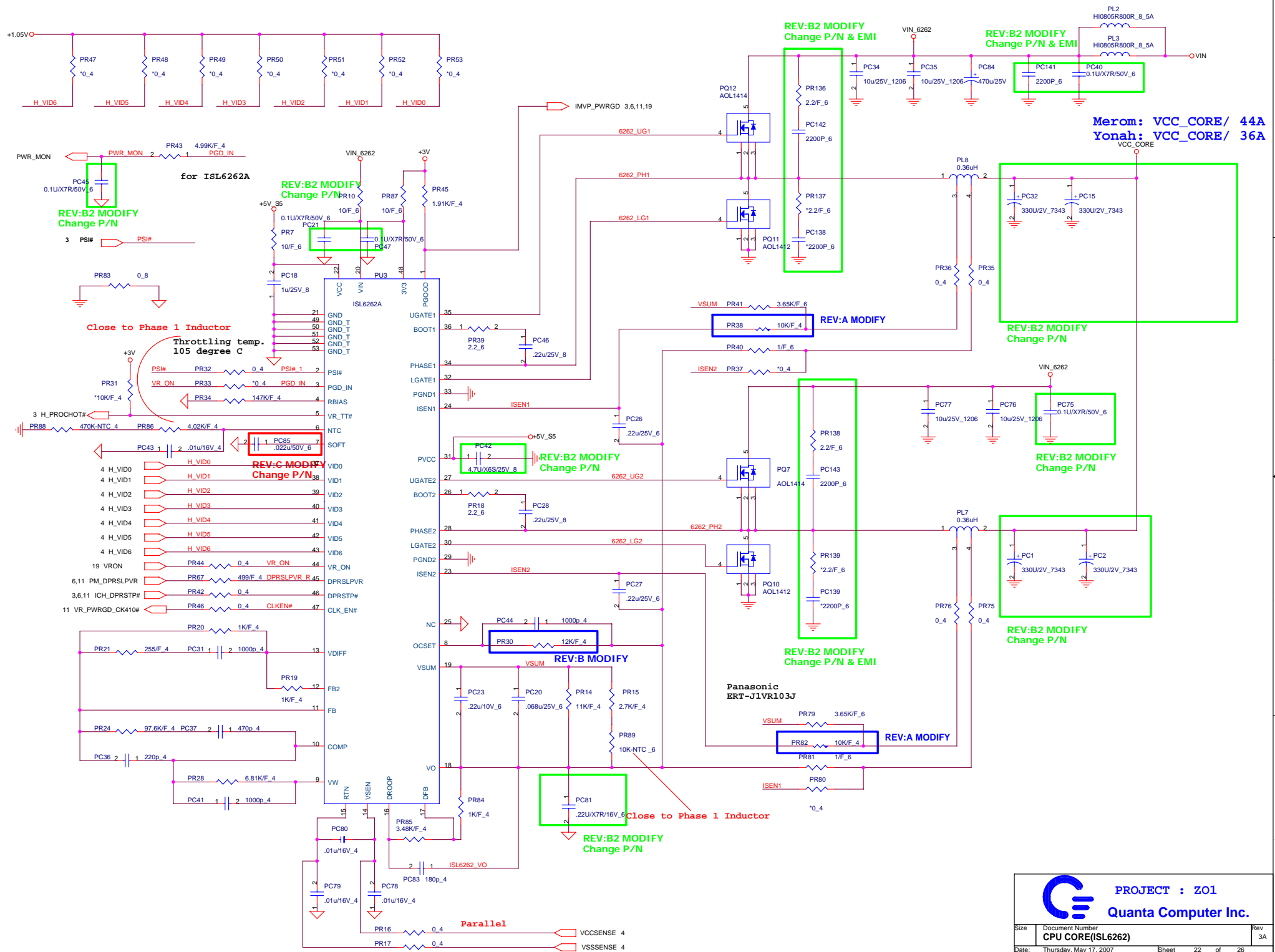
**REV:B2 MODIFY**  
PC89 and PC96  
Change P/N

**REV:B2 MODIFY**  
PC90, PC93,  
PC95, PC97, PC106,  
PC134 and PC135 Change P/N

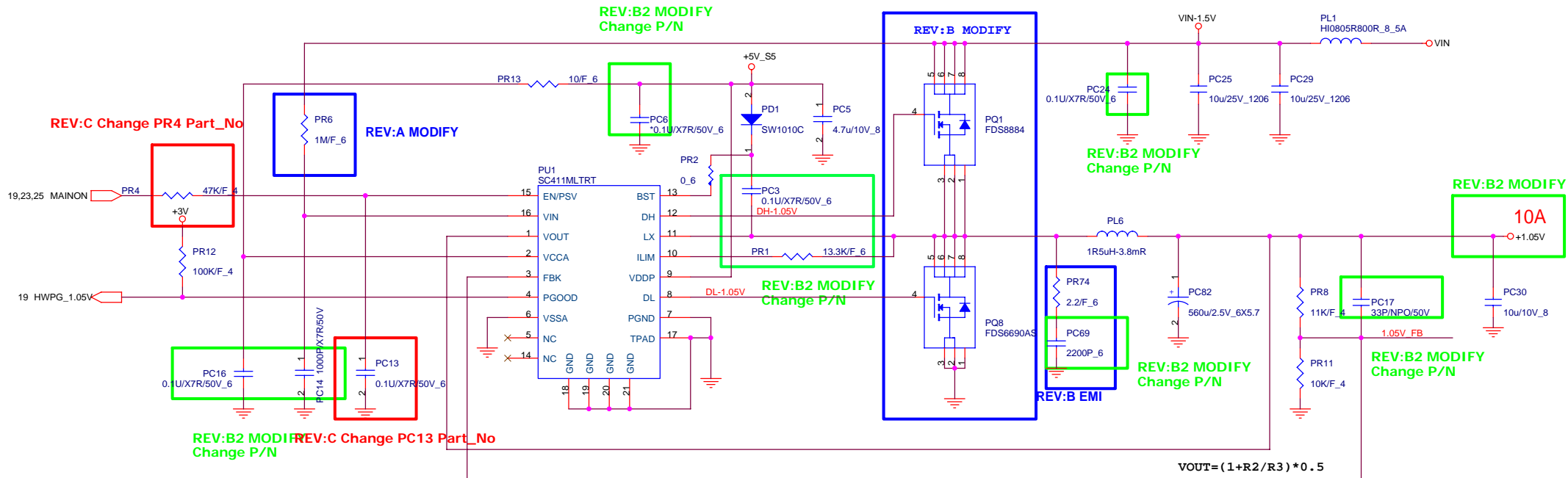


**PROJECT : ZO1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>SYSTEM 5V/3V (ISL6236)</b>	<b>2B</b>
Date:	Thursday, May 17, 2007	Sheet 21 of 26



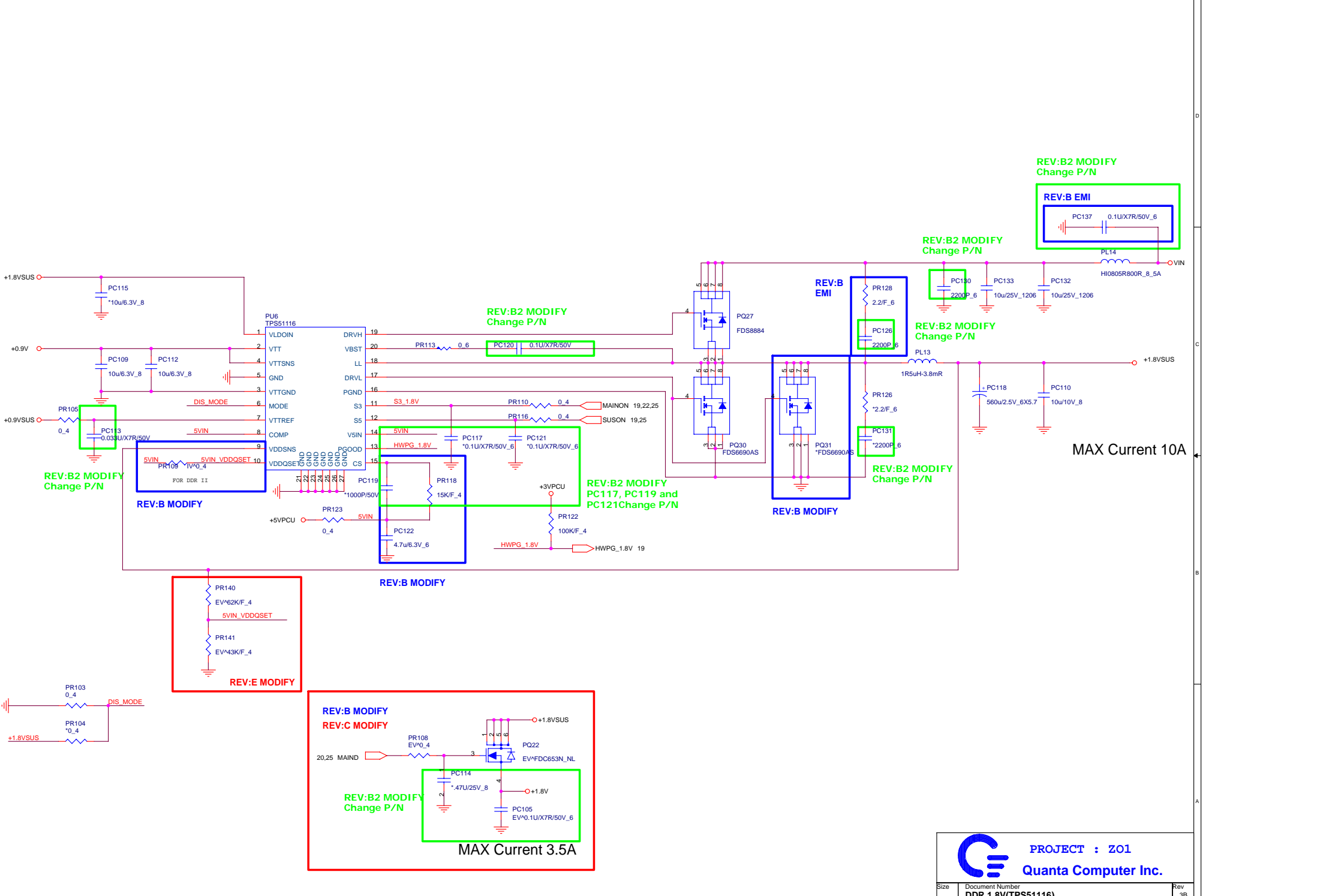
Merom: VCC\_CORE/ 44A  
 Yonah: VCC\_CORE/ 36A



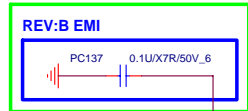
**PROJECT : ZO1**  
**Quanta Computer Inc.**

Size	Document Number <b>VTT 1.05V(SC411)</b>	Rev 3A
Date:	Thursday, May 17, 2007	Sheet 23 of 26





REV:B2 MODIFY  
Change P/N



REV:B2 MODIFY  
Change P/N

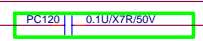
REV:B2 MODIFY  
Change P/N

REV:B2 MODIFY  
Change P/N

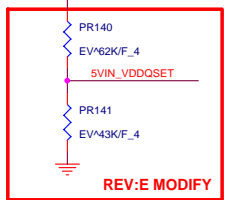
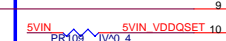
REV:B2 MODIFY  
Change P/N

REV:B2 MODIFY  
PC117, PC119 and  
PC121 Change P/N

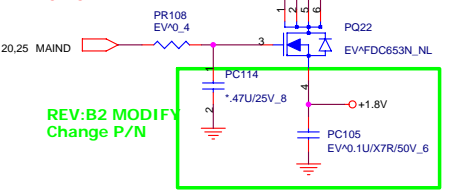
REV:B2 MODIFY  
Change P/N



REV:B MODIFY

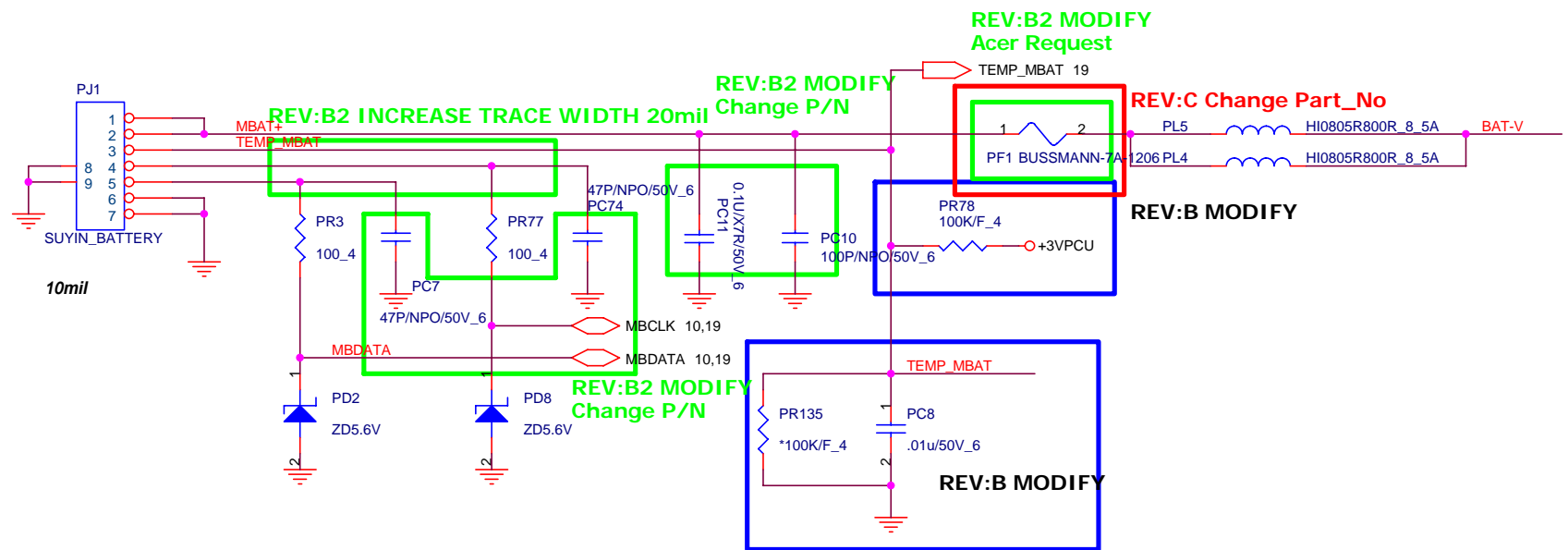
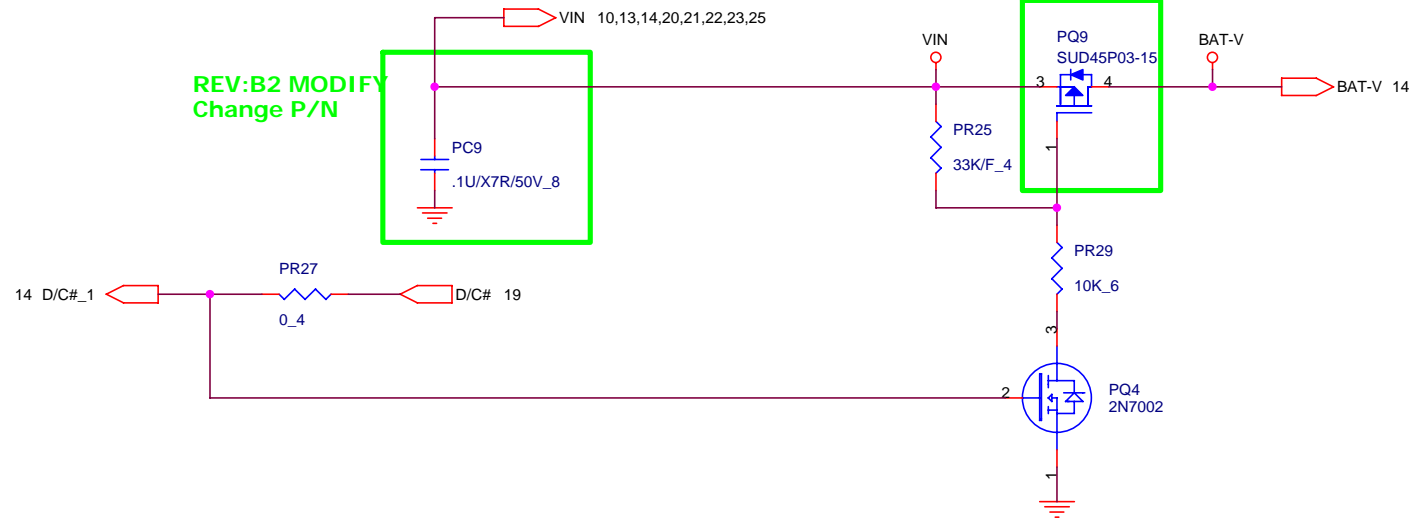


REV:B MODIFY  
REV:C MODIFY



MAX Current 3.5A

MAX Current 10A



**PROJECT : ZO1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>CHARGER (ISL6251A)</b>	3A
Date:	Thursday, May 17, 2007	Sheet 25 of 26

