

BAD40_HC

DIS/UMA Schematics Document

Sandy&Ivy Bridge


Intel PCH

DY :None Installed
DIS:DIS installed
DIS_Muxless :BOTH DIS or Muxless installed
DIS_PX:BOTH DIS or PX installed
DIS_PX_Muxless:DIS or PX or Muxless installed.
Muxless: Muxless installed.(PX4.0)
PX:MUX installed.(PX3.0)
PX_Muxless:BOTH PX or Muxless installed.
UMA:UMA installed
UMA_Muxless:BOTH UMA or Muxless installed
UMA_PX_Muxless:UMA or PX or Muxless installed

ANNIE: ONLY FOR ANNIE solution.
PSL: KBC795 PSL circuit for 10mW solution installed.
10mW: External circuit for 10mW solution installed.
65W: for 65W adaptor installed.
90W: for 90W adaptor installed.

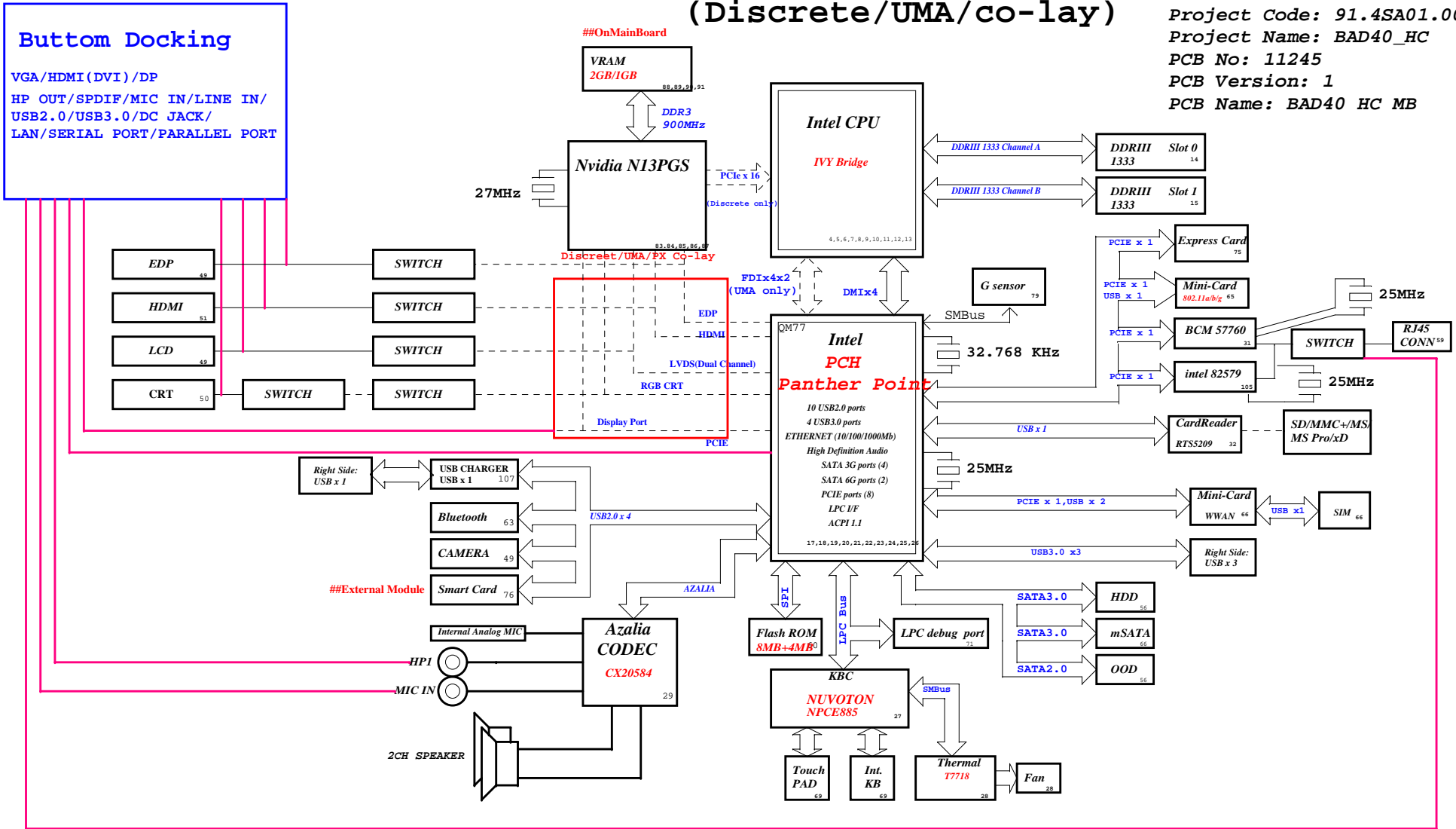
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<Variant Name>

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Title			
Cover Page			
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BAD40 HC Block Diagram (Discrete/UMA/co-lay)

Project Code: 91.4SA01.001
 Project Name: BAD40_HC
 PCB No: 11245
 PCB Version: 1
 PCB Name: BAD40 HC MB



SYSTEM DC/DC TPS5146 48	
INPUTS	OUTPUTS
SV_S5	OD85V_S0
CPU DC/DC VT1317SFCX 42-43	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
SYSTEM DC/DC RT8237AGQW 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT
SYSTEM DC/DC RT8239CGQW 41	
INPUTS	OUTPUTS
DCBATOUT	SV_AUX_S5 3D3V_AUX_S5 SV_S5 3D3V_S5
SYSTEM DC/DC RT8207LGQW 46	
INPUTS	OUTPUTS
DCBATOUT	1DSV_S3 OD75V_S0 DPS_VREF_S3
SYSTEM DC/DC VT1317SFCX 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE_PWR
VGA RT8208AGQW 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE
TI CHARGER BQ24745RHRD 40	
INPUTS	OUTPUTS
DCBATOUT	BT+
SYSTEM DC/DC RT8015AGQW 47	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0
SYSTEM DC/DC	
INPUTS	OUTPUTS
Switches	
INPUTS	OUTPUTS
1DSV_S3	1DSV_VGA_S0
3D3V_S0	3D3V_VGA_S0
PCB LAYER	
L1:Top	L5:Power
L2:GND	L6:Signal
L3:Signal	L7:GND
L4:Signal	L8:Bottom

HR PX

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Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	Enable Danbury: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable Danbury: Leave floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] Disable Danbury: Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

USB Table

Pair	Device
0	USB. port 1
1	USB. port 2
2	USB. port 3
3	Dock
4	X
5	Fingerprint
6	X
7	X
8	Mini Card2 (WWAN) &BT
9	X
10	3G SIM
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

SATA Table

SATA	
Pair	Device
0	HDD1
1	msATA
2	N/A
3	N/A
4	ODD
5	N/A

PCIE Routing

LANE1	N/A
LANE2	Mini Card2(WWAN)
LANE3	Card Reader
LANE4	Mini Card1(WLAN)
LANE5	N/A
LANE6	Intel /BCM LAN
LANE7	New Card
LANE8	N/A

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		Disabled - No Physical Display Port attached to 1: Embedded DisplayPort. Enabled - An external Display Port device is connect to the EMBEDDED display Port 0:	0
CFG[6:5]	PCI-Express Port Bifurcation Straps	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	PEG DEFER TRAINING	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training	

POWER PLANE	VOLTAGE	Voltage Rails		DESCRIPTION
		ACTIVE IN		
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_OPCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0		CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3		
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states		AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN		Legacy WOL
3D3V_AUX_KBC	3.3V	DSW_Sx		ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx		Powered by Li Coin Cell in G3 and +V3ALW in Sx

SMBus ADDRESSES

I ² C / SMBus Addresses		Ref	Des	HURON RIVER ORB		
Device	Address			Hex	Bus	
EC SMBus 1 Battery CHARGER				BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA		
EC SMBus 2 PCH eDP				SMML_CLK/SMML_DATA SMML_CLK/SMML_DATA SMML_CLK/SMML_DATA		
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital PoE G-Sensor MINE				PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK		

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Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

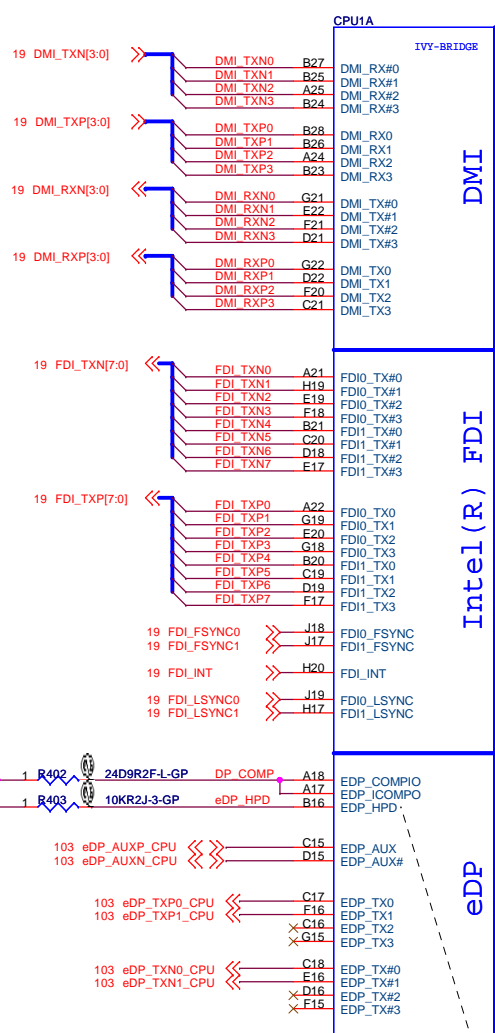
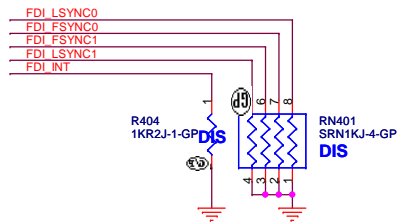
Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Lane reversal does not apply to FDI sideband signals.

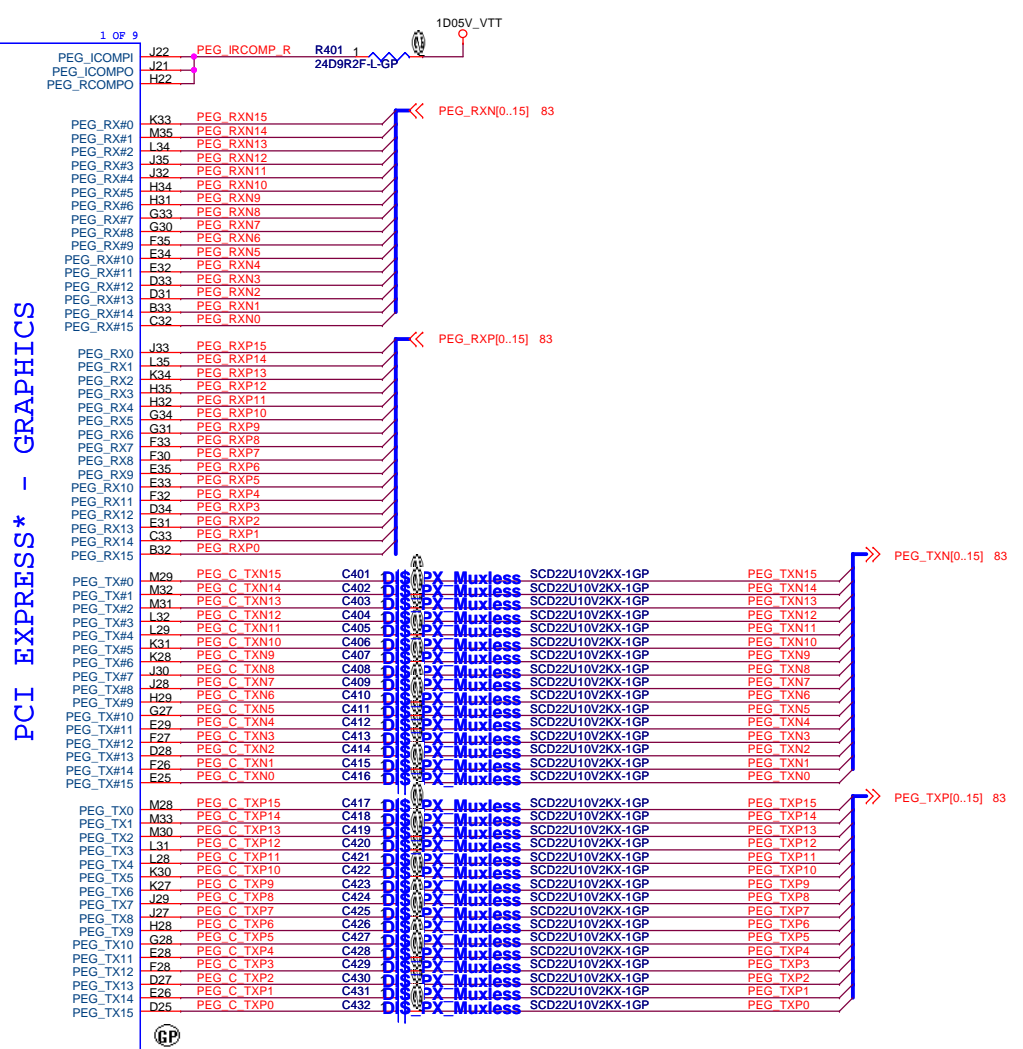
Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE:
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

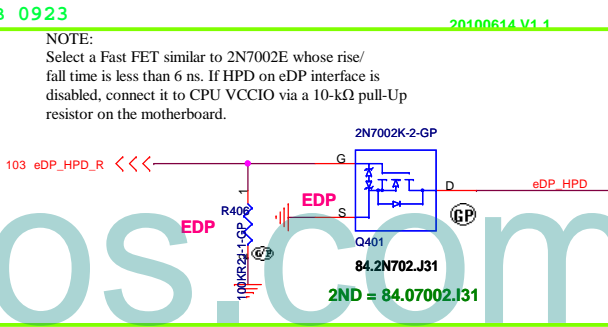
Stuff to disable internal graphics function for power saving.



Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCIMPO keep W/S=4/15 mils and routing length less than 500 mils.



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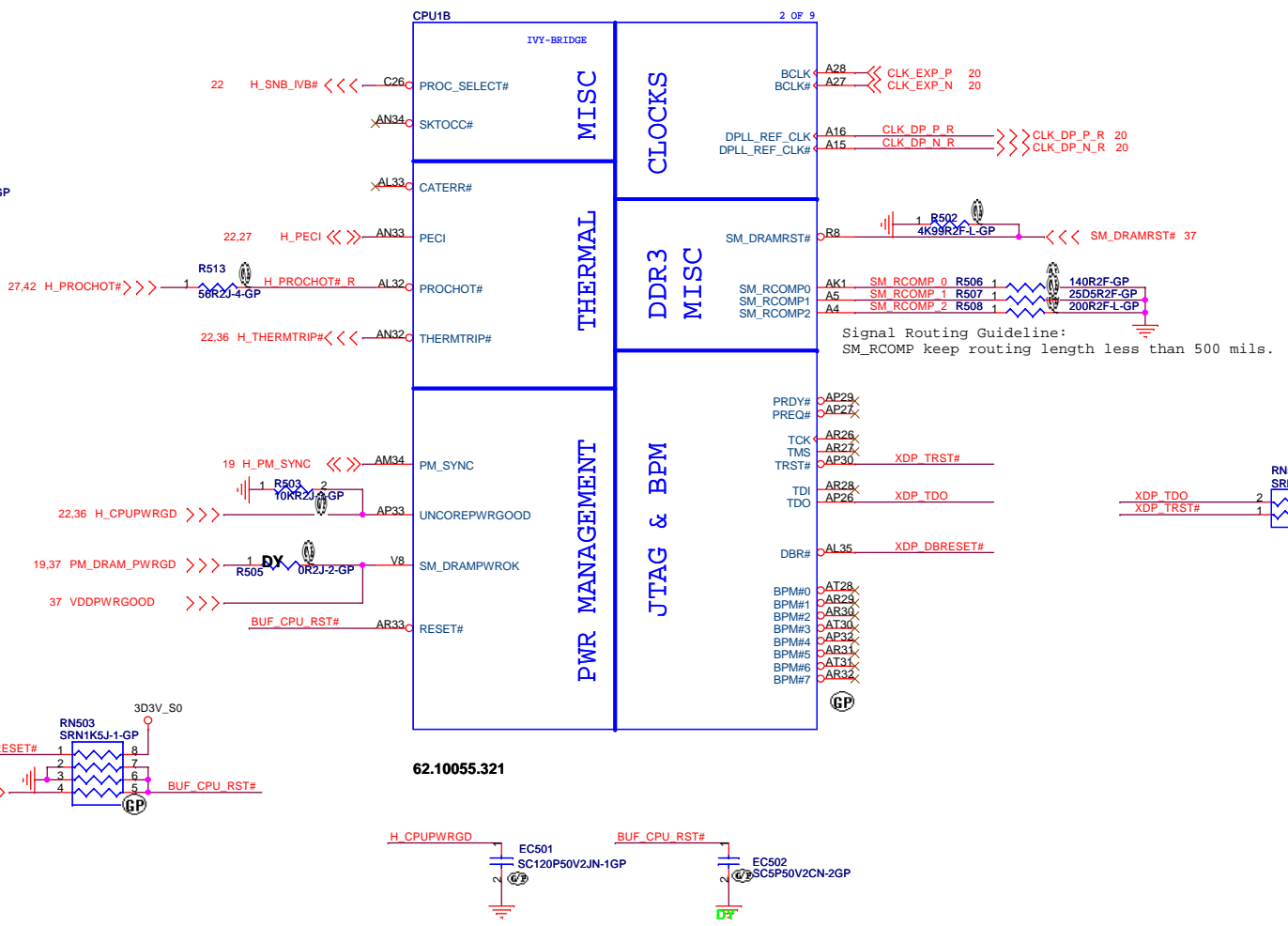
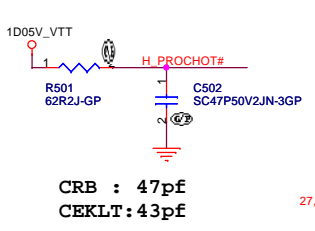
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Title: CPU (PCIe/DMI/FDI)

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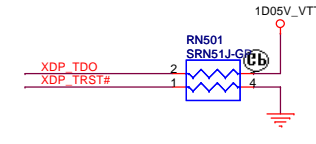
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SSID = CPU



Disabling Guidelines:
If motherboard only supports external graphics:
Connect DPLL_REF_SSCLK on Processor to GND through 1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K +/- 5% resistorpower (~15 mW) may be wasted.

DIS

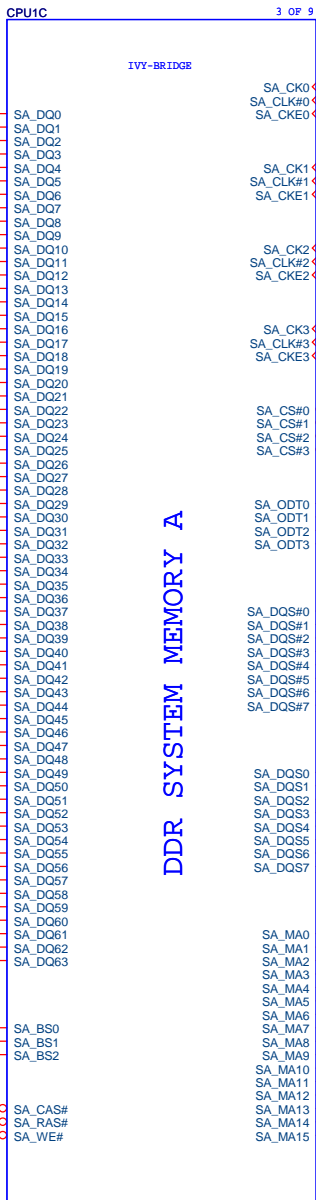


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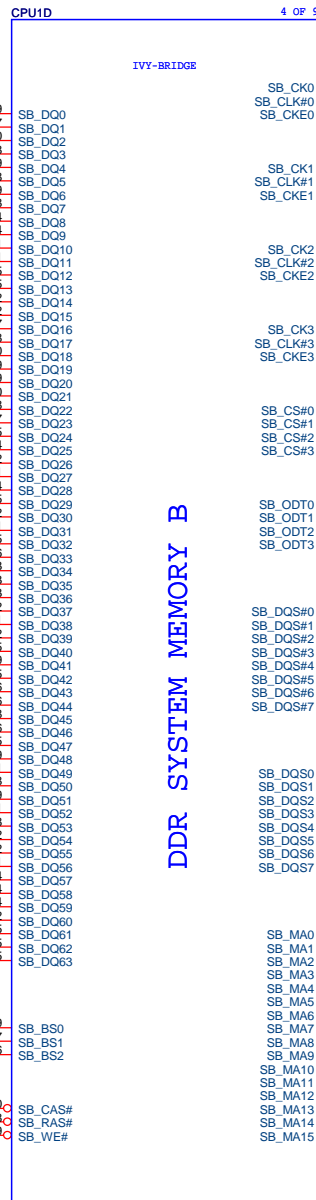
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Title CPU (THERMAL/CLOCK/PM)

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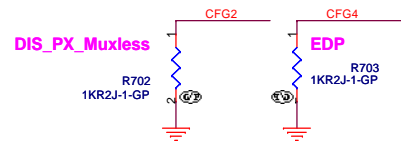


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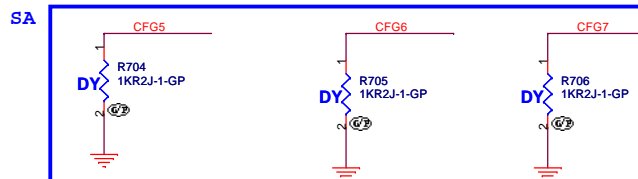
Title	CPU (DDR)	
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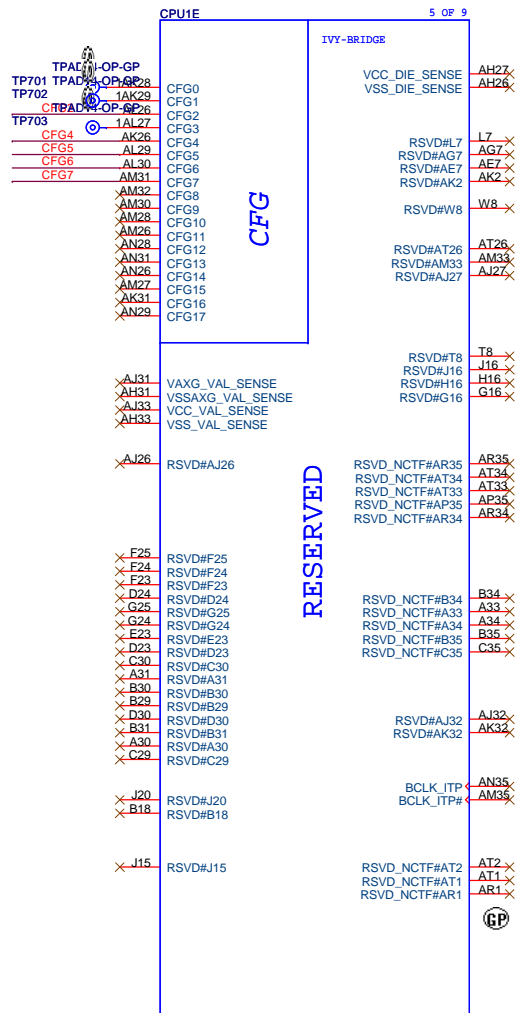


PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed

PCIe Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



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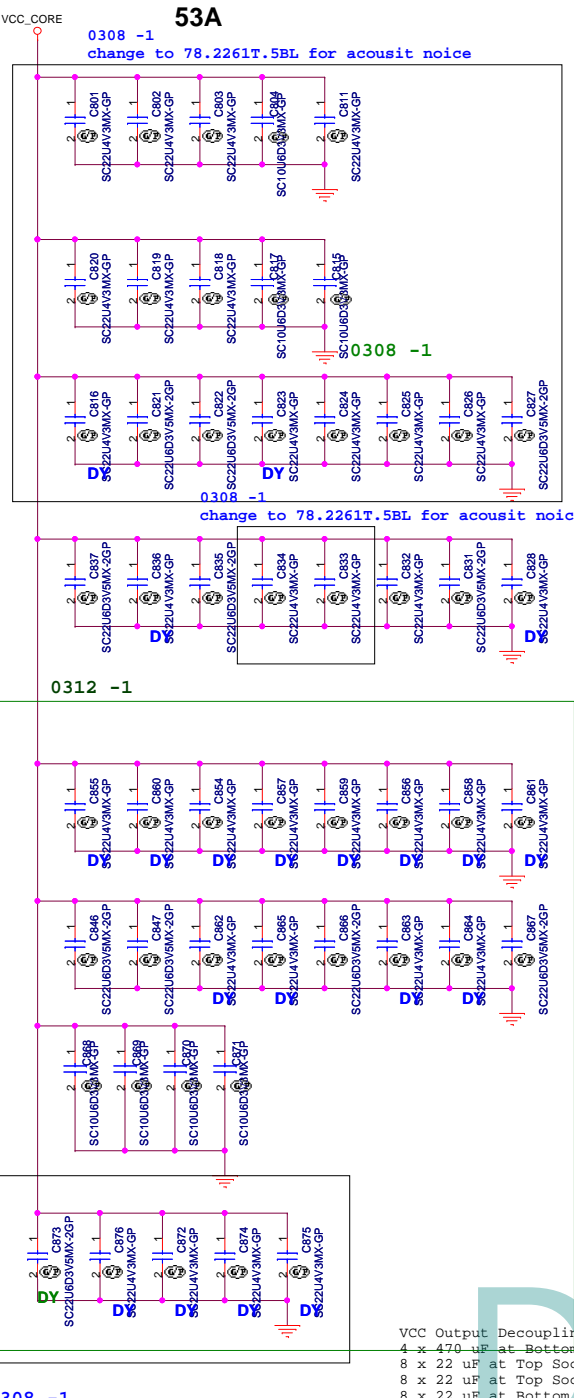
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Title CPU (RESERVED)	
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SSID = CPU

POWER

PROCESSOR CORE POWER



VCC Output Decoupling Recommendation:
 4 x 470 uF at Bottom Socket Edge
 8 x 22 uF at Top Socket Cavity
 8 x 22 uF at Top Socket Edge
 8 x 22 uF at Bottom Socket Cavity

- CPU1F 6 OF 9
- AG35 VCC1
 - AG34 VCC2
 - AG33 VCC3
 - AG32 VCC4
 - AG31 VCC5
 - AG29 VCC6
 - AG28 VCC7
 - AG27 VCC8
 - AG26 VCC9
 - AG25 VCC10
 - AF34 VCC11
 - AF33 VCC12
 - AF32 VCC13
 - AF31 VCC14
 - AF30 VCC15
 - AF29 VCC16
 - AF28 VCC17
 - AF27 VCC18
 - AD35 VCC19
 - AD34 VCC20
 - AD33 VCC21
 - AD32 VCC22
 - AD31 VCC23
 - AD30 VCC24
 - AD29 VCC25
 - AD28 VCC26
 - AD27 VCC27
 - AD26 VCC28
 - AD25 VCC29
 - AD24 VCC30
 - AC35 VCC31
 - AC34 VCC32
 - AC33 VCC33
 - AC32 VCC34
 - AC31 VCC35
 - AC29 VCC36
 - AC28 VCC37
 - AC27 VCC38
 - AC26 VCC39
 - AC25 VCC40
 - AA35 VCC41
 - AA34 VCC42
 - AA33 VCC43
 - AA32 VCC44
 - AA31 VCC45
 - AA30 VCC46
 - AA29 VCC47
 - AA28 VCC48
 - AA27 VCC49
 - AA26 VCC50
 - Y35 VCC51
 - Y34 VCC52
 - Y33 VCC53
 - Y32 VCC54
 - Y31 VCC55
 - Y30 VCC56
 - Y28 VCC57
 - Y27 VCC58
 - Y26 VCC59
 - Y25 VCC60
 - Y24 VCC61
 - Y23 VCC62
 - Y22 VCC63
 - Y21 VCC64
 - Y20 VCC65
 - V30 VCC66
 - V29 VCC67
 - V28 VCC68
 - V27 VCC69
 - V26 VCC70
 - V25 VCC71
 - V24 VCC72
 - V23 VCC73
 - V22 VCC74
 - V21 VCC75
 - V20 VCC76
 - V19 VCC77
 - V18 VCC78
 - V17 VCC79
 - V16 VCC80
 - V15 VCC81
 - V14 VCC82
 - R34 VCC83
 - R33 VCC84
 - R32 VCC85
 - R31 VCC86
 - R30 VCC87
 - R29 VCC88
 - R28 VCC89
 - R27 VCC90
 - R26 VCC91
 - P35 VCC92
 - P34 VCC93
 - P33 VCC94
 - P32 VCC95
 - P31 VCC96
 - P30 VCC97
 - P29 VCC98
 - P28 VCC99
 - P27 VCC100
 - P26 VCC100

CORE SUPPLY

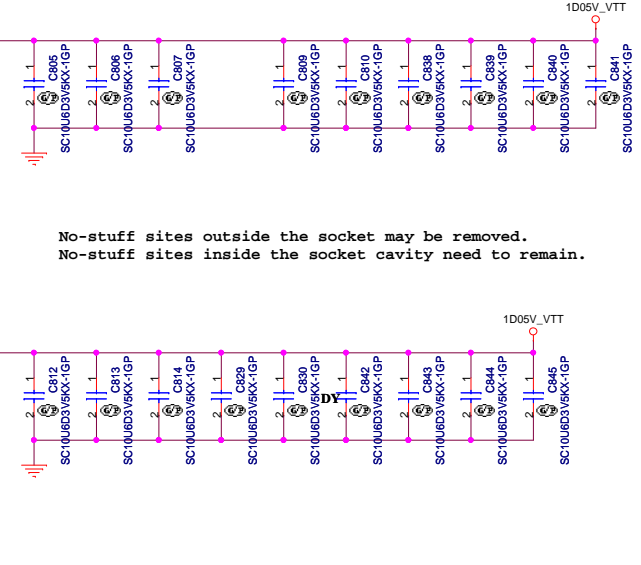
PEG AND DDR

SVID

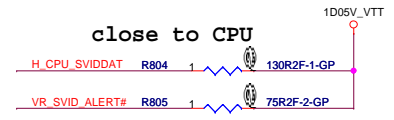
SENSE LINES



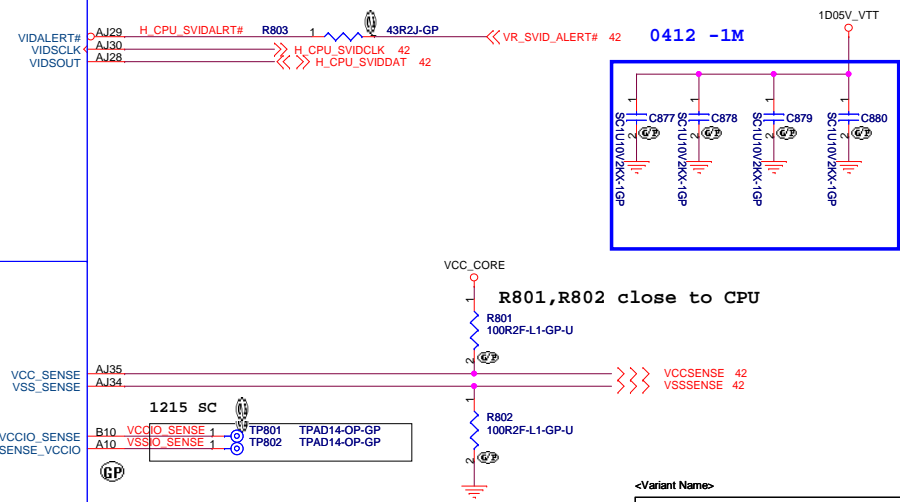
VCCIO Output Decoupling Recommendation:
 2 x 330 uF (3 x 330 uF for 2012 capable designs)
 5 x 22 uF & 5 x 0805 no-stuff at Bottom
 7 x 22 uF & 2 x 0805 no-stuff at Top



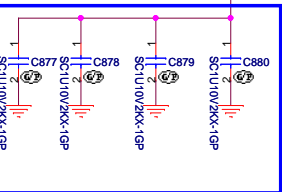
No-stuff sites outside the socket may be removed.
 No-stuff sites inside the socket cavity need to remain.



close to CPU



R801, R802 close to CPU



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CPU (VCC CORE)

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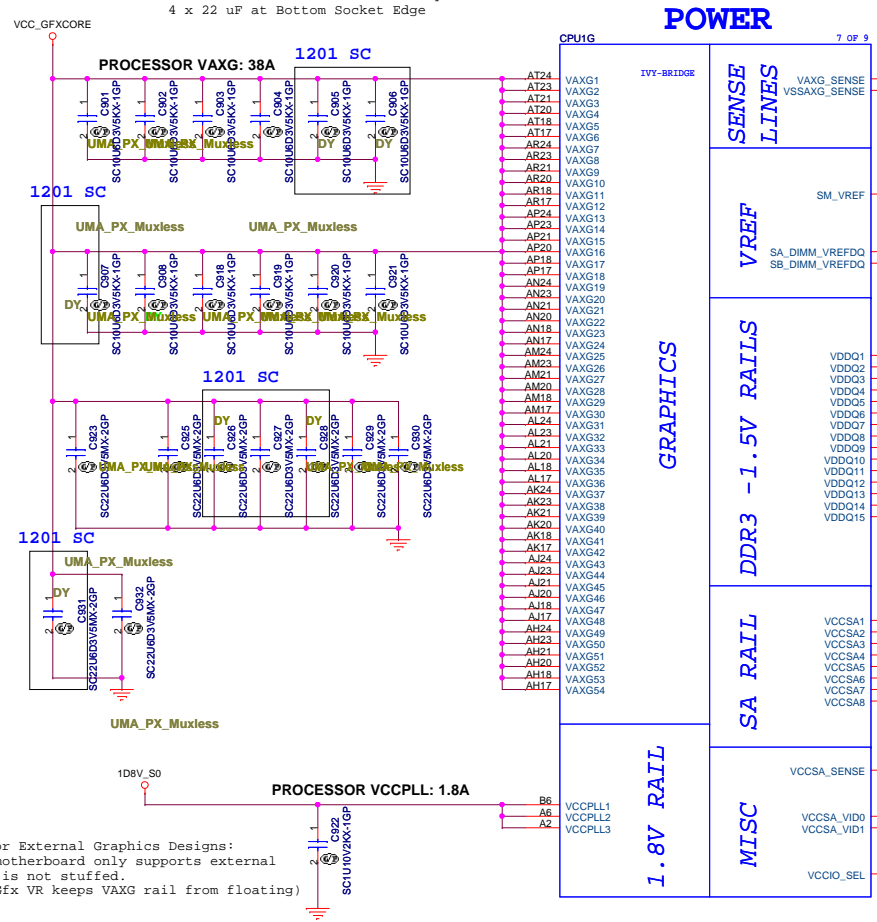
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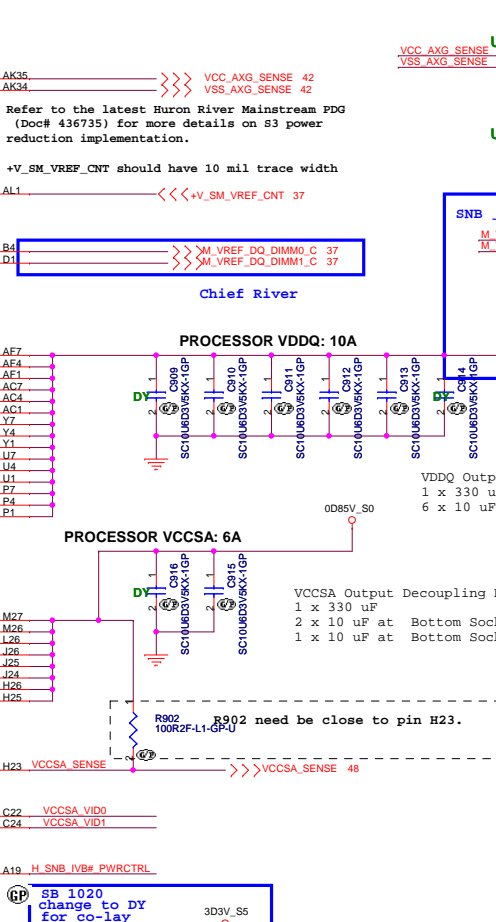
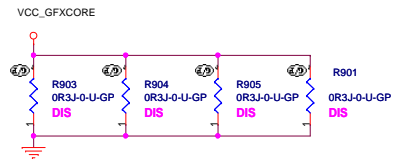
VAXG Output Decoupling Recommendation:
 2 x 470 uF at Bottom Socket Edge
 2 x 22 uF at Top Socket Cavity
 4 x 22 uF at Top Socket Edge
 2 x 22 uF at Bottom Socket Cavity
 4 x 22 uF at Bottom Socket Edge

R906, R907 close to CPU



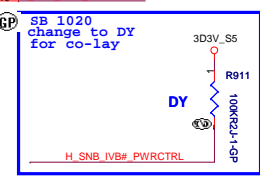
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VCCPLL Output Decoupling Recommendation:
 1 x 330 uF
 2 x 1 uF
 1 x 10 uF

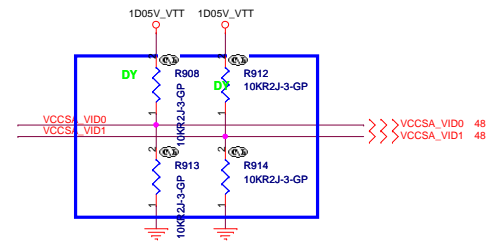
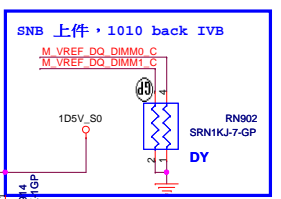
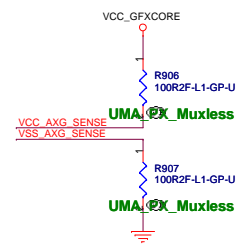


VDDQ Output Decoupling Recommendation:
 1 x 330 uF
 6 x 10 uF

VCCSA Output Decoupling Recommendation:
 1 x 330 uF
 2 x 10 uF at Bottom Socket Cavity
 1 x 10 uF at Bottom Socket Edge



	PIN A19
1.05V	H
1V	L

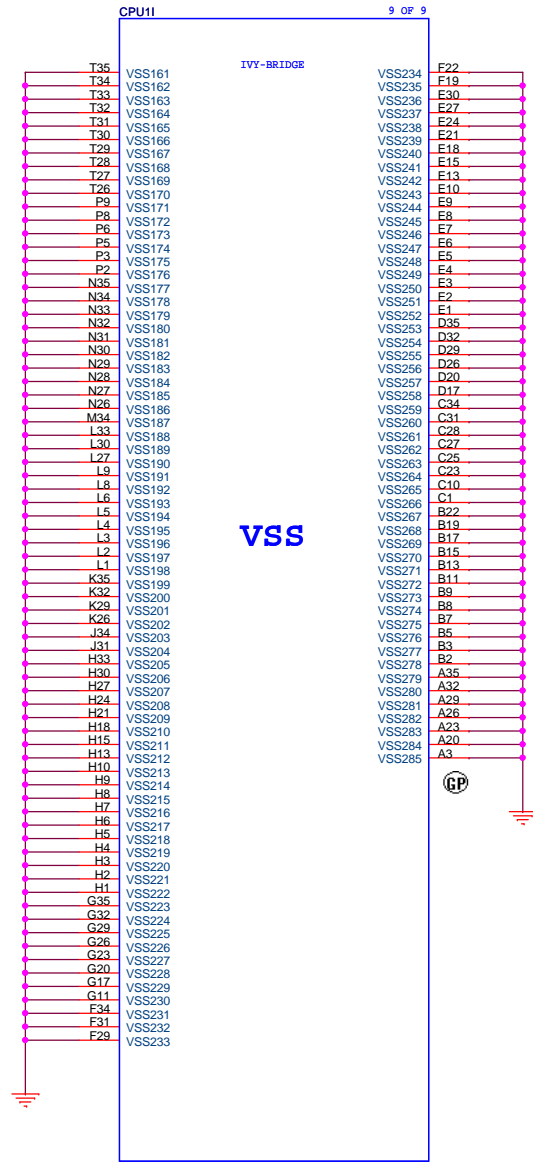
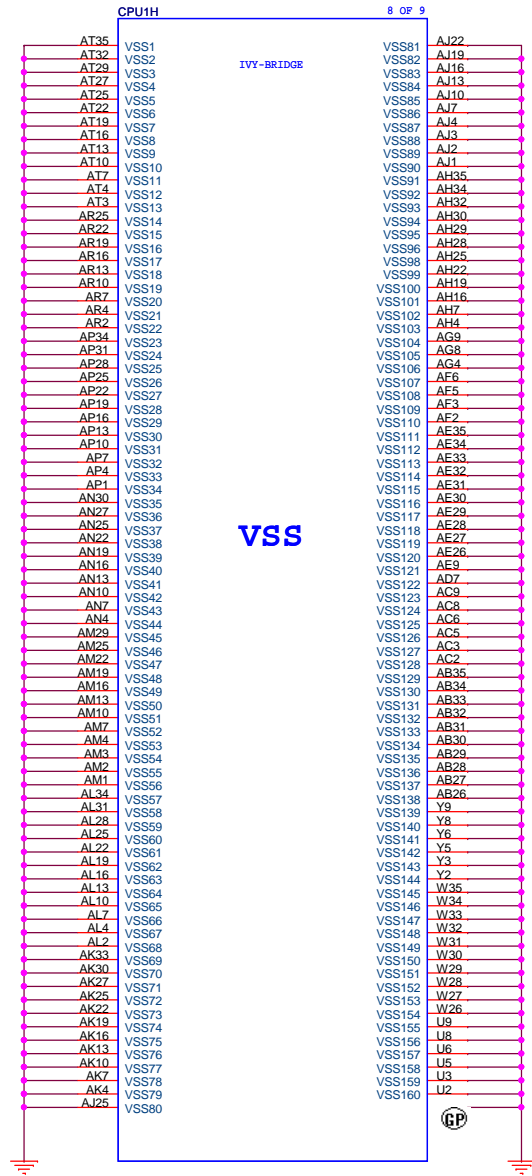


VID[1]	VID[0]	VCCSA
0	0	0.9 V
1	0	0.8 V
0	1	0.725 V
1	1	0.675 V

Disabling Guidelines for External Graphics Designs:
 Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed.
 Can be left floating (Gfx VR keeps VAXG rail from floating) if the VR is stuffed



SSID = CPU



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Title: **CPU (VSS)**

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reserve

JE40 delete XDP function

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Title

XDP

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A4

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Title **Reserved**

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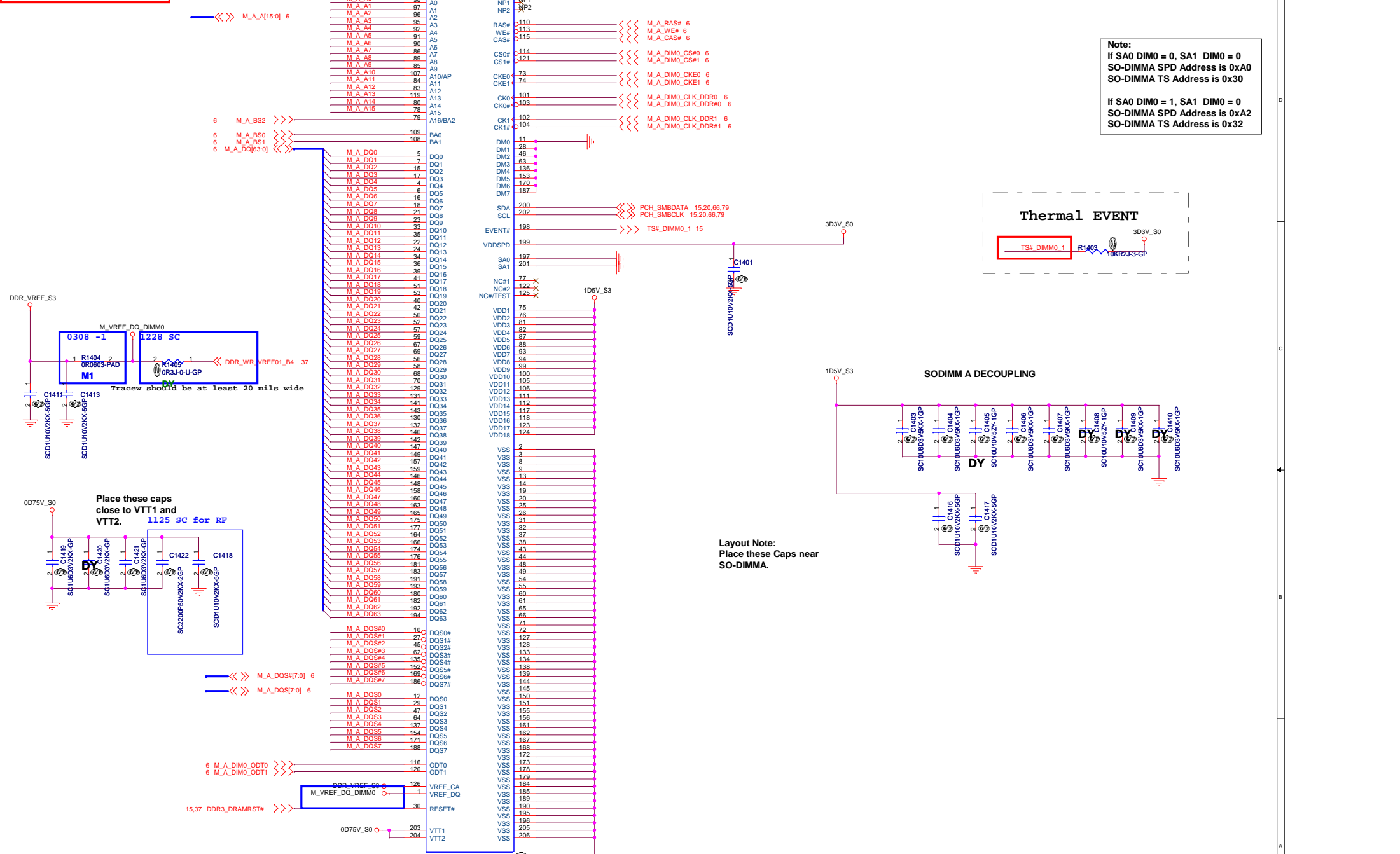
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<Variant Name>

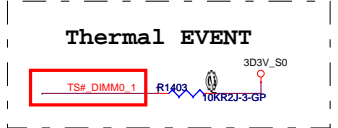
緯創資通			Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.					
Title					
Reserved					
Size	Document Number				Rev
A4	BAD40 HC				1
Date:	Thursday, April 12, 2012			Sheet 13 of	108

SSID = MEMORY

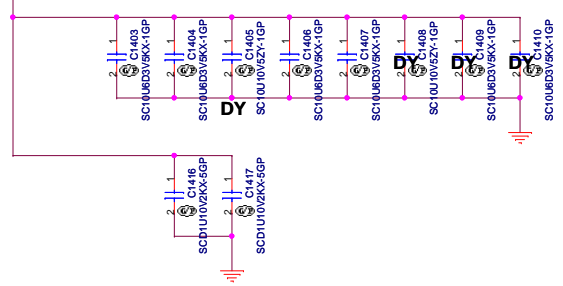


Note:
 If SA0_DIM0 = 0, SA1_DIM0 = 0
 SO-DIMMA SPD Address is 0xA0
 SO-DIMMA TS Address is 0x30

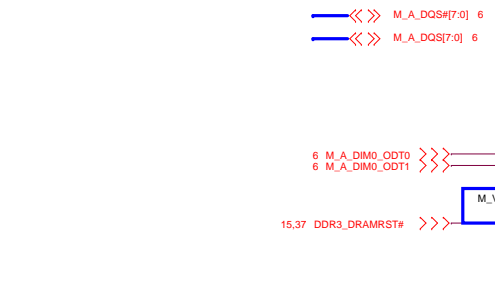
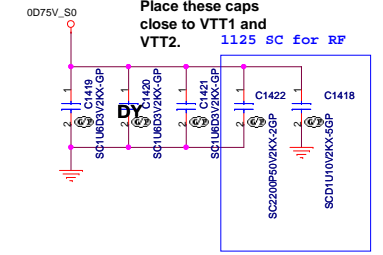
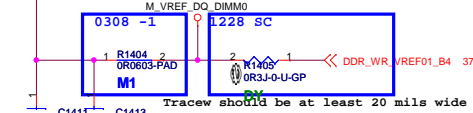
If SA0_DIM0 = 1, SA1_DIM0 = 0
 SO-DIMMA SPD Address is 0xA2
 SO-DIMMA TS Address is 0x32



SODIMM A DECOUPLING



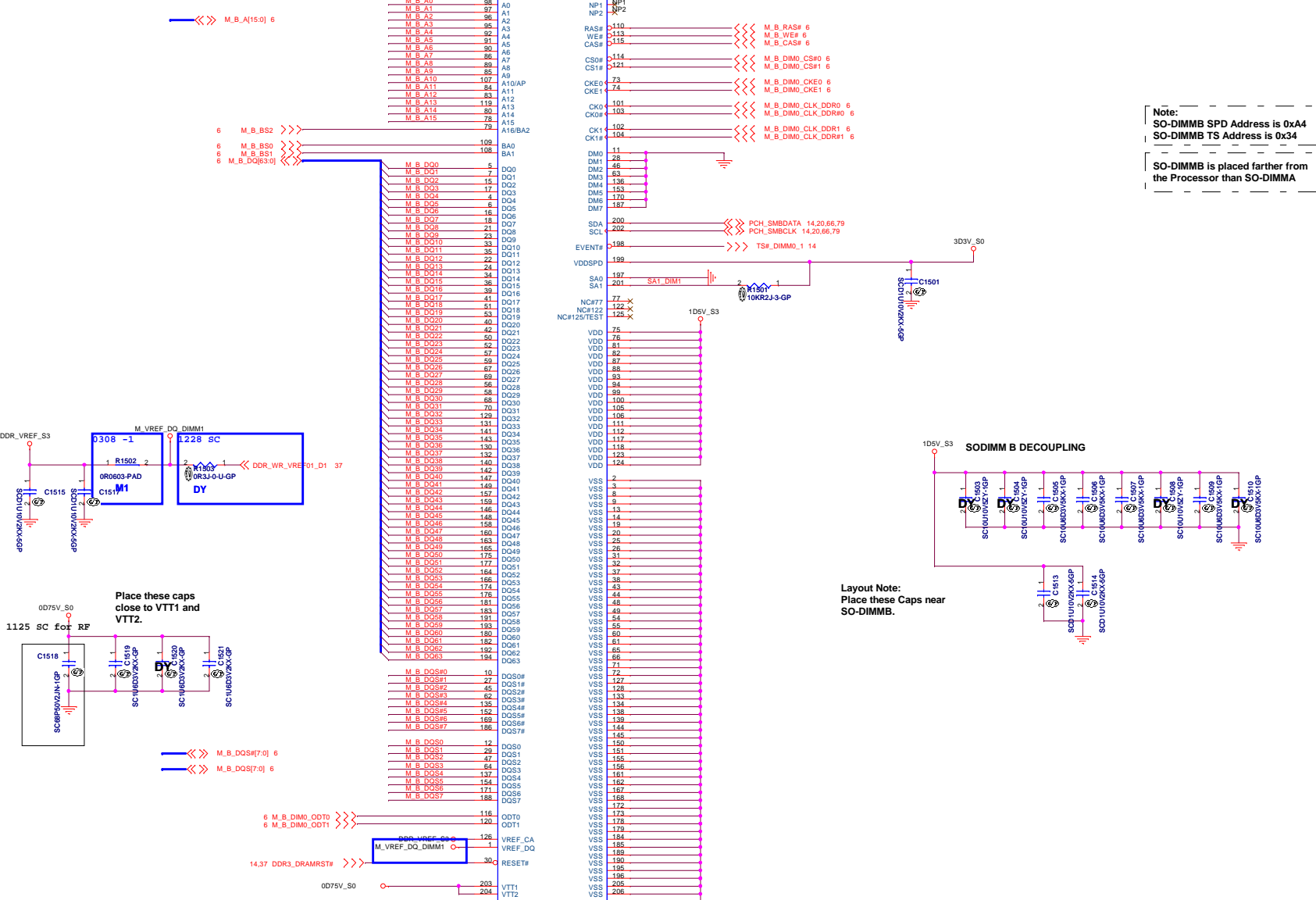
Layout Note:
 Place these Caps near SO-DIMMA.



H=4mm
 DDR3-204P-122-GP
 62.10017.Z51
 2nd = 62.10017.V51



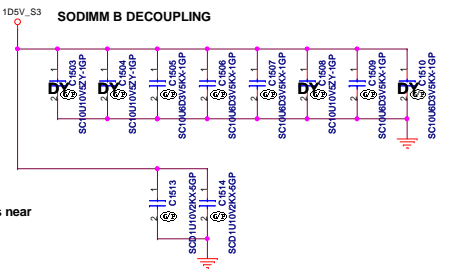
SSID = MEMORY



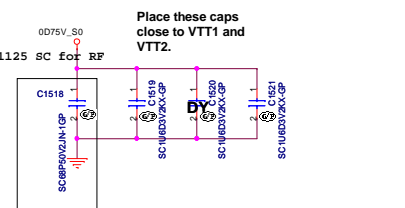
M_B_A0	88	A0	NP1
M_B_A1	87	A1	NP2
M_B_A2	86	A2	
M_B_A3	85	A3	RAS#
M_B_A4	84	A4	WE#
M_B_A5	81	A5	CAS#
M_B_A6	80	A6	
M_B_A7	79	A7	
M_B_A8	89	A8	CS0#
M_B_A9	88	A9	CS1#
M_B_A10	107	A10/AP	
M_B_A11	84	A11	CKE0
M_B_A12	83	A12	CKE1
M_B_A13	119	A13	CK0
M_B_A14	80	A14	CK0#
M_B_A15	78	A15	CK1
	79	A15	CK1#
	109	BA0	
	108	BA1	
M_B_D00	5	D00	
M_B_D01	7	D01	
M_B_D02	15	D02	
M_B_D03	17	D03	
M_B_D04	4	D04	
M_B_D05	6	D05	
M_B_D06	16	D06	
M_B_D07	18	D07	
M_B_D08	21	D08	
M_B_D09	23	D09	
M_B_D10	35	D10	
M_B_D11	35	D11	
M_B_D12	22	D12	
M_B_D13	24	D13	
M_B_D14	34	D14	
M_B_D15	36	D15	
M_B_D16	38	D16	
M_B_D17	41	D17	
M_B_D18	41	D18	
M_B_D19	53	D19	
M_B_D20	40	D20	
M_B_D21	42	D21	
M_B_D22	50	D22	
M_B_D23	52	D23	
M_B_D24	57	D24	
M_B_D25	59	D25	
M_B_D26	67	D26	
M_B_D27	69	D27	
M_B_D28	56	D28	
M_B_D29	58	D29	
M_B_D30	68	D30	
M_B_D31	70	D31	
M_B_D32	129	D32	
M_B_D33	131	D33	
M_B_D34	143	D34	
M_B_D35	141	D35	
M_B_D36	130	D36	
M_B_D37	142	D37	
M_B_D38	140	D38	
M_B_D39	142	D39	
M_B_D40	147	D40	
M_B_D41	149	D41	
M_B_D42	157	D42	
M_B_D43	159	D43	
M_B_D44	146	D44	
M_B_D45	148	D45	
M_B_D46	158	D46	
M_B_D47	160	D47	
M_B_D48	163	D48	
M_B_D49	165	D49	
M_B_D50	175	D50	
M_B_D51	177	D51	
M_B_D52	164	D52	
M_B_D53	166	D53	
M_B_D54	174	D54	
M_B_D55	176	D55	
M_B_D56	181	D56	
M_B_D57	183	D57	
M_B_D58	181	D58	
M_B_D59	183	D59	
M_B_D60	180	D60	
M_B_D61	182	D61	
M_B_D62	182	D62	
M_B_D63	184	D63	
M_B_DOS#0	10	DOS#0	
M_B_DOS#1	27	DOS#1	
M_B_DOS#2	45	DOS#2	
M_B_DOS#3	62	DOS#3	
M_B_DOS#4	136	DOS#4	
M_B_DOS#5	152	DOS#5	
M_B_DOS#6	169	DOS#6	
M_B_DOS#7	188	DOS#7	
M_B_DOS#0	12	DOS0	
M_B_DOS1	29	DOS1	
M_B_DOS2	47	DOS2	
M_B_DOS3	64	DOS3	
M_B_DOS4	137	DOS4	
M_B_DOS5	154	DOS5	
M_B_DOS6	171	DOS6	
M_B_DOS7	188	DOS7	
M_B_DIM0_ODT0	116	ODT0	
M_B_DIM0_ODT1	120	ODT1	
	126	VREF_CA	
	1	VREF_DQ	
	30	RESET#	
	203	VTT1	
	204	VTT2	

Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA



Layout Note:
Place these Caps near SO-DIMMB.



Place these caps close to VTT1 and VTT2.

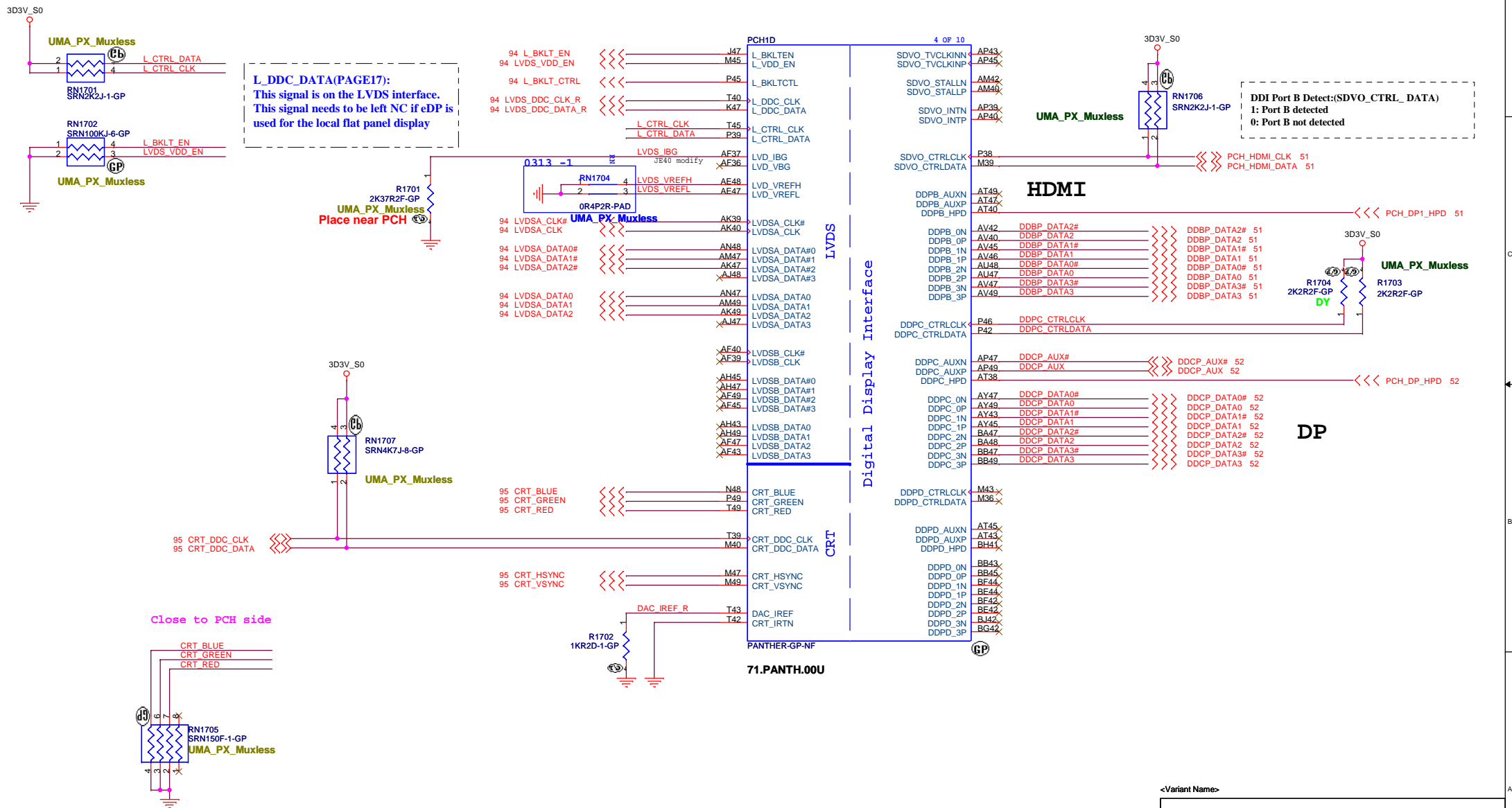
H = 8mm
62.10017.R91
1st = 62.10024.G01
2nd = 62.10024.D41

(Blanking)

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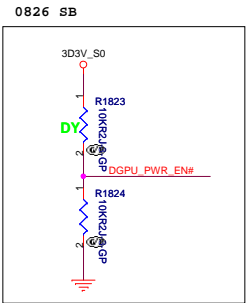
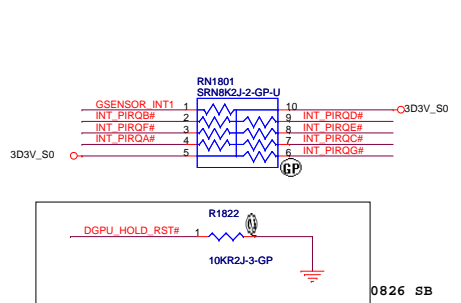
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Title			DDR3-SODIMM2		
Size	Document Number		Rev		
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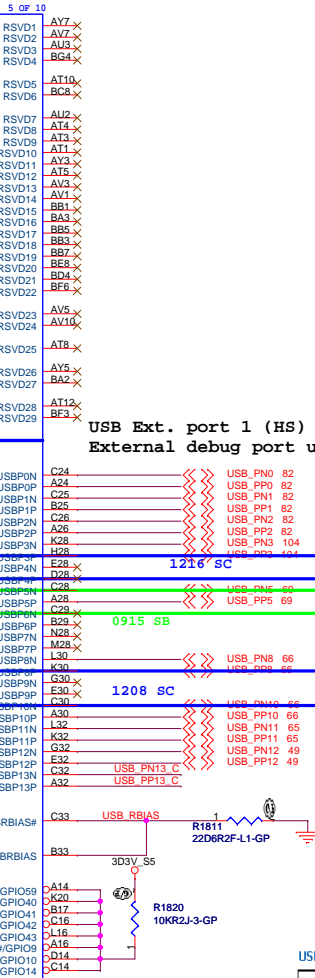
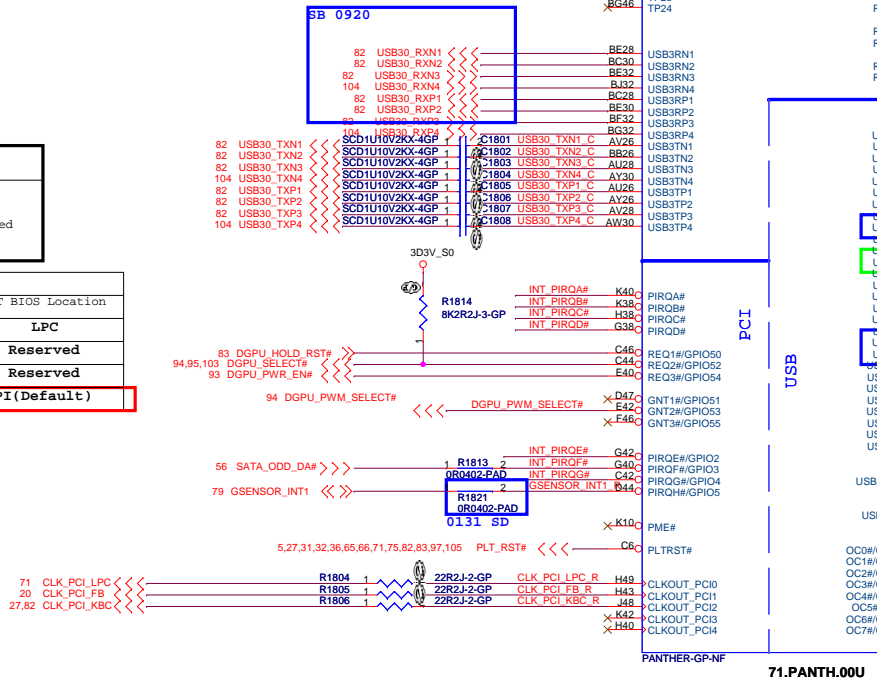
SSID = PCH



A16 swap override Strap/Top-Block Swap Override jumper

PCI_GNT#3 Low = A16 swap override/Top-Block Swap Override enabled High = Default

BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)



USB 2.0 Overcurrent Pin Default Usage

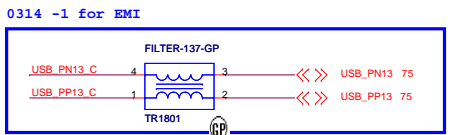
Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

USB Ext. port 1 (HS)
External debug port use on Huron river platform

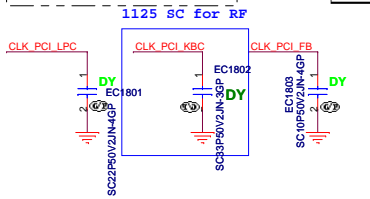
USB Table

Pair	Device
0	USB port 2 on S/B
1	USB port 3 on S/B
2	USB port 4 on S/B(usb charger)
3	DOCK
4	BLUETOOTH(from port3)
5	Fingerprint(from port2)(NO USE)
X	X
7	X
8	Mini Card2 (WWAN)
9	USB port1(SATA Combo), on M/B
10	3G Card
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card or USB HUB(New/Smart)

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OC[3:0]# for Device 29 (Ports 0-7)
OC[7:4]# for Device 26 (Ports 8-13)



<Variant Name>

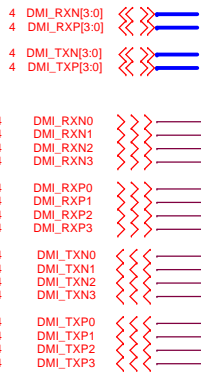
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (PCI/USB/NVRAM)**

Size: Custom Document Number: **BAD40 HC** Rev: **1**

Date: Thursday, April 12, 2012 Sheet: 18 of 108

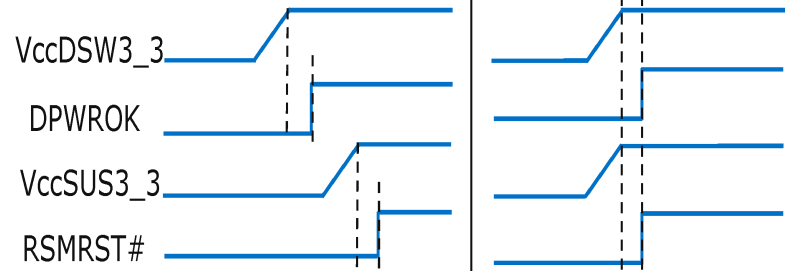
SSID = PCH



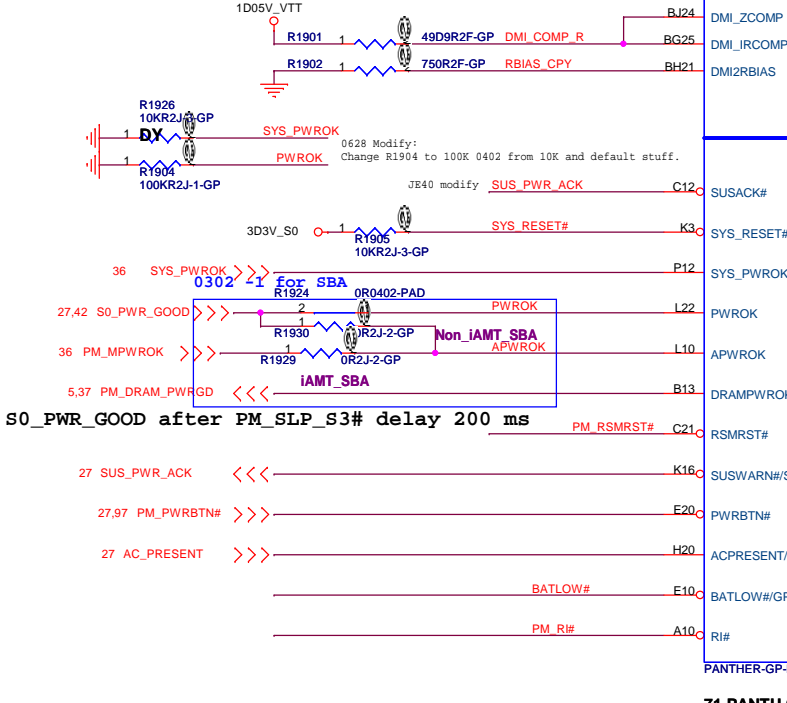
Signal Routing Guideline:
 DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
 DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.

Deep S4/S5 Supported

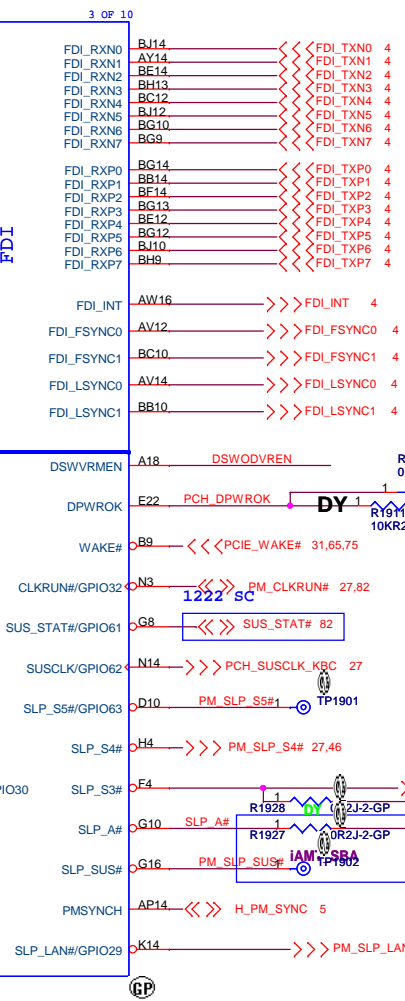
Deep S4/S5 Not Supported



For platforms not supporting Deep S4/S5
 1.VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
 2.DPWROK and RSMRST# will rise at the same time (connected on board)
 3.SLP_SUS# and SUSACK# are left as 'no connect'
 4.SUSWARN# used as SUSPWRDNACK/GPIO30



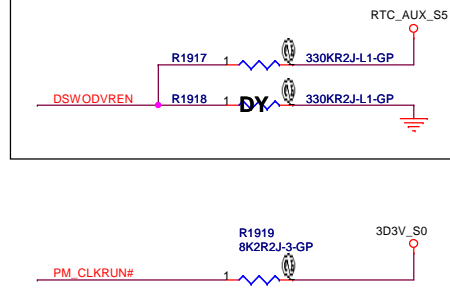
System Power Management



PCIE_WAKE#
 CRB : 1K
 CEKLT : 10K

PWRBTN#
 This signal has an internal pull-up resistor
 PM_RSMRST#
 CRB : PL 10K
 ANNIE : PL 100K

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled



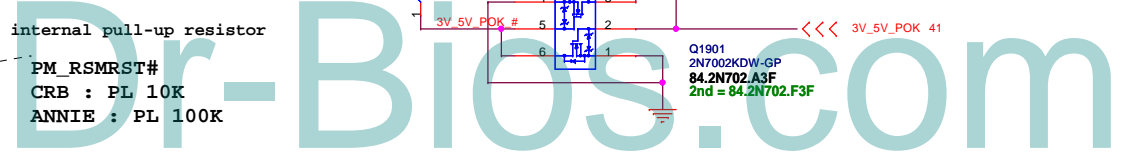
<Variant Name>

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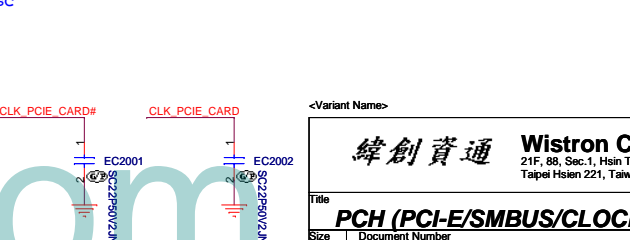
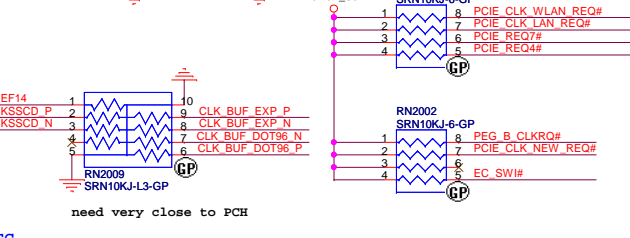
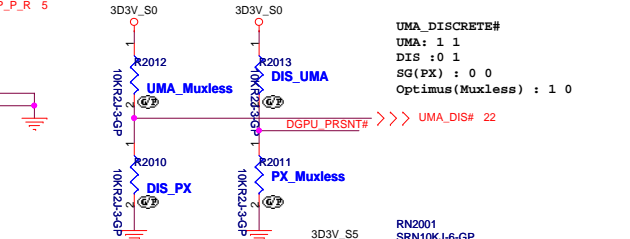
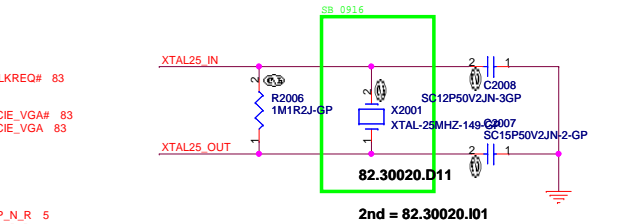
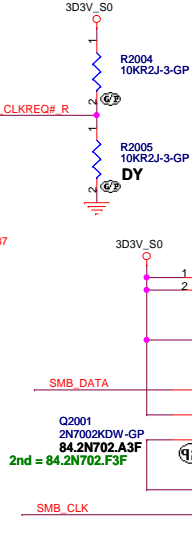
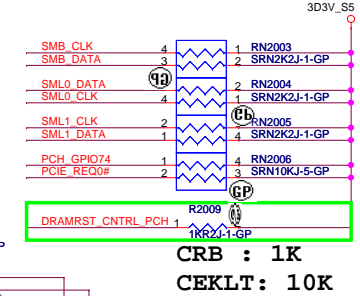
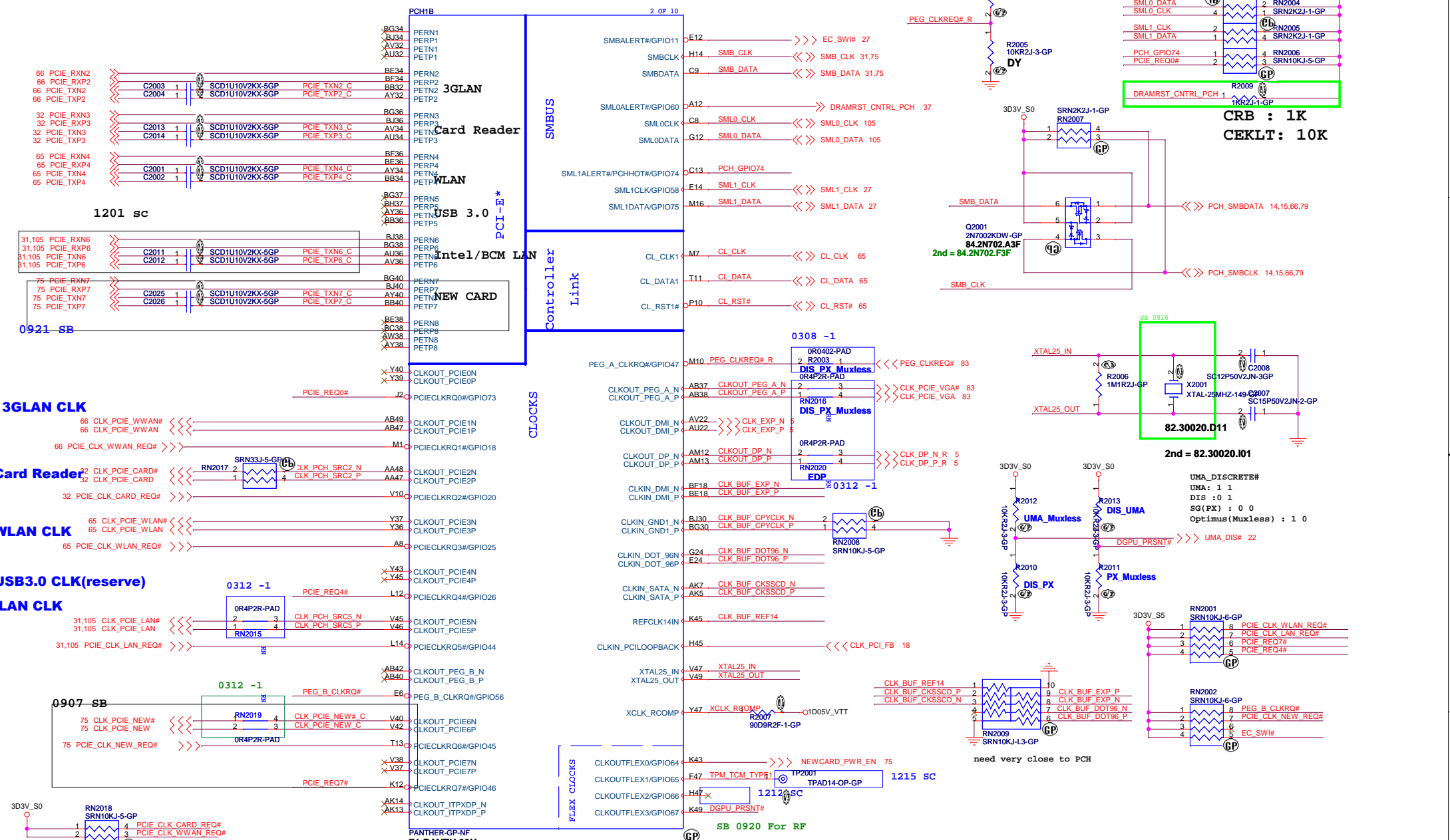
Title: **PCH (DM I/FDI/PM)**

Size A3 Document Number: **BAD40 HC** Rev: **1**

Date: Thursday, April 12, 2012 Sheet 19 of 108



SSID = PCH

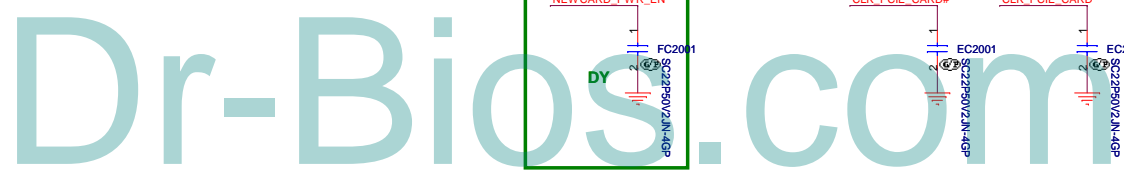


PCIECLKRQ1# and PCIECLKRQ2# Support S0 power only

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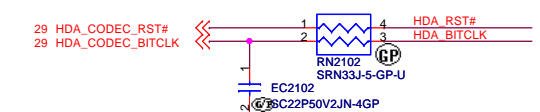
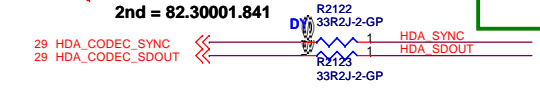
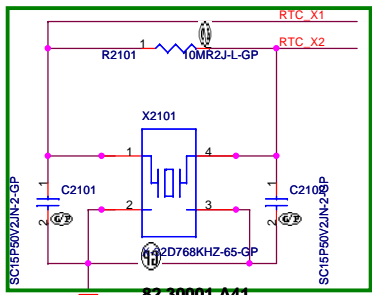
PCH (PCI-E/SMBUS/CLOCK/CL)

Size: Document Number
 Custom: **BAD40 HC**
 Date: Thursday, April 12, 2012 Sheet 20 of 108



SSID = PCH

SB 0923



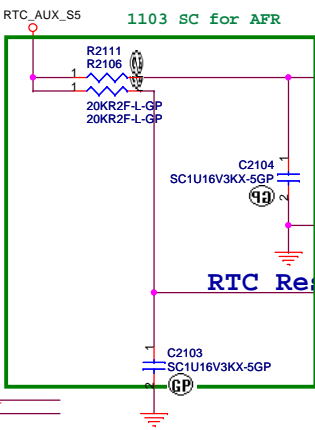
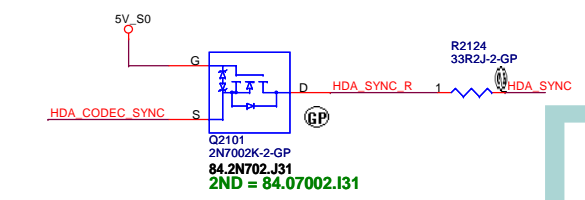
Flash Descriptor Security Override	
HDA_SDOUT	Low = Default High = Enable

No Reboot Strap	
HDA_SPKR	Low = Default High = No Reboot

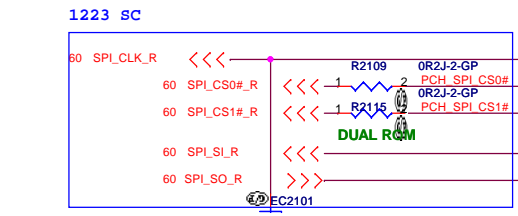
+3VS_+1.5VS_HDA_IO

This signal has a weak internal pull down. On Die PLL VR is supplied by 1.5V when sampled high, 1.8 V when sampled low. Needs to be pulled High for Huron River platform. co-operate with R2310

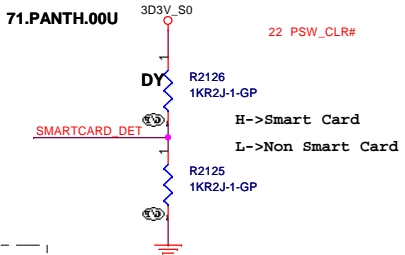
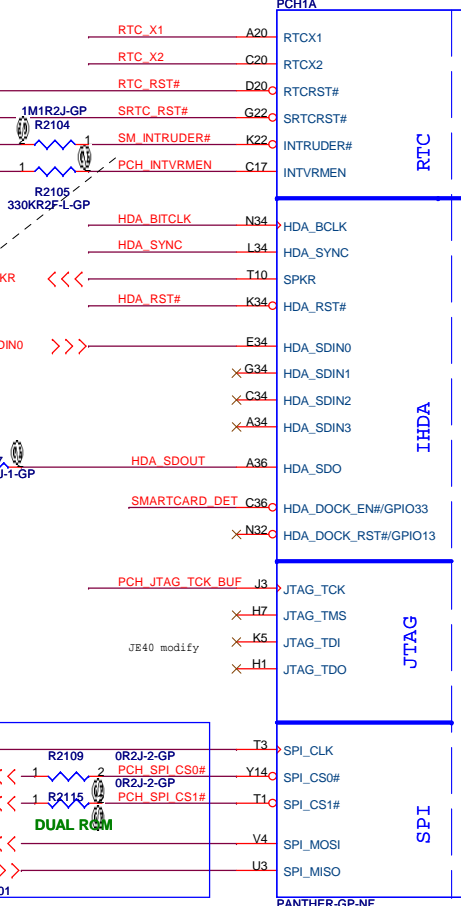
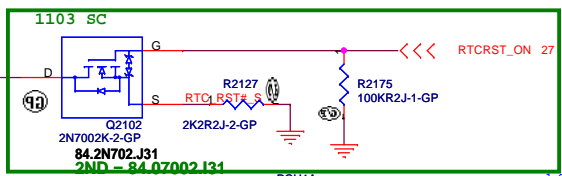
PLL ODVR VOLTAGE	
HDA_SYNC	Low = 1.8V (Default) High = 1.5V



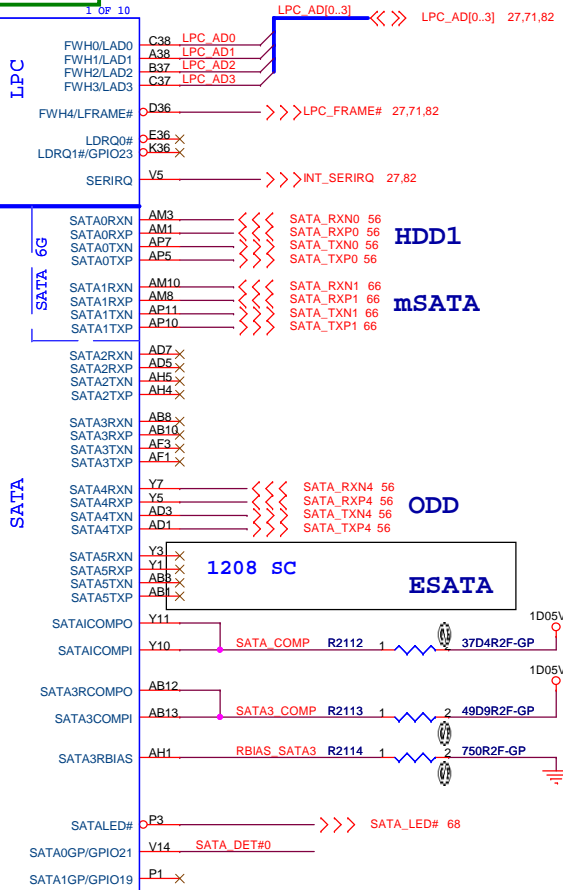
INTVRMEN- Integrated SUS
1.05V VRM Enable
High - Enable internal VRs
Low - Enable external VRs



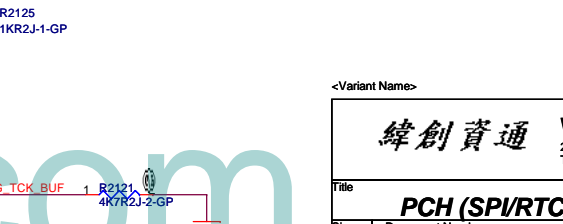
HDA_SYNC: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.



H->Smart Card
L->Non Smart Card



H->Smart Card
L->Non Smart Card

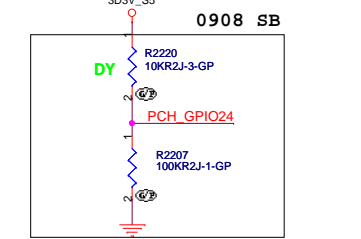
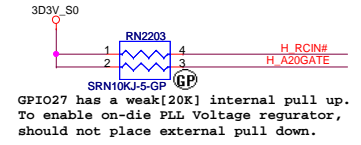


<Variant Name>

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PCH (SPI/RTC/LPC/SATA/IHDA)	
Title	Rev 1
Size A3	Document Number BAD40 HC
Date: Thursday, April 12, 2012	Sheet 21 of 108

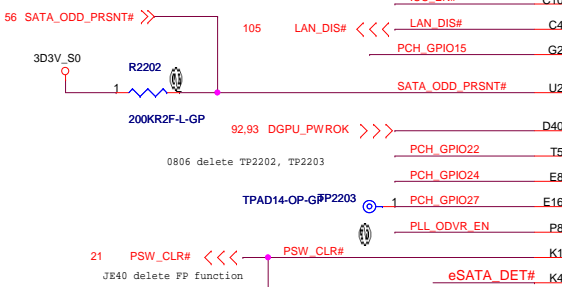
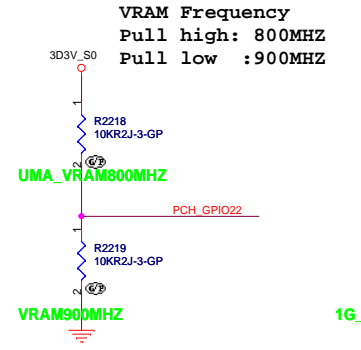
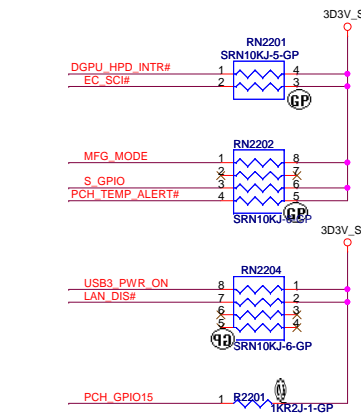
SSID = PCH

Note:
For PCH debug with XDP, need to NO STUFF R2218



	INTERNAL GFX	EXTERNAL GFX
R2205	DY	10K
R2206	100K	DY

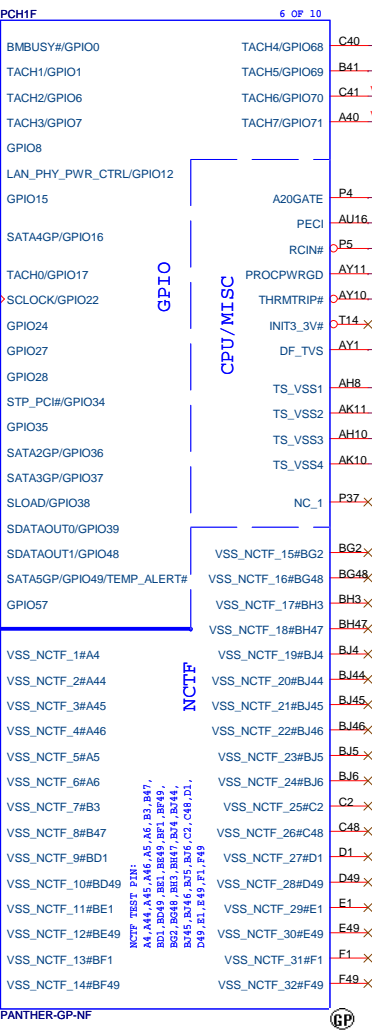
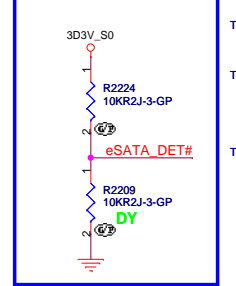
	LVDS	eDP
EDP#_LVDS	H	L



Password Clear
G2201
GAP-OPEN

1124 SC
del R2206

1208 SC for Del e-SATA

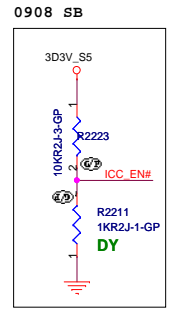
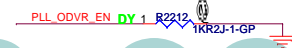


71.PANTH.00U

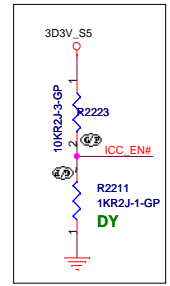
NCTF TEST PIN:
A5, A6, B3, B4, B7, B8, B9, B11, B14, B15, B16, B17, B18, B19, B20, B21, B22, B23, B24, B25, B26, B27, B28, B29, B30, B31, B32, B33, B34, B35, B36, B37, B38, B39, B40, B41, B42, B43, B44, B45, B46, B47, B48, B49, B50, B51, B52, B53, B54, B55, B56, C2, C8, D1, D49, E1, E49, F1, F49

PLL ON DIE VR ENABLE

NOTE: This signal has a weak internal pull-up 20K
ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT
DISABLED -- LOW (R2212 STUFFED)



0908 SB



Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY) - DISABLED [DEFAULT]
	LOW (R2211) - ENABLED

GPIO8 has a weak[20K] internal pull up. Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

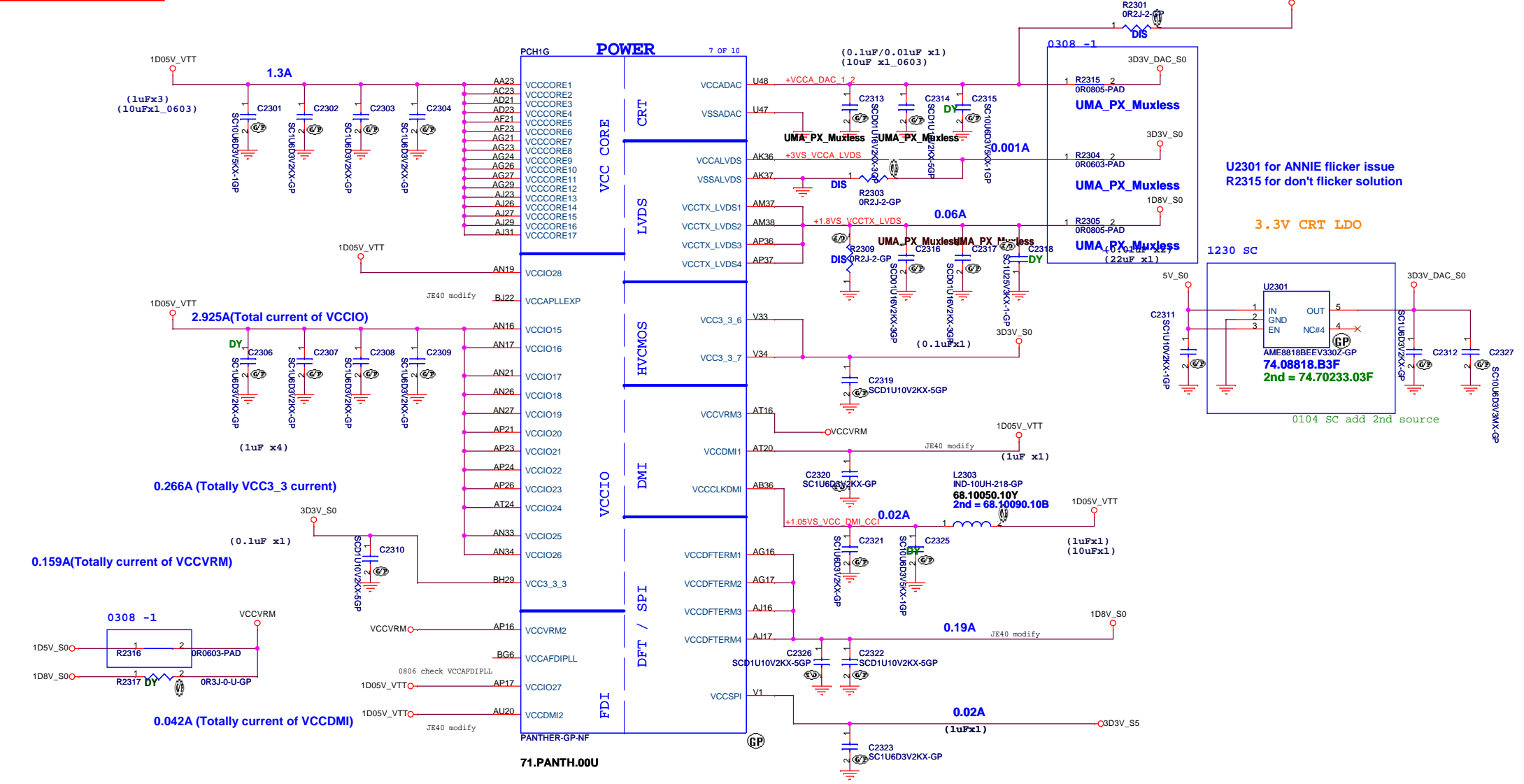
Title: **PCH (GPIO/CPU)**

Size Custom: **BAD40 HC**

Date: Thursday, April 12, 2012

Rev: **1**

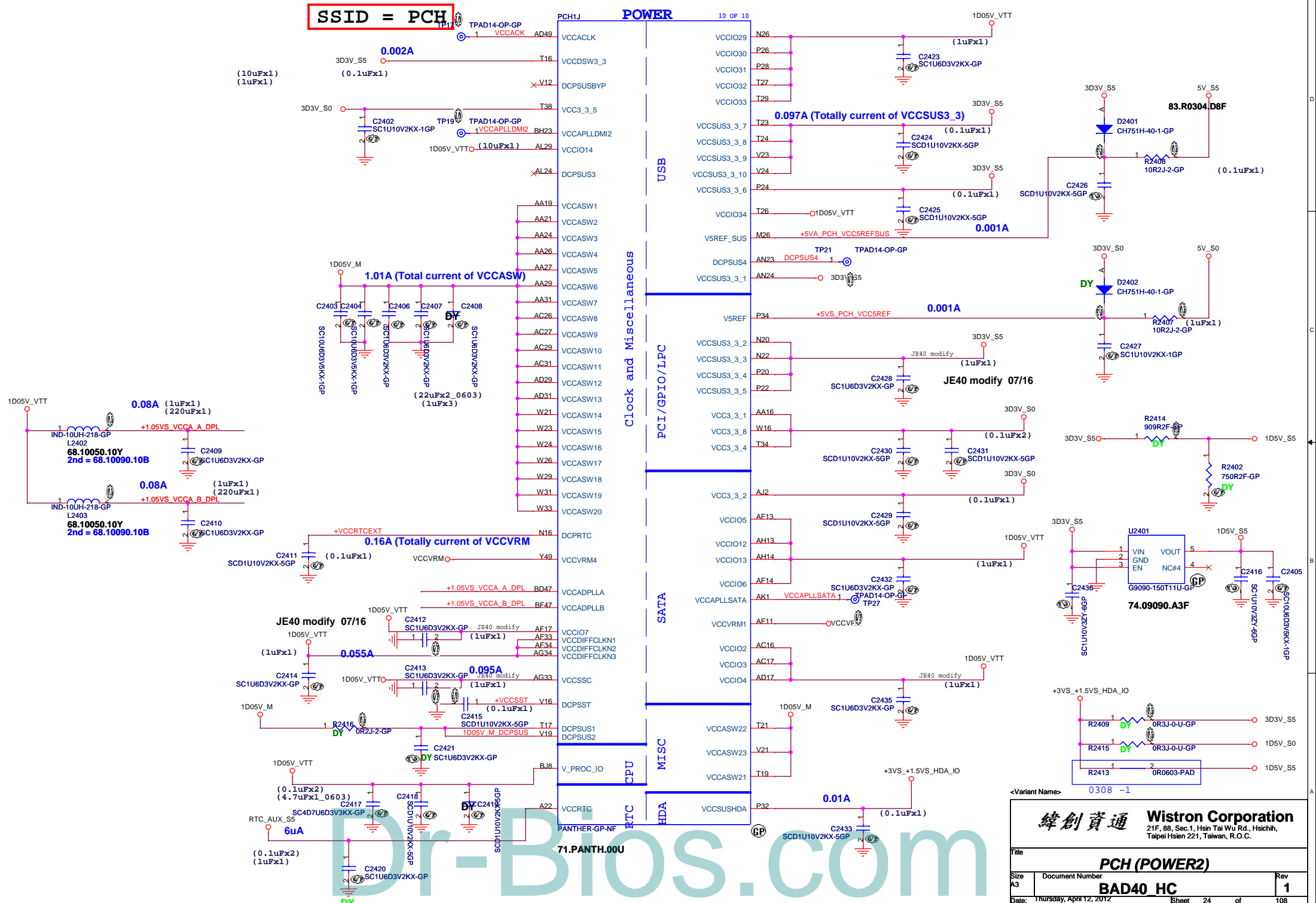
Sheet 22 of 108



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<Variant Name>		
緯創資通 Wistron Corporation		
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
PCH (POWER1)		
Size A3	Document Number	Rev
	BAD40_HC	1
Date: Thursday, April 12, 2012	Sheet 23	of 108

SSID = PCH



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Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

PCH (POWER2)

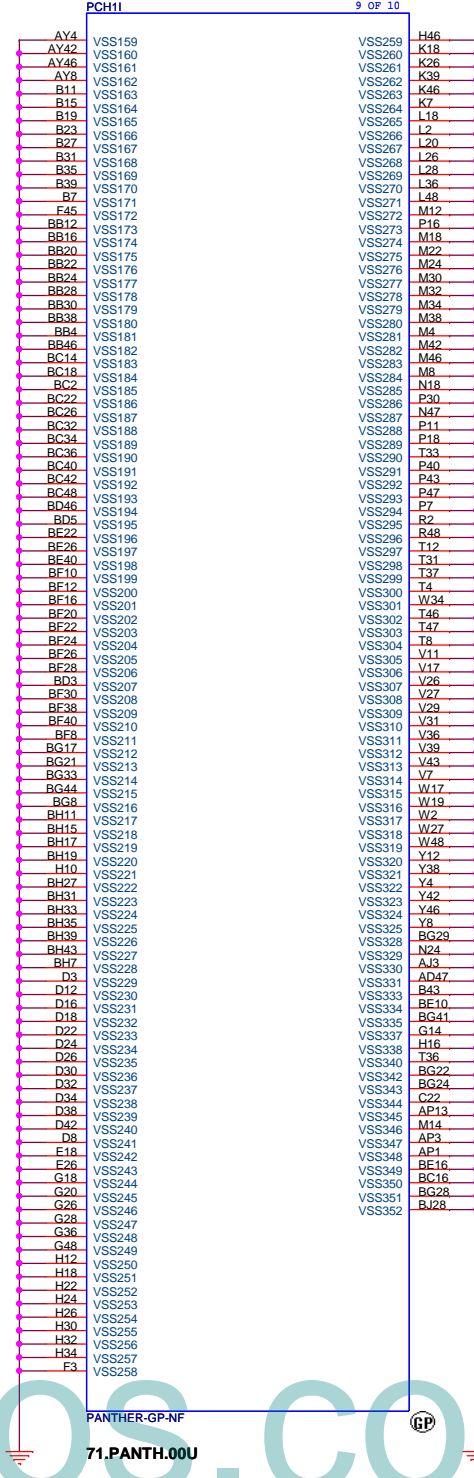
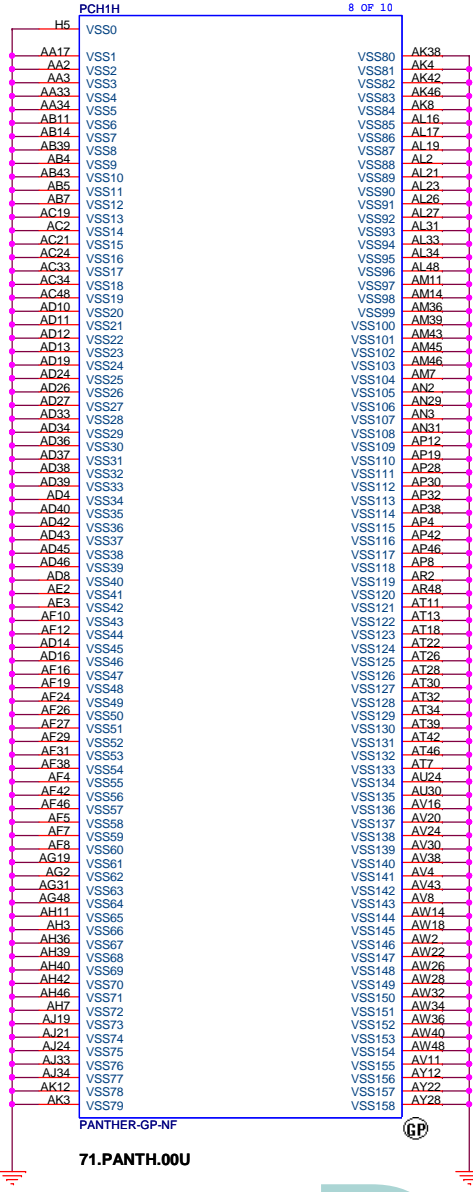
BAD40 HC

Rev 1

Thursday, April 12, 2012

Sheet 24 of 108

SSID = PCH



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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (VSS)**

Size: A3
Document Number: **BAD40 HC**
Rev: **1**

Date: Thursday, April 12, 2012 Sheet 25 of 108

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<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
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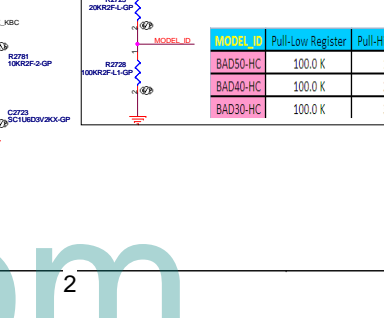
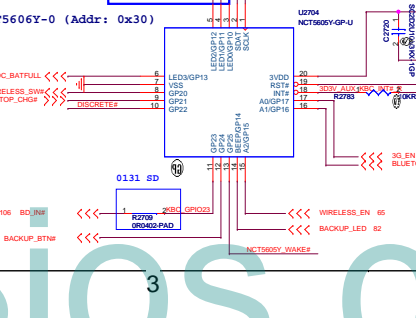
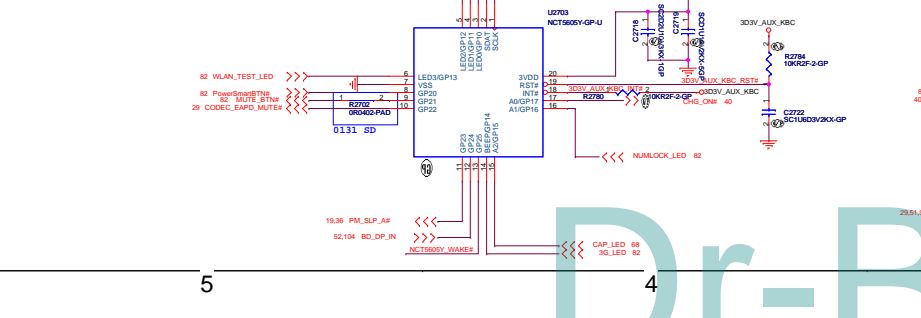
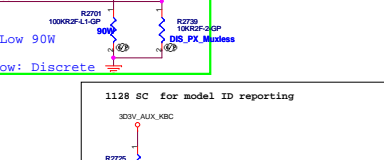
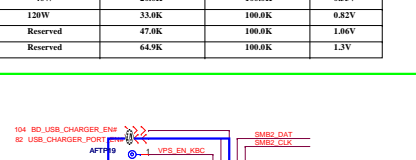
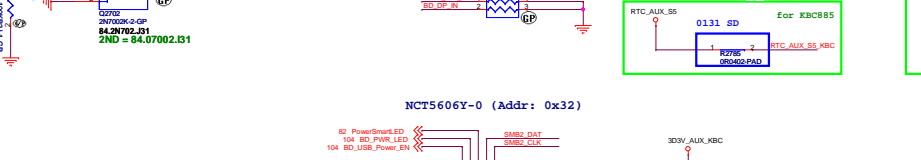
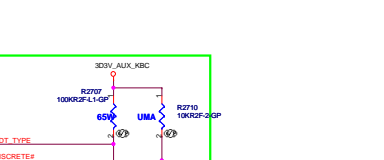
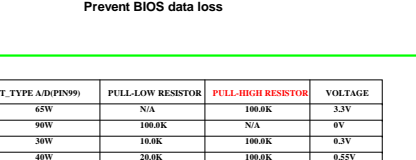
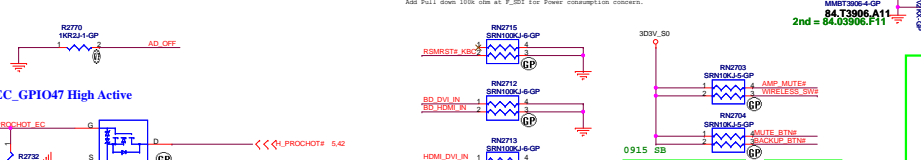
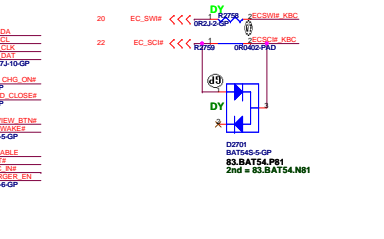
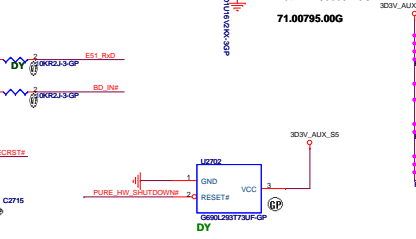
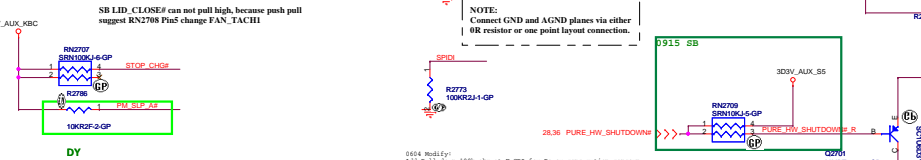
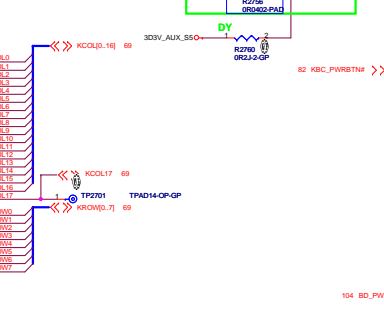
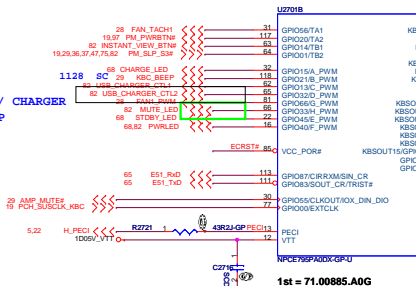
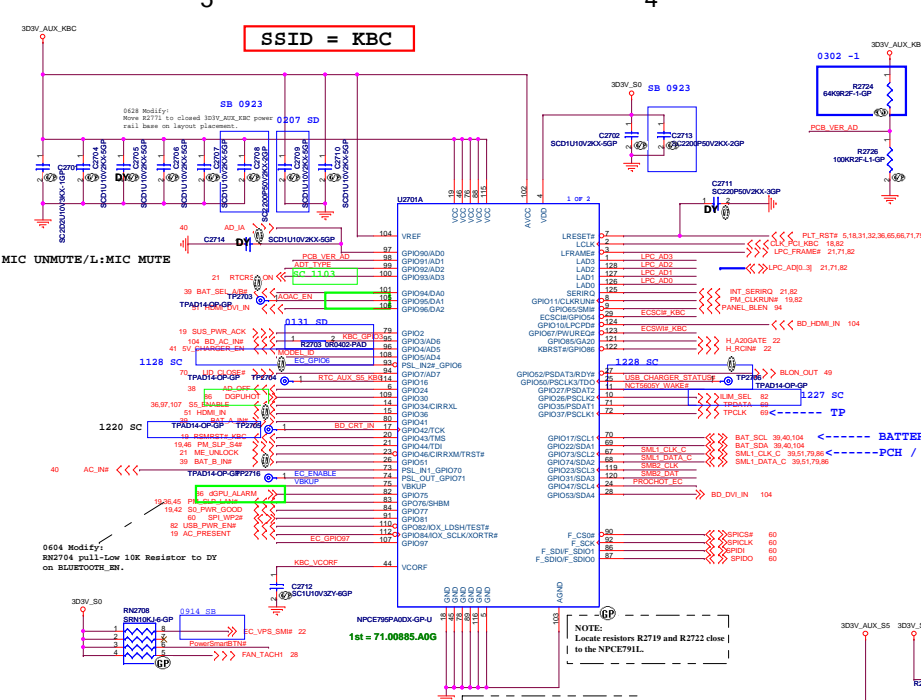
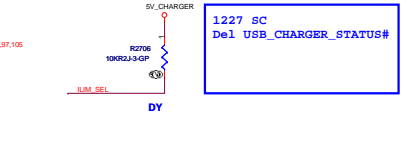
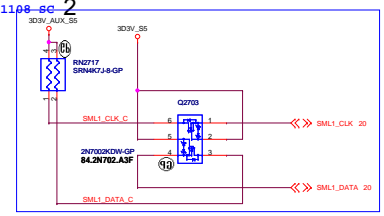
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Size	Document Number	Rev
A4	BAD40 HC	1

Date: Thursday, April 12, 2012	Sheet 26 of 108
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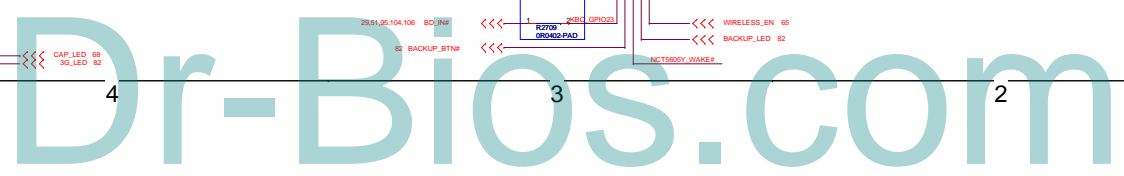
SSID = KBC

PCB VERSION A/(PIN#s)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.48V
SD	100.0K	47.0K	2.24V
-1	100.0K	64.9K	2.0V
-2	100.0K	76.8	1.87V
-3	100.0K	100.0K	1.65V



ADT_TYPE A/(PIN#9)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
65W	N/A	100.0K	3.3V
90W	100.0K	N/A	0V
30W	10.0K	100.0K	0.3V
40W	20.0K	100.0K	0.55V
120W	33.0K	100.0K	0.82V
Reserved	47.0K	100.0K	1.06V
Reserved	64.9K	100.0K	1.3V

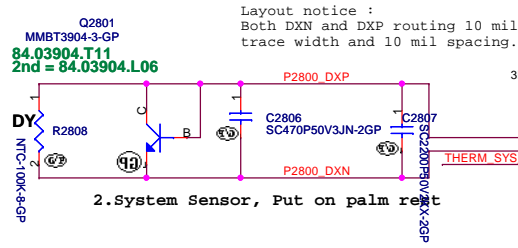
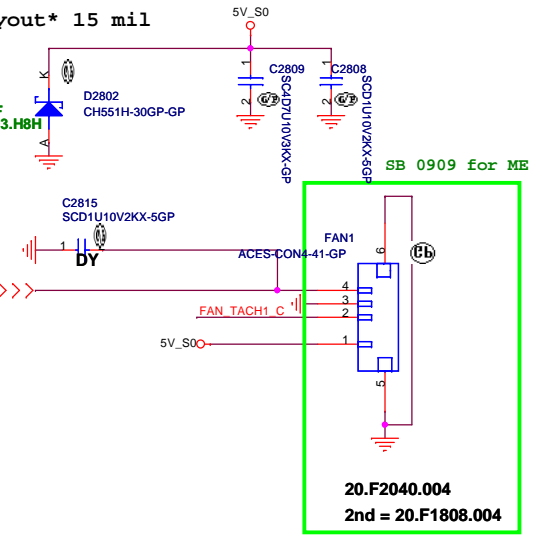
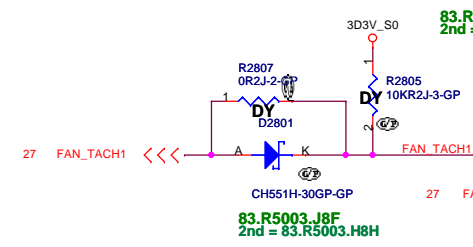
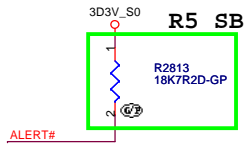
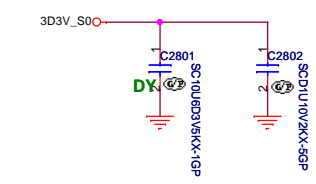
MODEL ID	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting
BAD50-HC	100.0 K	10.0 K	3.000 V	3.0054	>= 2.875 V
BAD40-HC	100.0 K	20.0 K	2.750 V	2.7591	>= 2.616 V < 2.875 V
BAD30-HC	100.0 K	33.0 K	2.481 V	2.4935	>= 2.363 V < 2.616 V



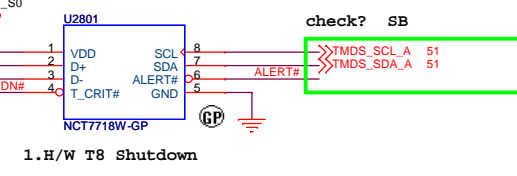
SSID = Thermal

Fan controller P2793

Layout 15 mil



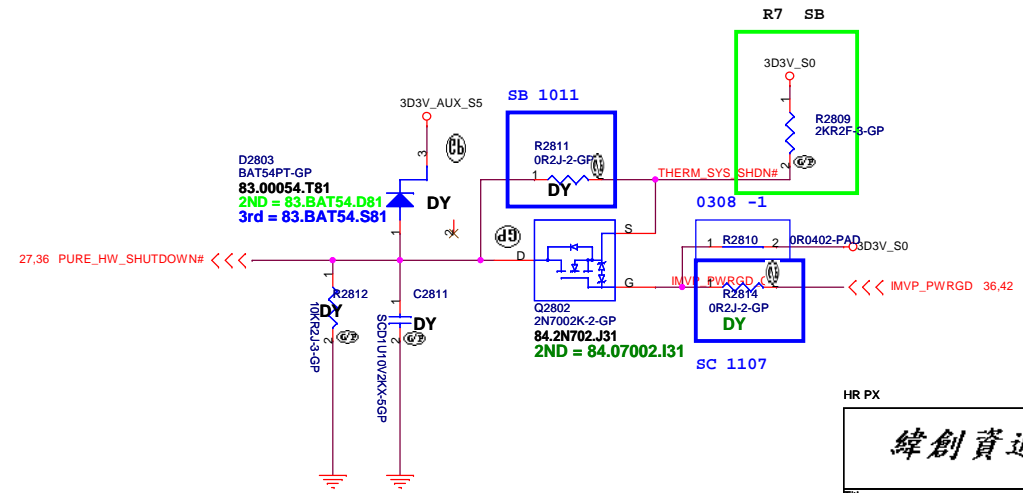
Layout notice :
Both DXN and DXP routing 10 mil trace width and 10 mil spacing.



ALERT# /T CRIT#
Pull-up Resistor

R5	2Kohm	7.5Kohm	R7	10.5Kohm	14Kohm	18.7Kohm
2Kohm	77°C	87°C	97°C	107°C	117°C	
7.5Kohm	79°C	89°C	99°C	109°C	119°C	
10.5Kohm	81°C	91°C	101°C	111°C	121°C	
14Kohm	83°C	93°C	103°C	113°C	123°C	
18.7Kohm	85°C	95°C	105°C	115°C	125°C	

T_CRIT temperature strapping point



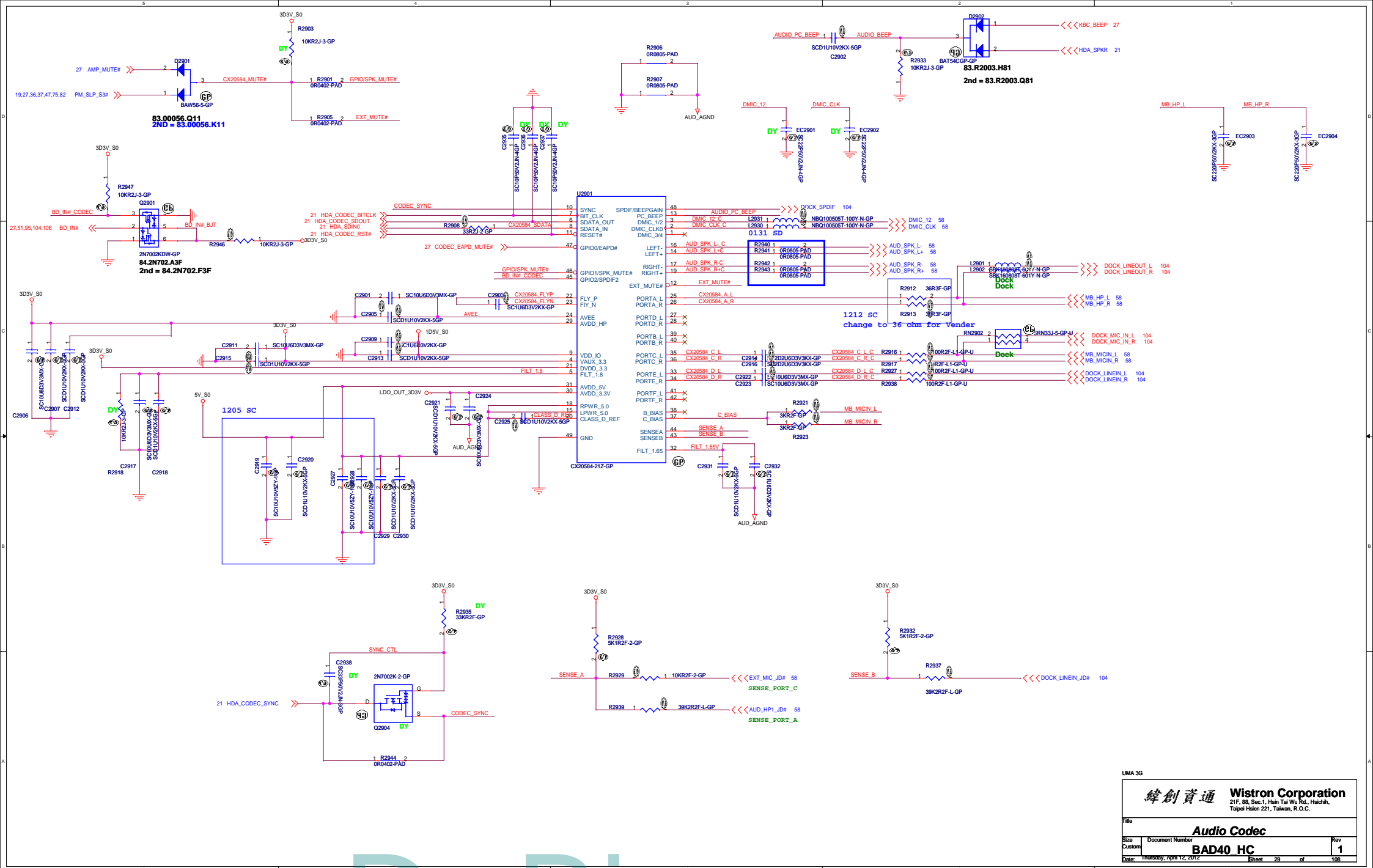
HR PX

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Thermal T7718/Fan Controller P2793**

Size: Custom Document Number: **BAD40 HC** Rev: **1**

Date: Thursday, April 12, 2012 Sheet 28 of 108



AUDIO OP AMPLIFIER

<Variant Name>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Audio AMP

Size

A4

Document Number

BAD40 HC

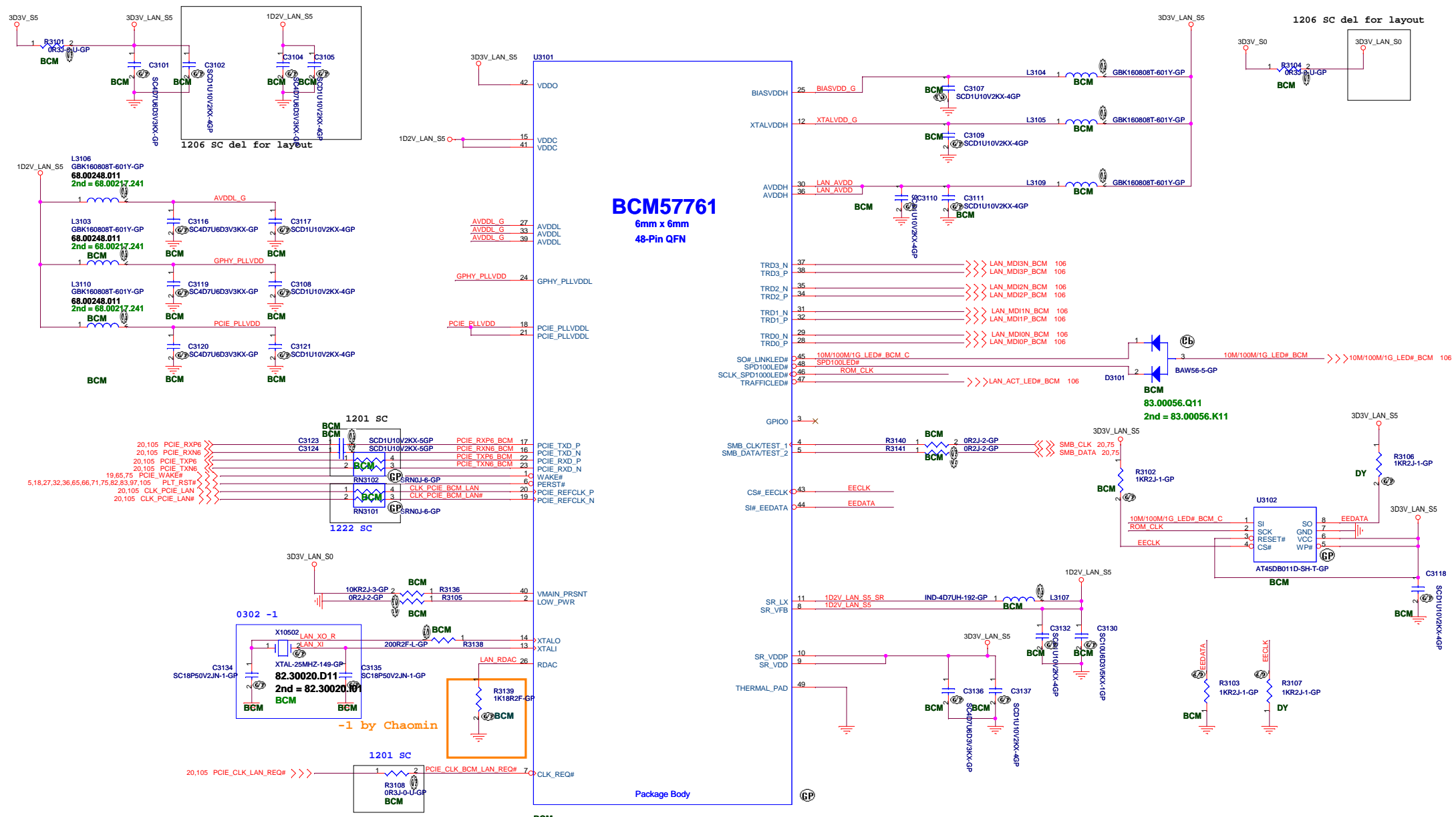
Rev

1

Date: Thursday, April 12, 2012

Sheet 30 of 108

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BCM
1st = 71.57761.M02

<Variant Name>

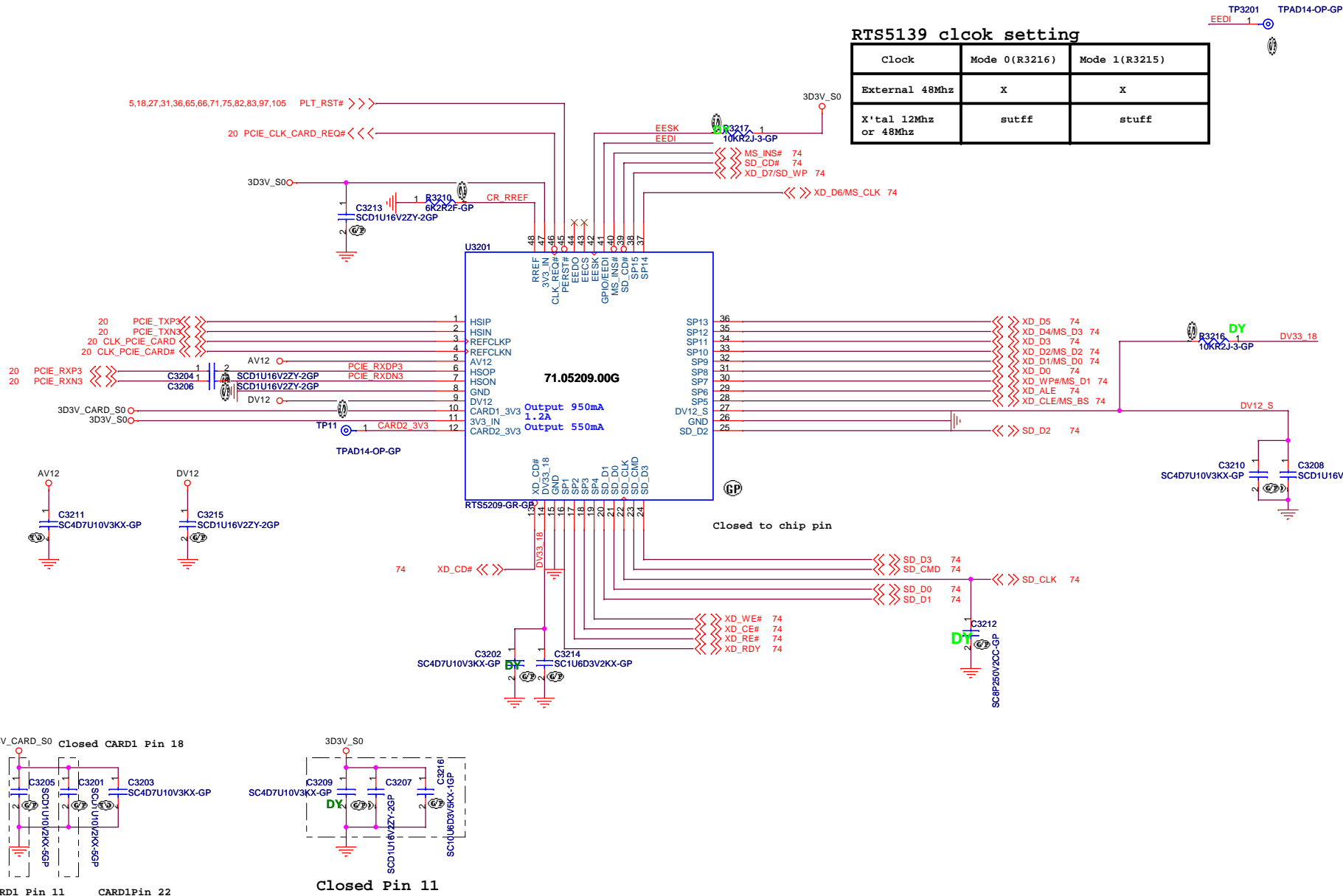
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **BCM57780**

Size	Document Number	Rev
Custom	BAD40 HC	1

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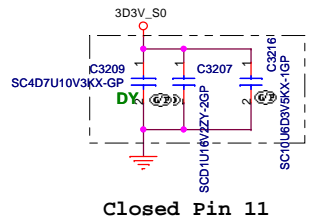
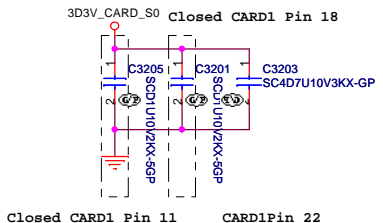
RTS5139 clcok setting

Clock	Mode 0(R3216)	Mode 1(R3215)
External 48Mhz	X	X
X'tal 12Mhz or 48Mhz	stuff	stuff

TP3201 TPAD14-OP-GP
EEDI 1

71.05209.00G
Output 950mA
1.2A
Output 550mA

Closed to chip pin



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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **RTS5209(CARD READER)**

Size A3 Document Number: **BAD40_HC** Rev: **1**

Date: Thursday, April 12, 2012 Sheet 32 of 108

(Blanking)

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<Variant Name>

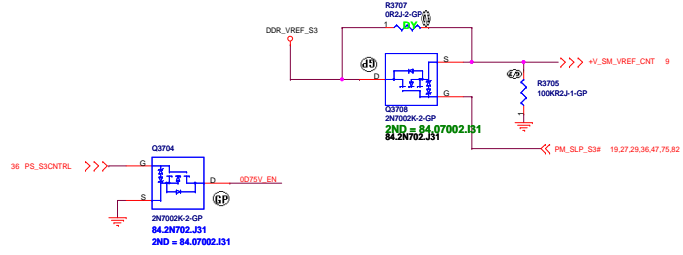
緯創資通			Wistron Corporation		
			21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
Reserved					
Size	Document Number				Rev
A4	BAD40 HC				1
Date:	Thursday, April 12, 2012			Sheet 33	of 108

reserve

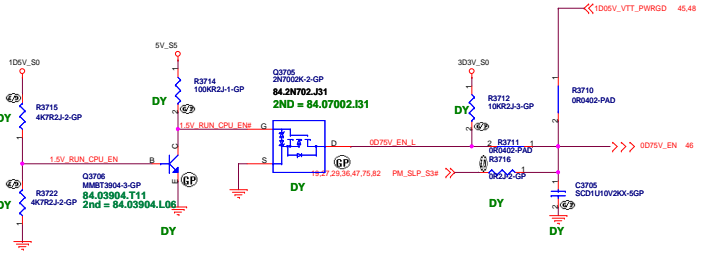
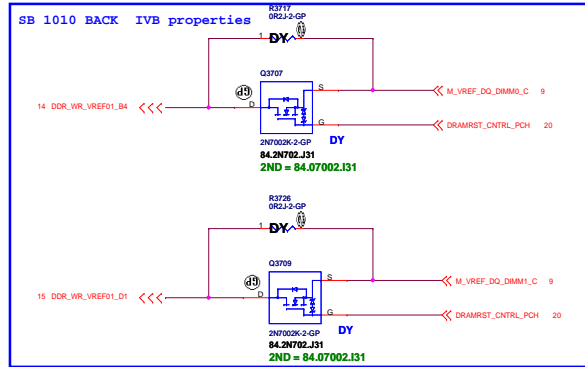
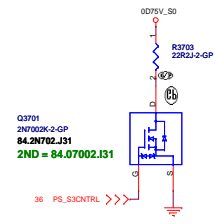
Dr-Bios.com

HR		
緯創資通		Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	USB 3.0 Controller	
Size	Document Number	Rev
Custom	BAD40 HC	1
Date: Thursday, April 12, 2012	Sheet 35	of 108

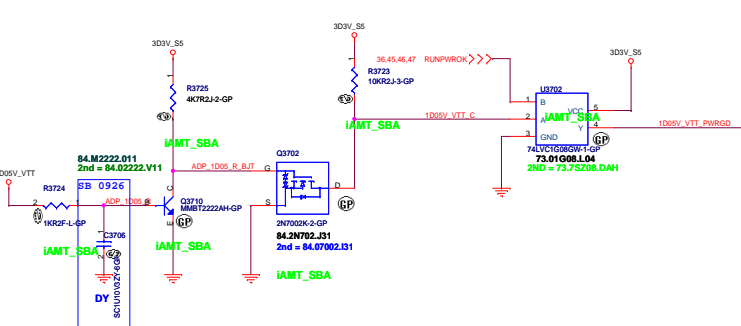
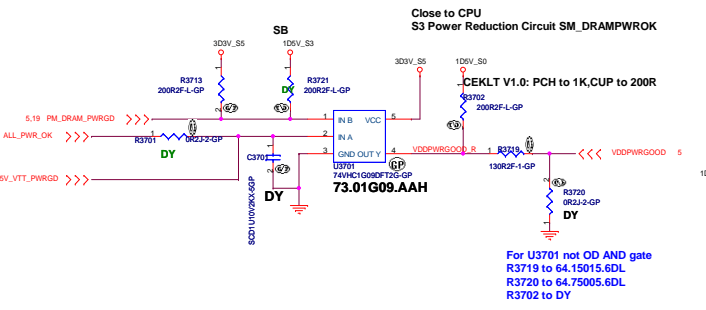
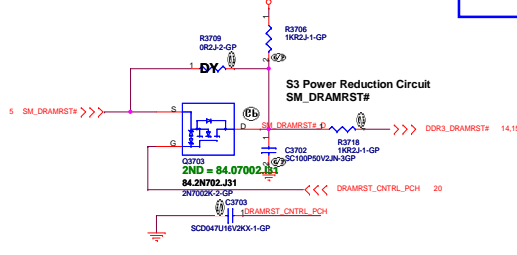
**Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation**



**Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK**

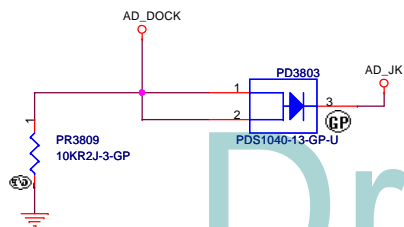
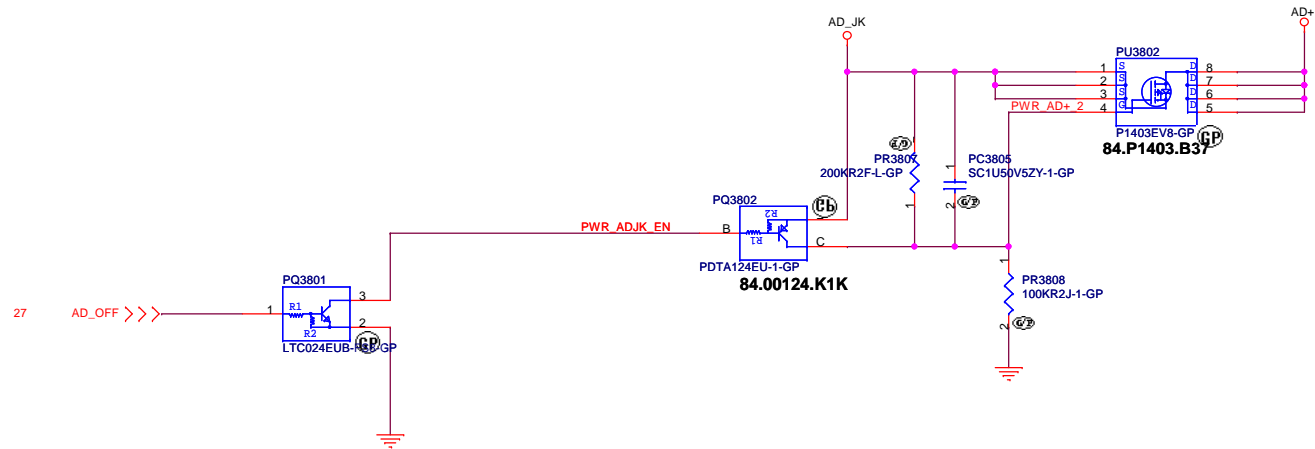
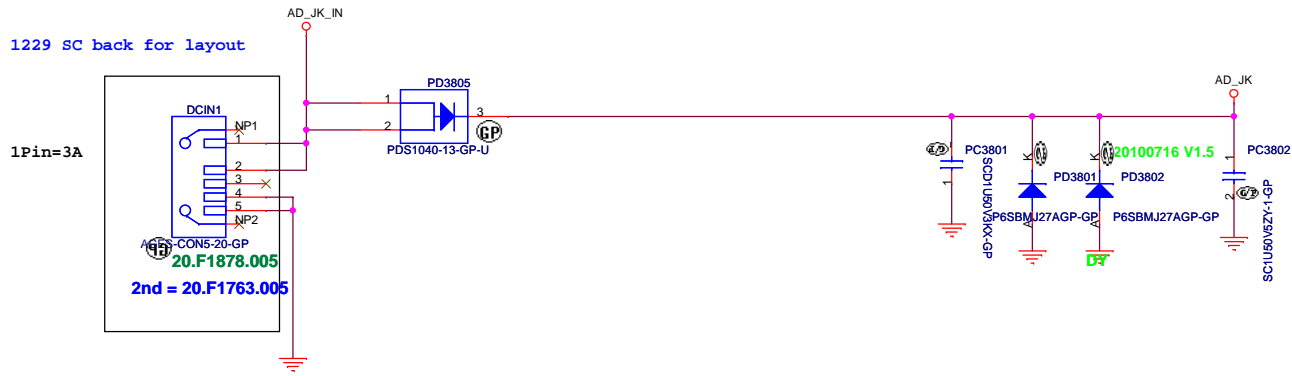


**Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK**



For U3701 not OD AND gate
R3719 to 64.15015.GDL
R3720 to 64.75005.GDL
R3702 to DY

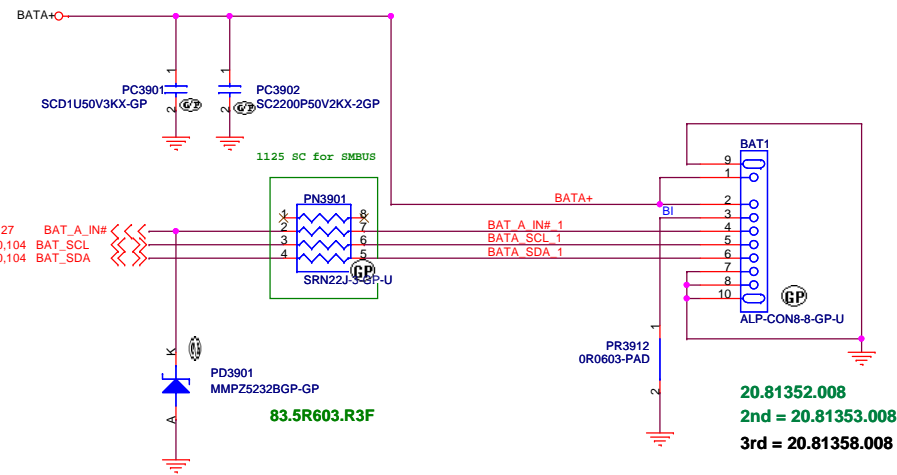
HR PX		Wistron Corporation	
緯創資通		2/F, No. Sec-1, Hsin Tai Wu Rd, Hsinshui, Taipei Hsein 221, Taiwan, R.O.C.	
File	ADAPTER		
Size	Document Number	New	
Custom	BAD40 HC	1	
Date: Thursday, April 12, 2012	Sheet	37	of 106



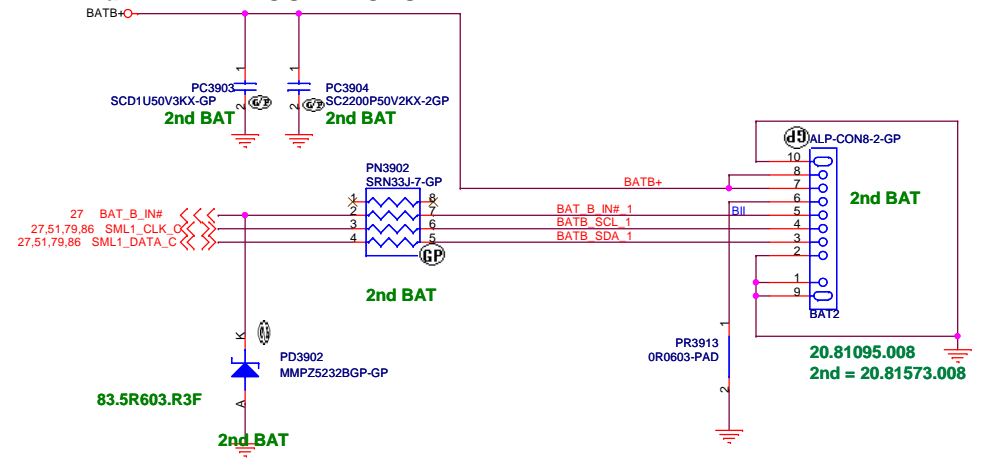
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緯創資通 Wistron Corporation		
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title DCIN JACK		
Size A3	Document Number BAD40_HC	Rev 1
Date: Thursday, April 12, 2012	Sheet 38	of 108

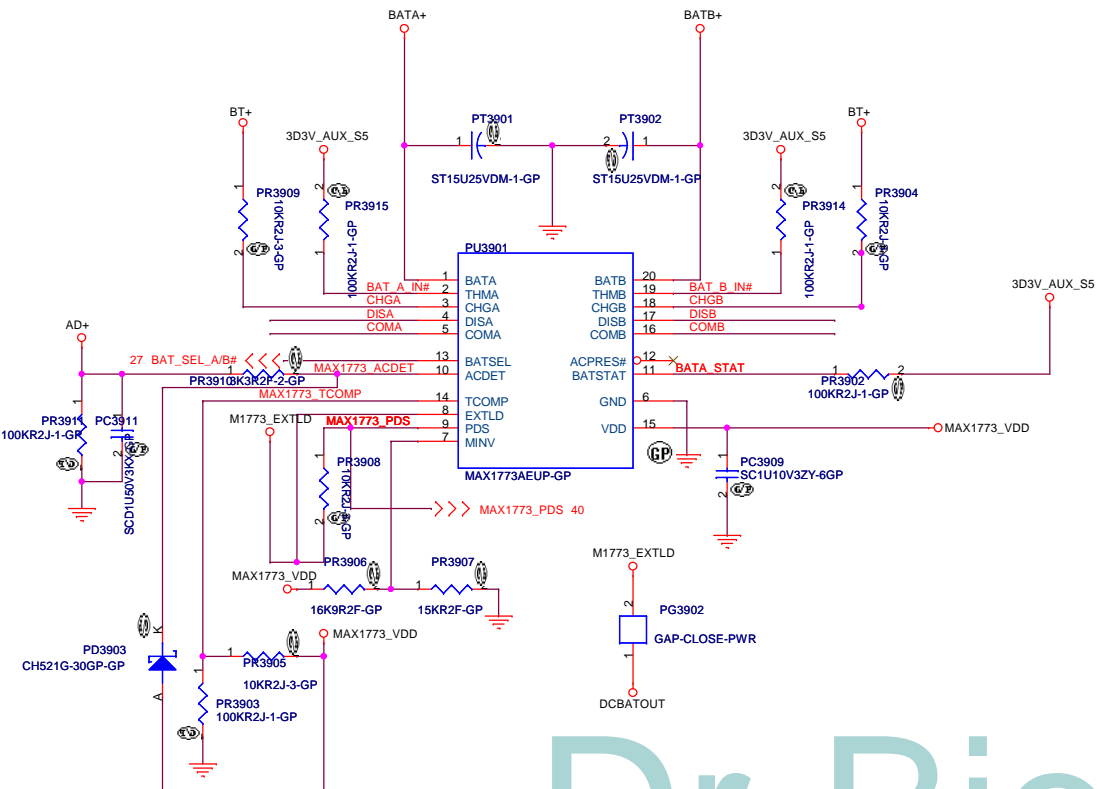
MAIN BATTERY CONNECTOR



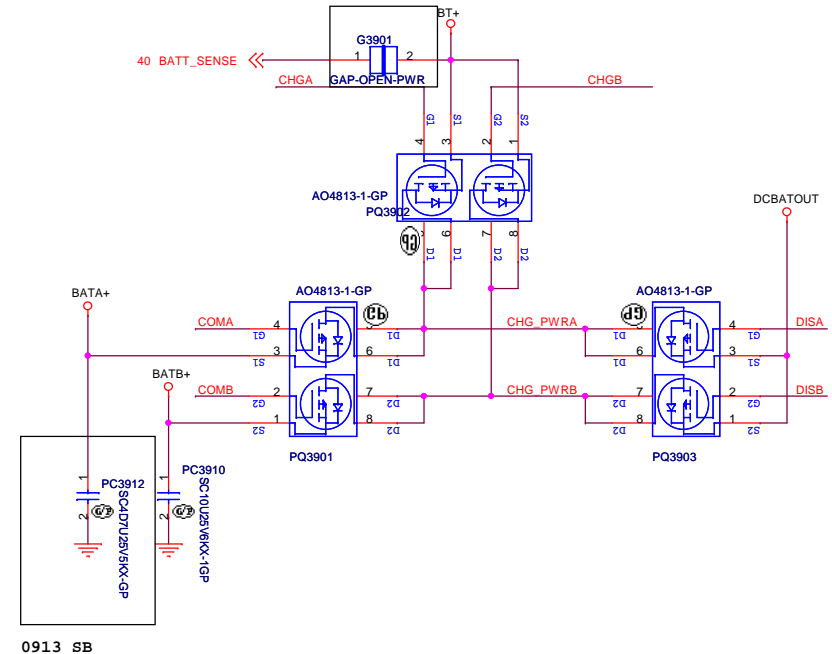
2nd BATTERY CONNECTOR



BATTERY SWITCH



1108 SC

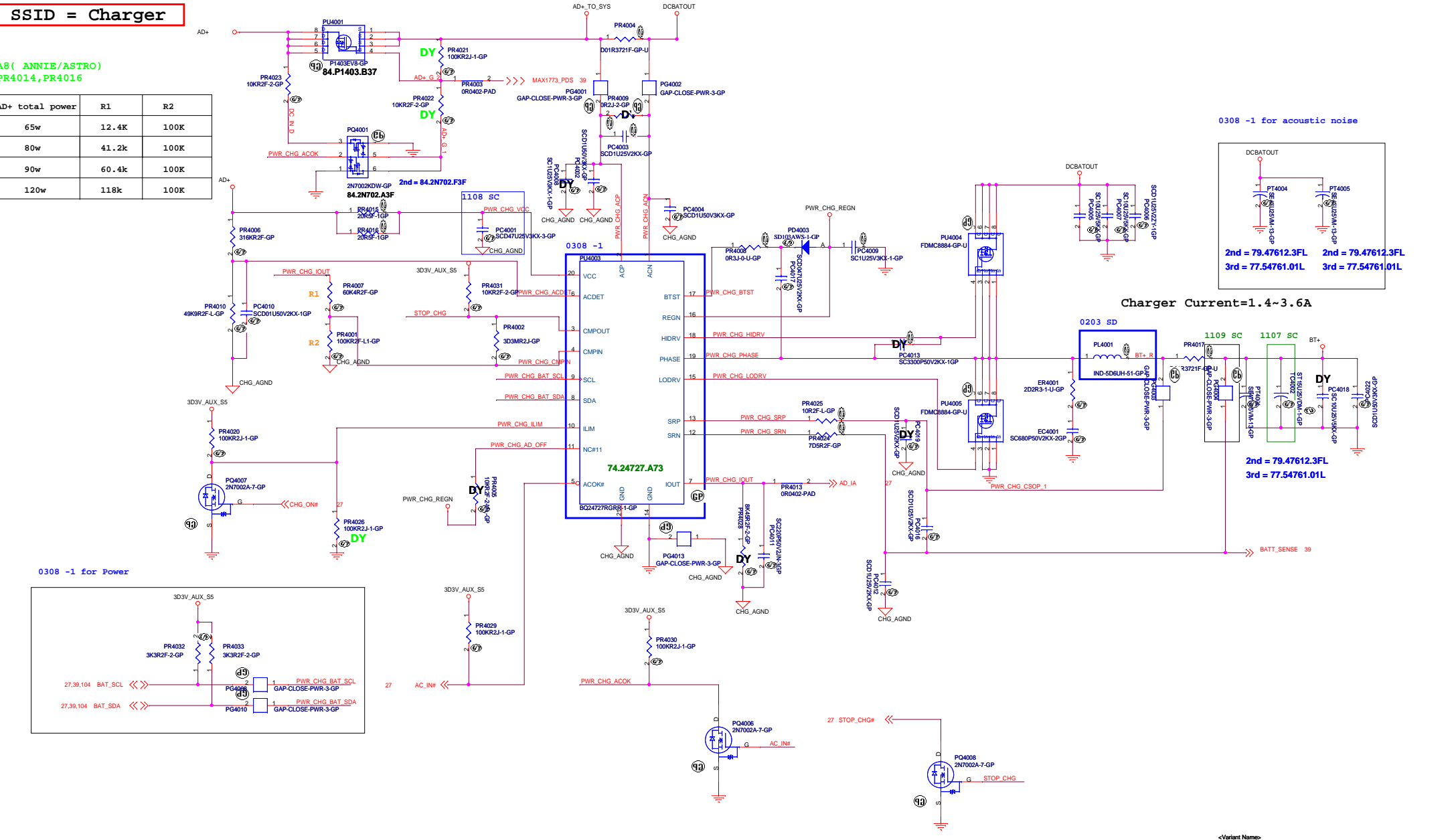


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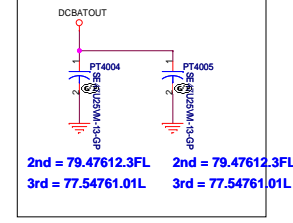
SSID = Charger

A8 (ANNIE/ASTRO)
PR4014, PR4016

AD+ total power	R1	R2
65w	1.2.4k	100K
80w	41.2k	100K
90w	60.4k	100K
120w	118k	100K

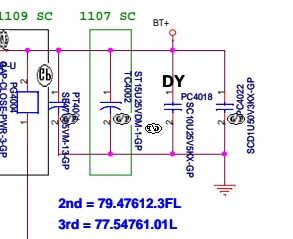


0308 -1 for acoustic noise



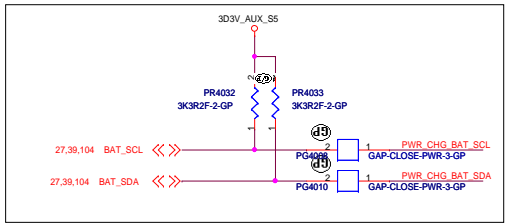
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3rd = 77.54761.01L 3rd = 77.54761.01L

Charger Current=1.4~3.6A



2nd = 79.47612.3FL 2nd = 79.47612.3FL
3rd = 77.54761.01L 3rd = 77.54761.01L

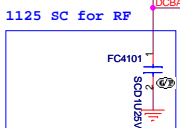
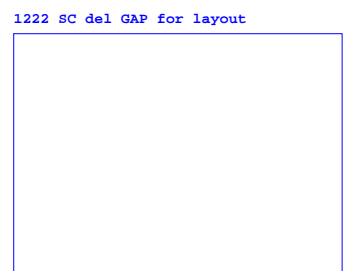
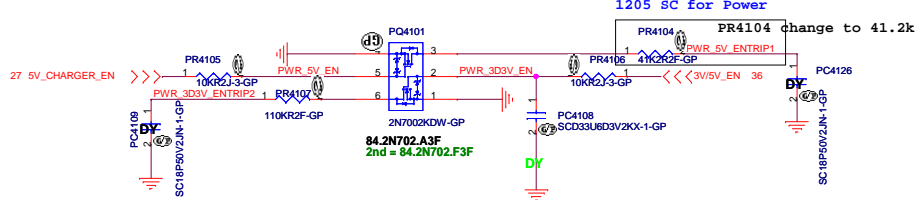
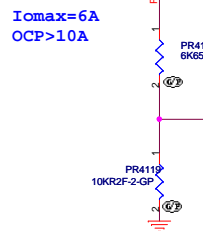
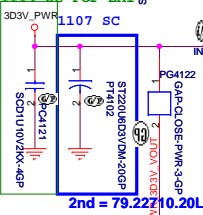
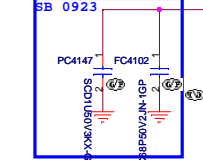
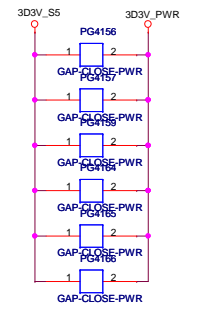
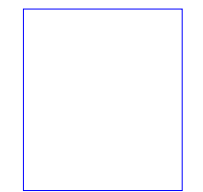
0308 -1 for Power



<Variant Name>

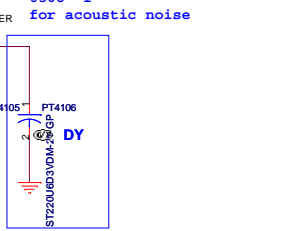
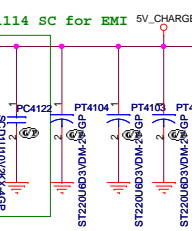
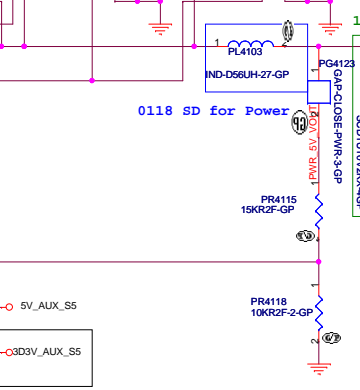
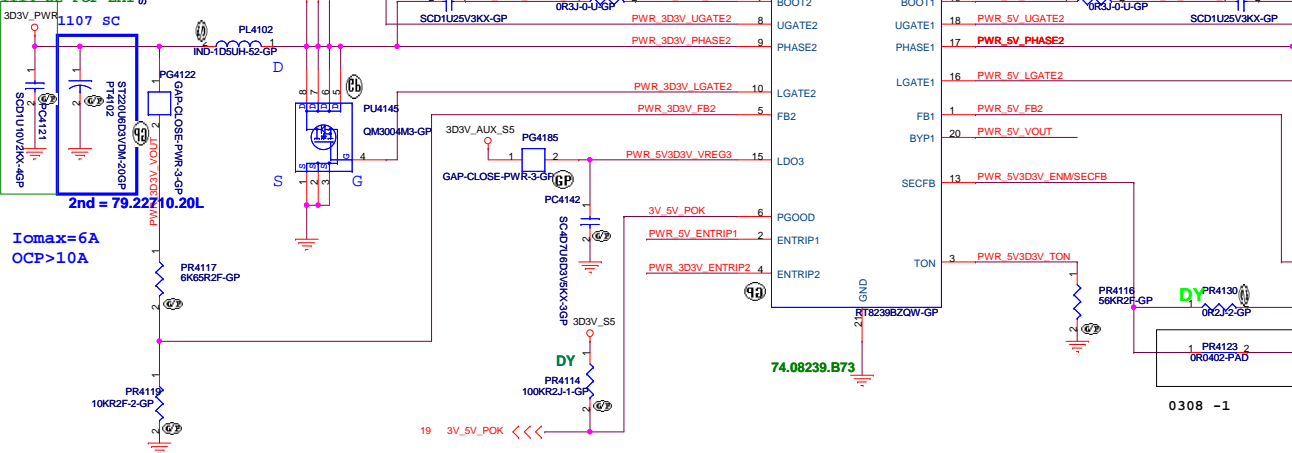
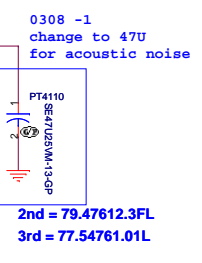
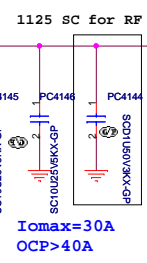
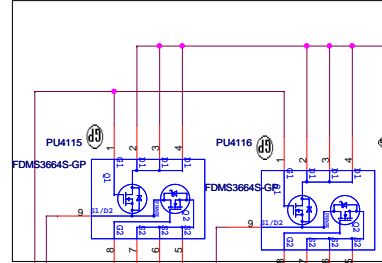
緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
File	CHARGER BQ24707A
Size	Document Number
Custom	BAD40 HC
Date	Thursday, April 12, 2012
Rev	1
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0315 -1
del close gap for Layout



Vz=3.9V
UVP Function
DCBATOUT<7.5V 3/5V disable

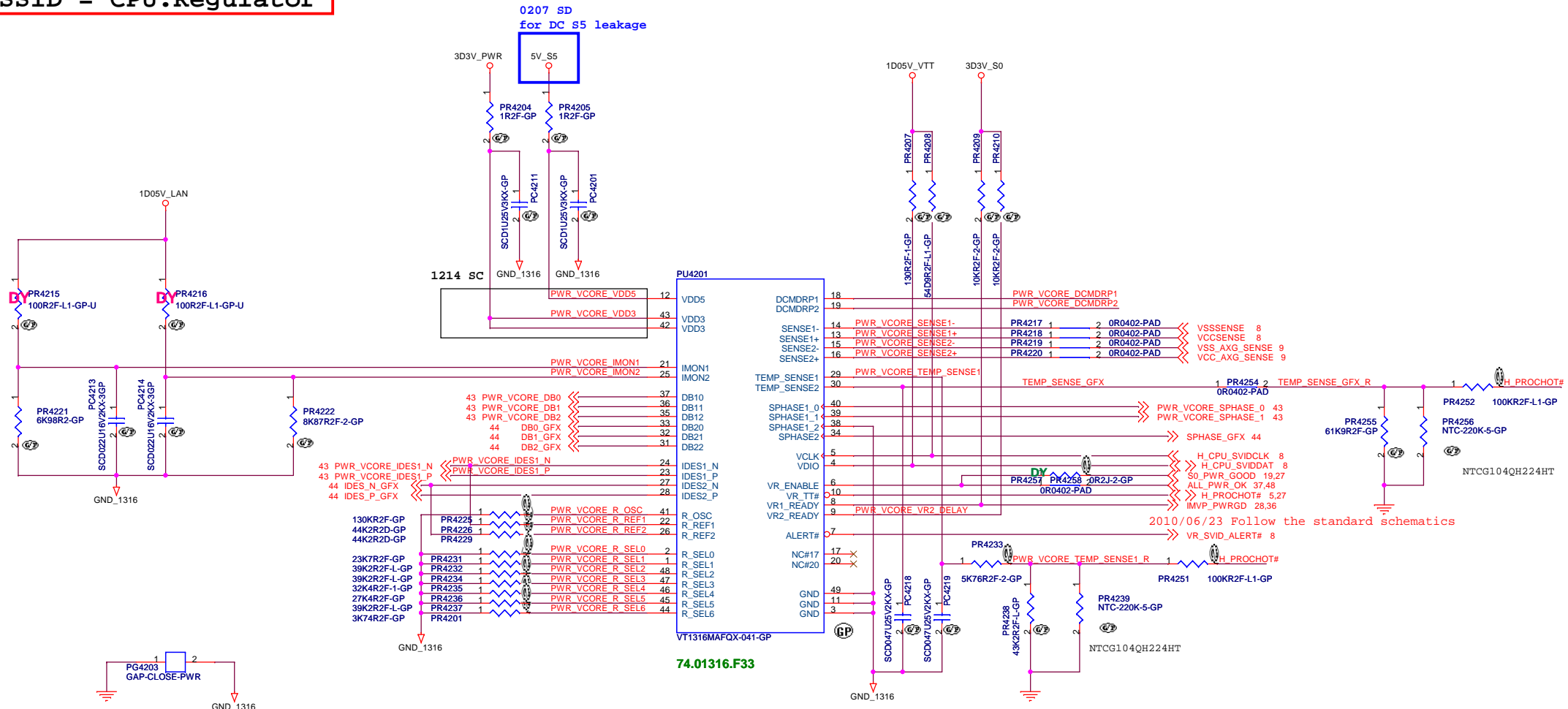
1212 SC change to 84.03664.037 for Power



<Variant Name>

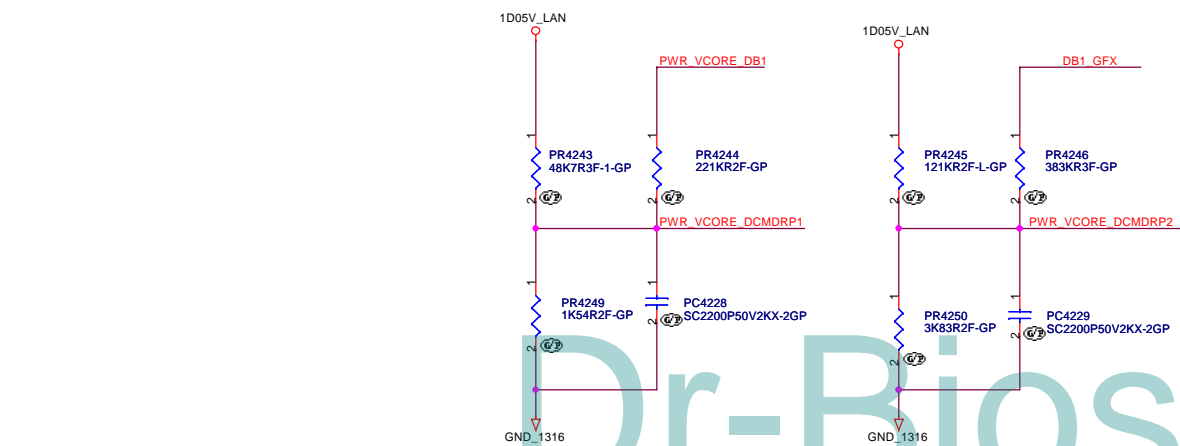
緯創資通 Wistron Corporation		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
File RT8329 5V/3D3V			
Size Custom	Document Number BAD40 HC	Rev 1	
Date: Thu8/09, April 12, 2012	Sheet 41	of 108	

SSID = CPU.Regulator



0207 SD
for DC S5 leakage

2010/06/23 Follow the standard schematics



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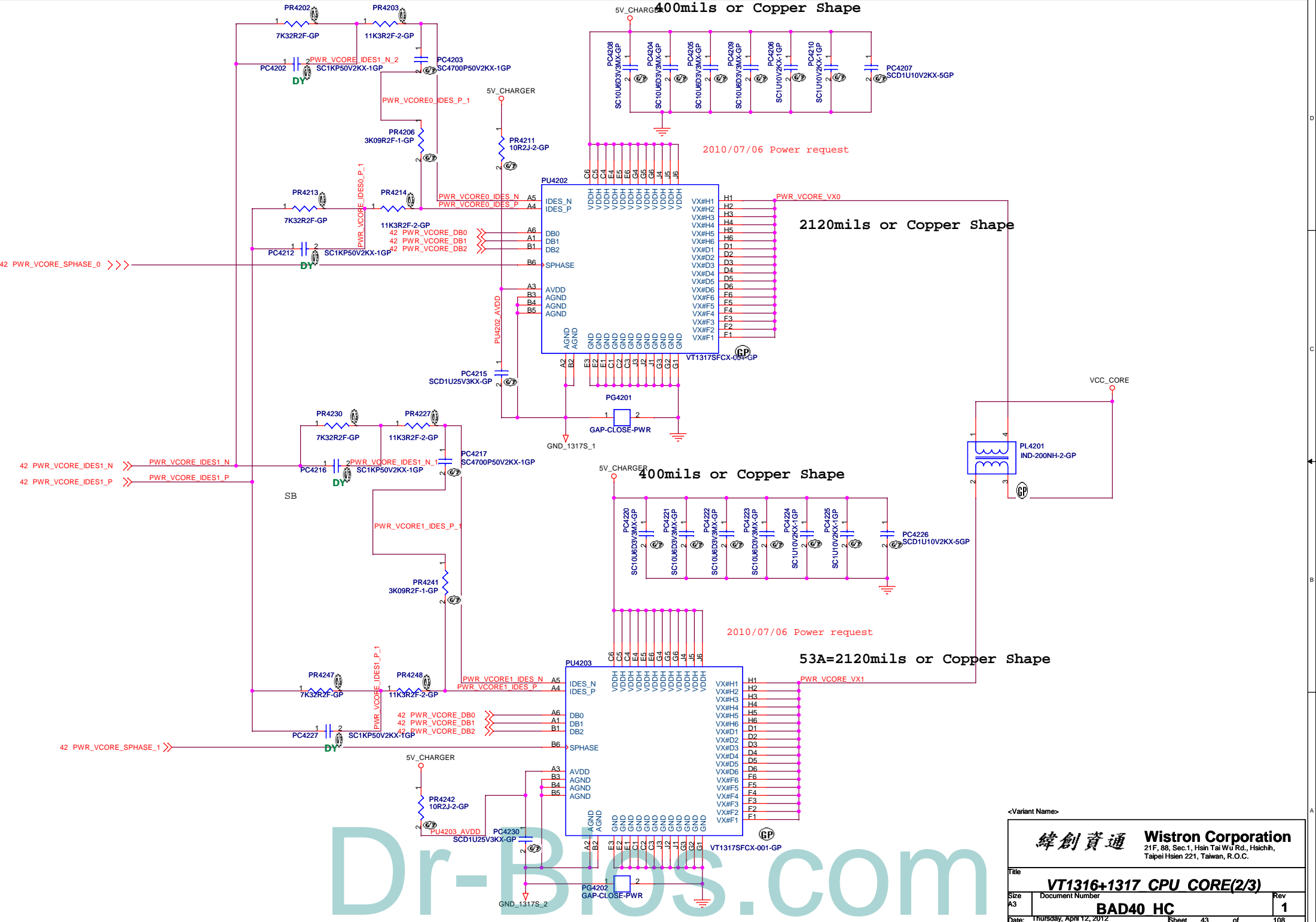
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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **VT1316+1317 CPU CORE(1/3)**

Size: A3 Document Number: **BAD40 HC** Rev: **1**

Date: Thursday, April 12, 2012 Sheet: 42 of 108



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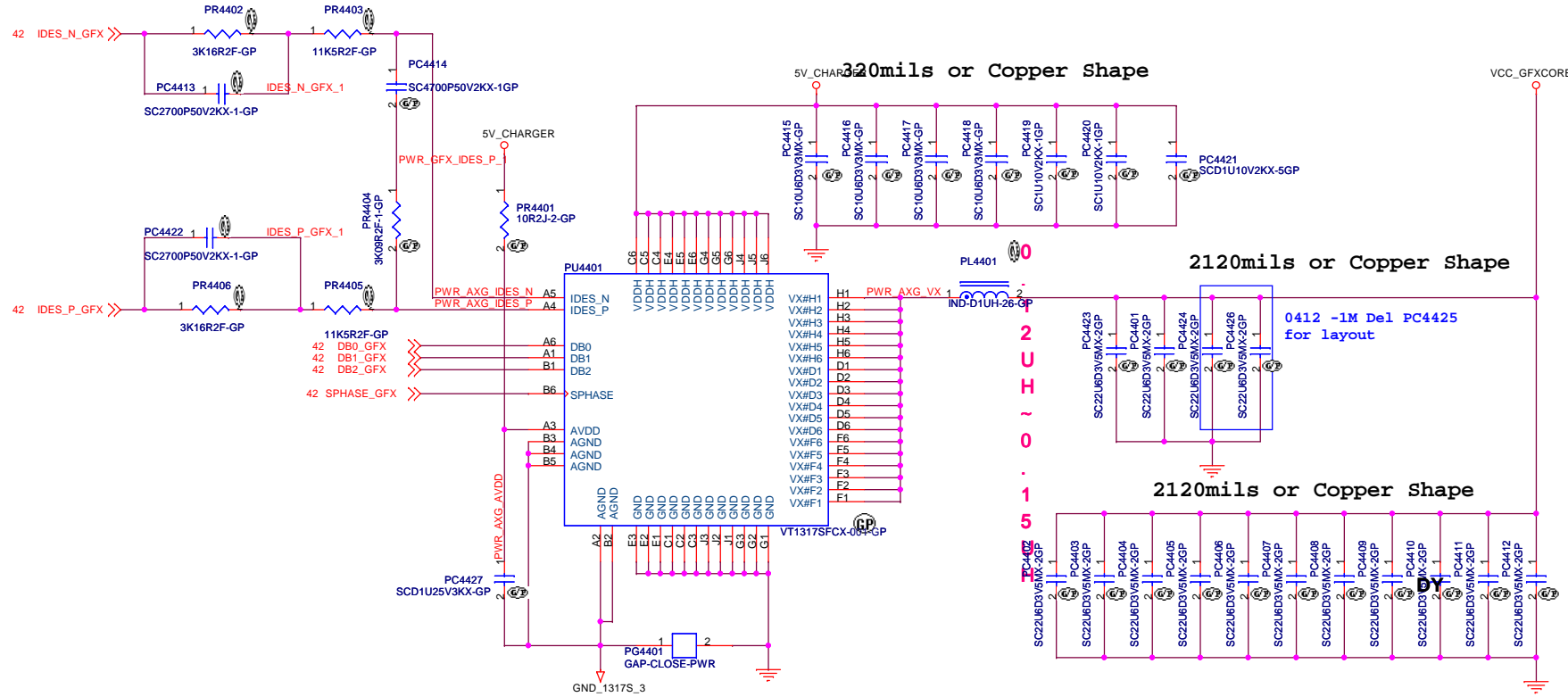
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緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **VT1316+1317 CPU CORE(2/3)**

Size A3 Document Number: **BAD40 HC** Rev: **1**

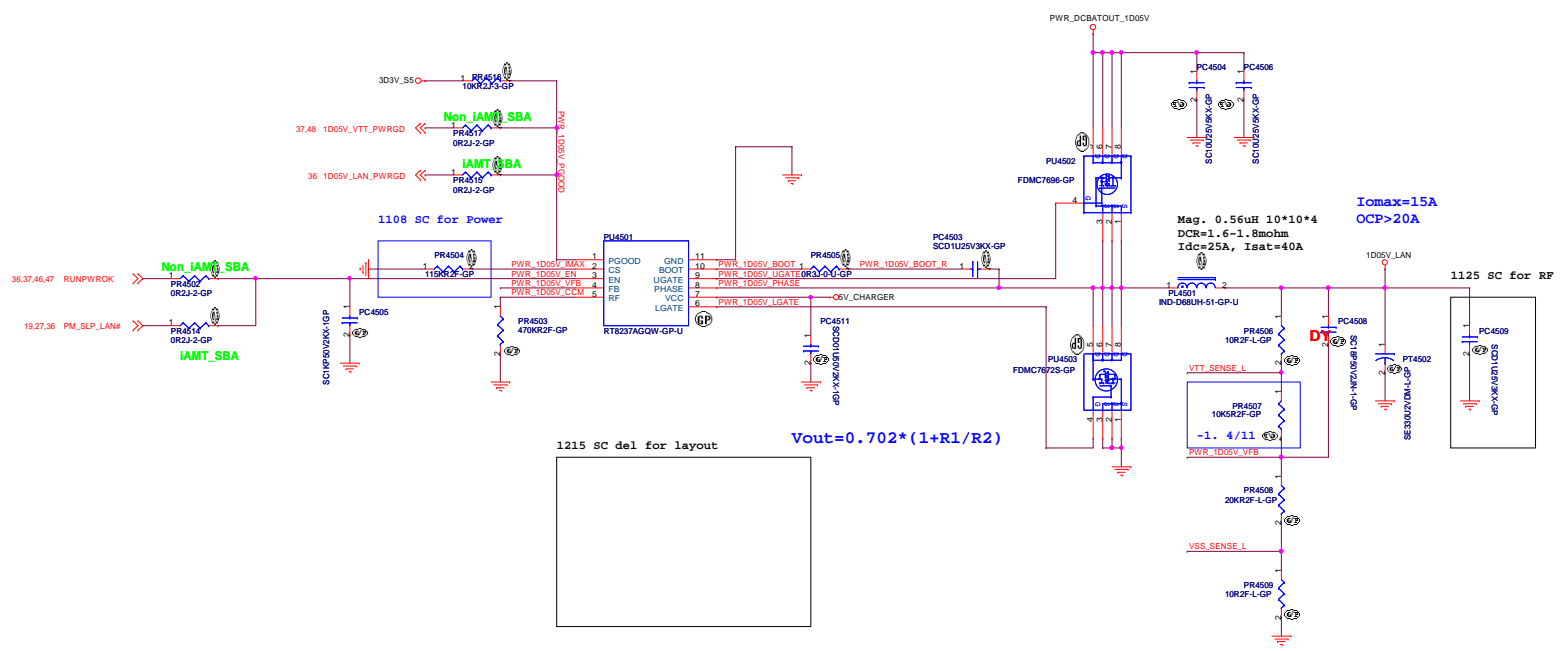
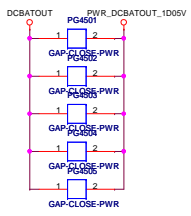
Date: Thursday, April 12, 2012 Sheet 43 of 108



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<Variant Name>		
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
VT1316+1317 CPU CORE(3/3)		
Size	Document Number	Rev
A3	BAD40 HC	1
Date:	Thursday, April 12, 2012	Sheet 44 of 108

RT8237 for 1D05V



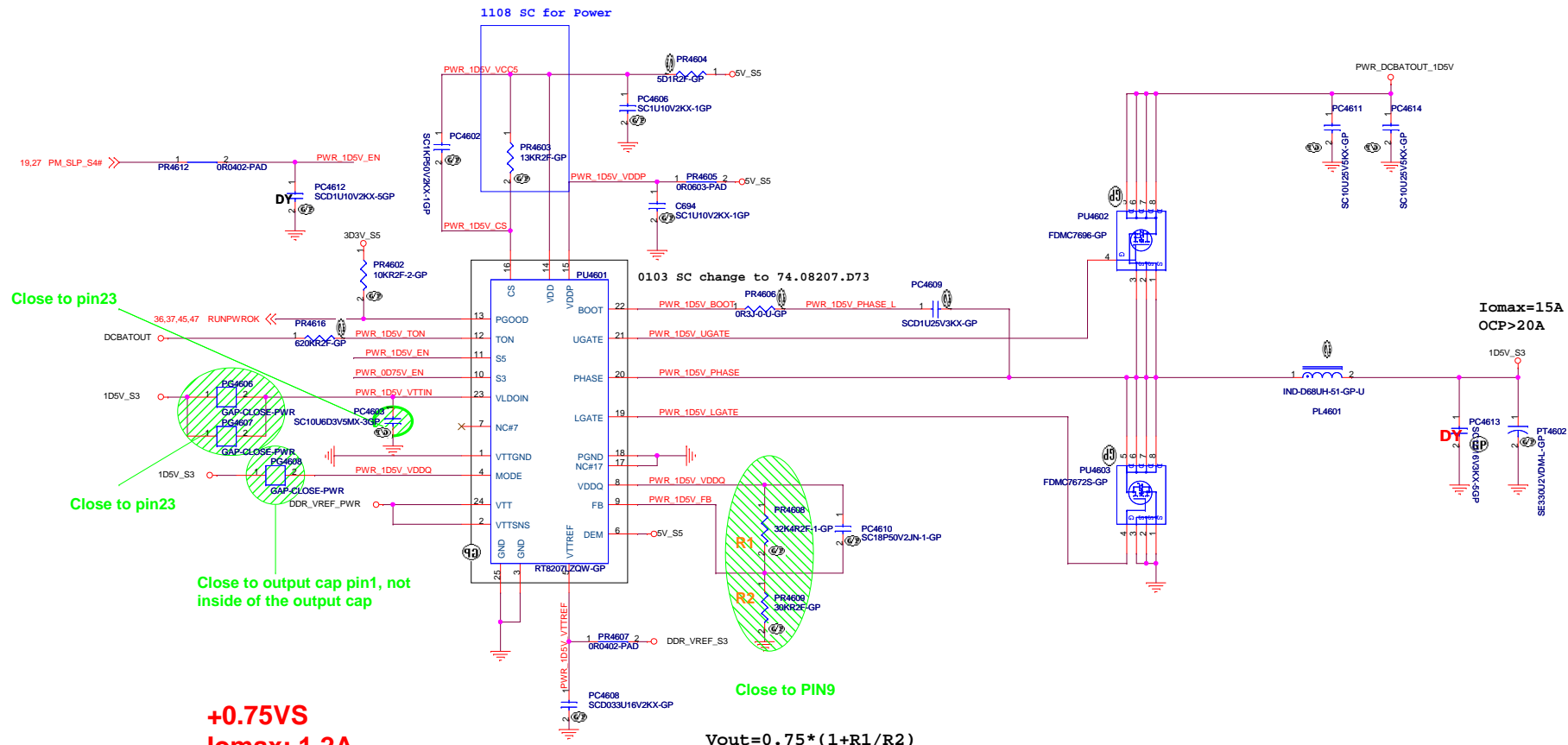
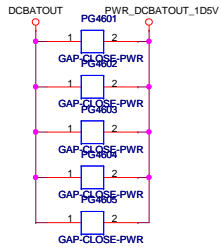
1215 SC del for layout

$$V_{out} = 0.702 * (1 + R1/R2)$$

I_{omax}=15A
OCP>20A

1125 SC for RF

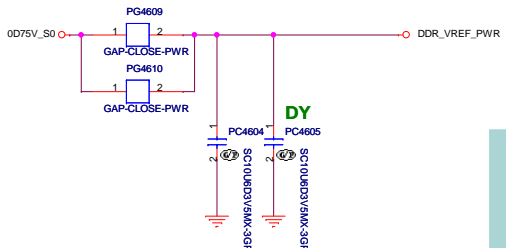
RT8207L for 1D5V



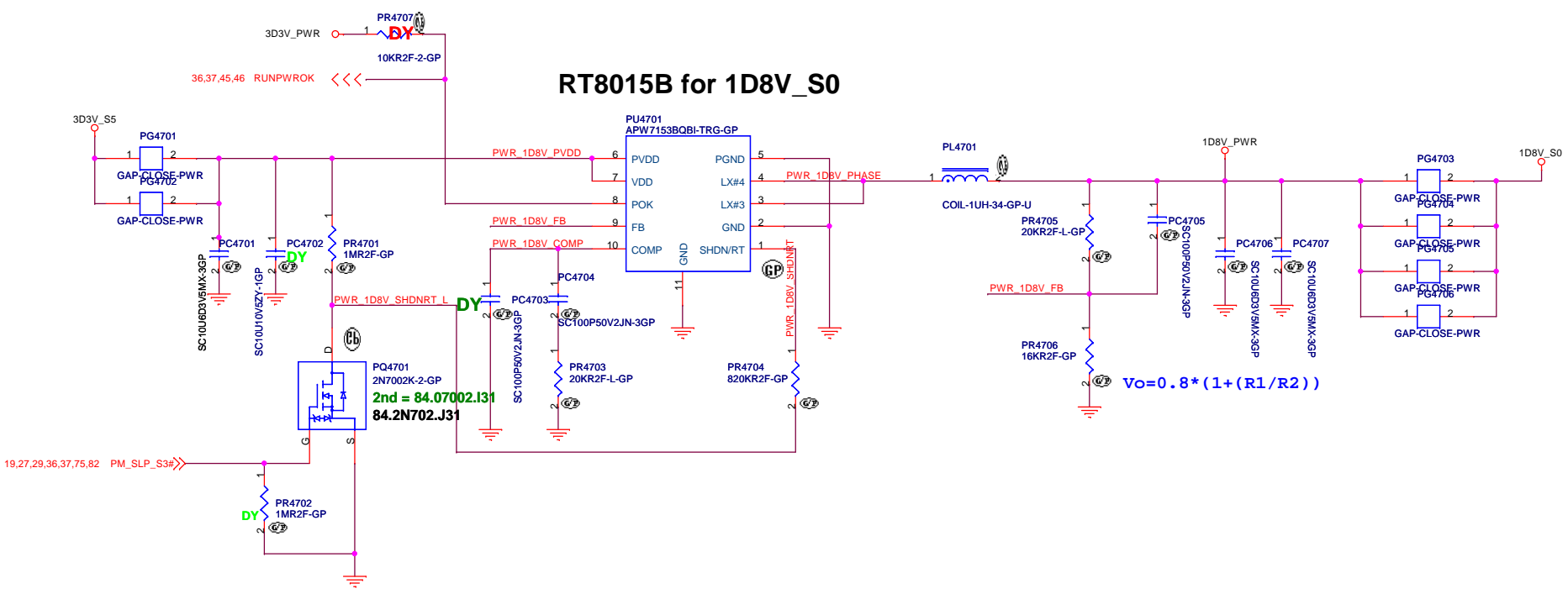
I_{max}=15A
OCP>20A

+0.75VS
I_{omax}: 1.2A

$$V_{out} = 0.75 * (1 + R1/R2)$$



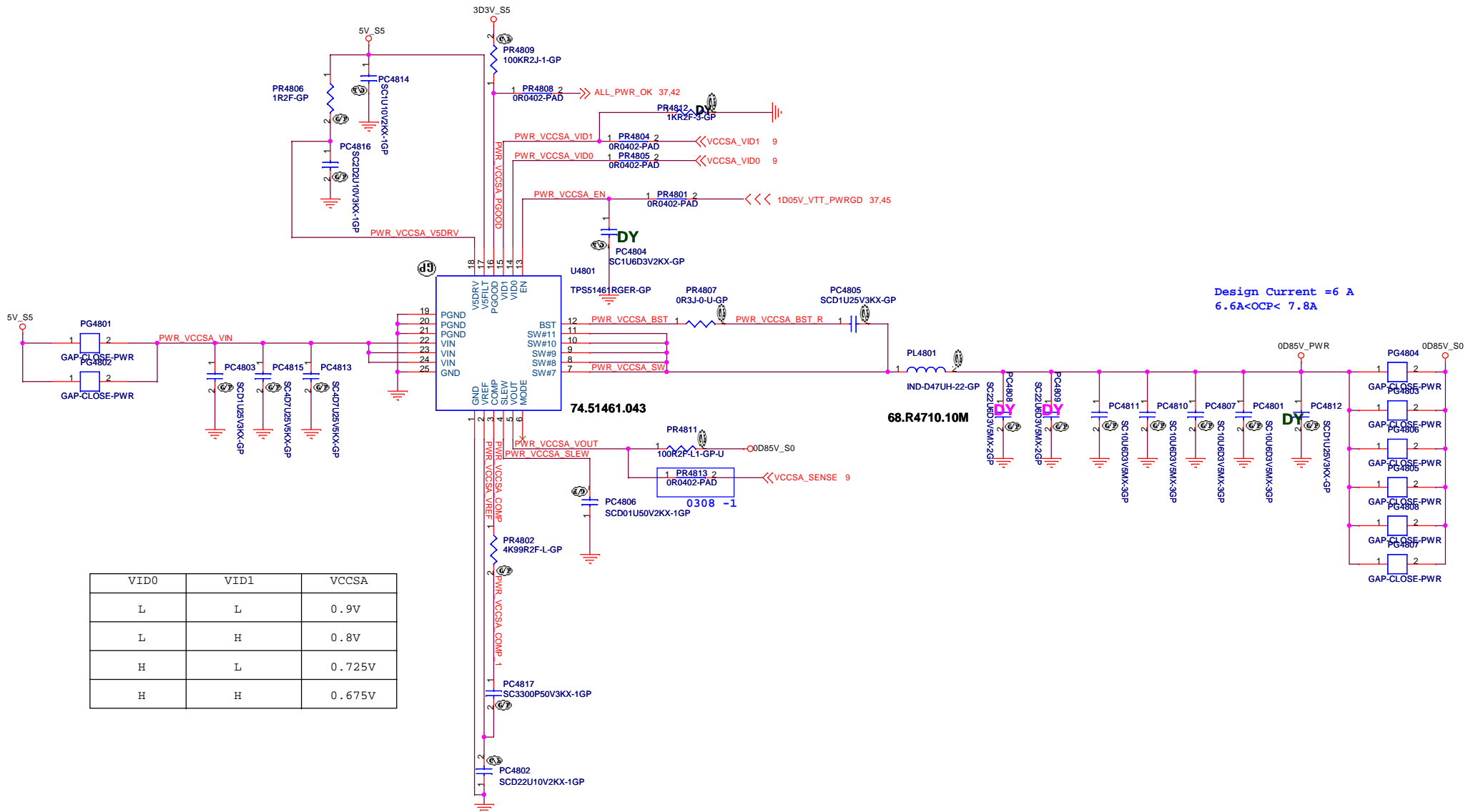
SSID = PWR.Plane.Regulator_1p8v



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<Variant Name>		
緯創資通 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title DC CONVERTER 1D8V(RT8015A)		
Size A3	Document Number BAD40_HC	Rev 1
Date: Thursday, April 12, 2012	Sheet 47 of 108	

TPS51461 for VCCSA



Design Current = 6 A
6.6A < OCP < 7.8A

VID0	VID1	VCCSA
L	L	0.9V
L	H	0.8V
H	L	0.725V
H	H	0.675V

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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

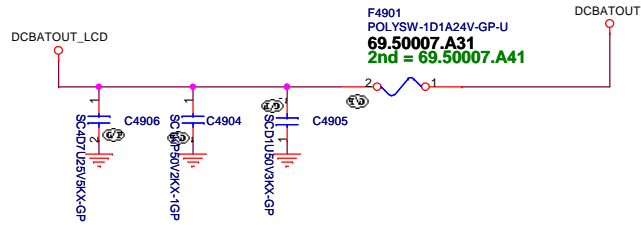
Title: **DC CONVERTER VCCSA(TPS51461)**

Size A3 Document Number **BAD40_HC** Rev **1**

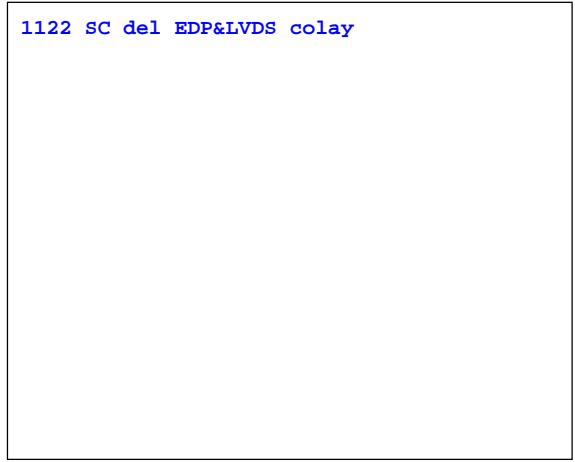
Date: Thursday, April 12, 2012 Sheet 48 of 108

SSID = VIDEO

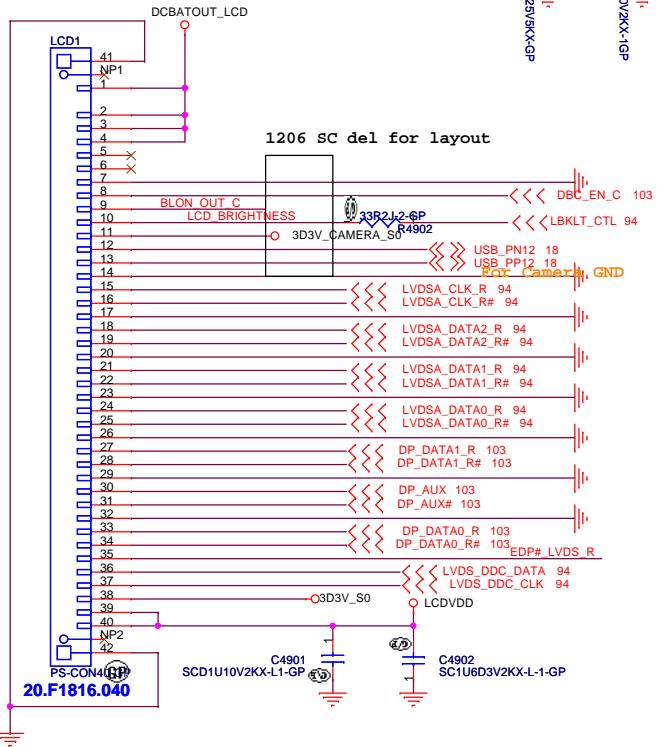
INVERTER POWER



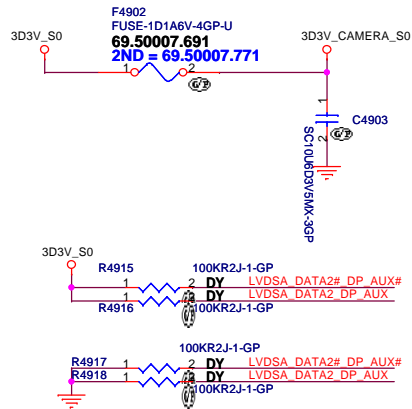
1122 SC del EDP&LVDS colay



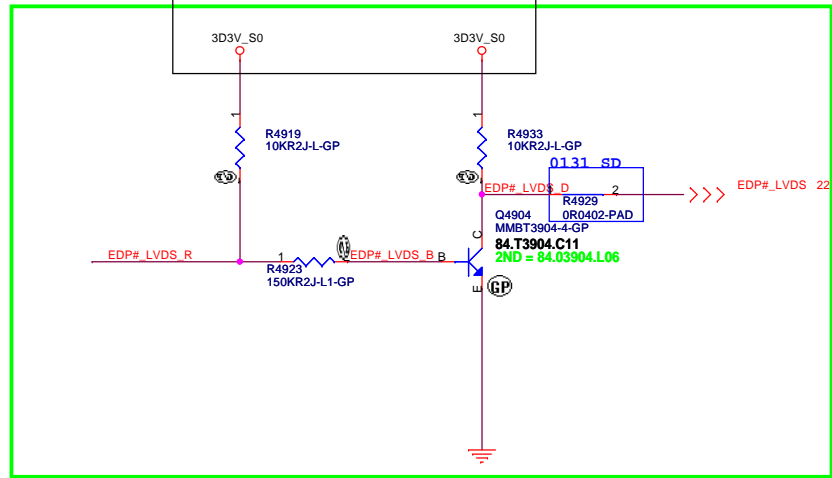
LVDS CONNECTOR



Camera Power

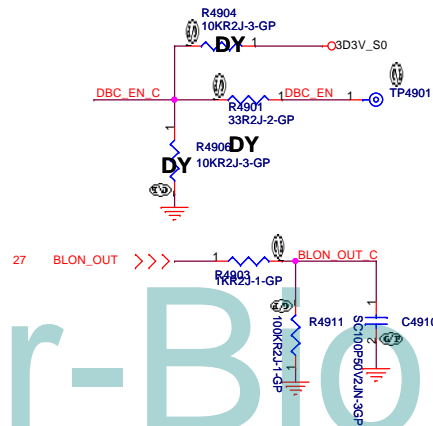
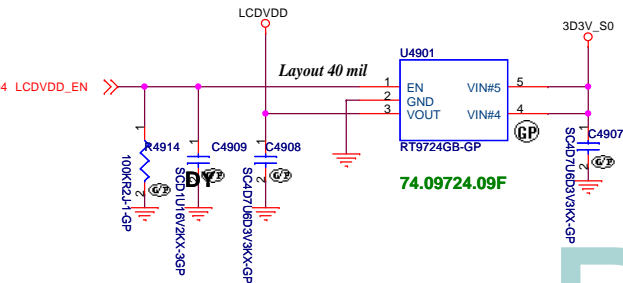


1121 SC



SSID = VIDEO

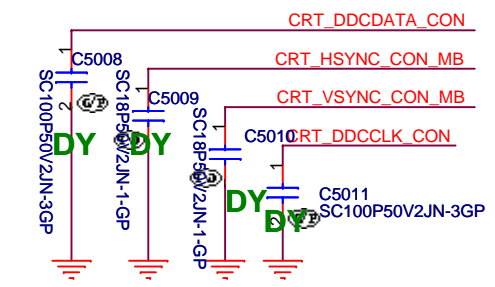
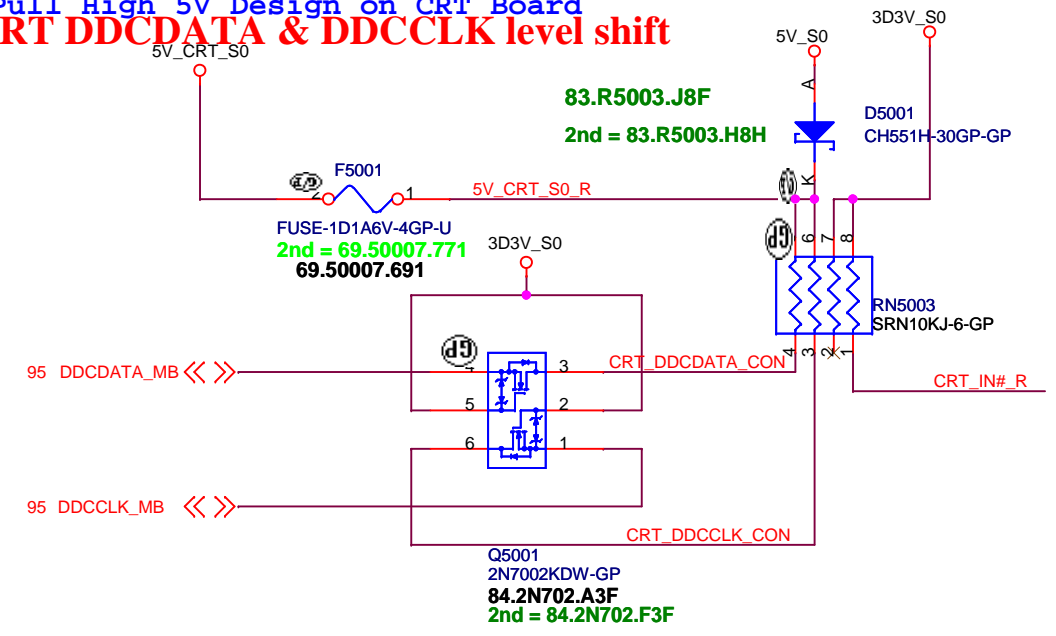
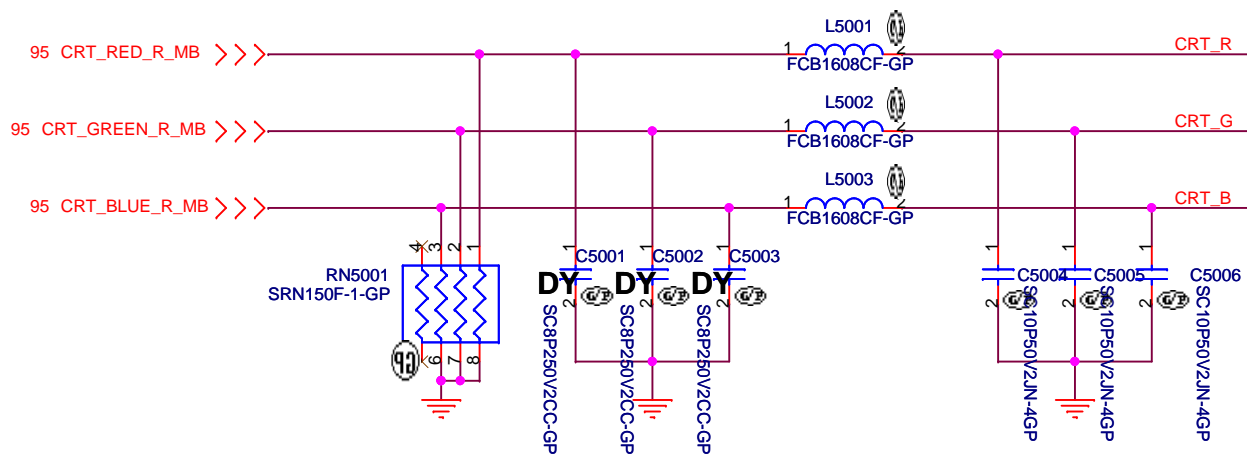
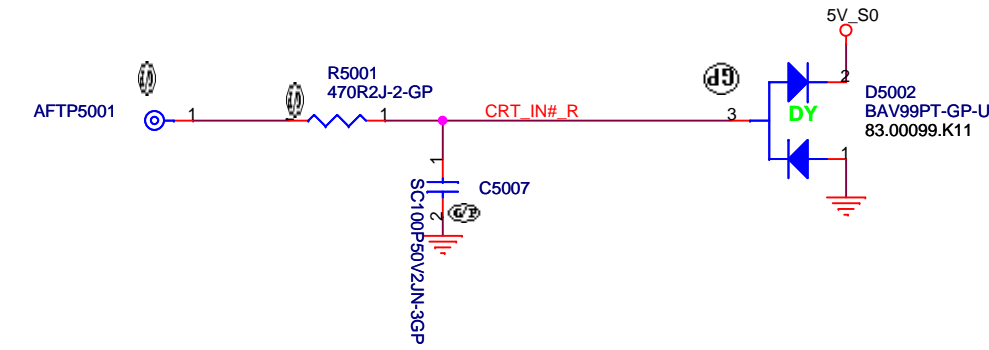
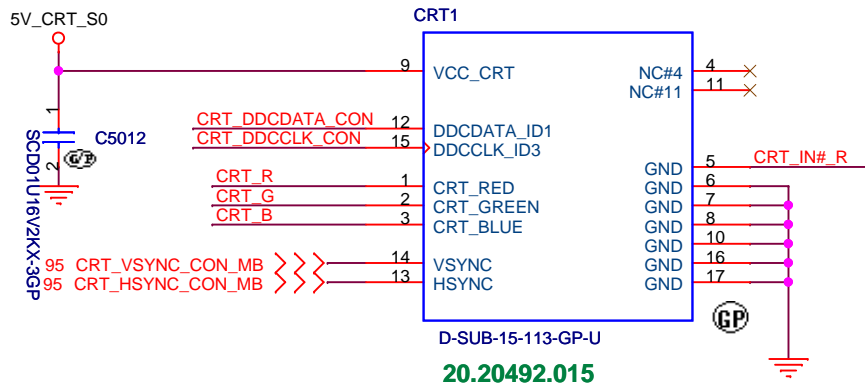
LCD POWER for ANNIE



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-Variant Name-		緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
File	LCD Connector		
Size A3	Document Number	BAD40 HC	
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Rev	1		

Pull High 5V Design on CRT Board CRT DDCDATA & DDCCLK level shift

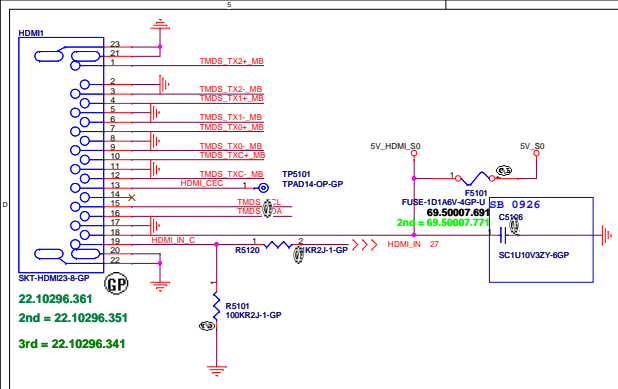


<Variant Name>

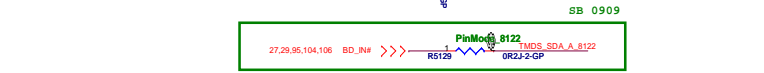
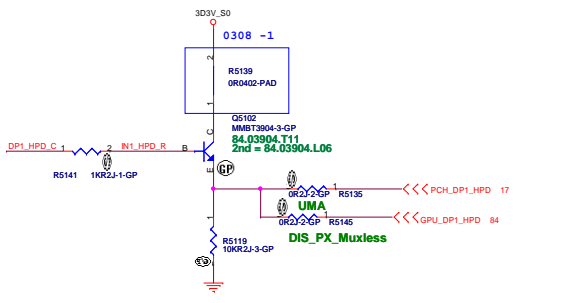
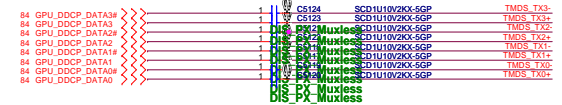
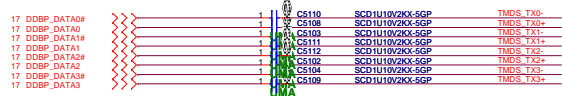
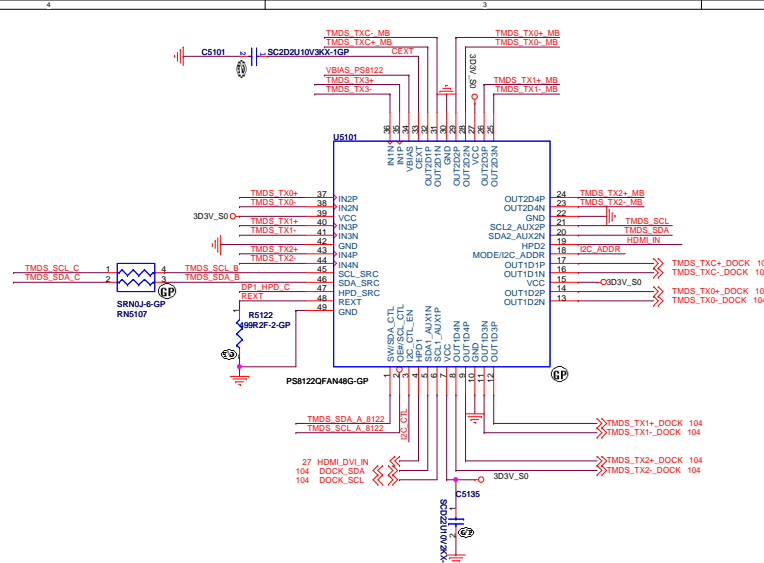
	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
--	---

Title		CRT Connector
Size	Document Number	Rev
A4	BAD40 HC	1
Date	Thursday, April 12, 2012	Sheet 50 of 108

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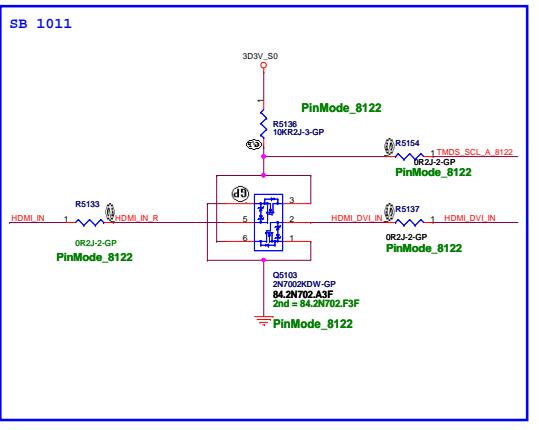
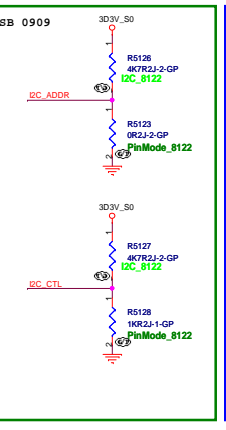
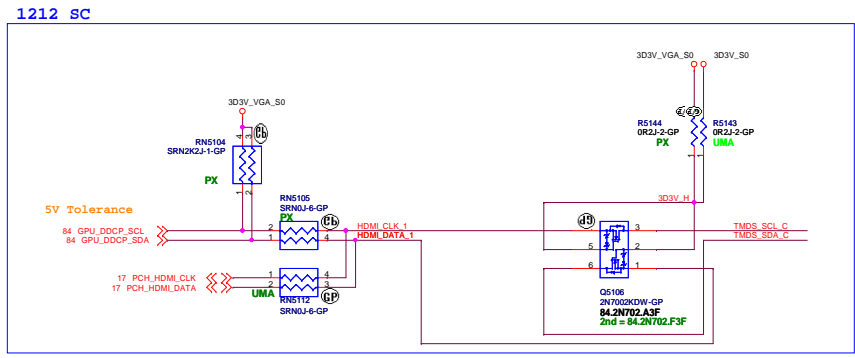


22.10296.361
2nd = 22.10296.351
3rd = 22.10296.341

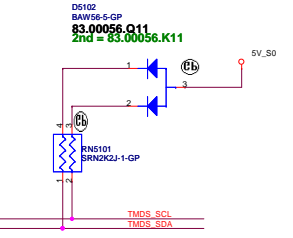
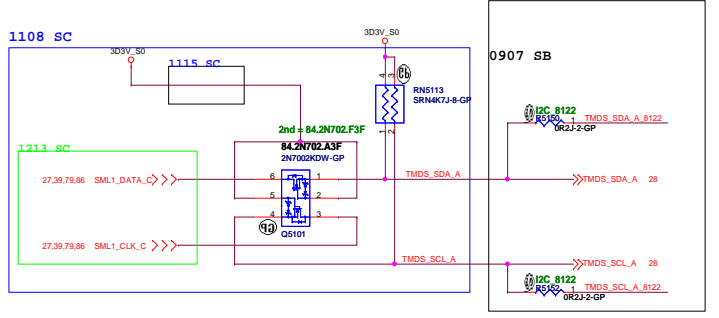


SW	H	L
	OUT2	OUT1

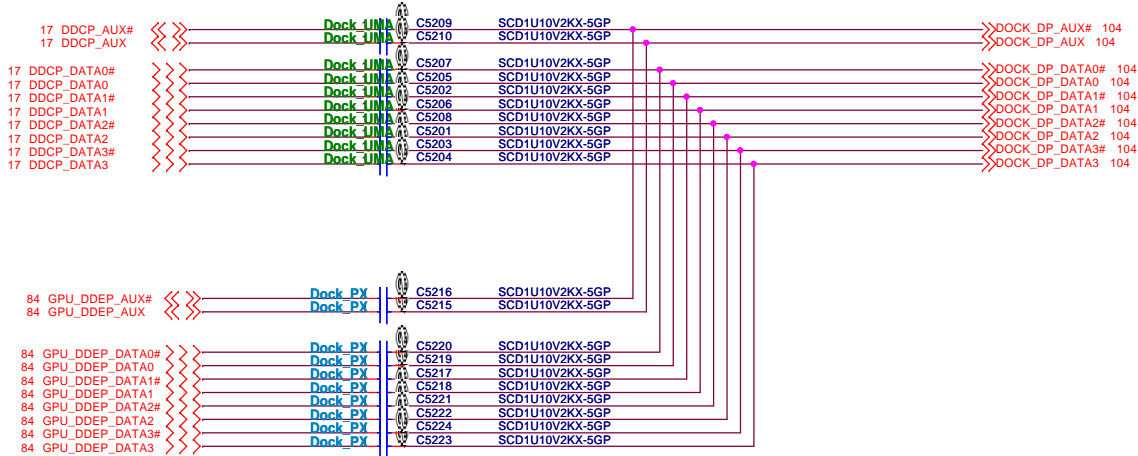
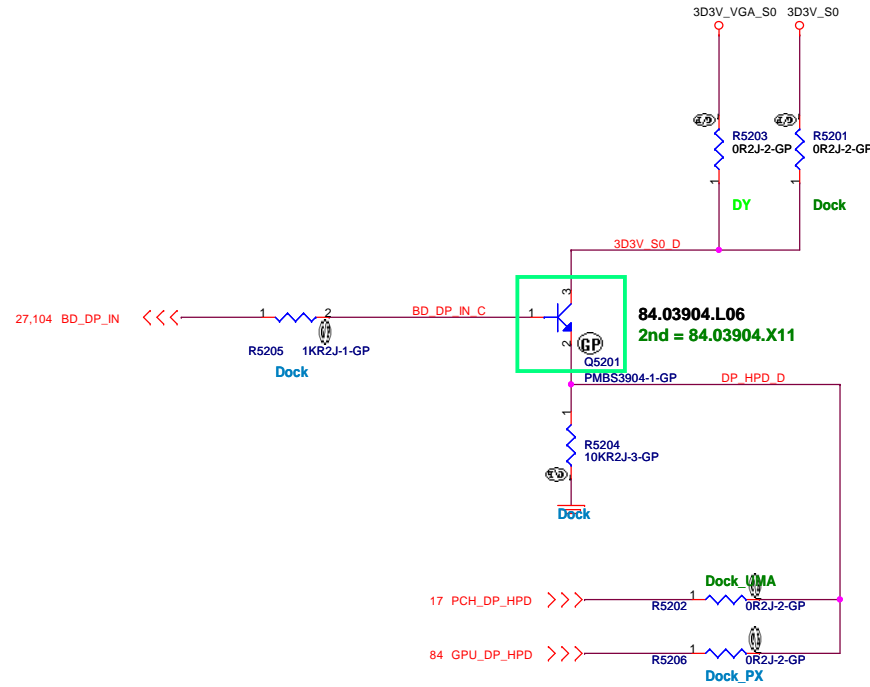
VBias
For DC coupled HDMI/DVI input, connect to VCC.
For AC coupled HDMI/DVI input, connect to either VCC or GND.



I2C_CTL_EN	LOW or NC	LOW or NC	HIGH	HIGH
MODE / I2C_ADDR	LOW	HIGH	LOW	HIGH
	PinMode HDMI/DVI	PinMode DP	I2C addresses 9E/9F	I2C addresses BE/BF



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HR PX

Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Display Port	
Title Display Port	Document Number BAD40_HC
Size A3	Rev 1
Date: Thursday, April 12, 2012	Sheet 52 of 108

(Blanking)

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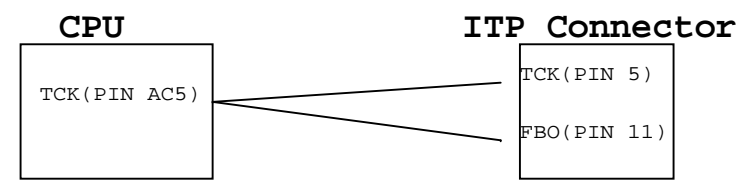
<Variant Name>

緯創資通			Wistron Corporation		
			21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
Reserved					
Size	Document Number				Rev
A4	BAD40 HC				1
Date:	Thursday, April 12, 2012			Sheet	54 of 108

SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



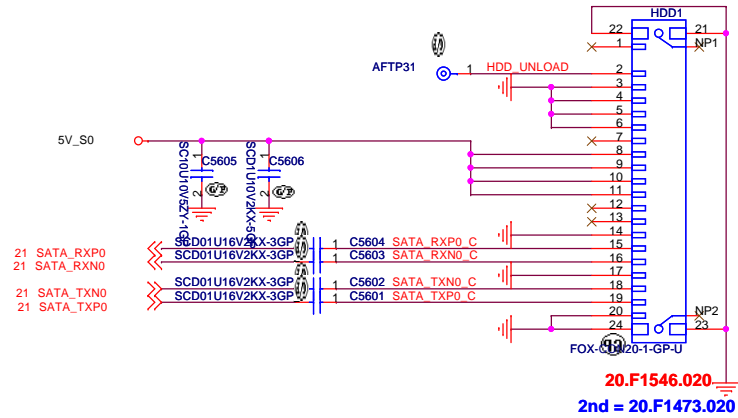
Dr-Bios.com

<Variant Name>

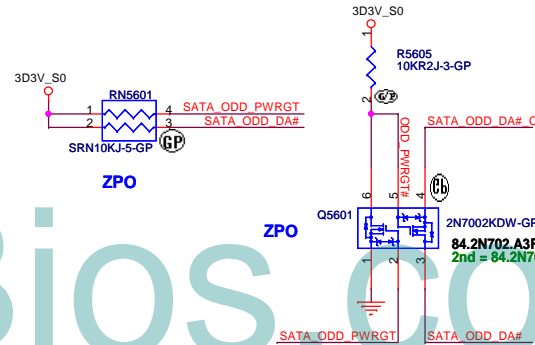
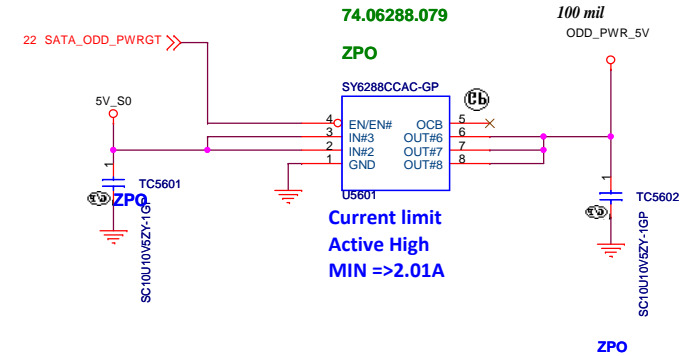
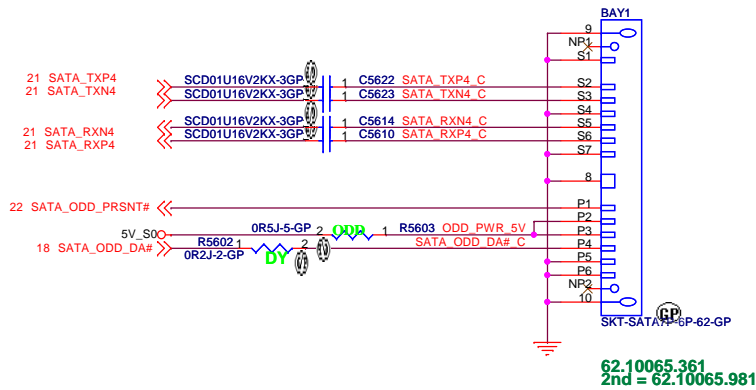
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
ITP		
Size	Document Number	Rev
A4	BAD40 HC	1
Date:	Thursday, April 12, 2012	Sheet 55 of 108

SATA HDD Connector



ODD Connector



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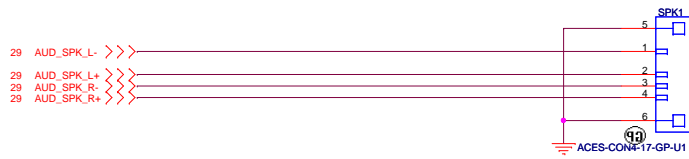
reserved

<Variant Name>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
E-SATA/USB CHARGER			
Size	Document Number		Rev
Custom	BAD40 HC		1
Date:	Thursday, April 12, 2012	Sheet 57	of 108

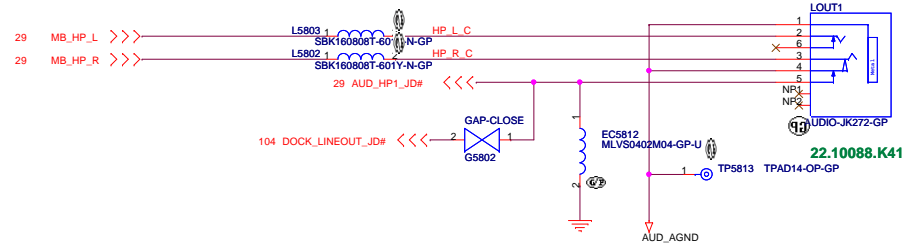
Dr-Bios.com

Speaker Connector



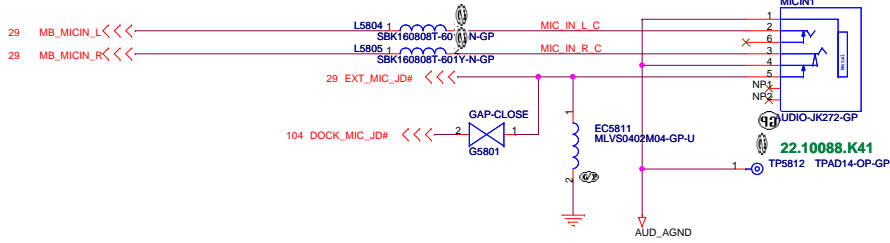
20.F1621.004
2nd = 20.F1937.004

LINE OUT



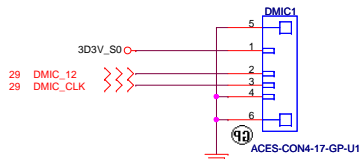
22.10088.K41

MIC IN



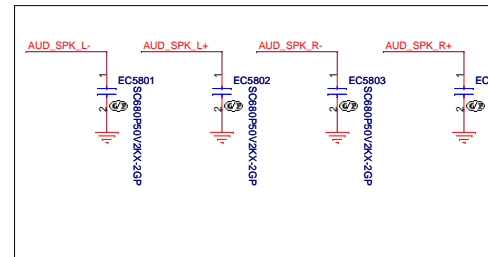
22.10088.K41

Internal Microphone

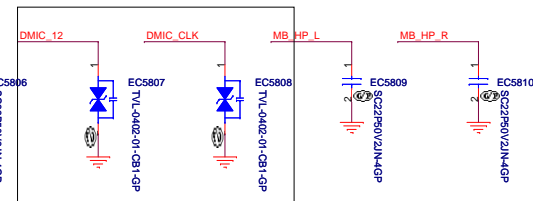
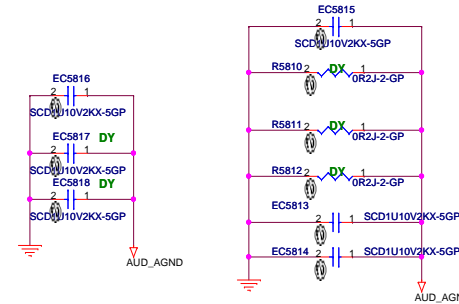


20.F1621.004
2nd = 20.F1937.004

0308 -1 for EMI



1128 SC



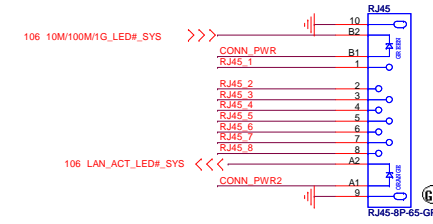
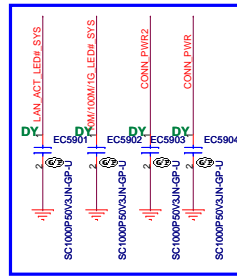
Dr-Bios.com

<Variant Name>

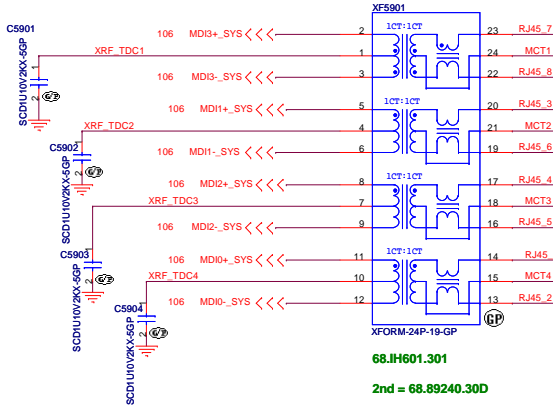
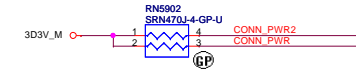
<p>緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taippei Hsien 221, Taiwan, R.O.C.</p>		
<p>Title Audio Jack</p>		
Size Custom	Document Number BAD40 HC	Rev 1
Date: Thursday, April 12, 2012	Sheet 58 of 108	

SSID = LOM

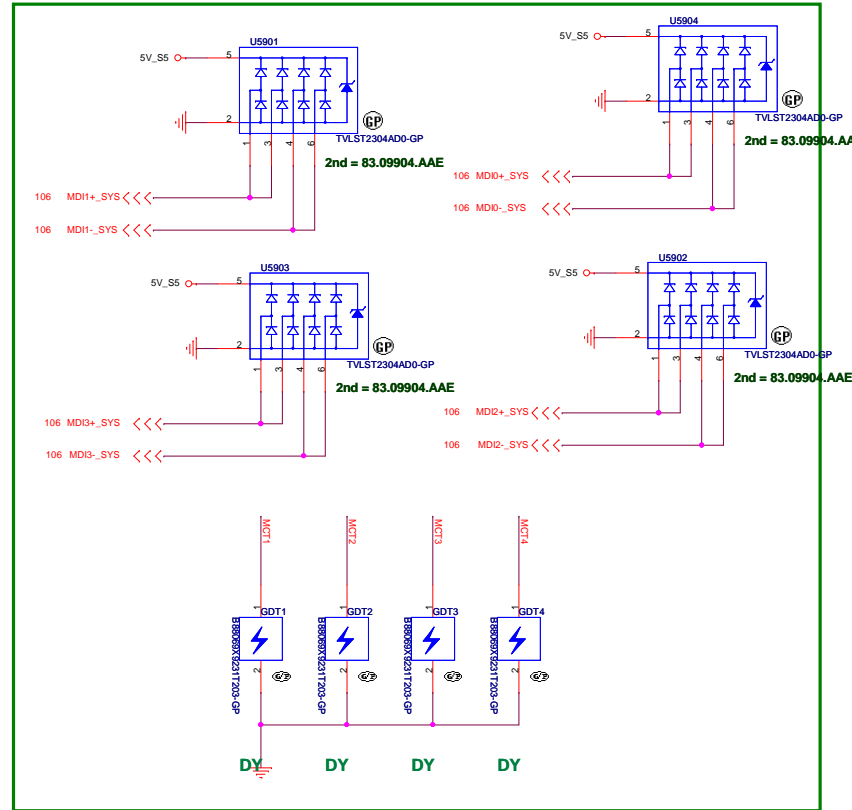
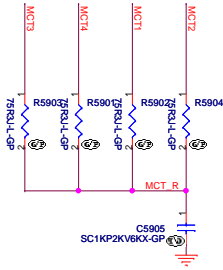
SB 0922



22.10177.J21
2nd = 22.10177.J51



68.IH601.301
2nd = 68.89240.30D



Title		Wistron Corporation	
Size		21F, 8B, Sec 1, Han Ta Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Date		Thursday, April 12, 2012	
Document Number		LAN CONNECTOR	
Sheet		59 of 108	
Rev		1	
Customer		BAD40 HC	

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SPI FLASH ROM (8M byte) for PCH

SPI ROM Equal length need to less than 500mil

PCH and EC length less than 6.5 inch

Cougar Point Chipset

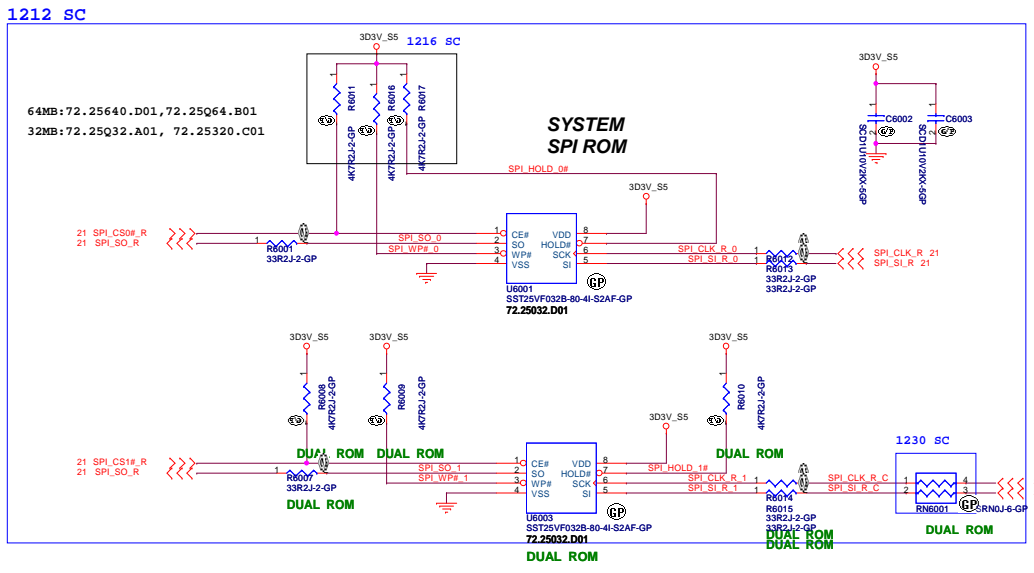
Control

NPCE795x
EC

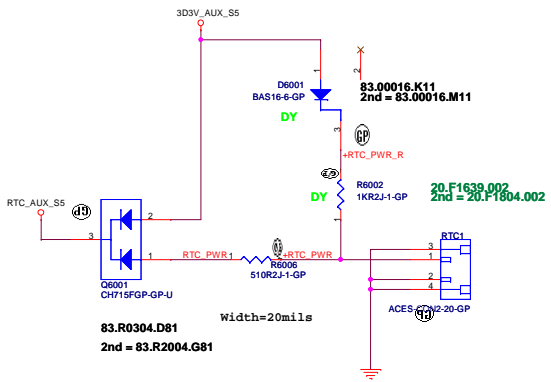
On-Chip
96K RAM

SPI Flash

SSID = Flash.ROM

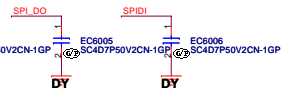
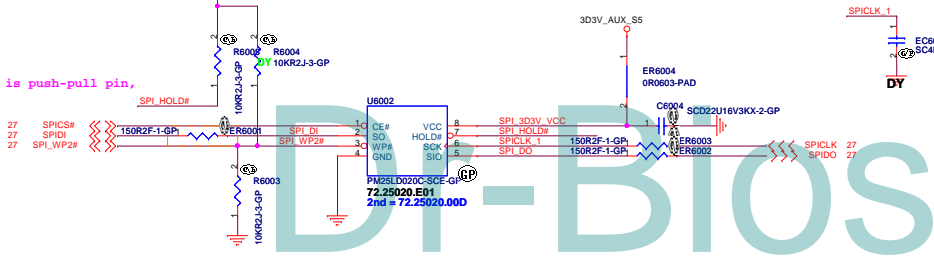


SSID = RBATT



**EC BIOS Flash ROM
256KB**

for ENE FAE suggest, SPICs# is push-pull pin,
don't need to pull high



HR PX

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu,
Taipei Hsin 221, Taiwan, R.O.C.

Title	Flash/RTC		Rev
Size	Document Number	BAD40_HC	1
Customer	Date: Thursday, April 12, 2012		Sheet 60 of 108

SSID = USB

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

USB Power SW

Size
A4

Document Number

BAD40 HC

Rev
1

Date: Thursday, April 12, 2012

Sheet 61 of 108

Dr-Bios.com

Dr-Bios.com

<Variant Name>		
緯創資通		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
USB 3.0 Port		
Size	Document Number	Rev
A3	BAD40_HC	1
Date:	Thursday, April 12, 2012	Sheet 62 of 108

5 4 3 2 1

SSID = User.Interface
Bluetooth Module conn.

reserved 1216

Dr-Bios.com

<Variant Name>

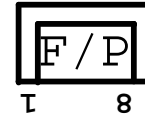
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **Bluetooth**

Size A4 Document Number **BAD40 HC** Rev **1**

Date: Thursday, April 12, 2012 Sheet 63 of 108

Finger printer



<Variant Name>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

RESERVED

Size
A4

Document Number

BAD40 HC

Rev
1

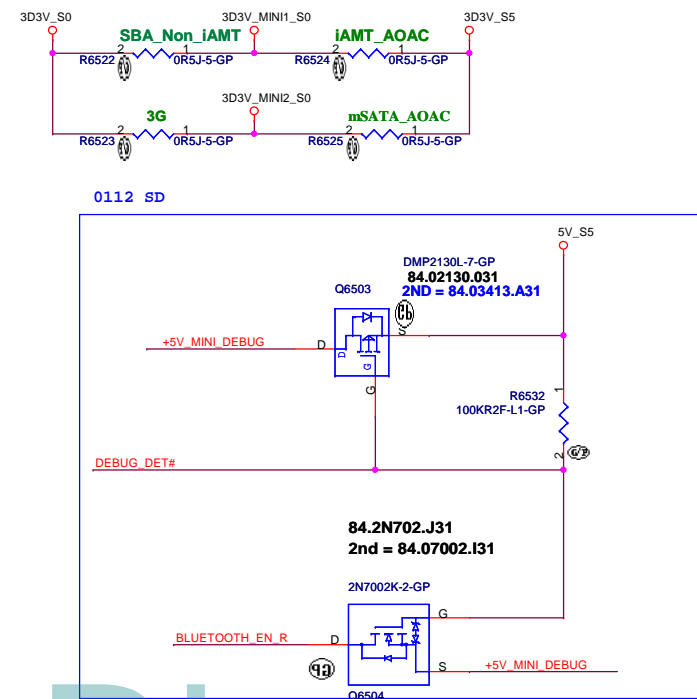
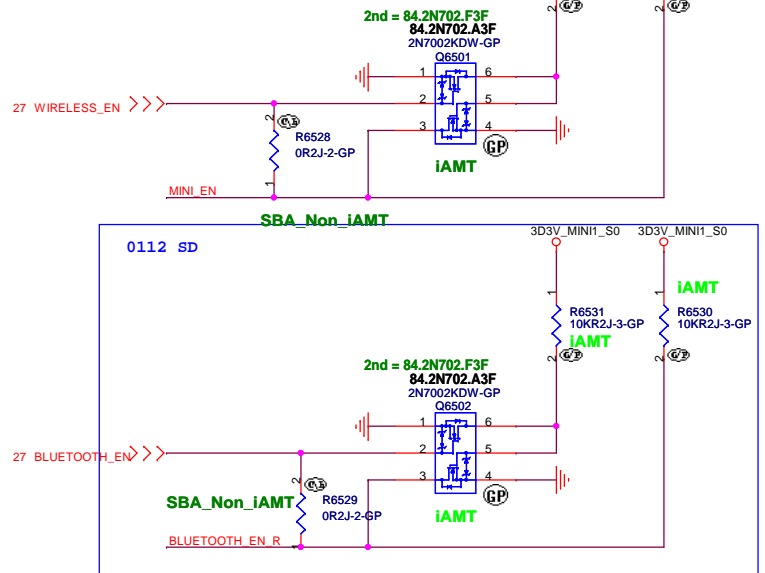
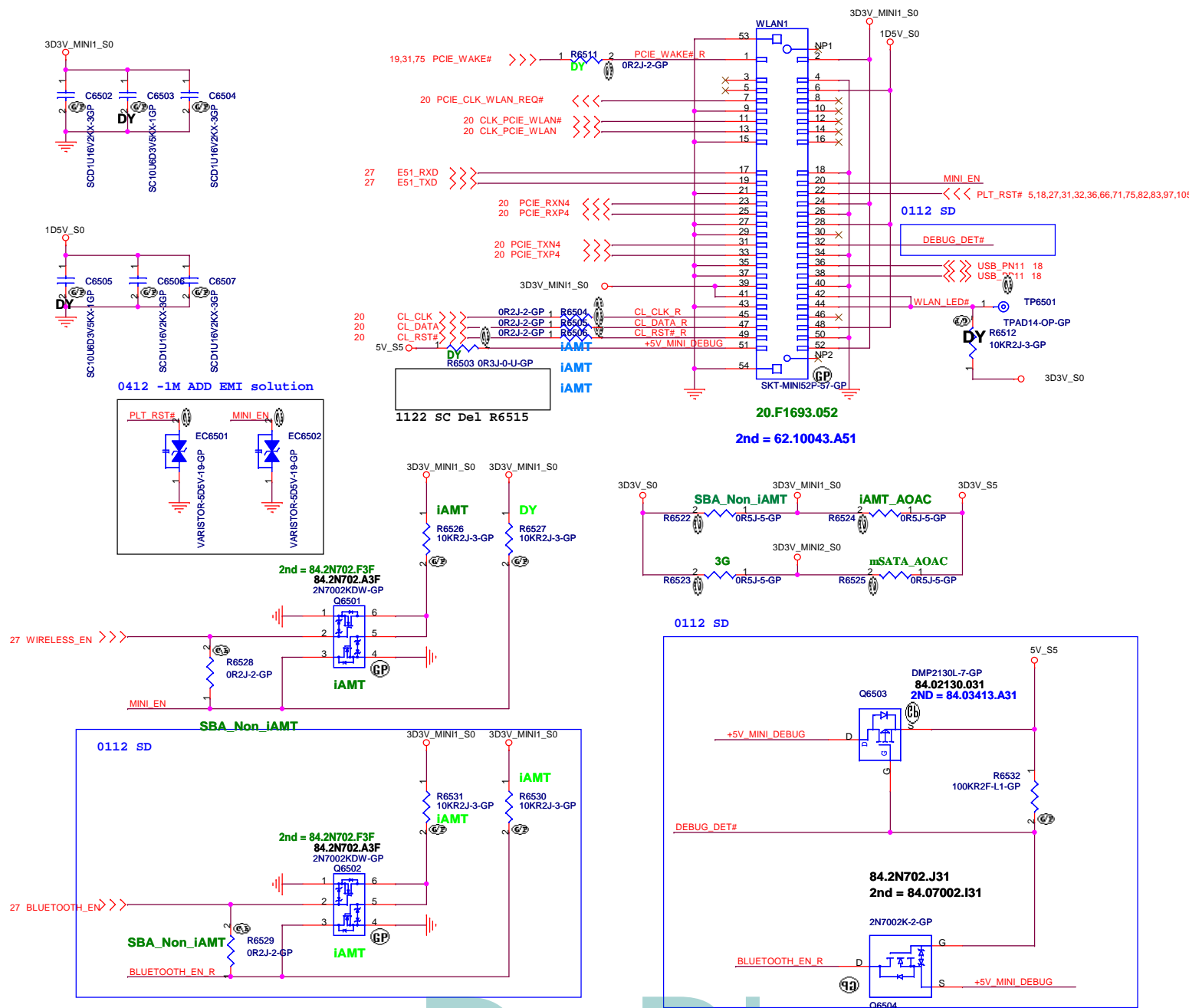
Date: Thursday, April 12, 2012

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Dr-Bios.com

SSID = Wireless

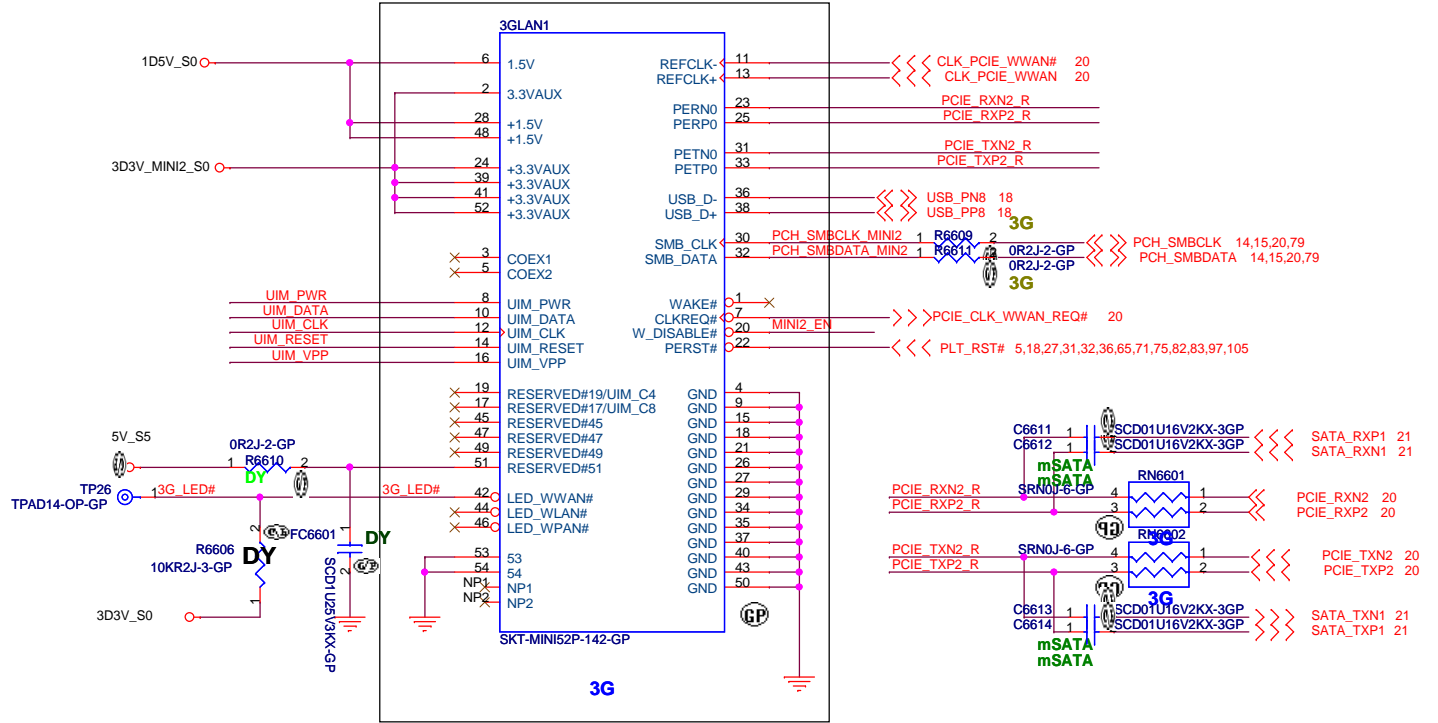
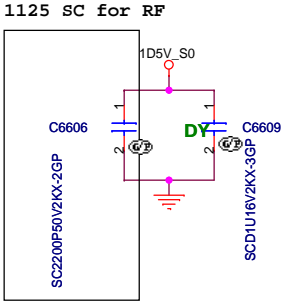
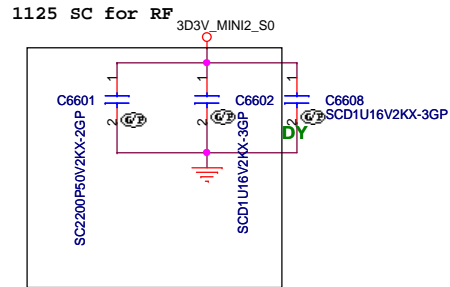
Mini Card Connector(802.11a/b/g/n)



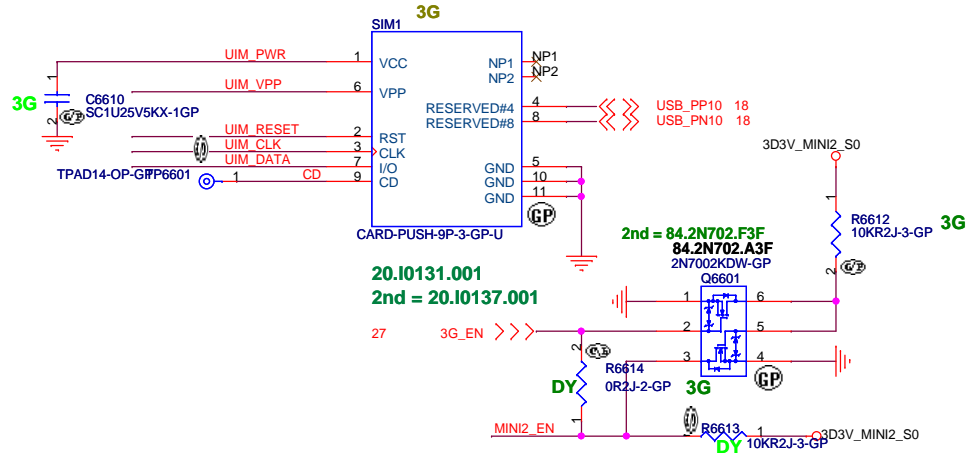
Dr-Bios.com

SSID = Wireless

Mini Card Connector(3GLAN)



0103 SC change to 62.10043.H61



<Variant Name>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
3G			
Size	Document Number	Rev	
Custom	BAD40 HC	1	
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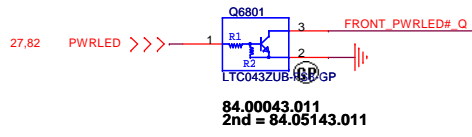
reserved

Dr-Bios.com

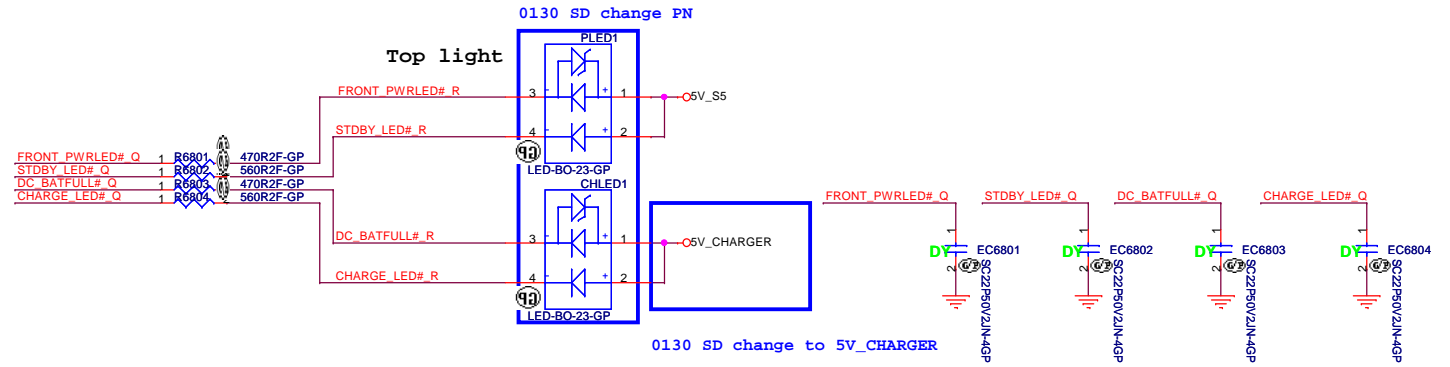
<Variant Name>

緯創資通			Wistron Corporation		
			21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
mSATA					
Size	Document Number				Rev
A4	BAD40 HC				1
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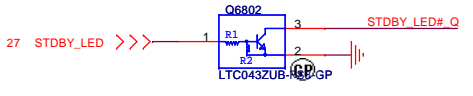
Power button LED



84.00043.011
2nd = 84.05143.011

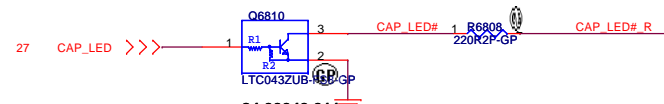


Power STDBY_LED

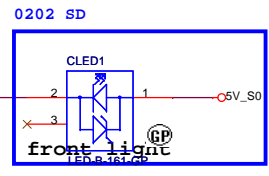


84.00043.011
2nd = 84.05143.011

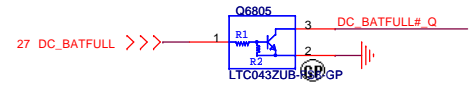
Caps Lock LED



84.00043.011
2nd = 84.05143.011

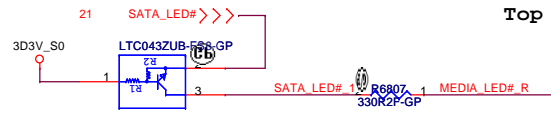


Battery LED2(DC_BATFULL)

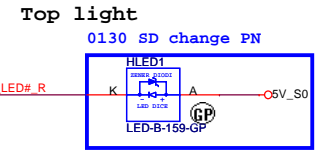


84.00043.011
2nd = 84.05143.011

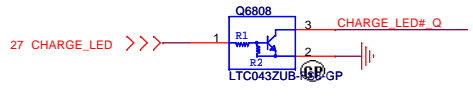
SATA HDD LED



84.00043.011
2nd = 84.05143.011



Battery LED1(CHARGE)



84.00043.011
2nd = 84.05143.011

1107 SC Del BXD PWR LED

0302 -1 Del PWR BTN

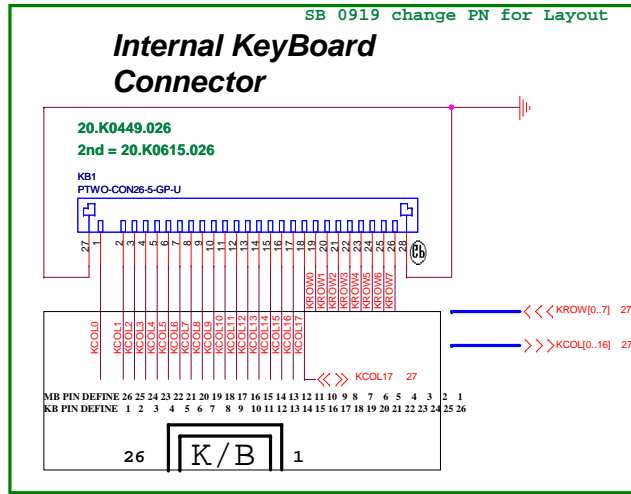
Dr-Bios.com

<Variant Name>

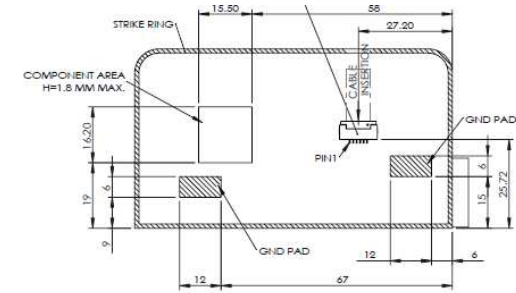
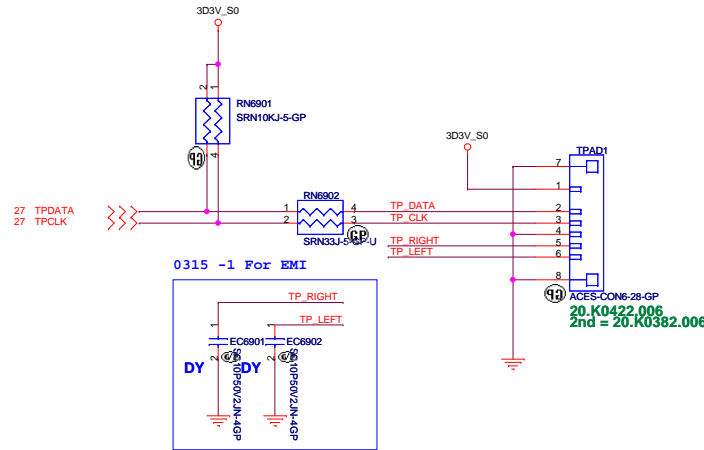
Title		LED Bard/Power Button	
Size	Document Number	Rev	
Custom	BAD40 HC	1	
Date:	Thursday, April 12, 2012	Sheet	68 of 108

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

SSID = KBC



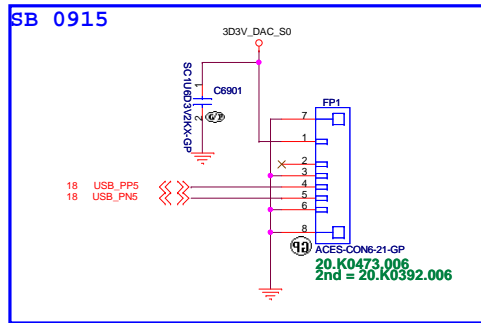
TOUCH PAD 1.0 pitch



COMPONENT - BOTTOM VIEW

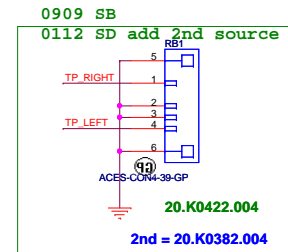
J1 PIN ASSIGNMENT:
PIN1 : TP_L
PIN2 : TP_R
PIN3 : GND
PIN4 : PS2_CLK
PIN5 : PS2_DAT
PIN6 : VDD

Finger Printer 0.5 pitch



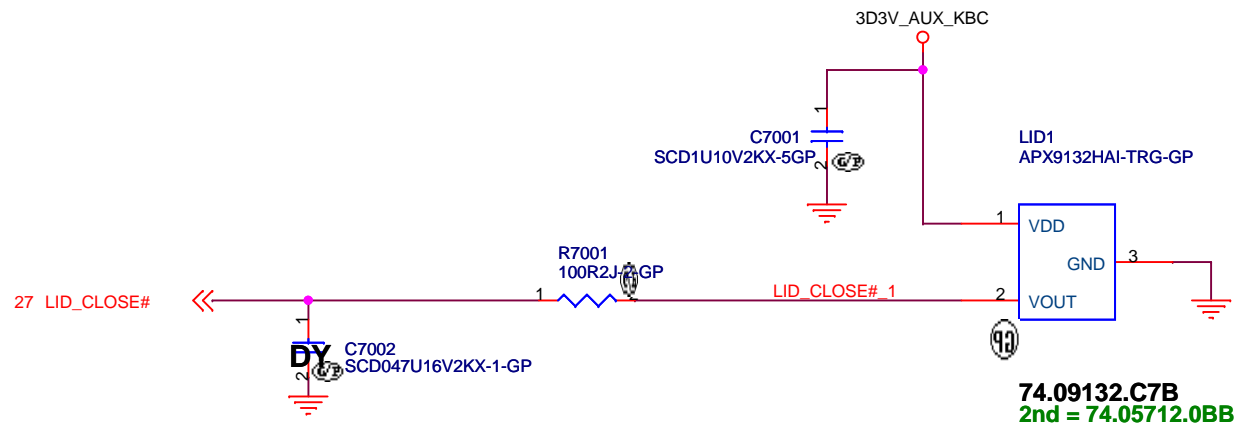
Pin No.	Define
1	ESD ground
2	USB D- Signal
3	USB D+ Signal
4	GND
5	NC
6	3.3V Power pin

Rubber Dome 1.0 pitch



<Variant Name>

緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsieh, Taipei Hsien 221, Taiwan, R.O.C.	
Title Key Board/Touch Pad	
Size Custom	Document Number BAD40 HC
Date: Thursday, April 12, 2012	Rev 1
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<Variant Name>

緯創資通 **Wistron Corporation**
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

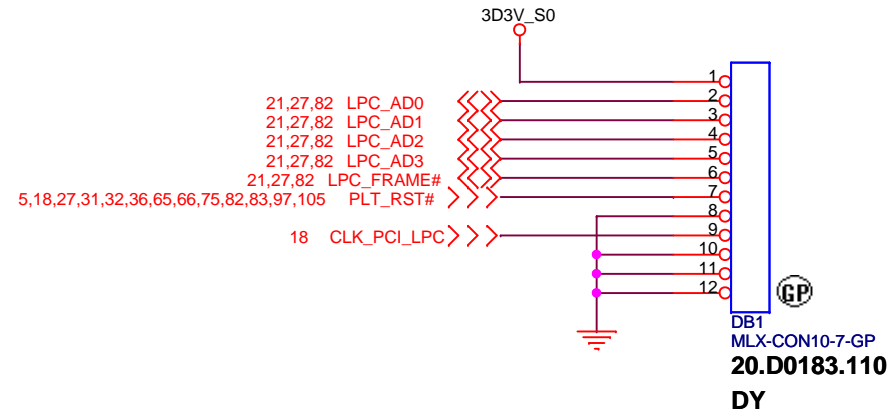
Title **Hall Sensor**

Size A4	Document Number BAD40 HC	Rev 1
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SB modify to test pad



<Variant Name>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Dubug connector

Size

Document Number

Rev

A4

BAD40 HC

1

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Dr-Bios.com

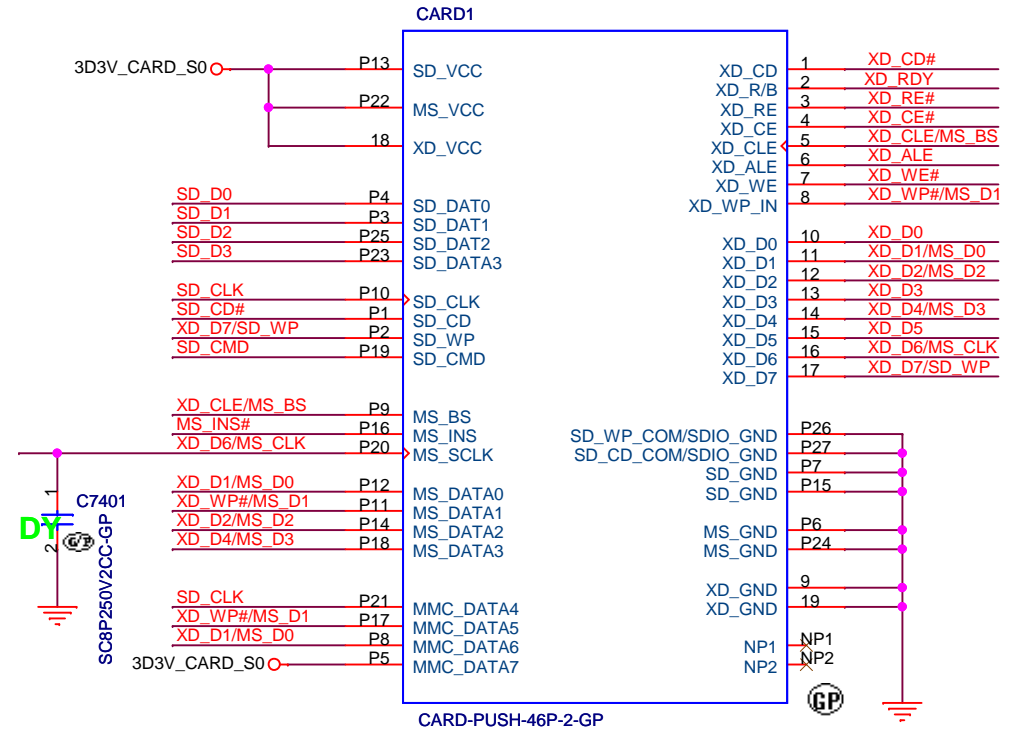
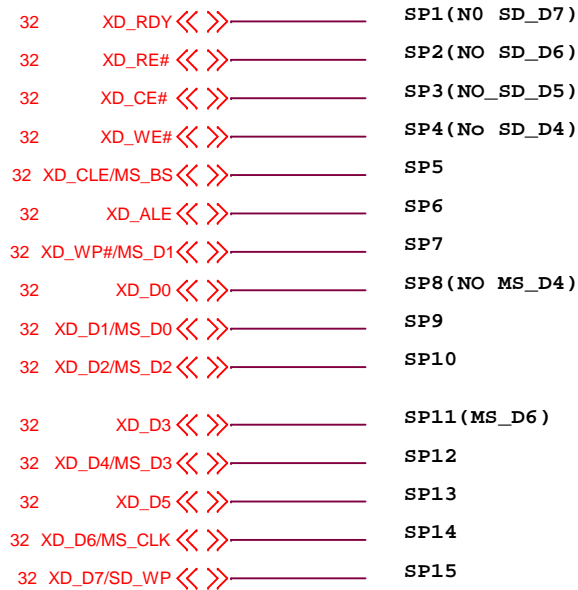
(Blanking)

Dr-Bios.com

<Variant Name>		
緯創資通 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
Reserved		
Size A3	Document Number BAD40_HC	Rev 1
Date: Thursday, April 12, 2012		
Sheet 73 of 108		1

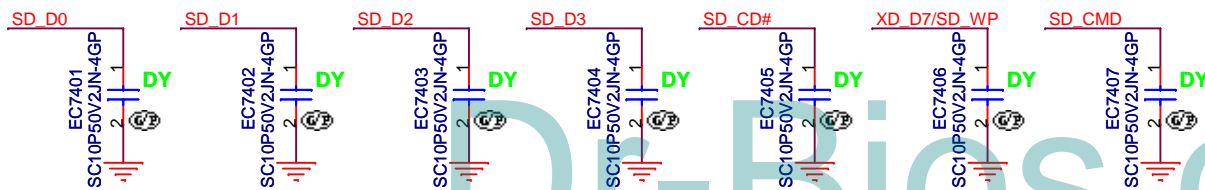
SD/XD/MS Card Reader

SSID = SDIO



20.I0135.001

2nd = 20.I0129.001

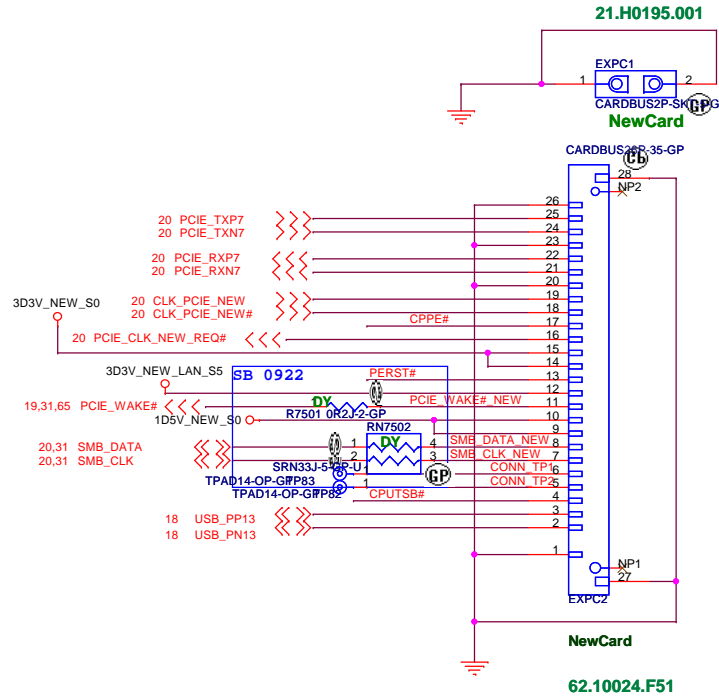


<Variant Name>

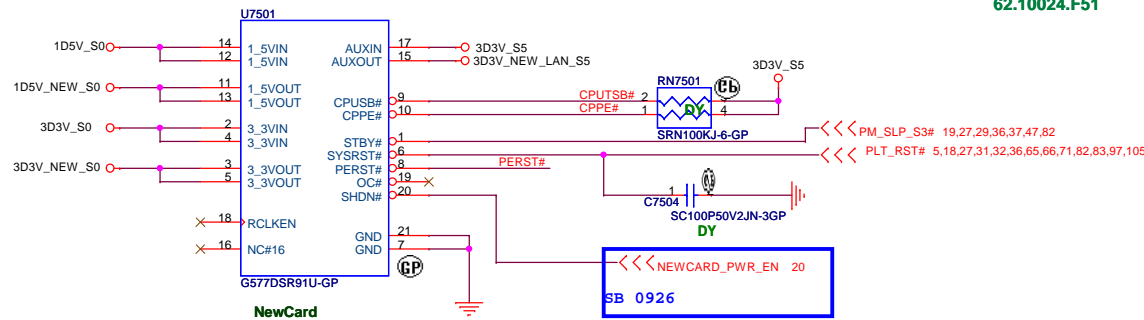
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
CARD Reader CONN			
BAD40 HC			
Size A4	Document Number		Rev 1
Date: Thursday, April 12, 2012	Sheet 74 of 108		

SSID = ExpressCard

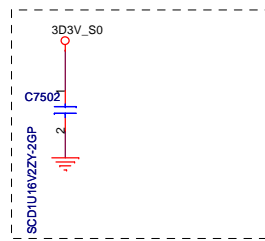
DIP階 For Expresscard socket



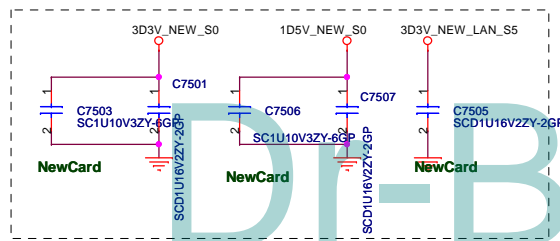
+1.5V_CARD Max. 650mA, Average 500mA.
 +3.3V_CARD Max. 1300mA, Average 1000mA
 +3.3V_CARDAUX Max. 275mA



Place them Near to Chip



Place them Near to Connector



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Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title New Card		
Size A3	Document Number BAD40_HC	Rev 1
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<Variant Name>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
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Title		Reserved
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Size	Document Number	Rev
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<Variant Name>		
緯創資通 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
Reserved		
Size A3	Document Number BAD40_HC	Rev 1
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(Blanking)

<Variant Name>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size
A4

Document Number

BAD40 HC

Rev
1

Date: Thursday, April 12, 2012

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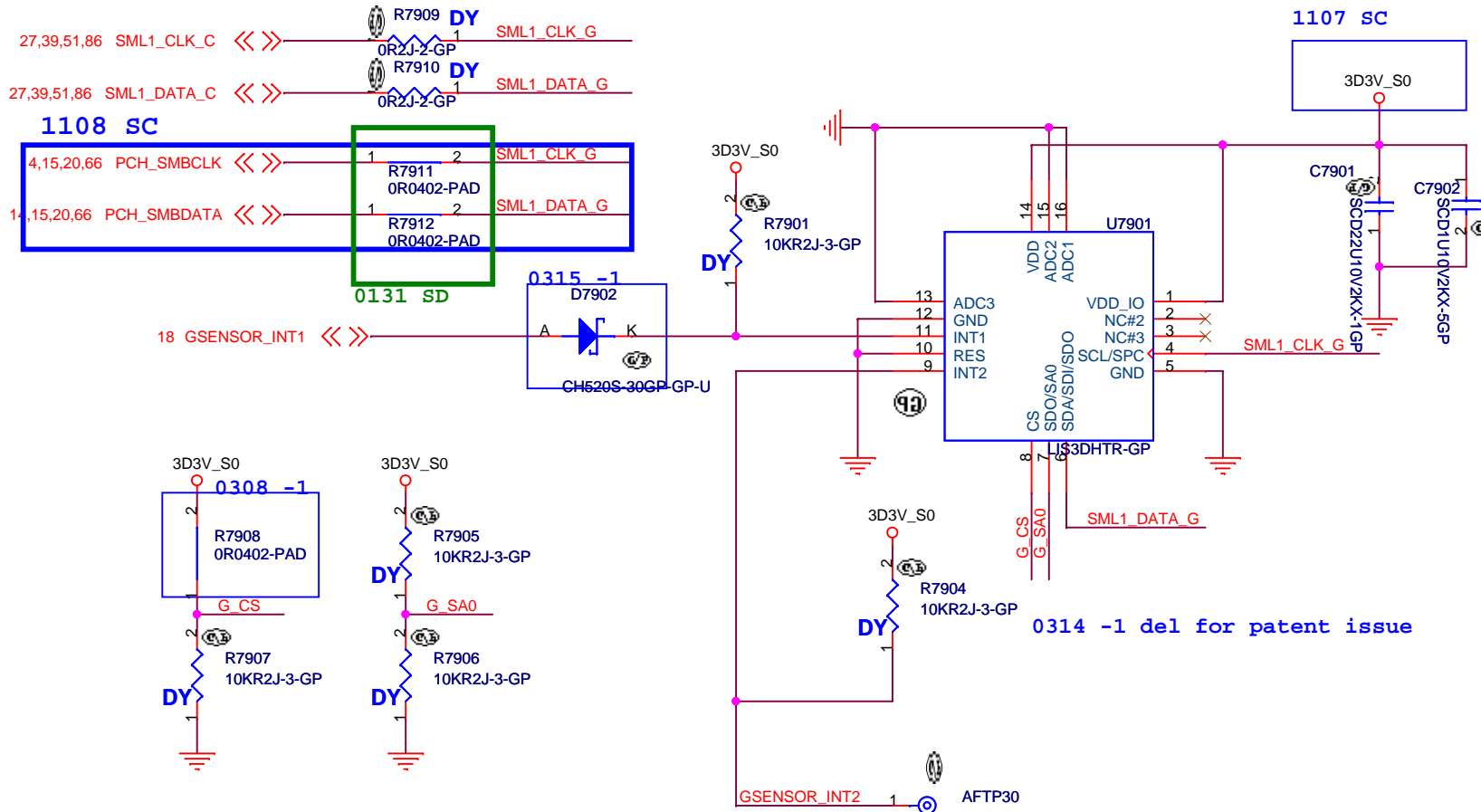
Dr-Bios.com

SSID = User.Interface

Free Fall Sensor

Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



SDO="H"; address="3Ah"
 *SDO="L"; address="38h"

*CS="H"; mode="I2C"
 CS="L"; mode="SPI"

<Variant Name>

緯創資通 **Wistron Corporation**
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title			Free Fall Sensor		
Size	Document Number				Rev
A4	BAD40 HC				1
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Dr-Bios.com

(Blanking)

Dr-Bios.com

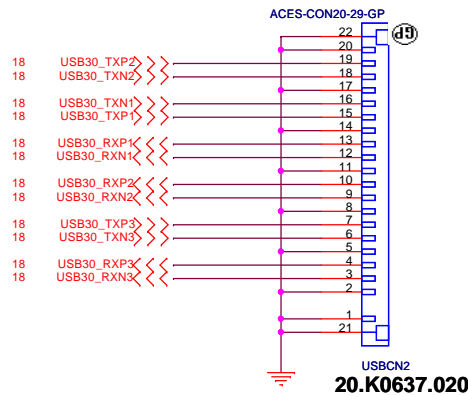
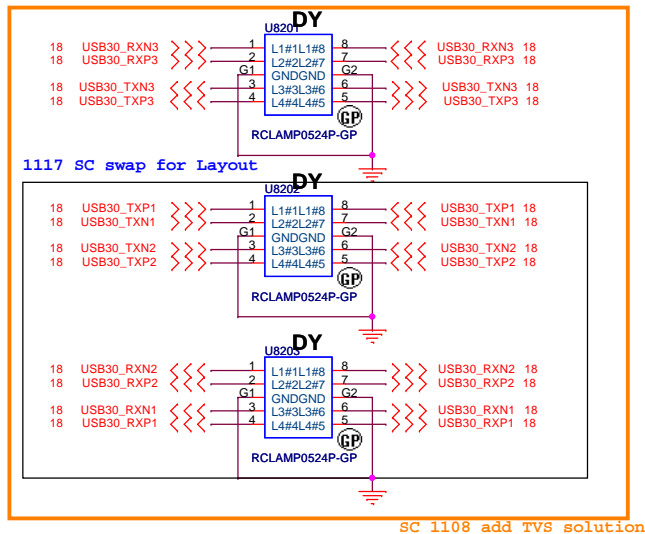
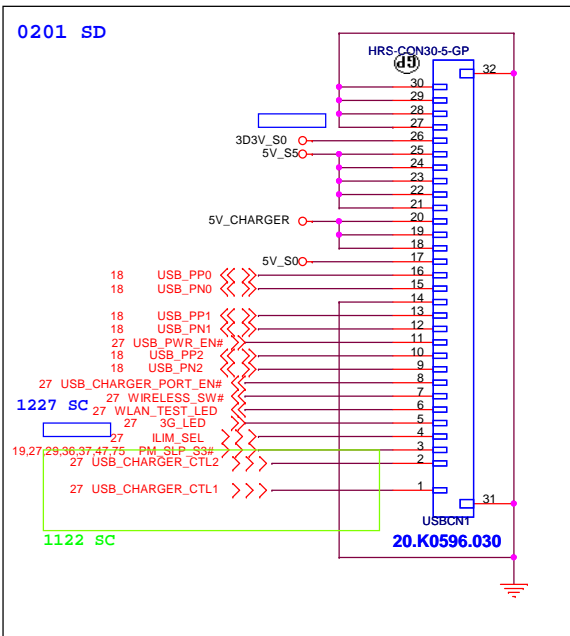
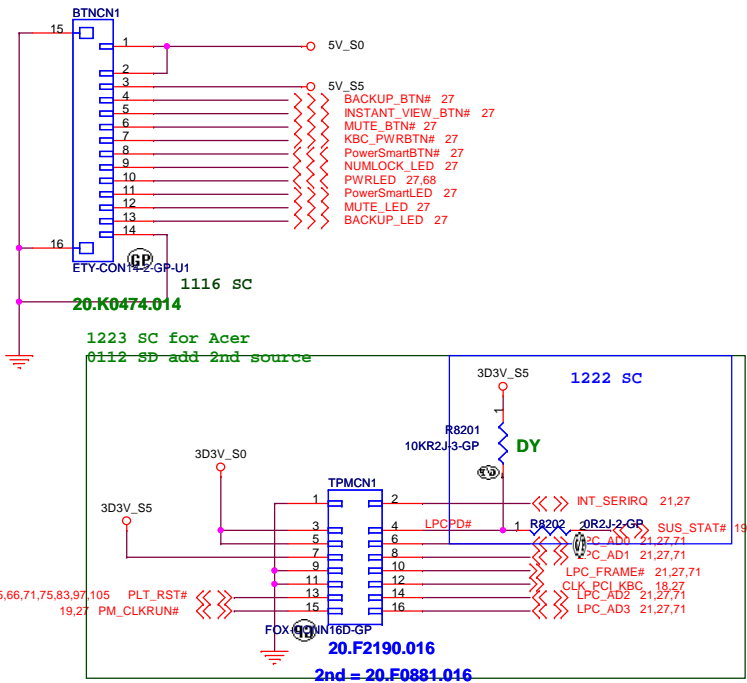
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **Reserved**

Size A4	Document Number BAD40 HC	Rev 1
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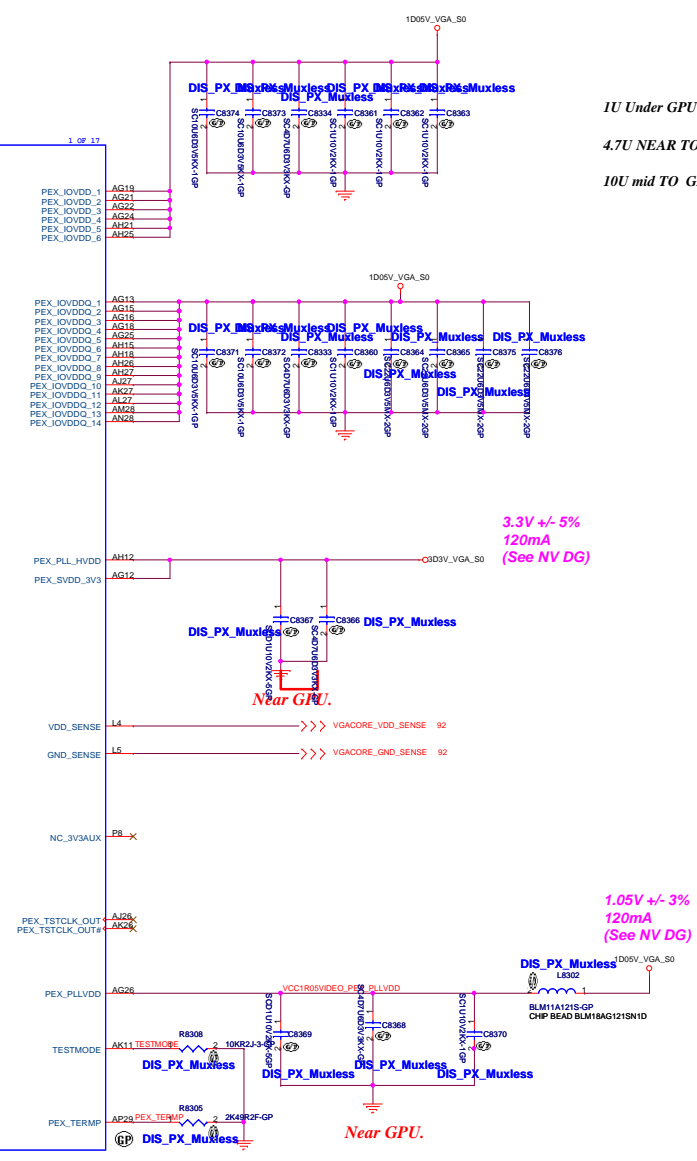
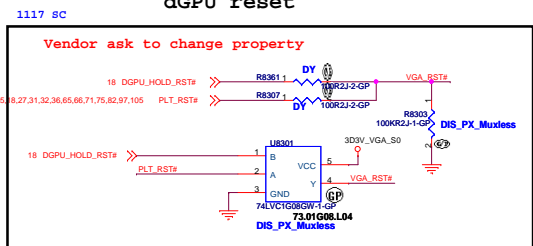
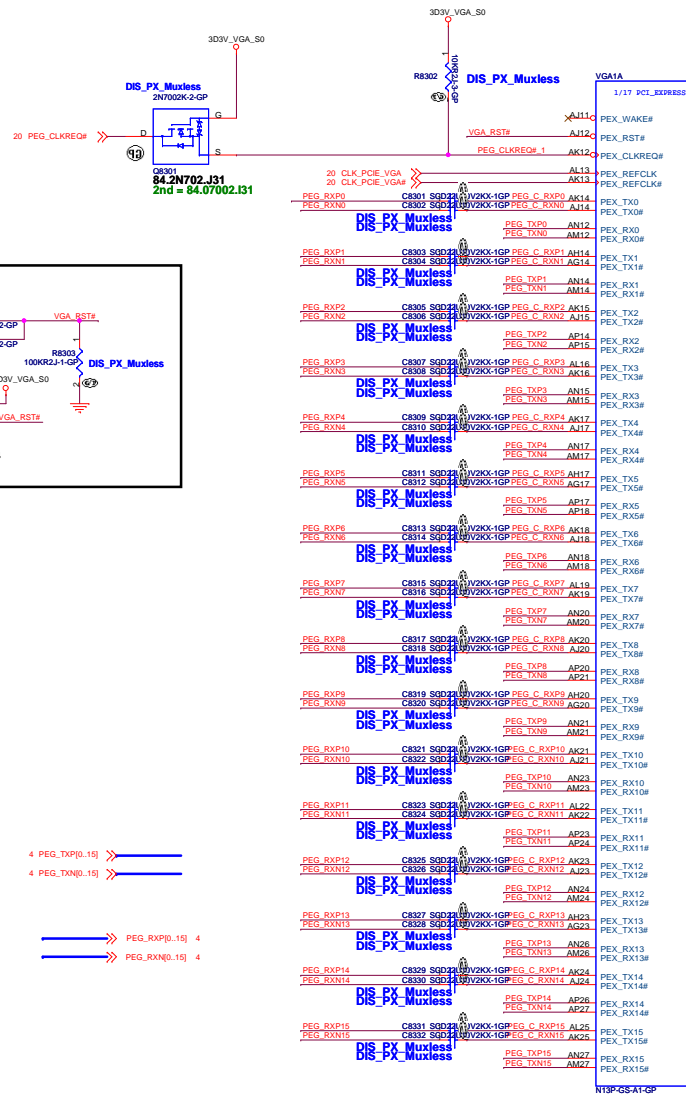
Date: Thursday, April 12, 2012 Sheet 80 of 108



<Variant Name>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.	
IO Board Connector			
Title	Document Number		Rev
Size	BAD40 HC		1
Custom			
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IU Under GPU
 4.7U NEAR TO GPU
 10U mid TO GPU

IU Under GPU
 4.7U NEAR TO GPU
 10U mid TO GPU

3.3V +/- 5%
 120mA
 (See NV DG)

1.05V +/- 3%
 120mA
 (See NV DG)

4 PEG_TXP[0..15] >>> 4
 4 PEG_TXN[0..15] >>> 4

PEG_RXP[0..15] 4
 PEG_RXN[0..15] 4

71.0N13P.000 DIS_PX_Muxless

Dr-Bios.com

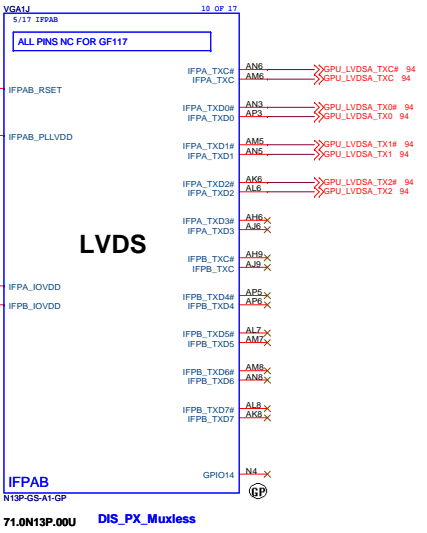
1.05V +/- 3%
220mA
(See NV DG)
1005V_VGA_S0

120ohm@100MHz DCR=0.05
L8401
DIS_PX

3.3V +/- 5%
220mA
(See NV DG)
303V_VGA_S0

180ohm@100MHz ESR=0.15 DCR=0.09
DIS_PX_Muxless

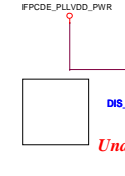
Near GPU Under GPU



LVDS

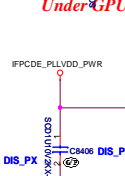
71.0N13P.00 DIS_PX_Muxless

1
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S
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e
l
C
8
4
0
2
f
o
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l
a
y
o
u
t



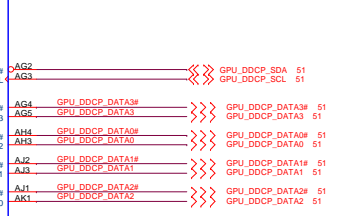
IFPC HDMI

DIS_PX_Muxless



IFPD eDP

DIS_PX_Muxless



GPU DDCP

GPU eDP

1.05V +/- 3%
285mA
(See NV DG)
1005V_VGA_S0

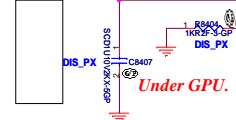
220ohm@100MHz ESR=0.05

3.3V +/- 5%
440mA (220mA each, max 2 links)
(See NV DG) 300ohm@100MHz ESR=0.25

Near GPU.

Near GPU.

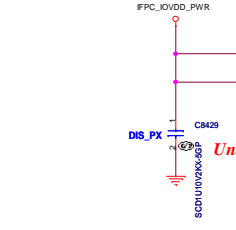
1117 SC del for layout



IFPE

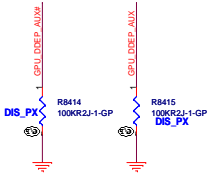
IFPF

71.0N13P.00 DIS_PX_Muxless



IFPF

71.0N13P.00 DIS_PX_Muxless



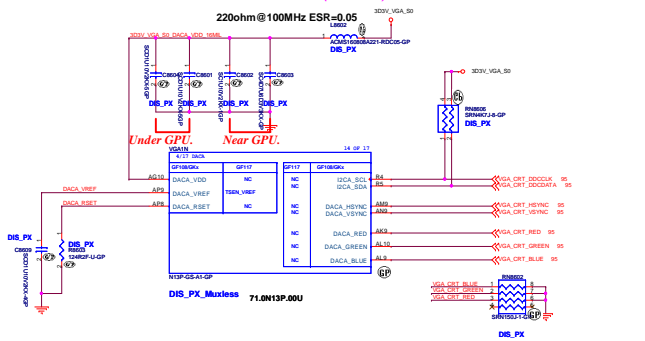
GPU DDEP

<Core Design>

300ohm@100MHz ESR=0.25ohm

3.3V +/- 3%
120mA
(See NV DG)

1.05V +/- 3%
150mA
(See NV DG)



300ohm@100MHz DCR=0.02

180ohm@100MHz ESR=0.15 DCR=0.09

71.0N13P.000

DIS_PX_Muxless

DIS_PX

DIS_PX_Muxless

DIS_PX

DIS_PX_Muxless

DIS_PX

DIS_PX_Muxless

DIS_PX

DIS_PX_Muxless

DIS_PX

DIS_PX_Muxless

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DIS_PX

DIS_PX_Muxless

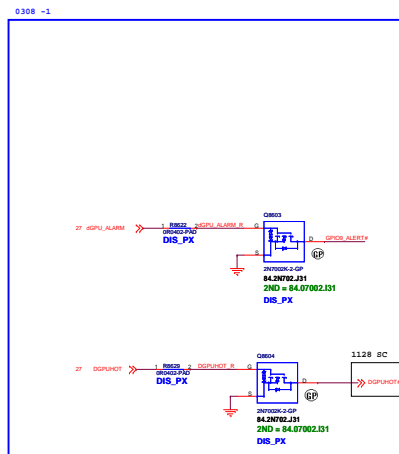


Table 15.8 User Straps

User[3:0]	Type	Resolution	Sync	Notes
0000	XGA	1024 x 768	-/-	
0001	XGA	1024 x 768	+/+	
0010	SXGA	1280 x 1024	-/-	
0011	SXGA+	1400 x 1050	-/-	
0100	UXGA	1600 x 1200	+/+	
0101	QXGA	2048 x 1536	+/+	Reduced Blanking
0110	SXGA+	1400 x 1050	-/-	
0111	SVGA	800 x 600	+/+	
1000 - 1100	-	-	-	Customer defined (Default)
1111	-	-	-	EDID is used

Strap0

Table 15.3 Resistance Mapping to Hex Values

Resistor Values	Pull-up to VDD	Pull-down to GND
5k	1000	0000
10k	1001	0001
15k	1010	0010
20k	1011	0011
25k	1100	0100
30k	1101	0101
35k	1110	0110
45k	1111	0111

25Kohm 5Kohm 10Kohm 30Kohm
64.24925.6DL 64.49915.6DL 64.10025.6DL 64.30025.6DL

NVIDIA TABLE

	Hynix 2G 0110 128M*16*8 900MHZ	Hynix 1G 0010 64M*16*8 900MHZ	Samsung 1G 0011 64M*16*8 900MHZ	Samsung 2G 0111 128M*16*8 900MHZ
ROM_SI	34.8Kohm 64.34825.6DL	15Kohm 64.15025.6DL	20Kohm 64.20025.6DL	45Kohm 64.45325.6DL

Table 111. Display Link to SORX_EXPOSED Bit Mapping

Displays Link Mode	I/FPA/B	SOR1_EXPOSED = 1	SOR2_EXPOSED = 1	SOR3_EXPOSED = 1	LVDS	eDP	Not in Use
Dual Link Mode	IFPA/B	SOR1_EXPOSED = 1	SOR2_EXPOSED = 1	SOR3_EXPOSED = 1	SOR0_EXPOSED = 0	eDP	SOR0_EXPOSED = 0
	IFPD	SOR2_EXPOSED = 1	SOR3_EXPOSED = 1	SOR0_EXPOSED = 1	SOR1_EXPOSED = 0	eDP	SOR1_EXPOSED = 0
	IFPE/F	SOR3_EXPOSED = 1	SOR0_EXPOSED = 1	SOR2_EXPOSED = 1	SOR1_EXPOSED = 0	eDP	SOR2_EXPOSED = 0
Split Mode	IFPA/B	SOR1_EXPOSED = 1	SOR2_EXPOSED = 1	SOR3_EXPOSED = 1	SOR0_EXPOSED = 0	eDP	SOR0_EXPOSED = 0
	IFPD	SOR2_EXPOSED = 1	SOR3_EXPOSED = 1	SOR0_EXPOSED = 1	SOR1_EXPOSED = 0	eDP	SOR1_EXPOSED = 0
	IFPE	SOR3_EXPOSED = 1	SOR0_EXPOSED = 1	SOR2_EXPOSED = 1	SOR1_EXPOSED = 0	eDP	SOR2_EXPOSED = 0

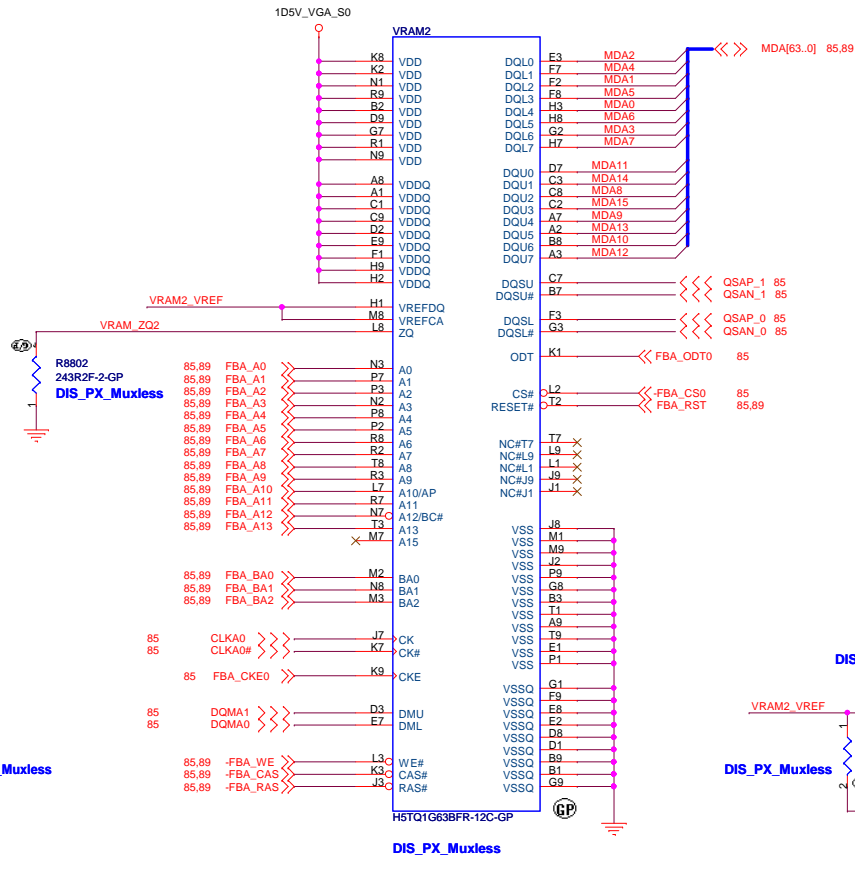
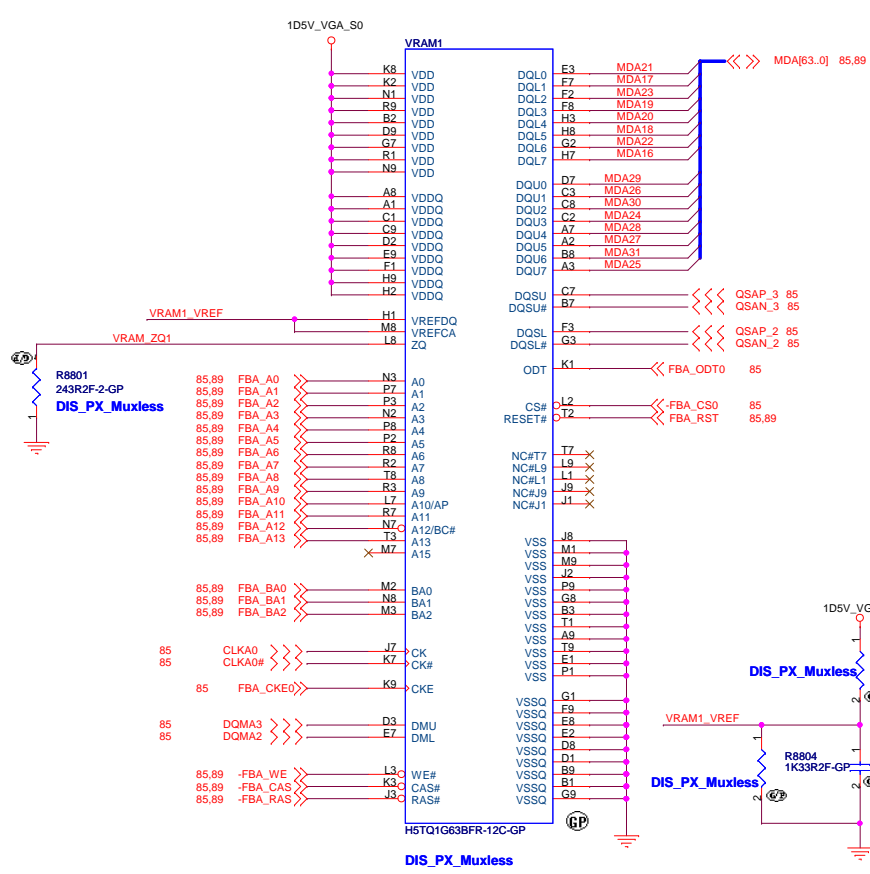
Strap3

	DEVID	ROM-SCLK	strap2
N13P-GL-A1	0x0DE9	0010 PD 15K	1001 PU 10K
N13P-GS-ES-A1	0x0FDE	1000 PU 4.99K	1011 PU 20K
N13P-GS-A1	0x0FD2	1000 PU 4.99K	0010 PD 15K

For N13P-GS-A1

Strap Pin Name	Logical strapping name bit#3	Logical strapping name bit#2	Logical strapping name bit#1	Logical strapping name bit#0
ROM_SCLK	PCL_DEVID[4]	SUB_VENDOR	PCL_DEVID[5]	PEX_PLL_EN_TER_#1
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
Hynix 2G	0	1	1	0
ROM_SO	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	3GIO_PADC7[2]	3GIO_PADC7[2]	3GIO_PADC7[1]	3GIO_PADC7[0]
STRAP2	PCL_DEVID[3]	PCL_DEVID[2]	PCL_DEVID[1]	PCL_DEVID[0]
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	RESERVED	PCL_SPEED_CHANGE_GEN3	PCE_MAX_SPEED	DP_PLL_VDD33V



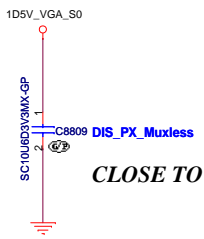
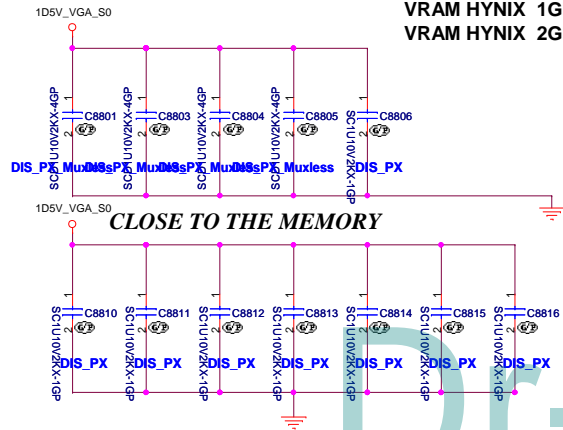


Hy2GX8_VR.2GB0G.001,Sam1GX8_VR.1GB0B.006,,Hy1GX8_72.51G63.C0U,Sam512X4_VR.1GB0B.006,Sam2GX8

VRAM = Hy2GX8,Sam1GX8,,Hy1GX8,Sam512X4,Sam2GX8
FB CMD mapping Mode D-N12x

VRAM SAMSUNG 1Gb VR.1GB0B.006
VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005
VRAM HYNIX 2Gb VR.2GB0G.001

DG requires 4x0.1uF and 8x1.0uF per VRAM chip



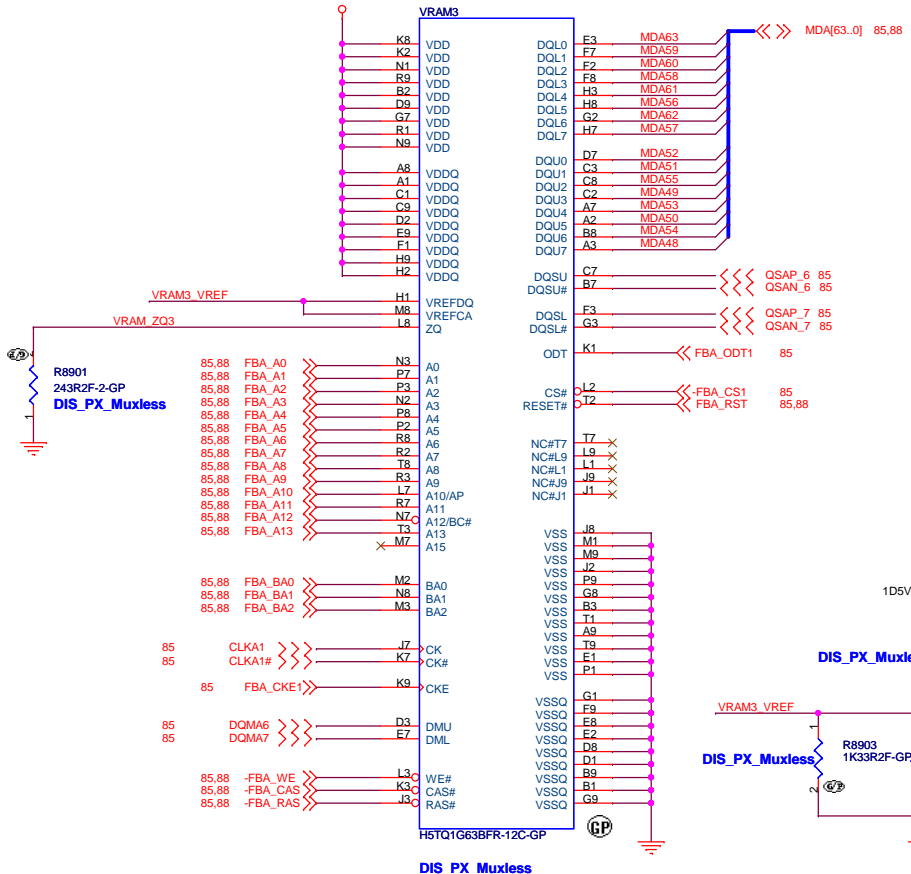
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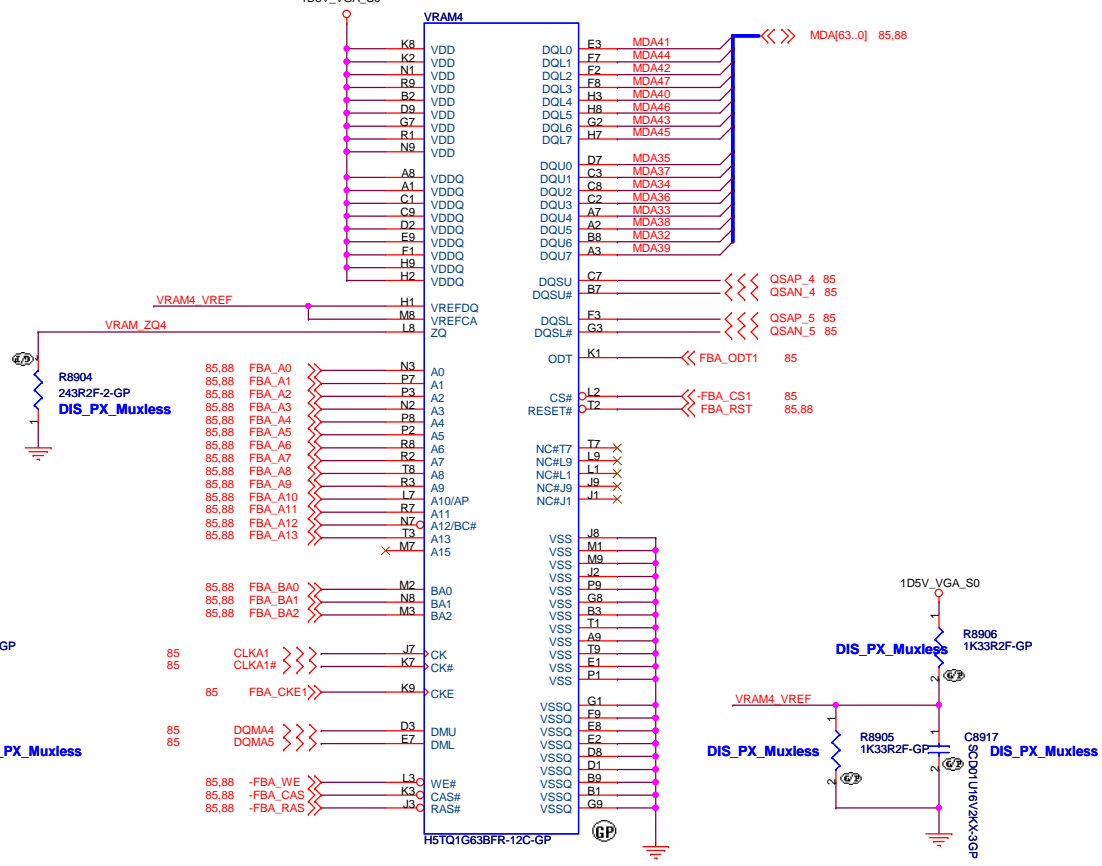
Title: **GPU-VRAM1,2 (1/4)**

Size Custom Document Number: **BAD40_HC** Rev: **1**

Date: Thursday, April 12, 2012 Sheet 88 of 108



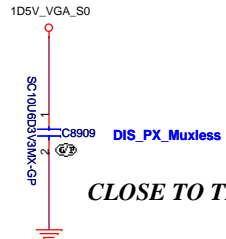
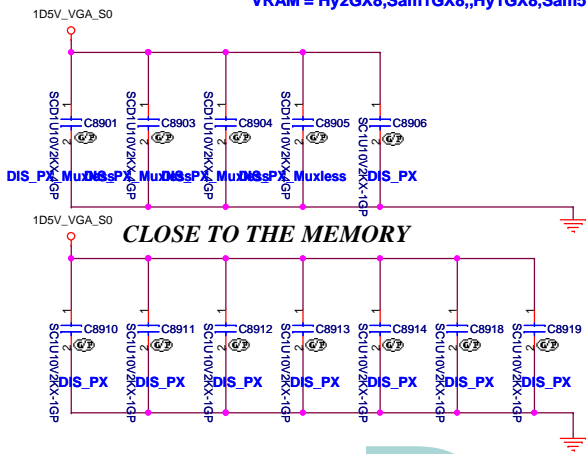
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VRAM = Hy2GX8,Sam1GX8,,Hy1GX8,Sam512X4,Sam2Gx8

FB CMD mapping Mode D-N12x

- VRAM SAMSUNG 1Gb VR.1GB0B.006
- VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005
- VRAM HYNIX 2Gb VR.2GB0G.001



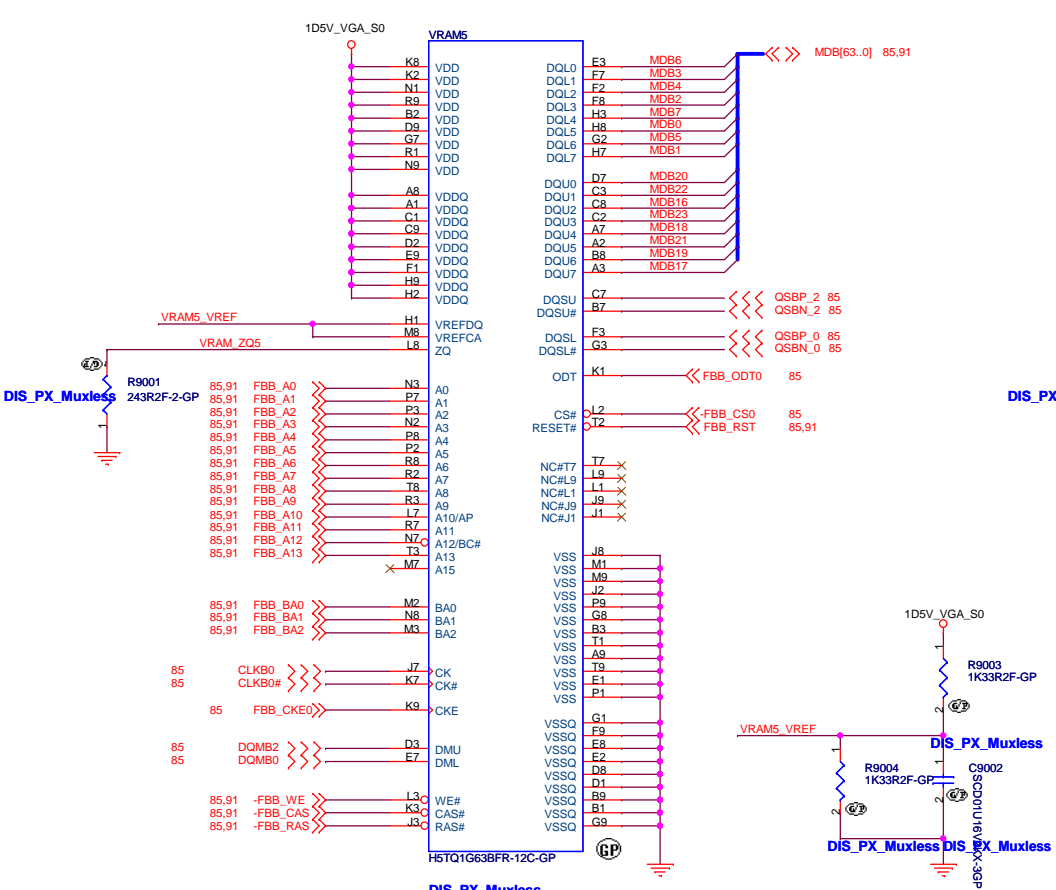
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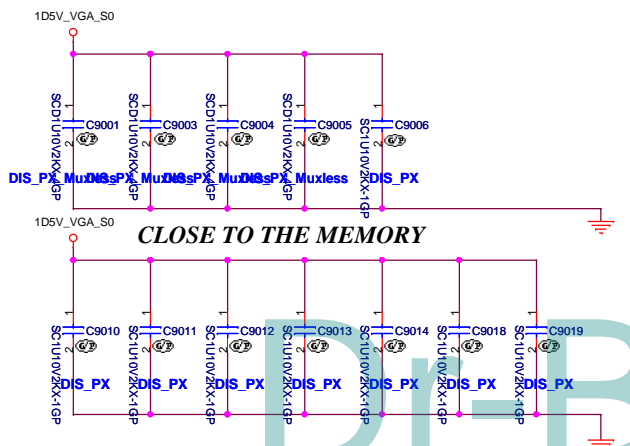
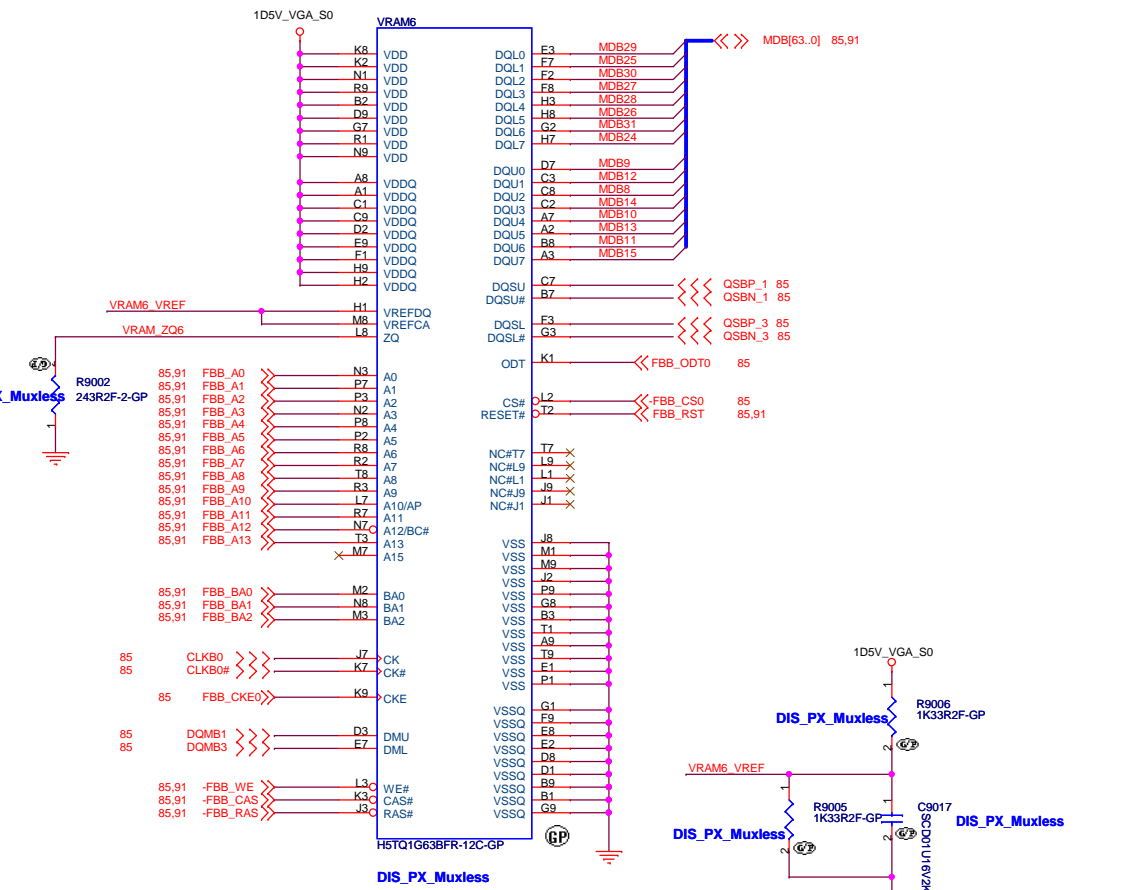
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Size: Custom Document Number: **BAD40_HC** Rev: **1**

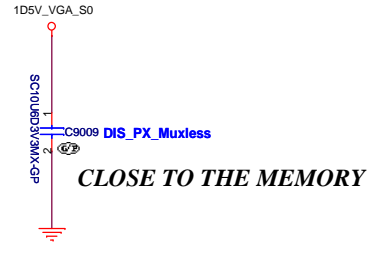
Date: Thursday, April 12, 2012 Sheet: 89 of 108

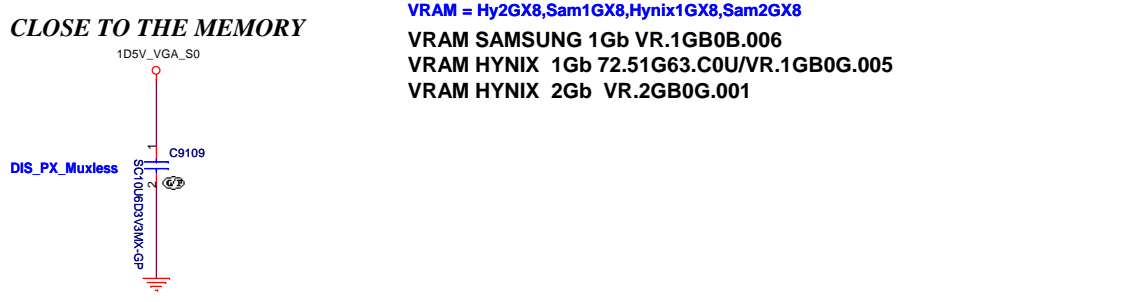
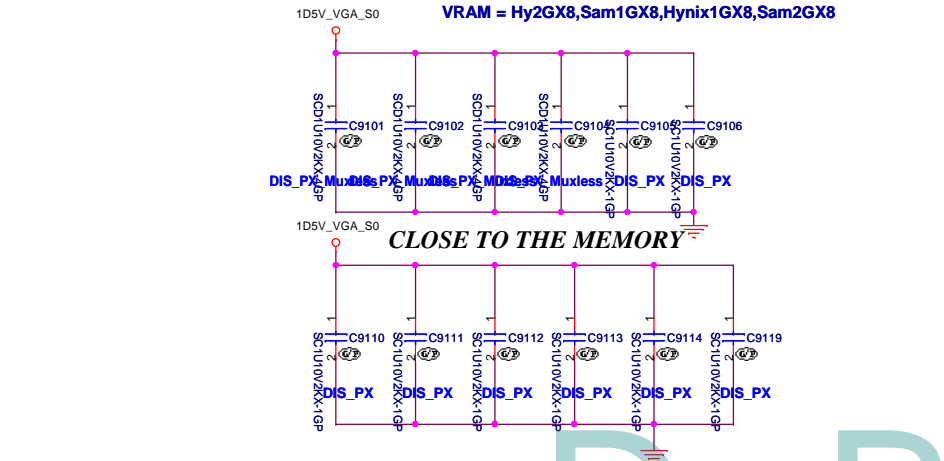
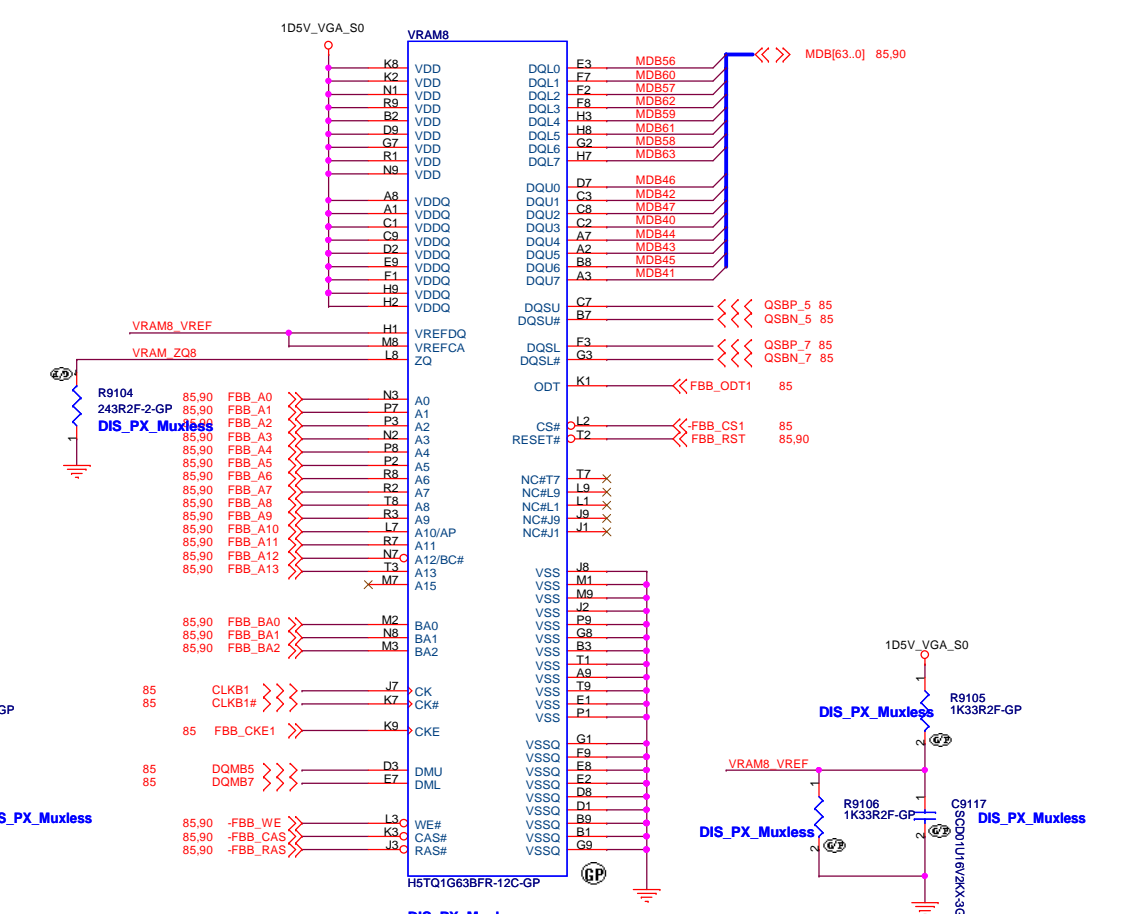
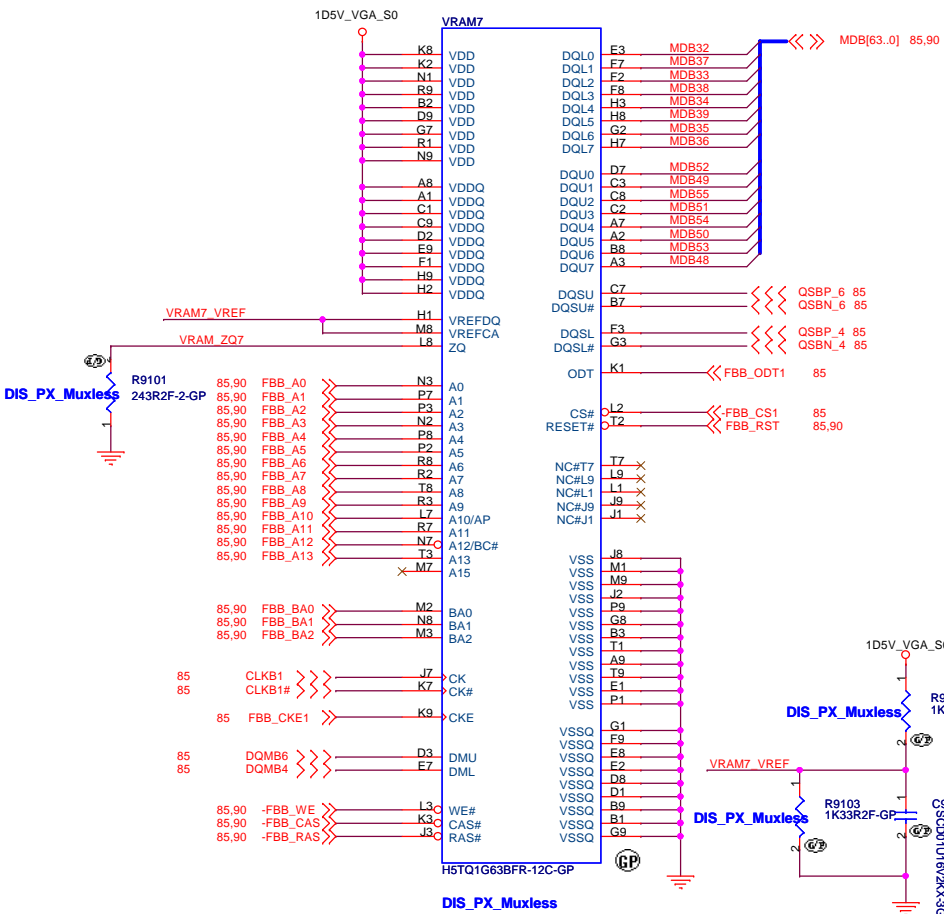


VRAM SAMSUNG 1Gb VR.1GB0B.006
 VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005
 VRAM HYNIX 2Gb VR.2GB0G.001



DG requires 4x0.1uF and 8x1.0uF per VRAM chip





CLOSE TO THE MEMORY

DIS_PX_Muxless
 VRAM = Hy2GX8,Sam1GX8,Hynix1GX8,Sam2GX8
 VRAM SAMSUNG 1Gb VR.1GB0B.006
 VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005
 VRAM HYNIX 2Gb VR.2GB0G.001

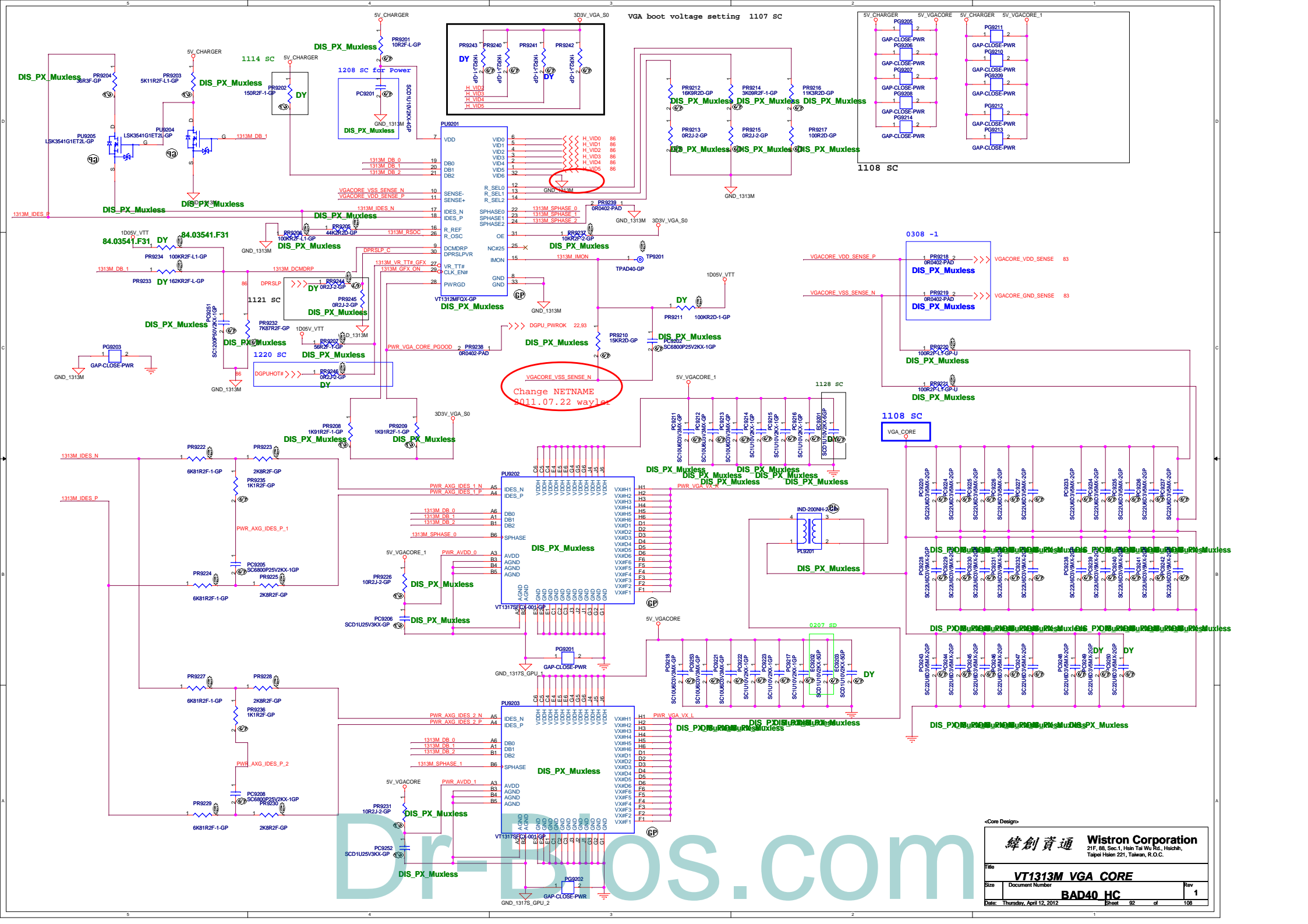
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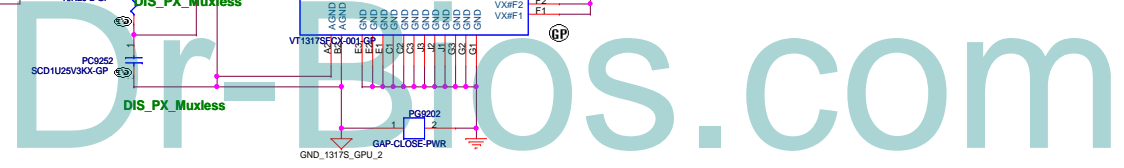
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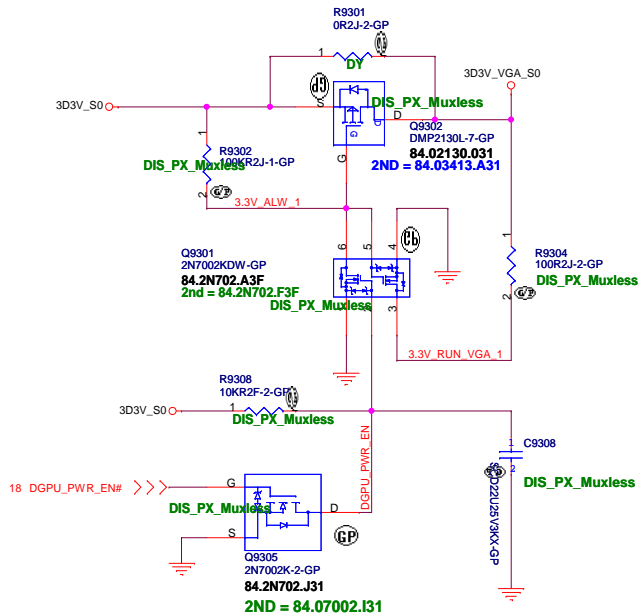




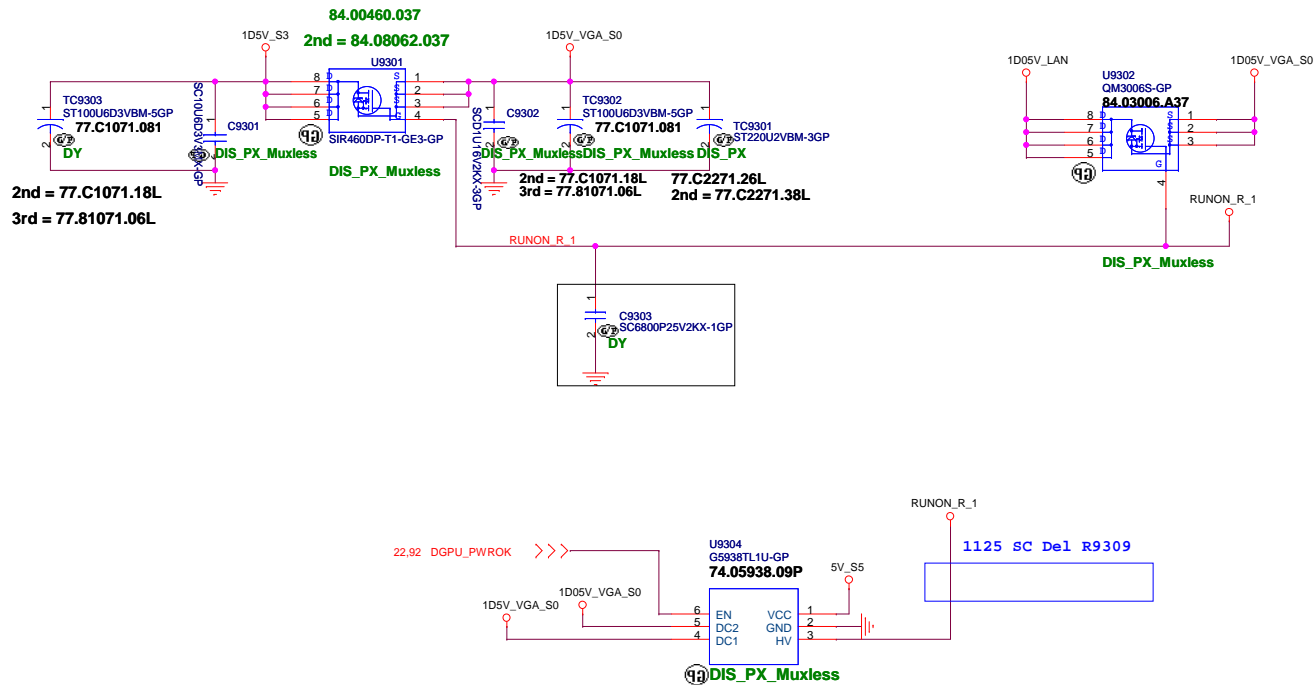
Change NETNAME
2011.07.22 way1ex



+3VS to 3.3V_DELAY Transfer



1D5V_VGA_S0



1D8V_S0 to 1D8V_VGA_S0

1125 SC Del Q9306

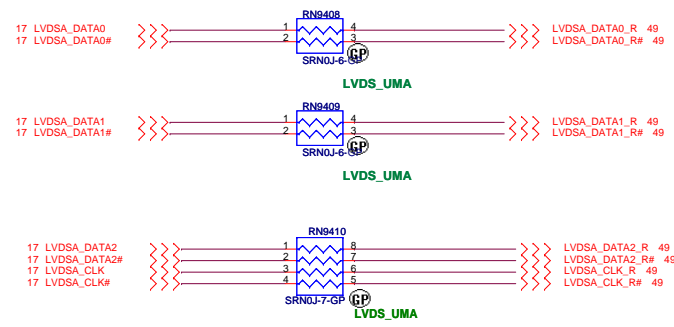
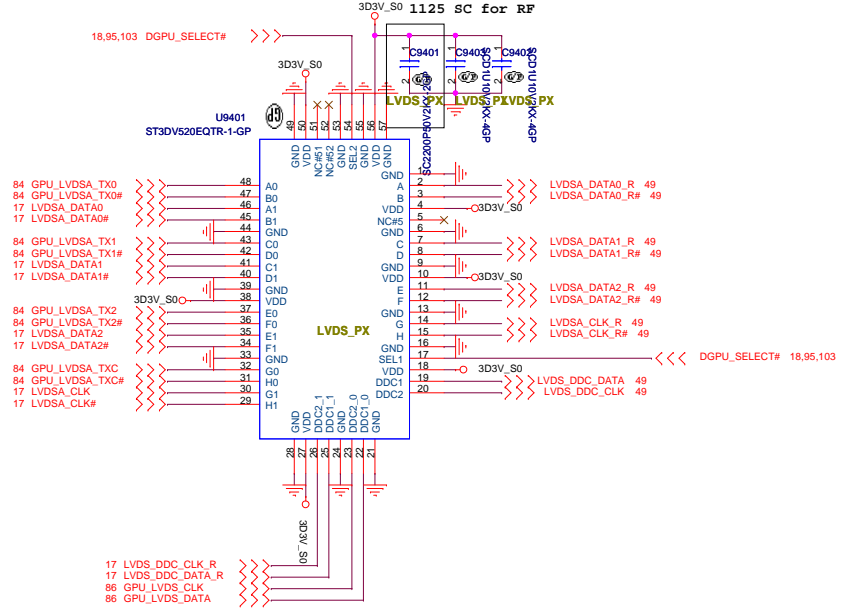


1D8V_S0_NV = IFPA_IOVDD & IFPB_IOVDD, it should be the latest ramp up rail.

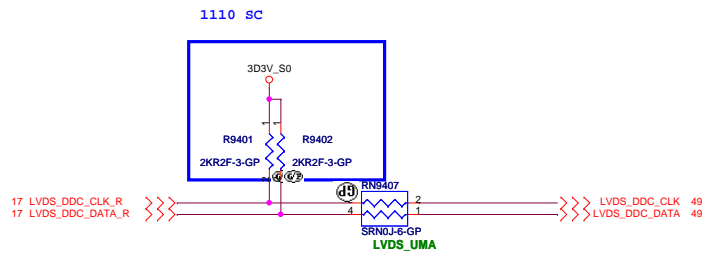
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 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
DISCRETE VGA POWER	
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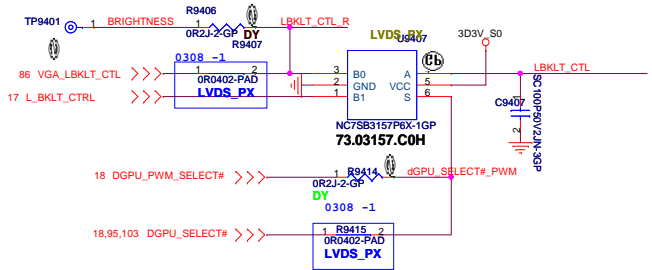
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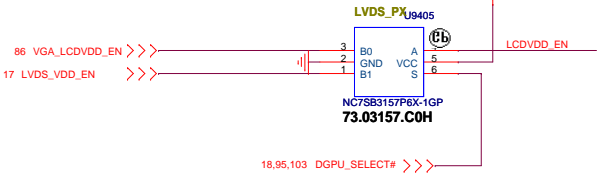
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 SEL1 Control A~H
 SEL2 Control DDC1, DDC2



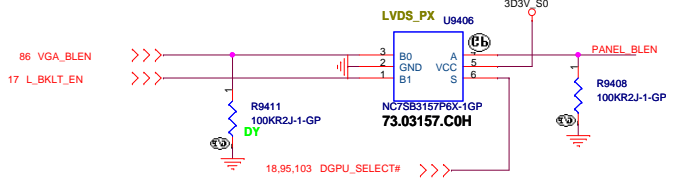
Panel BL brightness



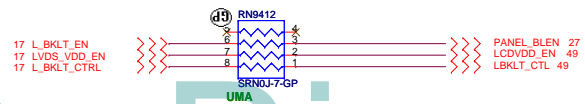
Power En



BL En



Panel BL brightness/Power En/BL En

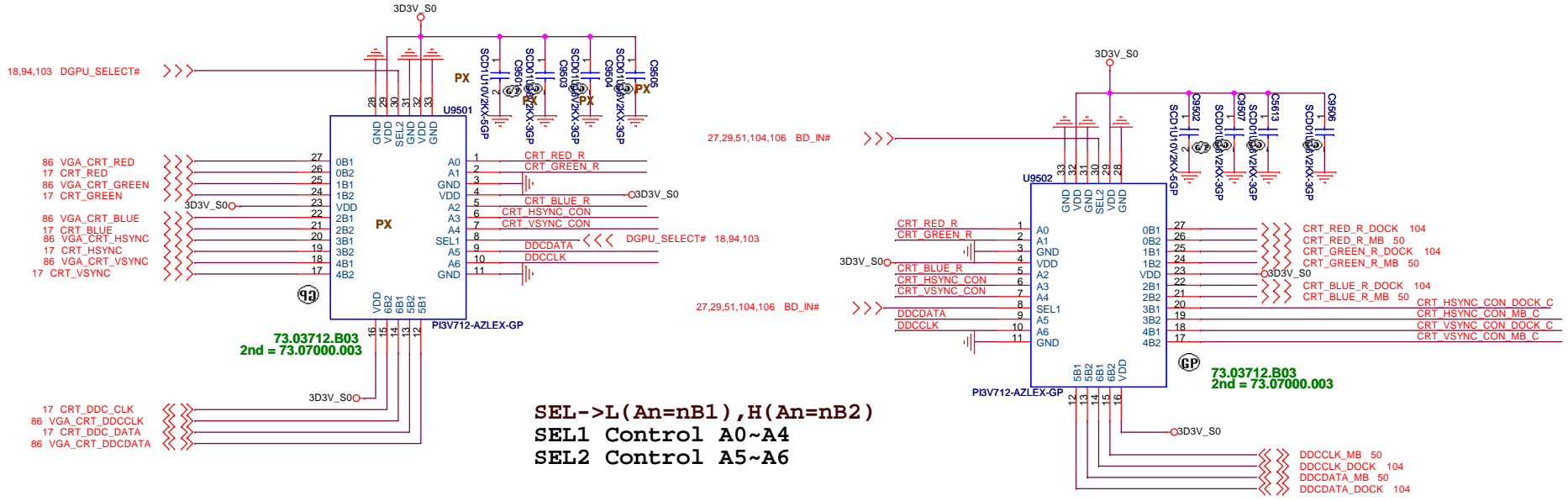


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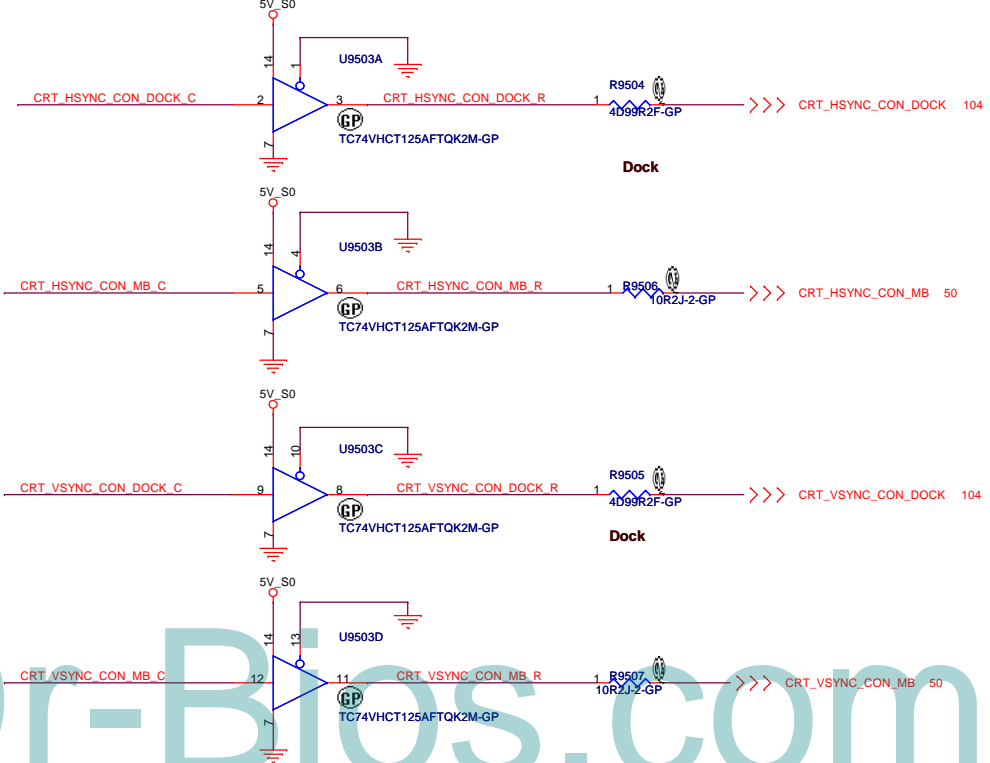
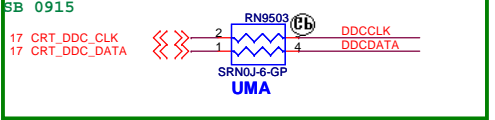
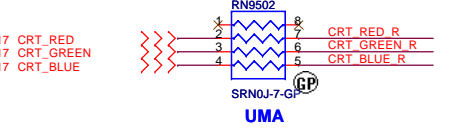
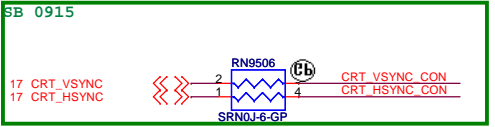
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CRT DDCDATA & DDCCLK



SEL->L (An=nB1) , H (An=nB2)
SEL1 Control A0~A4
SEL2 Control A5~A6



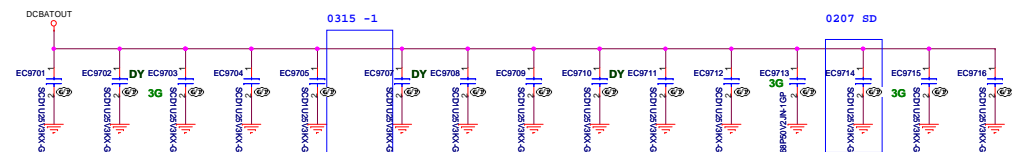
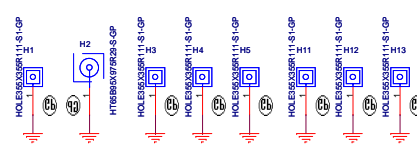
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緯創資通		Wistron Corporation
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CRT Switch		
Title		
Size A3	Document Number	Rev
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SSID = SDIO

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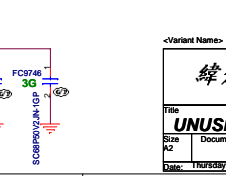
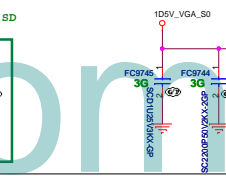
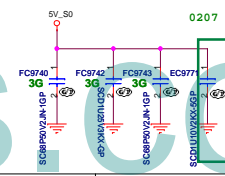
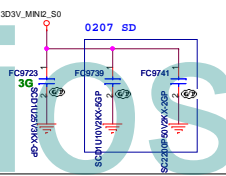
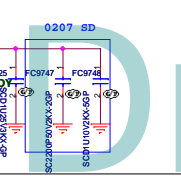
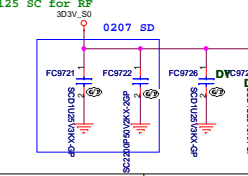
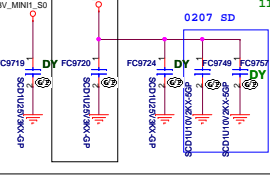
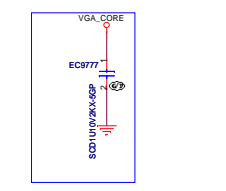
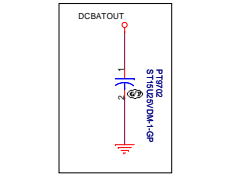
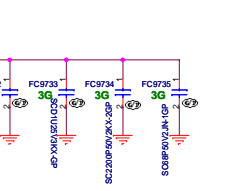
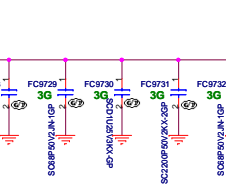
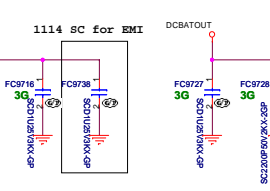
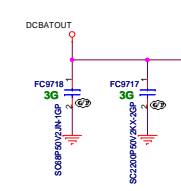
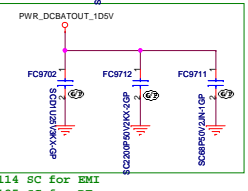
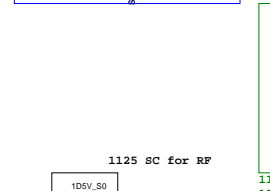
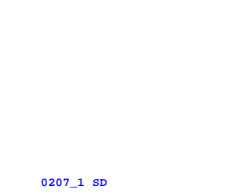
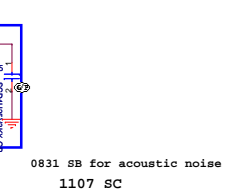
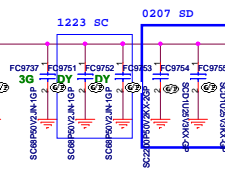
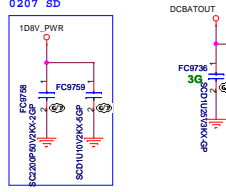
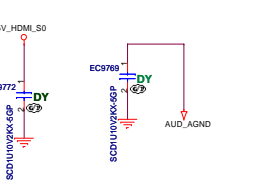
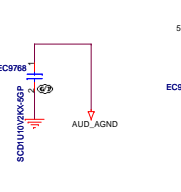
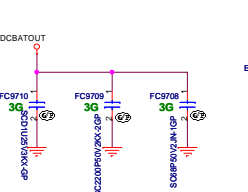
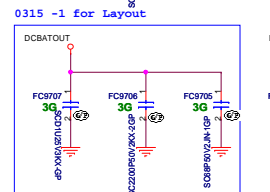
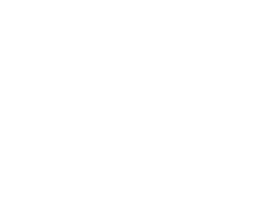
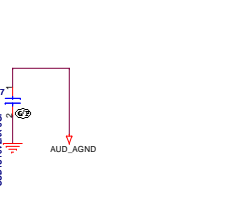
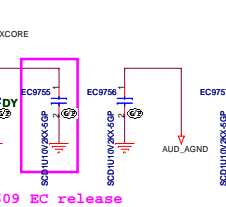
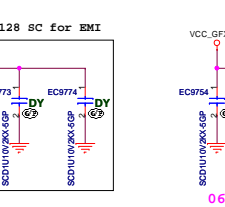
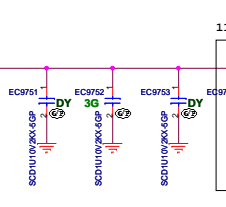
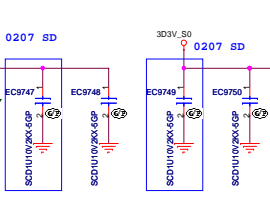
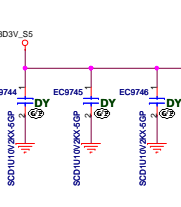
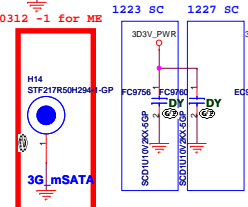
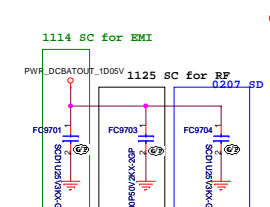
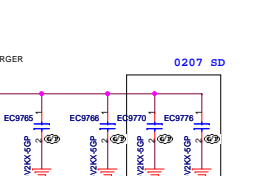
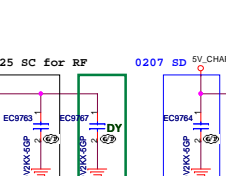
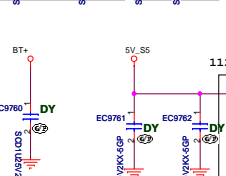
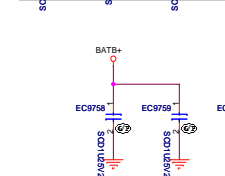
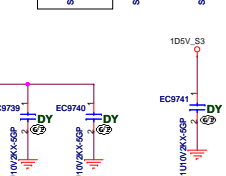
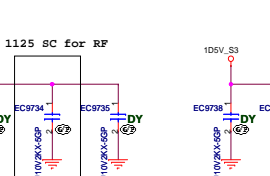
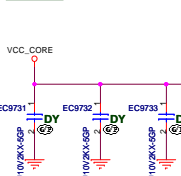
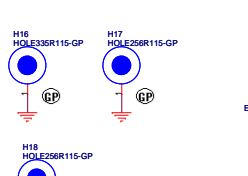
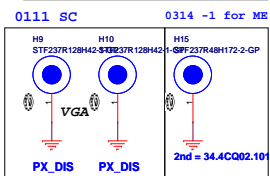
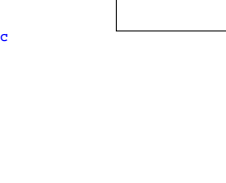
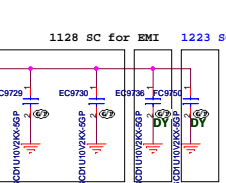
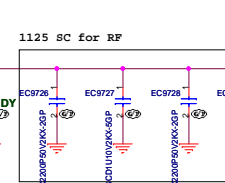
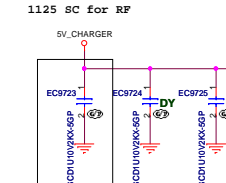
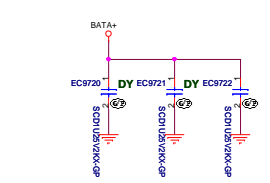
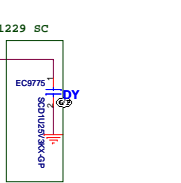
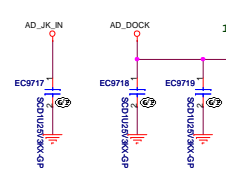
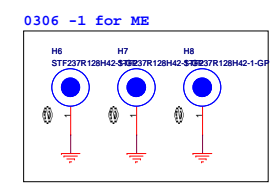
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緯創資通		Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichia, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
TOUCH PANEL		
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Check test point

- 303V_S0 1 AFTP1
- 303V_AUX_S0 1 AFTP7
- 303V_S0 1 AFTP8
- 5V_S0 1 AFTP9
- 19.27 PM_PWRBTNA <<< AFTP10
- 1.4/1.1 H_CPUVWRGD AFTP12
- 27.36,107 SS_ENABLE <<< AFTP13
- 5.18,27.31,32.36,65.67,71.75,82.83,105 PLT_RSTA >>> AFTP13

Test Point放在Dimm Door打開可量測處



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<Variant Name>

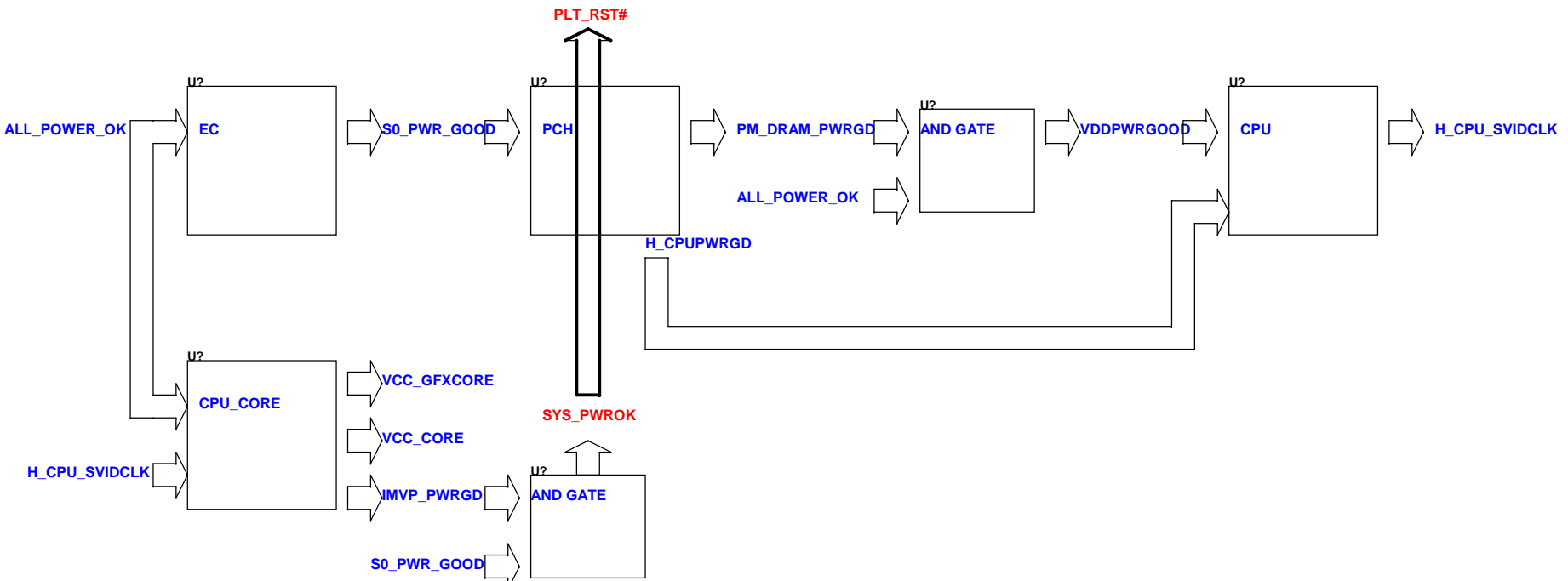
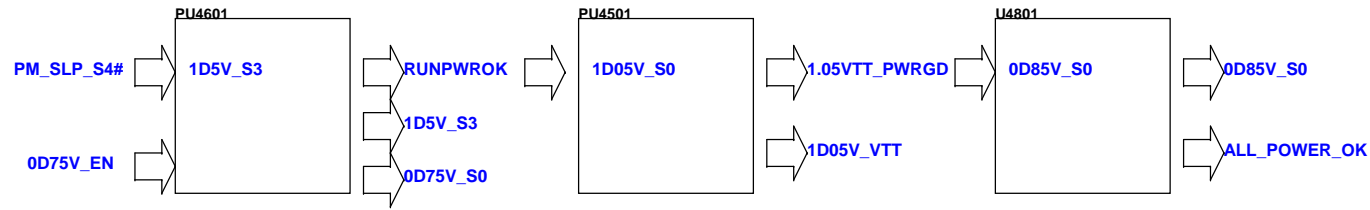
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsein 221, Taiwan, R.O.C.

Part No: **UNUSED PARTS/EMI Capacitors**

Size: **BAD40 HC**

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Power Sequence



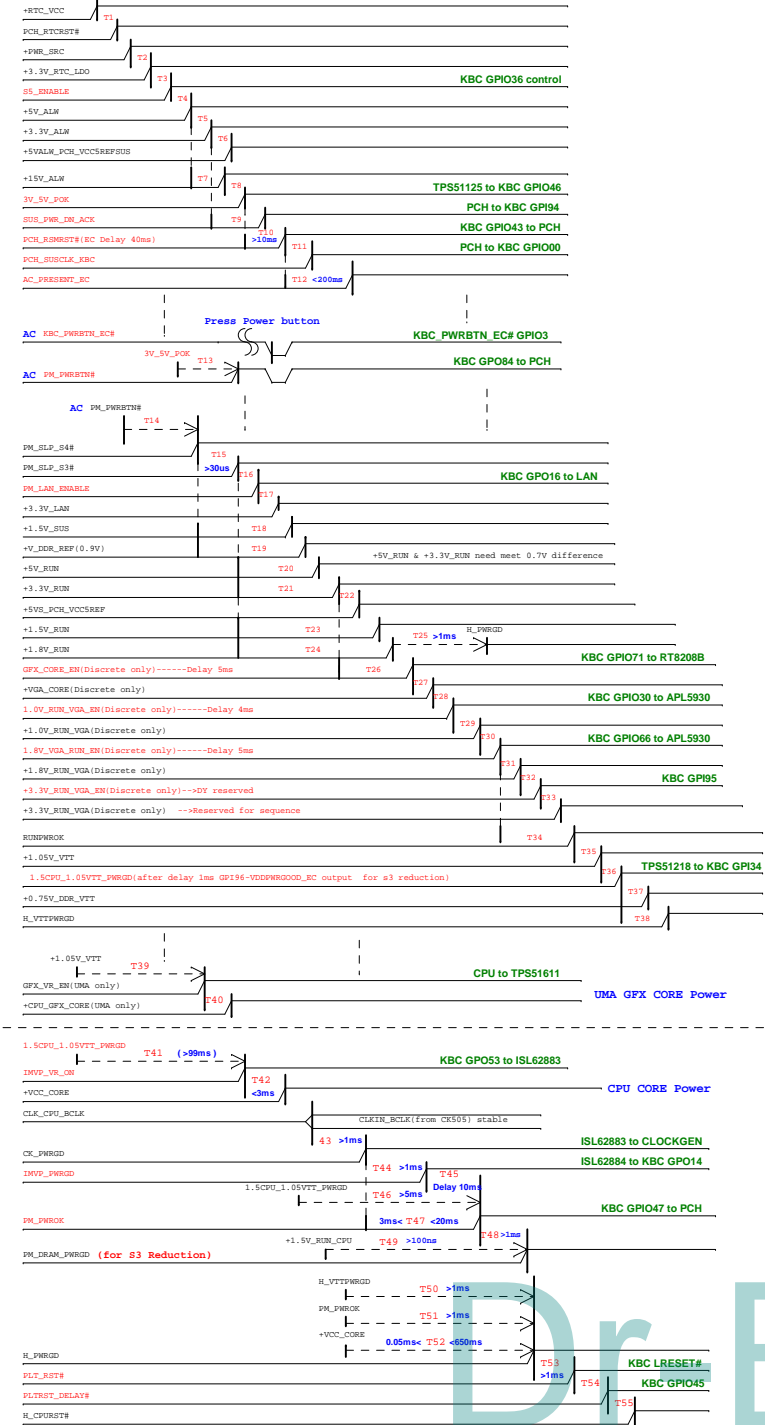
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Change History		
Size A3	Document Number BAD40_HC	Rev 1
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Intel-Power Up Sequence

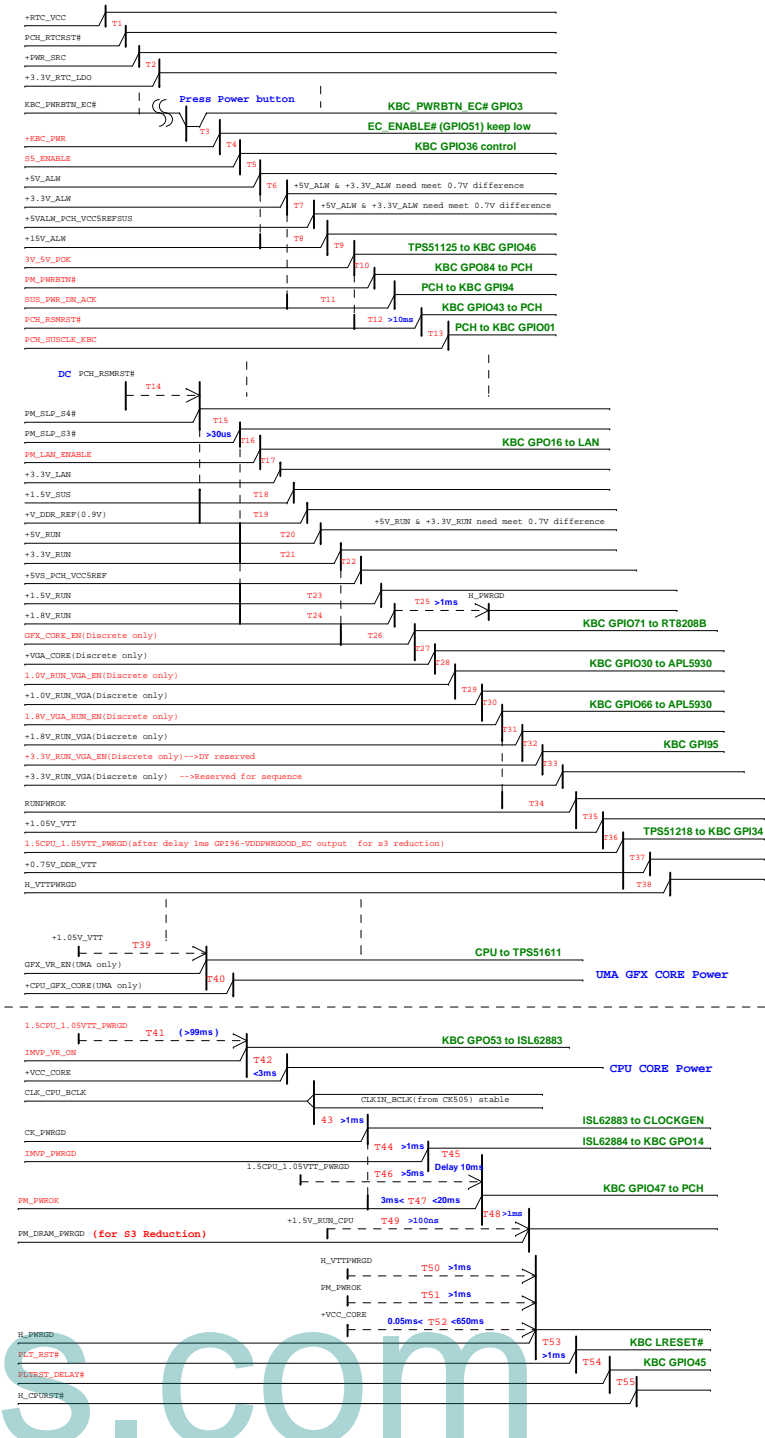
(AC mode)

red word: KBC GPIO

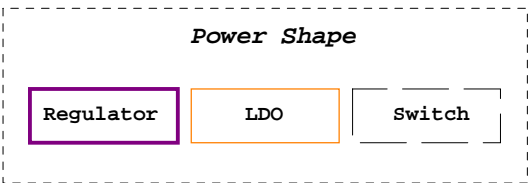
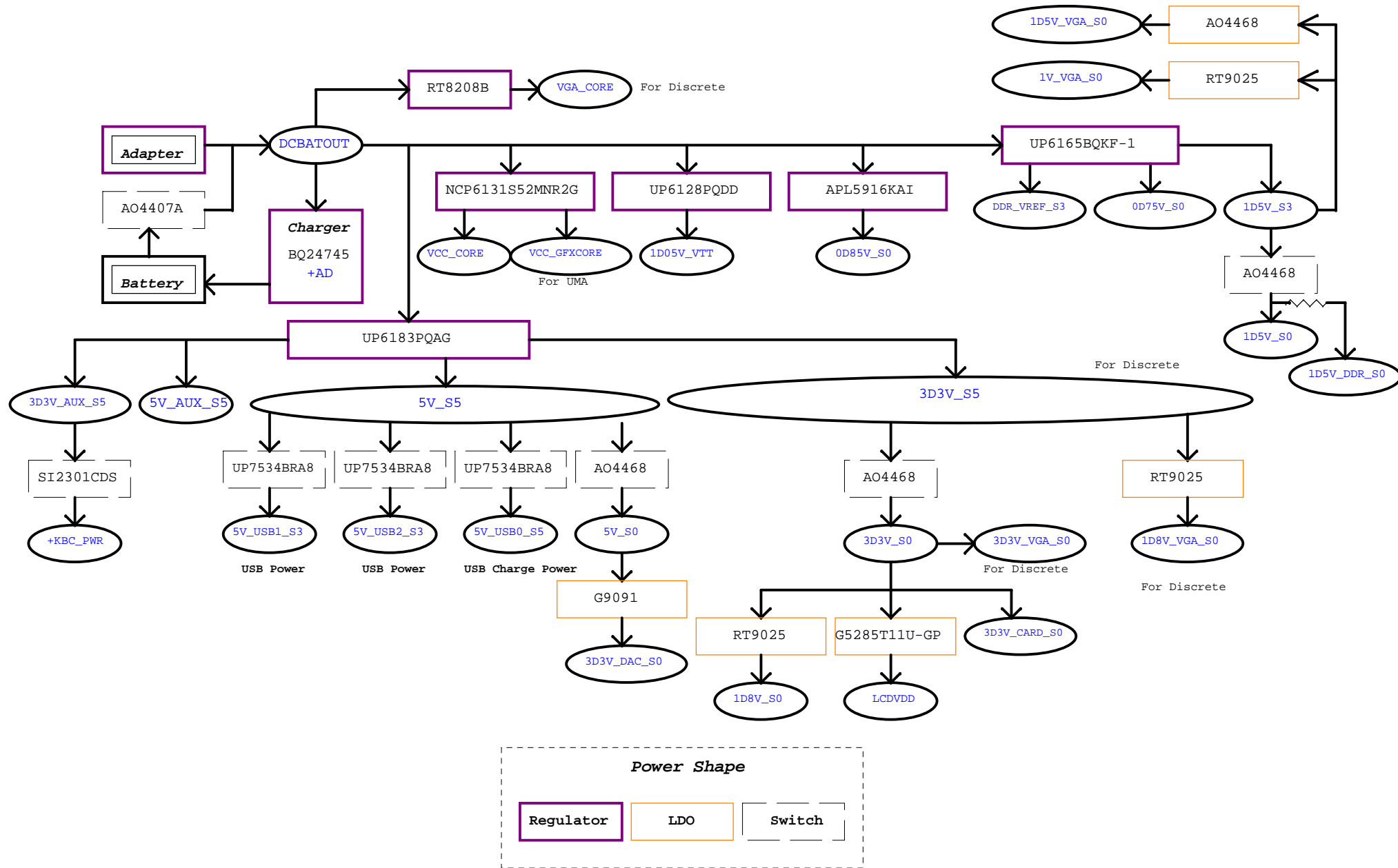


(DC mode)

red word: KBC GPIO



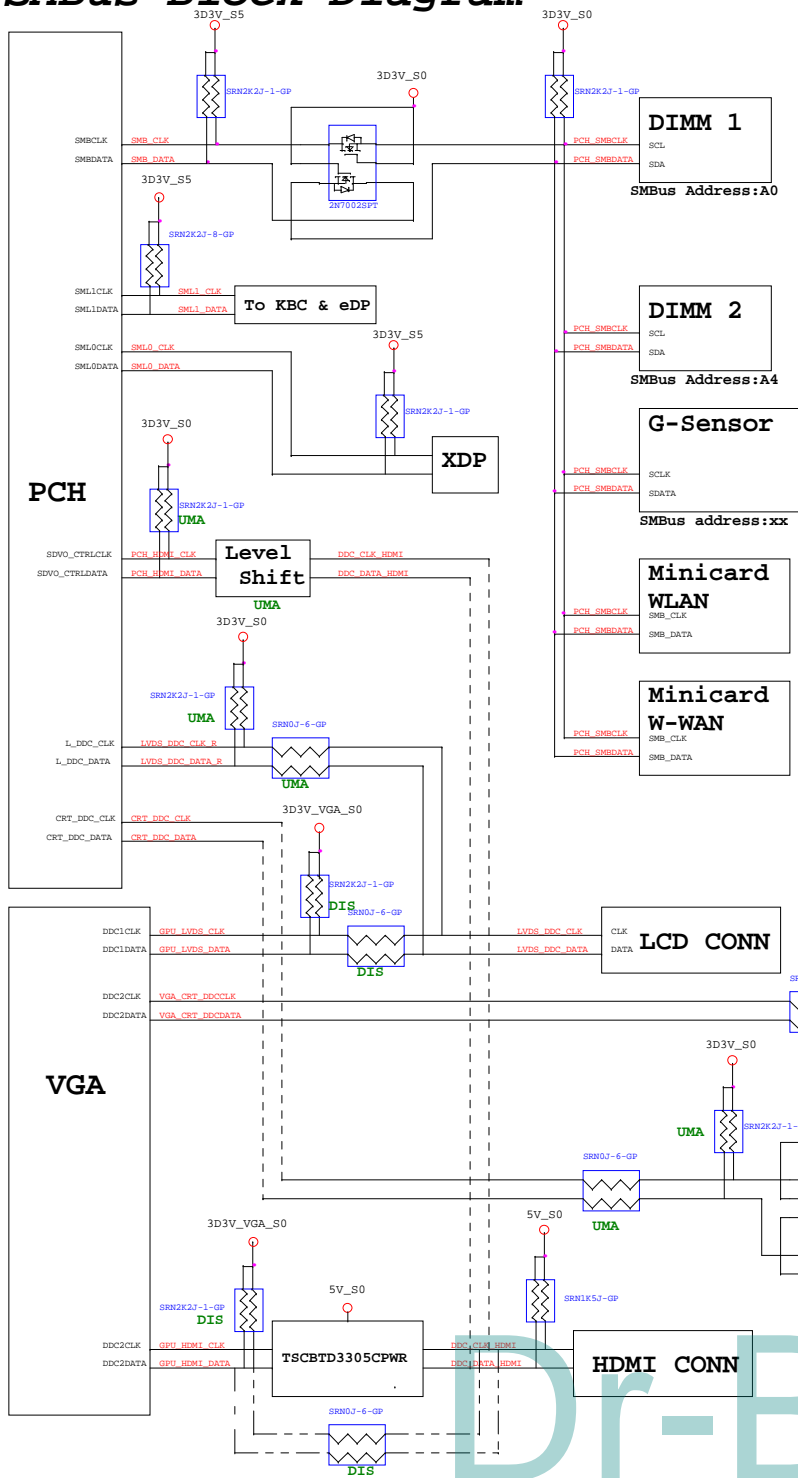
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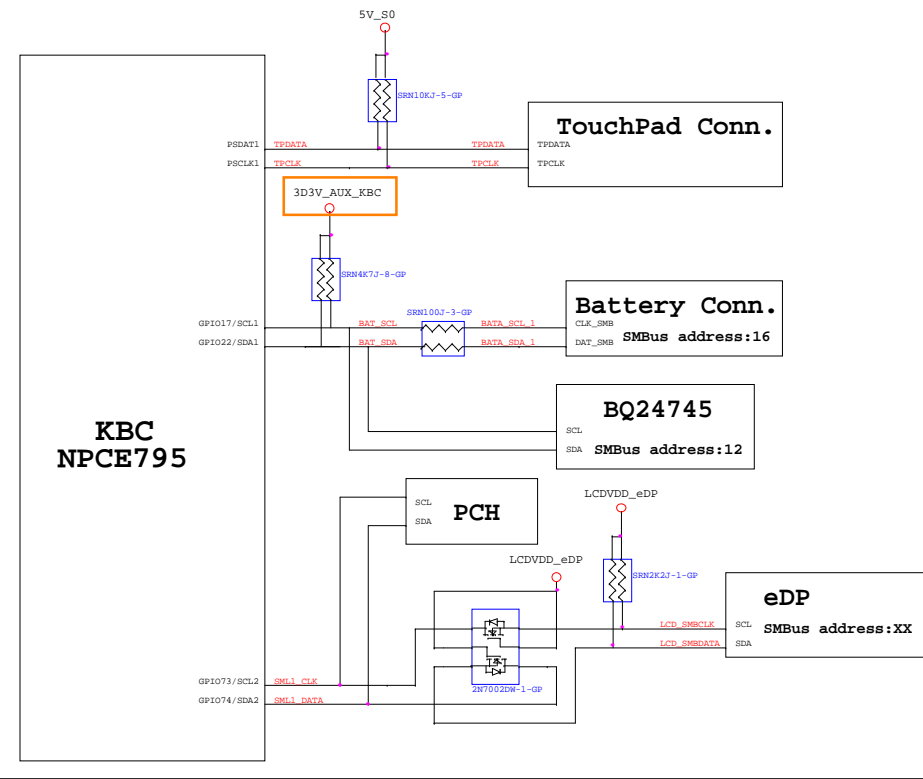
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HR PX		緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: Power Block Diagram			
Size: A3	Document Number: BAD40 HC	Rev: 1	
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PCH SMBus Block Diagram

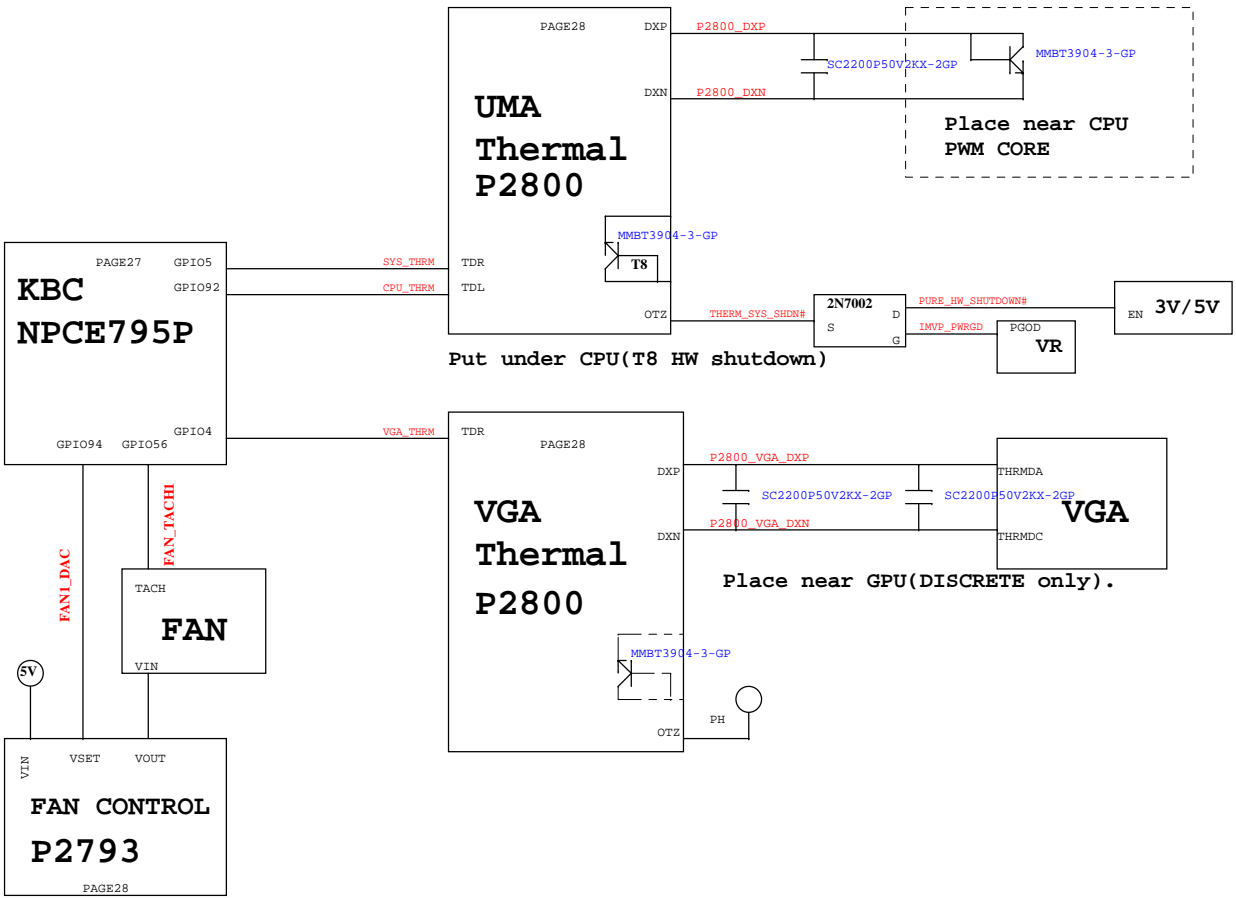


KBC SMBus Block Diagram

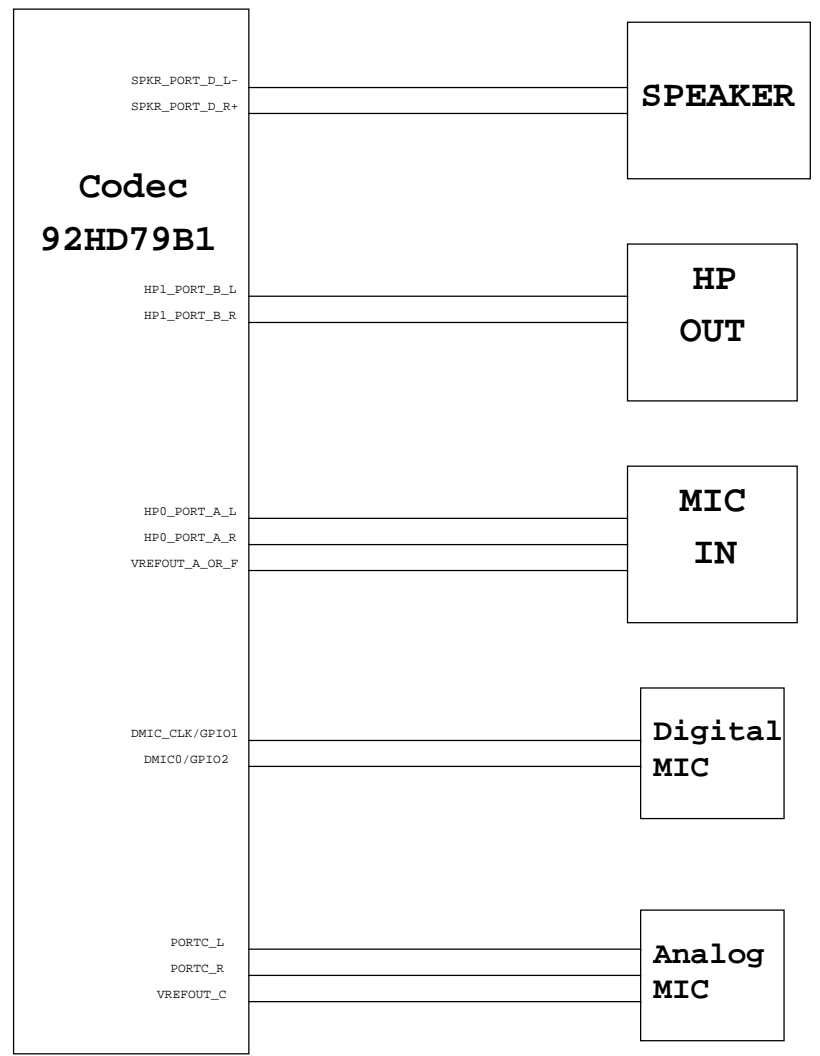


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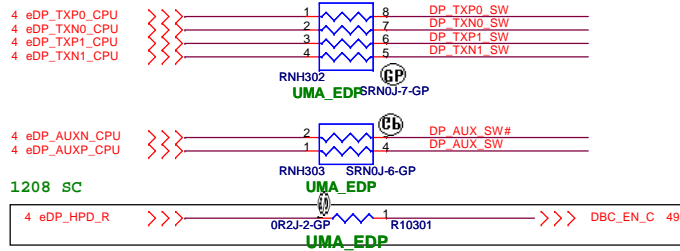
Thermal Block Diagram



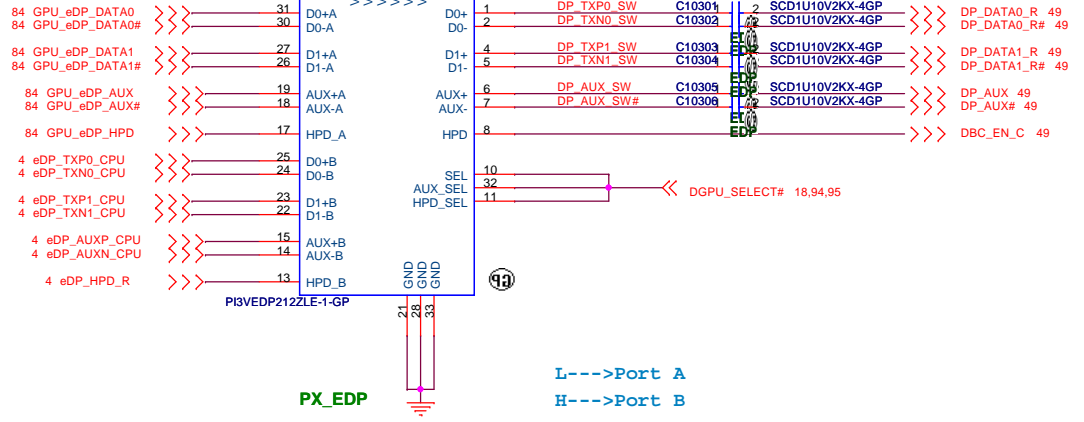
Audio Block Diagram



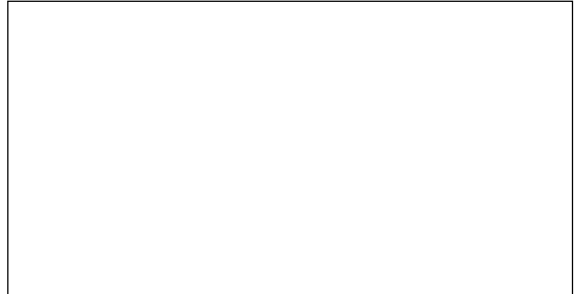
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From GPU



1117 SC del eDP SMBUS



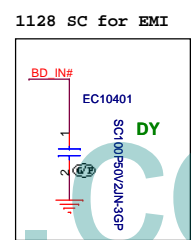
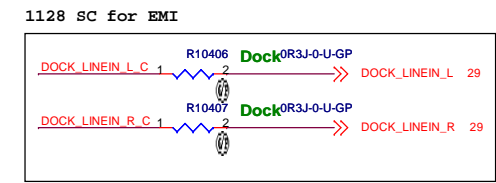
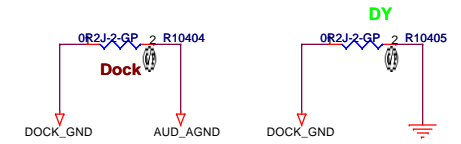
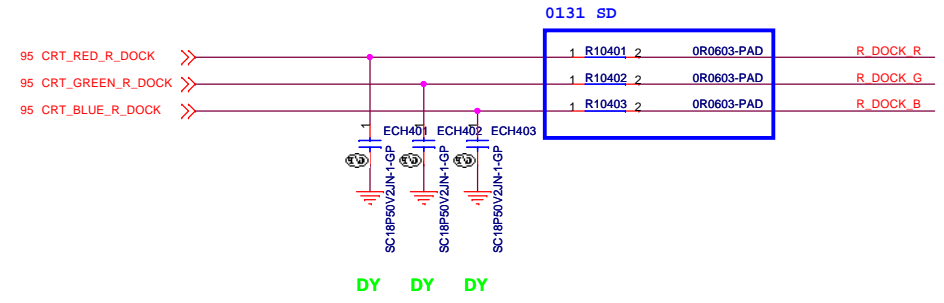
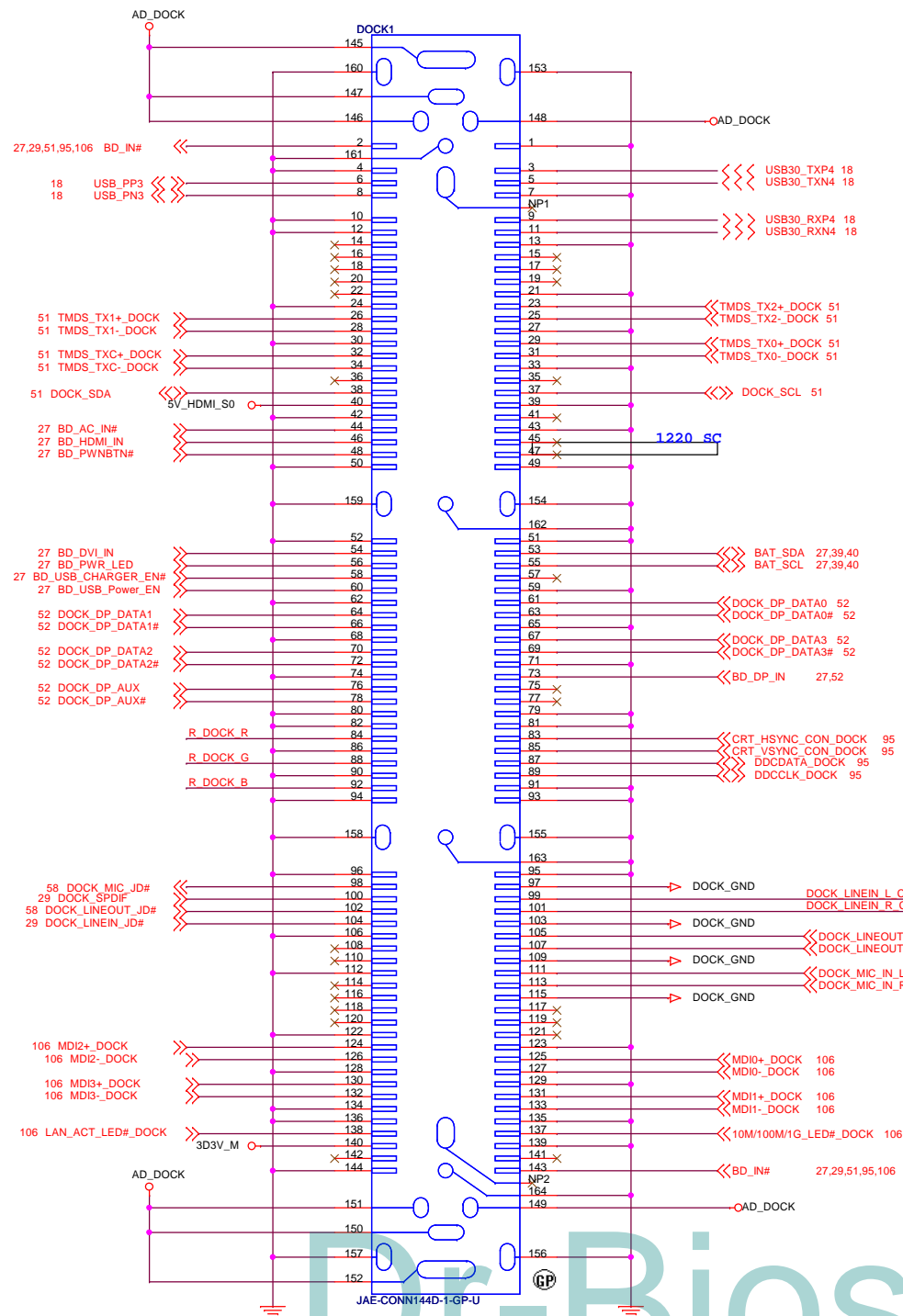
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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title Switch GFX DP

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<Variant Name>

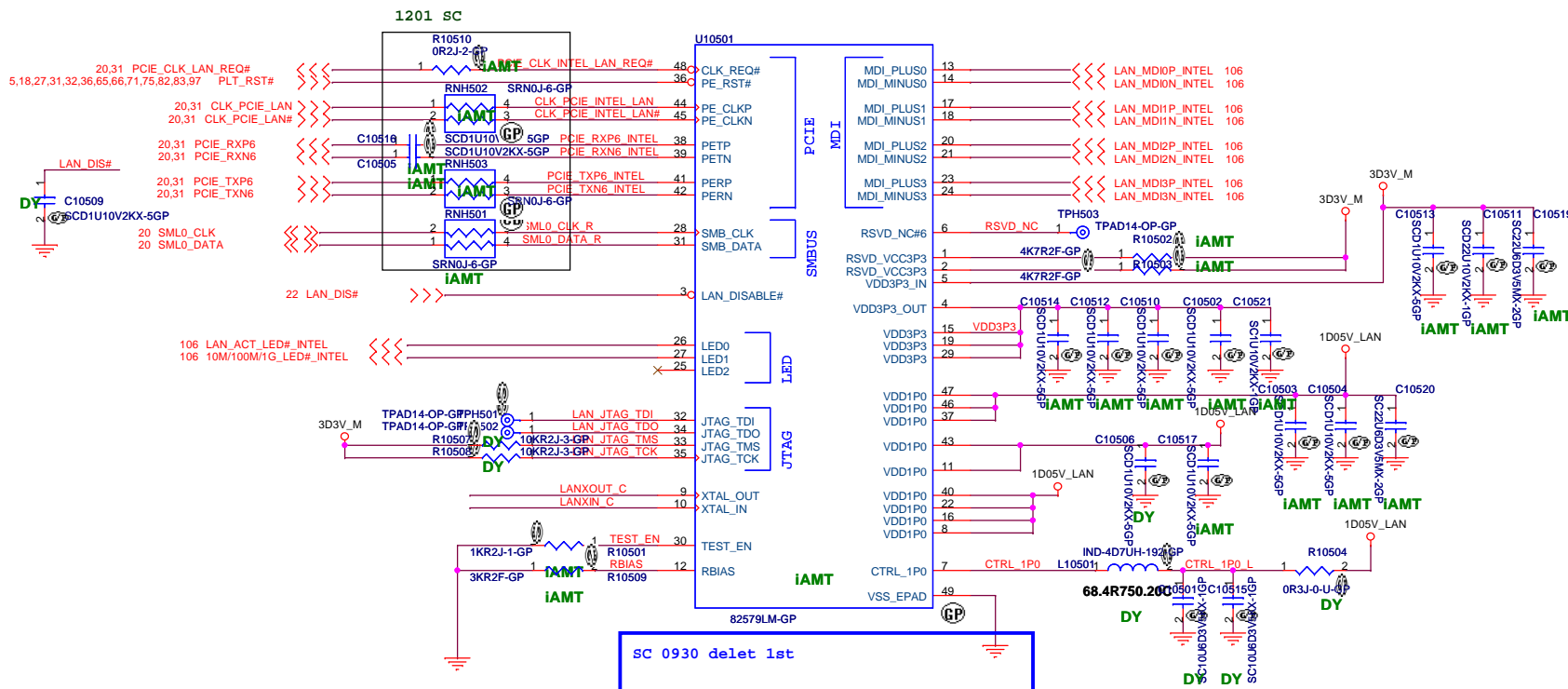
緯創資通 **Wistron Corporation**
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **BOTTOM DOCKING**

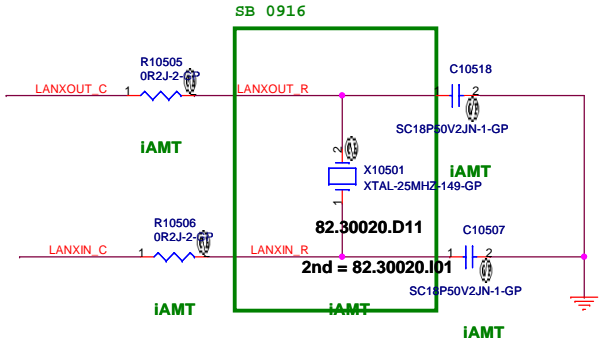
Size A3 Document Number **BAD40 HC** Rev **1**

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SC 0930 delet 1st



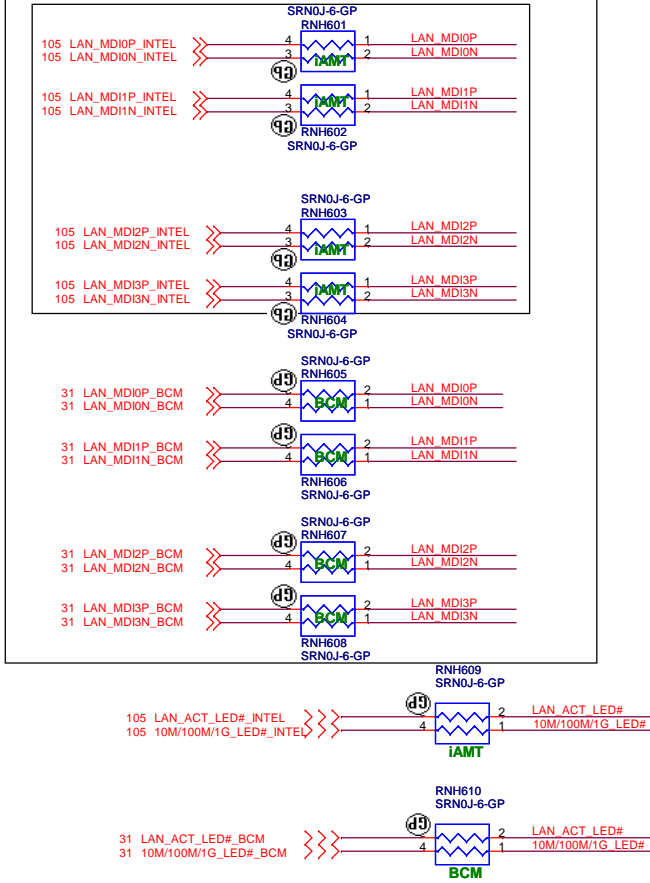
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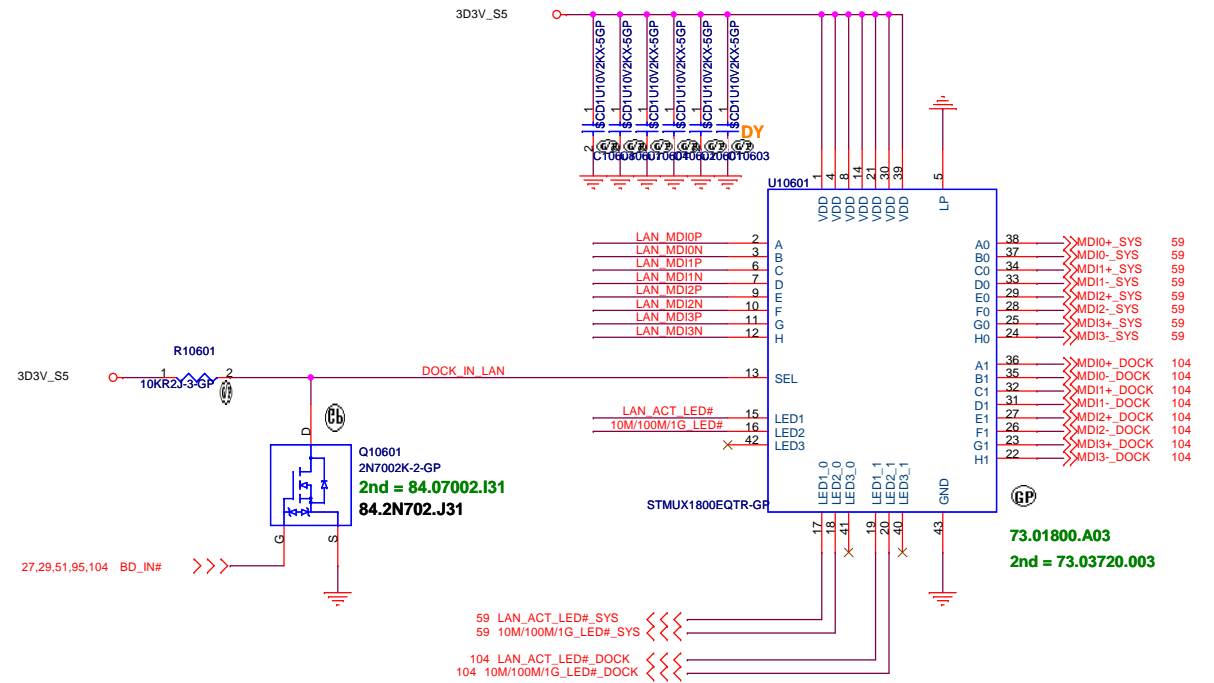
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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
LAN INTEL 82579			
Size	Document Number		Rev
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1201 SC

1206 SC swap for layout



LAN switch



- 59 LAN_ACT_LED#_SYS
- 59 10M/100M/1G_LED#_SYS
- 104 LAN_ACT_LED#_DOCK
- 104 10M/100M/1G_LED#_DOCK

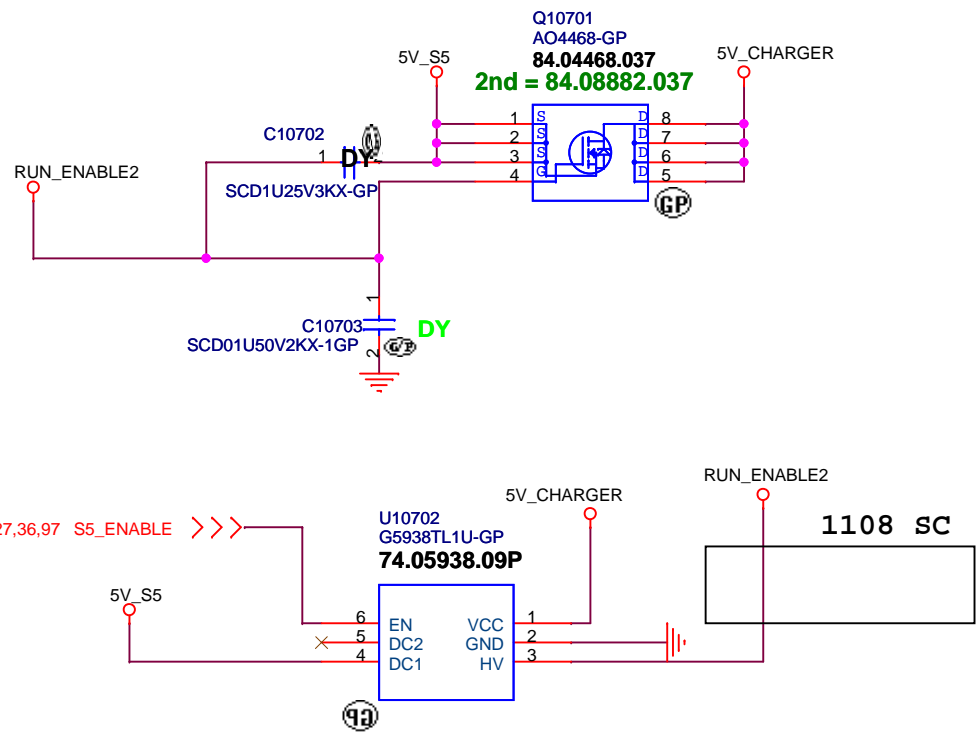
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to X0	L	SYSTEM
to X1	H	DOCK

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	LAN SWITCH	
Size A3	Document Number	Rev
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USB charger @ USB30 BD

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<Variant Name>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
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USB Charger/ 5V S5		
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reserve

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<Core Design>

緯創資通			Wistron Corporation		
			21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
USB2 HUB AU6256					
Size	Document Number				Rev
	BAD40 HC				1
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