Model Name : JE50-HR/SJV50-HR
Compal Project Name : P5WE0/P5WS0
File Name : LA-6901P

Compal Confidential

JE50-HR/SJV50-HR(P5WE0/P5WS0) M/B Schematics Document

Intel Sandy Bridge Processor with DDRIII + Cougar Point PCH
Nvidia N12P GS/GV

2010-11-1

REV:0.5

Security Classification	Compal Secret Data		
Issued Date	2010/11/1	Deciphered Date	2011/11/1

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Title: Cover Page			
Size: Custom	Document Number: JE50-HR/SJV50-HR M/B Schematics		Rev: 0.5
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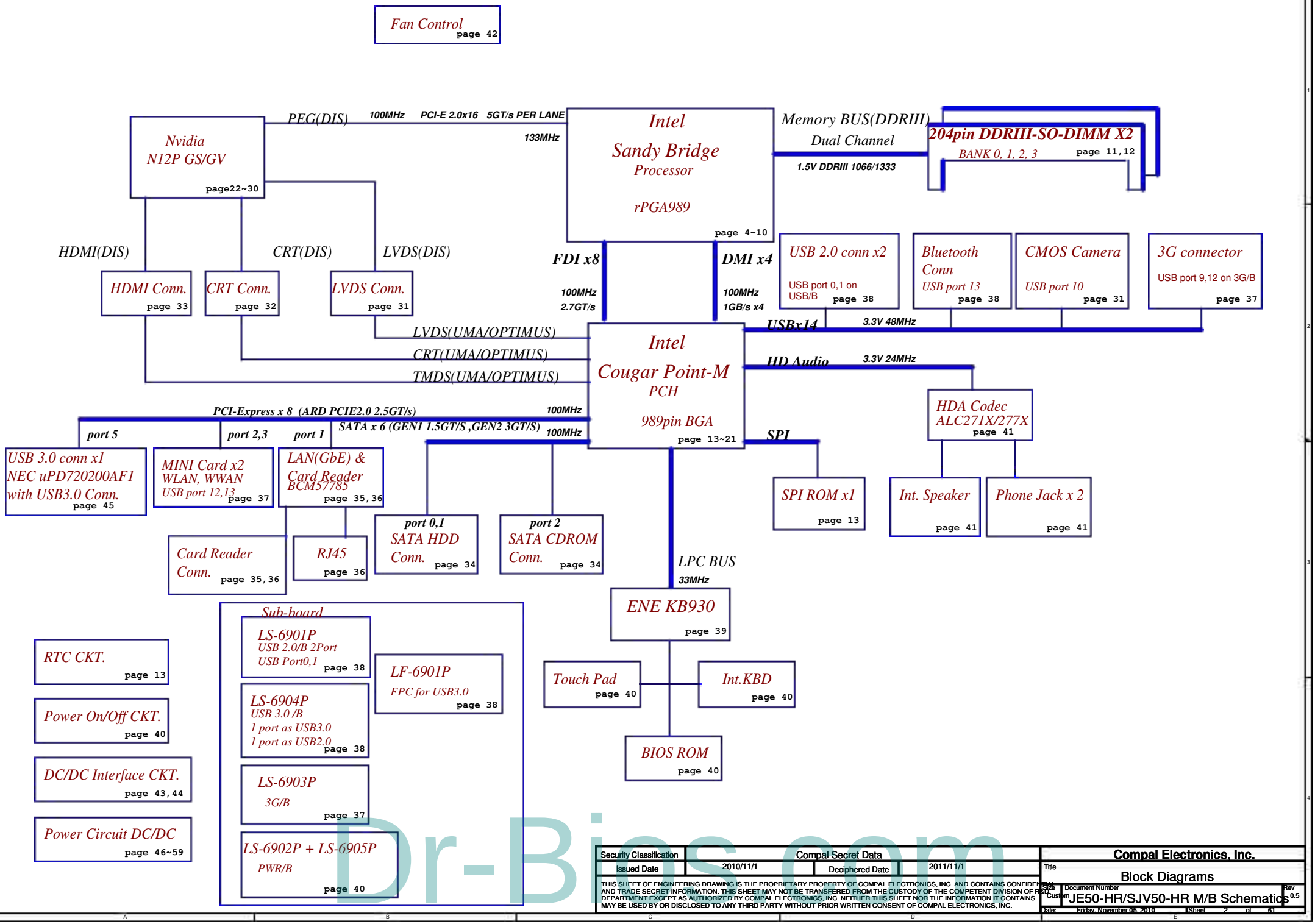

Security Classification	Compal Secret Data		
Issued Date	2010/11/1	Deciphered Date	2011/11/1

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Title: Block Diagrams

Size: Custom	Document Number: JE50-HR/SJV50-HR M/B Schematics	Rev: 0.5
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VSDGPU	+1.0VSPDGPU to +1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VCCPP to +1.05VS_VCCP switched power rail for CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VCCP to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VS to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+1.8VSDGPU	+1.8VS to +1.8VSDGPU switched power rail for GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+3V_LAN	+3VALW to +3V_LAN power rail for LAN	ON	ON	ON*
+3VALW_PCH	+3VALW to +3VALW_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VALW_PCH	+5VALW to +5VALW_PCH power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address

PCH SM Bus address

Device	Address
Clock Generator (9LVS3199AKLFT, RTM890N-631-VB-GRT)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

3G & BT & USB30 & USB20 Config

3G SKU: 3G@ USB30 SKU: USB30@ OPTMIUS SKU: OPT@

BT SKU: BT@ USB20 SKU: USB20@ Non-OPTMIUS SKU: NOPT@

LAN Chip A0 version: A0@ N12P-GS: GS@

LAN chip B0 Version: B0@ N12P-GV: GV@

BOM Config

UMA Only: BT@/3G@/USB30@/UMA@/UMAO@/NOPT@/A0@

OPTIMUS(N12P-GS) : BT@/3G@/USB30@/UMA@/DIS@/X76@/OPT@/A0@/GS@

DIS Only(N12P-GS) : BT@/3G@/USB30@/DISO@/DIS@/X76@/NOPT@/A0@/GS@

OPTIMUS(N12P-GV) : BT@/3G@/USB30@/UMA@/DIS@/X76@/OPT@/A0@/GV@

DIS Only(N12P-GV) : BT@/3G@/USB30@/DISO@/DIS@/X76@/NOPT@/A0@/GV@

VRAM P/N :

64*16

Samsung : SA000035700

Hynix : SA000032400/SA0000324C0

128*16

Samsung : SA00003MQ40

Hynix : SA00003VS00

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

EVT
EVT2
DVT
PVT
Pre-MP

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	1.0
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
UMA Only	UMAO@
UMA with OPTIMUS	UMA@
Dis with OPTIMUS	DIS@
DIS Only	DISO@
OPTIMUS	OPT@
Non-OPTIMUS	NOPT@
3G	3G@
Blue Tooth	BT@
USB2.0	USB20@
USB3.0	USB30@
VRAM	X76@
Connector	CONN@
Unpop	@
LAN Chip A0 version	A0@
LAN Chip B0 version	B0@
N12P-GS	GS@
N12P-GV	GV@

USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB/B (Right Side)
		1	USB/B (Right Side)
	UHCI1	2	USB3.0 colay USB2.0 Conn.
		3	USB/B Colay USB3.0
	UHCI2	4	
		5	
	UHCI3	6	
		7	
EHCI2	UHCI4	8	Mini Card 1(WLAN)
		9	3G/B(WWAN)
	UHCI5	10	Camera
		11	Mini Card 2(Reserved)
	UHCI6	12	3G/B(SIM Card)
		13	BlueTooth

Security Classification	Compal Secret Data		
Issued Date	2010/11/1	Deciphered Date	2011/11/1

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Title: Notes List

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ZZZ
DA60000KC00

+1.05VS_VTT

R517
24.9_0402_1%

PEG_ICOMPI and PEG_RCOMPO signals should be shorted and routed,
max length = 500 mils,trace width=4mils
PEG_ICOMPO signals should be routed with - max length = 500 mils,trace width=12mils
spacing =15mils

JCPU1A

PEG_ICOMPI J22
PEG_ICOMPO J21
PEG_RCOMPO H22
PEG_COMP

DMI
15 DMI_CRX_PTX_N0 B27 DMI_RX#[0]
15 DMI_CRX_PTX_N1 B25 DMI_RX#[1]
15 DMI_CRX_PTX_N2 A25 DMI_RX#[2]
15 DMI_CRX_PTX_N3 B24 DMI_RX#[3]
15 DMI_CRX_PTX_P0 B28 DMI_RX[0]
15 DMI_CRX_PTX_P1 B26 DMI_RX[1]
15 DMI_CRX_PTX_P2 A24 DMI_RX[2]
15 DMI_CRX_PTX_P3 B23 DMI_RX[3]
15 DMI_CTX_PRX_N0 G21 DMI_TX#[0]
15 DMI_CTX_PRX_N1 E22 DMI_TX#[1]
15 DMI_CTX_PRX_N2 F21 DMI_TX#[2]
15 DMI_CTX_PRX_N3 D21 DMI_TX#[3]
15 DMI_CTX_PRX_P0 G22 DMI_TX[0]
15 DMI_CTX_PRX_P1 D22 DMI_TX[1]
15 DMI_CTX_PRX_P2 F20 DMI_TX[2]
15 DMI_CTX_PRX_P3 C21 DMI_TX[3]

Intel(R) FDI
15 FDI_CTX_PRX_N0 A21 FDI0_TX#[0]
15 FDI_CTX_PRX_N1 H19 FDI0_TX#[1]
15 FDI_CTX_PRX_N2 E19 FDI0_TX#[2]
15 FDI_CTX_PRX_N3 F18 FDI0_TX#[3]
15 FDI_CTX_PRX_N4 B21 FDI1_TX#[0]
15 FDI_CTX_PRX_N5 C20 FDI1_TX#[1]
15 FDI_CTX_PRX_N6 D18 FDI1_TX#[2]
15 FDI_CTX_PRX_N7 E17 FDI1_TX#[3]
15 FDI_CTX_PRX_P0 A22 FDI0_TX[0]
15 FDI_CTX_PRX_P1 G19 FDI0_TX[1]
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15 FDI_CTX_PRX_P3 G18 FDI0_TX[3]
15 FDI_CTX_PRX_P4 B20 FDI1_TX[0]
15 FDI_CTX_PRX_P5 C19 FDI1_TX[1]
15 FDI_CTX_PRX_P6 D19 FDI1_TX[2]
15 FDI_CTX_PRX_P7 E17 FDI1_TX[3]
15 FDI_FSYNC0 J18 FDI0_FSYNC
15 FDI_FSYNC1 J17 FDI1_FSYNC
15 FDI_INT H20 FDI_INT
15 FDI_LSYNC0 J19 FDI0_LSYNC
15 FDI_LSYNC1 H17 FDI1_LSYNC

eDP
EDP_COMP A18 eDP_COMPIO
A17 eDP_ICOMPO
B16 eDP_HPD
C15 eDP_AUX
D15 eDP_AUX#
C17 eDP_TX[0]
E16 eDP_TX[1]
C16 eDP_TX[2]
G15 eDP_TX[3]
C18 eDP_TX#[0]
E16 eDP_TX#[1]
D16 eDP_TX#[2]
E15 eDP_TX#[3]

PCI EXPRESS* - GRAPHICS

PEG_RX#[0] K33 PEG_GTX_C_HRX_N15 C46 1 2 DIS@ 0.22U_0402_10V6K PEG_GTX_HRX_N15
PEG_RX#[1] M35 PEG_GTX_C_HRX_N14 C49 1 2 DIS@ 0.22U_0402_10V6K PEG_GTX_HRX_N14
PEG_RX#[2] L34 PEG_GTX_C_HRX_N13 C51 1 2 DIS@ 0.22U_0402_10V6K PEG_GTX_HRX_N13
PEG_RX#[3] J35 PEG_GTX_C_HRX_N12 C53 1 2 DIS@ 0.22U_0402_10V6K PEG_GTX_HRX_N12
PEG_RX#[4] J32 PEG_GTX_C_HRX_N11 C60 1 2 DIS@ 0.22U_0402_10V6K PEG_GTX_HRX_N11
PEG_RX#[5] H34 PEG_GTX_C_HRX_N10 C71 1 2 DIS@ 0.22U_0402_10V6K PEG_GTX_HRX_N10
PEG_RX#[6] H31 PEG_GTX_C_HRX_N9 C75 1 2 DIS@ 0.22U_0402_10V6K PEG_GTX_HRX_N9
PEG_RX#[7] G33 PEG_GTX_C_HRX_N8 C82 1 2 DIS@ 0.22U_0402_10V6K PEG_GTX_HRX_N8
PEG_RX#[8] G30 PEG_GTX_C_HRX_N7 C92 1 2 DIS@ 0.22U_0402_10V6K PEG_GTX_HRX_N7
PEG_RX#[9] E35 PEG_GTX_C_HRX_N6 C93 1 2 DIS@ 0.22U_0402_10V6K PEG_GTX_HRX_N6
PEG_RX#[10] E34 PEG_GTX_C_HRX_N5 C102 1 2 DIS@ 0.22U_0402_10V6K PEG_GTX_HRX_N5
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PEG_RX[3] H35 PEG_GTX_C_HRX_P12 C56 1 2 DIS@ 0.22U_0402_10V6K PEG_GTX_HRX_P12
PEG_RX[4] H32 PEG_GTX_C_HRX_P11 C66 1 2 DIS@ 0.22U_0402_10V6K PEG_GTX_HRX_P11
PEG_RX[5] G34 PEG_GTX_C_HRX_P10 C68 1 2 DIS@ 0.22U_0402_10V6K PEG_GTX_HRX_P10
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PEG_TX#[13] D28 PEG_HTX_GRX_N2 C556 1 2 DIS@ 0.22U_0402_10V6K PEG_HTX_C_GRX_N2
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PEG_TX[2] M30 PEG_HTX_GRX_P13 C533 1 2 DIS@ 0.22U_0402_10V6K PEG_HTX_C_GRX_P13
PEG_TX[3] L31 PEG_HTX_GRX_P12 C536 1 2 DIS@ 0.22U_0402_10V6K PEG_HTX_C_GRX_P12
PEG_TX[4] L28 PEG_HTX_GRX_P11 C539 1 2 DIS@ 0.22U_0402_10V6K PEG_HTX_C_GRX_P11
PEG_TX[5] K30 PEG_HTX_GRX_P10 C541 1 2 DIS@ 0.22U_0402_10V6K PEG_HTX_C_GRX_P10
PEG_TX[6] K27 PEG_HTX_GRX_P9 C543 1 2 DIS@ 0.22U_0402_10V6K PEG_HTX_C_GRX_P9
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PEG_TX[13] D27 PEG_HTX_GRX_P2 C557 1 2 DIS@ 0.22U_0402_10V6K PEG_HTX_C_GRX_P2
PEG_TX[14] F26 PEG_HTX_GRX_P1 C559 1 2 DIS@ 0.22U_0402_10V6K PEG_HTX_C_GRX_P1
PEG_TX[15] D25 PEG_HTX_GRX_P0 C561 1 2 DIS@ 0.22U_0402_10V6K PEG_HTX_C_GRX_P0

Sandy Bridge_rPGA_Rev0p61
CONN@

PEG_GTX_HRX_N[0..15] 22
PEG_GTX_HRX_P[0..15] 22
PEG_HTX_C_GRX_N[0..15] 22
PEG_HTX_C_GRX_P[0..15] 22

+1.05VS_VTT

R145
24.9_0402_1%

EDP_COMP

eDP_COMPIO and ICOMPO signals should be shorted near balls,
Trace Width for EDP_COMPIO=4mils,
EDP_ICOMPO=12mils,
and both length less than 500 mils...
should not be left floating
,even if disable eDP function...

Typ- suggest 220nF. The change in AC capacitor value from 100nF to 220nF is to enable compatibility with future platforms having PCIE Gen3 (8GT/s)

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Title: PROCESSOR(1/7) DMI,FDI,PEG

Size	Document Number	Rev
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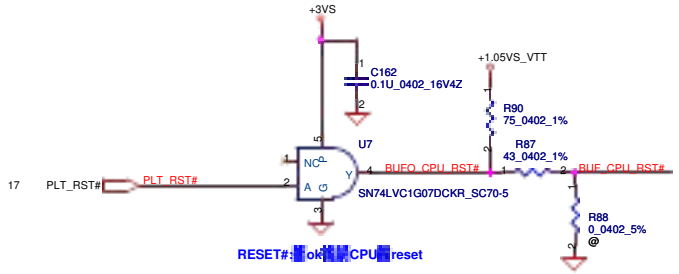
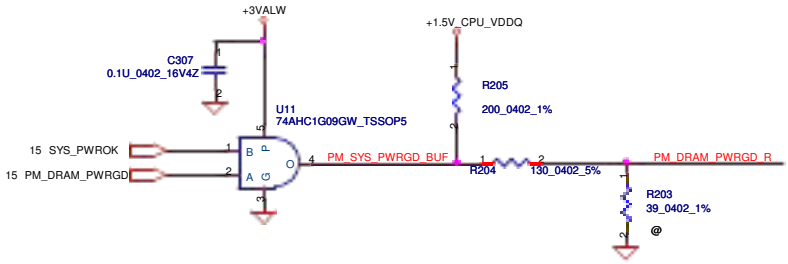
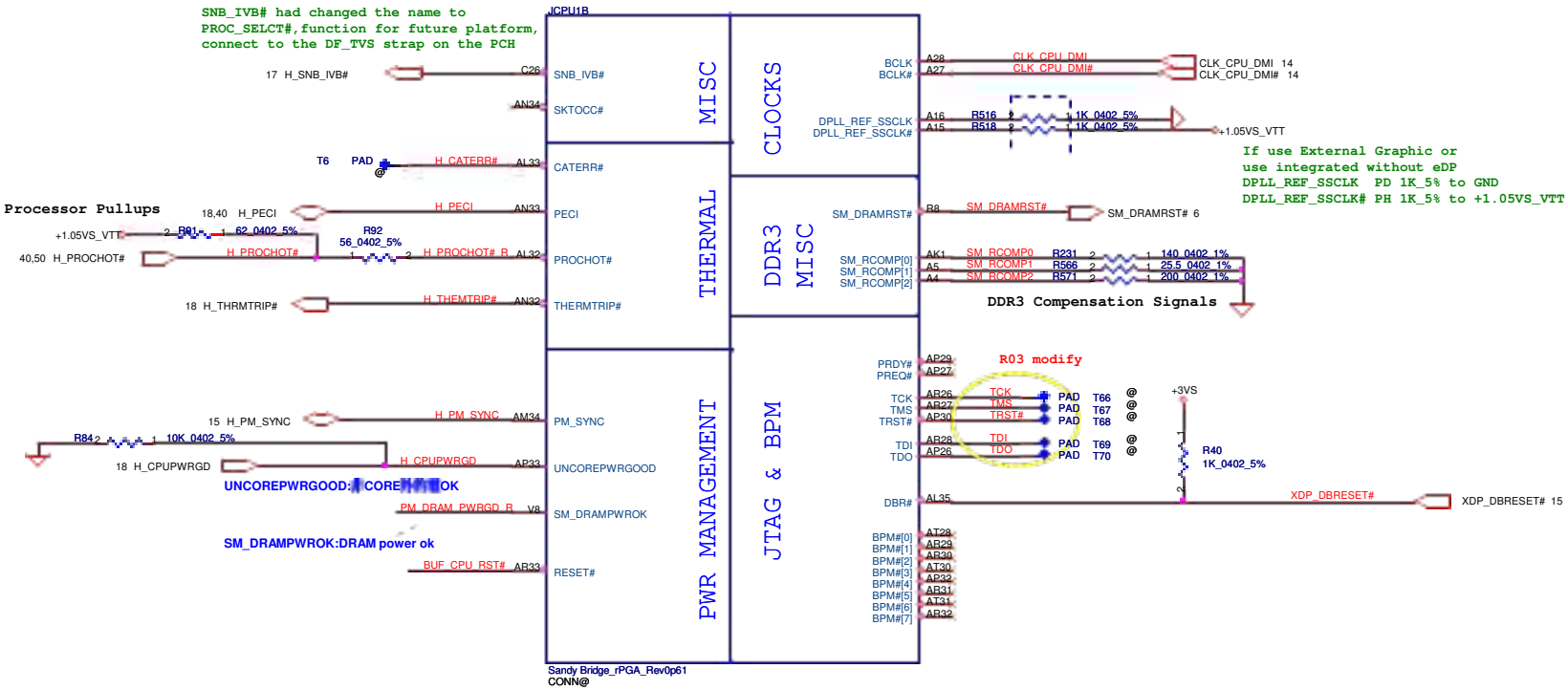
Buffered reset to CPU





SNB_IVB# had changed the name to PROC_SELCT#,function for future platform, connect to the DF_TVS strap on the PCH



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Issued Date	2010/11/1	Deciphered Date	2011/11/1

Compal Electronics, Inc.

Title: PROCESSOR(2/7) PM,XDP,CLK

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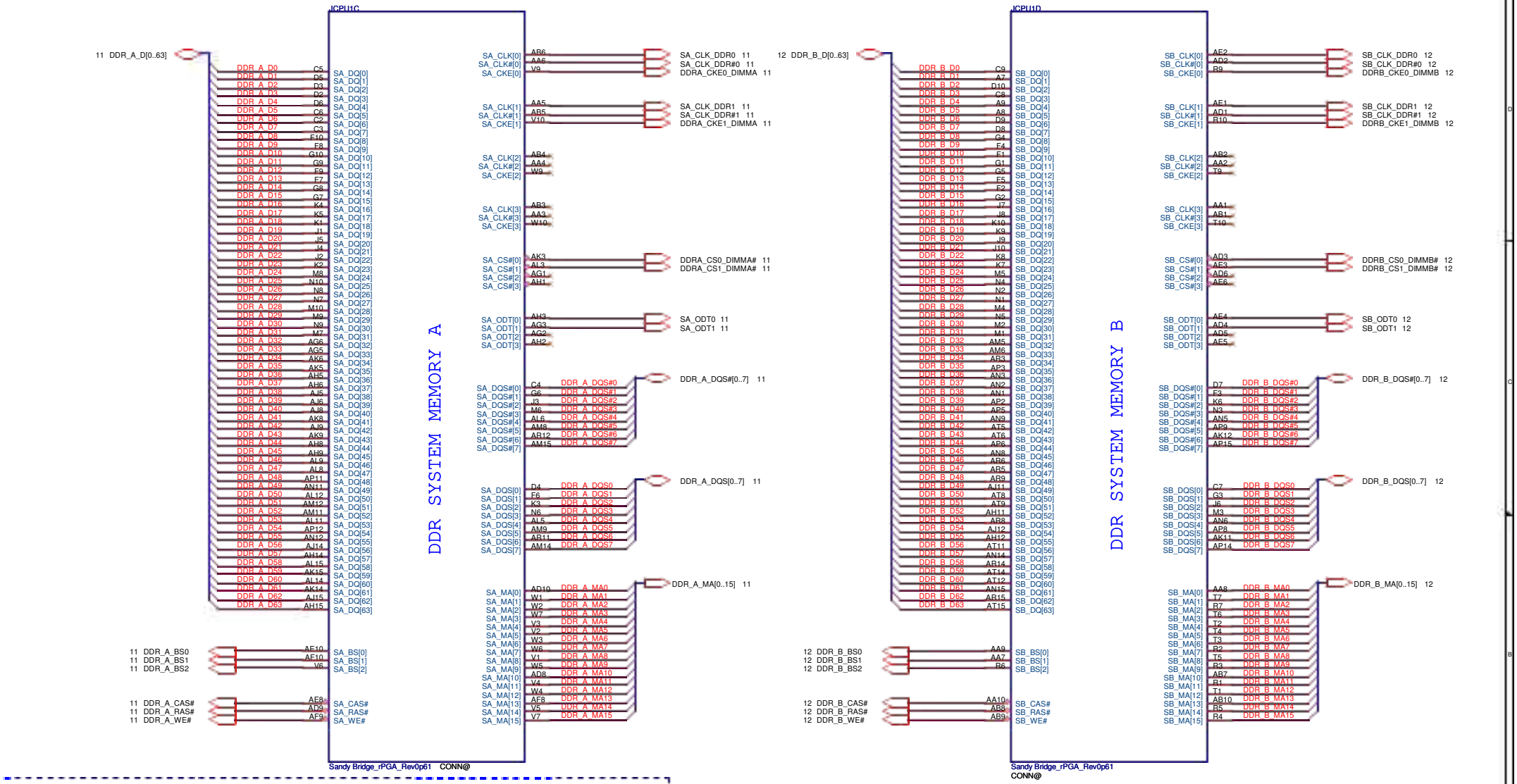
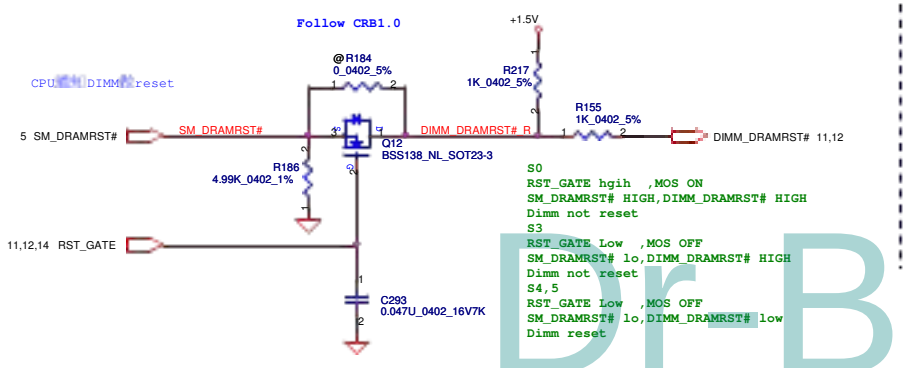
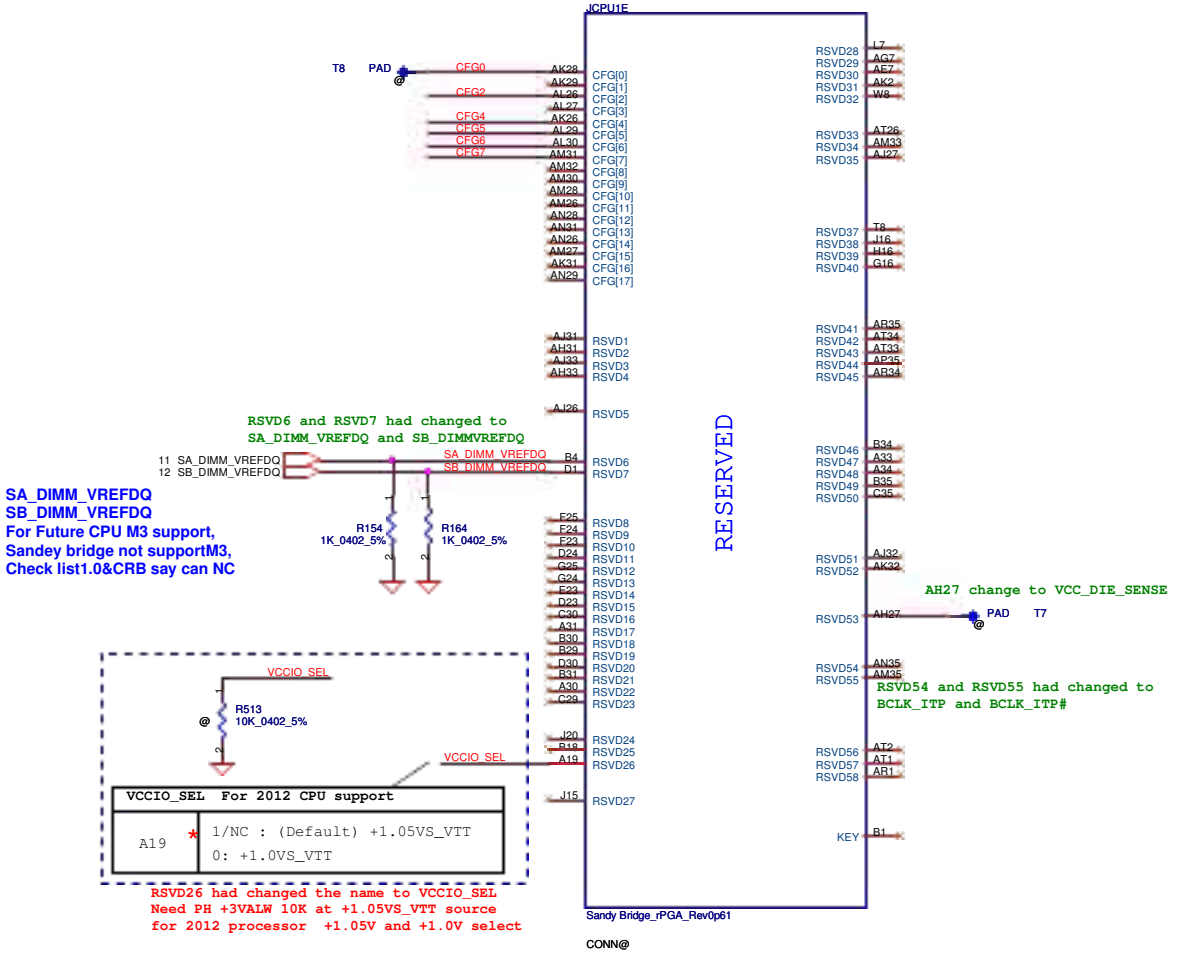




Security Classification	Compal Secret Data		
Issued Date	2010/11/1	Deciphered Date	2011/11/1

Compal Electronics, Inc.			
Title: PROCESSOR(3/7) DDRIII			
Size: Custom	Document Number: JE50-HR/SJV50-HR M/B Schematics		Rev: 0.5
Date: Friday, November 05, 2010		Sheet 6 of 61	

CFG Straps for Processor



CFG2

R112 1K_0402_5%

PEG Static Lane Reversal – CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed

CFG4

R109 1K_0402_5%

Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

CFG6
CFG5

R107 1K_0402_5% @ R108 1K_0402_5%

PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 – Device 1 functions 1 and 2 disabled 10: x8, x8 – Device 1 function 1 enabled ; function 2 disabled 01: Reserved – (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 – Device 1 functions 1 and 2 enabled

CFG7

R102 1K_0402_5%

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

Security Classification	Compal Secret Data		
Issued Date	2010/11/1	Deciphered Date	2011/11/1

Compal Electronics, Inc.

Title: PROCESSOR(4/7) RSVD,CFG

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: 0.5

Date: Friday, November 05, 2010 | Sheet 7 of 61

POWER

SV type CPU

QC 94A
DC 53A

8.5A

INTEL Recommend
4*470uF,16*22uF and 10*10uF
from PDDG 1.0

INTEL Recommend
2*330uF,12*22uF
from PDDG 1.0

Follow Power Suggestion ,
place 3-pin Cap for CPU_CORE

P4W00
use 470uF*2
330uF*3

Place the PU
resistors close to VR

Place the PU
resistors close to CPU

R02 modify
ME interefer,not pop!!

Should change to connect form
power cirucit & layout differential
with VCCIO_SENSE.

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

Security Classification	Compal Secret Data		
Issued Date	2010/11/1	Deciphered Date	2011/11/1

Compal Electronics, Inc.

Title: PROCESSOR(5/7) PWR,BYPASS

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: 0.5

Date: Friday, November 05, 2010 | Sheet 8 of 61

POWER

INTEL Recommend
2*470uF,12*22uF
from PDDG 1.0

QC 33A
DC 26A

+VGFX_CORE

R151 0_0402_5% DISO@

JCPU1G

UMA@ C611 22U_0805_6.3V6M
UMA@ C625 22U_0805_6.3V6M
UMA@ C212 22U_0805_6.3V6M
UMA@ C272 22U_0805_6.3V6M
UMA@ C211 22U_0805_6.3V6M
UMA@ C231 22U_0805_6.3V6M
UMA@ C210 22U_0805_6.3V6M
UMA@ C209 22U_0805_6.3V6M
UMA@ C274 22U_0805_6.3V6M
UMA@ C271 22U_0805_6.3V6M
UMA@ C242 22U_0805_6.3V6M
UMA@ C275 22U_0805_6.3V6M
@ C646 330U_D2_2V_Y
UMA@ C645 330U_D2_2V_Y
@ C208 22U_0805_6.3V6M
UMA@ C273 22U_0805_6.3V6M
@ C600 22U_0805_6.3V6M
UMA@ C589 22U_0805_6.3V6M

AT24 AT23 AT21 AT20 AT18 AT17 AR24 AR23 AR21 AR20 AR18 AR17 AP24 AP23 AP21 AP20 AP18 AP17 AN24 AN23 AN21 AN20 AN18 AN17 AM24 AM23 AM21 AM20 AM18 AM17 AL24 AL23 AL21 AL20 AL18 AL17 AK24 AK23 AK21 AK20 AK18 AK17 AJ24 AJ23 AJ21 AJ20 AJ18 AJ17 AH24 AH23 AH21 AH20 AH18 AH17

VAXG1 VAXG2 VAXG3 VAXG4 VAXG5 VAXG6 VAXG7 VAXG8 VAXG9 VAXG10 VAXG11 VAXG12 VAXG13 VAXG14 VAXG15 VAXG16 VAXG17 VAXG18 VAXG19 VAXG20 VAXG21 VAXG22 VAXG23 VAXG24 VAXG25 VAXG26 VAXG27 VAXG28 VAXG29 VAXG30 VAXG31 VAXG32 VAXG33 VAXG34 VAXG35 VAXG36 VAXG37 VAXG38 VAXG39 VAXG40 VAXG41 VAXG42 VAXG43 VAXG44 VAXG45 VAXG46 VAXG47 VAXG48 VAXG49 VAXG50 VAXG51 VAXG52 VAXG53 VAXG54

Vaxg

- Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed in a common motherboard design,
- VAXG can be left floating in a common motherboard design (Gfx VR keeps VAXG from floating) if the VR is stuffed

SENSE LINES

VAXG_SENSE AK35 → VCC_AXG_SENSE 55
VSSAXG_SENSE AK34 → VSS_AXG_SENSE 55

VREF

+V_SM_VREF should have 20 mil trace width

+1.5V_CPU_VDDQ
R582 100_0402_1%
SM_VREF AL1 +V_SM_VREF
C688 0.1U_0402_16V4Z
R575 100_0402_1%

GRAPHICS DDR3 -1.5V RAILS

10A

+1.5V_CPU_VDDQ

VDDQ1 AF7
VDDQ2 AF4
VDDQ3 AF1
VDDQ4 AC7
VDDQ5 AC4
VDDQ6 AC1
VDDQ7 Y7
VDDQ8 Y4
VDDQ9 Y1
VDDQ10 U7
VDDQ11 U4
VDDQ12 U1
VDDQ13 P7
VDDQ14 P4
VDDQ15 P1

10U_0805_10V4Z C363
10U_0805_10V4Z C364
10U_0805_10V4Z C362
10U_0805_10V4Z C341
10U_0805_10V4Z C365
10U_0805_10V4Z C361
330U_D2_2V_Y C355

+1.5V
J4 PAD-OPEN 4x4m @
+1.5VS
J5 PAD-OPEN 4x4m @

Short for +1.5VS to +1.5V_1

INTEL Recommend
1*330uF,6*10uF
from PDDG 1.0

INTEL Recommend
1*330uF,3*10uF
from PDDG 1.0

SA RAIL

6A

+VCCSA

VCCSA1 M27
VCCSA2 M26
VCCSA3 L26
VCCSA4 J26
VCCSA5 J25
VCCSA6 J24
VCCSA7 H26
VCCSA8 H25

10U_0805_10V4Z C214
10U_0805_10V4Z C205
10U_0805_10V4Z C219
@
10U_0603_6.3V6M C213
220U_B2_2.5VM_R35 C221

R137 0_0402_5% VCCSA_SENSE
R141 0_0402_5% VSSSA_SENSE 52

If possible,use os-con cap
if not,use the D2 size

MISC

VCCSA_SENSE H23 → VCCSA_SENSE 52

FC_C22 C22
VCCSA_VID1 C24

VCCSA_VID0
VCCSA_VID1 → VCCSA_VID1 52

FC_C22 change to VCCSA_VID0

R143 10K_0402_5%
R138 @0_0402_5%

VCCSA				
VID0	VID1	Vout	2011CPU	2012CPU
0	0	0.9V	V	V
0	1	0.8V	V	V
1	0	0.725V	X	V
1	1	0.675V	X	V

1.8V RAIL

1.2A

+1.8VS R528 0_0805_5%
+1.8VS_VCCPLL B6 A6 A2 → VCCPLL1 VCCPLL2 VCCPLL3

C664 220U_B2_2.5VM_R35
C655 10U_0805_10V4Z
C654 1U_0402_6.3V6K
C653 1U_0402_6.3V6K

Sandy Bridge_rPGA_Rev0p61

CONN@

INTEL Recommend
1*330uF,1*10uF and 2*1uF(0402)
from PDDG 1.0

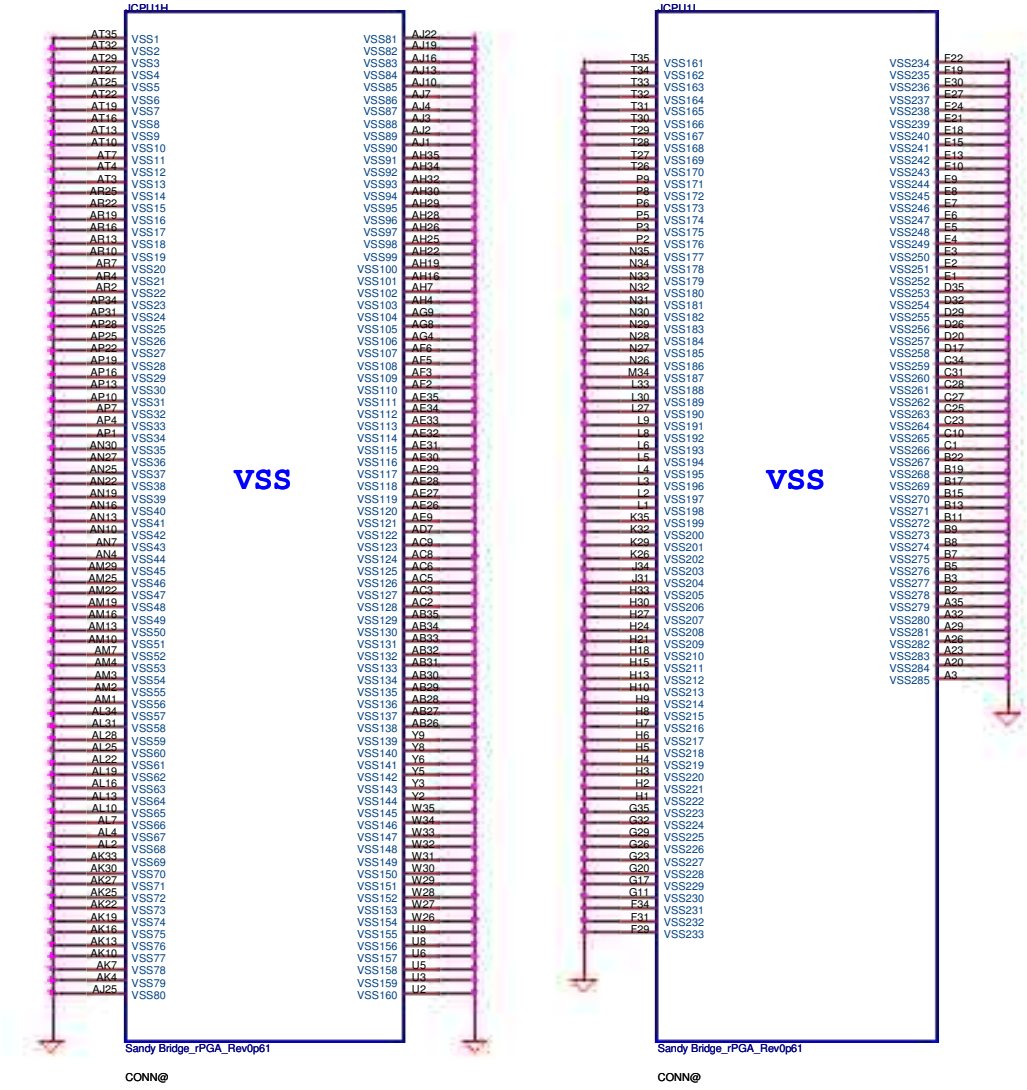
Security Classification	Compal Secret Data		
Issued Date	2010/11/1	Deciphered Date	2011/11/1

Compal Electronics, Inc.

Title: PROCESSOR(6/7) PWR

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: 0.5

Date: Friday, November 05, 2010 | Sheet 9 of 61



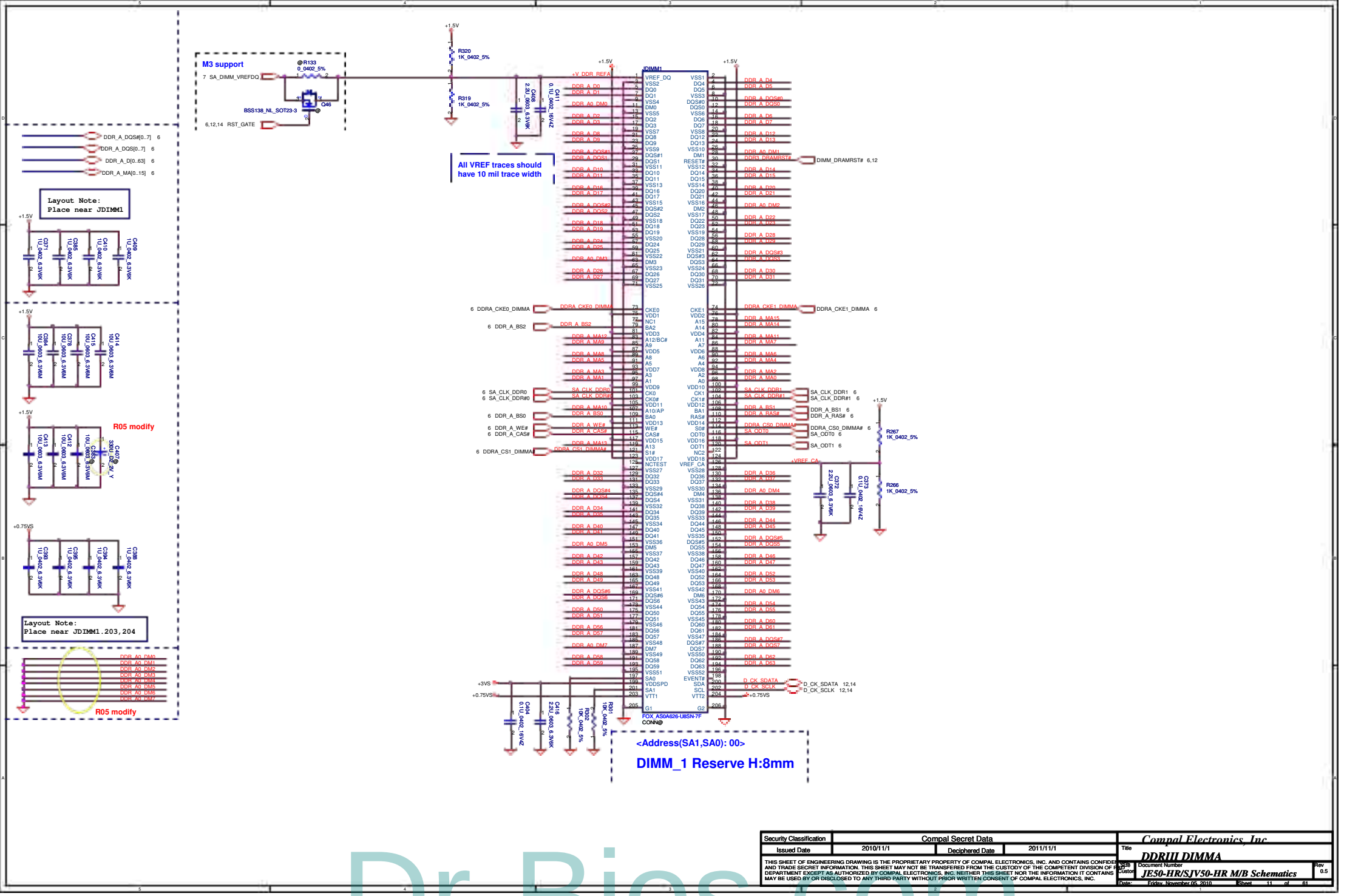
Security Classification	Compal Secret Data		
Issued Date	2010/11/1	Deciphered Date	2011/11/1

Compal Electronics, Inc.

Title: PROCESSOR(7/7) VSS

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: 0.5

Date: Friday, November 05, 2010 | Sheet 10 of 61



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Issued Date	2010/11/1	Deciphered Date	2011/11/1

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Compal Electronics, Inc

Title: DDRIII DIMMA

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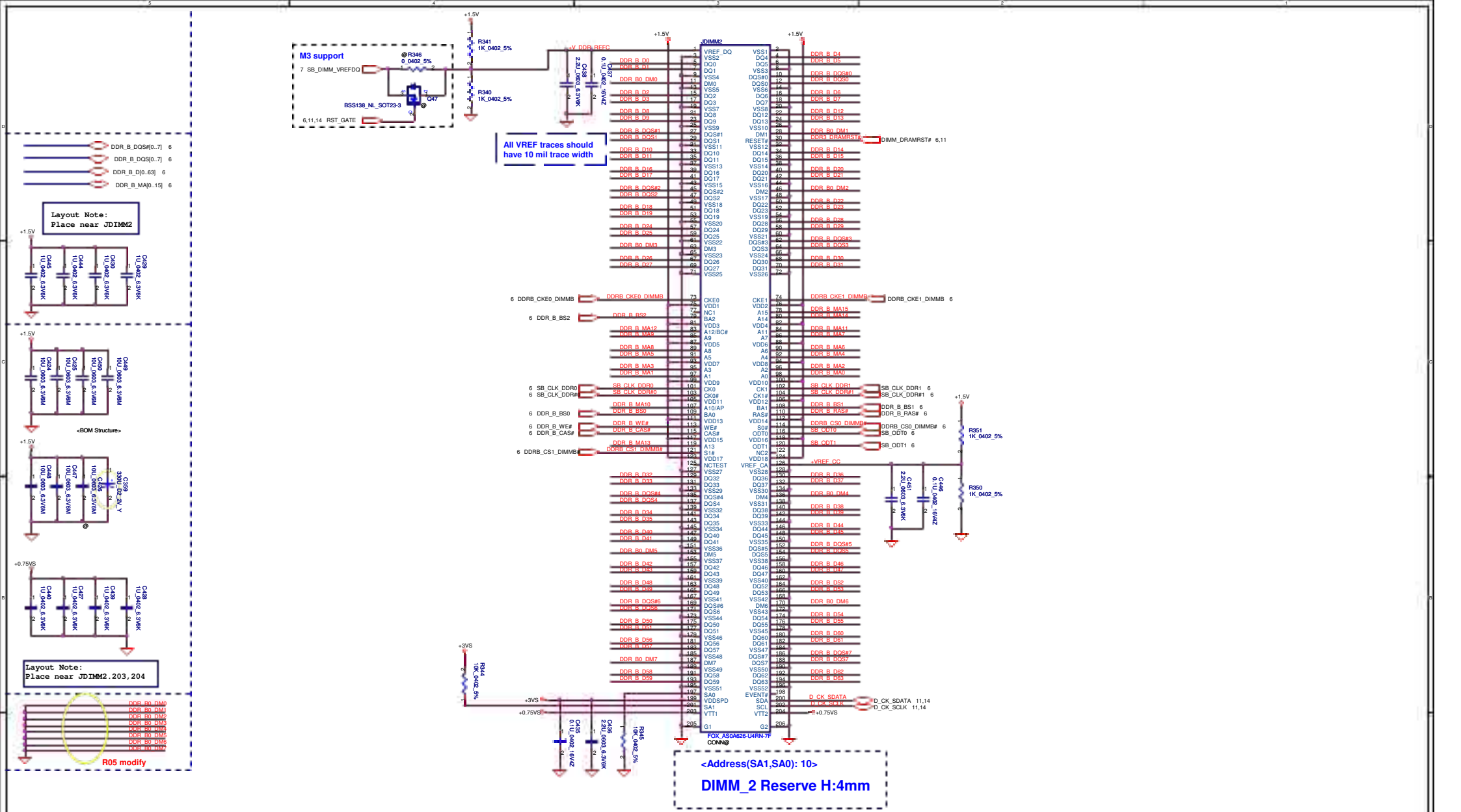
Date: Friday, November 05, 2010 | Sheet 11 of 61



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Compal Electronics, Inc

Title: DDRIII DIMMB

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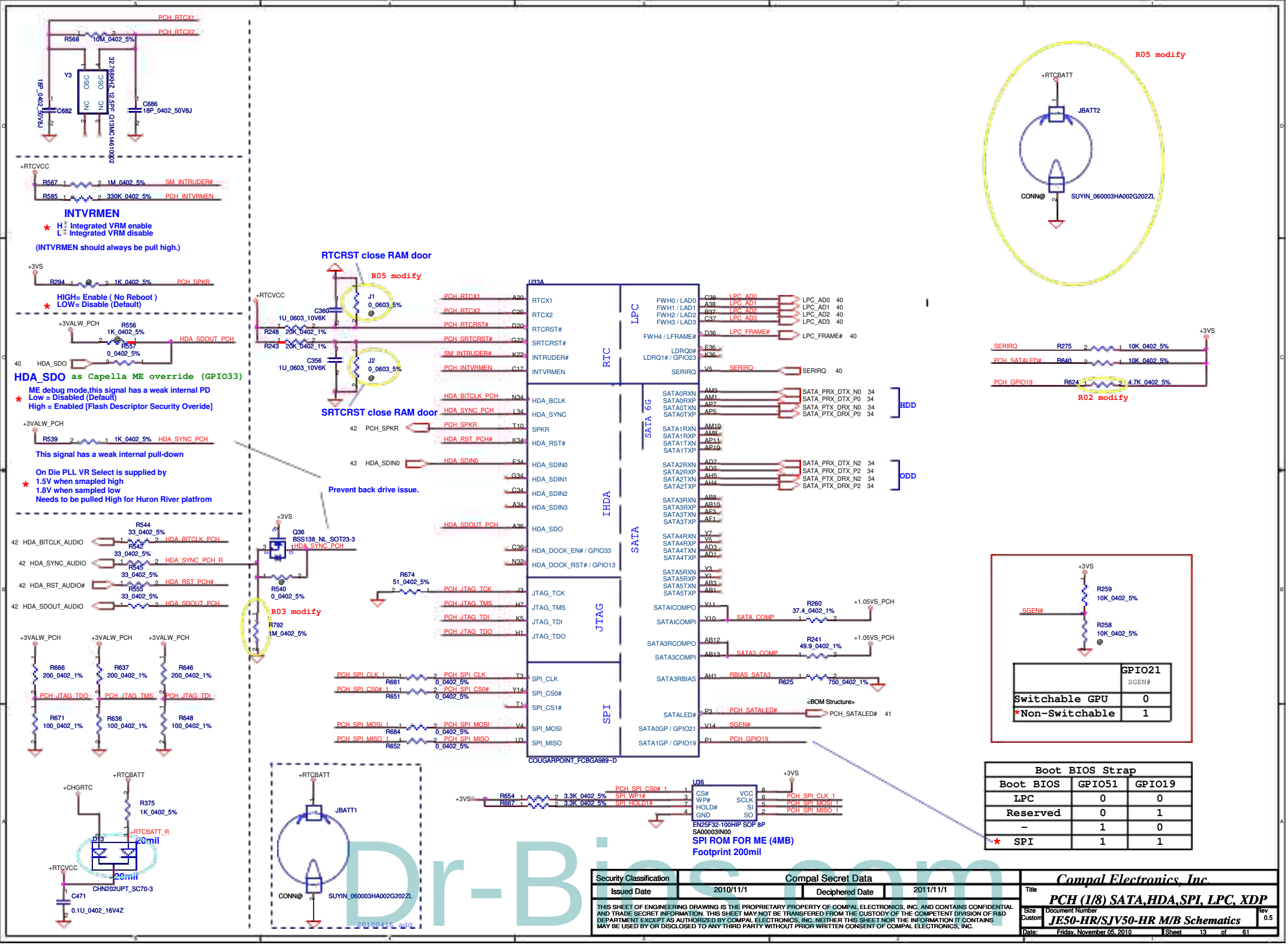
Date: Friday, November 05, 2010 | Sheet 12 of 61



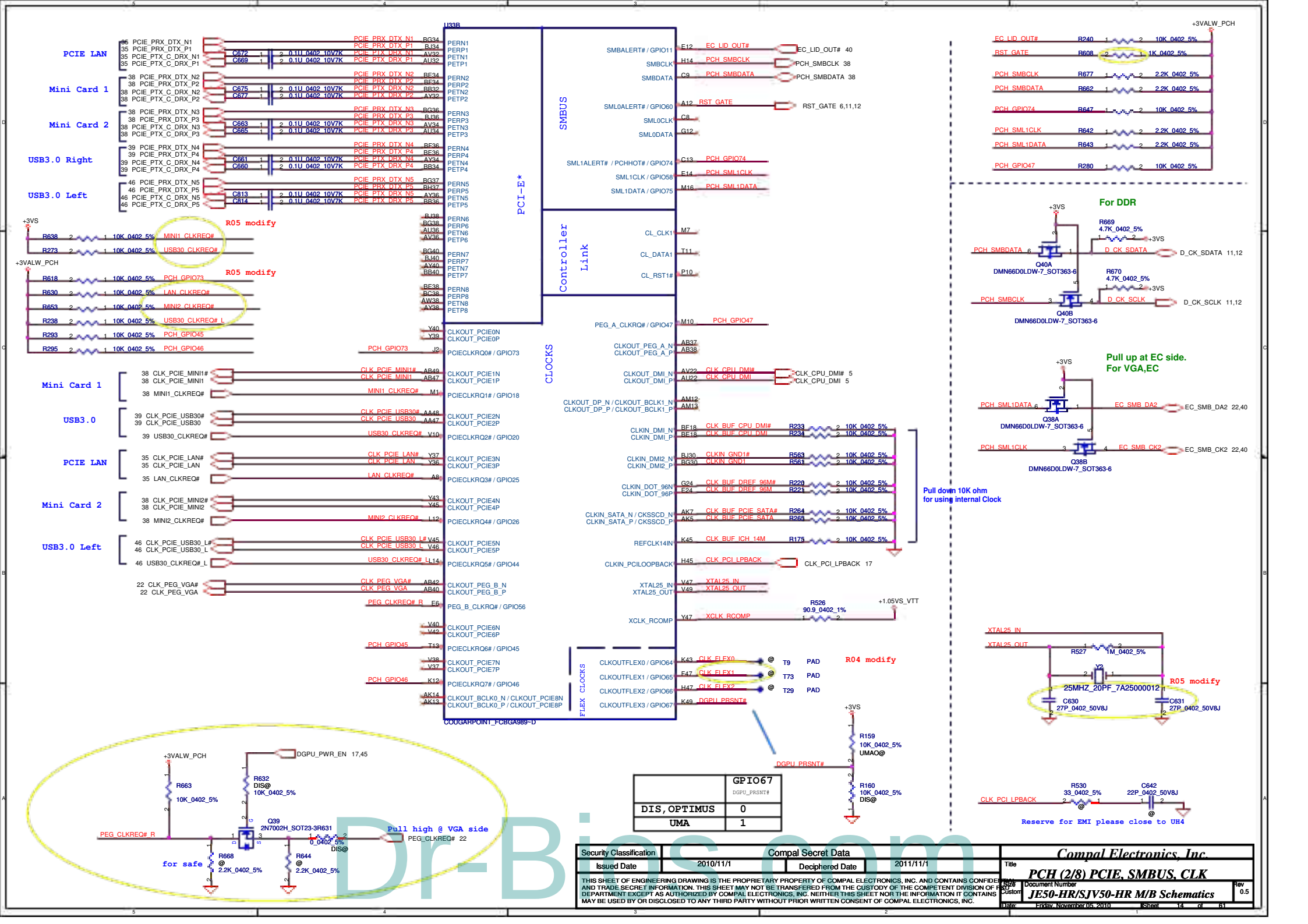
Security Classification	Compal Secret Data
Issued Date	2010/11/1
Deciphered Date	2011/11/1

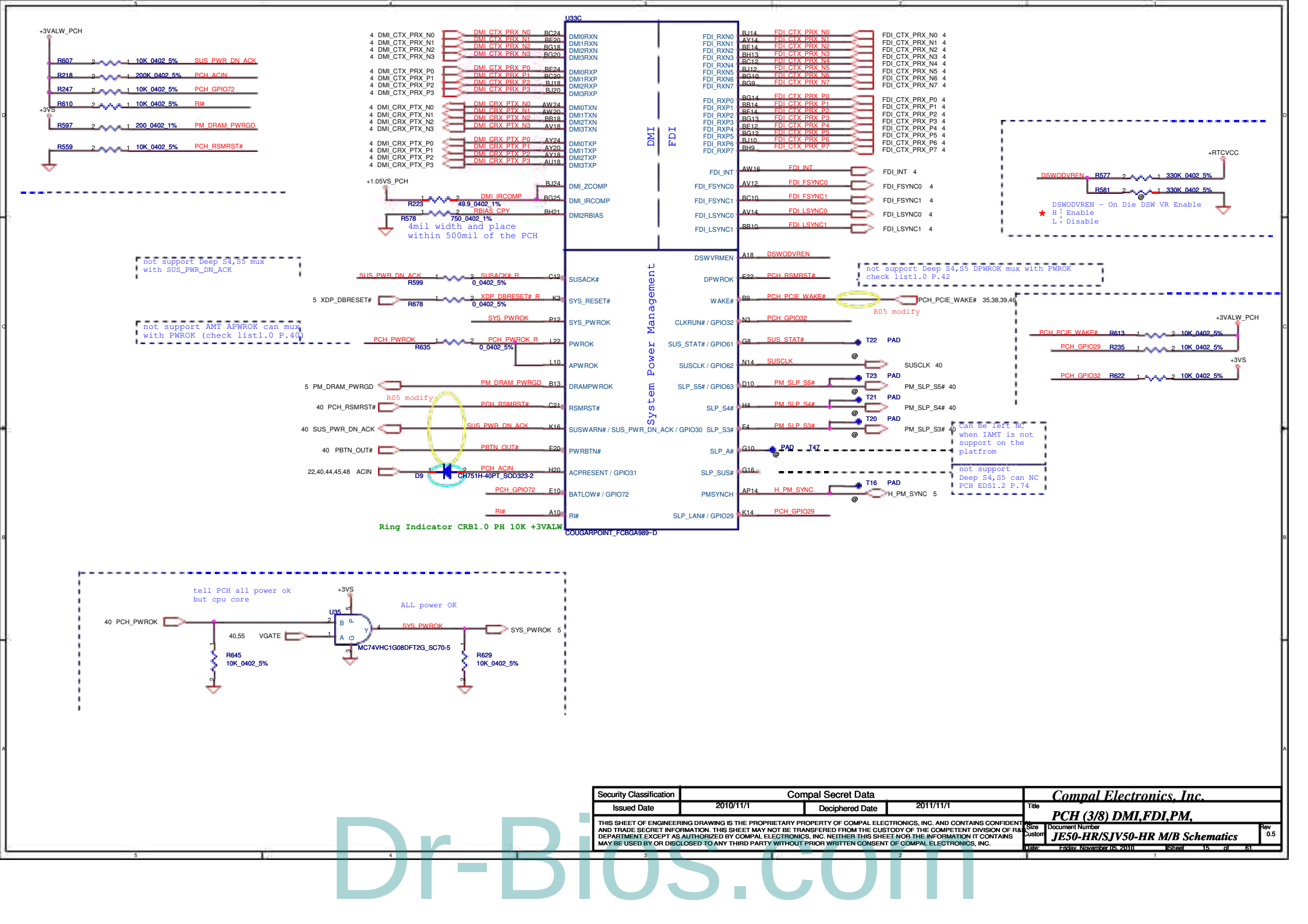
Compal Electronics, Inc.

Title: PCH (1/8) SATA,HDA,SPI, LPC, XDP

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: 0.5

Date: Friday, November 05, 2010 | Sheet 13 of 61


PCIE LAN
Mini Card 1
Mini Card 2
USB3.0 Right
USB3.0 Left
R05 modify
R05 modify
Mini Card 1
USB3.0
PCIE LAN
Mini Card 2
USB3.0 Left
U33B
PCI-E*
SMBUS
Controller Link
CLOCKS
FLEX CLOCKS
COUGARPOINT_FCBGA989-D
Pull down 10K ohm for using internal Clock
R04 modify
R05 modify
For DDR
Pull up at EC side. For VGA,EC
Pull high @ VGA side
for safe
Reserve for EMI please close to UH4
DIS,OPTIMUS 0
UMA 1
Compal Electronics, Inc.
PCH (2/8) PCIE, SMBUS, CLK
JE50-HR/SJV50-HR M/B Schematics
Compal Secret Data
2010/11/1
2011/11/1
Friday, November 05, 2010



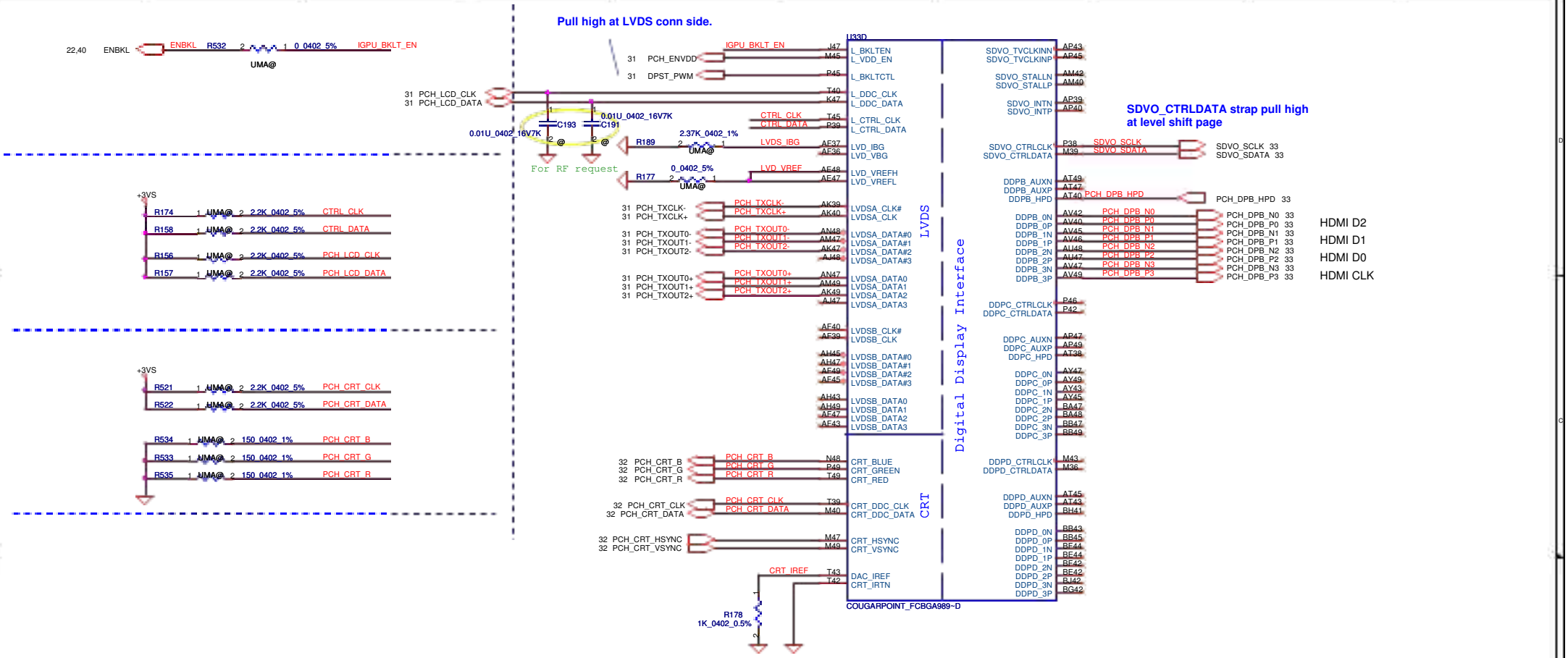
Security Classification	Compal Secret Data		
Issued Date	2010/11/1	Deciphered Date	2011/11/1

Compal Electronics, Inc.

Title: PCH (3/8) DMI,FDI,PM,

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: 0.5

Date: Friday, November 05, 2010 | Sheet 15 of 61



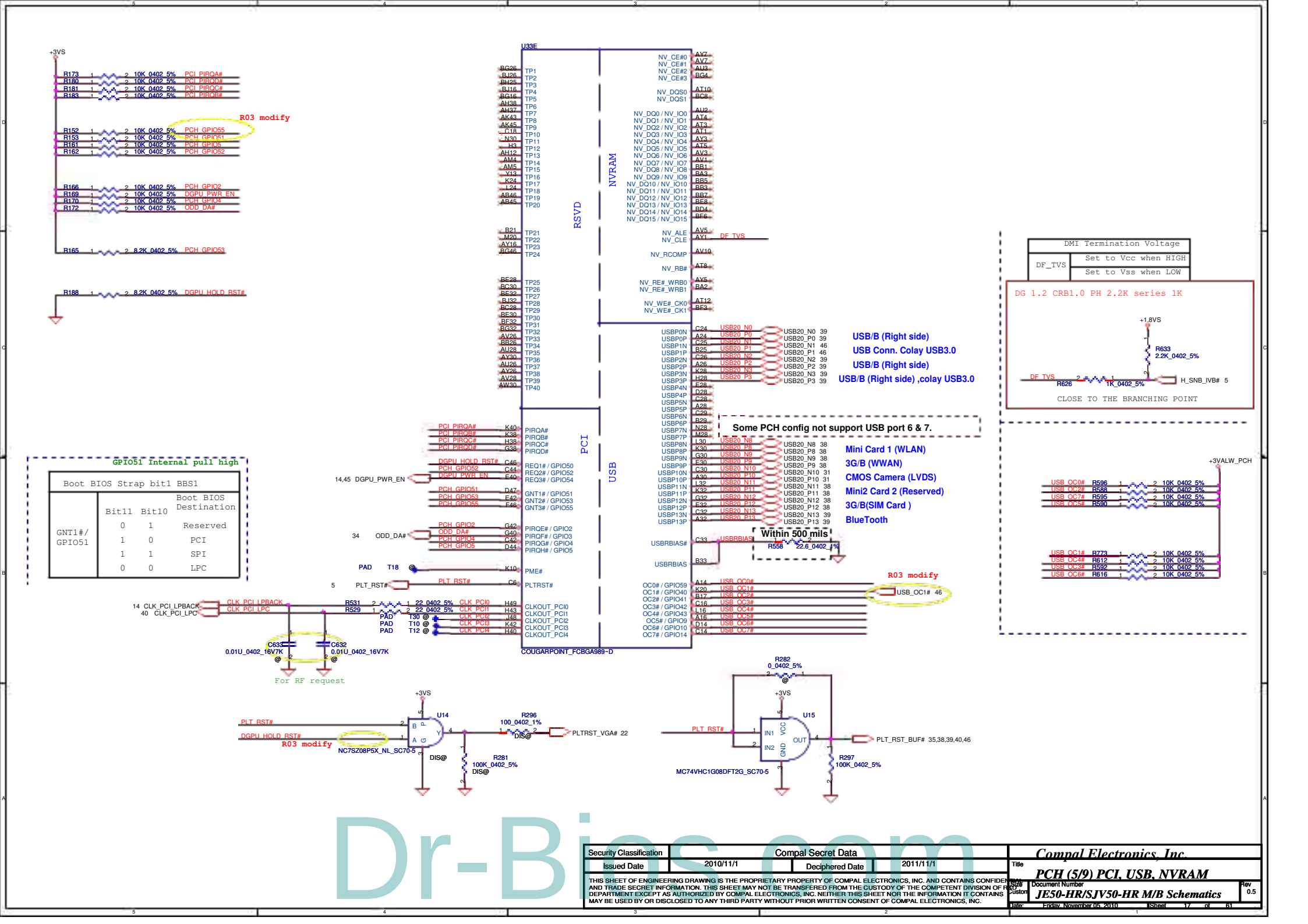
Security Classification	Compal Secret Data		
Issued Date	2010/11/1	Deciphered Date	2011/11/1

Compal Electronics, Inc.

Title: PCH (4/9) LVDS,CRT,DP,HDMI

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: 0.5

Date: Friday, November 05, 2010 | Sheet 16 of 61



Security Classification	Compal Secret Data		
Issued Date	2010/11/1	Deciphered Date	2011/11/1

Compal Electronics, Inc.

Title: PCH (5/9) PCI, USB, NVRAM

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: 0.5

Date: Friday, November 05, 2010 | Sheet 17 of 61

HDA_SYNC PH(PLL =+1.5VS)

GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up

* H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable

R272 1 @ 2 1K_0402_5% PCH_GPIO28
+3VALW_PCH R768 1 2 4.7K_0402_5%

Deep S4,S5 wake event signal
RTC alarm,Power BTN,GPIO27
PCH_GPIO27 (Have internal Pull-High)
Deep S4,S5 wake event signal
No use PD to GND Check list1.0 P.70

R661 1 2 10K_0402_5% PCH_GPIO27

+3VS
R623 1 NOPT@ 2 10K_0402_5% OPTIMUS_EN#
R639 1 OPT@ 2 10K_0402_5%

	GPIO38 OPTIMUS_EN#
* OPTIMUS	0
Non-OPTIMUS	1

+3VS
R04 modify
R277 1 2 200K_0402_5% WWAN_OFF#
R276 1 2 10K_0402_5% PCH_GPIO0
R546 1 2 10K_0402_5% WL_EN#
R191 1 2 10K_0402_5% DGPU_HPD_INT#
R641 1 2 10K_0402_5% PCH_GPIO16
R194 1 2 10K_0402_5% DGPU_PWROK
R290 1 2 10K_0402_5% PCH_GPIO22
R649 1 2 10K_0402_5% PCH_GPIO39
R04 modify
R291 1 2 200K_0402_5% ODD_DETECT#
R619 1 2 10K_0402_5% BT_ON#
R292 1 2 10K_0402_5% PCH_GPIO48
R274 1 2 10K_0402_5% WL_OFF#

+3VALW_PCH
R262 1 2 10K_0402_5% PCH_GPIO24
R620 1 2 10K_0402_5% PCH_GPIO12
R672 1 2 1K_0402_5% SMIB
R263 1 2 10K_0402_5% PCH_GPIO57

GPIO24 Unmultiplexed
NOTE: GPIO24 configuration register bits are not cleared by CF9h reset event.

CRB1.0 PH10K to +3VALW

U33F

R05 modify
39 WL_EN# — PCH_GPIO0 — T7 — BMBUSY# / GPIO0
WL_EN# — A42 — TACH1 / GPIO1
33 DGPU_HPD_INT# — DGPU_HPD_INT# — H36 — TACH2 / GPIO6
40 EC_SCI# — EC_SCI# — E38 — TACH3 / GPIO7
40 EC_SMI# — EC_SMI# — C10 — GPIO8
PCH_GPIO12 — C4 — LAN_PHY_PWR_CTRL / GPIO12
39,46 SMIB — SMIB — G2 — GPIO15
PCH_GPIO16 — U2 — SATA4GP / GPIO16
54 VGA_PWROK — R193 1 DIS@ 2 0_0402_5% — DGPU_PWROK — D40 — TACH0 / GPIO17
R05 modify
PCH_GPIO22 — T5 — SCLOCK / GPIO22
PCH_GPIO24 — E8 — GPIO24 / MEM_LED
PCH_GPIO27 — E16 — GPIO27
PCH_GPIO28 — P8 — GPIO28
38,39 BT_ON# — BT_ON# — K1 — STP_PCI# / GPIO34
K4 — GPIO35
34 ODD_DETECT# — ODD_DETECT# — V8 — SATA2GP / GPIO36
R03 modify 38 WWAN_OFF# — WWAN_OFF# — M5 — SATA3GP / GPIO37
OPTIMUS_EN# — N2 — SLOAD / GPIO38
PCH_GPIO39 — M3 — SDATAOUT0 / GPIO39
PCH_GPIO48 — V13 — SDATAOUT1 / GPIO48
R03 modify 38 WL_OFF# — WL_OFF# — V3 — SATA5GP / GPIO49
PCH_GPIO57 — D6 — GPIO57

GPIO

PAD T61 — A4 — VSS_NCTF_1
PAD T46 — A44 — VSS_NCTF_2
PAD T44 — A45 — VSS_NCTF_3
PAD T41 — A46 — VSS_NCTF_4
PAD T52 — A5 — VSS_NCTF_5
PAD T51 — A6 — VSS_NCTF_6
PAD T64 — B3 — VSS_NCTF_7
PAD T37 — B47 — VSS_NCTF_8
PAD T55 — BD1 — VSS_NCTF_9
PAD T34 — BD49 — VSS_NCTF_10
PAD T56 — BE1 — VSS_NCTF_11
PAD T35 — BE49 — VSS_NCTF_12
PAD T57 — BE1 — VSS_NCTF_13
PAD T36 — BE49 — VSS_NCTF_14

NCTF

C40 — ODD_EN# — ODD_EN# 34
B41 — PCH_GPIO69 — TACH4 / GPIO68
C41 — PCH_GPIO70 — TACH5 / GPIO69
A40 — PCH_GPIO71 — TACH6 / GPIO70
TACH7 / GPIO71

+3VS
R278 10K_0402_5%
P4 — A20GATE — GATEA20 40
AU16 — PCH_PECI_R 1 0_0402_5%@ 2 R239 — PECI — H_PECI 5,40
P5 — EC_KBRST# — RCIN# — EC_KBRST# 40
AY11 — PROCPWRGD — H_CPUPWRGD 5
AY10 — PCH_THRMTRIP# R 1 R627 2 390_0402_5% H_THRMTRIP# — THRMTRIP# — H_THRMTRIP# 5
T14 — INIT3_3V

PECI CPU-EC
CTRL+ALT+DEL
non CPU power ok
130 degree shut sown

INIT3_3V Checklist1.0 P.59
This signal has weak internal PU, can't pull low,leave NC

AH8 — NC_1
AK11 — NC_2
AH10 — NC_3
AK10 — NC_4
P37 — NC_5

TS_VSS1~4 PD to GND

CPU/MISC

BG2 @ T58 PAD — VSS_NCTF_15
BG48 @ T39 PAD — VSS_NCTF_16
BH3 @ T59 PAD — VSS_NCTF_17
BH47 @ T40 PAD — VSS_NCTF_18
BJ4 @ T60 PAD — VSS_NCTF_19
BJ44 @ T45 PAD — VSS_NCTF_20
BJ45 @ T43 PAD — VSS_NCTF_21
BJ46 @ T42 PAD — VSS_NCTF_22
BJ5 @ T50 PAD — VSS_NCTF_23
BJ6 @ T49 PAD — VSS_NCTF_24
C2 @ T65 PAD — VSS_NCTF_25
C48 @ T38 PAD — VSS_NCTF_26
D1 @ T63 PAD — VSS_NCTF_27
D49 @ T32 PAD — VSS_NCTF_28
F1 @ T54 PAD — VSS_NCTF_29
F49 @ T33 PAD — VSS_NCTF_30
F1 @ T53 PAD — VSS_NCTF_31
F49 @ T31 PAD — VSS_NCTF_32

COUGARPOINT_FCBGA989~D

+3VS
ODD_EN# R771 1 2 10K_0402_5%
EC_KBRST# R279 1 2 10K_0402_5%

+3VS +3VS
R554 10K_0402_5% @ PCH_GPIO69
R548 10K_0402_5% @ PCH_GPIO70
R553 10K_0402_5%
R549 10K_0402_5%

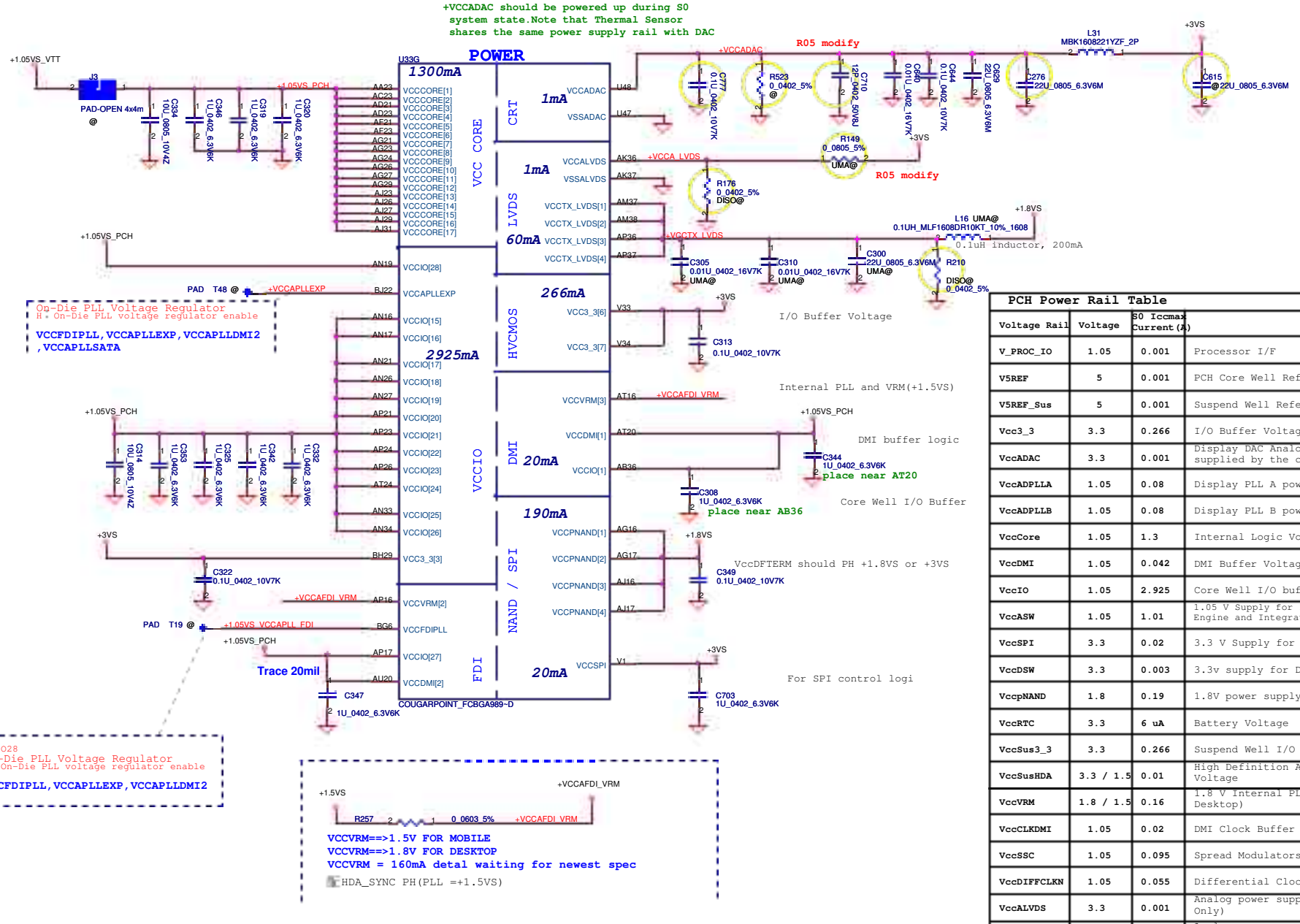
R02 modify
+3VS
R550 10K_0402_5% X76@ PCH_GPIO71
R551 10K_0402_5% X76@

Project ID	GPIO69	GPIO70
* P5WE0	0	0
P7YE0	0	0
x	1	0
x	1	1

	GPIO71 PCH_GPIO71
*VRAM 800 MHz	0
VRAM 900 MHz	1

Security Classification	Compal Secret Data		
Issued Date	2010/11/1	Deciphered Date	2011/11/1

Compal Electronics, Inc.
Title: PCH (6/9) GPIO, CPU, MISC
Size: Custom
Document Number: JE50-HR/SJV50-HR M/B Schematics
Rev: 0.5
Date: Friday, November 05, 2010
Sheet 18 of 61



PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current(A)	
V_PROC_IO	1.05	0.001	Processor I/F
V5REF	5	0.001	PCH Core Well Reference Voltage
V5REF_Sus	5	0.001	Suspend Well Reference Voltag
Vcc3_3	3.3	0.266	I/O Buffer Voltage
VccADAC	3.3	0.001	Display DAC Analog Power. This power is supplied by the core well.
VccADPLLA	1.05	0.08	Display PLL A power
VccADPLLB	1.05	0.08	Display PLL B power
VccCore	1.05	1.3	Internal Logic Voltage
VccDMI	1.05	0.042	DMI Buffer Voltage
VccIO	1.05	2.925	Core Well I/O buffers
VccASW	1.05	1.01	1.05 V Supply for Intel R Management Engine and Integrated LAN
VccSPI	3.3	0.02	3.3 V Supply for SPI Controller Logic
VccDSW	3.3	0.003	3.3v supply for Deep S4/S5 well
VccpNAND	1.8	0.19	1.8V power supply for DF_TVS
VccRTC	3.3	6 uA	Battery Voltage
VccSus3_3	3.3	0.266	Suspend Well I/O Buffer Voltage
VccSusHDA	3.3 / 1.5	0.01	High Definition Audio Controller Suspend Voltage
VccVRM	1.8 / 1.5	0.16	1.8 V Internal PLL and VRMs (1.8 V for Desktop)
VccCLKDMI	1.05	0.02	DMI Clock Buffer Voltage
VccSSC	1.05	0.095	Spread Modulators Power Supply
VccDIFFCLKN	1.05	0.055	Differential Clock Buffers Power Supply
VccALVDS	3.3	0.001	Analog power supply for LVDS (Mobile Only)
VccTX_LVDS	1.8	0.06	Analog power supply for LVDS (Mobile Only)

Security Classification	Compal Secret Data		
Issued Date	2010/11/1	Deciphered Date	2011/11/1

Compal Electronics, Inc.

Title: PCH (7/9) PWR

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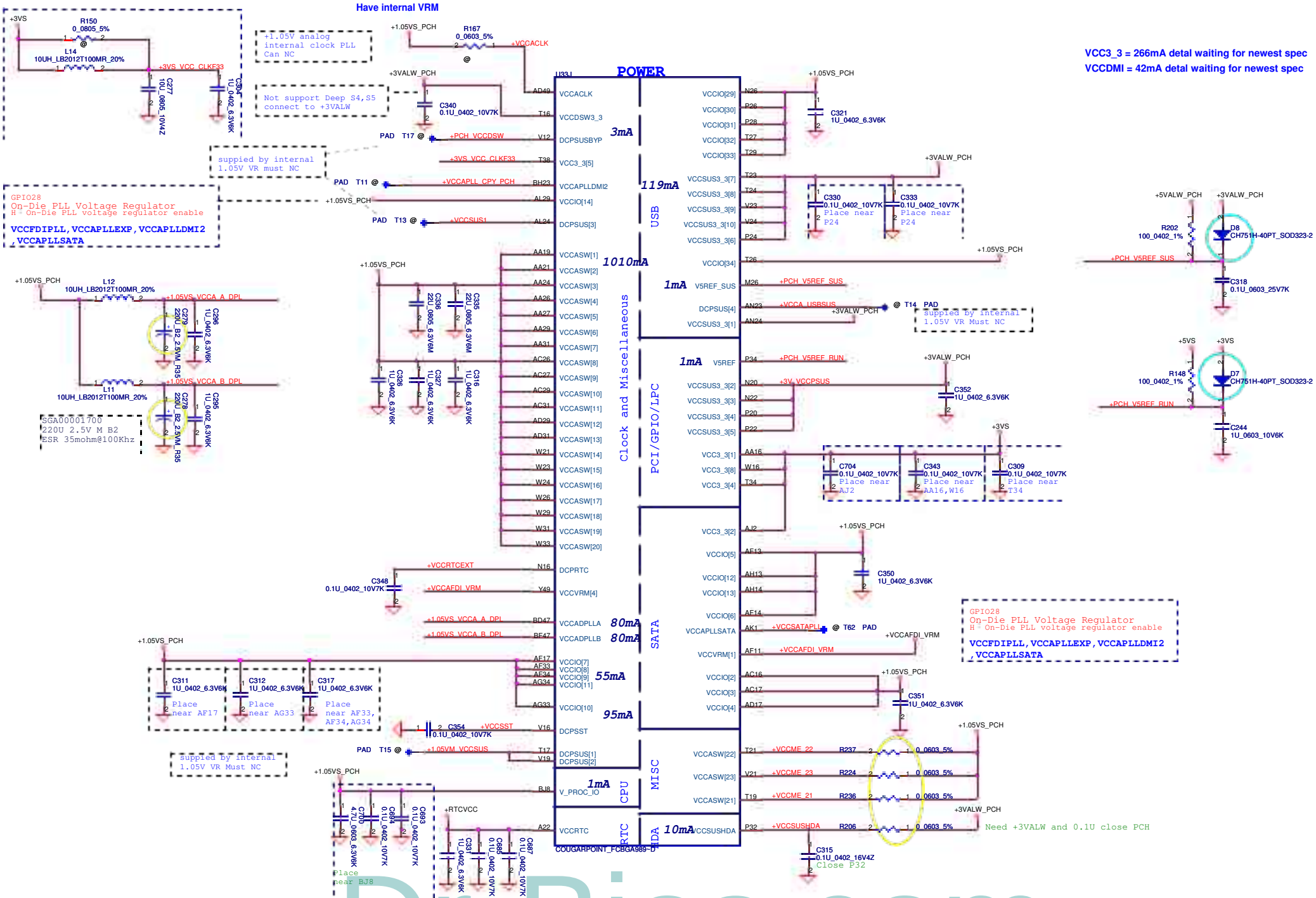

Security Classification	Compal Secret Data		
Issued Date	2010/11/1	Deciphered Date	2011/11/1

Compal Electronics, Inc.

Title: PCH (8/9) PWR

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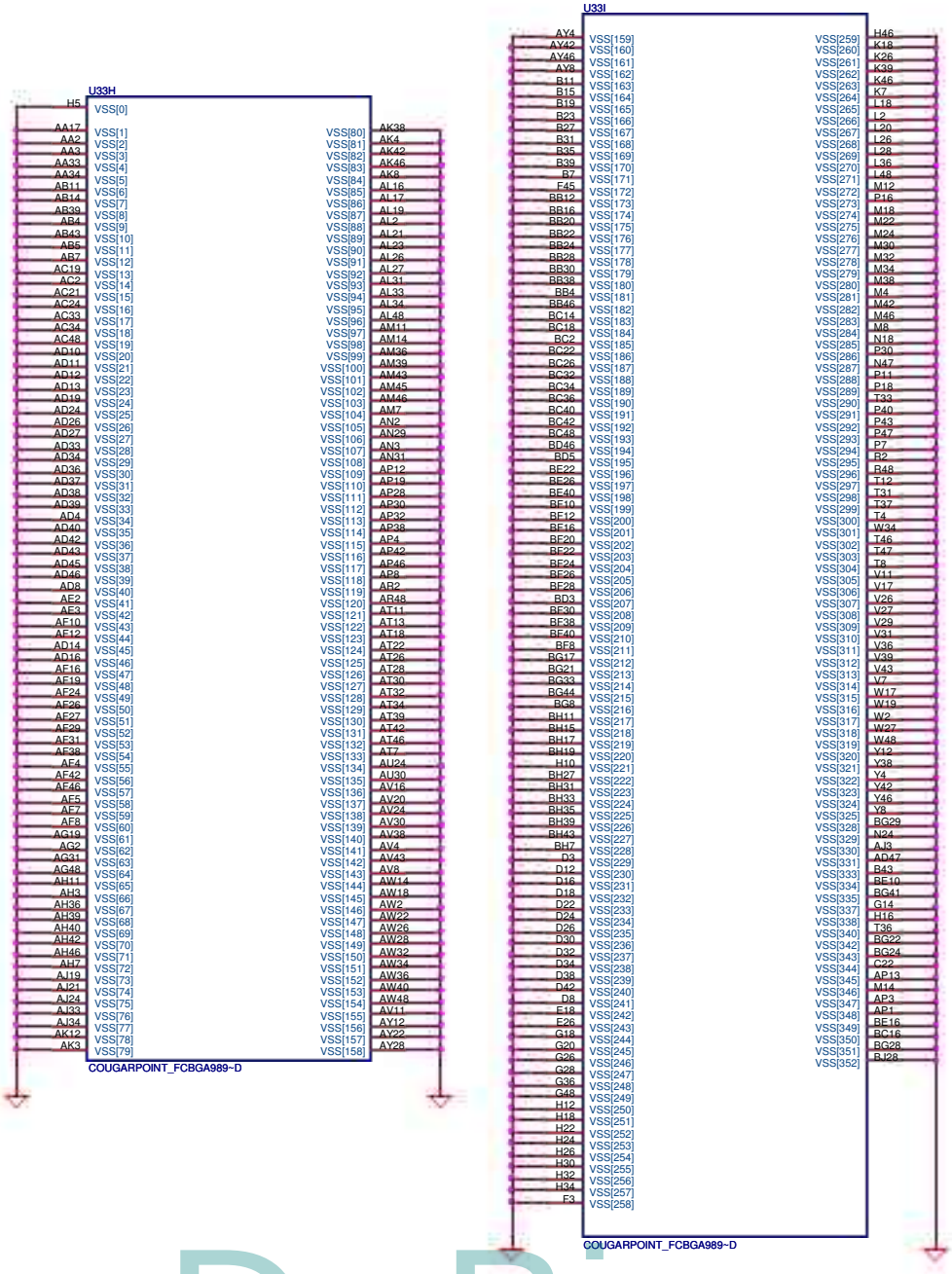

Security Classification	Compal Secret Data		
Issued Date	2010/11/1	Deciphered Date	2011/11/1

Compal Electronics, Inc.

Title: PCH (9/9) VSS

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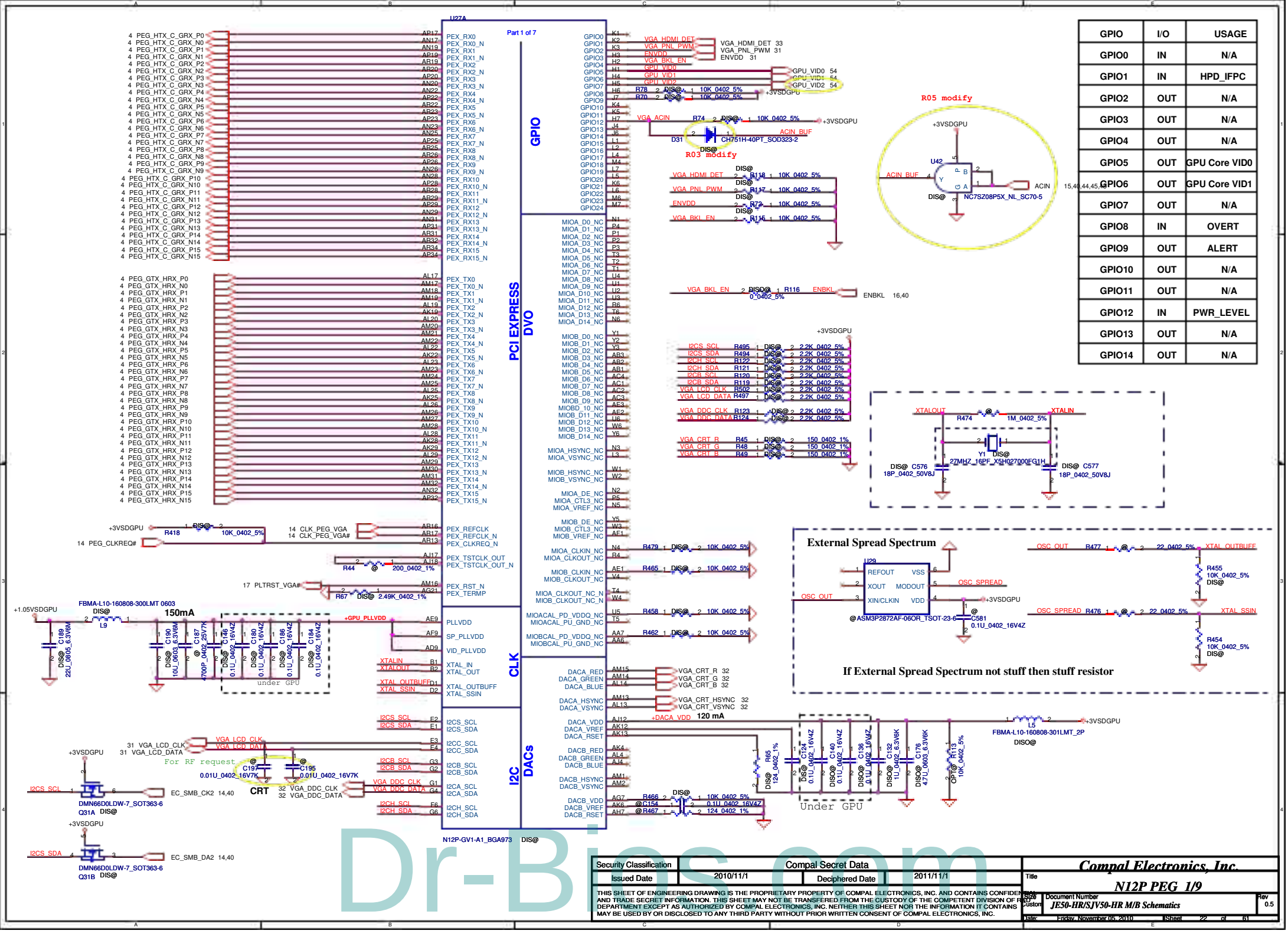

GPIO	I/O	USAGE
GPIO0	IN	N/A
GPIO1	IN	HPD_IFPC
GPIO2	OUT	N/A
GPIO3	OUT	N/A
GPIO4	OUT	N/A
GPIO5	OUT	GPU Core VID0
GPIO6	OUT	GPU Core VID1
GPIO7	OUT	N/A
GPIO8	IN	OVERT
GPIO9	OUT	ALERT
GPIO10	OUT	N/A
GPIO11	OUT	N/A
GPIO12	IN	PWR_LEVEL
GPIO13	OUT	N/A
GPIO14	OUT	N/A

Security Classification	Compal Secret Data		
Issued Date	2010/11/1	Deciphered Date	2011/11/1

Compal Electronics, Inc.

Title: N12P PEG 1/9

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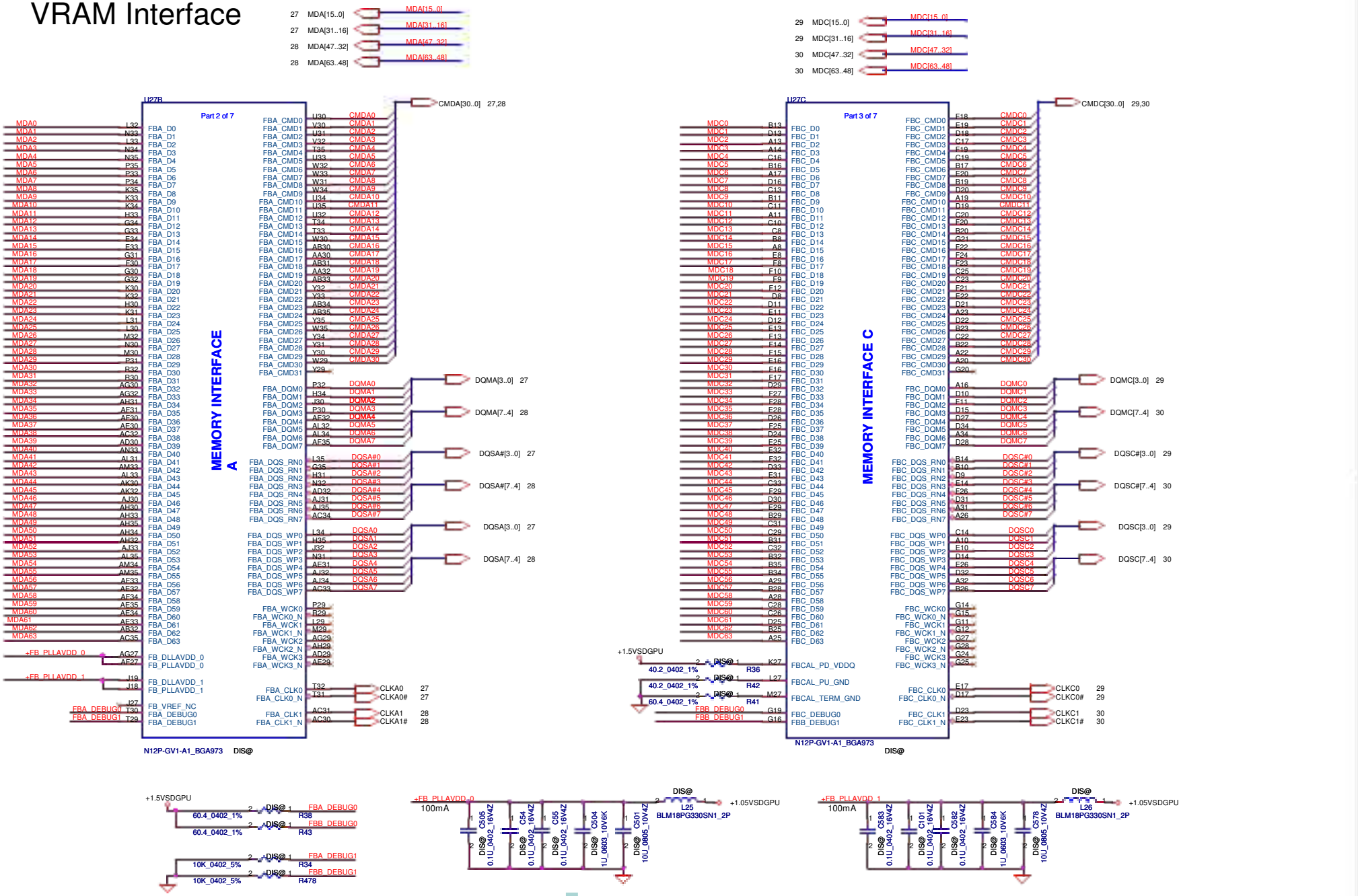
VRAM Interface



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Compal Electronics, Inc.			
Title: N12P VRAM 2/9			
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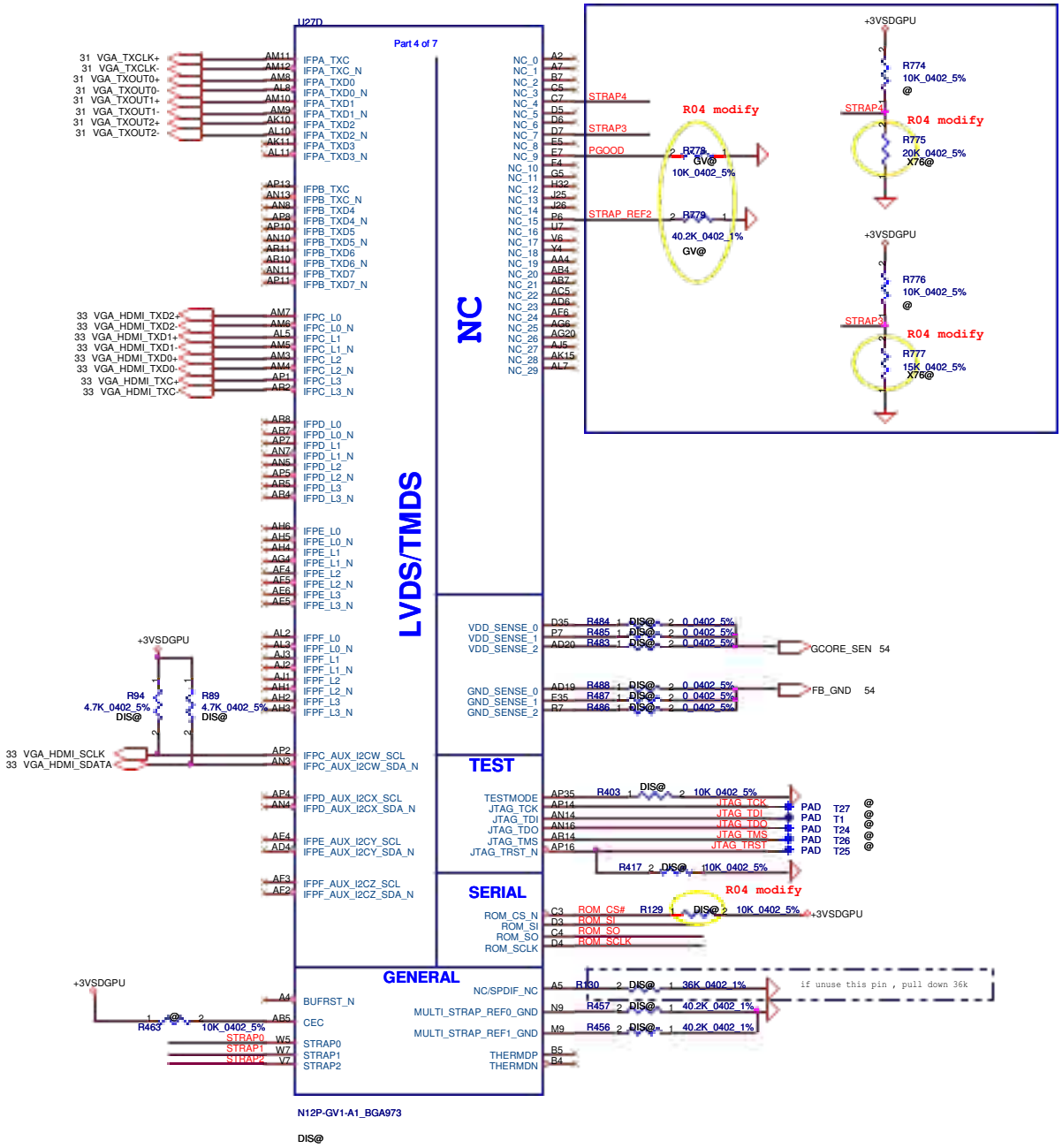
For GB2-128 & GB2b-128 colayout....

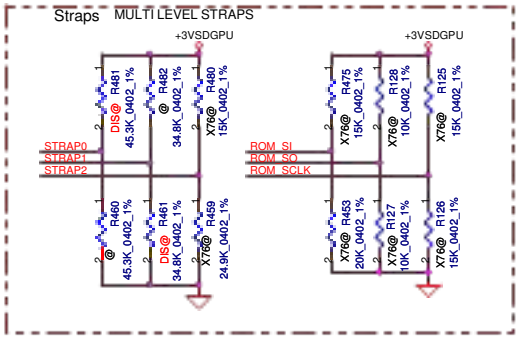


For N12P-GV ES strap table

Frenq.	N12P-GS	strap0	strap1	strap2	ROM_SI	ROM_SO	ROM_SCLK	strap3	strap4
800 MHz	64MX16 Hynix SA000032420	H 45K	L 35K	H 45K	L 15K	H 10K	H 15K	L 15K	L 20K
900 MHz	64MX16 Hynix SA000041S40	H 45K	L 35K	H 45K	L 15K	H 10K	H 15K	L 15K	L 20K
900 MHz	64MX16 Samsung SA00004GS10	H 45K	L 35K	H 45K	L 25K	H 10K	H 15K	L 15K	L 20K
800 MHz	128MX16 Samsung SA00003MQ60	H 45K	L 35K	H 45K	L 45K	H 10K	H 15K	L 15K	L 20K
800 MHz	128MX16 Hynix SA00003VS10	H 45K	L 35K	H 45K	L 35K	H 10K	H 15K	L 15K	L 20K

For N12P-GV A1 strap table

Frenq.	N12P-GS	strap0	strap1	strap2	ROM_SI	ROM_SO	ROM_SCLK	strap3	strap4
800 MHz	64MX16 Hynix SA000032420	H 45K	L 35K	L 5K	L 15K	H 10K	H 5K	L 15K	L 20K
900 MHz	64MX16 Hynix SA000041S40	H 45K	L 35K	L 5K	L 15K	H 10K	H 5K	L 15K	L 20K
900 MHz	64MX16 Samsung SA00004GS10	H 45K	L 35K	L 5K	L 25K	H 10K	H 5K	L 15K	L 20K
800 MHz	128MX16 Samsung SA00003MQ60	H 45K	L 35K	L 5K	L 45K	H 10K	H 5K	L 15K	L 20K
800 MHz	128MX16 Hynix SA00003VS10	H 45K	L 35K	L 5K	L 35K	H 10K	H 5K	L 15K	L 20K



For N12P-GS strap table (strap 3 and strap4 left NC)

Frenq.	N12P-GS	strap0	strap1	strap2	ROM_SI	ROM_SO	ROM_SCLK
800 MHz	64MX16 Hynix SA000032420	H 45K	L 35K	L 25K	L 5K	L 10K	H 15K
900 MHz	64MX16 Hynix SA000041S40	H 45K	L 35K	L 25K	L 15K	L 10K	H 15K
900 MHz	64MX16 Samsung SA00004GS10	H 45K	L 35K	L 25K	L 20K	L 10K	H 15K
800 MHz	128MX16 Samsung SA00003MQ60	H 45K	L 35K	L 25K	L 45K	L 10K	H 15K
800 MHz	128MX16 Hynix SA00003VS10	H 45K	L 35K	L 25K	L 35K	L 10K	H 15K

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Issued Date	2010/11/1	Deciphered Date	2011/11/1

Compal Electronics, Inc.

Title: N12P LVDS 3/9

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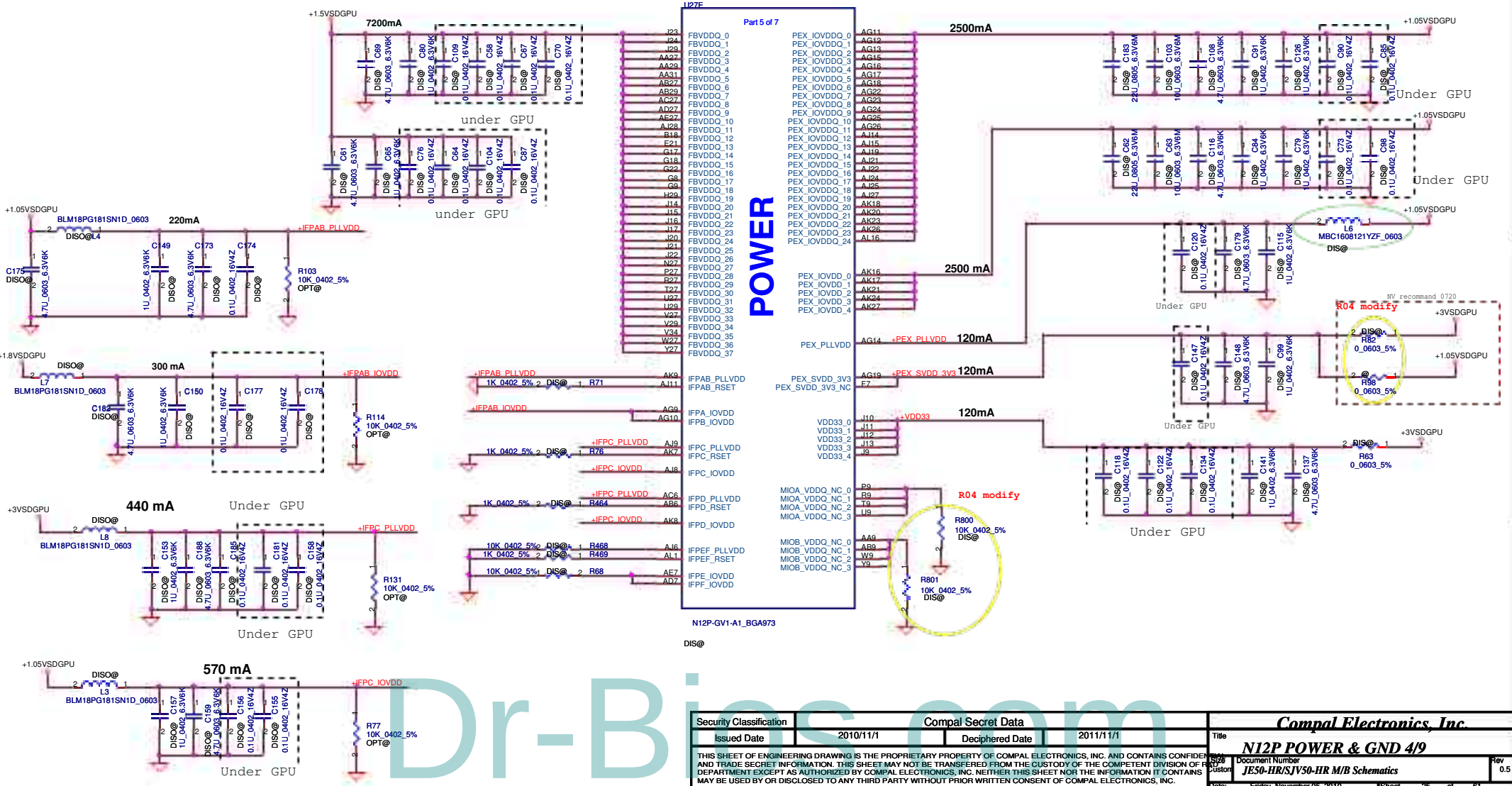

Security Classification	Compal Secret Data		
Issued Date	2010/11/1	Deciphered Date	2011/11/1

Compal Electronics, Inc.

Title: N12P POWER & GND 4/9

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: 0.5

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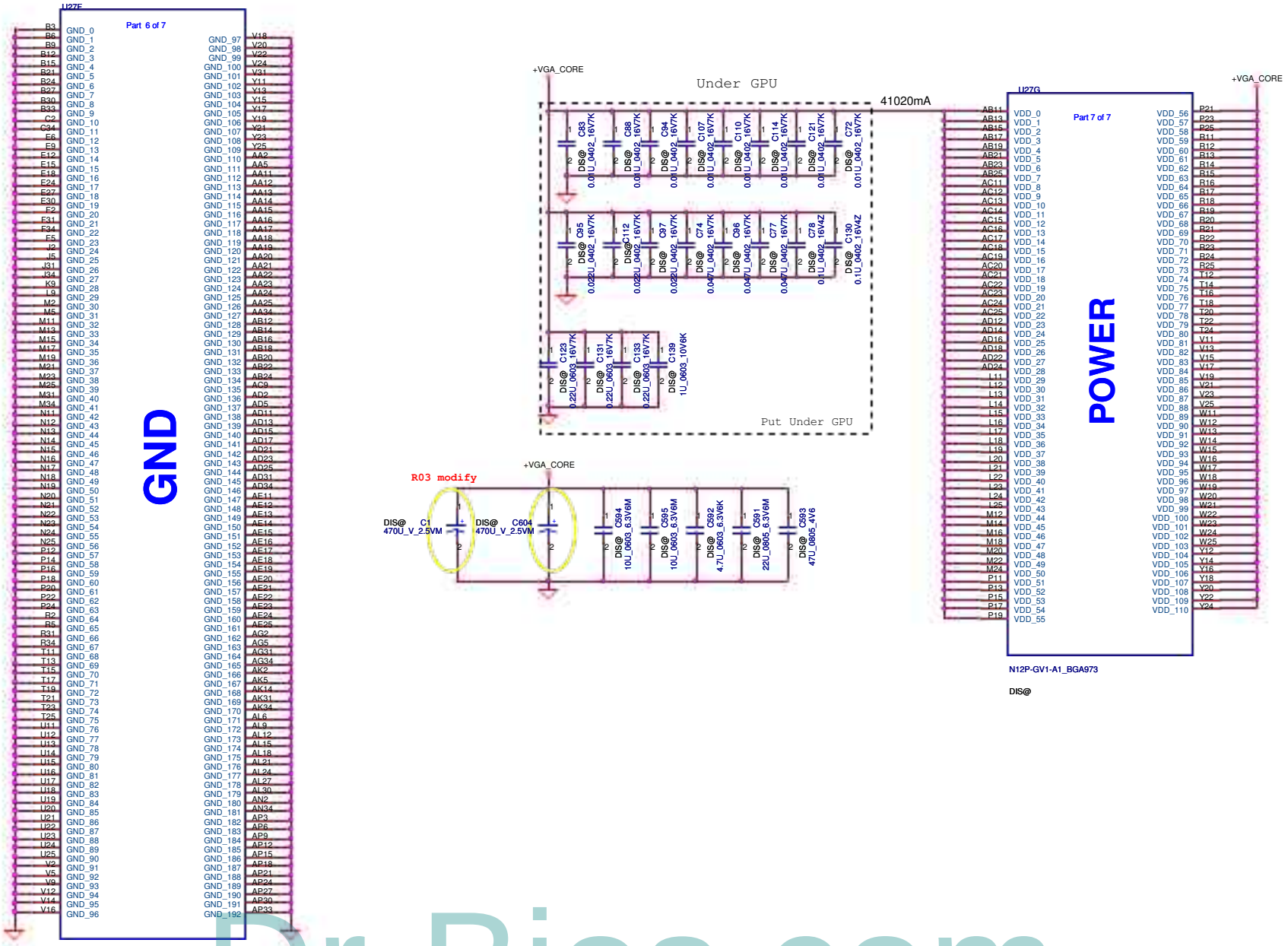

Security Classification	Compal Secret Data		
Issued Date	2010/11/1	Deciphered Date	2011/11/1

Compal Electronics, Inc.

Title: N12P POWER & GND 5/9

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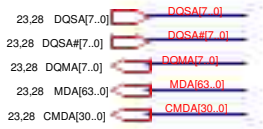
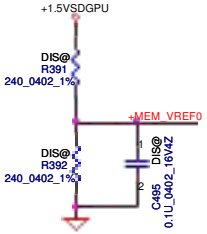
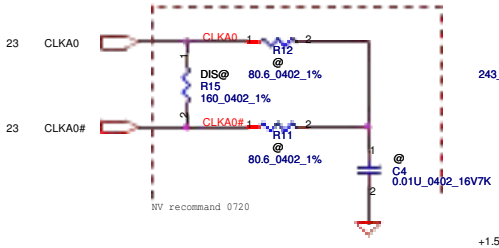
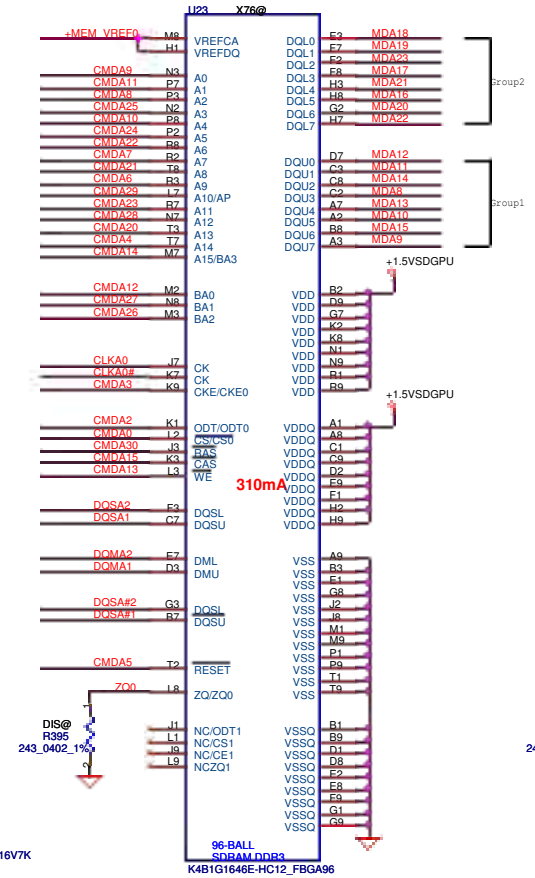
VRAM DDR3 chips (1GB)

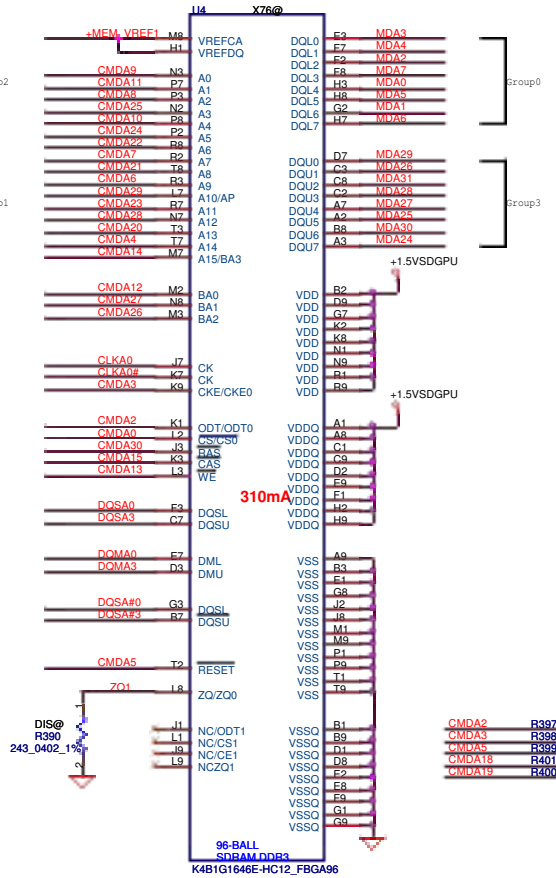
64Mx16 DDR3 *8==>1GB

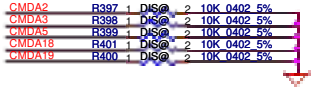






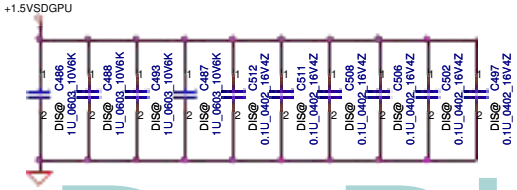


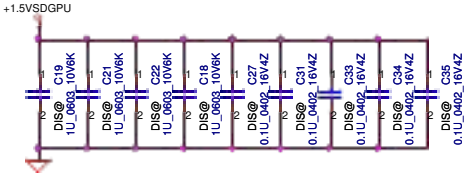




	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH





Samsung : SA000035700 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA 96P)
Hynix : SA000032400 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA 1.5V)
AMD :SA00003PF10
(S IC D3 64M16/800 23EY2387MB-12 PG-TFBGA 96P 1.5V)

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Title: N12P DDR3 6/9

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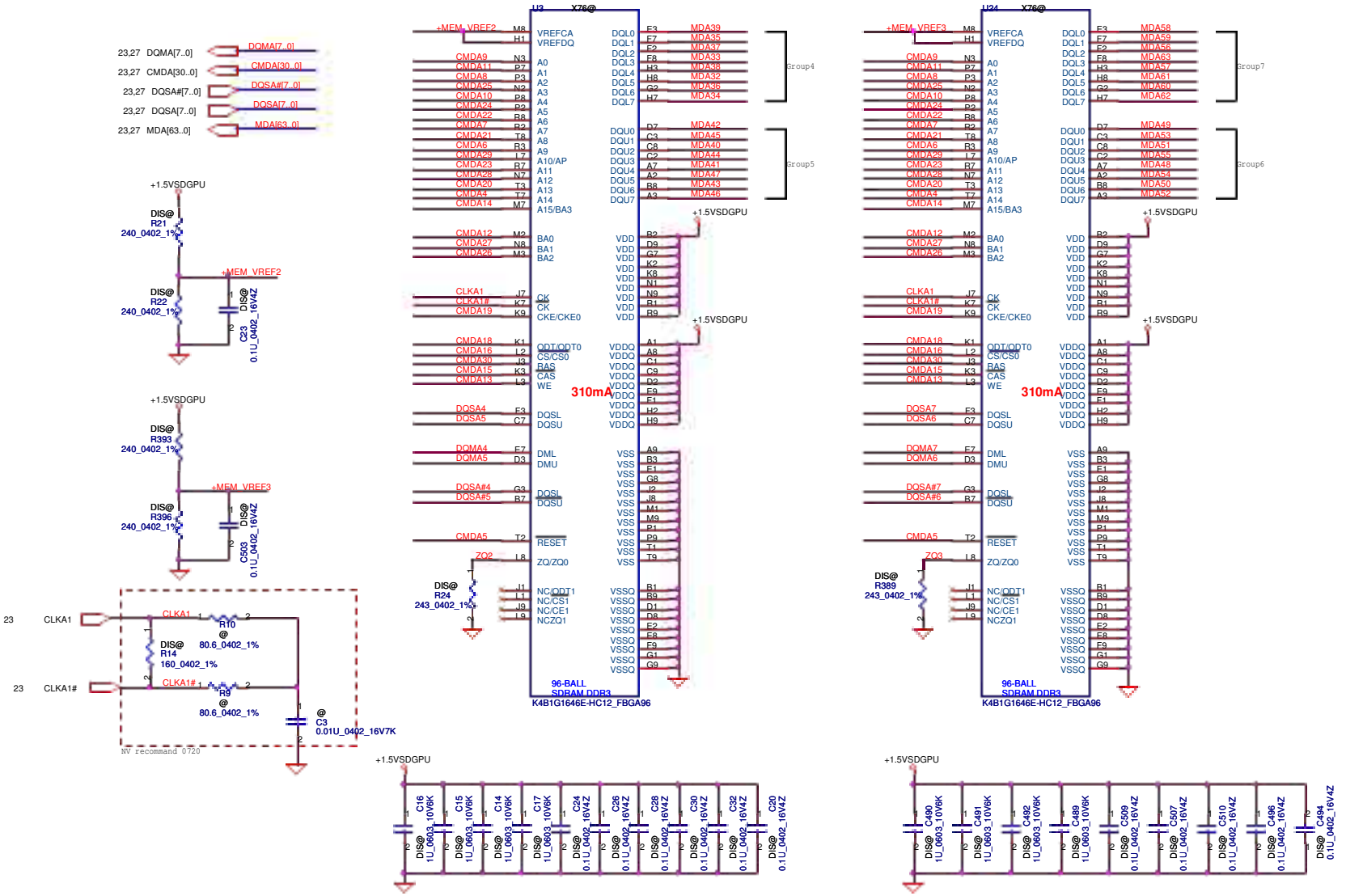
VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: N12P DDR3 7/9

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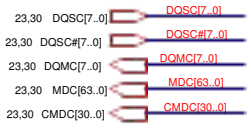
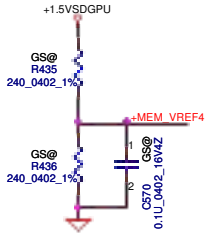
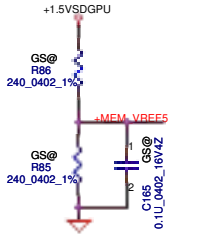
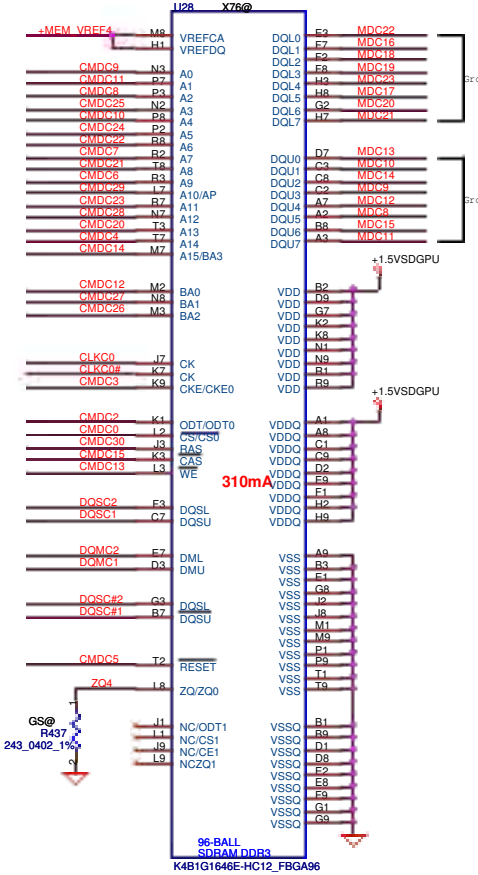
VRAM DDR3 chips (1GB)

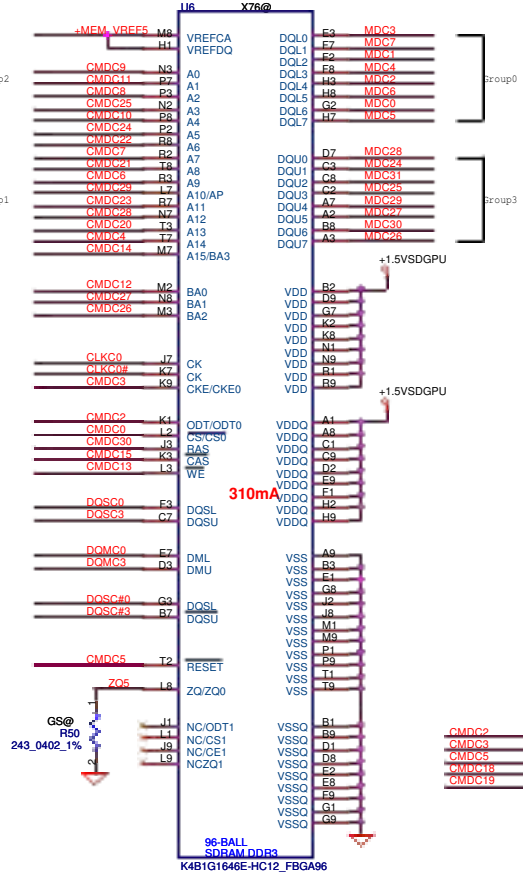
64Mx16 DDR3 *8==>1GB





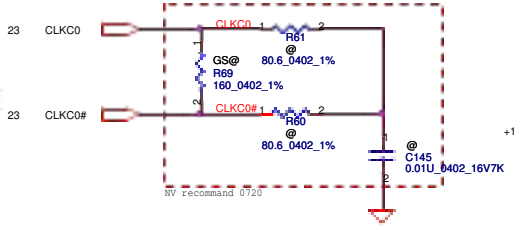


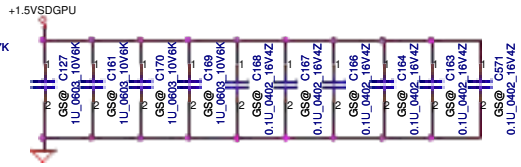


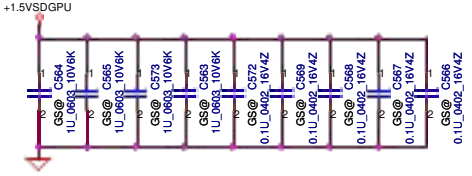


Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination







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Title: N12P DDR3 8/9

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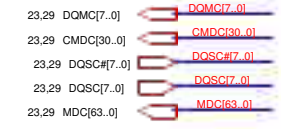
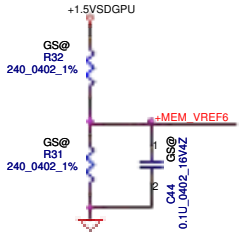
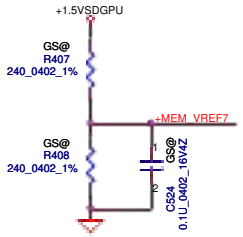
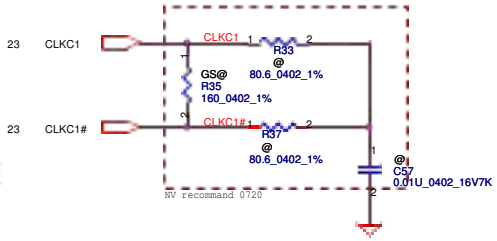
VRAM DDR3 chips (1GB)

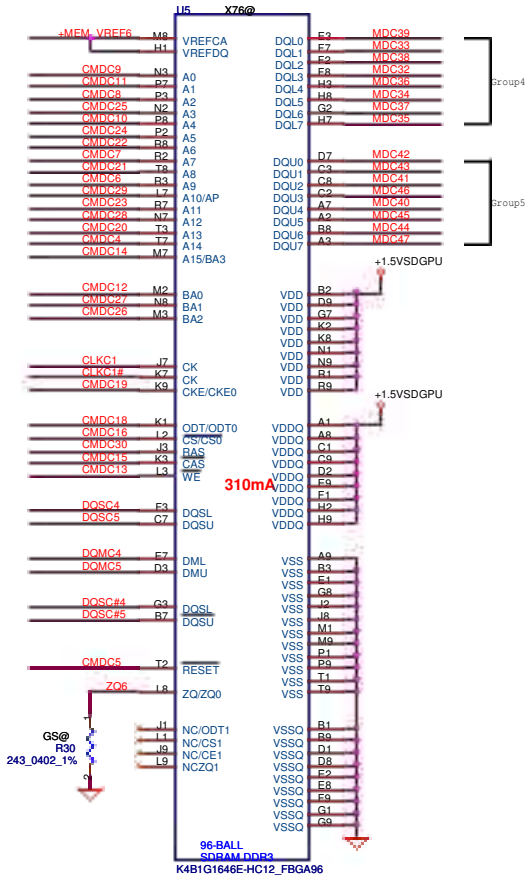
64Mx16 DDR3 *8==>1GB

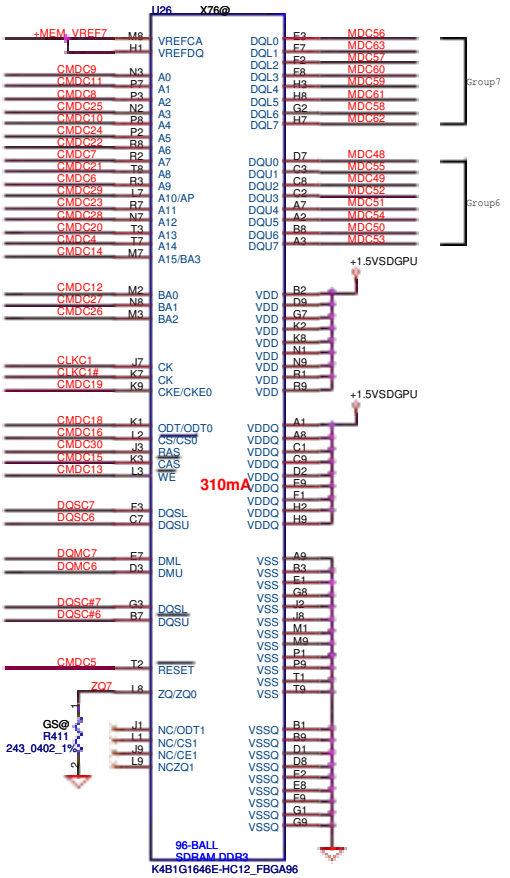


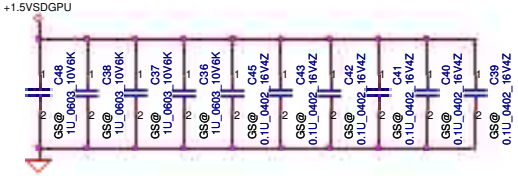


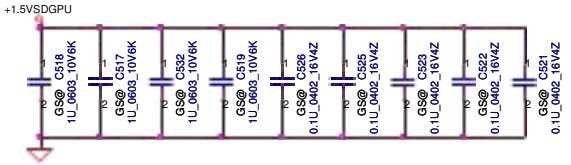












Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

Security Classification	Compal Secret Data		
Issued Date	2010/11/1	Deciphered Date	2011/11/1

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Title: N12P DDR3 9/9

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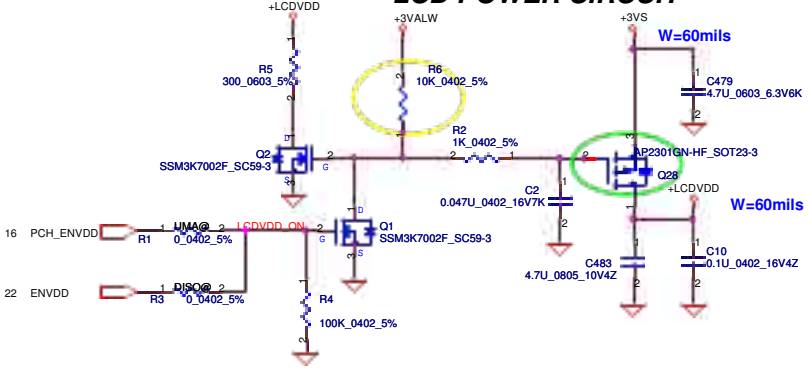
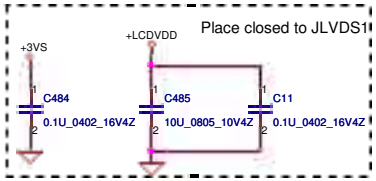
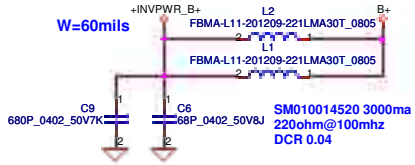
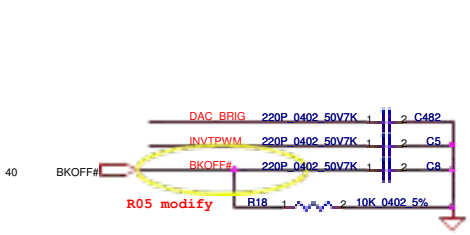
LCD POWER CIRCUIT

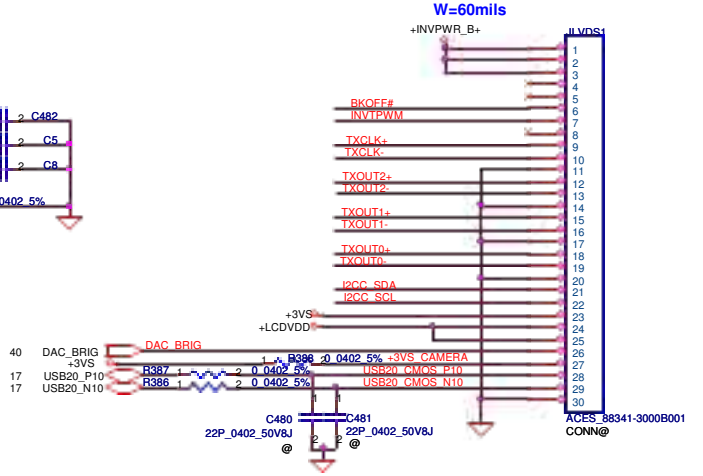




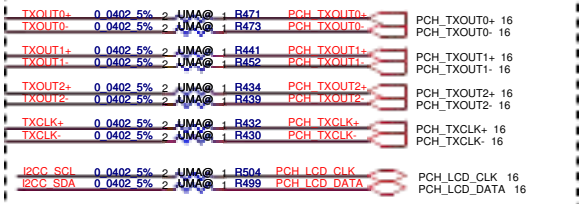


LCD/LED PANEL Conn.

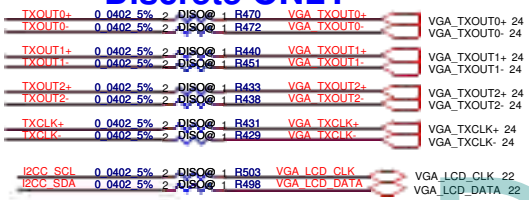


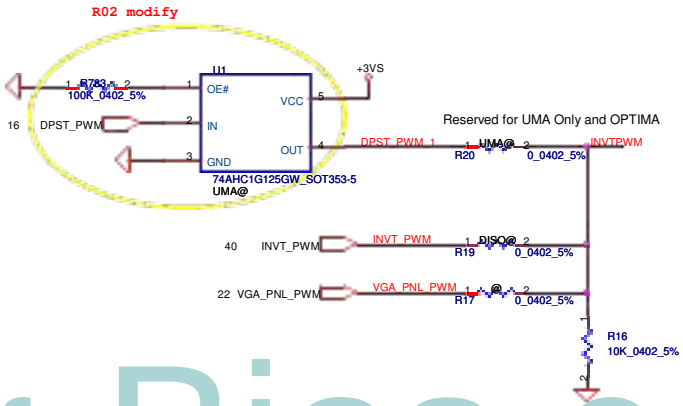


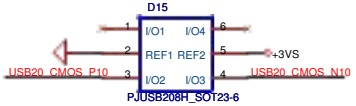
UMA Only / Optimus



Discrete ONLY







Security Classification	Compal Secret Data		
Issued Date	2010/11/1	Deciphered Date	2011/11/1

Compal Electronics, Inc.

Title: LVDS Connector

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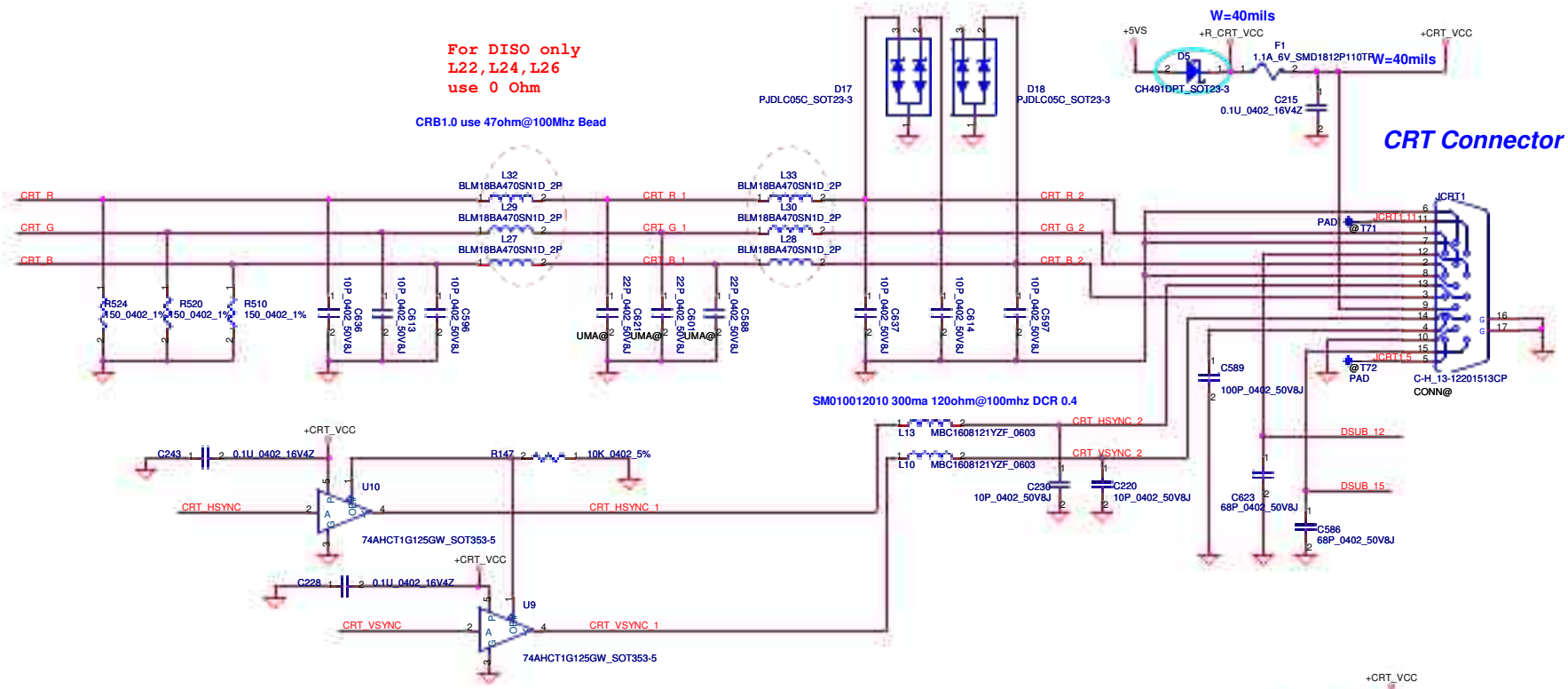

UMA Only / OPTIMUS

16 PCH_CRT_R	PCH_CRT_R	R420	UMA@	0_0402_5%	CRT_R
16 PCH_CRT_G	PCH_CRT_G	R424	UMA@	0_0402_5%	CRT_G
16 PCH_CRT_B	PCH_CRT_B	R422	UMA@	0_0402_5%	CRT_B
16 PCH_CRT_HSYNC	PCH_CRT_HSYNC	R428	UMA@	33_0402_5%	CRT_HSYNC
16 PCH_CRT_VSYNC	PCH_CRT_VSYNC	R426	UMA@	33_0402_5%	CRT_VSYNC
16 PCH_CRT_CLK	PCH_CRT_CLK	R506	UMA@	0_0402_5%	CRT_DDC_CLK
16 PCH_CRT_DATA	PCH_CRT_DATA	R501	UMA@	0_0402_5%	CRT_DDC_DATA

Discrete only

22 VGA_CRT_R	VGA_CRT_R	R419	DISO@	0_0402_5%	CRT_R
22 VGA_CRT_G	VGA_CRT_G	R423	DISO@	0_0402_5%	CRT_G
22 VGA_CRT_B	VGA_CRT_B	R421	DISO@	0_0402_5%	CRT_B
22 VGA_CRT_HSYNC	VGA_CRT_HSYNC	R427	DISO@	0_0402_5%	CRT_HSYNC
22 VGA_CRT_VSYNC	VGA_CRT_VSYNC	R425	DISO@	0_0402_5%	CRT_VSYNC
22 VGA_DDC_CLK	VGA_DDC_CLK	R505	DISO@	0_0402_5%	CRT_DDC_CLK
22 VGA_DDC_DATA	VGA_DDC_DATA	R500	DISO@	0_0402_5%	CRT_DDC_DATA

Security Classification	Compal Secret Data		
Issued Date	2010/11/1	Deciphered Date	2011/11/1

Compal Electronics, Inc.	
Title	CRT Connector
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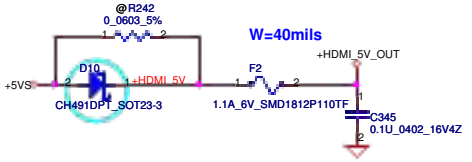
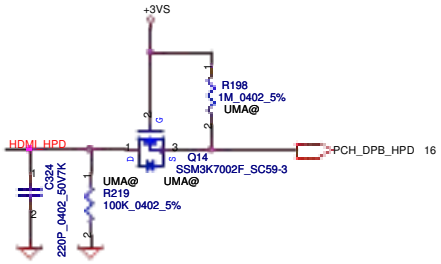
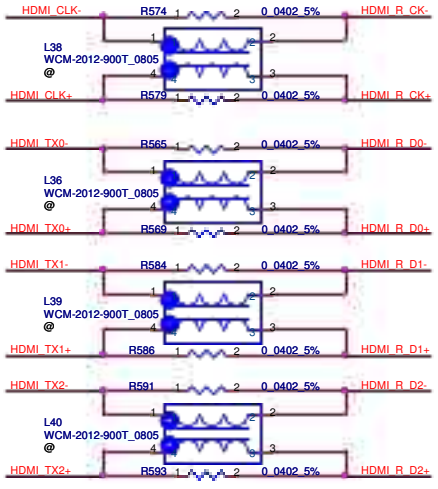
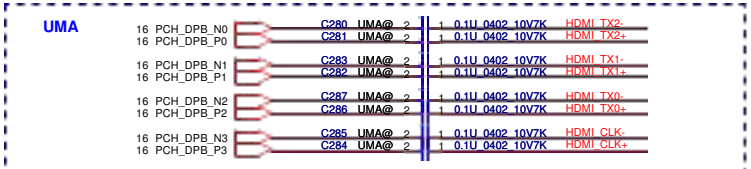
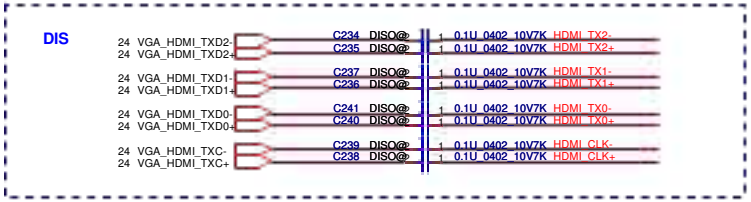


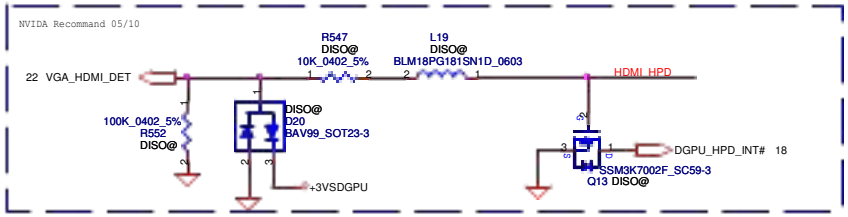


SM070001310 400ma 90ohm@100mhz DCR 0.3



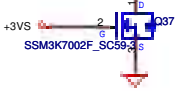




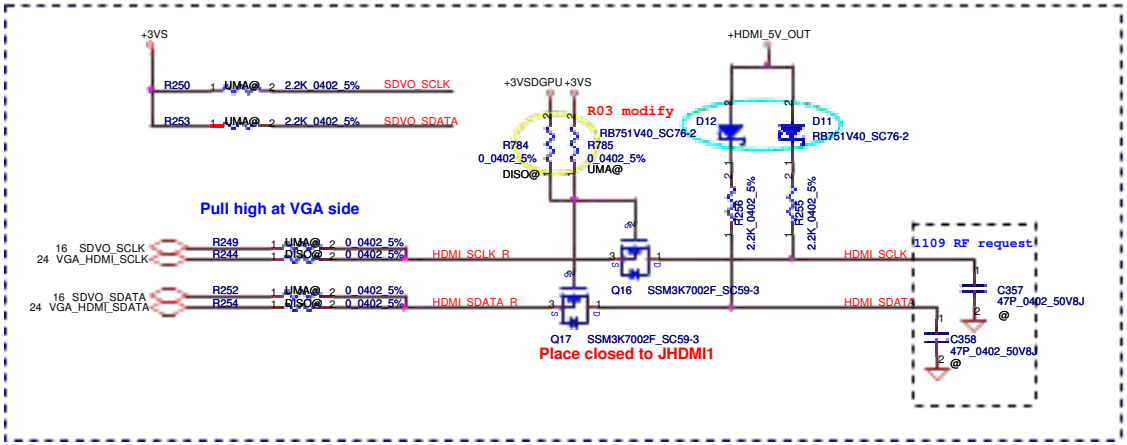


R03 modify

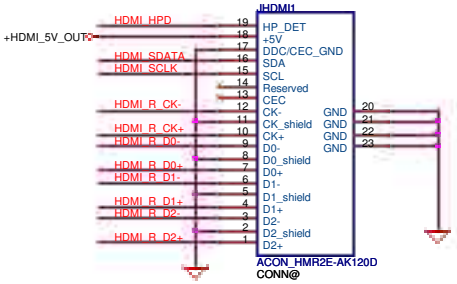
INTEL use 680 Ohm for terminationn in DG 1.5



NV use 499 Ohm for terminationn



HDMI connector



Security Classification	Compal Secret Data		
Issued Date	2010/11/1	Deciphered Date	2011/11/1

Compal Electronics, Inc.	
Title	HDMI Conn
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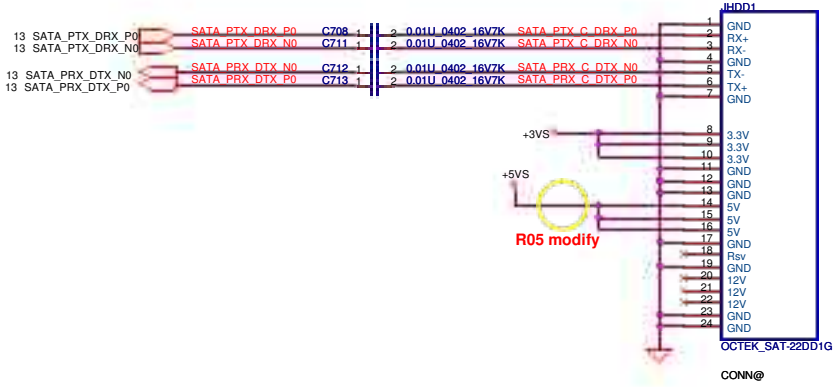
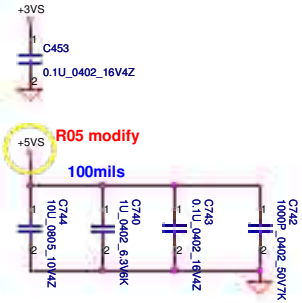
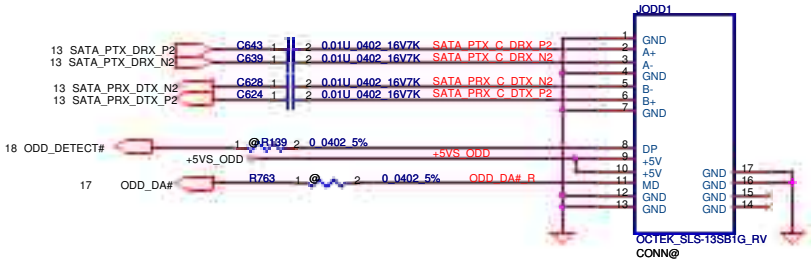
SATA HDD1 Conn.

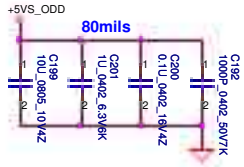
CL 4.0 mm

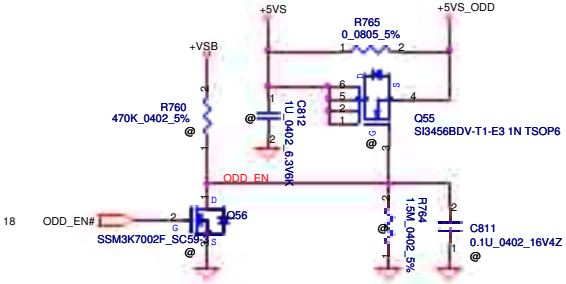




SATA ODD Conn.







Security Classification	Compal Secret Data		
Issued Date	2010/11/1	Deciphered Date	2011/11/1

Compal Electronics, Inc.

Title: HDD & ODD Connector

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: 0.5

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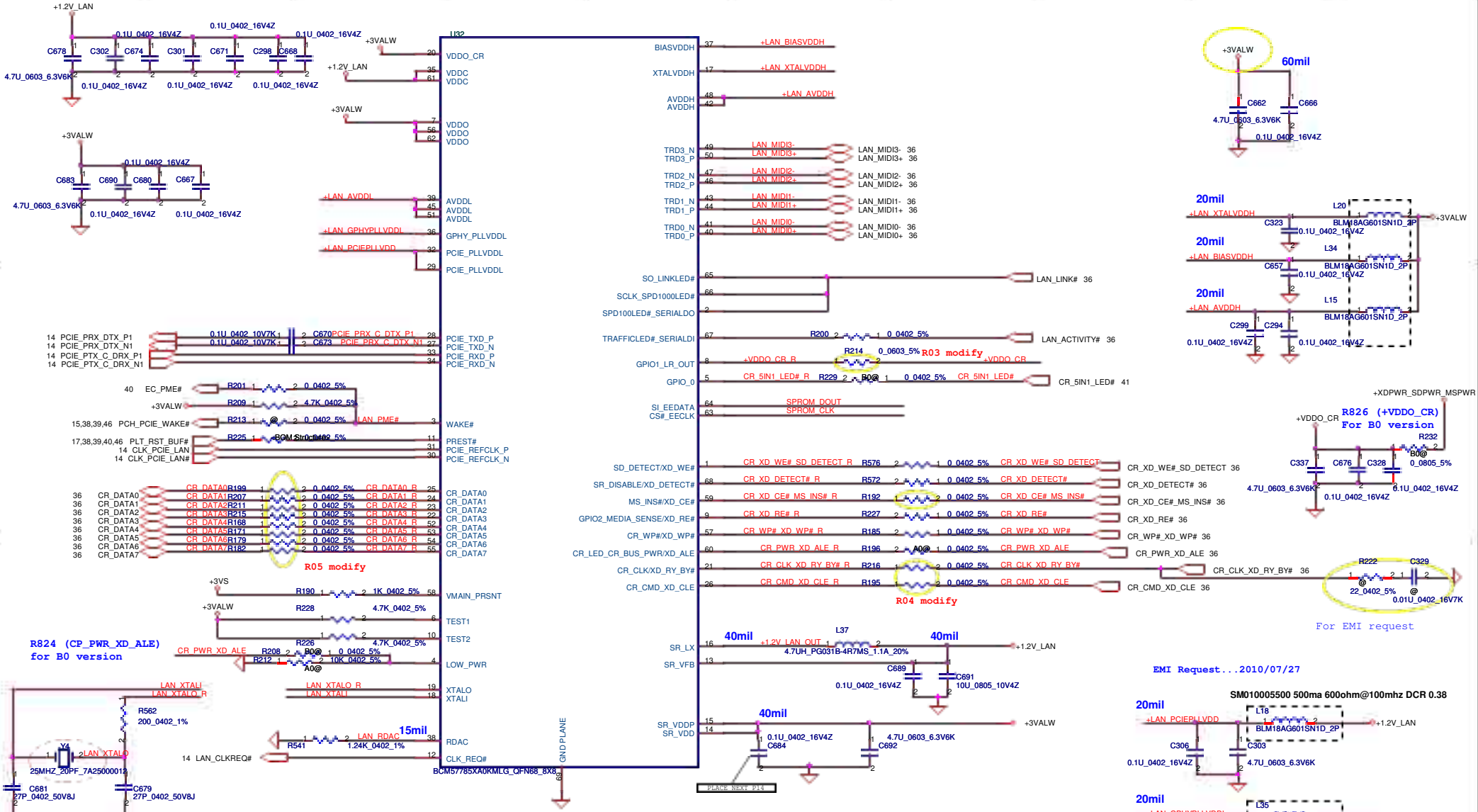

	SPROM_CLK (EECLK)	SPROM_DOUT (EEDATA)
On chip	1	0
AT24C02	1	1

Security Classification	Compal Secret Data		
Issued Date	2010/11/1	Deciphered Date	2011/11/1

Compal Electronics, Inc.

Title: Broadcom BCM57785

Size: B2B Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: 0.5

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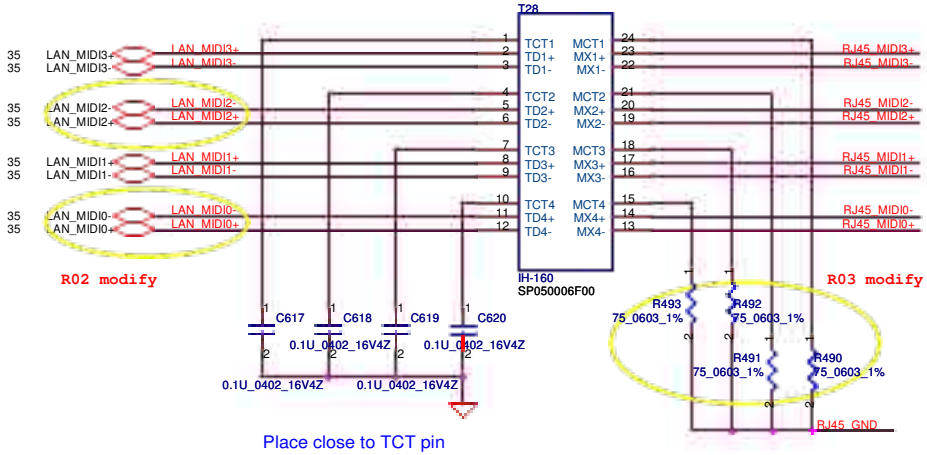
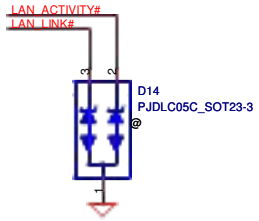
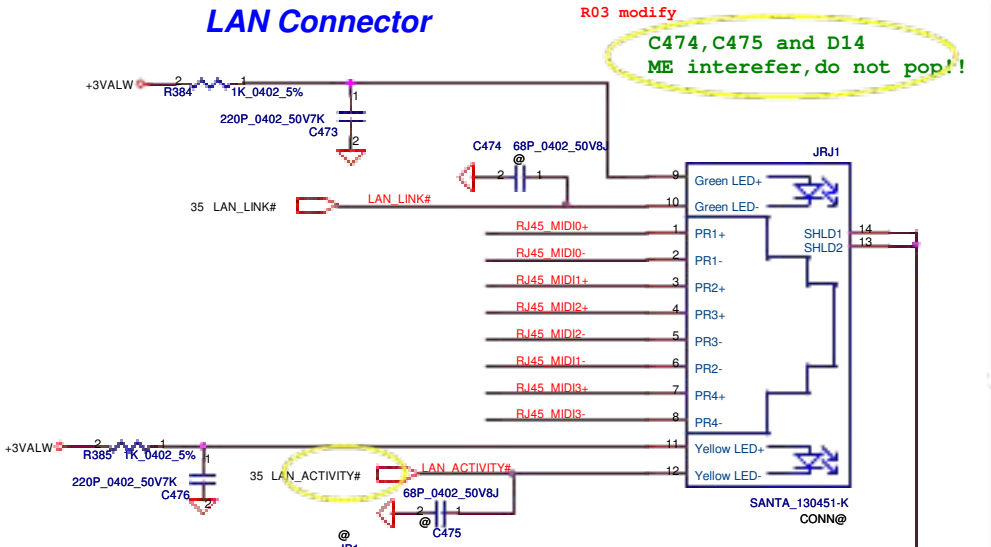


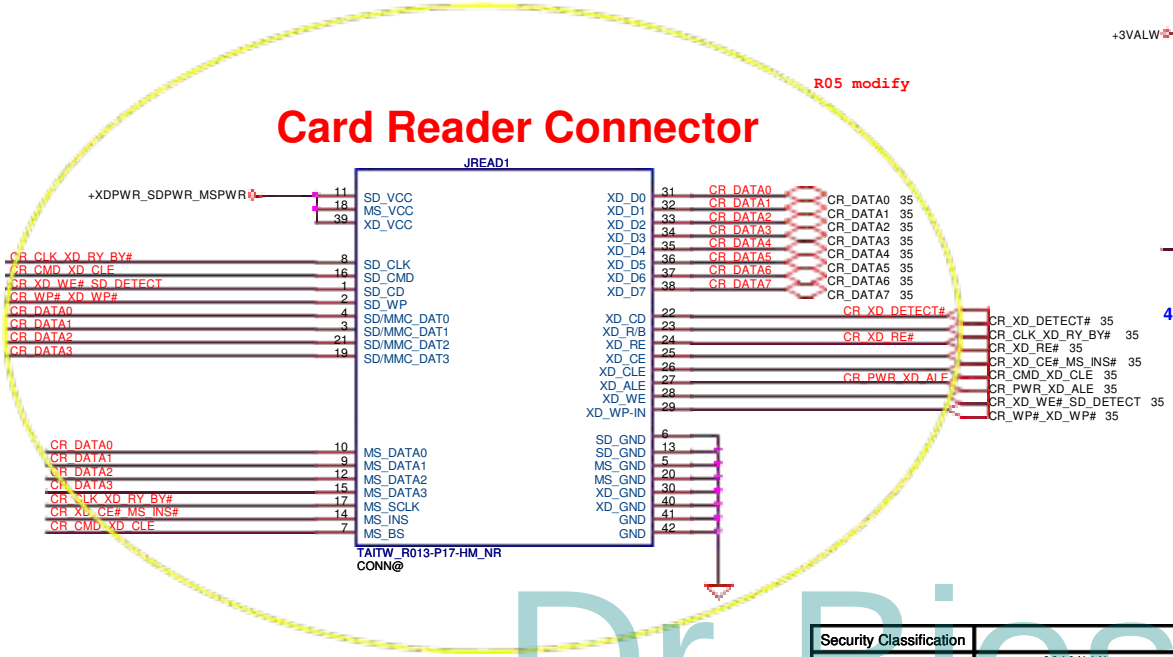
BOTHHAND: S X'FORM_ GST5009-D LF LAN, SP050006B00
TIMAG:S X'FORM_ IH-160 LAN , SP050006F00



LAN Connector



Card Reader Connector



Security Classification	Compal Secret Data		
Issued Date	2010/11/1	Deciphered Date	2011/11/1

Compal Electronics, Inc.			
Title	LAN Magnetic & RJ45		
Size	Document Number		Rev
Custom	JE50-HR/SJV50-HR M/B Schematics		0.5
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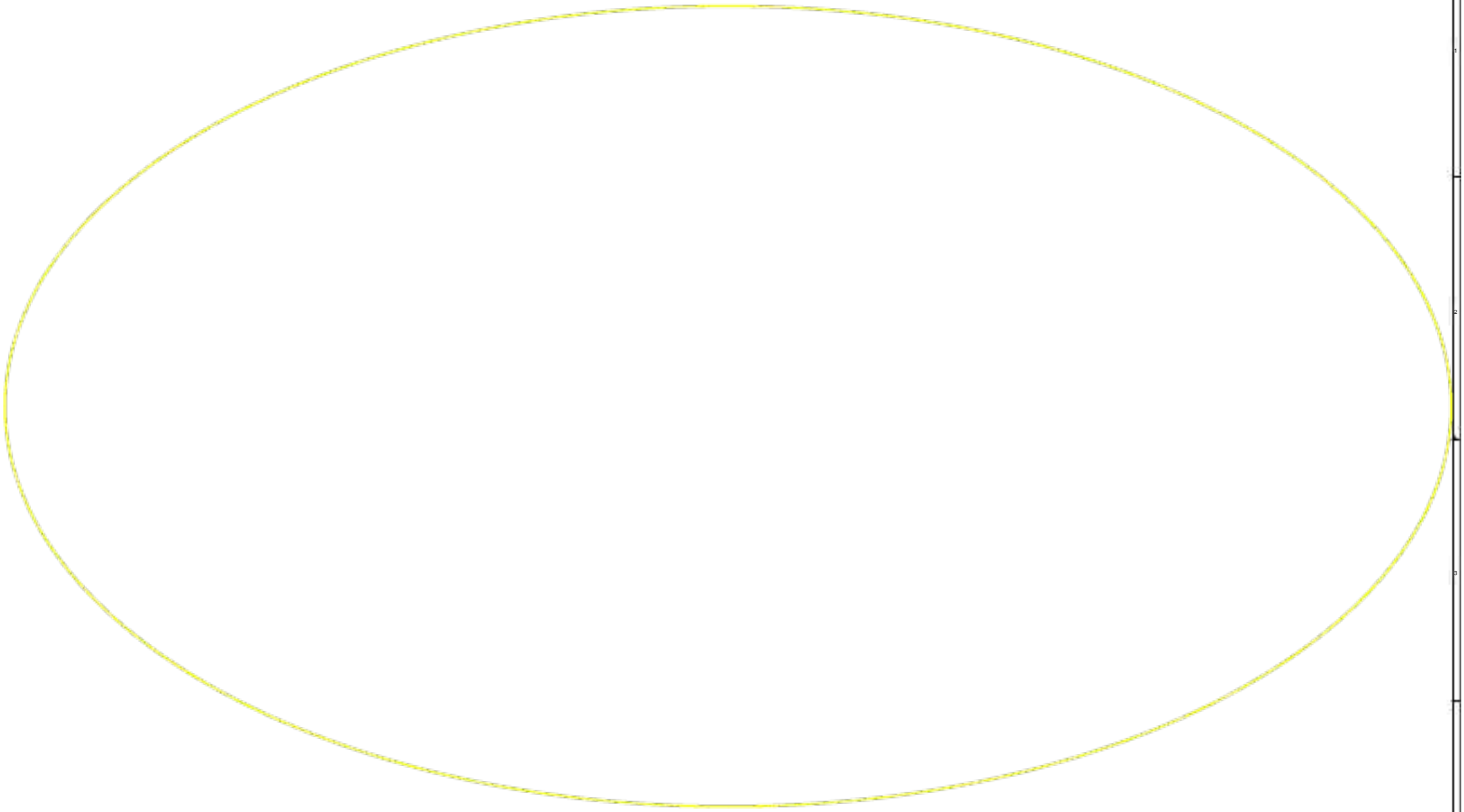

Security Classification	Compal Secret Data		
Issued Date	2010/11/1	Deciphered Date	2011/11/1

Compal Electronics, Inc.

Title: RTS5138 Card Reader

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: 0.5

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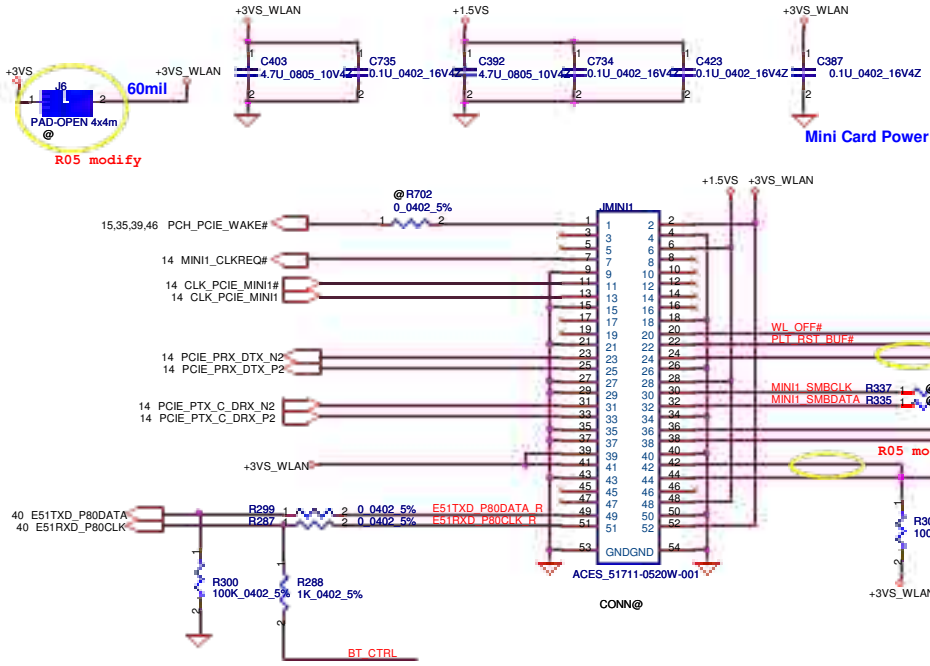
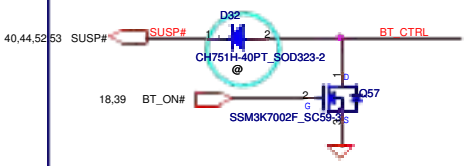
For Wireless LAN

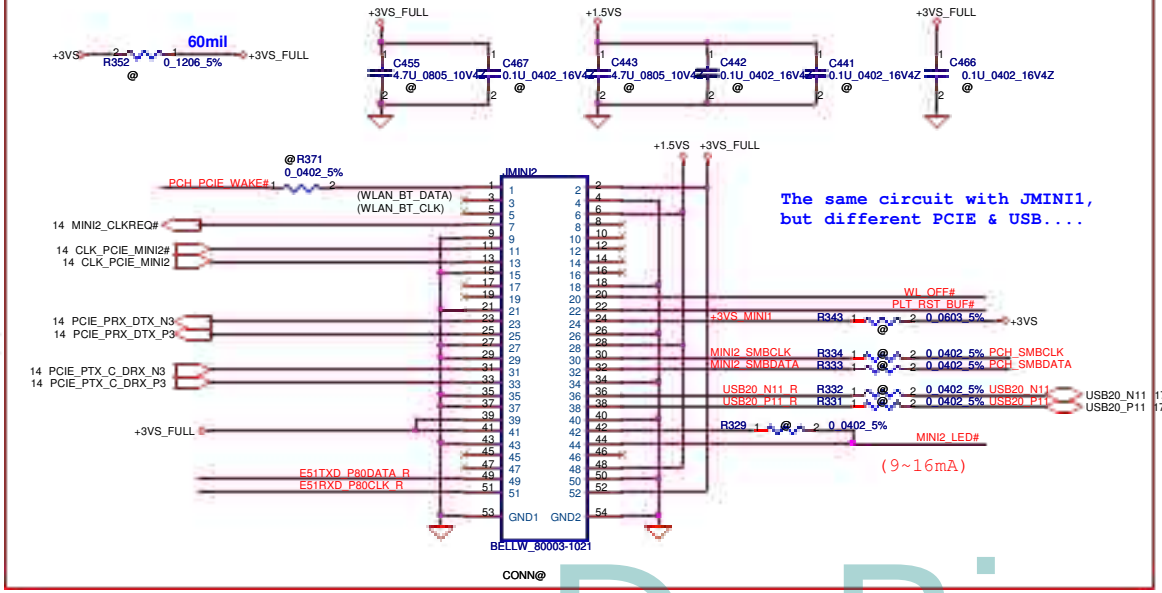


WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_CTRL	H	L
BT_ON#	L	H

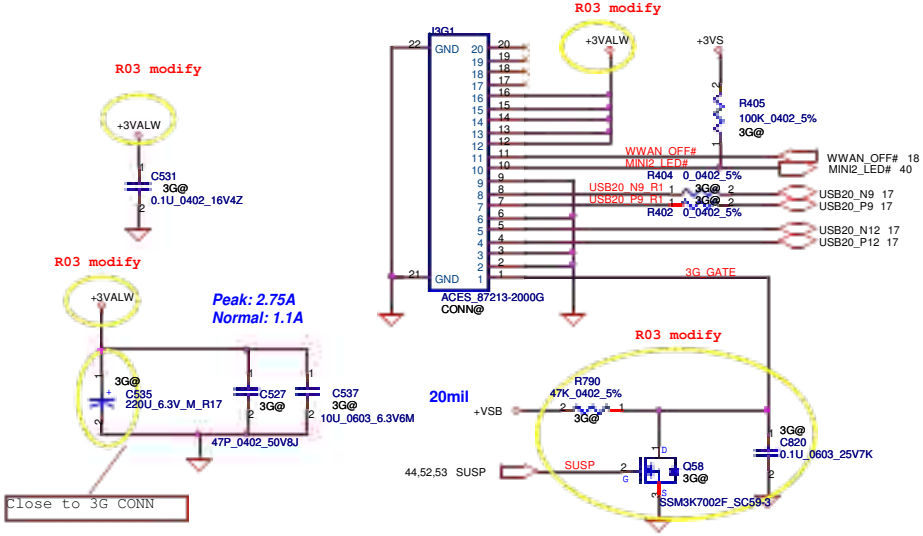


Reserve



For 3G / GPS

To 3G Module Connect



Security Classification	Compal Secret Data		
Issued Date	2010/11/1	Deciphered Date	2011/11/1

Compal Electronics, Inc.

Title: MINI CARD (WLAN & TV-Tuner)

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: 0.5

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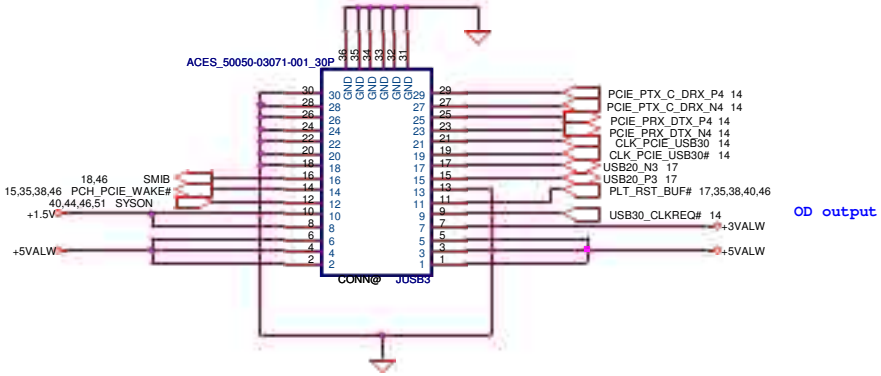
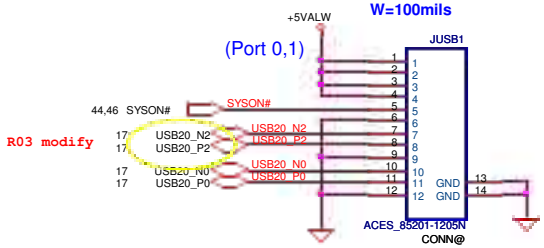
USB3.0 Conn.

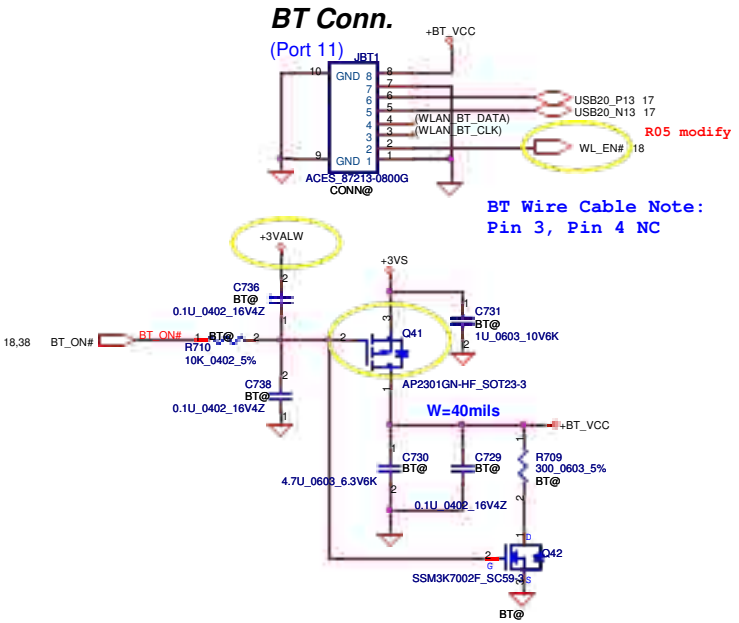


OD output

USB/B Conn.



BT Conn.



Security Classification	Compal Secret Data		
Issued Date	2010/11/1	Deciphered Date	2011/11/1

Compal Electronics, Inc.

Title: USB / BT / USBB

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: 0.5

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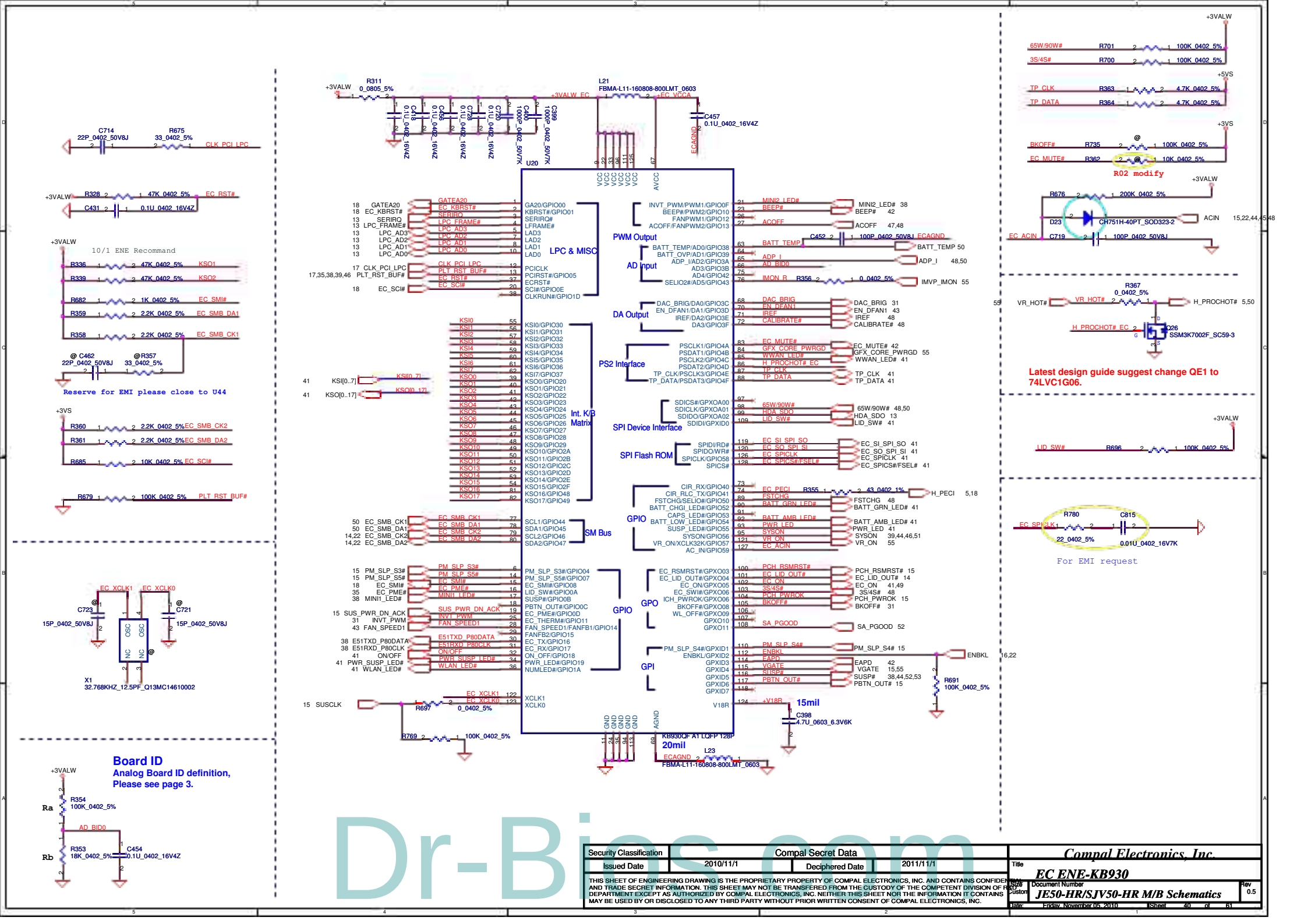

Security Classification	Compal Secret Data		
Issued Date	2010/11/1	Deciphered Date	2011/11/1

Compal Electronics, Inc.

Title: EC ENE-KB930

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: 0.5

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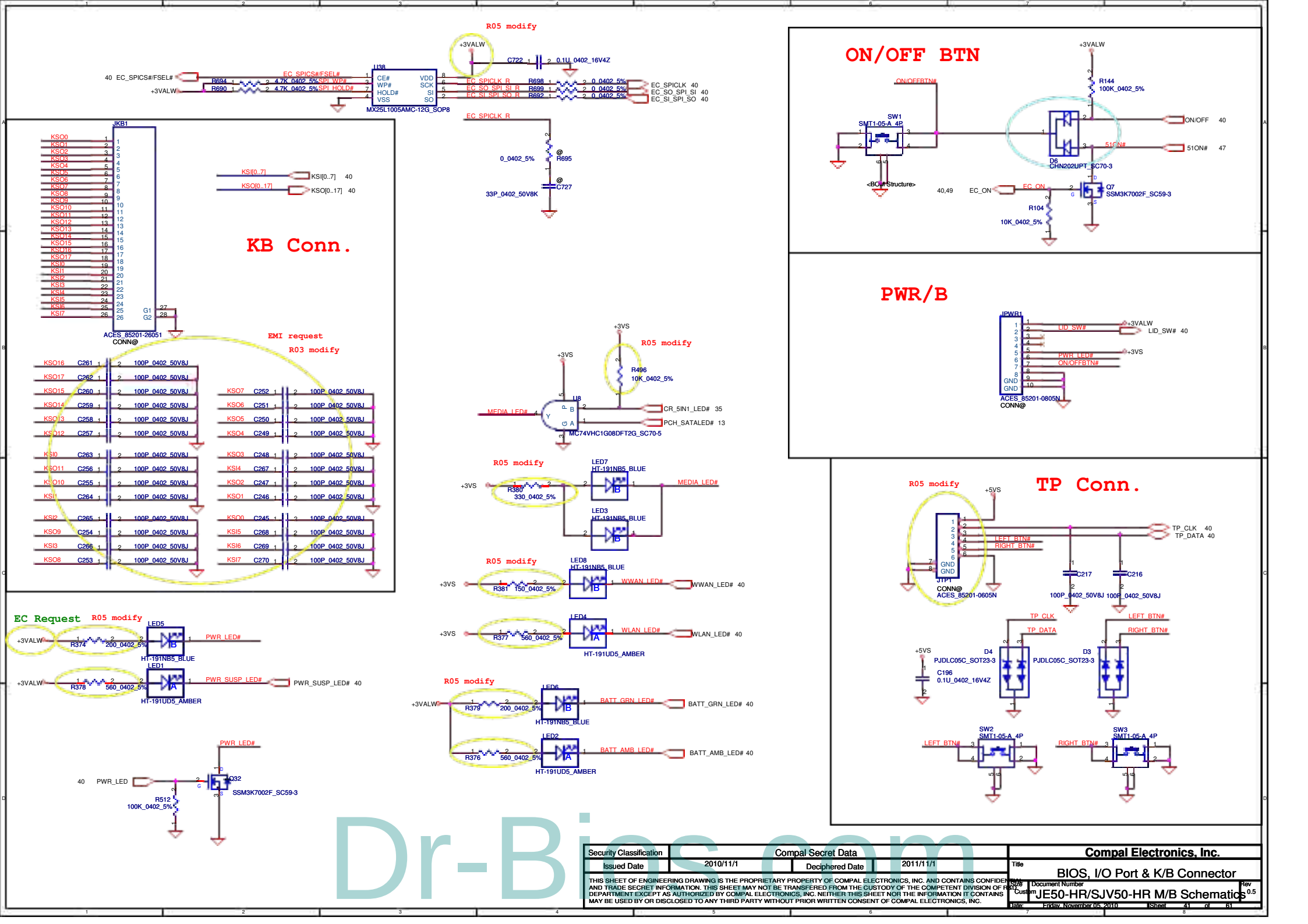

Security Classification	Compal Secret Data		
Issued Date	2010/11/1	Deciphered Date	2011/11/1

Compal Electronics, Inc.

Title: BIOS, I/O Port & K/B Connector

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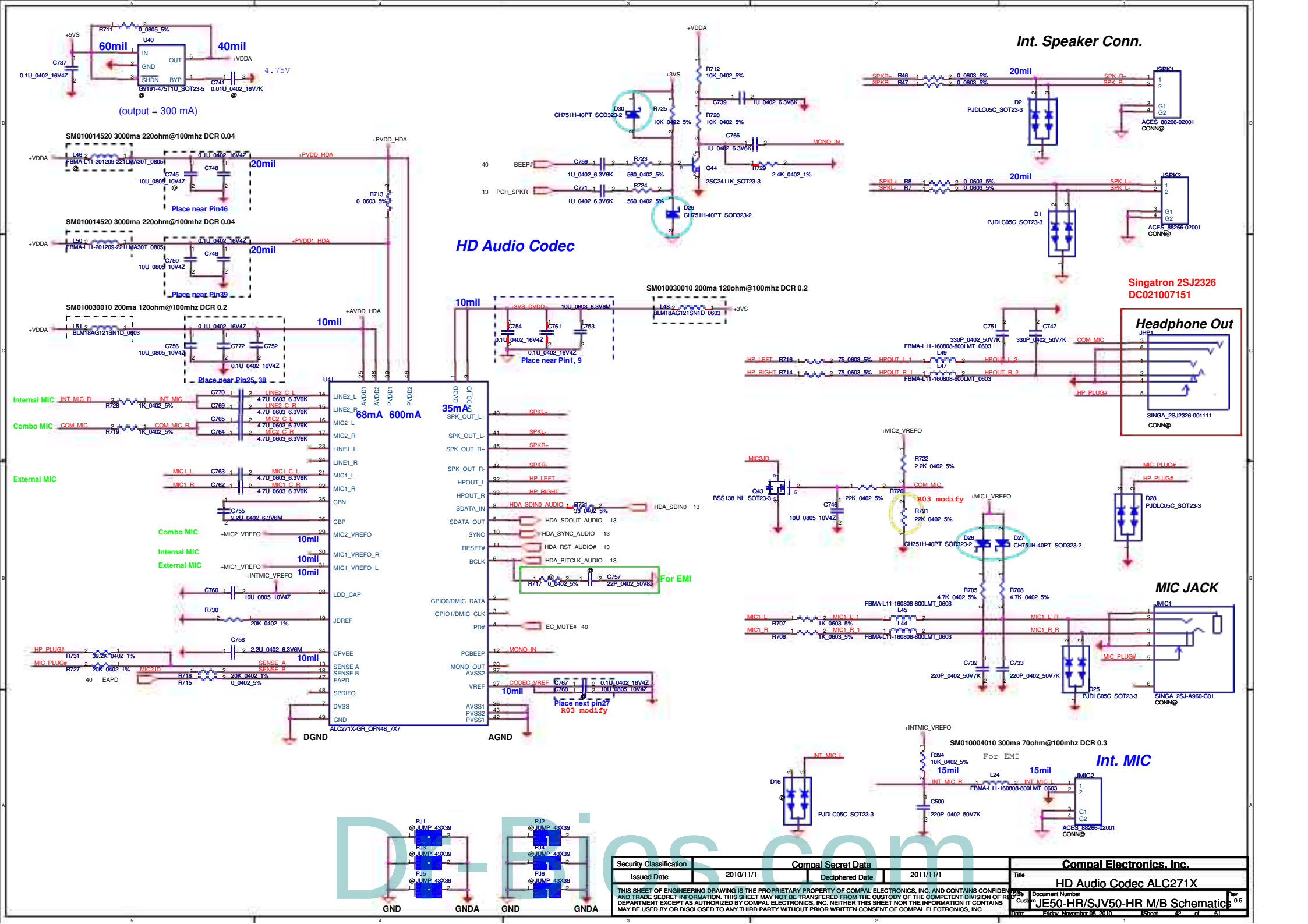
Int. Speaker Conn.
HD Audio Codec
Headphone Out
Singatron 2SJ2326
DC021007151
MIC JACK
Int. MIC
60mil
40mil
4.75V
(output = 300 mA)
SM010014520 3000ma 220ohm@100mhz DCR 0.04
SM010030010 200ma 120ohm@100mhz DCR 0.2
SM010004010 300ma 70ohm@100mhz DCR 0.3
Place near Pin46
Place near Pin39
Place near Pin25, 38
Place near Pin1, 9
Place next pin27
R03 modify
For EMI
Internal MIC
Combo MIC
External MIC
68mA 600mA
35mA
ALC271X-GR_QFN48_7X7
DGND
AGND
GND
GNDA
Security Classification
Compal Secret Data
Issued Date
2010/11/1
Deciphered Date
2011/11/1
Compal Electronics, Inc.
HD Audio Codec ALC271X
JE50-HR/SJV50-HR M/B Schematics
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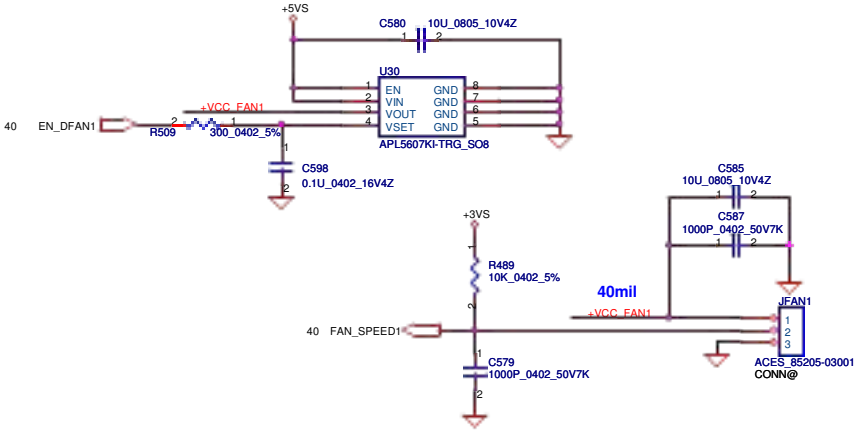
FAN Stand-Off

JUSB3 Stand-Off

H1 H_3P4 @
H2 H_3P4 @
H3 H_3P4 @
H4 H_3P4 @
H5 H_3P4 @
H6 H_3P4 @
H7 H_3P4 @
H8 H_3P0 @
H9 H_3P0 @
H10 H_3P0 @
H11 H_3P0 @
H12 H_3P0 @
H13 H_3P0 @
H14 H_3P0 @
H15 H_3P0 @
H16 H_3P0 @
H17 H_3P0 @
H18 H_3P0 @
H19 H_4P0 @
H20 H_4P0 @
H21 H_4P2 @
H22 H_4P2 @
H23 H_4P2 @
H24 H_4P2 @
H25 H_7P0N @
H26 H_3P0N @
H27 H_3P5X3P0N @

FAN1 Conn



FD1 FIDUCIAL_C40M80
FD3 FIDUCIAL_C40M80
FD2 FIDUCIAL_C40M80
FD4 FIDUCIAL_C40M80

Security Classification	Compal Secret Data		
Issued Date	2010/11/1	Deciphered Date	2011/11/1

Compal Electronics, Inc.	
Title	FAN & Screw Hole
Size: Custom	Document Number: JE50-HR/SJV50-HR M/B Schematics
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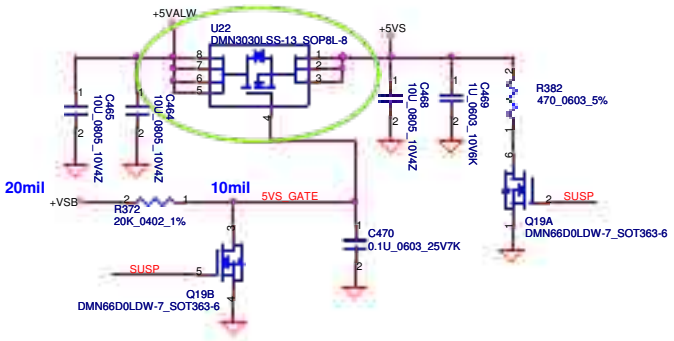
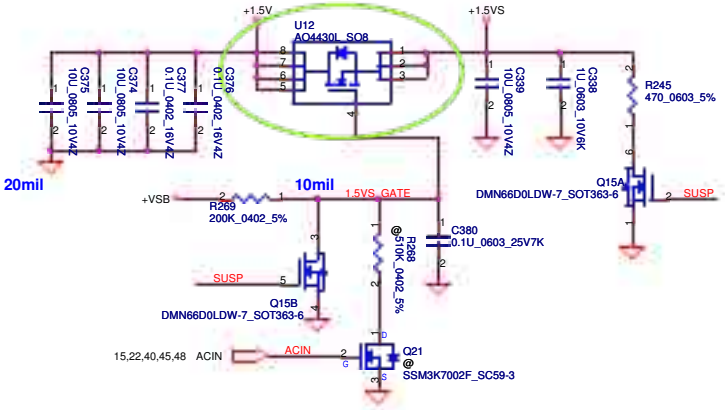
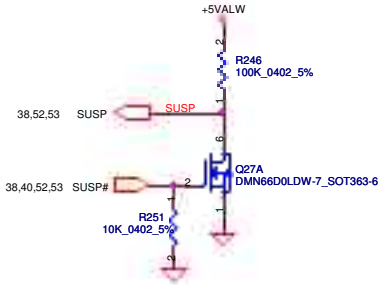
+5VALW TO +5VS

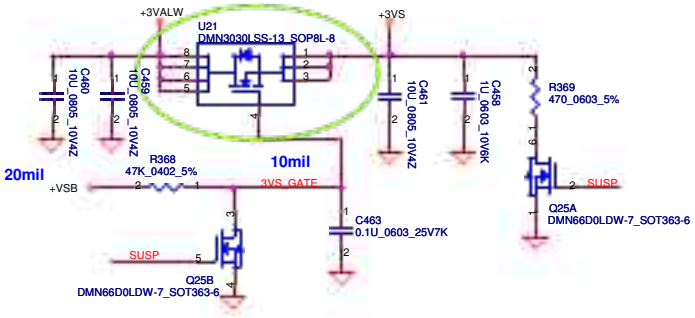


+1.5V to +1.5VS

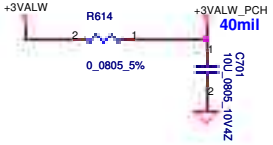


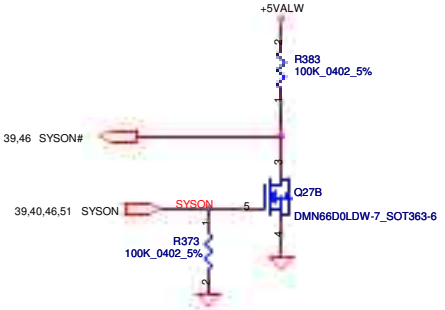


+3VALW TO +3VS

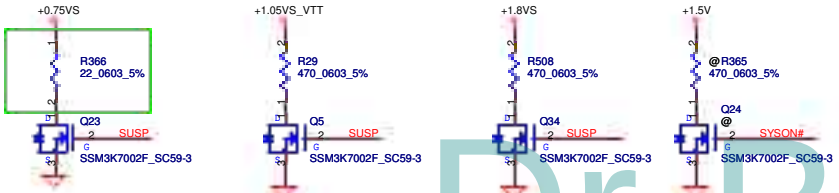


+3VALW TO +3VALW_PCH(PCH AUX Power)





+5VALW TO +5VALW_PCH(PCH AUX Power)



Security Classification	Compal Secret Data		
Issued Date	2010/11/1	Deciphered Date	2011/11/1

Compal Electronics, Inc.

Title: DC Interface

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: 0.5

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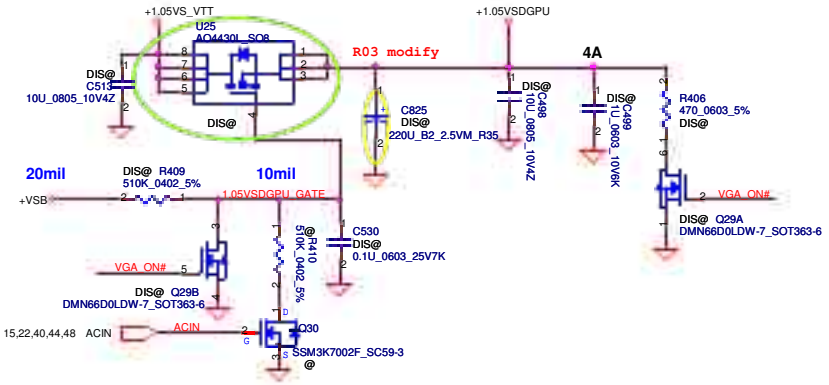
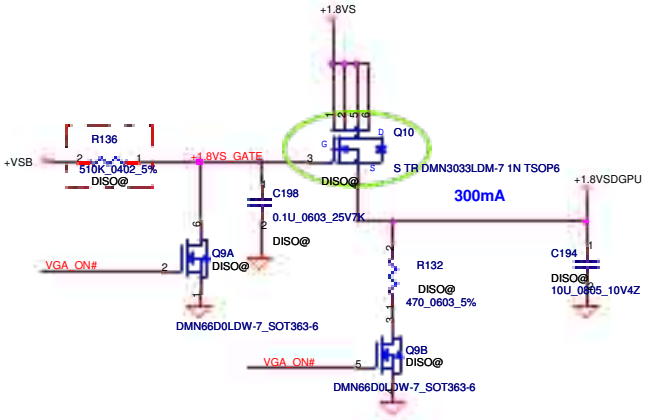
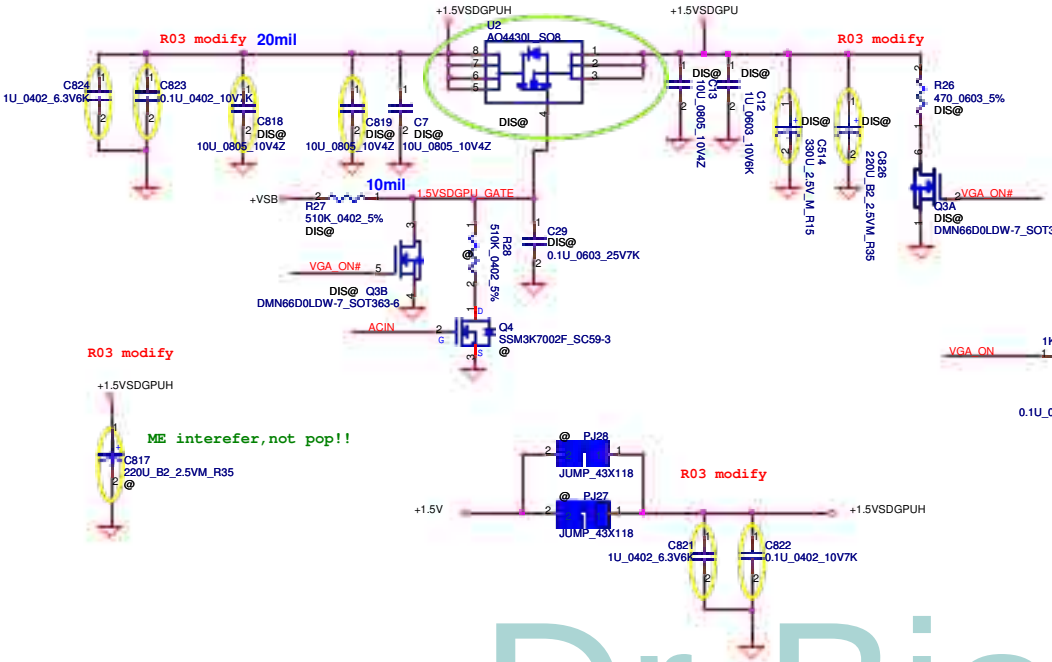
+1.05VS_VTT to +1.05VSDGPU for GPU



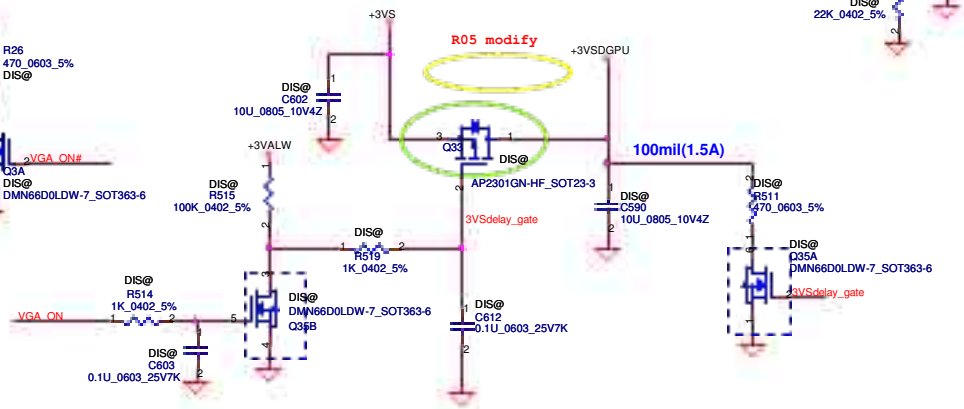
+1.8VS to +1.8VSDGPU for GPU

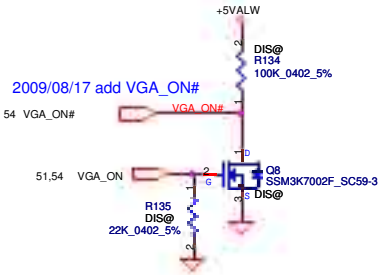


+1.5VSDGPUH to +1.5VSDGPU for GPU



+3VS to +3VSDGPU for GPU





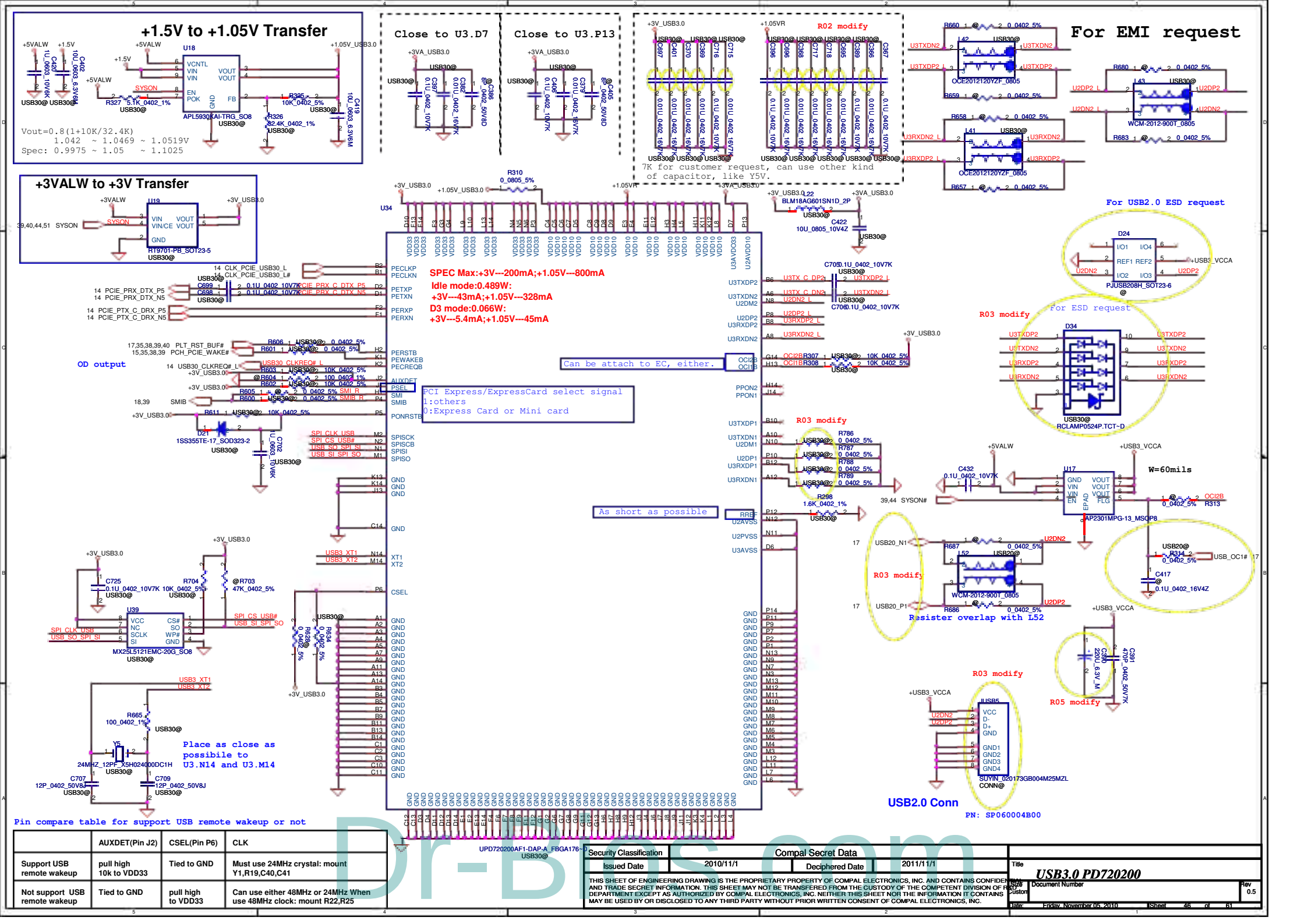
Security Classification	Compal Secret Data		
Issued Date	2010/11/1	Deciphered Date	2011/11/1

Compal Electronics, Inc.

Title: DC Interface

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: 0.5

Date: Friday, November 05, 2010 | Sheet 45 of 61



Pin compare table for support USB remote wakeup or not

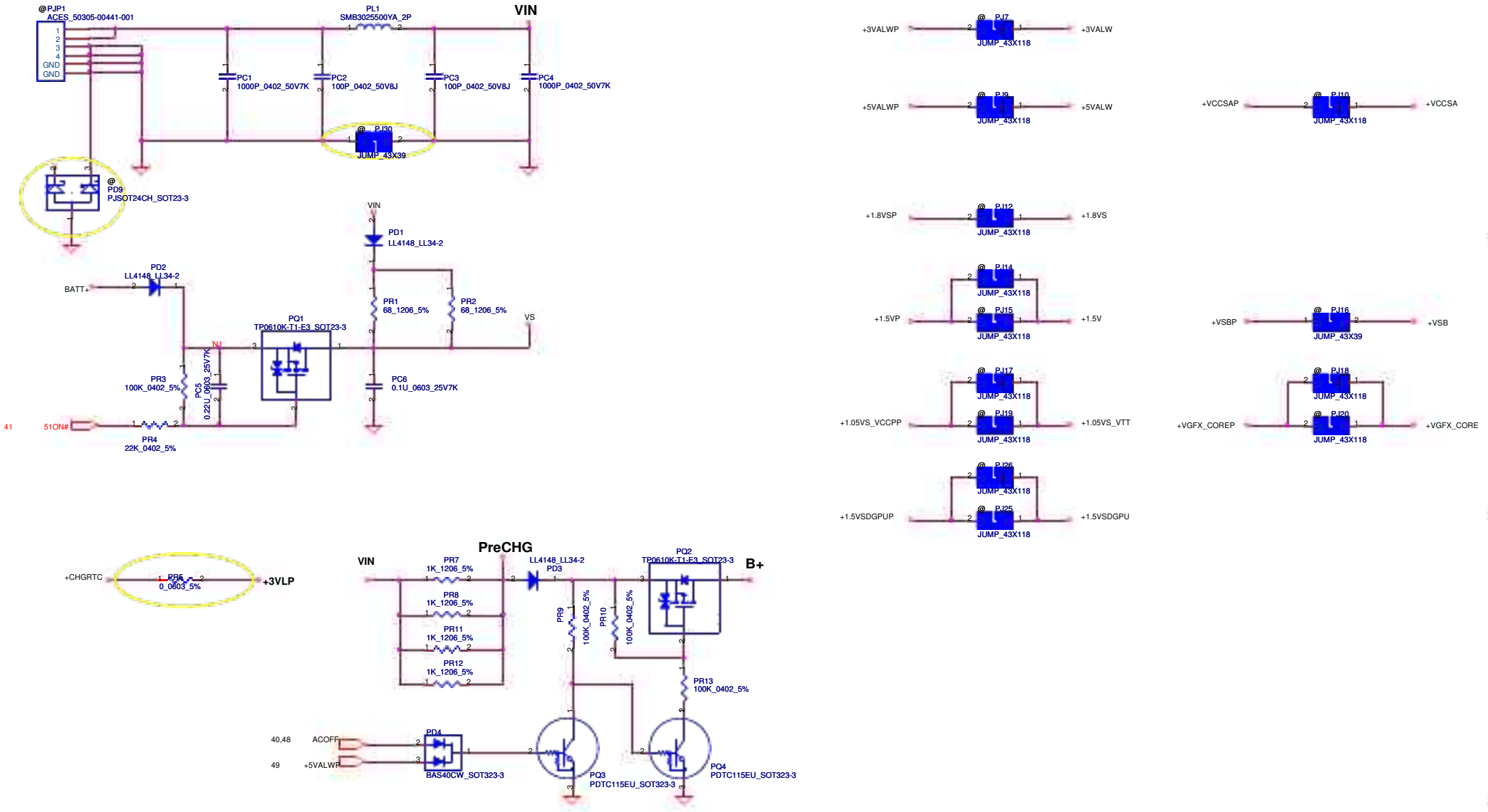
	AUXDET(Pin J2)	CSEL(Pin P6)	CLK
Support USB remote wakeup	pull high 10k to VDD33	Tied to GND	Must use 24MHz crystal: mount Y1,R19,C40,C41
Not support USB remote wakeup	Tied to GND	pull high to VDD33	Can use either 48MHz or 24MHz When use 48MHz clock: mount R22,R25

Security Classification	Compal Secret Data		
Issued Date	2010/11/1	Deciphered Date	2011/11/1

Title: USB3.0 PD720200

Size: Custom | Document Number | Rev: 0.5

Date: Friday, November 05, 2010 | Sheet 46 of 61



Security Classification	Compal Secret Data		
Issued Date	2010/11/1	Deciphered Date	2011/11/1

Compal Electronics, Inc.

Title: PWR DCIN / Pre-charge

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: 0.5

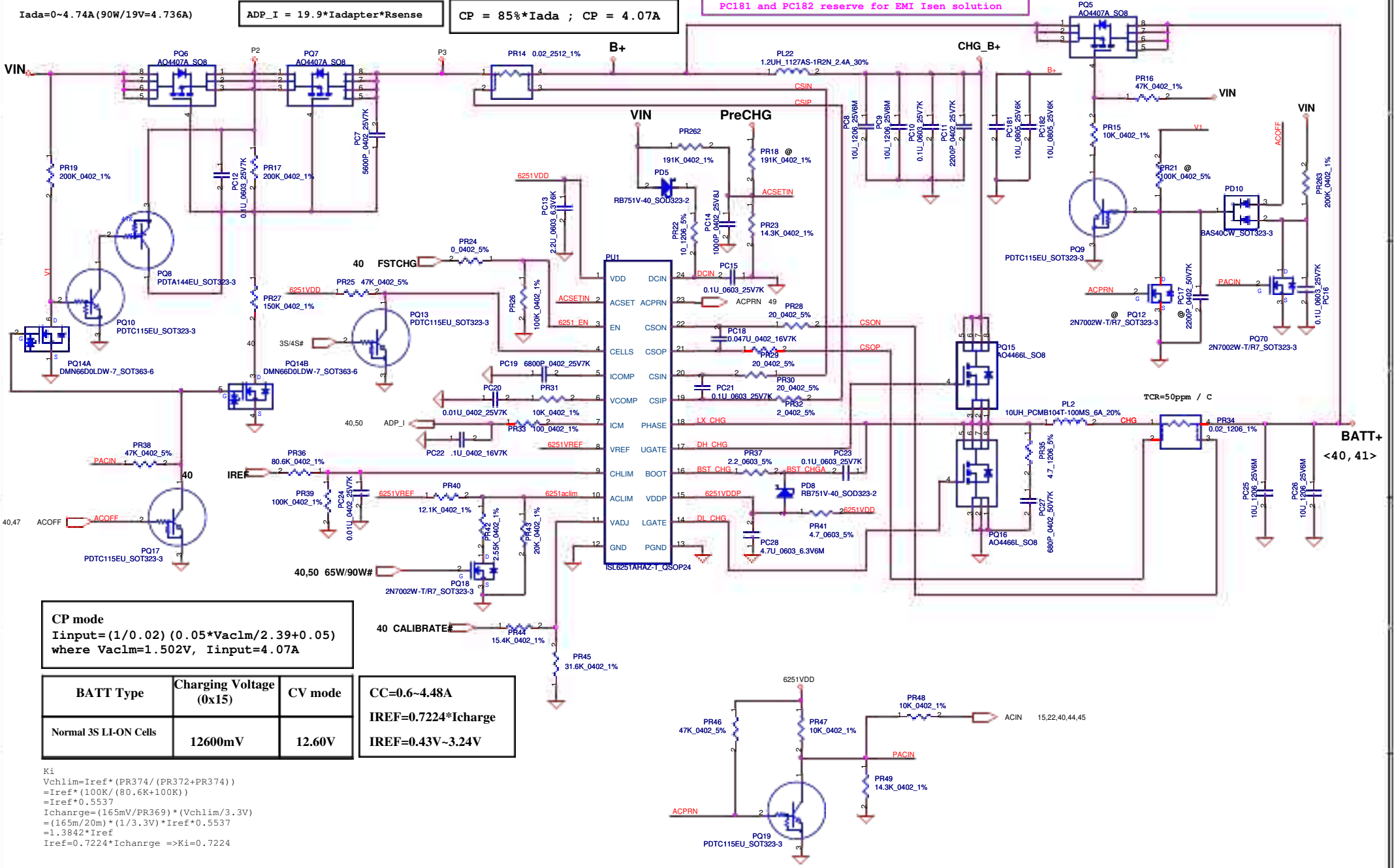
Date: Friday, November 05, 2010 | Sheet 47 of 61

Iada=0~4.74A(90W/19V=4.736A)

ADP_I = 19.9*Iadapter*Rsense

CP = 85%*Iada ; CP = 4.07A

PC181 and PC182 reserve for EMI Isen solution



CP mode

Iinput=(1/0.02)(0.05*Vaclm/2.39+0.05)
where Vaclm=1.502V, Iinput=4.07A

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

CC=0.6~4.48A

IREF=0.7224*Icharge

IREF=0.43V~3.24V

Ki
Vchlim=Iref*(PR374/(PR372+PR374))
=Iref*(100K/(80.6K+100K))
=Iref*0.5537
Ichanrge=(165mV/PR369)*(Vchlim/3.3V)
=(165m/20m)*(1/3.3V)*Iref*0.5537
=1.3842*Iref
Iref=0.7224*Ichanrge =>Ki=0.7224

Kv
Rinternal ic=514K Rec=3K R1=PR379=15.4K R2=PR381=31.6K
R=514K//31.6K//(15.4K+3k)=11.372K
r=514K//514K//31.6K=28.14K
Vcell=0.175*Vadj+3.99v
4.2V=0.175*Vadj+3.99V =>Vadj=1.2V
Vadj=Vref*(R/(R+514K))+CALIBRATE*(r/(r=514K))
1.1483=CALIBRATE*0.6046 =>CALIBRATE=1.899
1.899=(4.2-(Vcell+A*0.175))*Kv=(4.2-(4.2+A*0.175))*Kv
A=Vref*(R/(R+514K))=0.052
Kv=9.451

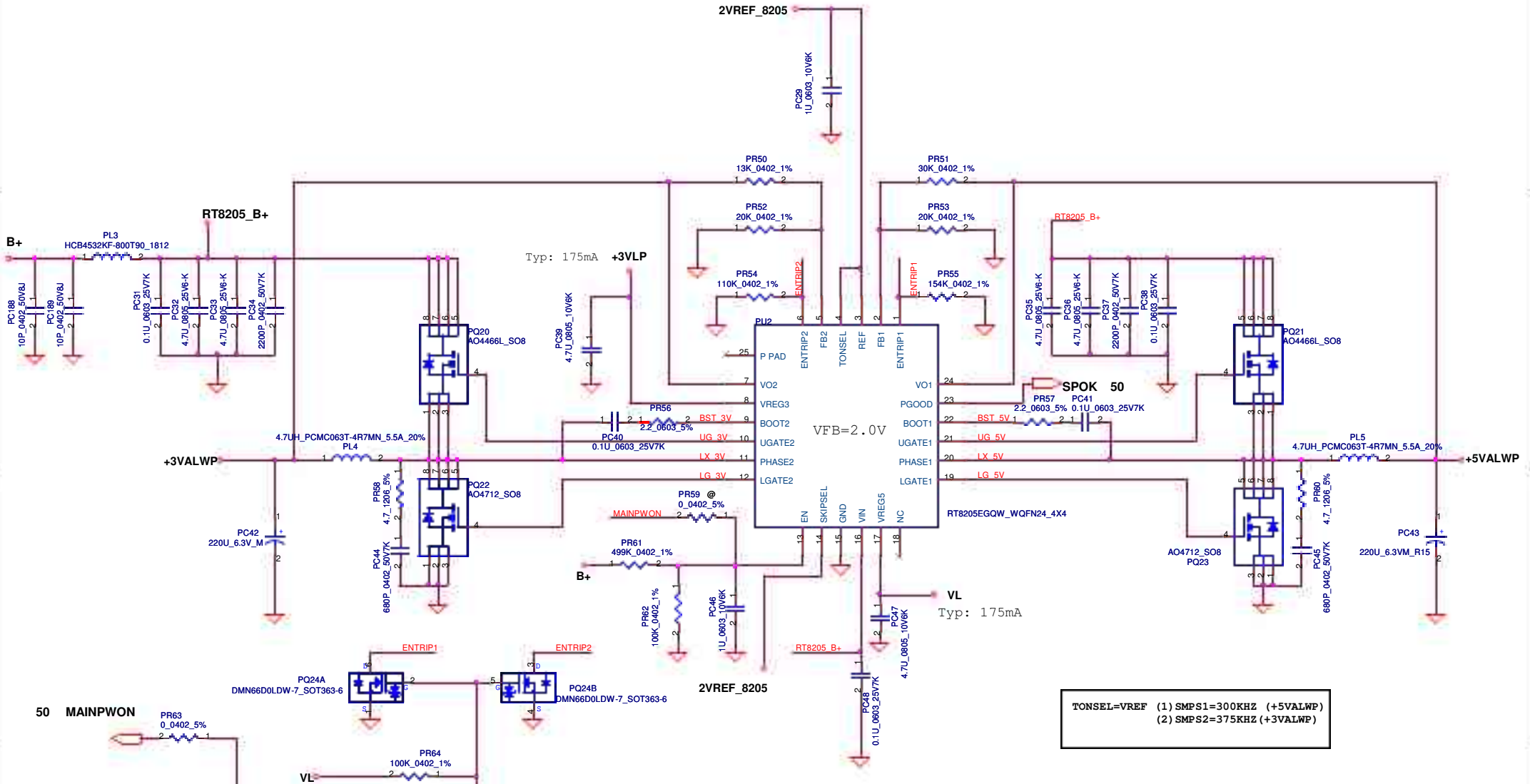
Security Classification	Compal Secret Data		
Issued Date	2010/11/1	Deciphered Date	2011/11/1

Compal Electronics, Inc.

Title: PWR-CHARGER

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: 0.5

Date: Friday, November 05, 2010 | Sheet 48 of 61



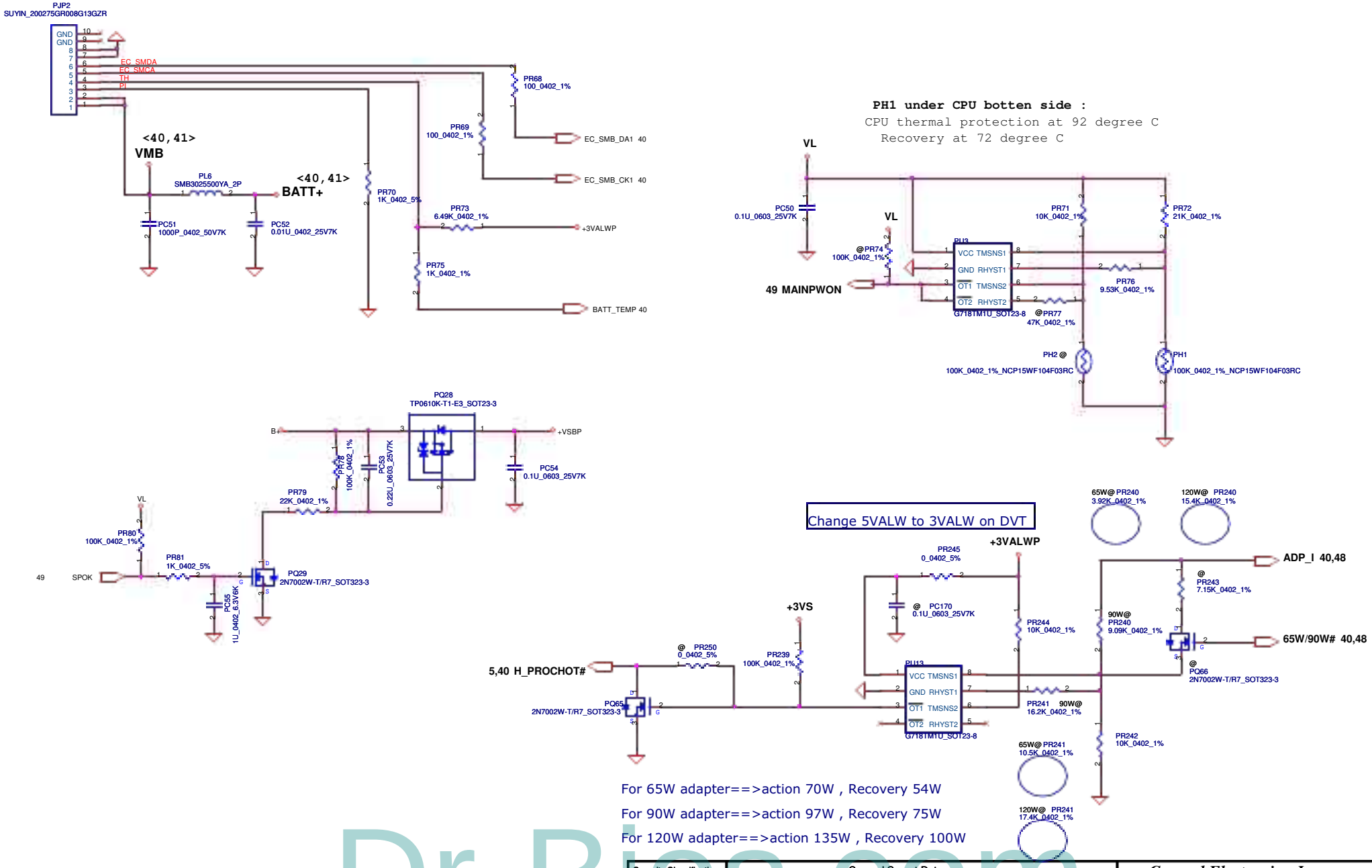
Security Classification	Compal Secret Data		
Issued Date	2010/11/1	Deciphered Date	2011/11/1

Compal Electronics, Inc.

Title: 3VALWP/5VALWP

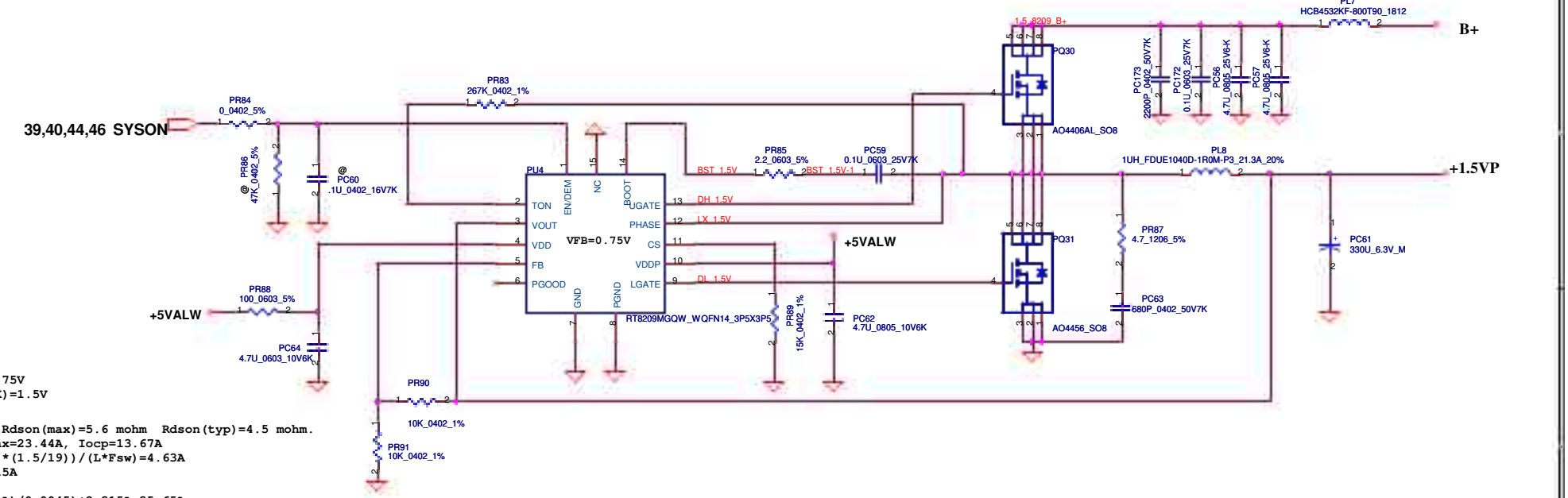
Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: 0.5

Date: Friday, November 05, 2010 | Sheet 49 of 61



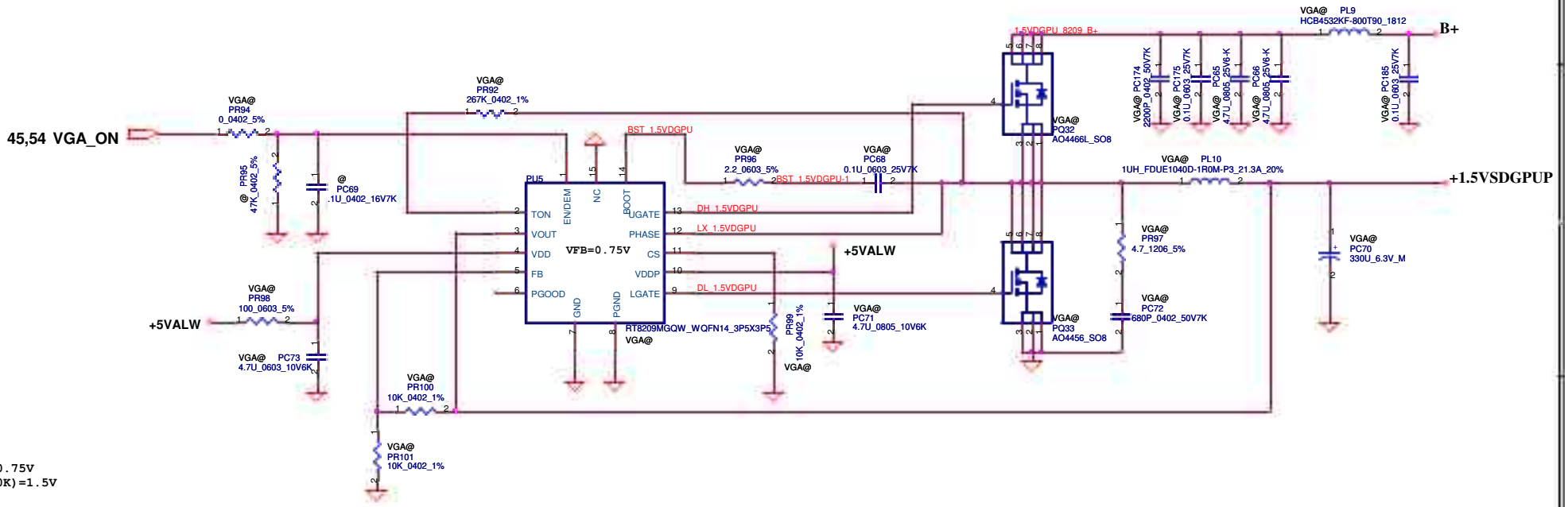
Security Classification	Compal Secret Data		
Issued Date	2010/11/1	Deciphered Date	2011/11/1

Compal Electronics, Inc.	
Title	PWR-BATTERY CONN/OTP
Size: Custom	Document Number: JE50-HR/SJV50-HR M/B Schematic
Rev	0.5
Date: Friday, November 05, 2010	Sheet 50 of 61



<Vo=1.5V> VFB=0.75V
V=0.75*(1+10K/10K)=1.5V
Fsw=298KHz

Cout ESR=15m ohm Rdson(max)=5.6 mohm Rdson(typ)=4.5 mohm.
Ipeak=19.53A, Imax=23.44A, Iocp=13.67A
Delta I=((19-1.5)*(1.5/19))/(L*Fsw)=4.63A
=>1/2Delta I=2.315A
choose Rcs=15K
Iocpmax=((15K*11uA)/0.0045)+2.315A=35.65A
Iocpmin=((15K*9uA)/(0.0056*1.3))+2.315A=23.06A
Iocp=23.06A~35.65A

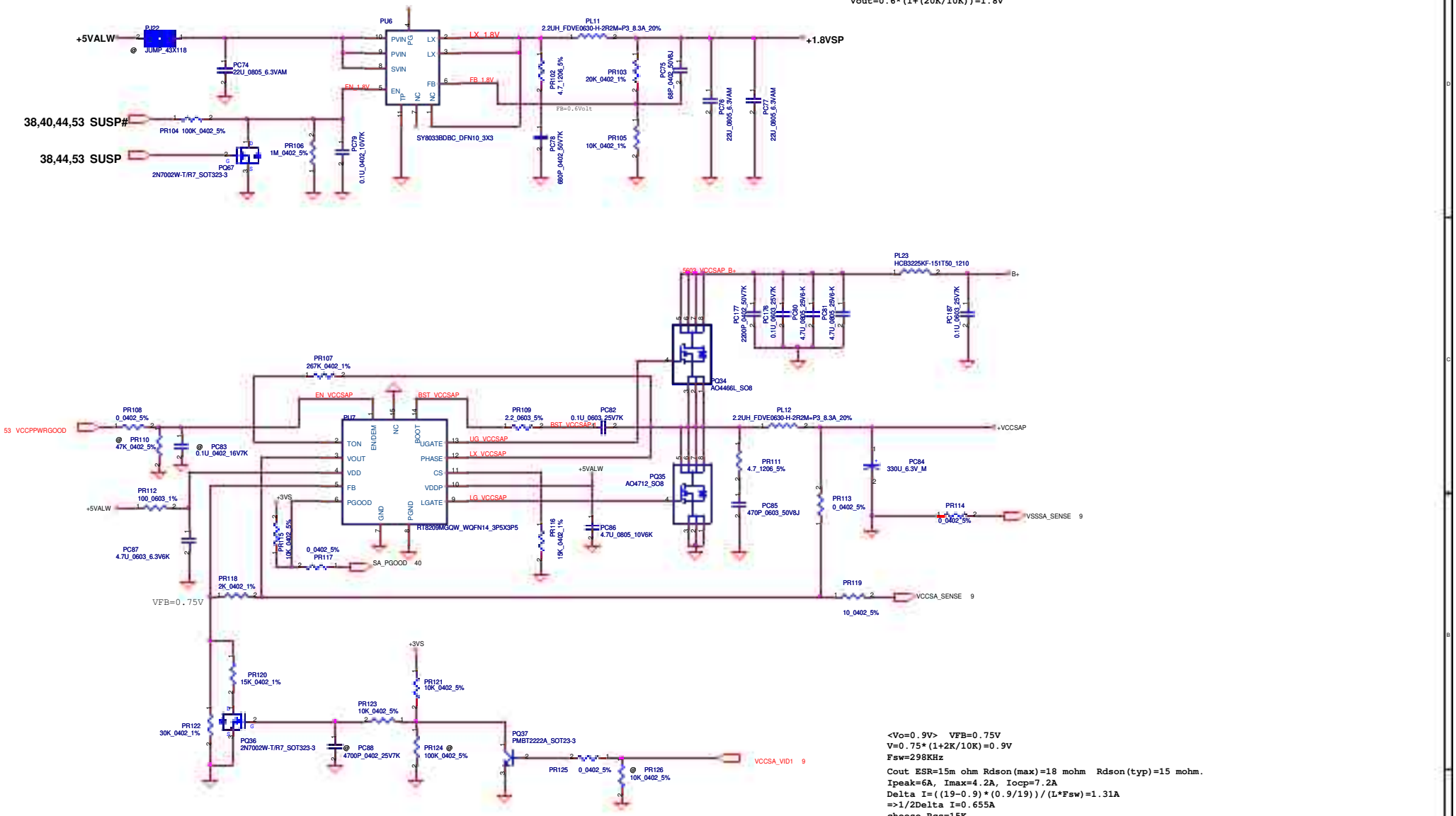


<Vo=1.5V> VFB=0.75V
V=0.75*(1+10K/10K)=1.5V
Fsw=298KHz

Cout ESR=15m ohm Rdson(max)=5.6 mohm Rdson(typ)=4.5 mohm.
Ipeak=10.4A, Imax=12.48A, Iocp=7.28A
Delta I=((19-1.5)*(1.5/19))/(L*Fsw)=4.63A
=>1/2Delta I=2.315A
choose Rcs=10K
Iocpmax=((10K*11uA)/0.0045)+2.315A=24.59A
Iocpmin=((10K*9uA)/(0.0056*1.3))+2.315A=15.95A
Iocp=15.95A~24.59A

Security Classification	Compal Secret Data		
Issued Date	2010/11/1	Deciphered Date	2011/11/1

Compal Electronics, Inc.			
Title	PWR-+1.5VP/+1.5VSDGPU		
Size: Custom	Document Number: JE50-HR/SJV50-HR M/B Schematics		Rev: 0.5
Date: Friday, November 05, 2010	Sheet 51 of 61		



VID[0]	VID[1]	VCCSA Vout	Require on 2011/ 2012 Required
0	0	0.9 V	Yes/Yes
0	1	0.8 V	Yes/Yes
1	1	0.75V	No/Yes
1	1	0.65V	No/Yes

Note:Use VCCSA_SEL to switch High & Low Level for VID[1]
(ie. VCCSA_SEL) due to the VID[0] is don't care for this setting.

<Vo=0.9V> VFB=0.75V
V=0.75*(1+2K/10K)=0.9V
Fsw=298KHz

Cout ESR=15m ohm Rdson(max)=18 mohm Rdson(typ)=15 mohm.
Ipeak=6A, Imax=4.2A, Iocp=7.2A
Delta I=((19-0.9)*(0.9/19))/(L*Fsw)=1.31A
=>1/2Delta I=0.655A
choose Rcs=15K
Iocpmax=((15K*11uA)/0.015)+0.655A=11.48A
Iocpmin=((15K*9uA)/(0.018*1.2))+0.655A=7.27A
Iocp=7.27A~11.48A

Security Classification	Compal Secret Data		
Issued Date	2010/11/1	Deciphered Date	2011/11/1

Compal Electronics, Inc.			
Title	PWR +VCCSAP		
Size	Document Number		Rev
C	JE50-HR/SJV50-HR M/B Schematics		0.5
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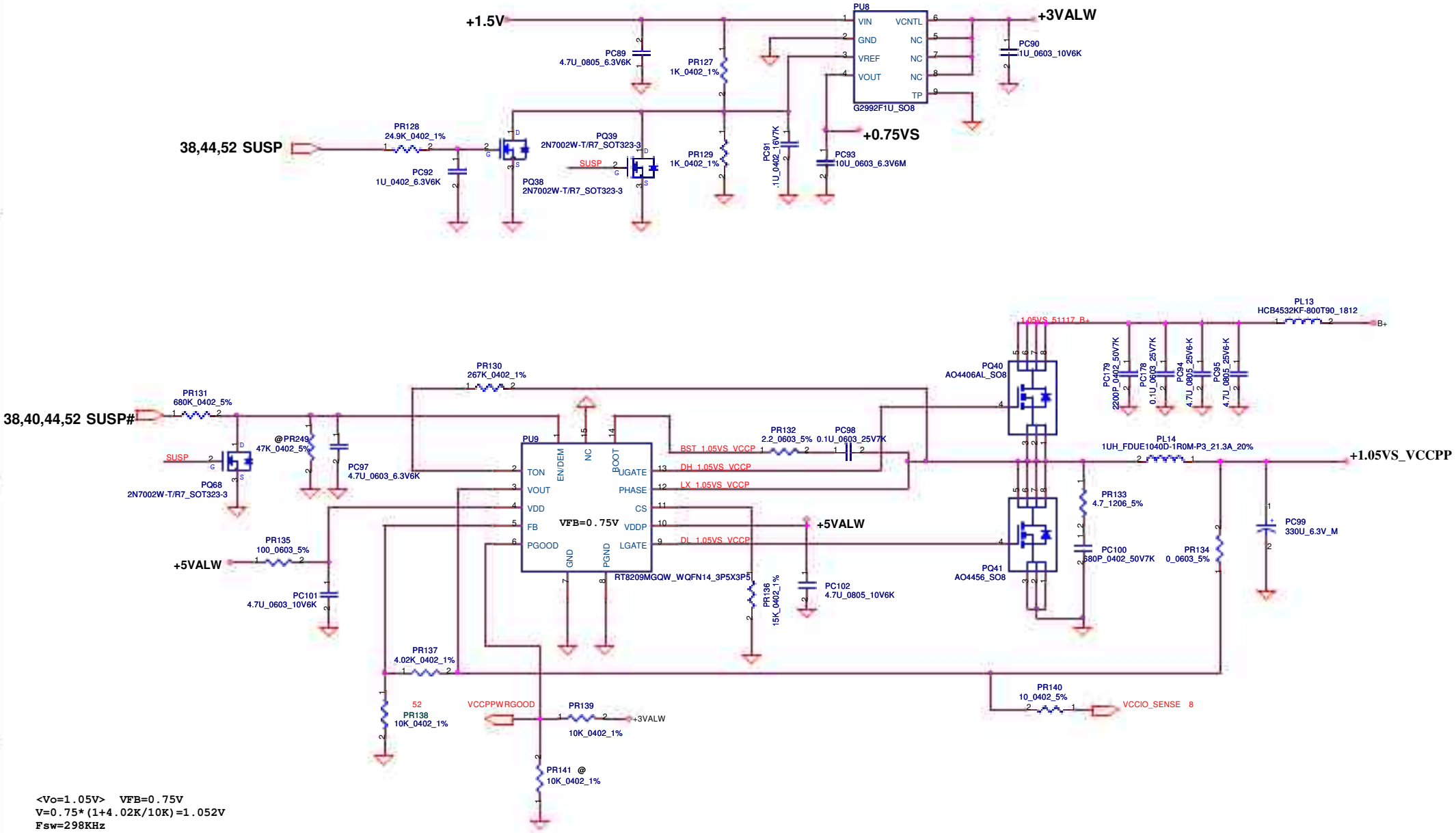
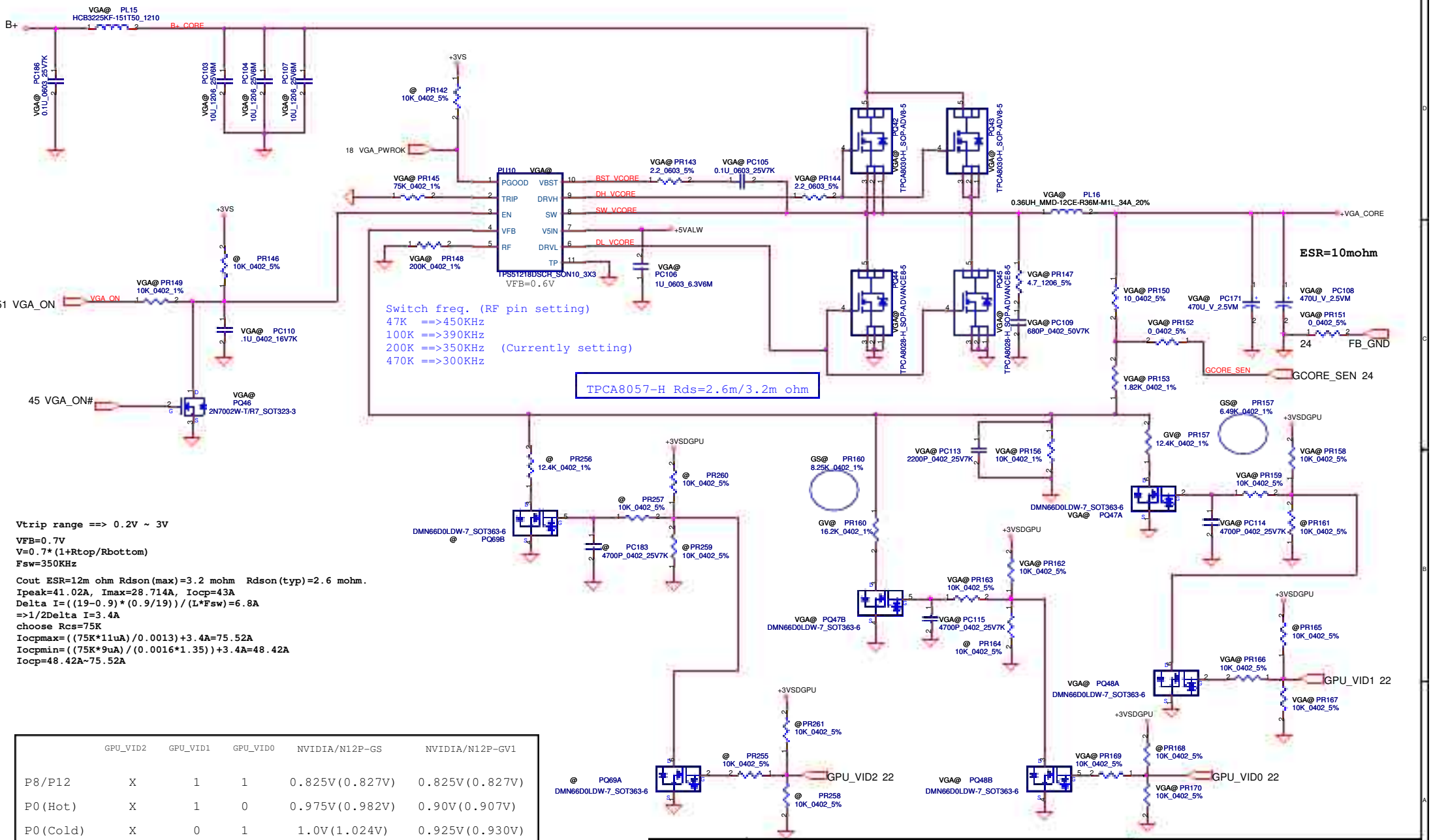


<Vo=1.05V> VFB=0.75V
V=0.75*(1+4.02K/10K)=1.052V
Fsw=298KHz

Cout ESR=15m ohm Rdson(max)=5.6 mohm Rdson(typ)=4.5 mohm.
Ipeak=12.866A, Imax=9A, Iocp=15.439A
Delta I=((19-1.05)*(1.05/19))/(L*Fsw)=3.33A
=>1/2Delta I=1.665A
choose Rcs=15K
Iocpmax=((15K*11uA)/0.0045)+1.665A=37.62A
Iocpmin=((15K*9uA)/(0.0056*1.3))+1.665A=23.02A
Iocp=23.02A~37.62A

Security Classification	Compal Secret Data		
Issued Date	2010/11/1	Deciphered Date	2011/11/1

Compal Electronics, Inc.			
Title	PWR +1.05VS_VCCPP/+0.75VSP		
Size	Custom	Document Number	JE50-HR/SJV50-HR M/B Schematics
Rev	0.5		
Date:	Friday, November 05, 2010	Sheet	53 of 61



	GPU_VID2	GPU_VID1	GPU_VID0	NVIDIA/N12P-GS	NVIDIA/N12P-GV1
P8/P12	X	1	1	0.825V(0.827V)	0.825V(0.827V)
P0(Hot)	X	1	0	0.975V(0.982V)	0.90V(0.907V)
P0(Cold)	X	0	1	1.0V(1.024V)	0.925V(0.930V)
	X	0	0	----	----

Security Classification	Compal Secret Data		
Issued Date	2010/11/1	Deciphered Date	2011/11/1

Compal Electronics, Inc.

Title: +VGA_COREP

Size: Custom | Document Number: P5WE0 | Rev: 0.5

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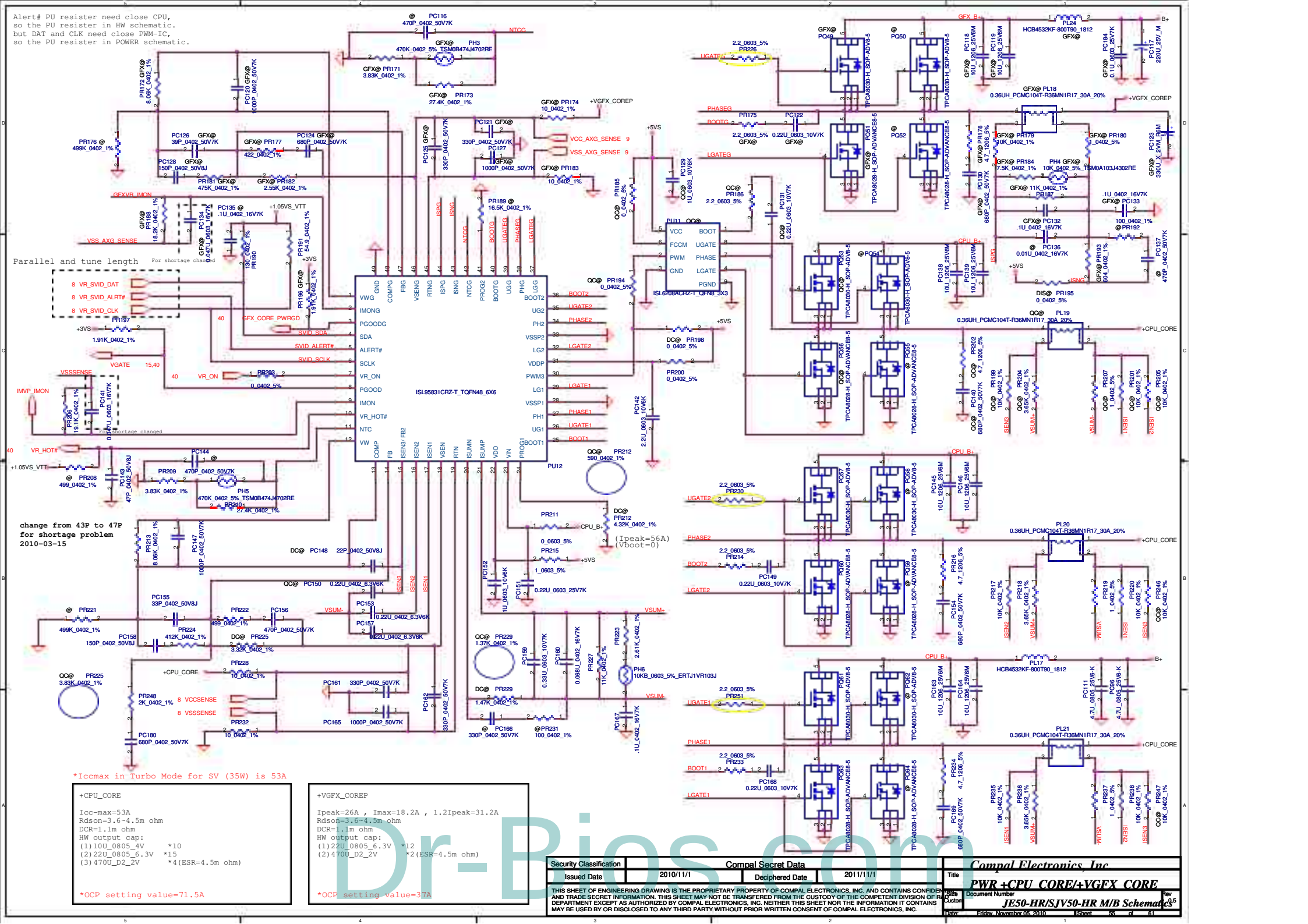
Alert# PU resister need close CPU,
so the PU resister in HW schematic.
but DAT and CLK need close PWM-IC,
so the PU resister in POWER schematic.
Parallel and tune length
change from 43P to 47P
for shortage problem
2010-03-15
ISL95831CRZ-T_TQFN48_6X6
PU12
ISL6208ACRZ-T_QFN8_3X3
PU11
*Iccmax in Turbo Mode for SV (35W) is 53A
+CPU_CORE
Icc-max=53A
Rdson=3.6~4.5m ohm
DCR=1.1m ohm
HW output cap:
(1)10U_0805_4V *10
(2)22U_0805_6.3V *15
(3)470U_D2_2V *4(ESR=4.5m ohm)
*OCP setting value=71.5A
+VGFX_COREP
Ipeak=26A , Imax=18.2A , 1.2Ipeak=31.2A
Rdson=3.6~4.5m ohm
DCR=1.1m ohm
HW output cap:
(1)22U_0805_6.3V *12
(2)470U_D2_2V *2(ESR=4.5m ohm)
*OCP setting value=37A
Security Classification
Compal Secret Data
Issued Date
2010/11/1
Deciphered Date
2011/11/1
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Compal Electronics, Inc
Title
PWR +CPU_CORE/+VGFX_CORE
Size
Custom
Document Number
JE50-HR/SJV50-HR M/B Schematics
Rev
0.5
Date: Friday, November 05, 2010
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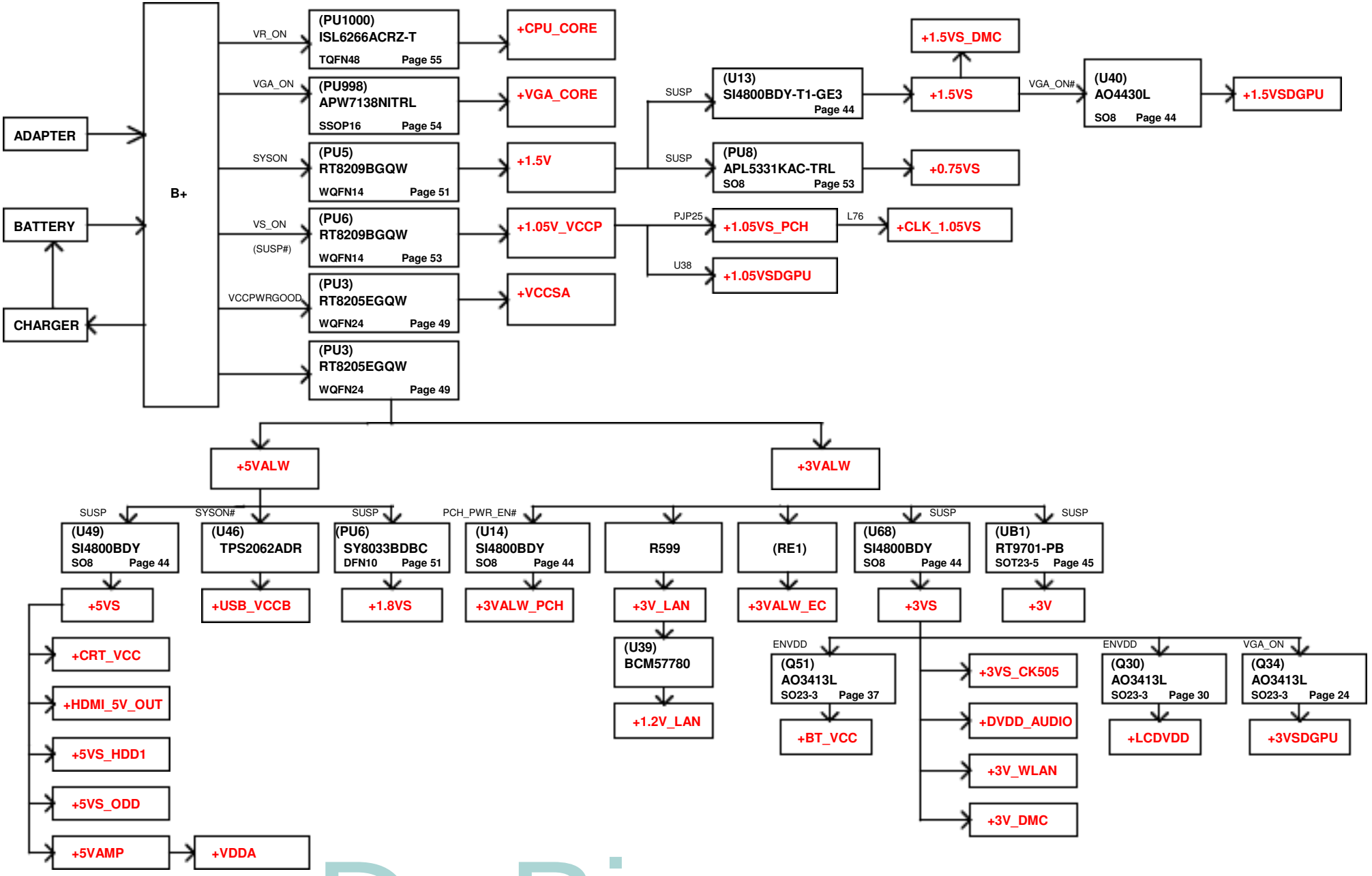
Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Add snubber R=4.7 ohm and C 680 pF	EMI solution	0.2	---	Add SD001470B80 for PR35,PR58,PR60,PR87,PR111, PR133,PR202,PR216,PR234 Add SE074681K80 for PC27,PC44,PC45,PC63,PC85, PC100,PC140,PC154,PC169	2010/10/20	DVT_P5WE0
2	Change boost R from 0 to 2.2 ohm	EMI solution	0.2	---	Change R to SD013220B80 forPR37,PR56,PR57,PR85, PR109,PR132,PR186,PR214,PR233	2010/10/20	DVT_P5WE0
3	Change PL11 and PL12 from SH00000F800 to SH00000M700	Cost saving	0.2	52	Change PL11 and PL12 from SH00000F800 to SH00000M700	2010/10/20	DVT_P5WE0
4	Change PL18,PL19,PL20,PL21 from SH000005680 to SH00000HK00	Change DCR tolerance to 5%	0.2	55	Change PL18,PL19,PL20,PL21 from SH000005680 to SH00000HK00	2010/10/20	DVT_P5WE0
5	CPU CORE transient compensation	CPU CORE transient compensation	0.2	55	Add PR248, PC160, PC180	2010/10/20	DVT_P5WE0
6							
7							
8							
9							
10							
11							
12							
13							
14							
15							

Security Classification	Compal Secret Data		
Issued Date	2010/11/1	Deciphered Date	2011/11/1

Compal Electronics, Inc.			
Title	PIR (PWR)		
Size: Custom	Document Number: JE50-HR/SJV50-HR M/B Schematics		Rev: 0.5
Date: Friday, November 05, 2010	Sheet 56 of 61		



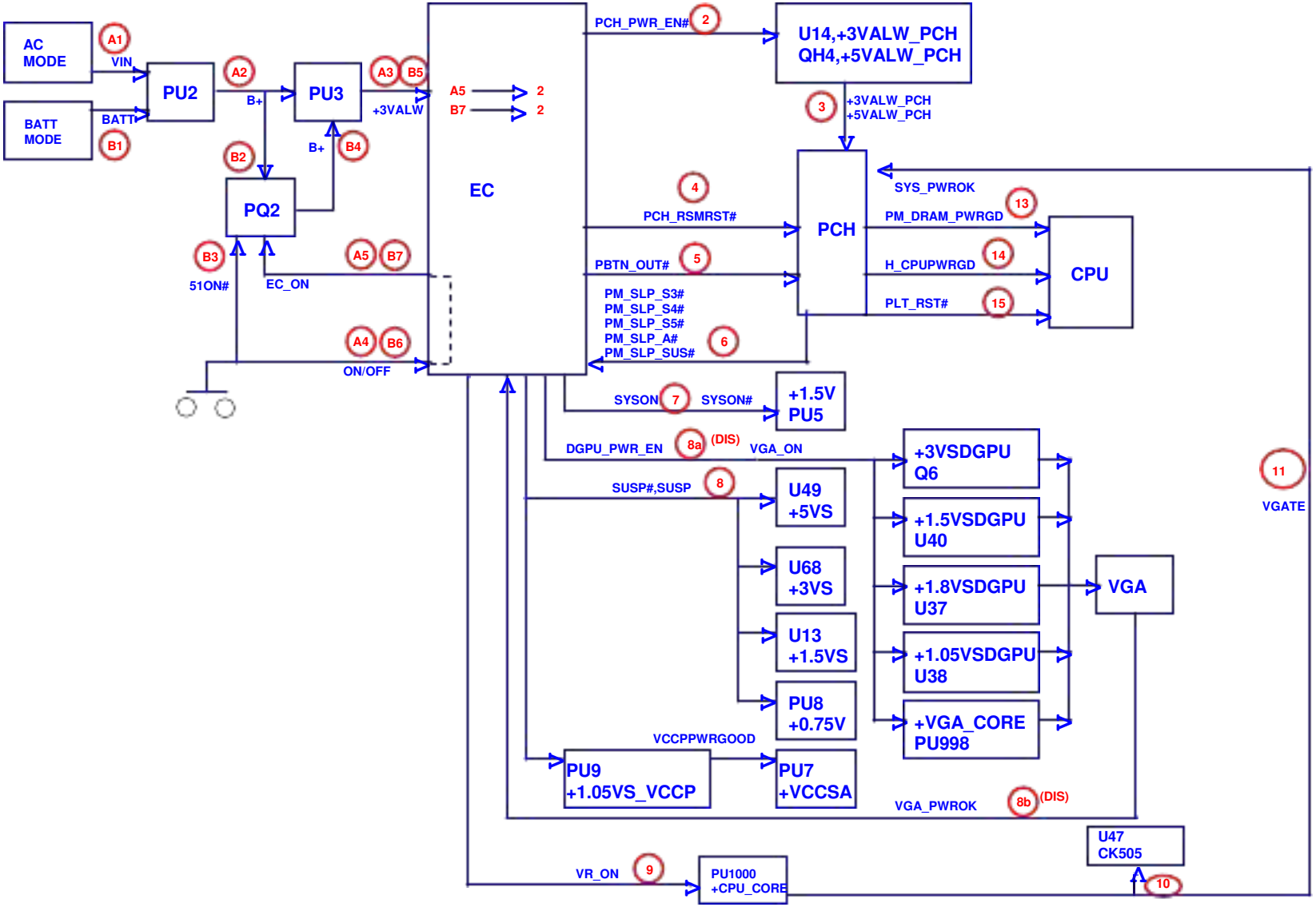
Security Classification	Compal Secret Data		
Issued Date	2010/11/1	Deciphered Date	2011/11/1

Compal Electronics, Inc.

Title: Power Rail

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: 0.5

Date: Friday, November 05, 2010 | Sheet 57 of 61



Security Classification	Compal Secret Data		
Issued Date	2010/11/1	Deciphered Date	2011/11/1

Compal Electronics, Inc.

Title: Power sequence

Size	Document Number	Rev
Custom	JE50-HR/SJV50-HR M/B Schematics	0.5

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	P.18	PCH_GPIO71	09/01	SW	For identofy VRAM 900 or 800 MHz		0.2
2	P.31	DPST buffer	09/03	HW	Change U1 from NOT gate to Buffer		0.2
3	P.39	EC_MUTE# pull high	09/03	HW	Change EC_MUTE# Pull high from +3VALW to +3VS		0.2
4	P.40	TP Conn. Reverse	09/03	HW	TP Mudule change,so reverse TP pin		0.2
5	P.13	R624 pop @	09/03	HW	Already pull high R655~		0.2
6	P.45	Change Cap from 0.1u to 0.01u	09/03	HW	C696,C368,C717,C718,C695,C366,C697, C401,C370,C369,C715 change to 0.01U Follow Vendor Suggest ..		0.2
7	P.35	Change 0 Ohm to 47 Ohm	09/04	Broadcom	R199,R207,R211,R215,R168,R171,R179, R182,R195,R216,R192 change to 47 Ohm Follow Vendor Suggest ..		0.2
8	P.5		09/17	HW	CPU XDP socket take off		0.2
9	P.40		09/17	HW	TP pin reverse		0.2
10	P.13		09/17	HW	R624 change to 4.7K		0.2
11	P.45		09/17	HW	OCI2B(R313) place @ for BOM		0.2
12	P.33		09/17	HW	HDMI output from PCH (by UMA)		0.2
13	P.35		09/17	HW	switch the LAN MIDI0 and MIDI2 pin		0.2
14	P.17,35 ,37,38, 39,45		09/17	HW	Change IO port PLT_RST# to PLT_RST_BUF#		0.2
15	P.18		09/17	HW	OPTIMUS_EN# pull high, pull low resistor value both change to 10K		0.2
16	P.24		09/20	HW	modify the VRAM strap pin ROM_SI pull low resistor for implement VRAM 900MHz		0.3
17	P.33		09/23	HW	Add R784 and R785 for DDC pull high...		0.3
18	P.44		09/23	HW	Add C818 and C819 for coupling noise from other spare trace...		0.3
19	P.45		09/23	HW	Add R786,R787,R788 and R789 pull down from vendor's suggestion..		0.3
20	P.37		09/23	HW	Add C820,R790 and Q58 for 3G/B and change source voltage from +3VS to +3VALW..		0.3
21	P.45		09/23	HW	Add C821,C822,C823,C824 for +1.5V... and move the PJ26 & PJ27 between 1.5V to 1.5VSDGPUH		0.3
22	P.46		09/24	HW	Change JUSB5 to USB2.0 Conn. Add D34 as ESD Diode for USB3.0		0.3

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Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
23	P.41		09/24	HW	Add R791 pull down 22k Ohm to ground Vendor's request...		0.3
24	P.22		09/24	HW	Add D31 to connect to ACIN Vendor's request...		0.3
25	P.36		09/29	HW	Add JP1,JP2 and JP3 for [redacted] ESD protection		0.3
26	P.36		09/29	ME	Update the JREAD1 symbol		0.3
27	P.13		09/29	HW	Add R792 follow DG1.5		0.3
28	P.33		09/29	HW	Change HDMI termination R to 680 Ohm		0.3
29	P.44		09/29	HW	Add C825 fro +1.05VSDGPU		0.3
30	P.17,38 ,45		09/30	HW	Change the M/B to USB port to port 1 Sub/B to port 0 and port 2		0.3
31	P.5		10/04	HW	Add test point for TCK,TMS, TRST#,TDO,TDI		0.3
32	P.17,18		10/04	HW	WWAN_OFF# from GPIO51 to GPIO37 WL_OFF# from GPIO55 to GPIO49		0.3
33	P.17,45		10/04	HW	M/B USB port from port 2 change to port1		0.3
34	P.26		10/04	HW	C1 and C604 chaneg to 470uF		0.3
35	P.36		10/04	HW	Add C827 as DGND and RJ45_GND bridge		0.3
36	P.36		10/04	HW	Change R490,R491,R492 and R493 to 0603 package		0.3
37	P.35		10/04	HW	Chaneg R214 to 0603 package		0.3
38	P.35		10/04	HW	Chaneg R192,R195,R199,R207,R211 ,R215,R168,R171,R179,R182 to 0 Ohm		0.3
39	P.40		10/04	HW	follow broadcom suggestion,add R496		0.3
40	P.40		10/04	HW	Add keyboard cap for EMI		0.3
41	P.44		10/04	HW	Add C826 for +1.5VSDGPU		0.3
42	P.37		10/05	HW	Add RTS5138 circuit		0.4
43	P.13		10/12	HW	Add D35 ,R799 and C838 for changing the RTC to samll size... and can be charged!!		0.4
44	P.14		10/12	HW	Add CLK_SD_48M for Card Reader 5138		0.4
45	P.24		10/12	HW	Pop R129 follow NV suggestion		0.4
46	P.25		10/12	HW	Pop R82 and De-pop R92 follow NV suggestion		0.4
47	P.25		10/12	HW	Add R800 and R801 10K Ohm pull down follow NV suggestion		0.4
48	P.24		10/12	HW	Change R775,R777,R778 and R779 to GV@		0.4

Version Change List (P. I. R. List)

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