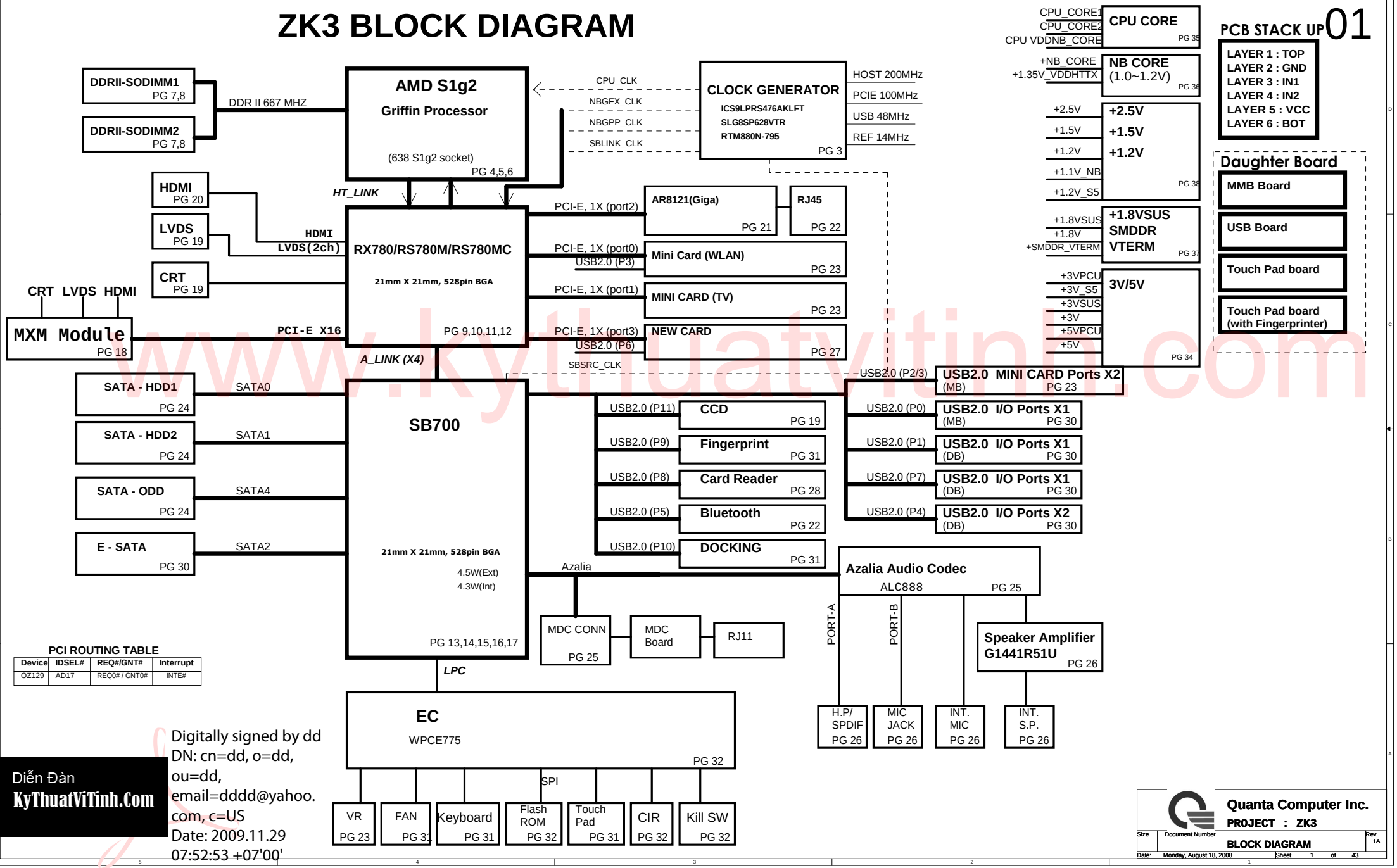
ZK3 BLOCK DIAGRAM



PCI ROUTING TABLE

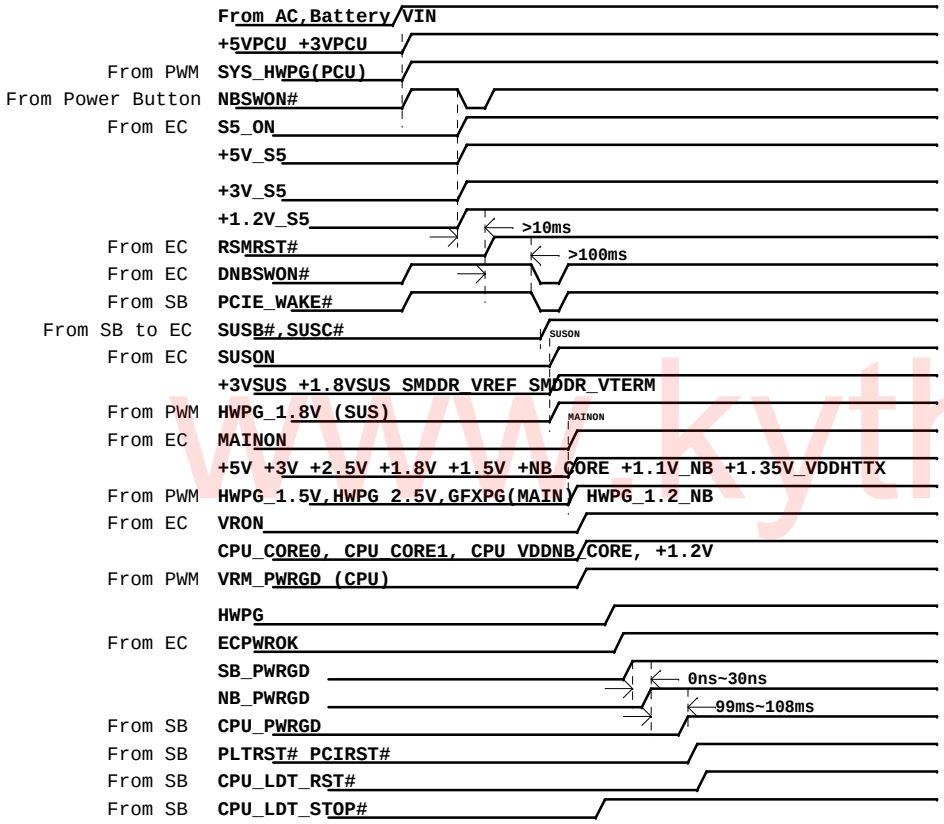
Device	IDSEL#	REQ#/GNT#	Interrupt
OZ129	AD17	REQ0# / GNT0#	INTE#

Quanta Computer Inc.
PROJECT : ZK3

Size	Document Number	Rev
	BLOCK DIAGRAM	1A

Date: Monday, August 18, 2008 Sheet 1 of 43

BD3G Power On Sequence



BOM naming rule

Items	Function	BTO	Name	Description
1	CIR	v	CIR@	
2	HDMI port	v	HDM@	
3	HDMI transmitter	v	SI@	Silicon image SiI 1392/1932
4	HDMI-CEC	v	CEC@	Renesas R8C/1B
5	Discrete VGA		EV@	External VGA stuff
6	UMA		IV@	Internal VGA stuff
7	New Card		NEW@	
8	RJ11	v	MD@	Modem
9	RJ45-10/100		40@	Marvell 8040T(10/100)
10	RJ45-1000		55@	Marvell 8055(Giga)
11	Option for RJ45-10/100 and RJ45-1000		40@55@	Option for 8040/8055
12	TV	v	TV@	
13	Cardbus		CB@	
14	FM transmitter	v	FM@	
15	Mainstream ID LED		MID@	
16	Low cost ID LED		LID@	
17	CCD	v	CCD@	
18	INT MIC	v	I_MIC@	
19	AMD Hyper Flash		HF@	Only for AMD platform
20	North bridge(690MC/RS780MC)		MC@	Only for AMD platform
21	North bridge(RX780)		RX@	Only for AMD platform
22	PowerXpress		PX@	Only for AMD platform
23	PowerXpress with UMA SKU		PX@IV@	Only for AMD platform
24	PowerXpress with Discrete VGA SKU		PX@EV@	Only for AMD platform
25	Power player/Power Shift		PP@	Only for AMD platform

***Note: EC will sampling SUSB# & SUSC# every 5ms.**

AMD SB700 SMBUS Table

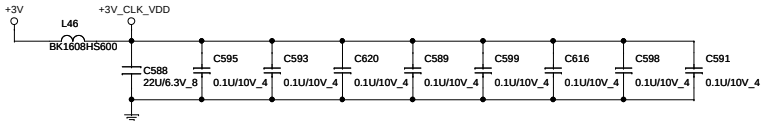
	CLK GEN	RAM	Mini Card (HD-Decoder)	Mini-card(WL)	New Card	HDMI
SB700 SDATA0/SCLK0(+3V)	V	V	V	V	V	
SB700 SDATA1/SCLK1(+3V_S5)						V
SB700 SDATA2/SCLK2(+3V_S5)						
Power	+3V	+3V	+3V	+3V (Atheros)	+3V	+3V_S5
Reserve MOS ckt	V	V	V	V	V	V

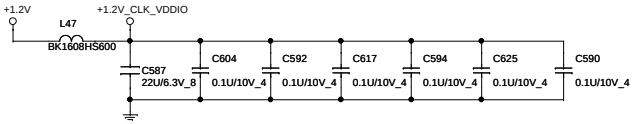
EC SMBUS Table

	Battery	CPU thermal Sensor	EC EEPROM	VGA thermal Sensor	Touch Sensor	HDMI CEC
EC775 SDATA1/SCLK1(+3VPCU)	V					
EC775 SDATA2/SCLK2(+3VPCU)		V	V			
EC775 SDATA3/SCLK3(+3VPCU)				V	V	V
EC775 SDATA4/SCLK4(+3VPCU)						
Power	+3VPCU	+3V	+3VPCU	+3V	+3VPCU	+5VPCU
Reserve MOS ckt	X	V	X	V	X	V

Quanta Computer Inc.
PROJECT : ZK3
Size | Document Number | SYSTEM INFORMATION | Rev 1A
Date: Monday, August 18, 2008 | Sheet 2 of 43

CLK_GEN_SLG8SP628





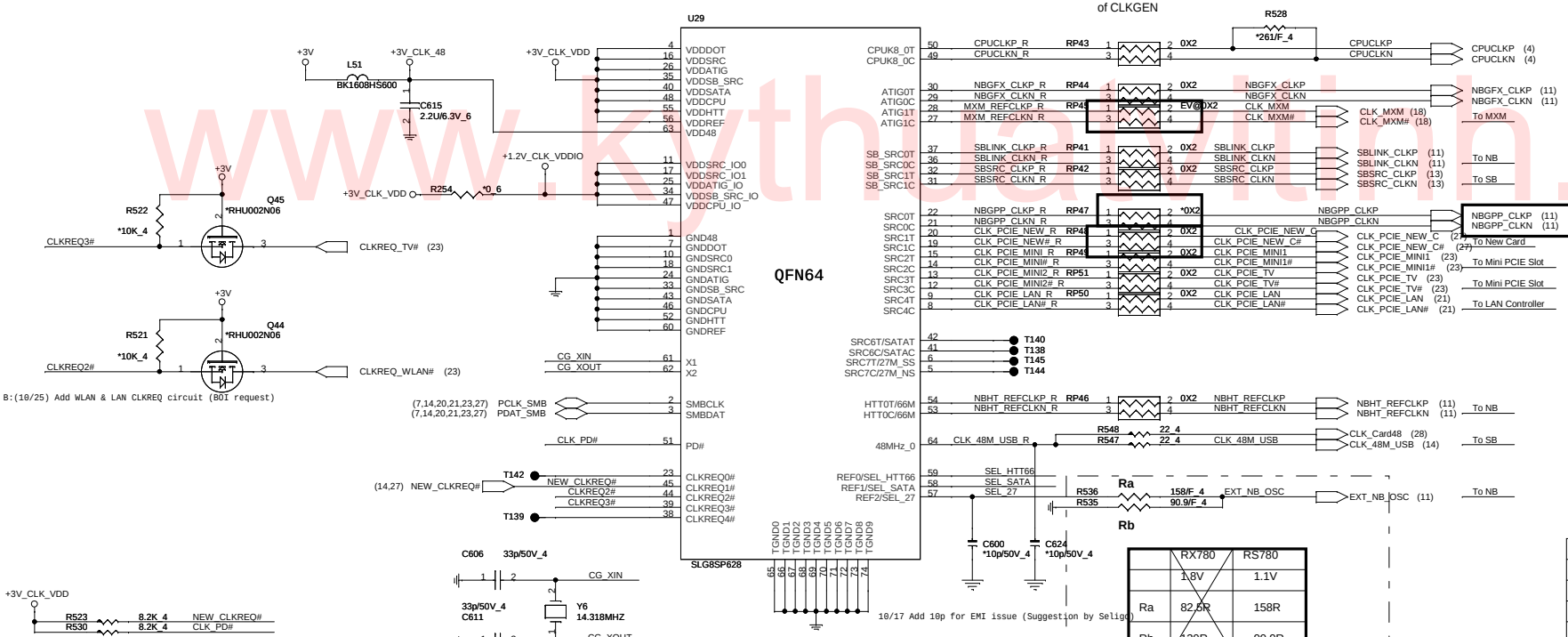
ICS9LPRS480 P/N :

SLG8SP628 P/N : AL8SP628000

RTM880N-796 P/N : AL000880000

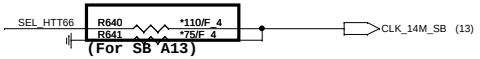
Clock chip has internal serial terminations for differencial pairs, external resistors are reserved for debug purpose.

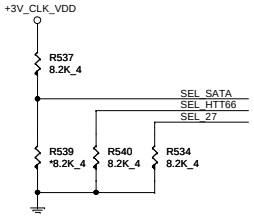
Place within 0.5" of CLKGEN



	RX780	RS780
	1.8V	1.1V
Ra	82.5R	158R
Rb	130R	90.9R

RES CHIP 130 1/16W +-1%(0402)L-F -->CS11302FB15
RES CHIP 158 1/16W +-1%(0402) -->CS11582FB00
RES CHIP 90.9 1/16W +-1%(0402) -->CS09092FB15
RES CHIP 82.5 1/16W +-1%(0402) -->CS08252FB11





SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1*	100 MHz non-spreading differential SRC clock
	0	100 MHz spreading differential SRC clock
SEL_27	1	27MHz and 27M SS outputs
	0*	100 MHz SRC clock

* default

NB CLOCK INPUT TABLE

NB CLOCKS	RX780	RS780
HT_REFCLKP	100M DIFF	100M DIFF
HT_REFCLKN	100M DIFF	100M DIFF
REFCLK_P	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF

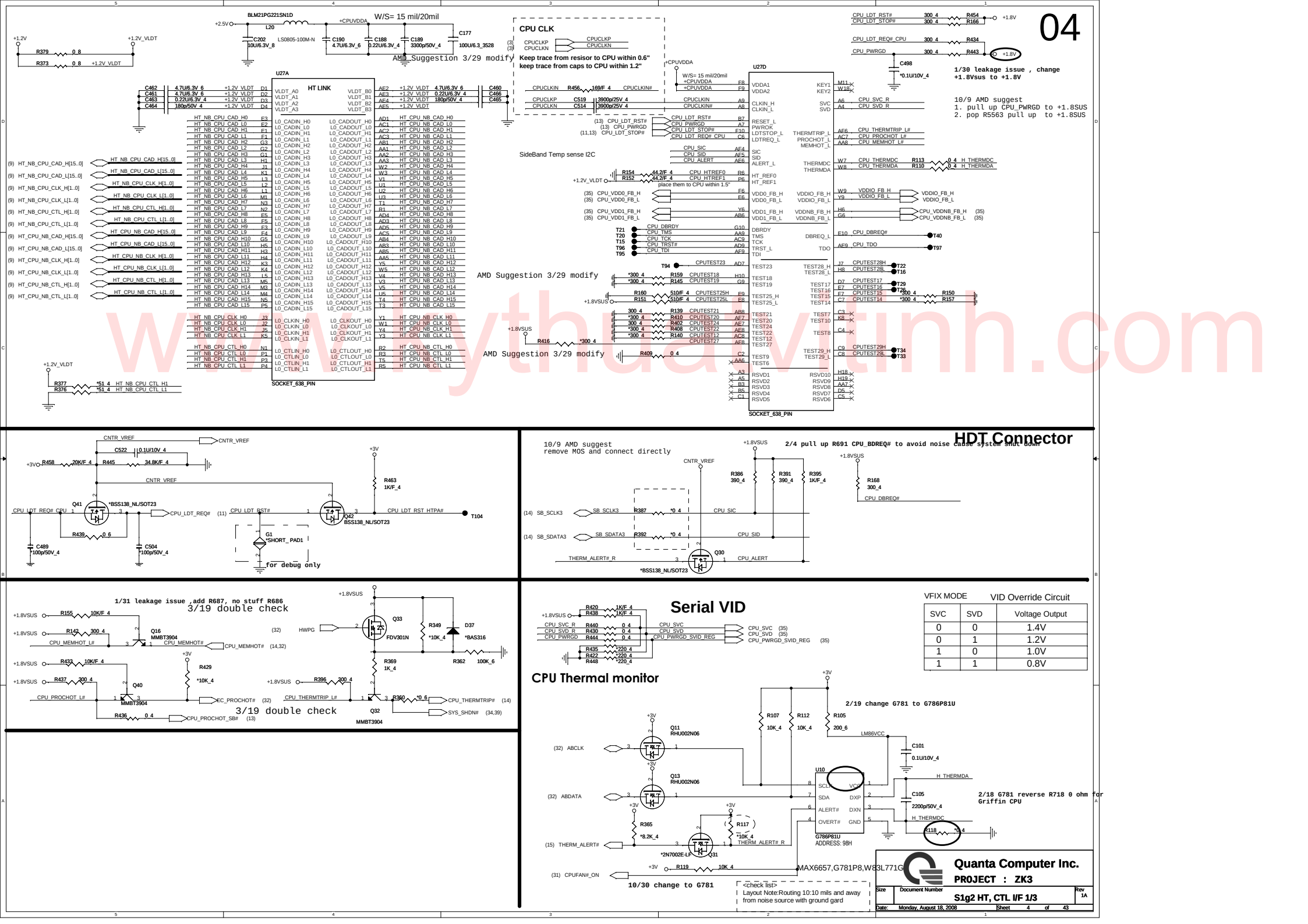
CLOCKS name	RX780	RS780	Clock pin function
NBGFX_CLKP NBGFX_CLKN	RP1001 STUFF	RP1001 STUFF	to NB for VGA reference clock
MXM_REFCLKP MXM_REFCLKN	RP66 STUFF	RP66 NC	to M82-S external reference clock -RX780 only
NBGPP_CLKP NBGPP_CLKN	RP1005 STUFF	RP1005 NC	to NB for RX780 for PCIEX2 interface reference clock only RS780 is internal share with AC-LINK clock,RS780 not need
SBLINK_CLKP SBLINK_CLKN	RP1003 STUFF	RP1003 STUFF	to NB for AC-LINK reference clock

Quanta Computer Inc.

PROJECT : ZK3

Size	Document Number	Rev
	CLOCK GENERATOR_SLG8SP628	1A

Date: Monday, August 18, 2008 Sheet 3 of 43



Processor Memory Interface

05

PLACE THEM CLOSE TO CPU WITHIN 1"

U27B

MEM:CMD/CTRL/CLK

+SMDDR_VTERM

750 mA

+1.8VSUS

+SMDDR_VREF

R192 2K/F_4

R173 Reserved *0_4

R179 2K/F_4

C218 0.1U/10V_4

C210 1000p/50V_4

R431 39.2/F_4 M_ZP

R432 39.2/F_4 M_ZN

SOCKET_638_PIN

U27C

MEM:DATA

Place close to socket

C534 4.7U/6.3V_6

C499 4.7U/6.3V_6

C507 4.7U/6.3V_6

C533 4.7U/6.3V_6

C200 0.22U/6.3V_4

C530 0.22U/6.3V_4

C511 0.22U/6.3V_4

C199 0.22U/6.3V_4

C520 1000p/50V_4

C201 1000p/50V_4

C529 1000p/50V_4

C176 1000p/50V_4

C185 180p/50V_4

C171 180p/50V_4

C517 180p/50V_4

C528 180p/50V_4

Close to CPU within 1500 mils

C544 1.5p/50V_4

C545 1.5p/50V_4

C532 1.5p/50V_4

C557 1.5p/50V_4

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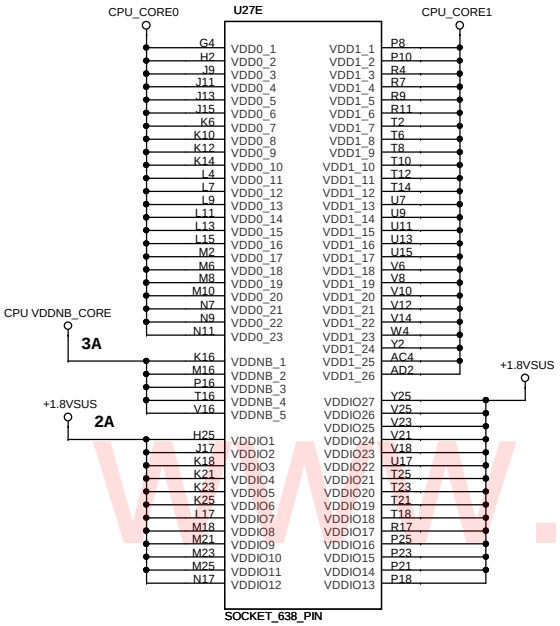
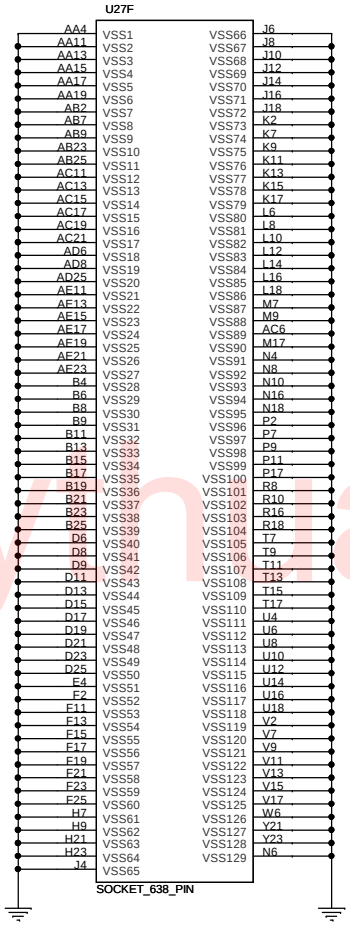
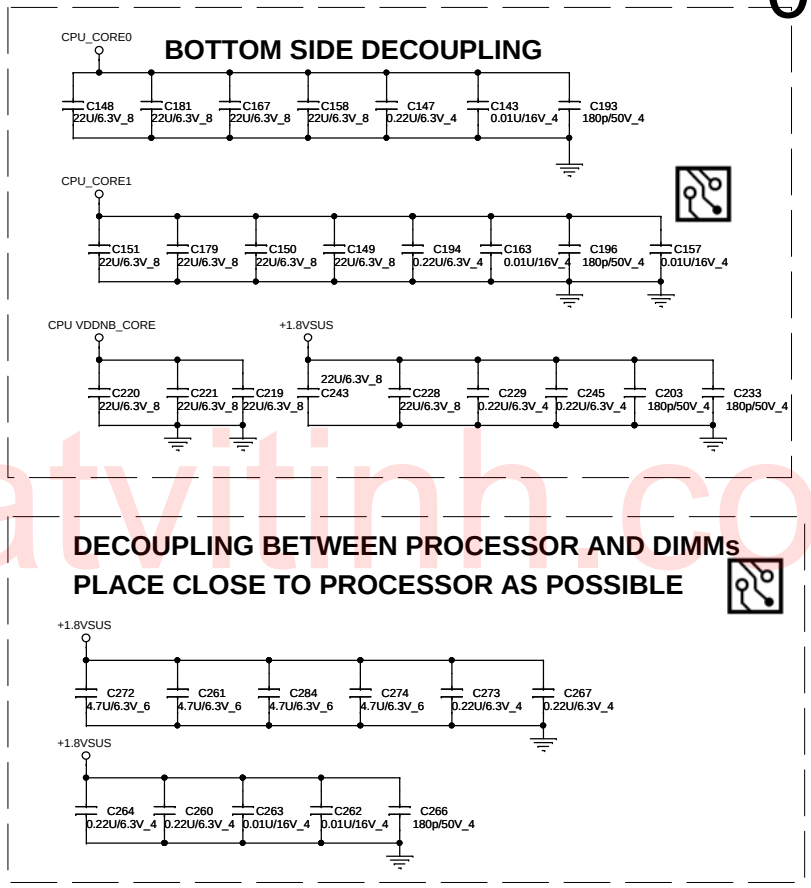
PROJECT : ZK3

Size	Document Number	Rev
	S1G2 DDRII MEMORY I/F 2/3	1A
Date: Monday, August 18, 2008	Sheet 5 of 43	

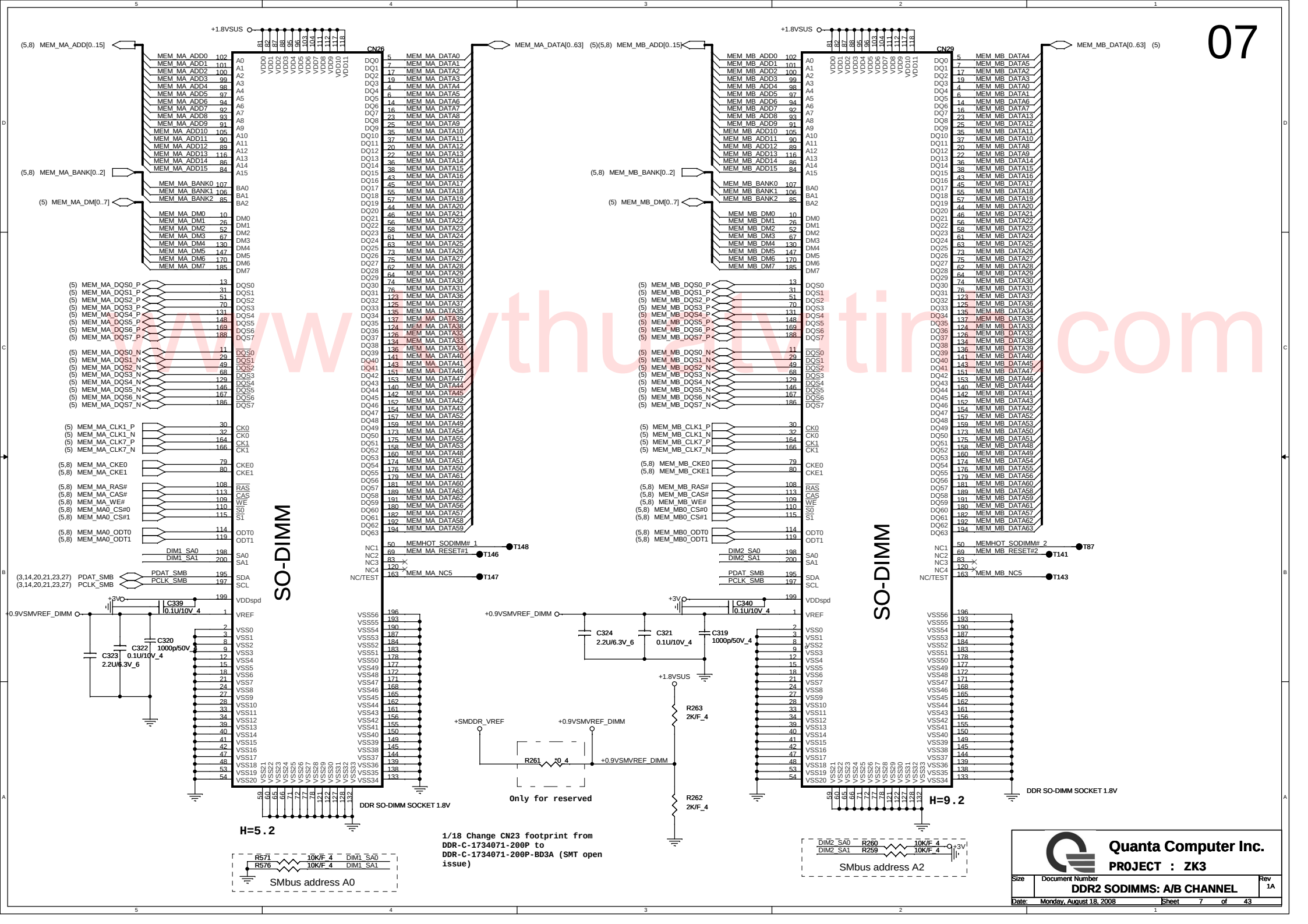




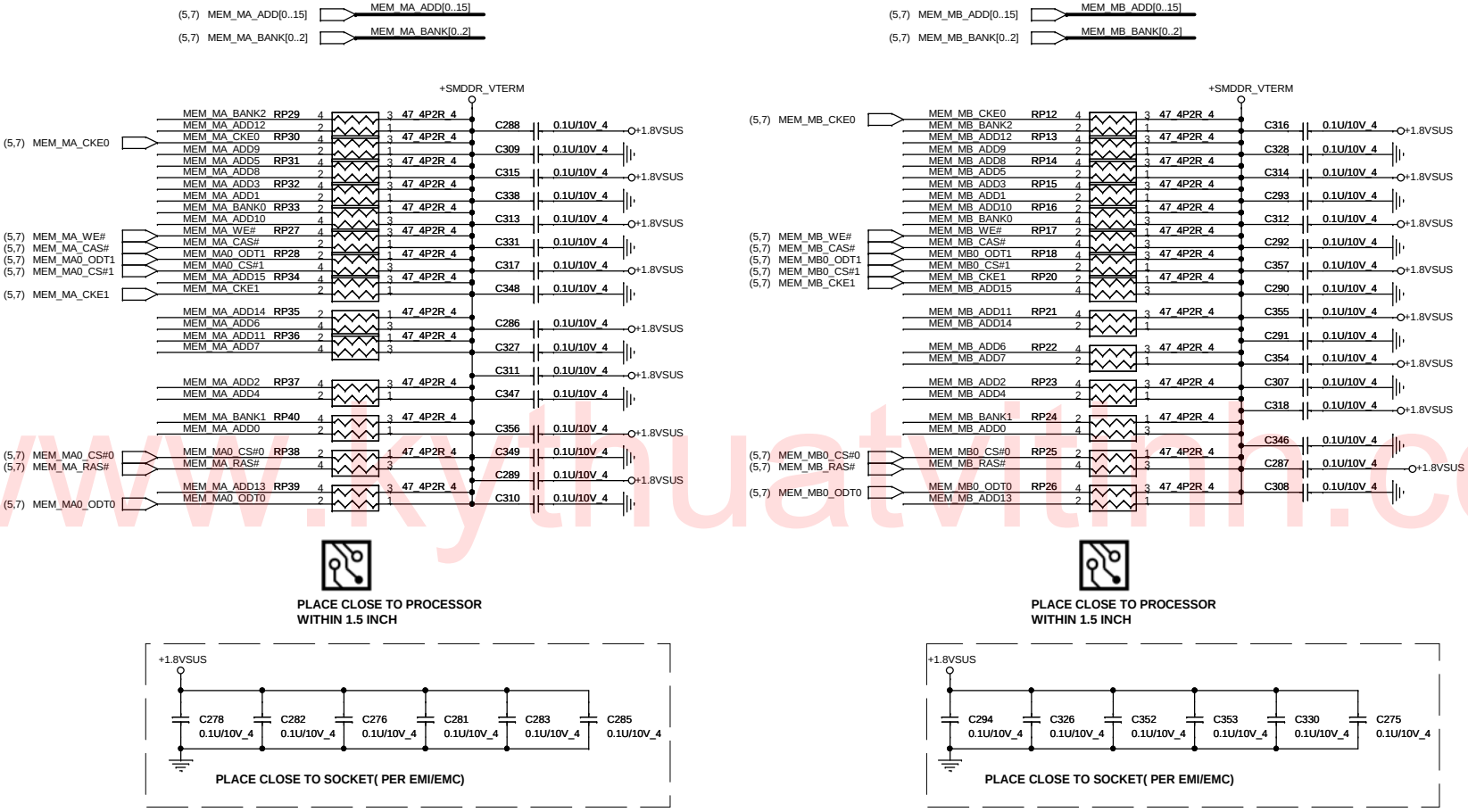


PROCESSOR POWER AND GROUND

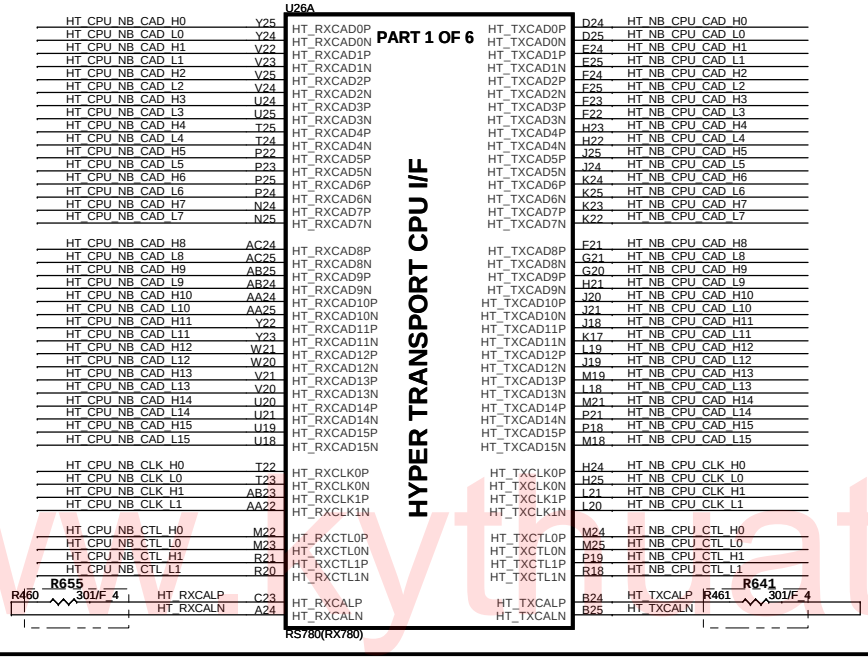
Quanta Computer Inc.		
PROJECT : ZK3		
Size	Document Number: S1G2 PWR & GND 3/3	Rev: 1A
Date: Monday, August 18, 2008	Sheet 6 of 43	



Quanta Computer Inc.		
PROJECT : ZK3		
Size	Document Number: DDR2 SODIMMS: A/B CHANNEL	Rev: 1A
Date: Monday, August 18, 2008	Sheet 7 of 43	



Quanta Computer Inc.		
PROJECT : ZK3		
Size	Document Number: DDR2 SODIMMS TERMINATIONS	Rev: 1A
Date: Monday, August 18, 2008	Sheet 8 of 43	



HT_CPU_NB_CAD_H[15..0] → HT_CPU_NB_CAD_H[15..0] (4)
HT_CPU_NB_CAD_L[15..0] → HT_CPU_NB_CAD_L[15..0] (4)
HT_CPU_NB_CLK_H[1..0] → HT_CPU_NB_CLK_H[1..0] (4)
HT_CPU_NB_CLK_L[1..0] → HT_CPU_NB_CLK_L[1..0] (4)
HT_CPU_NB_CTL_H[1..0] → HT_CPU_NB_CTL_H[1..0] (4)
HT_CPU_NB_CTL_L[1..0] → HT_CPU_NB_CTL_L[1..0] (4)
HT_NB_CPU_CAD_H[15..0] → HT_NB_CPU_CAD_H[15..0] (4)
HT_NB_CPU_CAD_L[15..0] → HT_NB_CPU_CAD_L[15..0] (4)
HT_NB_CPU_CLK_H[1..0] → HT_NB_CPU_CLK_H[1..0] (4)
HT_NB_CPU_CLK_L[1..0] → HT_NB_CPU_CLK_L[1..0] (4)
HT_NB_CPU_CTL_H[1..0] → HT_NB_CPU_CTL_H[1..0] (4)
HT_NB_CPU_CTL_L[1..0] → HT_NB_CPU_CTL_L[1..0] (4)

11/4 modify

signals	RS780	RX780
HT_TXCALP HT_TXCALN	R641 300 ohm 1%	R641 1.21k ohm 1%
HT_RXCALP HT_RXCALN	R655 300 ohm 1%	R655 1.21k ohm 1%

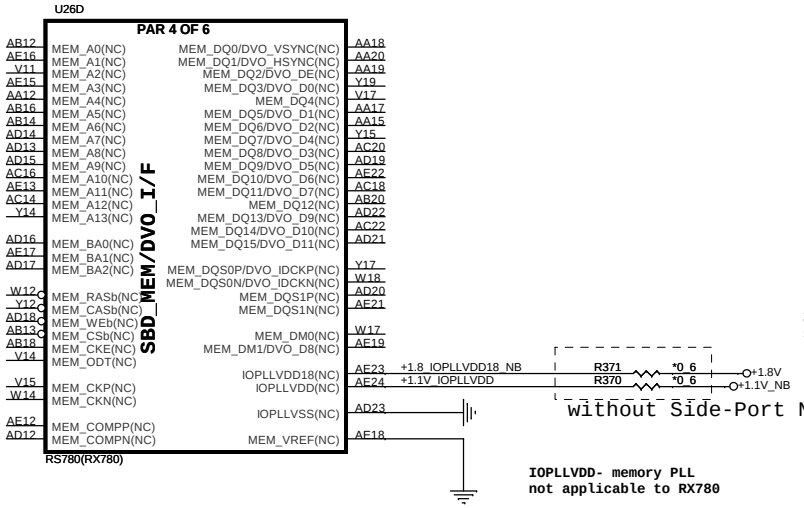
RES CHIP 1.21K 1/16W +-1%(0402)
P/N : CS21212FB18

RES CHIP 300 1/16W +-1%(0402)
P/N : CS13002FB00

A12 version
RS780M AJ067400T05 100-CK2612(216-0674008-00)
RS780MC AJ067400T06 100-CK2613(216-0674010-00)
RX781 AJ067400T10 100-CK2642(215-0674024)
SB700 AJA12FG0T18 100-CK2614(218S7EALA12FG)

A13 version
RS780M AJ067400T18 100-CK2699(216-0674022)
RS780MC AJ067400T20 100-CK2704(216-0674024)
RX781 AJ067400T21 100-CK2706(215-0674034)
A12 version
SB700 AJA12FG0T18

This block is for UMA RS780 only , RX780 can remove all component



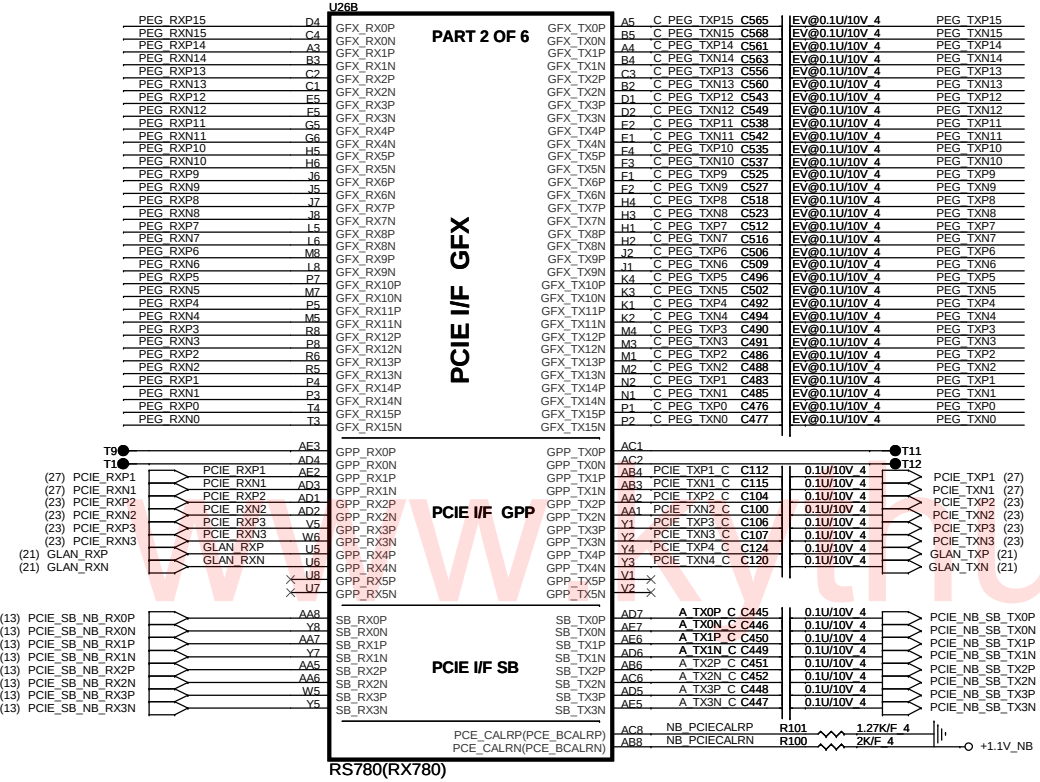
2/1 R480,R479 no stuff when RS780M without side port / RX781

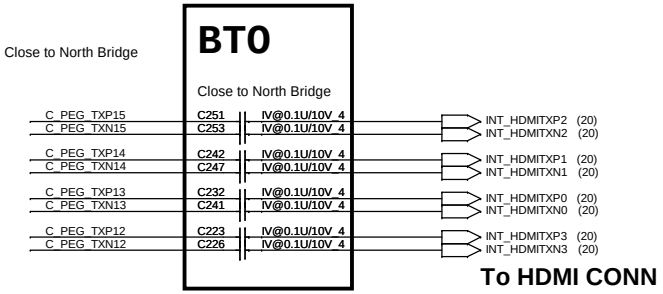
without Side-Port NU 4/8

IOPLLVDD- memory PLL not applicable to RX780

Quanta Computer Inc.
PROJECT : ZK3

Size	Document Number	Rev
	RS740/RS780-HT LINK I/F 1/5	1A
Date: Monday, August 18, 2008	Sheet 9 of 43	





TO EPRESS CARD
TO WLAN
TO MINI CARD
TO PCIE-LAN

NOTE:
RS780MC no support Graphic / HDMI

11/4 modify

RX780/RS740/RS780 difference table (PCIE LINK)

	RS740	RX780/RS780
NB_PCIECALRP	2.2R (GND)	1.27K (GND)
GPP4	NC	GPP4
GPP5	NC	GPP5

RS780 Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

Quanta Computer Inc.
PROJECT : ZK3

Size	Document Number	Rev
	RS740/RS780-PCIE I/F 2/5	1A

Date: Monday, August 18, 2008 Sheet 10 of 43

RX780: Powered from the 1.8-V rail and driven by SB600 LDT_RST#, or SB700 LDT_RST# or A_RST#.
RS780: Powered from the 3.3-V rail and driven by SB600 LDT_RST#, or SB700 LDT_RST# or A_RST#.

RS780
(13) NB_PLTRST# → NB_PLTRST#
North Bridge RESET

RX780
+1.1V_NB — R177 *2.2K_4 — INT_CRT_DDCDAT
R178 *2.2K_4 — INT_CRT_DDCCLK
10/9 add 2K pull up to DDCDAT /DDCCLK for RX780

11/4 no stuff for RS780M/MC/RX781

12/22 stuff R48 2.2K for power play

STRP_DATA — R191 *10K/F_4 — +3V
R196 2.2K_4

selects Loading of straps from EPROM
1 : use default vaule , default
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected
RX780 --RS780_AUX_CAL
RS780 -- SUS_ATAT

RX780
RS780_AUX_CAL — R468 *3K_4

Enables Debug Bus acess through memory T/O pads and GPIO.
1 : Enable RX780 , Default
0 : Disable RX780

RX780
Reserved only

Enables Debug Bus acess through memory T/O pads and GPIO.
1 : Enable RS780 , Default
0 : Disable RS780
(RS780 use VSYNC#)

RS780
INT_VSYNC — R462 3K_4 — +3V
R465 *3K_4

Indicates if memory Side port is available or not
0: available RS780 , Default
1: Not available RS780
(RS780 use HSYNC#)

RS780
INT_HSYNC — R464 3K_4 — +3V
R467 *3K_4

10/19 RS780M Databook rev 1.01 define High disable

U26C — PART 3 OF 6

CRT/TVOUT
- AVDD1(NC) F12
- AVDD2(NC) E12
- AVDDI(NC) F14
- AVSSDI(NC) G15
- AVDDQ(NC) H15
- AVSSQ(NC) H14
- C_Pr(DFT_GPIO5) F17
- Y(DFT_GPIO2) F17
- COMP_Pb(DFT_GPIO4) F15
- RED(DFT_GPIO0) G18
- REDb(NC) G17
- GREEN(DFT_GPIO1) E18
- GREENb(NC) F18
- BLUE(DFT_GPIO3) E19
- BLUEb(NC) F19
- DAC_HSYNC(PWM_GPIO4) A11
- DAC_VSYNC(PWM_GPIO6) B11
- DAC_SDA(PCE_TCALRN) E8
- DAC_SCL(PCE_RCALRN) F8
- DAC_RSET(PWM_GPIO1) G14

PLL PWR / LVTM
- PLLVDD(NC) A12
- PLLVDD18(NC) D14
- PLLVSS(NC) B12
- VDDA18HTPLL H17
- VDDA18PCIEPLL1 D7
- VDDA18PCIEPLL2 E7

PM
- SYSRESETb D8
- POWERGOOD A10
- LDTSTOPb C10
- ALLOW_LDTSTOP C12

CLOCKs
- HT_REFCLKP C25
- HT_REFCLKN C24
- REFCLK_P/OSCIN(OSCIN) E11
- REFCLK_N(PWM_GPIO3) F11
- GFX_REFCLKP T2
- GFX_REFCLKN T1
- GPP_REFCLKP U1
- GPP_REFCLKN U2
- GPPSB_REFCLKP(SB_REFCLKP) V4
- GPPSB_REFCLKN(SB_REFCLKN) V3

MIS.
- I2C_DATA A9
- I2C_CLK B9
- DDC_DATA/AUX0N(NC) B8
- DDC_CLK/AUX0P(NC) A8
- AUX1P(NC) B7
- AUX1N(NC) A7
- STRP_DATA B10
- RSVD G11
- AUX_CAL(NC) C8

RS780(RX780)

(18) INT_CRT_RED — R183 IV@140/F_4 — INT_CRT_RED
(18) INT_CRT_GRN — R181 IV@150/F_4 — INT_CRT_GRN
(18) INT_CRT_BLU — R182 IV@150/F_4 — INT_CRT_BLU
(18) INT_HSYNC — INT_HSYNC
(18) INT_VSYNC — INT_VSYNC
(18) INT_CRT_DDCDAT — INT_CRT_DDCDAT
(18) INT_CRT_DDCCLK — INT_CRT_DDCCLK
R163 IV@715/F_6 — DAC_RSET_NB
(17) NB_PWRGD_IN
(3) NBHT_REFCLKP
(3) NBHT_REFCLKN
(3) EXT_NB_OSC
+1.1V_NB — R184 4.7K_4 — R200 4.7K_4
(3) NBGFX_CLKP
(3) NBGFX_CLKN
(3) NBGPP_CLKP
(3) NBGPP_CLKN
(3) SBLINK_CLKP
(3) SBLINK_CLKN
(19) INT_LVDS_EDIDDATA
(19) INT_LVDS_EDIDCLK
(20) SDVO_CTRLDATA
(20) SDVO_CTRLCLK
T108 — T109 — RS740_DFT_GPIO1
(36) +NB_CORE_ON — R201 0_4 — STRP_DATA
T107 — RS780_AUX_CAL

+3V_AVDD_NB — +1.8V_AVDDDI_NB — +1.8V_AVDDQ_NB
+1.1V_PLLVDD — +1.8V_PLLVDD18 — +1.8V_VDDA18HTPLL — +1.8V_VDDA18PCIEPLL
NB_PLTRST# — NB_PWRGD_IN — NB_LDT_STOP# — NB_ALLOW_LDTSTOP
NBHT_REFCLKP — NBHT_REFCLKN
R210 0_4 — R194 0_4 — NB_REFCLK_P — NB_REFCLK_N
INT_LVDS_EDIDDATA — INT_LVDS_EDIDCLK — IV_HDMI_DDCDATA — IV_HDMI_DDCCLK

TXOUT_L0P(NC) A22 — INT_TXLOUT0+ (18)
TXOUT_L0N(NC) B22 — INT_TXLOUT0- (18)
TXOUT_L1P(NC) A21 — INT_TXLOUT1+ (18)
TXOUT_L1N(NC) B21 — INT_TXLOUT1- (18)
TXOUT_L2P(NC) B20 — INT_TXLOUT2+ (18)
TXOUT_L2N(DBG_GPIO0) A20 — INT_TXLOUT2- (18)
TXOUT_L3P(NC) A19 — T111
TXOUT_L3N(DBG_GPIO2) B19 — T106
TXOUT_U0P(NC) B18 — INT_TXUOUT0+ (18)
TXOUT_U0N(NC) A18 — INT_TXUOUT0- (18)
TXOUT_U1P(PCIE_RESET_GPIO3) A17 — INT_TXUOUT1+ (18)
TXOUT_U1N(PCIE_RESET_GPIO2) B17 — INT_TXUOUT1- (18)
TXOUT_U2P(NC) D20 — INT_TXUOUT2+ (18)
TXOUT_U2N(NC) D21 — INT_TXUOUT2- (18)
TXOUT_U3P(PCIE_RESET_GPIO5) D18 — T110
TXOUT_U3N(NC) D19 — T105
TXCLK_LP(DBG_GPIO1) B16 — INT_TXLCLKOUT+ (18)
TXCLK_LN(DBG_GPIO3) A16 — INT_TXLCLKOUT- (18)
TXCLK_UP(PCIE_RESET_GPIO4) D16 — INT_TXUCLKOUT+ (18)
TXCLK_UN(PCIE_RESET_GPIO1) D17 — INT_TXUCLKOUT- (18)
VDDLTP18(NC) A13 — +1.8V_VDDLTP18_NB — B13
VSSLTP18(NC)
VDDLT18_1(NC) A15 — +1.8V_VDDLT_18_NB — B15
VDDLT18_2(NC) A14 — +3V_VDLT33_NB — B14
VDDLT33_1(NC)
VDDLT33_2(NC)
VSSLT1(VSS) C14
VSSLT2(VSS) D15
VSSLT3(VSS) C16
VSSLT4(VSS) C18
VSSLT5(VSS) C20
VSSLT6(VSS) E20
VSSLT7(VSS) C22

11/01 exchange LVDS_PWM /LVDS_BLON
LVDS_DIGON(PCE_TCALRP) E9 — INT_LVDS_DIGON (19)
LVDS_BLON(PCE_RCALRP) F7 — L_BKLT_CTRL (19)
LVDS_ENA_BL(PWM_GPIO2) G12 — INT_LVDS_BLON (19)

TMDS_HPD(NC) D9 — TMDS_HPD0 — R205 IV@0_4 — TMDS_HPD# (20)
HPD(NC) D10 — TMDS_HPD1 — T39
TVCLKIN(PWM_GPIO5) D12 — SUS_STAT#_NB — R211 0_4 — SUS_STAT# (14)
THERMALDIODE_P AE8 — R_NB_THRMDA — T89
THERMALDIODE_N AD8 — R_NB_THRMDC — T90
TESTMODE D13 — TEST_EN — R203 1.82K/F_4
R252 *3K_4

1/17 RX781 connect to GND
C104,C110,C646,C98,C136,C103,C118 change to CS00003J951

+3V — L23 BLM18PG221SN1D — +3V_AVDD_NB — C172 10U/6.3V_6
AVDD-DAC Analog not applicable to RX780

+1.1V_NB — L22 BLM18PG221SN1D — +1.1V_PLLVDD — C192 2.2U/6.3V_6
PLLVDD - Graphics PLL not applicable to RX780

+1.8V — L27 BLM18PG221SN1D — +1.8V_PLLVDD18 — C236 10U/6.3V_8 — C175 22U/6.3V_8
PLLVDD18 - Graphics PLL not applicable to RX780

+1.8V — R197 0_6 — +1.8V_AVDDDI_NB — C162 2.2U/6.3V_6
AVDDI-DAC Digital not applicable to RX780

BLM18PG221SN1D — L29 — +1.8V_AVDDQ_NB — C246 2.2U/6.3V_6
AVDDQ-DAC Bandgap Reference not applicable to RX780

11/4 no stuff for RS780M/MC

+1.8V — BLM18PG221SN1D — L44 — +1.8V_VDDLTP18_NB — C173 2.2U/6.3V_6
VDDLTP18 - LVDS or DVI/HDMI PLL not applicable to RX780

BLM21PG221SN1D — L24 — +1.8V_VDDLT_18_NB — C215 4.7U/6.3V_6 — C207 0.1U/10V_4
VDDLT18 - LVDS or DVI/HDMI digital not applicable to RX780

1/17 RX781 no stuff them
L2,L12,C124,L52,R76,L17,L51,L10,C115

1/31 voltage leakage issue
remove Q5,Q3,R83,R80,R97
stuff R88,R77

+1.8V — L28 BLM18PG221SN1D — 20mils width — +1.8V_VDDA18PCIEPLL — C240 2.2U/6.3V_6
VDDA18PCIEPLL -PCIE PLL

L26 BLM18PG221SN1D — 20mils width — +1.8V_VDDA18HTPLL — C225 2.2U/6.3V_6
VDDA18HTPLL -HT LINK PLL

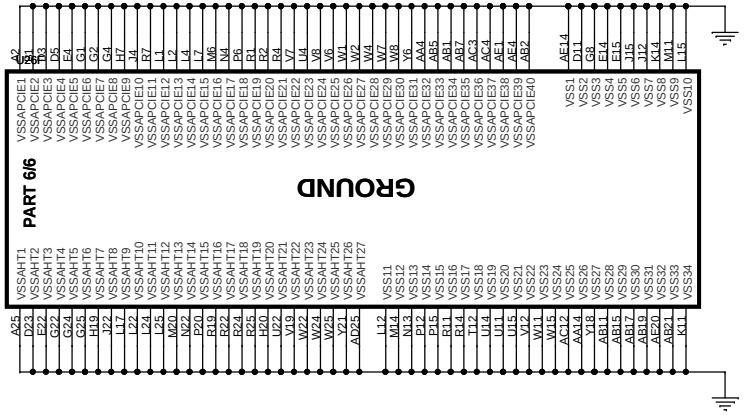
+1.8V — +VDDG_NB — Q18 *BSS138_NL/SOT23 — R215 *4.7K_4
(4,13) CPU_LDT_STOP# — NB_LDT_STOP# — R219 0_4 — **RS780**

+1.8V — +VDDG_NB — Q17 *BSS138_NL/SOT23 — R209 *4.7K_4
(4) CPU_LDT_REQ# — R214 0_4 — NB_ALLOW_LDTSTOP
(13) ALLOW_LDTSTOP — R208 0_4 — **RS780**

RX780 +1.8V — R218 *0_6 — +VDDG_NB
RS780 +3V — R217 *0_6 — +VDDG_NB

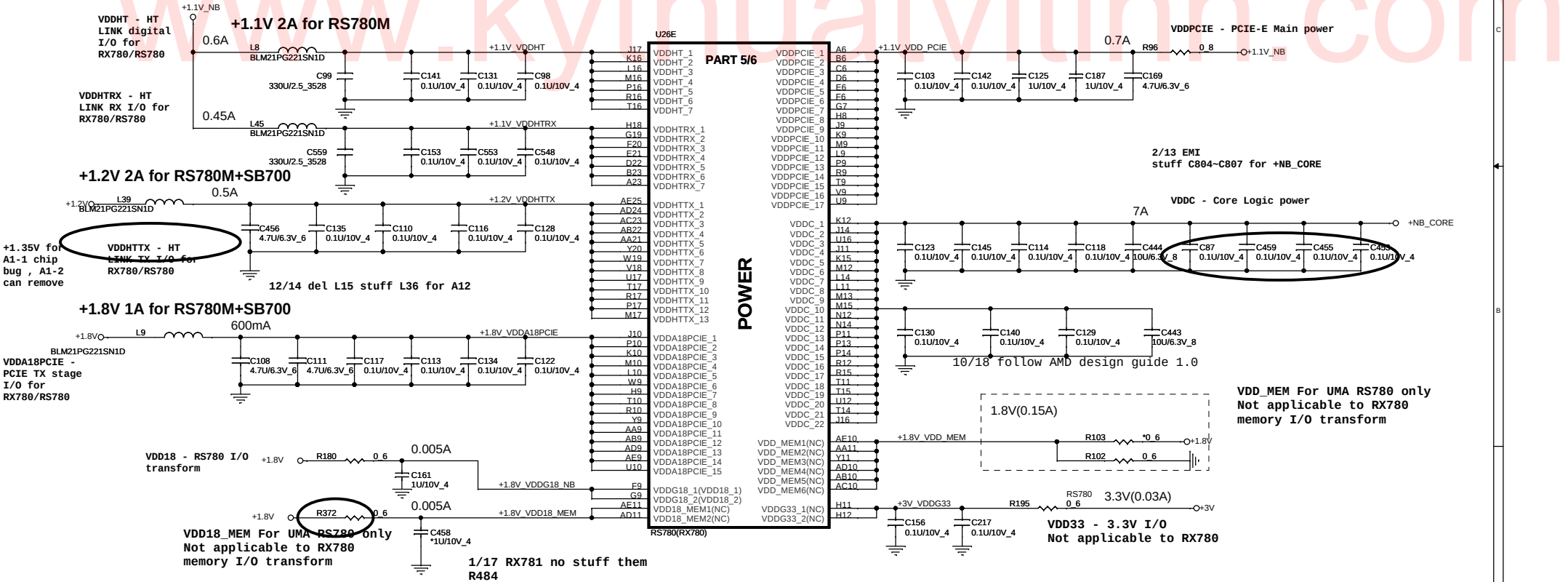
+3V — L43 *BLM21PG221SN1D — +3V_VDLT33_NB — C540 *2.2U/6.3V_6
VDDLT33 - LVDS or DVI/HDMI ANALOG RS740 only

Quanta Computer Inc.
PROJECT : ZK3
Size | Document Number: RS740/RS780-SYSTEM I/F 3/5 | Rev 1A
Date: Monday, August 18, 2008 | Sheet 11 of 43



RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RX780	RS780	PIN NAME	RX780	RS780
VDDHT	+1.1V	+1.1V	IOPLLVDD	NC	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	NC	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	NC	+1.8V
VDDG18	+1.8V	+1.8V	PLLVDD	NC	+1.1V
VDD18_MEM	NC	+1.8V	PLLVDD18	NC	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	NC	+1.8V/1.5V	VDDLTP18	NC	+1.8V
VDDG33	NC	+3.3V	VDDLT18	NC	+1.8V
IOPLLVDD18	NC	+1.8V	VDDLT33	NC	NC



Quanta Computer Inc.		
PROJECT : ZK3		
Size	Document Number: RS740/RS780-POWER5/5	Rev: 1A
Date: Monday, August 18, 2008	Sheet 12 of 43	

2/4 reserve C800 PLTRST#

PLACE THESE
PCIE AC
COUPLING CAPS
CLOSE TO U600

PCIE_PVDD-- PCIE PLL POWER

B test

1/31 voltage leakage remove R349

SB700
IC CTRL(528P) SB700 A11(218S7EALA11FG)
P/N : AJALA110T00

A11 default PCICLK5
A12 default GPIO41

All the PCI bus has build-in Pull-UP/Down resistors

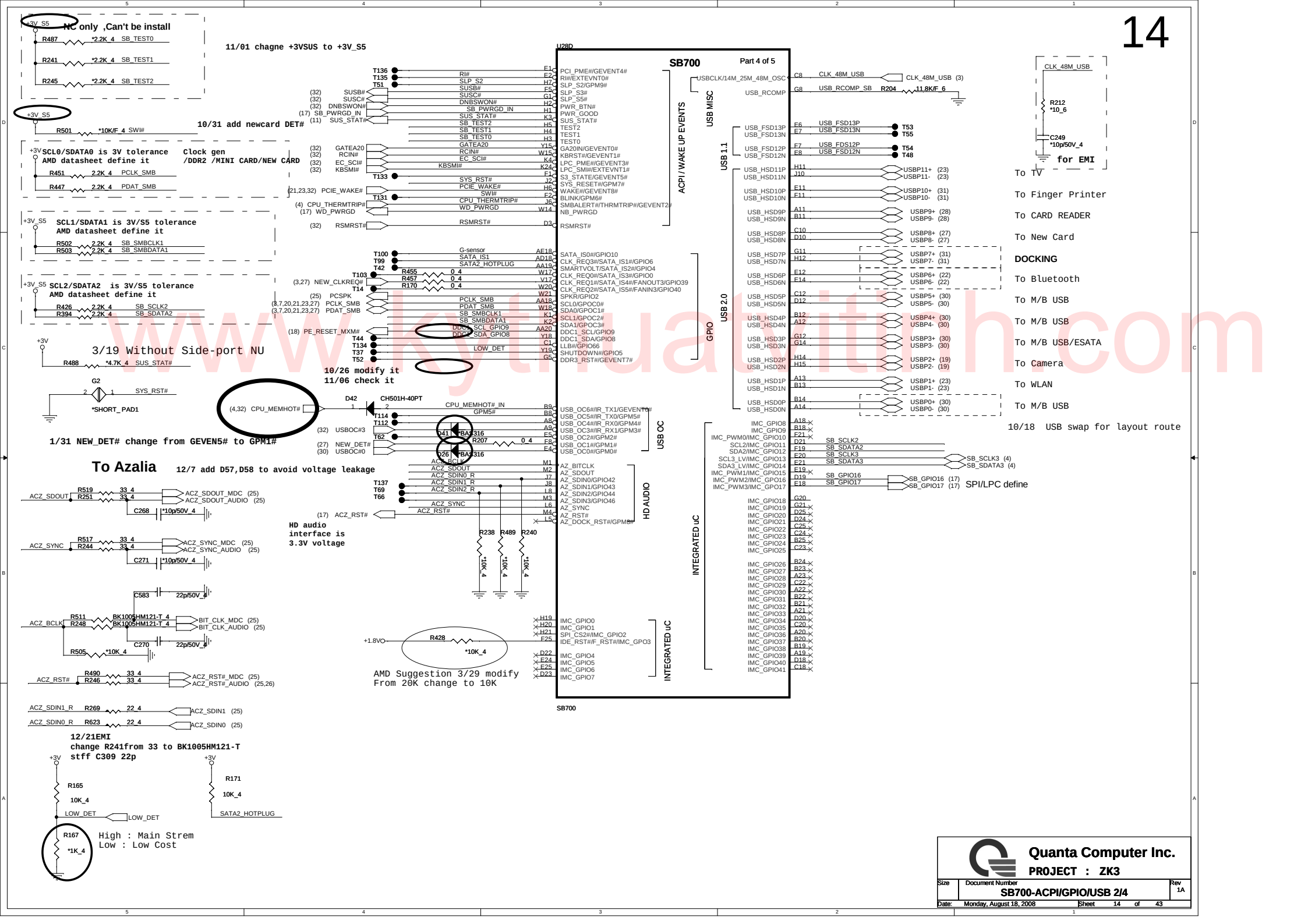
Maybe can remove

RTC

R571+R667 = (5V - 0.2V-2V)/0.2mA = 14k

4/14
R527, change from 2k to 0.
R524 change from 2K to 16K
R529,change from 6.8k to 68.1k
R531 change form 15k to 150k

Quanta Computer Inc.		
PROJECT : ZK3		
Size	Document Number: SB700-PCIE/PCI/CPU/LPC 1/4	Rev 1A
Date: Monday, August 18, 2008	Sheet 13 of 43	



Quanta Computer Inc.		
PROJECT : ZK3		
Size	Document Number: SB700-ACPI/GPIO/USB 2/4	Rev: 1A
Date: Monday, August 18, 2008	Sheet 14 of 43	

SATA PORT 0,1,2,3 can support AHCI mode

PLACE SATA AC COUPLING CAPS CLOSE TO SB700

MB ID Selection Table

Board ID	ID4	ID3	ID2	ID1	ID0
NEW CARD CARD BUS					H L
CCFL Panel LED Panel				H L	
W/ MXM W/O MXM			H L		
W/ S-VIDEO W/O S-VIDEO		H L			
W/ HDMI W/O HDMI	H L				

MB ID

Mount R441 and Unmout R442 for non IR SKU

SATA1 / SATA2 / E-SATA / ODD

2/22 change SATA ODD from port3 to port4 (solve ODD post detect fail)

SATA PORT 4,5 are only support IDE mode

PLACE SATA_CAL RES VERY CLOSE TO BALL OF SB700

NOTE:
R361 IS 1K 1% FOR 25MHz XTAL, 4.99K 1% FOR 100MHz INTERNAL CLOCK

PLVDD_SATA-- SATA PLL POWER

XTLVDD_SATA-- SATA crystal power

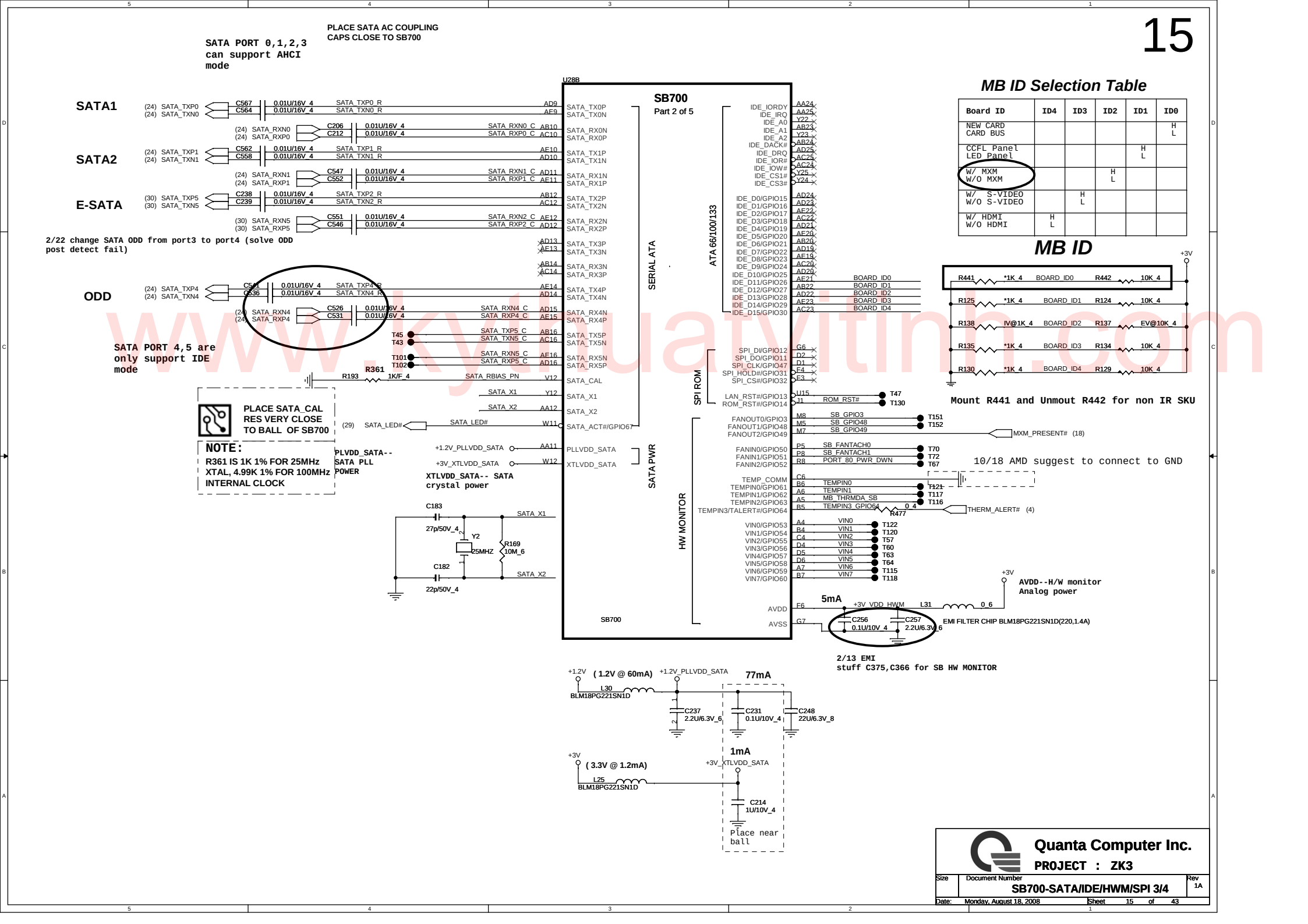
10/18 AMD suggest to connect to GND

AVDD--H/W monitor Analog power

2/13 EMI stuff C375,C366 for SB HW MONITOR

U28B SB700 Part 2 of 5

SERIAL ATA / ATA 66/100/133 / SPI ROM / SATA PWR / HW MONITOR



Quanta Computer Inc.
PROJECT : ZK3

Size	Document Number	Rev
	SB700-SATA/IDE/HWM/SPI 3/4	1A

Date: Monday, August 18, 2008 Sheet 15 of 43

PLACE ALL THE DECOUPLING CAPS ON
THIS SHEET CLOSE TO SB AS POSSIBLE.

12/14 del R234 stuff R235 for A12

VDD-- S/B CORE power

VDDQ--3.3V I/O power

0.8A

1.8V : FLASH MEMORY MODE(DEFAULT)
3.3V: IDE MODE

10/18 change to +1.8V

2008-MAR CHECK LIST CHANGE TO 3V because no IDE device

PCIE_VDDR--PCIE I/O power

844mA

AVDD_SATA--SATA phy power

0.2A

For support USB wakeup-->3V_S5

AVDDTX--USB Phy
Analog I/O power

0.2A

CKVDD_1.2V-- Internal
clock Generator I/O
power

286mA

S5_3.3--3.3v standby power

0.01A

Change to 0603

S5_1.2V--1.2V standby power

0.22A

0.2A

V5_VREF--PCI 5V TOLERANCE

4mA

7mA

44mA

16mA

USB_PHY_1.2V--USB Phy
digital power

AVDDC--USB Analog PLL power

AVDDCK_1.2--USB Phy
digital power

AVDDCK_3.3--Analog
system PLL power

SB700

Part 3 of 5

POWER

GROUND

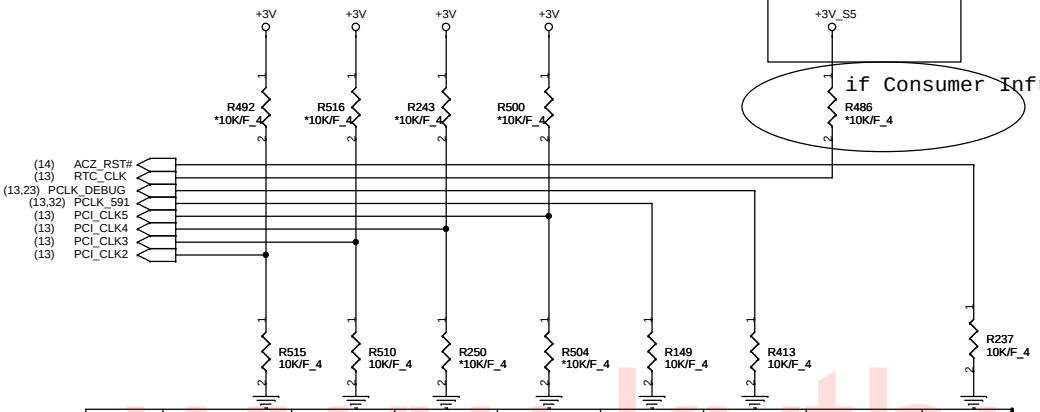
Part 5 of 5

Quanta Computer Inc.
PROJECT : ZK3

Size	Document Number	Rev
	SB700-PWR/DECOUPLING 4/4	1A
Date: Monday, August 18, 2008	Sheet 16 of 43	

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

It must ready refore RSMRST#

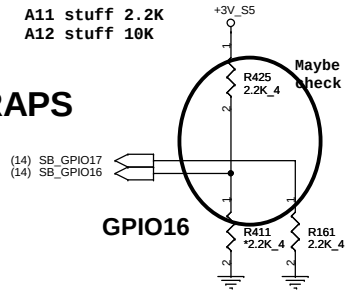


if Consumer Infrared is implemented

REQUIRED STRAPS

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT
					EC ENABLED			ENABLE PCI MEM BOOT

A11 stuff 2.2K
A12 stuff 10K



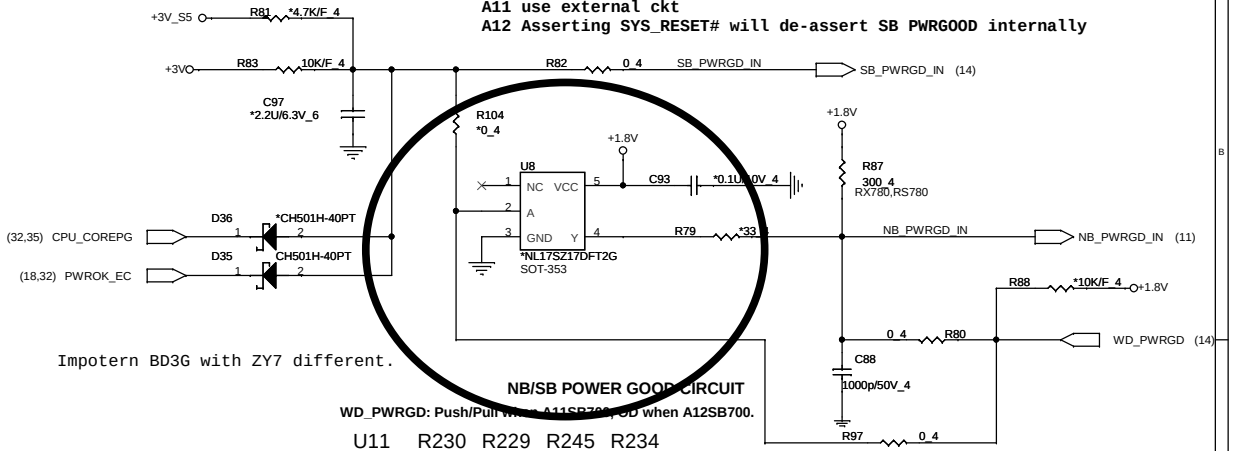
Maybe can be remove -- internla pull up check AMD

GPIO16 GPIO17

TYPE	GPIO16	GPIO17
FWH	L : 2.2K pull down	L : 2.2K pull down
LPC	NC	L : 2.2K pull down
SPI	L : 2.2K pull down	NC
RSVD	NC	NC

NB_PWRGD_IN:
RS780/RX780 = 1.8V; RS740 = 3.3V
Do NOT share it with SB_PWRGD when use Internal Clk Gen
(Need SB PLL initialize firstly)

SB_PWRGD
A11 use external ckt
A12 Asserting SYS_RESET# will de-assert SB PWRGOOD internally



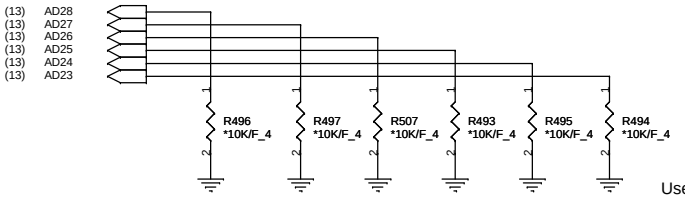
Impotern BD3G with ZY7 different.

NB/SB POWER GOOD CIRCUIT

WD_PWRGD: Push/Pull When A11SB700, OD when A12SB700.

DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



Use 2.2K PD.

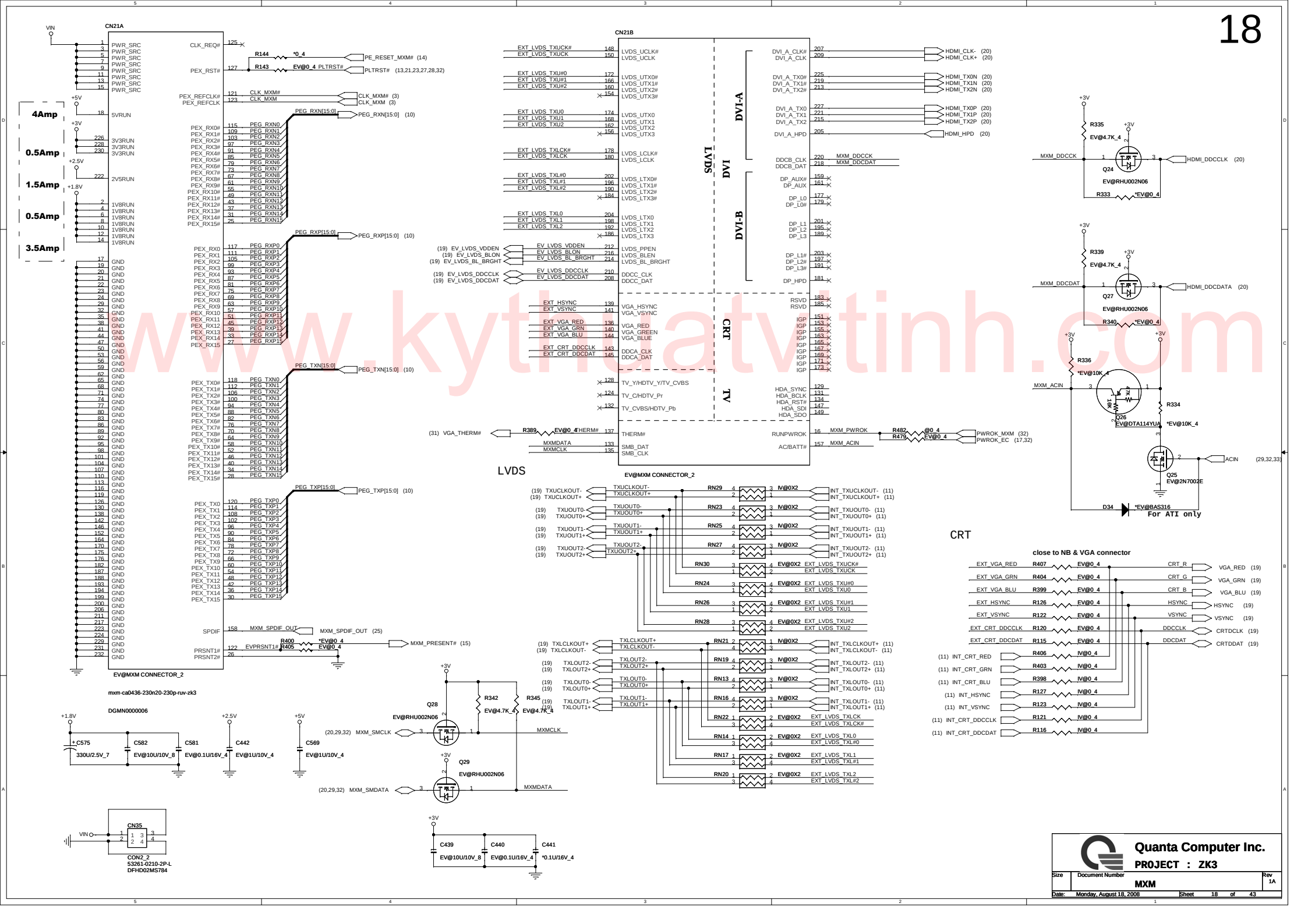
	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

	U11	R230	R229	R245	R234
RX780	V	V	V	X	X
RS780M					

AL17SZ17000	IC(5P) NL17SZ17DFT2G(SOT-353)	SOT-353
ALUC1G17000	IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5)	SOT23-5

Quanta Computer Inc.
PROJECT : ZK3

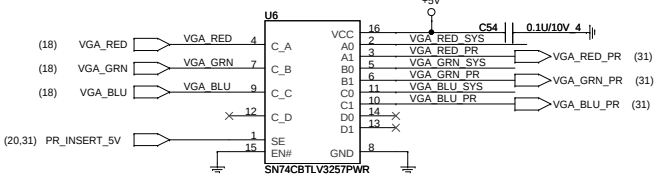
Size	Document Number	Rev
	SB700-STRAPS	1A
Date: Monday, August 18, 2008	Sheet 17 of 43	



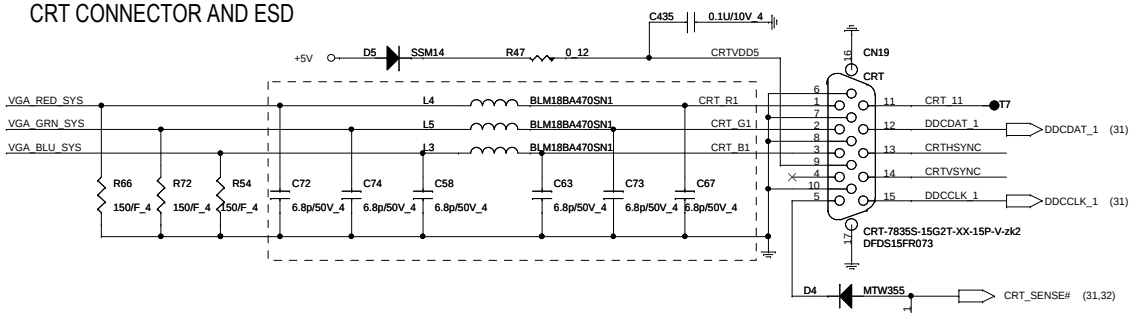
Quanta Computer Inc.			
PROJECT : ZK3			
Size	Document Number		Rev
	MXM		1A
Date: Monday, August 18, 2008	Sheet 18 of 43		

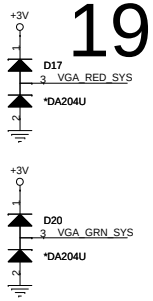
CRT

CRT SWITCH

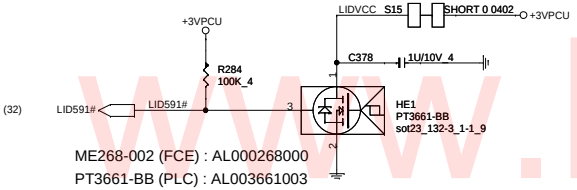


CRT CONNECTOR AND ESD

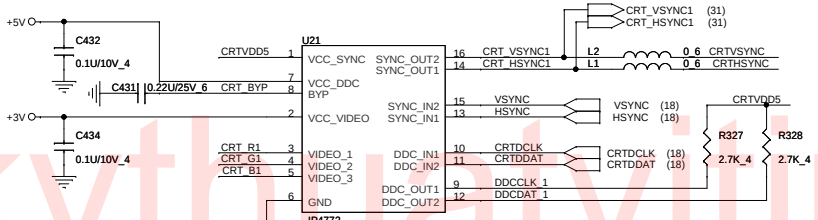


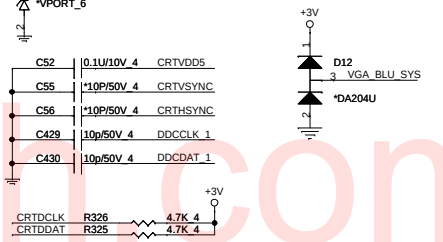


Lid Switch

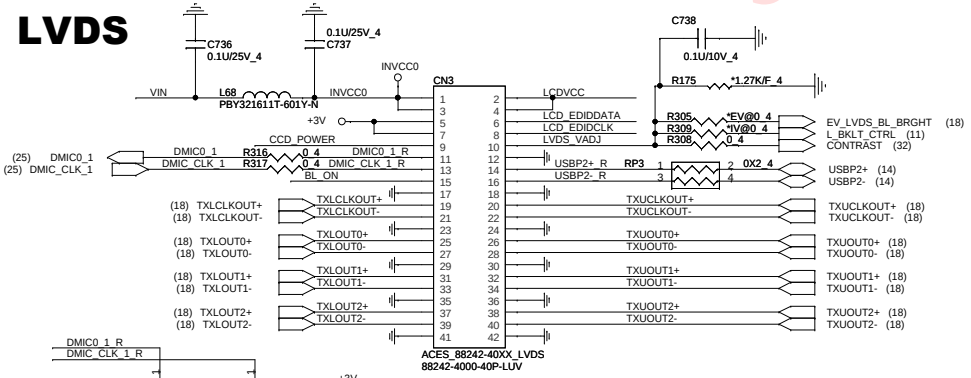


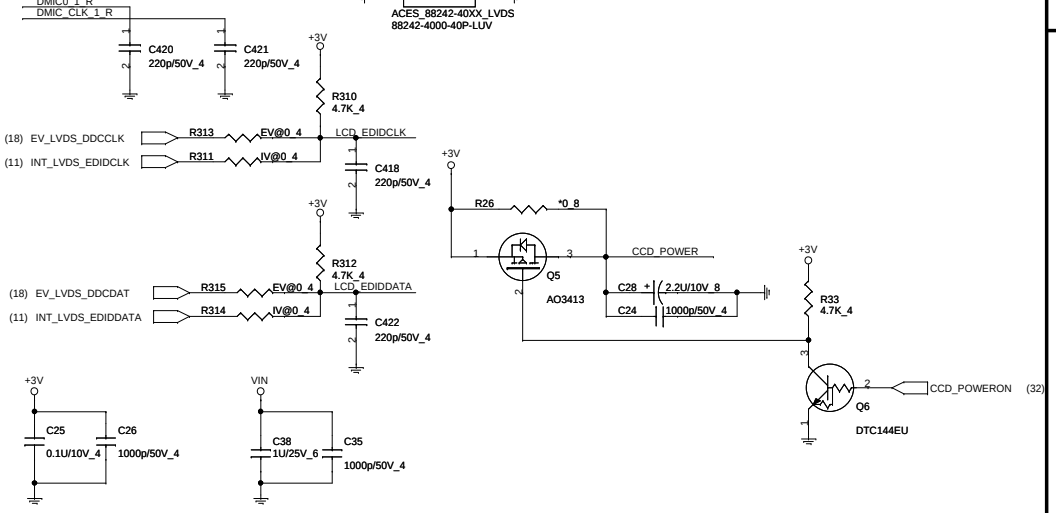
ME268-002 (FCE) : AL000268000
PT3661-BB (PLC) : AL003661003



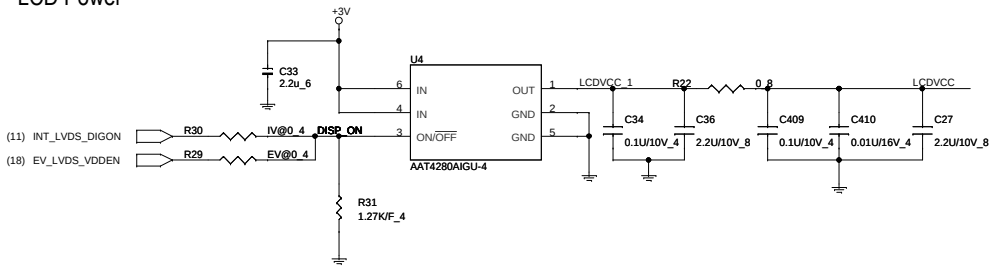


LVDS

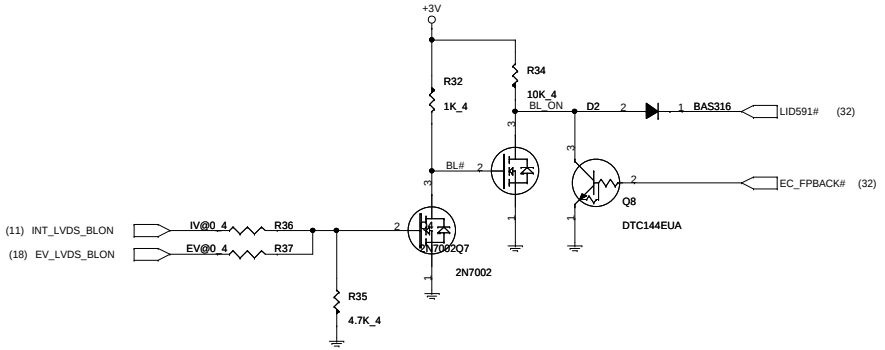




LCD Power

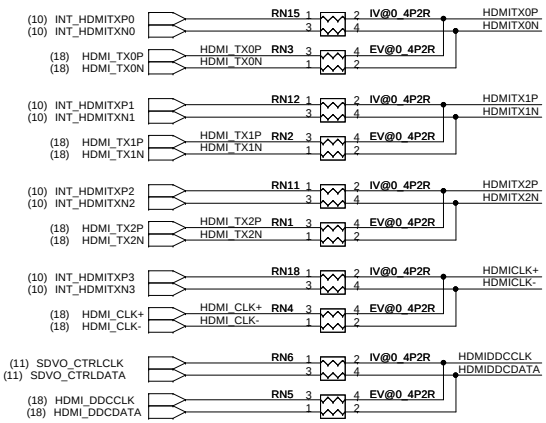


Backlight Control & LID

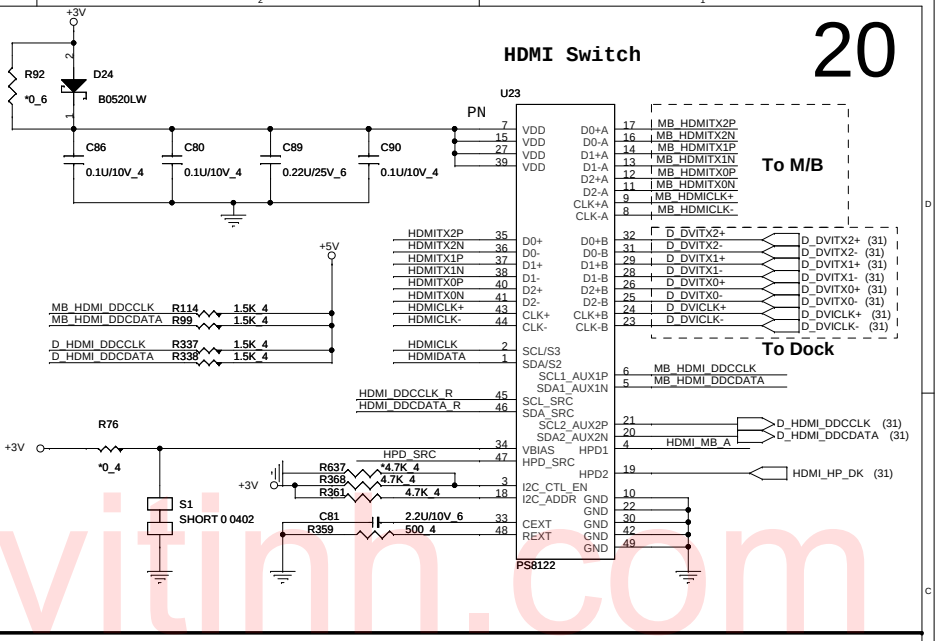


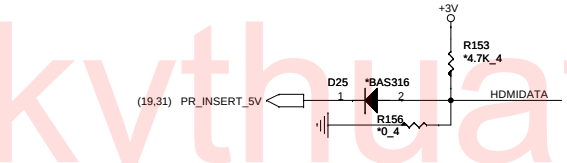
Quanta Computer Inc.		
PROJECT : ZK3		
Size	Document Number	Rev
	CRT/LVDS/CAMERA/LID	1A
Date: Monday, August 18, 2008	Sheet 19 of 43	

HDMI CONNECTOR (HDMI)

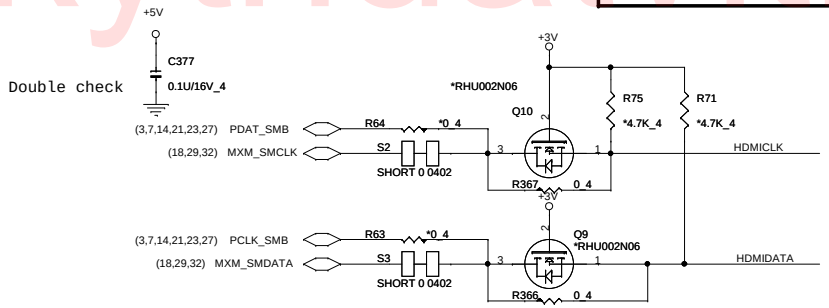


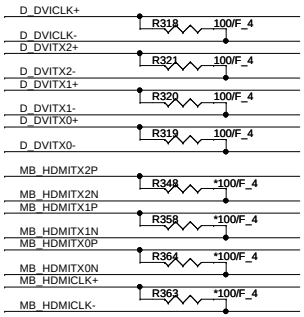
HDMI Switch

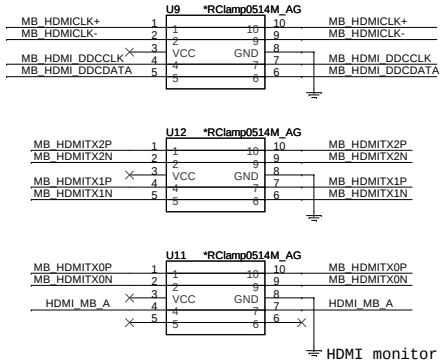




Double check

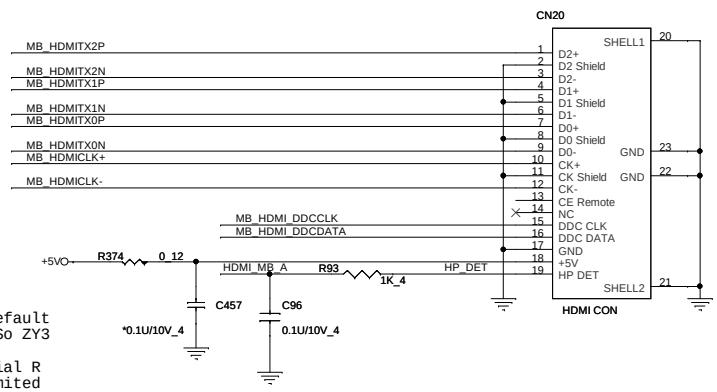


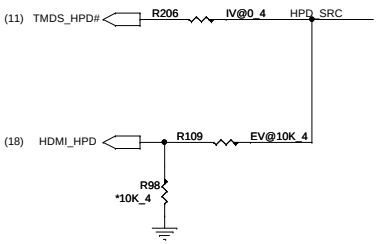




HDMI monitor default have PU to 5V.So ZY3 PD for level change.And serial R for current limited

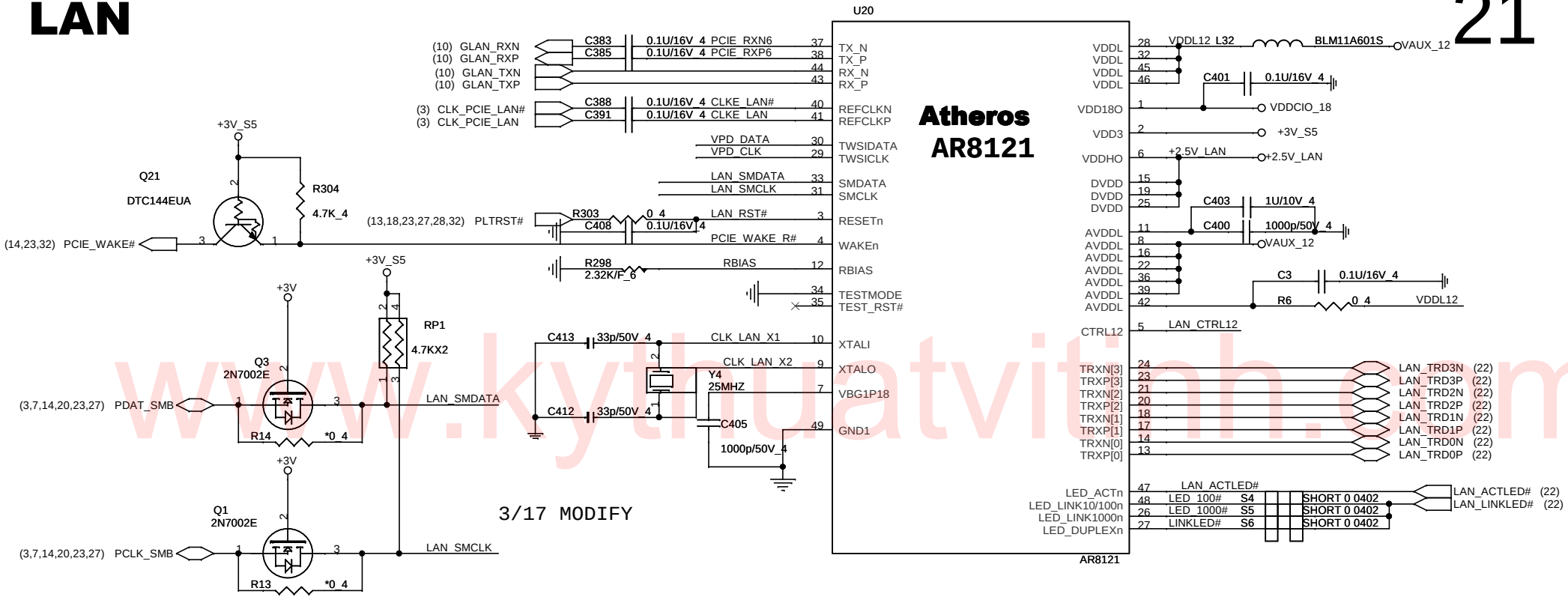
HDMI connector



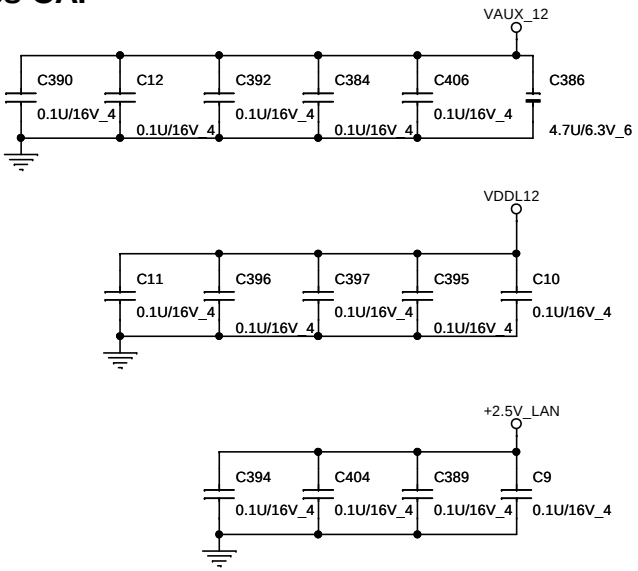


Quanta Computer Inc.		
PROJECT : ZK3		
Size	Document Number	Rev
	LVDS/HDMI/CAMERA/LID	1A
Date: Monday, August 18, 2008	Sheet 20 of 43	

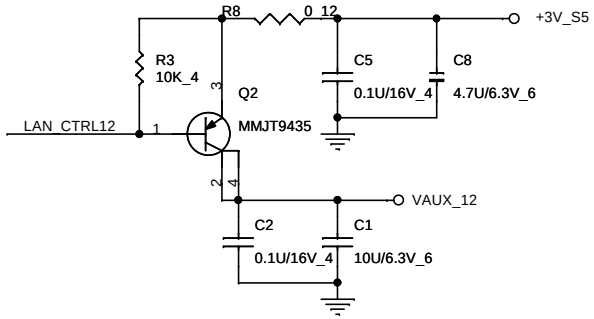
LAN



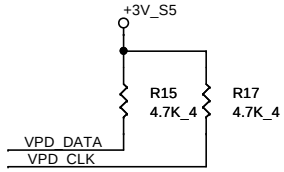
Bypass CAP



Regulator(1.2V)



EEPROM

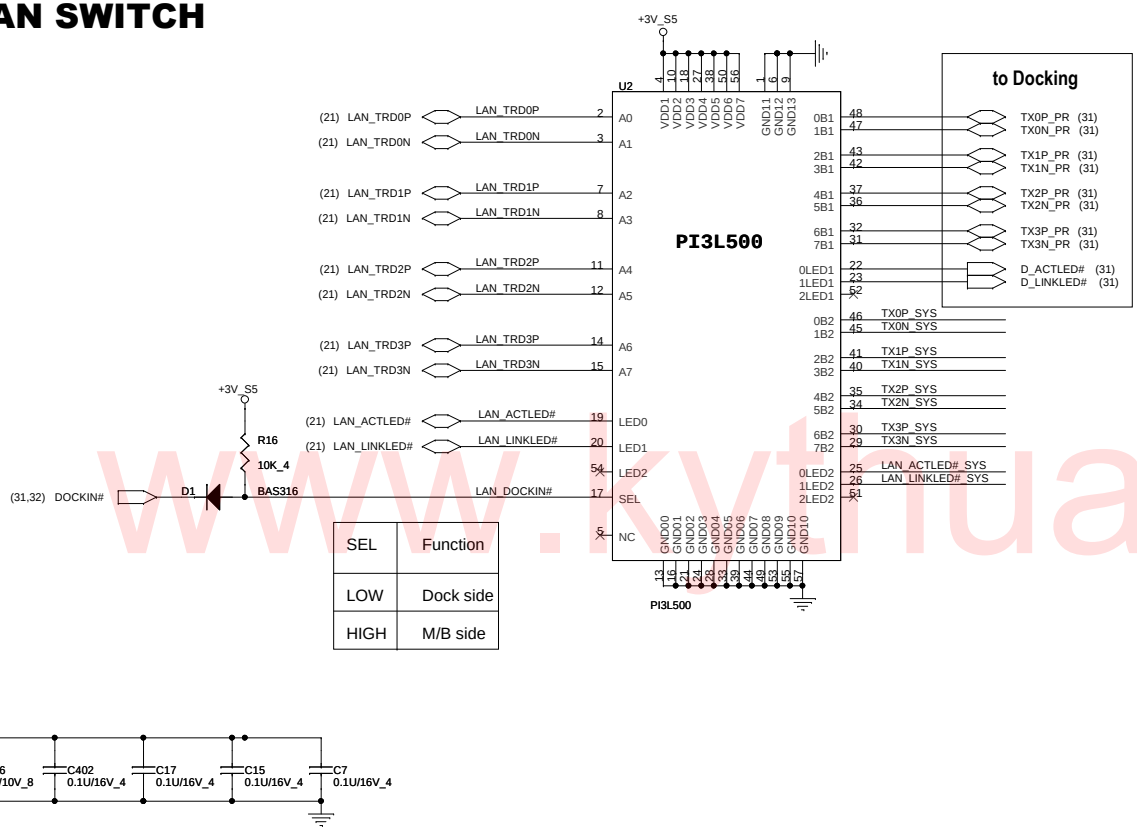


Quanta Computer Inc.

PROJECT : ZK3

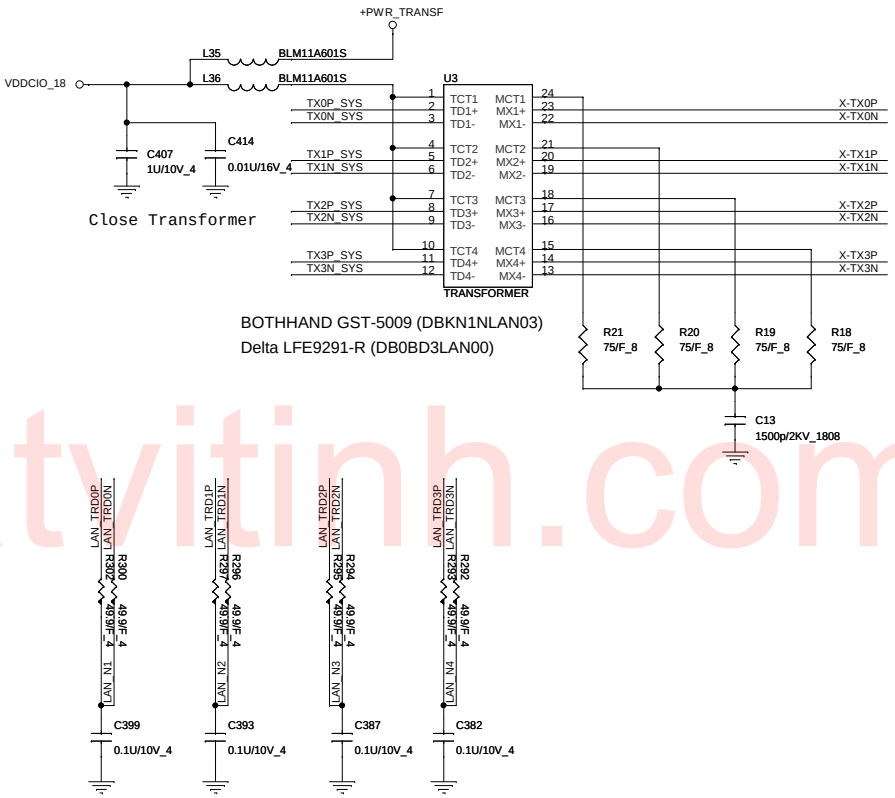
Size	Document Number	Rev
	AR8121 LAN	1A
Date: Monday, August 18, 2008	Sheet 21 of 43	

LAN SWITCH

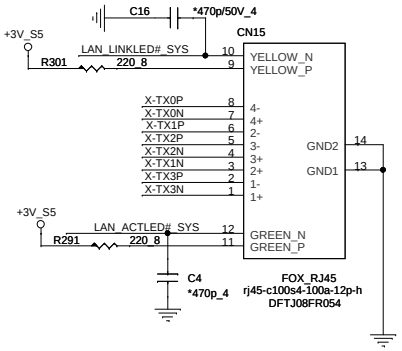


SEL	Function
LOW	Dock side
HIGH	M/B side

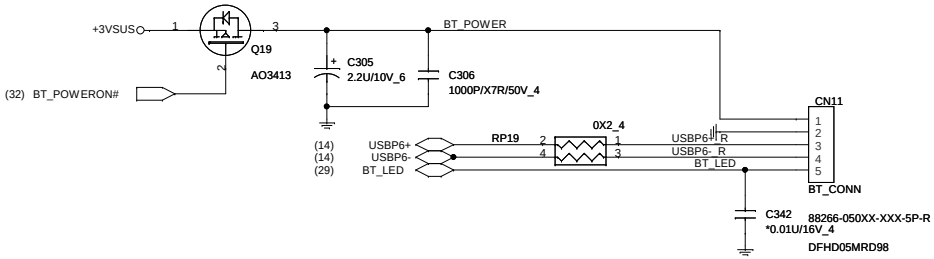
TRANSFORMER



RJ45



BLUETOOTH MODULE CONNECTOR

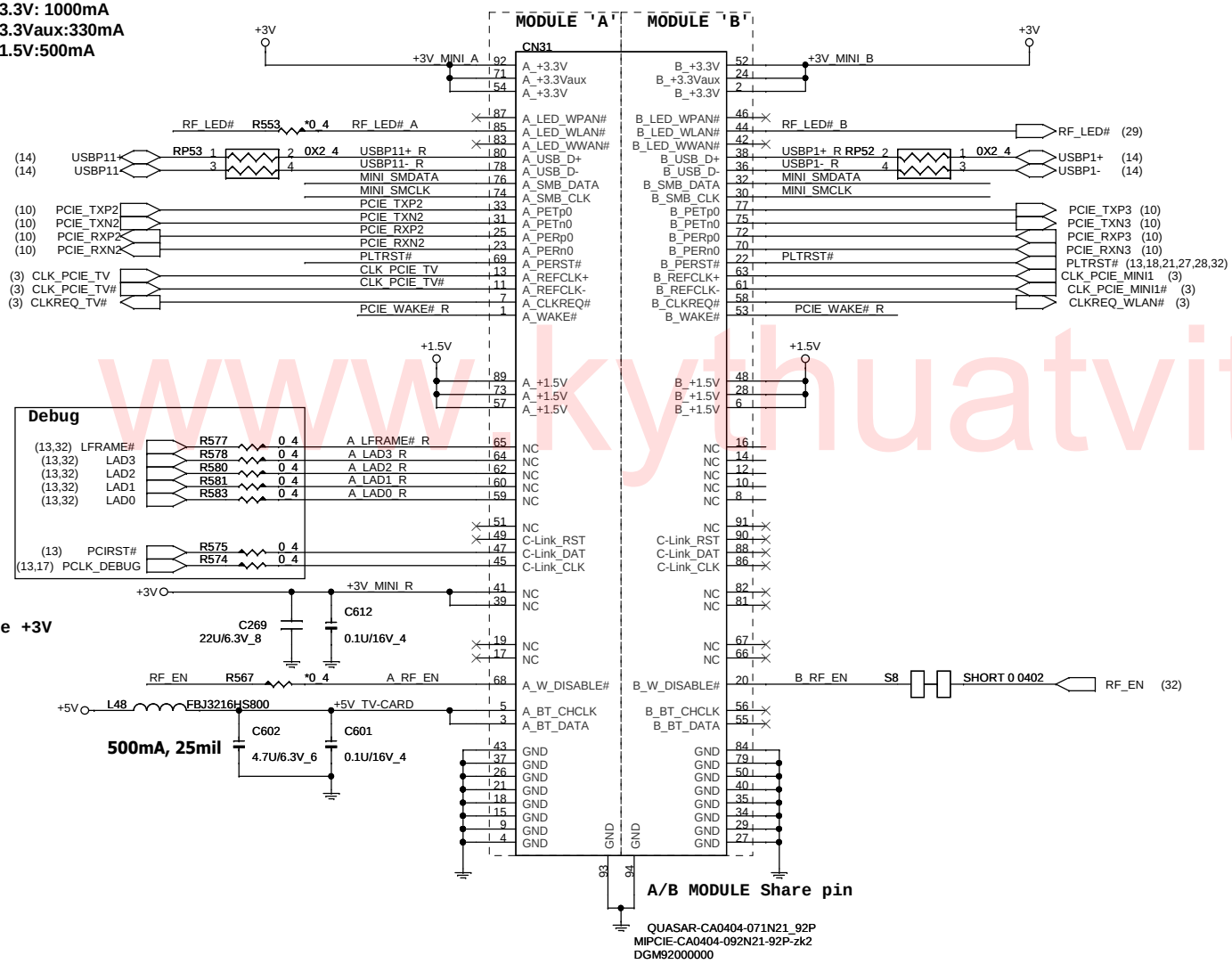


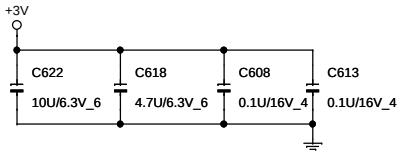
Quanta Computer Inc.
PROJECT : ZK3

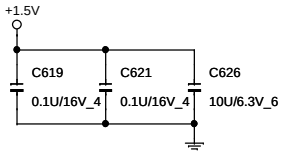
Size	Document Number	Rev
	LAN SWITCH/TRANSFORMER/RJ45/BT	1A
Date: Monday, August 18, 2008	Sheet 22 of 43	

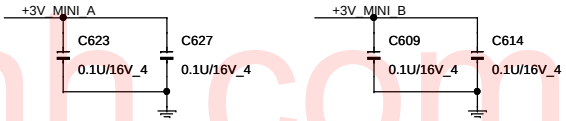
MINI-CARD

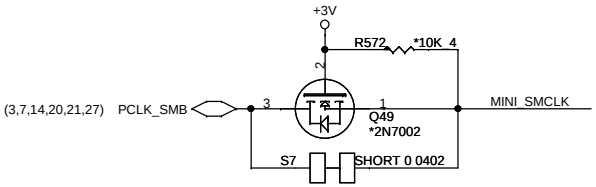
+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

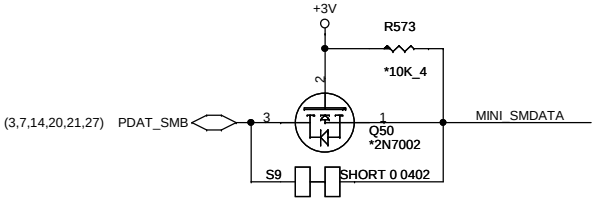


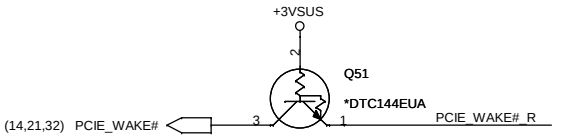


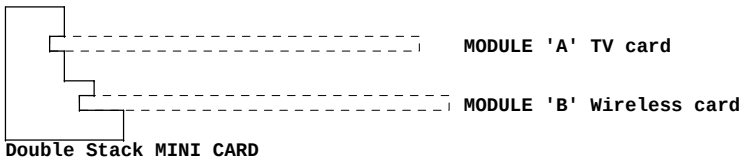






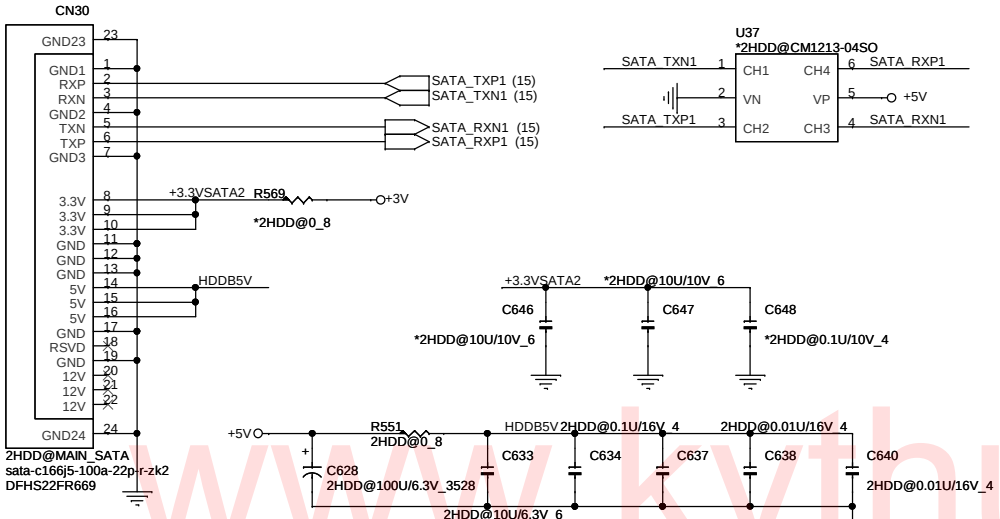




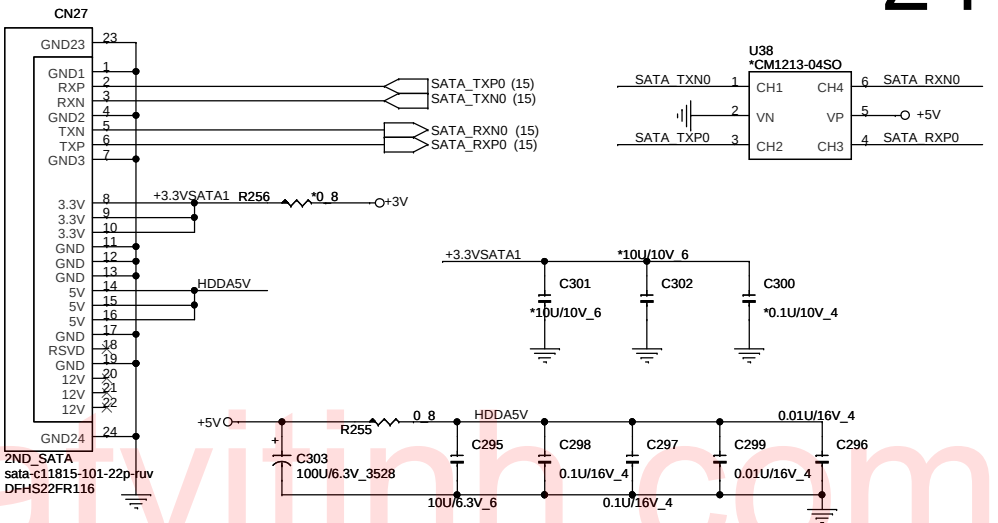


Quanta Computer Inc.		
PROJECT : ZK3		
Size	Document Number: MINI PCI-E card/TV	Rev: 1A
Date: Monday, August 18, 2008	Sheet 23 of 43	

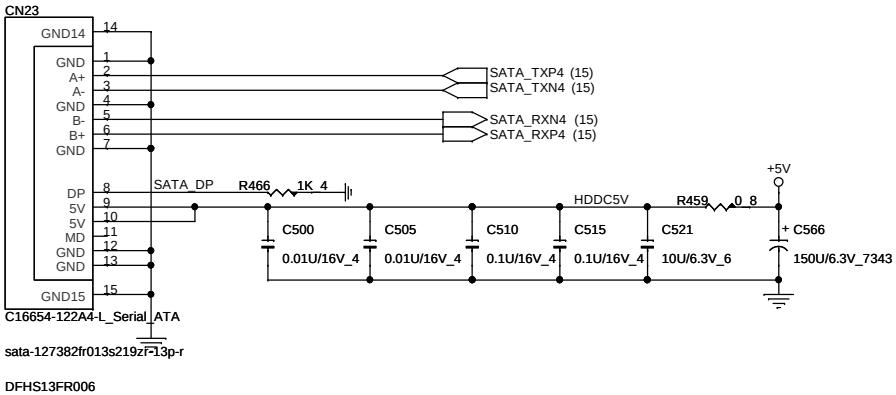
2ND SATA HDD



SATA HDD



ODD (SATA)



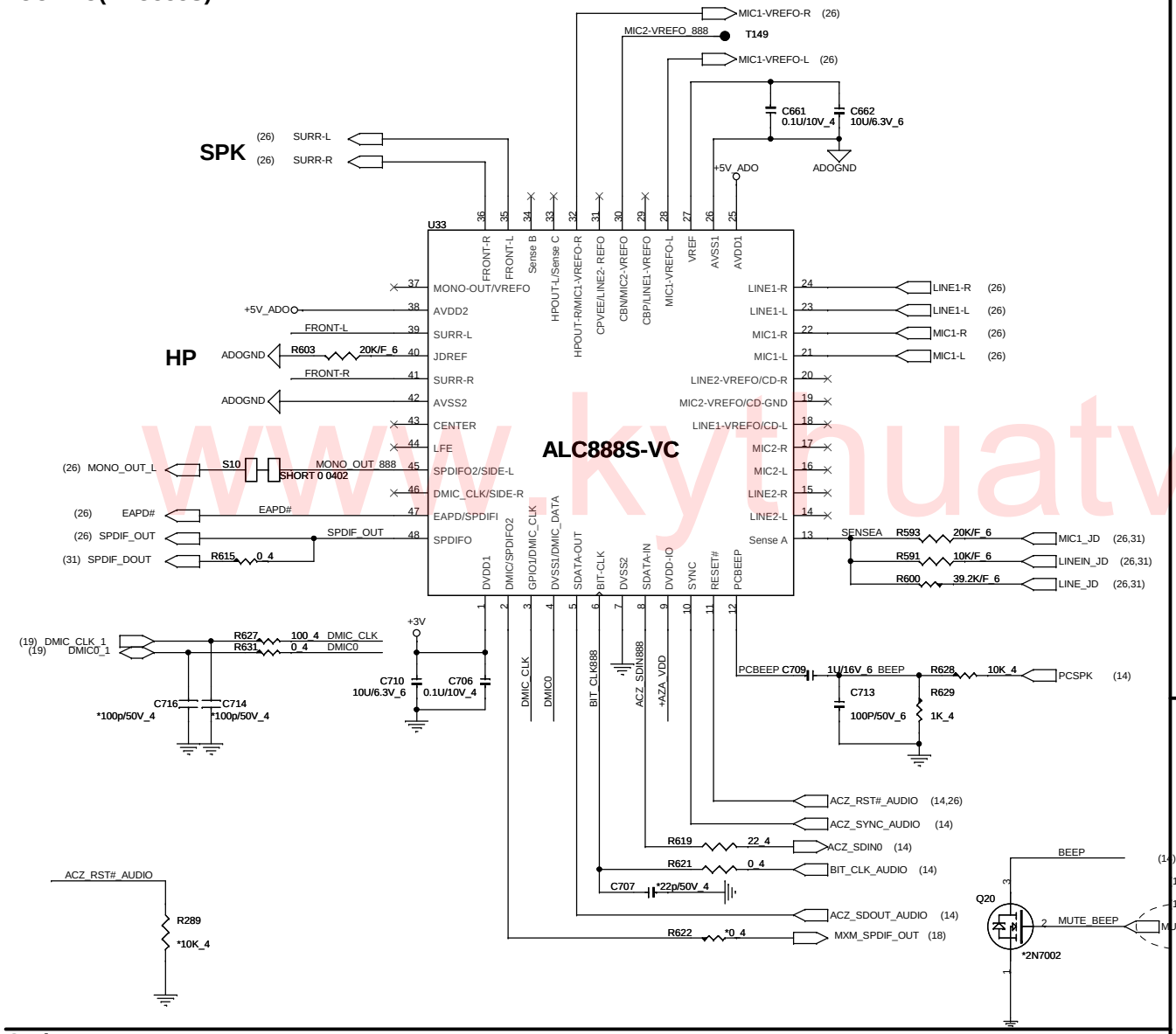
Quanta Computer Inc.

PROJECT : ZK3

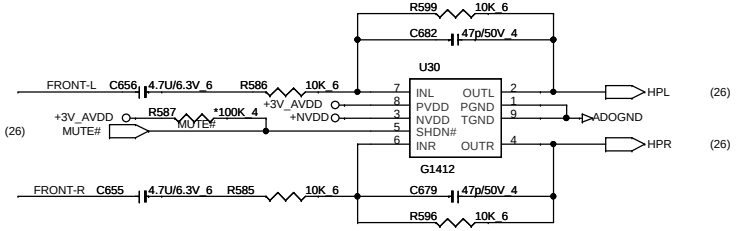
Size	Document Number	Rev
	SATA-HDD/ODD/USB-ESATA	1A

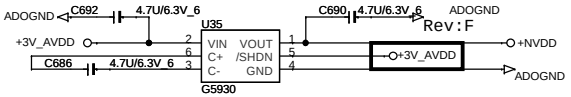
Date: Monday, August 18, 2008 Sheet 24 of 43

CODEC(ALC888S)

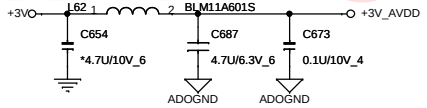


LINE-Out Amplifier

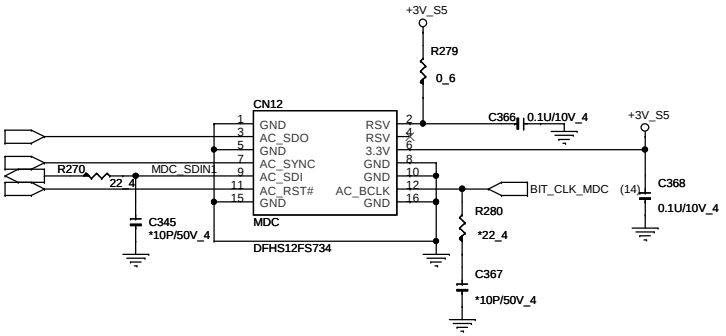




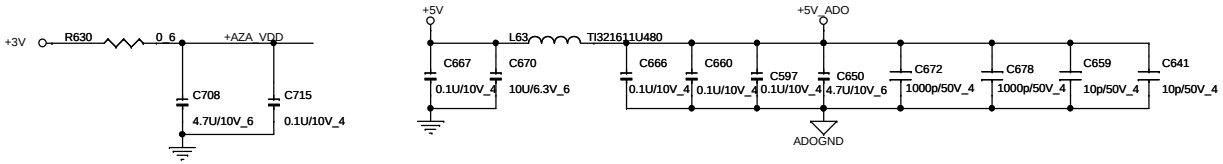
LINE-Out Amplifier Power



MDC



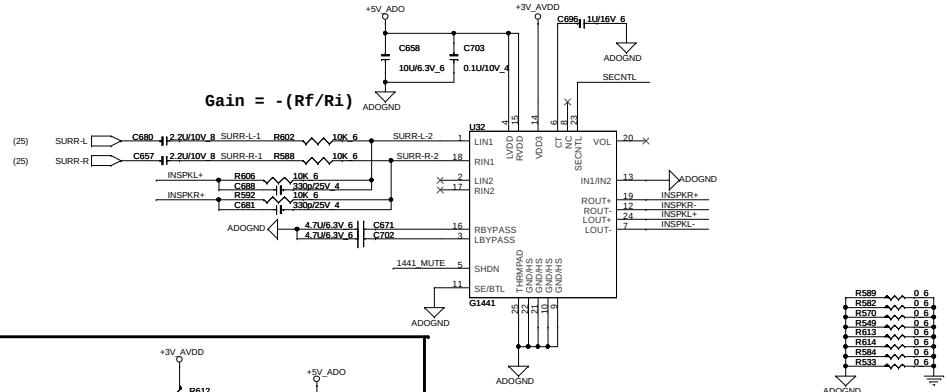
Codec Power



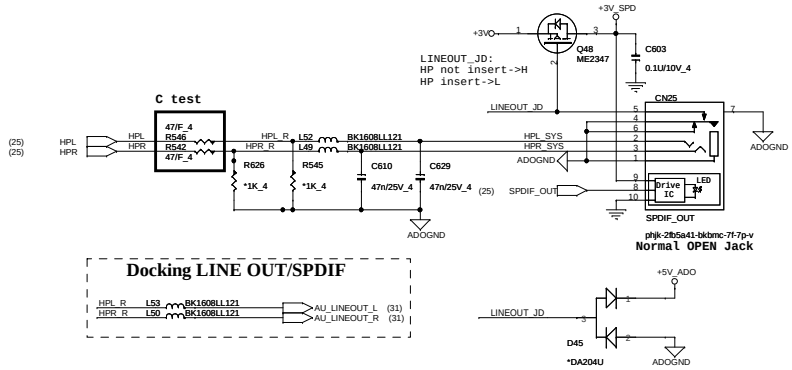
Quanta Computer Inc.
PROJECT : ZK3

Size	Document Number	Rev
	REALTEK ALC663&888/MDC	1A
Date: Monday, August 18, 2008	Sheet 25 of 43	

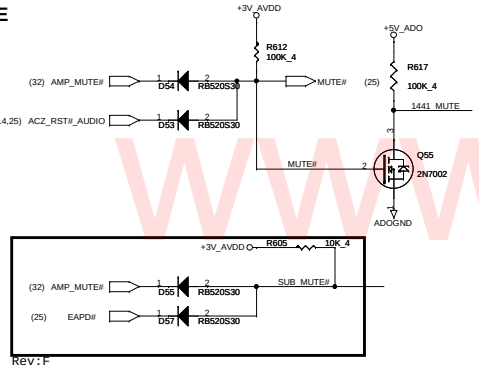
SPEAKER AMP.



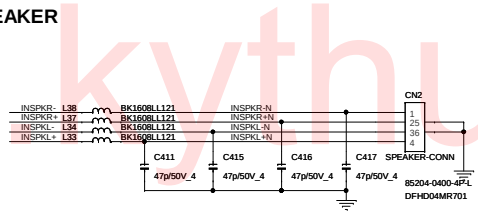
LINE-OUT/SPDIFO

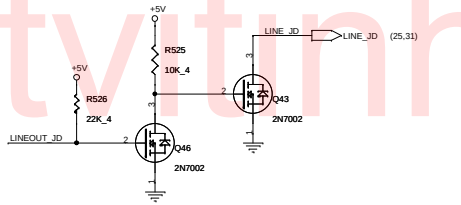


MUTE

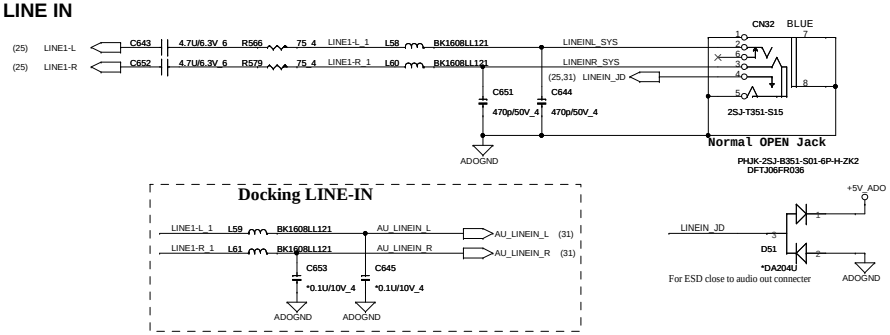


SPEAKER

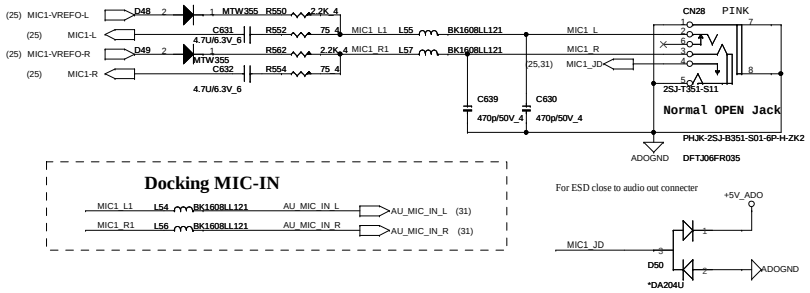




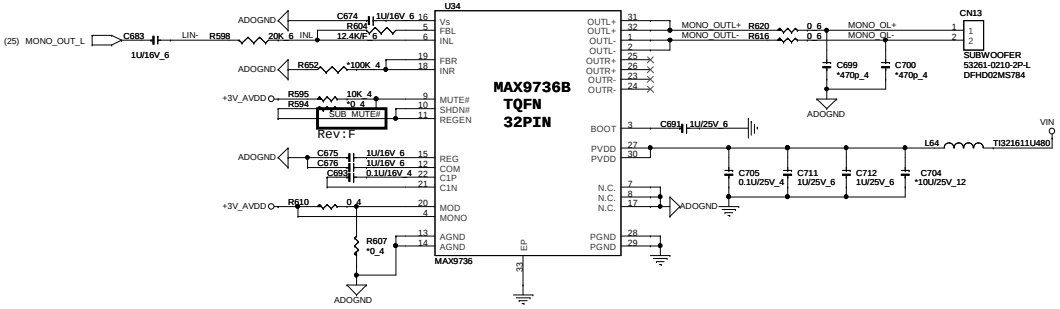
LINE IN



MIC



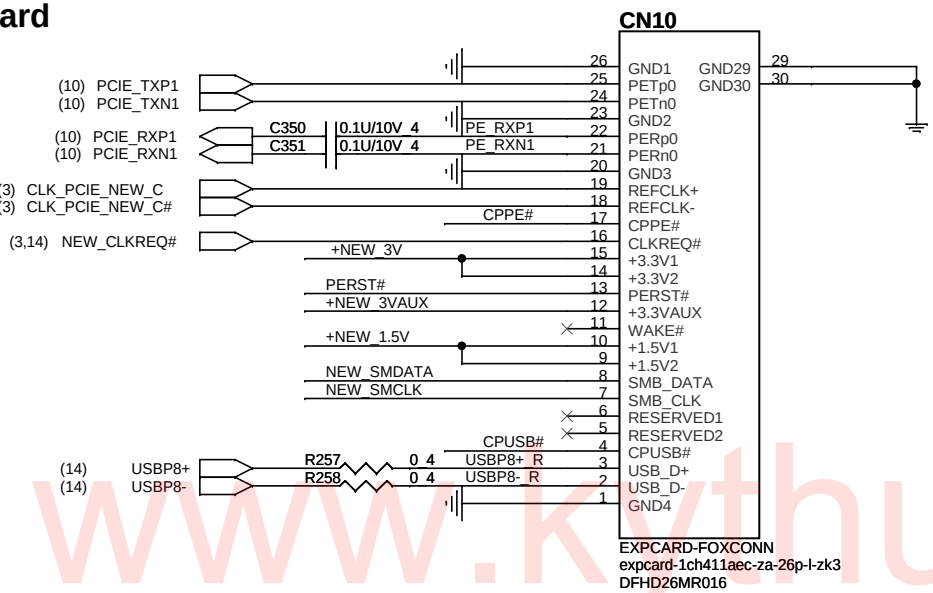
SUBWOOFER



Quanta Computer Inc.
PROJECT : ZK3

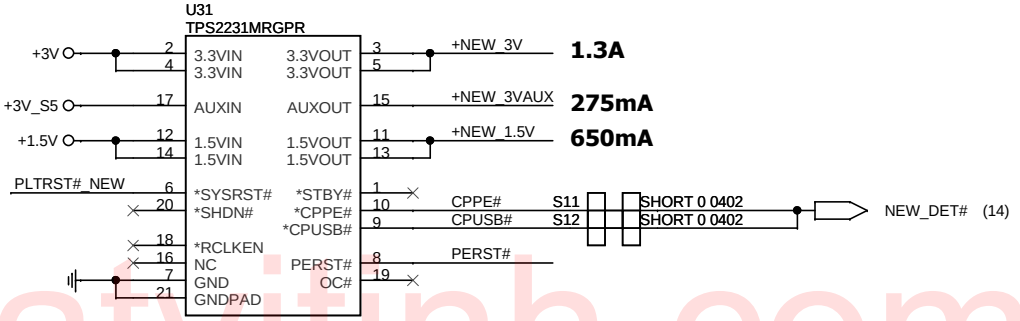
Size	Document Number	Rev
	AMP /AUDIO JACK CONN	1A
Date: Monday, August 18, 2008	Sheet 26 of 43	

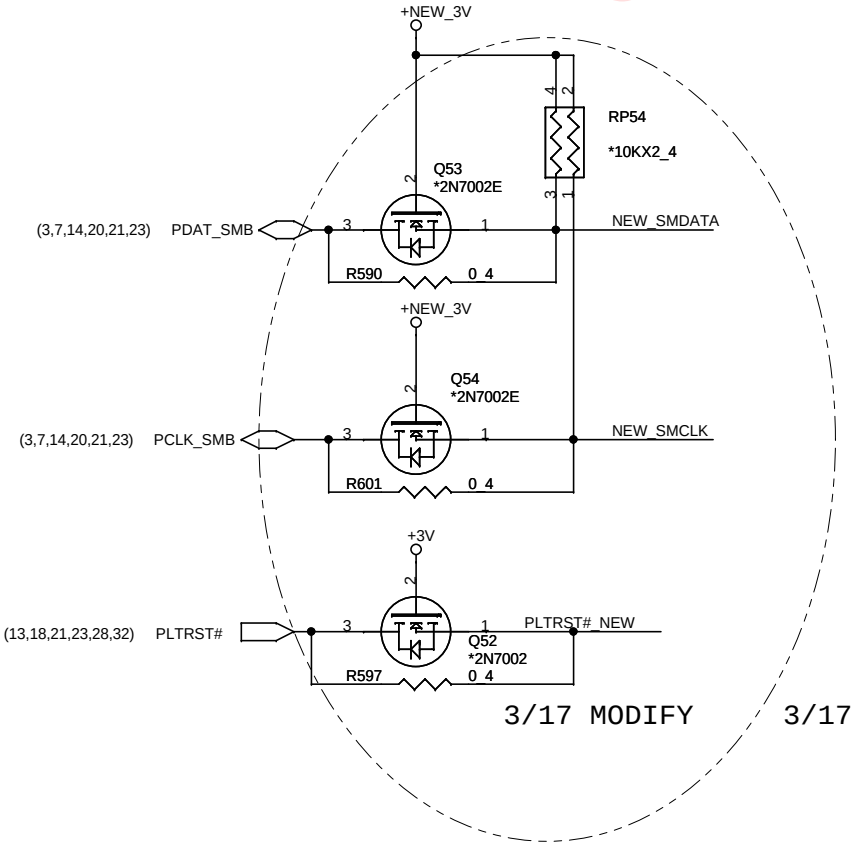
New card

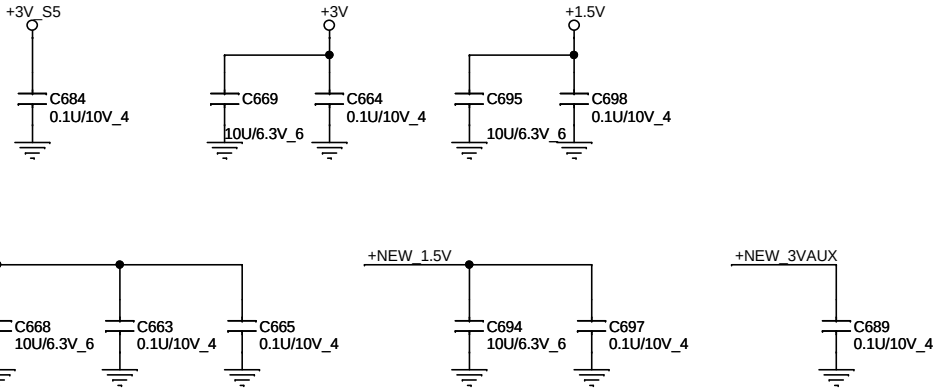


NEW CARD'S POWER SWITCH

TI: AL002231000
GMT: AL000577002



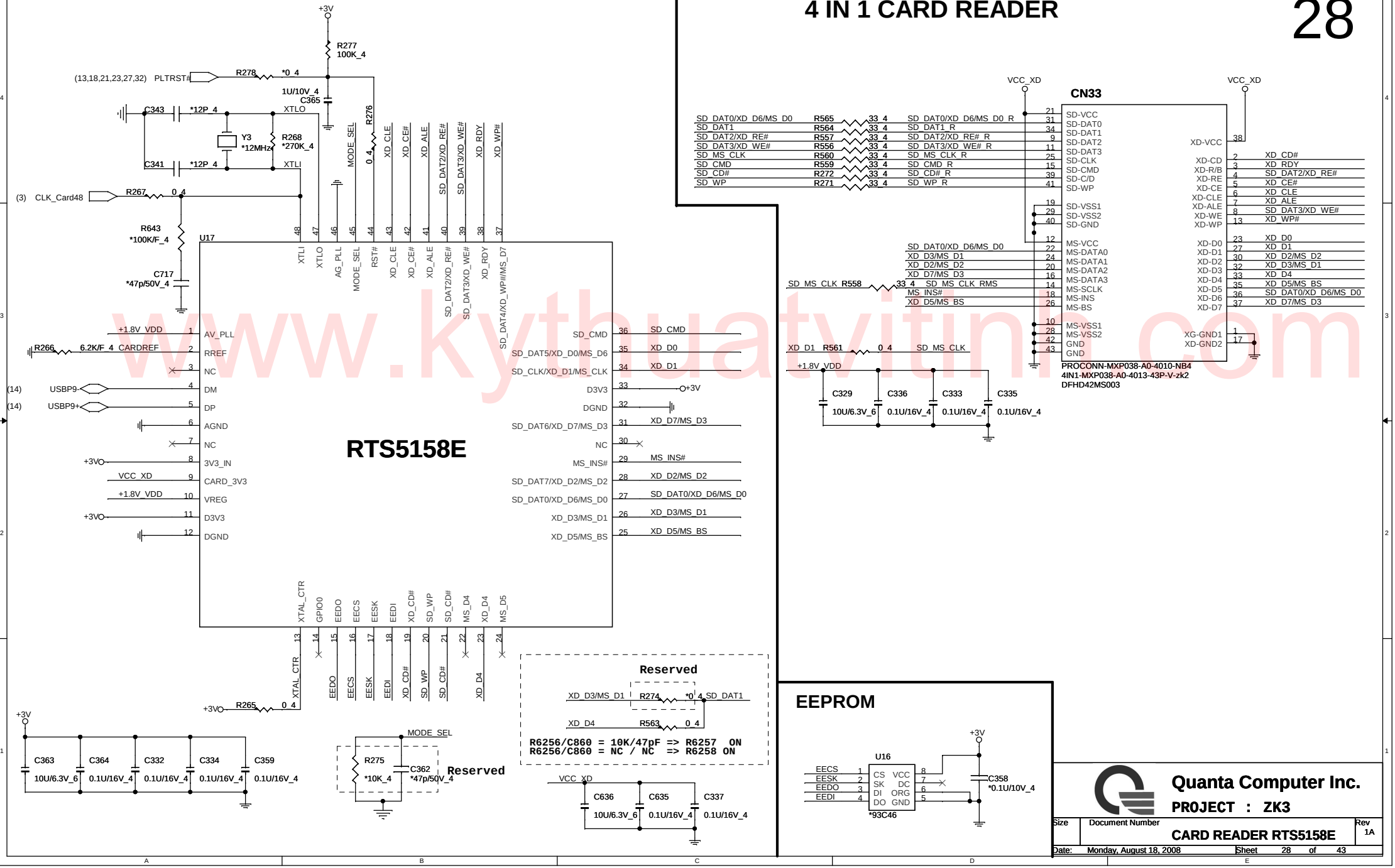




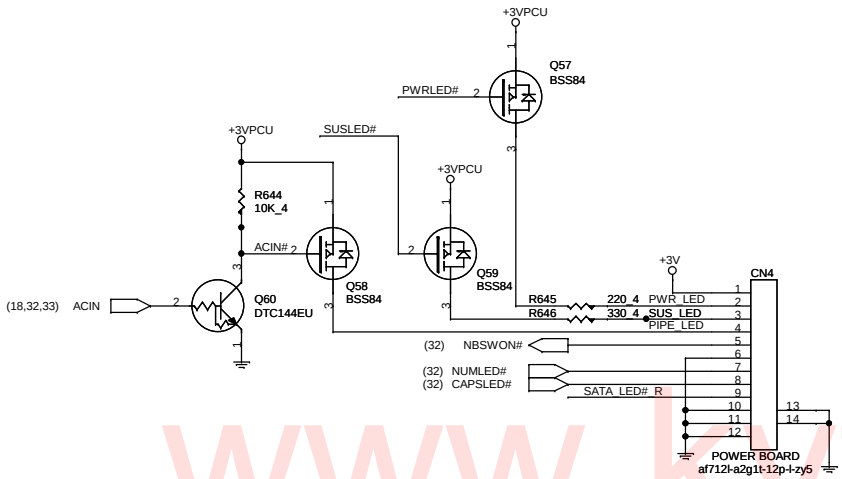
3/17 MODIFY 3/17 MODIFY

Quanta Computer Inc.		
PROJECT : ZK3		
Size	Document Number: NEW CARD	Rev: 1A
Date: Monday, August 18, 2008	Sheet 27 of 43	

4 IN 1 CARD READER

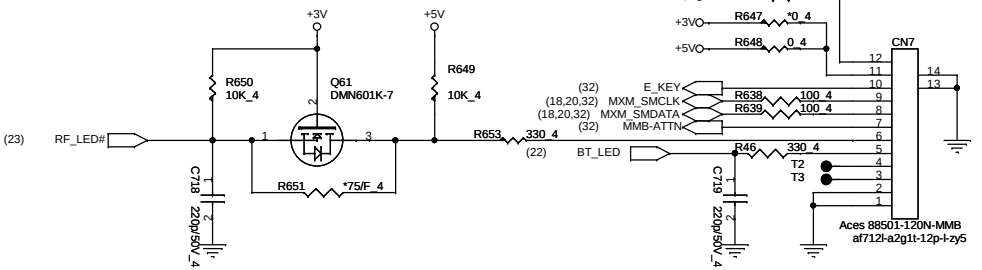


POWER BOARD



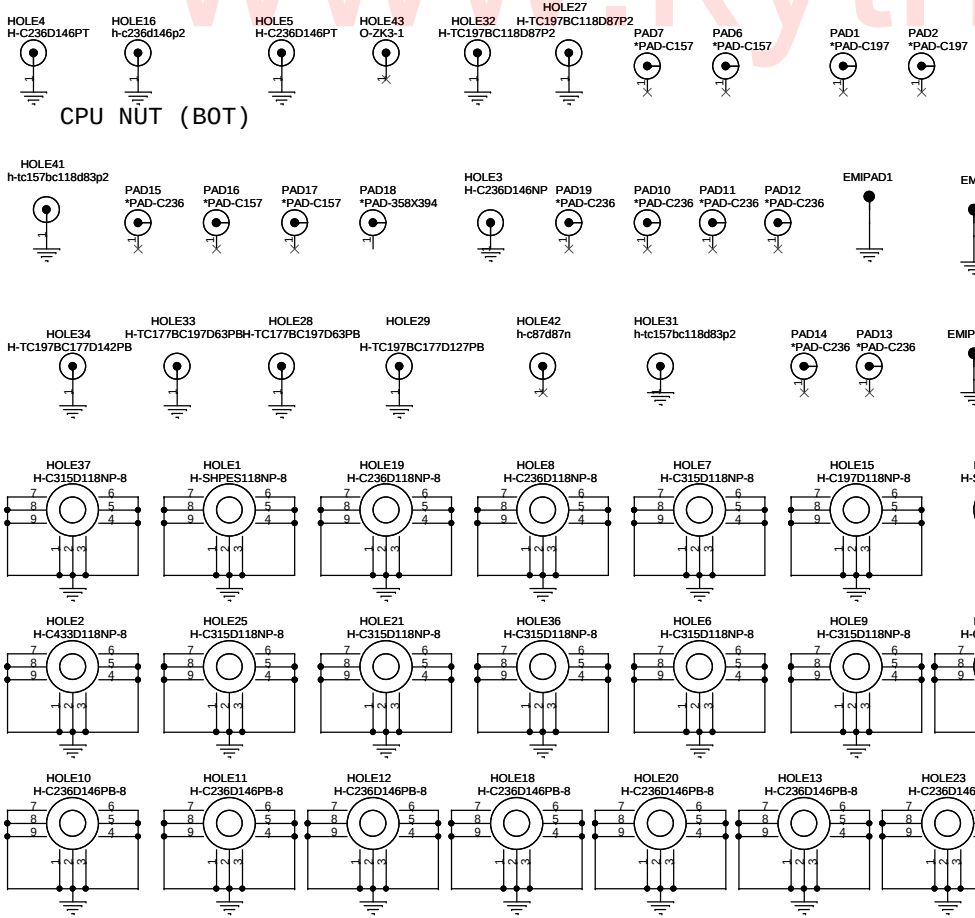
MMB

C test

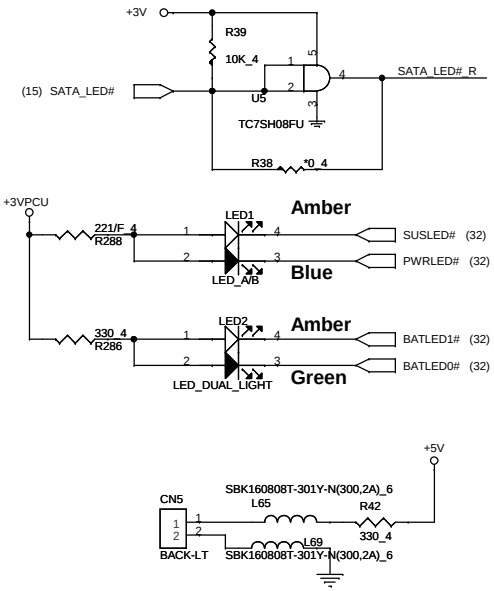


29

HOLES

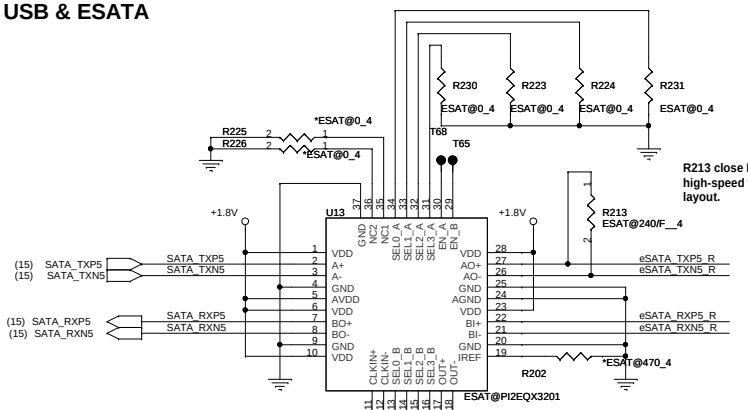


LED

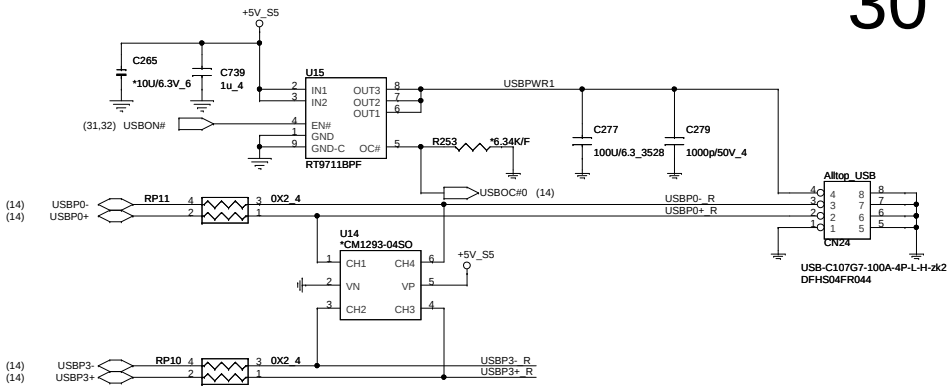


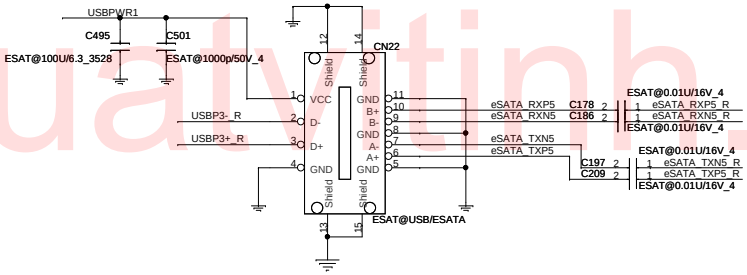
Quanta Computer Inc.		
PROJECT : ZK3		
Size	Document Number	Rev
	POWER/MMB/LAUNCH/LED	1A
Date: Monday, August 18, 2008	Sheet 29 of 43	

USB & ESATA

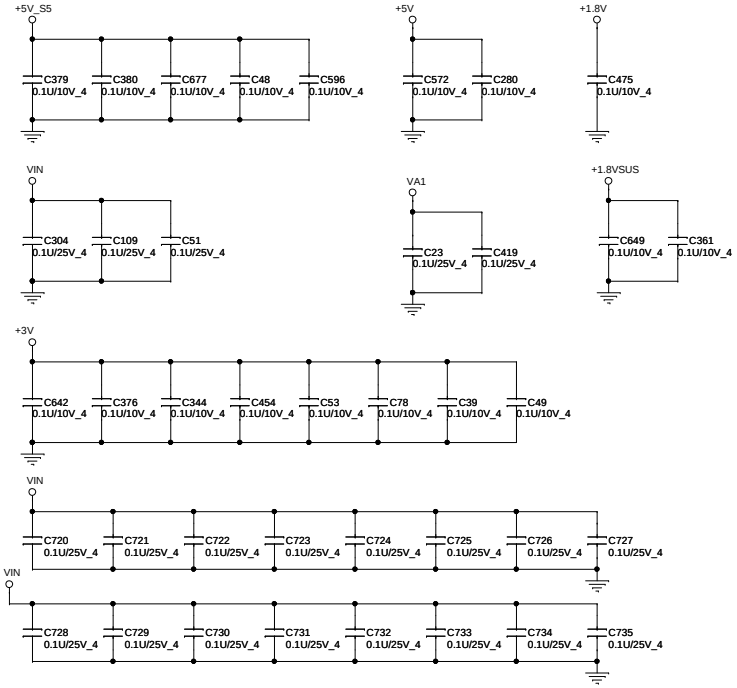


SEL0_X	SEL1_X	Eq	SEL2_X	Swing	SEL3_X	De-Emphasis
0	0	0dB	0	1.0X	0	0dB
0	1	2.5dB	1	1.2X	1	-3.5dB
1	0	4.5dB				
1	1	6.5dB				

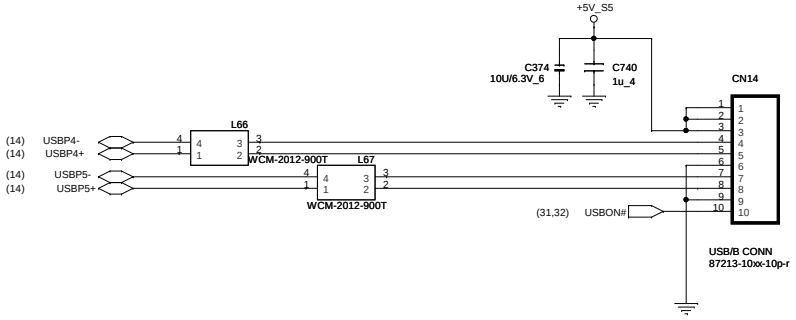




EMI cap



USB/B



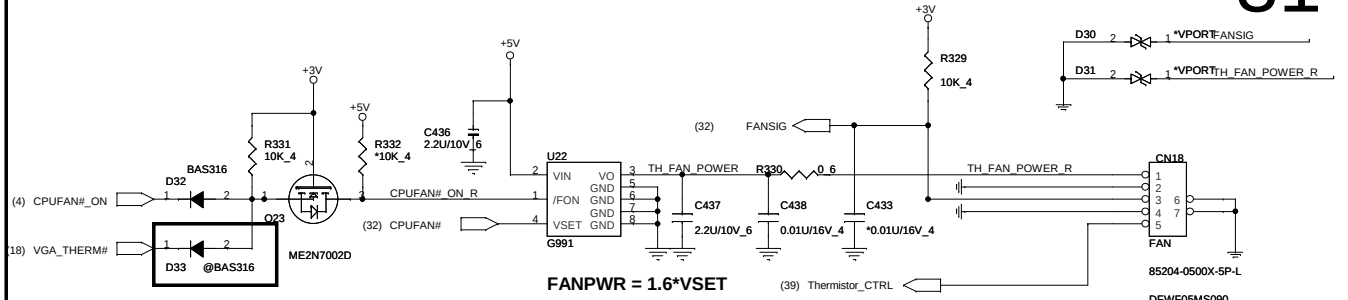
Quanta Computer Inc.

PROJECT : ZK3

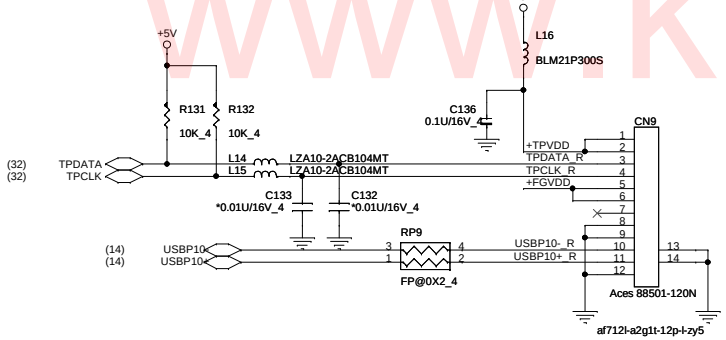
Size	Document Number	Rev
	USB	1A
Date: Monday, August 18, 2008	Sheet 30 of 43	

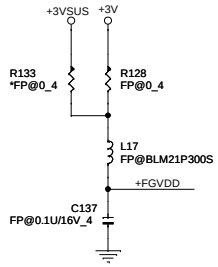
INT K/B

CPU FAN



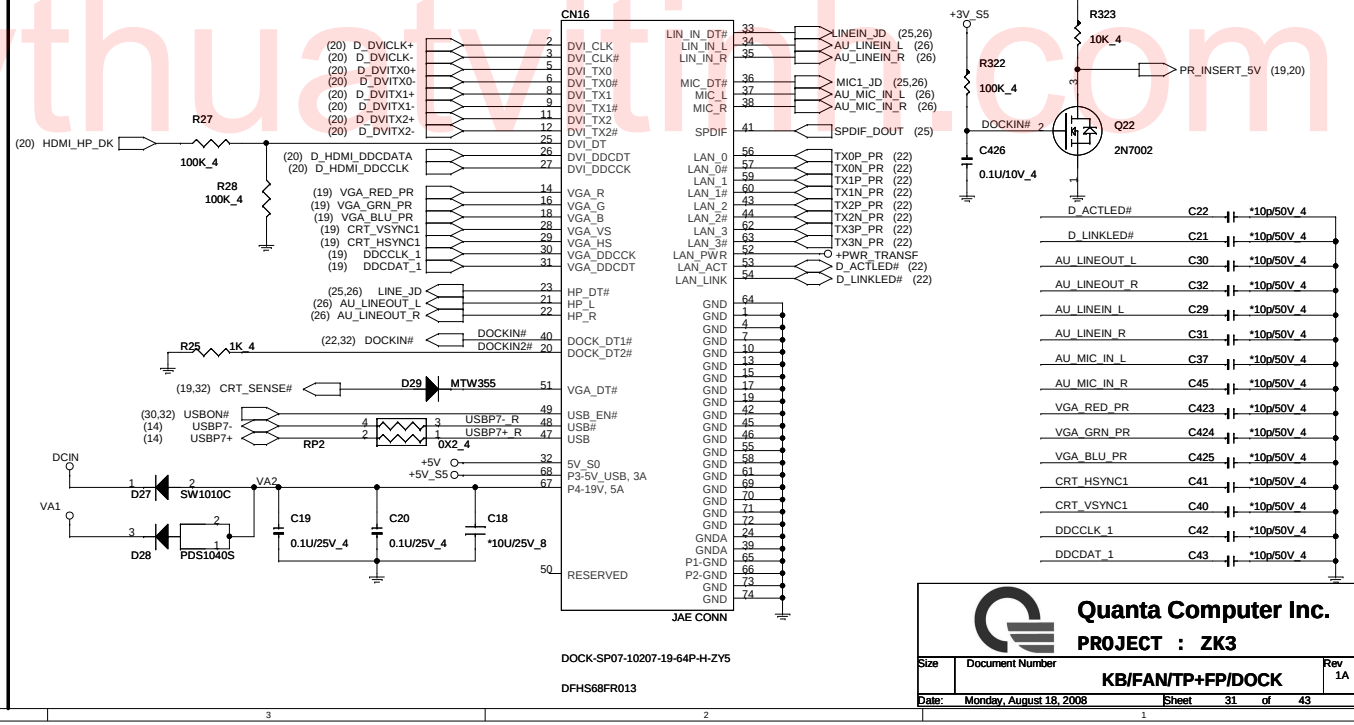
TOUCHPAD & Finger Printer CONN.





CABLE DOCK

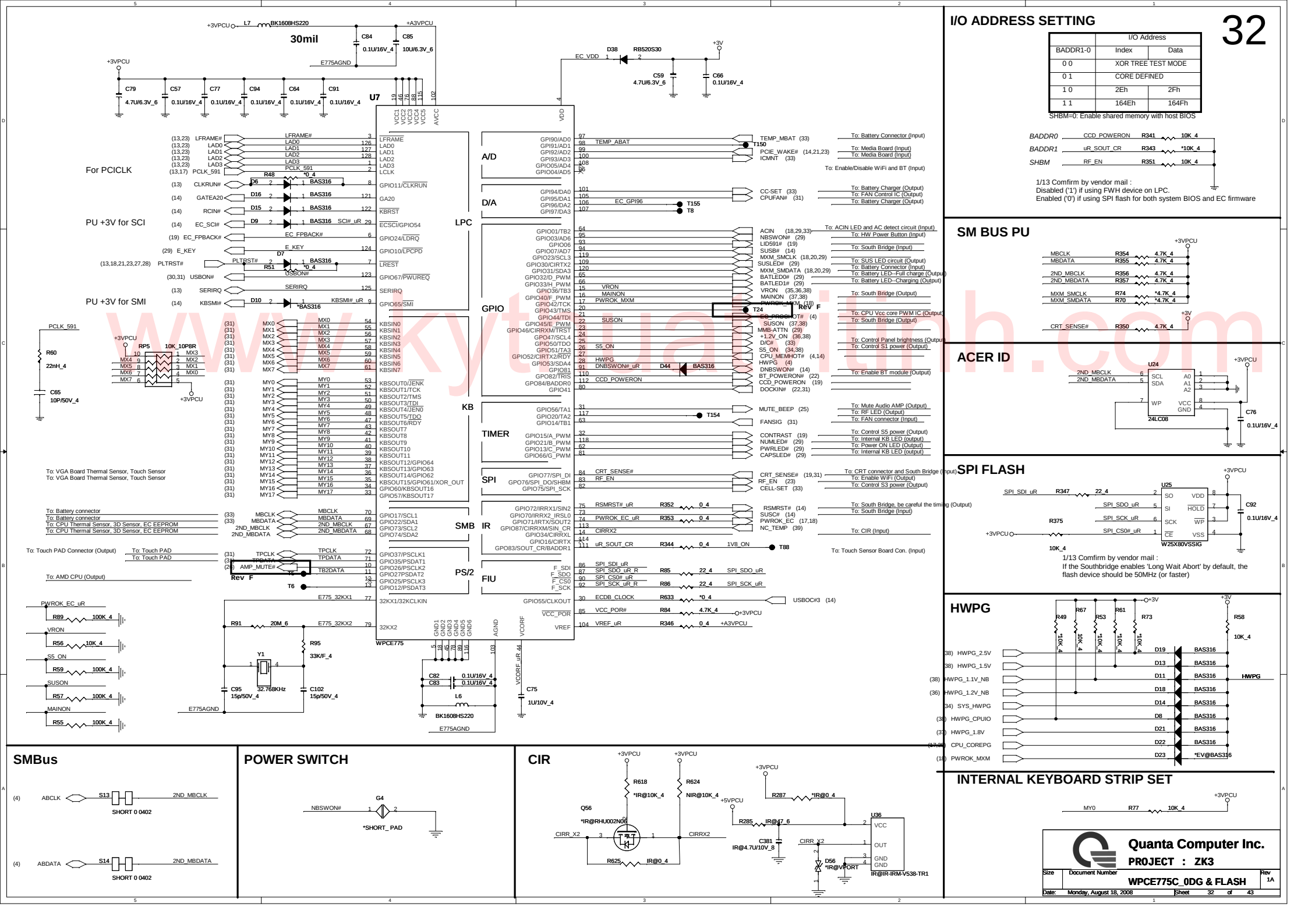
C test (update PN)



Quanta Computer Inc.
PROJECT : ZK3

Size	Document Number	Rev
	KB/FAN/TP+FP/DOCK	1A

Date: Monday, August 18, 2008 Sheet 31 of 43



I/O ADDRESS SETTING

BADDR1-0	I/O Address	
	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

SM BUS PU

ACER ID

SPI FLASH

1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

HWPG

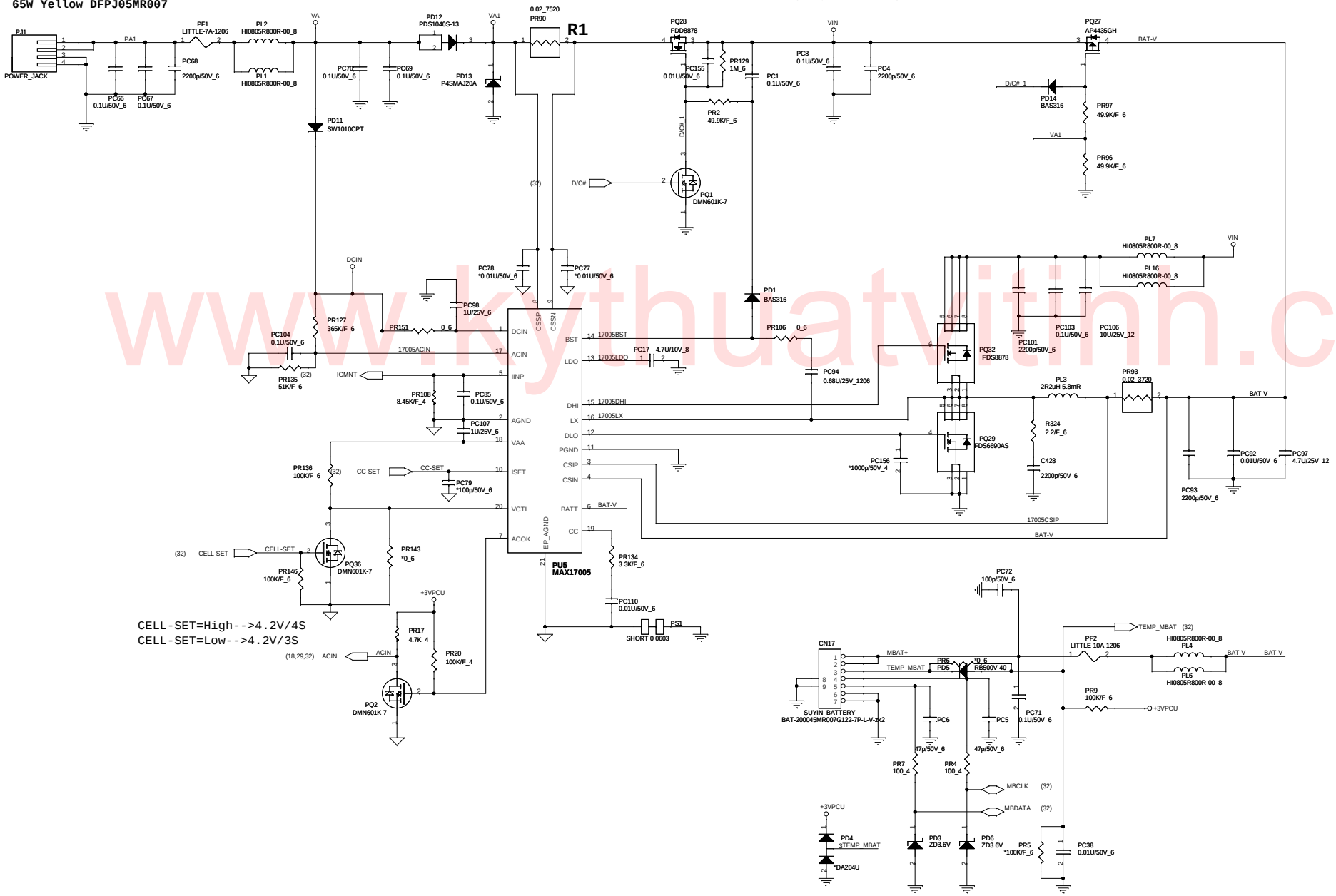
INTERNAL KEYBOARD STRIP SET

SMBus

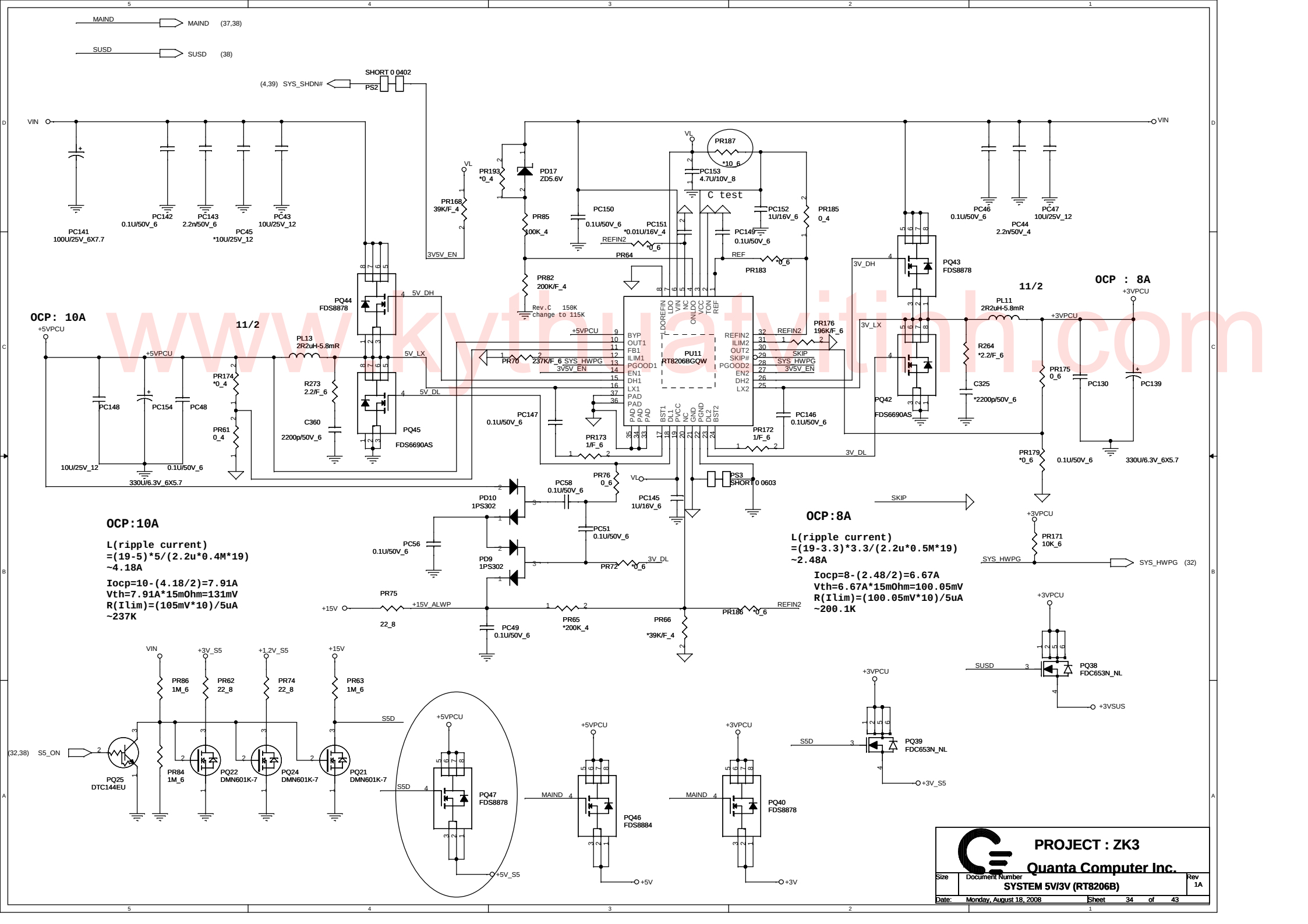
POWER SWITCH

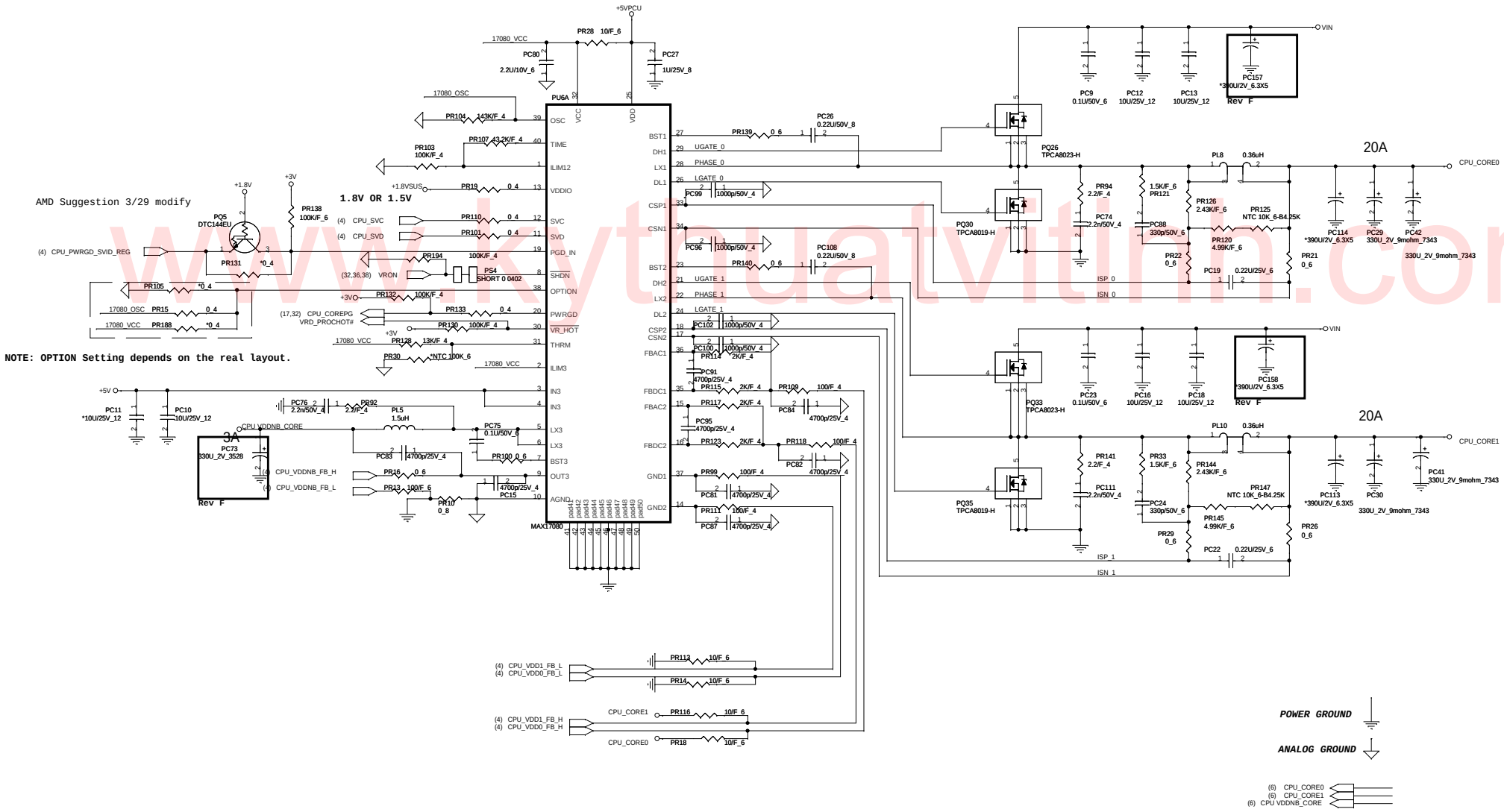
CIR

Quanta Computer Inc.			
PROJECT : ZK3			
Size	Document Number	WPCE775C_0DG & FLASH	Rev 1A
Date: Monday, August 18, 2008		Sheet 32 of 43	

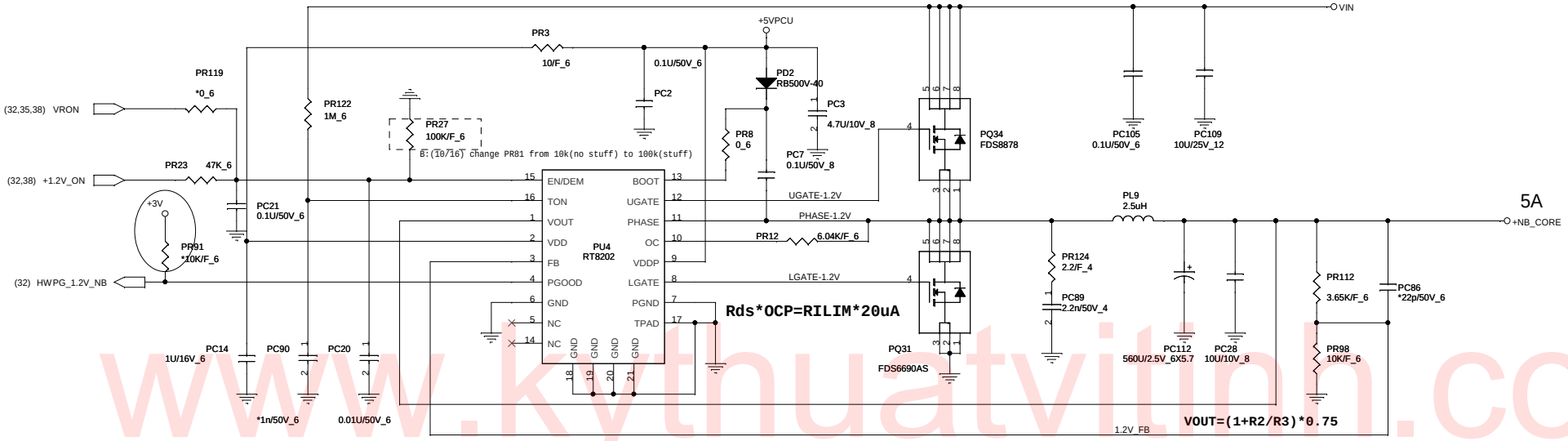


PROJECT : ZK3		
Quanta Computer Inc.		
Size: C	Document Number: CHARGER (MAX17005)	Rev: 1A
Date: Monday, August 18, 2008	Sheet 33 of 43	





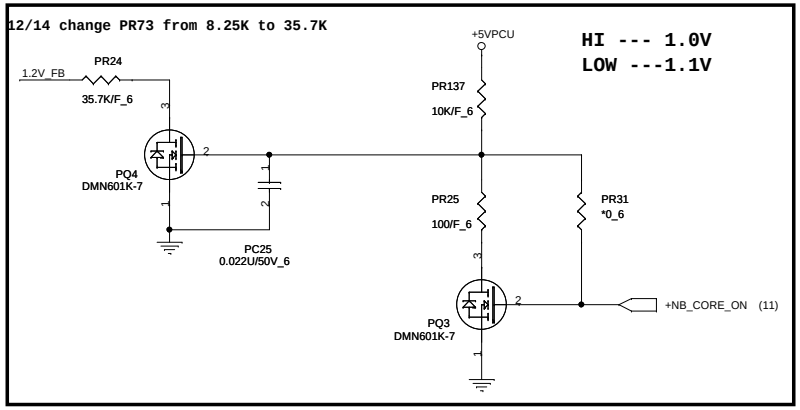
PROJECT : ZK3		
Quanta Computer Inc.		
Size: C	Document Number: MAX17080 CPU	Rev: 1A
Date: Monday, August 18, 2008	Sheet 35 of 43	

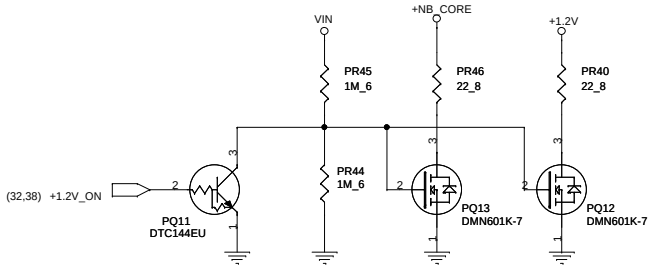


TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

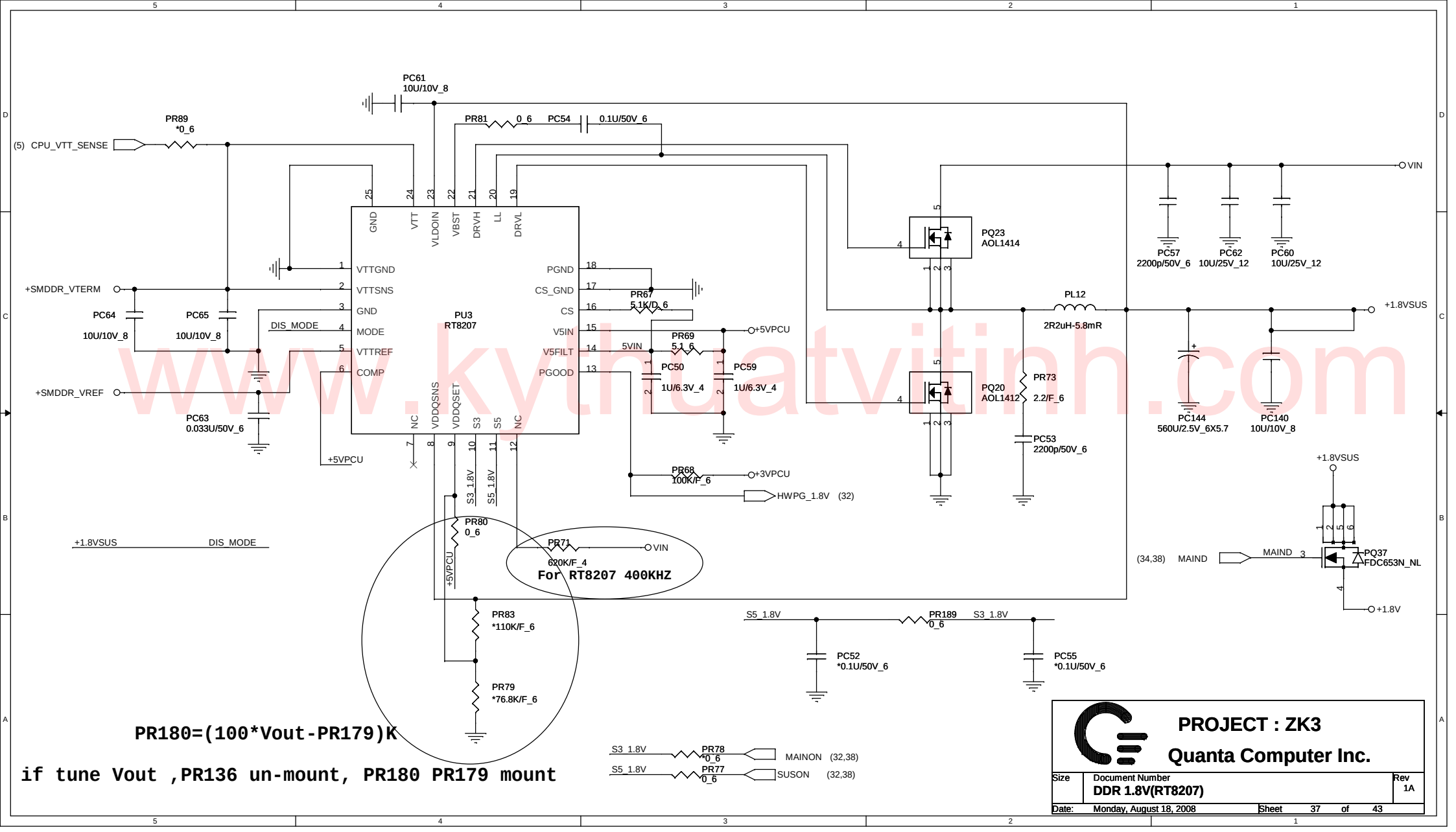
6A OCP --- OC=4.53K
FDS6690AS Rds=15mOhm



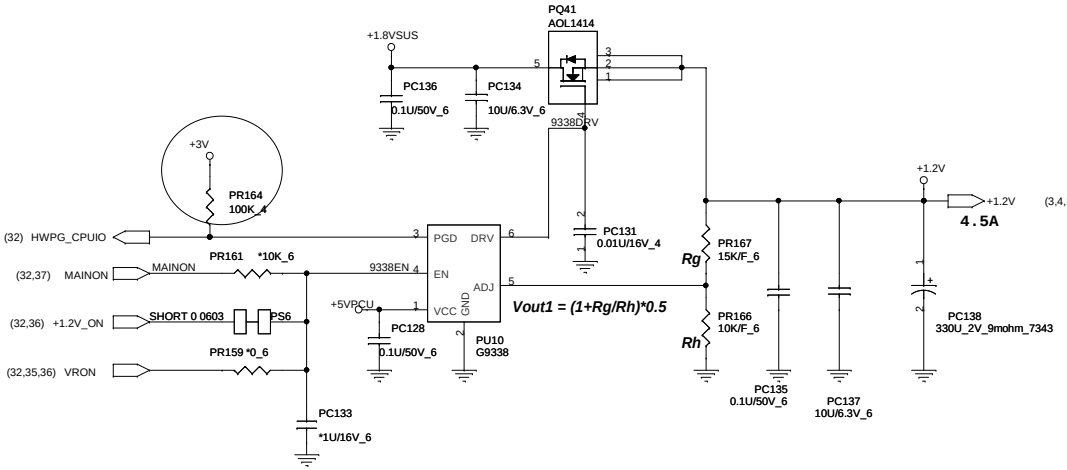


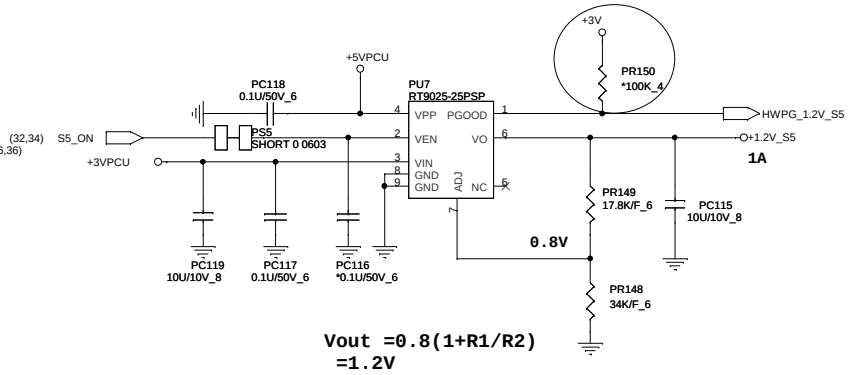
PROJECT : ZK3
Quanta Computer Inc.

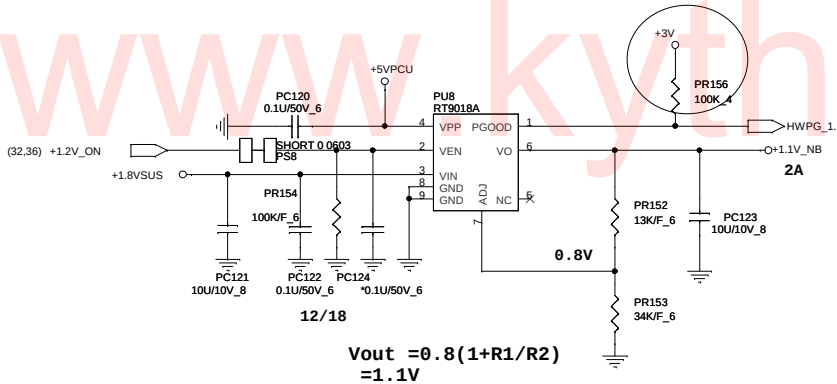
Size	Document Number	Rev
	NB_VCC (RT8202)	1A
Date: Monday, August 18, 2008	Sheet 36 of 43	

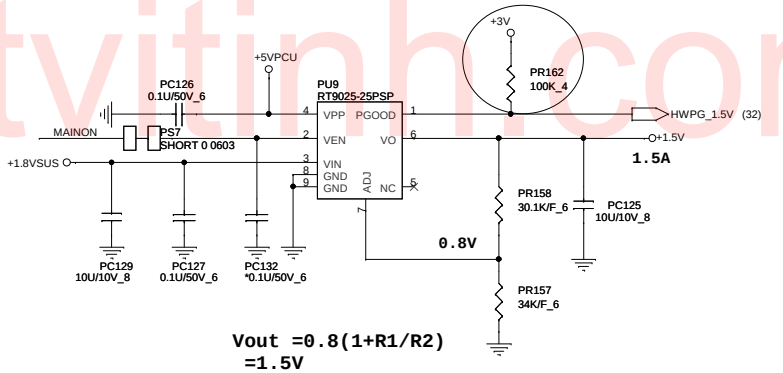


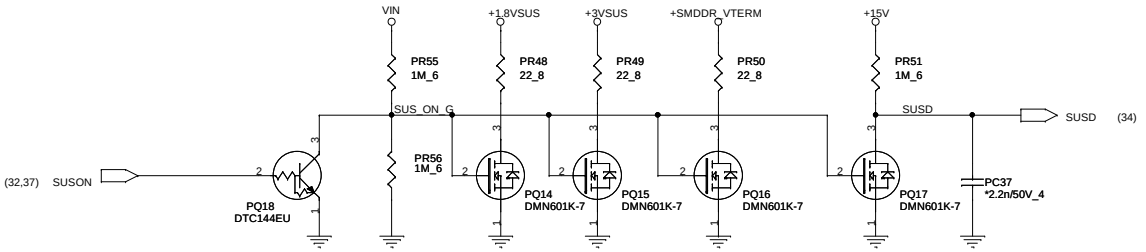
PROJECT : ZK3		
Quanta Computer Inc.		
Size	Document Number: DDR 1.8V(RT8207)	Rev: 1A
Date: Monday, August 18, 2008	Sheet 37 of 43	

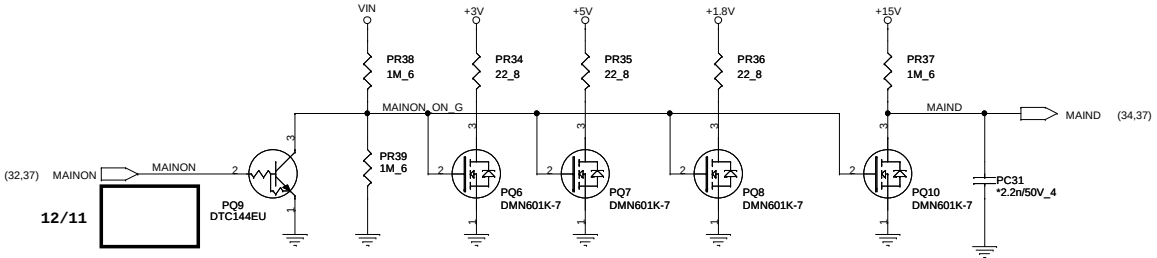


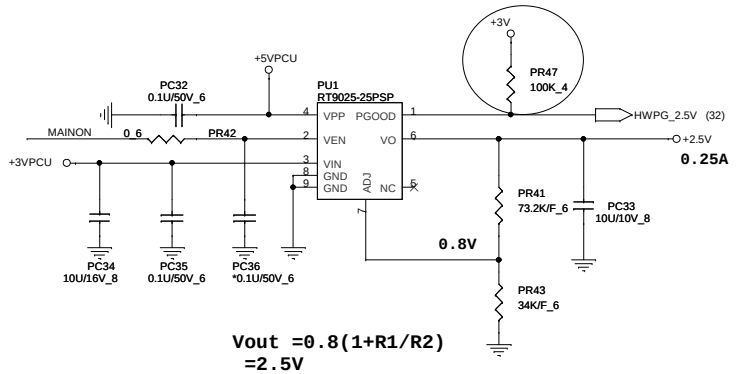










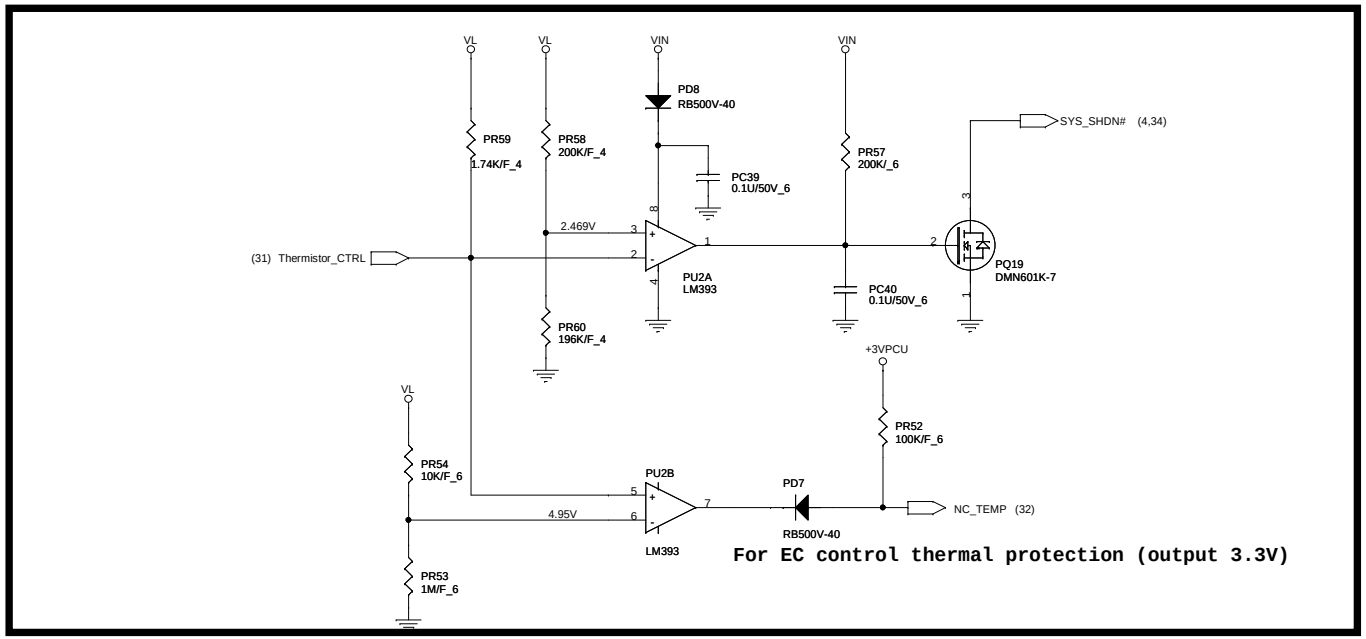


PROJECT : ZK3

Quanta Computer Inc.

Size	Document Number	Rev
	Discharge (1.25V/1.5V)	1A
Date: Monday, August 18, 2008	Sheet 38 of 43	

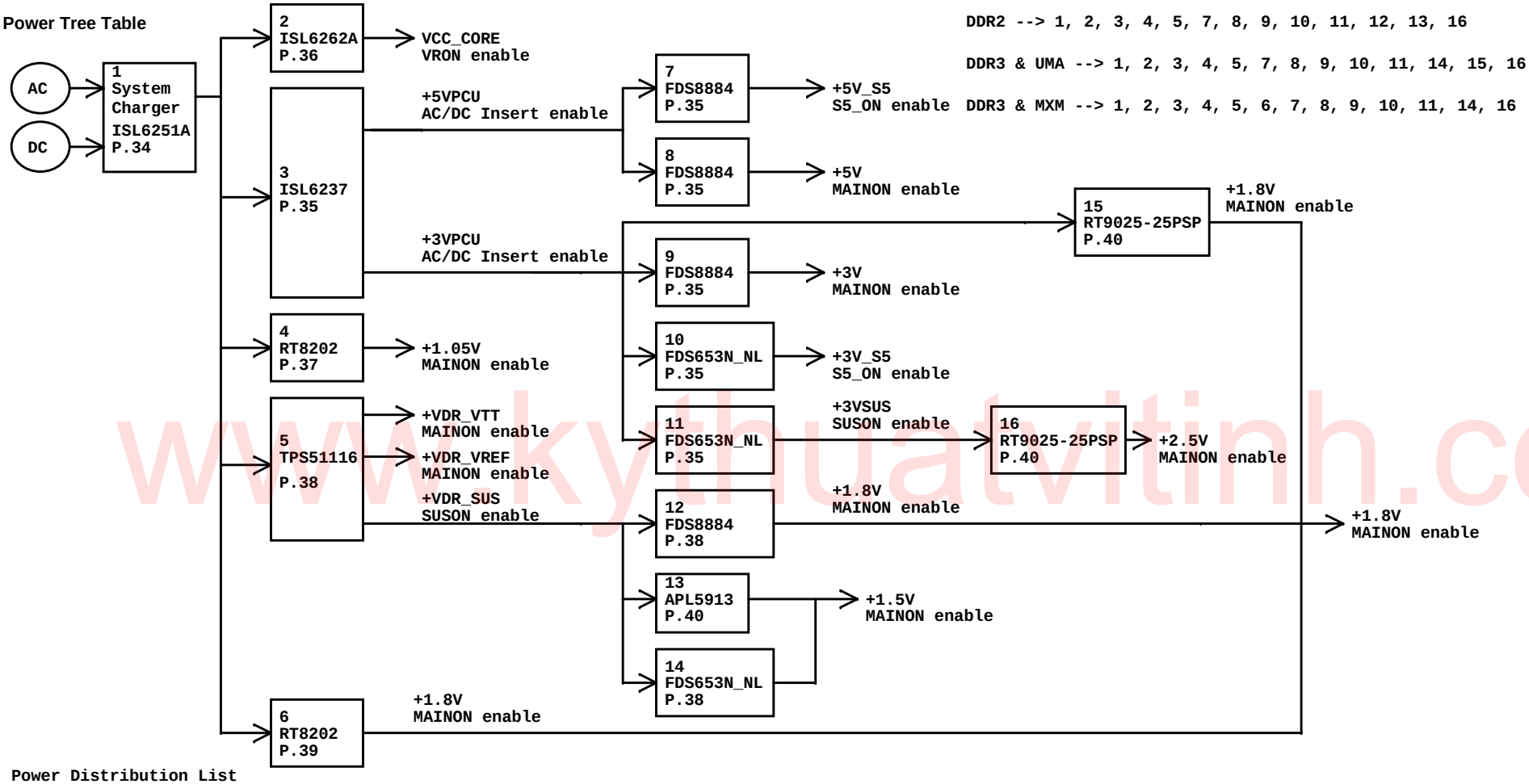
thermal protection --0928



For EC control thermal protection (output 3.3V)

PROJECT : ZK3		
Quanta Computer Inc.		
Size	Document Number: Thermal Protection	Rev: 1A
Date: Monday, August 18, 2008	Sheet 39 of 43	

Power Tree Table



Power Distribution List

Power	Distribution
VCC_CORE	CPU
+5VPCU	ICH8M, RJ45/USB /B, USB/eSATA, Satellite LED, CIR
+3VPCU	RTC, HALL SENSOR, KB, TP/FP/LED /B, Power /B, Kill SW, EC, ID, SPI Flash, CIR
+1.5V	CPU, GMCH, ICH9M, Mini Card, New Card
+VDR_SUS	GMCH, DDR
+VDR_VREF	GMCH, DDR
+VDR_VTT	DDR
+1.05V	CPU, CLK, Thermal Trip, GMCH, ICH8M
+5V_S5	ICH8M, G-SENSOR, Felica, USB/eSATA
+5V	CPU, ICH8M, VGA, Camera, CRT, HDMI, SATA HDD, PATA ODD, PCMCIA, TP/FP/LED /B, EC, Speaker, Headphone
+3V	CLK, CPU Thermal Monitor, FAN, GMCH, DDR, ICH8M, VGA, LCD/LED Panel, HALL SENSOR, CRT, HDMI, SATA HDD, PATA ODD, PCMCIA, Cardreader (OZ129T) Mini Card, KB, TP/FP/LED /B, RJ45/USB /B, Bluetooth, MMB, New Card, PC BEEP, EC, Codec (CX20561), VR, Headphone, MDC
+3V_S5	ICH8M, Mini Card, RJ45/USB /B, New Card
+3VSUS	ICH8M, FP
+1.8V	Cardreader
+2.5V	MXM

Quanta Computer Inc.
PROJECT : ZK3
Size | Document Number | Rev 1A
Power Tree Table
Date: Monday, August 18, 2008 | Sheet 40 of 43

CHANGE LIST

Model	REV		MODEL	ZK3 FROM	ZK3 To
ZK3 MB	A1A	FIRST RELEASED: E200804-2783 (PCB:)		X	1A
	A1A			X	1A

SMT inner document
1.Add RTC BATT (AHL03001401).
2.Del CRT BKT (FBZK1002010) (Material shortage)
3.Del CPU BKT (FBZK2010010) (Material shortage)
4.Page 38 : Change PC34,PC119,PC121,PC129 from CH6100KMEE3 to CH6103K9A00
5.Page 26 : Change C711,C712 from CH5103Z3905 to CH5104K9906
Change C675,C676 from CH41002KB93 to CH5103Z390
Change C683 from CH5222K9A09 to CH5103K9901
Change R612 from CS31002JB28 to CS41002JB20
6.Page 25 : Change C713 from CH11006J901 to CH11006K907
Change C650 from CH54702ZA38 to CH5472M9901
7.Page 21 : Change C405 from CH4103K1B08 to CH21006JB10.
Change C386,C8 from CH54702ZA38 to CH5471K9E07
Change R298 from CS21203F910(2.37K/F_6) to CS22372FB11(2.37K/F_4)
Change R8 from CS-1506J217 to CS00006J248
Change R3 from CS24702JB38 to CS31002JB28
8.Page 31 : Change C436,C437 from CH52202MA91 to CH5222K990
9.Page 20 : Change R374 from CS00006J248(0_12) to CS00002JB38(0_4)
10.Page 32 : Change U25 from AKE38ZP0N00 to AKE3GFP0N0
Change C95,C102 from CH01806JB07 to CH0156K0B06
Del R48,R51 (CS00002JB38)
Del R73,R61,R53,R49 (CS31002JB28)
Change C75 from CH5102M9B07 to CH5102K9B06
11.Page 35 : Change PR99, PR109, PR111, PR118 from CS41002FB28 to CS11002FB22
Change PR138 from CS31003J941 to CS41003F932.
Change PC88,PC24 from CH1336K1911 to CH13306K911. (Material shortage)
Change PR107 from CS34322FB16 to CS34302FB17. (Material shortage)
12.Page 09 : Change U26 from AJ067400T18 to AJ067400T2. (Material shortage)
13.Page 30 : Change C419,C23 from from CH41002KB93 to CH4104K9B03
14.Page 22 : Change R291,R301 from CS12204JA44(220_8) to CS12203J947(220_6)
15.Page 34 : Add PR171 (CS31003J941)
16.Page 33 : Change PQ28 from BAM88780011 to BAM62T00000. (Material shortage)
17.Page 29 : Change HOLE13,HOLE23,HOLE24 from MBZA1001012 to MBZK3001010
18.Page 28 : Change C365 from CH41003ZB35 to CH5102K9B06
19.Page 36 : Change PR3 from CS01003J953 to CS01003F93
20.Page 20 : R93 from CS00002JB38 to CS21002JB34
21.Page 19 : Change R47 from CS00006J248(0_12) to CS00002JB38(0_4)
Change L1,L2 from CX8BA220007 to CS00003J951
Add R35 (CS41002JB20)
Change C378 from CH5102M9B07 to CH5102K9B06

Below item for UMA sku only
22.Page 25 : Del R281 (CS00003J951)
Add R79 (CS41002JB20)
23.Add CN3 (DFWF40MS000) Add CN1,CN5,CN6 (DFHD02MR311)
Add CN4,CN7,CN9 (DFFC12FR234) Add CN11 (DFHD05MRD98)
Add CN2 (DFWF04MS079) Add CN12 (DFHS12FS734)
Add CN10 (DFHS26FR001) Add CN13 (DFHD02MS784)
Add CN8 (DFFC26FR261)

Modify items for B test

1.Update PCB footrptin :
Page 27 : New Card CN10 change to Z05
Page 20 : HDMI CN20 change to TE1M
Page 30 : ESATA CN22 change to TE1M
Page 28 : CardReader CN33 change to Z05
2.Page 24 : Update HDD connector PN (CN30) form DFHS22FR072 to DFHS22FR101
3.Page 07 : Update DDR connector PN : CN26 form DGMK0005791 to DGMK0005856, CN29 from DGMK0005627 to DGMK0000028
2008/0422
4.Page 29 : Del 3 EMIPAD. (EMIPAD197x134*2pcs, EMIPAD217x157*1pcs)

Quanta Computer Inc.
PROJECT : ZK3
Size | Document Number: Change list | Rev: 1A
Date: Monday, August 18, 2008 | Sheet 41 of 43

DOC NO.	PROJECT MODEL :	ZK3	APPROVED BY:		DATE:	2008/ 4/21
	PART NUMBER:		DRAWING BY:		REVISON:	1A

CHANGE LIST

Model	REV	
ZK3 MB		Modify items for B test 5.Page 20 : Change R374 from 0402 to 1206 size. Del Q34,Q35,Q38. 6.Page 19 : Change R47 from 0402 to 1206 size. 7.Page 21 : Change R298 from 0603 to 0402 size. Connect C3, R6 from U20.pin5 to U20.pin 42 and stuff C3, R6. 8.Page 22 : Change R291, R301 from 0805 to 0603 Del R306,R307 due to haven't LAN GND. Change LAN connector(CN15) differential pair routing. 9.Page 32 : Connect U7.98 pin to test point Connect D56 to U36.1 pin. Reserve R632 at U7.106pin, R633 at U7.30pin 2008/0423 10.Page 29 : Add R634,R635 to reserve +3VPCU and +3V power for MMB board 2008/0424 11.Page 15 : Modify U28.P5, U28.P8, U28.R8 net name and connect to Test point. 12.Page 29 : Update screw hole. 2008/0428 13.Page 38 : Change PR167 from 14K to 15K to modify 1.2V power rail. 14.Page 24 : Add ESD diode(U37,U38) at CN27,CN30. 15.Page 25 : Remove R626. (+1.5V) ; Remove R281(+1.5V_S5) 16.Page 26 : Update CN25(HP connector) pin definition ; Add R626 17.Page 19 : Change C33 from 0402(0.1u) to 0603(2.2u) 2008/0429 18.Page 29 : Change R634,R635 from 0402 to 0603 19.Page 30 : Remove U18,R282,C701,C373 and C375 ; Connect USBON# net to CN14 pin10. 20.Page 35 : Remove PR105 and mount PR15 for CPU issue 22.Page 38 : Change PC138 size for height limited issue 23.Page 35 : Reserve PR188. 24.Page 30 : Update U13 footprint (increase pad size) for SMT request. 25.Page 19 : Update CN19 footprint for SMT request. 26.Page 37 : Add PR189 27.Page 22 : Update U3 footprint for SMT request 28.Page 13 : Add R281. 2008/0430 29.Page 18 : Add R636 30.Page 20 : Connect R90 to HPD_SRC net. 31.Page 15 : Change C182 to 22p. 32.Page 21 : Change C412, C413 to 33p. 2008/0501 33.Page 19 : Change R35 from 100K to 4.7K.(Refer demo board) 34.Page 13 : Add R141. 35.Page 28 : Update CN33 PN for SMT issue. 36.Page 32 : Uninstall D23.	
		B test SMT inner document	

MODEL	ZK3	
	FROM	To
	X	1A
	X	1A

Quanta Computer Inc.
PROJECT : ZK3
Size | Document Number: Change list | Rev: 1A
Date: Monday, August 18, 2008 | Sheet 42 of 43

DOC NO.					
PROJECT MODEL :	ZK3	APPROVED BY:		DATE:	2008/ 4/21
PART NUMBER:		DRAWING BY:		REVISON:	1A

Model	REV	CHANGE LIST	MODEL	ZK3	
				FROM	To
				X	1A
				X	1A

ZK3 MB

Modify items for C test

01.Remove JP1~JP9.

02.Page03：Reserve R640,R641 for SB A13 version ：Change Y6 to BG614318F33 for vendor recommend

03.Page04：Connect R160 to GND, R151 to +1.8VSUS (AMD design guide update)；Del R449(Reserve 0Ω)

04.Page11：Del R198, R199(Reserve 0Ω)；Change C172 to 10U.

05.Page13：Unmount R141, Reserve R642；Add T156, T157 test point；Del R484 and R527 (0Ω)

06.Page14：Remove some pull down resistor (R164, R158, R176, R452, R453, R172, R512, R513, R412, R397, R470)
Del R518,R239,R247,R236 and R384 (Azalia bus to MXM card)

07.Page15：Remove some pull down resistor (R480,R481,R229,R221,R222,R220,R471,R472,R474,R473,R475,R478,R235,R233,R232)

08.Page17：Change C88 to 1000pF, R81 to 4.7KΩ;unmount D36, R81;Mount R83.

09.Page19：Del R50,R68 and R69(Reserve 0Ω),Change R283 from 330Ω to 180Ω(Hall sensor issue)；Update HE1 footprint：
Add C736,C737,C738,L68. Del R23,R24(For EMI request)：Change CRT connector PN to DFDS15FR073：
Change L3,L4 and L5 to 47Ω bead, C72,C74,C58,C63,C73,C67 to 6.8p for UMA SKU

10.Page20：Update HDMI switch circuit；Change location R78-->S1,R65-->S2,R62-->S3；Del D40
Del R90,R378,R380,R383,R385,R388,R390,R393,R401,Q39,RP4,RP6~RP8,R111, R106,R414,R417,R419,Q36,Q37R381,R382,D38,D39(ND@)
Mount R318~R320 for EMI request

11.Page21：Del R2,R4；Change R298 to 2.32KΩ；Change R298 from 0402 to 0603 size；Change location R299-->S4,R11-->S5,R12-->S6

12.Page22：Swap LAN connector pin12 and pin10：Del C398 and connect CN15's pin13, 14 to GND：Change R18~R21 from 0402 to 0805：
Change R18~R21 from 0402 to 0805 for factory request：Del RN7~RN10,R9,R10：Change U3 to DBKN1NLAN03

13.Page23：Del R555,Change location R568-->S8,R450-->S7,R446-->S9

14.Page24：Swap SATA port0 and port1.Change U30 to DFHS22FR669.Change U27 to DFHS22FR116;

15.Page25：Change location R609-->S10

16.Page26：Remove D55 and D52；Change R546,R542 to 47Ω for vendor recommend；Change R604 to 12.4K to subwoofer gain

17.Page27：Change location R605-->S12,R608-->S11

18.Page28：Reserve R643,C717 for EMI request

19.Page29：Update power board's circuit.(Add Q60,Q58,Q59,Q57,R644,R645 and R646)
Update MMB board circuit(Add R647,R648,R650,Q61,R649,R638,R639：Add C719 for EMI request)
Add L65,L69,2 EMI PAD：Connect R42 to +5V：Del CN1,CN6：Connect HOLE18 to GND

20.Page30：Add R230,R223,R224,R231 to 0Ω,Add R213 to 240Ω for ESATA eye pattern issue.
Change CN22 to DFHS11FR025；Add L66,L67 for EMI request.Add C720~C735 for EMI request.

21.Page32：Change U7.117pin to be test point；Change location R44-->S12,R43-->S14；Add R60,C65 for EMI request.
Remove SW1.

22.Page33：Connect PR97 net from VA to VA1 for can't power on when docking attached and plug adaptor in docking side.
Del PR1；Del PR11,PR95；Change location PR142-->PS1;Add R324,C428 for EMI reqeust.

23.Page34：Change location PR184-->PS3,PR169-->PS2：PR180,PR177,PR178,PR170：Change PR182 from 150K to 115K

33.Page35：Del PR129；Change location PR102-->PS4
Add PR94,PC74,PR141,PC111 for EMI request.

34.Page36：Del PR32；Add PR124,PC89 for EMI request.

35.Page37：Del PR85,PR87,PR88,PR82；

36.Page38：PR160；Change location PR165-->PS6,PR163-->PS7,PR155-->PS8,PR151-->PS5

Modify items for C2 test

01.Page35：Add PL15,PL16 for EMI request.

Modify items for ramp

01.Page 04: Connect Q33.2 to HWPG for reboot shut down issue.

02.Page 11: Change C175 to 22u for improving UMA LCD flicker issue.

03.Page 18: Add C575 for improving UMA LCD flicker issue.

04.Page 19: Update U4 to AAT4280-4 to meet LCD power spec.

05.Page 22: Modify R291 and R301 from 0603 to 0805 for facotry request.

06.Page 23: Remove R544 and R538(0Ω)

07.Page 24: ADd U37,U38 for ESD issue.

08.Page 26: Change C685 (0.1u) to R652 (100K) for improving power comsuption;connecto D53 to EAPD# for audio power down noise.

09.Page 29: Change R648 and R288 to fine tune LED brightness；Modify LED1 PN to meet acer LED spec.

10.Page 31: Remove C60~C62,C68~C71 for unnecessary parts.

11.Page 32: Change RP5 pin5,10 from +3VSUS to +3VPCU for preventing EC enter debug mode

12.Page 33: Change CN17 to DFHD07MR059;Reserve PL16,PC155,PR129 for vendor recommend

Quanta Computer Inc.	DOC NO.	PROJECT MODEL :	ZK3	APPROVED BY:		DATE:	2008/ 4/21
PROJECT : ZK3		PART NUMBER:		DRAWING BY:		REVISON:	1A
Size / Document Number: Change list / Rev: 1A							
Date: Monday, August 18, 2008 / Sheet 43 of 43							