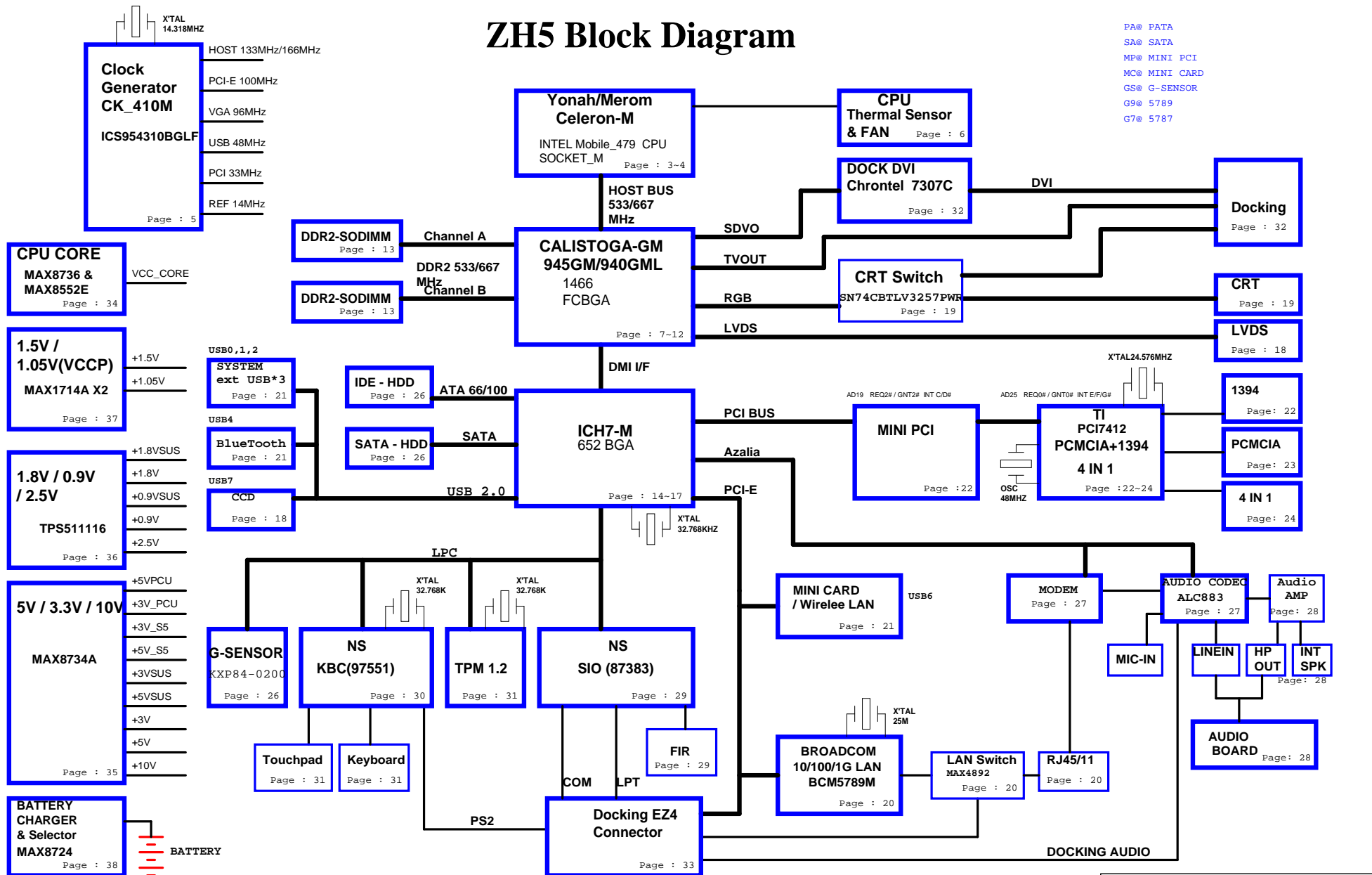


ZH5 Block Diagram

PA@ PATA
 SA@ SATA
 MP@ MINI PCI
 MC@ MINI CARD
 GS@ G-SENSOR
 G9@ 5789
 G7@ 5787



PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts
PCI7412	AD25	REQ0# / GNT0#	INT E/F/G#
MINI PCI	AD19	REQ2# / GNT2#	INT C/D#

PROJECT : ZH5
Quanta Computer Inc.

Size	Document Number	Rev
	BLOCK DIAGRAM	1A
Date:	Friday, September 06, 2006	Sheet 1 of 39

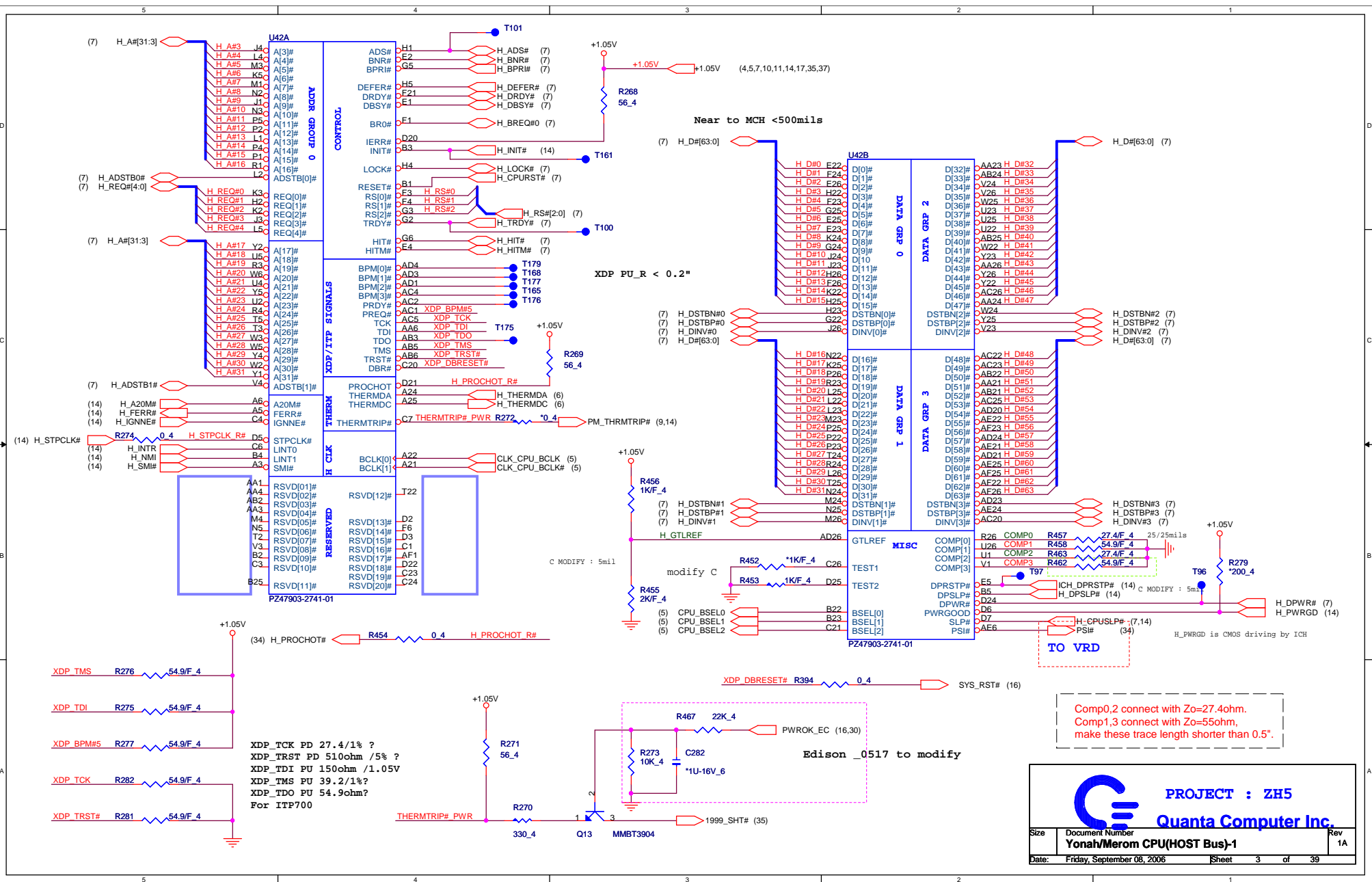
TABLE OF CONTENTS

Page 01 : BLOCK DIAGRAM
 Page 02 : TABLE OF CONTENTS
 Page 03 : Yonah/Merom CPU(HOST Bus)-1
 Page 04 : Yonah/Merom CPU(POWER/NC)-2
 Page 05 : CLOCK GENERATOR
 Page 06 : THERMAL SENSOR & FAN
 Page 07 : GMCH HOST Bus(1 of 6)
 Page 08 : GMCH DDRII MEMORY (2 of 6)
 Page 09 : GMCH DMI & VEDIO (3 of 6)
 Page 10 : GMCH POWER & STRAP(4 of 6)
 Page 11 : GMCH LVDS/DAC-PWR2 (5 of 6)
 Page 12 : GMCH GND (6 of 6)
 Page 13 : DDRII SO-DIMM & TERMINATOR
 Page 14 : ICH7-M RTC/SATA/IDE/AZALIA/CPU (1 OF 4)
 Page 15 : ICH7-M MDI/PCI E/PCI/USB (2 OF 4)
 Page 16 : ICH7-M GPIO/SMBus (3 of 4)
 Page 17 : ICH7-M POWER & GND (4 of 4)
 Page 18 : LVDS CONNECTOR & CCD
 Page 19 : CRT PORT
 Page 20 : GigaLAN BCM5787MKMLG & RJ45/RJ11
 Page 21 : PCMCIA /Mini Card /USB / Blue Tooth
 Page 22 : PCI7412-IEEE1394
 Page 23 : PCI7412-PCMCIA
 Page 24 : PCI7412-CARD READER
 Page 25 : HOLES
 Page 26 : SATA/PATA HDD /G SENSOR
 Page 27 : CODEC ALC883 & MDC
 Page 28 : AUDIO AMP & SPEAK/LIN OUT
 Page 29 : SIO (87383)
 Page 30 : EC Controller PC97551 & FLASH
 Page 31 : SWITCH,LED,KB,TP,TPM1.2,EMI PAD
 Page 32 : DOCK DVI CH7307C
 Page 33 : DOCK EZ4 CONNECTOR
 Page 34 : CPU CORE (MAX8736ETL+)
 Page 35 : SYSTEM +5V/+3V(MAX8734A)
 Page 36 : DDRII POWER 1.8VSUS / 0.9VTERM
 Page 37 : CHIPSET POWER +1.5V / VCCP(+1.05V)
 Page 38 : BATTERY CHARGER & SELECTOR

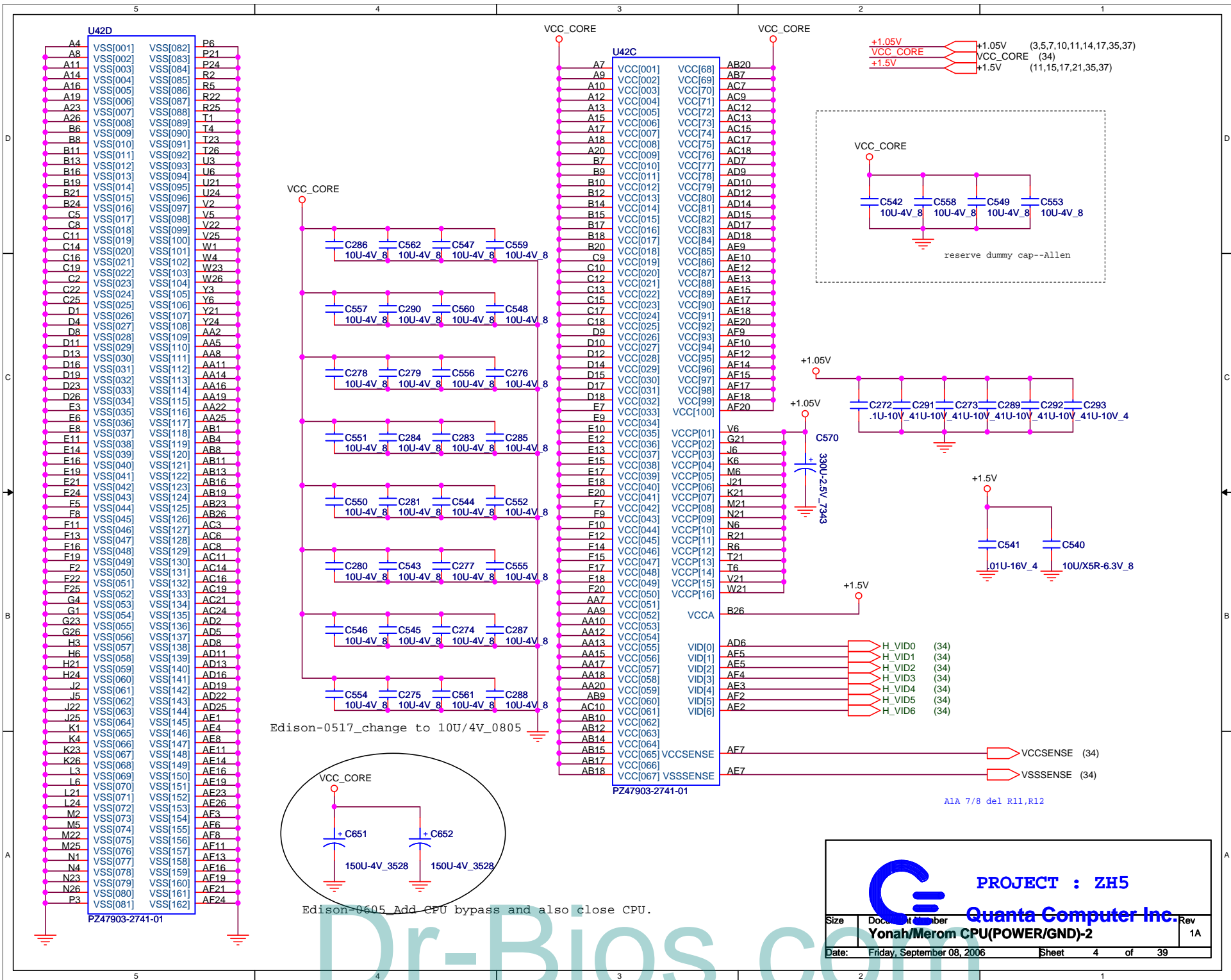


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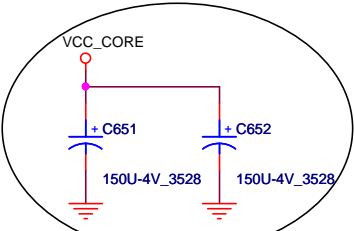
Size	Document Number	Rev
	TABLE OF CONTENTS	1A
Date:	Friday, September 08, 2006	Sheet 2 of 39



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Edison-0517_change to 10U/4V_0805



Edison-0605 Add CPU bypass and also close CPU.

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Yonah/Merom CPU(Power/GND)-2

Size	Docu	Number	Rev
			1A
Date:	Friday, September 08, 2006		Sheet 4 of 39

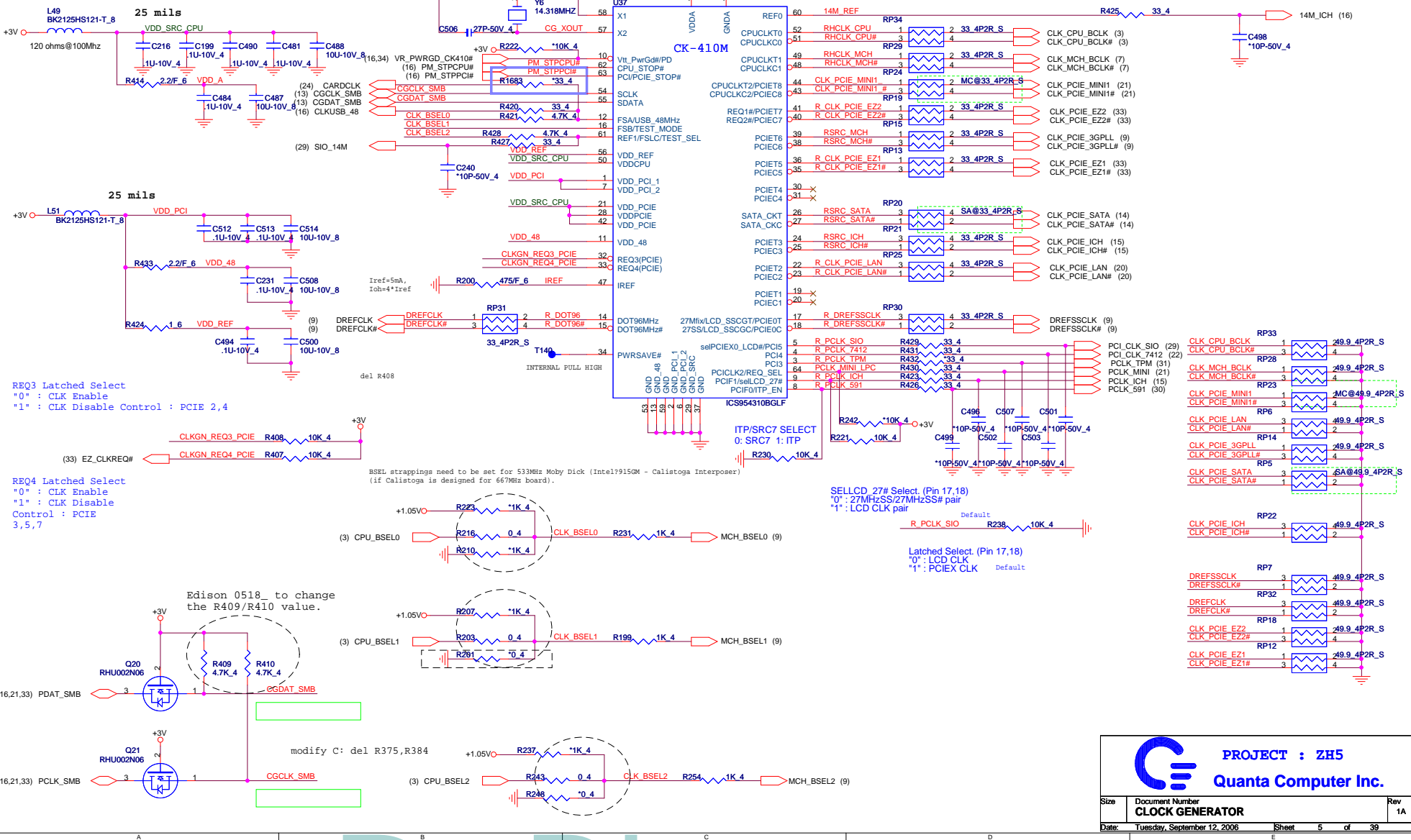
Dr-Bios.com

FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	200	100	33

Default

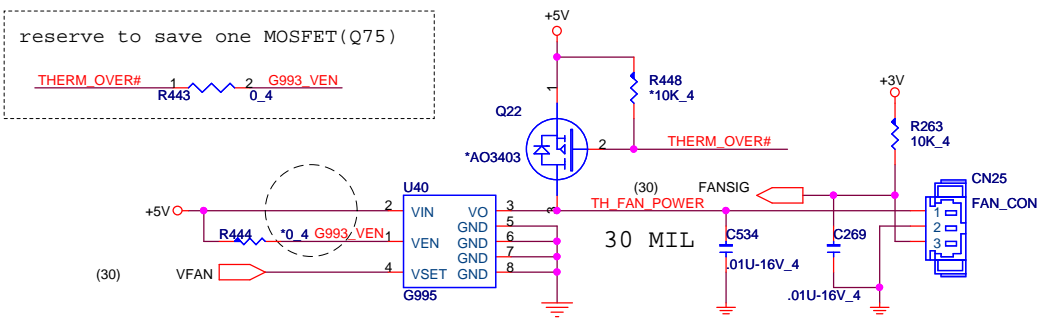
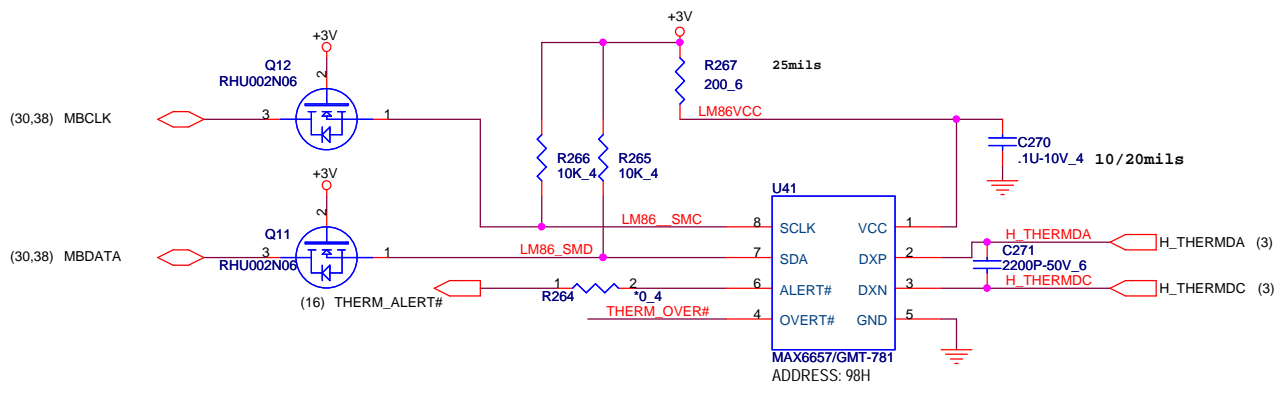
Close to IC <500mils

Place these termination to close CK410M.



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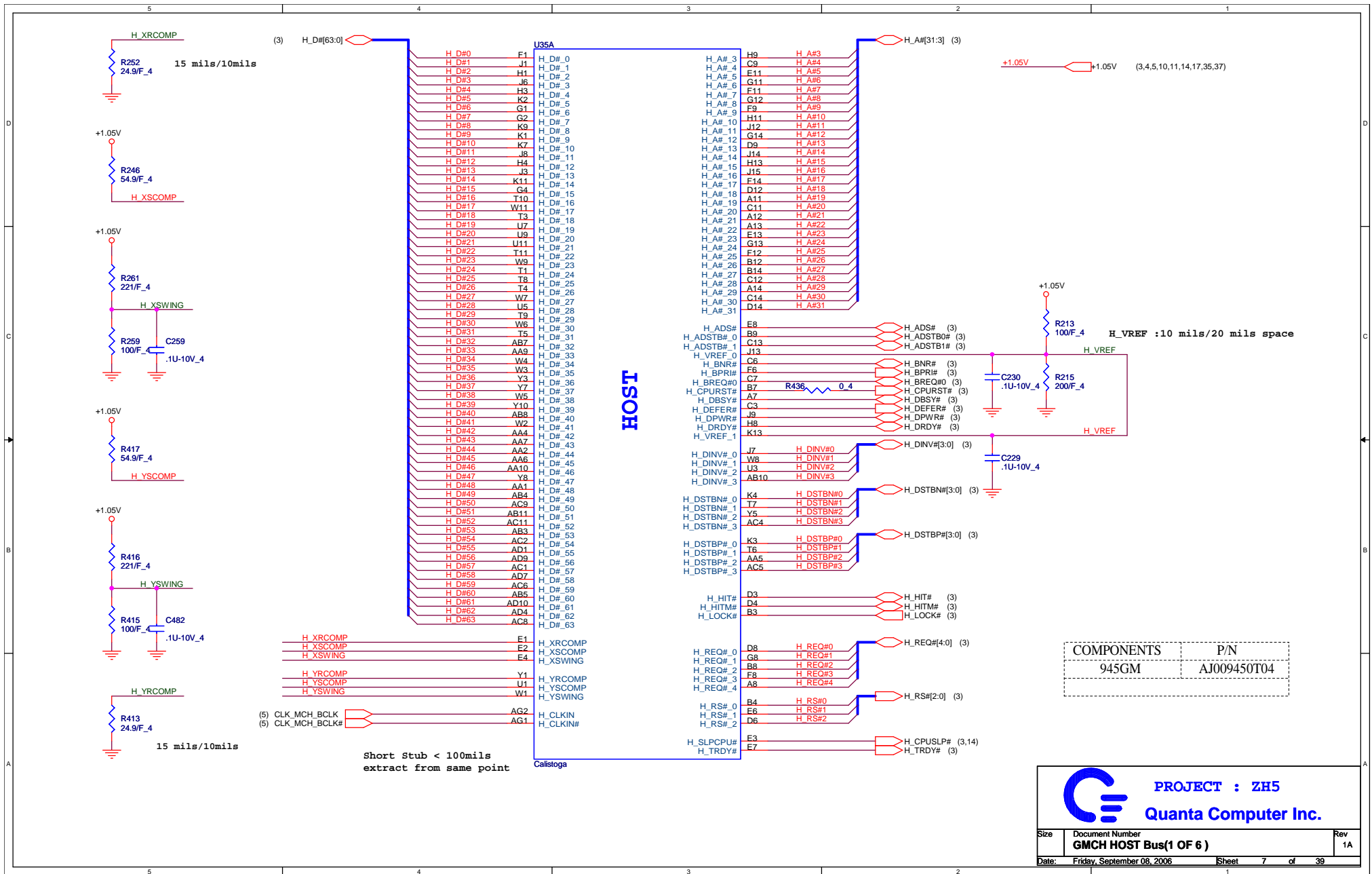
Size	Document Number	Rev
CLOCK GENERATOR		1A
Date:	Tuesday, September 12, 2006	Sheet 5 of 39



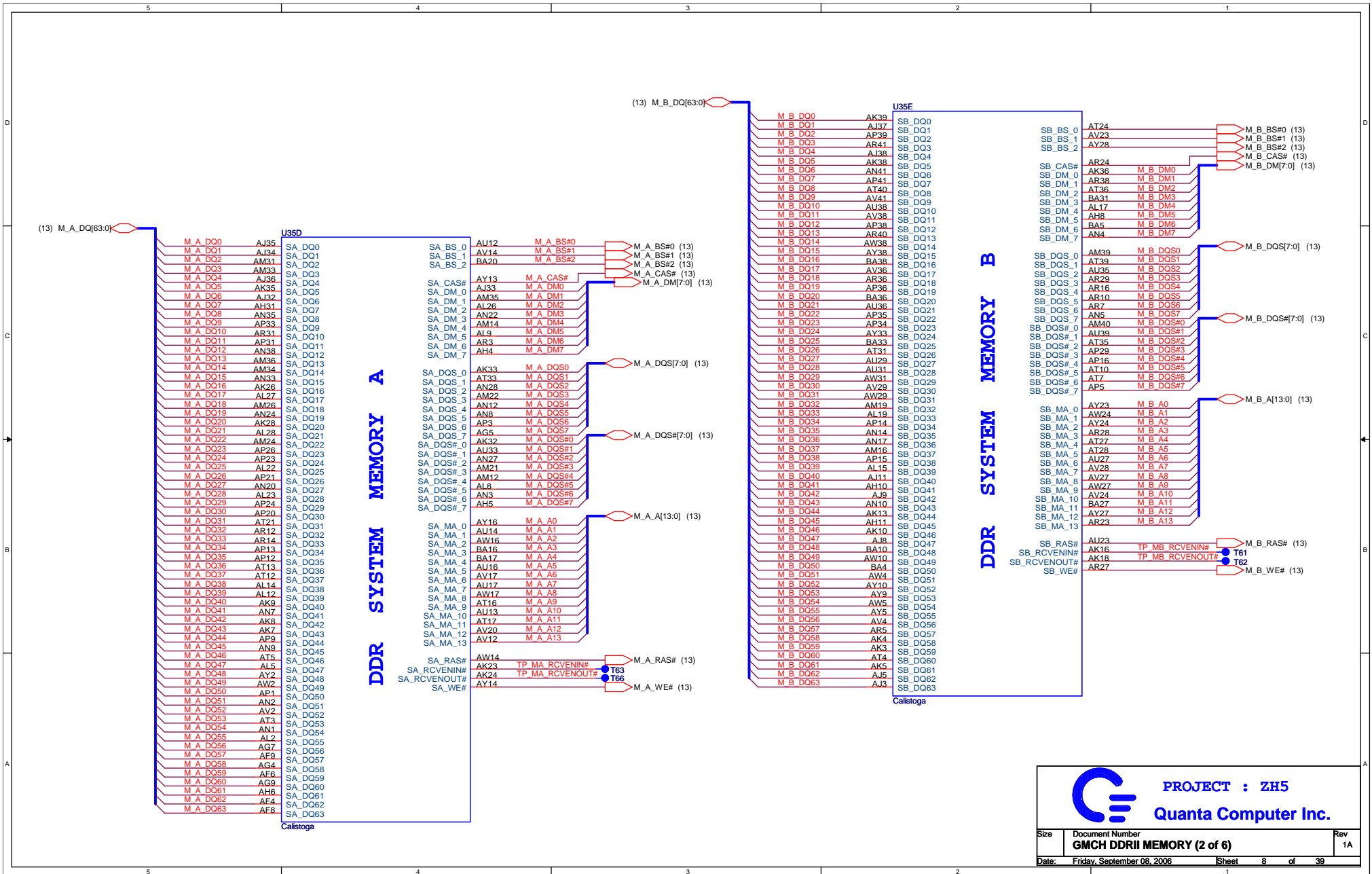
PROJECT : ZH5
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Size	Document Number	Rev
	CPU THERMAL SENSOR & FAN	1A
Date:	Friday, September 08, 2006	Sheet 6 of 39

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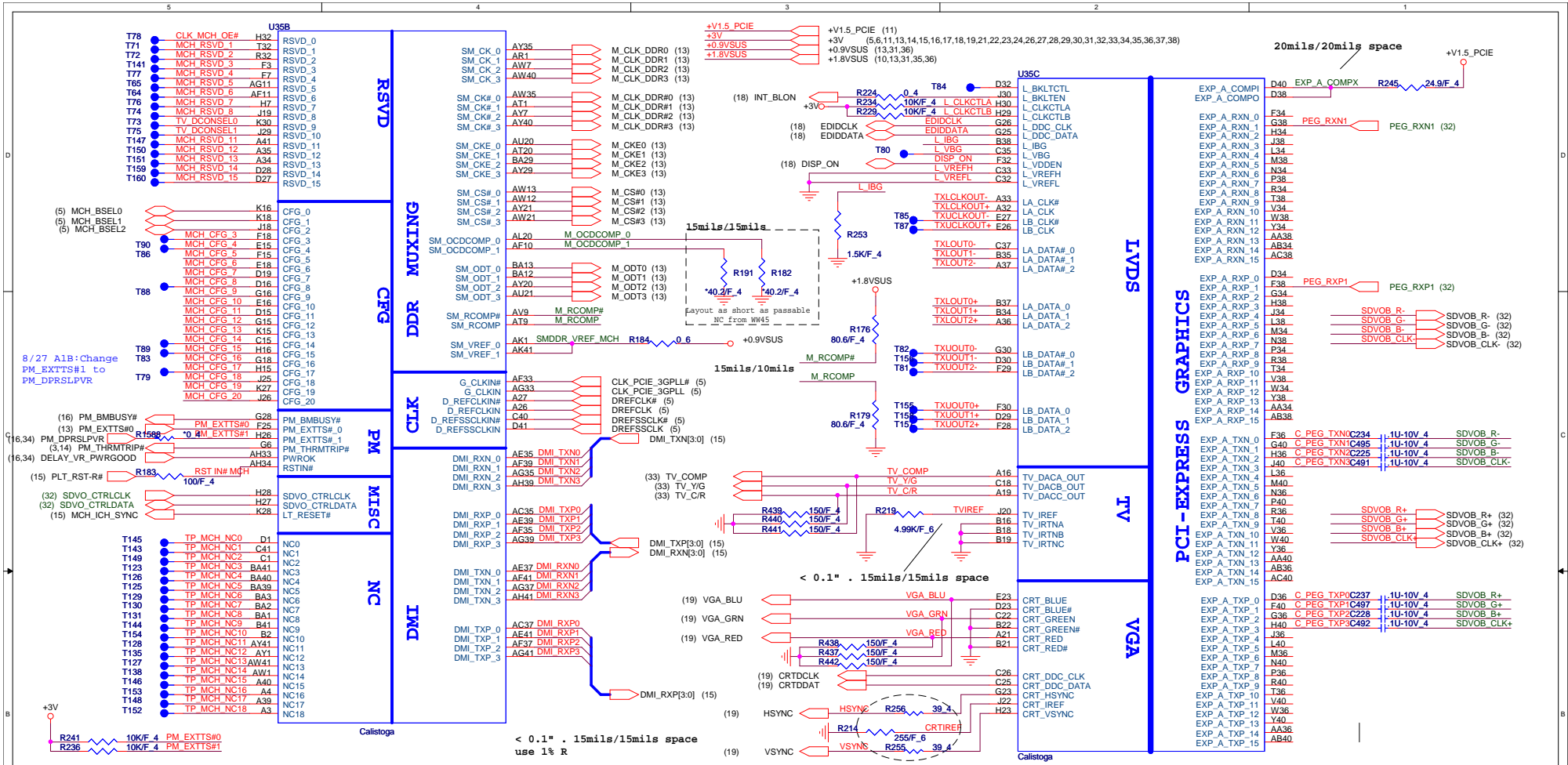


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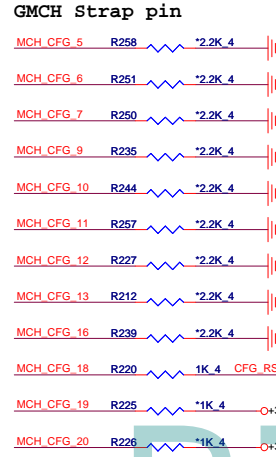
Size	Document Number	Rev
	GMCH DDRII MEMORY (2 of 6)	1A
Date:	Friday, September 08, 2006	Sheet 8 of 39



8/27 A1B:Change PM_EXTTSH1 to PM_DPRSLPVR

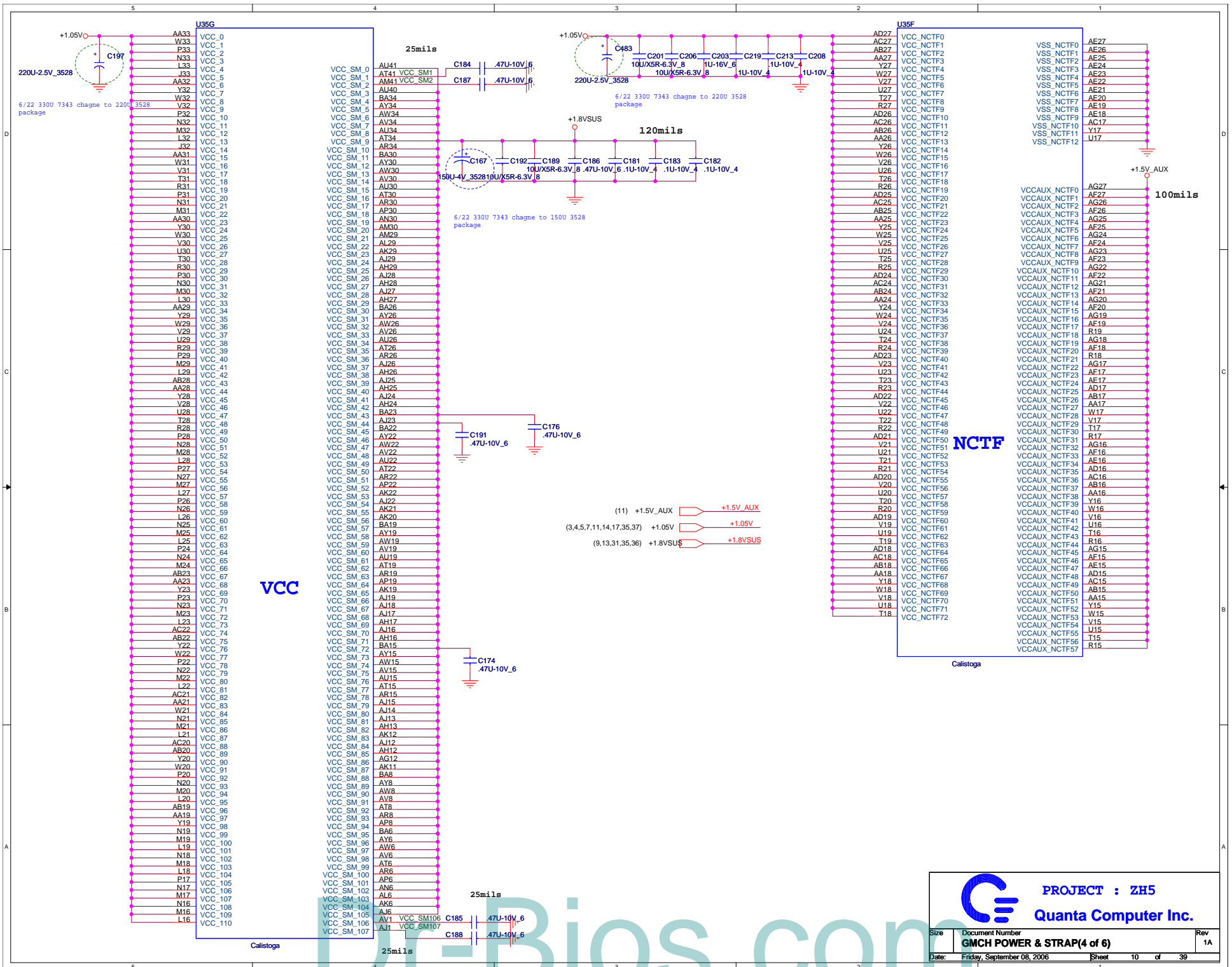
6/30 Add 39 in HSYNC and VSYNC

- GMCH Strap pin**
- MCH_CFG_5 Low = DMI X2, High=DMIX4
 - MCH_CFG_6 DDR : Low =Moby Dick, High= Calistoga (Default)
 - MCH_CFG_7 CPU Strap Low=RSVD, High=Mobile CPU
 - MCH_CFG_9 PCI Exp Graphics Lane: Low =Reserved,High=Mobility
 - MCH_CFG_10 Host PLL VCC Select: Low=Reserved, High=Mobility
 - MCH_CFG_11: PSB 4x CLK ENABLE Low=Reserved, High=Calistoga
 - MCH_CFG_16 PSB Dymnic ODT: Low=Dynamic ODT Disabled, High=Dynamic ODT Enabled.
 - MCH_CFG_18 VCC Select: LOW=1.05V, High=1.5V
 - MCH_CFG_19 DMI LANE Reversal: Low=Normal,High=LANES Reversed.
 - MCH_CFG_20 PCIE Backward interoperability mode: Low= only SDVO or PCIE xl is operational (defaults), High=SDVO and PCIE xl are operation simultaneously via the PEG port.



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Size	Document Number	Rev
	GMCH DMI & VEDIO (3 of 6)	1A
Date:	Friday, September 08, 2006	Sheet 9 of 39




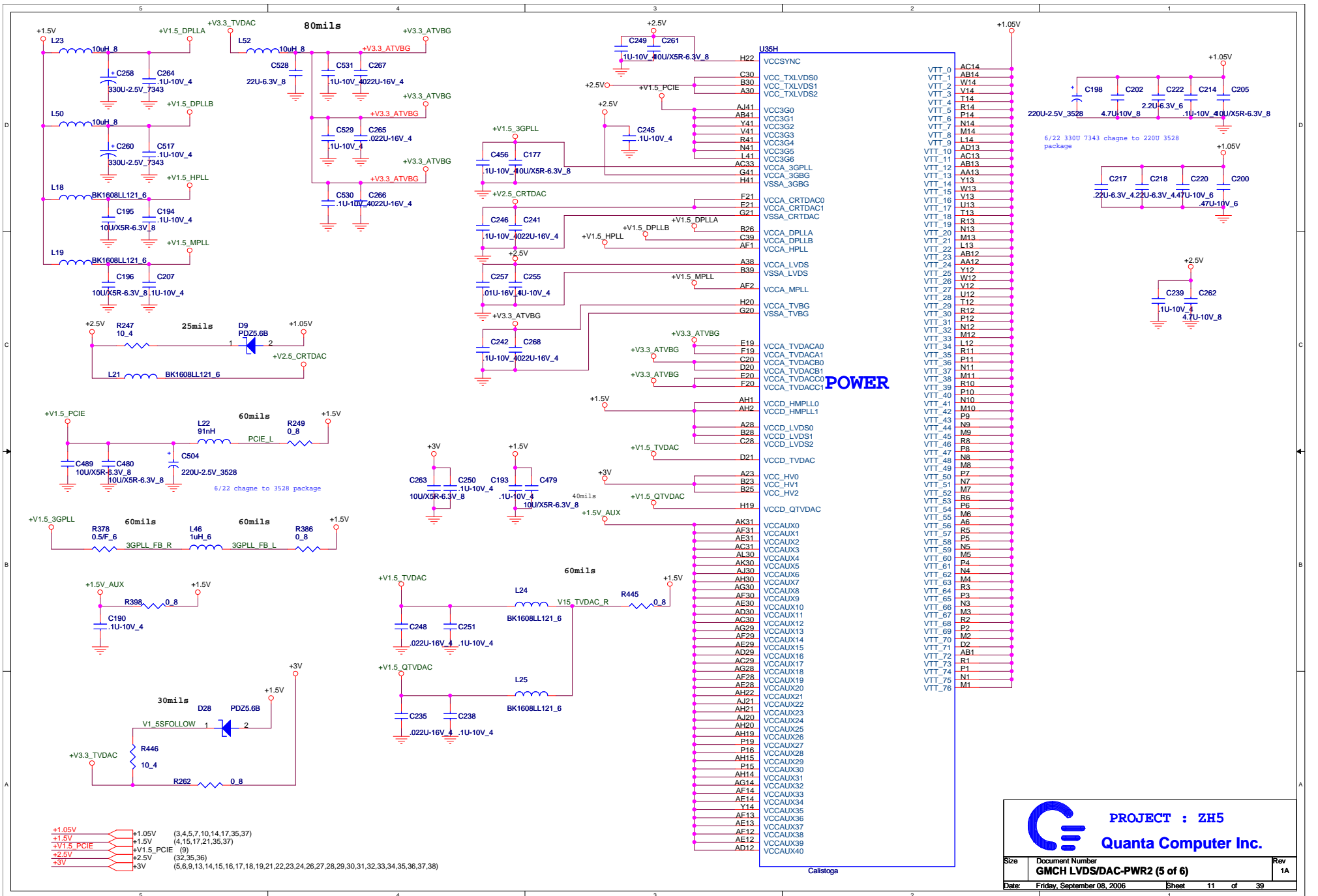
NCTF

Calistoga

VCC

(11) +1.5V_AUX
 (3,4,5,7,11,14,17,35,37) +1.05V
 (9,13,31,35,36) +1.8VSUS

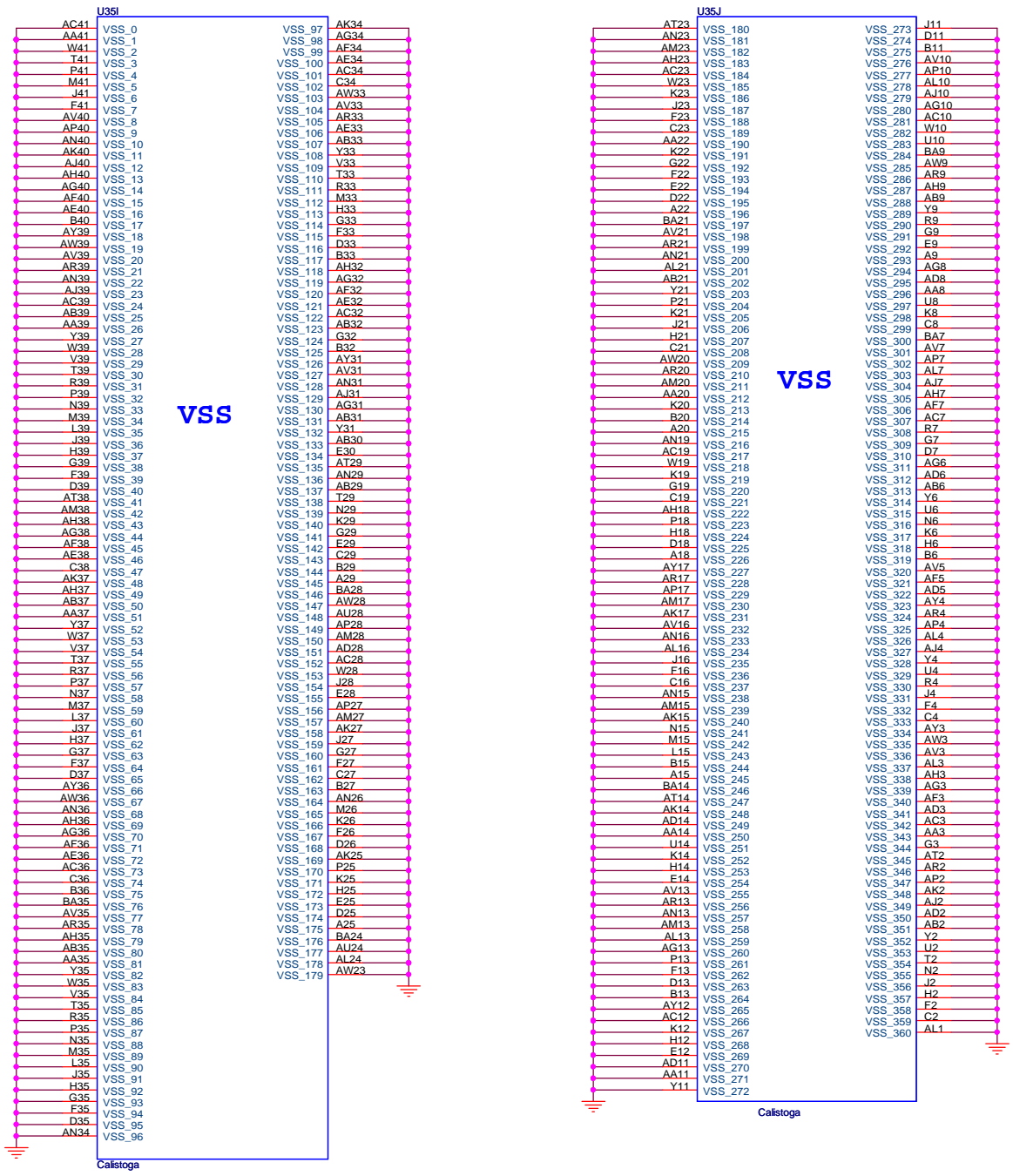
	PROJECT : ZH5		Rev 1A
	Quanta Computer Inc.		
Size	Document Number		
	GMCH POWER & STRAP(4 of 6)		
Date:	Friday, September 08, 2006	Sheet	10 of 39



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PROJECT : ZH5
Quanta Computer Inc.

Size	Document Number	Rev
	GMCH LVDS/DAC-PWR2 (5 of 6)	1A
Date:	Friday, September 08, 2006	Sheet 11 of 39

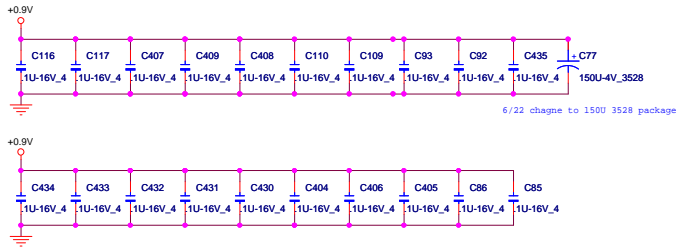


PROJECT : ZH5
Quanta Computer Inc.

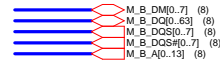
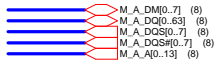
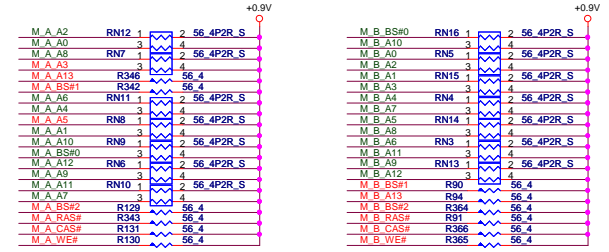
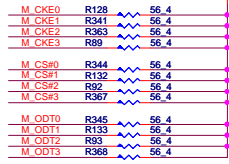
Size	Document Number	Rev
	GMCH GND(6 OF 6)	1A
Date:	Friday, September 08, 2006	Sheet 12 of 39

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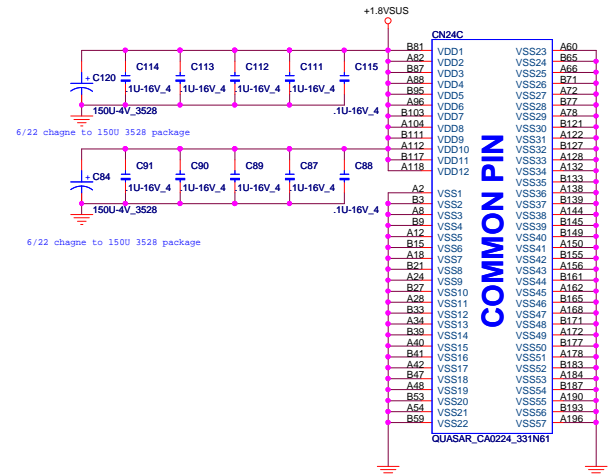
TERMINATOR DECOUPLING CAPACITOR



DDR2 TERMINATOR



DDR2 SO-DIMM SOCKET



CN24A

M_A DM0	A10	DM0
M_A DM1	A26	DM1
M_A DM2	A52	DM2
M_A DM3	A67	DM3
M_A DM4	A130	DM4
M_A DM5	A147	DM5
M_A DM6	A170	DM6
M_A DM7	A185	DM7
M_A DQ0	A13	DQ0
M_A DQ1	A31	DQ1
M_A DQ2	A51	DQ2
M_A DQ3	A70	DQ3
M_A DQ4	A131	DQ4
M_A DQ5	A148	DQ5
M_A DQ6	A169	DQ6
M_A DQ7	A188	DQ7
M_A DQS0	A11	DQS0
M_A DQS1	A29	DQS1
M_A DQS2	A49	DQS2
M_A DQS3	A68	DQS3
M_A DQS4	A129	DQS4
M_A DQS5	A146	DQS5
M_A DQS6	A167	DQS6
M_A DQS7	A186	DQS7
M_A A0	A102	A0
M_A A1	A101	A1
M_A A2	A100	A2
M_A A3	A99	A3
M_A A4	A98	A4
M_A A5	A97	A5
M_A A6	A94	A6
M_A A7	A92	A7
M_A A8	A93	A8
M_A A9	A91	A9
M_A A10	A105	A10/AP
M_A A11	A90	A11
M_A A12	A89	A12
M_A A13	A116	NC/A13
	A96	NC/A14
	A94	NC/A15
(8) M_A BS#0	M_A BS#0	BA0
(8) M_A BS#1	M_A BS#1	BA1
(8) M_A BS#2	M_A BS#2	BA2
(9) M_CLK_DDR0	M_CLK_DDR0	CK0
(9) M_CLK_DDR#0	M_CLK_DDR#0	CK0
(9) M_CLK_DDR1	M_CLK_DDR1	CK1
(9) M_CLK_DDR#1	M_CLK_DDR#1	CK1
(9) M_CKE0	M_CKE0	CKE0
(9) M_CKE1	M_CKE1	CKE1
(9) M_CS#0	M_CS#0	CS0
(9) M_CS#1	M_CS#1	CS1
(8) M_A RAS#	M_A RAS#	RAS
(8) M_A CAS#	M_A CAS#	CAS
(8) M_A WE#	M_A WE#	WE
(9) M_ODT0	M_ODT0	ODT0
(9) M_ODT1	M_ODT1	ODT1
(5) CGDAT_SMB	CGDAT_SMB	SMB
(5) CGCLK_SMB	CGCLK_SMB	SMB

QUASAR_CA0224_331N61

CN24B

M_B DM0	B10	DM0
M_B DM1	B26	DM1
M_B DM2	B52	DM2
M_B DM3	B67	DM3
M_B DM4	B130	DM4
M_B DM5	B147	DM5
M_B DM6	B170	DM6
M_B DM7	B185	DM7
M_B DQ0	B13	DQ0
M_B DQ1	B31	DQ1
M_B DQ2	B51	DQ2
M_B DQ3	B70	DQ3
M_B DQ4	B131	DQ4
M_B DQ5	B148	DQ5
M_B DQ6	B169	DQ6
M_B DQ7	B188	DQ7
M_B DQS0	B11	DQS0
M_B DQS1	B29	DQS1
M_B DQS2	B49	DQS2
M_B DQS3	B68	DQS3
M_B DQS4	B129	DQS4
M_B DQS5	B146	DQS5
M_B DQS6	B167	DQS6
M_B DQS7	B186	DQS7
M_B A0	B102	A0
M_B A1	B101	A1
M_B A2	B100	A2
M_B A3	B99	A3
M_B A4	B98	A4
M_B A5	B97	A5
M_B A6	B94	A6
M_B A7	B92	A7
M_B A8	B93	A8
M_B A9	B91	A9
M_B A10	B106	A10/AP
M_B A11	B90	A11
M_B A12	B89	A12
M_B A13	B116	NC/A13
	B96	NC/A14
	B94	NC/A15
(8) M_B BS#0	M_B BS#0	BA0
(8) M_B BS#1	M_B BS#1	BA1
(8) M_B BS#2	M_B BS#2	BA2
(9) M_CLK_DDR3	M_CLK_DDR3	CK3
(9) M_CLK_DDR#3	M_CLK_DDR#3	CK3
(9) M_CLK_DDR2	M_CLK_DDR2	CK2
(9) M_CLK_DDR#2	M_CLK_DDR#2	CK2
(9) M_CKE2	M_CKE2	CKE2
(9) M_CKE3	M_CKE3	CKE3
(9) M_CS#2	M_CS#2	CS2
(9) M_CS#3	M_CS#3	CS3
(8) M_B RAS#	M_B RAS#	RAS
(8) M_B CAS#	M_B CAS#	CAS
(8) M_B WE#	M_B WE#	WE
(9) M_ODT2	M_ODT2	ODT2
(9) M_ODT3	M_ODT3	ODT3
(5) CGDAT_SMB	CGDAT_SMB	SMB
(5) CGCLK_SMB	CGCLK_SMB	SMB

QUASAR_CA0224_331N61

DUAL DDR2 SO-DIMM MODULE A SIDE

DUAL DDR2 SO-DIMM MODULE B SIDE

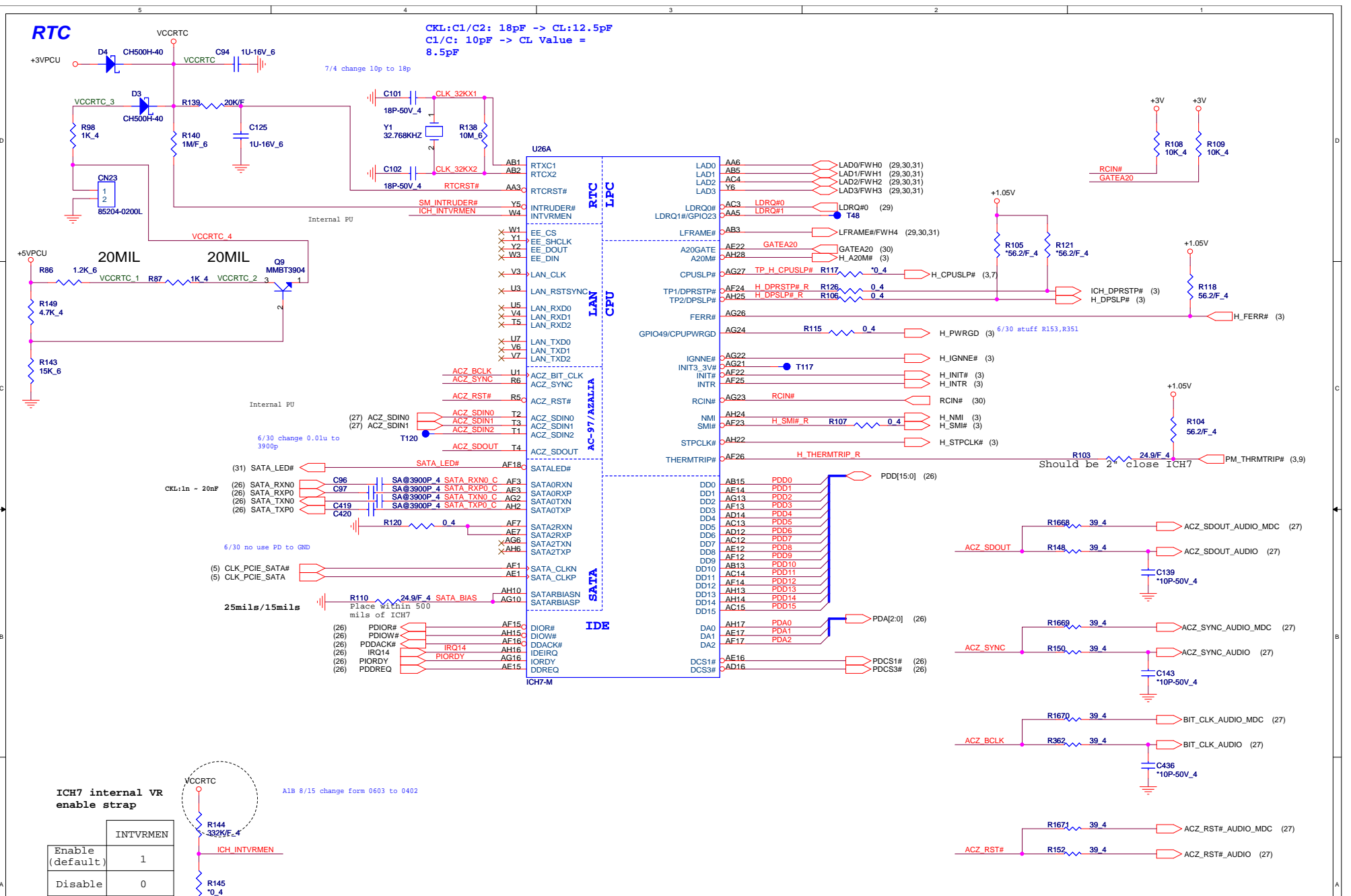
PROJECT : ZH5
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Size: Document Number: **DDR2 SO-DIMM & TERMINATOR** Rev: 1A
 Date: Friday, September 06, 2006 Sheet: 13 of 39



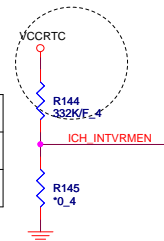
RTC

CKL:C1/C2: 18pF -> CL:12.5pF
 C1/C: 10pF -> CL Value = 8.5pF



ICH7 internal VR enable strap

	INTVRMEN
Enable (default)	1
Disable	0



A1B 8/15 change form 0603 to 0402

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Size	Document Number	Rev
	ICH7-M RTC/SATA/IDE/AZALIA/CPU (1 OF 4)	1A
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modify C

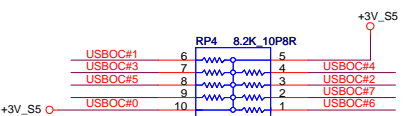
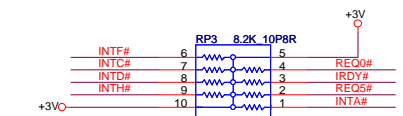
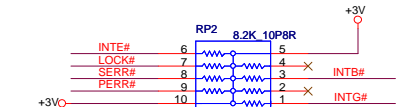
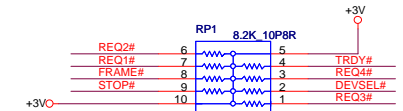
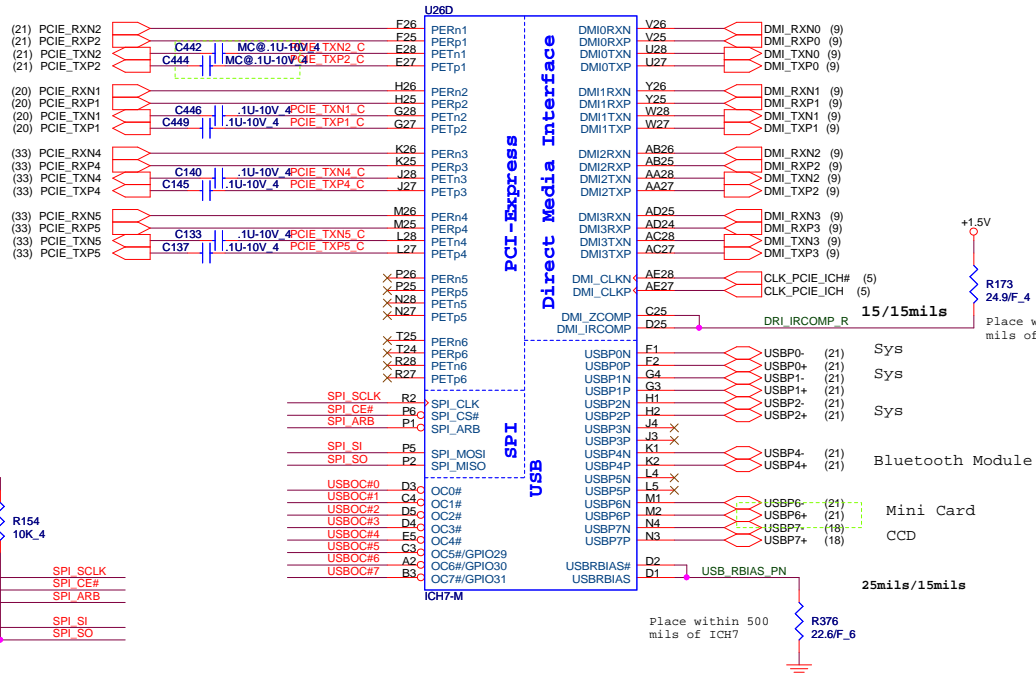
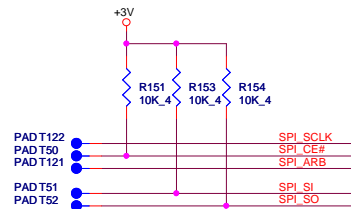
MINI CARD PCI-E

5789M

EZ4

EZ4

A1A 8/1 chagne PCI-E signal for different SB use

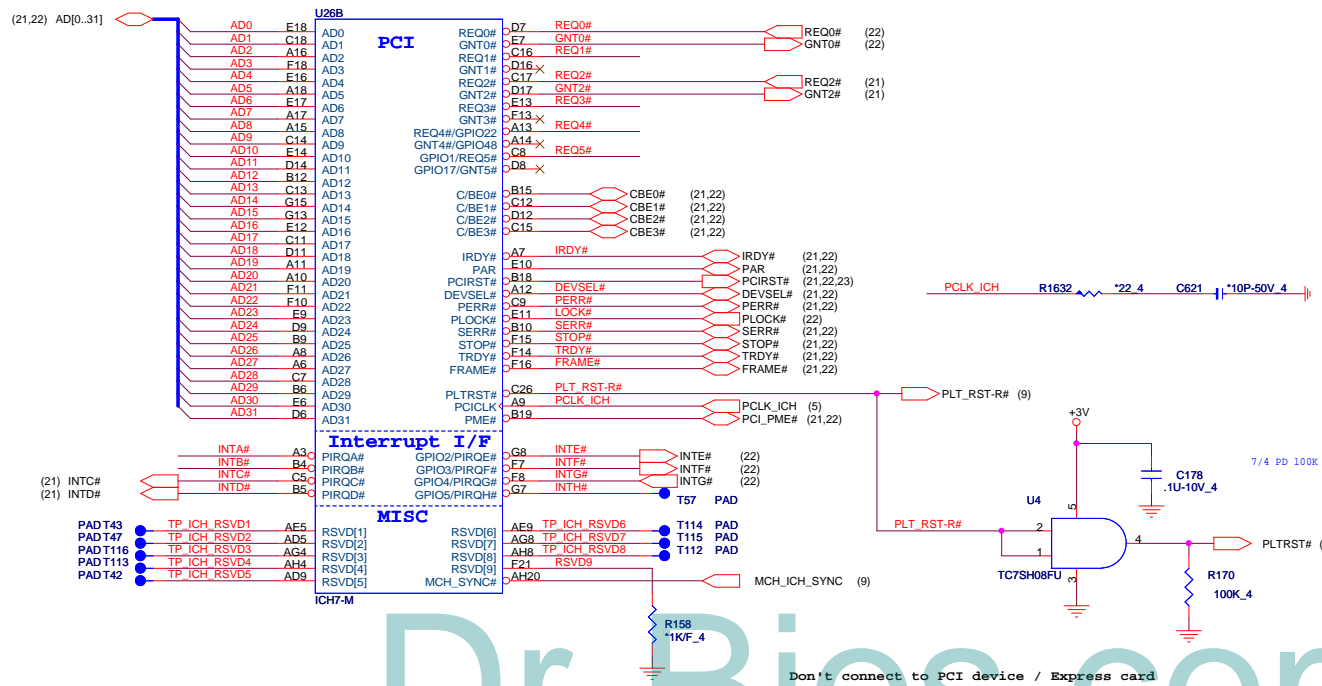


CKL use 10Kohm

ICH7 Boot BIOS select

	STRAP	GNT5# R1	GNT4# R2
LPC (default)	11	UNSTUFF	UNSTUFF
PCI	10	UNSTUFF	STUFF
SPI	01	STUFF	UNSTUFF

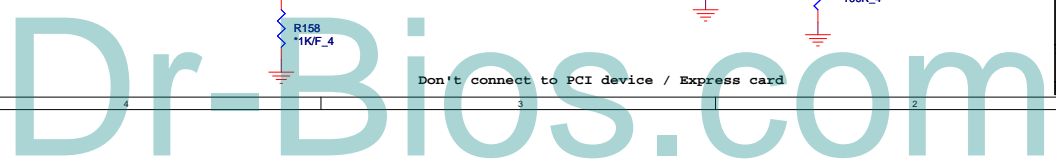
PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts
PCI7411	AD25	REQ0# / GNT0#	INT E/F/G#

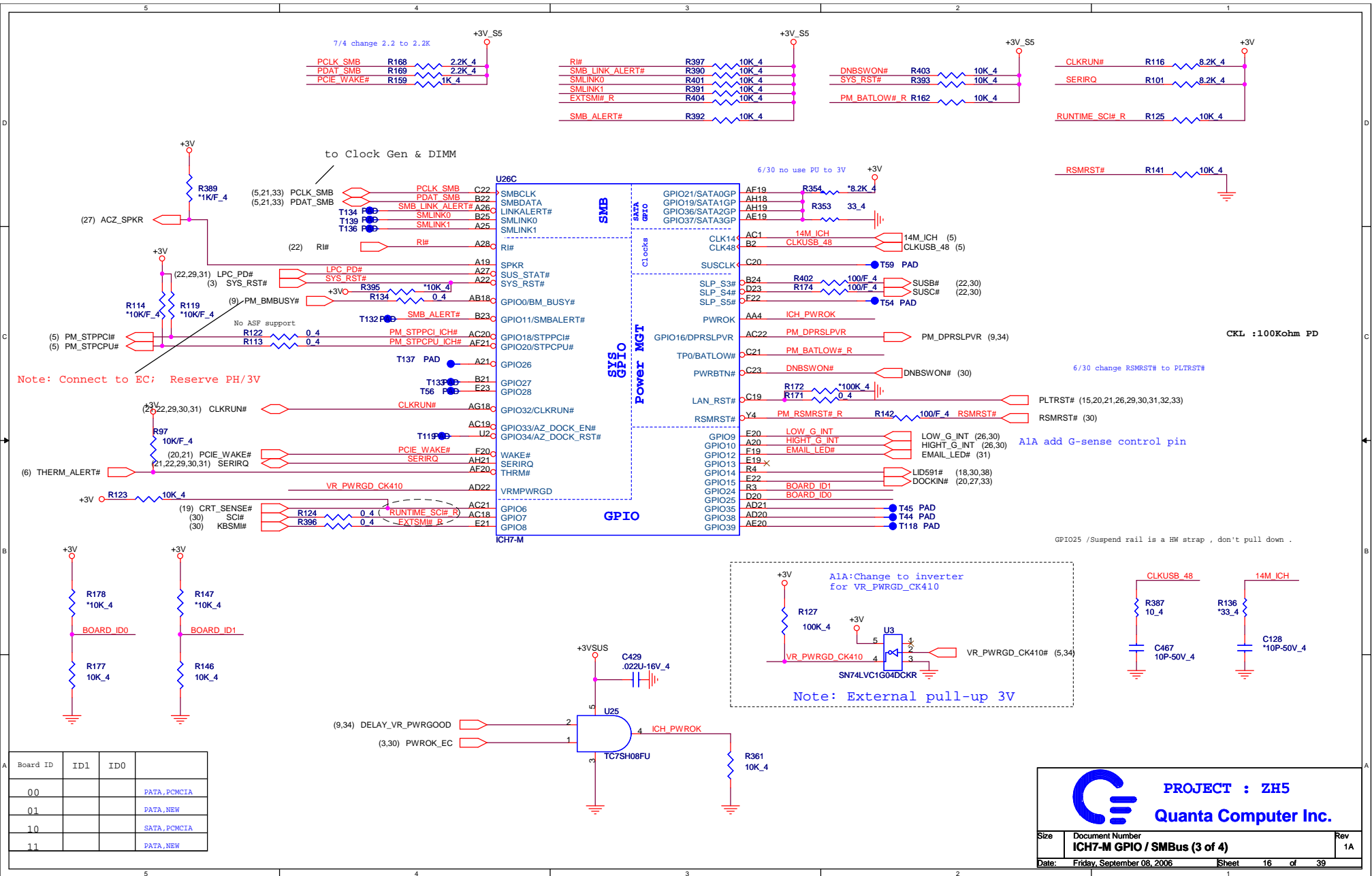


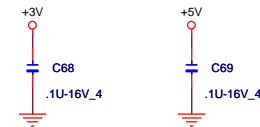
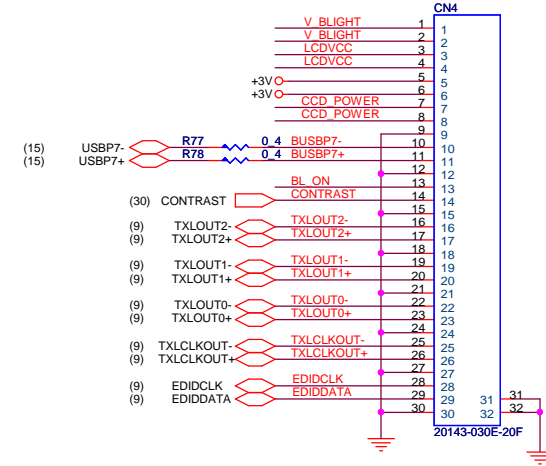
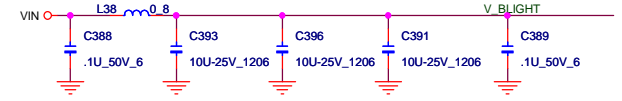
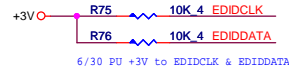
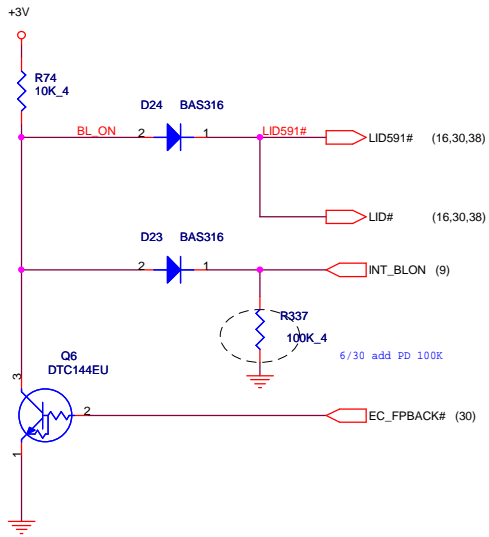
Don't connect to PCI device / Express card

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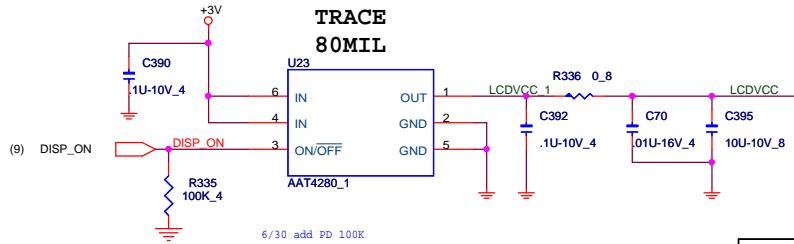
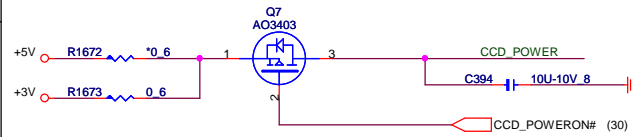
Size	Document Number	Rev
	ICH7-M MDI/PCI E/PC/USB (2 OF 4)	1A
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CAMERA MODULE CONNECTOR

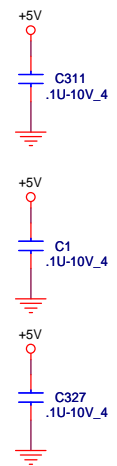
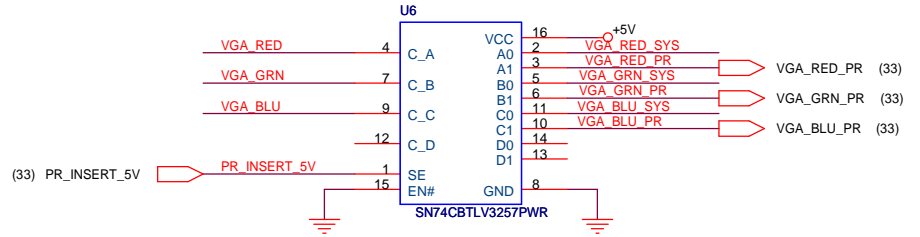




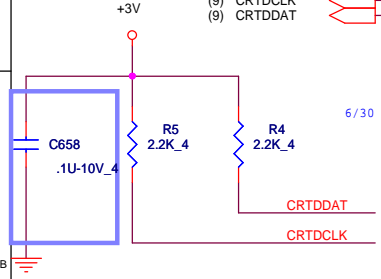
PROJECT : ZH5
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	LVDS CONNECTOR & CCD	1A
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- (9) VGA_RED
- (9) VGA_GRN
- (9) VGA_BLU
- (9) VSYNC
- (9) HSYNC
- (9) CRTDCLK
- (9) CRTDDAT

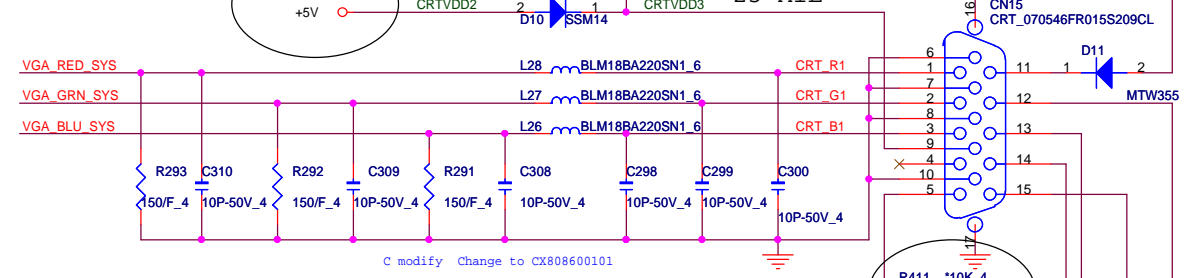


SEL	FUNCTION
LOW	IN_B0
HIGH	IN_B1



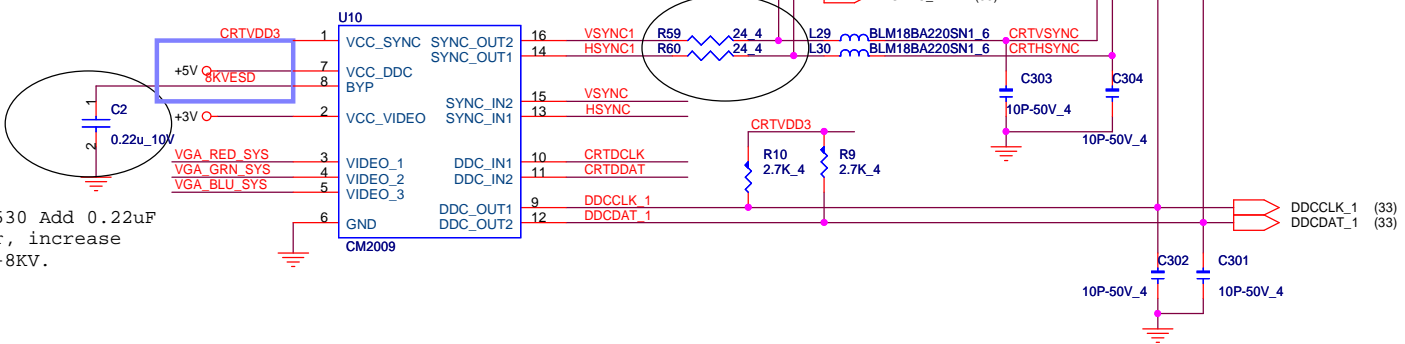
6/30 PU +3V to CRTDCLK & CRTDDATA

Edison 0523 Delete F2.



C modify Change to CX808600101

Edison 0530 Add 24 ohm resistor.



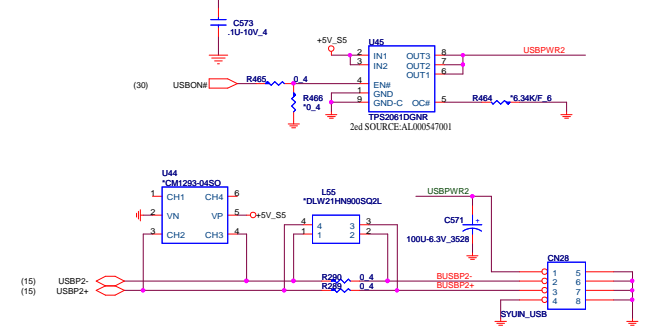
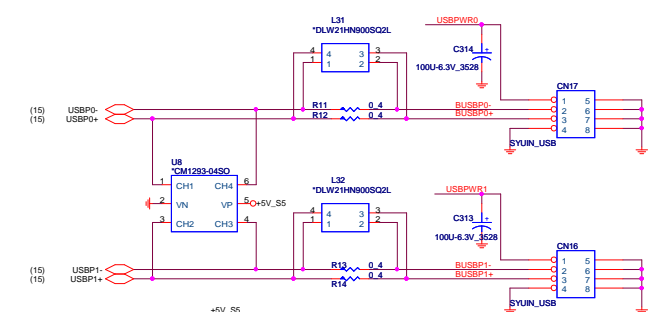
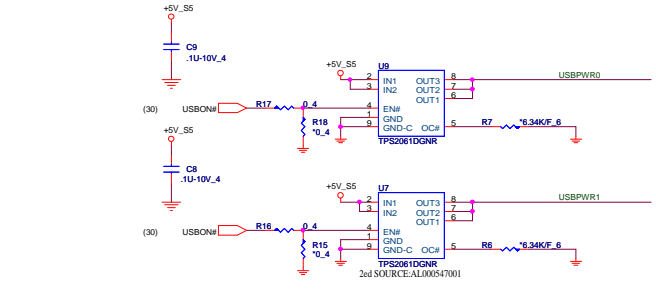
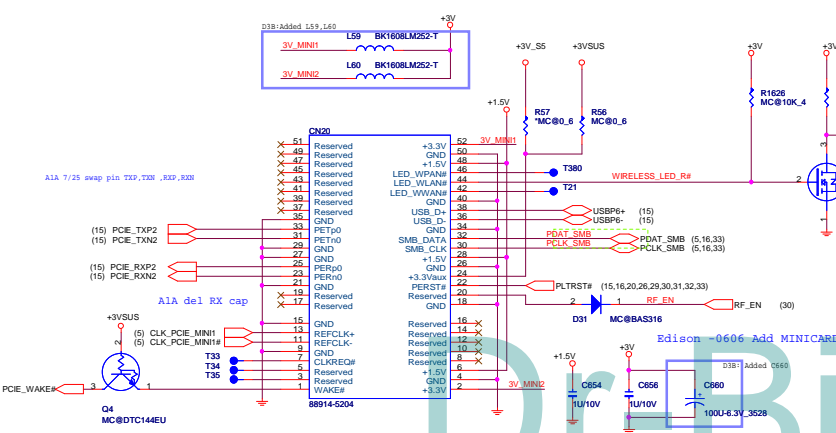
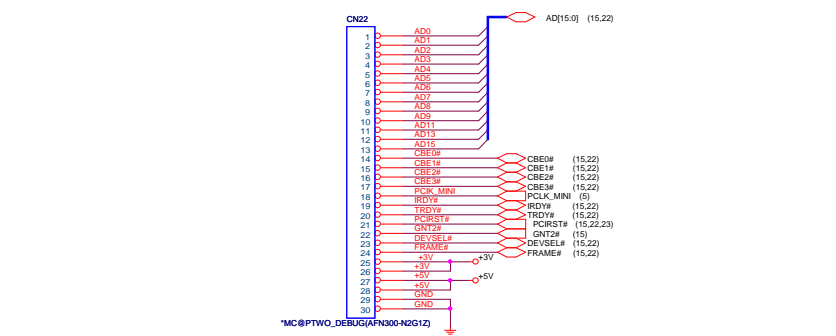
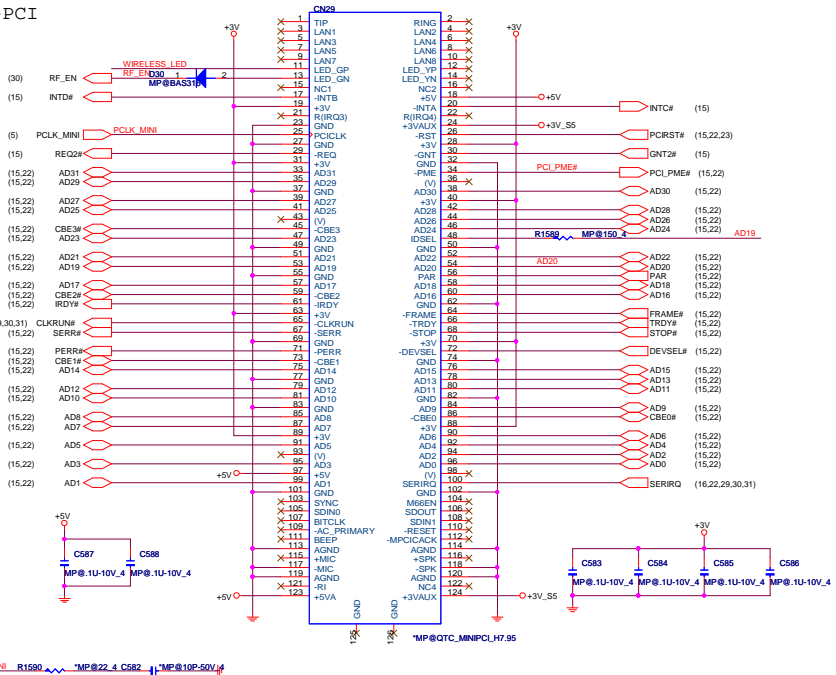
Edison 0530 Add 0.22uF capacitor, increase ESD to +-8KV.

PROJECT : ZH5
Quanta Computer Inc.

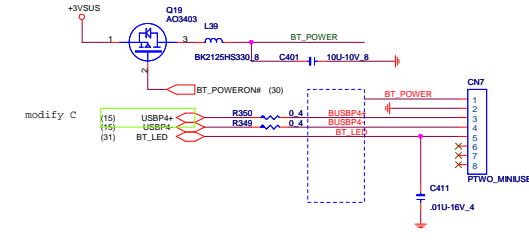
Size	Document Number	Rev
	CRT-PORT	1A
Date:	Friday, September 08, 2006	Sheet 19 of 39

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MINI-PCI

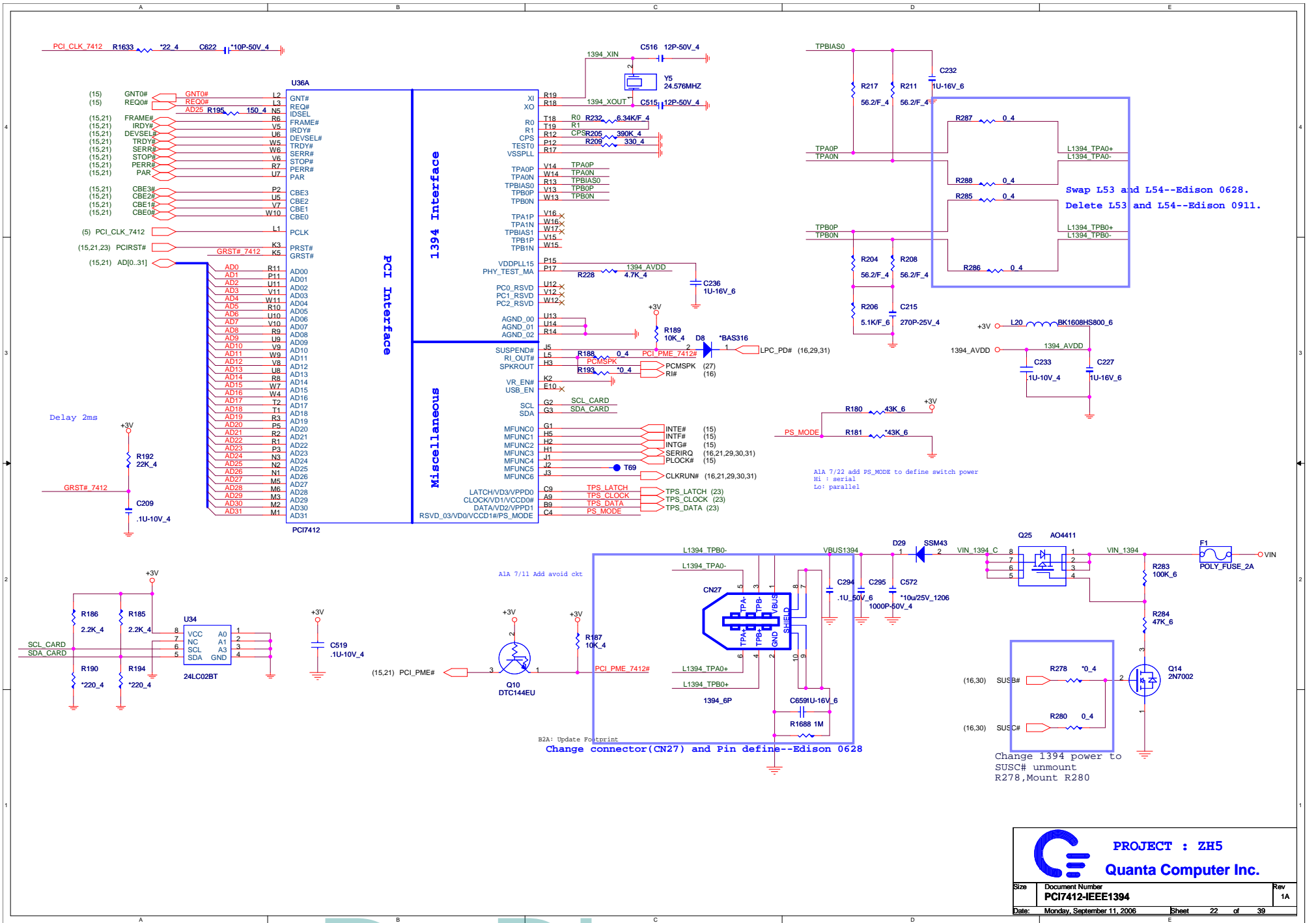


BLUETOOTH MODULE CONNECTOR



Edison -0606-Add MINICARD bypass Capacitors.

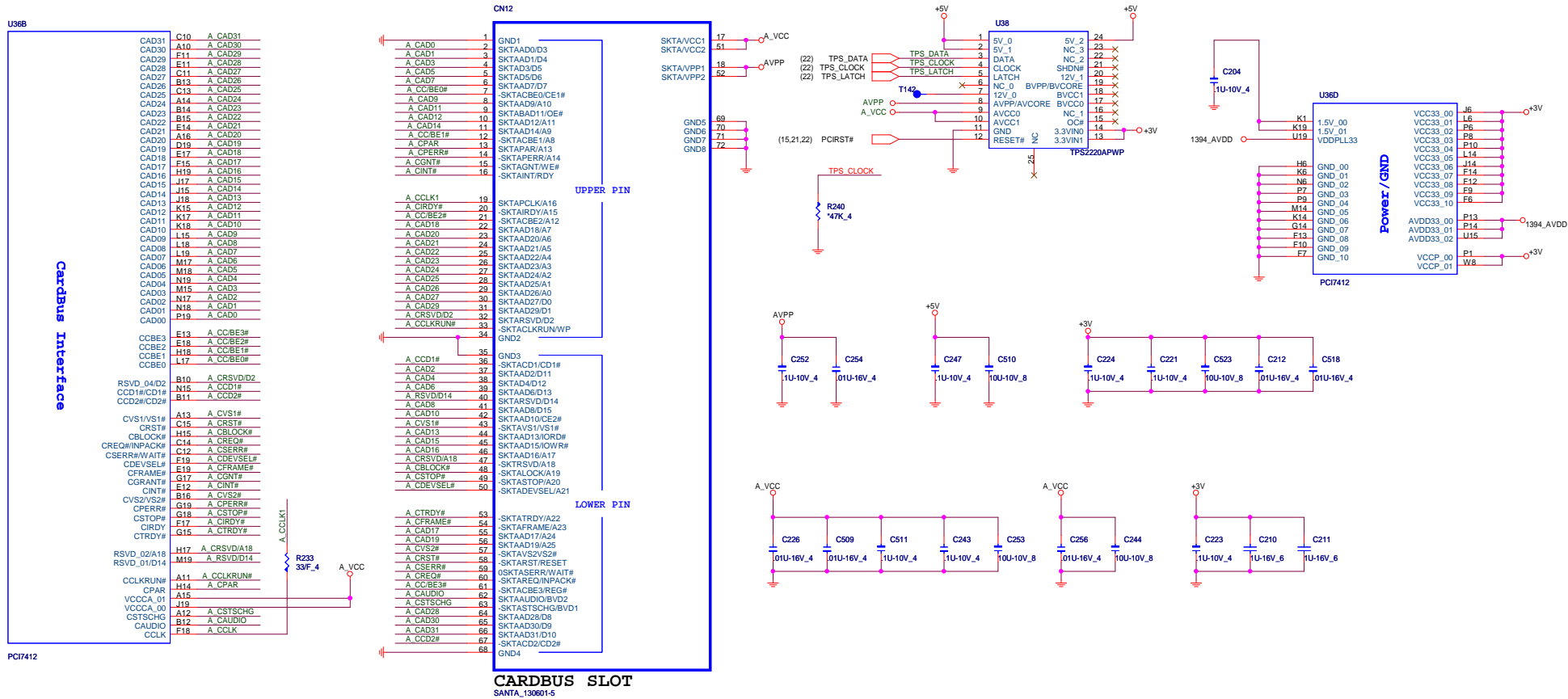
PROJECT : ZH5
Quanta Computer Inc.
 Size Document Number
PCMCIA /Mini Card /USB / Blue Tooth
 Date: Tuesday, September 12, 2006 Sheet 21 of 39

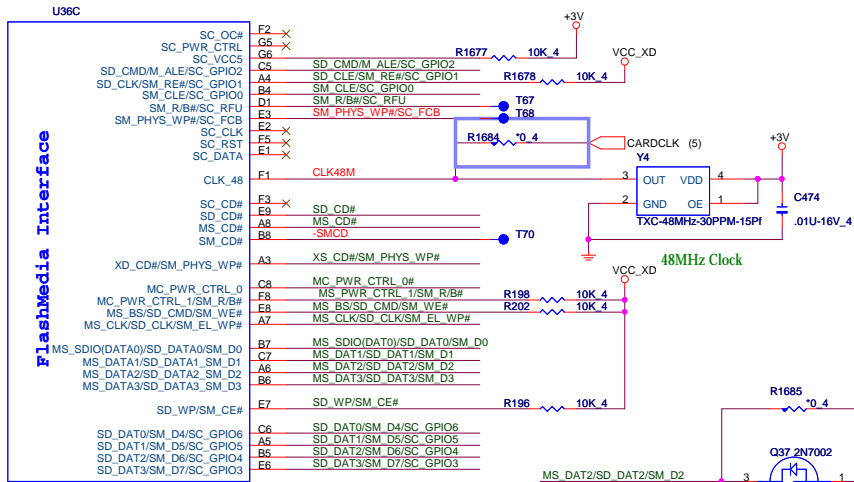


PROJECT : ZH5
Quanta Computer Inc.

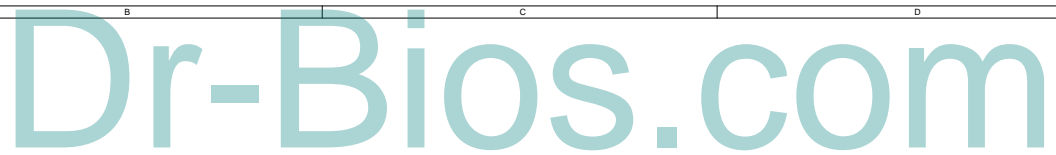
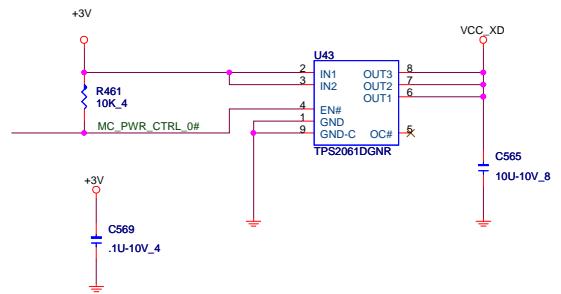
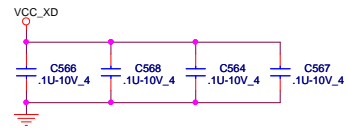
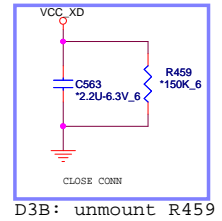
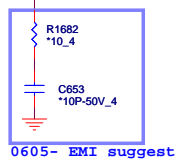
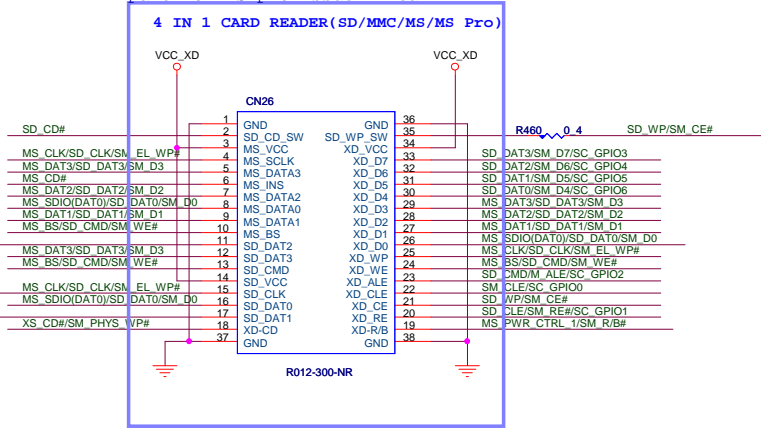
Size	Document Number	Rev
	PCI7412-IEEE1394	1A
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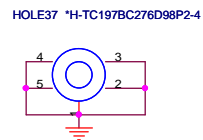
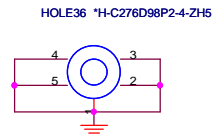
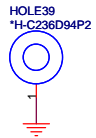
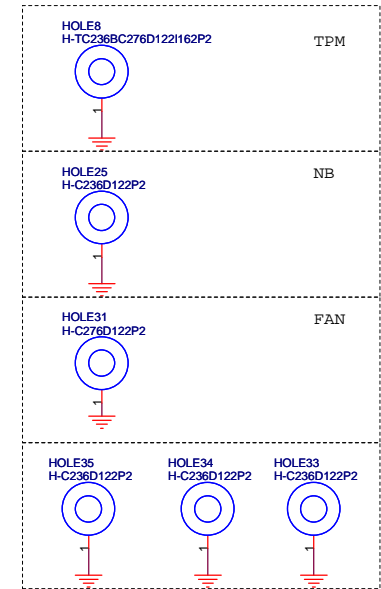
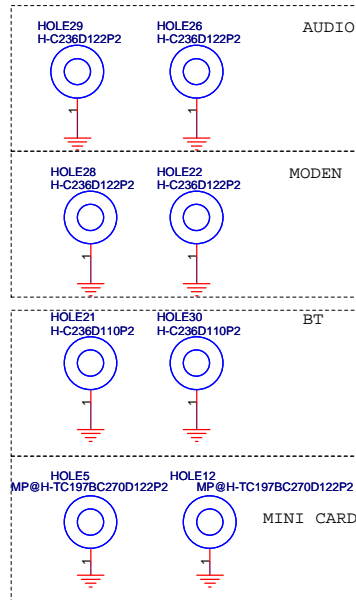
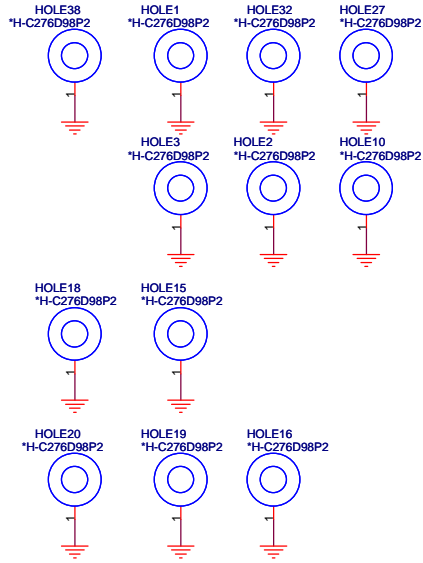



B2A: Change CN26, modify pin define and update part for MS pro issue fixed

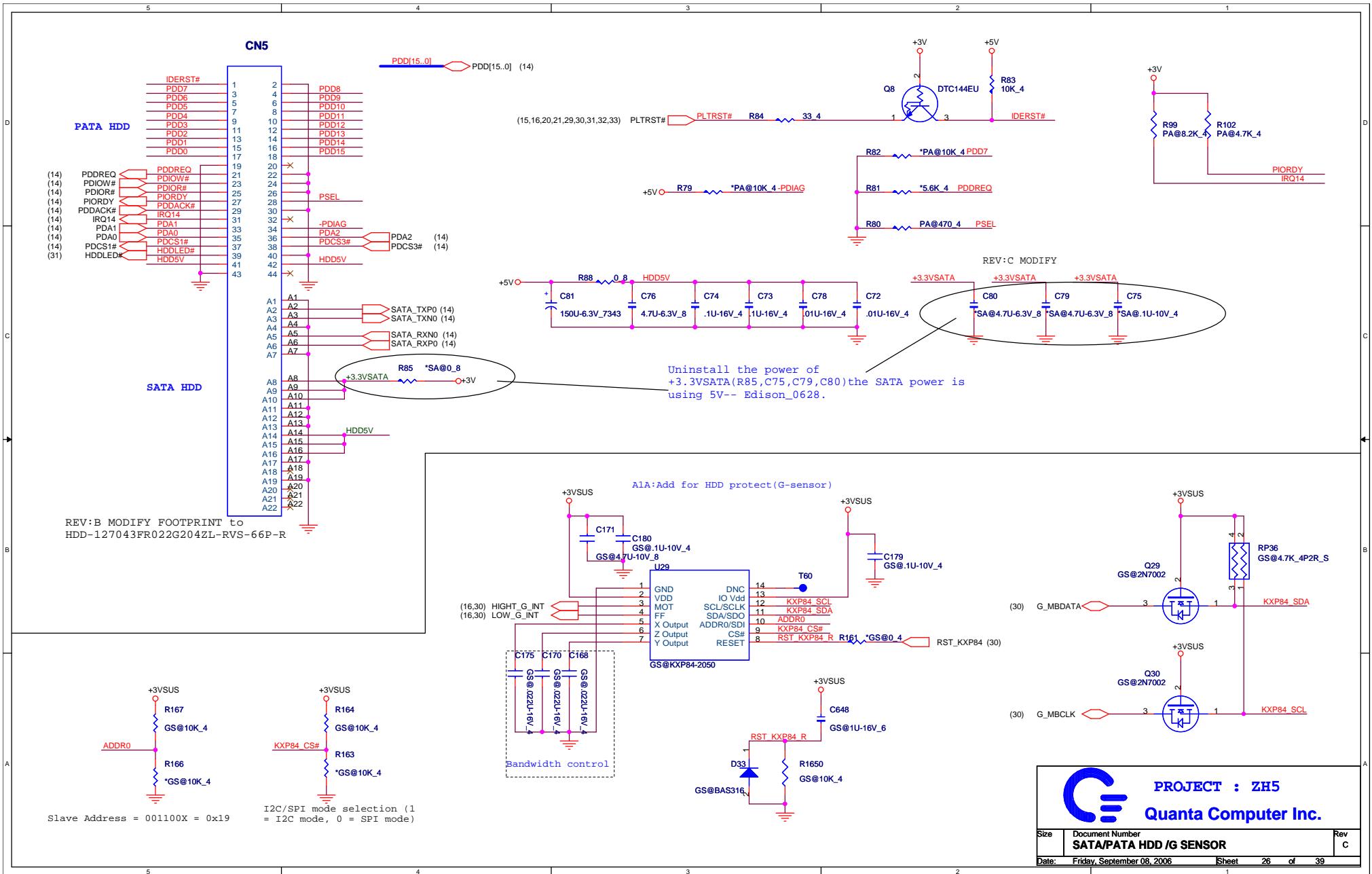


TOP

BOT

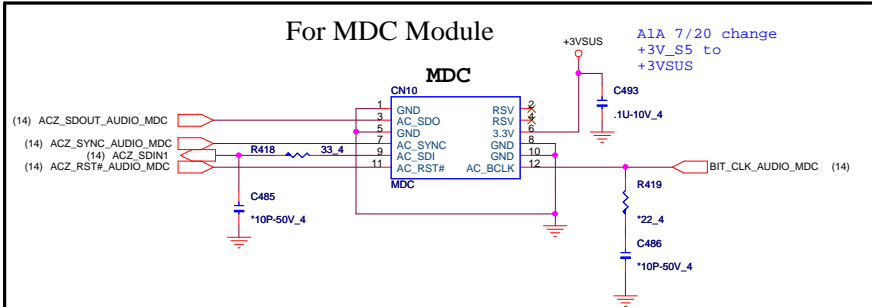
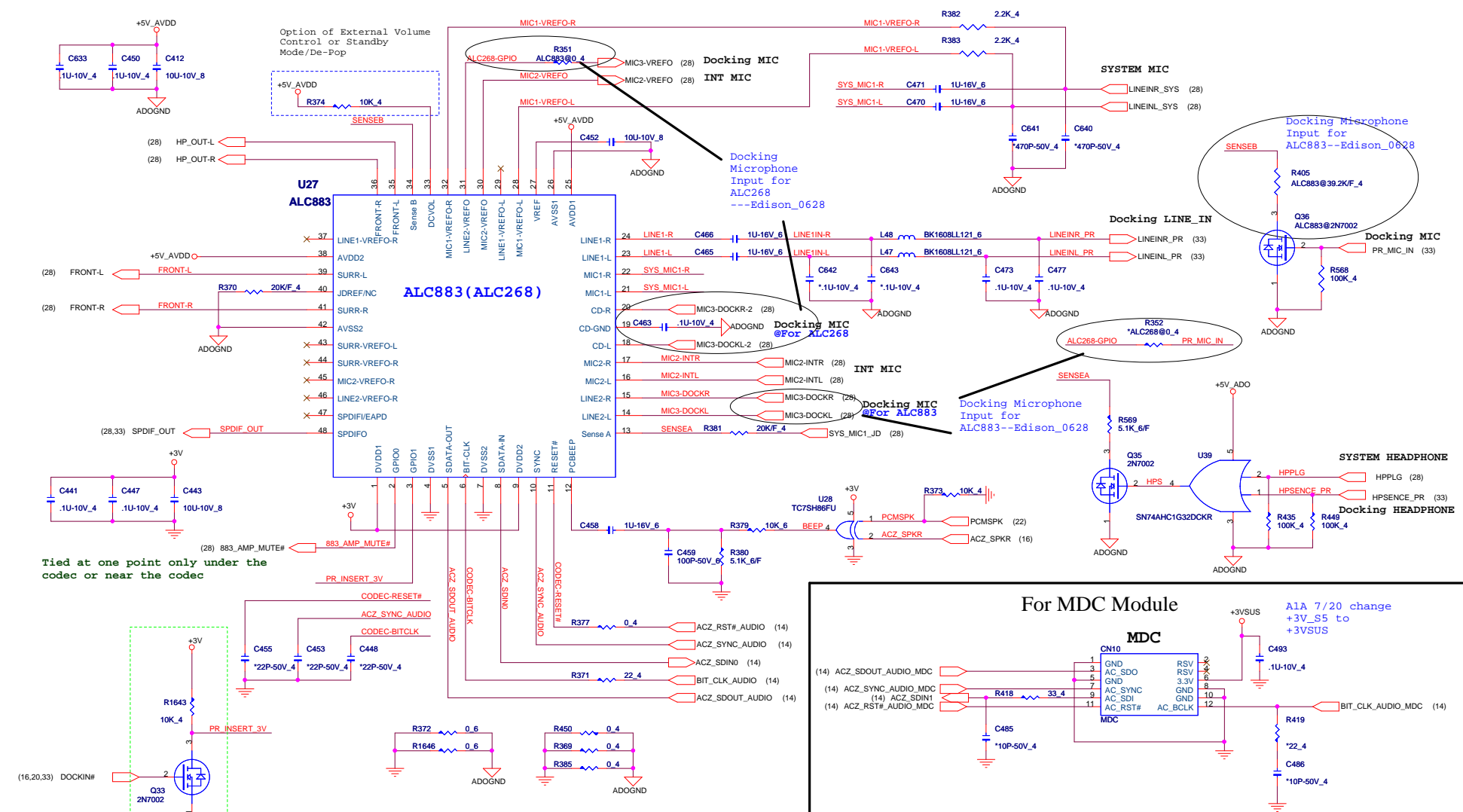


		PROJECT : ZH5	
		Quanta Computer Inc.	
Size	Document Number	Rev	
	HOLE	C	
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CODEC (ALC268)

LINE IN



PROJECT : ZH5
Quanta Computer Inc.

Size	Document Number	Rev
	CODEC ALC883 & MDC	1A
Date:	Friday, September 08, 2006	Sheet 27 of 39

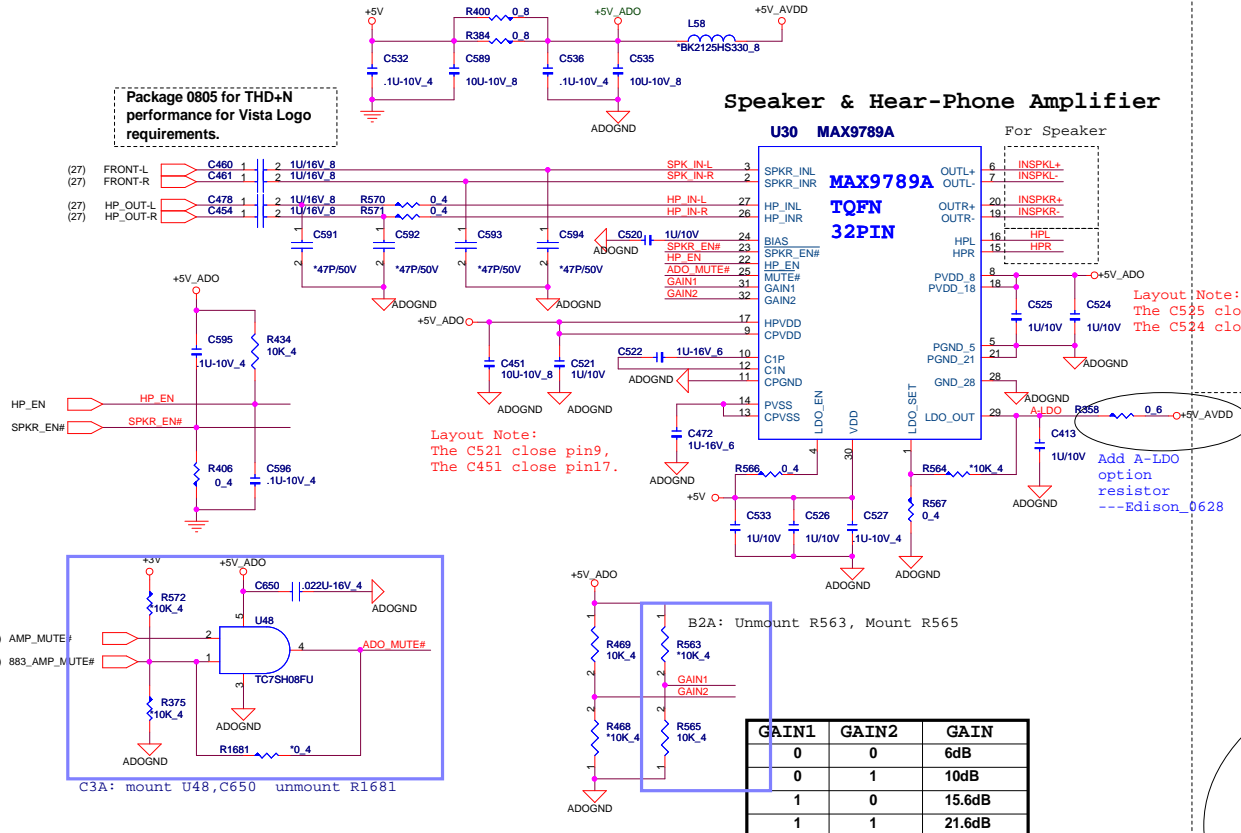
Package 0805 for THD+N performance for Vista Logo requirements.

Speaker & Hear-Phone Amplifier

U30 MAX9789A

MAX9789A
TQFN
32PIN

For Speaker

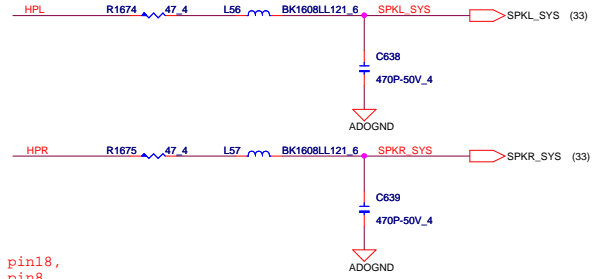


Layout Note:
The C521 close pin9,
The C451 close pin17.

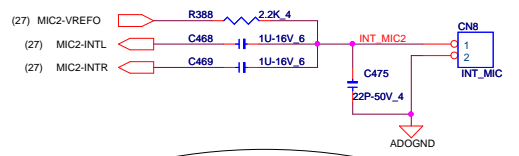
Layout Note:
The C525 close pin18,
The C524 close pin8.

Add A-LDO option resistor
---Edison_0628

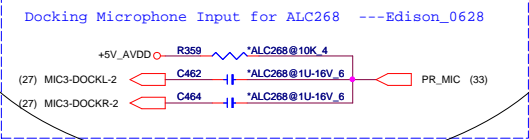
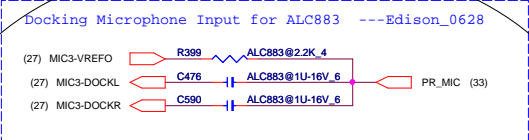
DOCK HEADPHONE



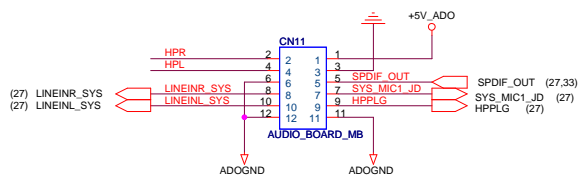
MIC



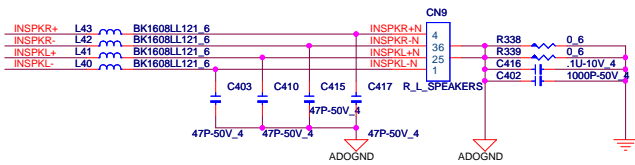
The Placement close to U27(ALC883/ALC268)



AUDIO BOARD



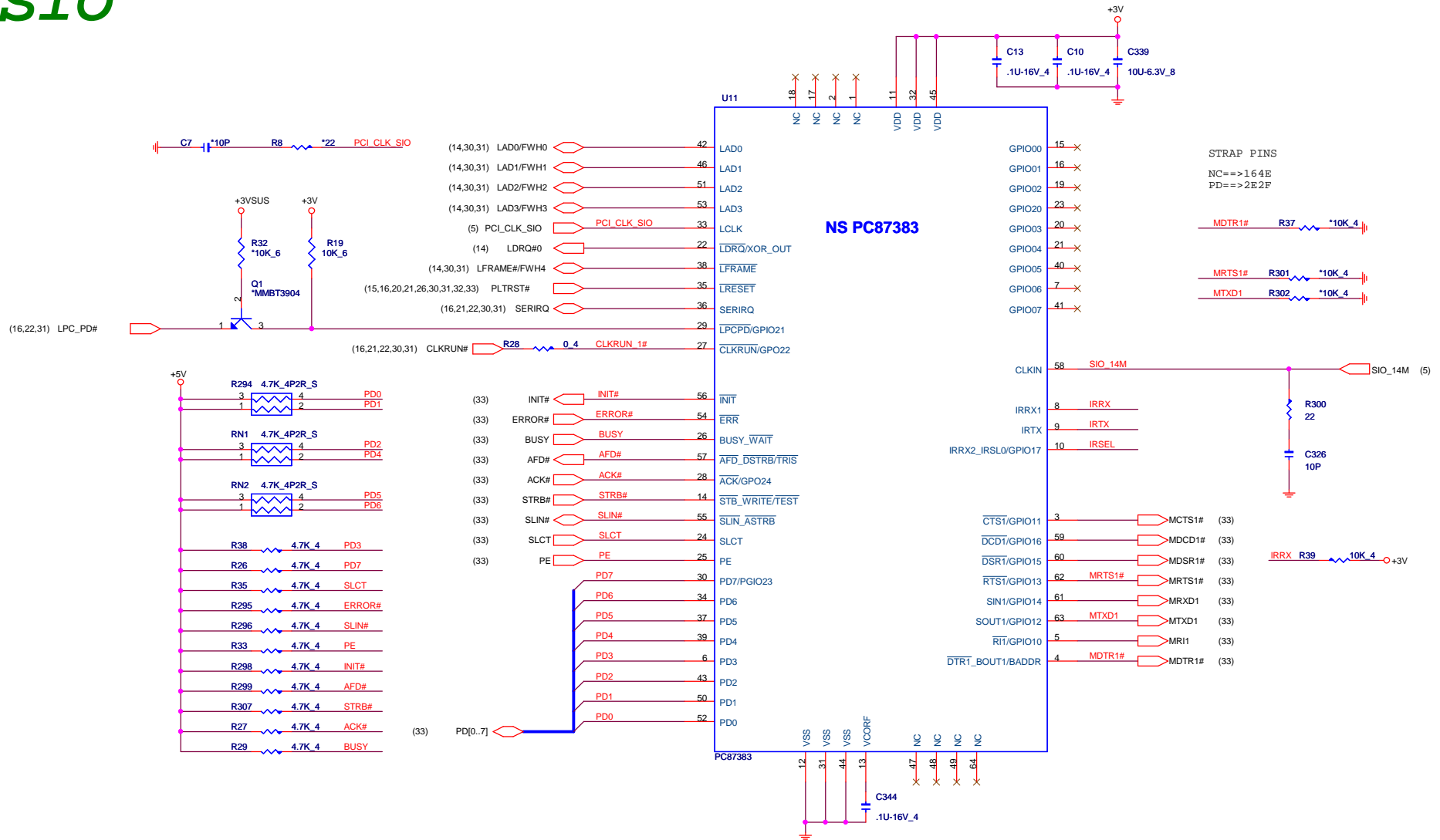
SPEAKER CONNECTOR



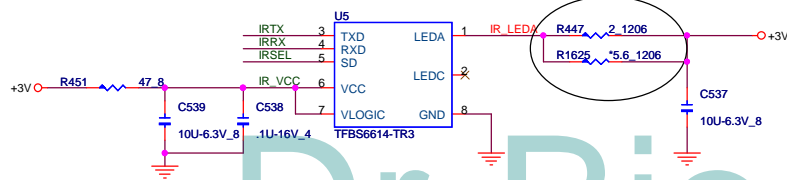
PROJECT : ZH5
Quanta Computer Inc.

Size	Document Number	Rev
	AUDIO AMP & SPEAK/LIN OUT	1A
Date:	Friday, September 08, 2006	Sheet 28 of 39

SIO



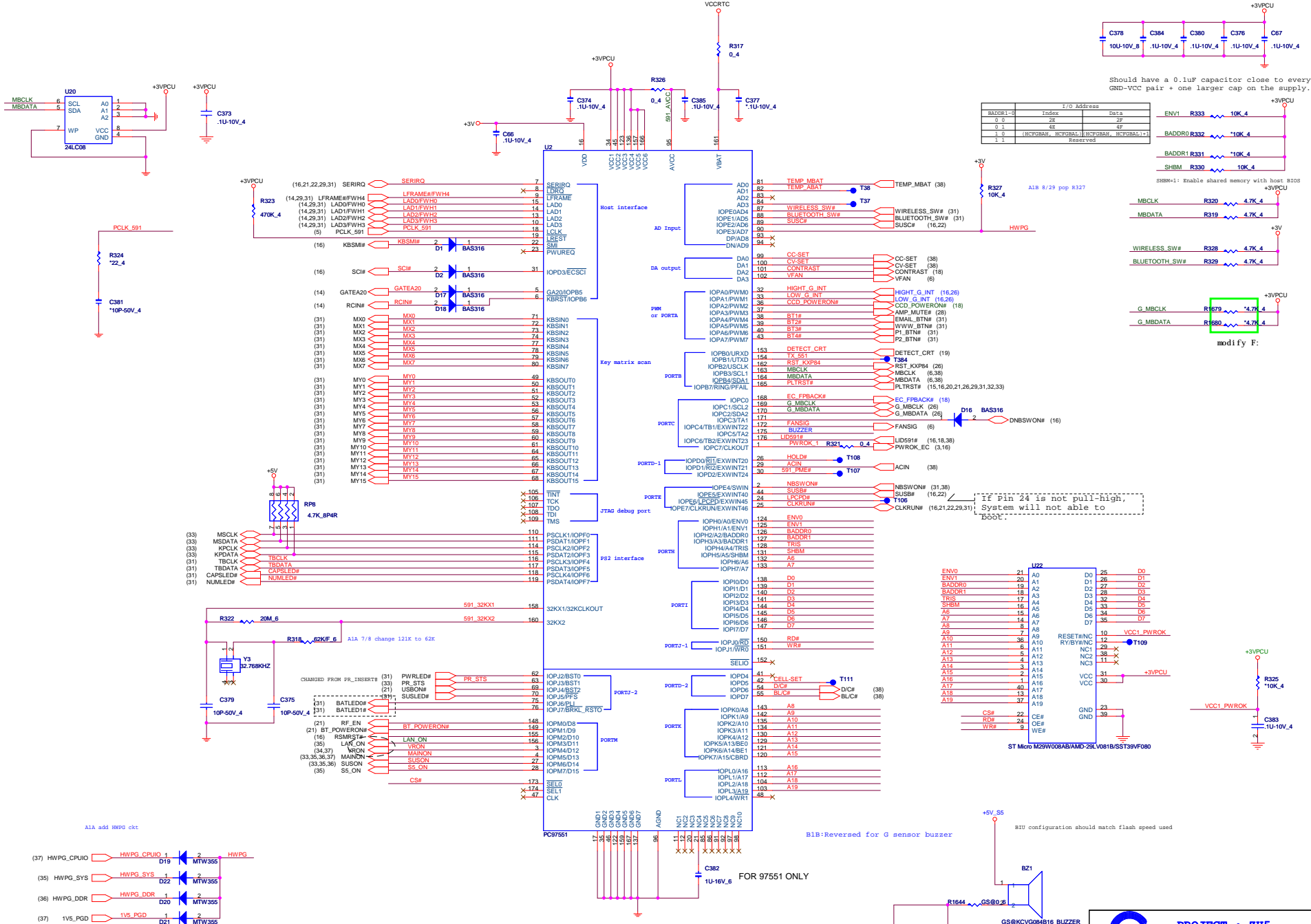
8/29 change trace to 30 mil



		PROJECT : ZH5	
		Quanta Computer Inc.	
Size Custom	Document Number SIO (87383)	Rev 1A	
Date: Friday, September 08, 2006	Sheet 29	of 39	Rev 1A

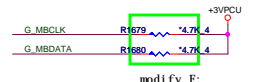
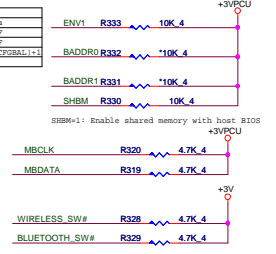
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LDRQ#(pin 8) internal is no use



Should have a 0.1uF capacitor close to every GND-VCC pair + one larger cap on the supply.

BAD0B1-0	I/O Address	Data
0	2E	2F
0	4E	4F
1	10CB0A, 10CB0B, 10CB0C, 10CB0D, 10CB0E, 10CB0F	Reserved
1		Reserved

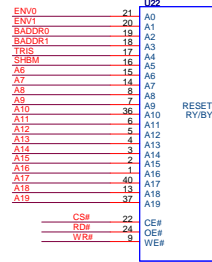


R327 10K_4
A1B 8/29 pop R327

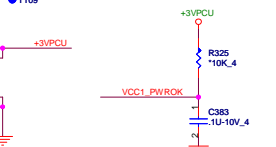
SHBM=1: Enable shared memory with host BIOS +3VPCU

D18 BAS316
DNBSWON# (16)

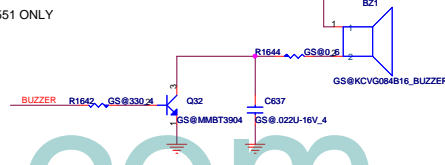
If Pin 24 is not pull-high, System will not able to Boot.



ST M925M008AB/AMD-ZS10818/SS13SVF80

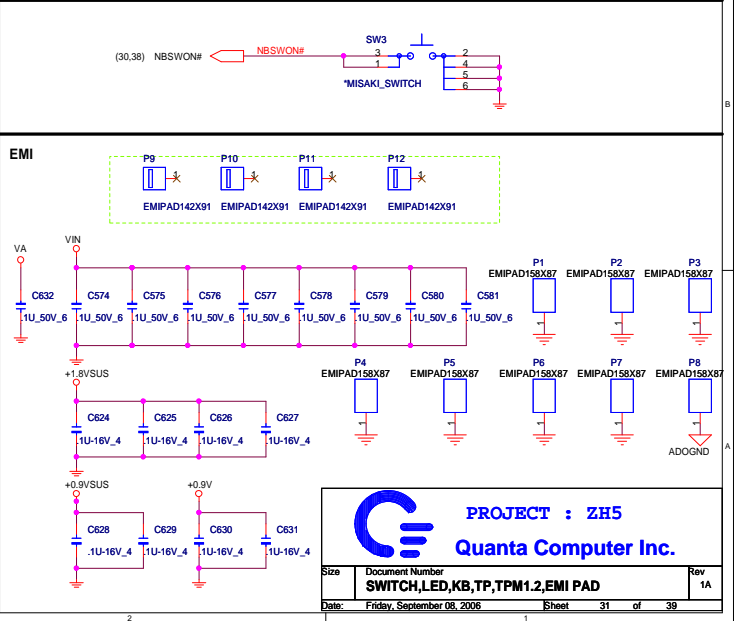
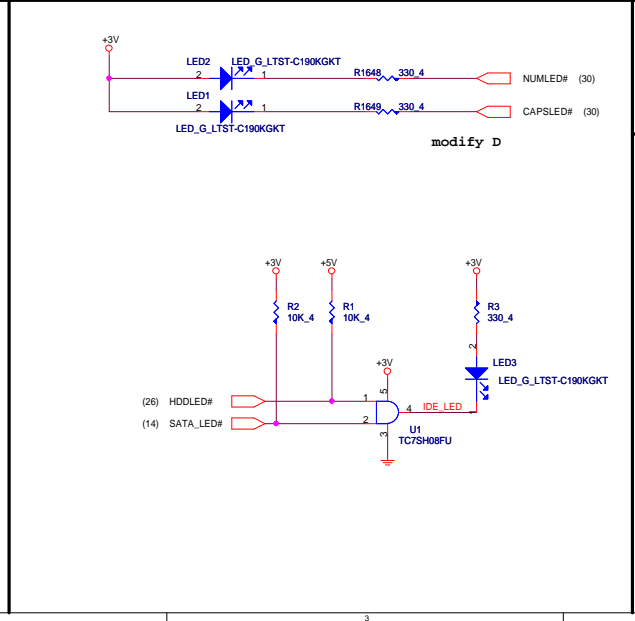
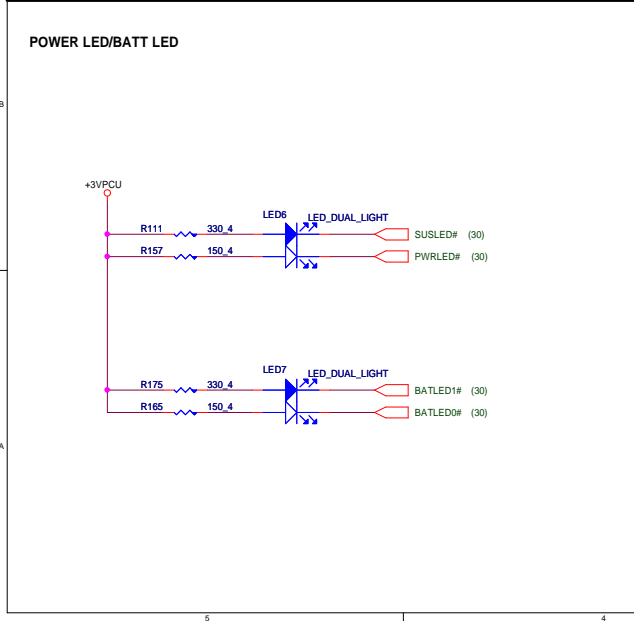
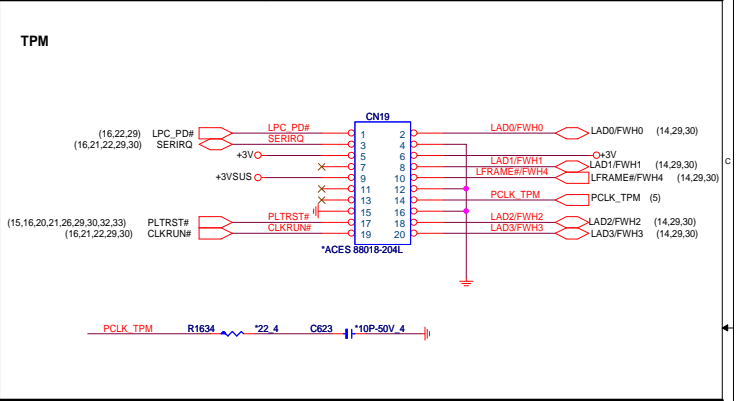
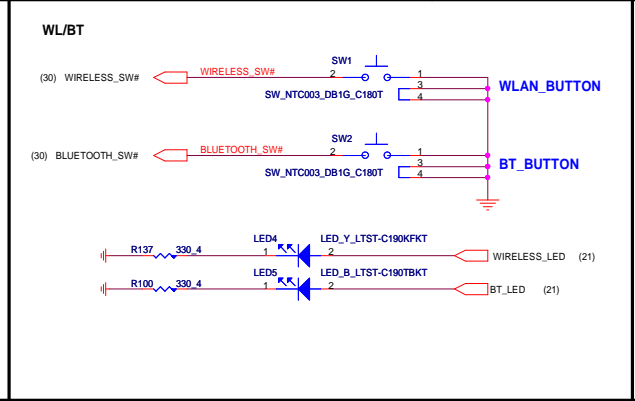
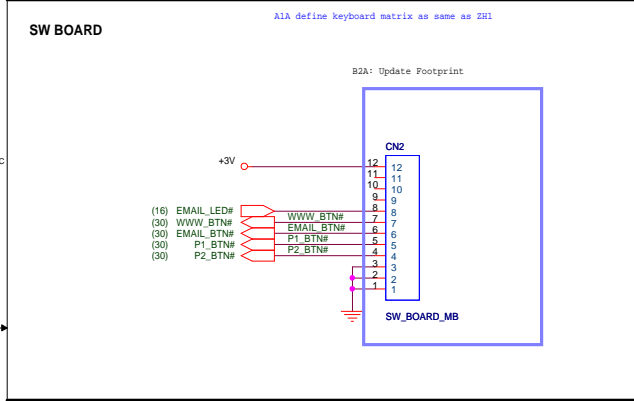
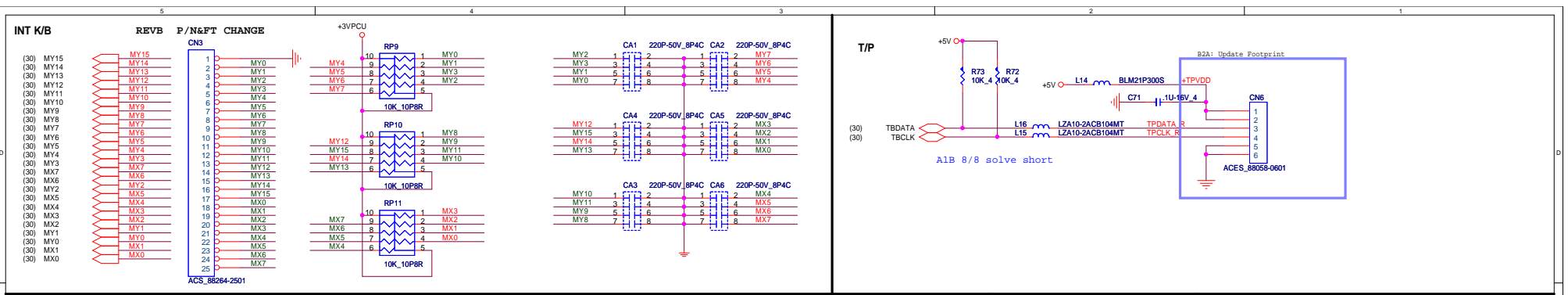


B1U configuration should match flash speed used



PROJECT : ZH5
Quanta Computer Inc.

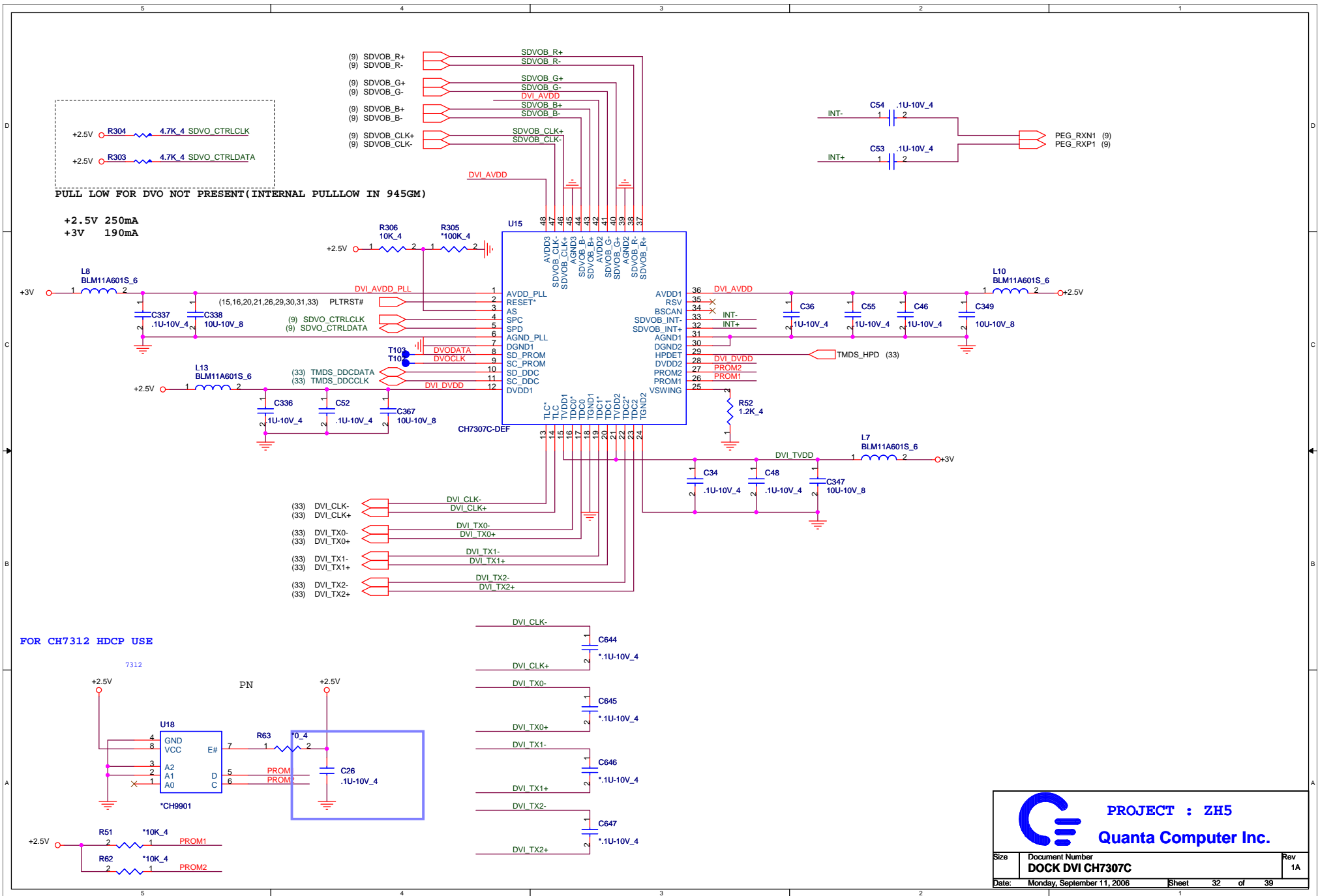
Size: Document Number: EC Controller PC97551&FLASH Rev: 1A
 Date: Friday, September 08, 2006 Sheet: 30 of 39



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Quanta Computer Inc.

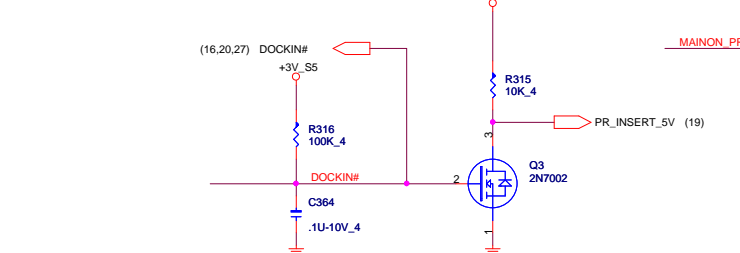
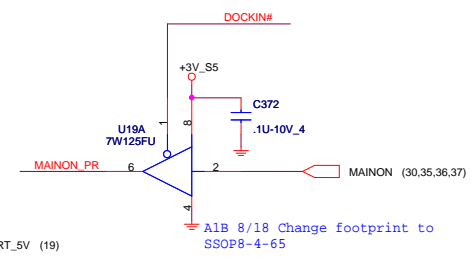
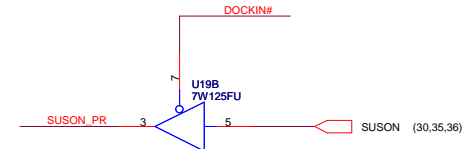
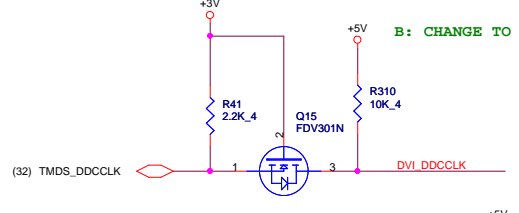
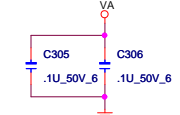
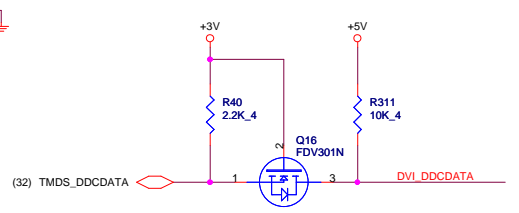
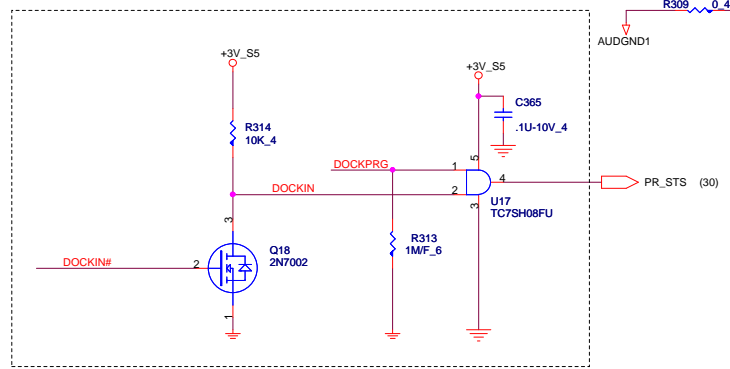
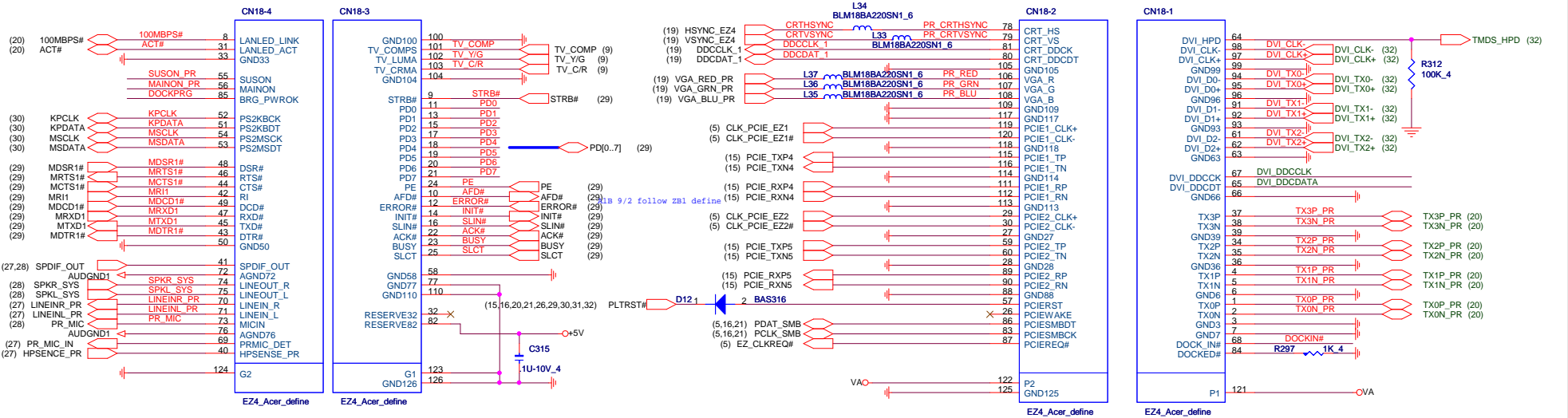
Size	Document Number	Rev
Date	SWITCH,LED,KB,TP,TPM1.2,EMI PAD	1A
Date:	Friday, September 08, 2006	Sheet 31 of 39

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Quanta Computer Inc.

Size	Document Number	Rev
	DOCK DVI CH7307C	1A
Date:	Monday, September 11, 2006	Sheet 32 of 39



SPKLR SYS	C343	220P-50V_4
SPKR SYS	C346	220P-50V_4
LINEINL_PR	C352	220P-50V_4
LINEINR_PR	C354	220P-50V_4
PR_MIC_IN	C351	47P-50V_4
PR_MIC	C340	47P-50V_4
100MBPS#	C357	1000P-50V_4
ACT#	C362	1000P-50V_4
TV_COMP	C348	10P-50V_4
TV_YG	C345	10P-50V_4
TV_C/R	C342	10P-50V_4

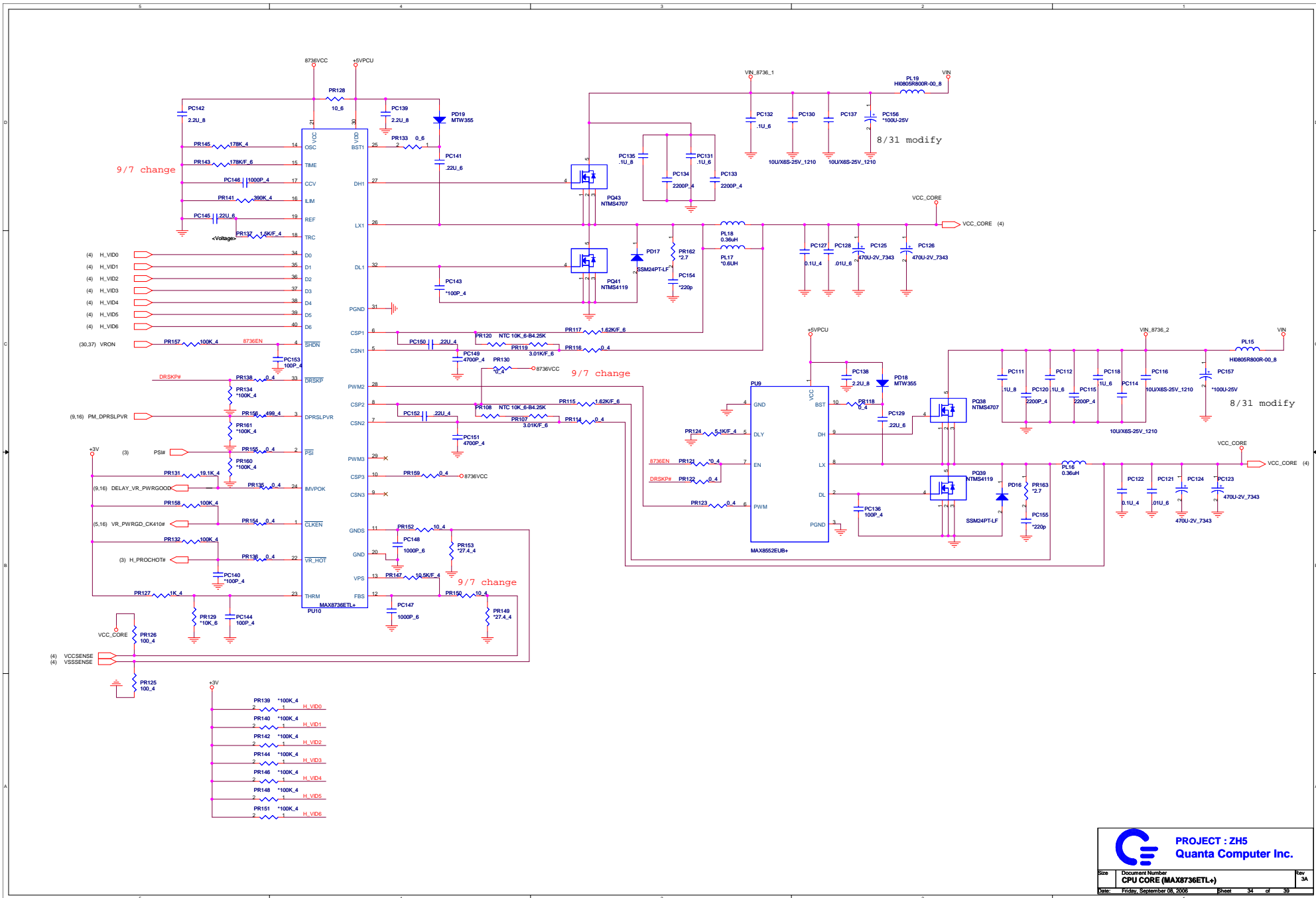
PR CRTHSYN	C331	*10P-50V_4
PR CRTVSYN	C328	*10P-50V_4
PR BLU	C332	*10P-50V_4
PR GRN	C334	*10P-50V_4
PR RED	C335	*10P-50V_4
CRTHSYN	C320	*10P-50V_4
CRTVSYN	C317	*10P-50V_4

DDCCLK_1	C318	10P-50V_4
DDCDAT_1	C319	10P-50V_4
TX3P_PR	C356	*10P-50V_4
TX3N_PR	C353	*10P-50V_4
TX2P_PR	C361	*10P-50V_4
TX2N_PR	C359	*10P-50V_4
TX1P_PR	C366	*10P-50V_4
TX1N_PR	C363	*10P-50V_4
TX0P_PR	C369	*10P-50V_4
TX0N_PR	C368	*10P-50V_4

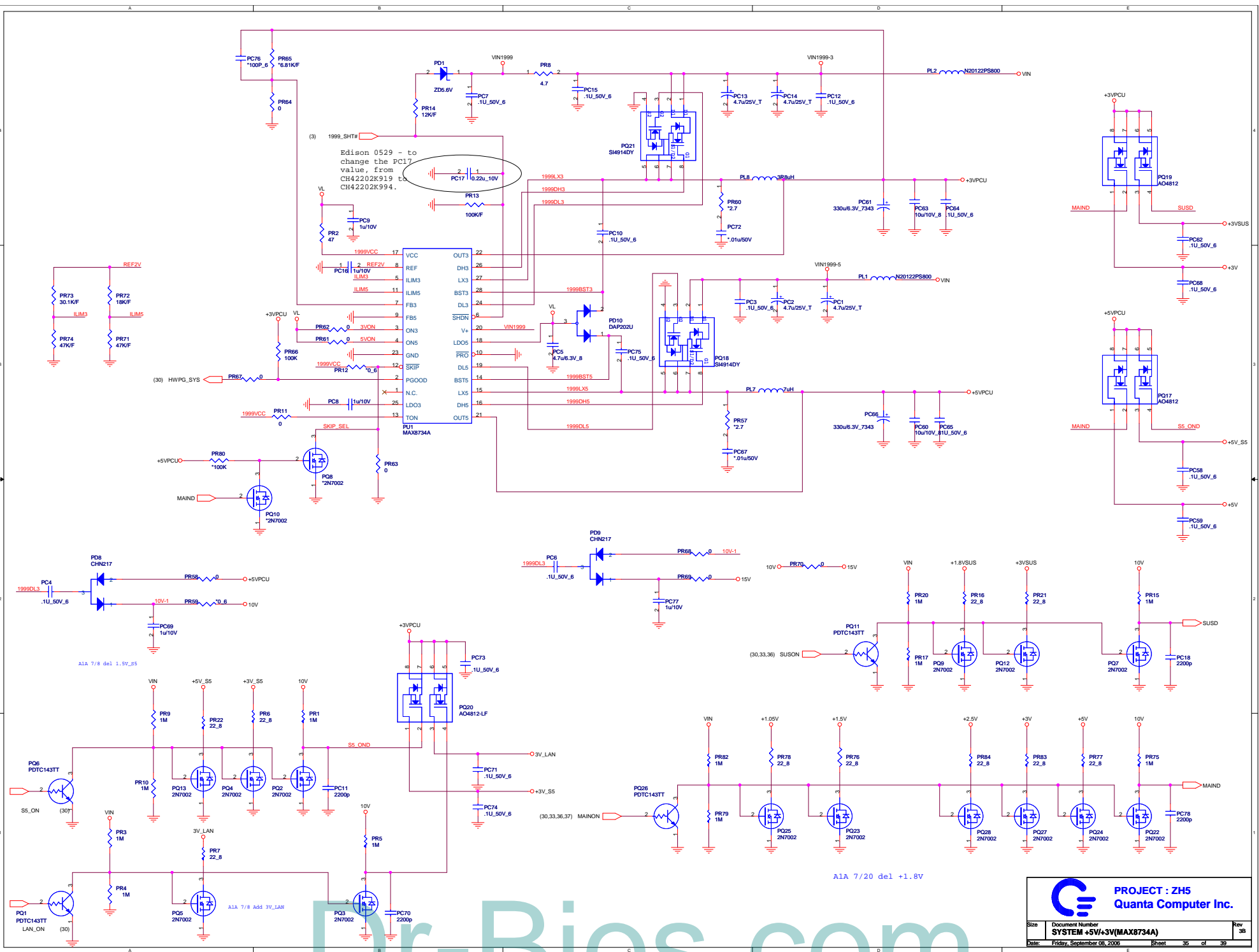
PROJECT : ZH5
Quanta Computer Inc.

Size	Document Number	Rev
	DOCK EZ4 CONNECTOR	1A
Date:	Friday, September 08, 2006	Sheet 33 of 39

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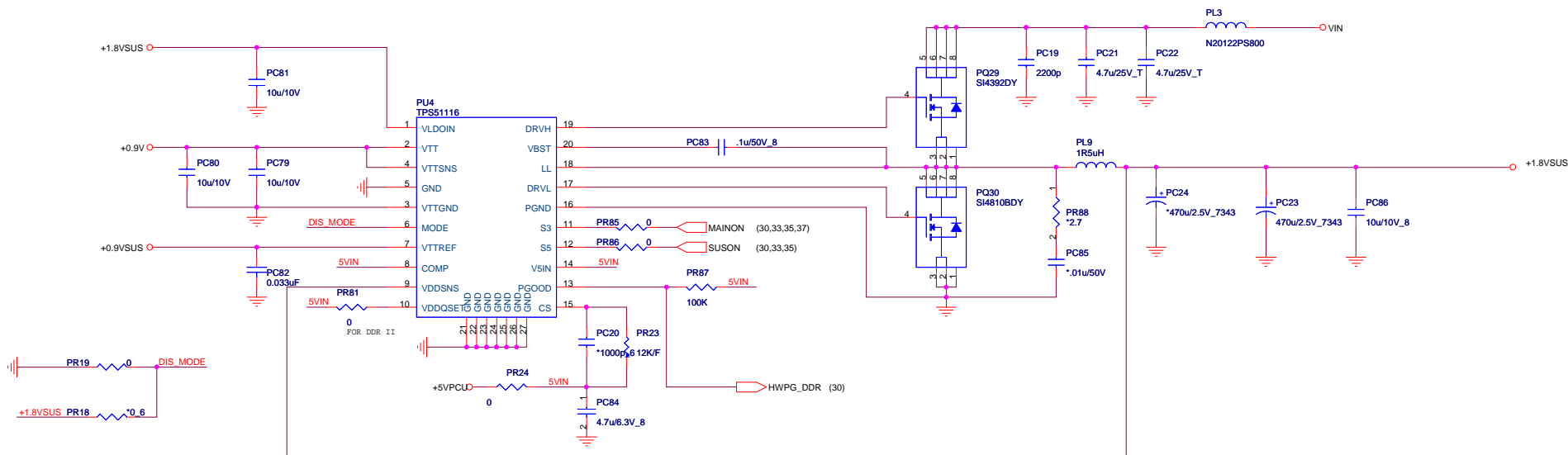
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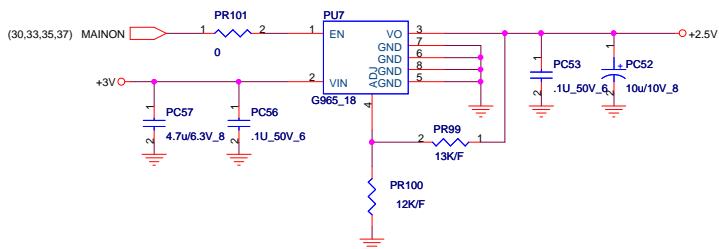
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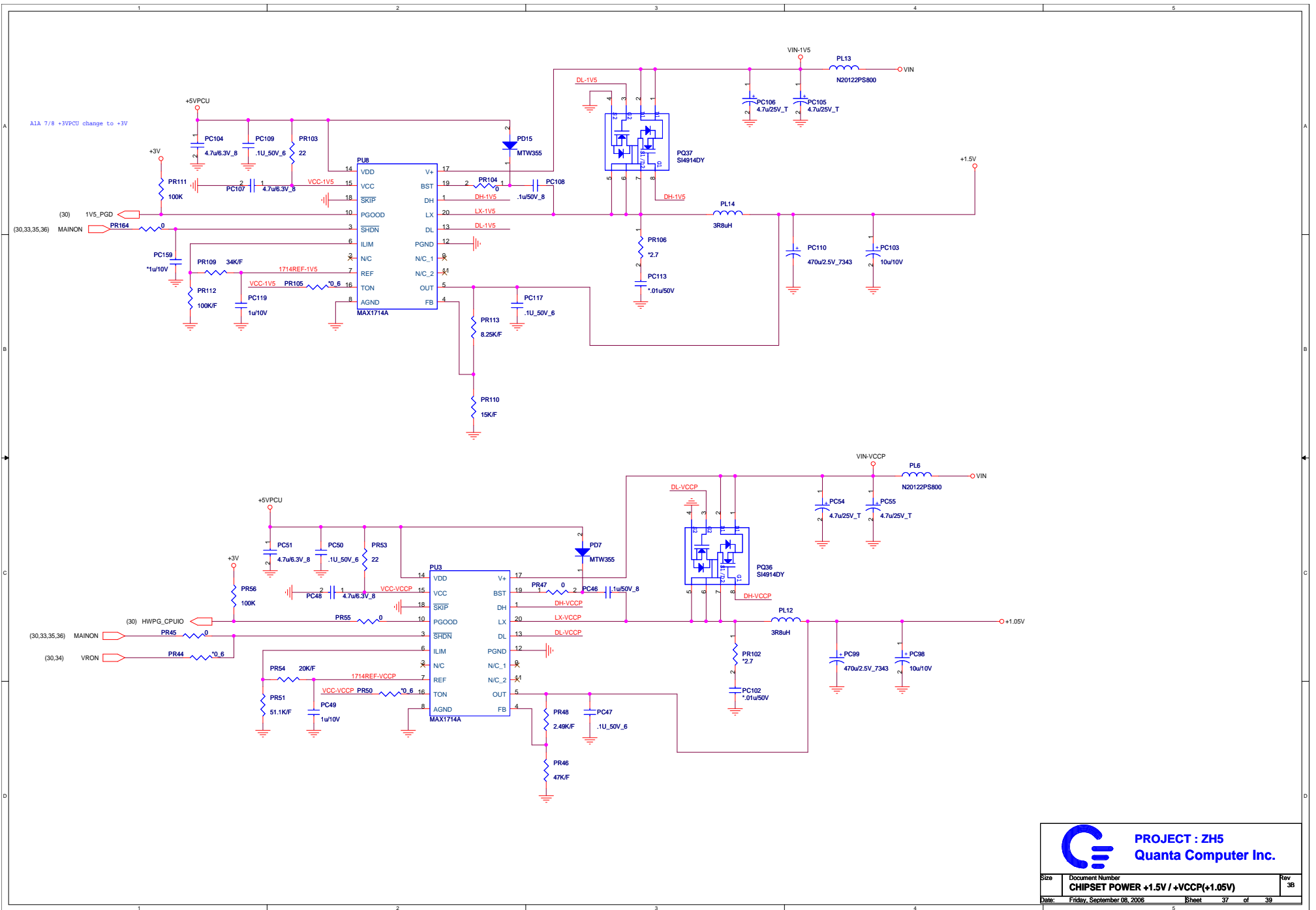
PROJECT : ZHS
Quanta Computer Inc.


Size	Document Number	Rev
	SYSTEM +5V/+3V(MAX8734A)	3B
Date:	Friday, September 08, 2006	Sheet 35 of 39

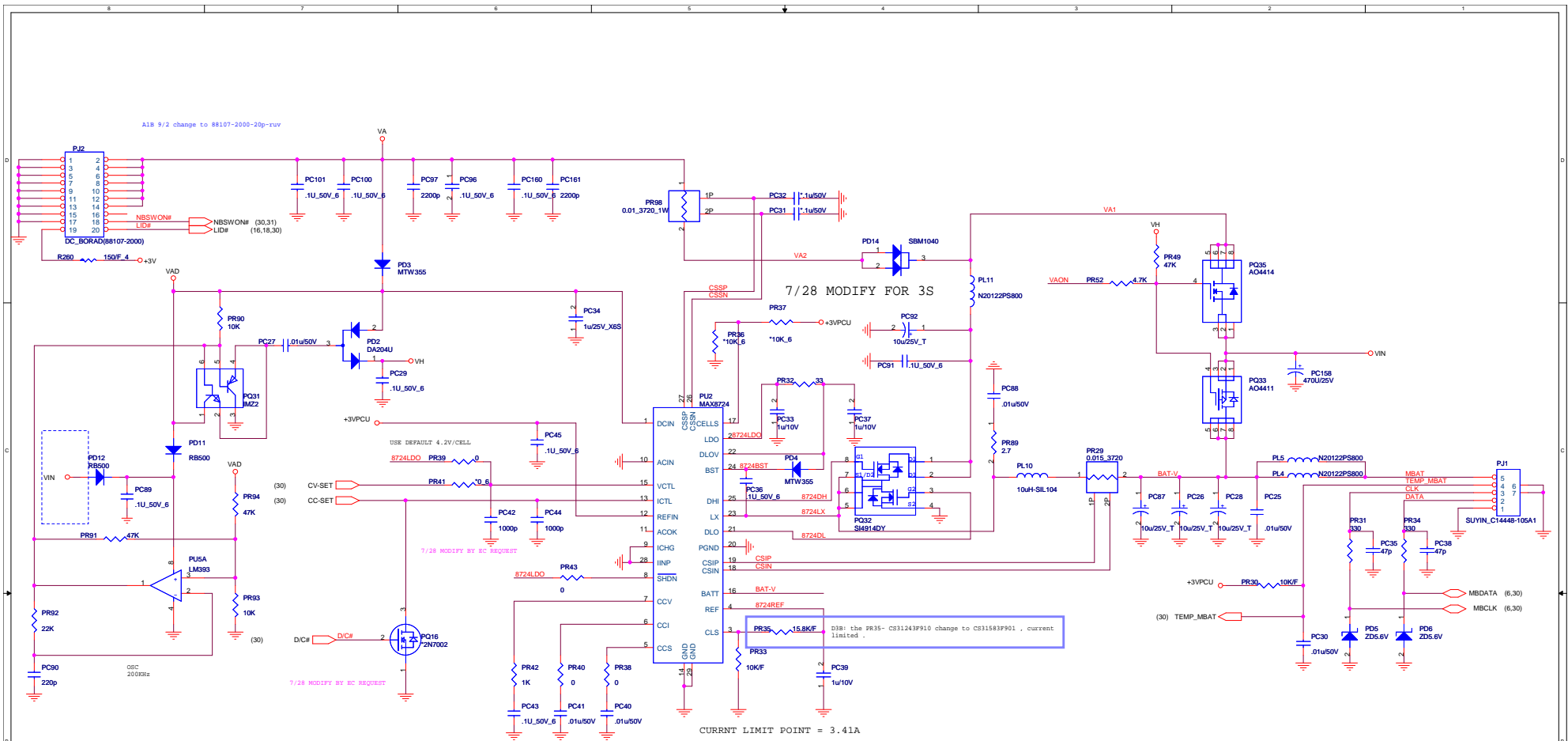


A1A 7/20 del +1.8V

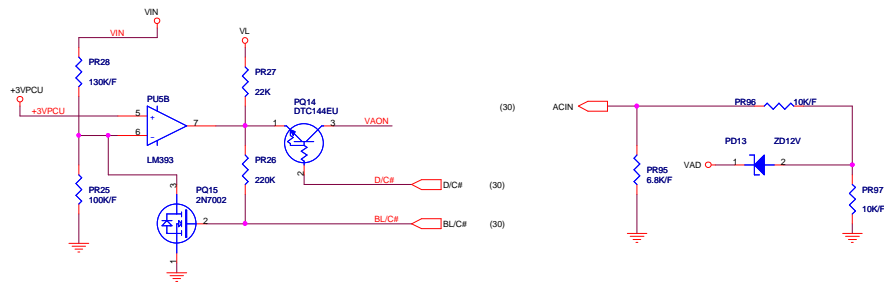




		PROJECT : ZH5	
		Quanta Computer Inc.	
Size	Document Number	Rev	38
CHIPSET POWER +1.5V / +VCCP(+1.05V)			
Date:	Friday, September 08, 2006	Sheet	37 of 39



BATTERY LOW = 7.6V



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