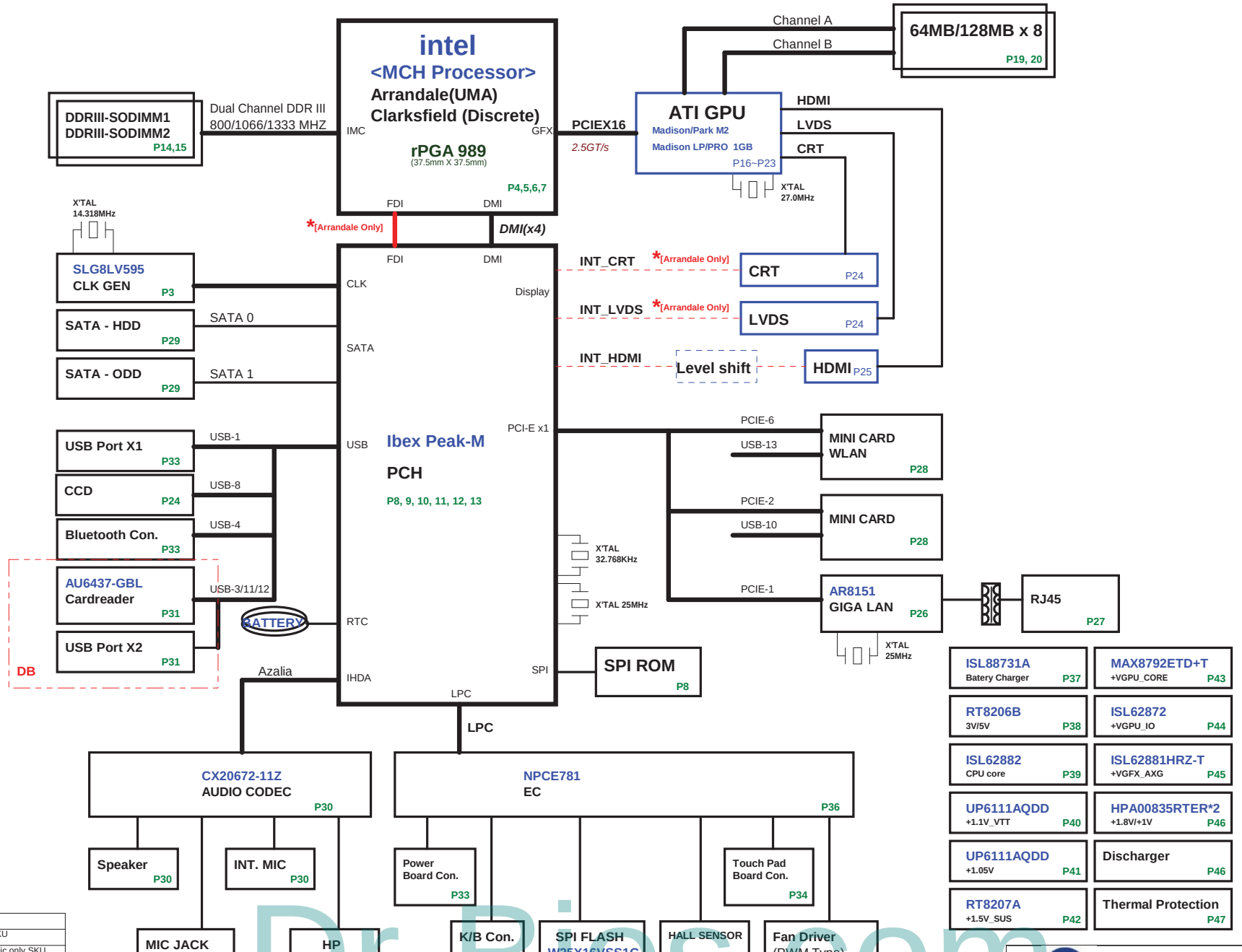
ZYD SYSTEM BLOCK DIAGRAM



BOM Option Table

Reference	Description
IV@	for UMA only SKU
EV@	for Discrete Graphic only SKU
SP@	special case component
*	do not stuff

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Block Diagram
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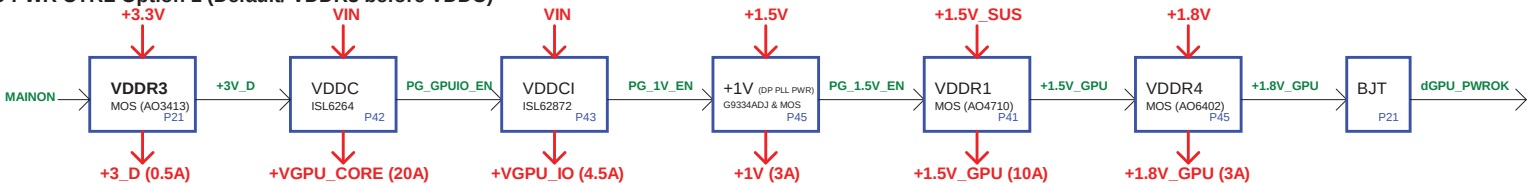
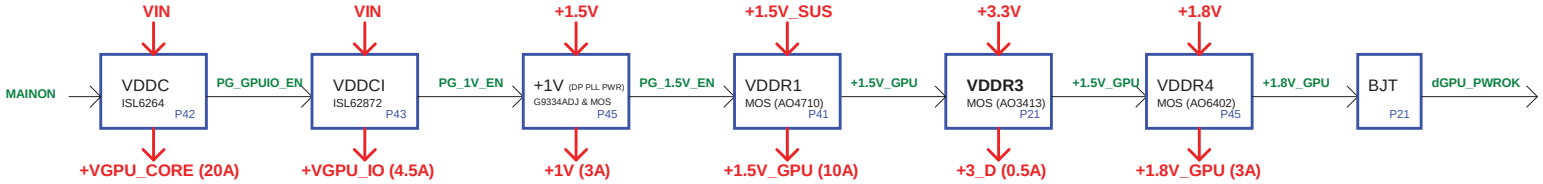
GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDC)



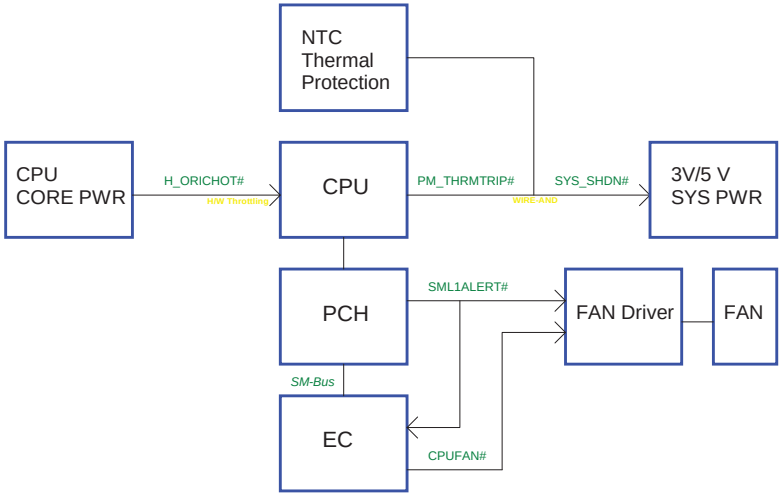
GPU PWR CTRL Option 2 (VDDR3 after VDDR1)



Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+VCCRTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT/PCH	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT	MAINON	S0
+3V	+3.3V	CLK GEN/PCH/GPU/LVDS/Mini card/Codec/card reader	MAINON	S0
+1.5V_SUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+VGFX_AXG	variation	Internal GPU POWER	GFX_ON	S0
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.1V_VTT	+1.05V or +1.1V	CPU VTT POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE POWER	MAINON	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+5V_GPU	+5V	SWITCHABLE PWM IC POWER	dGPU_PWR_EN#	Discrete enable
+3V_D	+3.3V	I/O POWER for 3.3V pins	dGPU_VRON	Discrete enable
+VGPU_CORE	+0.9V~+1.1V	GPU CORE POWER	+3V_D	Discrete enable
+VGPU_IO	+0.9V~+1.1V	GPU I/O POWER	PG_GPUIO_EN	Discrete enable
+1V	+1V	DP/PEG POWER	PG_1V_EN	Discrete enable
+1.5V_GPU	+1.5V	VRAM CORE POWER	PG_1.5V_EN	Discrete enable
+1.8V_GPU	+1.8V	GPU_CRE/LVDS/PLL POWER	+1.5V_GPU	Discrete enable

Thermal Follow Chart



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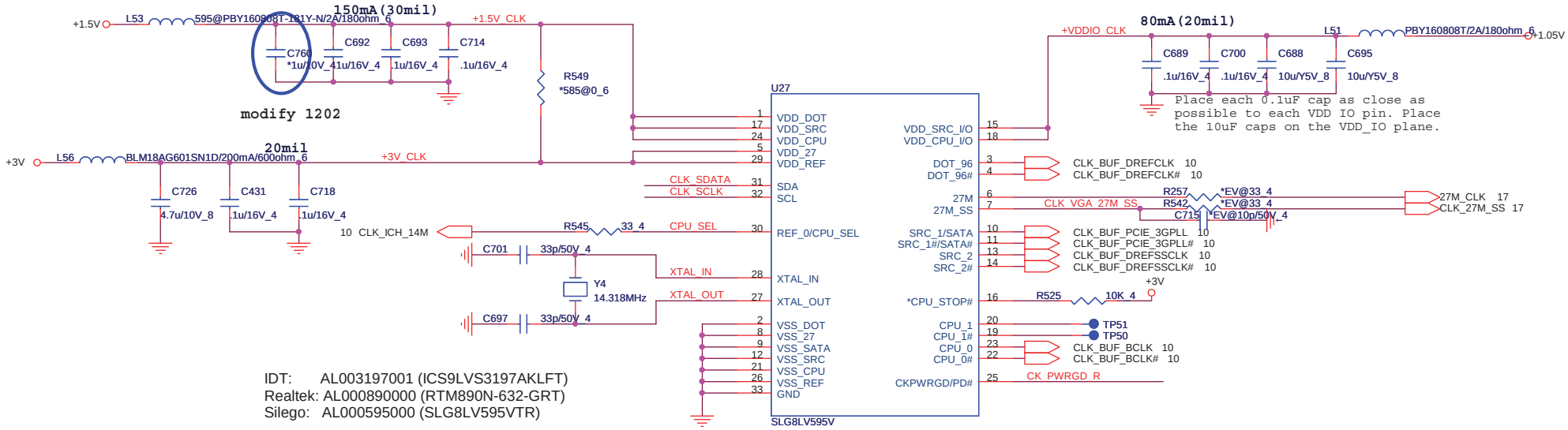
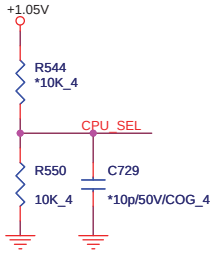


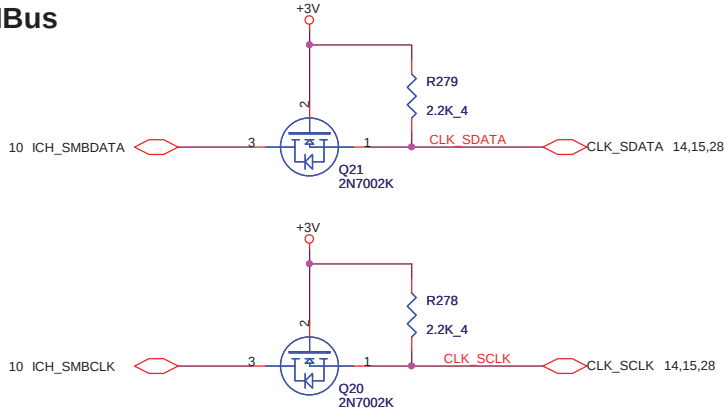
IDT: AL003197001 (ICS9LVS3197AKLFT)
Realtek: AL000890000 (RTM890N-632-GRT)
Silego: AL000595000 (SLG8LV595VTR)

CPU_CLK select

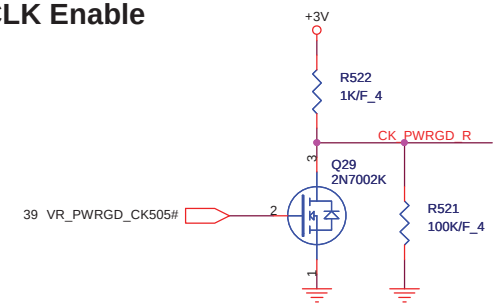


	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

SMBus



CLK Enable



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	Clock Generator	3B
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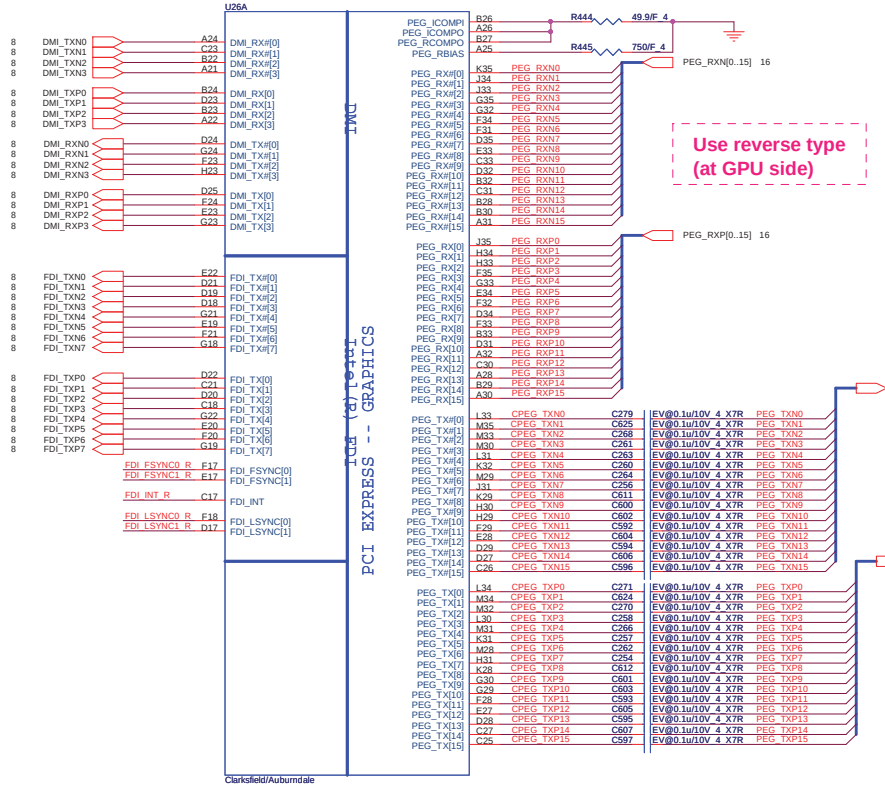
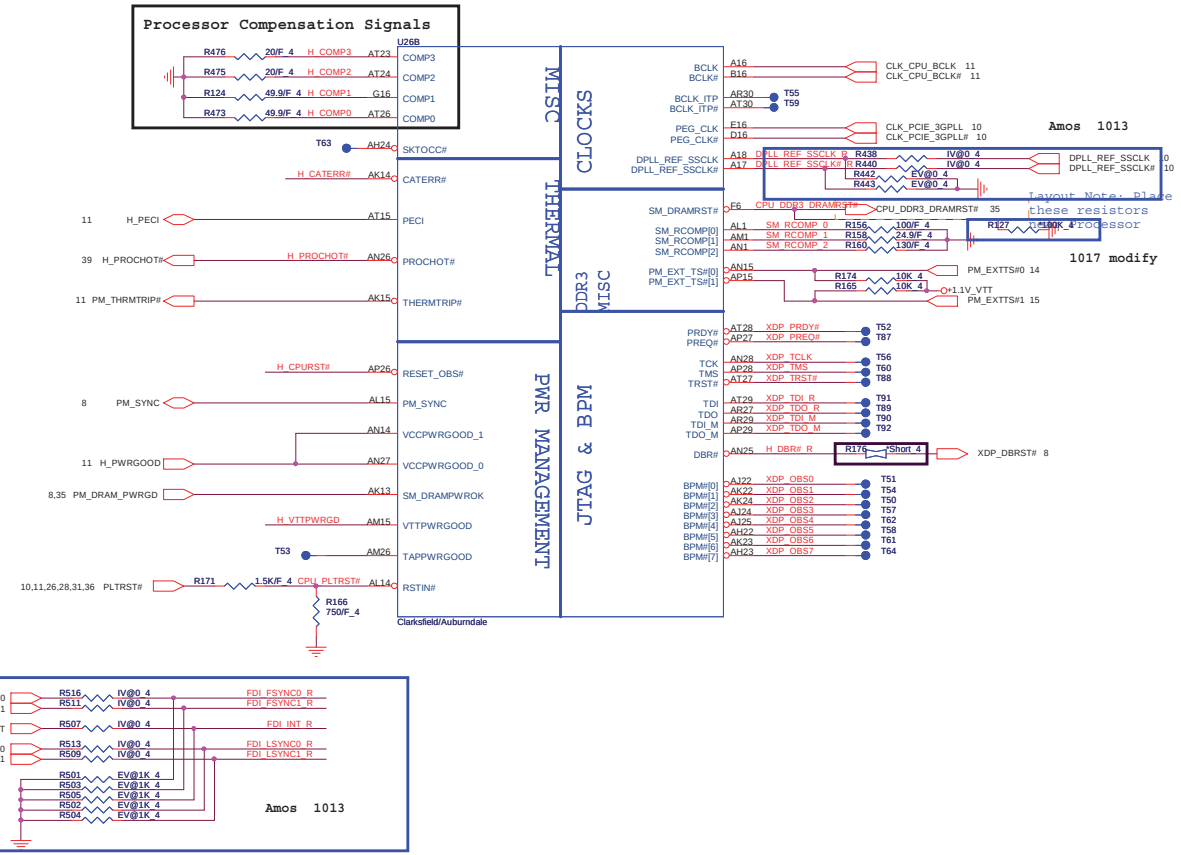
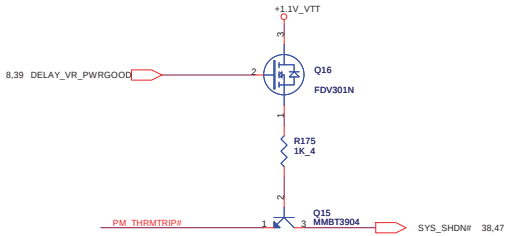
AUBURNDALE/CLARKSFIELD PROCESSOR (DMI,PEG,FDI)



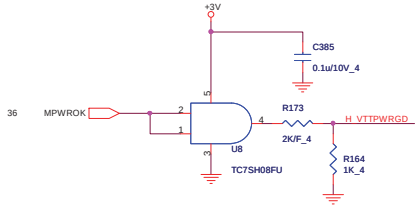
AUBURNDALE/CLARKSFIELD PROCESSOR (CLK,MISC,JTAG)



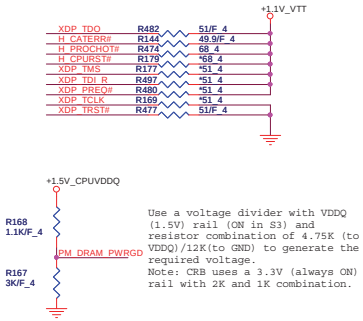
Thermaltrip protect



VTT PWR_Good

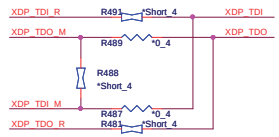


Processor pull-up



PM_DRAM_PWRGD:
Never drive hight before DDR3 voltage ramp to stable

JTAG MAPPING



Scan Chain (Default)	STUFF -> R469, R491, R507 NO STUFF -> R489, R490
CPU Only	STUFF -> R490, R491 NO STUFF -> R469, R489, R507
GMCH Only	STUFF -> R489, R507 NO STUFF -> R491, R490, R469

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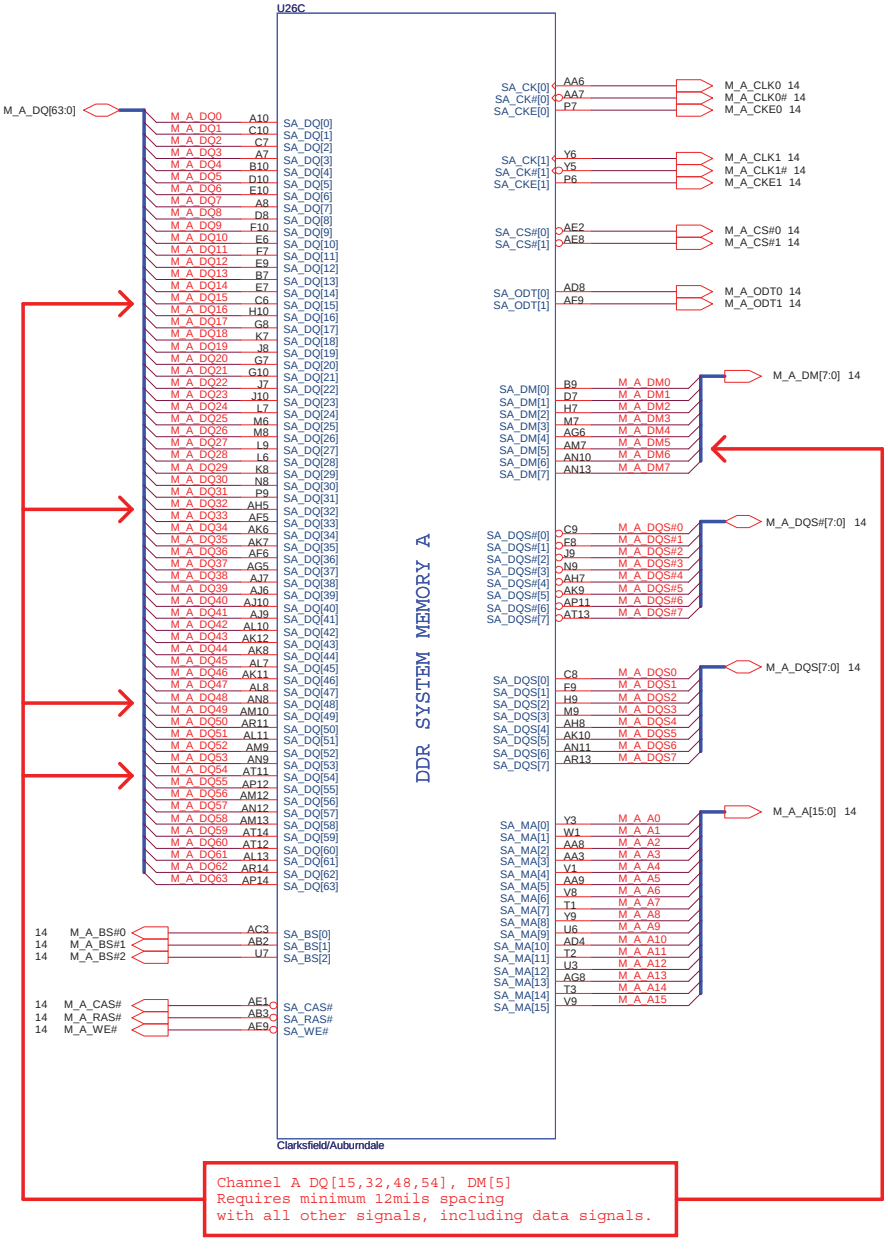
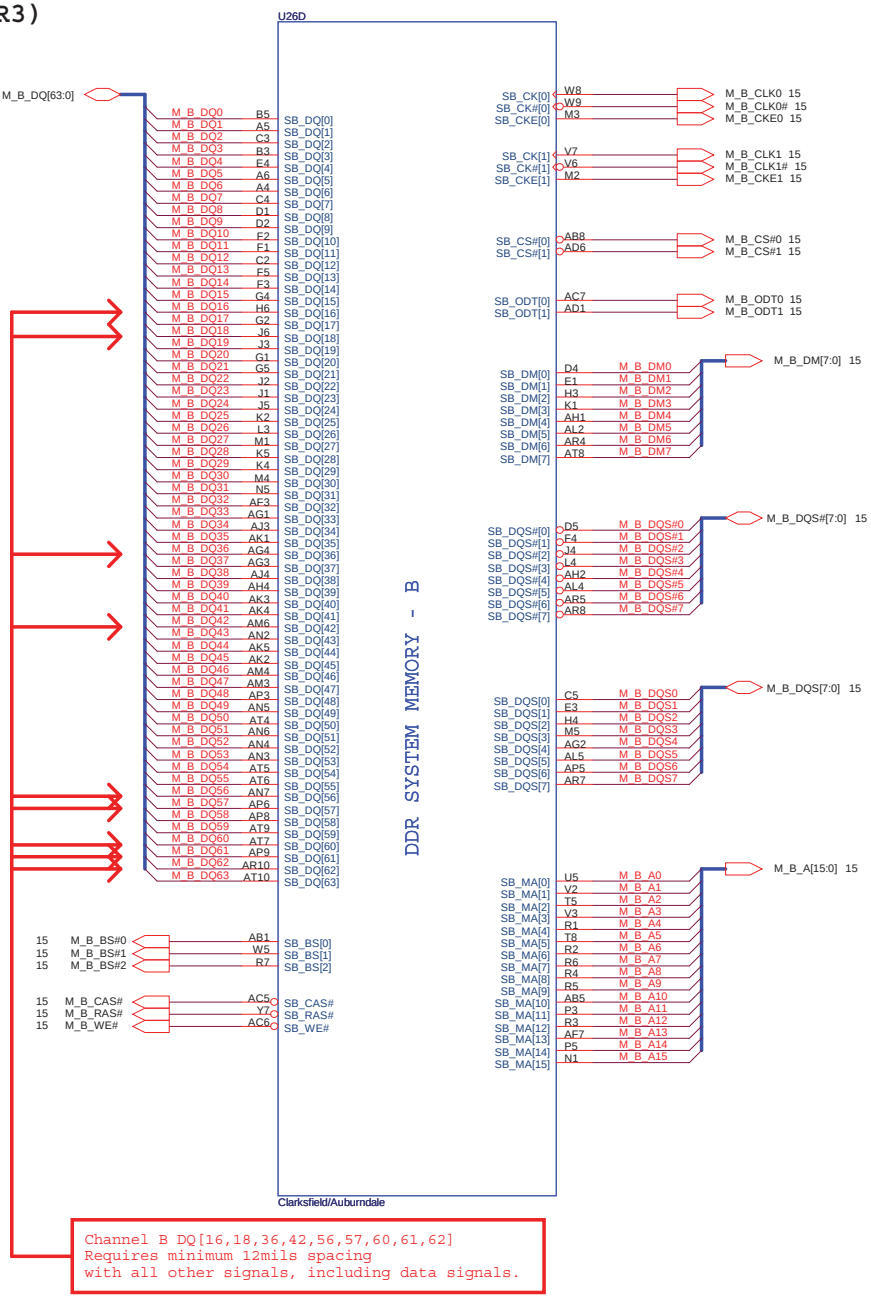
AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)





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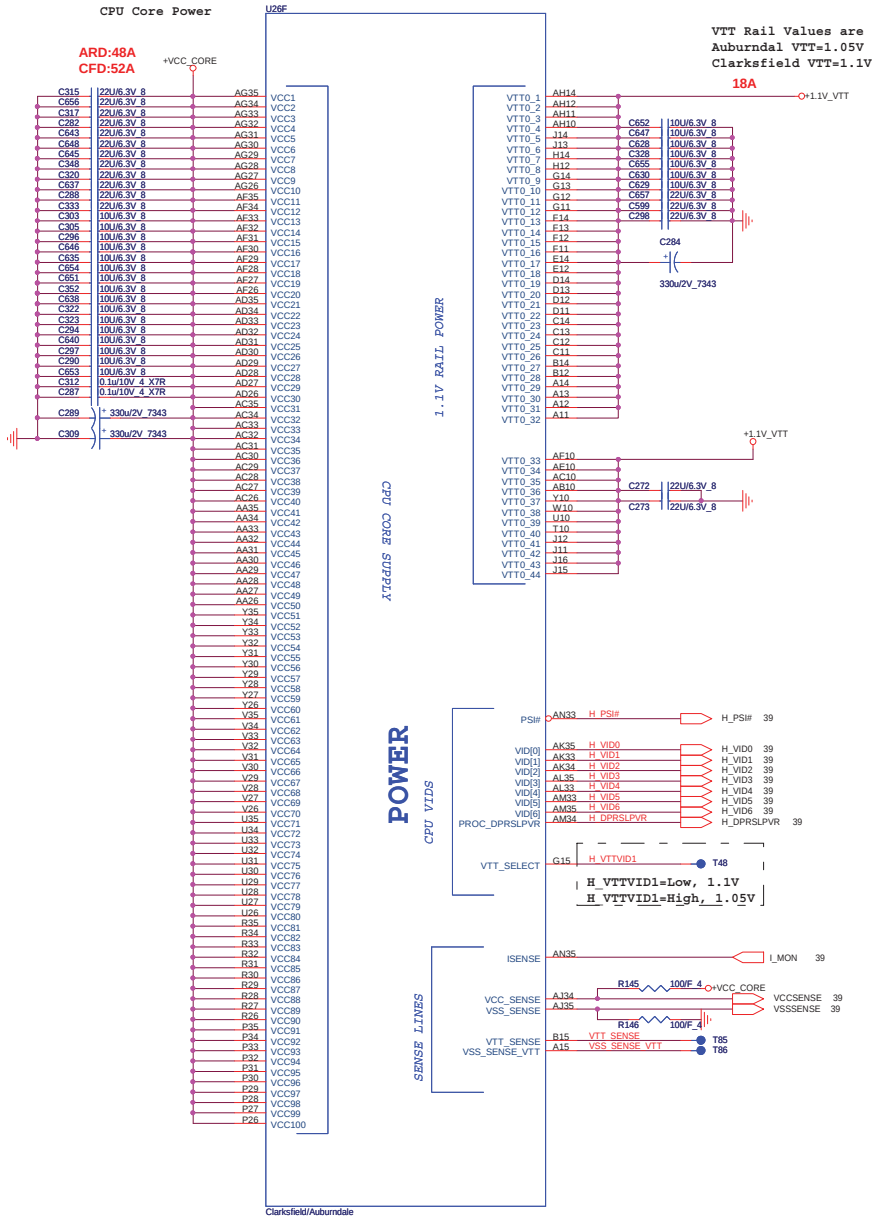
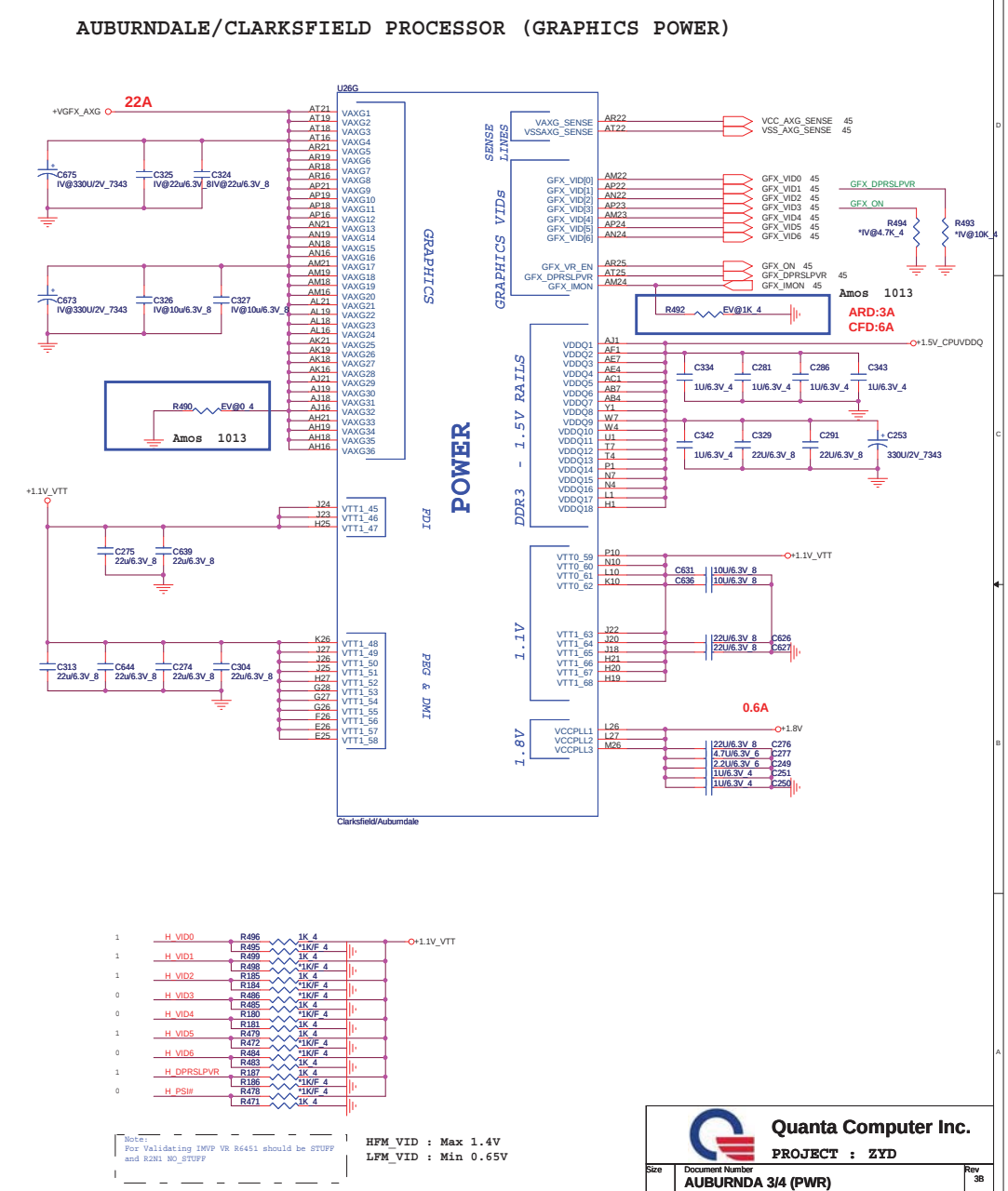


AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)



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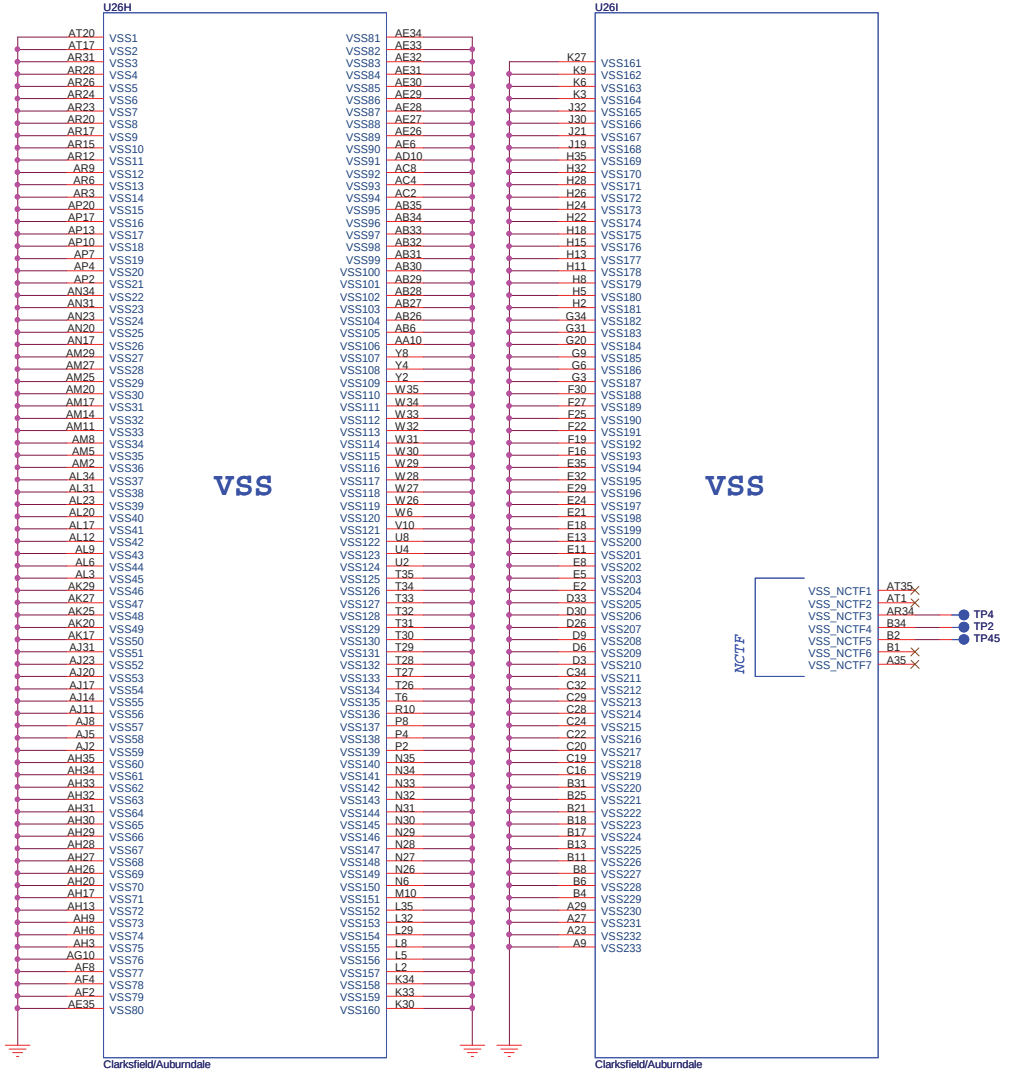
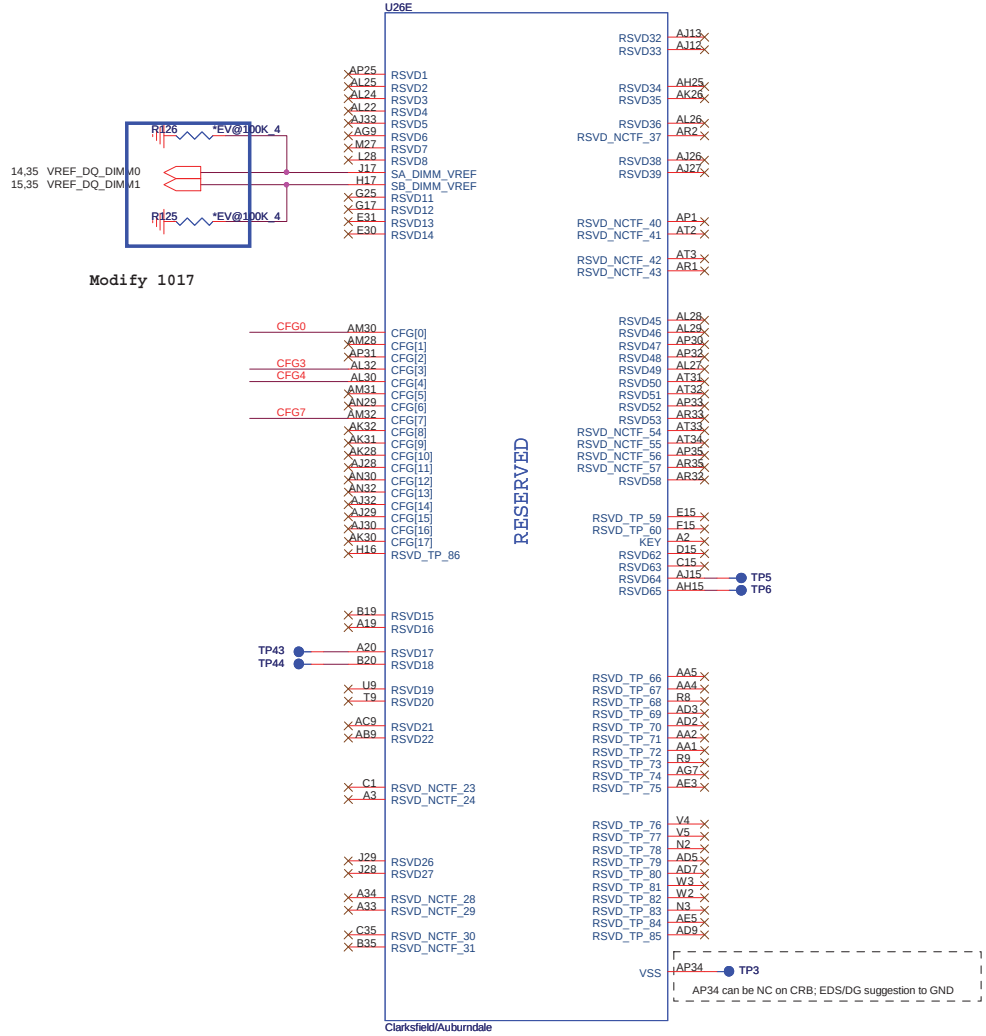
AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



Processor Strapping

	1	0	DEFAULT	
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled	1	CFG0 R172 *3.01K_NC
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed	1	CFG3 R159 *3.01K/F_4
CFG4 (Embended Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port	1	CFG4 R157 *3.01K
Thermal Monitor 2 Enable	Enabled	Disabled	1	CFG7 R161 *3.01K/F_4

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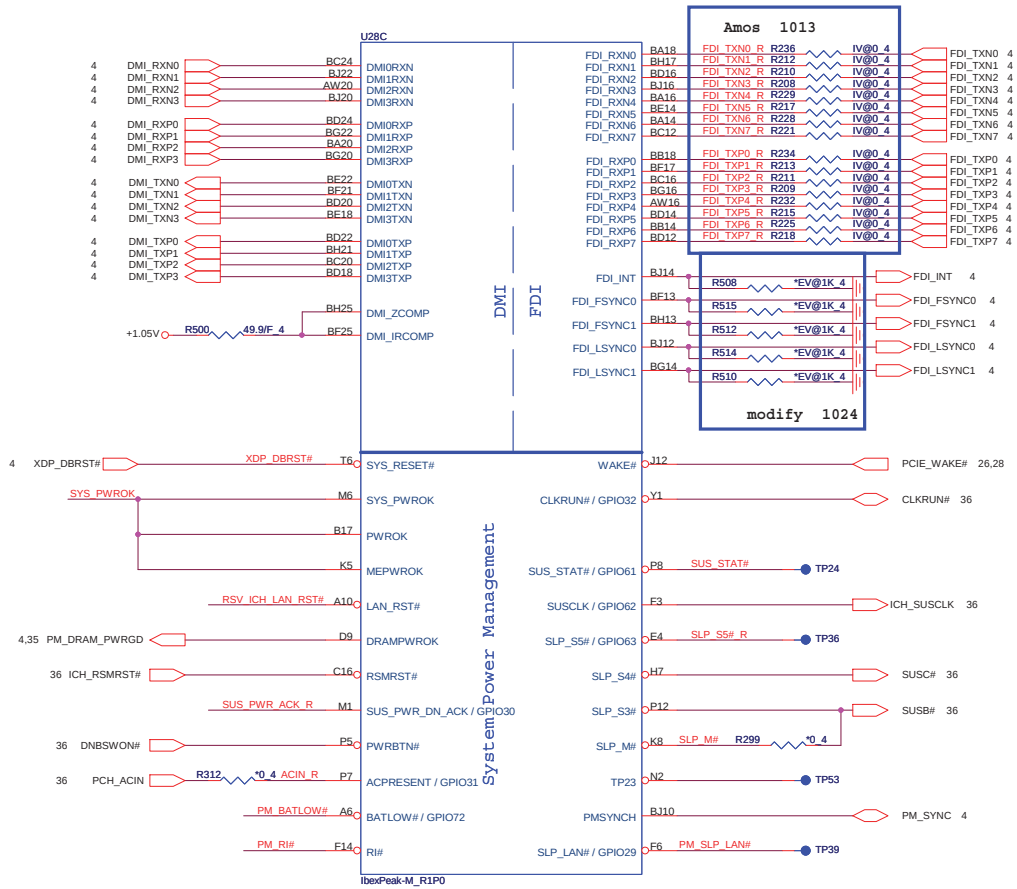
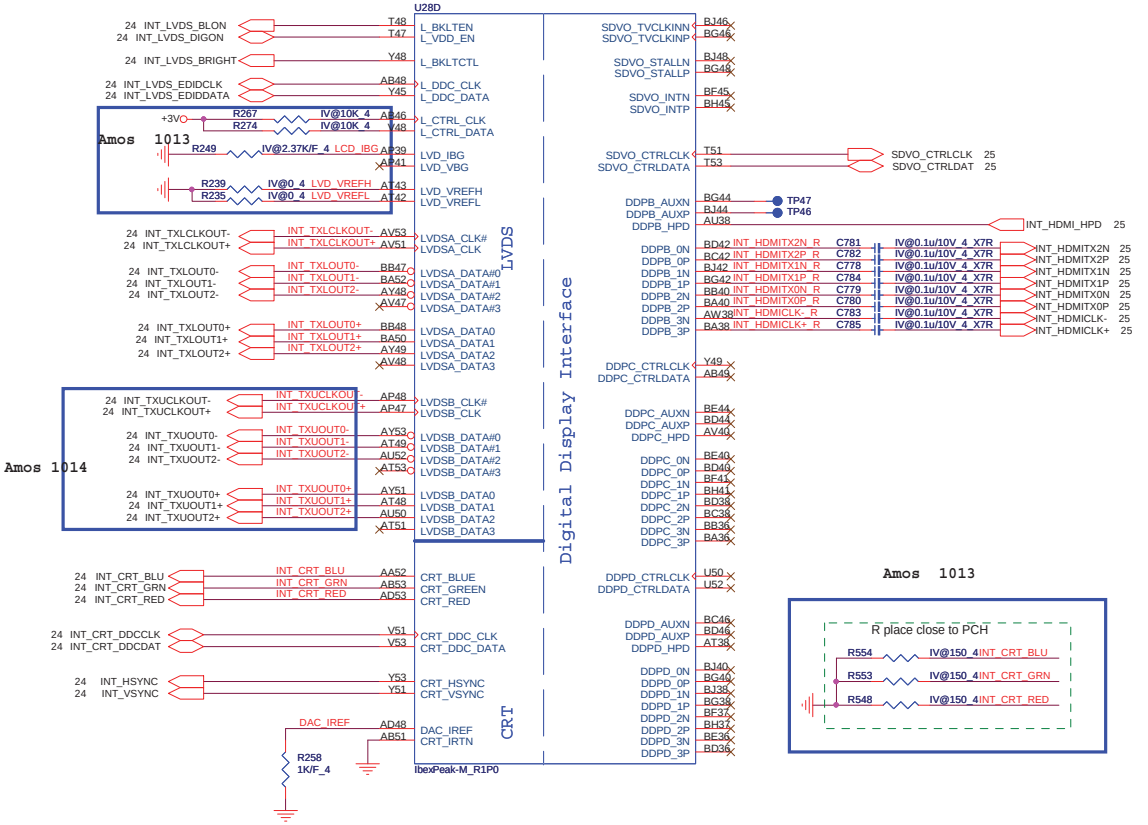
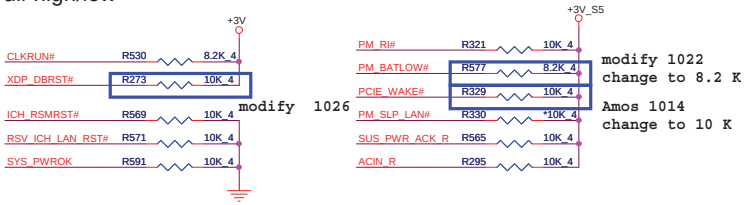
IBEX PEAK-M (DMI,FDI,GPIO)



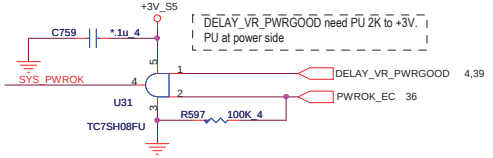
IBEX PEAK-M (LVDS,DDI)



PCH Pull-high/low



System PWR_OK



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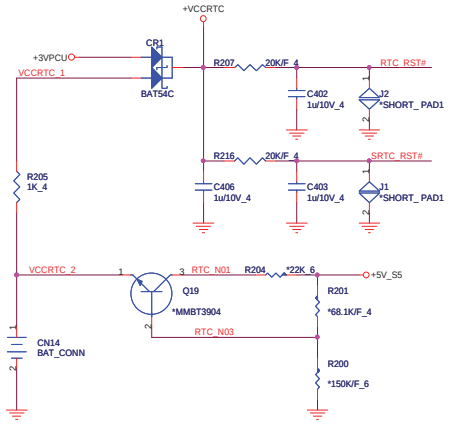
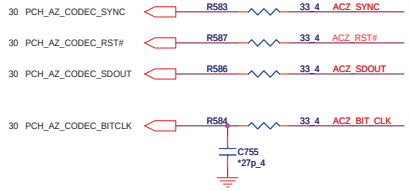
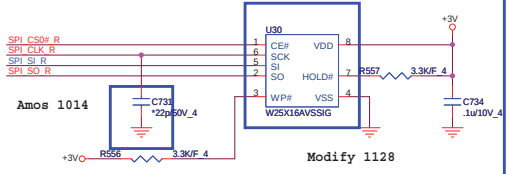
RTC Circuitry



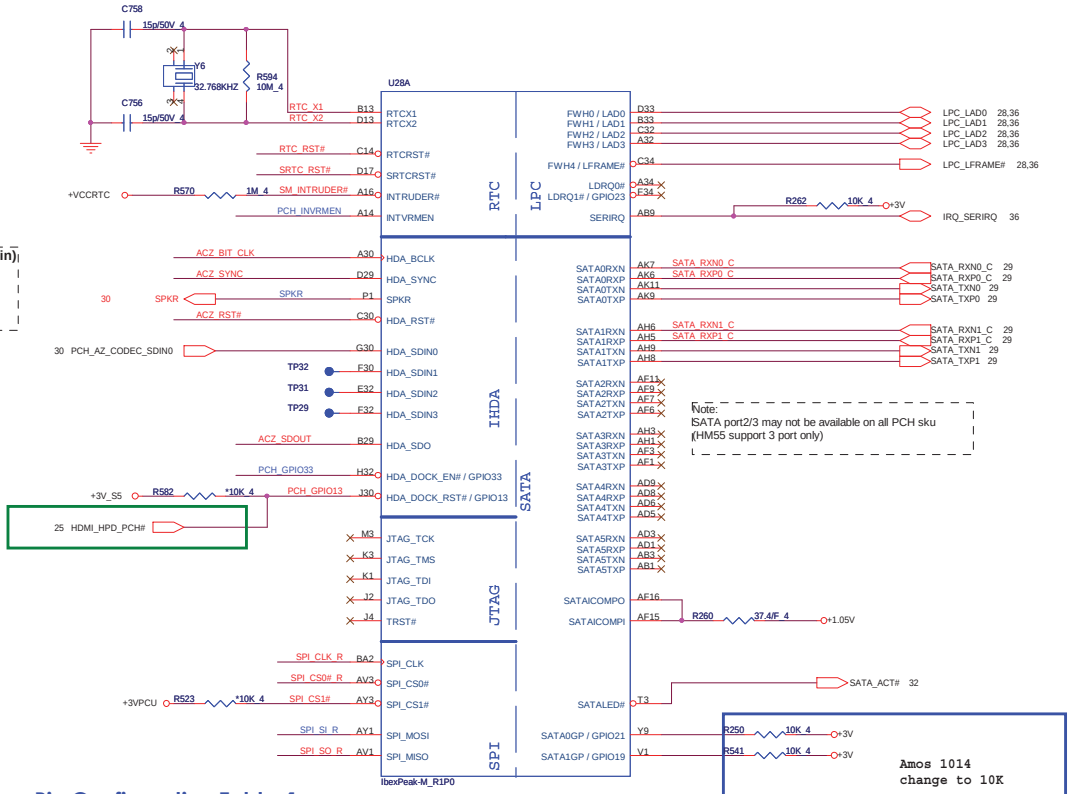
HDA Bus



MDC Bus



PCH SPI



HDA_SYNC (PCH strap pin)

Internal weak pull-down
VCCVRM=>+1.8V (default)
external pull-up
VCCVRM=>+1.5V

Note:
SATA port2/3 may not be available on all PCH sku
(HM55 support 3 port only)

PCH Strap Pin Configuration Table-1

INTVRMEN	Integrated 1.05V VRM Enable / Disable	1 = Integrated VRM is enabled 0 = Integrated VRM is disabled	+VCCRTC R593 330K_6 PCH_INVRMEN
SPI_MOSI	TPM Functionality Disable	1 = Enabled 0 = Disable	+3V R559 *1K_4 SPI_SI_R
SPKR	Reboot option at power-up	0 = Default Mode (Internal weak Pull-down) 1 = No Reboot Mode with TCO Disabled	+3V R307 *1K/F_4 SPKR
HDA_DOCK_EN #/GPIO33	Flash Descriptor Security Override	0 = Flash Descriptor Security will be overridden 1 = Security measure defined in the Flash Descriptor will be enabled.	PCH_GPIO33 J3 *SHORT_PAD1 R322 10K_4 +3V
GNT0#, GNT1#	Boot BIOS Strap	(0,0) = LPC (0,1) = Reserved NAND (1,0) = PCI (1,1) = SPI	10 PCI_GNT0# R315 1K_4 10 PCI_GNT1# R310 1K_4
GNT2#/ GPIO53	ESI Strap (Server Only)	ESI compatible mode is for server platforms only Modify 1019	10 PCI_GNT2# R313 *1K/F_4
GNT3#/ GPIO55	Top-Block Swap Override	0 = Top Block Swap Mode 1 = Default Mode (Internal pull-up)	10 PCI_GNT3# R560 *10K/F_4
NV_ALE	IntelR Anti-Theft Technology HDD Data Protection (Intel AT-d) Enable	1 = Enabled 0 = Disabled (Default)	10 NV_ALE R231 *1K/F_4 +1.8V
NV_CLE	DMI Termination Voltage	DMI termination voltage. Weak internal pull-up. Do not pull low.	10 NV_CLE R230 *1K/F_4 +1.8V

GPIO8	Reserved	This signal has a weak internal pull up. NOTE: This signal should not be pulled low	11 RSV_GPIO8 R325 10K_4 +3V_S5 R320 *1K_4
GPIO15	Reserved	0 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality	11 CR_WAKE# R282 1K_4 +3V_S5
GPIO27	On-Die PLL Voltage Regulator <internal weak pull-up>	0 = Disables the VccVRM. 1 = Enables the internal VccVRM to have a clean supply for analog rails.	11 PCH_GPIO27 R263 *10K_4

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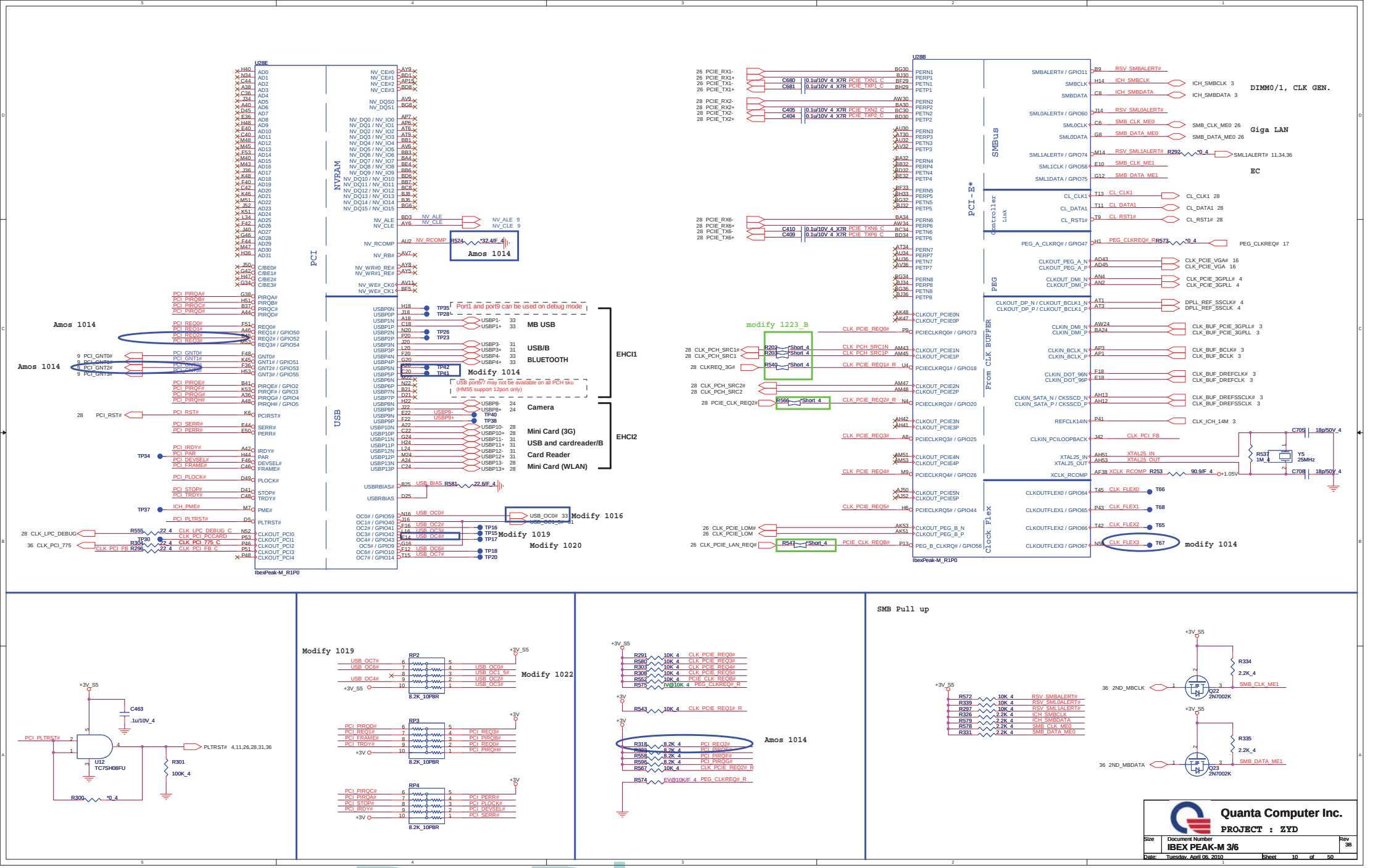

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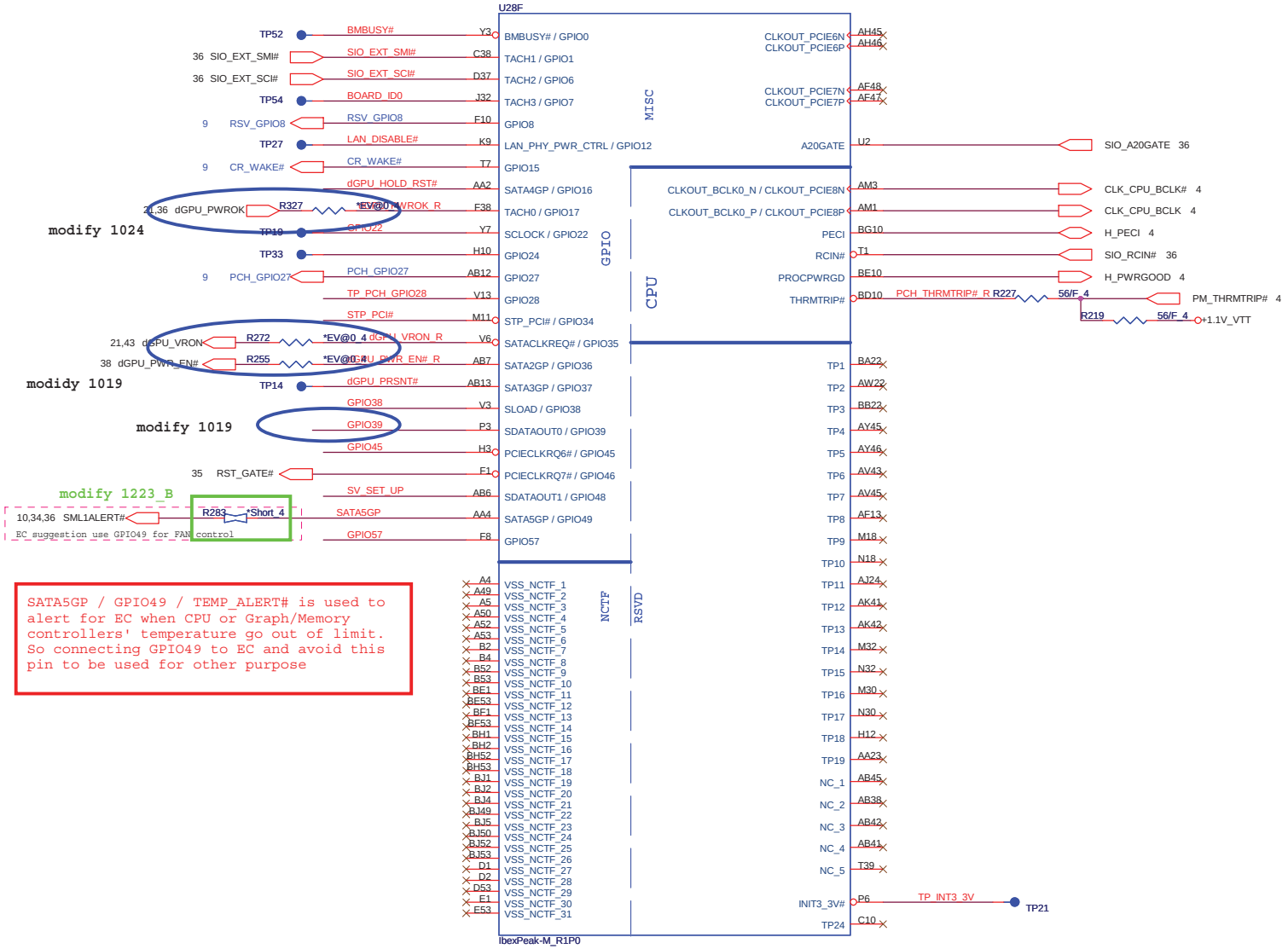
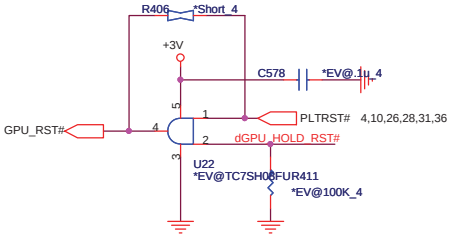
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

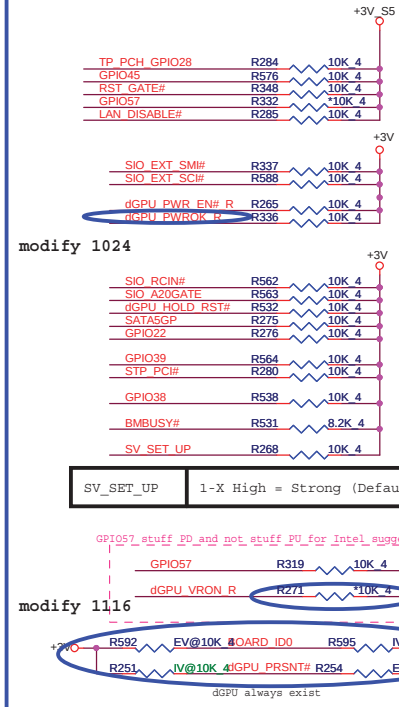


SATA5GP / GPIO49 / TEMP_ALERT# is used to alert for EC when CPU or Graph/Memory controllers' temperature go out of limit. So connecting GPIO49 to EC and avoid this pin to be used for other purpose

GPU RST#



GPIO Pull-up/Pull-down



SV_SET_UP	1-X High = Strong (Default)

modify 1116

Integrated Clock Chip Enable	
BOARD_ID0	High = Discrete Low = IV
RSV_GPIO8	High = Disable Low = Enable

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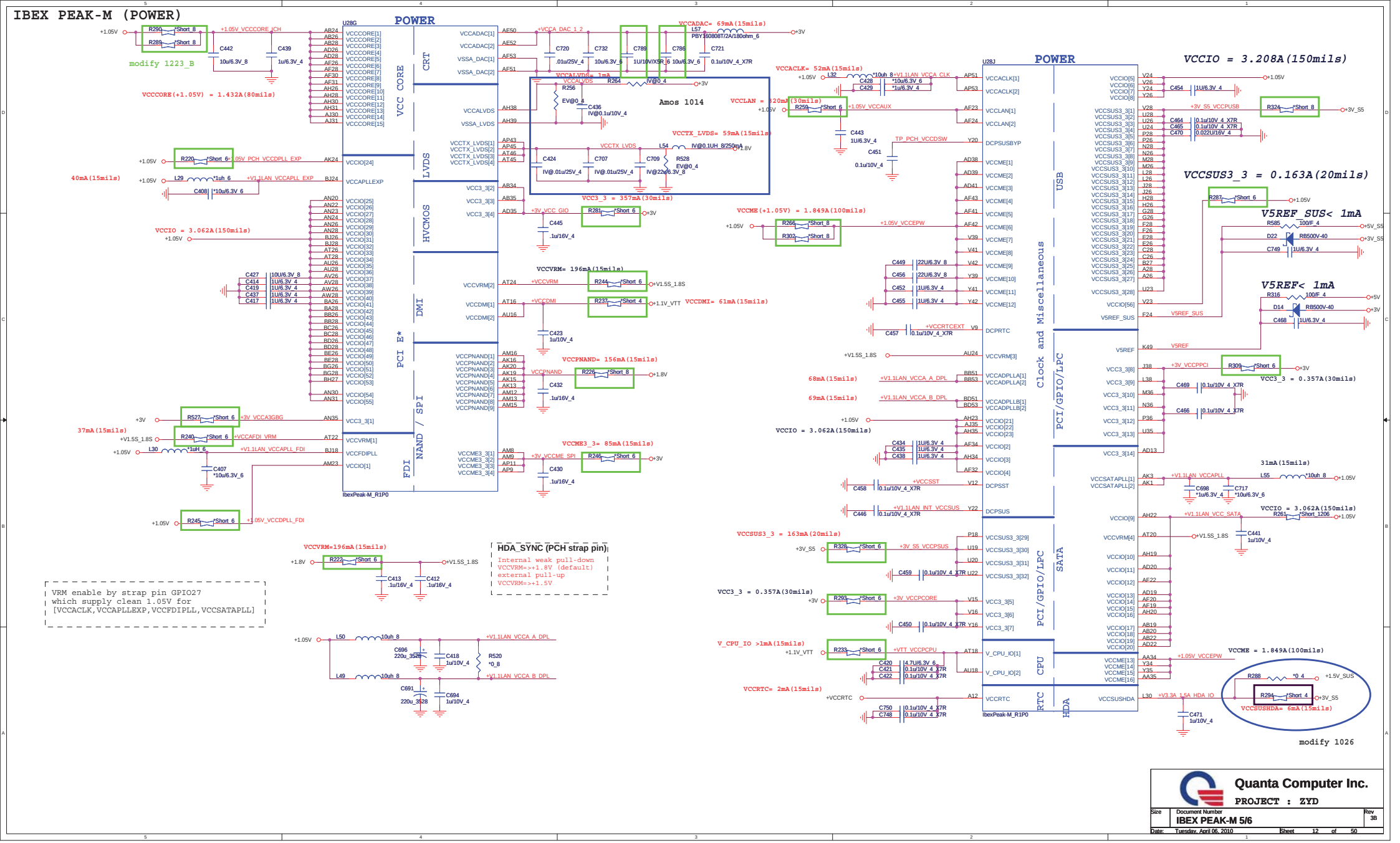
IBEX PEAK-M (POWER)



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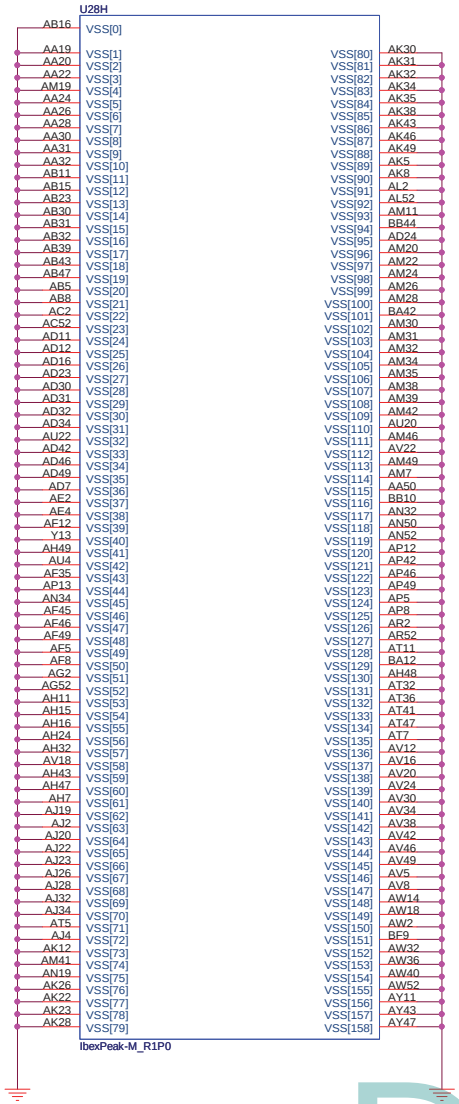
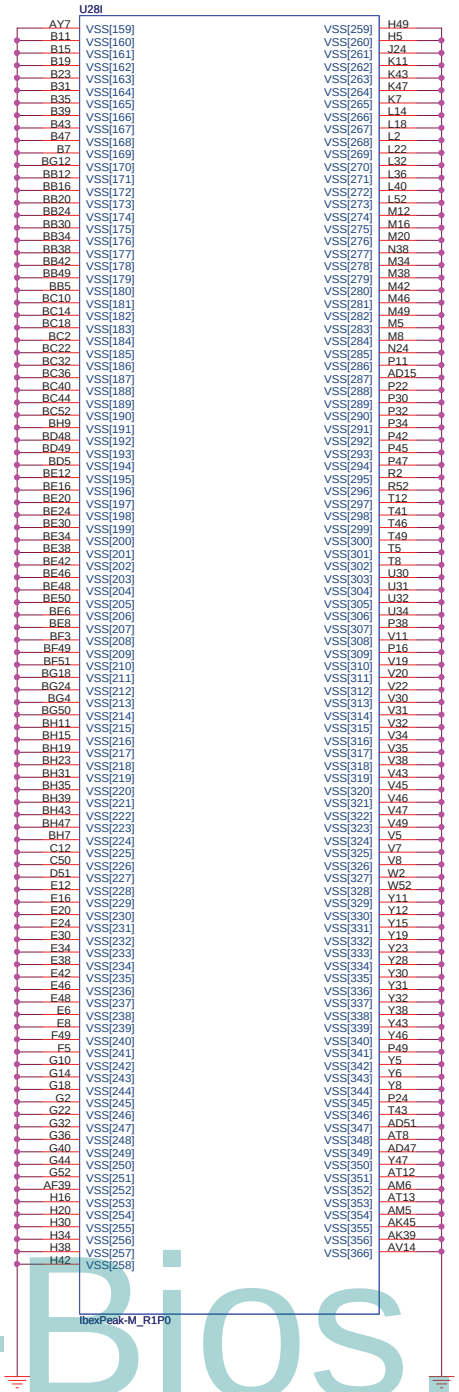
IBEX PEAK-M (GND)





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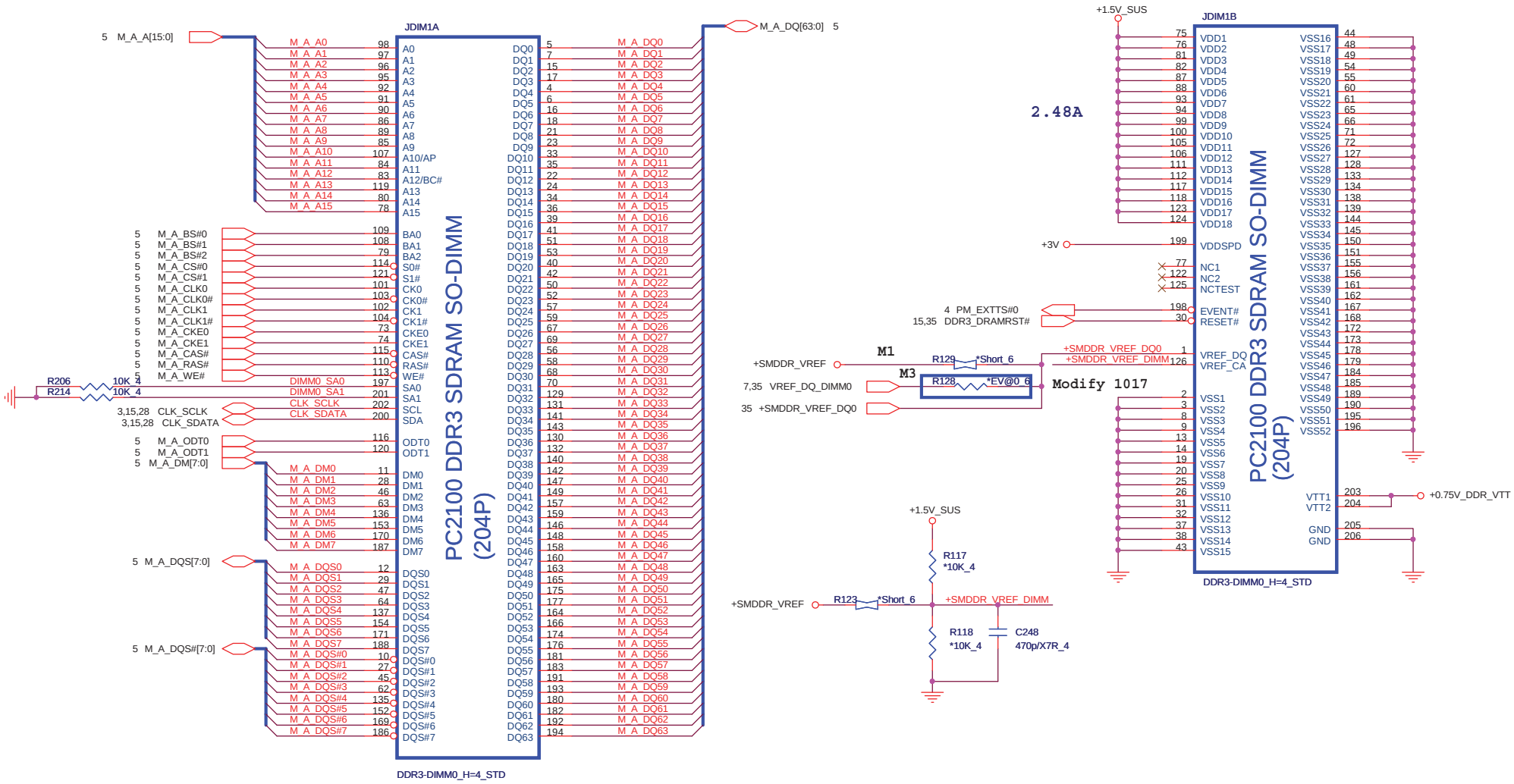
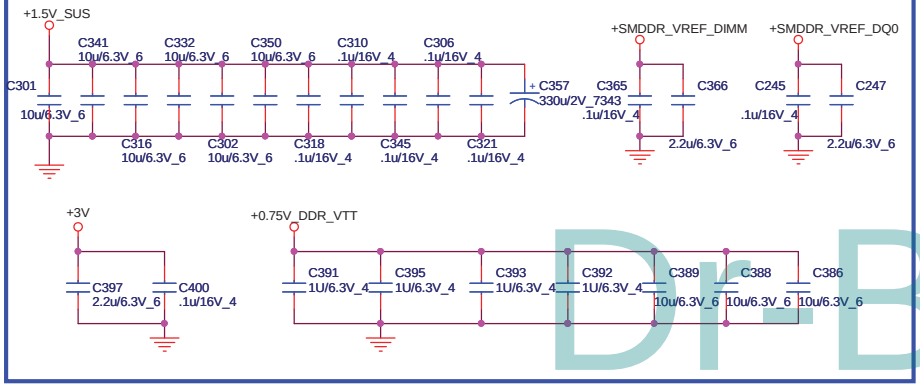


Place these Caps near So-Dimm0.



For Arrandale only designs--->Only method M1 should be enabled.
For Clarksfield only designs--->Both M1 AND M3 methods should be enabled simultaneously
For Common Motherboard designs--->Both M1 AND M3 methods should be enabled simultaneously.

M1:PWR SMDRR_VREF
M1+:voltage divider(Default)
M3:CPU VREF_DQ_DIMM0

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	DDRIII SO-DIMM-0	3B
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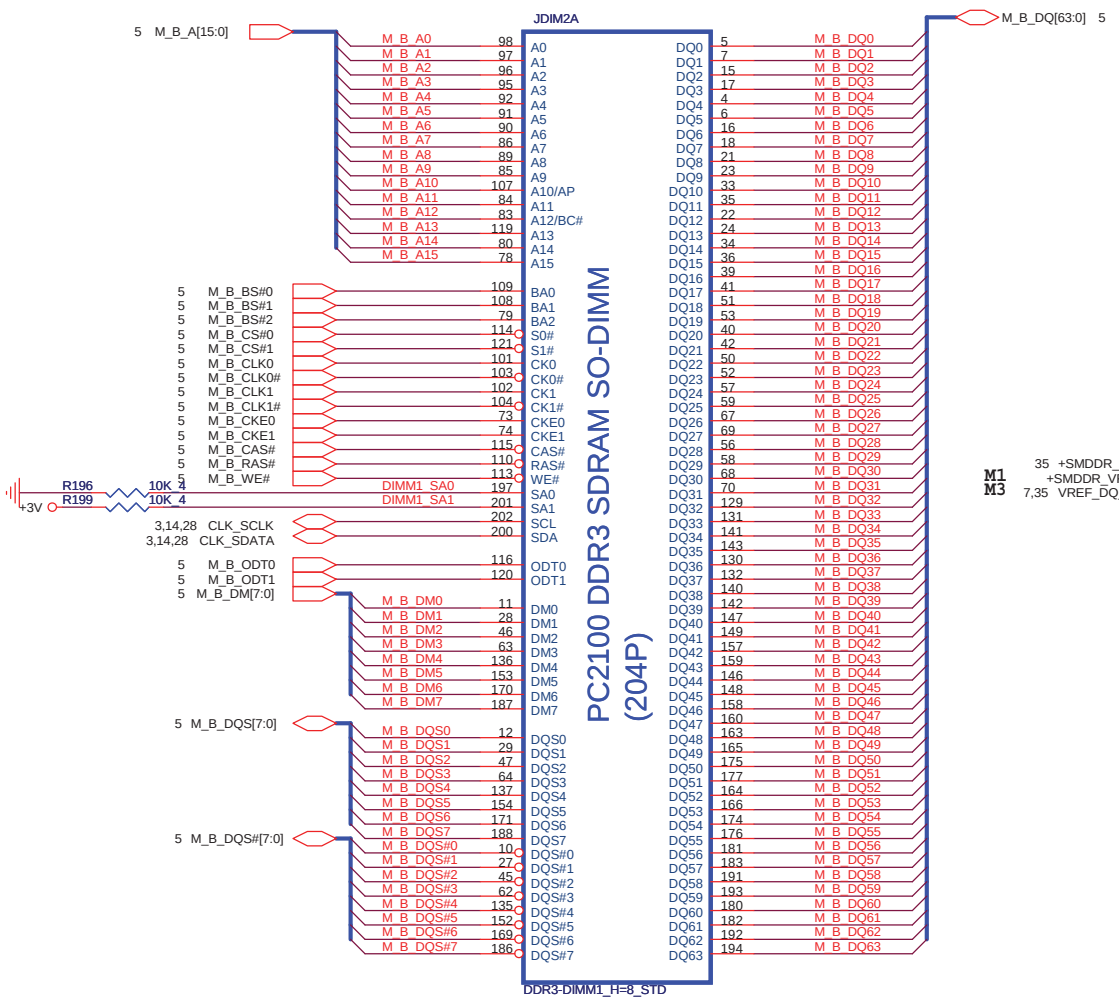

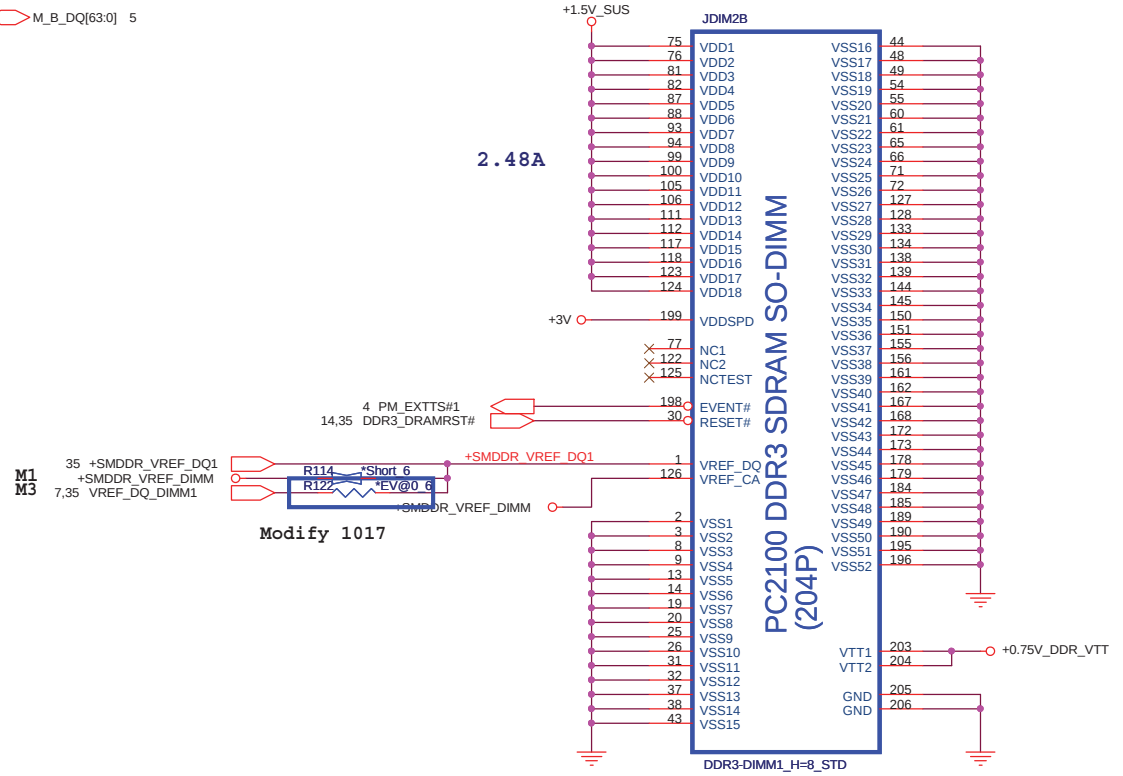

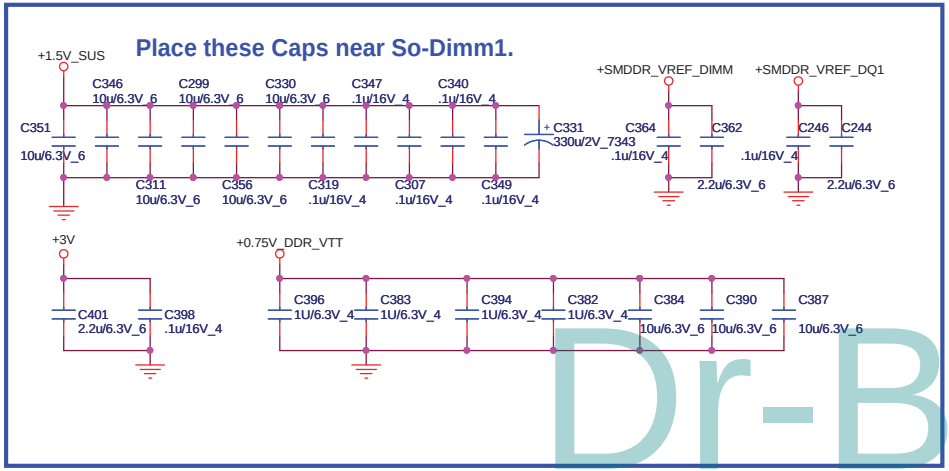

For Arrandale only designs--->Only method M1 should be enabled.
For Clarksfield only designs--->Both M1 AND M3 methods should be enabled simultaneously
For Common Motherboard designs--->Both M1 AND M3 methods should be enabled simultaneously.

Quanta Computer Inc.		
PROJECT : ZYD		
Size	Document Number: DDRIII SO-DIMM-1	Rev: 3B
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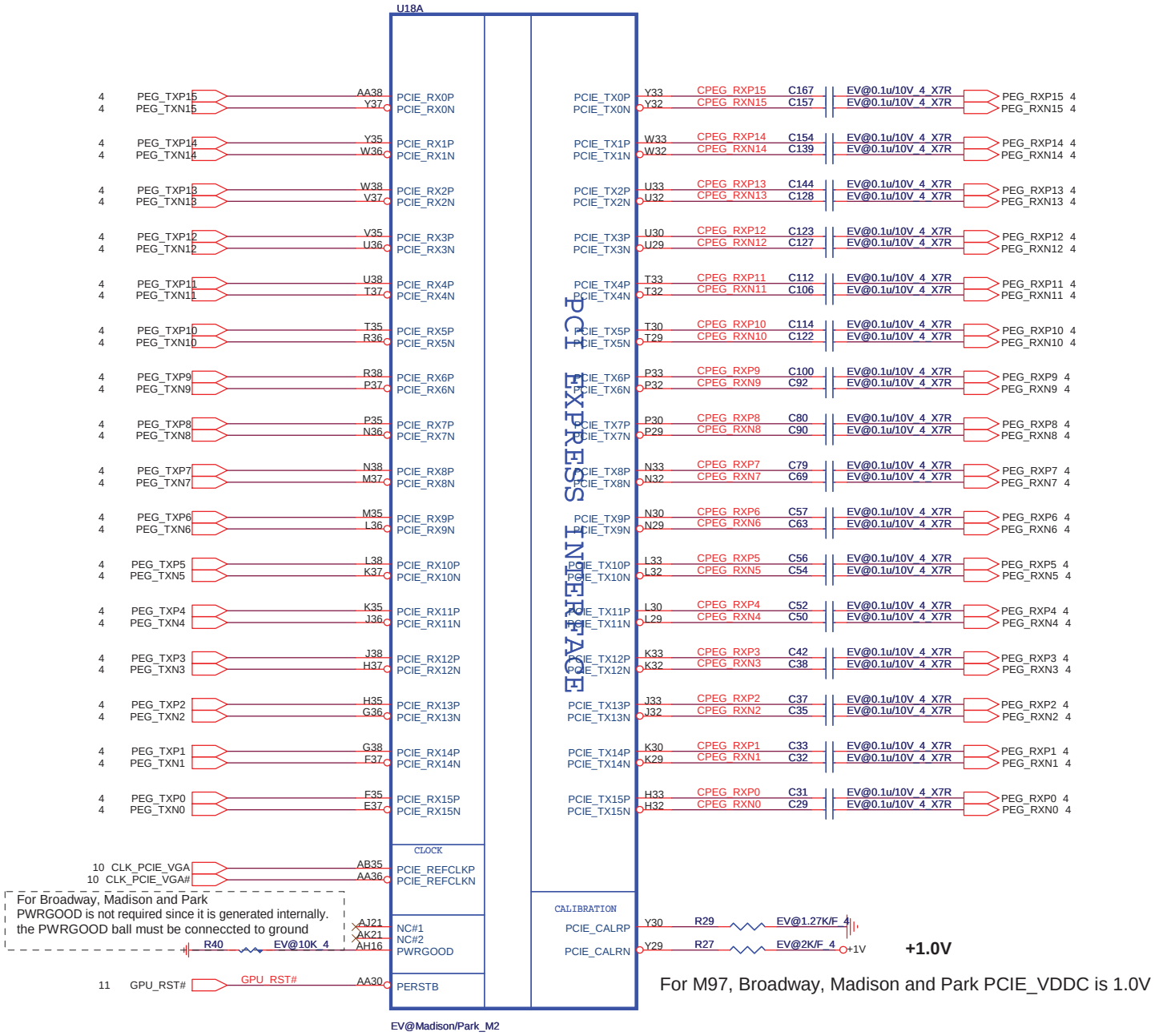
U18A
PCI EXPRESS INTERFACE
4 PEG_TXP15 AA38 PCIE_RX0P
4 PEG_TXN15 Y37 PCIE_RX0N
4 PEG_TXP14 Y35 PCIE_RX1P
4 PEG_TXN14 W36 PCIE_RX1N
4 PEG_TXP13 W38 PCIE_RX2P
4 PEG_TXN13 V37 PCIE_RX2N
4 PEG_TXP12 V35 PCIE_RX3P
4 PEG_TXN12 U36 PCIE_RX3N
4 PEG_TXP11 U38 PCIE_RX4P
4 PEG_TXN11 T37 PCIE_RX4N
4 PEG_TXP10 T35 PCIE_RX5P
4 PEG_TXN10 R36 PCIE_RX5N
4 PEG_TXP9 R38 PCIE_RX6P
4 PEG_TXN9 P37 PCIE_RX6N
4 PEG_TXP8 P35 PCIE_RX7P
4 PEG_TXN8 N36 PCIE_RX7N
4 PEG_TXP7 N38 PCIE_RX8P
4 PEG_TXN7 M37 PCIE_RX8N
4 PEG_TXP6 M35 PCIE_RX9P
4 PEG_TXN6 L36 PCIE_RX9N
4 PEG_TXP5 L38 PCIE_RX10P
4 PEG_TXN5 K37 PCIE_RX10N
4 PEG_TXP4 K35 PCIE_RX11P
4 PEG_TXN4 J36 PCIE_RX11N
4 PEG_TXP3 J38 PCIE_RX12P
4 PEG_TXN3 H37 PCIE_RX12N
4 PEG_TXP2 H35 PCIE_RX13P
4 PEG_TXN2 G36 PCIE_RX13N
4 PEG_TXP1 G38 PCIE_RX14P
4 PEG_TXN1 F37 PCIE_RX14N
4 PEG_TXP0 F35 PCIE_RX15P
4 PEG_TXN0 E37 PCIE_RX15N
PCIE_TX0P Y33 CPEG_RXP15 C167 EV@0.1u/10V_4_X7R PEG_RXP15 4
PCIE_TX0N Y32 CPEG_RXN15 C157 EV@0.1u/10V_4_X7R PEG_RXN15 4
PCIE_TX1P W33 CPEG_RXP14 C154 EV@0.1u/10V_4_X7R PEG_RXP14 4
PCIE_TX1N W32 CPEG_RXN14 C139 EV@0.1u/10V_4_X7R PEG_RXN14 4
PCIE_TX2P U33 CPEG_RXP13 C144 EV@0.1u/10V_4_X7R PEG_RXP13 4
PCIE_TX2N U32 CPEG_RXN13 C128 EV@0.1u/10V_4_X7R PEG_RXN13 4
PCIE_TX3P U30 CPEG_RXP12 C123 EV@0.1u/10V_4_X7R PEG_RXP12 4
PCIE_TX3N U29 CPEG_RXN12 C127 EV@0.1u/10V_4_X7R PEG_RXN12 4
PCIE_TX4P T33 CPEG_RXP11 C112 EV@0.1u/10V_4_X7R PEG_RXP11 4
PCIE_TX4N T32 CPEG_RXN11 C106 EV@0.1u/10V_4_X7R PEG_RXN11 4
PCIE_TX5P T30 CPEG_RXP10 C114 EV@0.1u/10V_4_X7R PEG_RXP10 4
PCIE_TX5N T29 CPEG_RXN10 C122 EV@0.1u/10V_4_X7R PEG_RXN10 4
PCIE_TX6P P33 CPEG_RXP9 C100 EV@0.1u/10V_4_X7R PEG_RXP9 4
PCIE_TX6N P32 CPEG_RXN9 C92 EV@0.1u/10V_4_X7R PEG_RXN9 4
PCIE_TX7P P30 CPEG_RXP8 C80 EV@0.1u/10V_4_X7R PEG_RXP8 4
PCIE_TX7N P29 CPEG_RXN8 C90 EV@0.1u/10V_4_X7R PEG_RXN8 4
PCIE_TX8P N33 CPEG_RXP7 C79 EV@0.1u/10V_4_X7R PEG_RXP7 4
PCIE_TX8N N32 CPEG_RXN7 C69 EV@0.1u/10V_4_X7R PEG_RXN7 4
PCIE_TX9P N30 CPEG_RXP6 C57 EV@0.1u/10V_4_X7R PEG_RXP6 4
PCIE_TX9N N29 CPEG_RXN6 C63 EV@0.1u/10V_4_X7R PEG_RXN6 4
PCIE_TX10P L33 CPEG_RXP5 C56 EV@0.1u/10V_4_X7R PEG_RXP5 4
PCIE_TX10N L32 CPEG_RXN5 C54 EV@0.1u/10V_4_X7R PEG_RXN5 4
PCIE_TX11P L30 CPEG_RXP4 C52 EV@0.1u/10V_4_X7R PEG_RXP4 4
PCIE_TX11N L29 CPEG_RXN4 C50 EV@0.1u/10V_4_X7R PEG_RXN4 4
PCIE_TX12P K33 CPEG_RXP3 C42 EV@0.1u/10V_4_X7R PEG_RXP3 4
PCIE_TX12N K32 CPEG_RXN3 C38 EV@0.1u/10V_4_X7R PEG_RXN3 4
PCIE_TX13P J33 CPEG_RXP2 C37 EV@0.1u/10V_4_X7R PEG_RXP2 4
PCIE_TX13N J32 CPEG_RXN2 C35 EV@0.1u/10V_4_X7R PEG_RXN2 4
PCIE_TX14P K30 CPEG_RXP1 C33 EV@0.1u/10V_4_X7R PEG_RXP1 4
PCIE_TX14N K29 CPEG_RXN1 C32 EV@0.1u/10V_4_X7R PEG_RXN1 4
PCIE_TX15P H33 CPEG_RXP0 C31 EV@0.1u/10V_4_X7R PEG_RXP0 4
PCIE_TX15N H32 CPEG_RXN0 C29 EV@0.1u/10V_4_X7R PEG_RXN0 4
CLOCK
10 CLK_PCIE_VGA AB35 PCIE_REFCLKP
10 CLK_PCIE_VGA# AA36 PCIE_REFCLKN
CALIBRATION
PCIE_CALRP Y30 R29 EV@1.27K/F_4
PCIE_CALRN Y29 R27 EV@2K/F_4 +1V
+1.0V
For Broadway, Madison and Park
PWRGOOD is not required since it is generated internally.
the PWRGOOD ball must be conneccted to ground
R40 EV@10K_4
AJ21 NC#1
AK21 NC#2
AH16 PWRGOOD
11 GPU_RST# GPU_RST# AA30 PERSTB
EV@Madison/Park_M2
For M97, Broadway, Madison and Park PCIE_VDDC is 1.0V
Quanta Computer Inc.
PROJECT : ZYD
Size
Document Number
Madison/Park M2 PCIE I/F
Rev 3B
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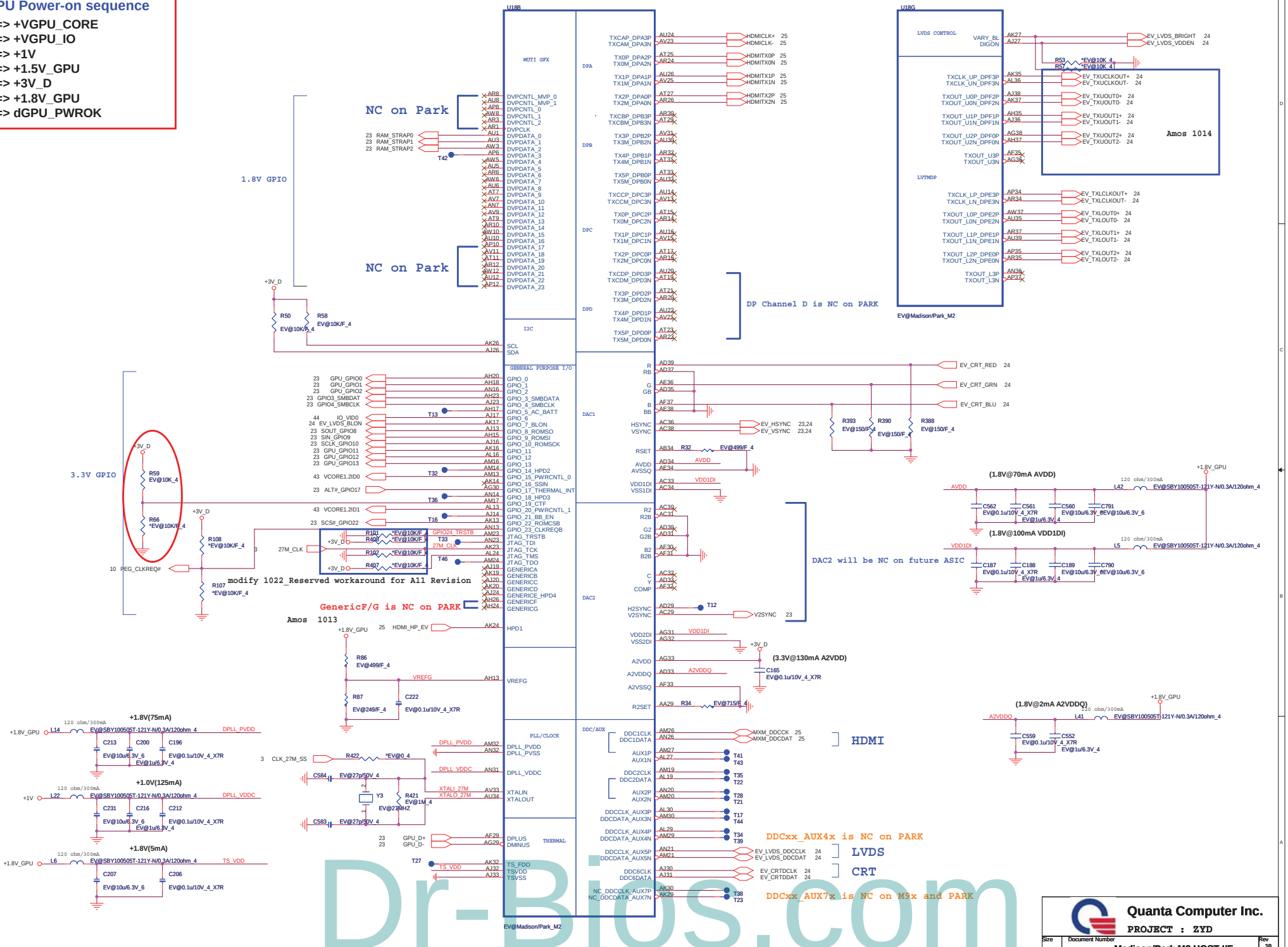
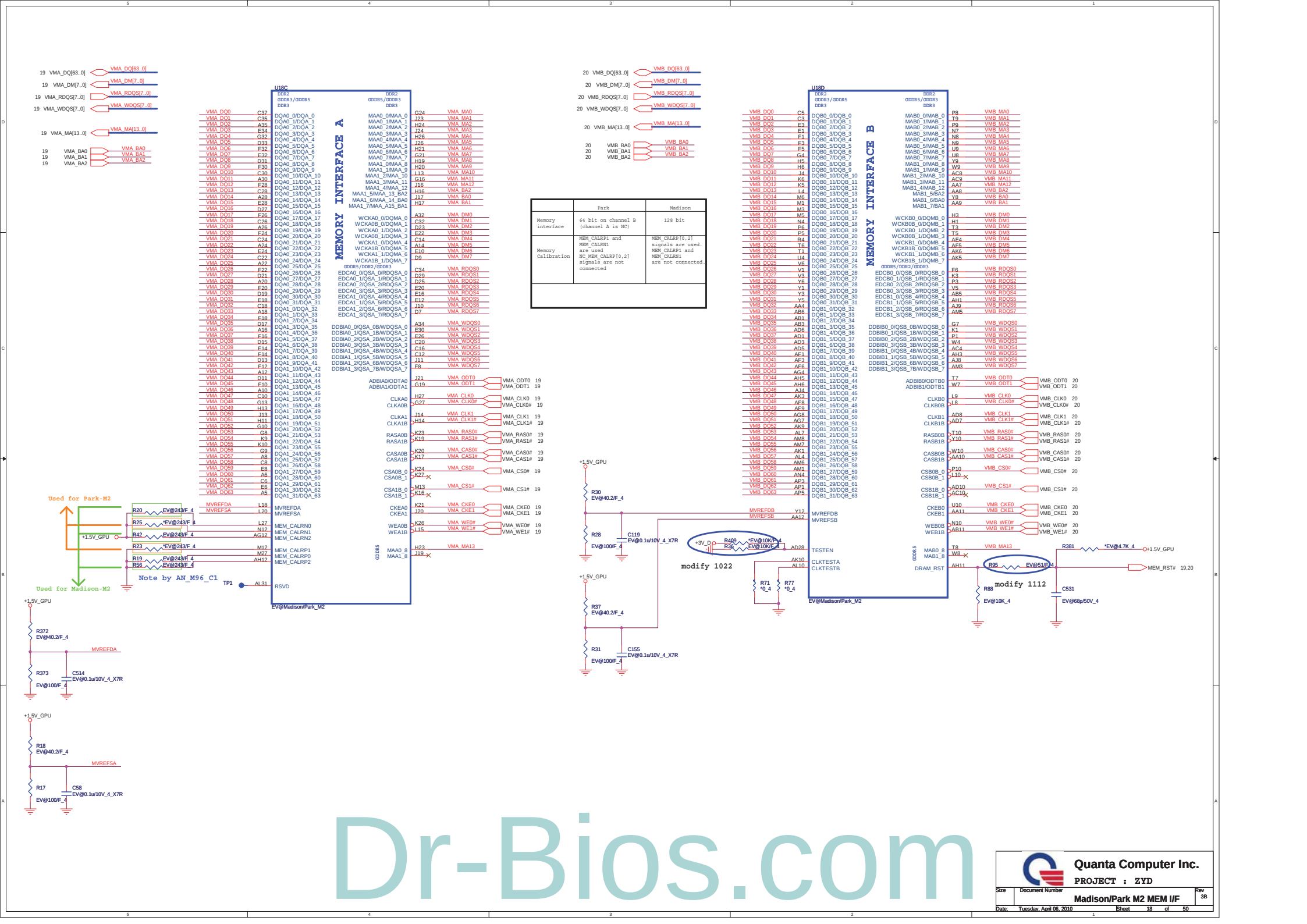
GPU Power-on sequence

1 => +VGPU_CORE
2 => +VGPU_IO
3 => +1V
4 => +1.5V_GPU
5 => +3V_D
6 => +1.8V_GPU
7 => dGPU_PWROK



Quanta Computer Inc.
PROJECT : ZYD

Size	Document Number	Rev
	Madison/Park M2 HOST I/F	3B
Date: Tuesday, April 06, 2010	Sheet 17 of 50	



Quanta Computer Inc.	
PROJECT : ZYD	
Size	Document Number: Madison/Park M2 MEM I/F
Rev	3B
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CHANNEL A: 512MB DDR3 (64M*16*4pcs)

Park, M92M Use Channel B Memory Interface Only

18 VMA_DQ[63..0] — VMA_DQ[63..0]
18 VMA_DM[7..0] — VMA_DM[7..0]
18 VMA_RDQS[7..0] — VMA_RDQS[7..0] — QSA[7..0]
18 VMA_WDQS[7..0] — VMA_WDQS[7..0] — QSA#[7..0]

TOP Left

BOT Left

BOT Right

TOP Right

Group-A0 VREF

Group-A1 VREF

MEM_A0 CLK

Group-A0 decoupling CAP

Group-A1 decoupling CAP

MEM_A1 CLK

Quanta Computer Inc.
PROJECT : ZYD
Size | Document Number | Rev
MEMORY 1 channel A | 3B
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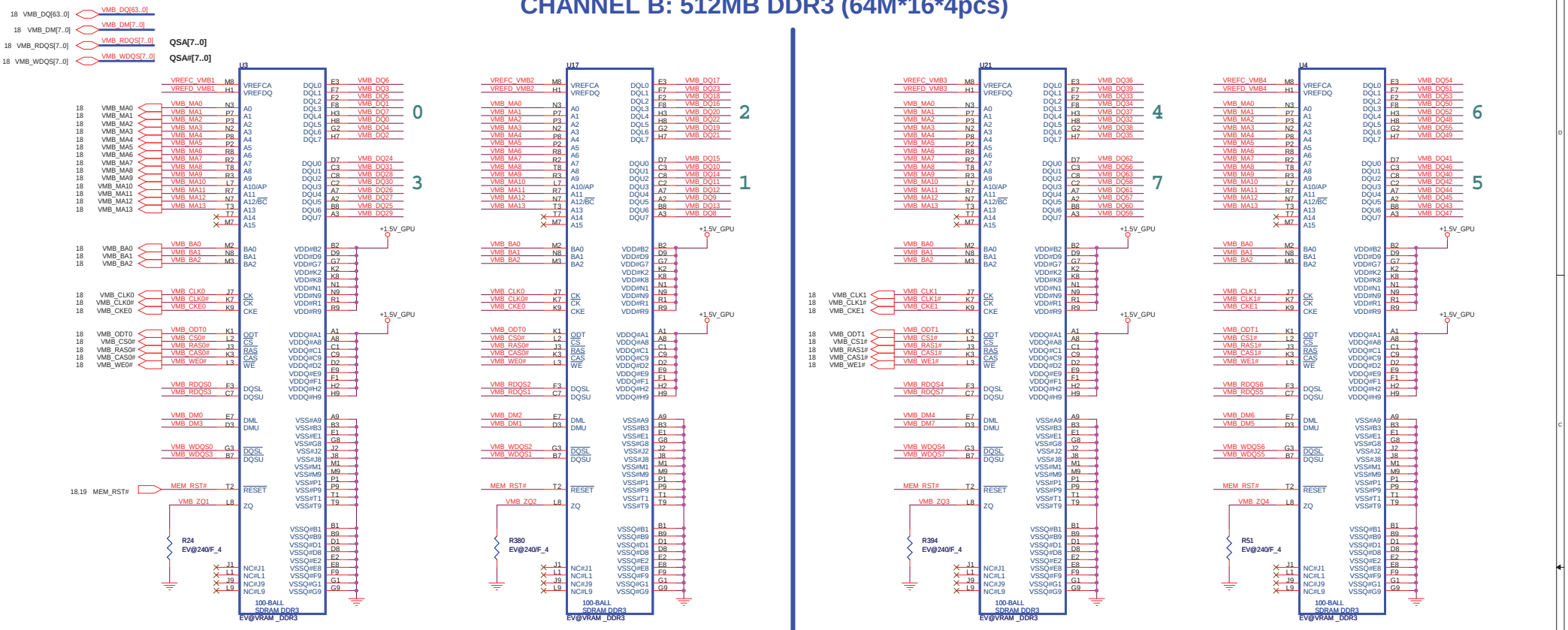
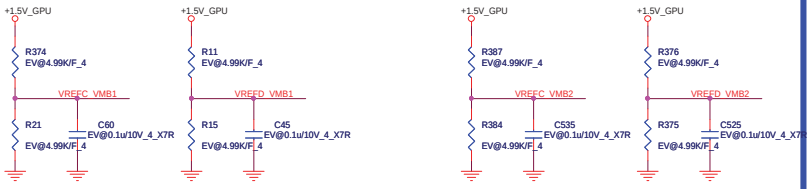
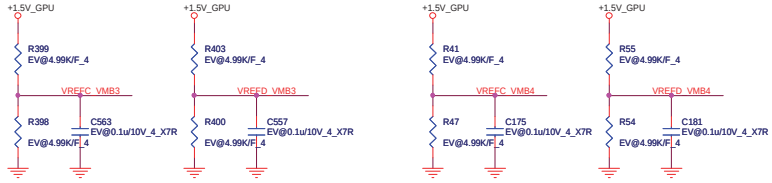
CHANNEL B: 512MB DDR3 (64M*16*4pcs)



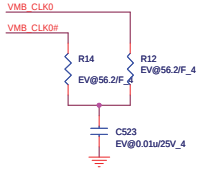
Group-B0 VREF



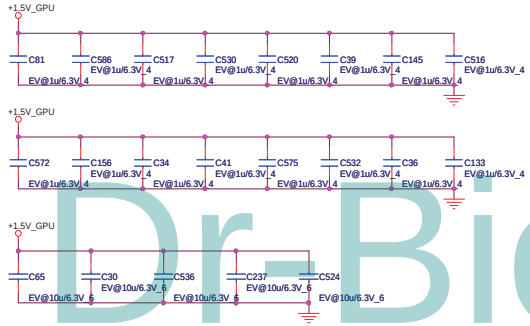
Group-B1 VREF



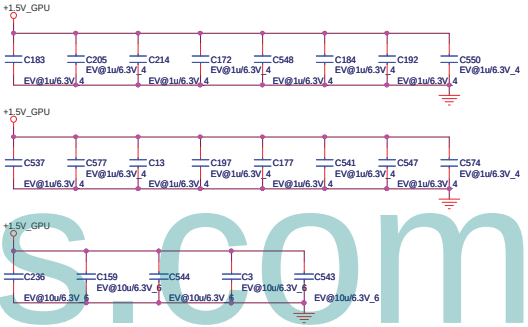
MEM_B0 CLK



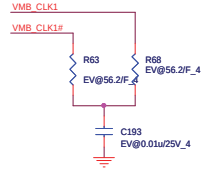
Group-B0 decoupling CAP



Group-B1 decoupling CAP



MEM_B1 CLK



Quanta Computer Inc.
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Size | Document Number | Rev
MEMORY 2 channel B | 3B
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For DDR3, MVDDQ = 1.5V (7.5A)

(For M97, Broadway, Madison and Park SPV10 = 1.0V)

BIF_VDDC should be connected to VDDC if BACO feature not used.
For BACO, refer to the databook
Connect to VDDC in non-PowerXpress designs.

PIN different between Broadway and Madison

Pin	Broadway	Madison
N27 T27	VDDC	BIF_VDDC

Modify 1022

VDDC and VDDCI are assigned to different sets of balls on M97, Madison and Park. As a result, VDDC and VDDCI will be shorted when a M96 is populated on a compatible design.

VDDCI and VDDC should have seperate regulators with a merge option on PCB
For Madison and Park, VDDCI and VDDC can share one common regulator

modify 1230_B

PowerXpress control signal for Madsion and Park only
If not used, can be disconnected.
PX_EN = LOW, turn on
PX_EN = HIGH, turn off
PX_EN is used to turn ON/OFF some regulators for PowerXpress mode. An output high "3.3V" will turn the regulators OFF. An output low "0V" will turn the regulators ON. PX_EN outputs low (0V) by default.
If this signal is unused, it can be NC (not connected) or connected to ground.

Modify 1022

VDDC_SENSE/VSS_SENSE and VDDCI_SENSE/VSS_SENSE route as differetial pair

GPU +3V power

GPU all PWROK

Quanta Computer Inc.
PROJECT : ZYD
Madison/Park M2 MEM I/F
Rev 3B
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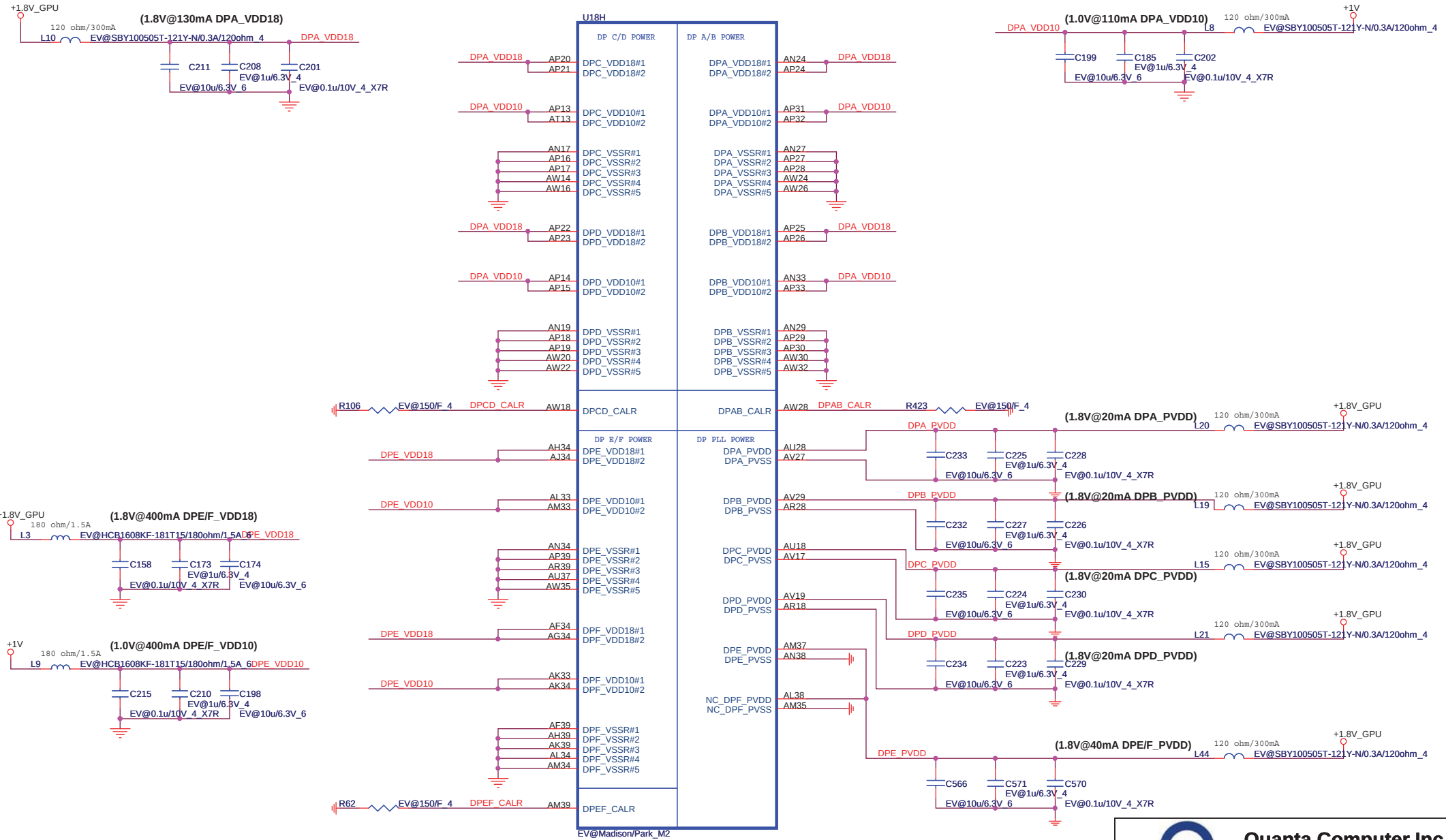

Quanta Computer Inc.

PROJECT : ZYD

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	Madison/Park M2 DPPW_GND	3B
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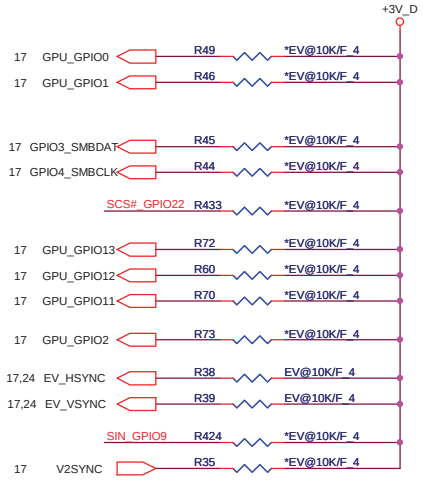
PIN STRAPS



Memory Aperture size	
GPIO[13:11]	Size
000	128MB
001	256MB
010	64MB
011	32MB

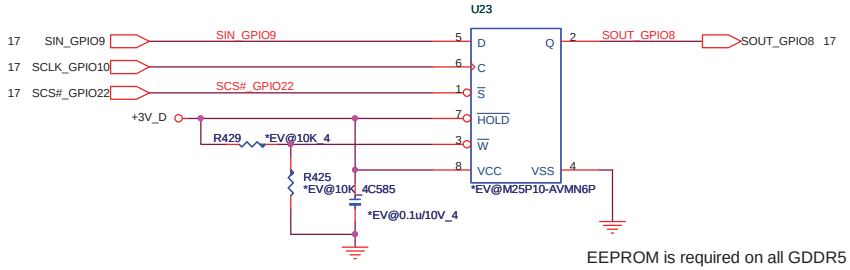
Audio Table		
EXT_HSYNC	EXT_VSYNC	Discription
0	0	No Audio
0	1	Any one by dectec
1	0	DP only
1	1	Both DP & HDMI

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM 0 = DISABLE 1 = ENABLE	0	
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	000	See Memory Aperture size
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

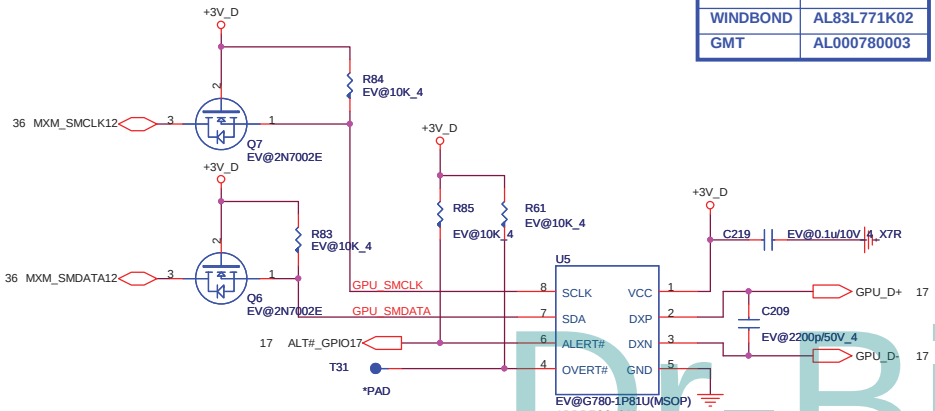
EEPROM



EEPROM is required on all GDDR5 designs

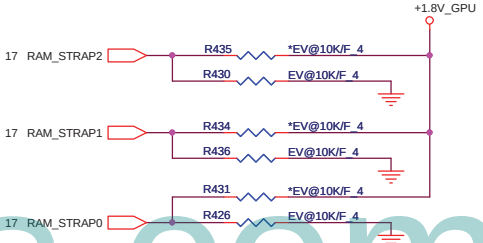
Thermal Sensor

NS	none
WINDBOND	AL83L771K02
GMT	AL000780003



DDR3 Memory Aperture size

DDR3 VRAM size						
Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0
Hynix			512MB	1	1	0
	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	1GB	1	0	0
			2GB	1	0	1
Samsung			512MB	0	1	0
	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	1GB	0	0	0
	K4W2G1646B-HC12	AKD5MGGT500	2GB	0	0	1
AMD	23EY2387MA-12	AKD5LGGT700		0	1	0



RAM_STRAP2 SET DDR3 Vendor
RAM_STRAP[1:0] SET SIZE.

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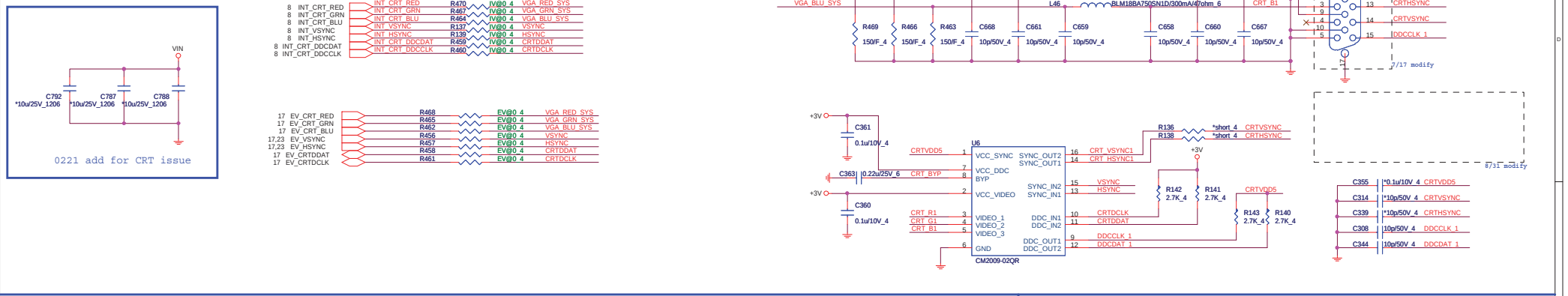
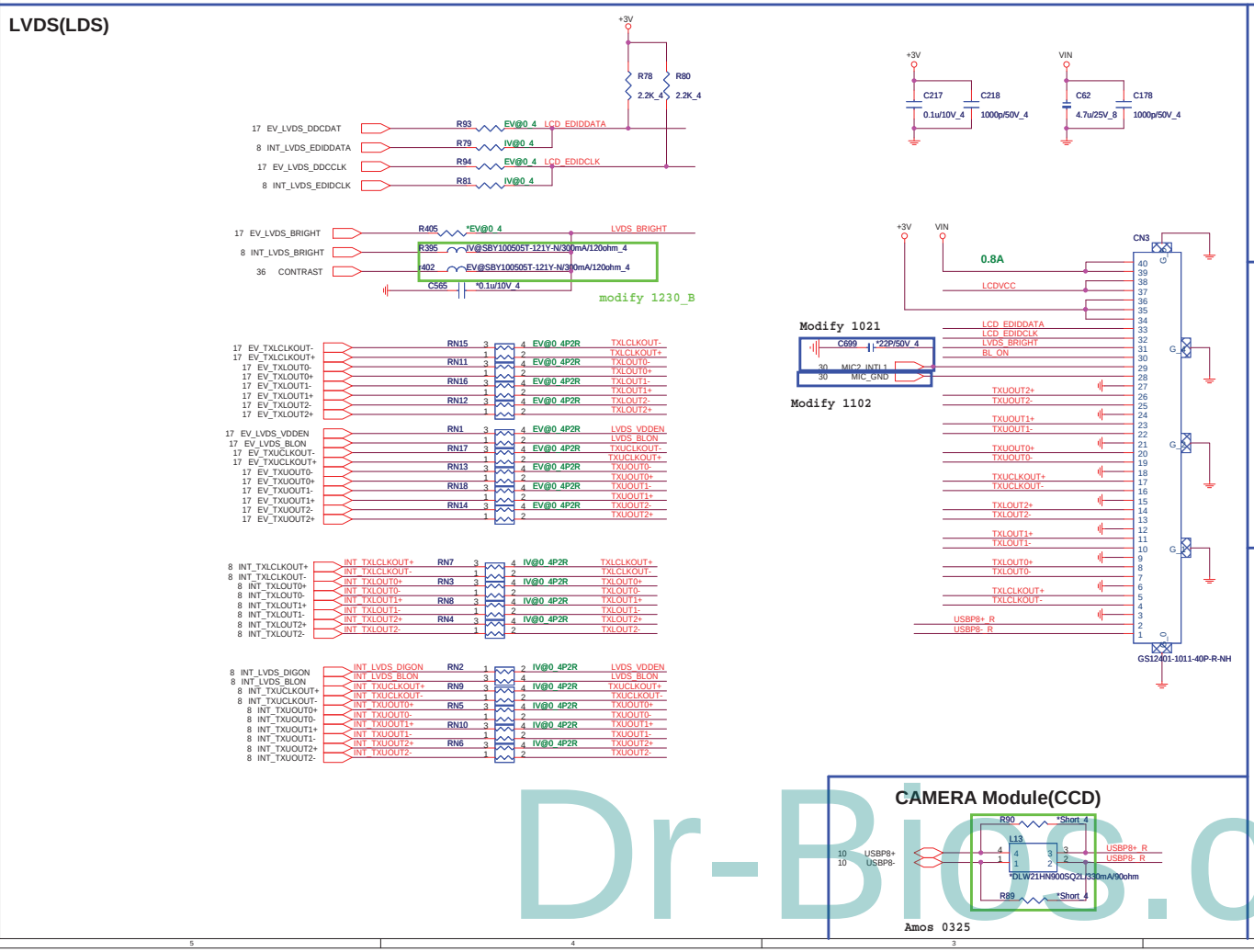
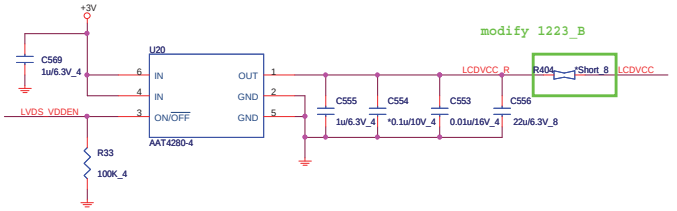
CRT(CRT)



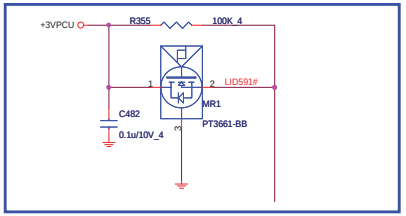
LVDS(LDS)



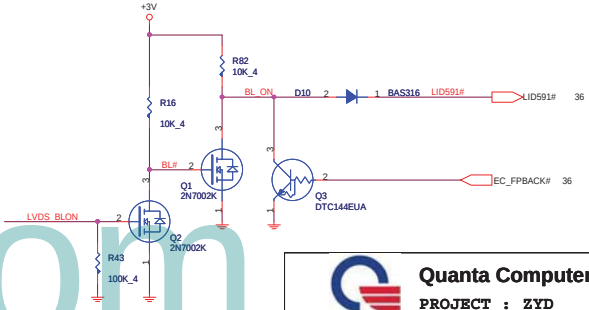
LCD Power(LDS)



Hall Sensor(HSR)



Backlight Control(LDS)



CAMERA Module(CCD)

Amos 0325

Quanta Computer Inc.		
PROJECT : ZYD		
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	CRT/LVDS	3B
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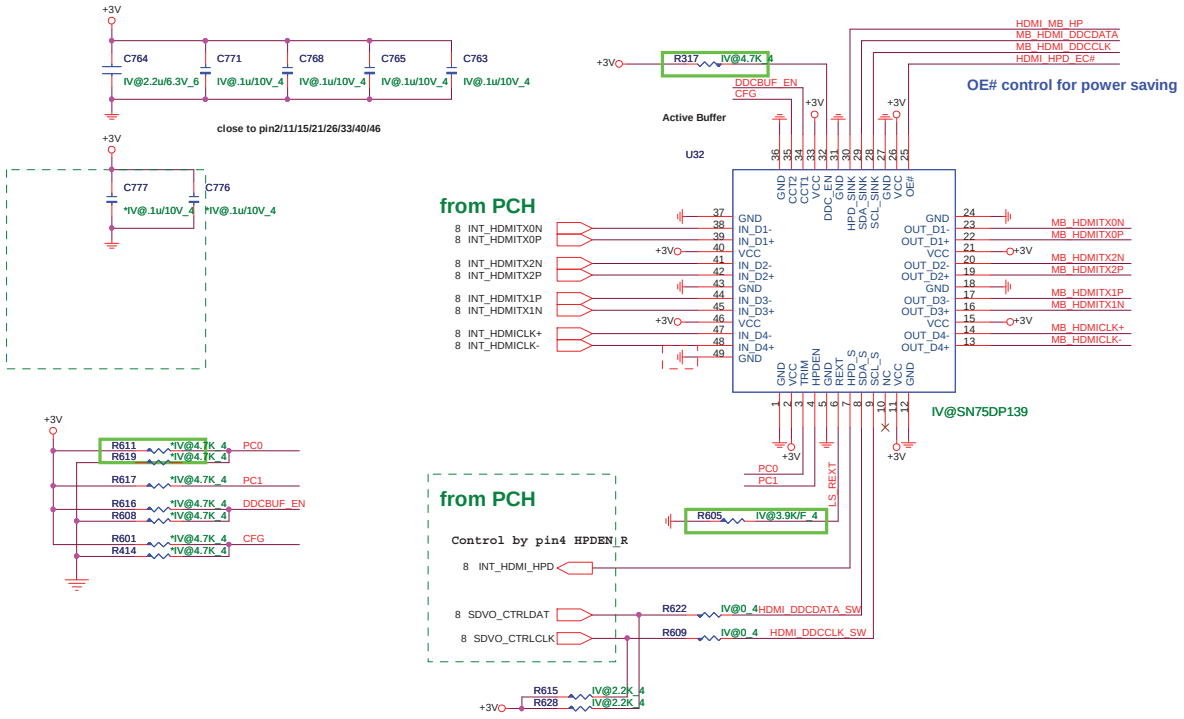
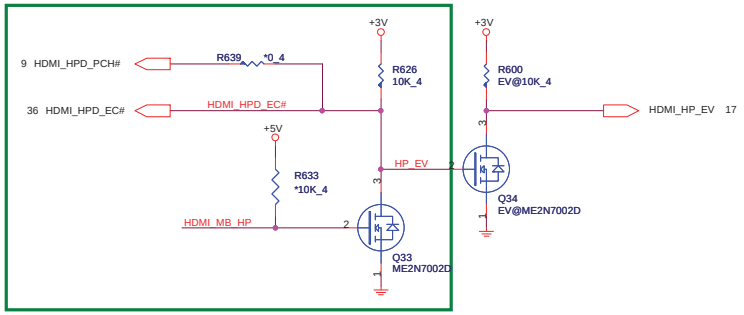
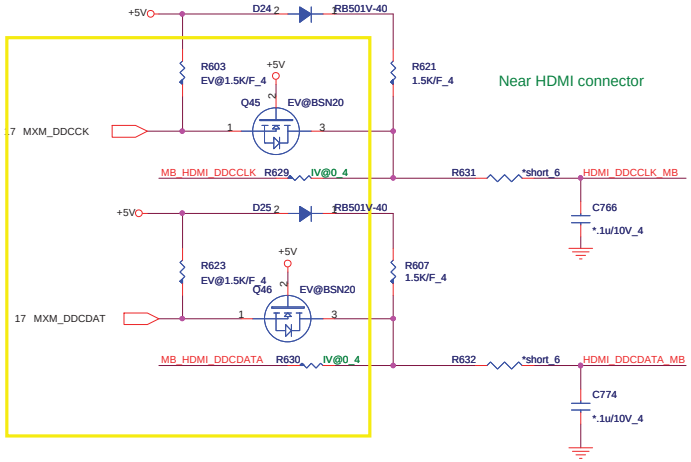
IV@ HDMI LEVEL SHIFTER



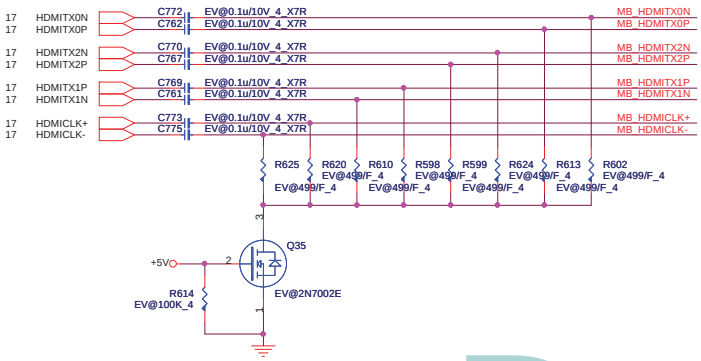
HDMI-detect



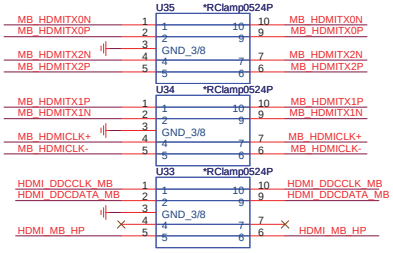
I2C



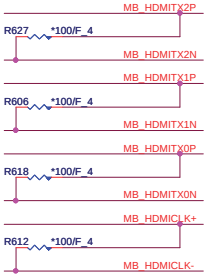
External Graphic HDMI source



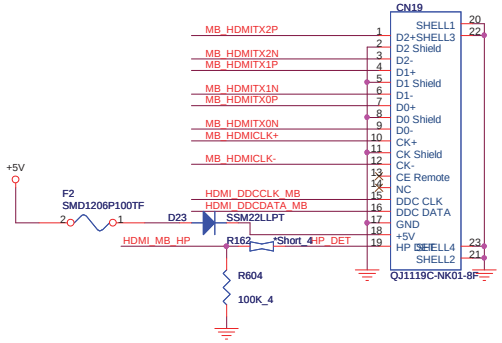
ESD Protect



EMI

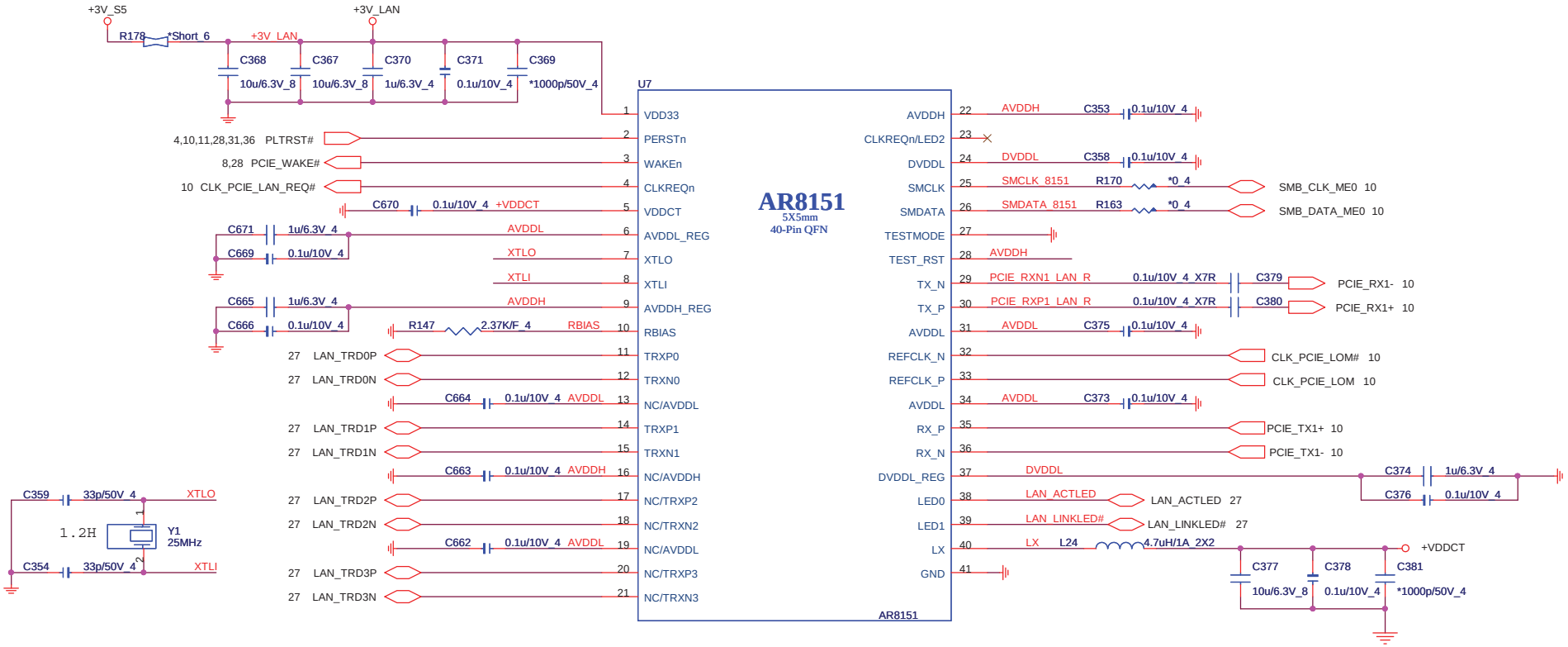


HDMI connector



Quanta Computer Inc.		
PROJECT : ZYD		
Size	Document Number: HDMI (SN75DP139)	Rev: 3B
Date: Tuesday, April 06, 2010	Sheet 25 of 50	

Giga-LAN AR8151

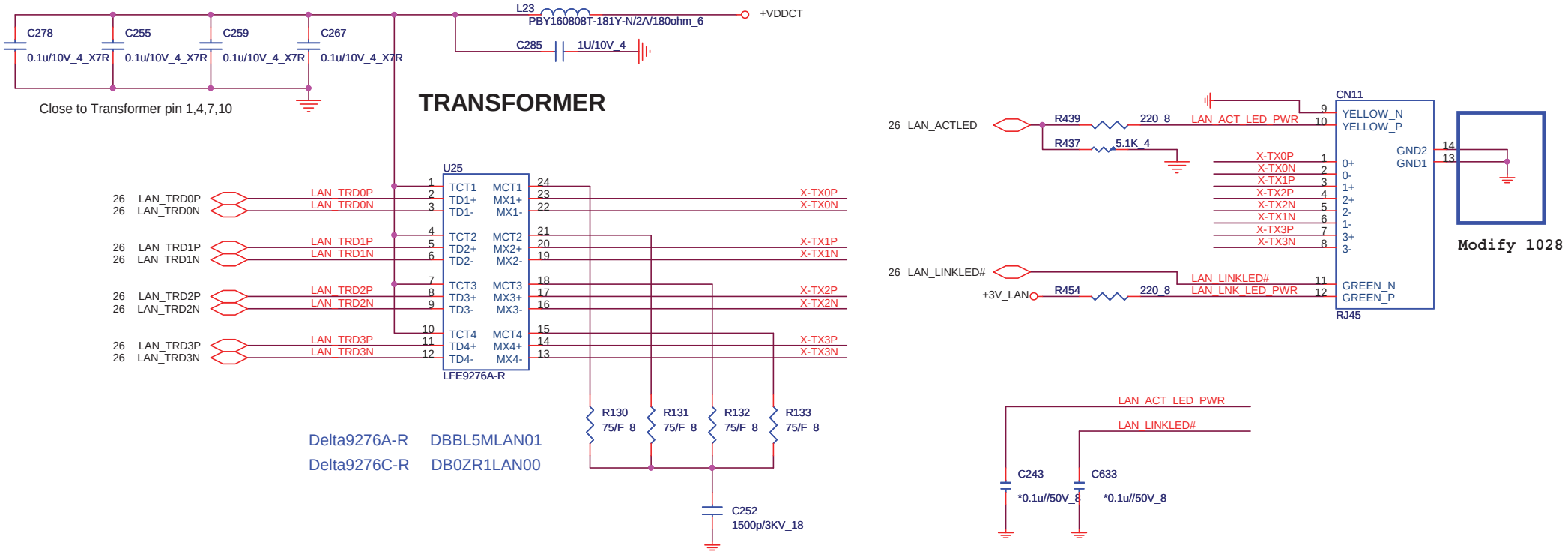


Quanta Computer Inc.

PROJECT : ZYD

Size	Document Number	Rev
	GLAN BCM57780	3B

Date: Tuesday, April 06, 2010 Sheet 26 of 50



Quanta Computer Inc.

PROJECT : ZYD

Size	Document Number	Rev
	LAN Transformer and RJ45	3B
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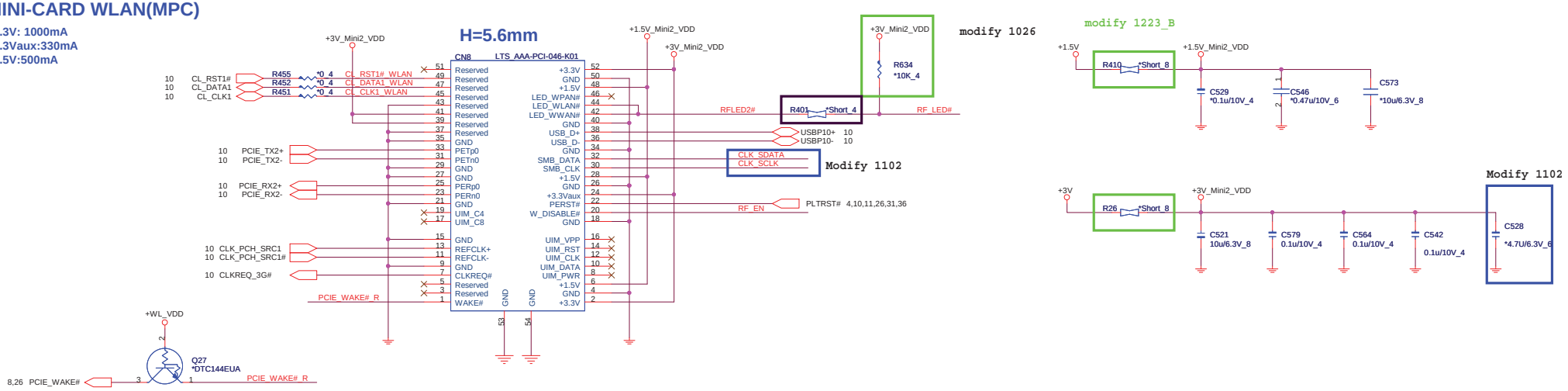
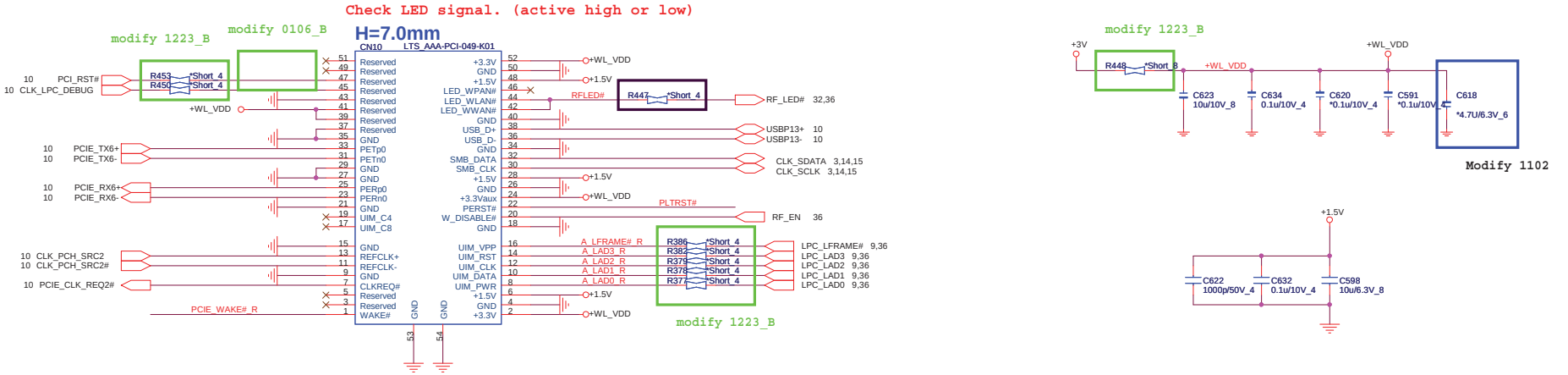
MINI-CARD WLAN(MPC)

+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA



MINI-CARD (MNC)Reserve for BA70



Quanta Computer Inc.
PROJECT : ZYD

Size	Document Number	Rev
	MINI PCI-E card/TV	3B

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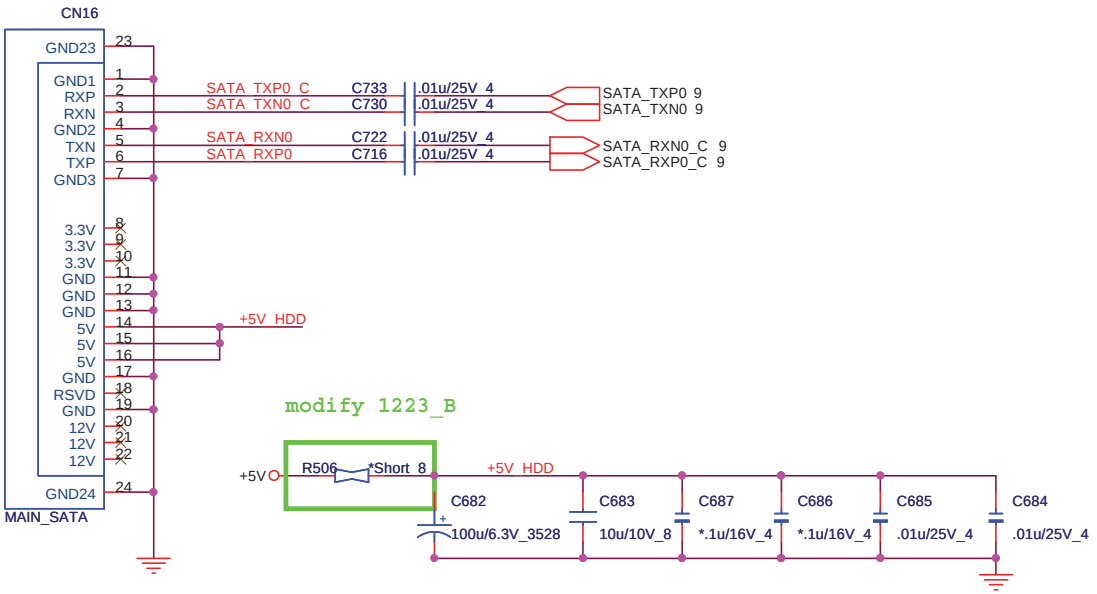
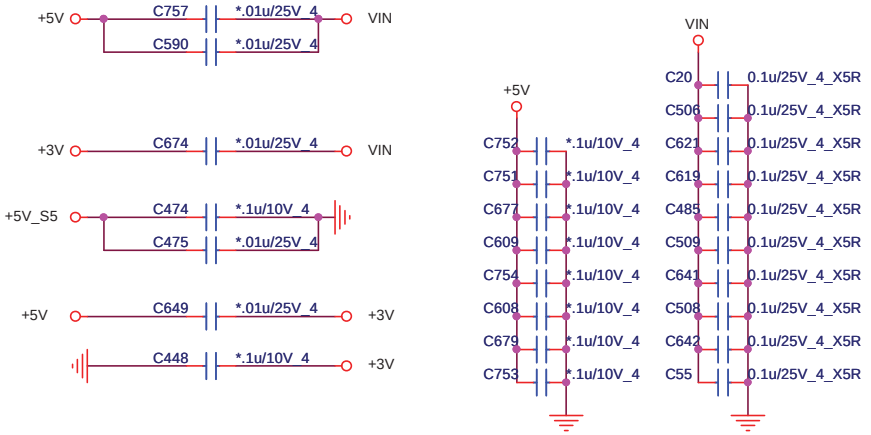
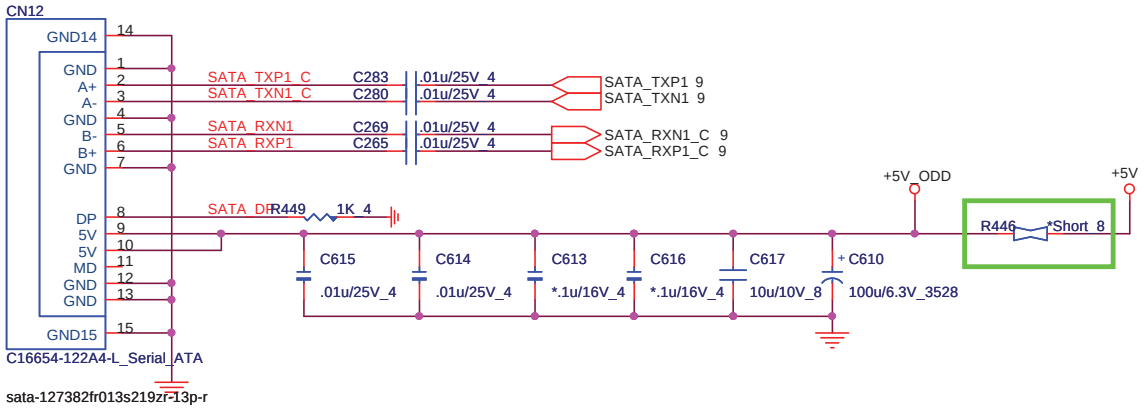
MAIN SATA HDD



EE RETURN-PATH CAPACITORS



ODD (SATA)



Quanta Computer Inc.		
PROJECT : ZYD		
Size	Document Number: SATA-HDD/ODD/USB-ESATA	Rev: 3B
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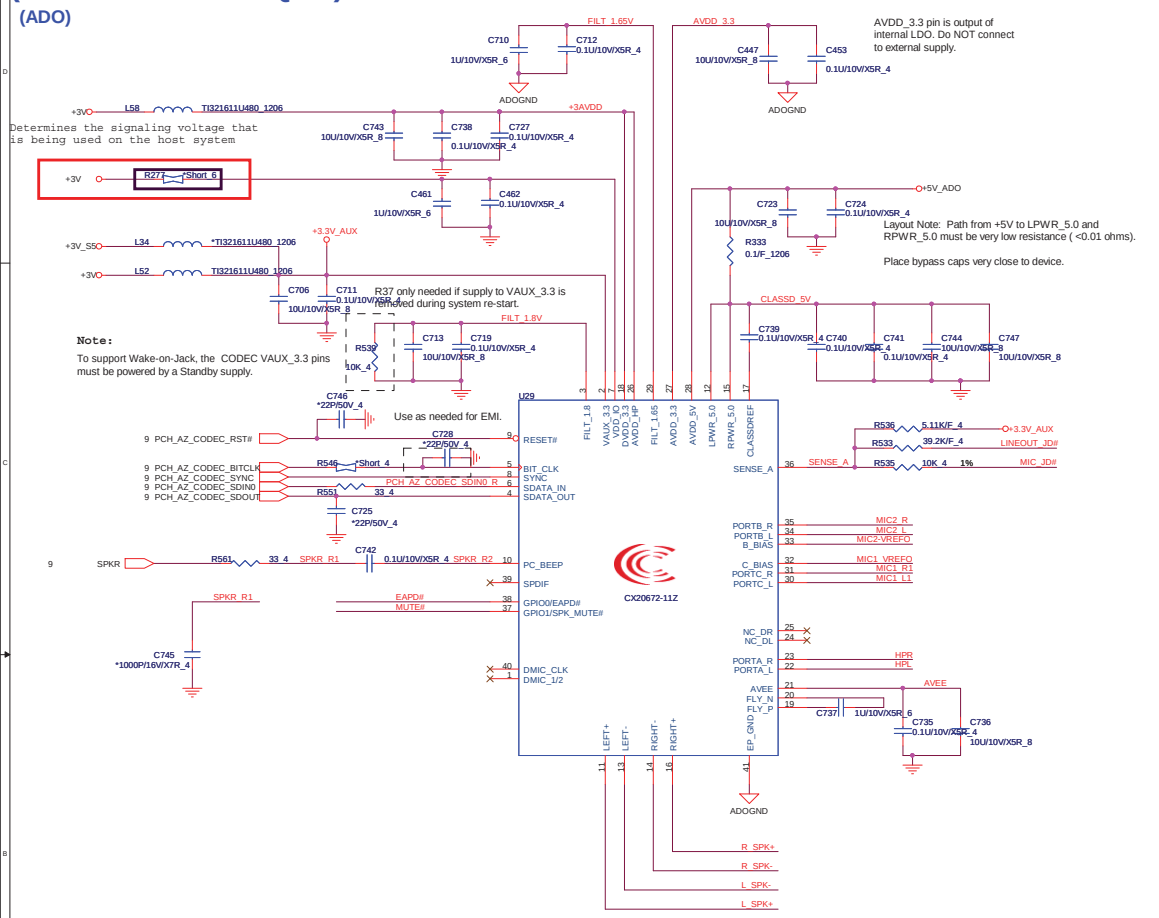
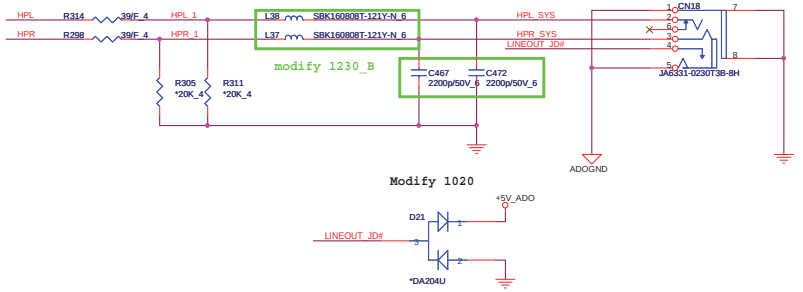
Codec(ADO)

(CX20672-11Z for QFN)

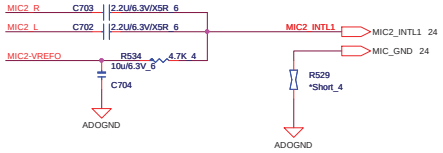
(ADO)



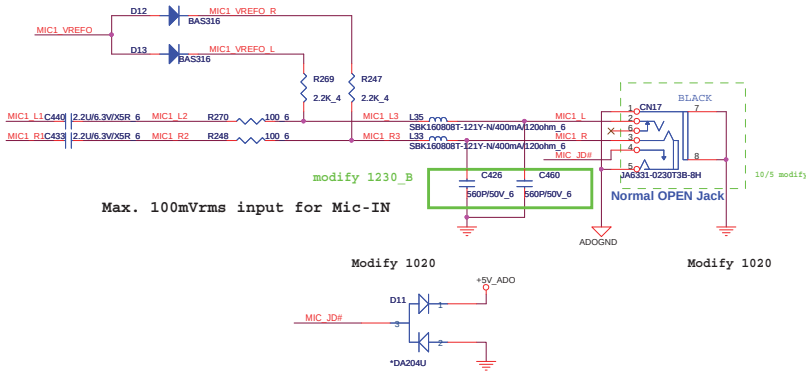
Headphone



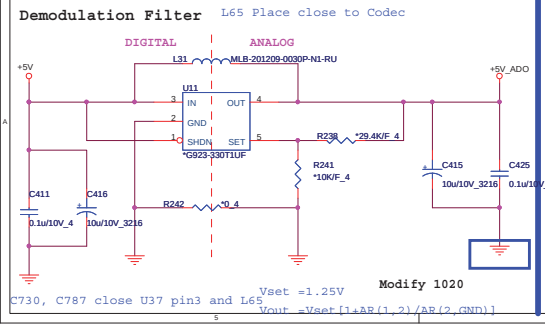
INT. MIC



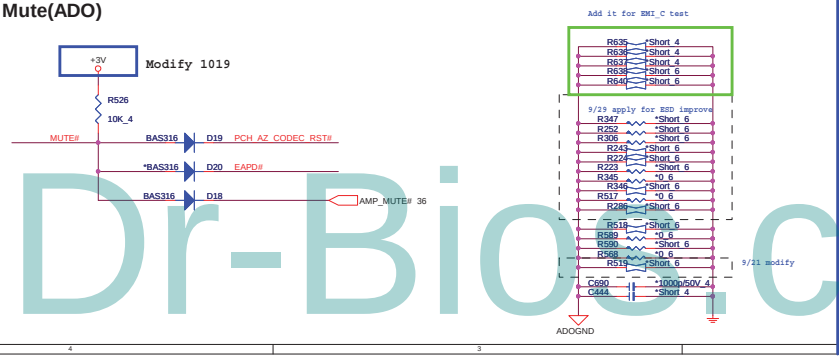
EXT. MIC



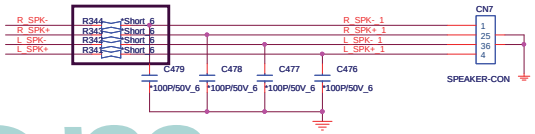
Power (ADO)



Mute(ADO)



Internal Speaker(AMP)



Quanta Computer Inc.		
PROJECT : ZYD		
Size	Document Number	Rev
	CX20672-11Z	3B
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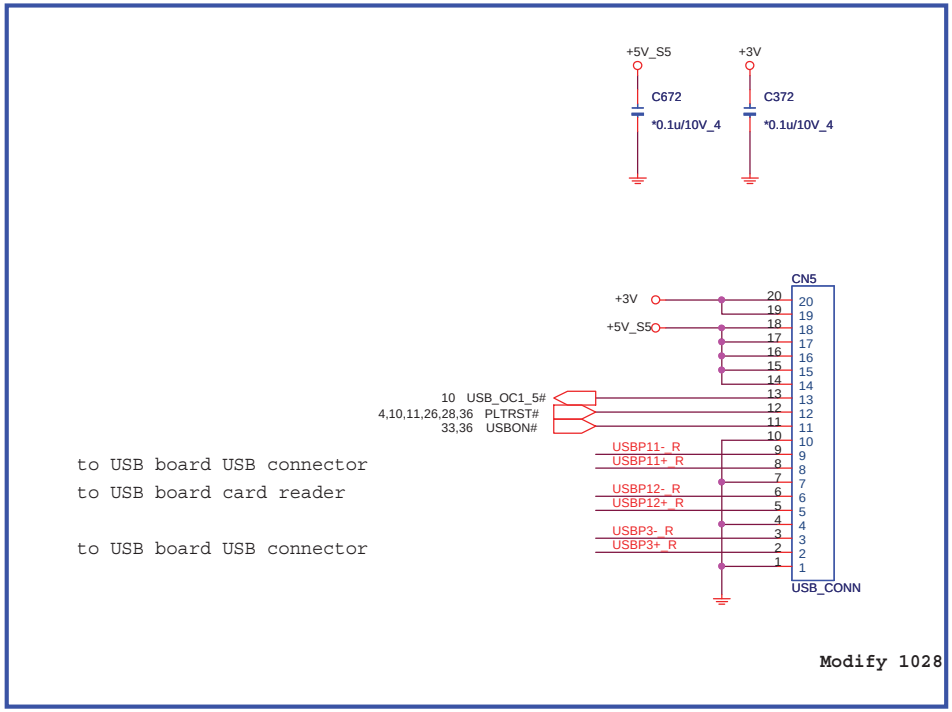
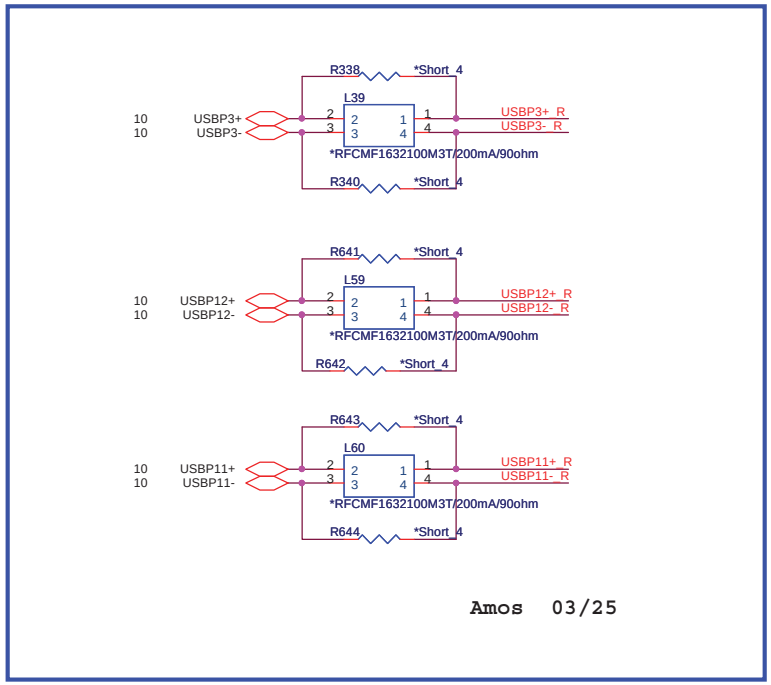
Cardreader CONN(MMC)





Quanta Computer Inc.
PROJECT : ZYD

Size	Document Number	Rev
	CardReader &USB/B	3B
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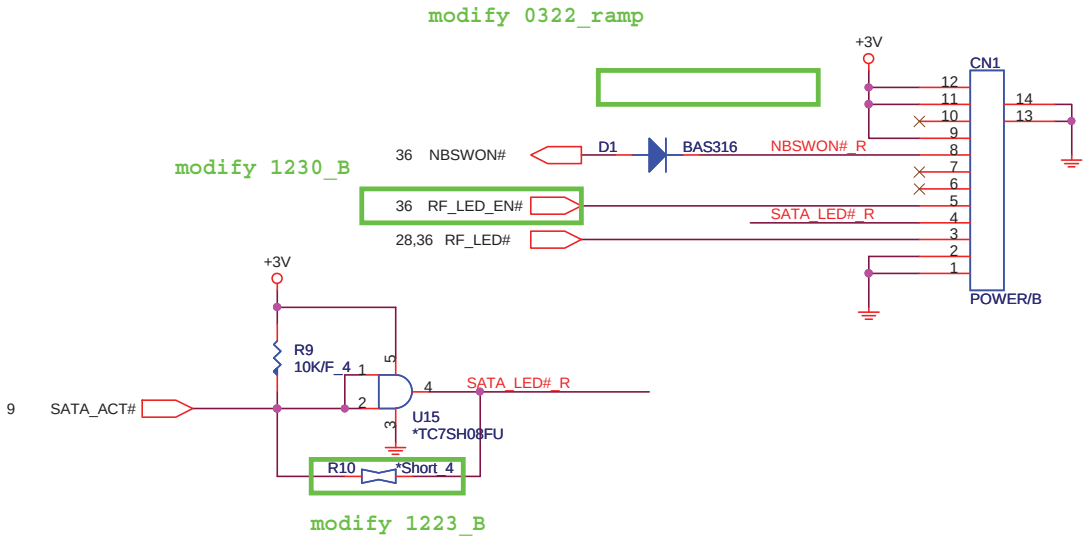
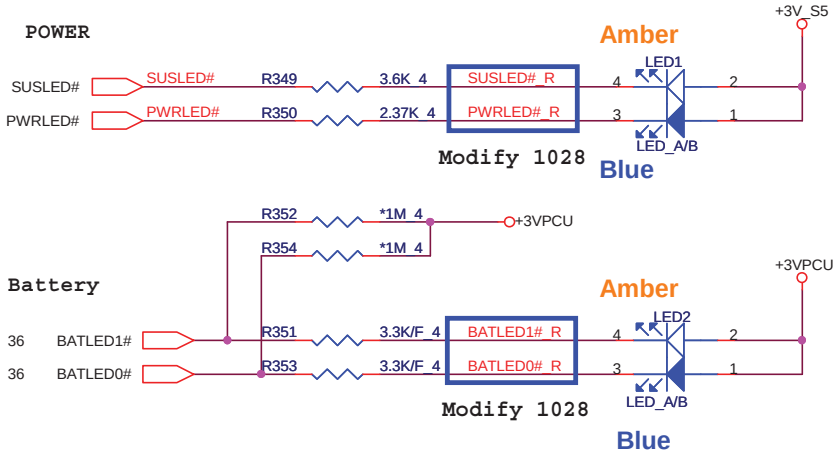
POWER BOARD CONN(UIF)



LED(UIF)



Quanta Computer Inc.

PROJECT : ZYD

Size	Document Number	Rev
	POWER/MMB/LAUNCH/LED	3B
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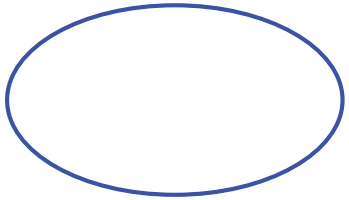
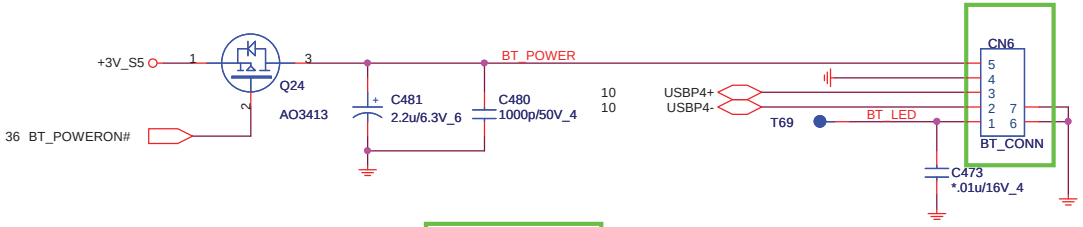


Modify 1022

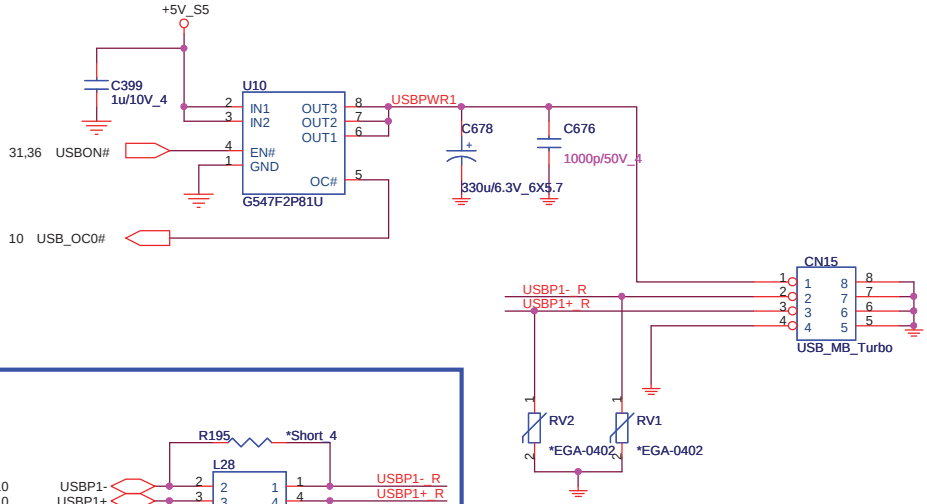
BLUETOOTH CONNECTOR(BTM)

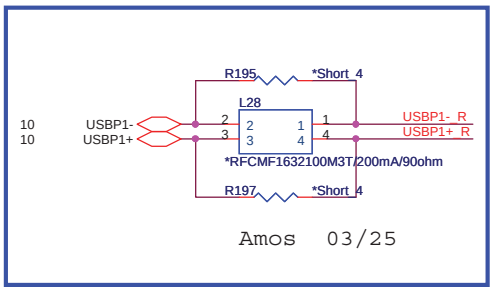
modify 1223_B



modify 0224_C

USBX1(USB)





Quanta Computer Inc.

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Size	Document Number	Rev
	USB/ BT	3B

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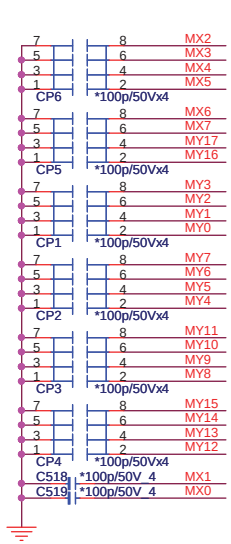
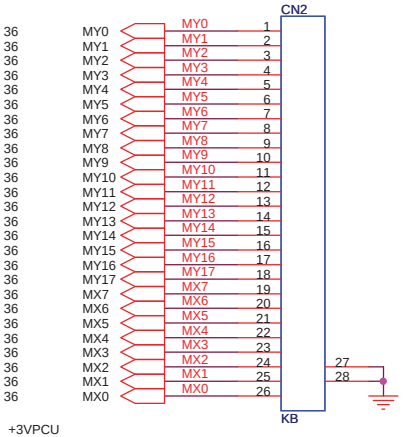
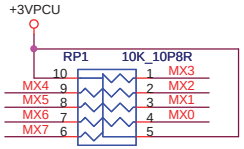
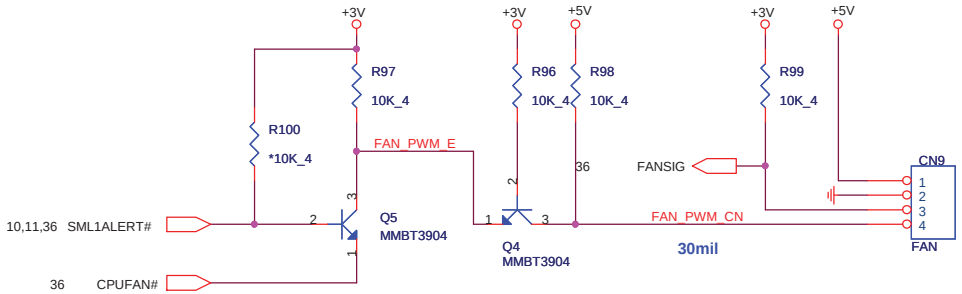
K/B



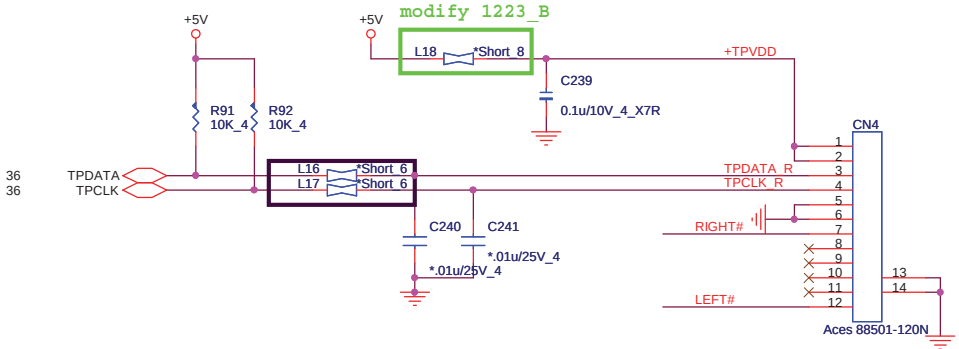


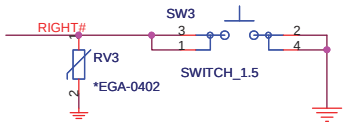


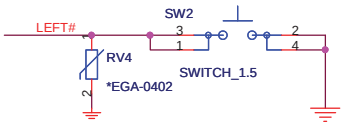
CPU FAN(THM)

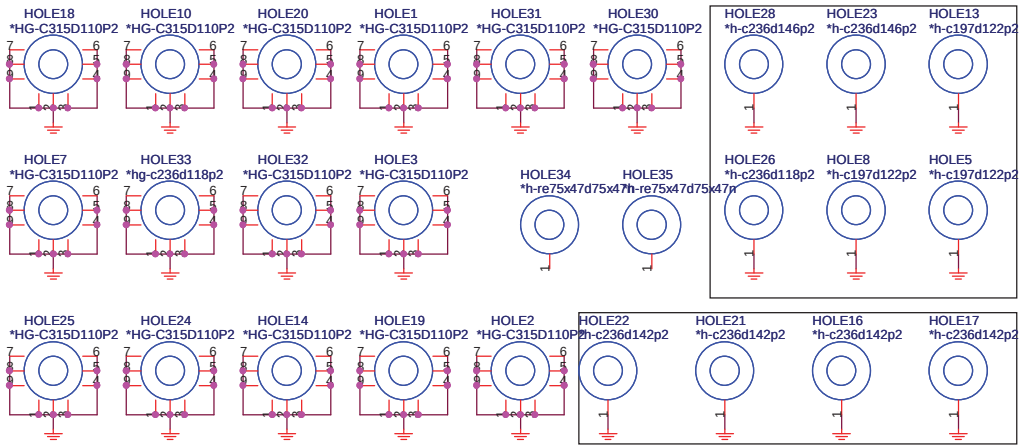


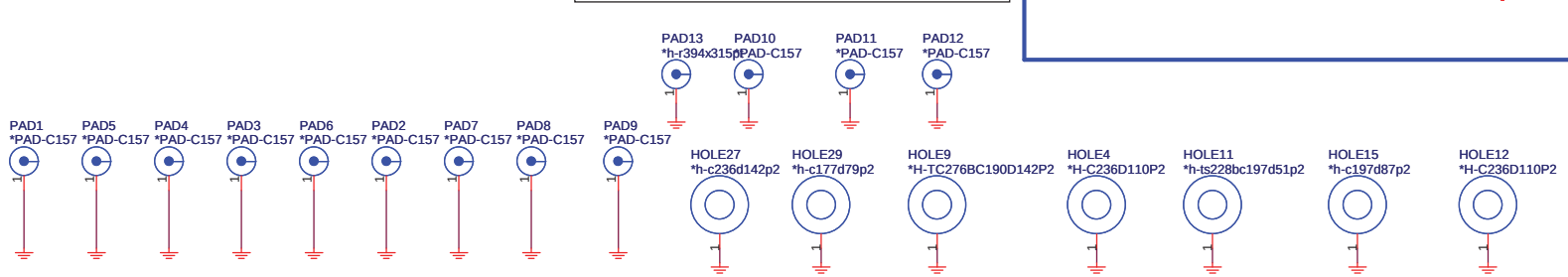
TOUCHPAD & Switch CONN.(TPD)











Quanta Computer Inc.

PROJECT : ZYD

Size	Document Number	Rev
	KB/FAN/TP+FP	3B

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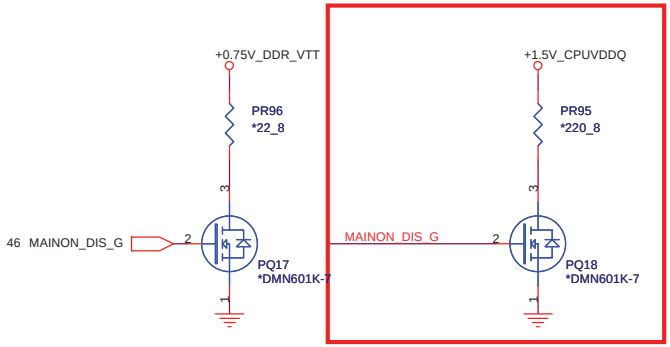
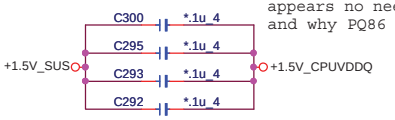
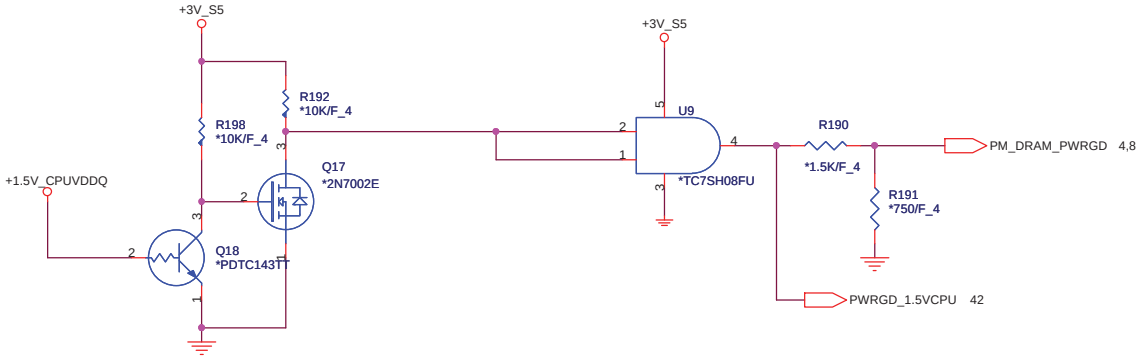
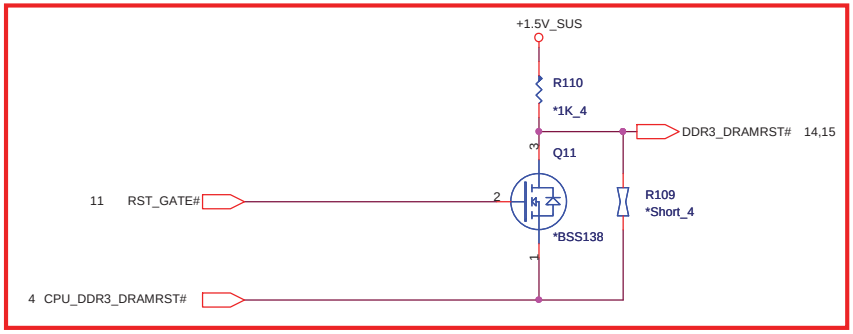
SM_DRAMRST# signal (to system memory) to be driven high
CKE signals (to system memory) to be driven low
VREFDQ and VREFCA voltage (on system memory) needs to be maintained
1.5-V power rail to system memory to be maintained.
All other DDR3 memory interface signals are don't care during S3 state for
memory self refresh.
SM_DRAMPWROK (to processor) is driven low during S3 as Processor VDDQ (1.5 V)
is turned off with this implementation.

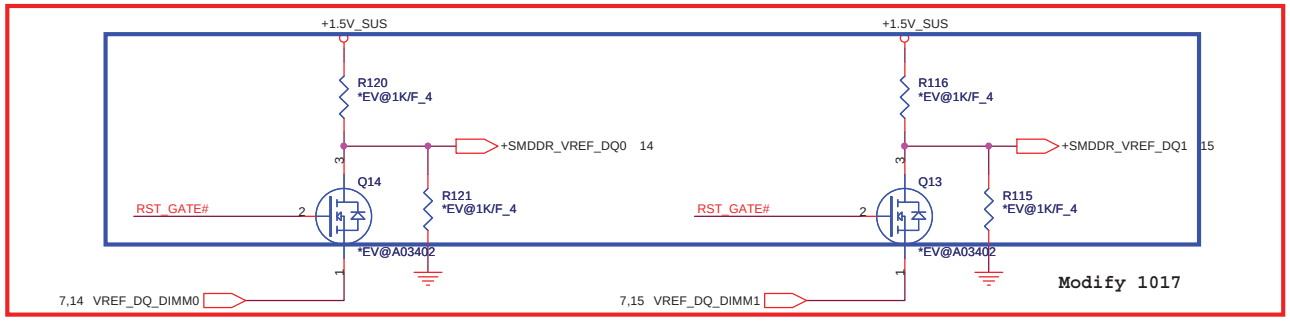


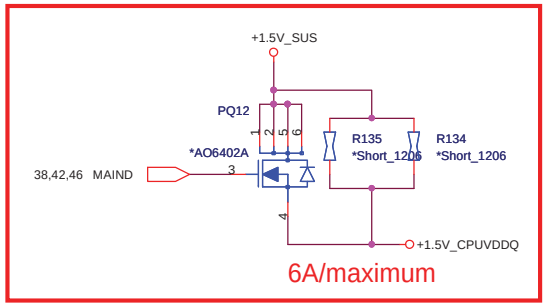
appears no need stuff if PQ12 don't stuff
and why PQ86 is 220ohm











These isolation FETs are not required for ARD-only
designs. Only CFD and common motherboard designs need to implement this circuit to
meet the DDR3 VREF specification during S3.

Quanta Computer Inc.
PROJECT : ZYD

Size	Document Number	Rev
	S3 power saving	3B
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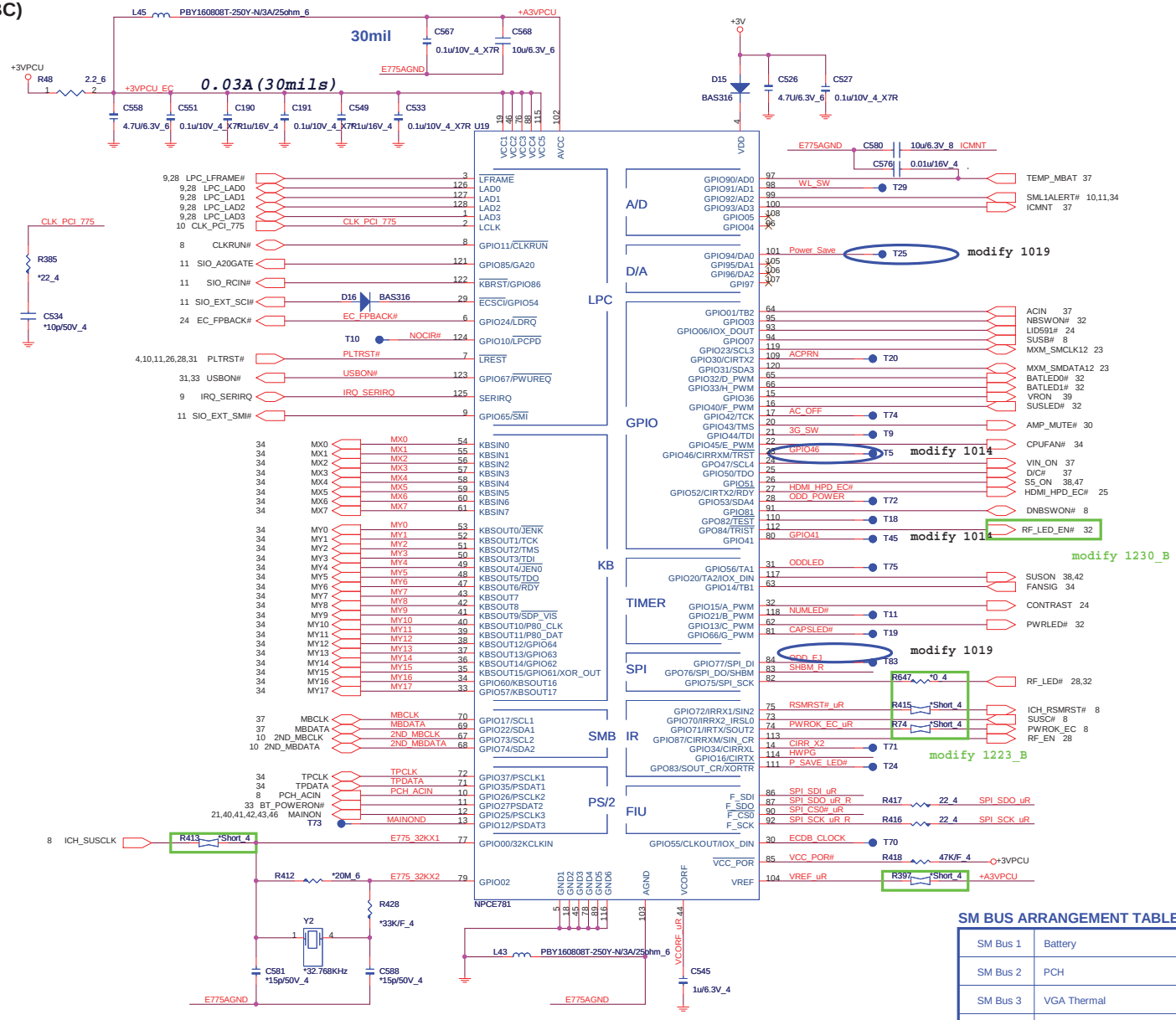
EC(KBC)

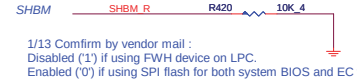


SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	VGA Thermal
SM Bus 4	

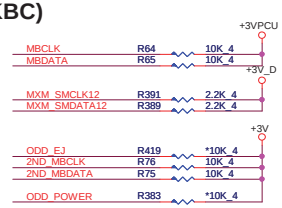
I/O ADDRESS SETTING(KBC)

SHBM=0: Enable shared memory with host BIOS

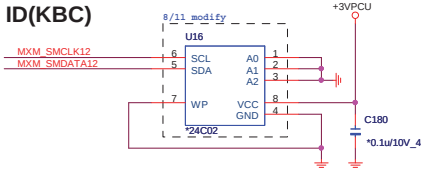


1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

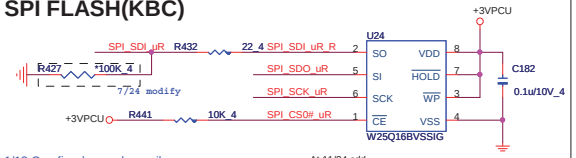
SM BUS PU(KBC)



ACER ID(KBC)



SPI FLASH(KBC)

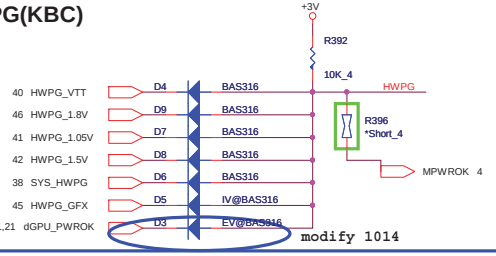


1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

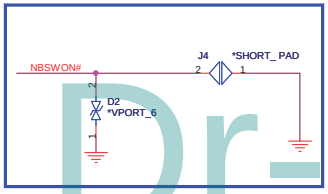
At 11/24 add

Winbond	W25X16AVSSIG	AKE38ZP0N01
MXIC	MX25L1605AM2C-15G	AKE37FP0Z13
EON	EN25F16-100HIP	AKE38ZA0Q00
AMIC	A25L016	AKE38ZN0800

HWPG(KBC)



POWER-ON Switch(KBC)



Modify 1028

INTERNAL KEYBOARD STRIP SET(KBC)

Quanta Computer Inc.
PROJECT : ZYD

Size	Document Number	Rev
	WPCE781 & FLASH	3B
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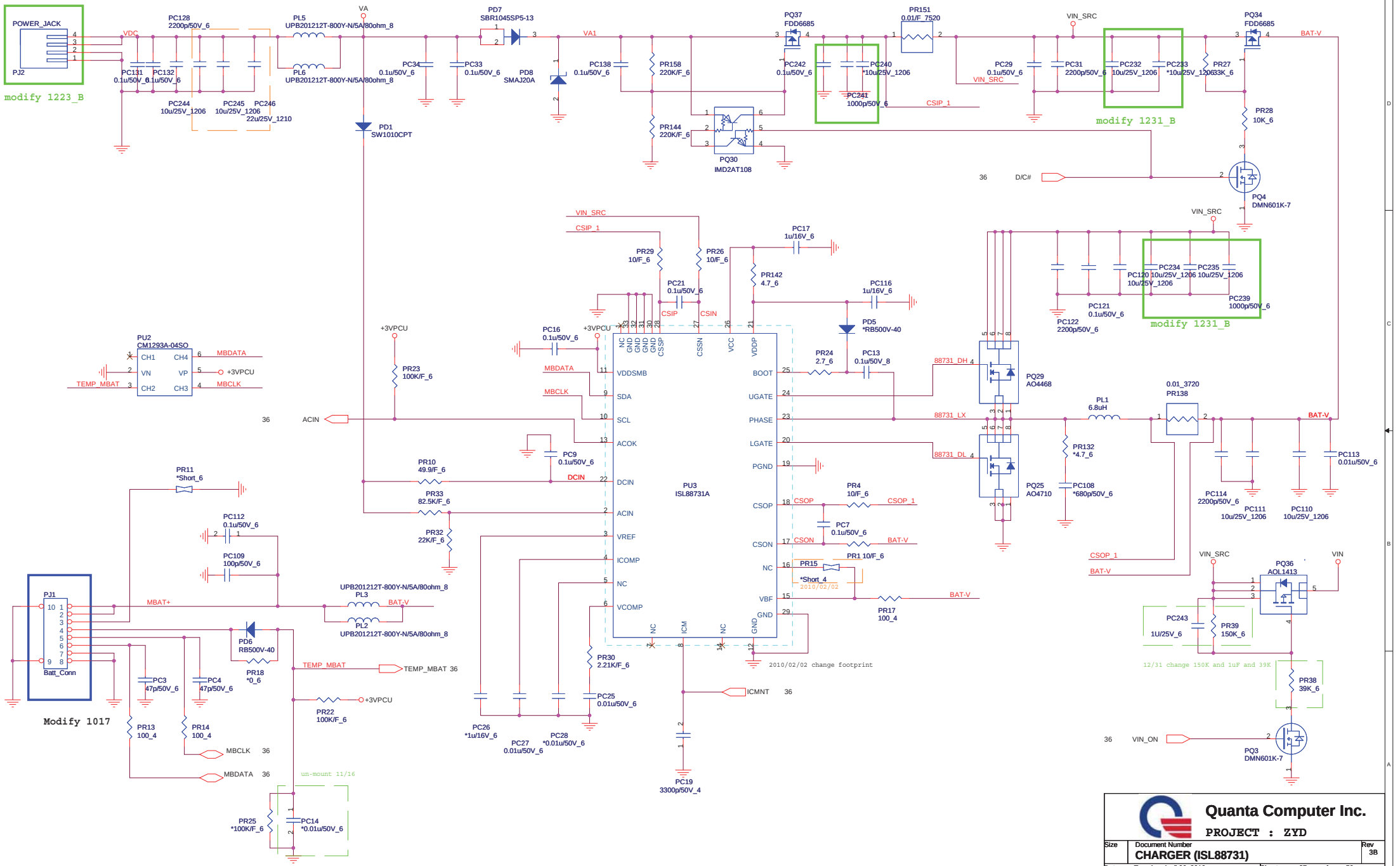
POWER_JACK
PJ2
modify 1223_B
VDC
PC128 2200p/50V_6
PC131 0.1u/50V_6
PC132 0.1u/50V_6
PC244 10u/25V_1206
PC245 10u/25V_1206
PC246 22u/25V_1210
PL5 UPB201212T-800Y-N/5A/80ohm_8
PL6 UPB201212T-800Y-N/5A/80ohm_8
VA
PD1 SW1010CPT
PC34 0.1u/50V_6
PC33 0.1u/50V_6
PD7 SBR1045SP5-13
PD8 SMAJ20A
VA1
PC138 0.1u/50V_6
PR158 220K/F_6
PR144 220K/F_6
PQ30 IMD2AT108
PQ37 FDD6685
PC242 0.1u/50V_6
PC240 *10u/25V_1206
PC241 1000p/50V_6
CSIP_1
PR151 0.01/F_7520
VIN_SRC
PC29 0.1u/50V_6
PC31 2200p/50V_6
PC232 10u/25V_1206
PC233 *10u/25V_1206
PR27 33K_6
modify 1231_B
PQ34 FDD6685
BAT-V
PR28 10K_6
36 D/C#
PQ4 DMN601K-7
VIN_SRC
PC234 10u/25V_1206
PC235 10u/25V_1206
PC120 10u/25V_1206
PC239 1000p/50V_6
PC121 0.1u/50V_6
PC122 2200p/50V_6
modify 1231_B
PU2 CM1293A-04SO
CH1
CH2
CH3
CH4
VN
VP
MBDATA
+3VPCU
MBCLK
TEMP_MBAT
36 ACIN
PR23 100K/F_6
+3VPCU
PC16 0.1u/50V_6
VIN_SRC
CSIP_1
PR29 10/F_6
PR26 10/F_6
PC17 1u/16V_6
PR142 4.7_6
PC21 0.1u/50V_6
CSIP
CSIN
PC116 1u/16V_6
PD5 *RB500V-40
PU3 ISL88731A
NC
GND
CSSP
CSSN
VCC
VDDP
VDDSMB
SDA
SCL
ACOK
DCIN
ACIN
VREF
ICOMP
NC
VCOMP
BOOT
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC
VBF
GND
ICM
PR24 2.7_6
PC13 0.1u/50V_8
88731_DH
88731_LX
88731_DL
PQ29 AO4468
PQ25 AO4710
PL1 6.8uH
0.01_3720
PR138
PR132 *4.7_6
PC108 *680p/50V_6
PC114 2200p/50V_6
PC111 10u/25V_1206
PC110 10u/25V_1206
PC113 0.01u/50V_6
PR4 10/F_6
CSOP
CSOP_1
PC7 0.1u/50V_6
CSON
BAT-V
PR1 10/F_6
PR15 *Short_4
2010/02/02
PR17 100_4
PC9 0.1u/50V_6
DCIN
PR10 49.9/F_6
PR33 82.5K/F_6
PR32 22K/F_6
PR11 *Short_6
PC112 0.1u/50V_6
PC109 100p/50V_6
PJ1
Batt_Conn
MBAT+
UPB201212T-800Y-N/5A/80ohm_8
PL3
PL2
UPB201212T-800Y-N/5A/80ohm_8
BAT-V
PD6 RB500V-40
PR18 *0_6
TEMP_MBAT
TEMP_MBAT 36
+3VPCU
PR22 100K/F_6
PC3 47p/50V_6
PC4 47p/50V_6
PR13 100_4
PR14 100_4
MBCLK 36
MBDATA 36
Modify 1017
un-mount 11/16
PR25 *100K/F_6
PC14 *0.01u/50V_6
PC26 *1u/16V_6
PC27 0.01u/50V_6
PC28 *0.01u/50V_6
PR30 2.21K/F_6
PC25 0.01u/50V_6
ICMNT 36
PC19 3300p/50V_4
2010/02/02 change footprint
PQ36 AOL1413
VIN
PC243 1U/25V_6
PR39 150K_6
12/31 change 150K and 1uF and 39K
PR38 39K_6
36 VIN_ON
PQ3 DMN601K-7
Quanta Computer Inc.
PROJECT : ZYD
Size
Document Number
CHARGER (ISL88731)
Rev 3B
Date: Tuesday, April 06, 2010
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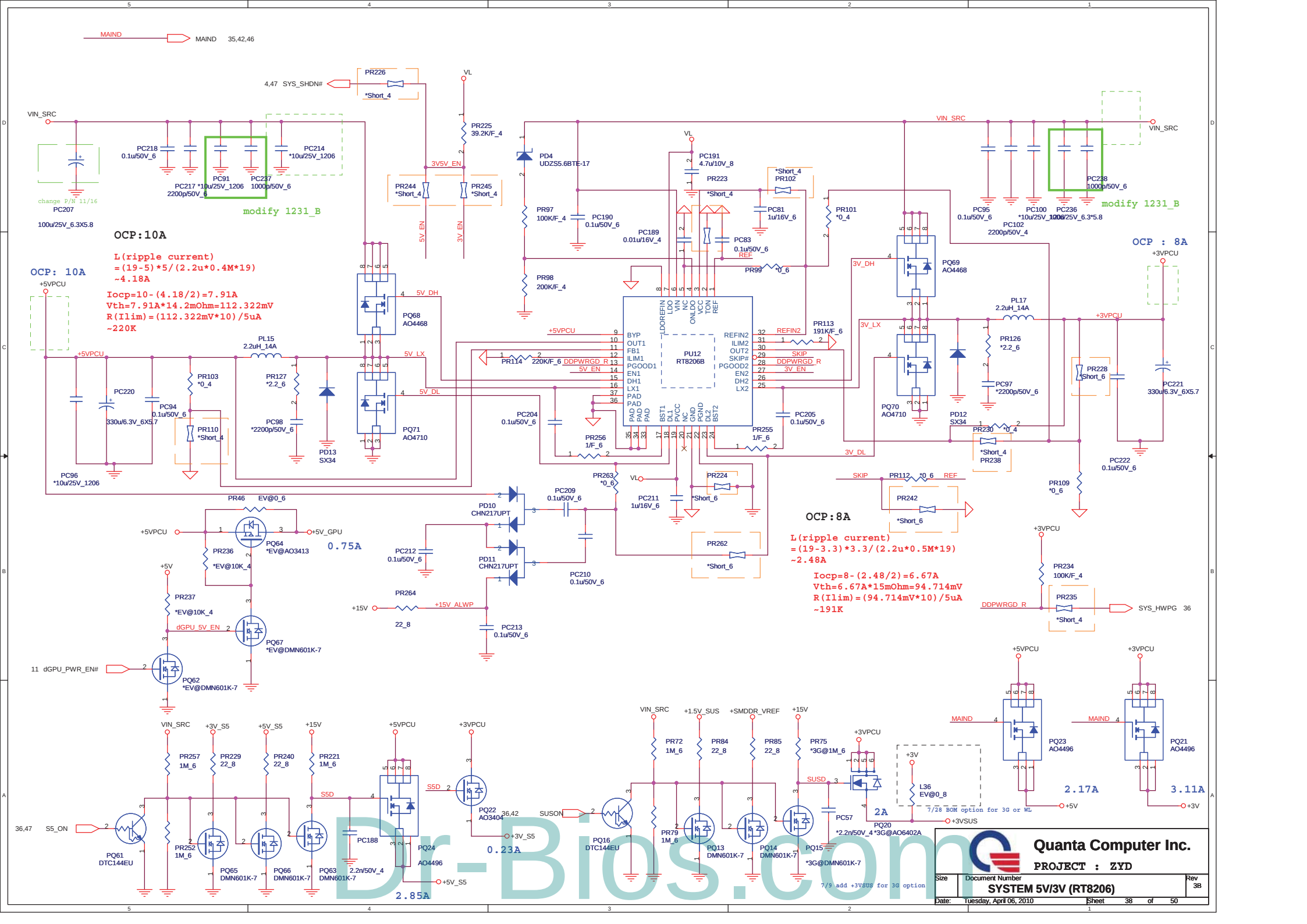
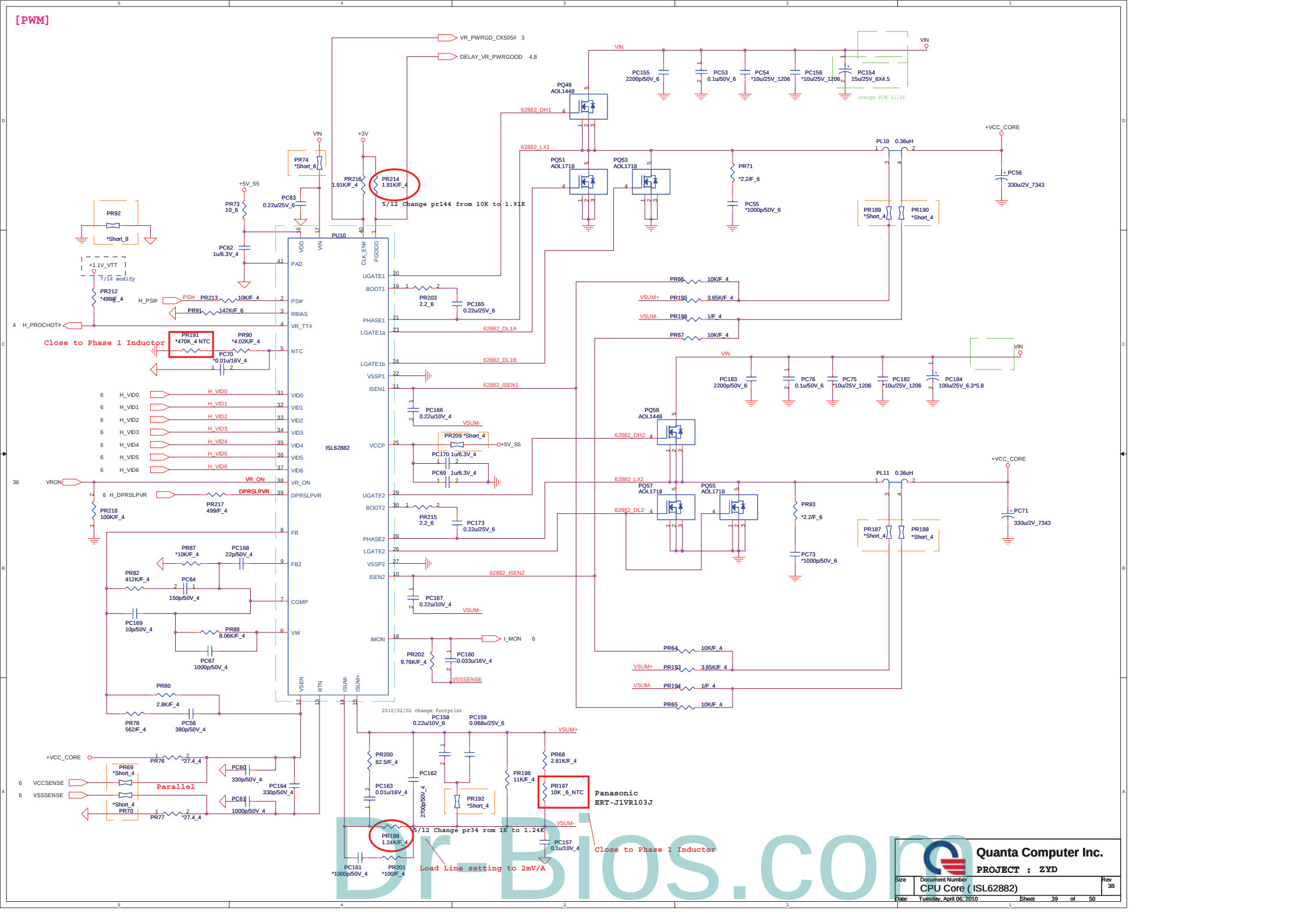


Quanta Computer Inc.

PROJECT : ZYD

Size	Document Number	Rev
	SYSTEM 5V/3V (RT8206)	3B
Date: Tuesday, April 06, 2010	Sheet 38 of 50	


[PWM]
VR_PWRGD_CK505# 3
DELAY_VR_PWRGOOD 4,8
VIN
+3V
+5V_S5
+VCC_CORE
PU10
ISL62882
PQ49 AOL1448
PQ51 AOL1718
PQ53 AOL1718
PQ58 AOL1448
PQ57 AOL1718
PQ55 AOL1718
PL10 0.36uH
PL11 0.36uH
62882_DH1
62882_LX1
62882_DL1A
62882_DL1B
62882_ISEN1
62882_DH2
62882_LX2
62882_DL2
62882_ISEN2
PR214 1.91K/F_4
5/12 Change pr144 from 10K to 1.91K
Close to Phase 1 Inductor
Parallel
Panasonic
ERT-J1VR103J
Close to Phase 1 Inductor
Load Line setting to 2mV/A
5/12 Change pr34 rom 1K to 1.24K
2010/02/02 change footprint
change P/N 11/16
7/16 modify
Quanta Computer Inc.
PROJECT : ZYD
CPU Core (ISL62882)
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Document Number
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3B
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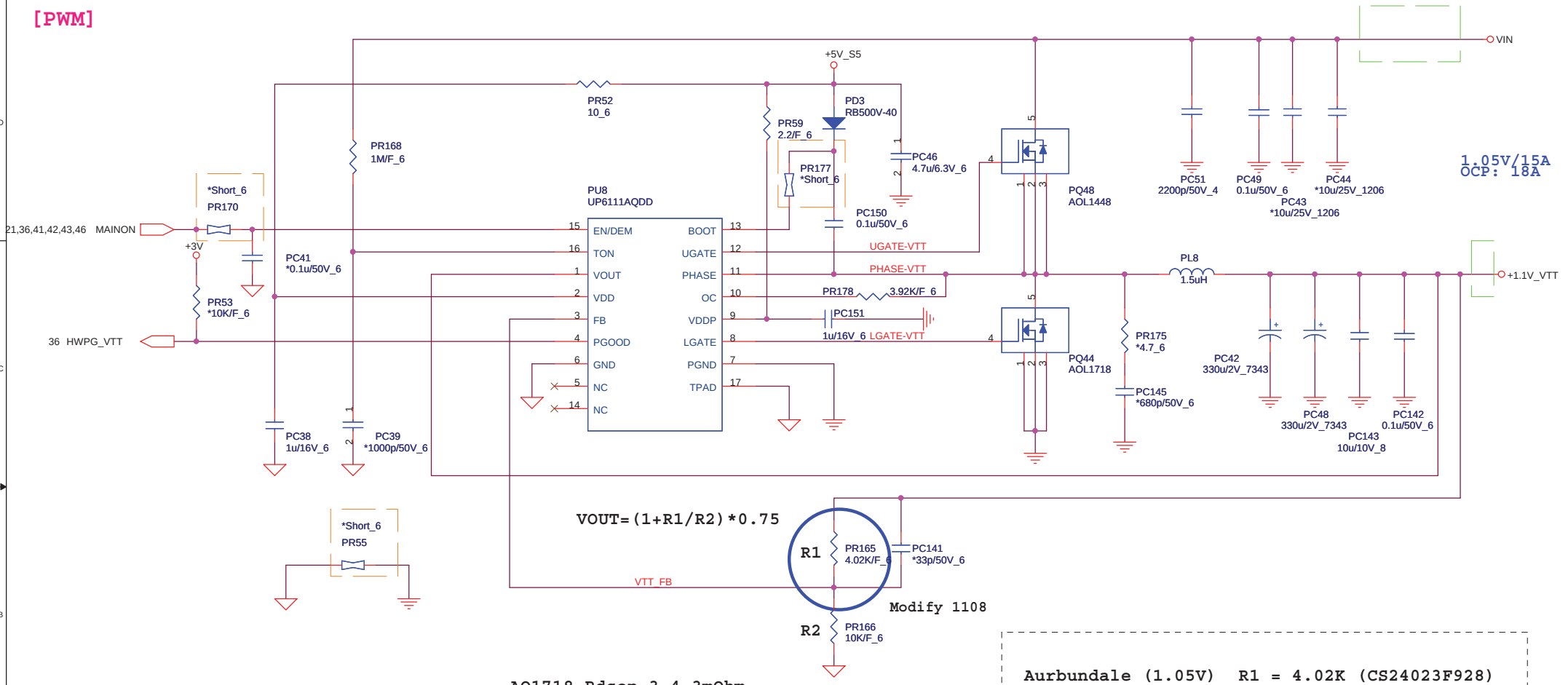
[PWM]



TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

AO1718 Rdson=3~4.3mOhm

L(ripple current)
=(19-1.05)*1.05/(1u*272k*19)
~3.64A

4.3m*18=RILIM*20uA
RILIM=3.87K --- 3.92K

Aurbundale (1.05V)	R1 = 4.02K (CS24023F928)
Clarksfield(1.1V)	R1 = 4.75K (CS24753F919)

Quanta Computer Inc.
PROJECT : ZYD

Size	Document Number	Rev
	+VTT (UP6111A)	3B
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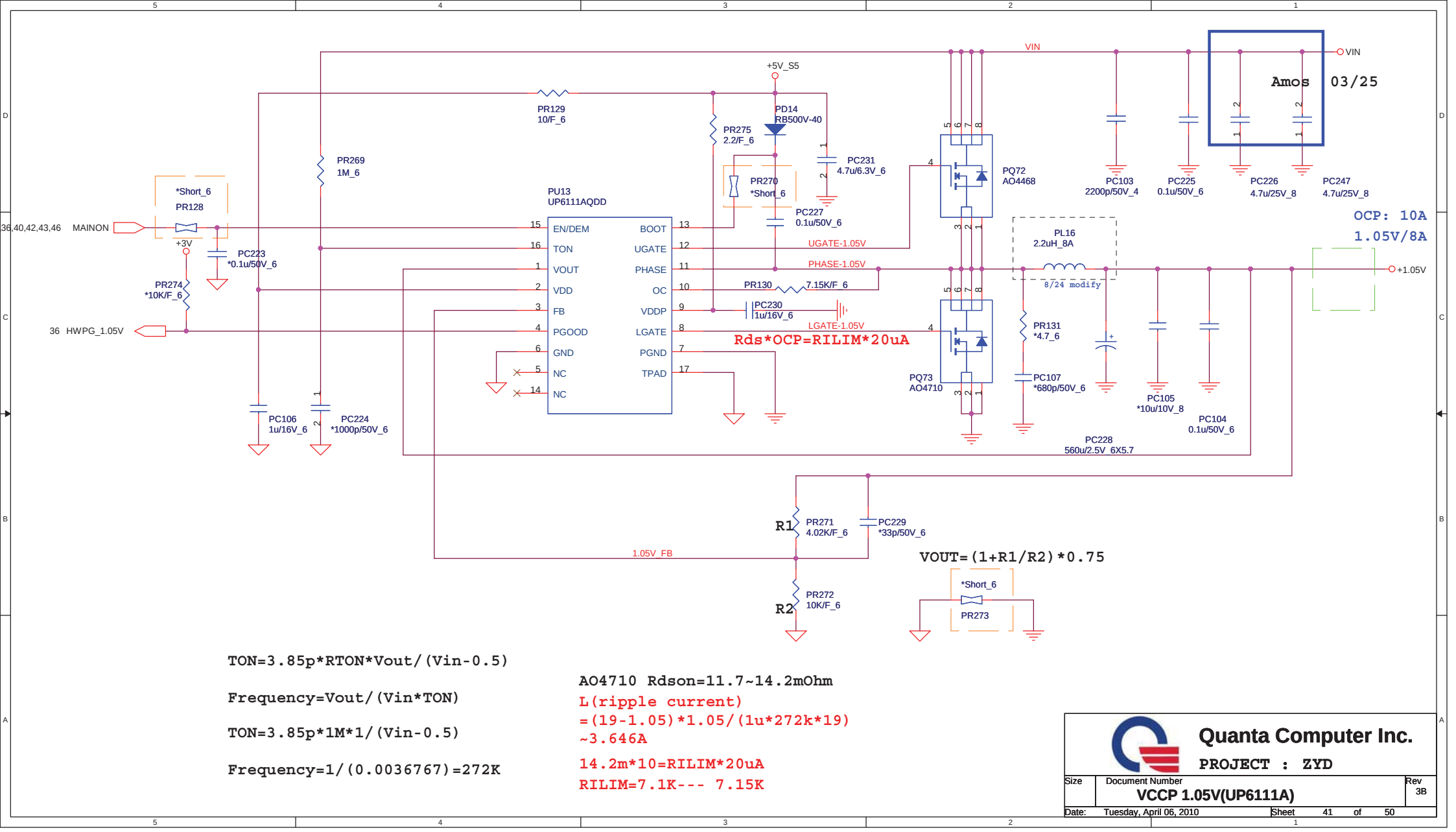


TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

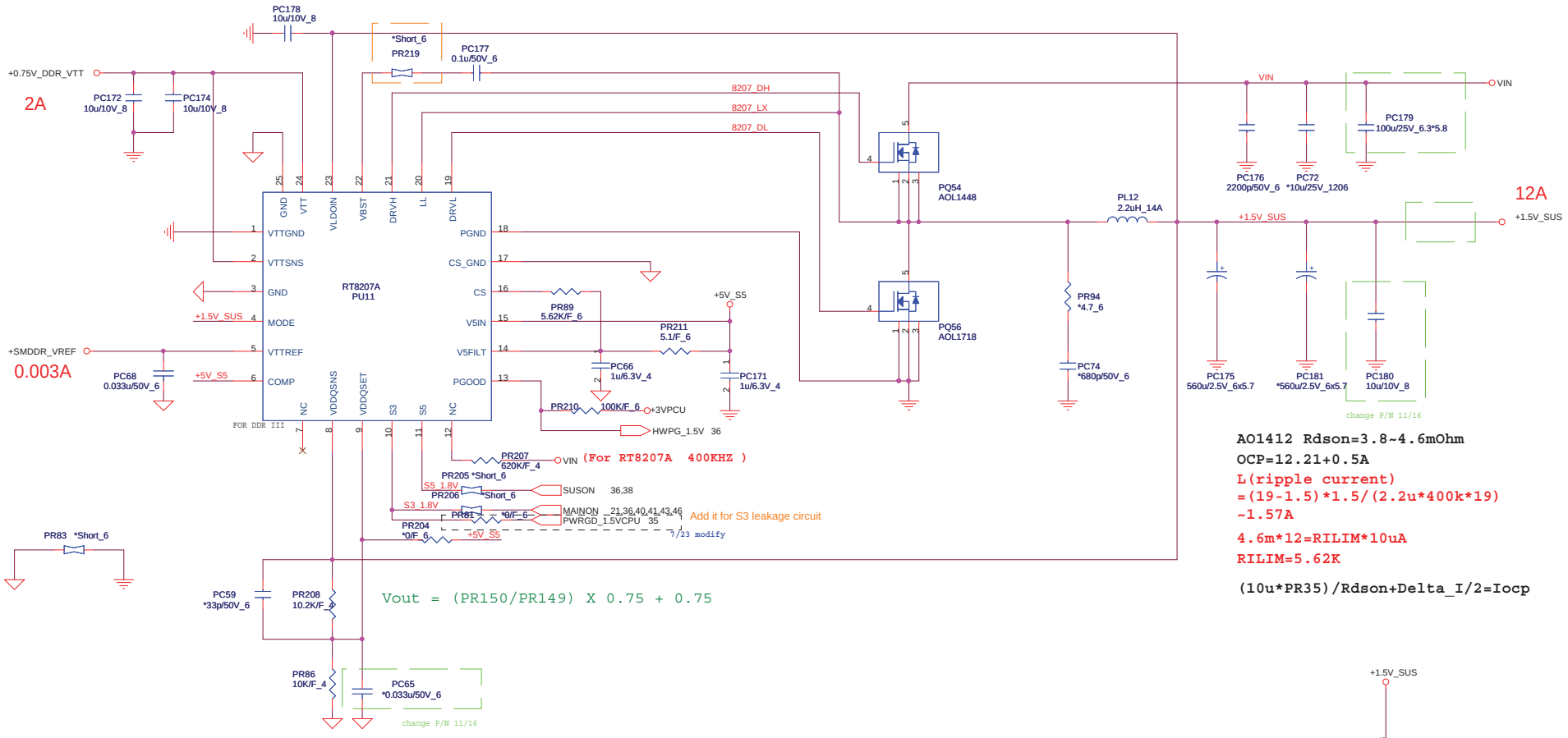
Frequency=1/(0.0036767)=272K

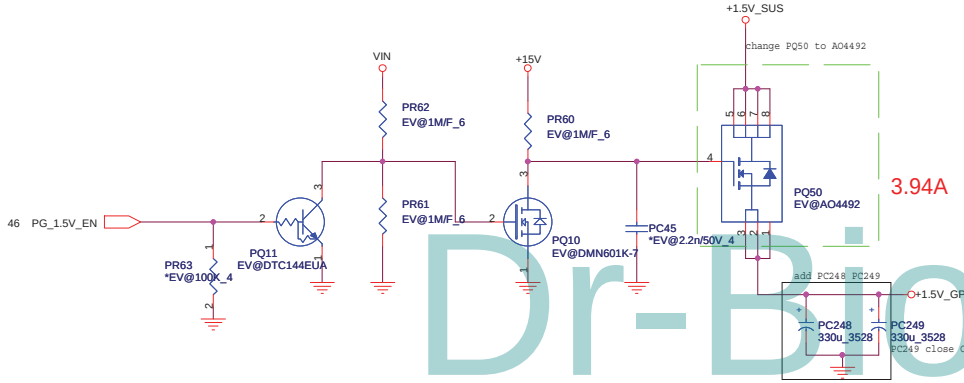
AO4710 Rdson=11.7~14.2mOhm

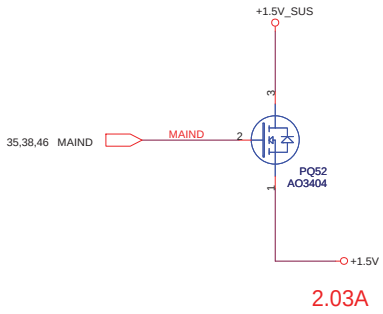
L(ripple current)
=(19-1.05)*1.05/(1u*272k*19)
~3.646A

14.2m*10=RILIM*20uA
RILIM=7.1K--- 7.15K

Quanta Computer Inc.		
PROJECT : ZYD		
Size	Document Number: VCCP 1.05V(UP6111A)	Rev: 3B
Date: Tuesday, April 06, 2010	Sheet 41 of 50	







Quanta Computer Inc.
PROJECT : ZYD

Size	Document Number	Rev
	DDR III 1.5V(TPS51116)	3B

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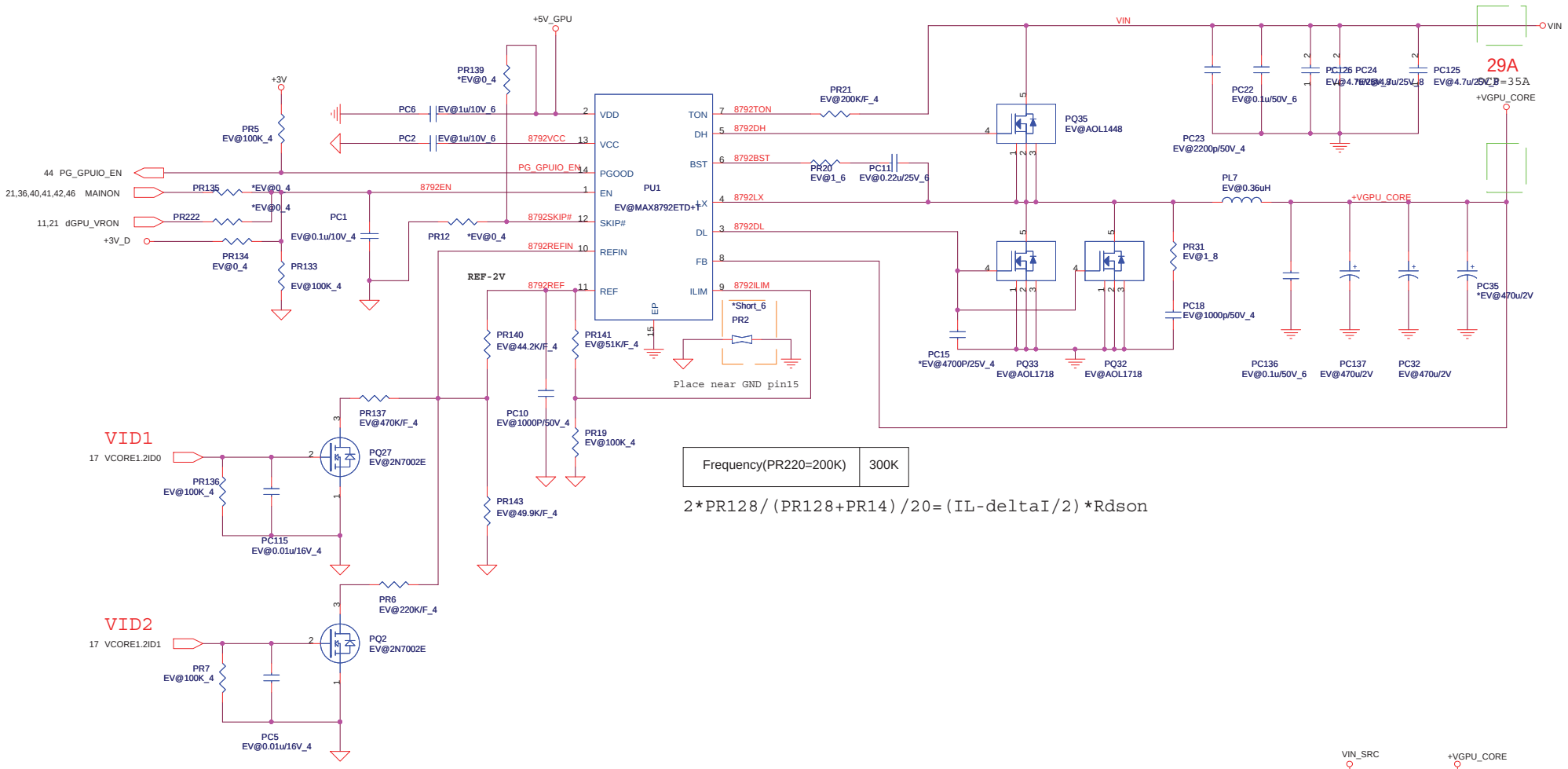


Frequency(PR220=200K)	300K

2*PR128/(PR128+PR14)/20=(IL-deltaI/2)*Rdson

Madison VID Table

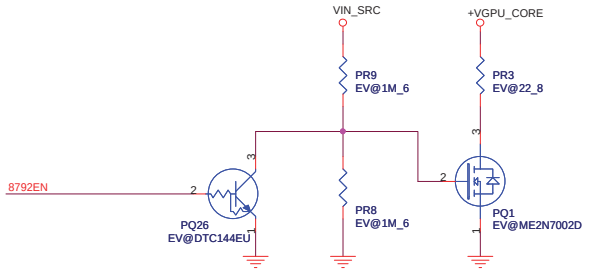
VID1	VID2		+VCC_GFX_CORE
VCORE1.2ID0	VCORE1.2ID1		
LOW (0)	LOW (0)		1.05V
HIGH (1)	LOW (0)		1.0V
LOW (0)	HIGH (1)		0.95V
HIGH (1)	HIGH (1)		0.90V

PR140 = 44.2K
PR143 = 49.9K
PR137 = 470K
PR6= 220K

PARK XT VID Table

VID1	VID2		+VCC_GFX_CORE
VCORE1.2ID0	VCORE1.2ID1		
LOW (0)	LOW (0)		1.12V
HIGH (1)	LOW (0)		1.05V
LOW (0)	HIGH (1)		0.95V
HIGH (1)	HIGH (1)		0.90V

PR140= 39.2K CS33922FB15
PR143 = 49.9K
PR137 = 332K CS43322FB15
PR6 = 130K CS41302FB00



Quanta Computer Inc.
PROJECT : ZYD

Size	Document Number	Rev
	GPU CORE(MAX8792)	3B

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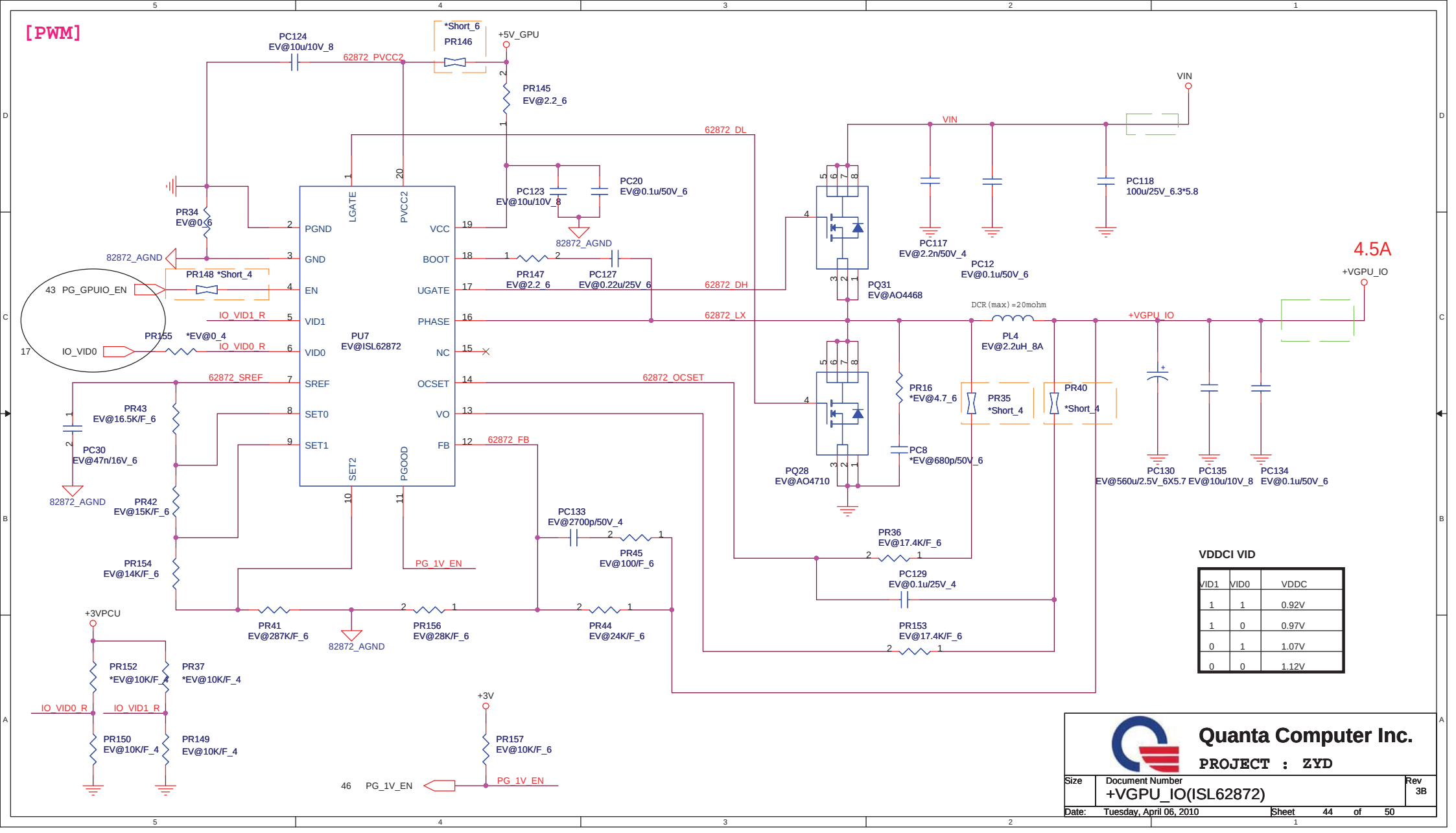
[PWM]
PC124
EV@10u/10V_8
62872_PVCC2
*Short_6
PR146
+5V_GPU
PR145
EV@2.2_6
62872_DL
VIN
PC118
100u/25V_6.3*5.8
PC117
EV@2.2n/50V_4
PC12
EV@0.1u/50V_6
PQ31
EV@AO4468
PC123
EV@10u/10V_8
PC20
EV@0.1u/50V_6
82872_AGND
PR34
EV@0_6
PR148 *Short_4
43 PG_GPUIO_EN
IO_VID1_R
IO_VID0
PR155 *EV@0_4
IO_VID0_R
PU7
EV@ISL62872
LGATE
PVCC2
PGND
GND
EN
VID1
VID0
SREF
SET0
SET1
SET2
PGOOD
VCC
BOOT
UGATE
PHASE
NC
OCSET
VO
FB
PR147
EV@2.2_6
PC127
EV@0.22u/25V_6
62872_DH
62872_LX
62872_SREF
62872_OCSET
62872_FB
DCR(max)=20mohm
PL4
EV@2.2uH_8A
4.5A
+VGPU_IO
PR16
*EV@4.7_6
PR35
*Short_4
PR40
*Short_4
PC8
*EV@680p/50V_6
PQ28
EV@AO4710
PC130
EV@560u/2.5V_6X5.7
PC135
EV@10u/10V_8
PC134
EV@0.1u/50V_6
PR43
EV@16.5K/F_6
PC30
EV@47n/16V_6
PR42
EV@15K/F_6
PR154
EV@14K/F_6
PC133
EV@2700p/50V_4
PR45
EV@100/F_6
PR36
EV@17.4K/F_6
PC129
EV@0.1u/25V_4
PR153
EV@17.4K/F_6
PR41
EV@287K/F_6
PR156
EV@28K/F_6
PR44
EV@24K/F_6
PG_1V_EN
+3VPCU
PR152
*EV@10K/F_4
PR37
*EV@10K/F_4
PR150
EV@10K/F_4
PR149
EV@10K/F_4
+3V
PR157
EV@10K/F_6
46 PG_1V_EN
VDDCI VID
VID1 VID0 VDDC
1 1 0.92V
1 0 0.97V
0 1 1.07V
0 0 1.12V
Quanta Computer Inc.
PROJECT : ZYD
Size
Document Number
+VGPU_IO(ISL62872)
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3B
Date: Tuesday, April 06, 2010
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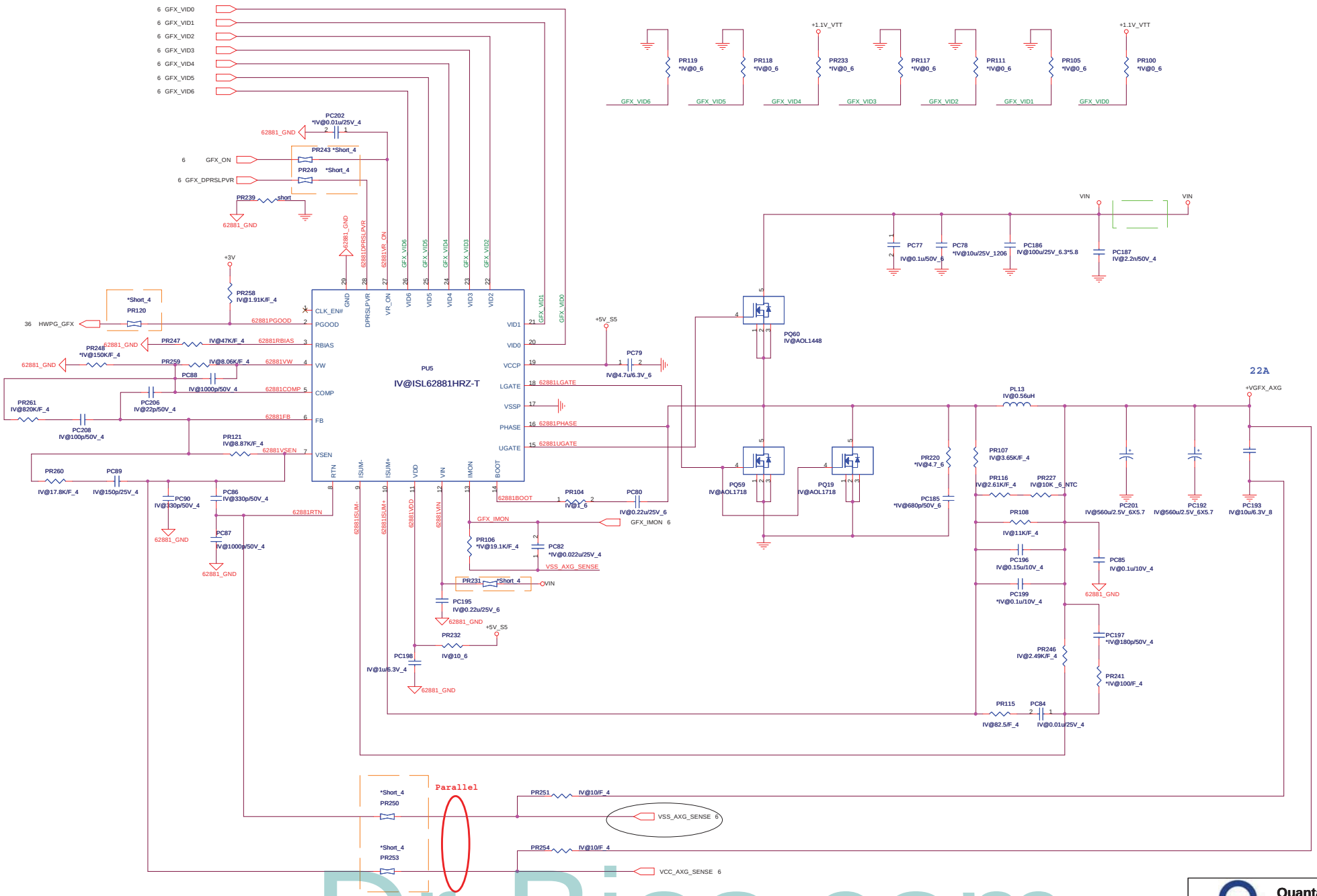
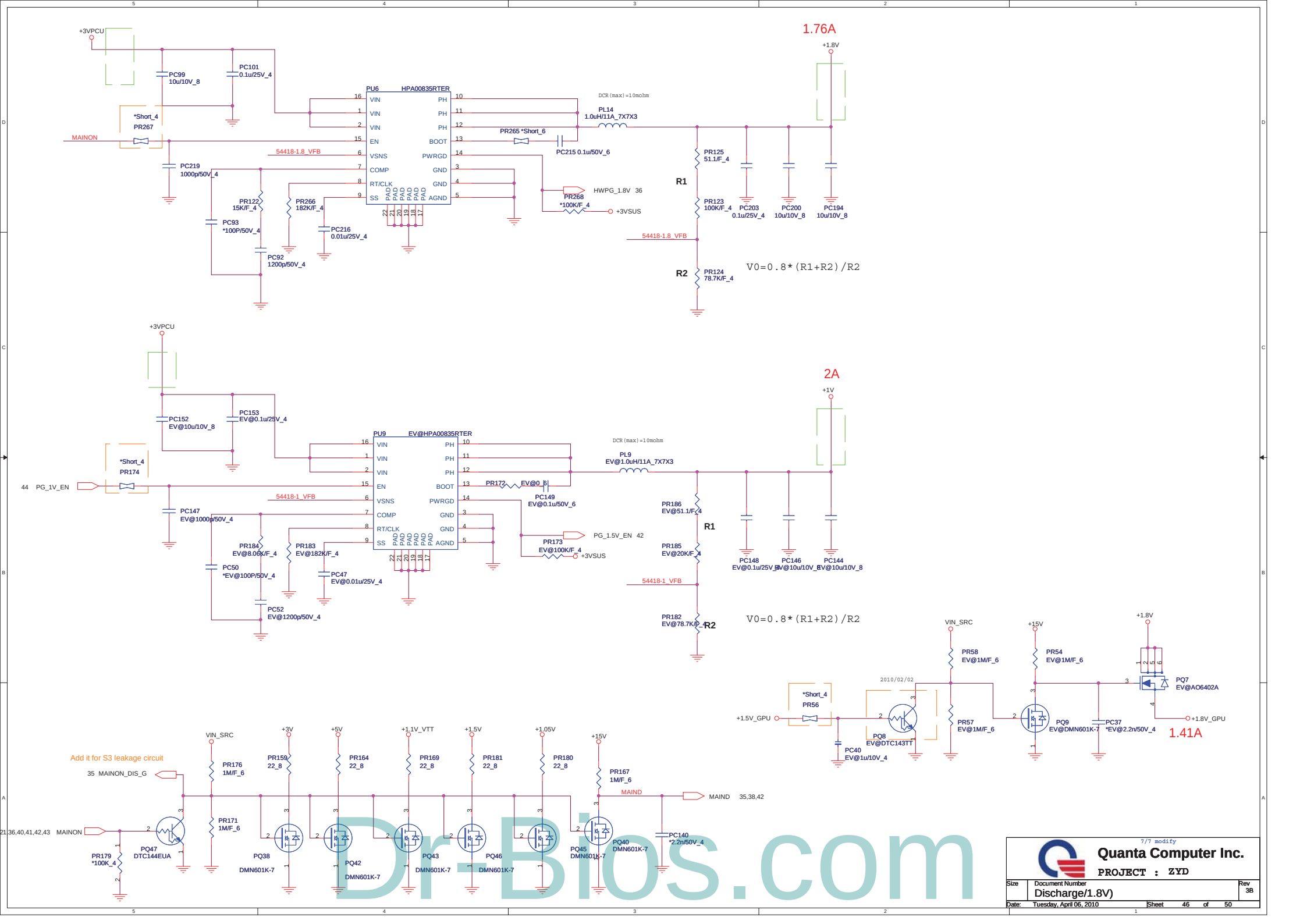
Int_VGA [PWM]



1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and molding resins only from the business Partners that Sony approves as Green Partners.

Quanta Computer Inc.
PROJECT : ZYD

Size	Document Number	Rev
	+VGFX_AXG (ISL62881)	3B
Date: Tuesday, April 06, 2010	Sheet 45 of 50	


1.76A
+3VPCU
PC99 10u/10V_8
PC101 0.1u/25V_4
*Short_4 PR267
MAINON
PU6 HPA00835RTER
VIN PH BOOT PWRGD GND AGND VSNS COMP RT/CLK SS EN PAD
PL14 1.0uH/11A_7X7X3
DCR(max)=10mohm
PR265 *Short_6
PC215 0.1u/50V_6
+1.8V
PR125 51.1/F_4
PR123 100K/F_4
R1
R2
PR124 78.7K/F_4
PC203 0.1u/25V_4
PC200 10u/10V_8
PC194 10u/10V_8
54418-1.8_VFB
PR268 *100K/F_4
HWPG_1.8V 36
+3VSUS
PC219 1000p/50V_4
PR122 15K/F_4
PR266 182K/F_4
PC93 *100P/50V_4
PC216 0.01u/25V_4
PC92 1200p/50V_4
V0=0.8*(R1+R2)/R2
2A
+3VPCU
PC152 EV@10u/10V_8
PC153 EV@0.1u/25V_4
*Short_4 PR174
44 PG_1V_EN
PU9 EV@HPA00835RTER
PL9 EV@1.0uH/11A_7X7X3
PR172 EV@0_8
PC149 EV@0.1u/50V_6
PG_1.5V_EN 42
PR173 EV@100K/F_4
+3VSUS
54418-1_VFB
PC147 EV@1000p/50V_4
PR184 EV@8.06K/F_4
PR183 EV@182K/F_4
PC50 *EV@100P/50V_4
PC47 EV@0.01u/25V_4
PC52 EV@1200p/50V_4
+1V
PR186 EV@51.1/F_4
PR185 EV@20K/F_4
PR182 EV@78.7K/F_4
PC148 EV@0.1u/25V_4
PC146 EV@10u/10V_8
PC144 EV@10u/10V_8
V0=0.8*(R1+R2)/R2
2010/02/02
VIN_SRC
+15V
+1.8V
PR58 EV@1M/F_6
PR54 EV@1M/F_6
PQ7 EV@AO6402A
*Short_4 PR56
+1.5V_GPU
PQ8 EV@DTC143TT
PC40 EV@1u/10V_4
PR57 EV@1M/F_6
PQ9 EV@DMN601K-7
PC37 *EV@2.2n/50V_4
+1.8V_GPU
1.41A
Add it for S3 leakage circuit
35 MAINON_DIS_G
VIN_SRC
+3V
+5V
+1.1V_VTT
+1.5V
+1.05V
+15V
PR176 1M/F_6
PR159 22_8
PR164 22_8
PR169 22_8
PR181 22_8
PR180 22_8
PR167 1M/F_6
MAIND
MAIND 35,38,42
21,36,40,41,42,43 MAINON
PR171 1M/F_6
PR179 *100K_4
PQ47 DTC144EUA
PQ38 DMN601K-7
PQ42 DMN601K-7
PQ43 DMN601K-7
PQ46 DMN601K-7
PQ45 DMN601K-7
PQ40 DMN601K-7
PC140 *2.2n/50V_4
Dr-Bios.com
7/7 modify
Quanta Computer Inc.
PROJECT : ZYD
Size
Document Number
Discharge/1.8V)
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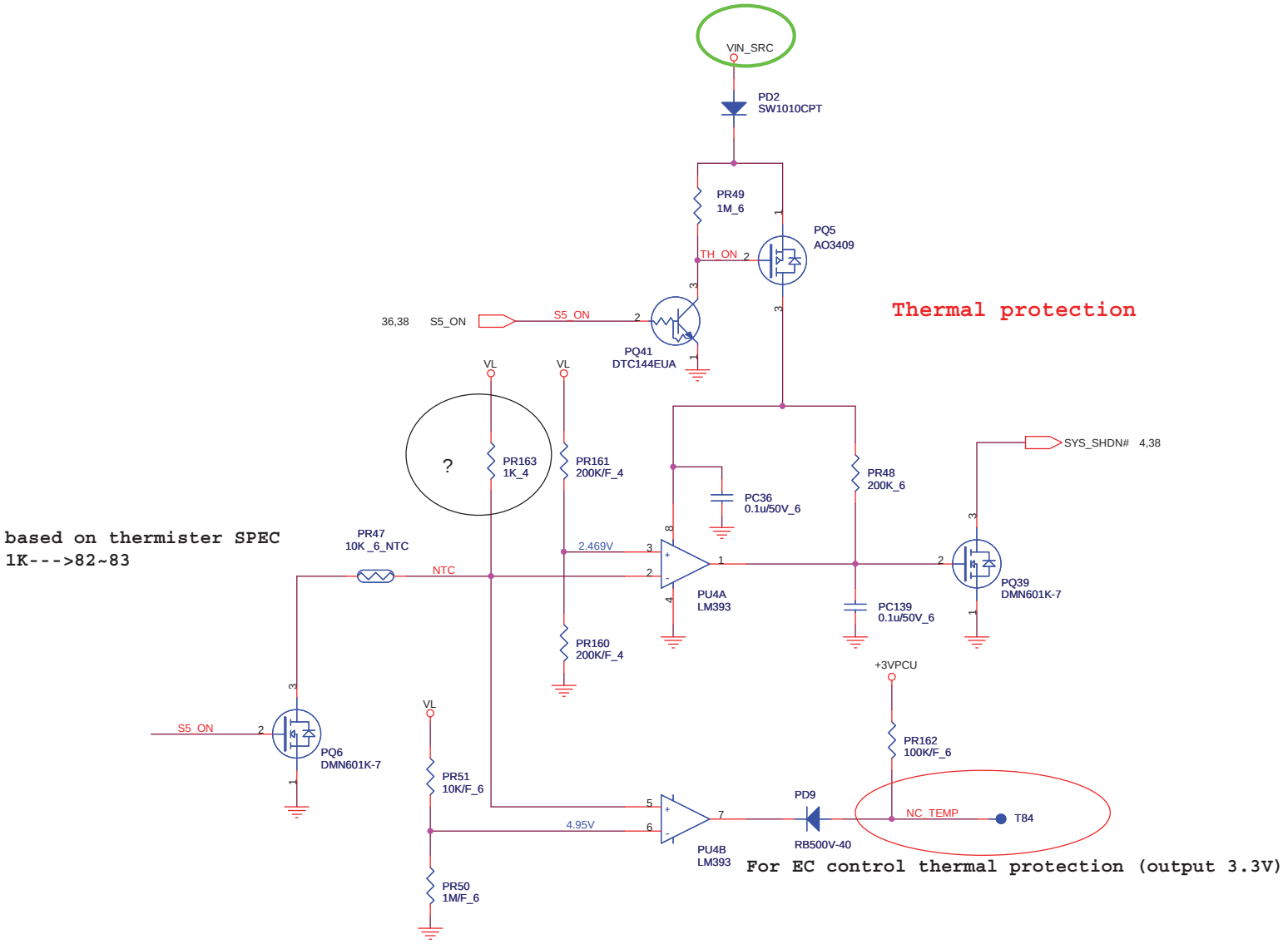
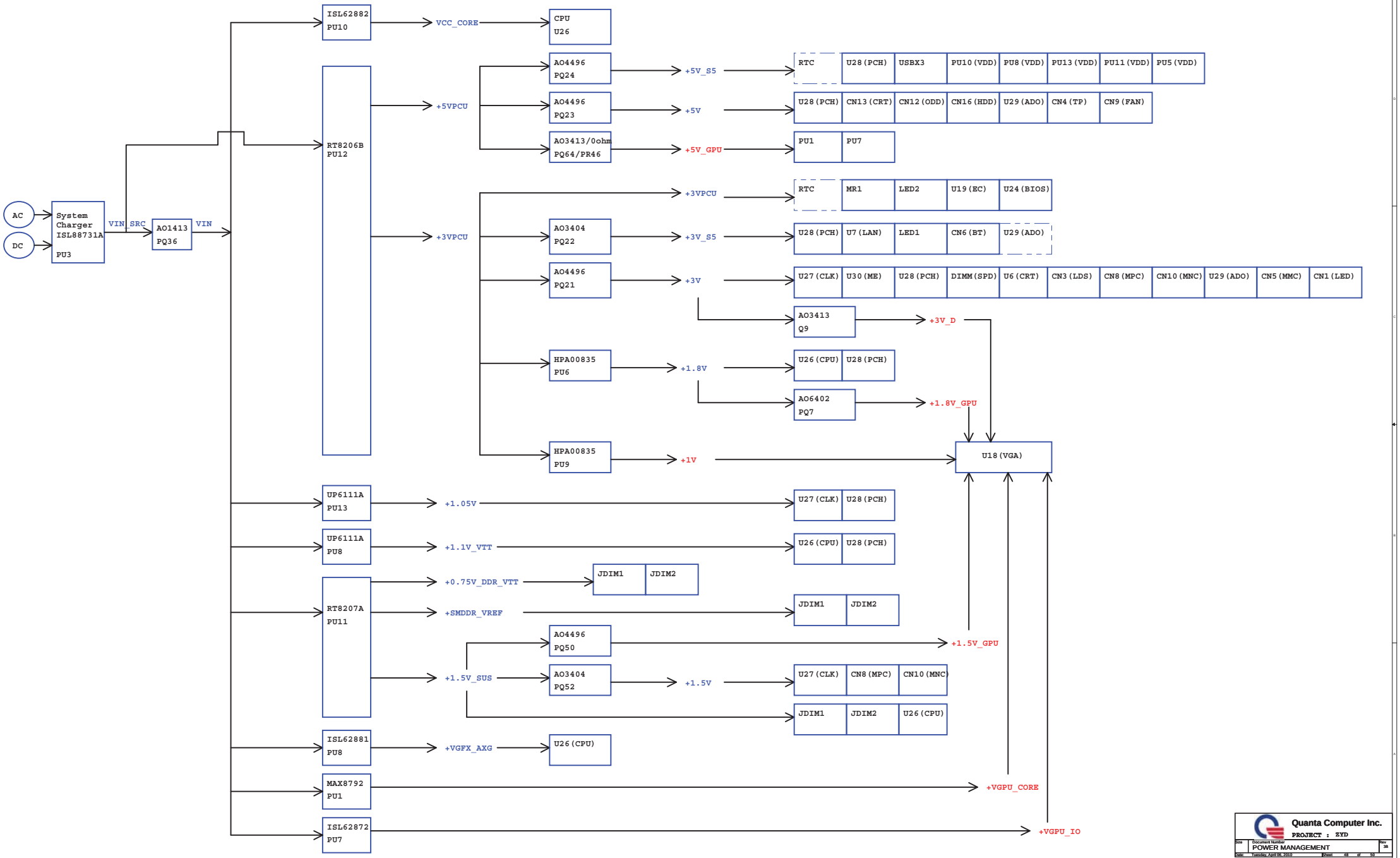


Quanta Computer Inc.

PROJECT : ZYD

Size	Document Number	Rev
	Thermal Protection	3B
Date: Tuesday, April 06, 2010	Sheet 47 of 50	



Quanta Computer Inc.
PROJECT : ZYD
Size | Document Number: POWER MANAGEMENT | Rev: 3A
Date: Tuesday, April 06, 2010 | Sheet 48 of 50

Model	REV	CHANGE LIST	MODEL	ZYD FROM	ZYD To
ZYD MB	1A	20091028 Page 30, Move the resisters and common chokes from M/B to daughter board		X	1A
		20091028 Page 30, Move the R1027 and R1059 to daughter board and change to 0402 (place closer).		X	1A
		20091028 Page 30, Move USB Power switch to daughter board		X	1A
		20091028 Page 30, Change card reader&USB board CONN P/N to DFFC20FR255		X	1A
		20091028 Page 26, Delete R203 and R171 to leave RJ45 chasiss contact to GND directly		X	1A
		20091028 Page 31, Add net name susled#_R, Pwrled#_R,BATLED0#_R, BATLED1#_R,RFLED#_R,RFLED2#_R		X	1A
		20091028 Page 35, Add SW1 for debug purpose		X	1A
		20091028 Page 33, update Hole footprints		X	1A
		20091029 Page 41, Change PR199, PR200 P/N from CS00003J951 to CS00003F916		X	1A
		20091102 Page 24, 29, Add Mic_GND for internal analog MIC		X	1A
		20091102 Page 27, Delete C204, C208, C558, R411, R385, R373, RP3, Q27, Q26. and change C578 from 0.47u to 4.7u		X	1A
		20091102 Page 10, Stuff R1001, R1002, R503		X	1A
		20091103 Page 33, Delete Hole4, Hole5, Hole8, Hole18		X	1A
		20091104 Page 33, update power schematic		X	1A
		20091104 Page 30, swap L38,L39,L58 USB nets for layout request.		X	1A
		20091108 Page 45, delete net name MAINON_G		X	1A
		20091108 Page 39, Change PR151 P/N from CS24703F908 to CS24023F928 for support Arrandale only		X	1A
		20091108 Page 33, Delete Hole36		X	1A
		20091110 Page 31, Move Wi-Fi LED to PB		X	1A
		20091111 Page 39, Delete PL8 and Change PL9 footprint and value(1.5uH footprint:CHOKE-ETQP4LR36WFC-NB4)		X	1A
		20091111 Page 41, Stuff +1.5V_GPU power source for EV# only		X	1A
		20091111 Page 37, reserve PR275 for GPU power		X	1A
		20091112 Page 18, Follow ATI suggestion to modify R419 from 680ohm to 51 ohm.		X	1A
		20091112 Page 27, Remove LPC from Mini PCIE port CN24		X	1A
		20091112 Page 37,45, unstuff +3V_SUS components		X	1A
		20091113 Page 27, Two Wi-Fi LED share one net RF_LED#		X	1A
		20091113 Page 31, Delete Q21,Q23, R347		X	1A
		20091113 Page 29, Reserve three more resistors R373, R368, R385 for ESD solution		X	1A
		20091116 Page 34, unstuff PR95, PR96, PQ17, PQ15		X	1A
		20091116 Page 24, Change C650 from 0.22u/6.3V_4 to 0.22u/10V_4		X	1A
		20091116 Page 32, Change C399 from 1U/6.3V_4 to 1u/10V_4		X	1A
		20091116 Page 7, unstuff R159		X	1A
		20091116 Page 11, stuff R592 for DIS and stuff R595 for UMA		X	1A
		20091116 Page 11, Reserve pull low for unused pin dGPU_VRON_R		X	1A
		20091116 Page 8, Delete R414		X	1A
		20091116 Page 25, Delete R162		X	1A
		20091116 Page 36-45, PC14 un-mount; PC207 change P/N; PC154 change P/N and value.; PC155 un-mount; PC180 change P/N; PC119 change P/N; PC118 change P/N		X	1A
	2A	20091119 Page 36, Modify Bat CONN P/N and footprint		1A	2A
		20091119 Page 29, Modify Speaker CN7 P/N from DFHD04MR779 to DFHD04MR057		1A	2A
		20091120 Page 8~13, Modify PCH P/N from AJ0QMGS0T05 to AJSLGZS0T07		1A	2A
		20091124 Page 27, Short Pin42 and Pin44 of CN8 and CN10 to support Intel WiMAX/WiFi combo module		1A	2A
		20091128 Page 37, stuff L36 for discrete sku		1A	2A
		20091128 Page 9, change U30(ME ROM) P/N from AKE391P0N00 to AKE38ZP0N01		1A	2A
		20091202 Page 3, reserve 1U for CLK GEN +1.5V power		1A	2A
		20091203 Page 27, Stuff Q26 and Q28; unstuff R401 and R447; and add LPC bus to CN24 for debug purpose		1A	2A
		20091209 Page 42, add VID table for Park XT		1A	2A
		20091209 Page 3, change R257 from 0ohm to 33ohm		1A	2A
		20091209 Page 3,17,18 follow AMD suggestion to stuff R257, R101, R407,R409 amd remove R36 to fix AMD pre-production silicon bug		1A	2A
		20091214 Page 9, change R317 to a JP and stuff R322		1A	2A
		20091214 Page 32, change CN6 from DFHD05MRD98 to DFWF05MR027		1A	2A
		20091221 Page 29, change R533 from CS03923F916 to CS33922FB15		1A	2A
		20091223 Page 10, change R202, R203, R540, R566, R547 to short pad		1A	2A
		20091223 Page 36, change DC jack P/N to DFHS04FR741		1A	2A
		20091223 Page 32, change CN6 P/N to DFWF05MR012		1A	2A
		20091225 Page 50, change CN19 P/N to DFHD19MR083		1A	2A
		20091230 Page 12, Add C786 for CRT flicker issue		1A	2A
		20091230 Page 27, change transformer footprint to TRF-10-1-24P-SMT		1A	2A
		20091230 Page 17, change VGFU_CORE VID control pin		1A	2A
		20091230 Page 28, Exchange P/N for cn8 and cn10		1A	2A
		20091230 Page 28, Move controller link from CN10 to CN8		1A	2A
	3A	20100129 Page 32, remove power LED MOS Q25		2A	3A
		20100130 Page 18, Remove AMD option 2 workaround for Madison and Park; and change R36 from 1K to 10K		2A	3A
		20100130 Page 28, Change Mini card footprint to MIPCI-800055FB052GX-52P-LDV-NB4		2A	3A
		20100201 Page 32, restore power LED MOS Q25		2A	3A
		20100201 Page 25, Change Q33,Q34 to ESD protection part		2A	3A
		20100222 Page 24, Reserve C787 and C788 for CRT flicker issue		2A	3A
		20100222 Page 36, Remove SW1		2A	3A
		20100222 Page 12, Add C789 for VCCADAC		2A	3A
		20100222 Page 17, Reserve 10U*2 caps for +1.8V_GPU		2A	3A
		20100222 Page 30, Add short Pad R635,R636,R637,R638,R640 for EMI		2A	3A
		20100222 Page 24, unstuff L13 and stuff R89 and R90		2A	3A

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Model	REV	CHANGE LIST
ZYD MB	3B	20100322 Page 32, delete Q25 20100322 Page 44,45 modify PU5,PU7 footprint 20100324 Page 44,45 change PC184,PC179,PC207,PC125,PC236,PC118,PC186 P/N to CC71004MZ04 20100324 Page 43 change PC126, PC24, PC125 to CH5474KEA06(4.7uF 25V 0805) 20100324 Page 30 change R298,R314 to 39ohm 20100325 reserved EMI chock lacation for USB 1/3/11/12/8 20100325 Page 41 change PC226 to 0805 4.7uF/25V,and add PC247 ,BOM stuff. 20100325 Page 30 change R223,R347,C444,R252, R590 and R306 to short pad.

MODEL	ZYD	
	FROM	To
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B

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