

# PEGATRON CONFIDENTIAL

MODEL NAME :

PCB NO :

69- P/N :

## BA52\_CP Colay Schematic

Intel Arrandale rPGA-989

PCH BGA 1071

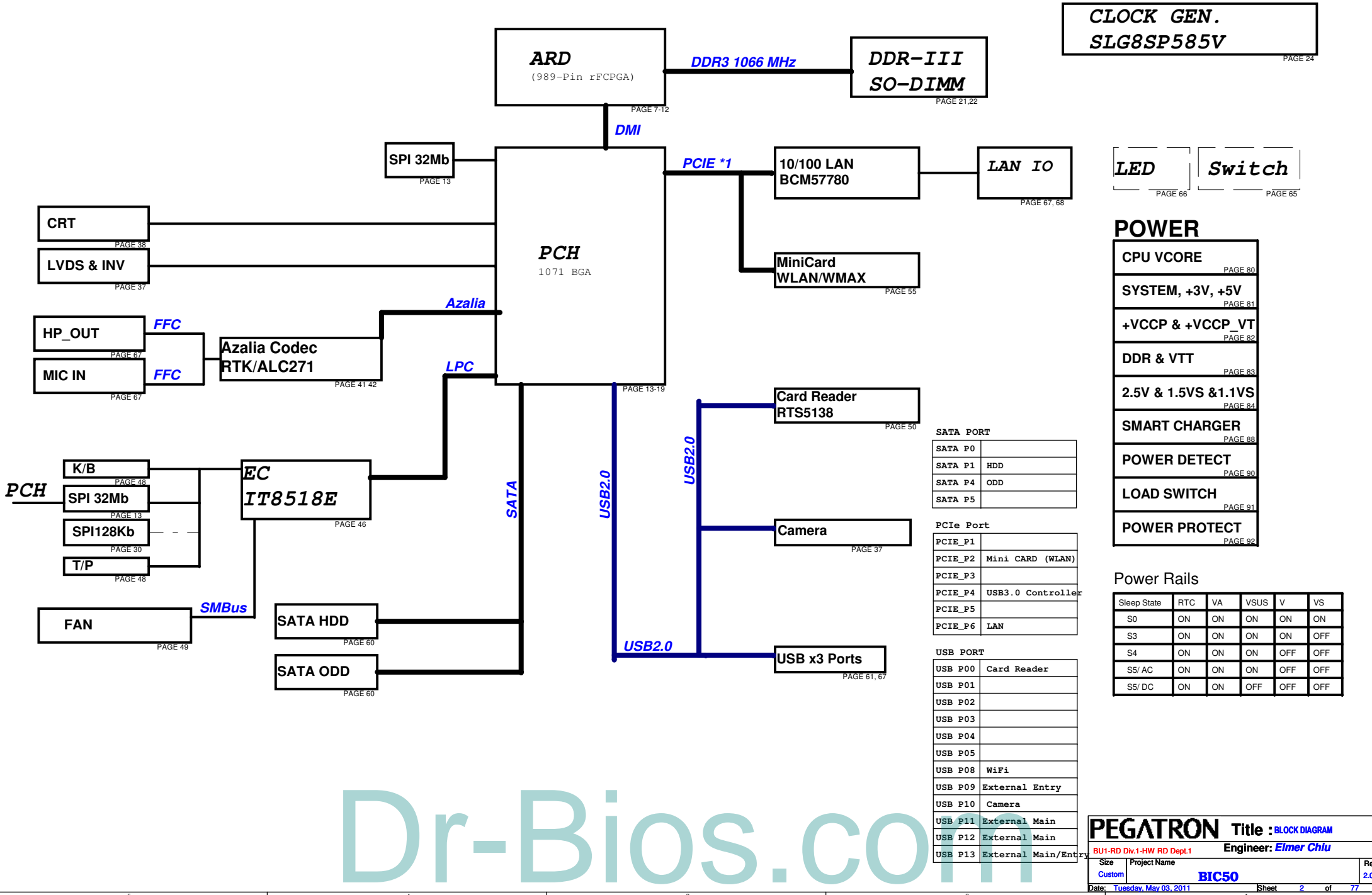
2011-0503

REV :R2.0

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<b>PEGATRON</b> Title : <i>Cover Page</i>		
BU1-RD Div.1-HW RD Dept.1 Engineer: <i>Elmer Chiu</i>		
Size Custom	Project Name <b>BIC50</b>	Rev 2.0
Date: <i>Wednesday, May 18, 2011</i>	Sheet 1 of 77	

# BA52\_CP BLOCK DIAGRAM



**CLOCK GEN.**  
**SLG8SP585V**

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**LED** (PAGE 66)      **Switch** (PAGE 65)

## POWER

- CPU VCORE** (PAGE 80)
- SYSTEM, +3V, +5V** (PAGE 81)
- +VCCP & +VCCP\_VT** (PAGE 82)
- DDR & VTT** (PAGE 83)
- 2.5V & 1.5VS & 1.1VS** (PAGE 84)
- SMART CHARGER** (PAGE 88)
- POWER DETECT** (PAGE 90)
- LOAD SWITCH** (PAGE 91)
- POWER PROTECT** (PAGE 92)

**SATA PORT**

SATA P0	
SATA P1	HDD
SATA P4	ODD
SATA P5	

**PCie Port**

PCIE_P1	
PCIE_P2	Mini CARD (WLAN)
PCIE_P3	
PCIE_P4	USB3.0 Controller
PCIE_P5	
PCIE_P6	LAN

**USB PORT**

USB P00	Card Reader
USB P01	
USB P02	
USB P03	
USB P04	
USB P05	
USB P08	WiFi
USB P09	External Entry
USB P10	Camera
USB P11	External Main
USB P12	External Main
USB P13	External Main/Entry

## Power Rails

Sleep State	RTC	VA	VSUS	V	VS
S0	ON	ON	ON	ON	ON
S3	ON	ON	ON	ON	OFF
S4	ON	ON	ON	OFF	OFF
S5/ AC	ON	ON	ON	OFF	OFF
S5/ DC	ON	ON	OFF	OFF	OFF

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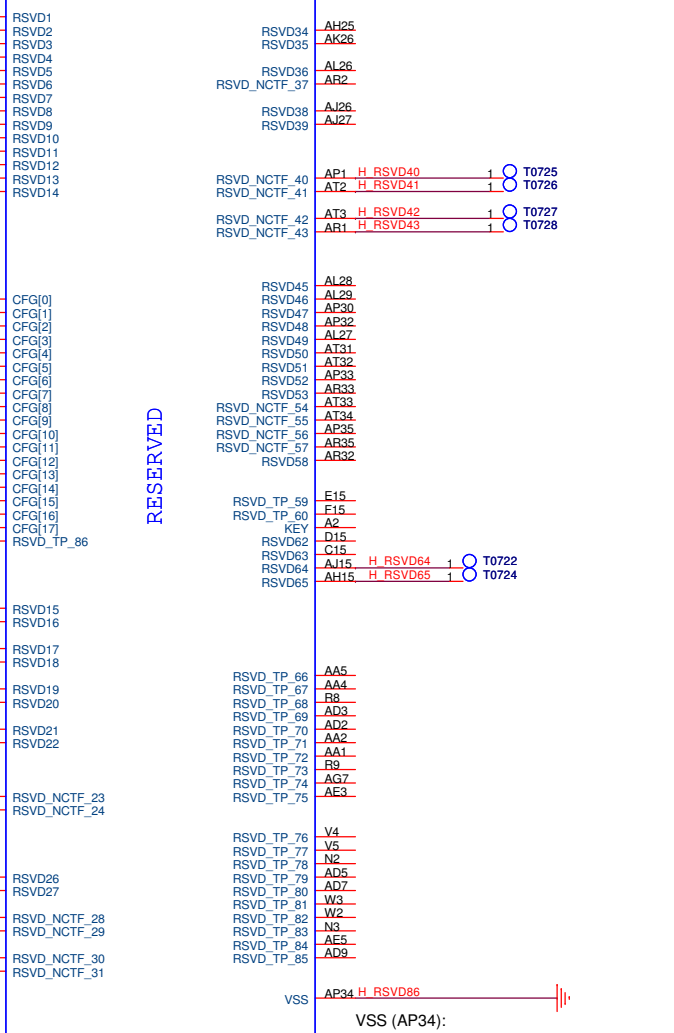
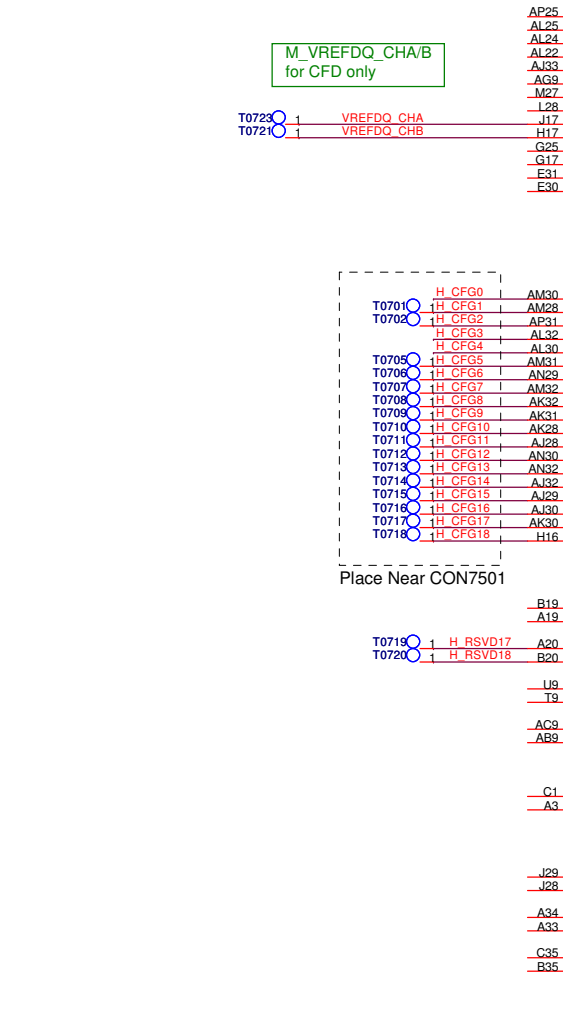
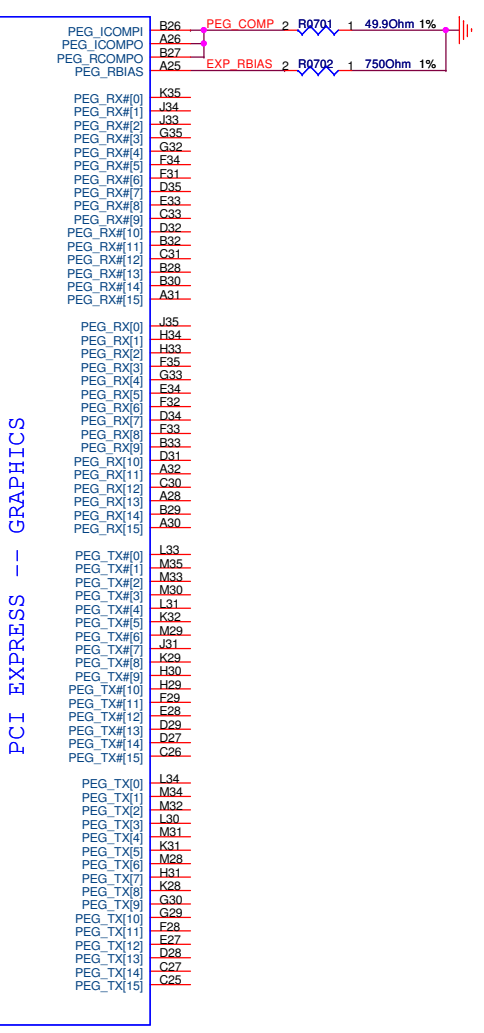
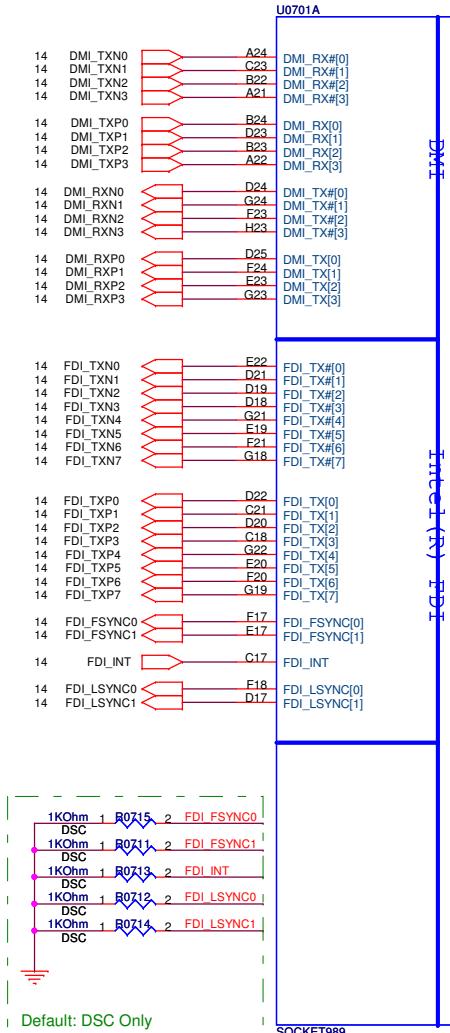
**PEGATRON** Title : BLOCK DIAGRAM  
 BU1-RD Div.1-HW RD Dept.1 Engineer: Elmer Chiu  
 Size Custom Project Name **BIC50** Rev 2.0  
 Date: Tuesday, May 03, 2011 Sheet 2 of 77

# SCHEMATIC INDEX V1.0

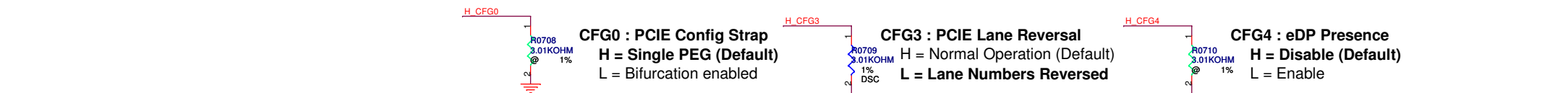
PAGE#	Description	NOTE
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02	Block Diagram	
03	PAGE INDEX	
04	Bus connection	
05	SMBus Diagram	
06	Power Rail	
07-10	CPU	
11-16	GMCH	
17-20	ICH	
21-23	DDR2/3 SO-DIMM	
24	Clock Generator	
25-33	Reserved	
34	Power Express/ SLI Logic	
35-36	Reserved VGA port	
37	LVDS CON	
38	RGB CON	
39	HDMI (Level shift for UMA)	
40	Dispaly port	
41-45	AUDIO CODEC & AMP & Jack	
46-48	EC ITE8512E / FLASH / KB / TP	
49	THERMAL / FAN	
50-52	CARD READER / 1394	
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54	PCI-Express Card	
55	MINI CARD -WUSB /UPCONVERT	
56	MINI CARD -WWAN	
57	MINI CARD -WiFi/WMAX	
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60	SATA(HDD & CD_ROM)	
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63-64	DC-IN / Discharge / NVM	Reserved
65-66	CIR, LID, MDC, SW, LED, Power BTN, Debug	Other int CONNS
67-68	LAN / RJ45 / RJ11	

PAGE#	Description	NOTE
69	3D sensor	
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72	SCREW PAD	
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76	Port Docking	
77	DC-IN & BAT connector and discharge	
78	Power Sequence Logic	
79	POWER LOAD SWITCH	
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101-	Daughter Board Combined Solutions	

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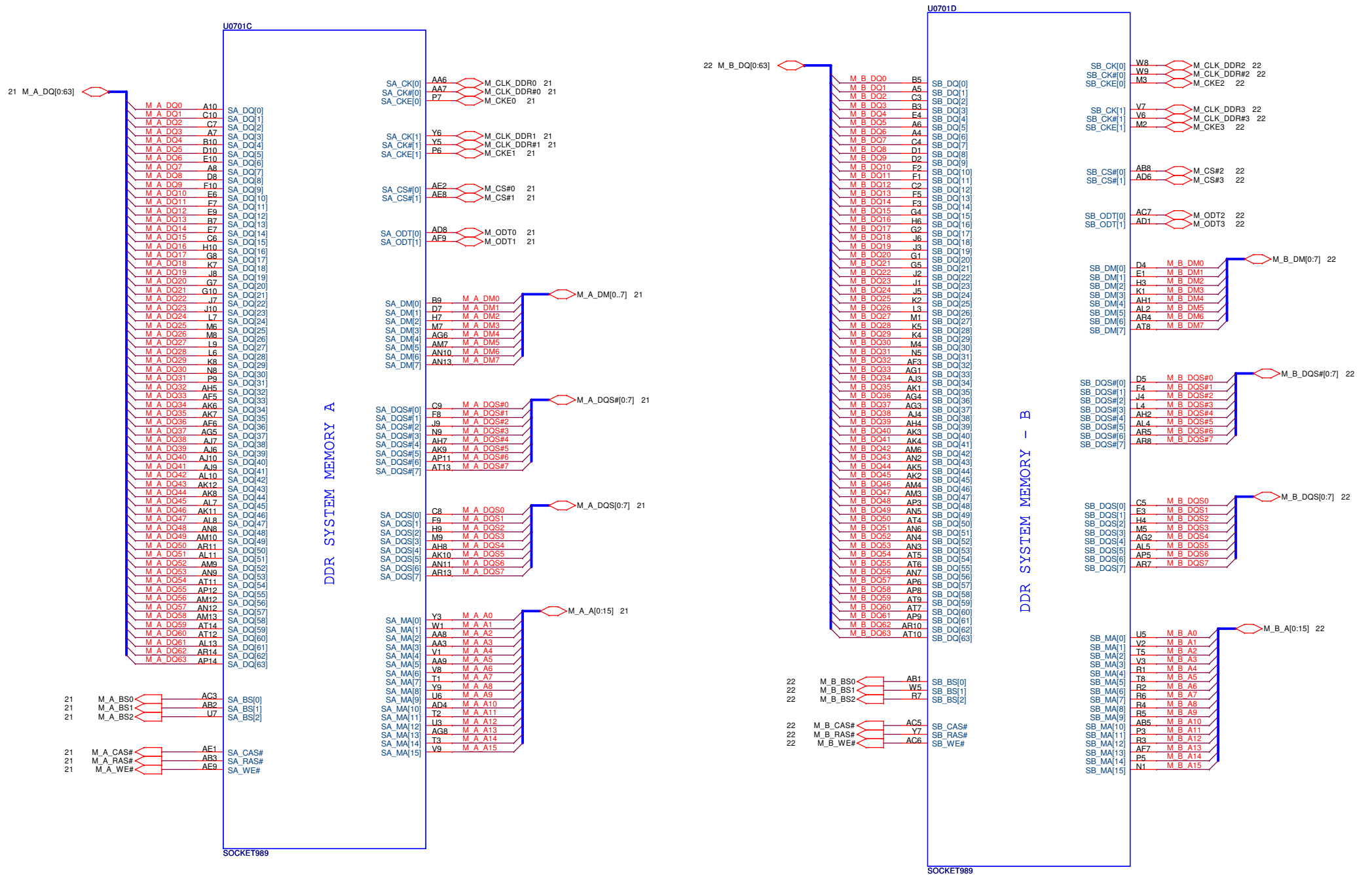


Default: DSC Only  
 DSC only: Pop all resistors  
 UMA only: Depop all resistors

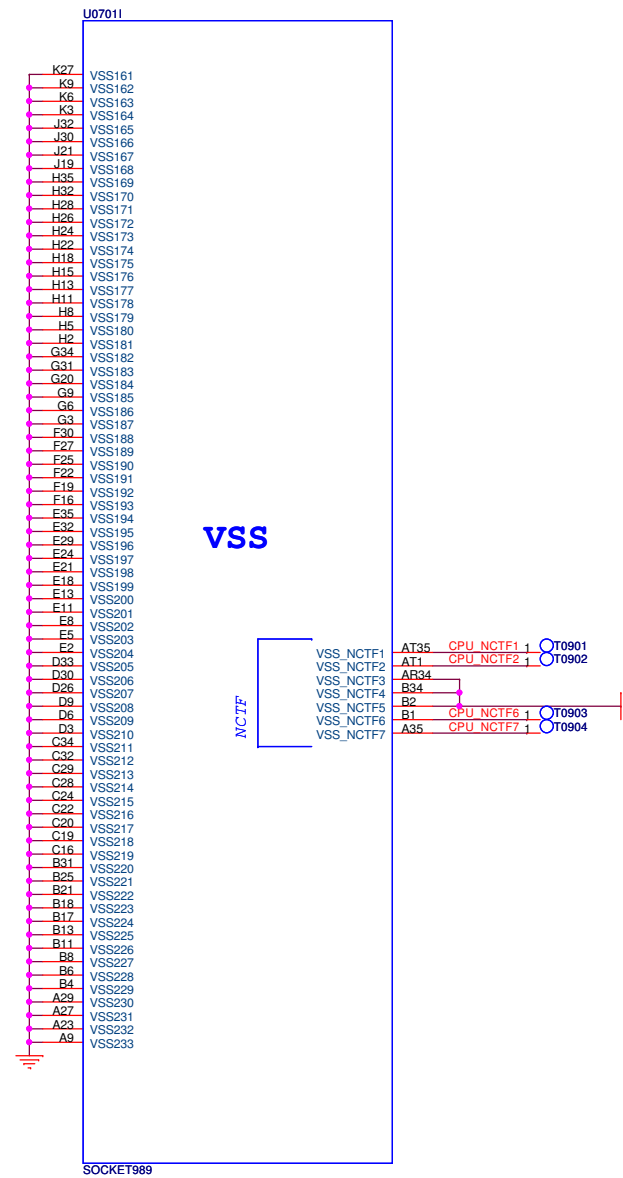
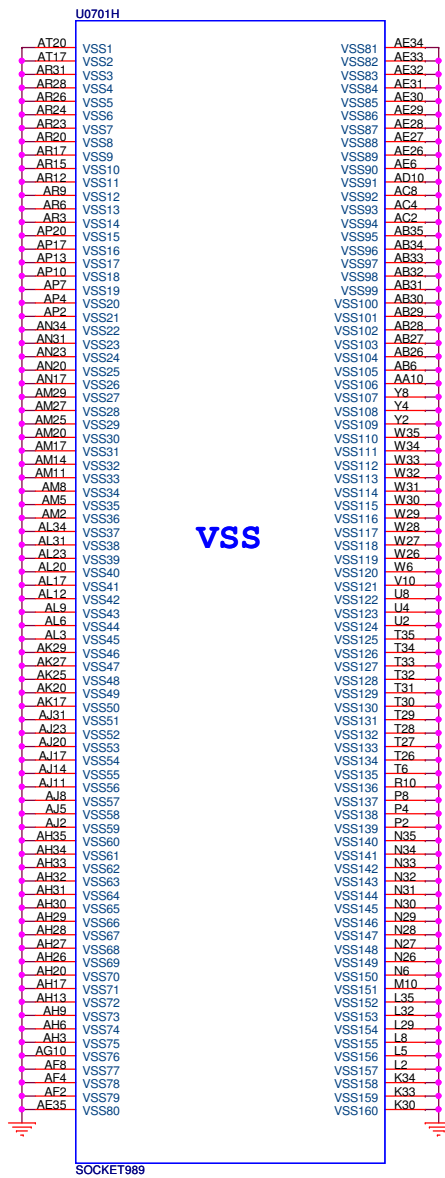


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**PEGATRON** Title : CPU(1)  
 BU-1-RD Div.1-HW RD Dept.1 Engineer: Elmer Chiu  
 Size Project Name  
 Custom Project Name **BIC50**  
 Date: Tuesday, May 03, 2011 Sheet 7 of 77  
 Rev 2.0



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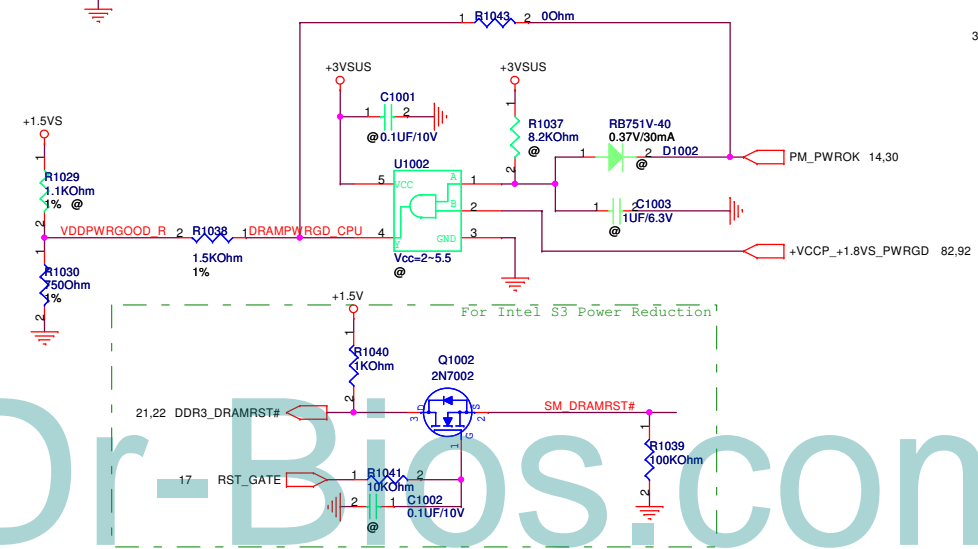
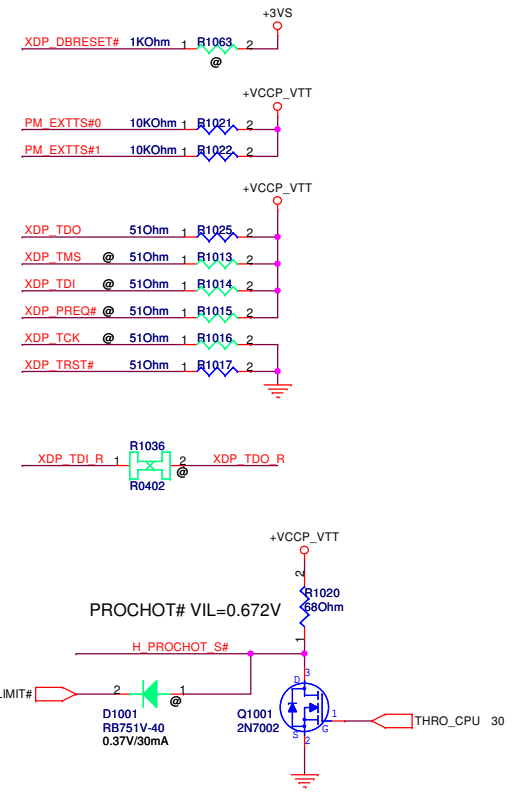
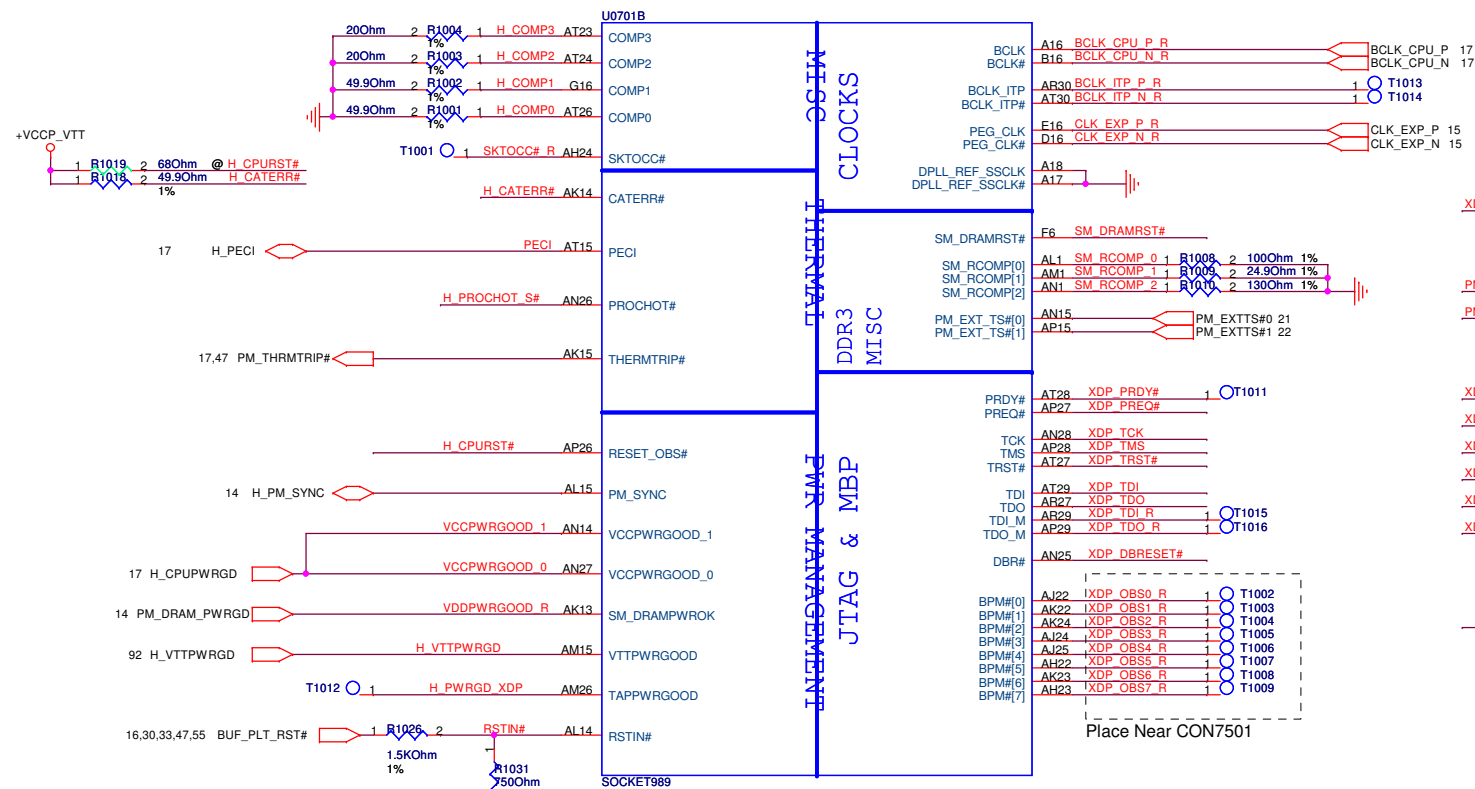
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**PEGATRON** Title : CPU GND

BU1-RD Div.1-HW RD Dept.1 Engineer: Elmer Chiu

Size	Project Name	Rev
Custom	BIC50	2.0

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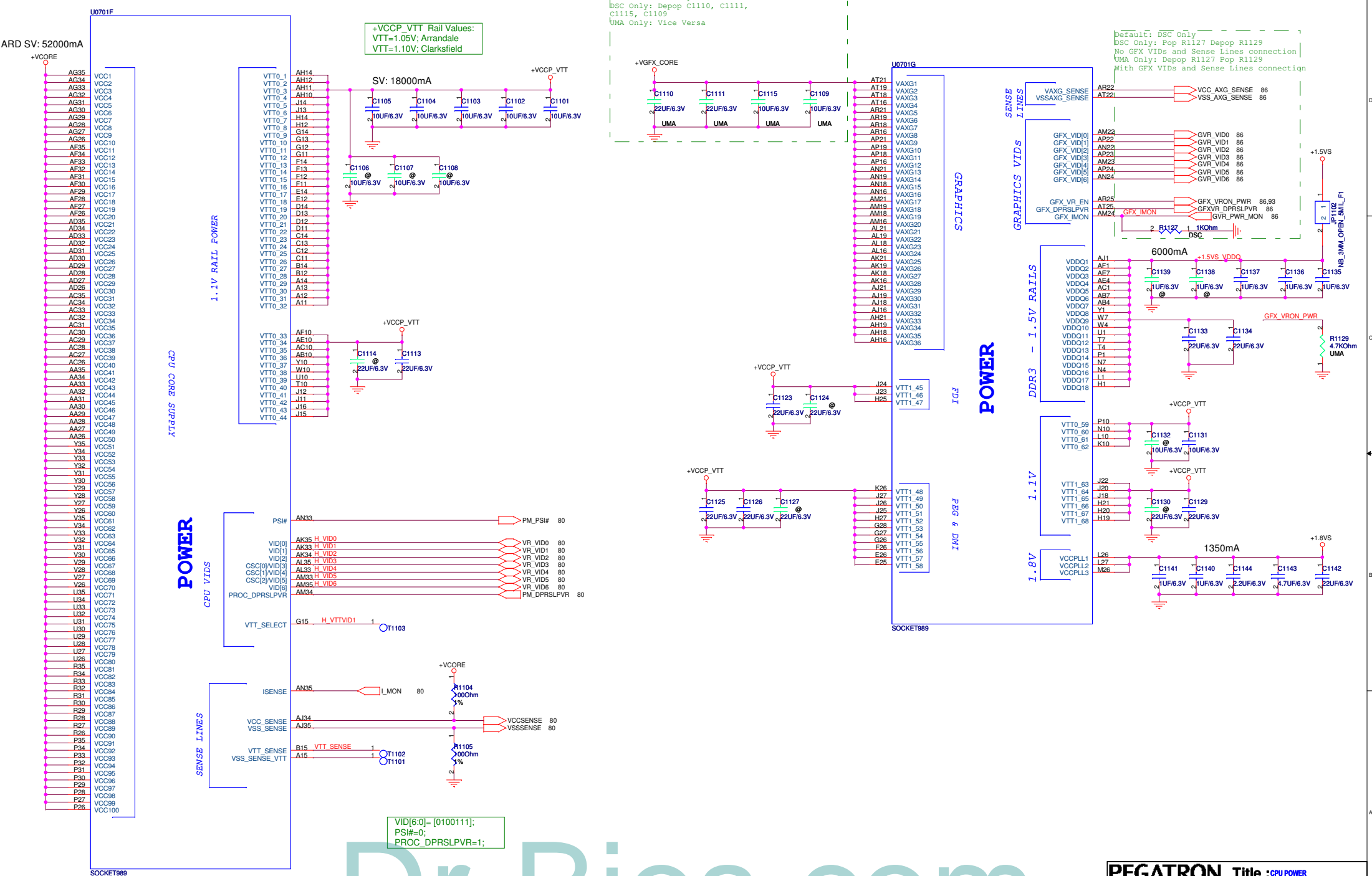
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Default: D5C Only  
 D5C Only: Depop C1110, C1111, C1115, C1109  
 UMA Only: Vice Versa

Default: D5C Only  
 D5C Only: Pop R1127 Depop R1129  
 No GFX VID's and Sense Lines connection  
 UMA Only: Depop R1127 Pop R1129  
 With GFX VID's and Sense Lines connection

+VCCP\_VTT Rail Values:  
 VTT=1.05V; Arrandale  
 VTT=1.10V; Clarksfield

VID[6:0] = [0100111];  
 PS#=#0;  
 PROC\_DPRSPLPVR=1;



ARD SV: 52000mA

SOCKET989

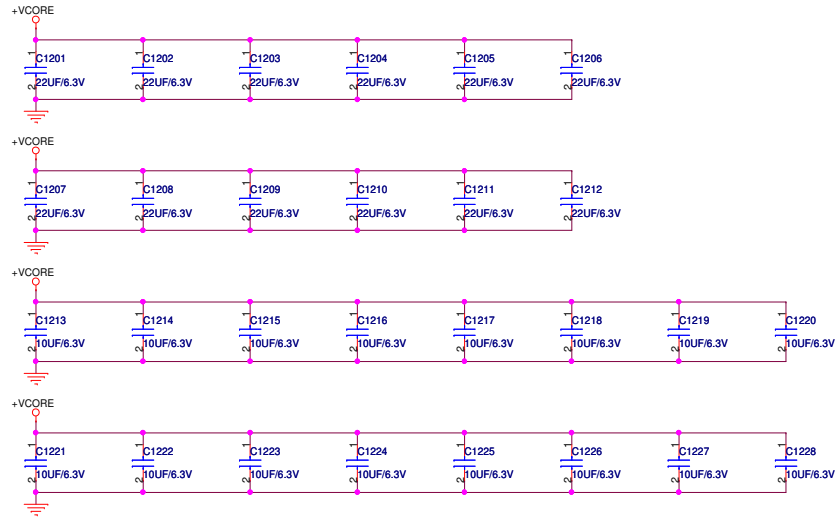
SOCKET989





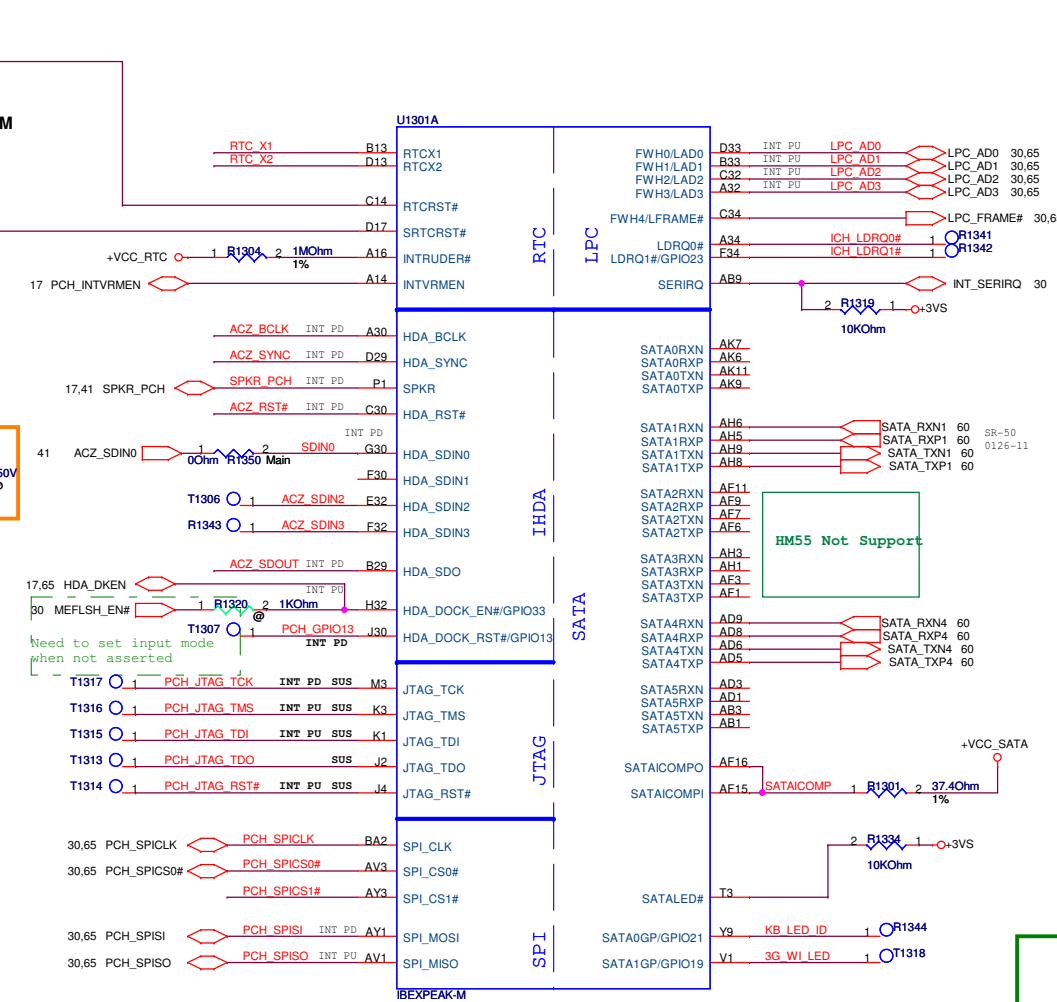
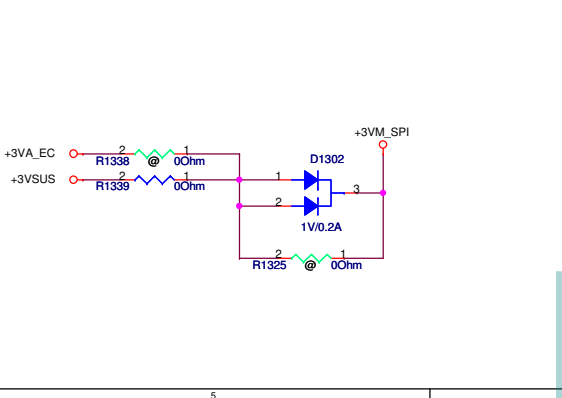
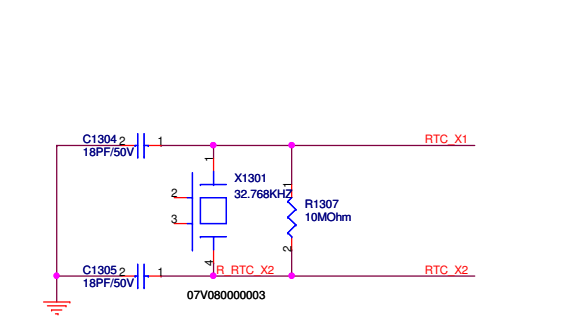
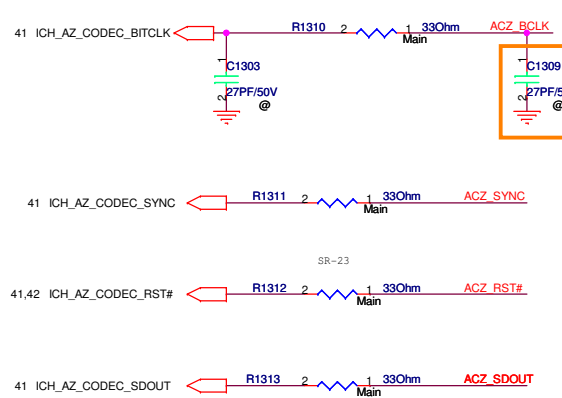
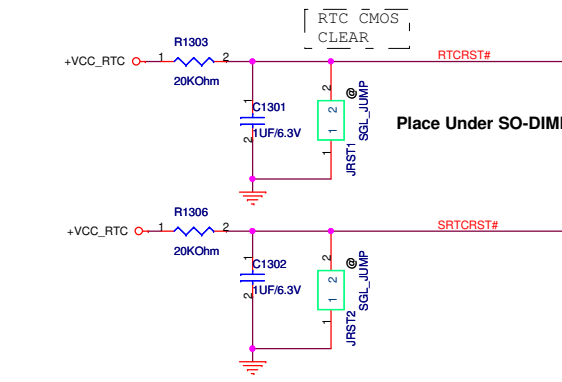
Decoupling guide from INTEL

VCORE 10uF x 16pcs  
22uF x 12pcs



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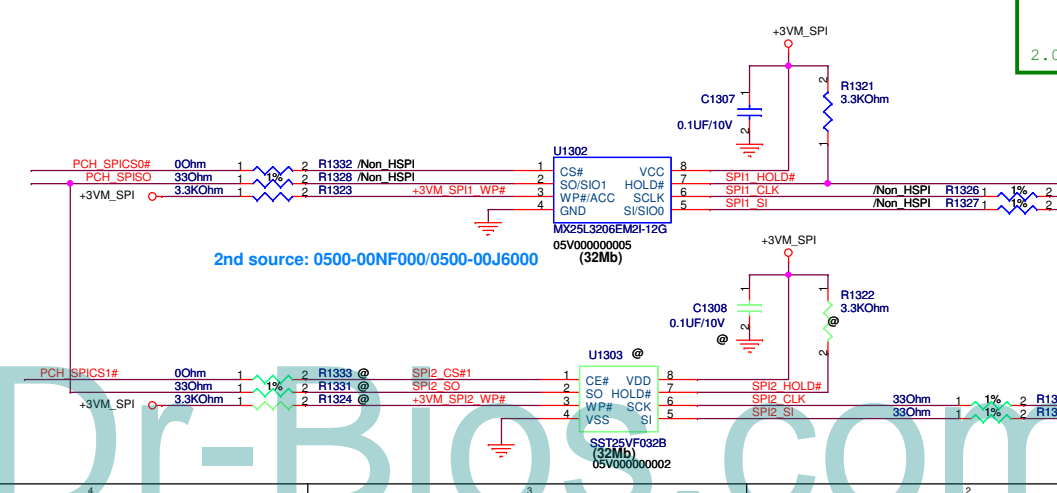
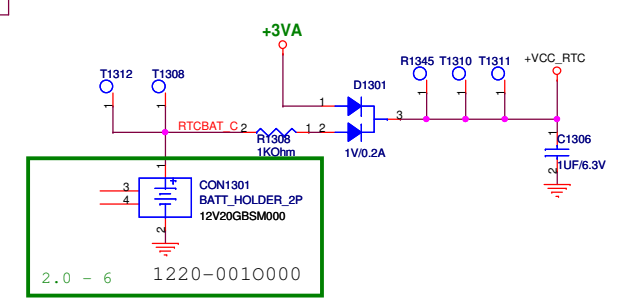
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BU1-RD Div.1-HW RD Dept.1	
Engineer:	
Size	Project Name
Custom	<b>BIC50</b>
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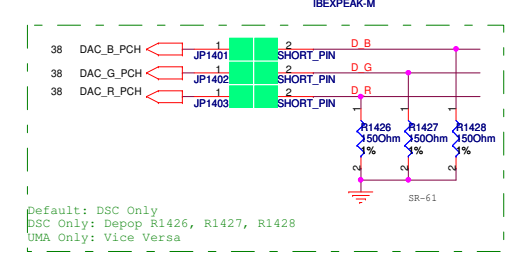
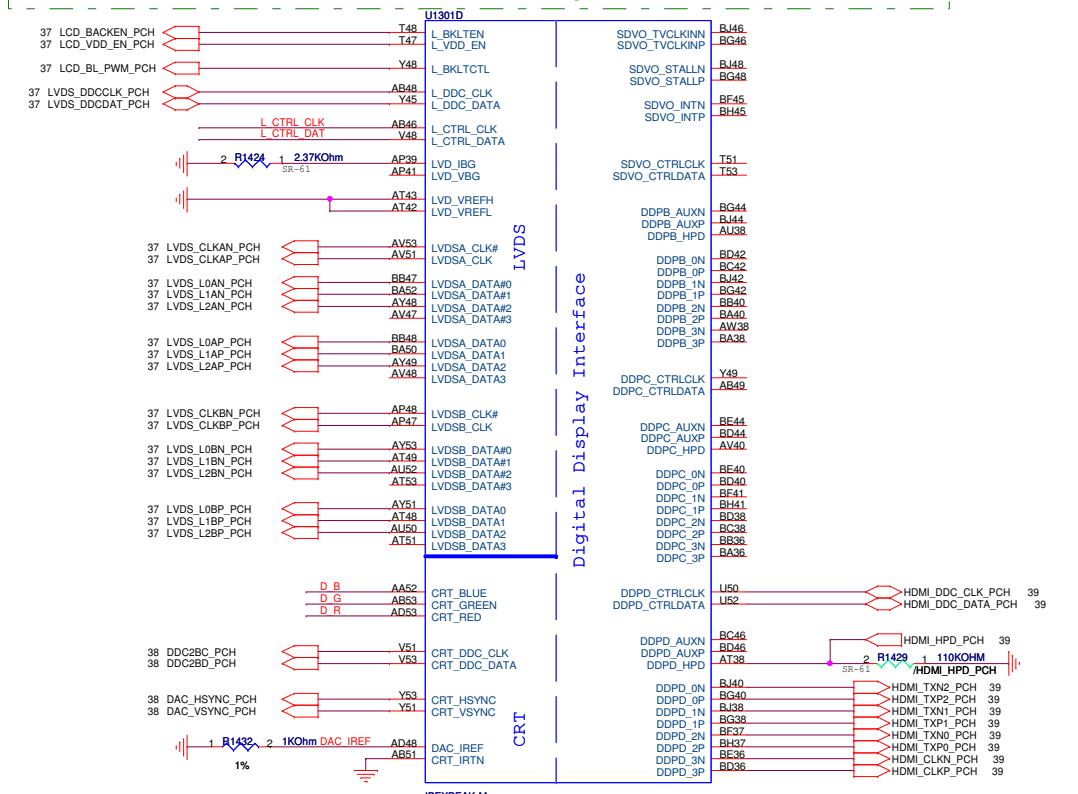
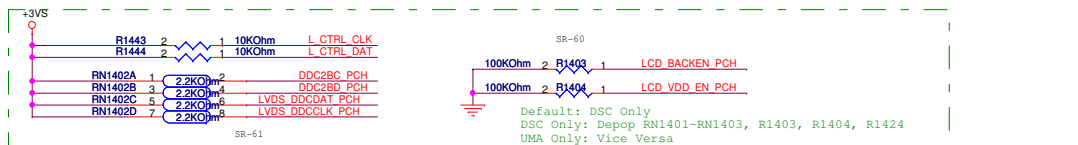
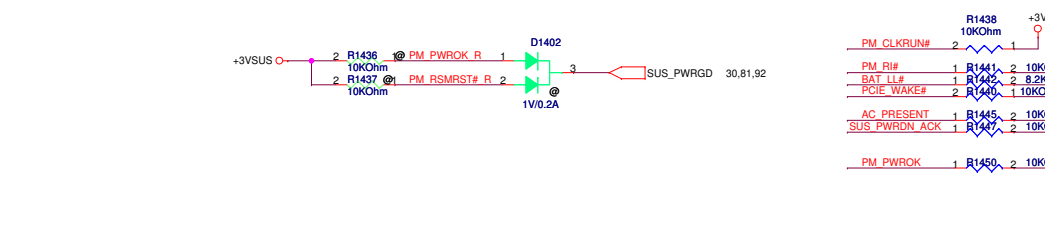
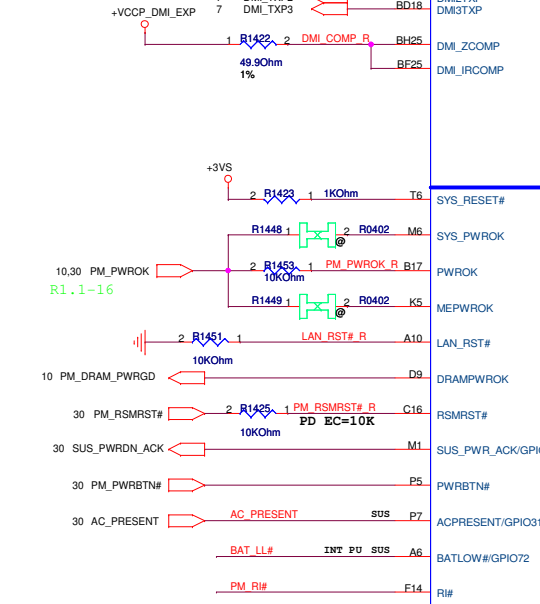
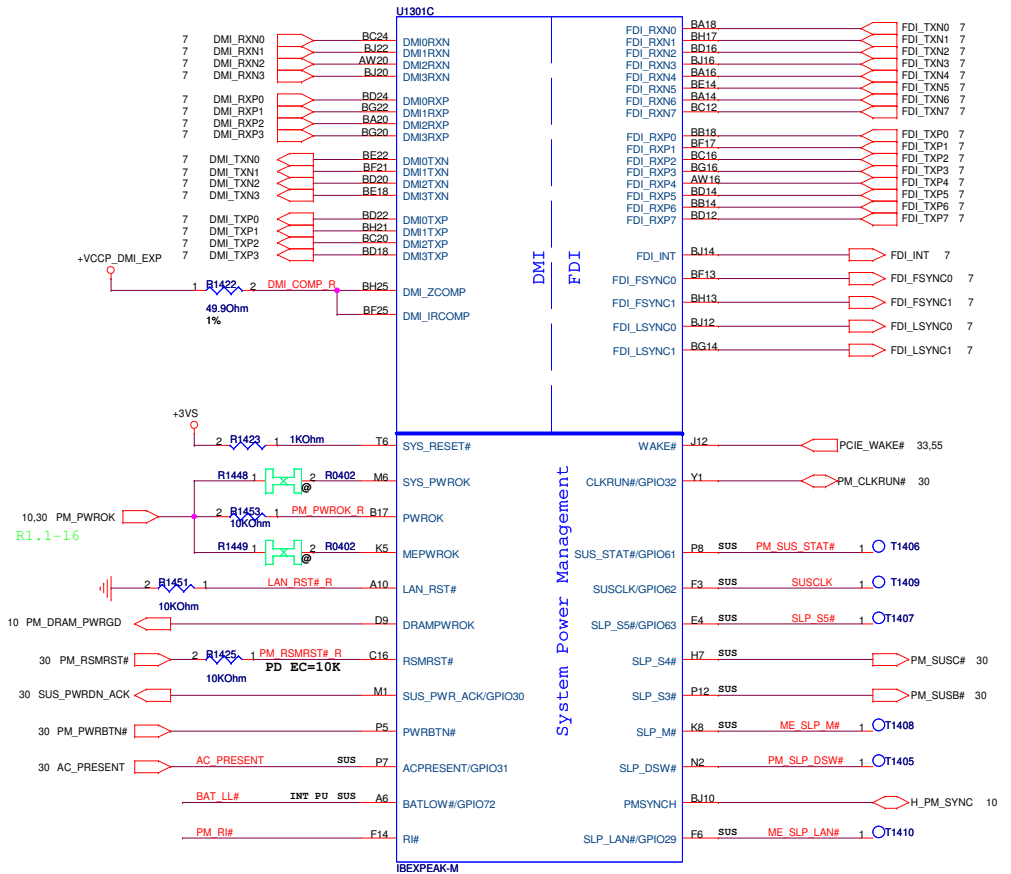


**SATA PORT**

SATA P0	
SATA P1	HDD
SATA P4	ODD
SATA P5	eSATA Removed

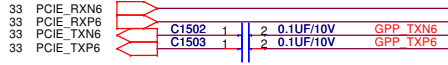
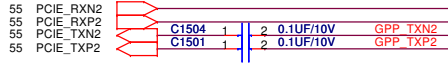
**RTC BAT**



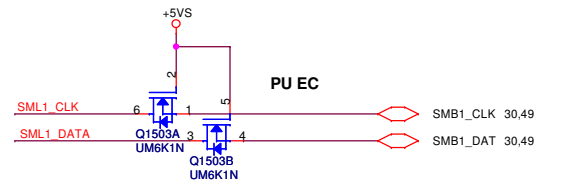
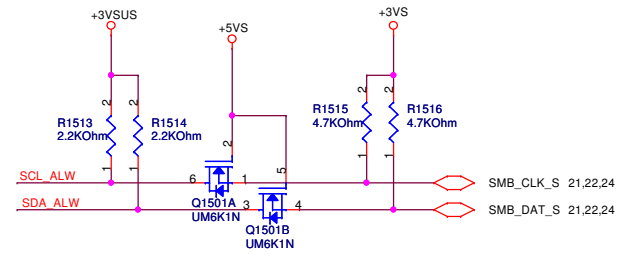
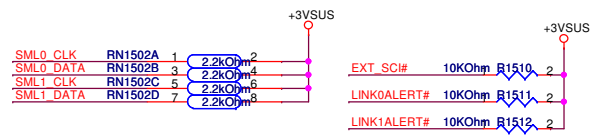
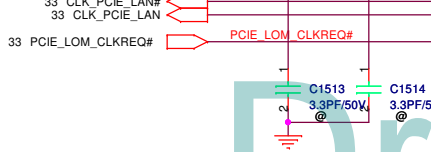
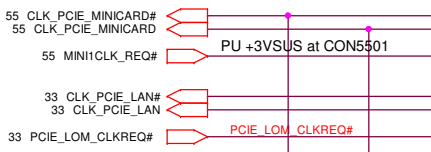
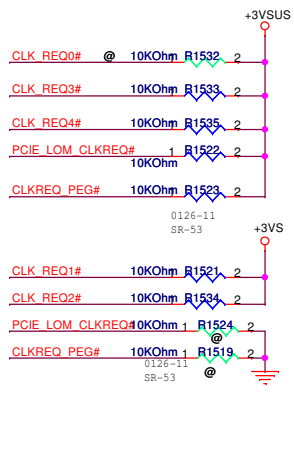


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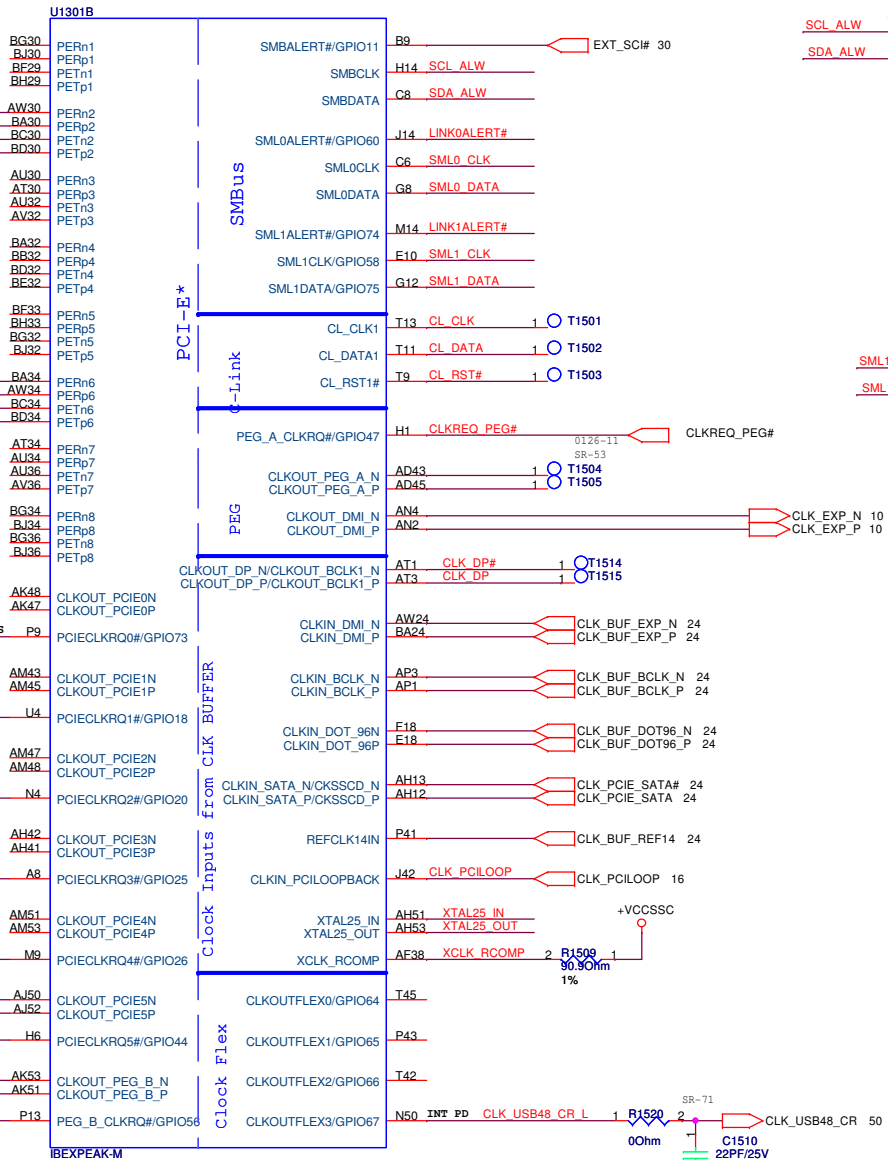
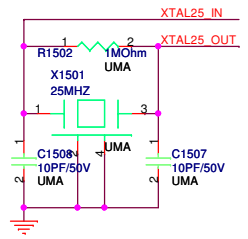
PCIE 1	
PCIE 2	Mini CARD (WLAN)
PCIE 3	
PCIE 4	
PCIE 5	
PCIE 6	LAN

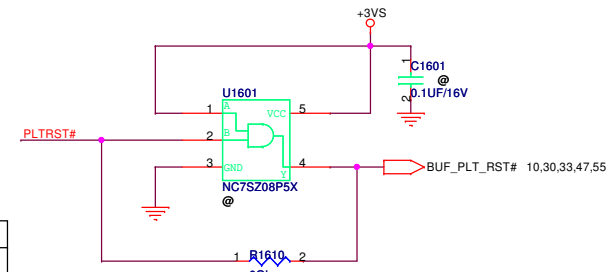
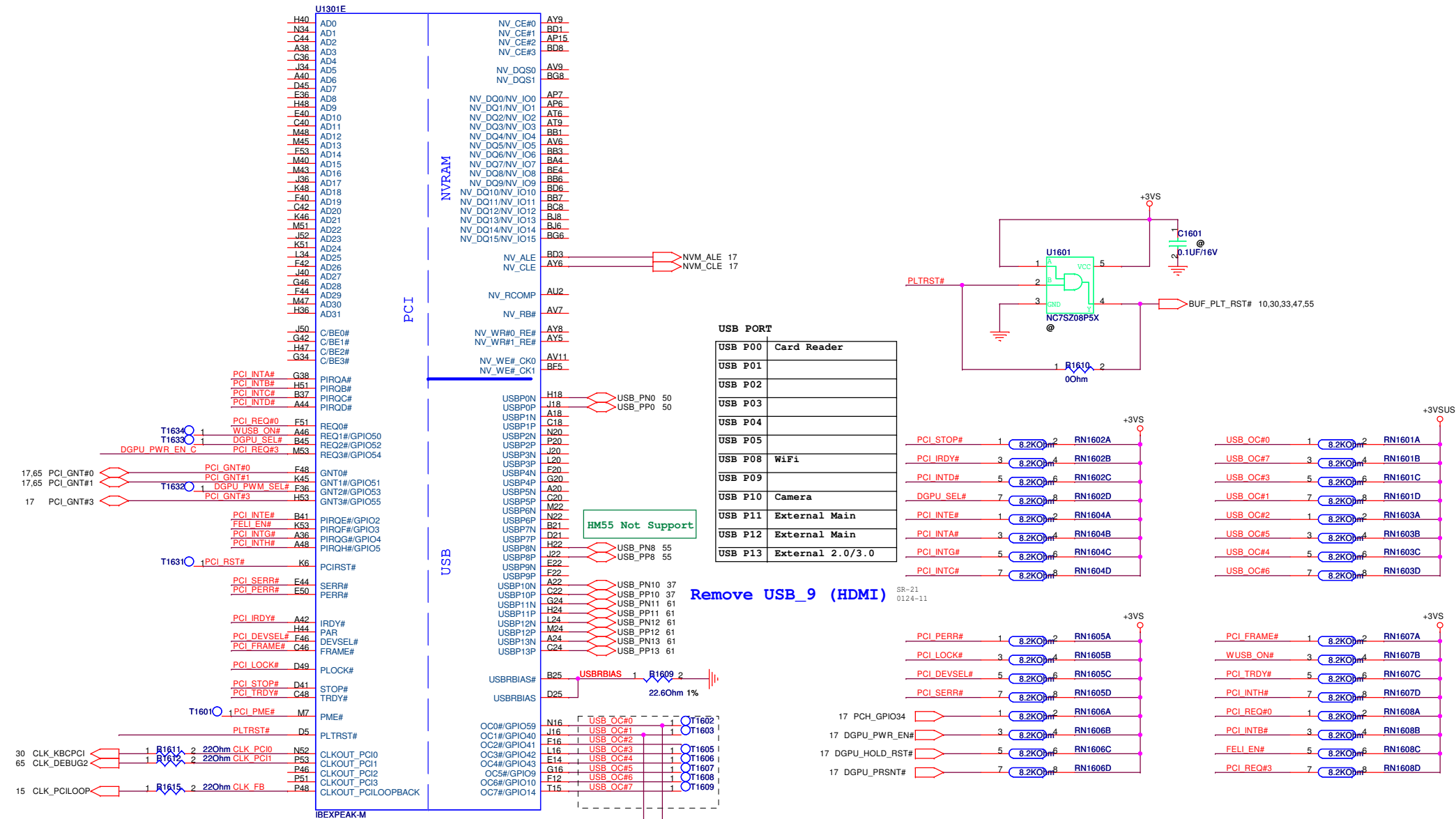


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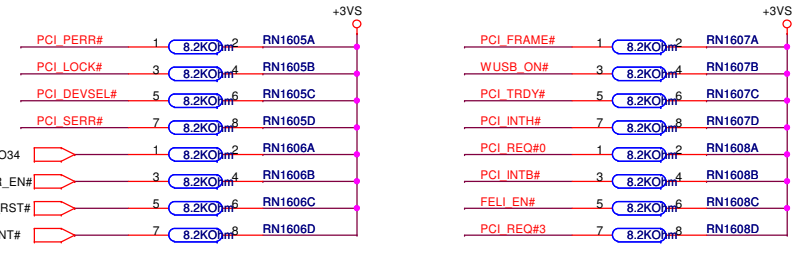
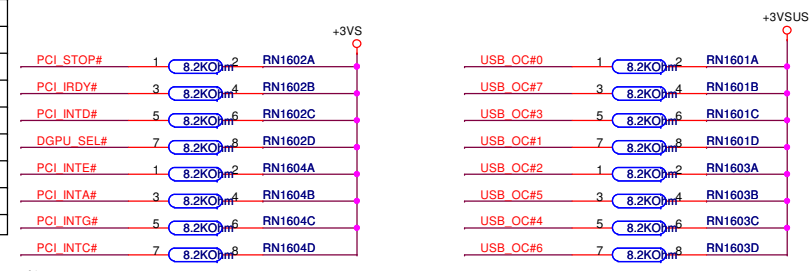


Damping CPU Side

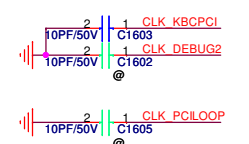
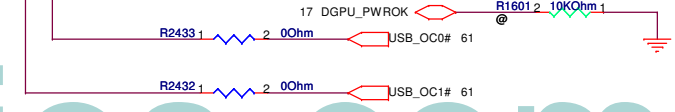
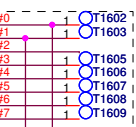




USB PORT	Function
USB P00	Card Reader
USB P01	
USB P02	
USB P03	
USB P04	
USB P05	
USB P08	WiFi
USB P10	Camera
USB P11	External Main
USB P12	External Main
USB P13	External 2.0/3.0

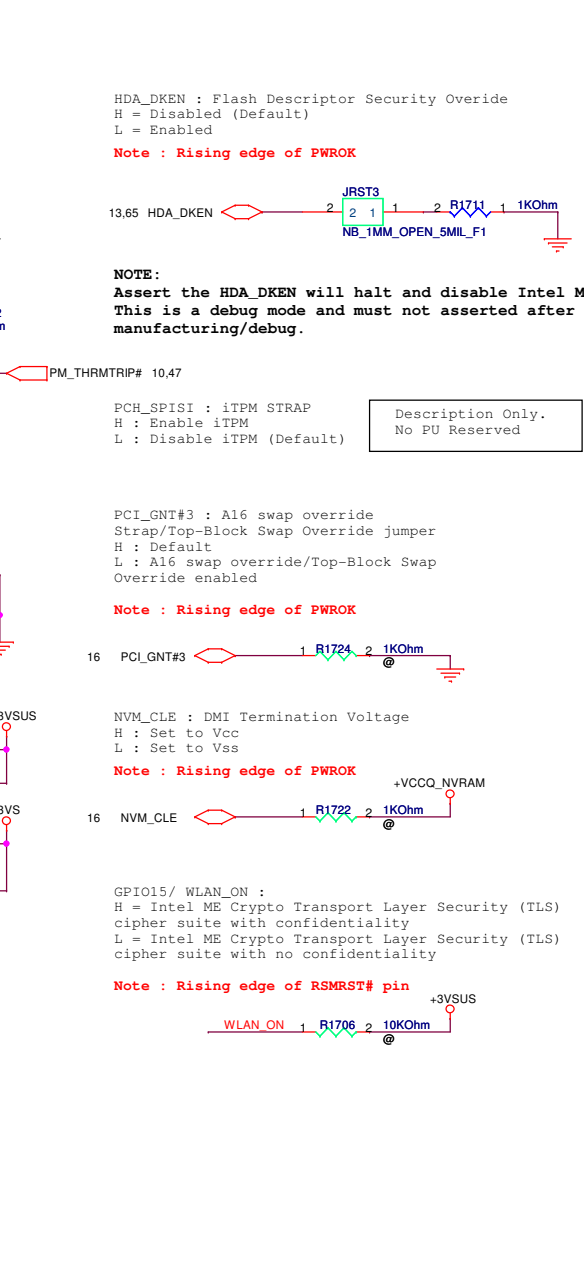
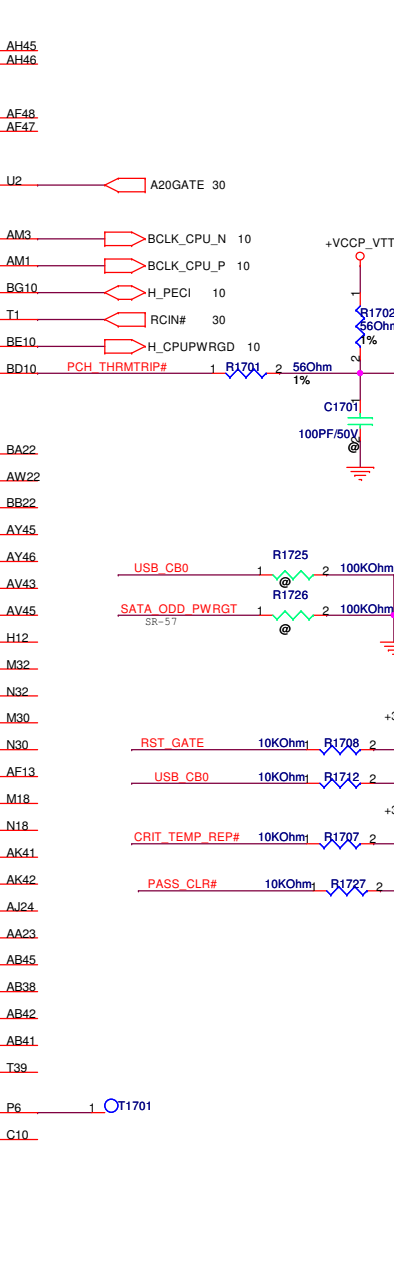
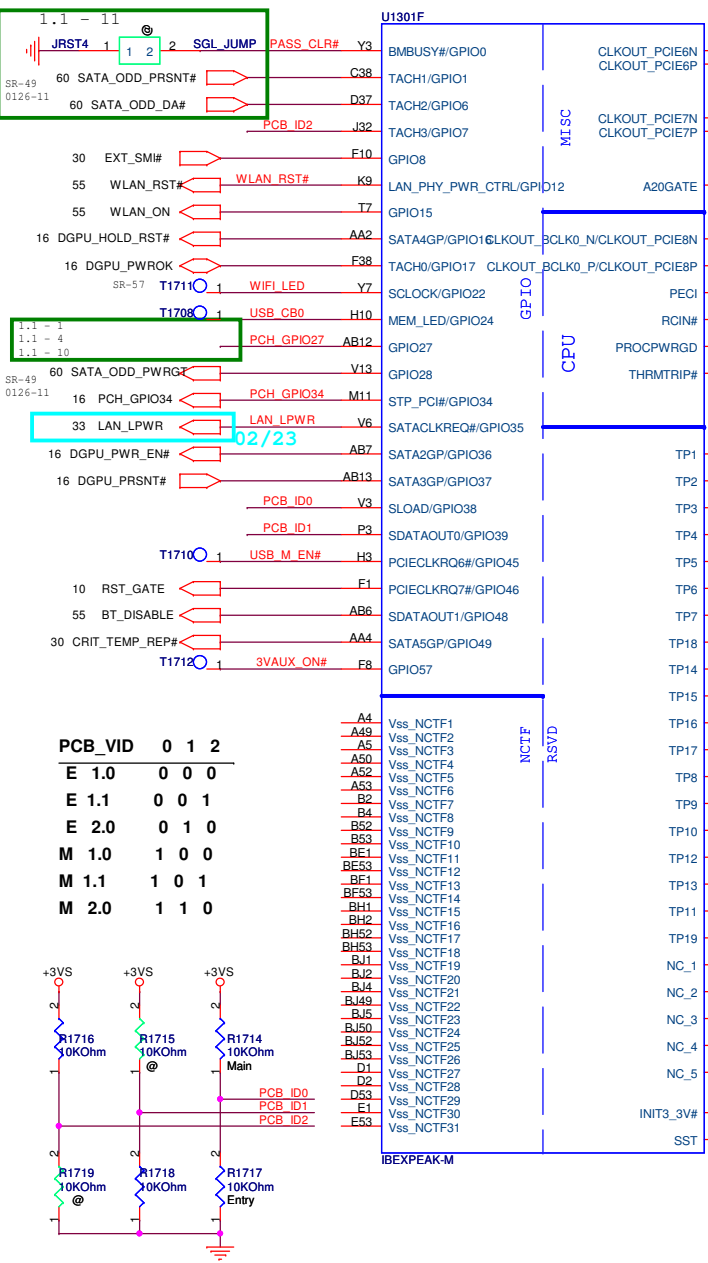


Remove USB\_9 (HDMI) SR-21 0124-11



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change USB power switch circuit



HDA\_DKEN : Flash Descriptor Security Override  
 H = Disabled (Default)  
 L = Enabled  
**Note : Rising edge of PWROK**

**NOTE:**  
 Assert the HDA\_DKEN will halt and disable Intel ME.  
 This is a debug mode and must not asserted after manufacturing/debug.

PCB\_SPI1 : iTPM STRAP  
 H : Enable iTPM  
 L : Disable iTPM (Default)

PCI\_GNT#3 : A16 swap override  
 Strap/Top-Block Swap Override jumper  
 H : Default  
 L : A16 swap override/Top-Block Swap Override enabled

16 PCL\_GNT#3 : 1KOhm

NVM\_CLE : DMI Termination Voltage  
 H : Set to Vcc  
 L : Set to Vss

16 NVM\_CLE : 1KOhm

GPIO15/ WLAN\_ON :  
 H = Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality  
 L = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality

**Note : Rising edge of RSMRST# pin**

PCH\_INTVRMEN : Integrated SUS 1.05V VRM Enable  
 H : Integrated VRM is enabled  
 L : Integrated VRM is disabled  
**Note : This signal should always be pulled high**

SPKR\_PCH : NO REBOOT STRAP  
 H : Enable  
 L : Disable (Default)  
**Note : Rising edge of PWROK**

PCI\_GNT#1, PCI\_GNT#0 : Boot BIOS Strap

PCI_GNT#0	PCI_GNT#1	
0	0	LPC
0	1	PCI
1	1	SPI

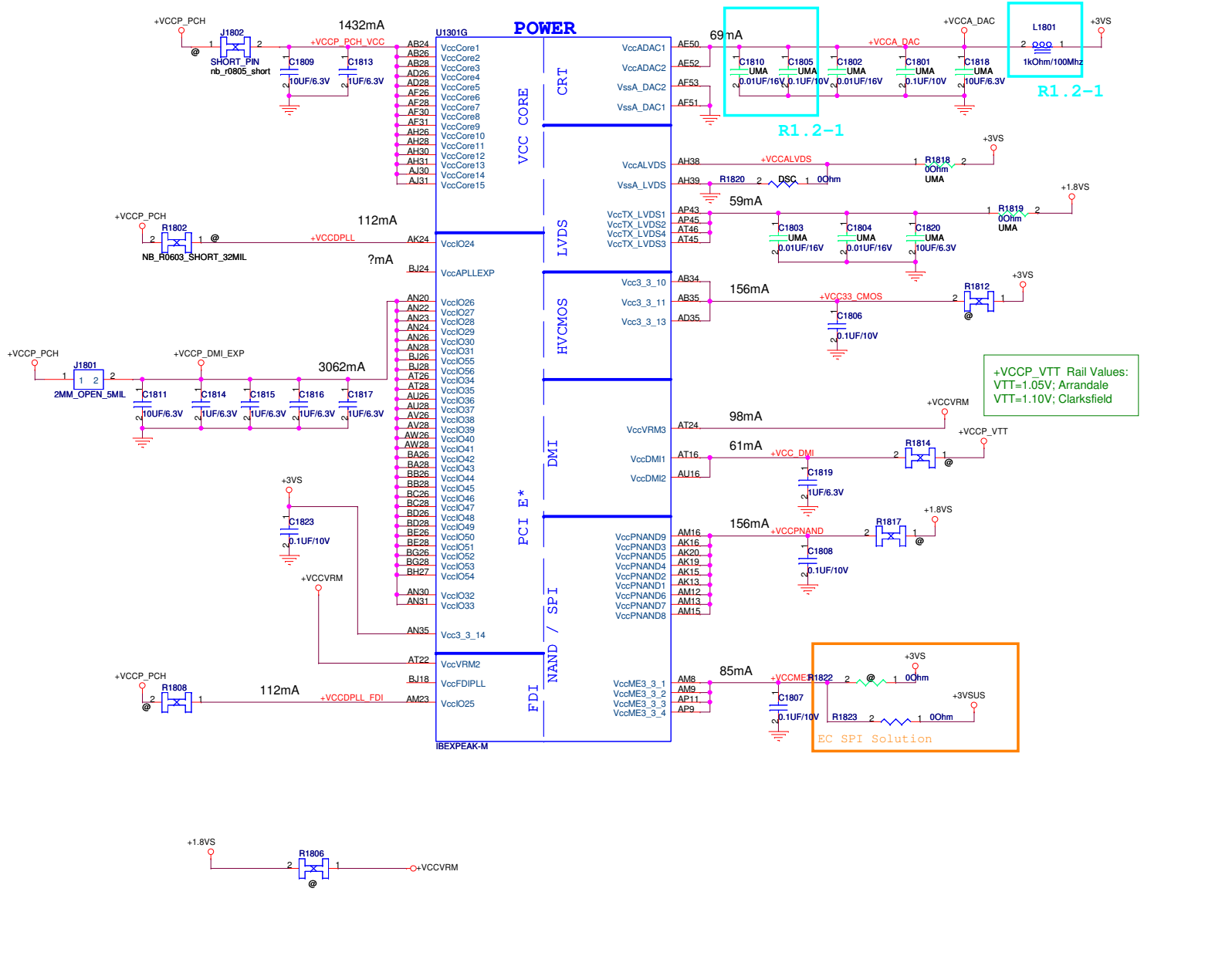
**Note : Rising edge of PWROK**

NVM\_ALE : Danbury Technology Enabled  
 High--> Enable Intel Anti-Theft Technology.  
 Low--> Disable Intel Anti-Theft Technology.  
**Note : Rising edge of PWROK**

GPIO27/ USB\_SW :  
 H = Enables the internal VccVRM. (Default)  
 L = Disables the VccVRM.  
**Note : Rising edge of RSMRST# pin**

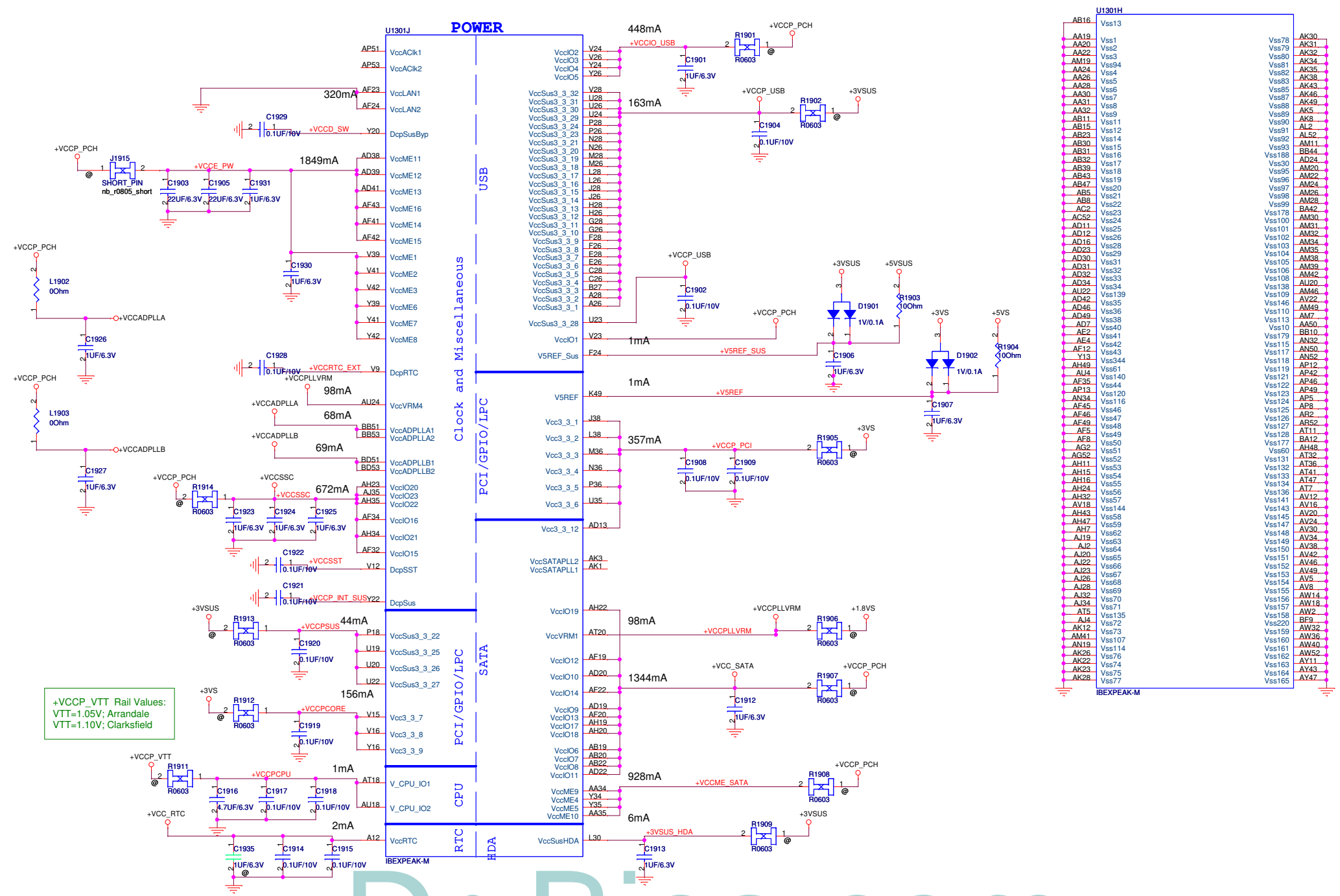


Default: DSC Only  
 DSC Only: Depop R1818, R1819, C1802, C1801, C1818  
 C1803, C1804, C1820  
 Pop R1820, and C1803 change to 0ohm  
 UMA Only: Vice Versa



U1301I			
AY7	Vss166	Vss270	H49
B11	Vss167	Vss271	H5
B15	Vss168	Vss272	J24
B19	Vss169	Vss273	K1
B23	Vss170	Vss274	K43
B31	Vss171	Vss275	K47
B35	Vss172	Vss276	K7
B39	Vss173	Vss277	L14
B43	Vss174	Vss278	L18
B47	Vss175	Vss279	L2
B7	Vss176	Vss280	L22
BG12	Vss177	Vss281	L32
BB12	Vss180	Vss282	L36
BB16	Vss181	Vss283	L40
BB20	Vss182	Vss284	L52
BB24	Vss183	Vss285	M12
BB30	Vss184	Vss286	M16
BB34	Vss185	Vss287	M20
BB38	Vss186	Vss288	M36
BB42	Vss187	Vss289	M38
BB49	Vss189	Vss290	M42
BB5	Vss190	Vss291	M46
BC10	Vss191	Vss292	M49
BC14	Vss192	Vss293	M49
BC18	Vss193	Vss294	M8
BC22	Vss194	Vss295	M8
BC26	Vss195	Vss296	M24
BC32	Vss196	Vss297	P11
BC36	Vss197	Vss298	P22
BC40	Vss198	Vss299	P30
BC44	Vss199	Vss300	P32
BC52	Vss200	Vss302	P34
BH9	Vss202	Vss303	P42
BD48	Vss201	Vss305	P45
BD5	Vss202	Vss306	P47
BE12	Vss203	Vss307	P47
BE16	Vss204	Vss309	R2
BE24	Vss205	Vss310	R52
BE28	Vss206	Vss311	T12
BE30	Vss207	Vss312	T4
BE34	Vss208	Vss314	T46
BE38	Vss209	Vss315	T49
BE42	Vss210	Vss316	T5
BE46	Vss211	Vss317	T5
BE48	Vss212	Vss318	L80
BE50	Vss213	Vss319	U31
BE6	Vss214	Vss320	U32
BF6	Vss215	Vss321	U34
BF8	Vss216	Vss322	P38
BF3	Vss217	Vss323	V19
BF49	Vss218	Vss324	P16
BF51	Vss219	Vss325	V19
BG18	Vss222	Vss326	V20
BG24	Vss223	Vss327	V22
BG4	Vss224	Vss328	V30
BG50	Vss225	Vss329	V31
BH11	Vss226	Vss328	V32
BH15	Vss227	Vss329	V34
BH19	Vss228	Vss330	V35
BH23	Vss229	Vss330	V38
BH31	Vss229	Vss331	V43
BH35	Vss230	Vss332	V43
BH39	Vss231	Vss333	V46
BH43	Vss232	Vss334	V47
BH47	Vss233	Vss335	V49
BH7	Vss234	Vss336	V5
C12	Vss235	Vss337	V5
C12	Vss237	Vss338	V7
C50	Vss238	Vss339	V8
D51	Vss239	Vss340	W2
E16	Vss240	Vss341	W2
E12	Vss241	Vss342	W52
E20	Vss242	Vss343	Y11
E24	Vss243	Vss344	Y12
E30	Vss244	Vss345	Y15
E34	Vss245	Vss346	Y19
E38	Vss246	Vss347	Y23
E42	Vss247	Vss348	Y28
E46	Vss248	Vss349	Y30
E48	Vss249	Vss350	Y31
E8	Vss250	Vss351	Y32
E8	Vss251	Vss352	Y36
F49	Vss252	Vss353	Y43
F5	Vss253	Vss354	Y46
G10	Vss254	Vss355	P49
G14	Vss255	Vss356	Y5
G18	Vss256	Vss357	Y6
G2	Vss257	Vss358	Y8
G2	Vss258	Vss359	Y8
G32	Vss259	Vss360	P24
G36	Vss260	Vss361	T43
G40	Vss261	Vss362	AD51
G44	Vss262	Vss363	AT8
G52	Vss263	Vss364	AD47
AF39	Vss264	Vss365	Y47
H16	Vss265	Vss366	AT12
H20	Vss266	Vss367	AM6
H30	Vss267	Vss368	AT13
H34	Vss268	Vss369	AM5
H38	Vss269	Vss370	AK45
H42	Vss270	Vss371	AK39
	Vss271	Vss372	AV14
	Vss272	Vss373	
	Vss273	Vss374	
	Vss274	Vss375	
	Vss275	Vss376	
	Vss276	Vss377	
	Vss277	Vss378	
	Vss278	Vss379	
	Vss279	Vss380	
	Vss280	Vss381	
	Vss281	Vss382	
	Vss282	Vss383	
	Vss283	Vss384	
	Vss284	Vss385	
	Vss285	Vss386	
	Vss286	Vss387	
	Vss287	Vss388	
	Vss288	Vss389	
	Vss289	Vss390	
	Vss290	Vss391	
	Vss291	Vss392	
	Vss292	Vss393	
	Vss293	Vss394	
	Vss294	Vss395	
	Vss295	Vss396	
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	Vss297	Vss398	
	Vss298	Vss399	
	Vss299	Vss400	

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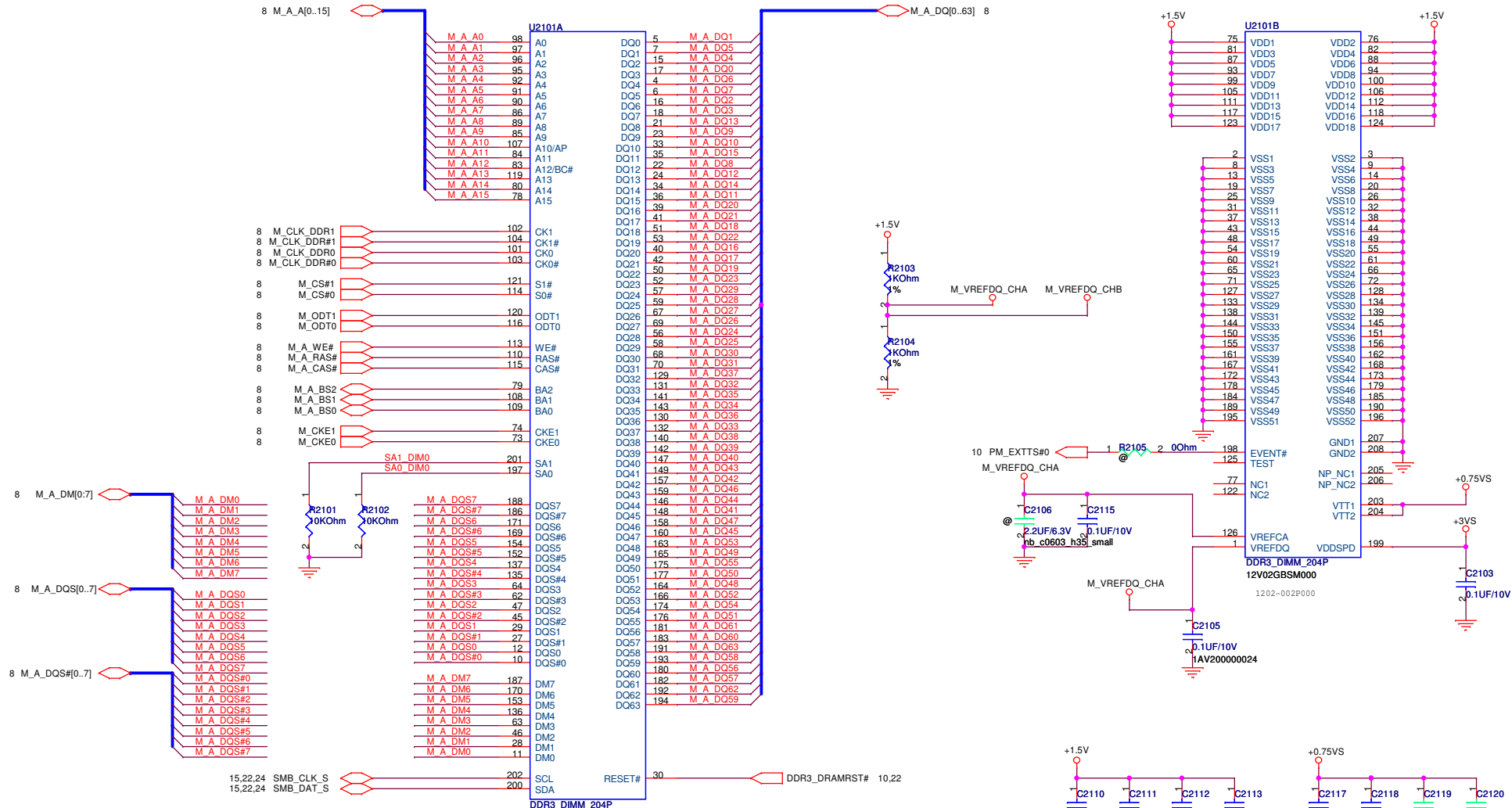
+VCCP\_VTT Rail Values:  
 VTT=1.05V; Arrandale  
 VTT=1.10V; Clarksfield



**U1301H**

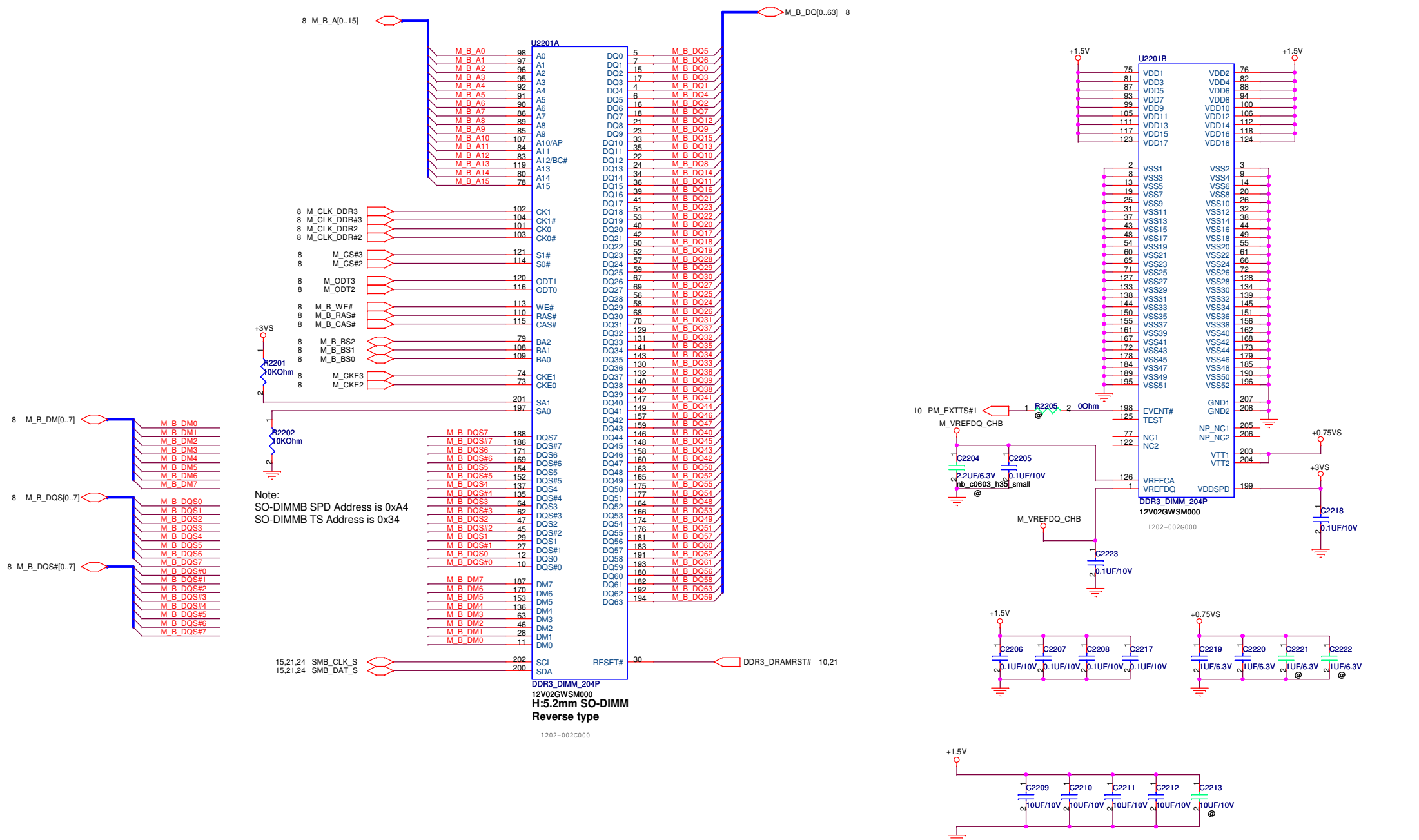
AA19	Vss1	Vss78	AK30
AA20	Vss2	Vss79	AK31
AA22	Vss3	Vss80	AK32
AA19	Vss4	Vss81	AK34
AA24	Vss5	Vss82	AK35
AA28	Vss6	Vss83	AK38
AA28	Vss7	Vss84	AK43
AA30	Vss8	Vss85	AK46
AA31	Vss9	Vss86	AK49
AA32	Vss10	Vss87	AK5
AB11	Vss11	Vss88	AK8
AB15	Vss12	Vss89	AL2
AB23	Vss13	Vss90	AL52
AB30	Vss14	Vss91	AM11
AB30	Vss15	Vss92	AM22
AB31	Vss16	Vss93	AM24
AB32	Vss17	Vss94	AM25
AB39	Vss18	Vss95	AM26
AB43	Vss19	Vss96	AM27
AB47	Vss20	Vss97	AM28
AB5	Vss21	Vss98	AM29
AB5	Vss22	Vss99	AM30
AC2	Vss23	Vss100	AM31
AC52	Vss24	Vss101	AM32
AD11	Vss25	Vss102	AM34
AD12	Vss26	Vss103	AM35
AD16	Vss27	Vss104	AM38
AD23	Vss28	Vss105	AM39
AD30	Vss29	Vss106	AM42
AD31	Vss30	Vss107	AM44
AD32	Vss31	Vss108	AM46
AD34	Vss32	Vss109	AM49
AU22	Vss33	Vss110	AM7
AD42	Vss34	Vss111	AM7
AD46	Vss35	Vss112	BB10
AD49	Vss36	Vss113	BB10
AD7	Vss37	Vss114	BB10
AE2	Vss38	Vss115	AN32
AE4	Vss39	Vss116	AN50
AE12	Vss40	Vss117	AN52
VSS43	Vss41	Vss118	AP2
AH49	Vss42	Vss119	AP46
AU4	Vss43	Vss120	AP5
AU4	Vss44	Vss121	AP8
AF35	Vss45	Vss122	AR2
AP13	Vss46	Vss123	AR2
AN34	Vss47	Vss124	AR2
AF45	Vss48	Vss125	AR52
AF46	Vss49	Vss126	AT11
AF49	Vss50	Vss127	AT11
AF5	Vss51	Vss128	AT36
AG52	Vss52	Vss129	AT36
AH11	Vss53	Vss130	AT41
AH15	Vss54	Vss131	AT47
AH16	Vss55	Vss132	AT7
AH24	Vss56	Vss133	AV12
AH32	Vss57	Vss134	AV12
AV18	Vss58	Vss135	AV16
AH43	Vss59	Vss136	AV20
AH47	Vss60	Vss137	AV24
AH7	Vss61	Vss138	AV30
AJ19	Vss62	Vss139	AV34
AJ	Vss63	Vss140	AV38
AJ20	Vss64	Vss141	AV42
AJ22	Vss65	Vss142	AV46
AJ23	Vss66	Vss143	AV49
AJ26	Vss67	Vss144	AV5
AJ28	Vss68	Vss145	AV8
AJ32	Vss69	Vss146	AW14
AJ34	Vss70	Vss147	AW18
AJ5	Vss71	Vss148	AW2
AJ4	Vss72	Vss149	AW2
AK12	Vss73	Vss150	AW32
AM41	Vss74	Vss151	AW36
AN19	Vss75	Vss152	AW40
AK26	Vss76	Vss153	AW52
AK22	Vss77	Vss154	AY11
AK23	Vss78	Vss155	AY43
AK28	Vss79	Vss156	AY47
	Vss80	Vss157	
	Vss81	Vss158	
	Vss82	Vss159	
	Vss83	Vss160	
	Vss84	Vss161	
	Vss85	Vss162	
	Vss86	Vss163	
	Vss87	Vss164	
	Vss88	Vss165	
	Vss89		
	Vss90		
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	Vss163		
	Vss164		
	Vss165		





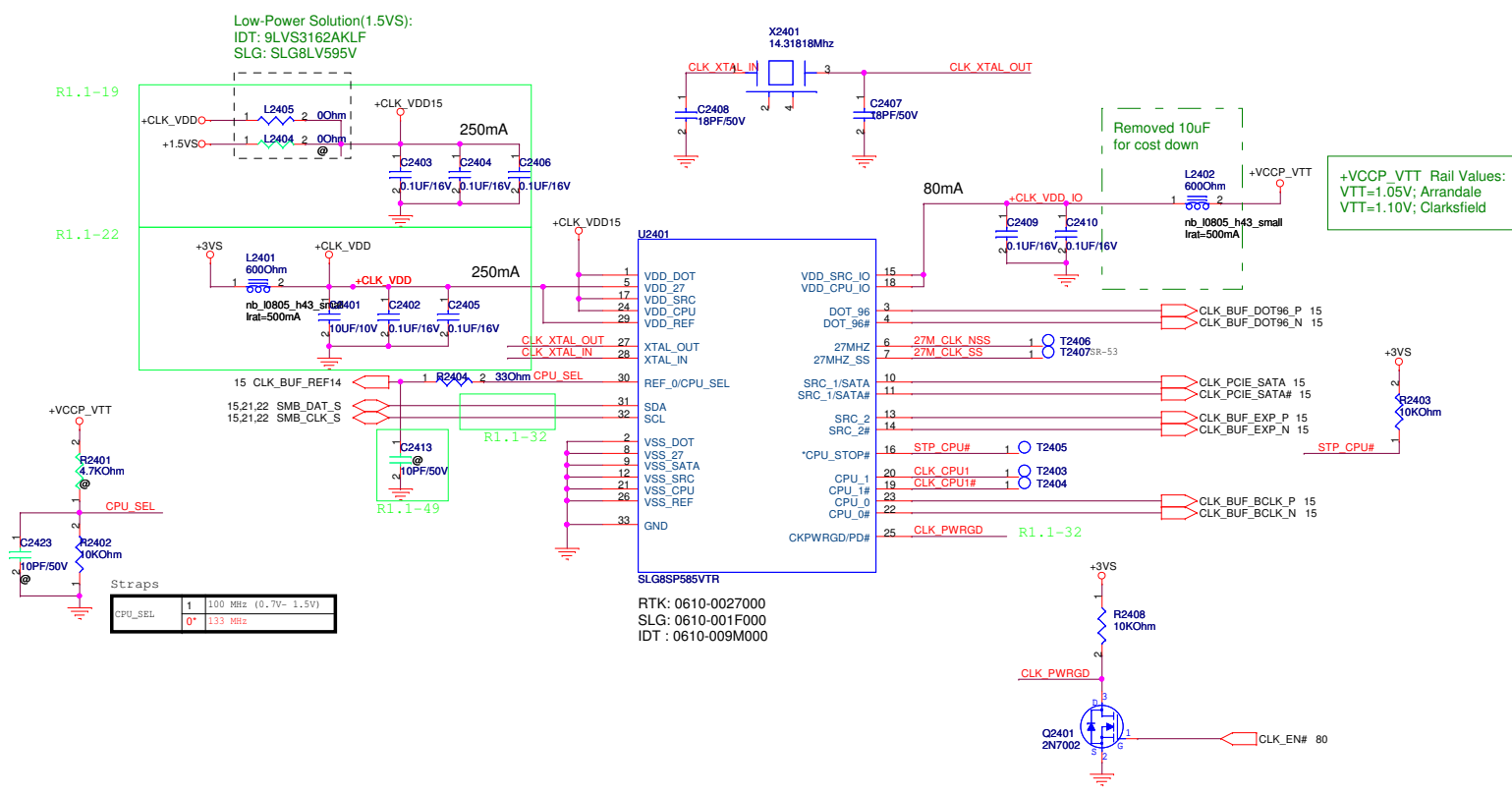
Note:  
 If SA0\_DIM0 = 0, SA1\_DIM0 = 0  
 SO-DIMMA SPD Address is 0xA0  
 SO-DIMMA TS Address is 0x30  
 If SA0\_DIM0 = 1, SA1\_DIM0 = 0  
 SO-DIMMA SPD Address is 0xA2  
 SO-DIMMA TS Address is 0x32





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**PEGATRON** Title : DDR3 SO-DIMM-Channel B  
 BU1-RD Div.1-HW RD Dept.1 Engineer: Elmer Chiu  
 Size Project Name  
 Custom BIC50  
 Date: Tuesday, May 03, 2011 Sheet 22 of 77  
 Rev 2.0



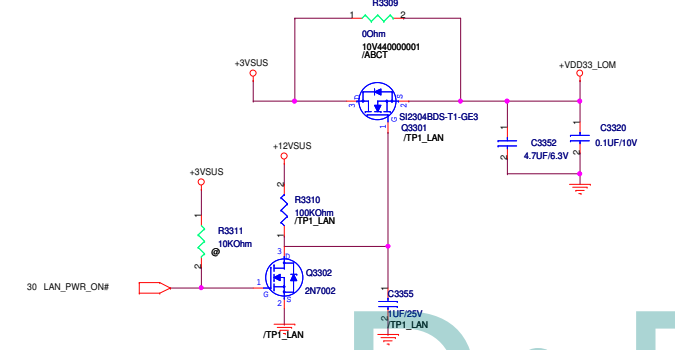
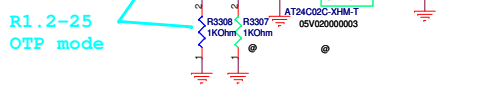
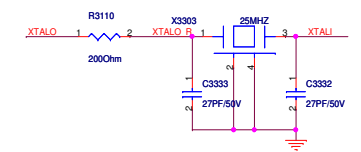
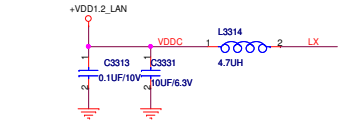
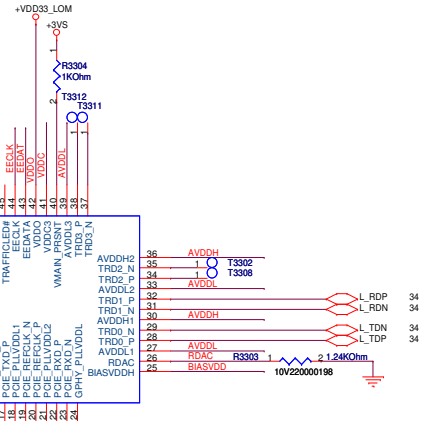
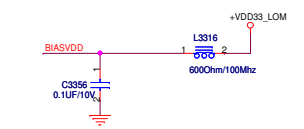
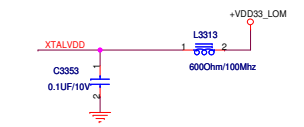
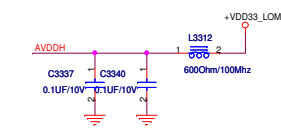
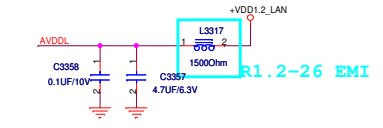
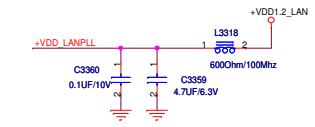
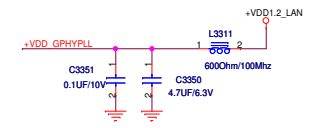
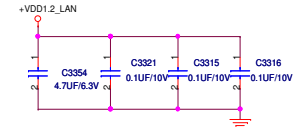
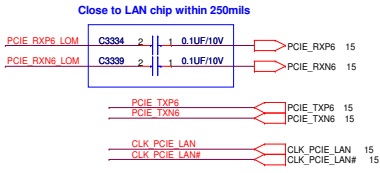
Straps

CPU_SEL	1	100 MHz (0.7V-1.5V)
	0*	133 MHz

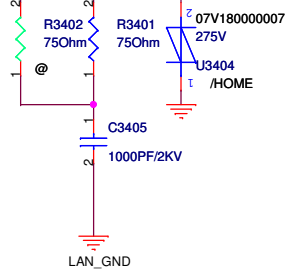
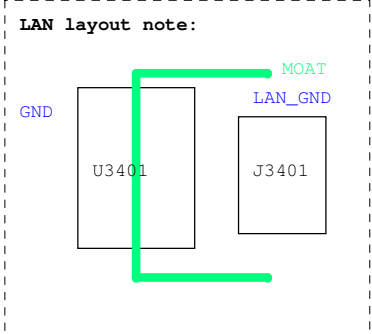
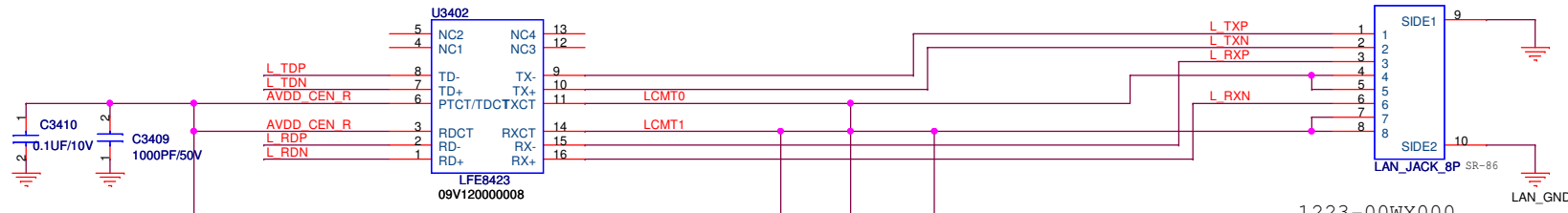
SLG8SP585VTR  
 RTK: 0610-0027000  
 SLG: 0610-001F000  
 IDT: 0610-009M000

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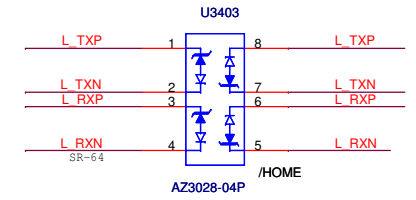




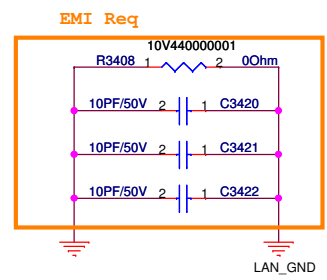
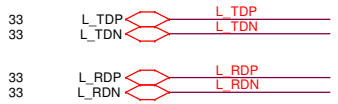
**Dr-Bios.com**



1223-00WX000  
**Change RJ45 CON3401** SR-4 0120-11



**Modify LAN ESD circuit** SR-33 0125-11

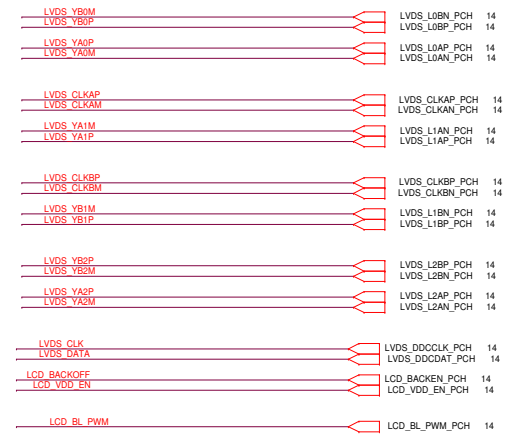
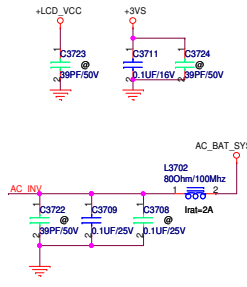
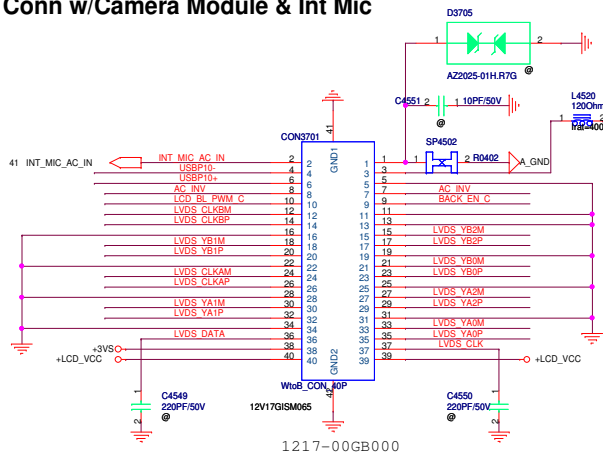


**Modify LAN AR8158 circuit** SR-12 0121-11

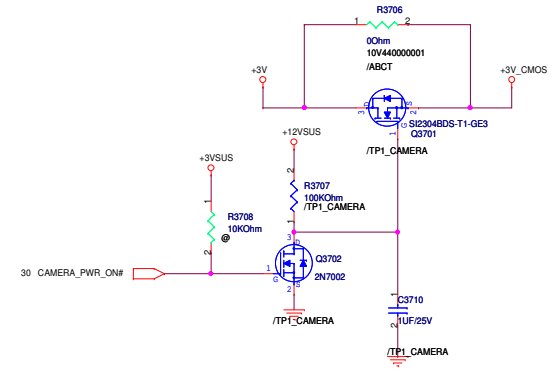
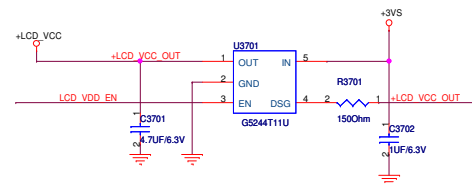
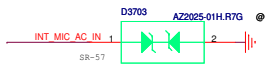
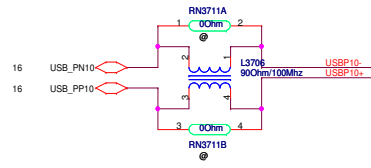
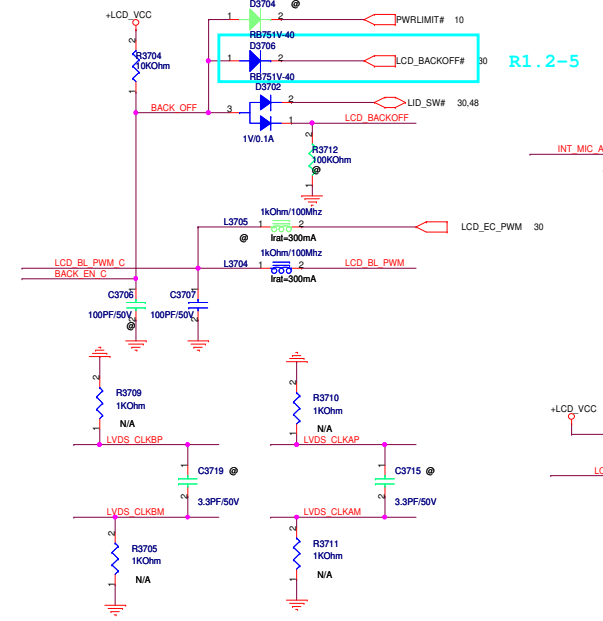
**Modify Transformer circuit** SR-40 0125-11 SR-45 0125-11 SR-48 0125-11

<b>PEGATRON</b> Title :RJ45		
BG1-HW RD Div.2-NB RD Dept.5		Engineer: <b>Elmer Chiu</b>
Size B	Project Name <b>BIC50</b>	Rev 1.0
Date: Tuesday, May 03, 2011		Sheet 34 of 77

# LVDS Conn w/Camera Module & Int Mic



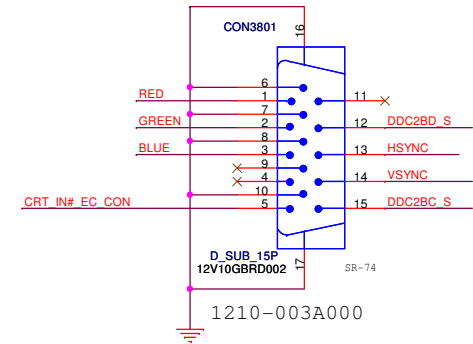
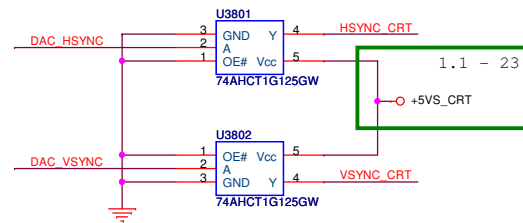
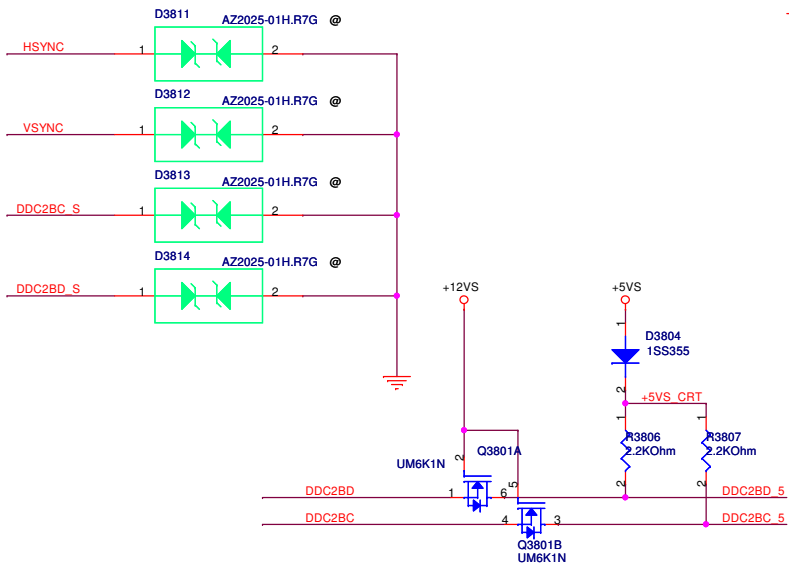
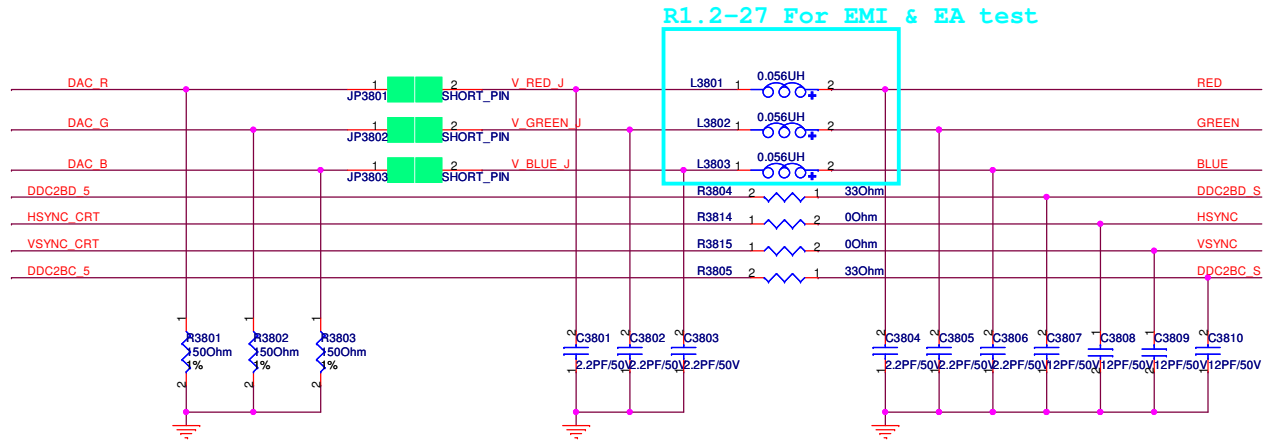
## Modify LVDS Pin definition



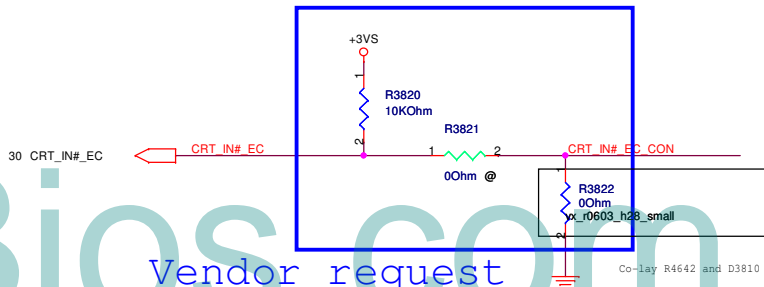
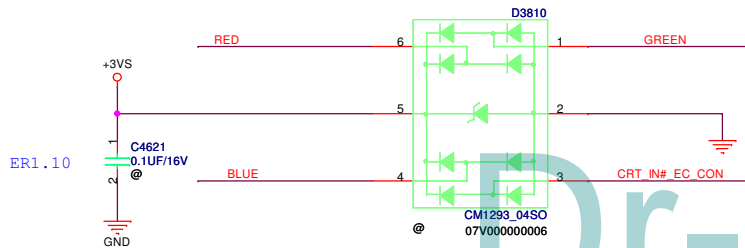
FOR TP1 02/23

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- 14 DAC\_R\_PCH → DAC\_R
- 14 DAC\_G\_PCH → DAC\_G
- 14 DAC\_B\_PCH → DAC\_B
- 14 DAC\_HSYNC\_PCH → DAC\_HSYNC
- 14 DAC\_VSYNC\_PCH → DAC\_VSYNC
- 14 DDC2BD\_PCH → DDC2BD
- 14 DDC2BC\_PCH → DDC2BC



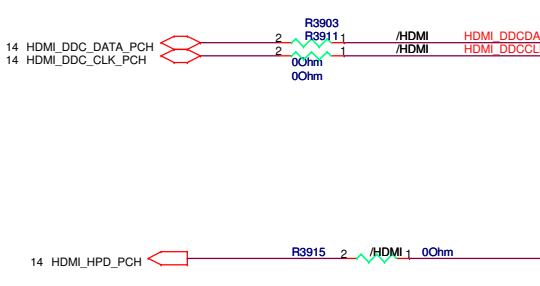
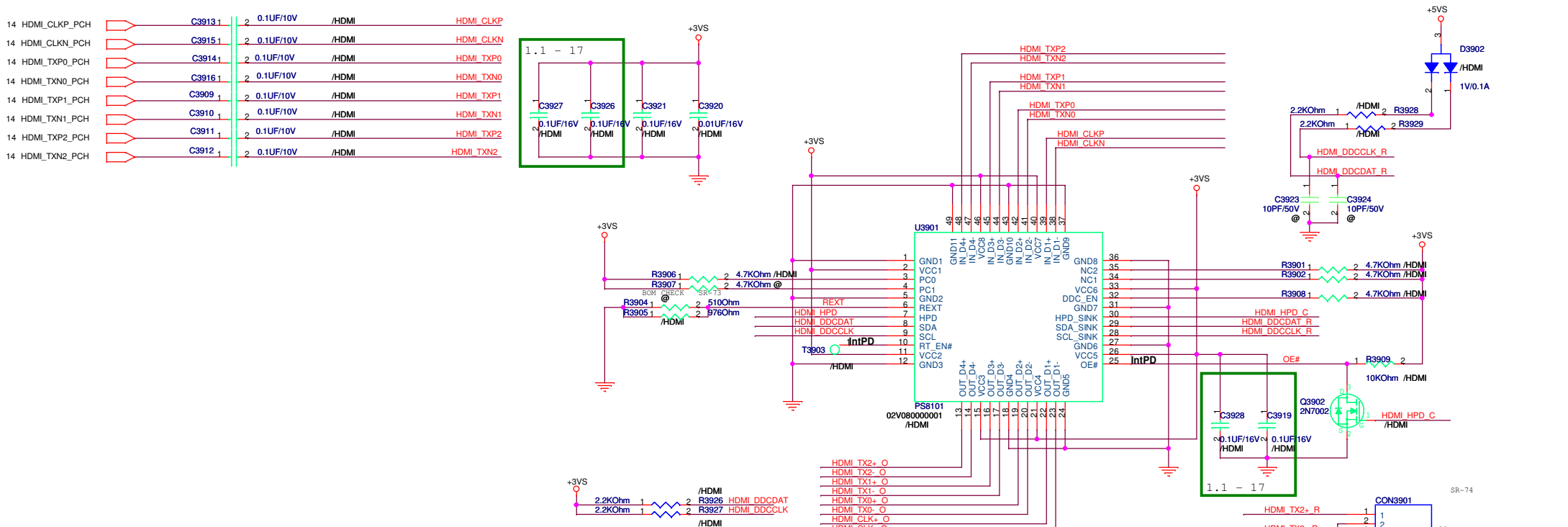
Del F3801, C3811 ADD CRT IN SR-36 0125-11



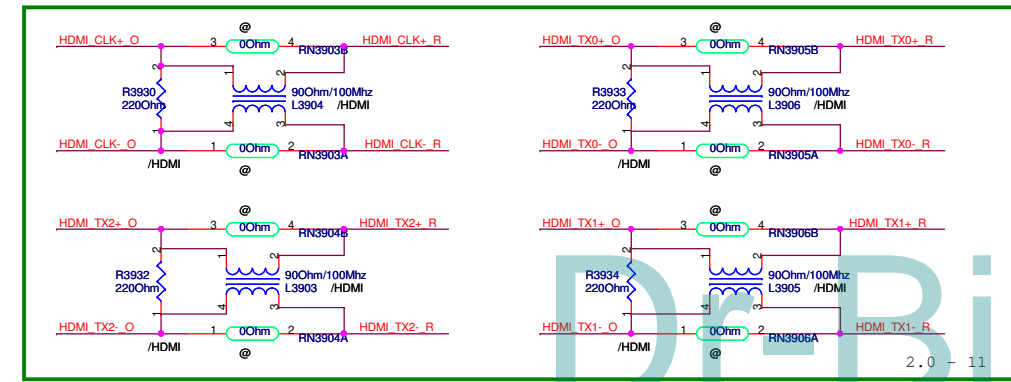
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Vendor request

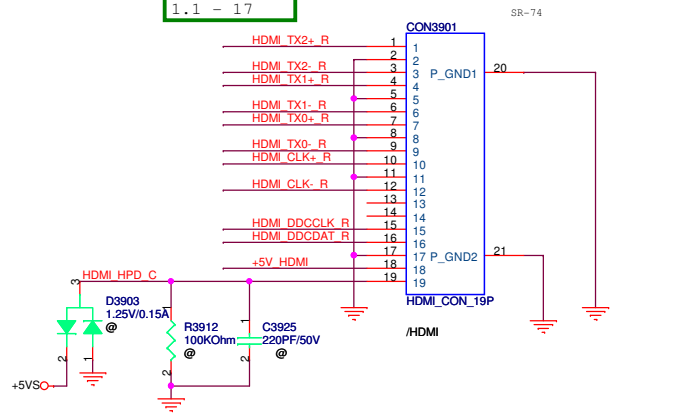




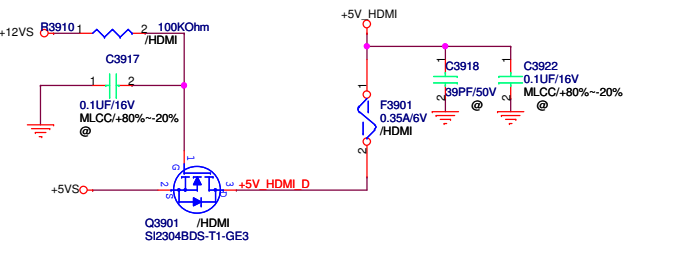
1.1 - 14



2.0 - 11



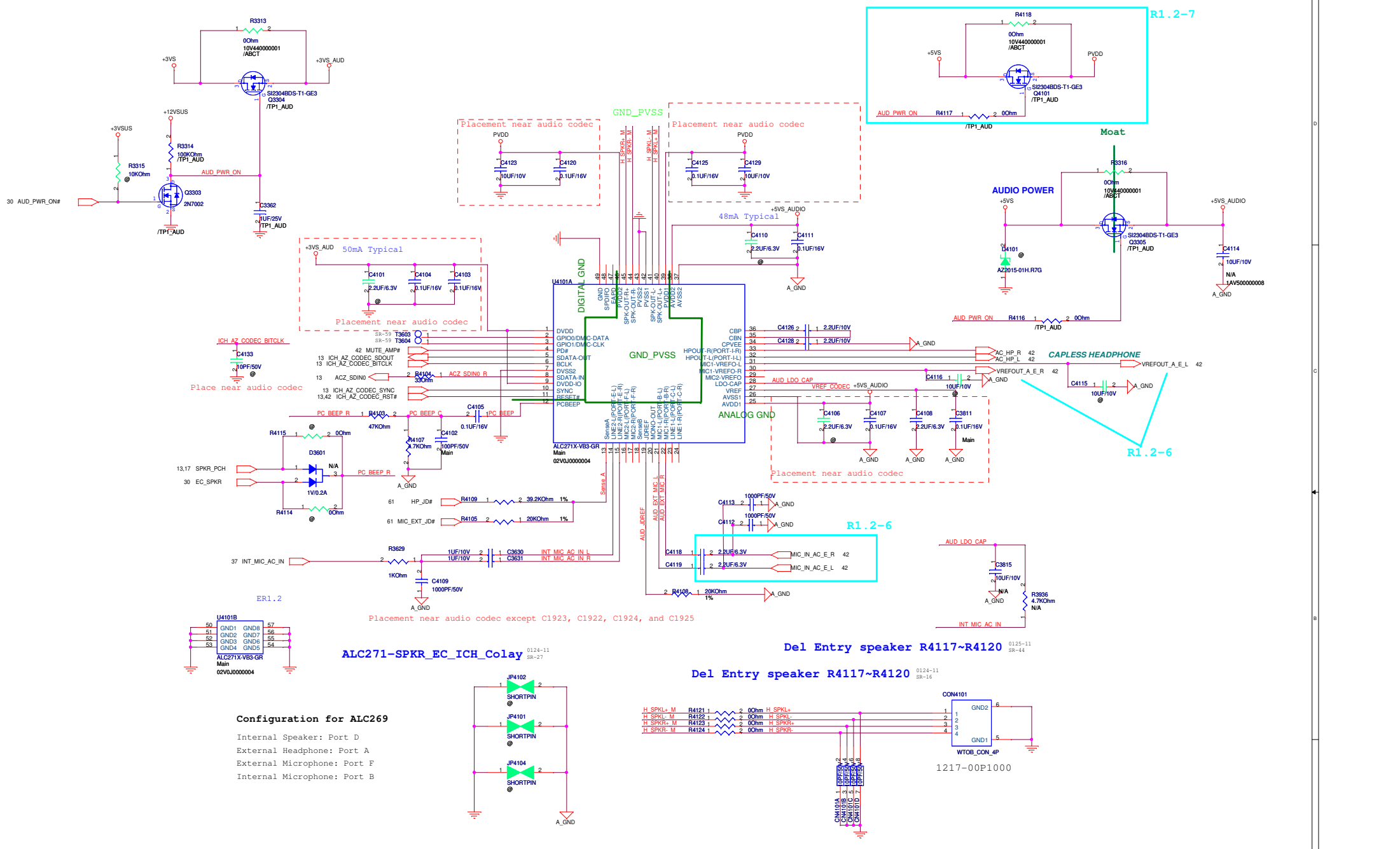
HDMI SPEC : 4.8~5.3V



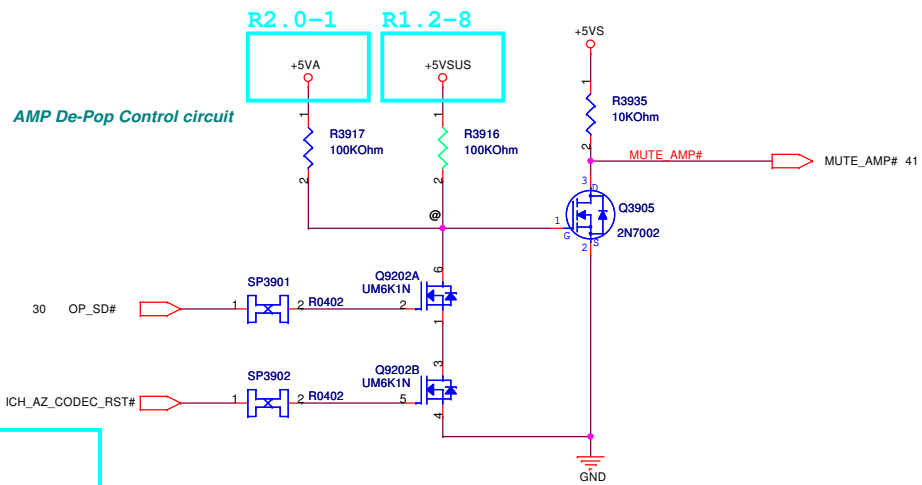
<b>PEGATRON</b> Title : <b>HDMI</b>		
BG1-HW RD Div.2-NB RD Dept.5		Engineer: <b>Elmer Chiu</b>
Size: Custom	Project Name: <b>BIC50</b>	Rev: 2.0
Date: Tuesday, May 03, 2011	Sheet: 39	of 77

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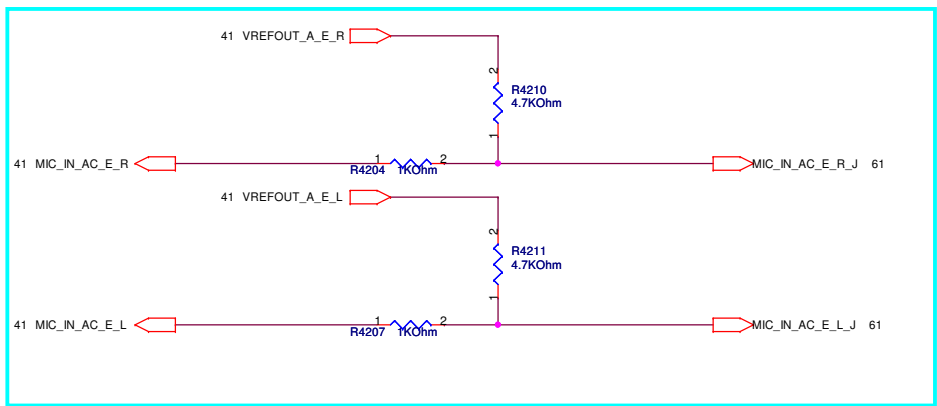
<b>PEGATRON</b> Title : <i>Display Port</i>		
BU1-RD Div.1+HW RD Dept.1 Engineer: <i>Elmer Chiu</i>		
Size Custom	Project Name <b>BIC50</b>	Rev 2.0
Date: <i>Tuesday, May 03, 2011</i>	Sheet 40	of 77



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**Modify De-Pop circuit** SR-43 0125-11



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<b>PEGATRON</b> Title : AUDIO ALC269	
BU1-RD Div.1-HW RD Dept.1 Engineer: Elmer Chiu	
Size Custom	Project Name <b>BIC50</b>
Date: Tuesday, May 03, 2011	Rev 2.0
Sheet 42 of 77	

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<b>PEGATRON</b>		Title : <b>MDC CONN</b>	
BG1-HW RD Div:2-NB RD Dept.5		Engineer: <b>Elmer Chiu</b>	
Size	Project Name	Rev	
C	<b>BIC50</b>	2.0	
Date: <b>Tuesday, May 03, 2011</b>		Sheet	43 of 77

Del Entry audio circuit

SR-8  
0121-11

Dr-Bios.com

<b>PEGATRON</b>		Title : <b>CODEC-ALC269</b>	
ASUSTeK COMPUTER INC. NB1		Engineer: <b>Elmer Chiu</b>	
Size Custom	Project Name <b>BIC50</b>	Rev 2.0	
Date: <b>Tuesday, May 03, 2011</b>		Sheet	44 of 77

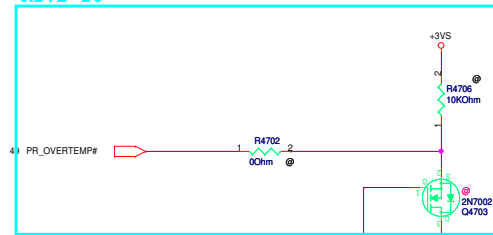
Del Entry audio circuit SR-8  
0121-11

Dr-Bios.com

<b>PEGATRON</b> Title : <b>AUDIO ALC269</b>	
BU1-RD Div.1+HW RD Dept.1 Engineer: <b>Elmer Chiu</b>	
Size Custom	Project Name <b>BIC50</b>
Date: <b>Tuesday, May 03, 2011</b>	Rev <b>2.0</b>
Sheet 45 of 77	

R1.2-10

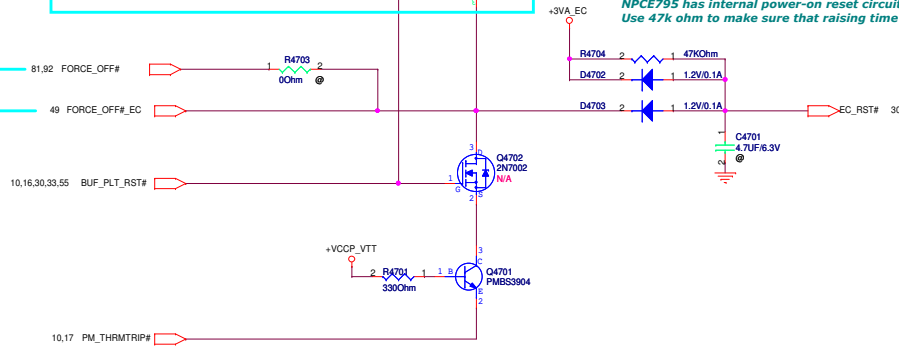
### Thermal Policy



NPCE795 has internal power-on reset circuit  
Use 47k ohm to make sure that raising time of POR is less than 10us

R1.2-9 From PWR protect

From thermistor



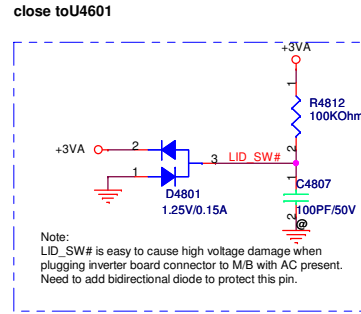
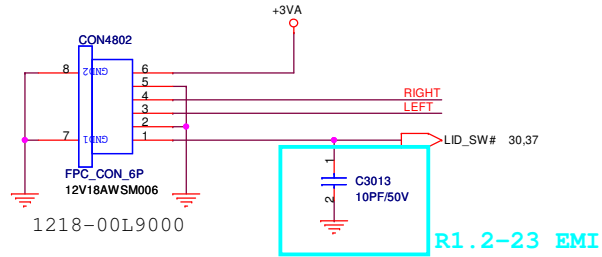
Input Signal

- +3VA\_EC -> +3VA\_EC 13,30
- +3VS -> +3VS 10,13,14,15,16,17,18,19,21,22,24,30,33,37,38,39,41,49,60,63,65,80,86,91,92

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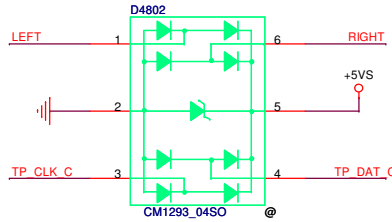
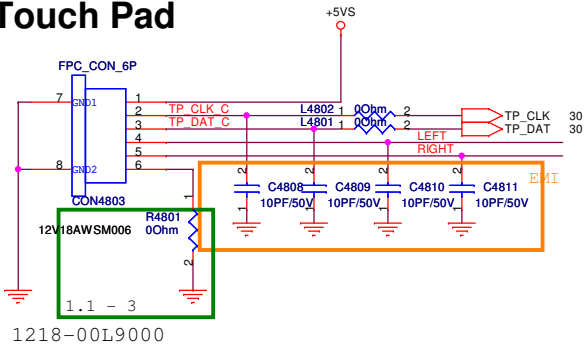


# Touch Pad Button/ Hall Sensor



R1.2-23 EMI

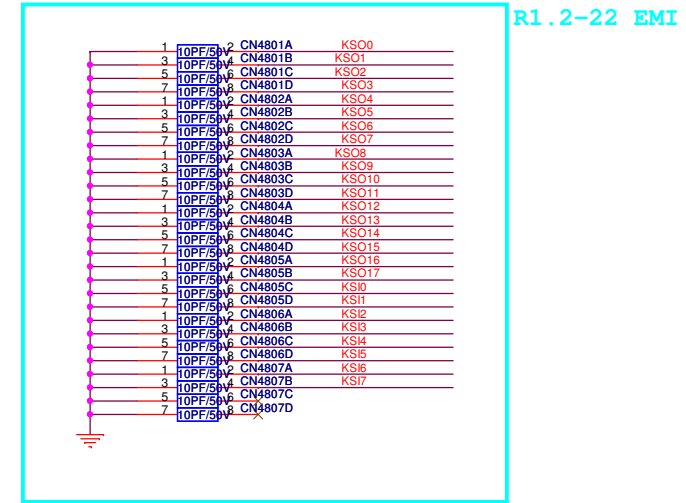
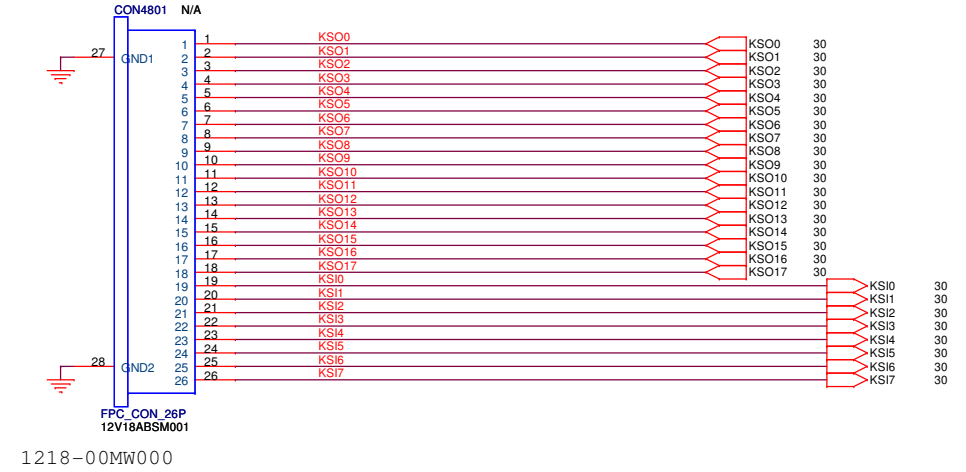
# Touch Pad



1.1 - 3

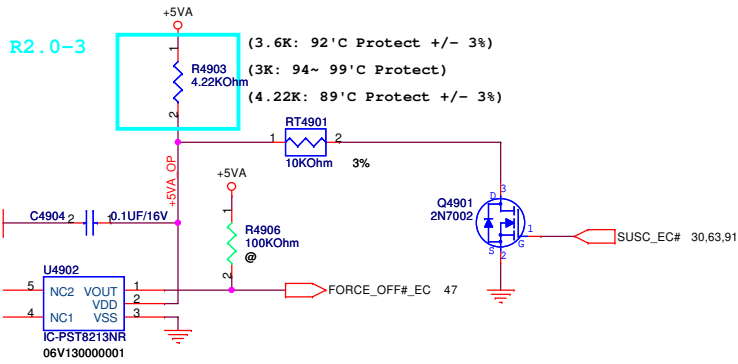
Remove TP button circuit SR-22 0124-11

# Keyboard

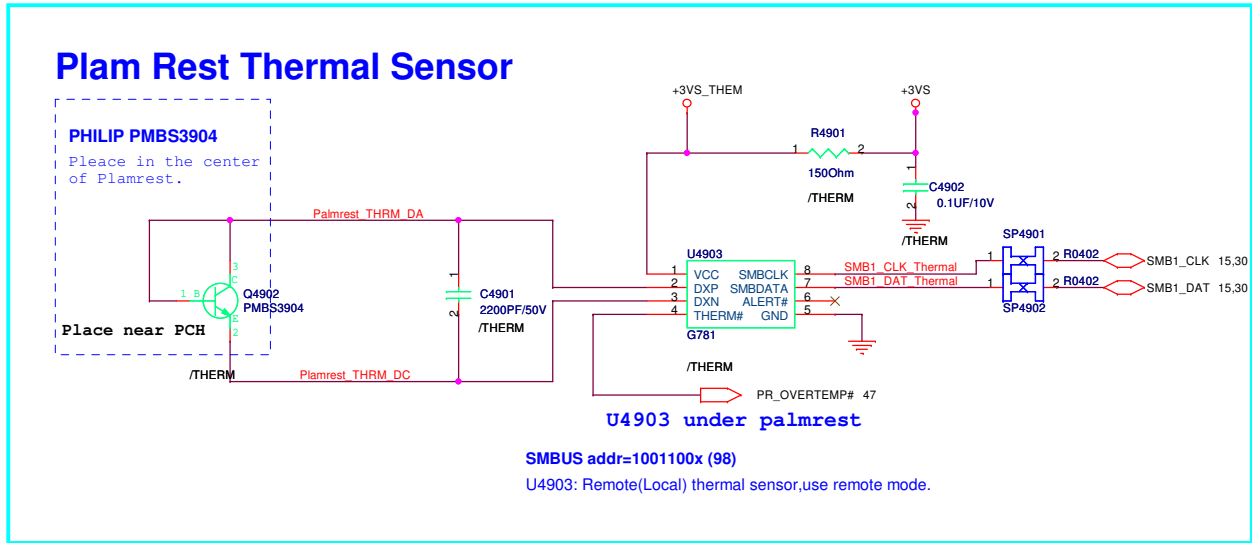


R1.2-22 EMI

# Thermister

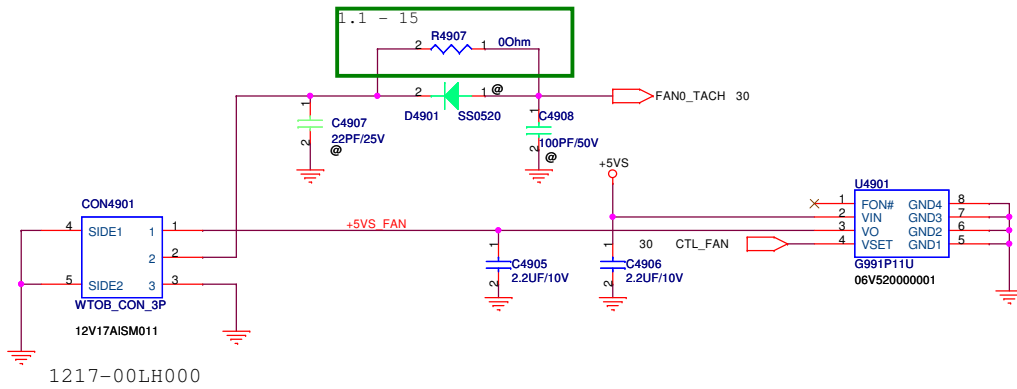


# Plam Rest Thermal Sensor



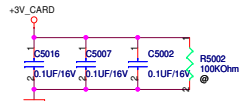
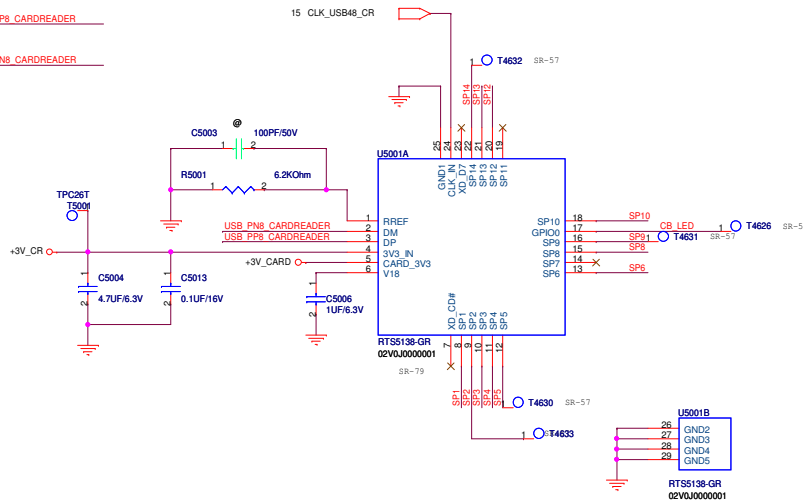
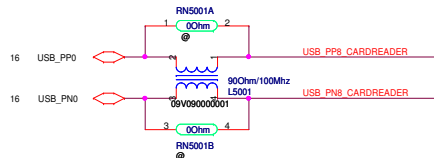
R1.2-10

# FAN



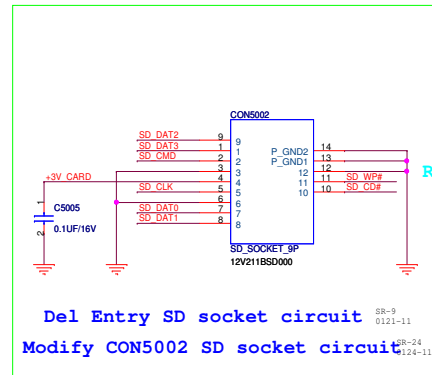
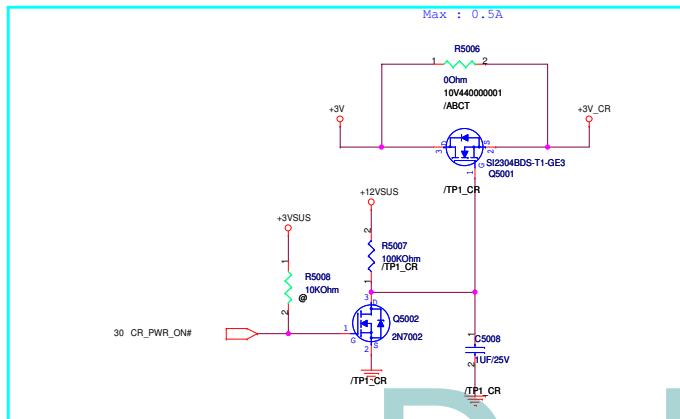
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<b>PEGATRON</b> Title : THERMAL/ FAN	
BU1-RD Div.1-HW RD Dept.1 Engineer: Elmer Chiu	
Size	Project Name
Custom	<b>BIC50</b>
Date: Wednesday, May 18, 2011	Sheet 49 of 77
Rev	2.0



Close to connector

FOR TP1 02/23



Del Entry SD socket circuit SR-9 0121-11  
 Modify CON5002 SD socket circuit SR-24 1124-11

Pin Name	Description
SP1	SDWP# / MSCLK
SP2	MS_IN#
SP3	SD_DAT1
SP4	SD_DAT0
SP5	MS_D3
SP6	SD_CD#
SP8	SD_CLK / MS_D2
SP9	MS_D0
SP10	SD_CMD
SP12	SD_DAT3 / MS_D1
SP13	SD_DAT2
SP14	MS_BS

SP1	SD_WP#	MS_CLK
SP2		MS_IN#
SP3	SD_DAT1	
SP4	SD_DAT0	
SP5		MS_D3
SP6	SD_CD#	
SP8	SD_CLK	MS_D2
SP9		MS_D0
SP10	SD_CMD	
SP12	SD_DAT3	MS_D1
SP13	SD_DAT2	
SP14		MS_BS

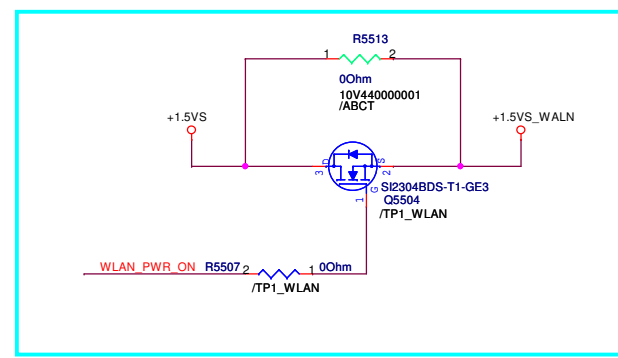
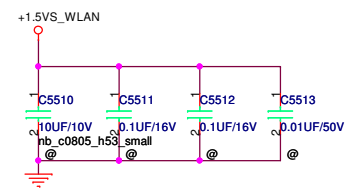
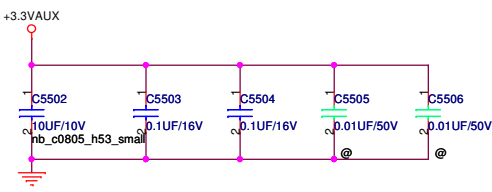
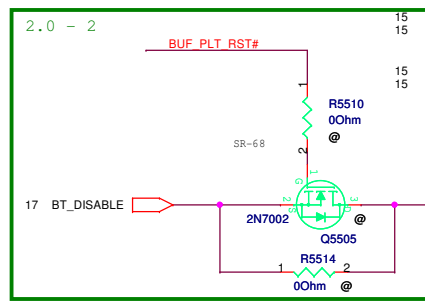
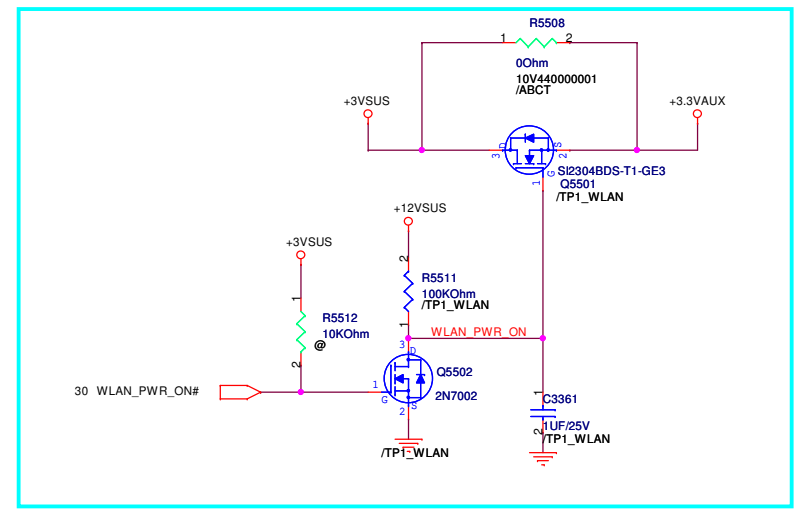
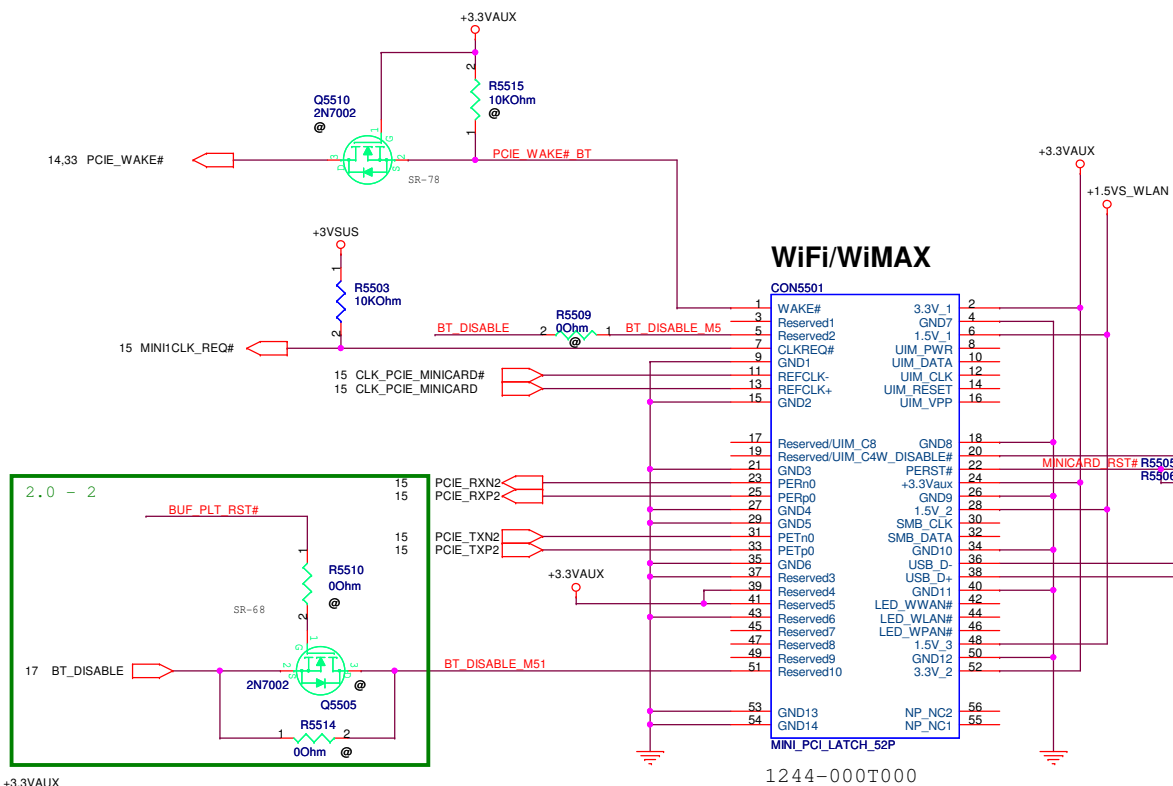
Dr-Bios.com

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<b>PEGATRON</b>		Title : <b>USB3.0 uPD720200</b>	
BG11HW1		Engineer: <b>Elmer Chiu</b>	
Size	Project Name	Rev	
C	<b>BIC50</b>	2.0	
Date: <b>Tuesday, May 03, 2011</b>		Sheet	<b>53</b> of <b>77</b>

Dr-Bios.com

<b>PEGATRON</b> Title : <b>PCIE NEW CARD</b>	
BU1-RD Div.1+HW RD Dept.1 Engineer: <b>Elmer Chiu</b>	
Size Custom	Project Name <b>BIC50</b>
Date: <b>Tuesday, May 03, 2011</b>	Rev <b>2.0</b>
Sheet <b>54</b> of <b>77</b>	



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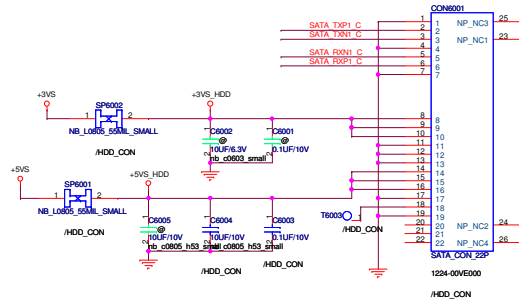
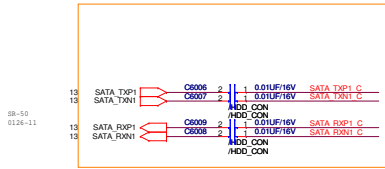
<b>PEGATRON</b> Title : <b>MINICARD (WWAN)</b>	
BU1-RD Div.1+HW RD Dept.1 <b>Engineer:</b>	
Size Custom	Project Name
Date: <b>Tuesday, May 03, 2011</b>	Rev <b>2.0</b>
Sheet <b>56</b> of <b>77</b>	

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<b>PEGATRON</b> Title : <b>MINICARD (WUSB /UPCONVERT)</b>		
BU1-RD Div.1+HW RD Dept.1 Engineer: <b>Elmer Chiu</b>		
Size Custom	Project Name <b>BIC50</b>	Rev 2.0
Date: <b>Tuesday, May 03, 2011</b>	Sheet <b>57</b> of <b>77</b>	



R2.0-28

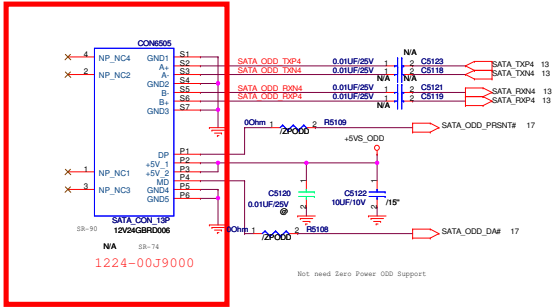


Change HDD CON6001 02/17

### HDD

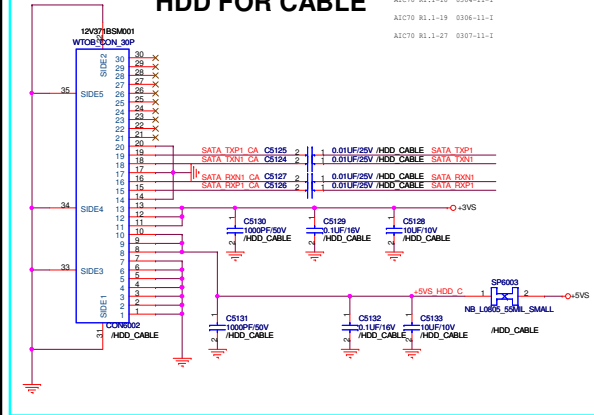
### SSD

#### ODD



Not need Zero Power ODD Support

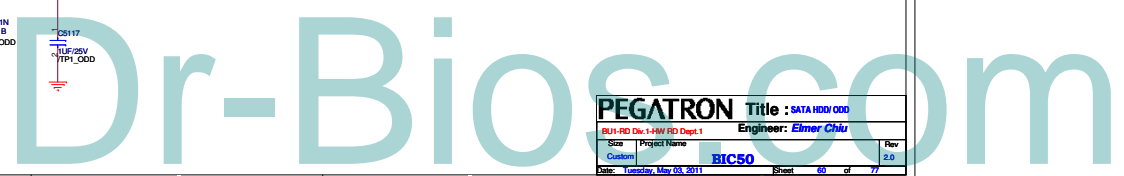
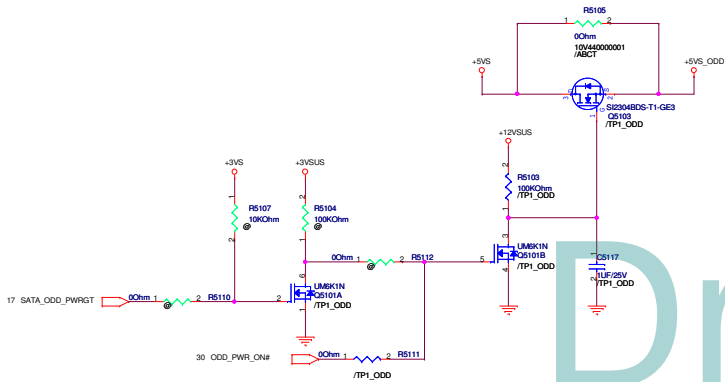
#### HDD FOR CABLE

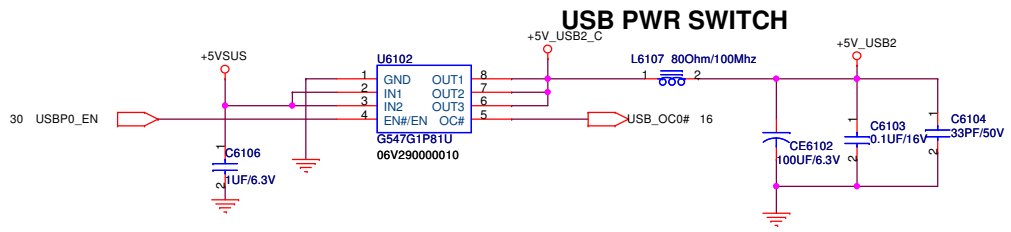


R1.2-13

### ZERO POWER ODD SUPPORT

support Hokey turn off ODD power

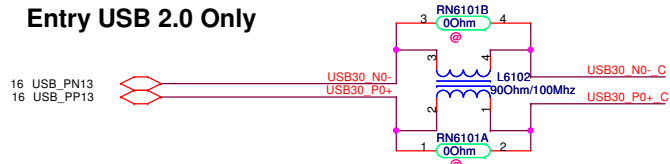




change USB power switch circuit

SR-1 0120-11 SR-26 0124-11 SR-34 0125-11

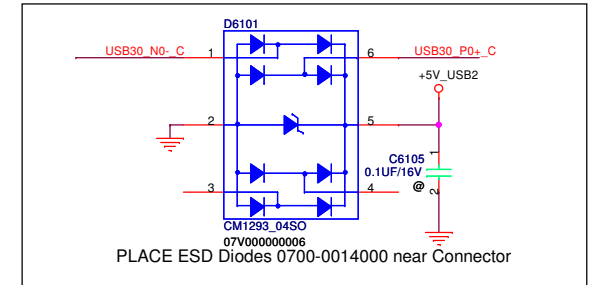
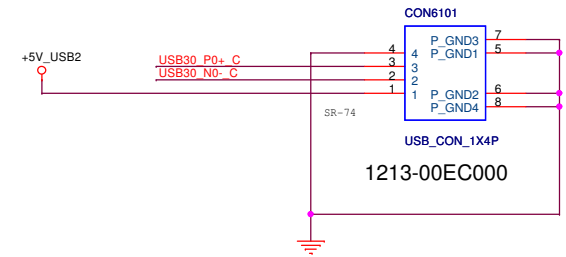
Entry USB 2.0 Only



Modify D6101, RN6101, RN6105, RN6106

SR-30 0125-11

USB 2.0

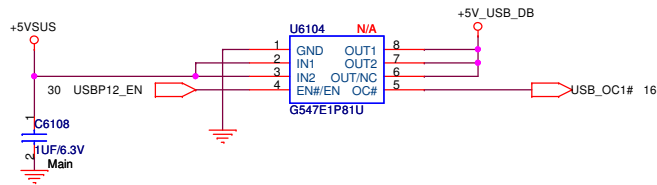


USB Conn. for Entry colay HDMI USB 2.0

Remove USB\_9 (HDMI)

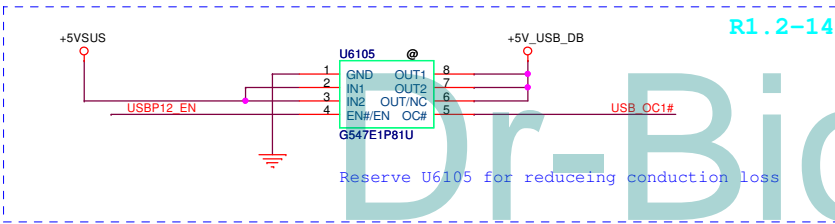
SR-21 0124-11

USB Power Switch for USB DB Main



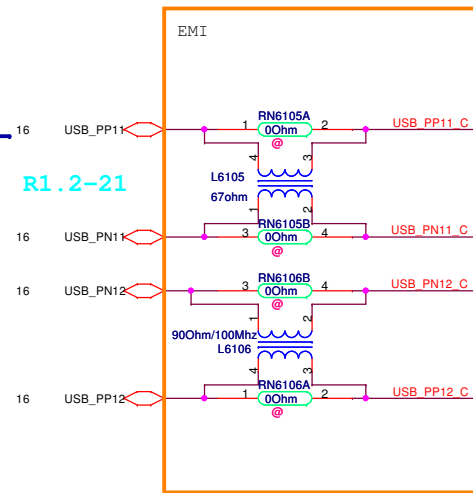
change USB power switch circuit

SR-26 0124-12 SR-38 0125-13

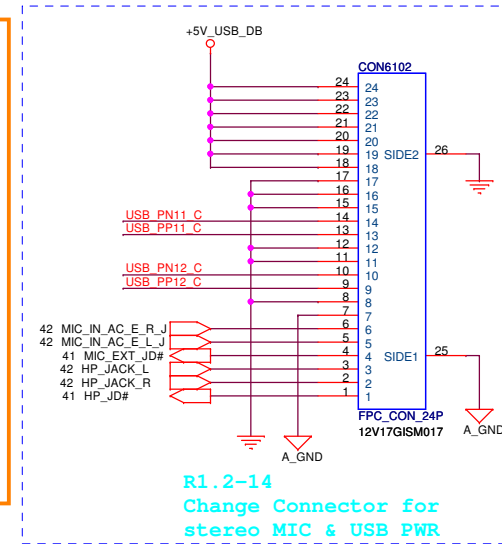


R1.2-14

AUDIO BOARD/w USB2.0 x2



R1.2-21



R1.2-14 Change Connector for stereo MIC & USB PWR

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TouchPanel CON

Camera Module CON

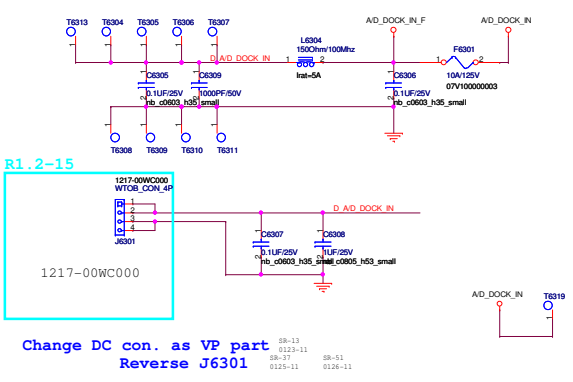
B/T MODULE

FELICA MODULE

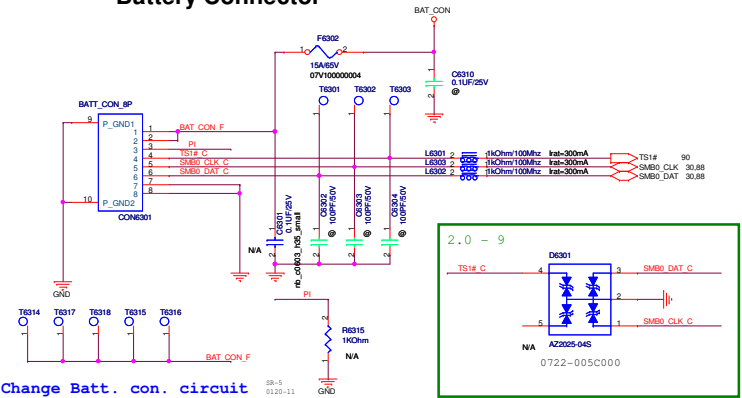
Dr-Bios.com

<b>PEGATRON</b>		Title : <i>Camera/ BT/ FL CONN</i>	
BU1-RD Div.1+HW RD Dept.1		Engineer: <i>Elmer Chiu</i>	
Size Custom	Project Name <b>BIC50</b>	Date: <i>Tuesday, May 03, 2011</i>	Rev 2.0
Date: <i>Tuesday, May 03, 2011</i>		Sheet	62 of 77

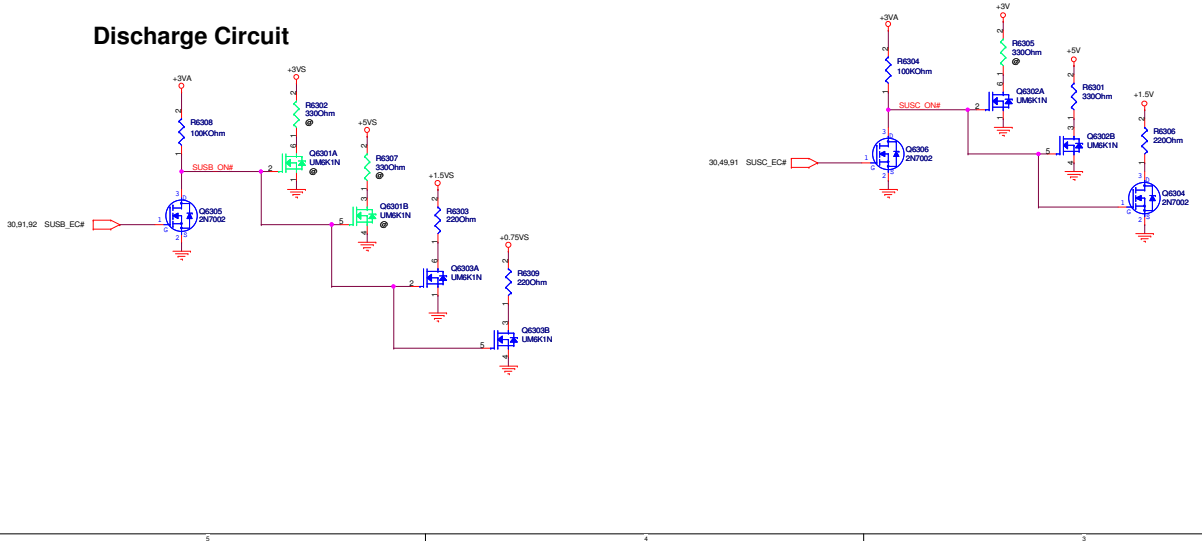
### DC IN



### Battery Connector



### Discharge Circuit



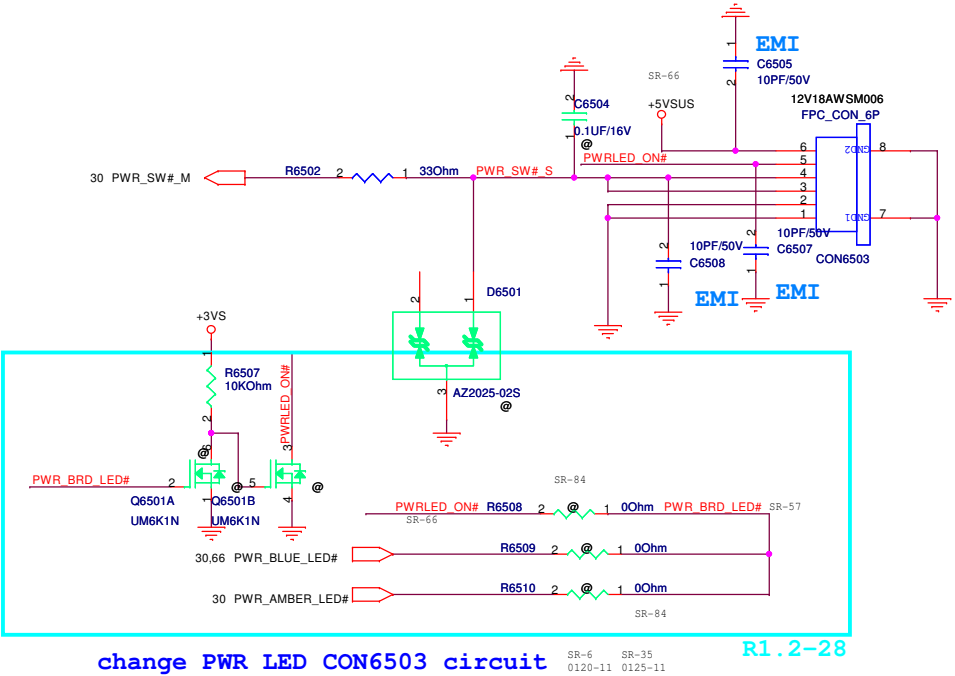
<b>PEGATRON</b>		Title : DC-IN DISCHARGE	
BLU-FD Dc-1+HW FID Dept.1		Engineer: <i>Elmer Chiu</i>	
Size	Project Name	Rev	
Custom	<b>BICSO</b>	2.0	
Date: Tuesday, May 03, 2011	Sheet	65	of 77

Notes:  
BRAIDWOOD right angled Connector (1.8V keyed)  
Compatible BRAIDWOOD Modules  
1.8V Mobile NVM 4GB 31.60mm x21.5mm  
1.8V Mobile NVM 8GB 31.60mm x 21.5mm  
1.8V Mobile NVM 16GB 31.60mm x 32.5mm

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<b>PEGATRON</b> Title : <i>NVM</i>		
BU1-RD Div.1+HW RD Dept.1 Engineer: <i>Elmer Chiu</i>		
Size Custom	Project Name <b>BIC50</b>	Rev 2.0
Date: <i>Tuesday, May 03, 2011</i>		Sheet 64 of 77

# PWR BRD/ AMBIENT/ HALL CONN.

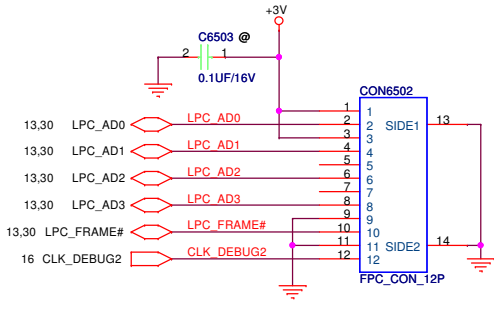
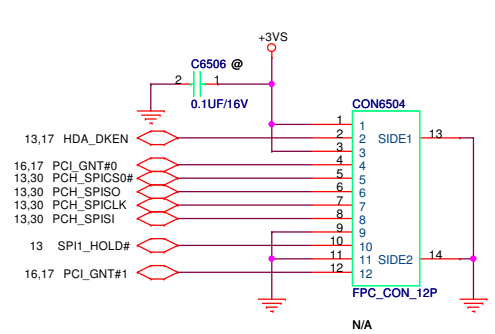


change PWR LED CON6503 circuit

# MODEM MODULE

# KILL SWITCH.

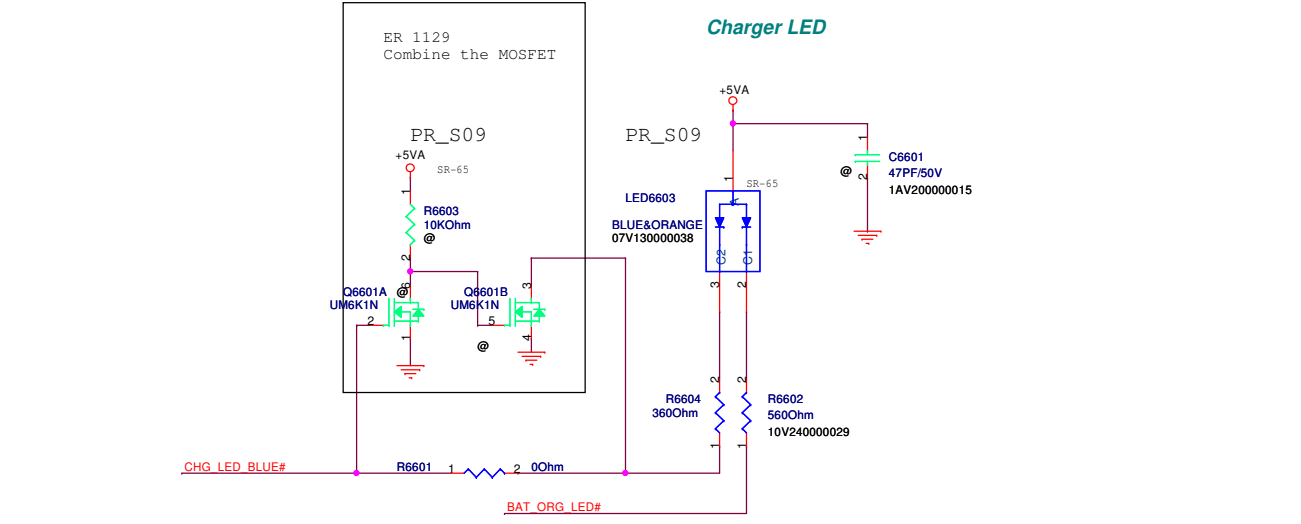
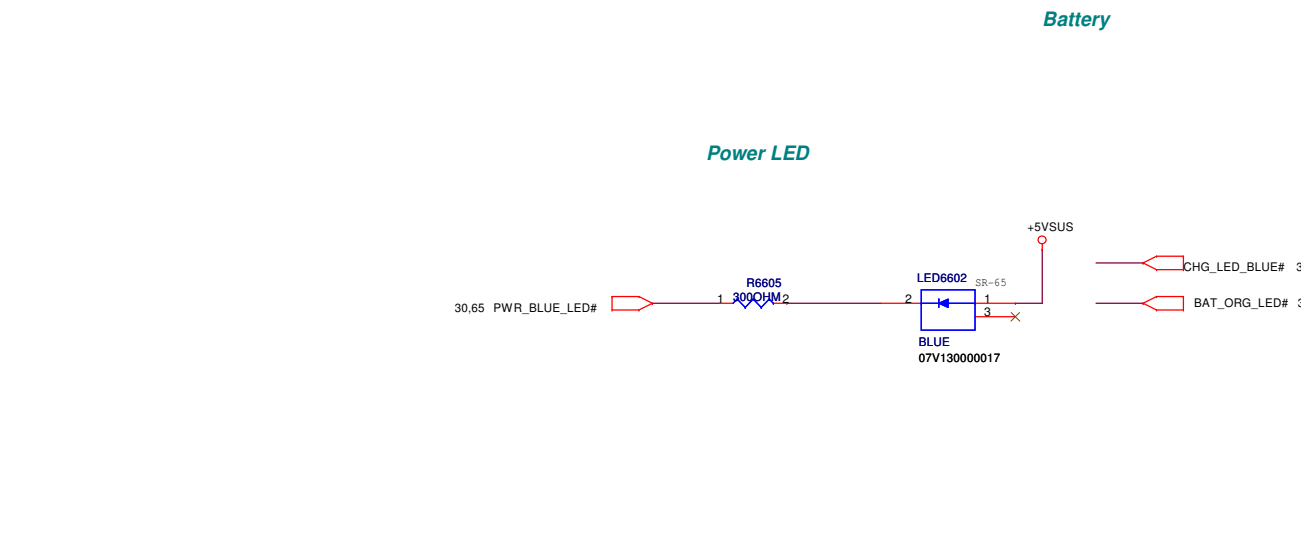
# DEBUG CARD CONN.



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**LED (Main)** ← Right

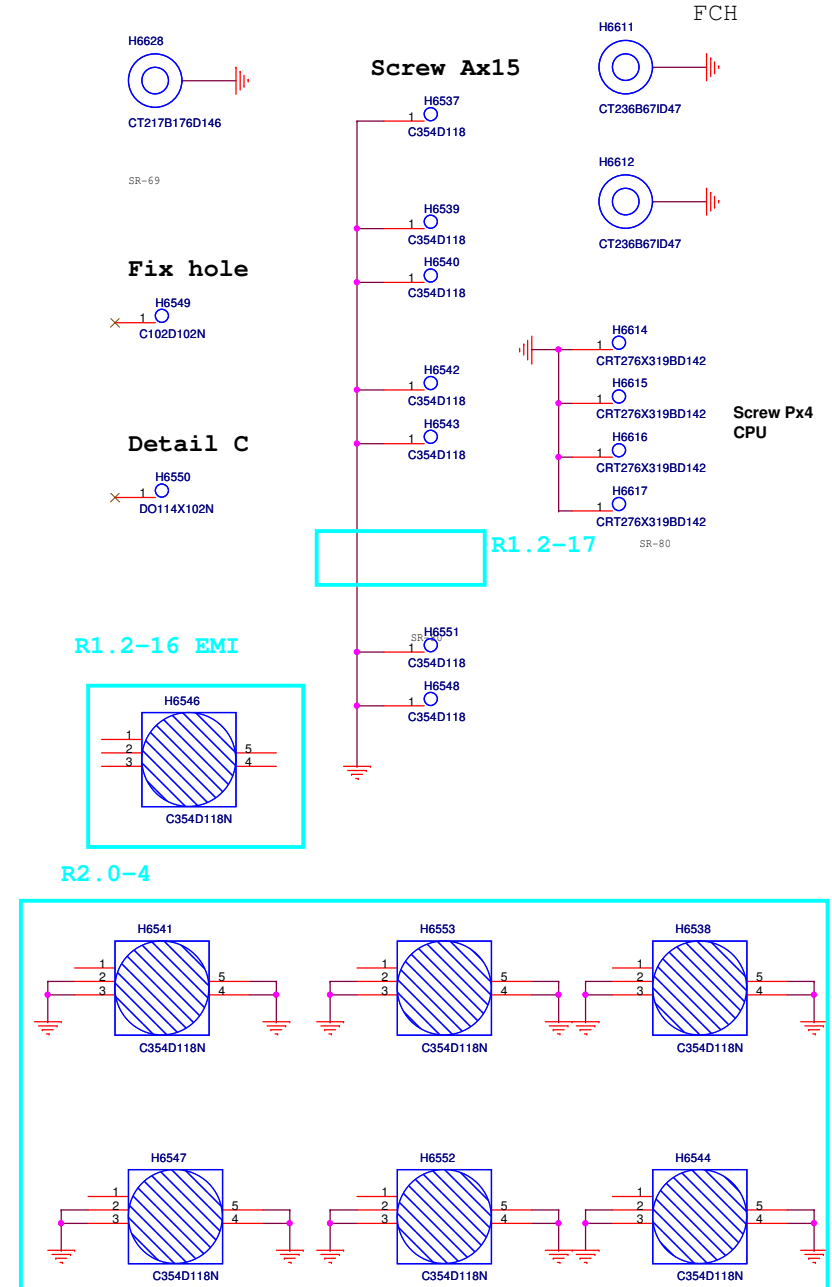
<b>DC-IN</b>	<b>Power</b>	<b>Main Battery</b>	<b>HDD/ODD</b>	<b>Bridge Media</b>	<b>WiFi</b>
White	White Amber (Blink)	White Amber (Blink)	White	White	Amber



Remove LED circuit SR-18 0124-11  
 Modify LED circuit SR-28 0124-11 SR-39 0125-11

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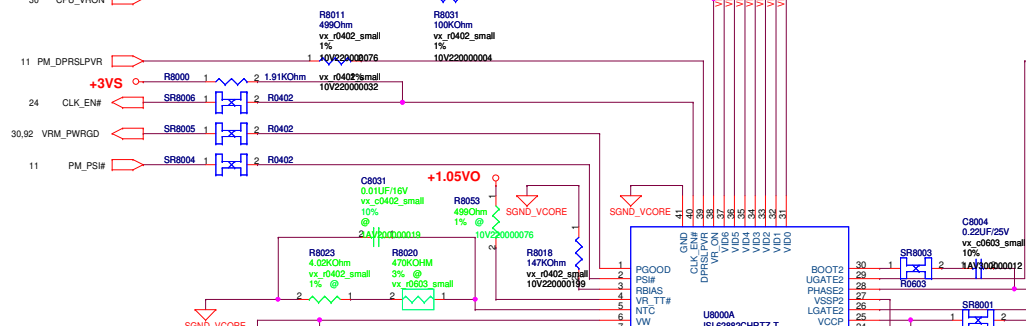
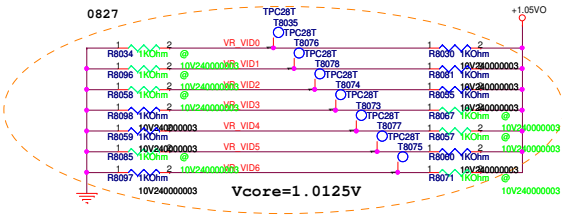
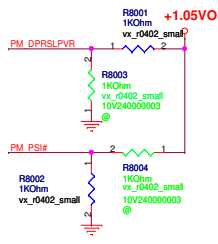
WLAN NUT PCH Local Side Symbol



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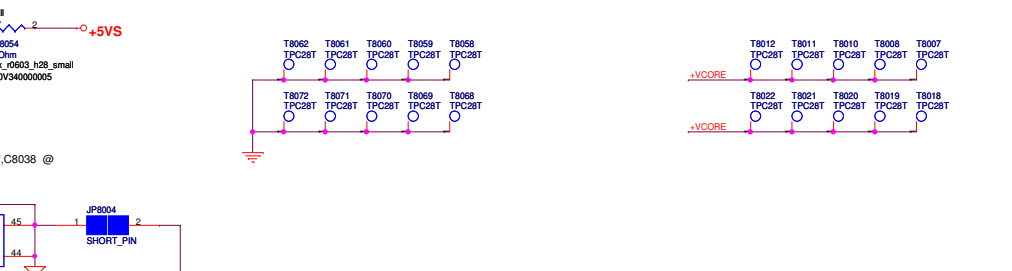
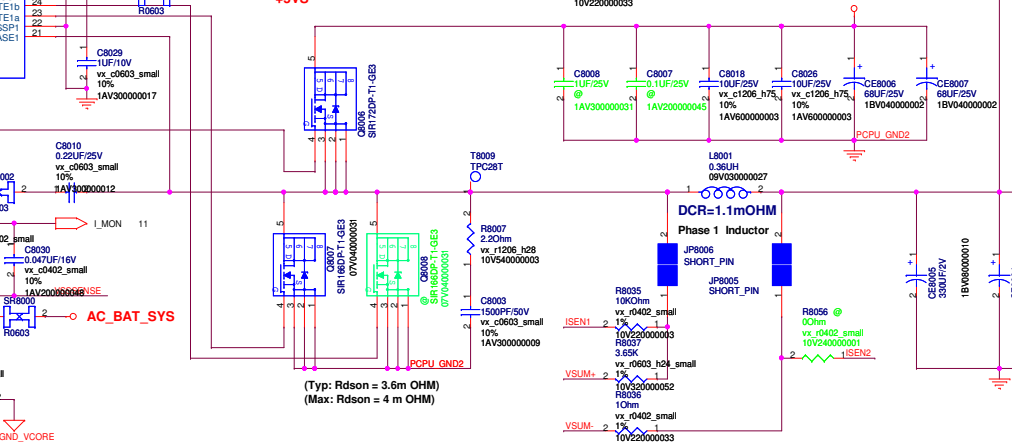
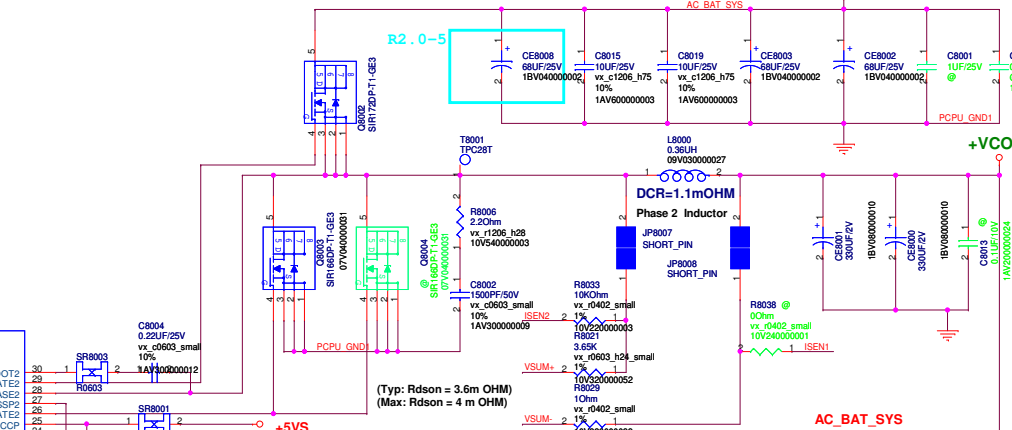
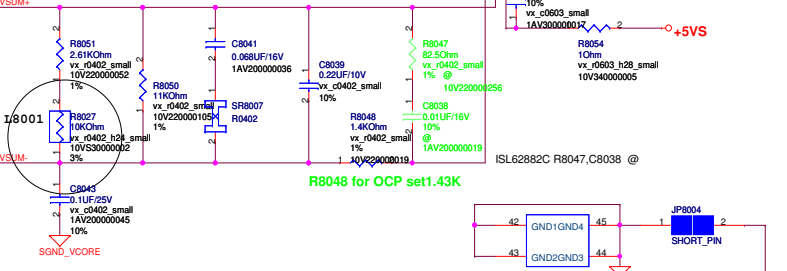
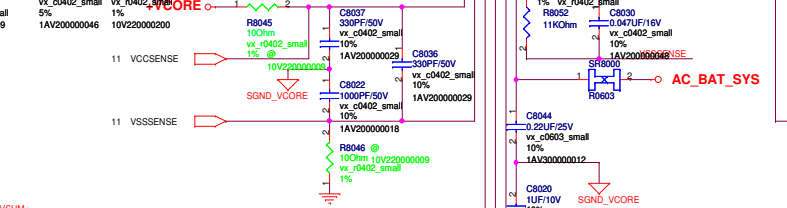
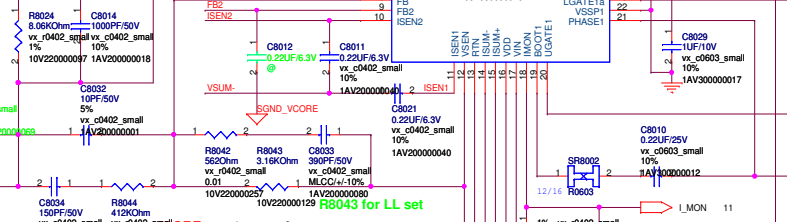
<b>PEGATRON</b>		Title : G-Sensor TSH35TR	
BU1-RD Div.1+HW RD Dept.1		Engineer: <i>Elmer Chiu</i>	
Size	Project Name	Rev	
Custom		2.0	
Date: Tuesday, May 03, 2011	Sheet	69	of 77



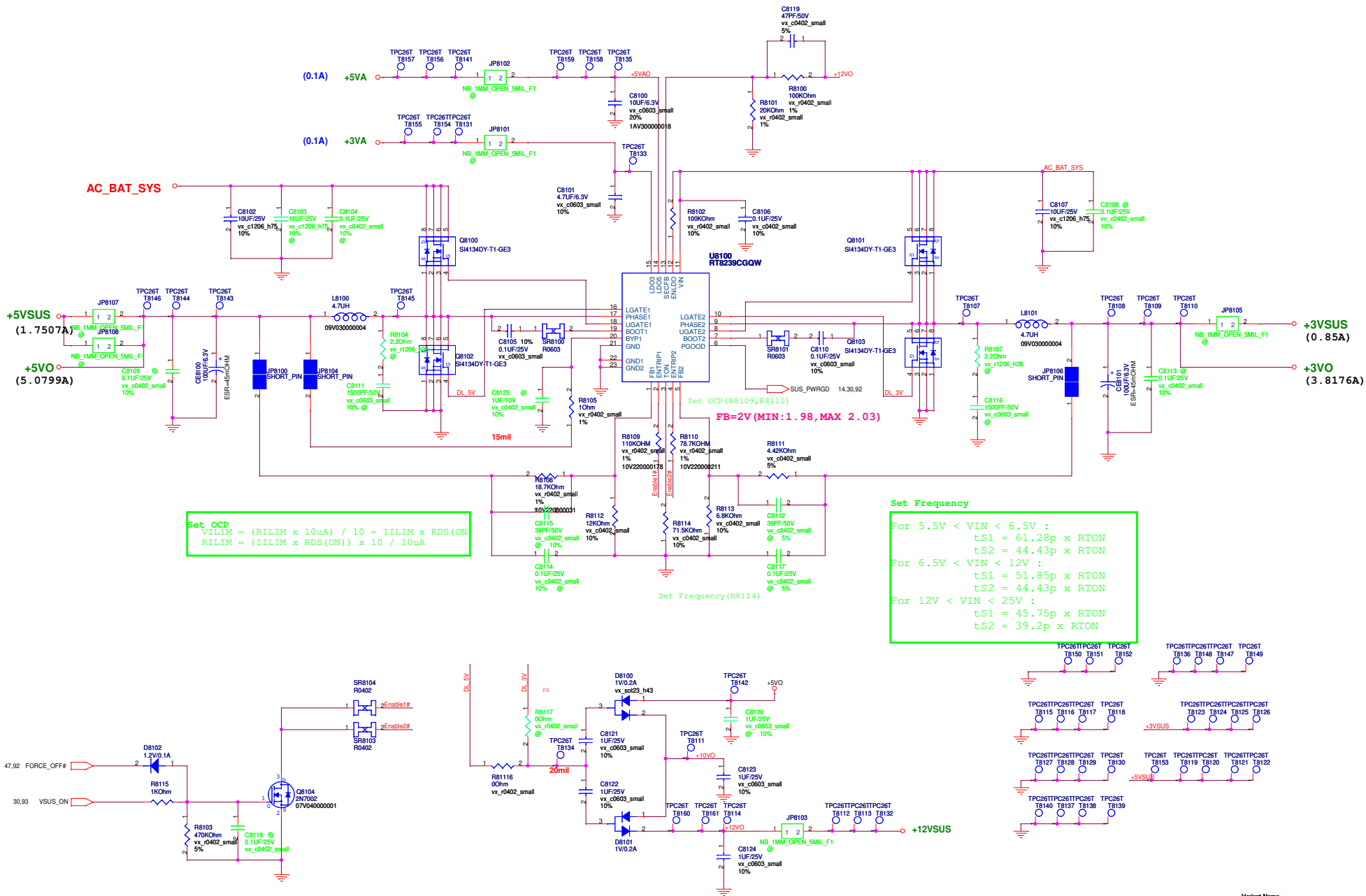


R8024=(Period(us)-0.29)\*2.65  
 Period(us)=1/300KHz  
 Adjust R8043 for  
 (Loadline = -1.9mV/A calpella SV)  
 R8025 Setting OCP

PM_DPRSPLVR	PM_PSI#	VO_action
L	L	1 Phase DE
H	L	1 Phase DE
L	H	2 Phase CCM
H	H	1 Phase DE



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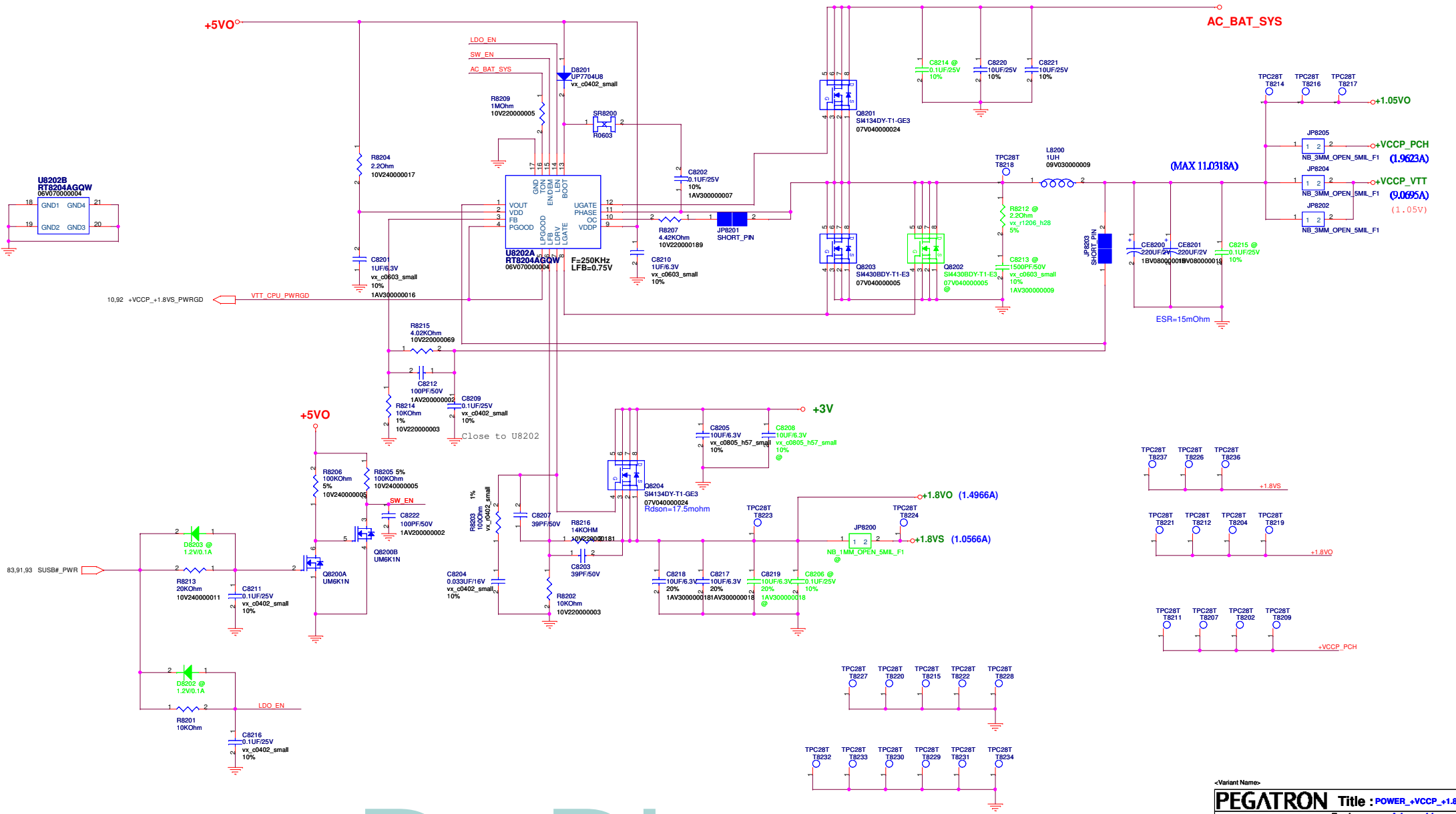
Set OCP  
 $V_{ILLIM} = (R_{ILIM} \times 10\mu A) / 10 = I_{ILIM} \times R_{DS(ON)}$   
 $R_{ILIM} = (I_{ILIM} \times R_{DS(ON)}) \times 10 / 10\mu A$

Set Frequency  
 For  $5.5V < V_{IN} < 6.5V$  :  
 $t_{S1} = 61.28p \times R_{TON}$   
 $t_{S2} = 44.43p \times R_{TON}$   
 For  $6.5V < V_{IN} < 12V$  :  
 $t_{S1} = 51.85p \times R_{TON}$   
 $t_{S2} = 44.43p \times R_{TON}$   
 For  $12V < V_{IN} < 25V$  :  
 $t_{S1} = 45.75p \times R_{TON}$   
 $t_{S2} = 39.2p \times R_{TON}$

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<Variant Name>

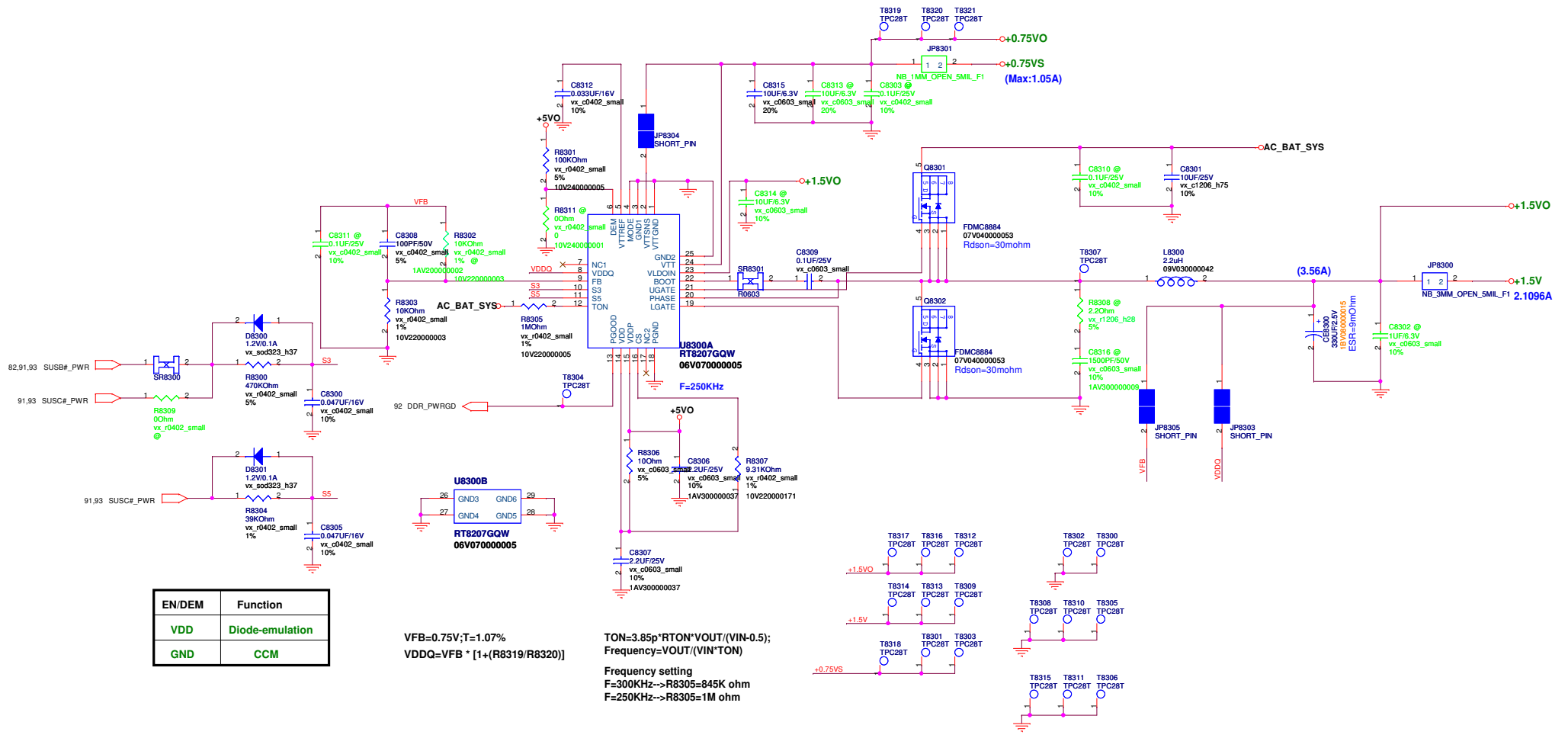
<b>PEGATRON</b> Title : <b>POWER_SYSTEM</b>	
Engineer: <b>Adams_Lin</b>	
Size	Project Name
Custom	<b>BIC50</b>
Date: <b>Tuesdkv, May 03, 2011</b>	Sheet <b>81</b> of <b>77</b>
Rev	1.0



<Variant Name>

<b>PEGATRON</b>		Title : POWER_+VCCP_+1.8VS	
		Engineer: Adams_Lin	
Size	Project Name		Rev
Custom	BIC50		1.0
Date:	Tuesday, May 03, 2011	Sheet	82 of 77

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EN/DEM	Function
VDD	Diode-emulation
GND	CCM

VFB=0.75V;T=1.07%  
VDDQ=VFB \* [1+(R8319/R8320)]

TON=3.85p\*RTON\*VOUT/(VIN-0.5);  
Frequency=VOUT/(VIN\*TON)

Frequency setting  
F=300KHz-->R8305=845K ohm  
F=250KHz-->R8305=1M ohm

-Variant Name-

**PEGATRON** Title : **POWER\_DDR & VTT**  
 Engineer: **Adams\_Lin**

Size	Project Name	Rev
Custom	<b>BIC50</b>	1.0

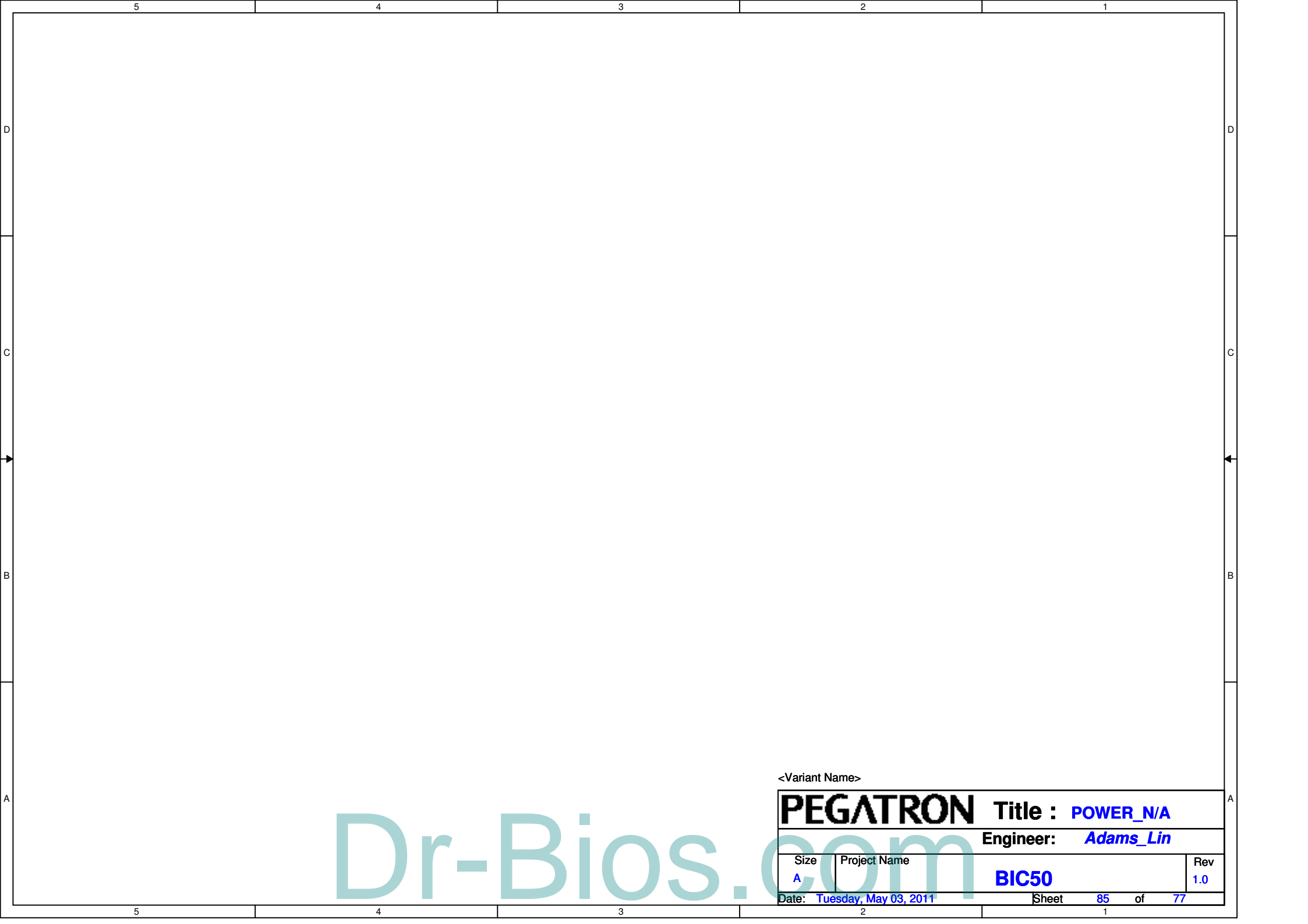
Date: Tuesday, May 03, 2011 Sheet 83 of 77



<Variant Name>

<b>PEGATRON</b>		Title : <b>POWER_N/A</b>	
		Engineer: <b>Adams_Lin</b>	
Size Custom	Project Name <b>BIC50</b>	Rev 1.0	
Date: <b>Tuesday, May 03, 2011</b>		Sheet	<b>84</b> of <b>77</b>

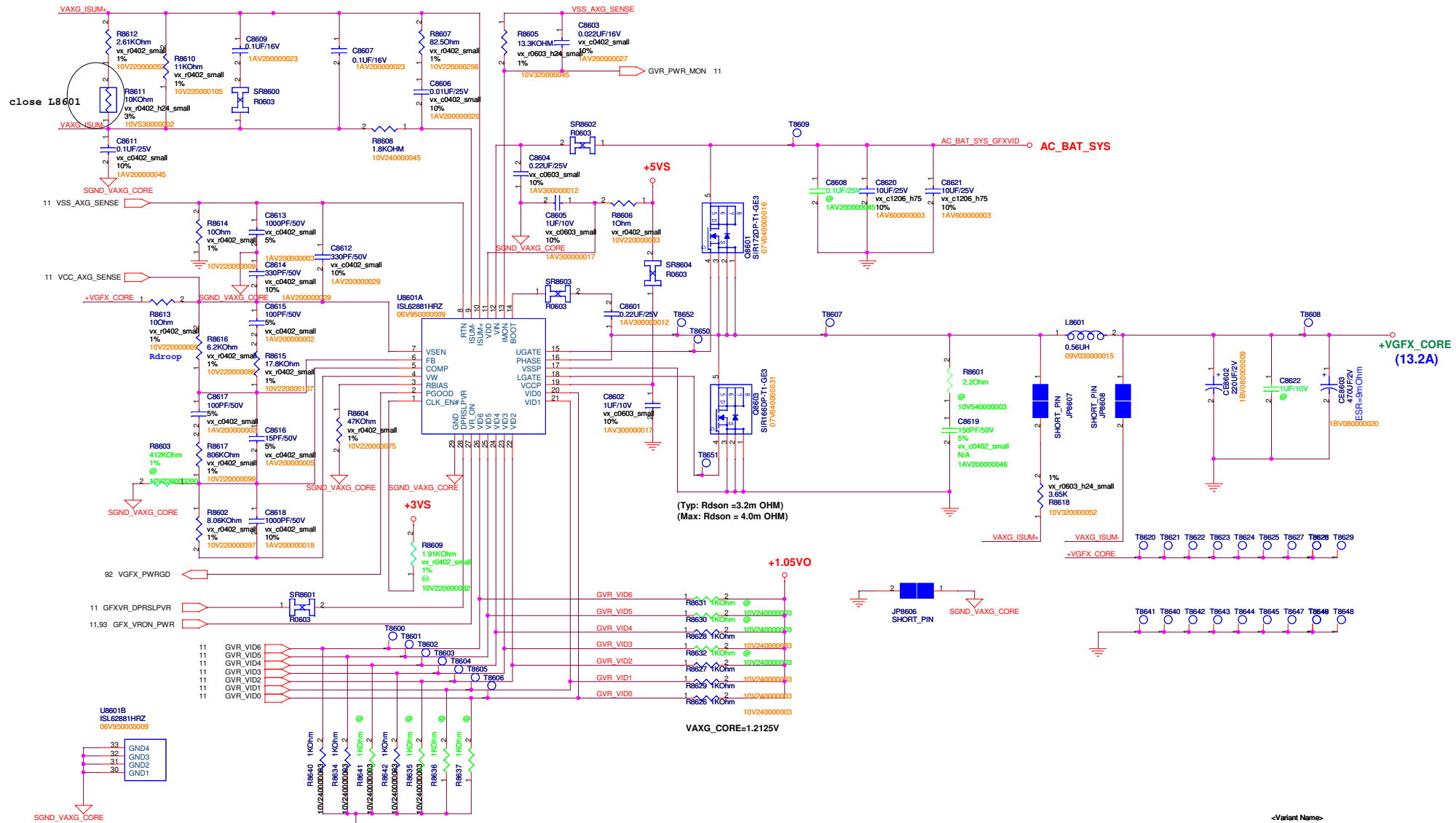
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<Variant Name>

<b>PEGATRON</b>		Title : <b>POWER_N/A</b>	
		Engineer: <b>Adams_Lin</b>	
Size	Project Name		Rev
<b>A</b>	<b>BIC50</b>		<b>1.0</b>
Date: <b>Tuesday, May 03, 2011</b>		Sheet	<b>85</b> of <b>77</b>

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<-Variant Name:>

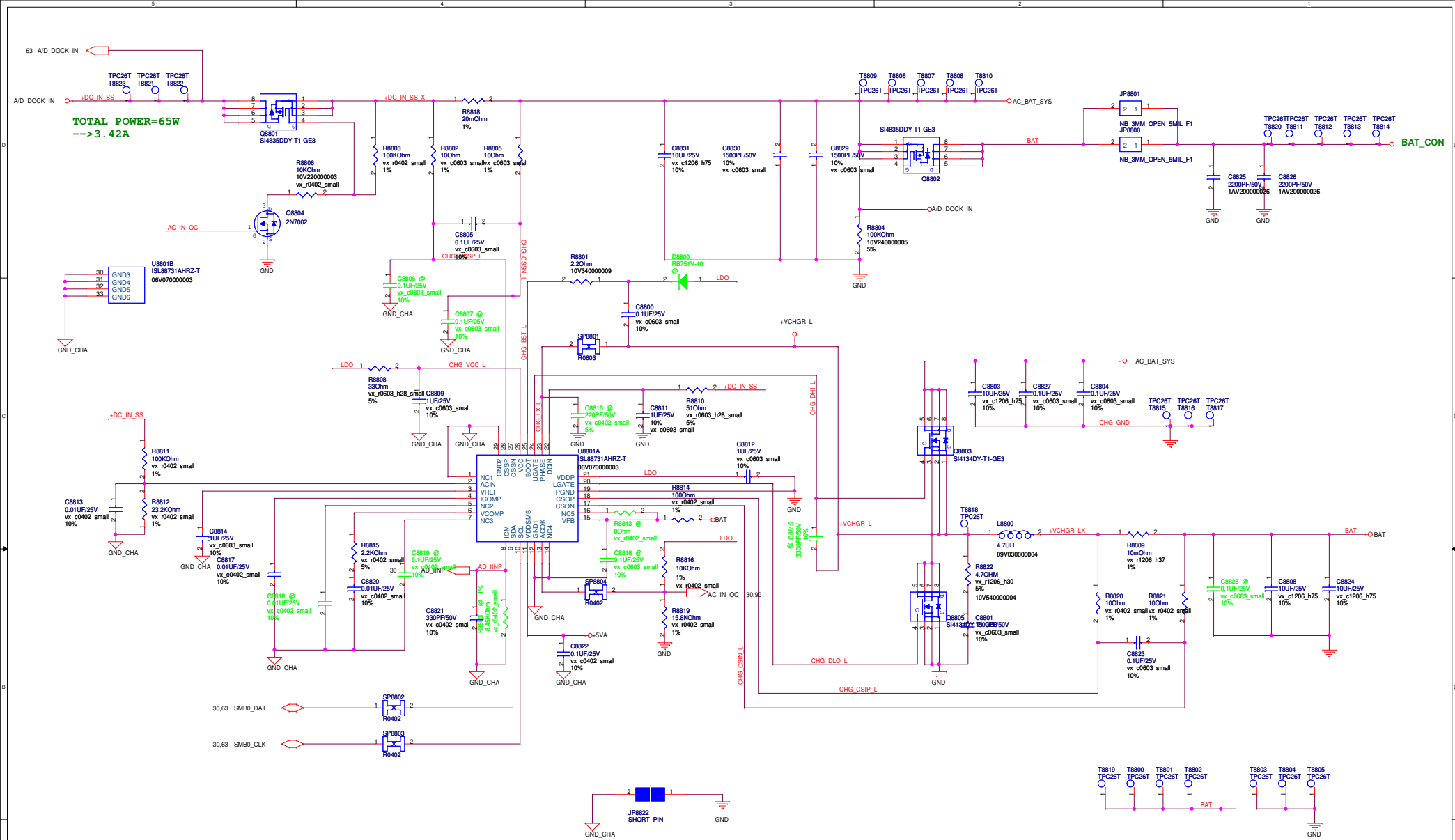
<b>PEGATRON</b>		Title : POWER_VGFX_CORE	
		Engineer: Adams_Lin	
Size	Project Name		Rev
Custom	BIC50		1.0
Date: Tuesday, May 03, 2011	Sheet	86	of 77



-<Variant Name>		
<b>PEGATRON</b>		Title : <b>POWER_*****</b>
		Engineer: <b>Adams Lin</b>
Size	Project Name	Rev
Custom	<b>BIC50</b>	1.0
Date: <b>Tuesday, May 03, 2011</b>		Sheet <b>87</b> of <b>77</b>

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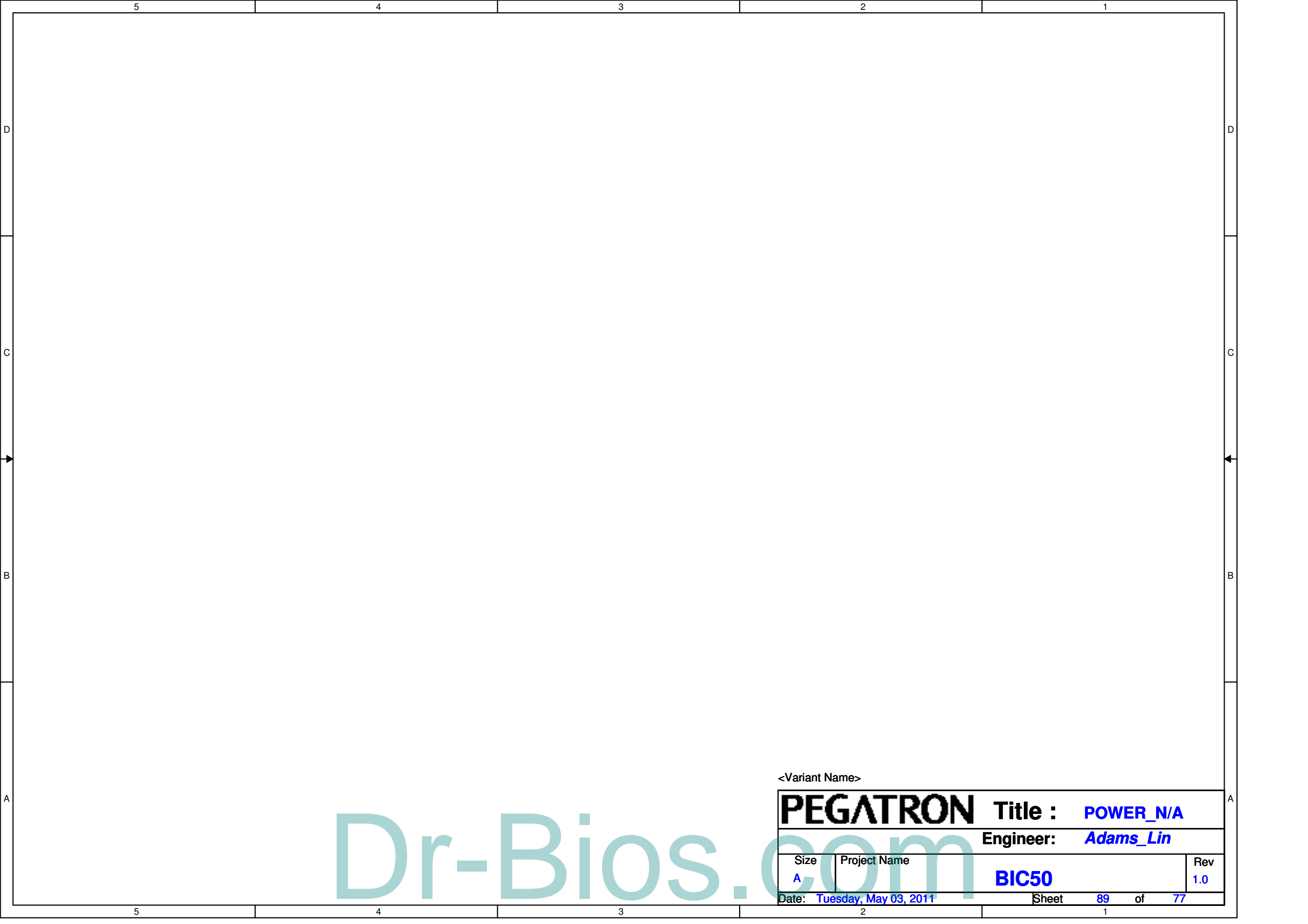




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<Variant Name>

PEGATRON Title POWER CHARGER		
Engineer: Adams Lin		
Size C	Project Name BIC50	Rev 1.0
Date: Tuesday, May 03, 2011	Sheet 88	of 77

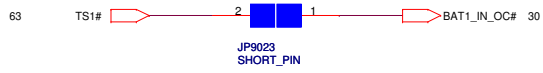


<Variant Name>

<b>PEGATRON</b>		<b>Title :</b>	<b>POWER_N/A</b>
		<b>Engineer:</b>	<b>Adams_Lin</b>
Size	Project Name		Rev
A	BIC50		1.0
Date: <b>Tuesday, May 03, 2011</b>		Sheet	89 of 77

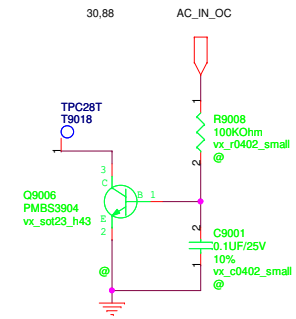
Dr-Bios.com

### BATTERY IN DETECT



### ADAPTER IN DETECT

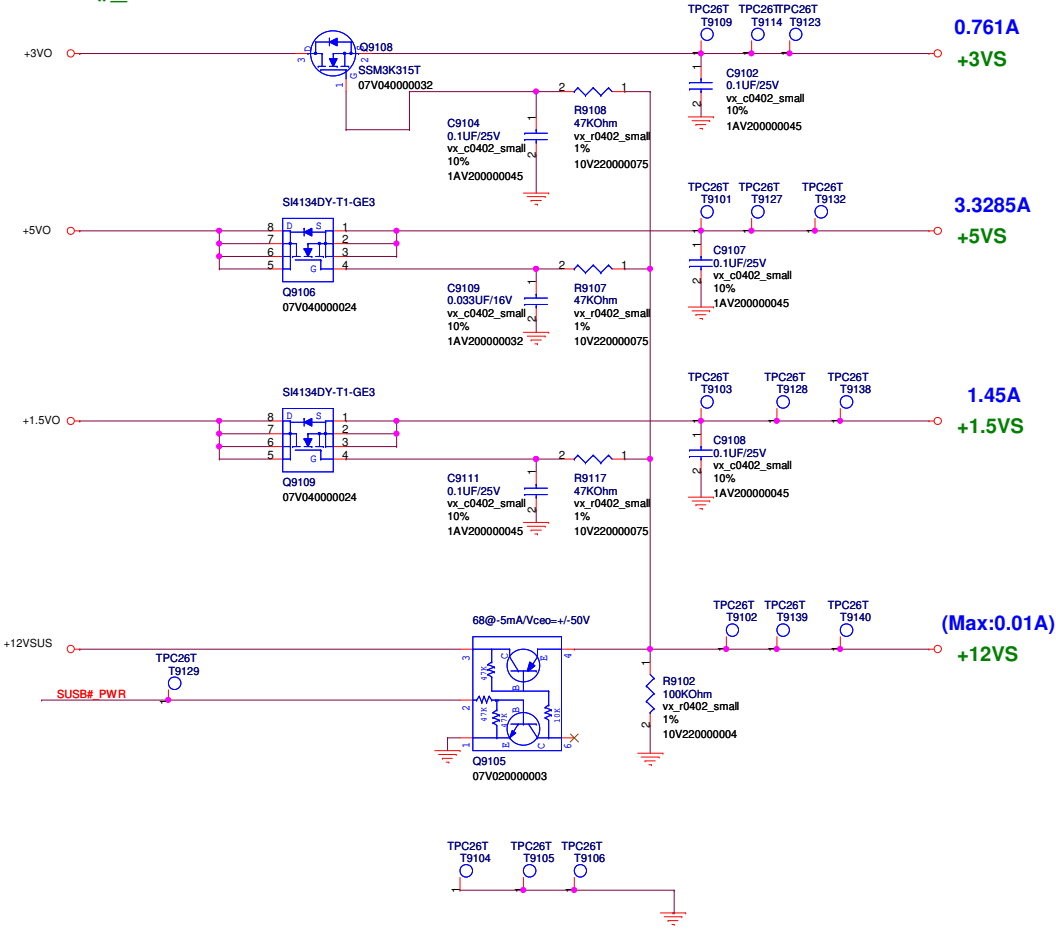
Use MAX17015 IC function to Cost down component



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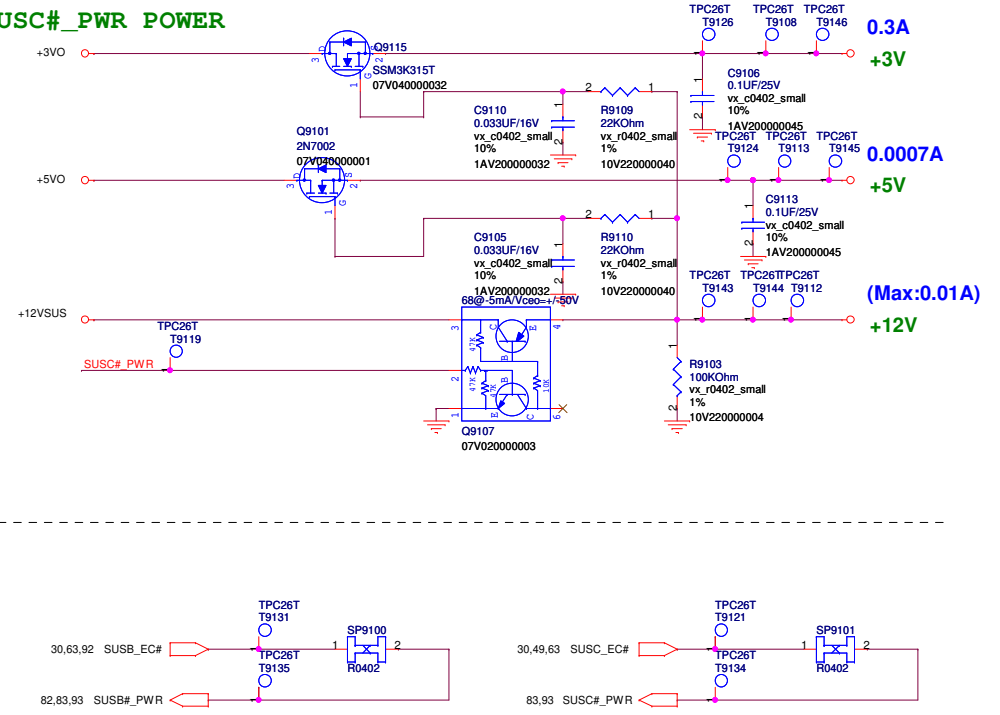
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<b>PEGATRON</b> Title : <b>POWER_DETECT</b>		Engineer: <b>Adams_Lin</b>
Size Custom	Project Name <b>BIC50</b>	Rev 1.0
Date: <b>Tuesday, May 03, 2011</b>	Sheet <b>90</b> of <b>77</b>	

SUSB#\_PWR POWER



Ron = 41.5 mΩ (max) (θVGS = 4.5 V)  
Ron = 27.6 mΩ (max) (θVGS = 10 V)

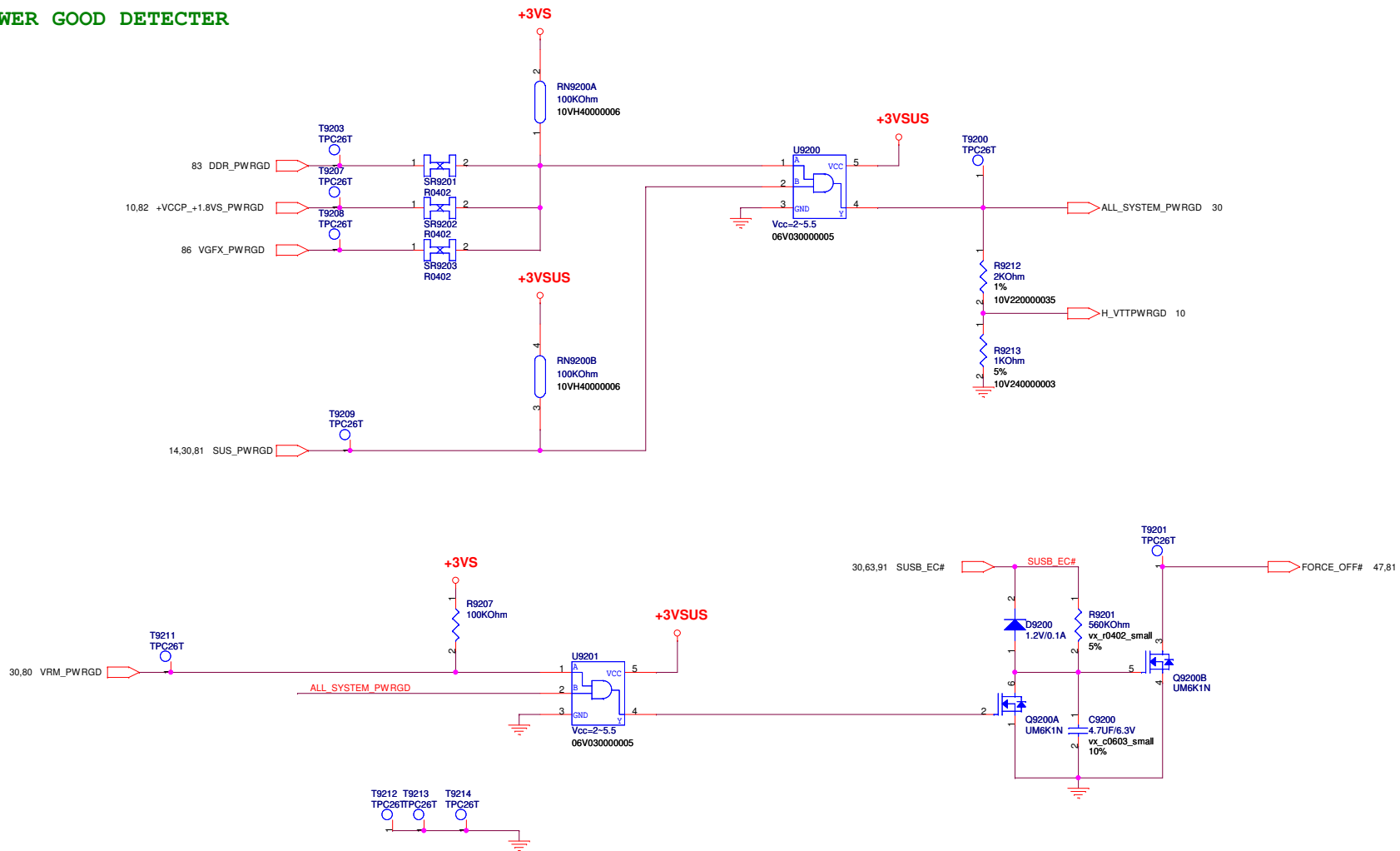
SUSC#\_PWR POWER



<Variant Name>

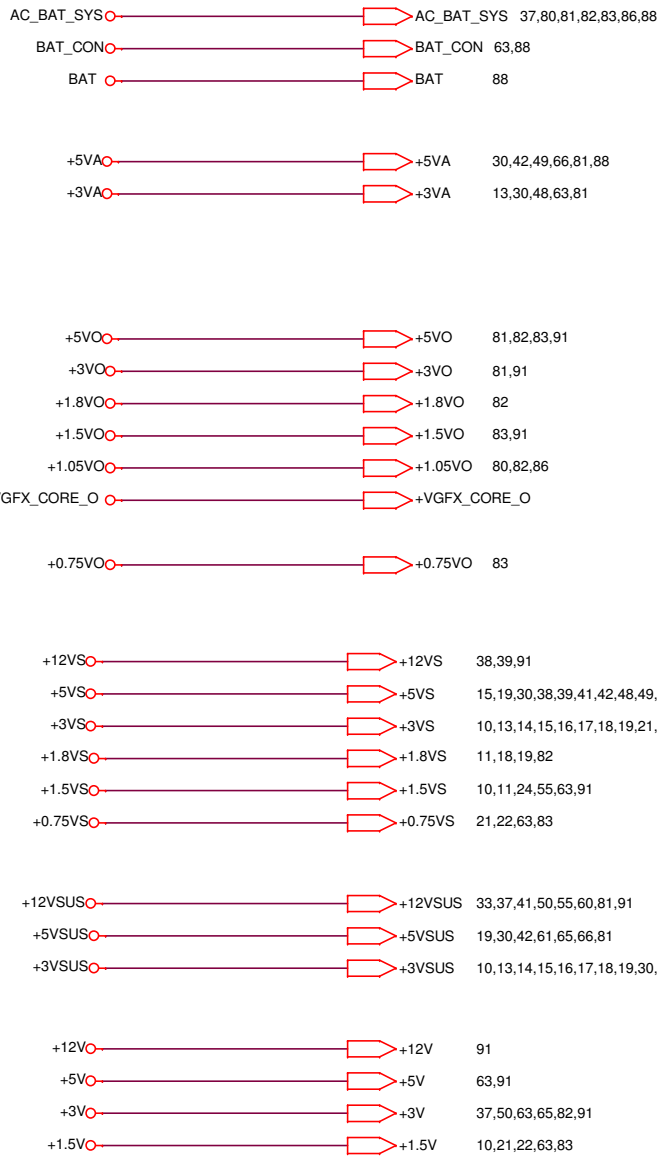
<b>PEGATRON</b> Title : POWER_LOAD SWITCH		
Engineer: <b>Adams_Lin</b>		
Size Custom	Project Name <b>BIC50</b>	Rev 1.0
Date: <b>Tuesday, May 03, 2011</b>	Sheet <b>91</b> of <b>77</b>	

# POWER GOOD DETECTOR

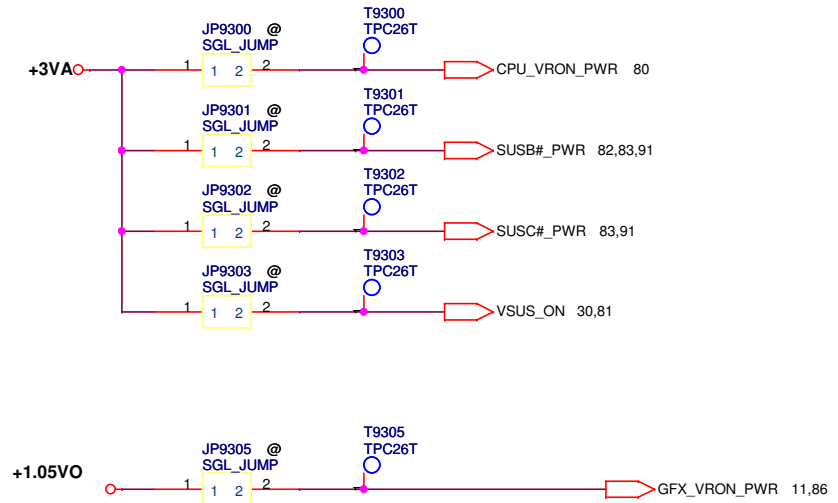


<Variant Name>

<b>PEGATRON</b> Title : <b>POWER_PROTECT</b>		
Engineer: <b>Adams_Lin</b>		
Size	Project Name	Rev
Custom	<b>BIC50</b>	1.0
Date: <b>Tuesday, May 03, 2011</b>	Sheet <b>92</b> of <b>77</b>	

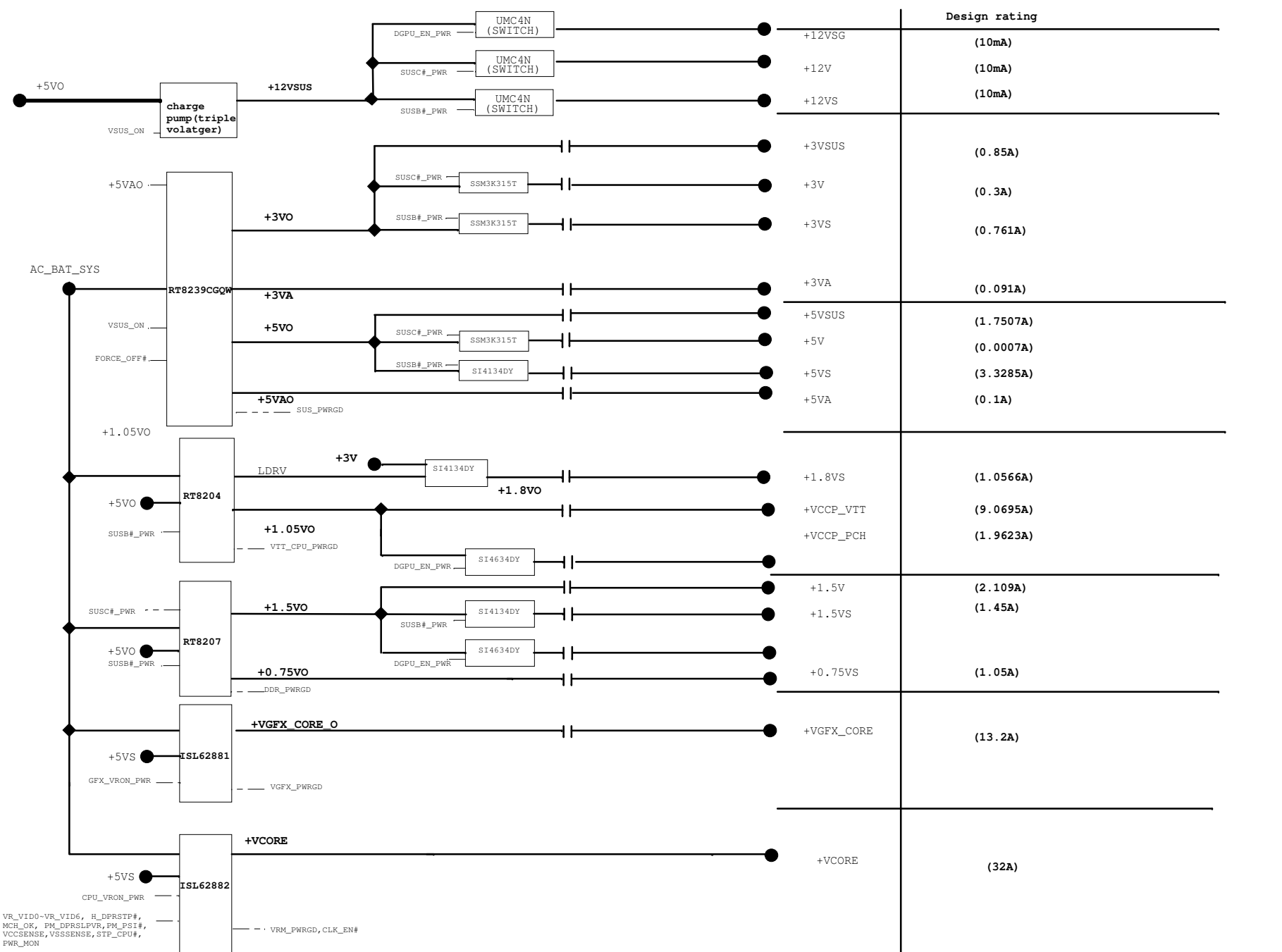


## FOR POWER TEST



<Variant Name>

<b>PEGATRON</b>		Title : <b>POWER_SIGNAL</b>	
		Engineer: <b>Adams_Lin</b>	
Size	Project Name	Rev	
Custom	<b>BIC50</b>	1.0	
Date: <b>Tuesday, May 03, 2011</b>		Sheet	93 of 77



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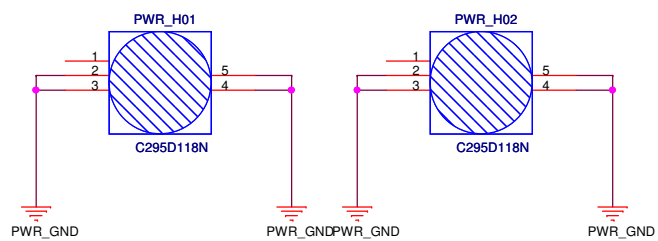
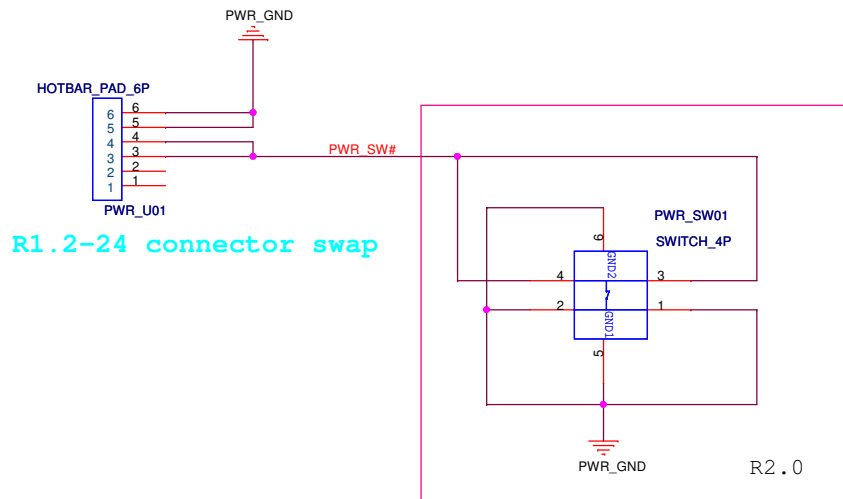
modify notice

Item	Date	Description	Item	Date	Description
SR-1	0120-11	P61, A04IO. change USB power switch circuit	SR-71	0128-11	P15. Add C1510 (22pF) for Clock fine-tune
SR-2	0120-11	Del P67, P68. Add P33, P34 for LAN	SR-72	0128-11	P33. change R3325, R3331 (4.7k ohm)
SR-3	0120-11	P48. change KB CON4801	SR-73	0128-11	P39. Un-mount R3907 (HDMI)
SR-4	0120-11	P34. change RJ45 CON3401	SR-74	0128-11	Change connector by list of 0128-11
SR-5	0120-11	P63. change BATT. con. circuit	SR-75	0129-11	Change HDD CON6001(1224-001N000)
SR-6	0120-11	P65, A02 change PWR LED CON6503 circuit	SR-76	0129-11	P97 (A02). Change Hotbar 6 Pad (PWR_U01)
SR-7	0120-11	P60. change HDD CON6001	SR-77	0129-11	P41~P50 Change VP part
SR-8	0121-11	P44, P45 Del Entry audio circuit (Full)	SR-78	0129-11	P55. Add Q5510, R5515 for BT PCI-E wake up event
SR-9	0121-11	P50. Del Entry SD socket circuit	SR-79	0130-11	P50. change footprint for U5001 Card reader controller
SR-10	0121-11	P77. Del B channel VRAM * 4 circuit	SR-80	0130-11	P66. change CPU*4, GPU*2, System screw hole*10
SR-11	0121-11	P46. Add EC GPIO35 DGPU_PWR_EN for Power	SR-81	0130-11	P46. change RN4601C (RN9202C)
SR-12	0121-11	P34, P35. Modify LAN AR8158 (Full)	SR-82	0130-11	P66. change F screw hole *2
SR-13	0123-11	P63. Change DC con. as VP part	SR-83	0130-11	P46. change SHORT PIN (R4601,R4602)
SR-14	0123-11	P60. Change HDD CON6001	SR-84	0130-11	P46, P65. change EC GPIO21 (PWR_AMBER_LED#) for PWR Brd.
SR-15	0123-11	P7~P37 Change VP part	SR-85	0130-11	Modify Sub board screw hole
SR-16	0124-11	P41 Del Entry speaker R4117~R4120	SR-86	0130-11	P34. Change RJ45 CON3401 1223-00BT000
SR-17	0124-11	P38~P39 Change VP part	SR-87	0131-11	P74. Change Q7401B(Q9203B)
SR-18	0124-11	P66 Remove LED circuit	SR-88	0131-11	P96, P99. Del Screw hole ODD_H02, change IOH3
SR-19	0124-11	P48. Reverse KB CON4801	SR-89	0131-11	P97. Change Power Board LED PWR_LED01
SR-20	0124-11	P71. Remove GPU Channel B dummy NET	SR-90	0131-11	P60. Change 15" ODD CON6505 as VP
SR-21	0124-11	P16, P61. Remove USB_9(HDMI)	SR-91	0131-11	P96~P99. Copy from AAB70 (sub board)
SR-22	0124-11	P48. Remove TP button circuit			
SR-23	0124-11	P13. Remove Entry AZ R1318, R1346, R1347, R1348, R1349	R1.2-1		P18 Add Bead and cap for CRT noise issue
SR-24	0124-11	P50. Modify CON5002 SD socket circuit	R1.2-2		P30 PWR_SW#_M 10kohm P/U to +3VA_EC
SR-25	0124-11	P48. Change KB CON4801 PIN definition	R1.2-3		P30 PWR_BLUE_LED# P/U to +5VSUS; BAT_ORG_LED# P/U to +5VA; CHG_LED_BLUE# P/U to +5VA to fix LED leakage issue
SR-26	0124-11	P16, P61. change USB power switch circuit	R1.2-4		P30 Reverse Q4602 for circuit design error
SR-27	0124-11	P41, P46. ALC271-SPKR_EC_ICH_Colay	R1.2-5		P37 add LCD_BACKOFF# for LCD on/off control by EC
SR-28	0124-11	P46, P65. Modify LED circuit and EC GPIO definition	R1.2-6		P41&P42&99 modify Int. MIC design from mono to stereo
SR-29	0125-11	P33 Remove LAN LED circuit	R1.2-7		P41 Reserve load switch to control PVDD on/off
SR-30	0125-11	P61 Modify D6101, RN6101, RN6105, RN6106	R1.2-8		P42 R3916 P/U to +5VSUS
SR-31	0125-11	P33 Change R3311 as VP	R1.2-9		P47 connect to EC_RST# for power protect
SR-32	0125-11	P33 Change U3301 to AR8158 and delete SM BUS	R1.2-10		P47,P49 Add Palm rest thermal circuit to follow thermal design spec
SR-33	0125-11	P34 Modify LAN ESD circuit	R1.2-11		P50 CON5002 pin.12 connect to GND to fix SD card can't be detected issue
SR-34	0125-11	P61. Modify Q6101	R1.2-12		P55 Reserve load switch to control +1.5VS_WLAN on/off
SR-35	0125-11	P65. Modify Q6501	R1.2-13		P60 Reserve connector for HDD connect by cable
SR-36	0125-11	P38, P46. Del F3801, C3811 Add CRT IN Detect	R1.2-14		P61 change Audio BD connector to 24 pin & reserve one more power switch for USB power test
SR-37	0125-11	P63. Reverse J6301	R1.2-15		P63 Change J6301 to 1217-00WC000 to fix SMT issue
SR-38	0125-11	P61, P46. change USB power switch and GPIO	R1.2-16		P66 H6546 floating by EMI request
SR-39	0125-11	P46,P66. change LED power and Net name	R1.2-17		P66 delete screw hole H6545
SR-40	0125-11	P34. Modify Transformer circuit	R1.2-18		P98 TP_H1 & TP_H2 change P/N by ME request
SR-41	0125-11	P33. Modify H/W strap setting	R1.2-19		P98 TP_SW1 & TP_SW2 change to 1209-00VF000 by ME request
SR-42	0125-11	P37. Modify LVDS PIN definition	R1.2-20		P98 TP_H1 & TP_H2 change P/N by ME request
SR-43	0125-11	P42. Modify De-Pop circuit	R1.2-21		P61 L6105 change to 67 ohm common choke to fix USB eye-diagram fail issue
SR-44	0125-11	P41. Modify Audio Pin 14, 15, 27~31	R1.2-22		P48 Add cap for K/B signal by EMI request
SR-45	0126-11	P34. Modify Transformer circuit	R1.2-23		P48 Add C3013 by EMI request
SR-46	0126-11	P16. GPIO54 DGPU_PWR_EN	R1.2-24		P97 hotbar pin define swap to meet cable define
SR-47	0126-11	U1301, U7001 keypad no; U4602, F6302 Modify for BOM	R1.2-25		P33 unmount R3306, mount R3308 for LAN OPT mode
SR-48	0126-11	P34. Modify Transformer circuit	R1.2-26		P33 L3317 change to 1500ohm Bead by EMI request
SR-49	0126-11	P63, P60, P17, P48. Add 15" circuit BATT, ODD, Keyboard	R1.2-27		P38 L3801,L3802,L3803 change to 0.056uH inductor for EMI & EA test
SR-50	0126-11	P13, P60 Rename SATA 0 to SATA 1	R1.2-28		P65 unmount R6507&Q6501 and delet PWR_SW BD LED circuit
SR-51	0126-11	P63. Reverse DC-IN J6301 PIN1 as GND	R2.0-1		P42 change OP_SD# to +5VA power rail to prevent DC mode has noise when shutdown (follow eih30)
SR-52	0126-11	P48. Reverse KB CON4801	R2.0-2		P30 remove EC xtal, EC clock control by EC itself.
SR-53	0126-11	DGPU Sync with EIH31	R2.0-3		P49 change R4903 to 4.22Kohm to set thermistor operating temp at 89'C (request by thermal RD)
SR-54	0126-11	P.76. T7, M7 Setting	R2.0-4		P66 change H6541,H6538,H6553,H6552,H6547,H6544 to NPTH hole for factory ICT test purpose
SR-55	0126-11	Modify as OPT display output	R2.0-5		P80 Add CER008 to fix electrical noise over 15msones issue
SR-56	0127-11	P.76. Cancel T7, M7 Setting			
SR-57	0127-11	P.46, P50 Modify single net			
SR-58	0127-11	P.42 Change R4205, R4206 = 51 ohm			
SR-59	0127-11	P.41 DEL C4109, C4112			
SR-60	0127-11	P.14 R1403, R1404 option N/A			
SR-61	0127-11	P.14 R1443, R1444, RN1402, R1424, R1426, R1427, R1428 option N/A; R1429 option /HDMI_HPD_PCH			
SR-62	0127-11	P71, P74. R7101, R7103, R7435, R7437 option @			
SR-63	0127-11	P74. Del R7433, R7434, GPIO Test Pad			
SR-64	0128-11	P34. U3403.4 RXN			
SR-65	0128-11	P66. change R6603.1 (+5VA), LED6602, LED6603			
SR-66	0128-11	P65. change R6508.1 (PWRLED_ON#), CON6503.6 (+5VSUS)			
SR-67	0128-11	P97. Modify A04 Pwr Board			
SR-68	0128-11	P55. Un-mount Q5505, R5510			
SR-69	0128-11	P66. Modify Screw Hole (Sync with AAB70)			
SR-70	0128-11	P63. Modify Battery CON6302, D6302 signal name			



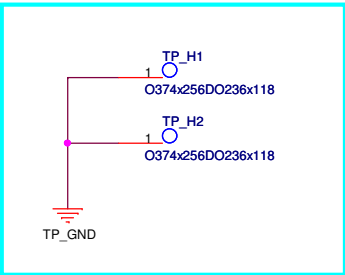


**POWER LED 0129**

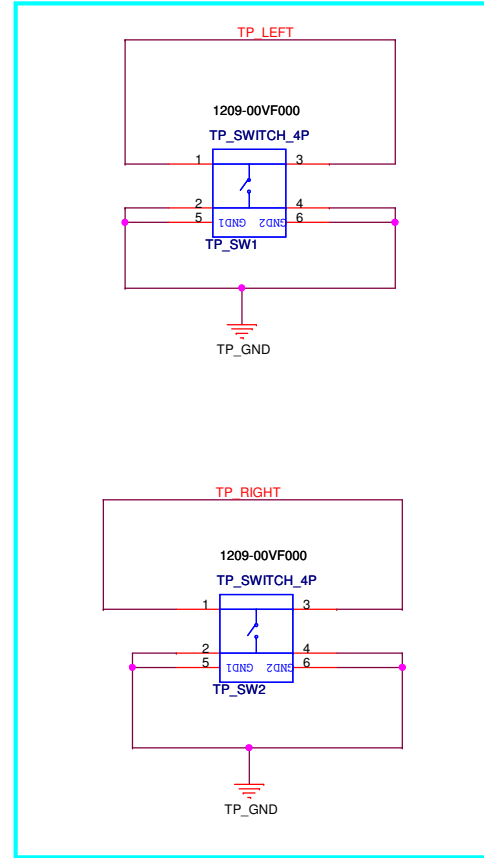
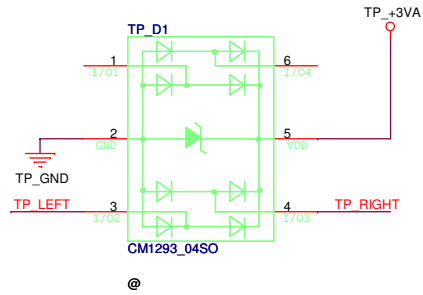


- PWR\_H03  
1 ○  
C102D102N
- PWR\_H4  
1 ○  
C102D102N
- SR-85

<b>PEGATRON</b> Title : <b>PWR BTN</b>	
BU1-RD Div.1-HW RD Dept.1 Engineer: <b>Elmer Chiu</b>	
Size B	Project Name <b>BIC50</b>
Date: <b>Tuesday, May 03, 2011</b>	Rev 1.1
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R1.2-18

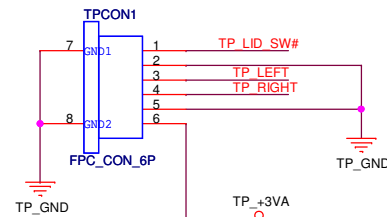
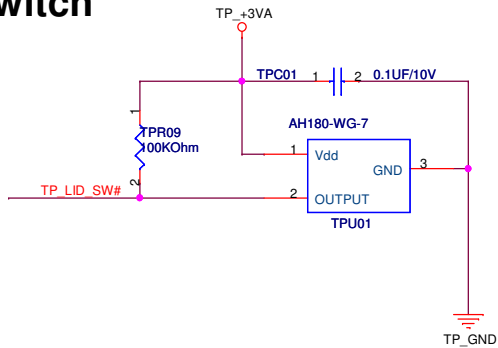


R1.2-19



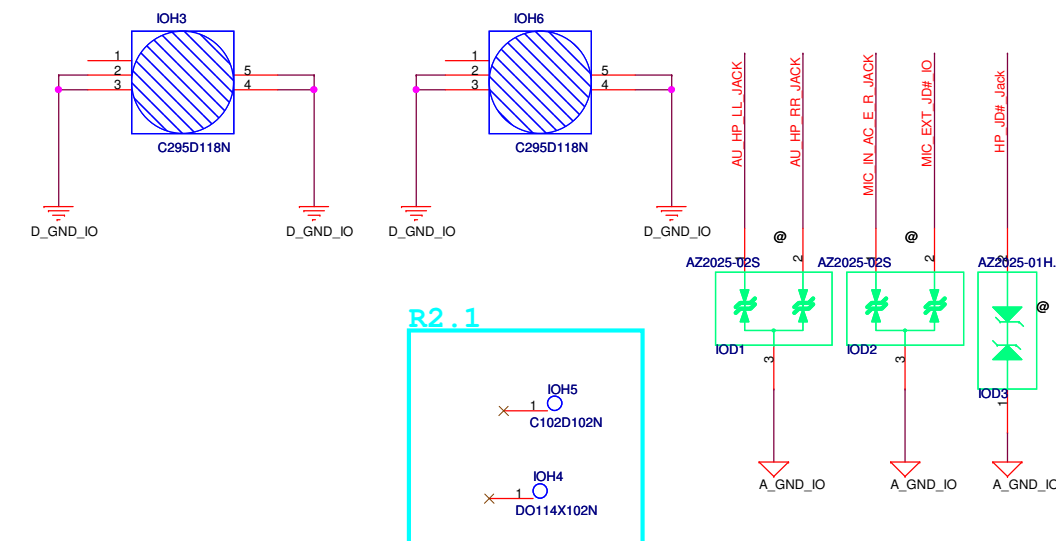
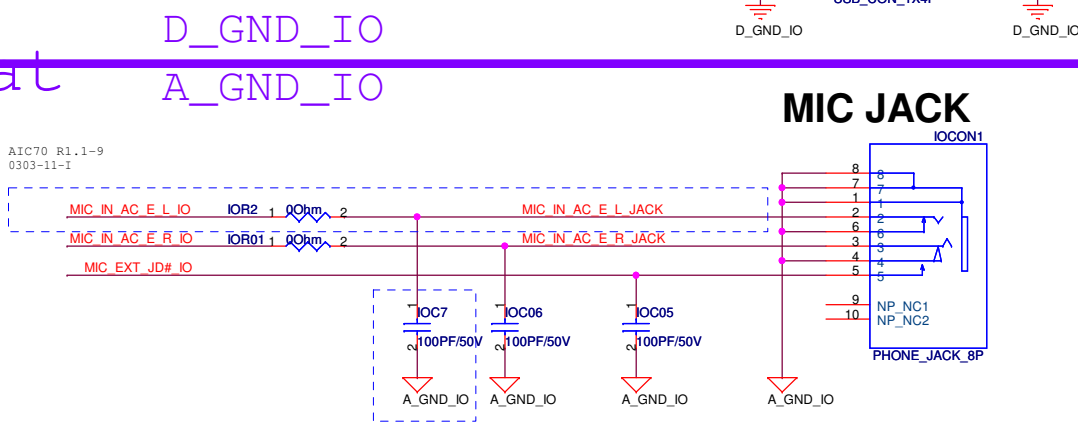
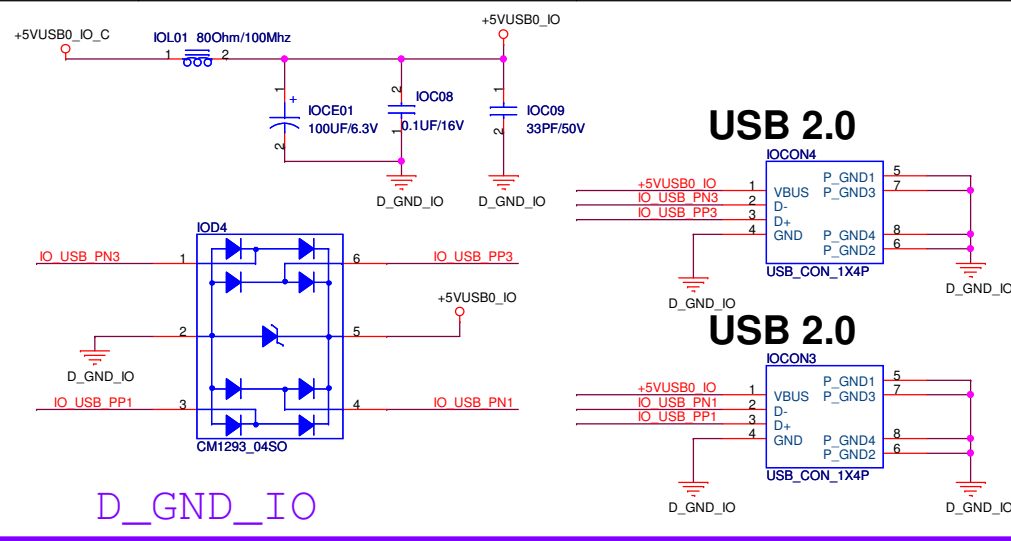
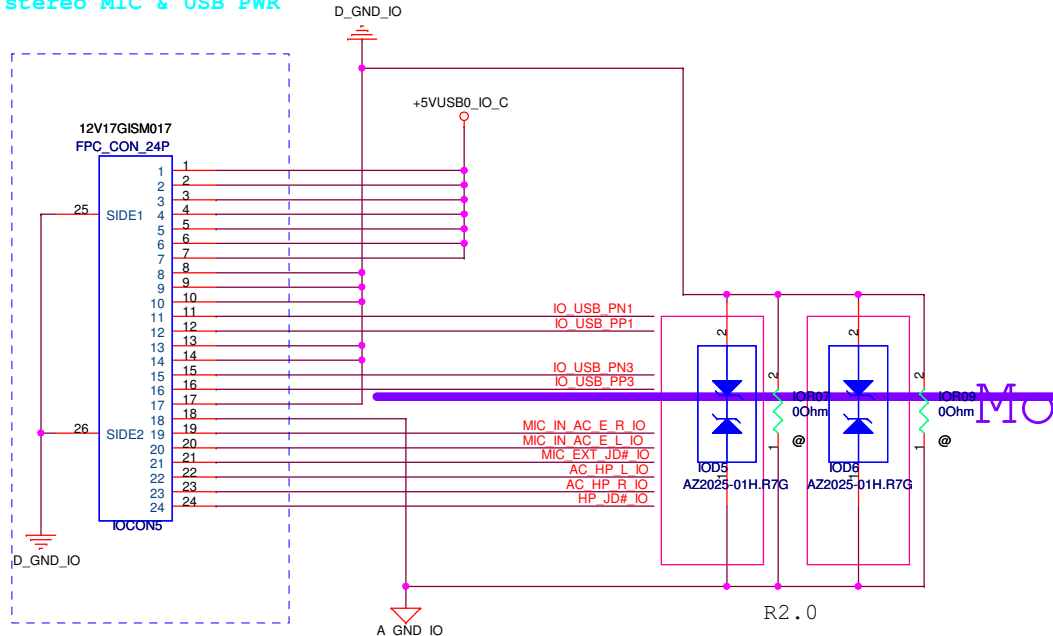
SR-85

### LID Switch



<b>PEGATRON</b> Title :TP_M		
BG1-HW RD Div.2-NB RD Dept.5 Engineer: Elmer Chiu		
Size B	Project Name BIC50	Rev 1.0
Date: Tuesday, May 03, 2011	Sheet 98	of 77

**R1.2-6**  
Change Connector for stereo MIC & USB PWR



<b>PEGATRON</b> Title : 0		
BG1-NB1-HW-NB5		Engineer: Elmer Chiu
Size B	Project Name <b>BIC50</b>	Rev 1.0
Date: Wednesday, May 11, 2011	Sheet 99	of 77