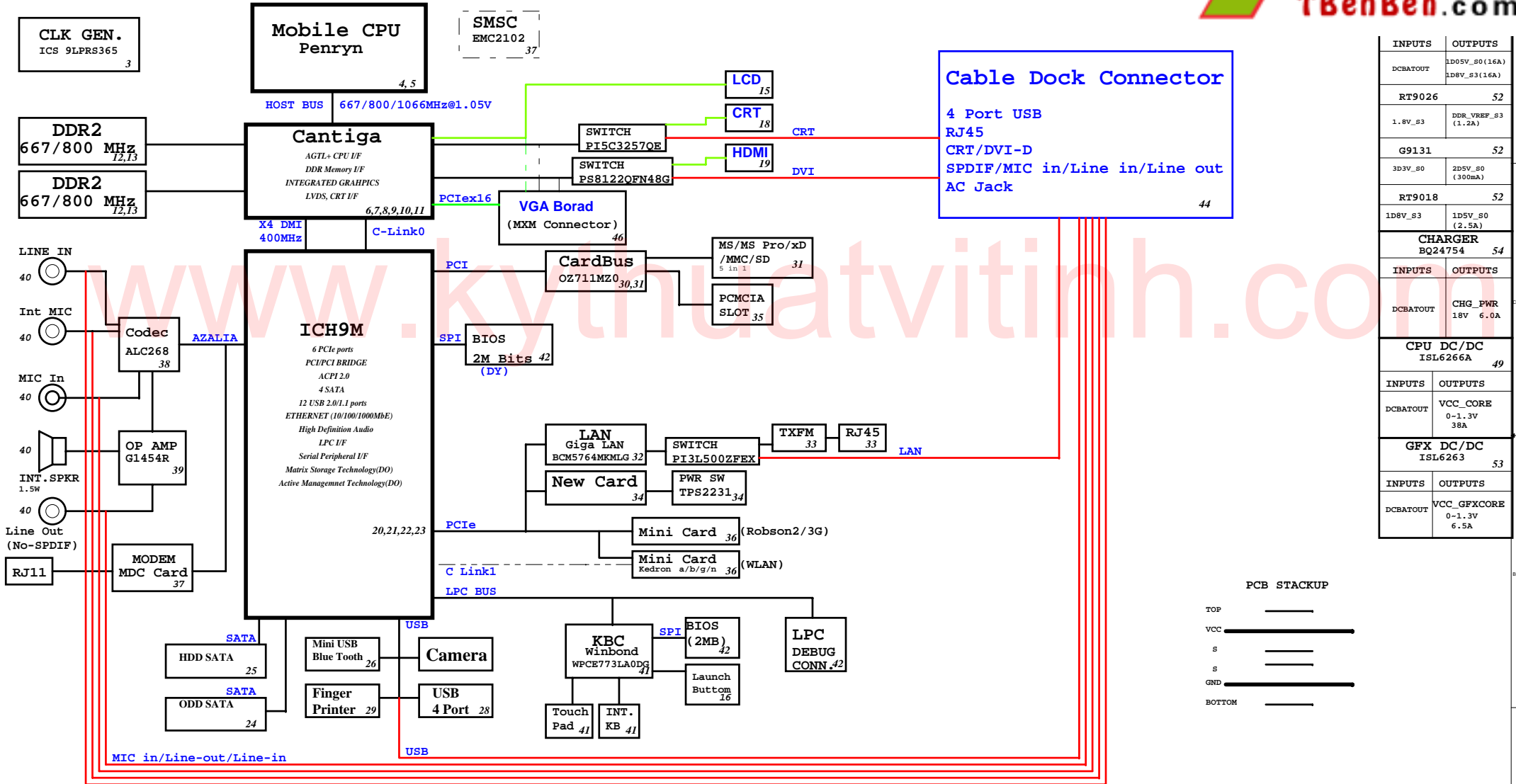
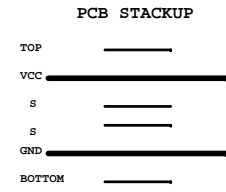


HOMA 3G Block Diagram

Project co
PCB P/N
REVISION



INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 (16A) 1D8V_S3 (16A)
RT9026	52
1.8V_S3	DDR_VREF_S3 (1.2A)
G9131	52
3D3V_S0	2D5V_S0 (300mA)
RT9018	52
1D8V_S3	1D5V_S0 (2.5A)
CHARGER BQ24754	
54	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 1.8V 6.0A
CPU DC/DC ISL6266A	
49	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0-1.3V 38A
GFX DC/DC ISL6263	
53	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE 0-1.3V 6.5A



ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIe Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIe config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/GPIO53	PCIe config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#:SPI_CS1#/GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resistor.

ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSPLVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native LAN DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5 page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) 1=The iTPM Host Interface is disabled(default)
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (default)
CFG9	PCIe Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG10	PCIe Loopback enable	0 = Enable (Note 3) 1= Disabled (default)
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) 11 = Disabled (default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation(Default): Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3 DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/IHDMI) Concurrent with PCIe	0 = Only Digital Display Port or PCIe is operational (Default) 1 = Digital display Port and PCIe are operating simultaneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 =No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1= LFP Card Present; PCIe disabled

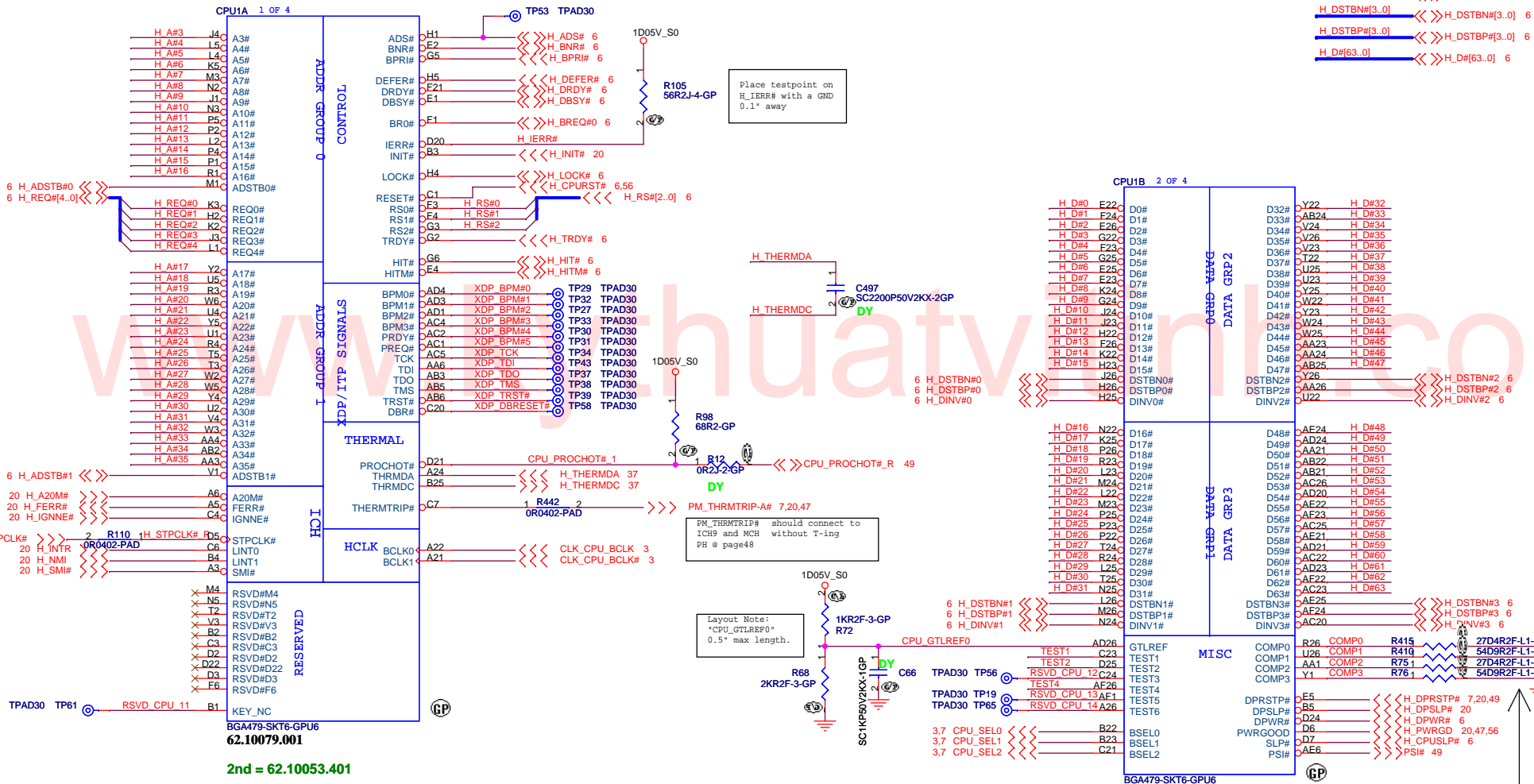
NOTE:

- All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
- iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6. Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Reference			
Title	Document Number		Rev
	HOMA 3G		-1
Date:	Friday, May 30, 2008	Sheet	2 of 56

6 H_A#(35..3) <<<>> H_A#(35..3)

H_DIN#(3..0) <<>> H_DIN#(3..0) 6
H_DSTBN#(3..0) <<>> H_DSTBN#(3..0) 6
H_DSTBP#(3..0) <<>> H_DSTBP#(3..0) 6
H_D#(63..0) <<>> H_D#(63..0) 6



Place testpoint on H_IERR# with a GND 0.1" away

PM_THRMTRIP-A# 7.20,47
PM_THRMTRIP# should connect to ICH9 and MCH without T-ing PH @ page48

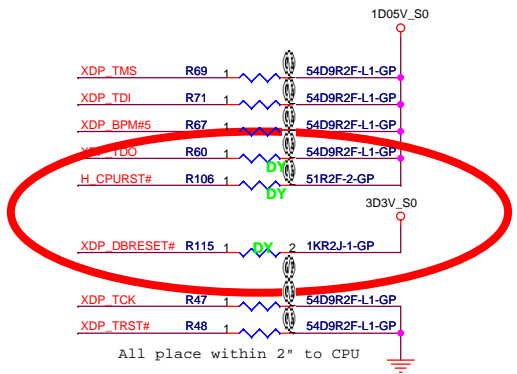
Layout Note:
"CPU_GTLREF0"
0.5" max length.

Layout Note:
Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5"
Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5"

Net "TEST4" as short as possible, make sure "TEST4" routing is reference to GND and away other noisy signals

H DPRSTP# TP55 TPAD30
 H DPSLP# TP63 TPAD30
 H DPWR# TP79 TPAD30
 H PWRGD TP81 TPAD30
 H CPUSLP# TP78 TPAD30
 H INIT# TP60 TPAD30
 H CPURST# TP57 TPAD30

Place these TP on button-side, easy to measure.

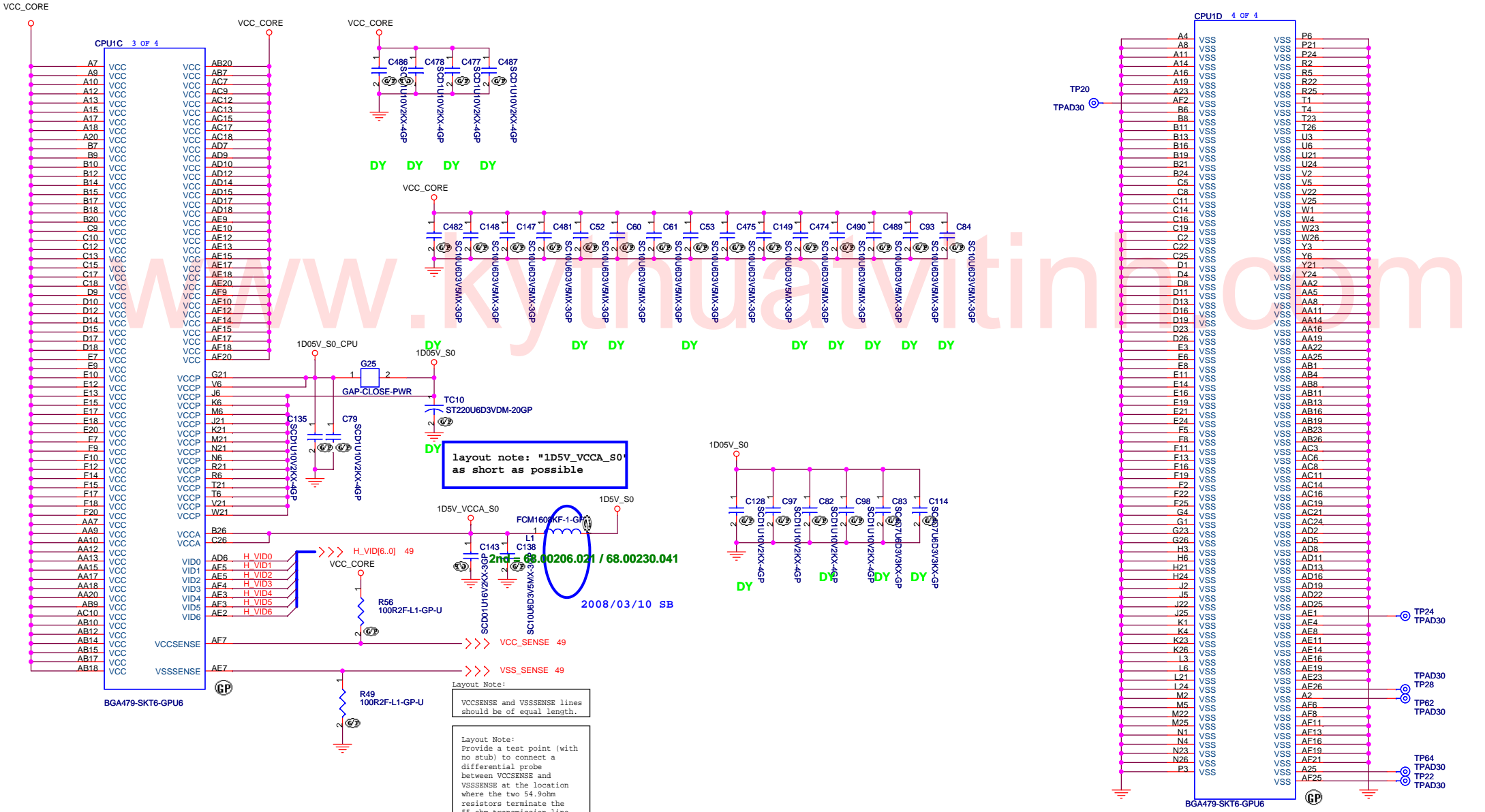


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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

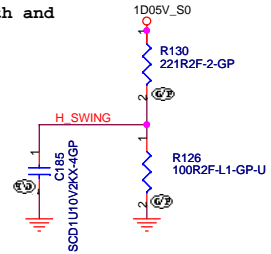
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Size: Document Number: Rev: -1

Date: Friday, May 30, 2008 Page: 4 of 56

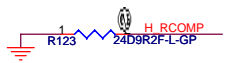


H_SWING routing Trace width and Spacing use 10 / 20 mil

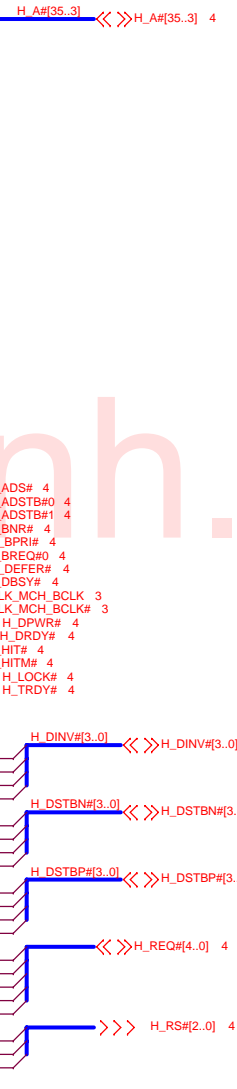
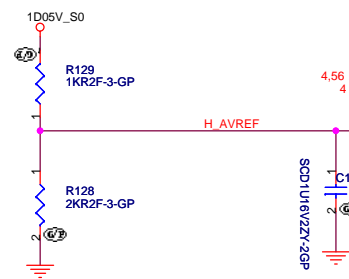


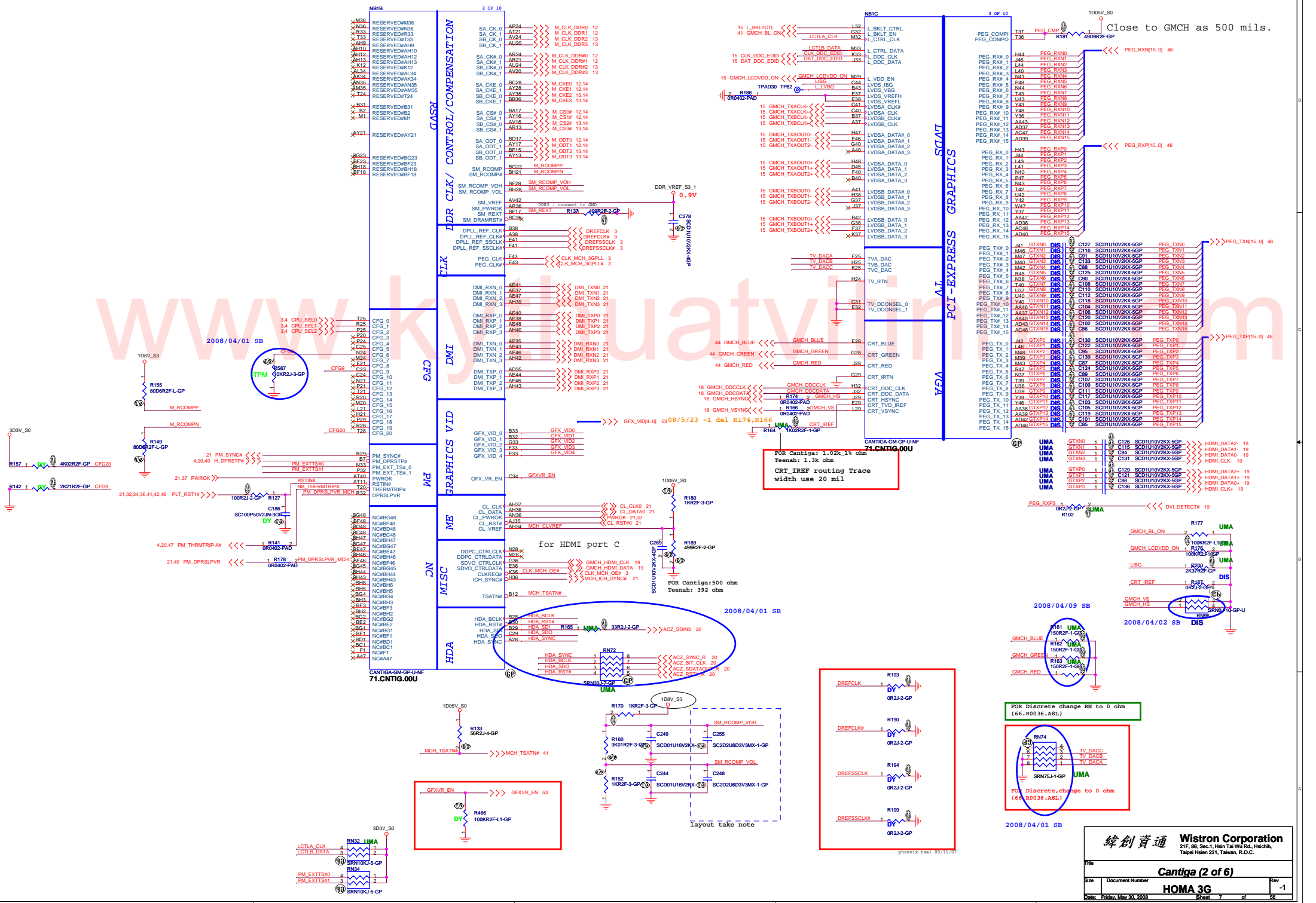
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)

H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")





Close to GMCH as 500 mils.

FOR Cantiga: 1.02k_19 ohm
 CRT_IREF routing Trace width use 20 mil

FOR Discrete change R1 to 0 ohm
 (66.R0036.ABL)

FOR Discrete, change to 0 ohm
 (66.R0036.ABL)

12 M_A_DQ[63.0] <<< M_A_DQ[63.0]

M A DQ0	AJ38	SA_DQ_0
M A DQ1	AJ41	SA_DQ_1
M A DQ2	AN38	SA_DQ_2
M A DQ3	AJ36	SA_DQ_3
M A DQ4	AJ40	SA_DQ_4
M A DQ5	AM44	SA_DQ_5
M A DQ6	AM42	SA_DQ_6
M A DQ7	AN43	SA_DQ_7
M A DQ8	AN44	SA_DQ_8
M A DQ9	AJ40	SA_DQ_9
M A DQ10	AT38	SA_DQ_10
M A DQ11	AN41	SA_DQ_11
M A DQ12	AN39	SA_DQ_12
M A DQ13	AJ44	SA_DQ_13
M A DQ14	AJ42	SA_DQ_14
M A DQ15	AV39	SA_DQ_15
M A DQ16	BA40	SA_DQ_16
M A DQ17	BD43	SA_DQ_17
M A DQ18	AV41	SA_DQ_18
M A DQ19	AV43	SA_DQ_19
M A DQ20	BC41	SA_DQ_20
M A DQ21	BC40	SA_DQ_21
M A DQ22	AY37	SA_DQ_22
M A DQ23	BD38	SA_DQ_23
M A DQ24	AV37	SA_DQ_24
M A DQ25	AT36	SA_DQ_25
M A DQ26	AY38	SA_DQ_26
M A DQ27	BC39	SA_DQ_27
M A DQ28	AV36	SA_DQ_28
M A DQ29	AW36	SA_DQ_29
M A DQ30	BD13	SA_DQ_30
M A DQ31	AU11	SA_DQ_31
M A DQ32	BC11	SA_DQ_32
M A DQ33	BA12	SA_DQ_33
M A DQ34	AU13	SA_DQ_34
M A DQ35	AV13	SA_DQ_35
M A DQ36	BD12	SA_DQ_36
M A DQ37	BC12	SA_DQ_37
M A DQ38	BA9	SA_DQ_38
M A DQ39	AU10	SA_DQ_39
M A DQ40	AV9	SA_DQ_40
M A DQ41	BA11	SA_DQ_41
M A DQ42	BD9	SA_DQ_42
M A DQ43	AY8	SA_DQ_43
M A DQ44	BA6	SA_DQ_44
M A DQ45	AV5	SA_DQ_45
M A DQ46	AV7	SA_DQ_46
M A DQ47	AT9	SA_DQ_47
M A DQ48	AN8	SA_DQ_48
M A DQ49	AU5	SA_DQ_49
M A DQ50	AU6	SA_DQ_50
M A DQ51	AT5	SA_DQ_51
M A DQ52	AN10	SA_DQ_52
M A DQ53	AM11	SA_DQ_53
M A DQ54	AM5	SA_DQ_54
M A DQ55	AJ9	SA_DQ_55
M A DQ56	AJ8	SA_DQ_56
M A DQ57	AN12	SA_DQ_57
M A DQ58	AM13	SA_DQ_58
M A DQ59	AJ11	SA_DQ_59
M A DQ60	AJ12	SA_DQ_60
M A DQ61		SA_DQ_61
M A DQ62		SA_DQ_62
M A DQ63		SA_DQ_63

NB1D 4 OF 10

SA_BS_0	BD21	M A_BS#0 12,14
SA_BS_1	BG18	M A_BS#1 12,14
SA_BS_2	AT25	M A_BS#2 12,14
SA_RAS#	BB20	M A_RAS# 12,14
SA_CAS#	BD20	M A_CAS# 12,14
SA_WE#	AY20	M A_WE# 12,14
SA_DM_0	AM37	M A_DM[7.0] 12
SA_DM_1	AT41	M A_DM1
SA_DM_2	AY41	M A_DM2
SA_DM_3	AJ39	M A_DM3
SA_DM_4	BB12	M A_DM4
SA_DM_5	AY6	M A_DM5
SA_DM_6	AT7	M A_DM6
SA_DM_7	AJ5	M A_DM7
SA_DQS_0	AJ44	M A_DQS[7.0] 12
SA_DQS_1	AT44	M A_DQS1
SA_DQS_2	BA43	M A_DQS2
SA_DQS_3	BC37	M A_DQS3
SA_DQS_4	AW12	M A_DQS4
SA_DQS_5	BC8	M A_DQS5
SA_DQS_6	AJ8	M A_DQS6
SA_DQS_7	AM7	M A_DQS7
SA_DQS#_0	AJ43	M A_DQS#0
SA_DQS#_1	AT43	M A_DQS#1
SA_DQS#_2	BA44	M A_DQS#2
SA_DQS#_3	BC37	M A_DQS#3
SA_DQS#_4	AY12	M A_DQS#4
SA_DQS#_5	BD8	M A_DQS#5
SA_DQS#_6	AJ9	M A_DQS#6
SA_DQS#_7	AM8	M A_DQS#7
SA_MA_0	BA21	M A_A[14.0] 12,14
SA_MA_1	BC24	M A_A1
SA_MA_2	BG24	M A_A2
SA_MA_3	BH24	M A_A3
SA_MA_4	BG25	M A_A4
SA_MA_5	BA24	M A_A5
SA_MA_6	BD24	M A_A6
SA_MA_7	BG27	M A_A7
SA_MA_8	BE25	M A_A8
SA_MA_9	AW24	M A_A9
SA_MA_10	BC21	M A_A10
SA_MA_11	BG26	M A_A11
SA_MA_12	BH26	M A_A12
SA_MA_13	BH17	M A_A13
SA_MA_14	AY25	M A_A14

DDR SYSTEM MEMORY A

CANTIGA-GM-GP-U-NF
71.CNTIG.00U

13 M_B_DQ[63.0] <<< M_B_DQ[63.0]

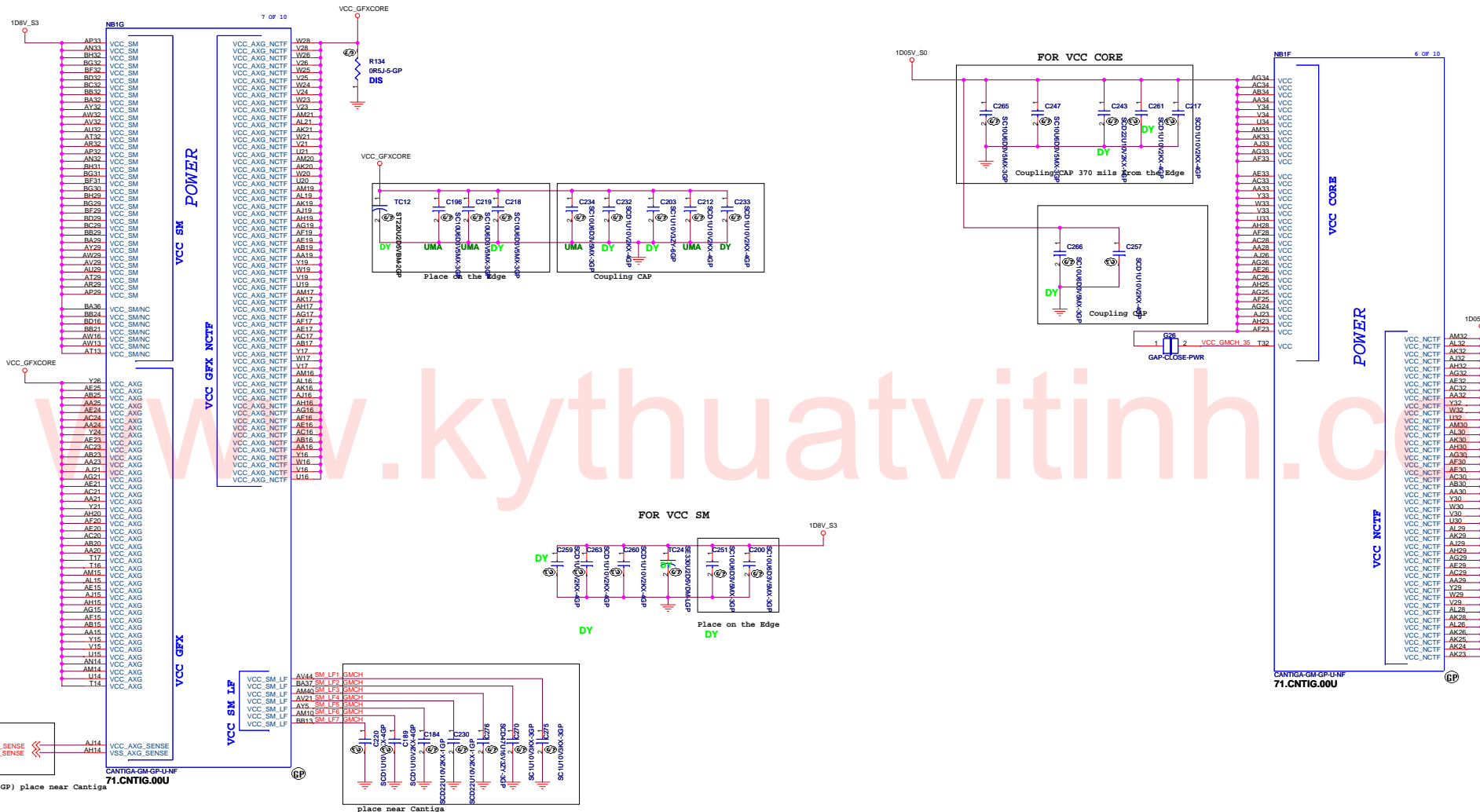
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SB_DQ_1	AH46	M B_DQ1
SB_DQ_2	AP47	M B_DQ2
SB_DQ_3	AP46	M B_DQ3
SB_DQ_4	AJ46	M B_DQ4
SB_DQ_5	AJ48	M B_DQ5
SB_DQ_6	AM48	M B_DQ6
SB_DQ_7	AP48	M B_DQ7
SB_DQ_8	AJ47	M B_DQ8
SB_DQ_9	AJ46	M B_DQ9
SB_DQ_10	AY48	M B_DQ10
SB_DQ_11	AT47	M B_DQ11
SB_DQ_12	AR47	M B_DQ12
SB_DQ_13	BA47	M B_DQ13
SB_DQ_14	BC47	M B_DQ14
SB_DQ_15	BC46	M B_DQ15
SB_DQ_16	BQ44	M B_DQ16
SB_DQ_17	BG43	M B_DQ17
SB_DQ_18	BF43	M B_DQ18
SB_DQ_19	BE45	M B_DQ19
SB_DQ_20	BC41	M B_DQ20
SB_DQ_21	BF40	M B_DQ21
SB_DQ_22	BE41	M B_DQ22
SB_DQ_23	BG38	M B_DQ23
SB_DQ_24	BF38	M B_DQ24
SB_DQ_25	BH35	M B_DQ25
SB_DQ_26	BC35	M B_DQ26
SB_DQ_27	BH40	M B_DQ27
SB_DQ_28	BC38	M B_DQ28
SB_DQ_29	BG34	M B_DQ29
SB_DQ_30	BH34	M B_DQ30
SB_DQ_31	BH14	M B_DQ31
SB_DQ_32	BG12	M B_DQ32
SB_DQ_33	BH11	M B_DQ33
SB_DQ_34	BG8	M B_DQ34
SB_DQ_35	BH12	M B_DQ35
SB_DQ_36	BF11	M B_DQ36
SB_DQ_37	BF8	M B_DQ37
SB_DQ_38	BG7	M B_DQ38
SB_DQ_39	BC5	M B_DQ39
SB_DQ_40	BC6	M B_DQ40
SB_DQ_41	AY3	M B_DQ41
SB_DQ_42	BF6	M B_DQ42
SB_DQ_43	BF5	M B_DQ43
SB_DQ_44	BA1	M B_DQ44
SB_DQ_45	BD3	M B_DQ45
SB_DQ_46	AV2	M B_DQ46
SB_DQ_47	AJ3	M B_DQ47
SB_DQ_48	AR3	M B_DQ48
SB_DQ_49	AN2	M B_DQ49
SB_DQ_50	AY2	M B_DQ50
SB_DQ_51	AV1	M B_DQ51
SB_DQ_52	AP3	M B_DQ52
SB_DQ_53	AR1	M B_DQ53
SB_DQ_54	AL1	M B_DQ54
SB_DQ_55	AL2	M B_DQ55
SB_DQ_56	AJ1	M B_DQ56
SB_DQ_57	AH1	M B_DQ57
SB_DQ_58	AM2	M B_DQ58
SB_DQ_59	AM3	M B_DQ59
SB_DQ_60	AH3	M B_DQ60
SB_DQ_61	AJ3	M B_DQ61
SB_DQ_62	AJ3	M B_DQ62
SB_DQ_63	AJ3	M B_DQ63

NB1E 5 OF 10

SB_BS_0	BC16	M_B_BS#0 13,14
SB_BS_1	BB17	M_B_BS#1 13,14
SB_BS_2	BB33	M_B_BS#2 13,14
SB_RAS#	AU17	M_B_RAS# 13,14
SB_CAS#	BG16	M_B_CAS# 13,14
SB_WE#	BF14	M_B_WE# 13,14
SB_DM_0	AM47	M_B_DM[7.0] 13
SB_DM_1	AY47	M_B_DM1
SB_DM_2	BD40	M_B_DM2
SB_DM_3	BE35	M_B_DM3
SB_DM_4	BC11	M_B_DM4
SB_DM_5	BA3	M_B_DM5
SB_DM_6	AP1	M_B_DM6
SB_DM_7	AK2	M_B_DM7
SB_DQS_0	AL47	M_B_DQS[7.0] 13
SB_DQS_1	AV48	M_B_DQS1
SB_DQS_2	BG41	M_B_DQS2
SB_DQS_3	BG37	M_B_DQS3
SB_DQS_4	BH9	M_B_DQS4
SB_DQS_5	BB2	M_B_DQS5
SB_DQS_6	AU1	M_B_DQS6
SB_DQS_7	AN6	M_B_DQS7
SB_DQS#_0	AV47	M_B_DQS#0
SB_DQS#_1	BH41	M_B_DQS#1
SB_DQS#_2	BH37	M_B_DQS#2
SB_DQS#_3	BG9	M_B_DQS#3
SB_DQS#_4	BC2	M_B_DQS#4
SB_DQS#_5	AT2	M_B_DQS#5
SB_DQS#_6	AN6	M_B_DQS#6
SB_DQS#_7	AN6	M_B_DQS#7
SB_MA_0	AV17	M_B_A[14.0] 13,14
SB_MA_1	BA25	M_B_A1
SB_MA_2	BC25	M_B_A2
SB_MA_3	AU25	M_B_A3
SB_MA_4	AW25	M_B_A4
SB_MA_5	BB28	M_B_A5
SB_MA_6	AU28	M_B_A6
SB_MA_7	AW28	M_B_A7
SB_MA_8	AT33	M_B_A8
SB_MA_9	BD33	M_B_A9
SB_MA_10	BB16	M_B_A10
SB_MA_11	AY33	M_B_A11
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SB_MA_13	AU33	M_B_A13
SB_MA_14	AU33	M_B_A14

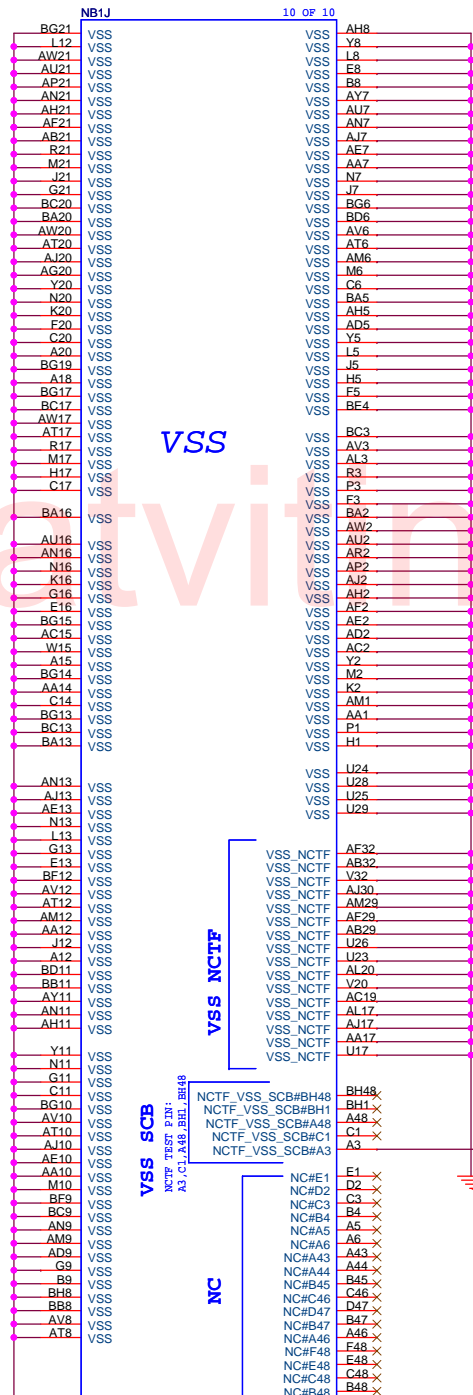
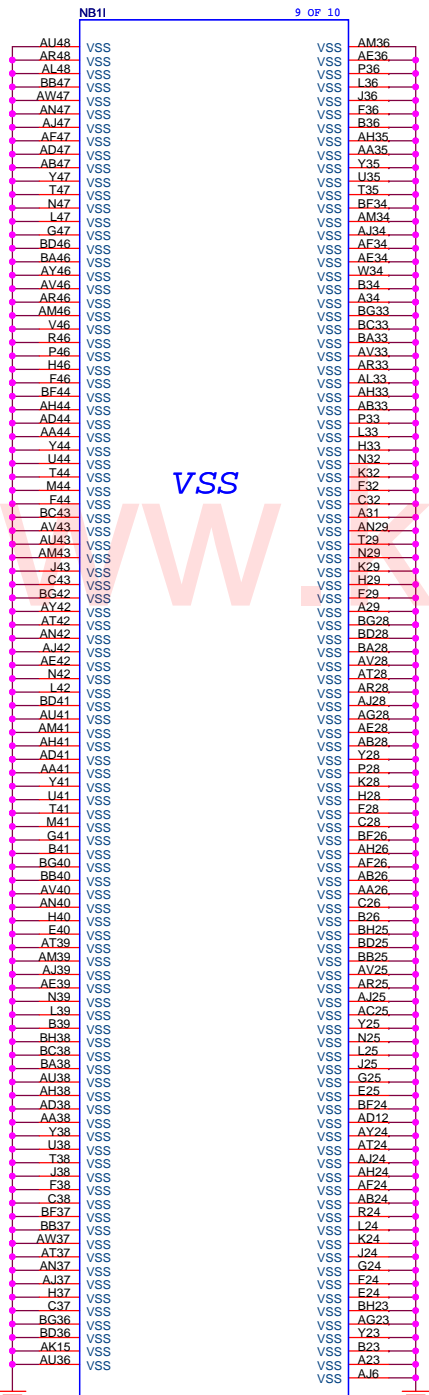
DDR SYSTEM MEMORY B

CANTIGA-GM-GP-U-NF
71.CNTIG.00U



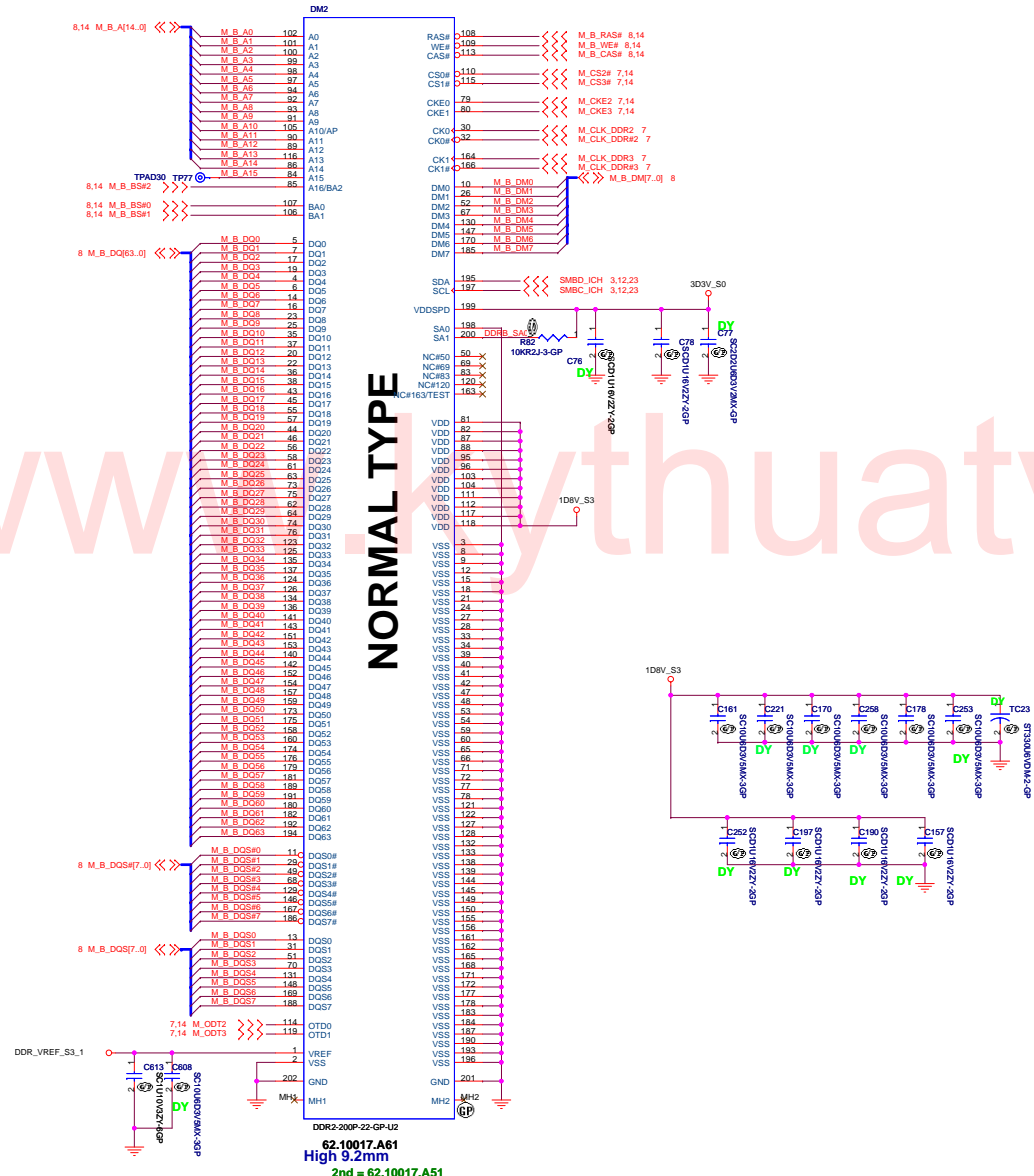
U60 (I8L263AKRZ-T-GP) place near Cantiga 71.CNTIG.000

place near Cantiga



緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

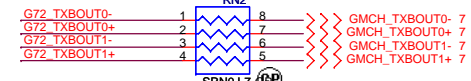
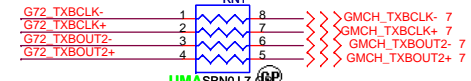
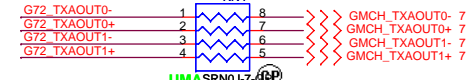
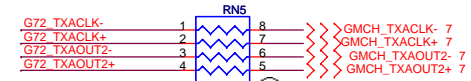
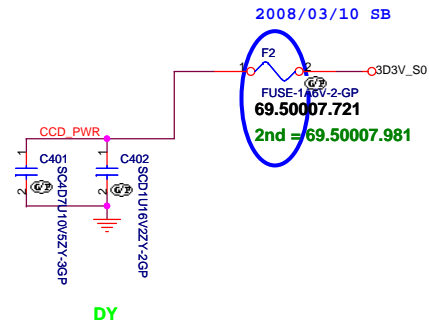
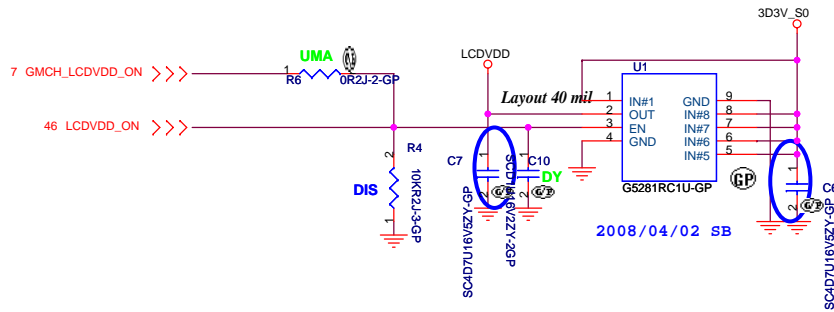
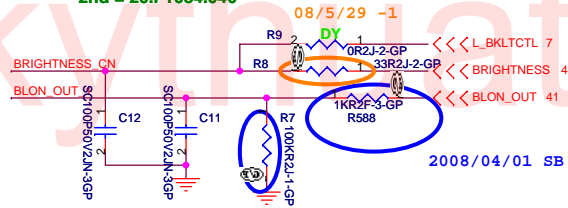
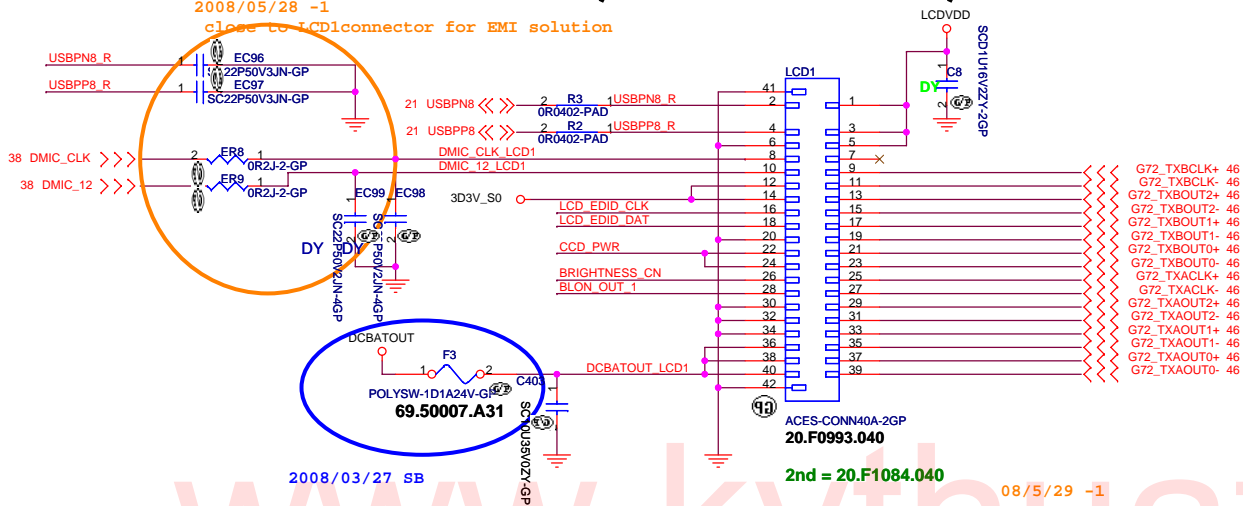
DDR2 SOCKET_2



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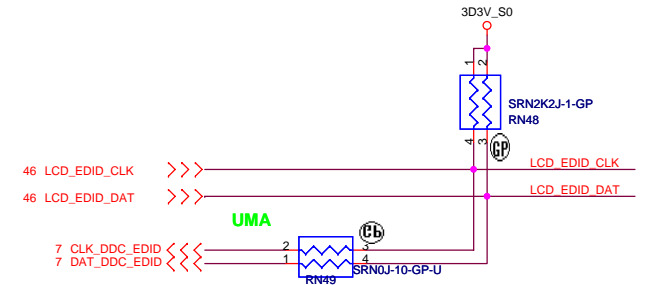
LCD/INVERTER/CCD CONN

2008/05/28 -1
close to LCDconnector for EMI solution



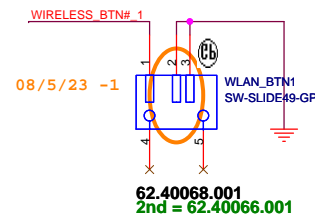
Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	PWM
4	BLON
5	GND
6	GND

CCD Pin	
Pin	Symbol
1	GND
2	GND
3	5V
4	USB-
5	USB+



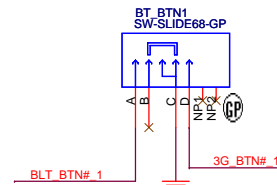
www.kythuativinh.com

Wireless ON/OFF
Check Wireless Button left or right

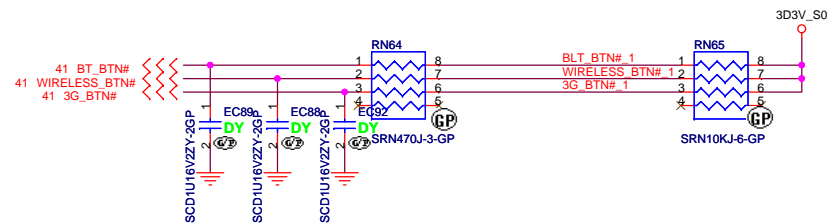


62.40068.001
2nd = 62.40066.001

BlueTooth ON/OFF



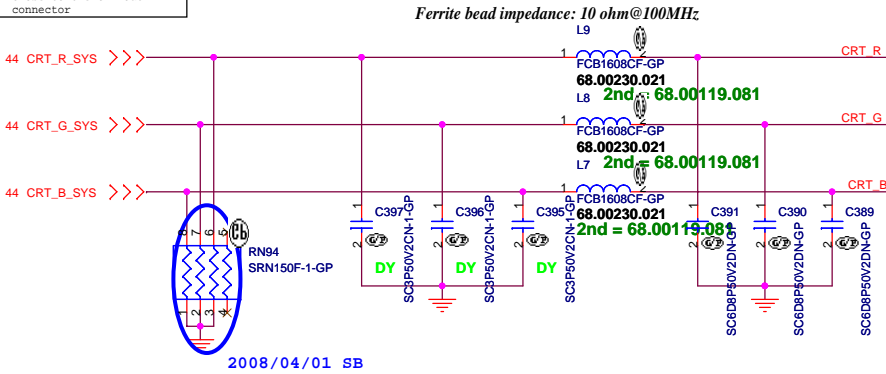
62.40018.401
2nd = 62.40018.411



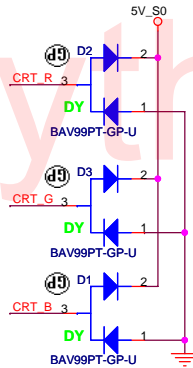
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Taipei Hsien 221, Taiwan, R.O.C.

Title		SWITCH	
Size	Document Number	Rev	
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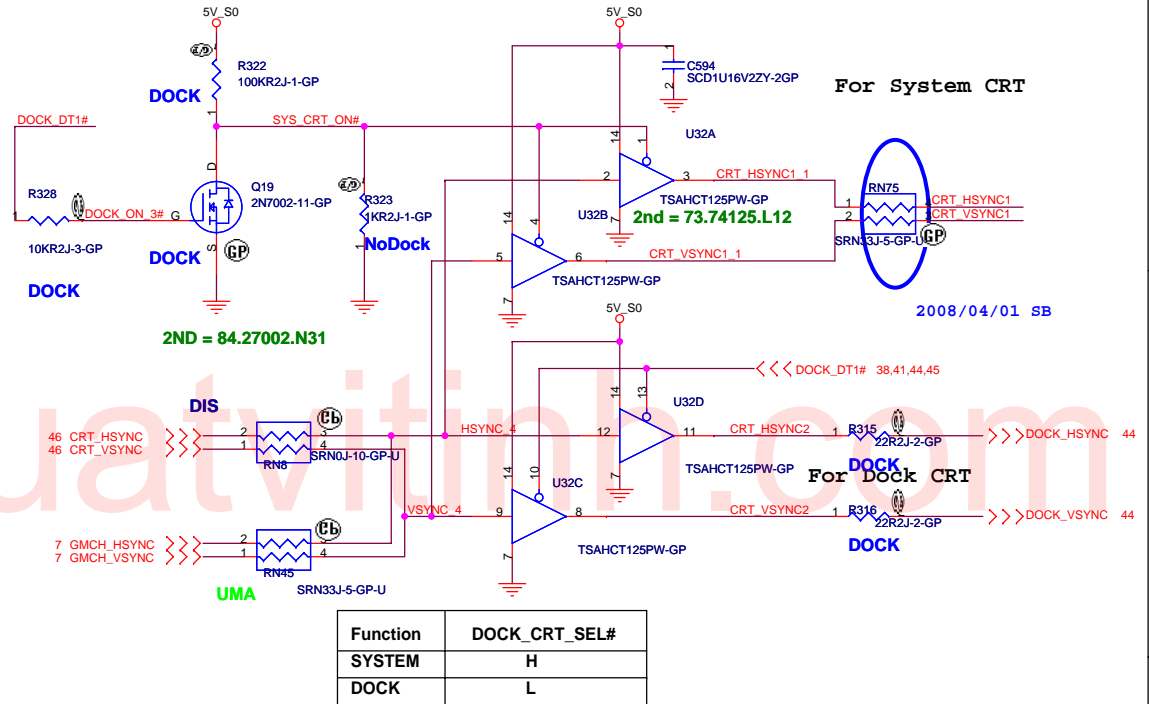
Layout Note:
Place these resistors
close to the CRT-out
connector



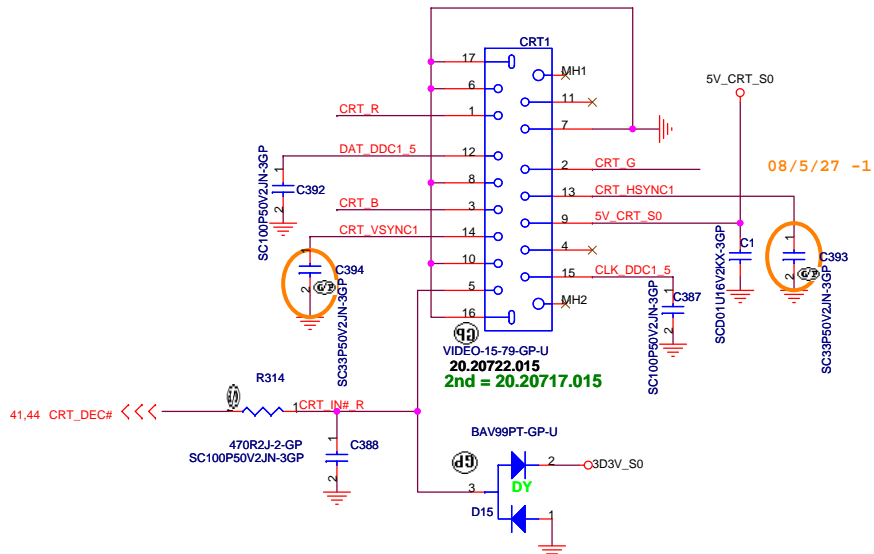
Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



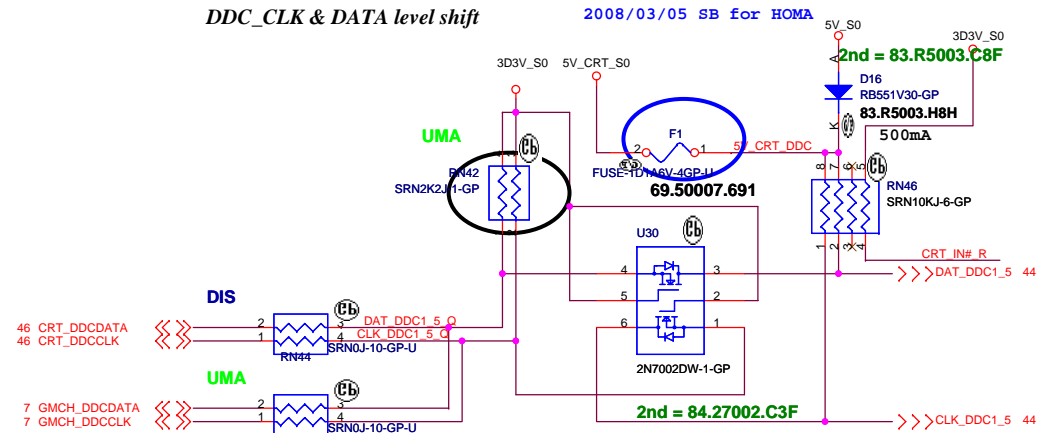
Hsync & Vsync level shift



CRT I/F & CONNECTOR

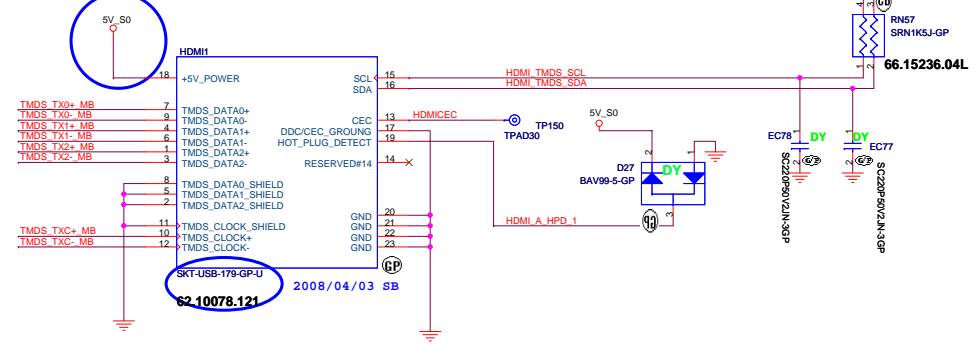


DDC_CLK & DATA level shift



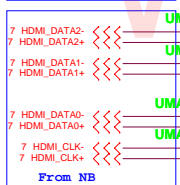
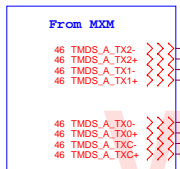
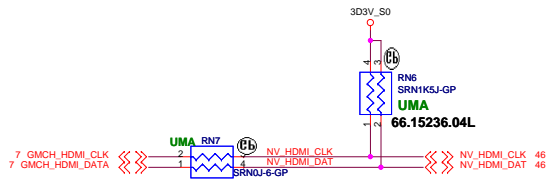
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2008/04/01 SB

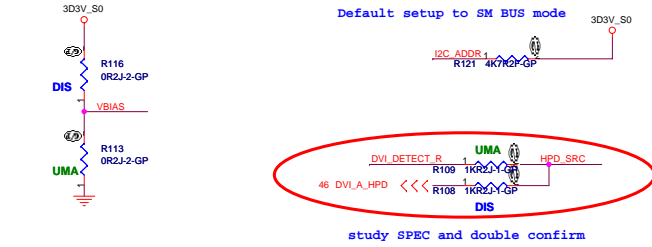
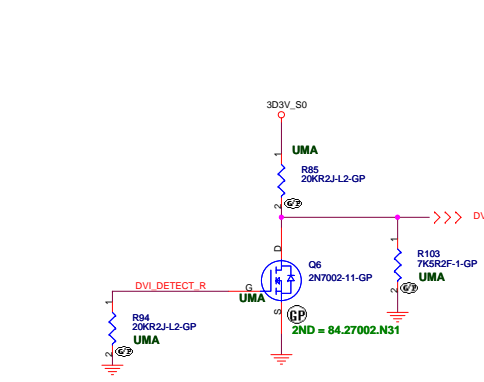
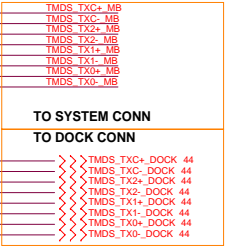
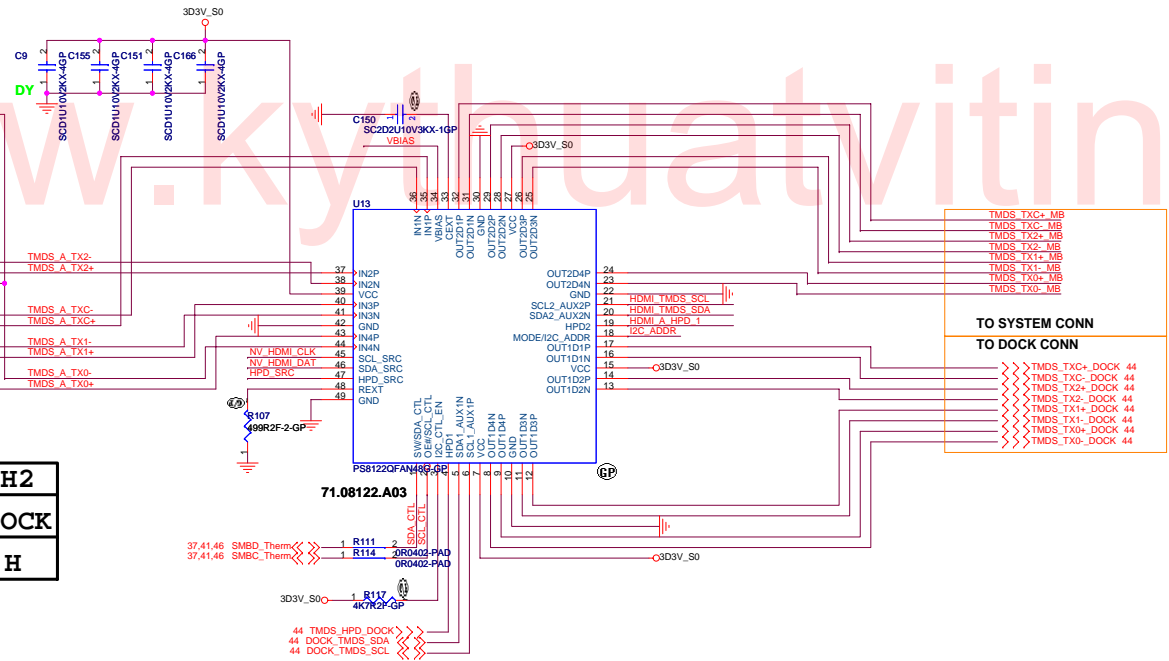


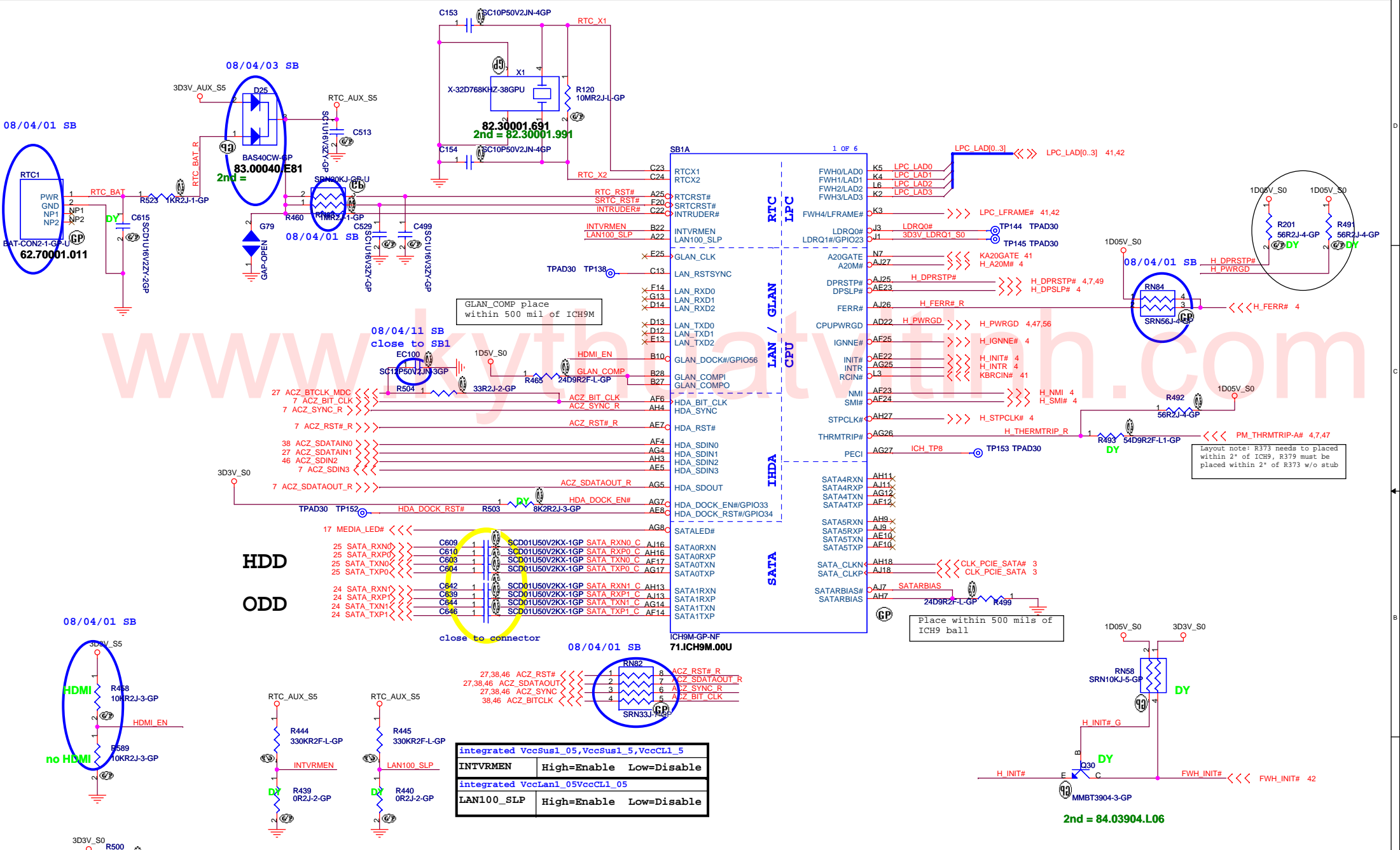
SKT-USB-179-GP-U
62.10078.121

2008/04/03 SB



CH1	CH2
HDMI	DOCK
L	H





08/04/01 SB

08/04/03 SB

BAT-CON2-1-GP-U
62.70001.011

BAS40CW-6P
83.00040.E81
2nd =

82.30001.691
2nd = 82.30001.991

08/04/11 SB
close to SB1

HDD
ODD

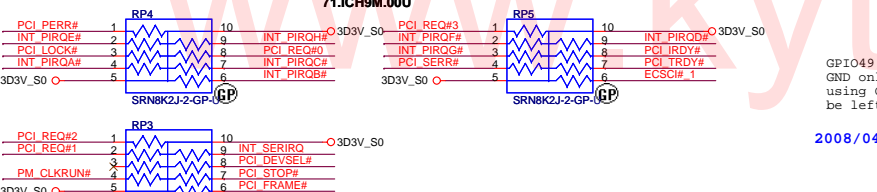
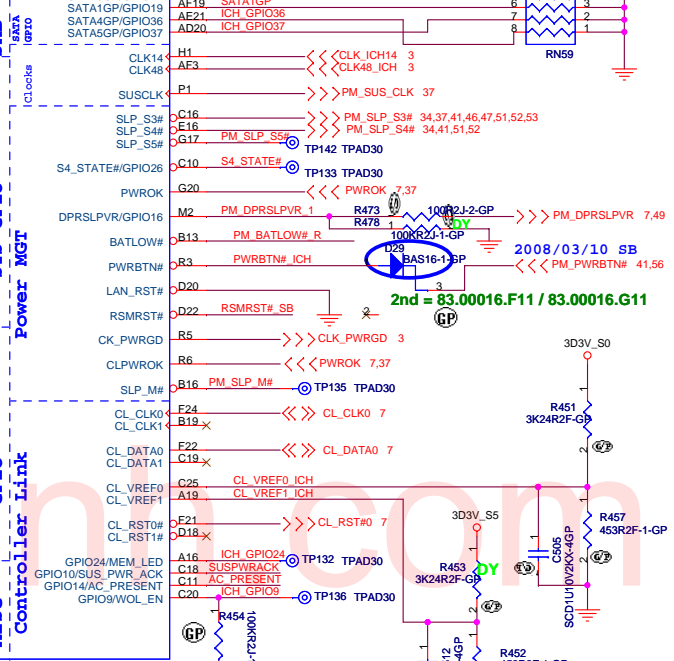
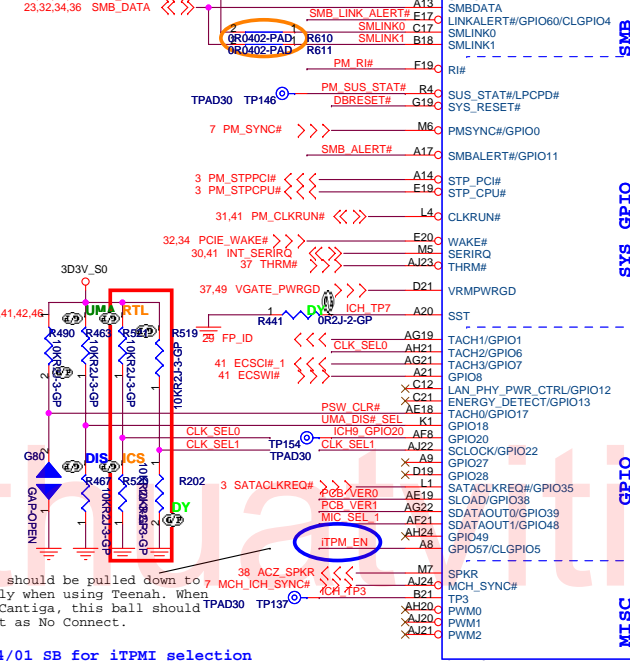
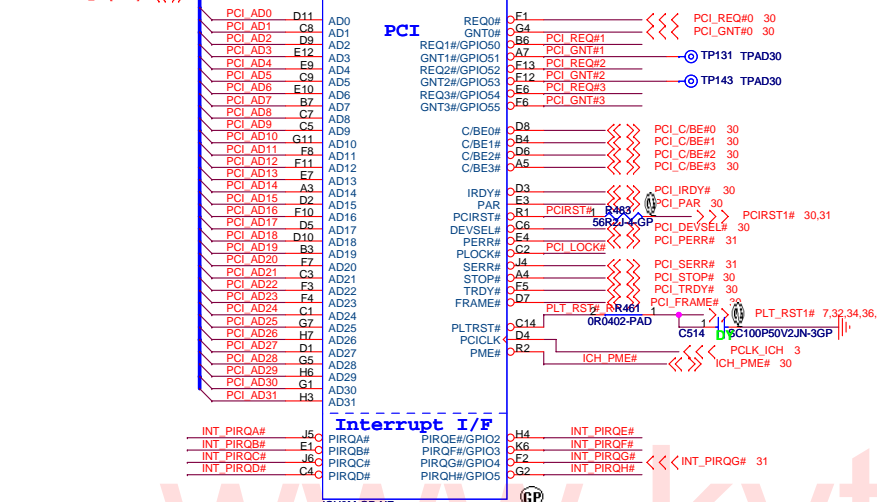
08/04/01 SB

08/04/01 SB

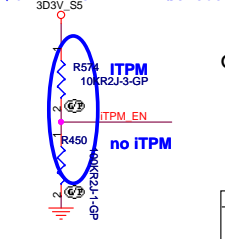
integrated VccSus1_05,VccSus1_5,VccCLI_5	
INTVRMEN	High=Enable Low=Disable
integrated VccLan1_05VccCLI_05	
LAN100_SLP	High=Enable Low=Disable

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2008/04/01 SB for iTPMI selection



CLK_SELECT CLERK_SELECT CLK_SEL

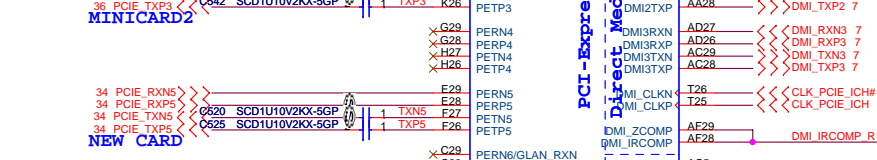
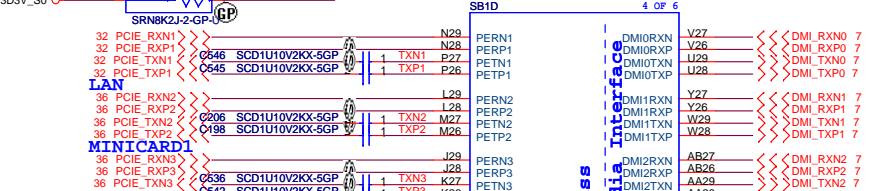
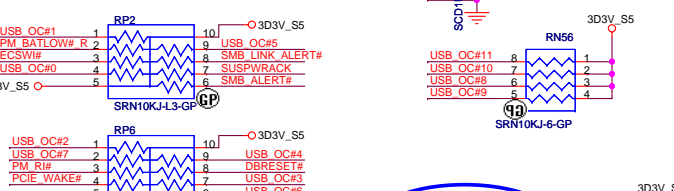
CLK_SEL1	CLK_SEL0	CLK_SEL
0	0	??
0	1	??
1	0	ICS
1	1	RTL

MIC IN

MIC_SEL LOW = Analog
HIGH = Digital

No Reboot Strap

SPKR LOW = Default
HIGH = No Reboot



USB

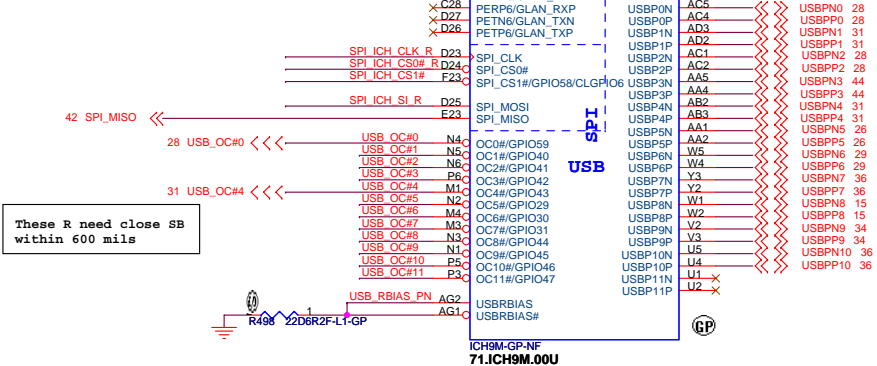
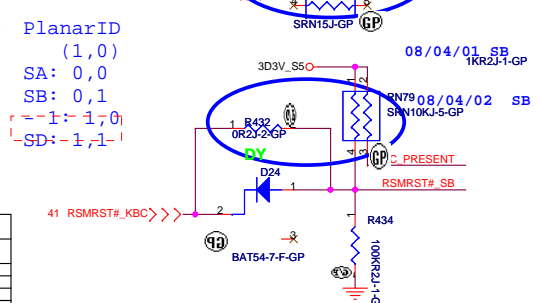
Pair	Device
0	USB1
1	USB4
2	USB2
3	DOCK USB
4	USB3
5	Bluetooth
6	FingerPrint
7	MINIC1
8	WENIC44
9	NEW1
10	MINIC2
11	NC

BOOT BIOS Strap

PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPT
1	0	PCT
1	1	LPC(Default)

A16 swap override strap

PCI_GNT#3	low = A16 swap override enable	high = default
0	low	high
1	high	low

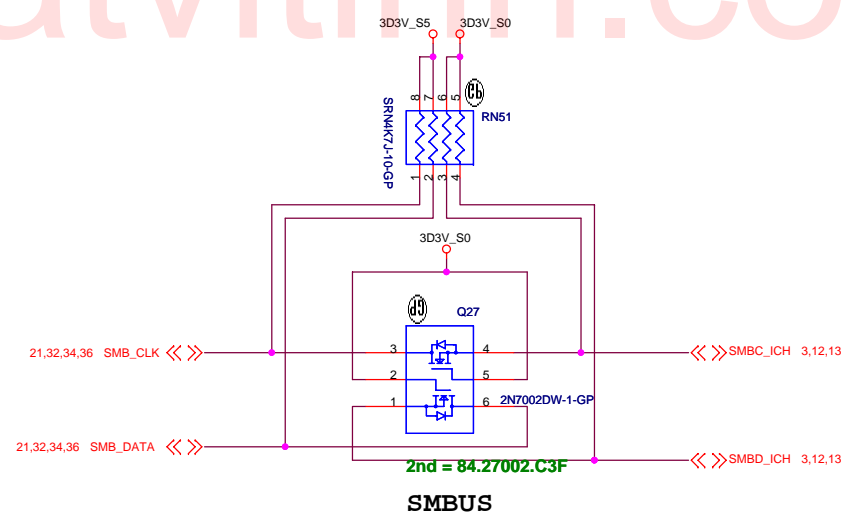
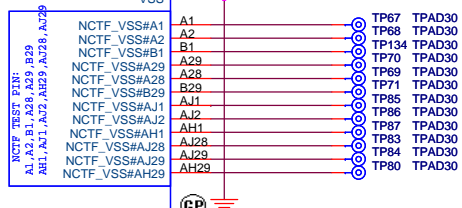


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File: ICH9-M (2 of 4)
HOMA 3G

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SB1E	5 OF 6	
AA26	VSS	VSS
AA27	VSS	J23
AA3	VSS	J26
AA6	VSS	J27
AB1	VSS	VSS
AA23	VSS	AC22
AB26	VSS	K28
AB29	VSS	K29
AB4	VSS	L13
AB5	VSS	L15
AC17	VSS	L2
AC26	VSS	L26
AC27	VSS	L27
AC3	VSS	L5
AD1	VSS	L7
AD10	VSS	M12
AD12	VSS	M13
AD13	VSS	M14
AD14	VSS	M15
AD17	VSS	M16
AD18	VSS	M17
AD21	VSS	M23
AD28	VSS	M28
AD29	VSS	M29
AD4	VSS	N11
AD5	VSS	N12
AD6	VSS	N13
AD7	VSS	N14
AD9	VSS	N15
AE12	VSS	N16
AE13	VSS	N17
AE14	VSS	N18
AE16	VSS	N26
AE17	VSS	N27
AE2	VSS	P12
AE20	VSS	P13
AE24	VSS	P14
AE3	VSS	P15
AE4	VSS	P16
AE6	VSS	P17
AE9	VSS	P2
AF13	VSS	P23
AF16	VSS	P28
AF18	VSS	P29
AF22	VSS	P4
AF26	VSS	P7
AF27	VSS	R11
AF5	VSS	R12
AF7	VSS	R13
AF9	VSS	R14
AG13	VSS	R15
AG16	VSS	R16
AG18	VSS	R17
AG20	VSS	R18
AG23	VSS	R28
AG3	VSS	T12
AG6	VSS	T13
AG9	VSS	T14
AH12	VSS	T15
AH14	VSS	T16
AH17	VSS	T17
AH19	VSS	T23
AH2	VSS	B26
AH22	VSS	U12
AH25	VSS	U13
AH28	VSS	U14
AH5	VSS	U15
AH8	VSS	U16
AJ12	VSS	U17
AJ14	VSS	U18
AJ17	VSS	AD23
AJ8	VSS	U26
B11	VSS	U27
B14	VSS	U3
B17	VSS	V1
B2	VSS	V13
B20	VSS	V15
B23	VSS	V23
B5	VSS	V28
B8	VSS	V29
C26	VSS	V4
C27	VSS	V5
E11	VSS	W26
E14	VSS	W27
E18	VSS	W3
E2	VSS	Y1
E21	VSS	Y28
E24	VSS	Y29
E5	VSS	Y4
F8	VSS	Y5
F16	VSS	AG28
F28	VSS	AH6
F29	VSS	AF2
G12	VSS	B25
G14	VSS	
G18	VSS	
G21	VSS	
G24	VSS	
G26	VSS	
G27	VSS	
G8	VSS	
H2	VSS	
H23	VSS	
H28	VSS	
H29	VSS	



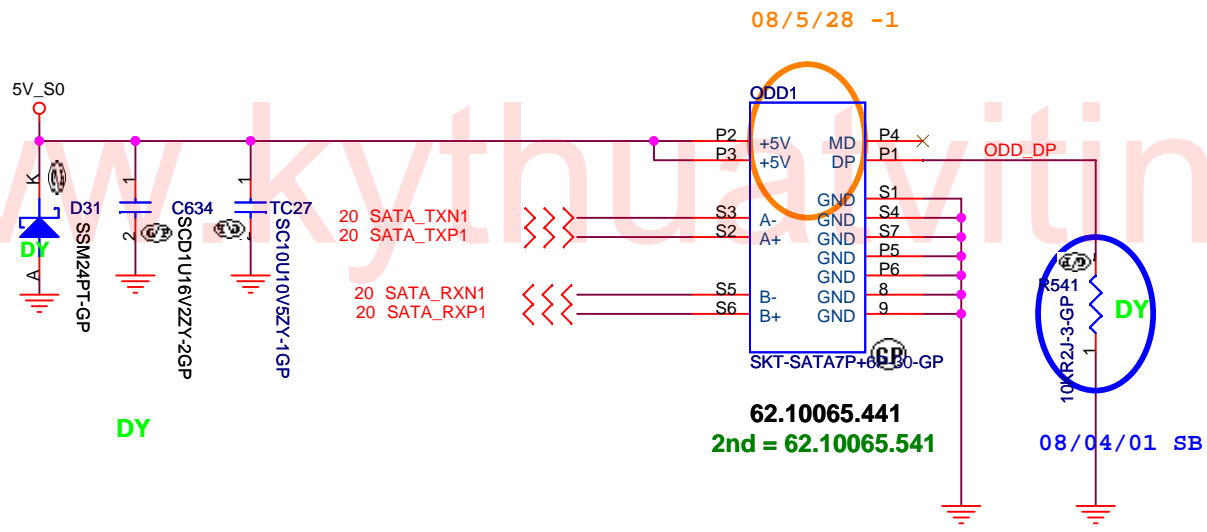
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Title: **ICH9-M (4 of 4)**

Size: Document Number: **HOMA 3G** Rev: **-1**

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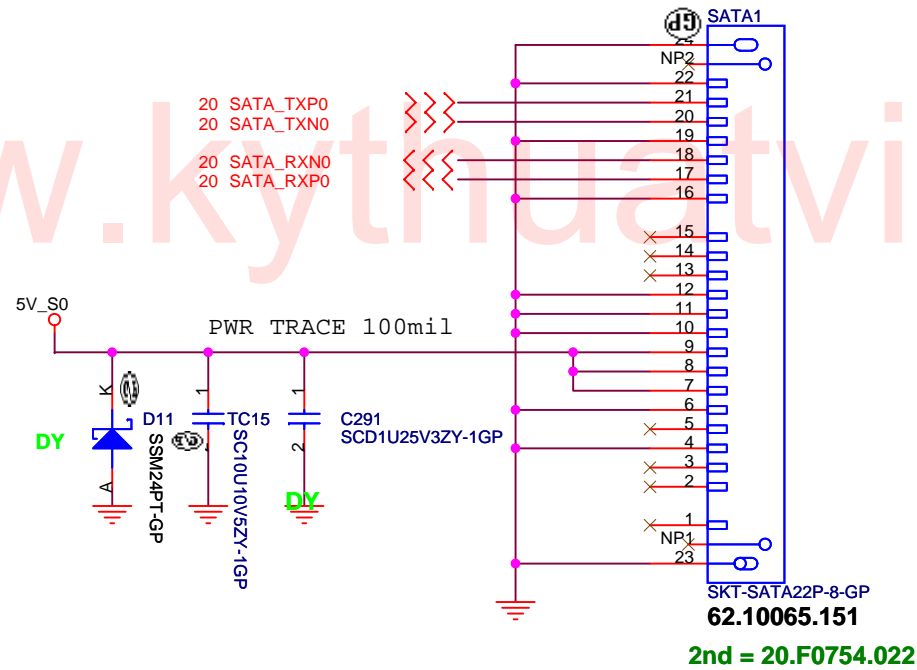
ODD Connector

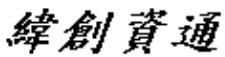


 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
ODD	
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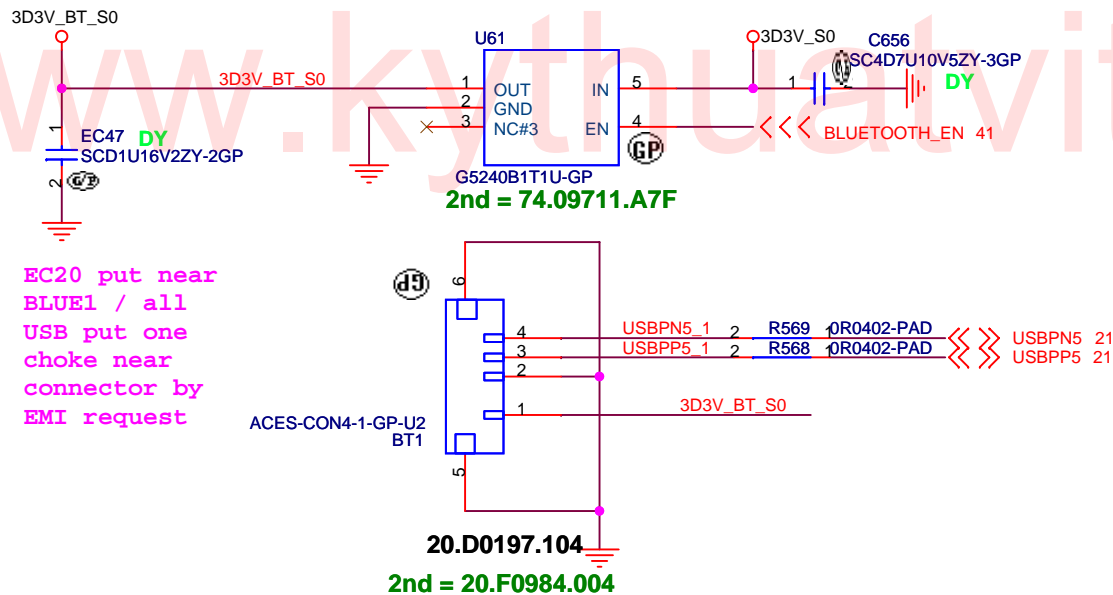
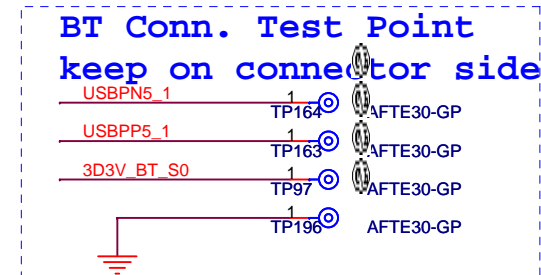
SATA Connector

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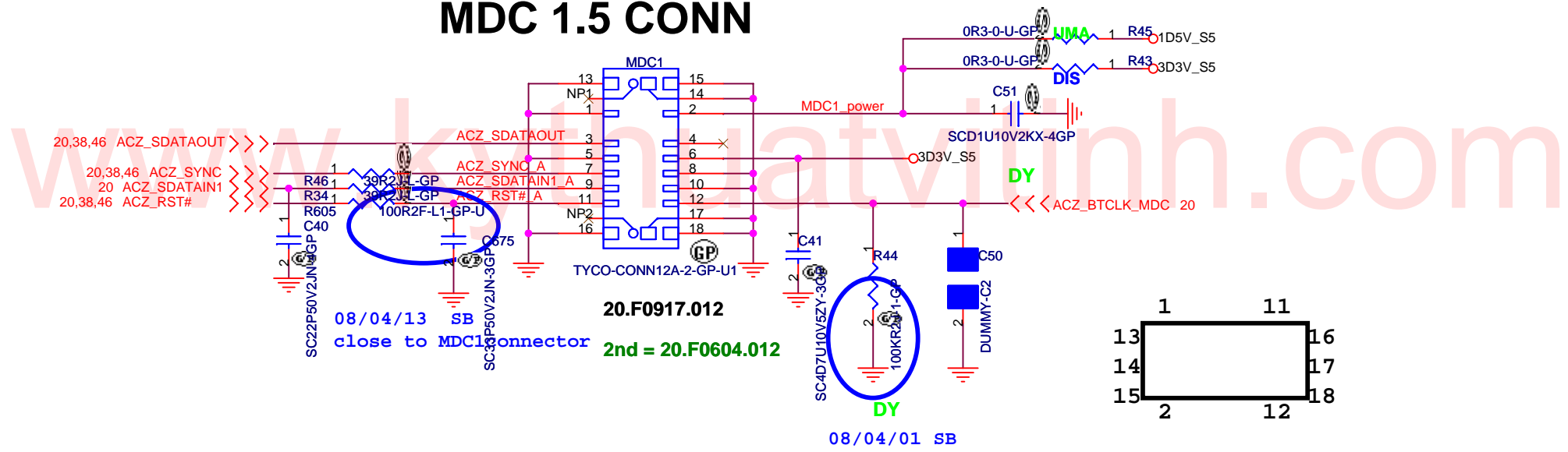
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Title		
HDD CONN		
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BLUETOOTH MODULE




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Title			
BLUETOOTH			
Size	Document Number		Rev
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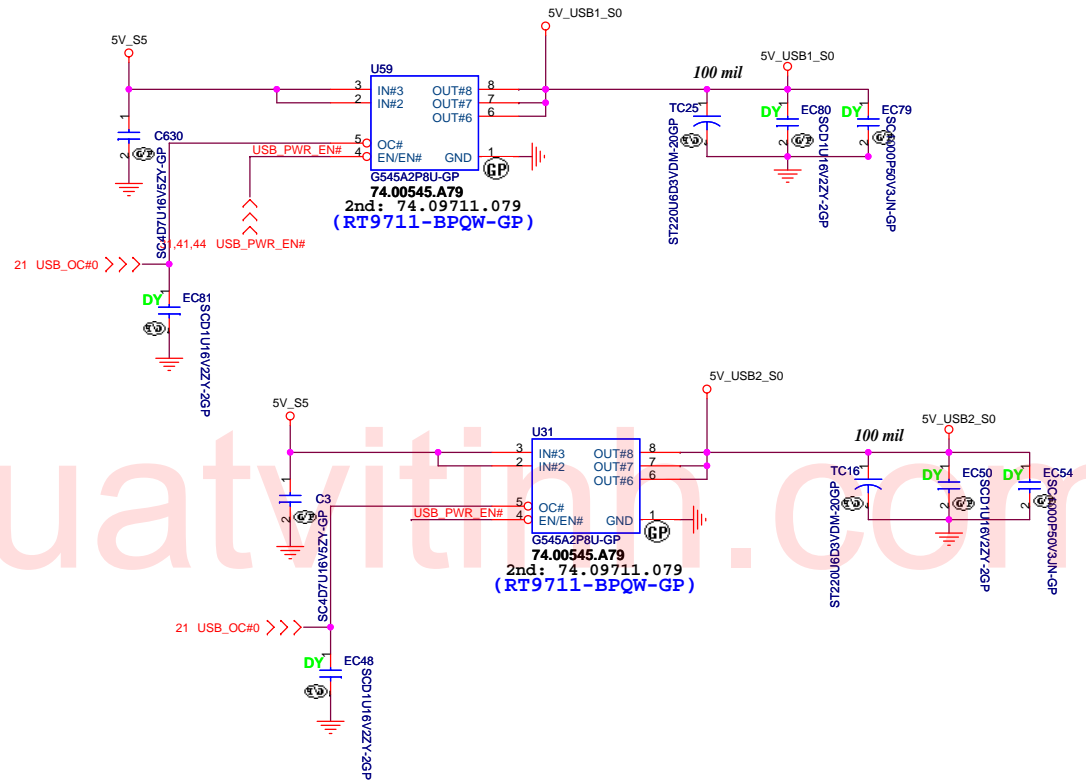
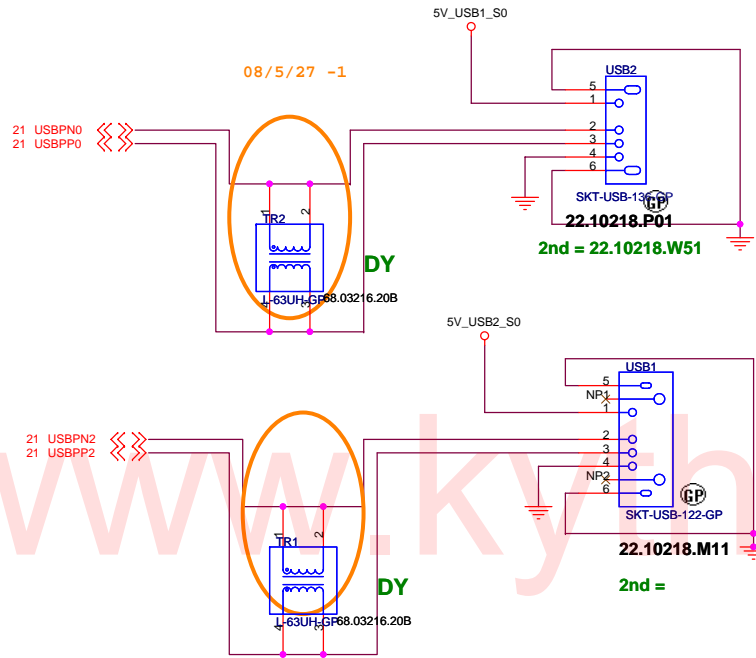
MDC 1.5 CONN



08/04/13 SB
close to MDC1 connector
20.F0917.012
2nd = 20.F0604.012

08/04/01 SB

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Title	
MDC	
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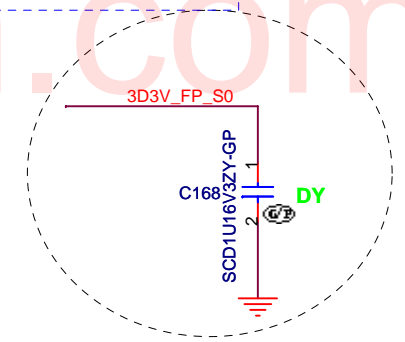
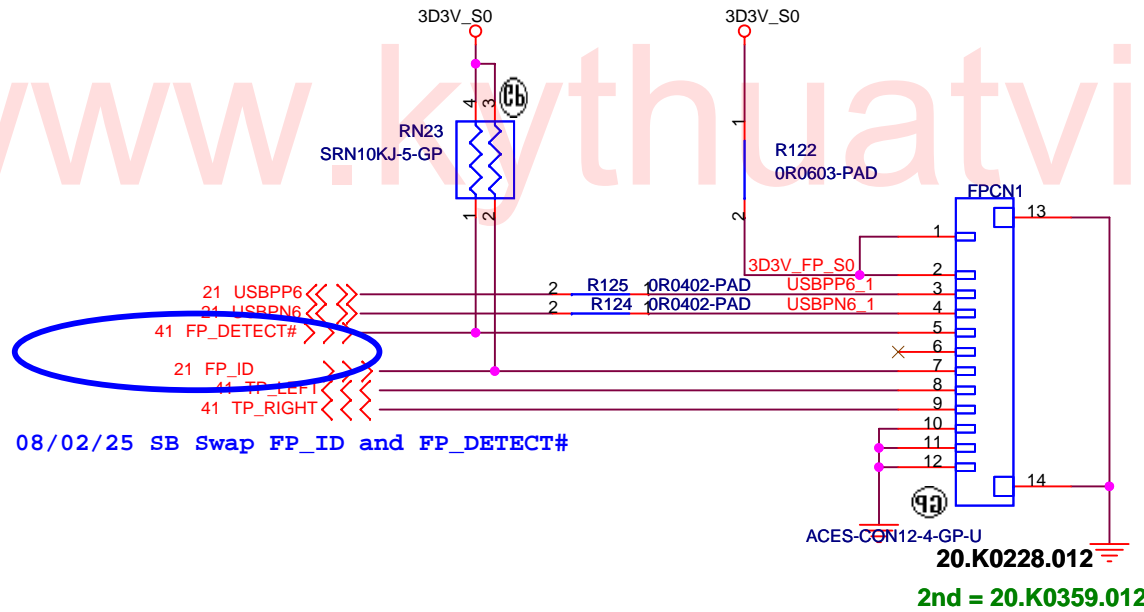


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Finger printer

FP Conn. Test Point
keep on connector side

USBPP6_1	1	TP76	AFTE30-GP
USBP6_1	1	TP74	AFTE30-GP
FP_DETECT#	1	TP140	AFTE30-GP
FP_ID	1	TP141	AFTE30-GP
TP_LEFT	1	TP73	AFTE30-GP
TP_RIGHT	1	TP72	AFTE30-GP
3D3V_FP_S0	1	TP185	AFTE30-GP
	1	TP197	AFTE30-GP



For EMI

緯創資通

Wistron Corporation

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Title

Finger Printer

Size

Document Number

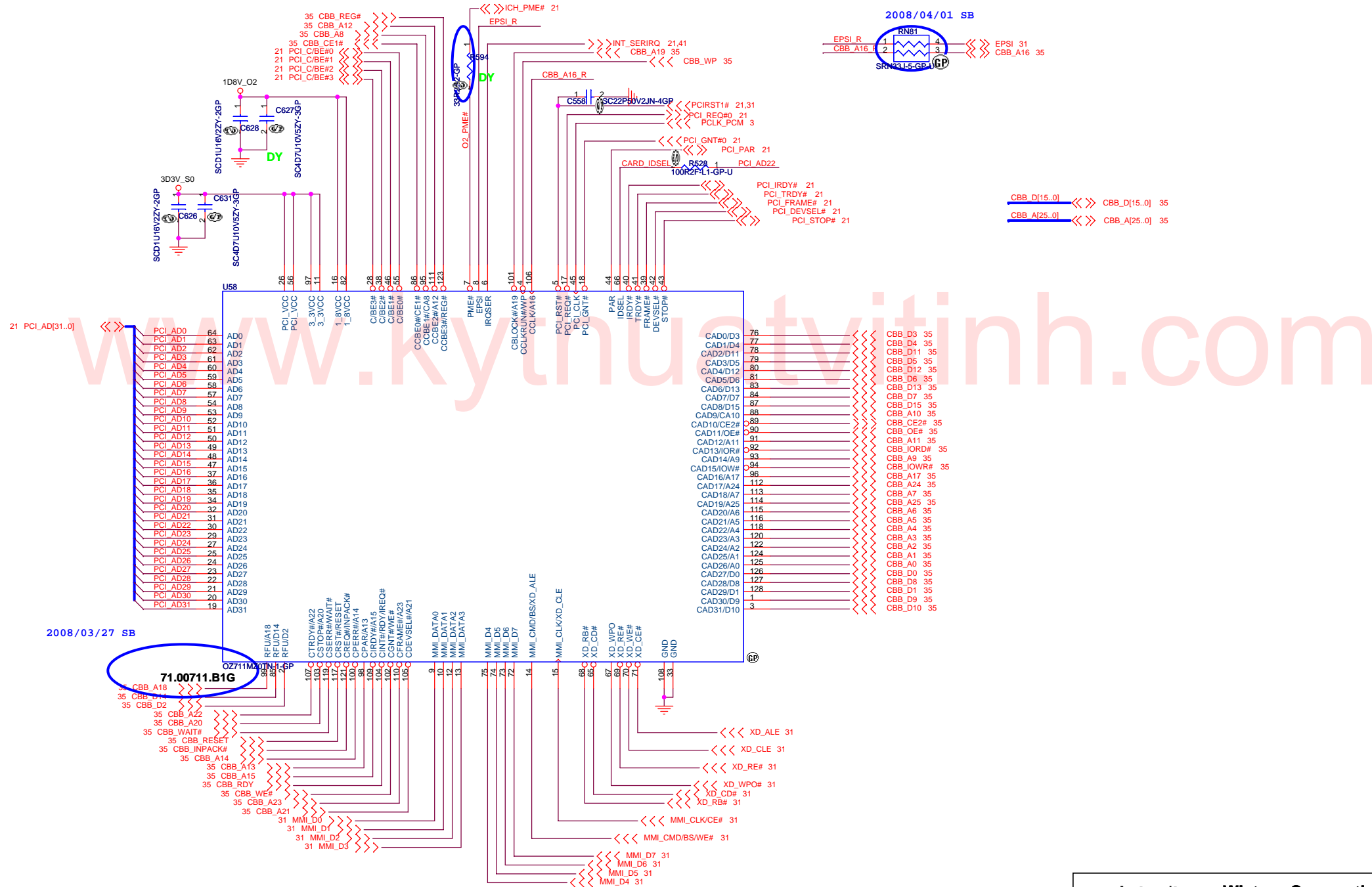
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Title: **Card Reader - OZ711MZ0**

Size	Document Number	Rev
		-1

DATE: Friday, May 30, 2008

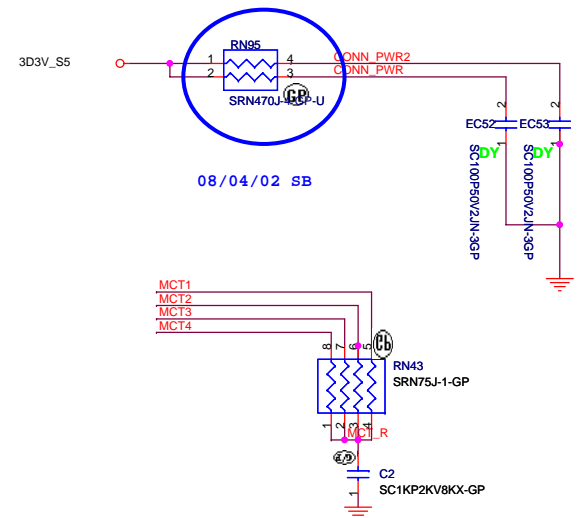
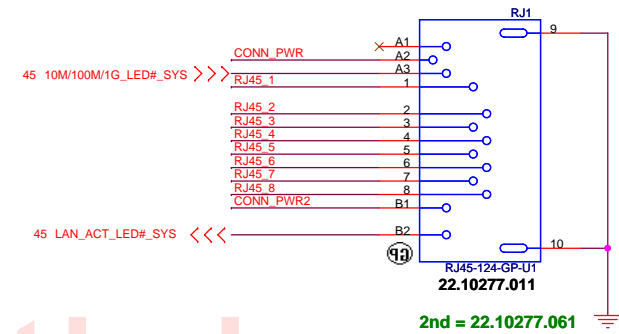
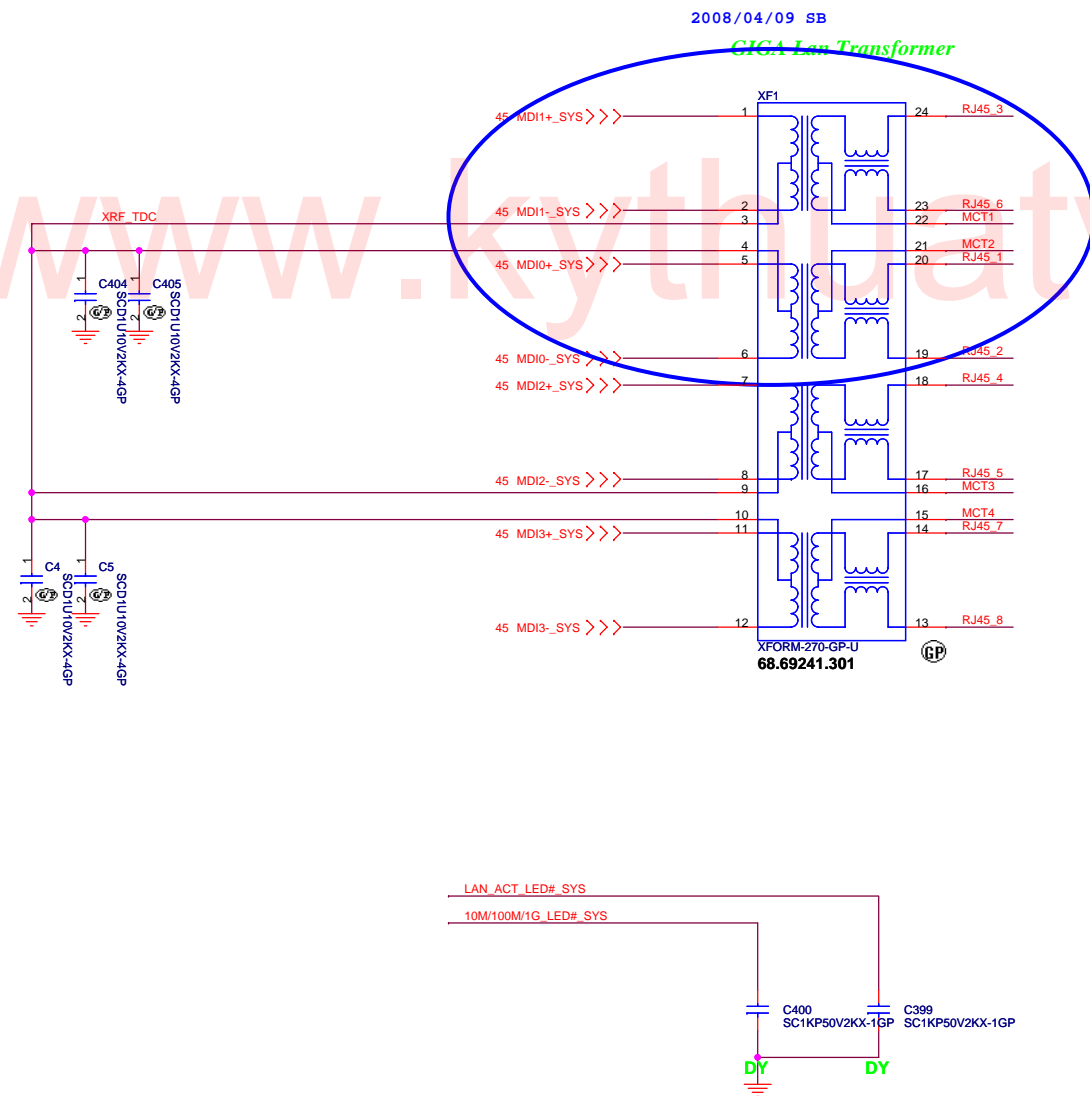
HOMA 3G

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- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

LAN Connector

LAN Connector



HOMA 3G

HOMA 3G

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Title **LAN CONN**

Size A3	Document Number	Rev -1
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PCMCIA Socket

Cardbus I/F

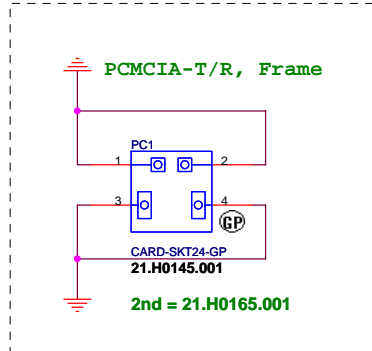
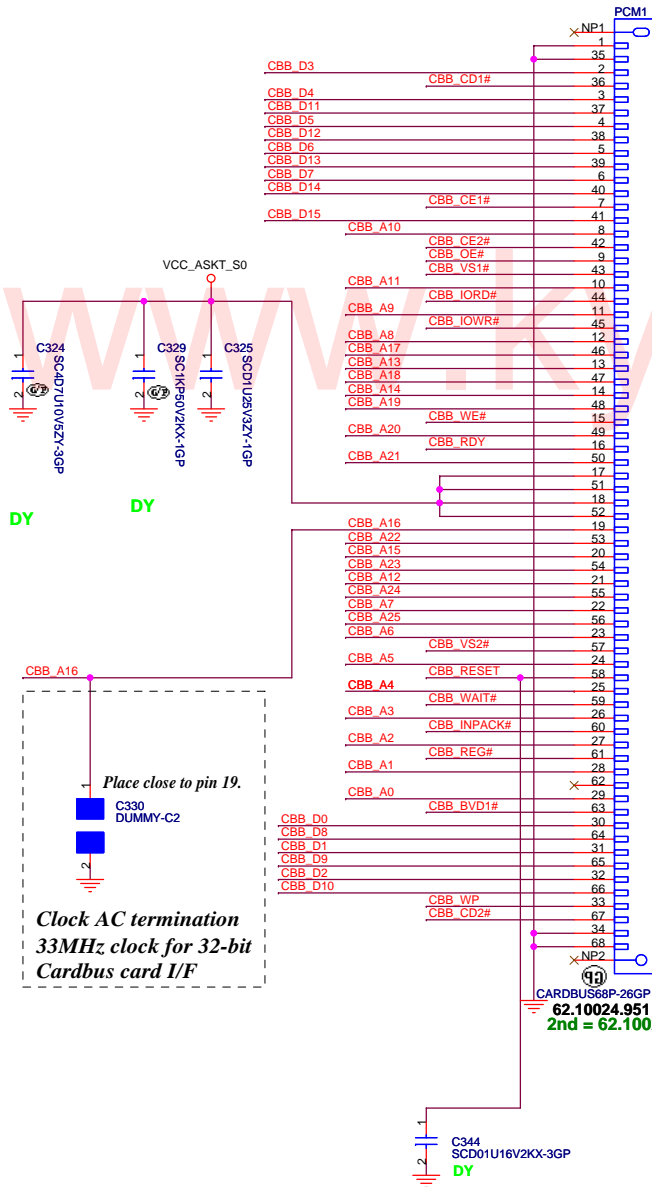
CBB_D[15..0] <<>> CBB_D[15..0] 30

CBB_A[25..0] <<>> CBB_A[25..0] 30

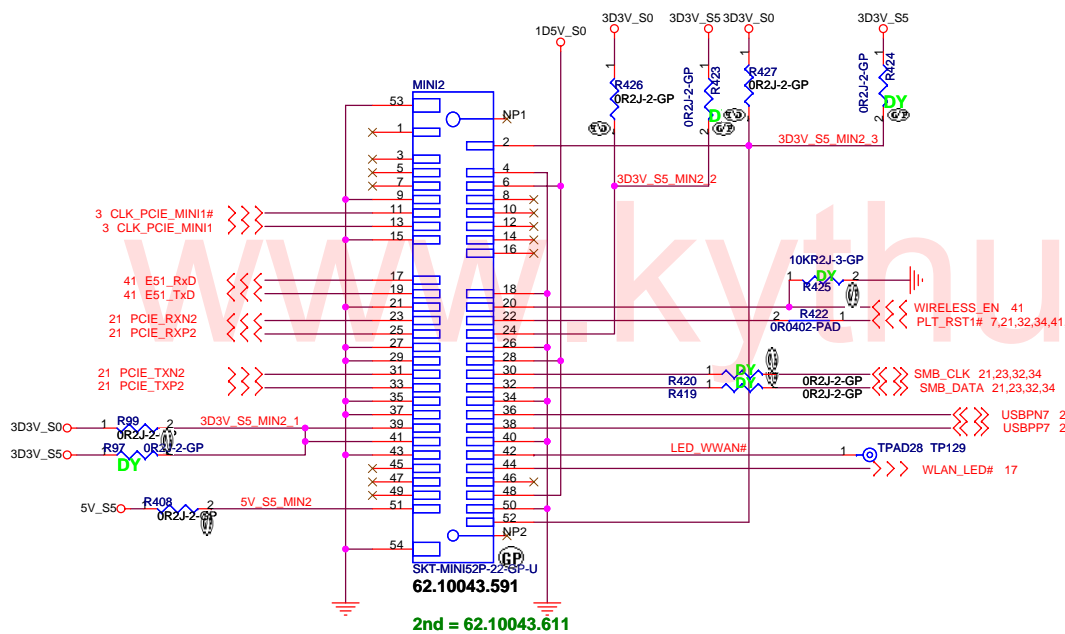
CBB_IORD# 30
 CBB_IOWR# 30
 CBB_OE# 30
 CBB_WE# 30
 CBB_REG# 30
 CBB_RDY 30
 CBB_WP 30
 CBB_RESET# 30
 CBB_WAIT# 30
 CBB_INPACK# 30

CBB_CE1# 30
 CBB_CE2# 30

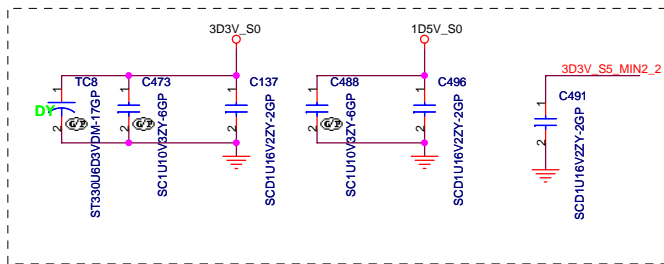
CBB_CD1# 31
 CBB_CD2# 31
 CBB_VS1# 31
 CBB_VS2# 31
 CBB_BVD1# 31



Mini Card Connector(WLAN)

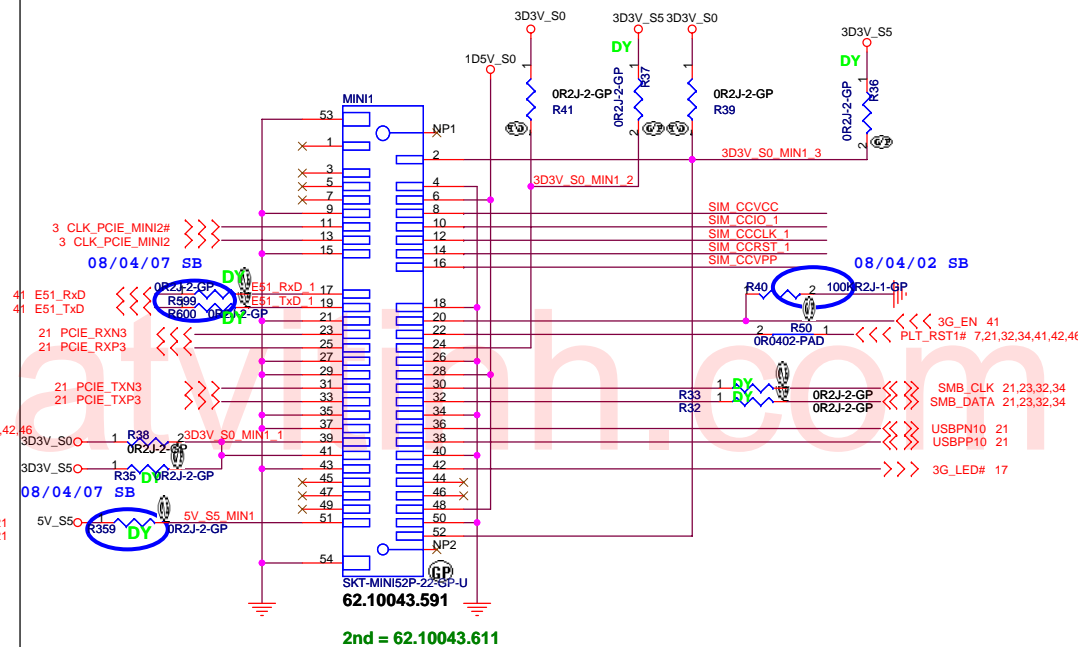


Place near MINIC1

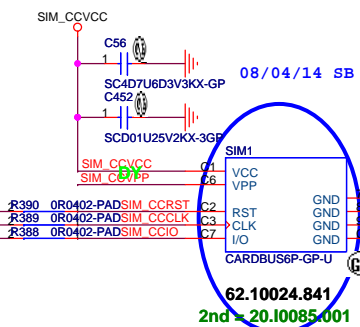
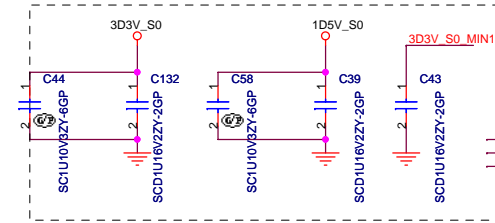


Mini Card Connector(Robson2 and 3G)

Support debug-card



Place near MINIC2

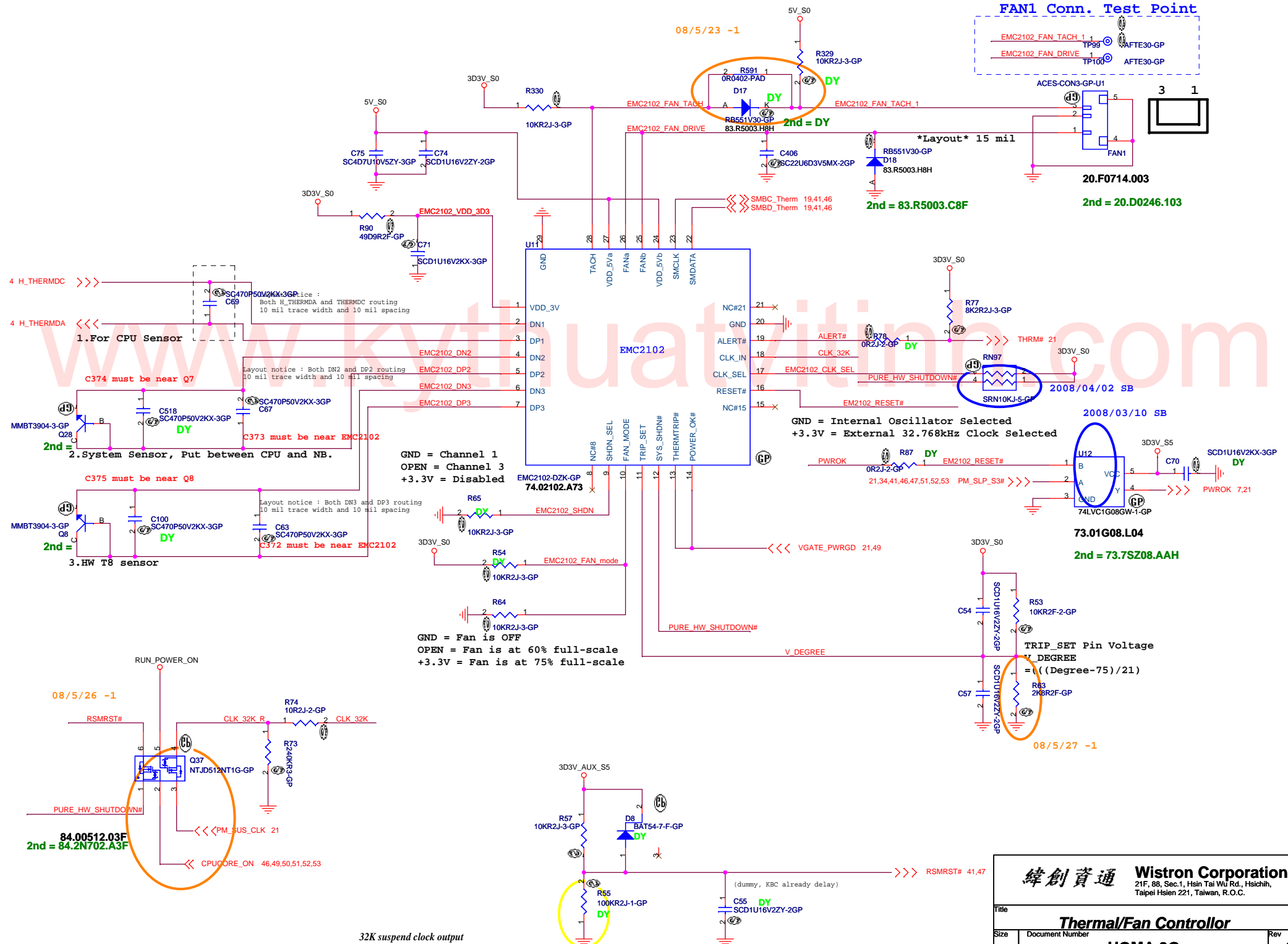


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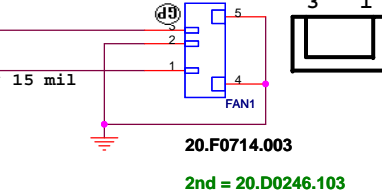
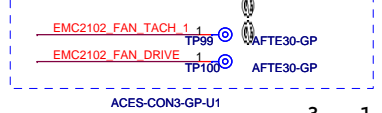
Title: **MINI & SIM CARD**

Size A3 Document Number **HOMA 3G** Rev **-1**

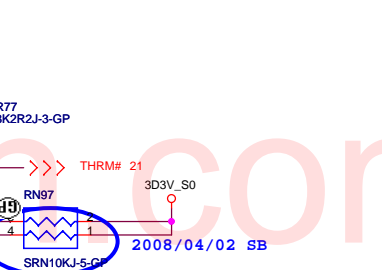
Date: Friday, May 30, 2008 Sheet 36 of 56



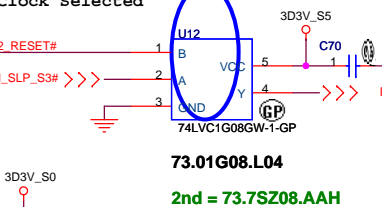
FAN1 Conn. Test Point



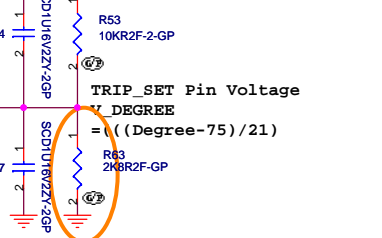
20.F0714.003
2nd = 20.D0246.103



2008/04/02 SB
2008/03/10 SB



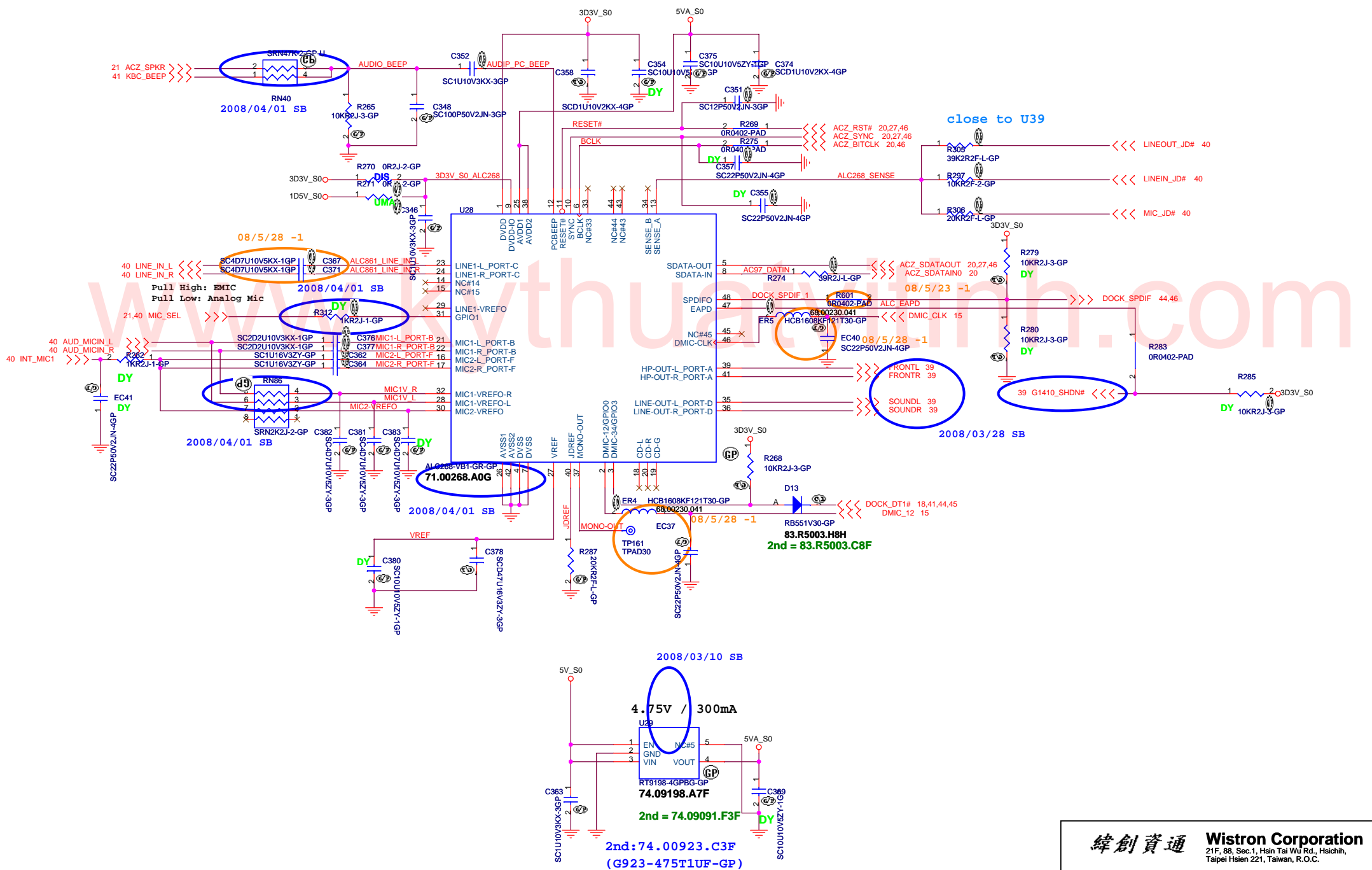
73.01G08.L04
2nd = 73.7S208.AAH



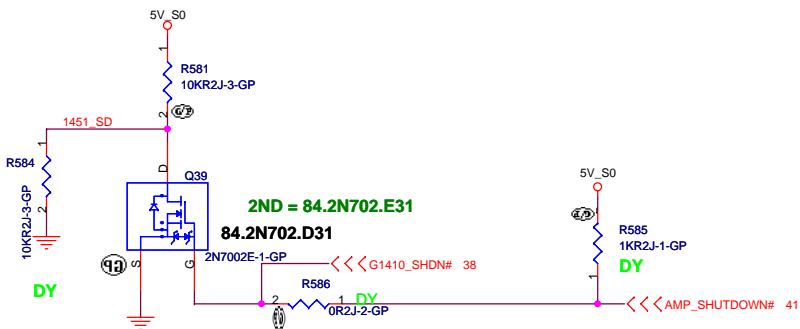
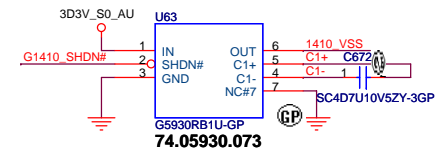
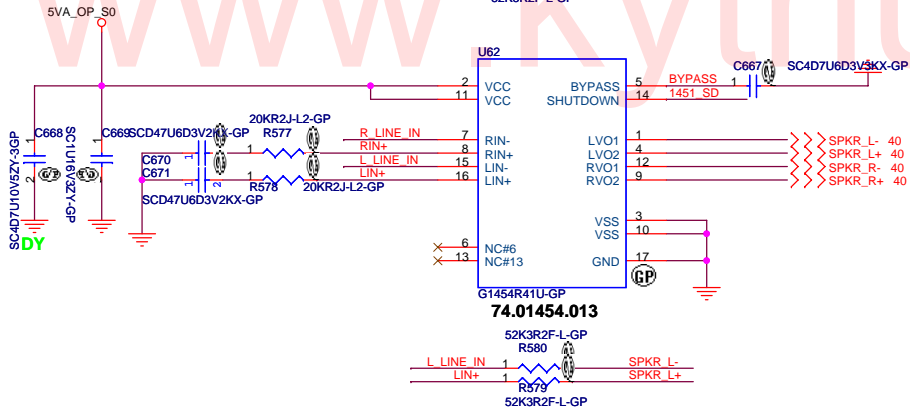
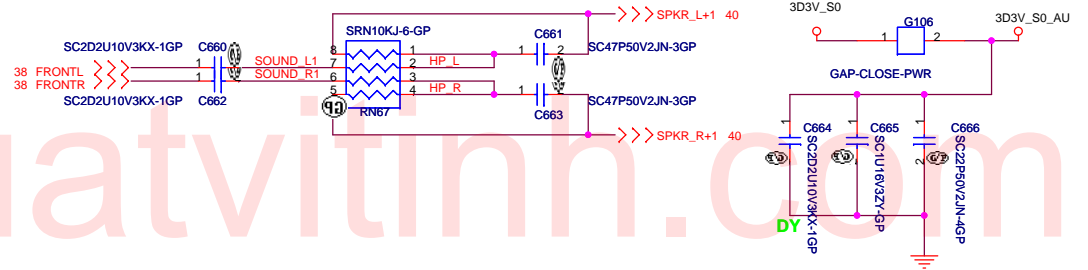
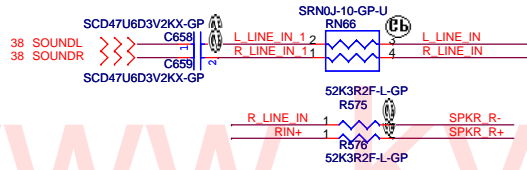
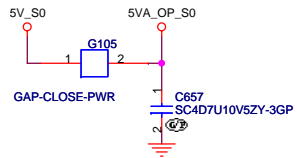
08/5/27 -1

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		21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Thermal/Fan Controller			
Size	Document Number	HOMA 3G	
Date: Friday, May 30, 2008	Sheet	37	of 56
			Rev -1

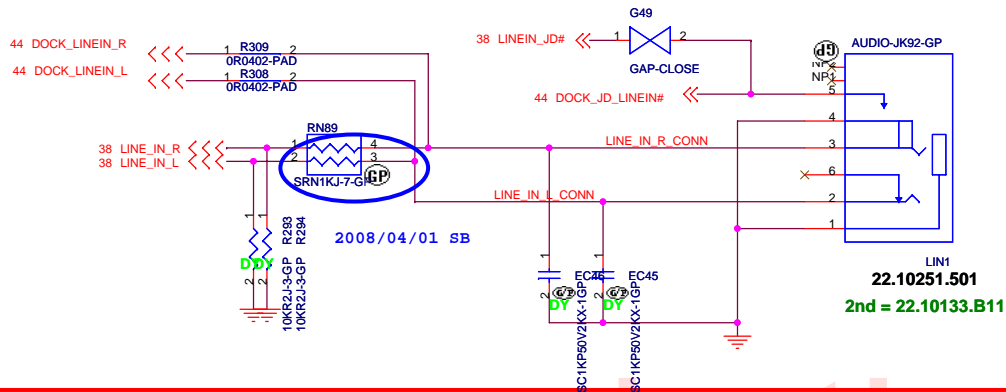
32K suspend clock output



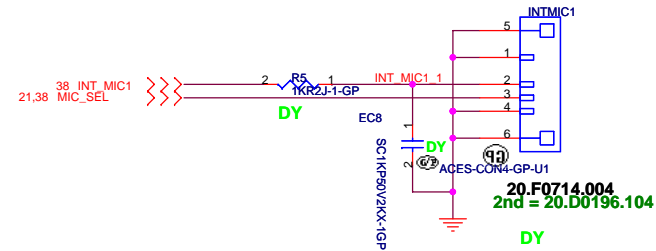
AUDIO OP AMPLIFIER



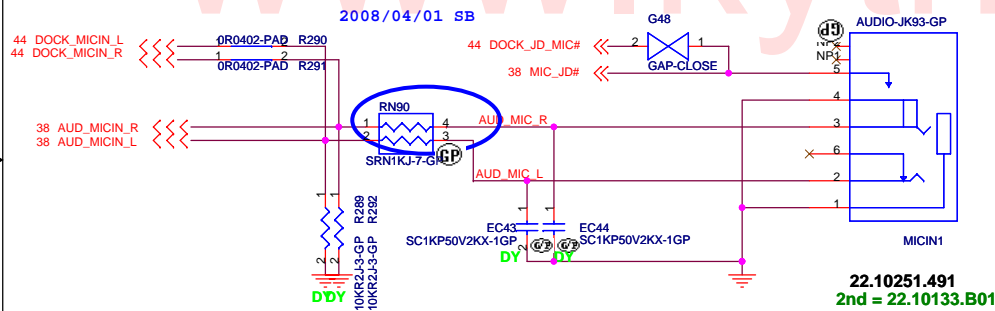
LINE IN



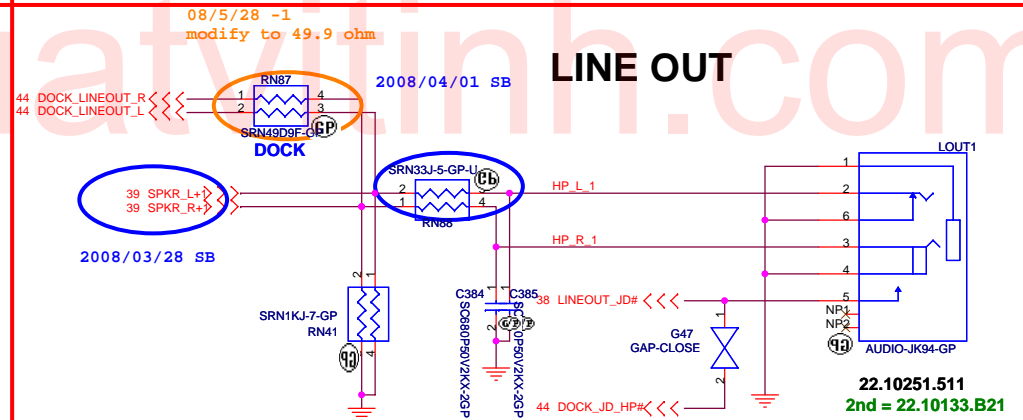
Internal Microphone



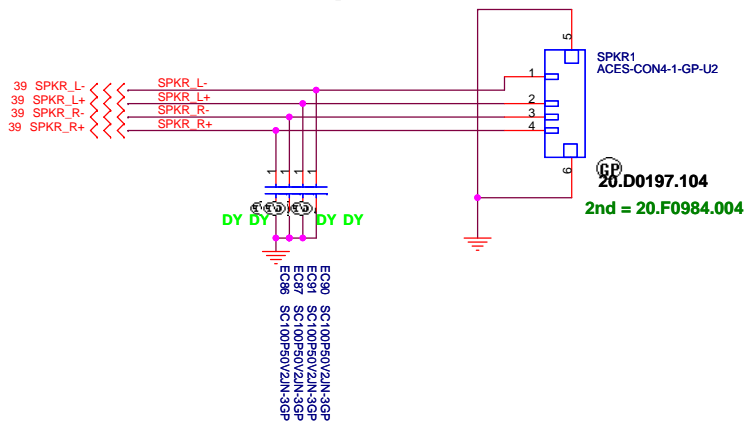
MIC IN



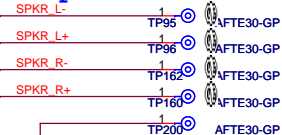
LINE OUT



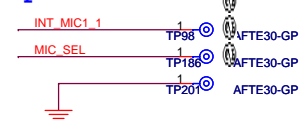
Internal Speaker



SPKR1 Conn. Test Point keep on connector side

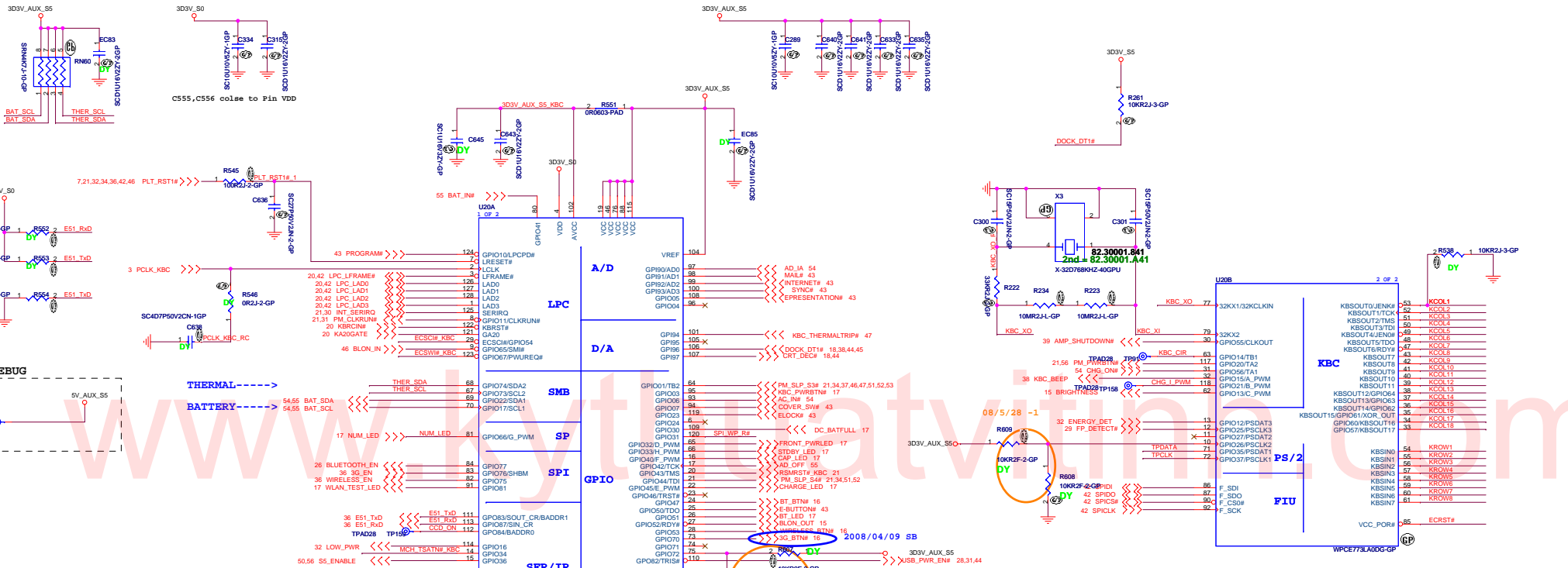


INTMIC1 Conn. Test Point keep on connetor side

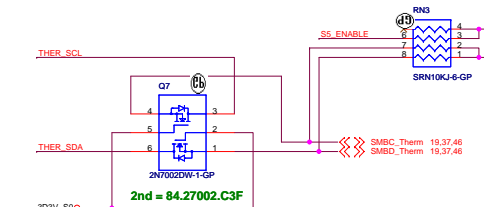


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Taipei Hsien 221, Taiwan, R.O.C.

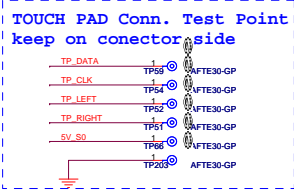
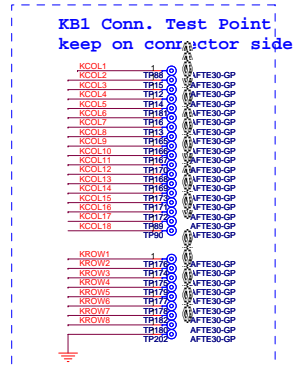
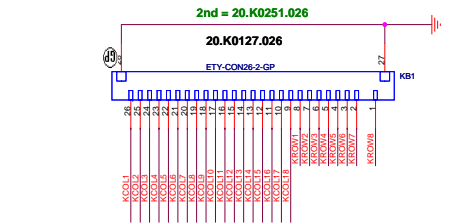
Title		
AUDIO JACK		
Size	Document Number	Rev
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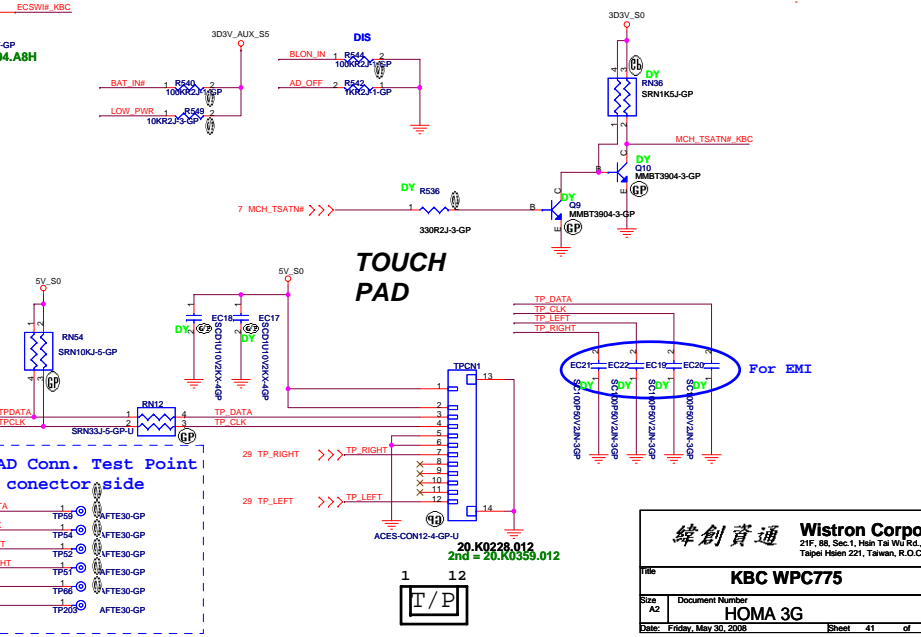
FOR KBC DEBUG

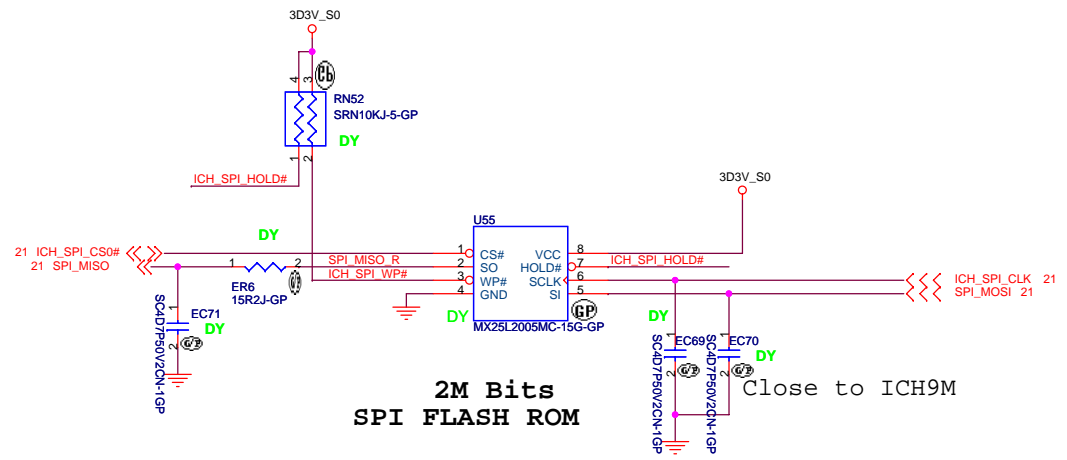
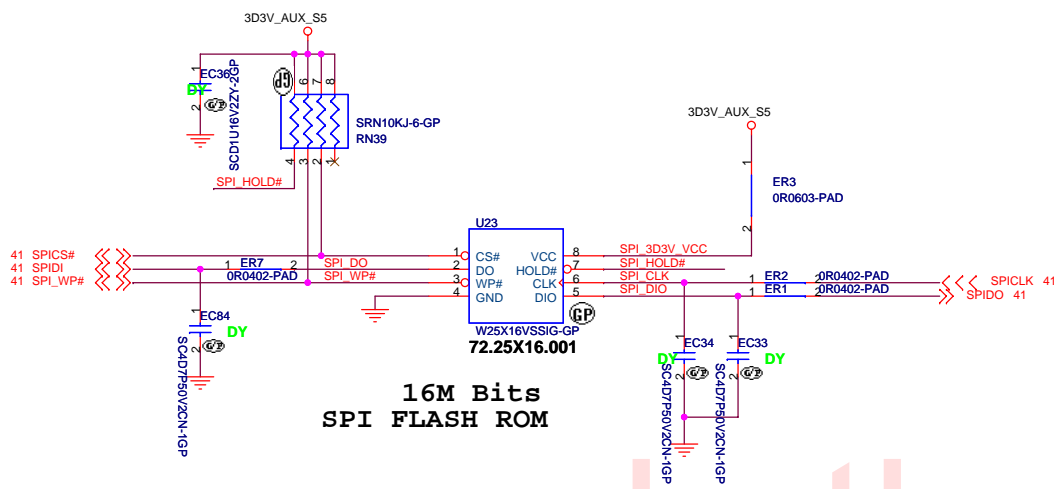


Internal Keyboard Connector



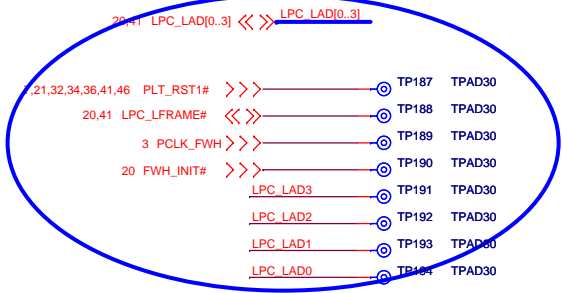
TOUCH PAD



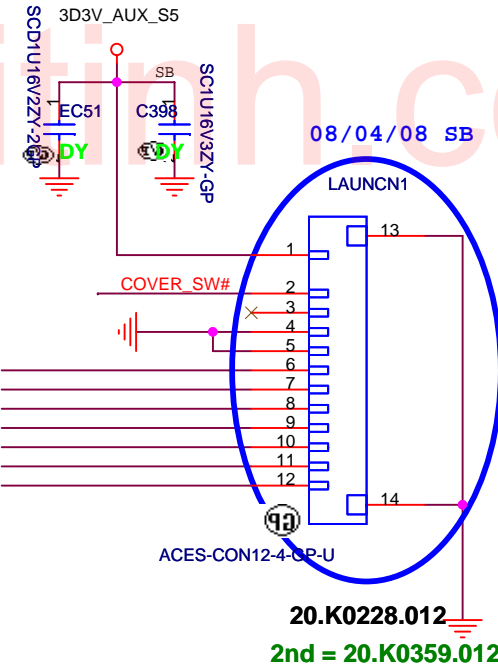
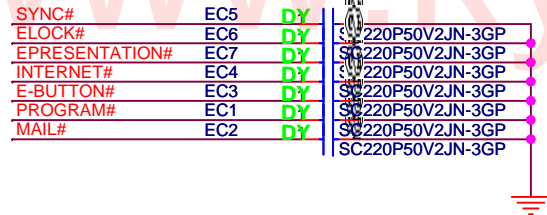
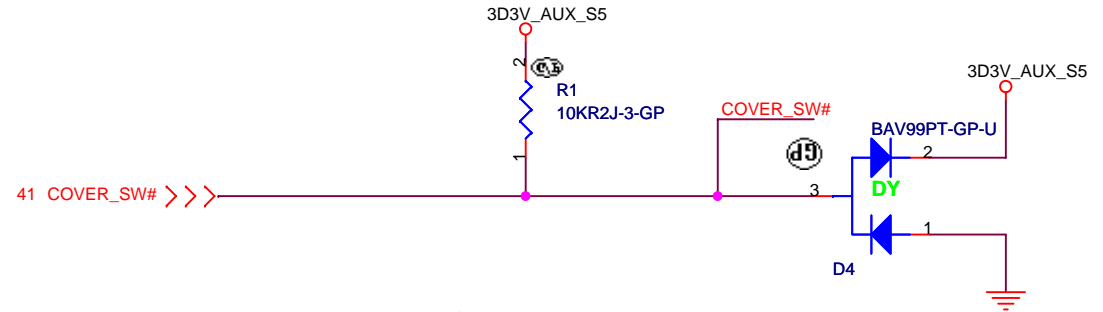
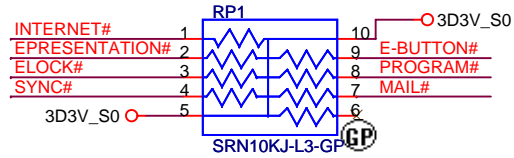


www.kythuativinh.com

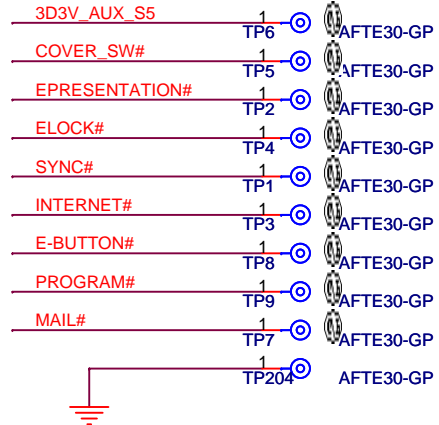
2008/04/11 SB
close to U21 position before this



Cover Up Switch



LAUNCH Conn. Test Point keep on conector side



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Title

LAUNCH

Size

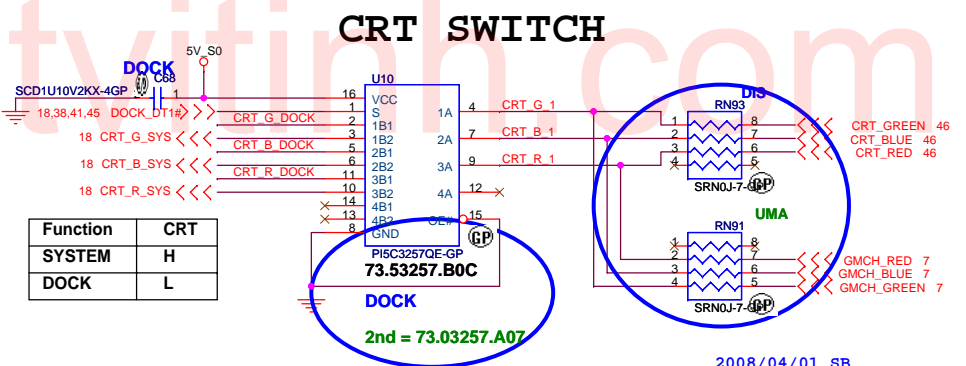
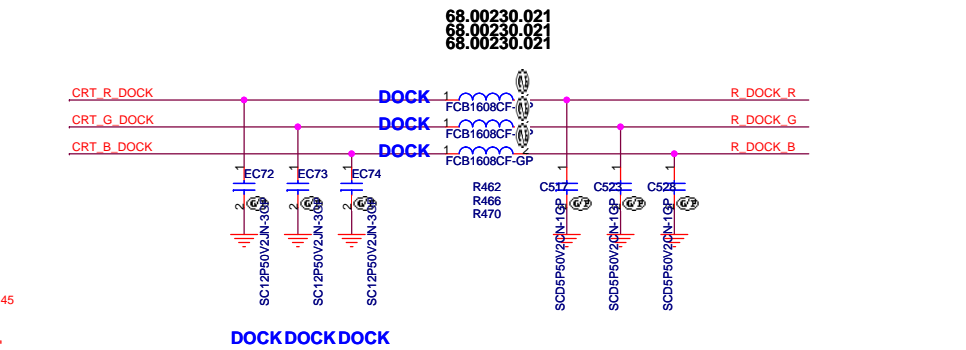
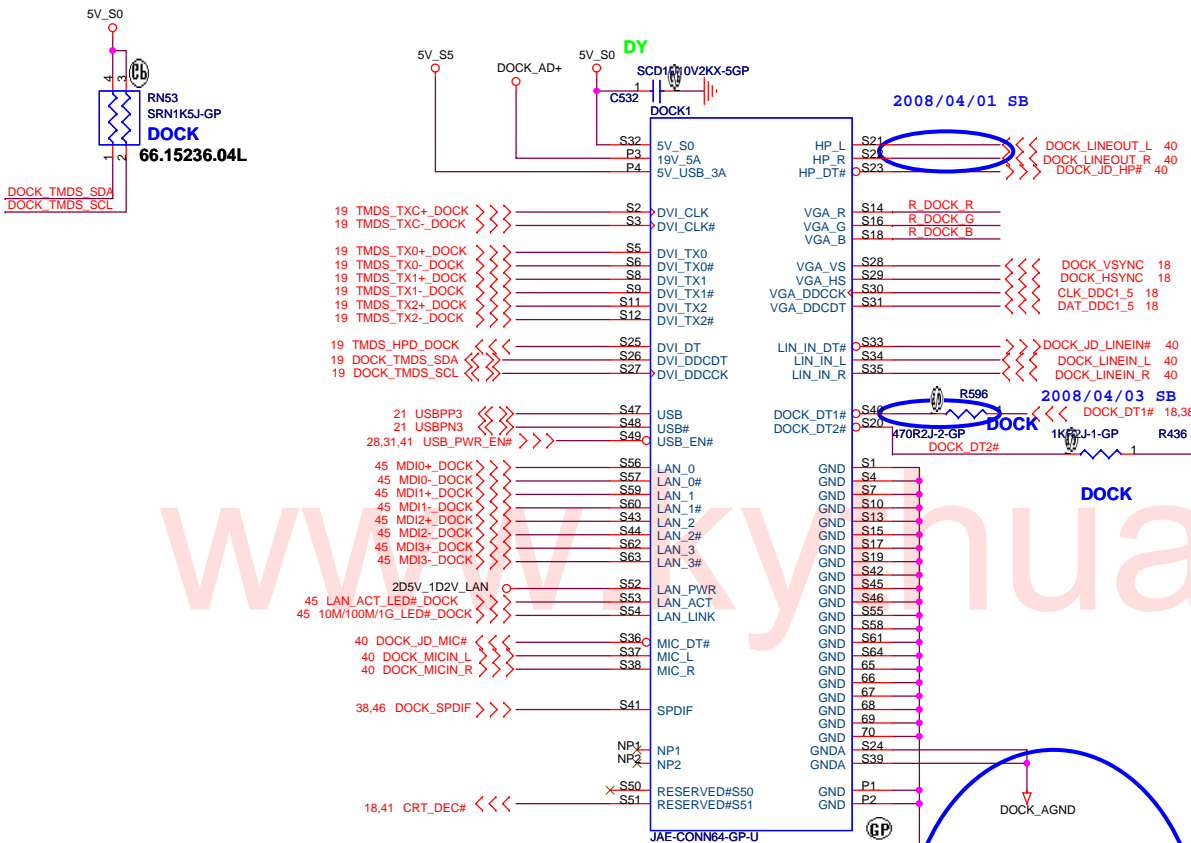
Document Number

HOMA 3G

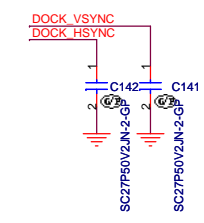
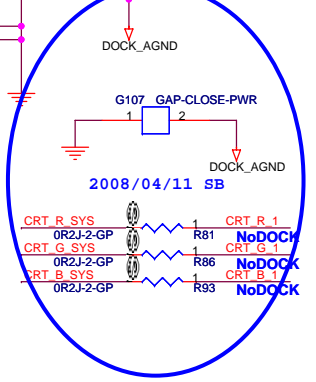
Rev
-1

Date: Friday, May 30, 2008

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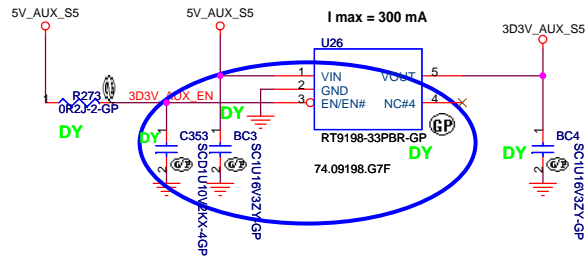
Function	CRT
SYSTEM	H
DOCK	L



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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

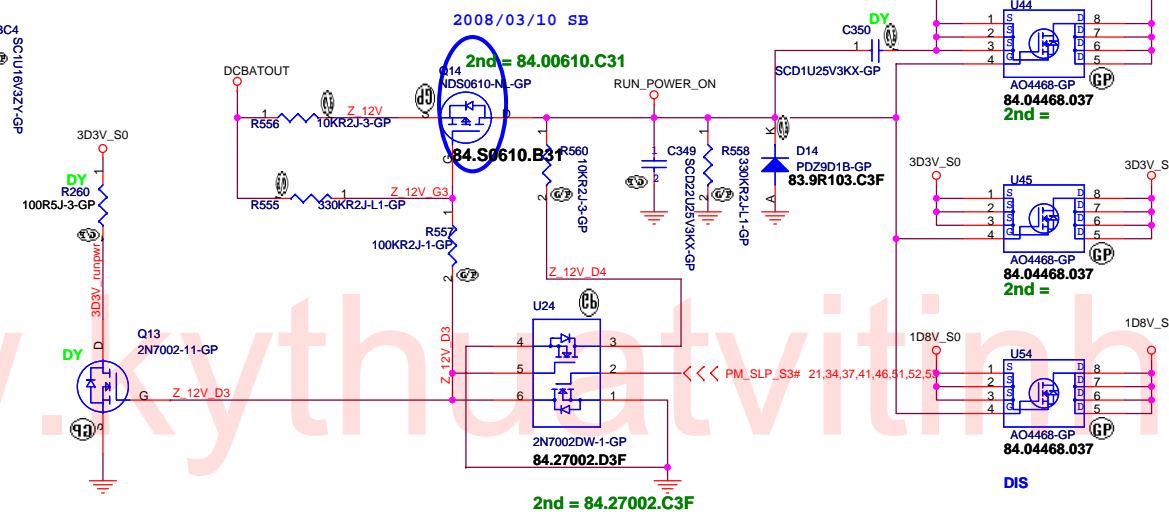
Aux Power

3D3V_AUX_S5



2008/04/02 SB

Run Power



2008/03/10 SB

2nd = 84.00610.C31

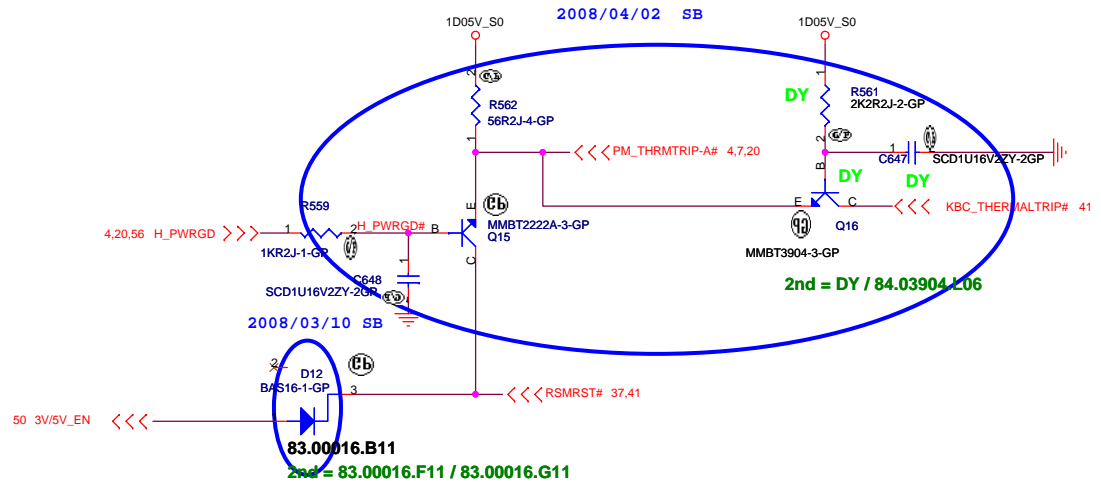
84.S0610.E3

2N7002DW-1-GP

84.27002.D3F

2nd = 84.27002.C3F

DIS



2008/04/02 SB

2nd = DY / 84.03904.L06

2008/03/10 SB

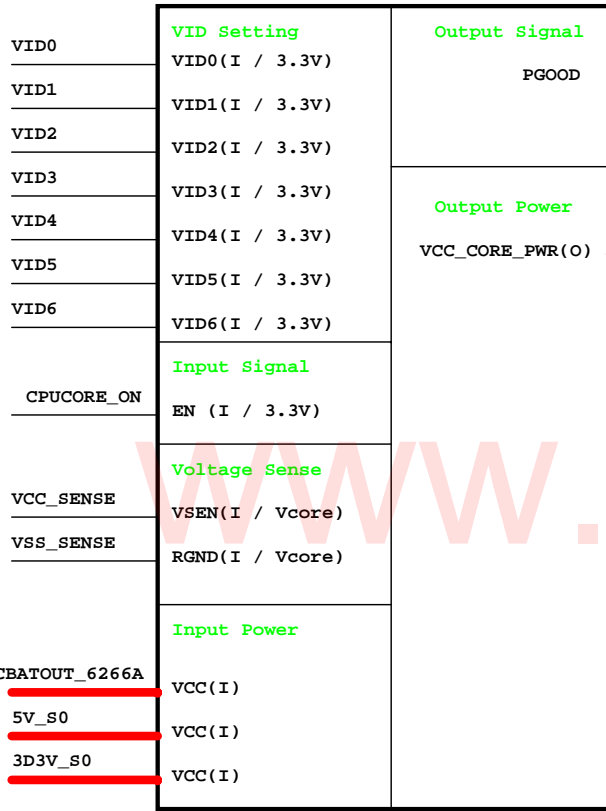
83.00016.B11

2nd = 83.00016.F11 / 83.00016.G11

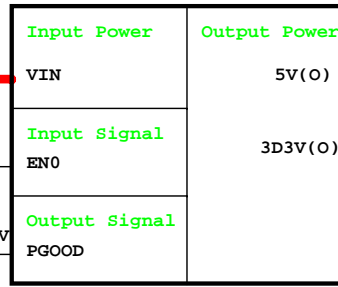
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Title RUN POWER and 3D3V_AUX_S5	
Size Document Number	Rev -1
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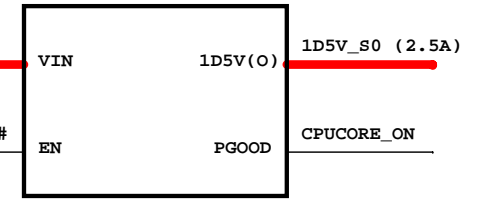
CPU_CORE
ISL6266A



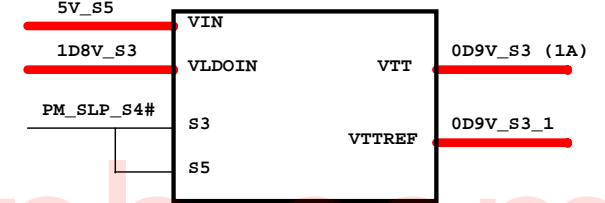
TPS51125
5V/3D3V



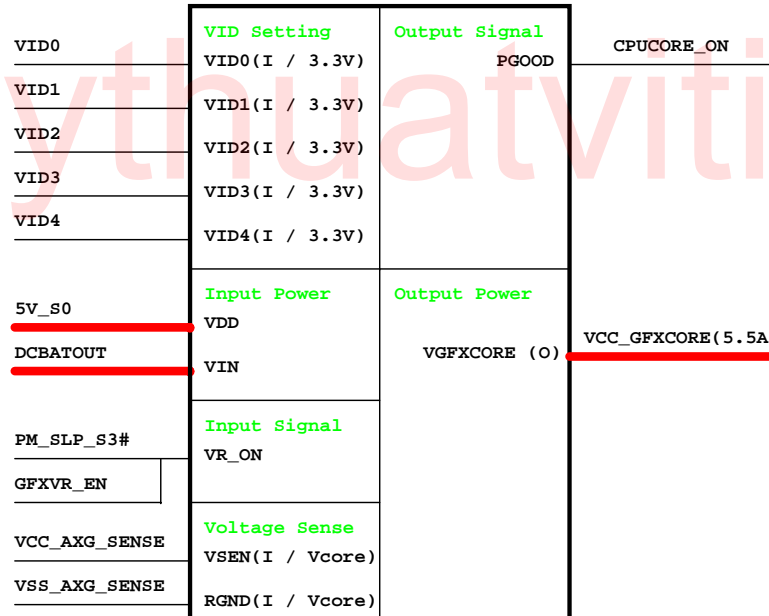
RT9018A
1D5V_S0



RT9026 0D9V_S0



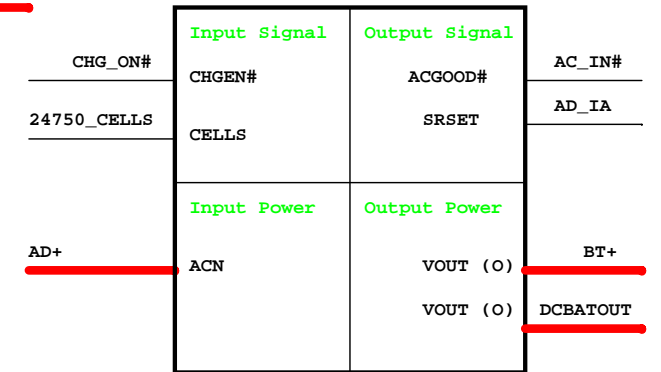
GFX_CORE
ISL6263A



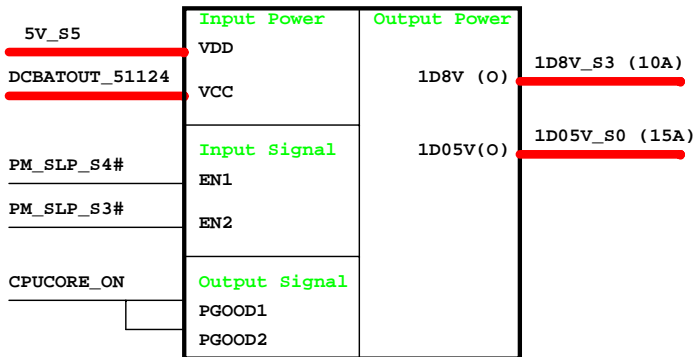
G9131 2D5V_S0



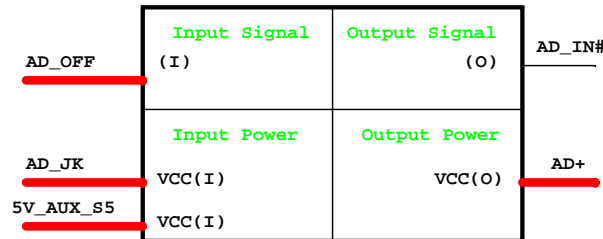
Charger BQ24750



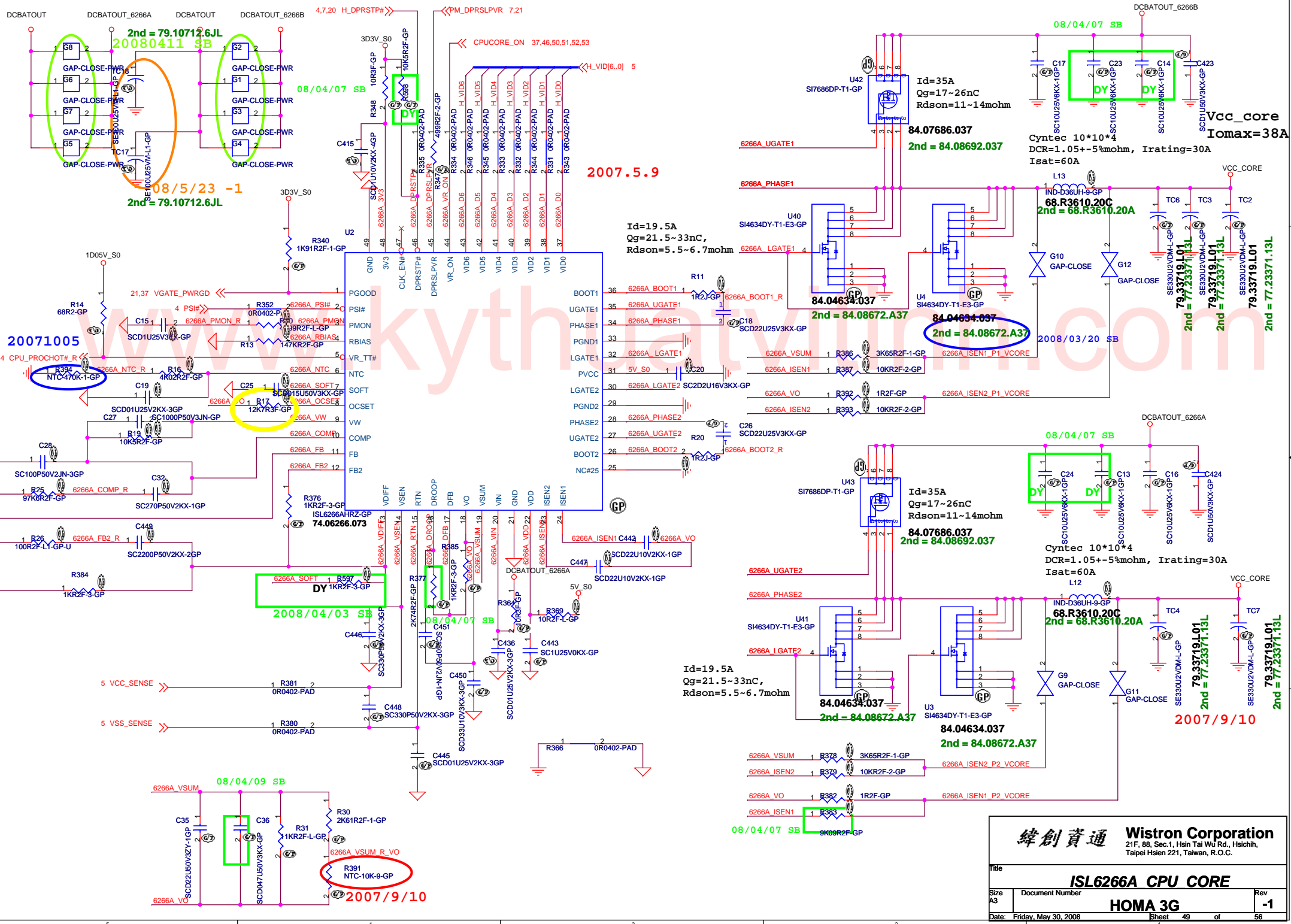
TPS51124
1D8V/1D05V

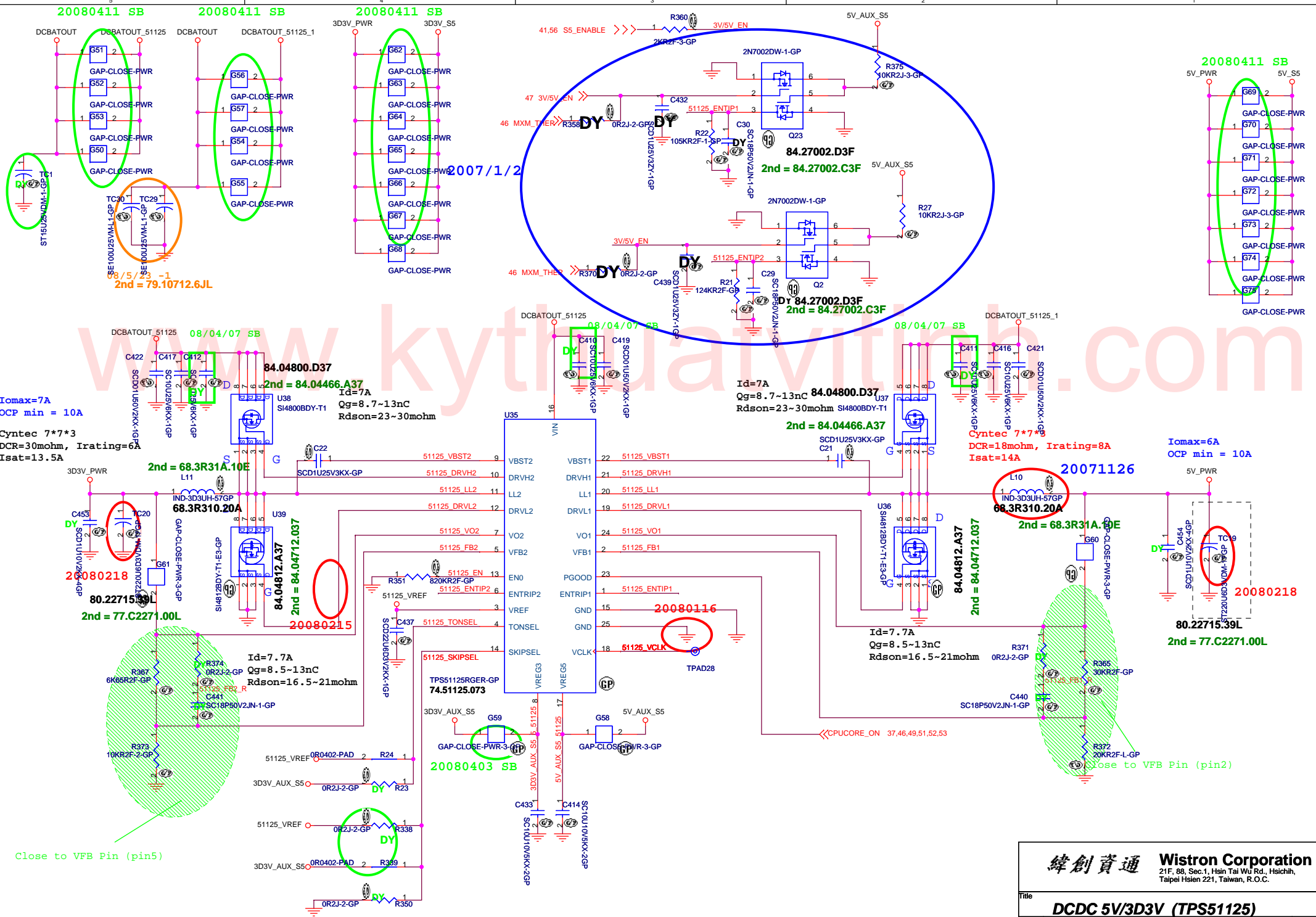


Adapter



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Iomax=7A
 OCP min = 10A
 Cyntec 7*7*3
 DCR=30mohm, Irating=6A
 Isat=13.5A

Iomax=6A
 OCP min = 10A

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Title	DCDC 5V/3D3V (TPS51125)		
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A3		HOMA 3G -1	
Date:	Friday, May 30, 2008	Sheet	50 of 56

Close to VFB Pin (pin5)

Close to VFB Pin (pin2)

2007/1/2

20071126

20080116

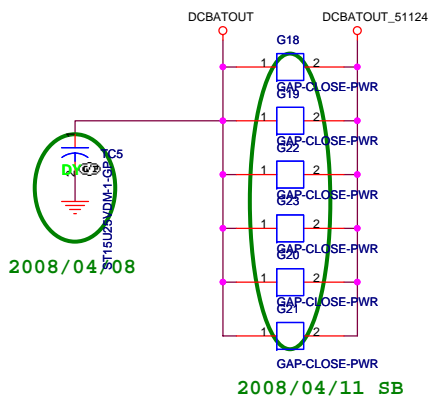
20080218

20080411 SB

20080411 SB

08/04/07 SB

08/04/07 SB



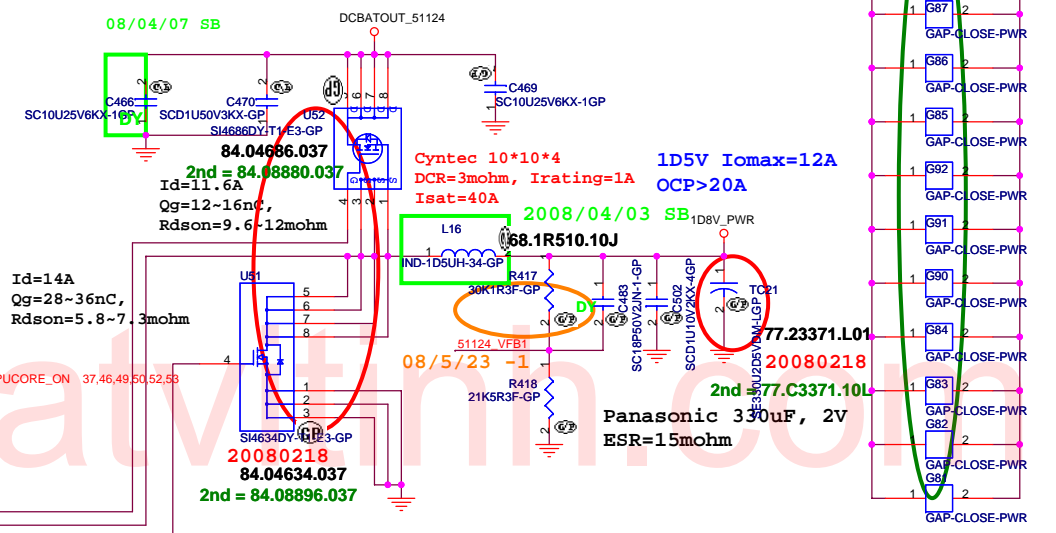
$$V_{trip}(mV) = R_{trip}(Kohm) * 10(uA)$$

$$I_{ocp} = (V_{trip}/R_{dson}) + ((1/(2*L*f)) * ((V_{in}-V_{out}) * V_{out}) / V_{in})$$

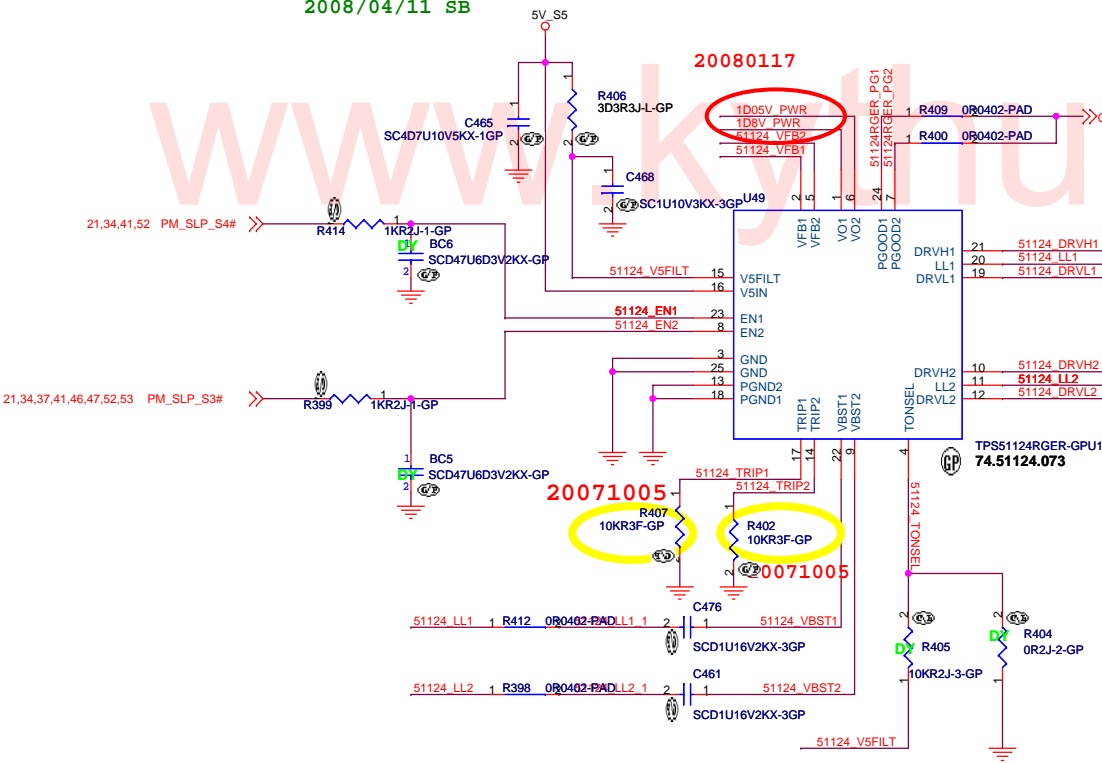
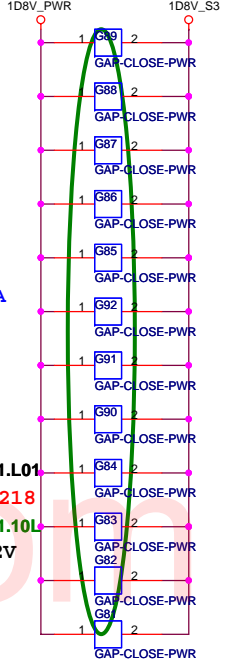
I/P cap: 10U 25V K1206 X5R/ 78.10622.52L

2008/04/08

2008/04/11 SB



2008/04/11 SB



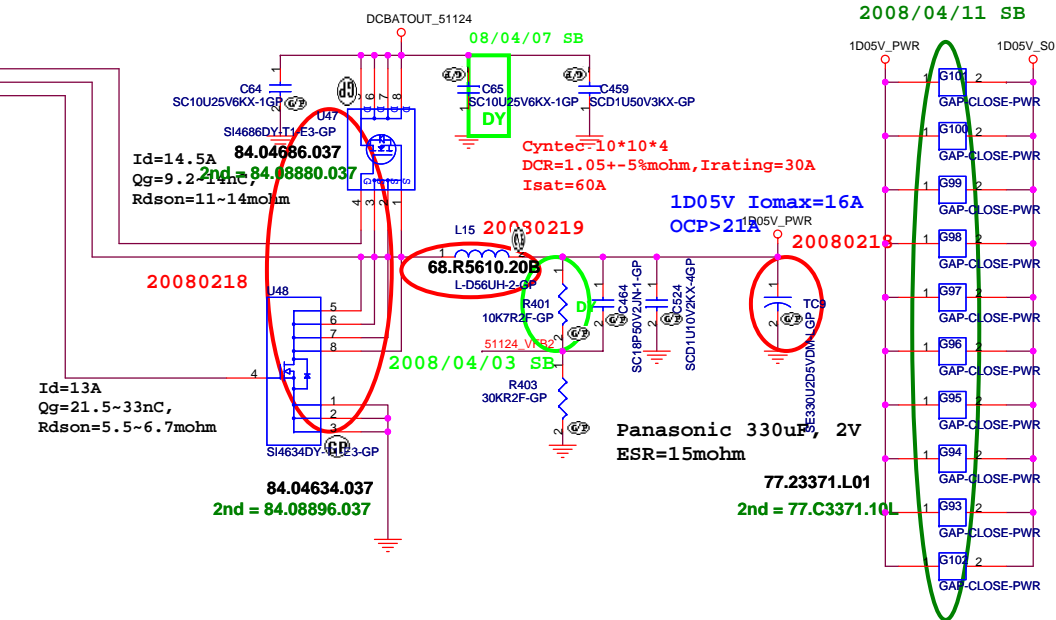
21,34,41,52 PM_SLP_S4#

21,34,37,41,46,47,52,53 PM_SLP_S3#

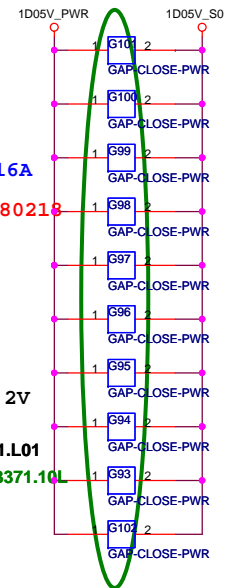
	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

$$V_{out} = 0.758V * (R1+R2) / R2 \text{ --> PWM mode}$$

$$V_{out} = 0.764V * (R1+R2) / R2 \text{ --> Skip Mode}$$

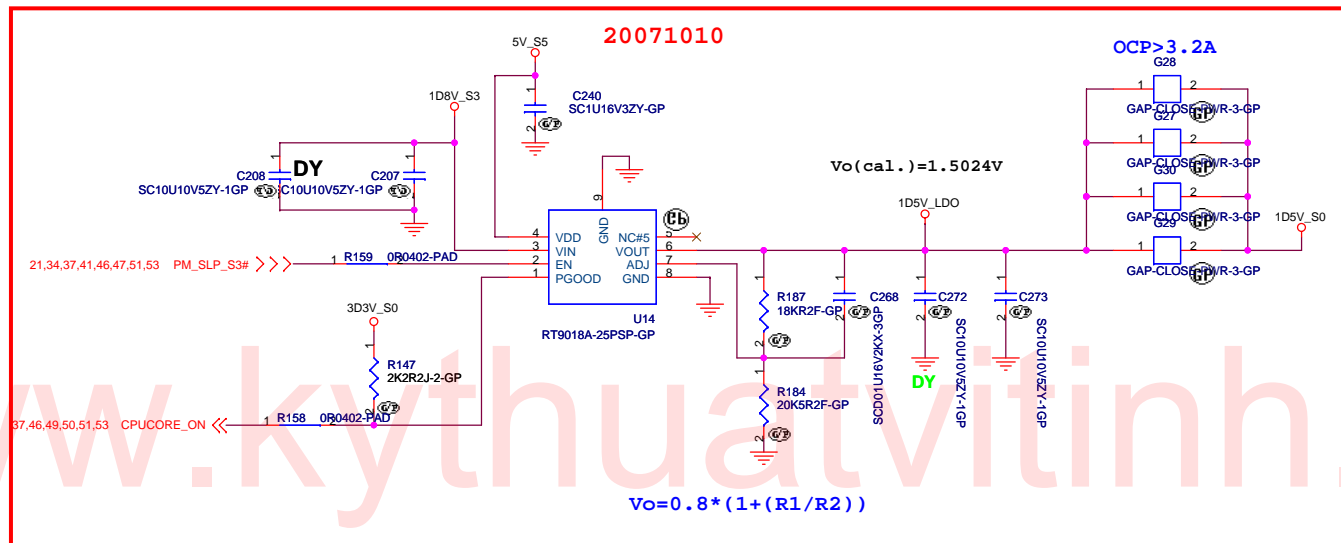


2008/04/11 SB

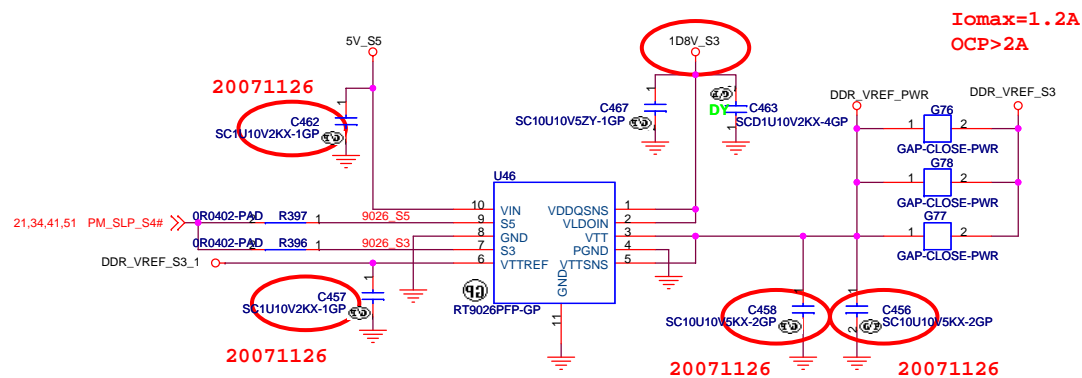
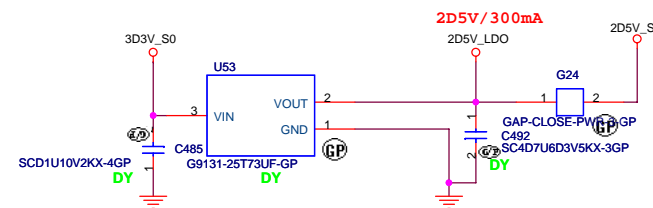


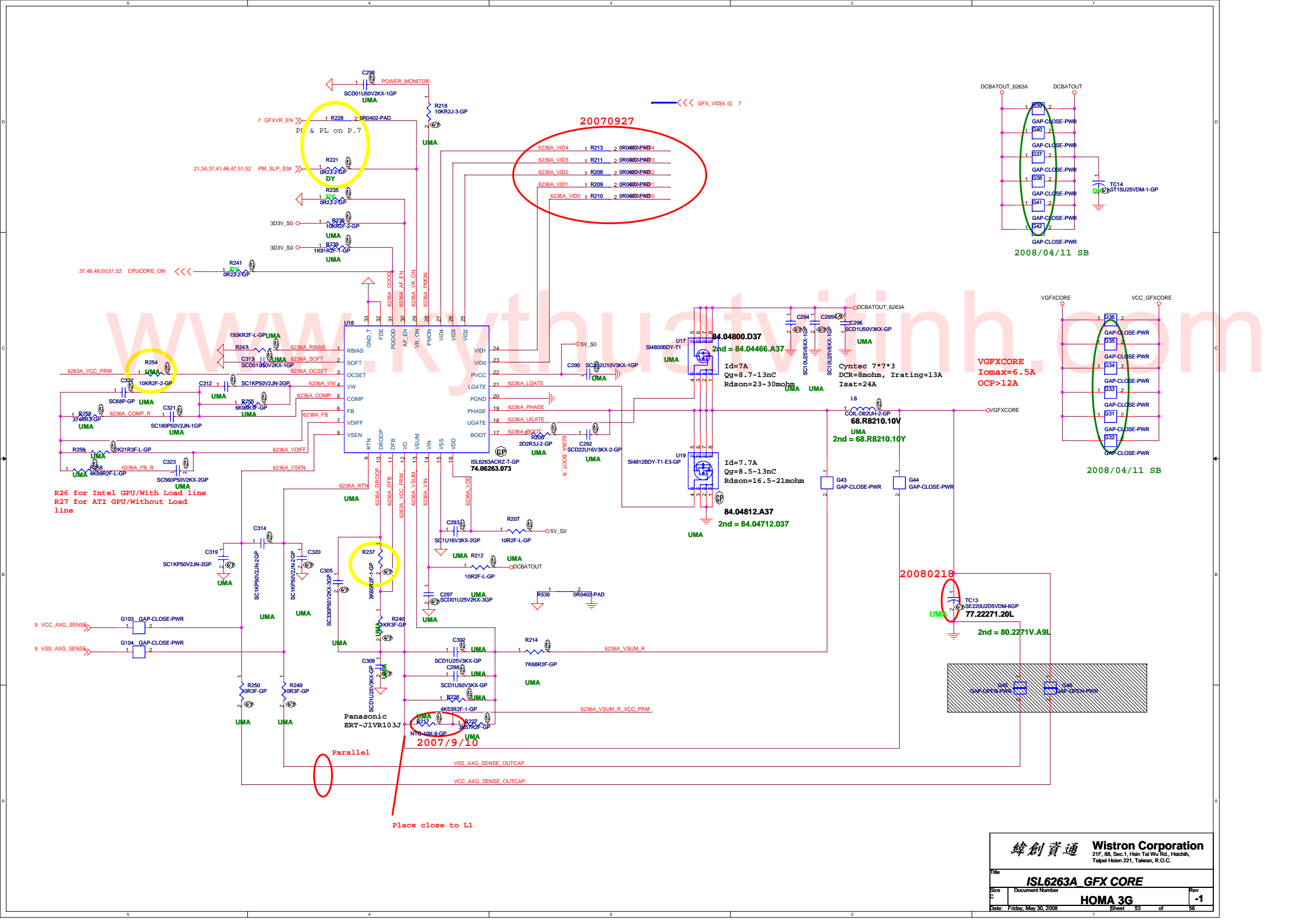
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1D5V_S0
Iomax=2.5A



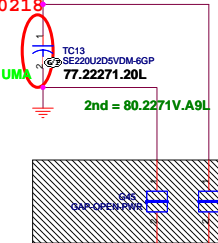
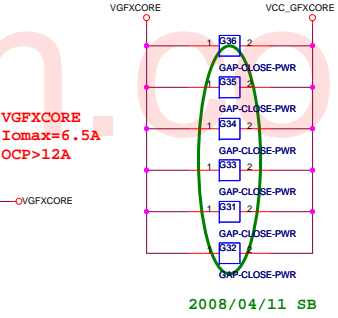
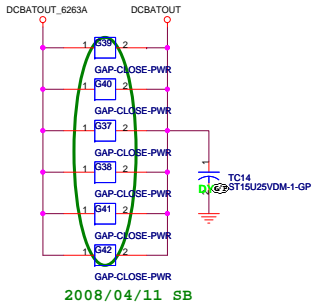
2D5V_S0
Iomax=0.3A





20070927

6236A_VID4 1 R213 2 0R0402-PAD-4
 6236A_VID3 1 R211 2 0R0402-PAD-3
 6236A_VID2 1 R208 2 0R0402-PAD-2
 6236A_VID1 1 R209 2 0R0402-PAD-1
 6236A_VID0 1 R210 2 0R0402-PAD-0



R26 for Intel GPU/With Load line
 R27 for ATI GPU/Without Load line

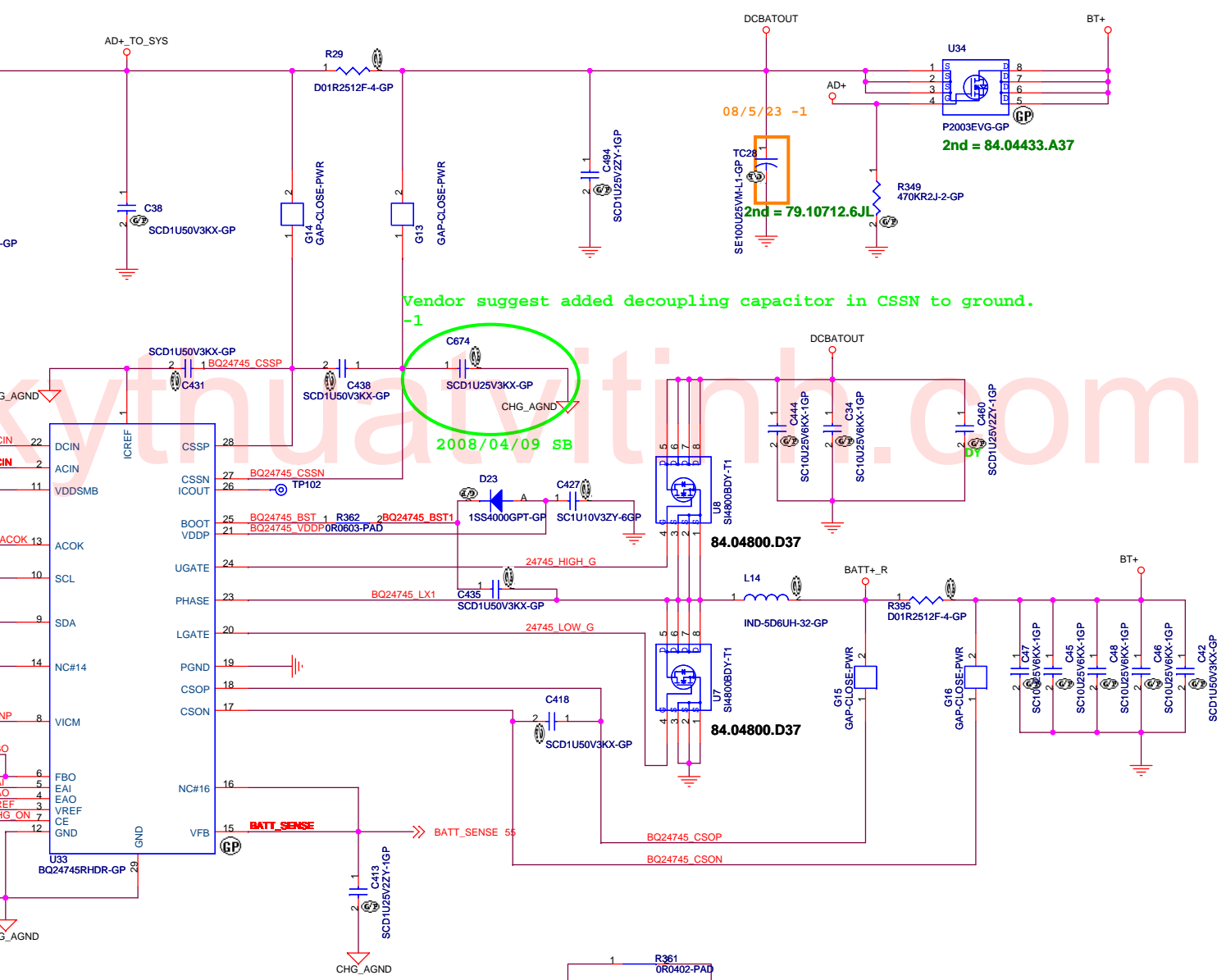
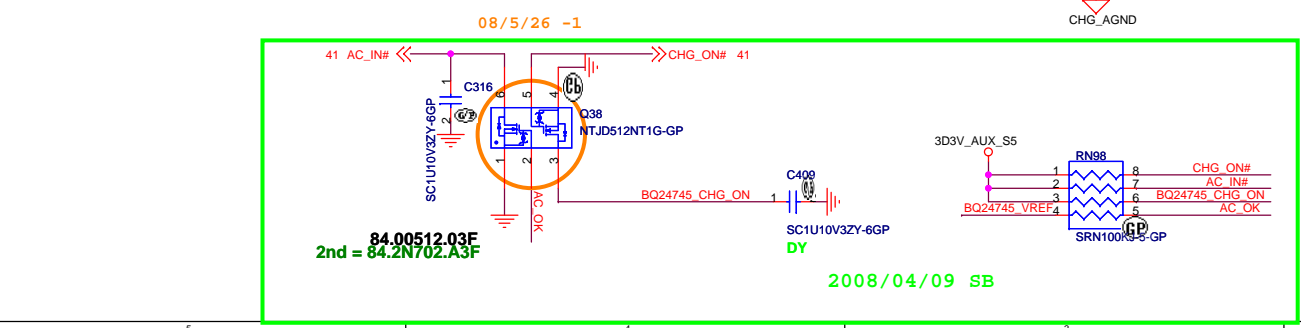
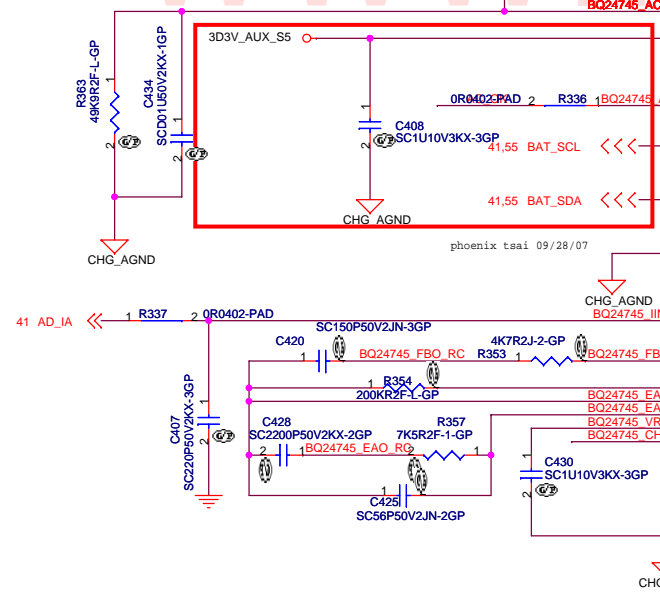
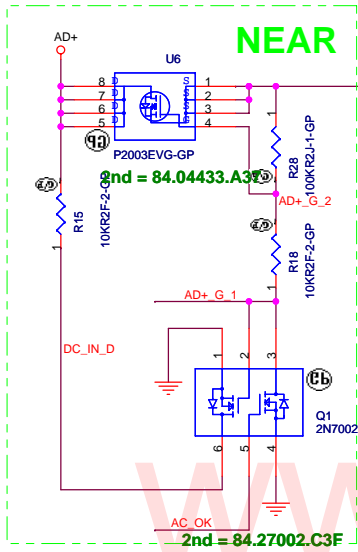
Parallel

Place close to L1

2007/9/10

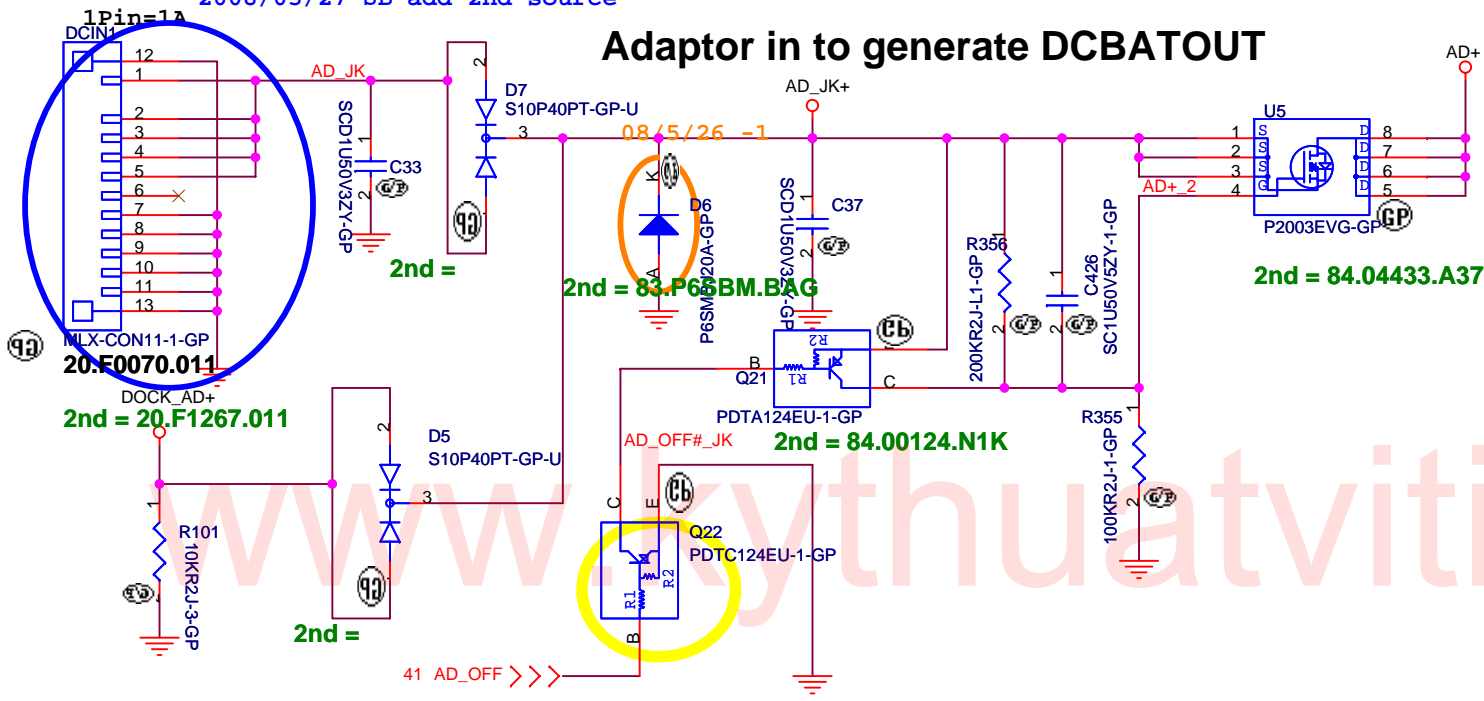
VSS_AGX_SENSE_OUTCAP

VCC_AGX_SENSE_OUTCAP

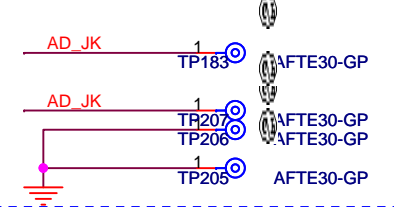


2008/03/27 SB add 2nd source

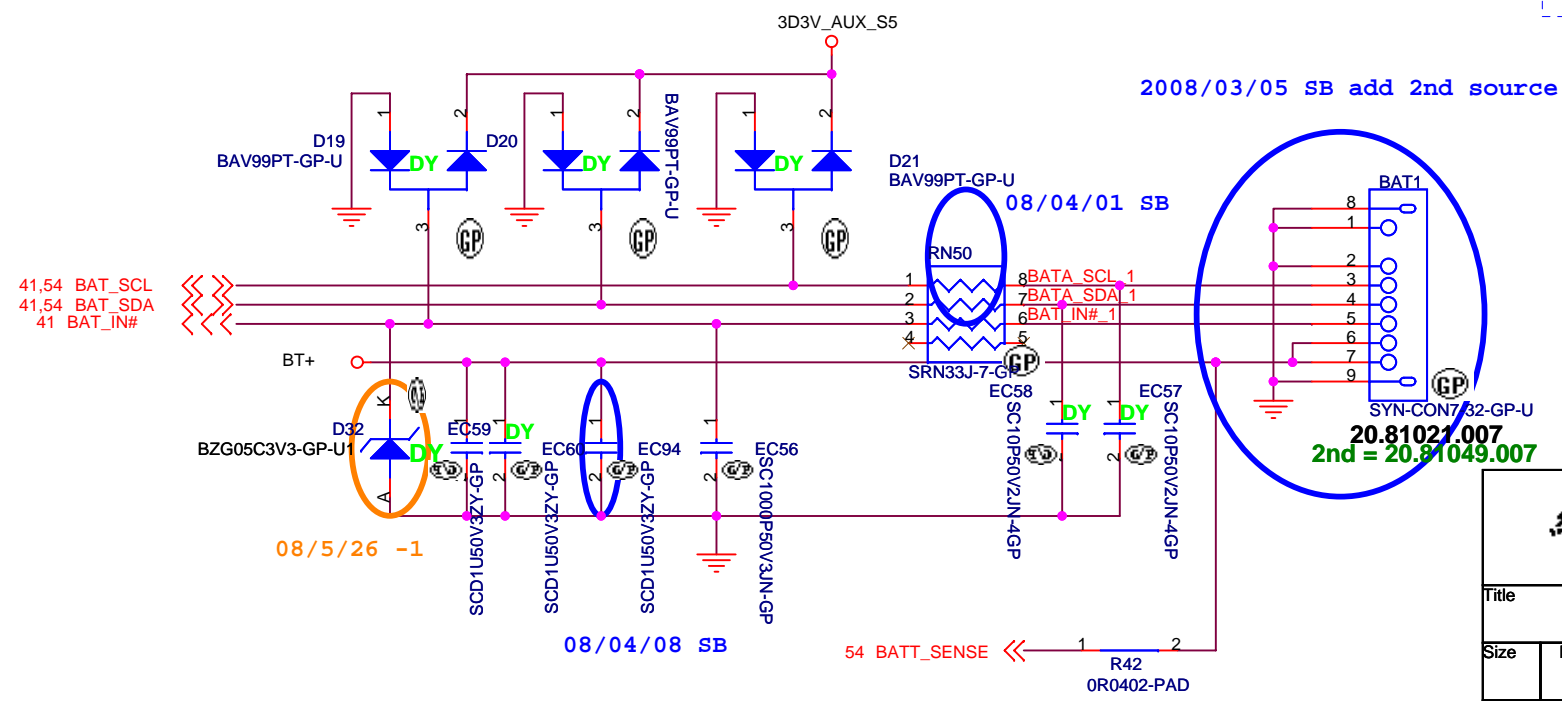
Adaptor in to generate DCBATOUT



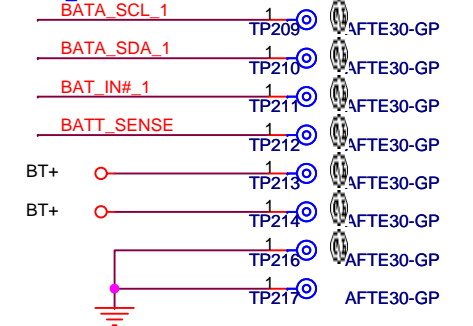
KB Conn. Test Point keep on connector side



MAIN BATTERY CONNECTOR

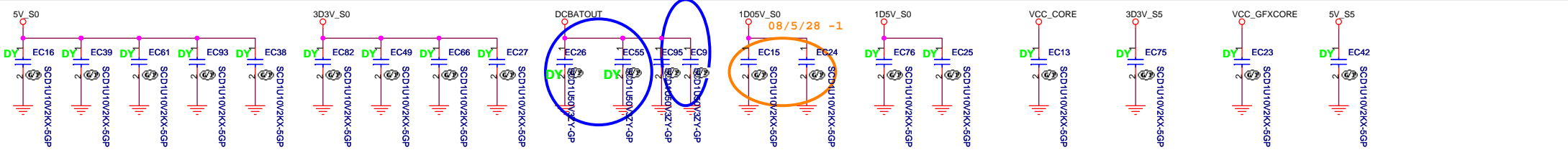


BAT1 Conn. Test Point keep on connector side

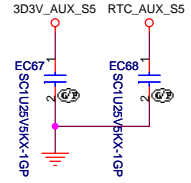
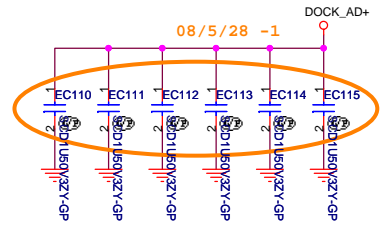


緯創資通 **Wistron Corporation**
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

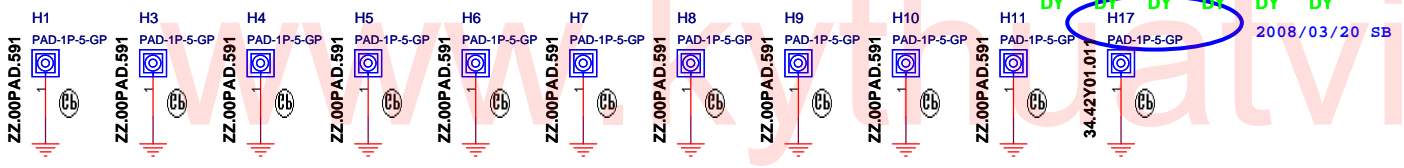
Title			AD&BTY CONNECTER		
Size	Document Number				Rev
HOMA 3G					-1
Date:	Friday, May 30, 2008			Sheet	55 of 56



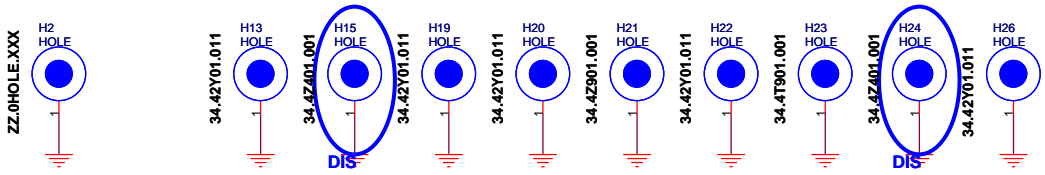
2008/04/11 SB 2008/04/08 SB



Stand off Location



2008/04/14 SB



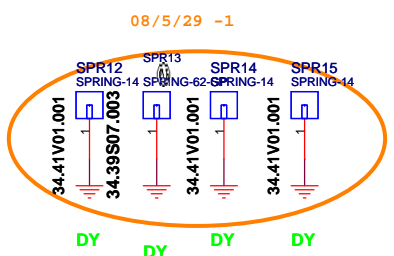
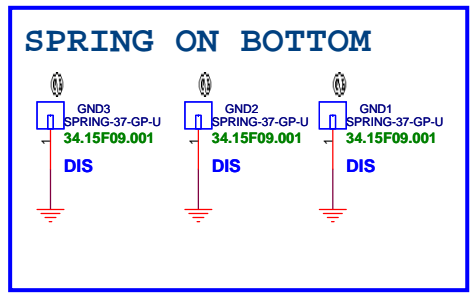
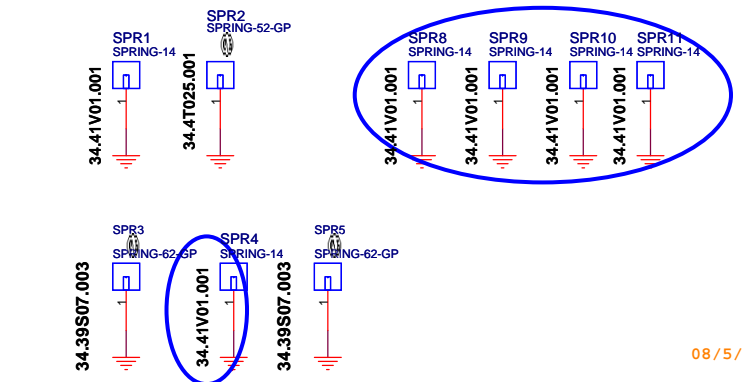
2008/04/09 SB

2008/04/14 SB

Check test point

3D3V_S0	TP104	AFTE30-GP
3D3V_AUX_S5	TP101	AFTE30-GP
3D3V_S5	TP103	AFTE30-GP
5V_S5	TP105	AFTE30-GP
21.41 PM_PWRBTN#	TP107	AFTE30-GP
4.20.47 H_PWRGD	TP108	AFTE30-GP
41.50 S5_ENABLE	TP106	AFTE30-GP
4.6 H_CPURST#	TP109	AFTE30-GP

Test Point放在Dimm Door打開可量測處



2008/04/14 SB