

Compal Confidential

PEW52 M/B Schematics Document

Intel Penryn Processor with Cantiga + DDRIII + ICH9M + ATI Park

2010-08-09

REV: 0.2

Dr-Bios.com

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.75VS	0.75V power rail for DDR	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for DDR	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8VS power rail for LVDS	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail for SB	ON	ON	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
+VGA_CORE	VGA power	ON	OFF	OFF
+1.0VSDGPU	VGA power	ON	OFF	OFF
+1.5VSDGPU	VGA power	ON	OFF	OFF
+1.8VSDGPU	VGA power	ON	OFF	OFF
+3VSDGPU	VGA power	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	CPU EMC1402-1	0100 1100 b
EEPROM(24C16/02)	1010 000X b	VGA ADM1032-2	0100 1101 b
GMT G781-1	1001 101X b		

EC SM Bus2 address

ICH9M SM Bus address

Device	Address
Clock Generator (ICS9LPRS387, SLG8SP556V)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

BTO Option

PLEASE REFER PAGE 52

USB table

	UHCI1	Port0	MB USB Conn.
EHCI1	UHCI2	Port1	USB/B Conn.
		Port2	
		Port3	CMOS Camera
		Port4	Card Reader
		Port5	
EHCI2	UHCI3	Port6	USB/B Conn.
		Port7	
		Port8	Blue Tooth
		Port9	
		Port10	Wireless Card
		Port11	

PCIE table

PCIE port1	
PCIE port2	Wireless Card
PCIE port3	PCIE LAN
PCIE port4	
PCIE port5	
PCIE port6	

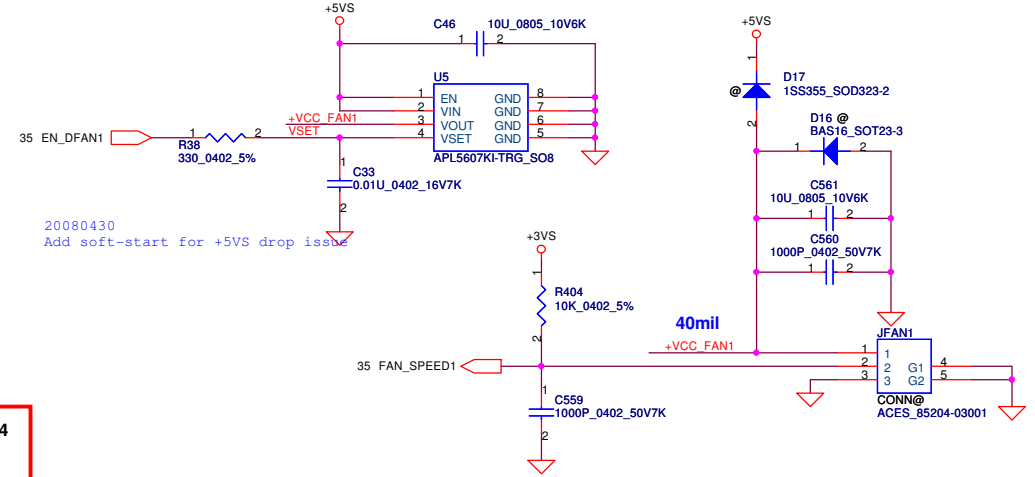
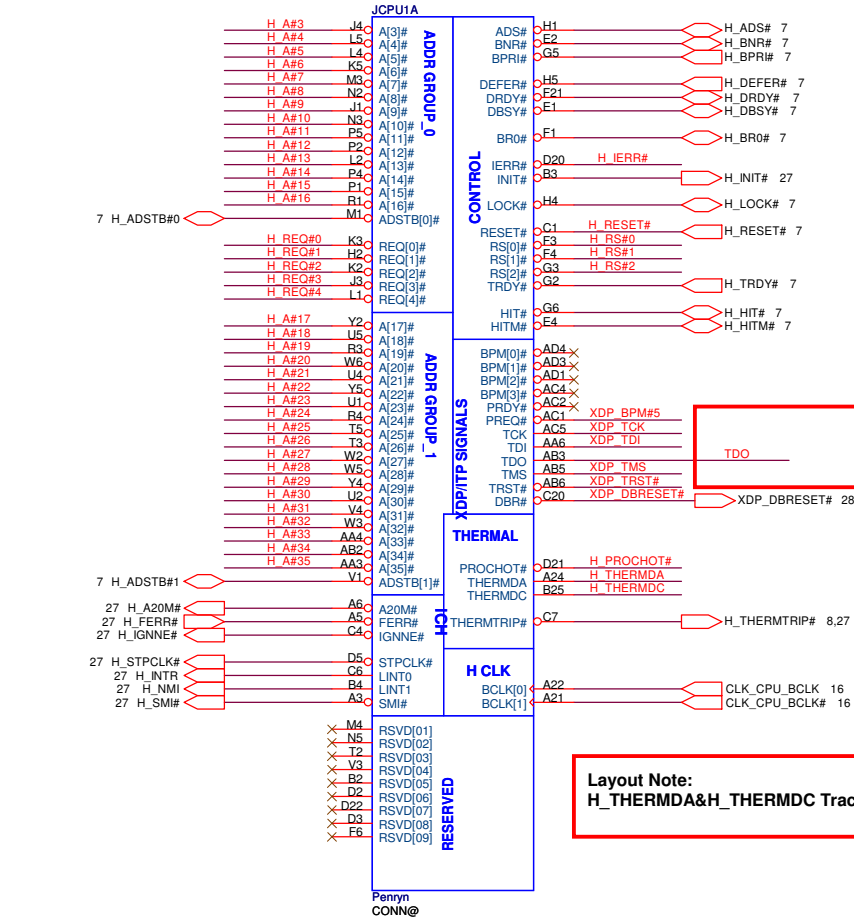
SATA table

SATA port0	HDD
SATA port1	ODD
SATA port2	
SATA port3	
SATA port4	
SATA port5	

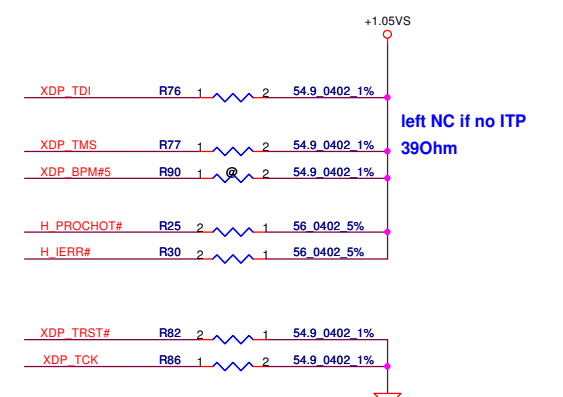
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- 7 H_A#[3..35] H_A#[3..35]
- 7 H_REQ#[0..4] H_REQ#[0..4]
- 7 H_RS#[0..2] H_RS#[0..2]

FAN1 Conn

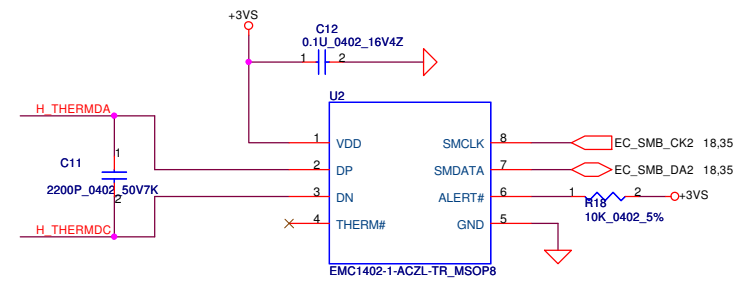
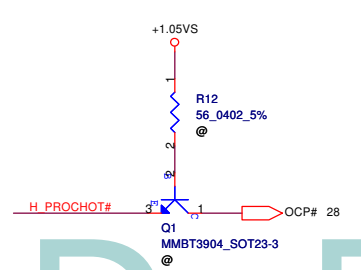


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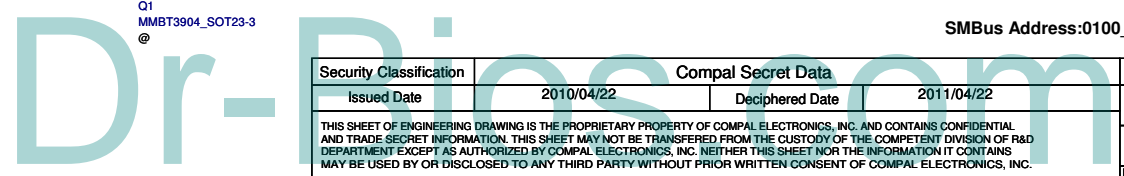


Layout Note:
H_THERMDA&H_THERMDC Trace / Space = 10 / 10 mil

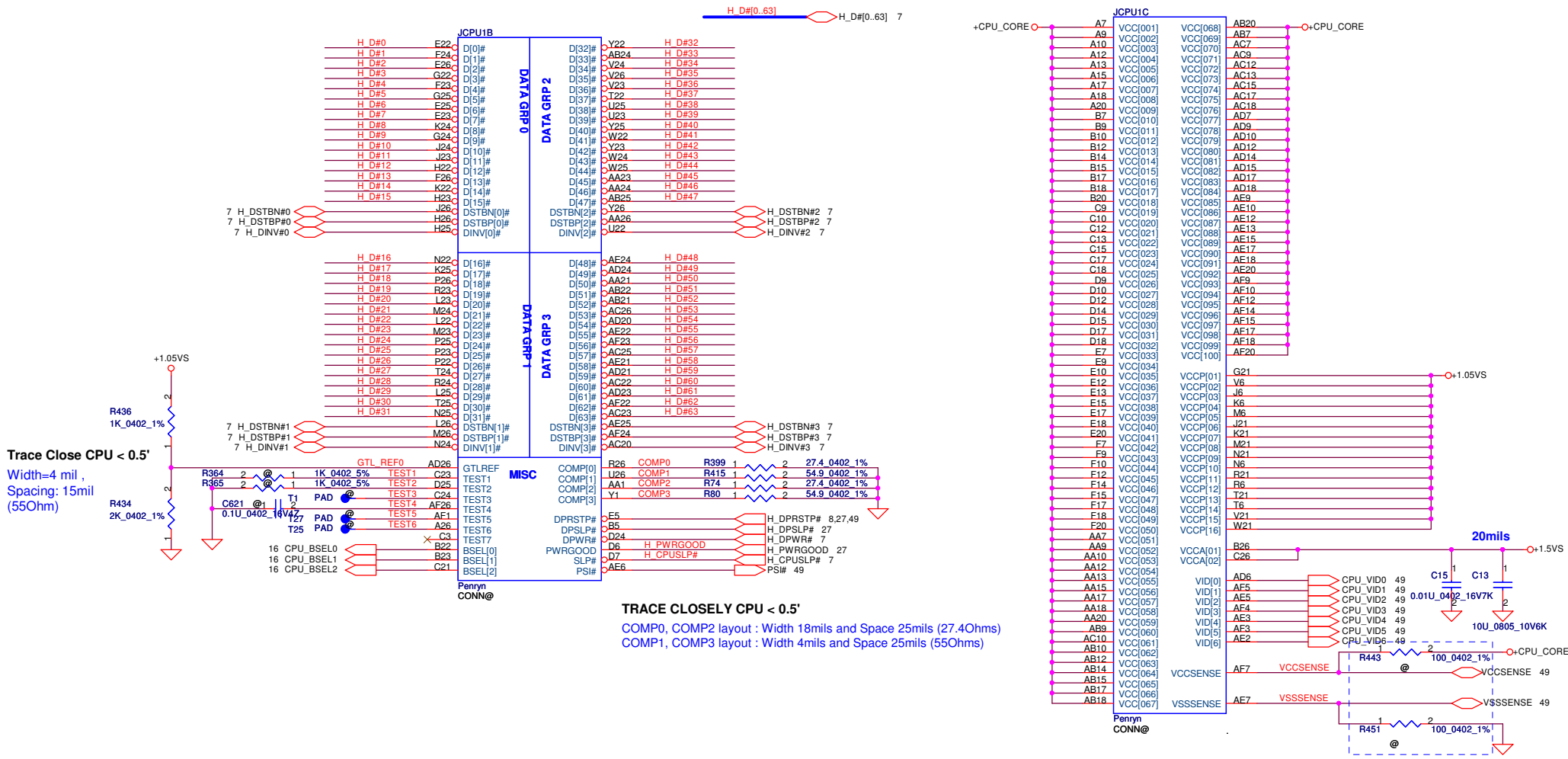
BSEL2	BSEL1	BSEL0	BCLK
0	0	0	266
0	1	0	200
0	1	1	166



SMBus Address:0100_1100b



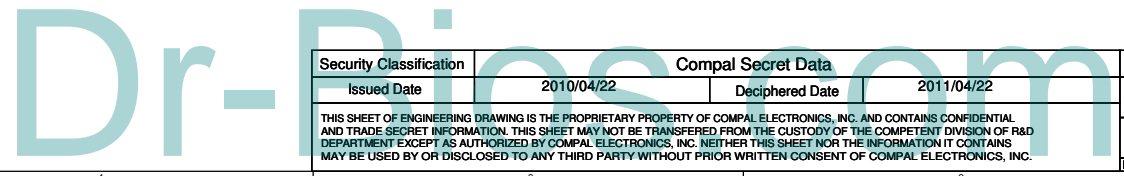
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Trace Close CPU < 0.5'
 Width=4 mil,
 Spacing: 15mil
 (55Ohm)

TRACE CLOSELY CPU < 0.5'
 COMP0, COMP2 layout : Width 18mils and Space 25mils (27.4Ohms)
 COMP1, COMP3 layout : Width 4mils and Space 25mils (55Ohms)

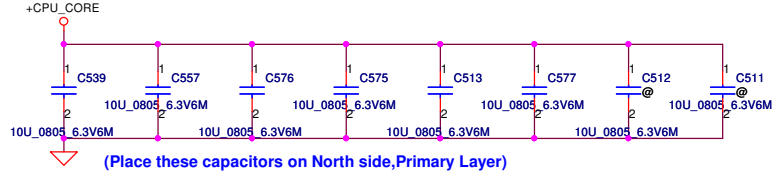
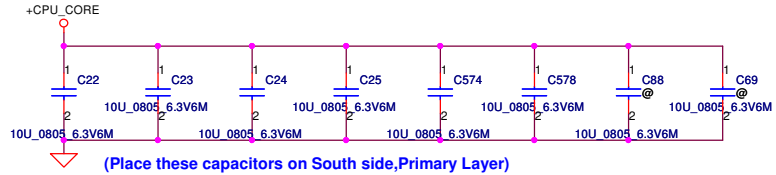
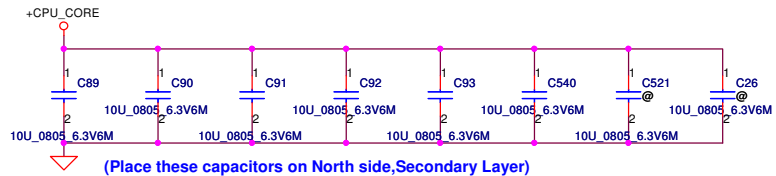
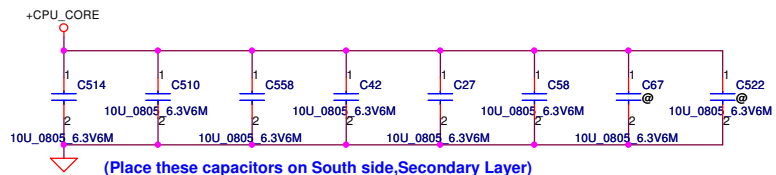
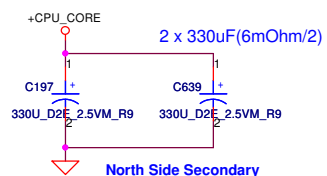
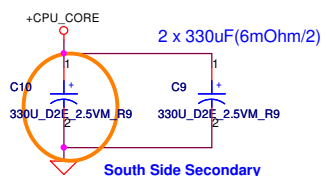
R443 & R451 改不上件,0702



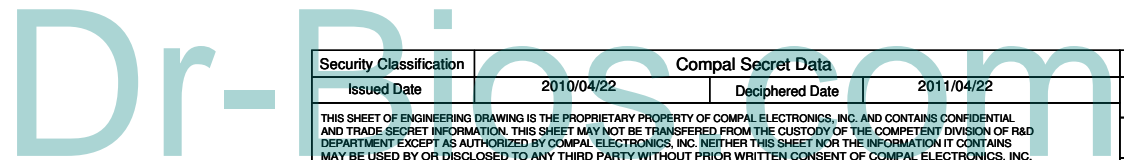
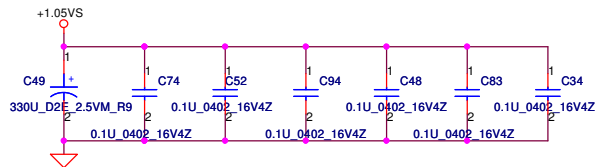
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JCPUID		
A4	VSSJ001	P6
A8	VSSJ002	P21
A11	VSSJ003	P24
A14	VSSJ004	R2
A16	VSSJ005	R5
A19	VSSJ006	R22
A23	VSSJ007	R25
AF2	VSSJ008	T1
B6	VSSJ009	T4
B8	VSSJ010	T23
B11	VSSJ011	T26
B13	VSSJ012	U3
B16	VSSJ013	U6
B19	VSSJ014	U21
B21	VSSJ015	U24
B24	VSSJ016	V2
C5	VSSJ017	V5
C8	VSSJ018	V22
C11	VSSJ019	V25
C14	VSSJ020	W1
C16	VSSJ021	W4
C19	VSSJ022	W23
C2	VSSJ023	W26
C22	VSSJ024	Y3
C25	VSSJ025	Y6
D1	VSSJ026	Y21
D4	VSSJ027	Y24
D8	VSSJ028	AA2
D11	VSSJ029	AA5
D13	VSSJ030	AA8
D16	VSSJ031	AA11
D19	VSSJ032	AA14
D23	VSSJ033	AA16
D26	VSSJ034	AA19
E3	VSSJ035	AA22
E6	VSSJ036	AA25
E8	VSSJ037	AB1
E11	VSSJ038	AB4
E14	VSSJ039	AB8
E16	VSSJ040	AB11
E19	VSSJ041	AB13
E21	VSSJ042	AB16
E24	VSSJ043	AB19
F5	VSSJ044	AB23
F8	VSSJ045	AB26
F11	VSSJ046	AC3
F13	VSSJ047	AC6
F16	VSSJ048	AC8
F19	VSSJ049	AC11
F2	VSSJ050	AC14
F22	VSSJ051	AC16
F25	VSSJ052	AC19
G4	VSSJ053	AC21
G1	VSSJ054	AC24
G23	VSSJ055	AD2
G26	VSSJ056	AD5
H3	VSSJ057	AD8
H6	VSSJ058	AD11
H21	VSSJ059	AD13
H24	VSSJ060	AD16
J2	VSSJ061	AD19
J5	VSSJ062	AD22
J22	VSSJ063	AD25
J25	VSSJ064	AE1
K1	VSSJ065	AE4
K4	VSSJ066	AE8
K23	VSSJ067	AE11
K26	VSSJ068	AE14
L3	VSSJ069	AE16
L6	VSSJ070	AE19
L21	VSSJ071	AE23
L24	VSSJ072	AE26
M2	VSSJ073	A2
M5	VSSJ074	AF6
M22	VSSJ075	AF8
M25	VSSJ076	AF11
N1	VSSJ077	AF13
N4	VSSJ078	AF16
N23	VSSJ079	AF19
N26	VSSJ080	AF21
P3	VSSJ081	A25
	VSSJ163	AE25

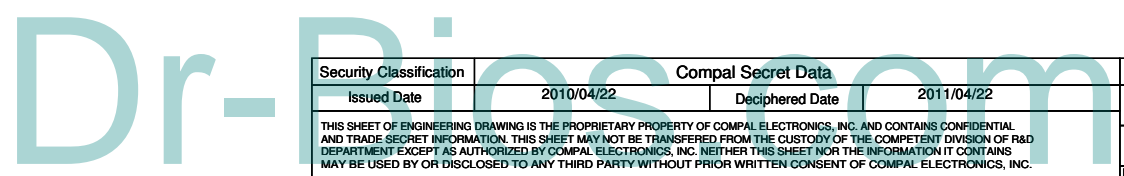
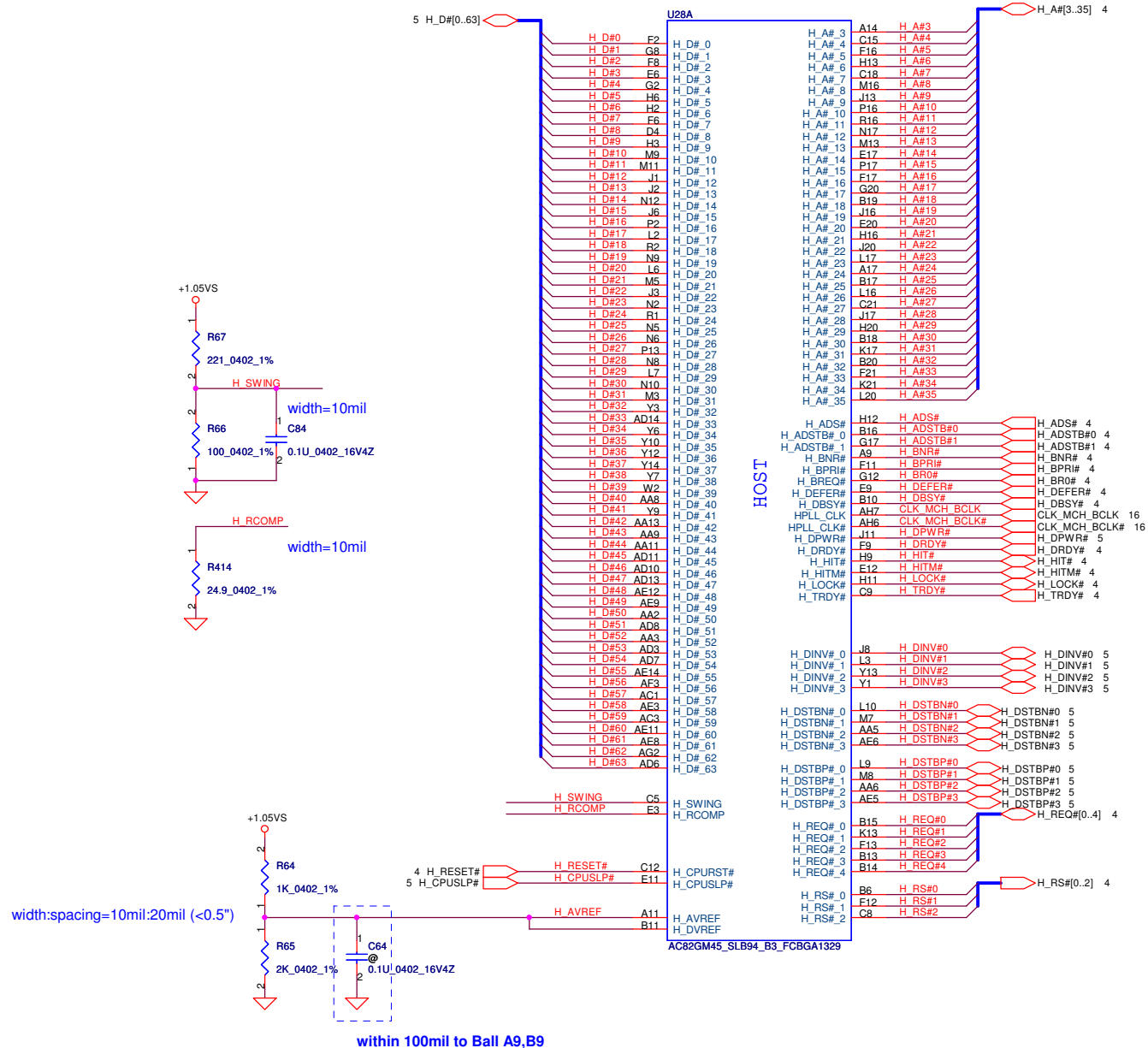
Penryn
CONN@



+CPU-CORE Decoupling	C, uF	ESR, mohm	ESL, nH
SPCAP, Polymer	4X330uF	6m ohm/4	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32
	32X10uF	3m ohm/32	0.6nH/32



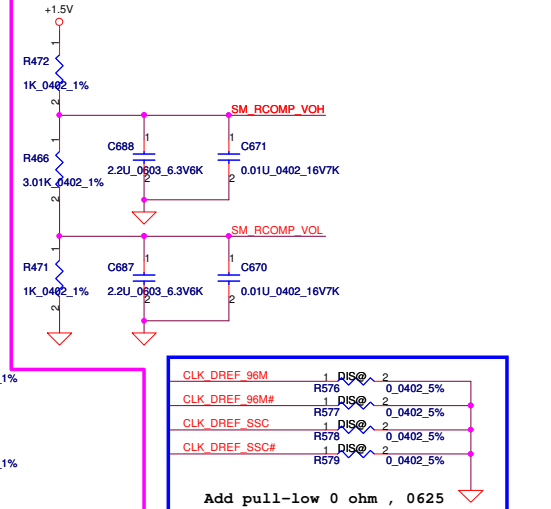
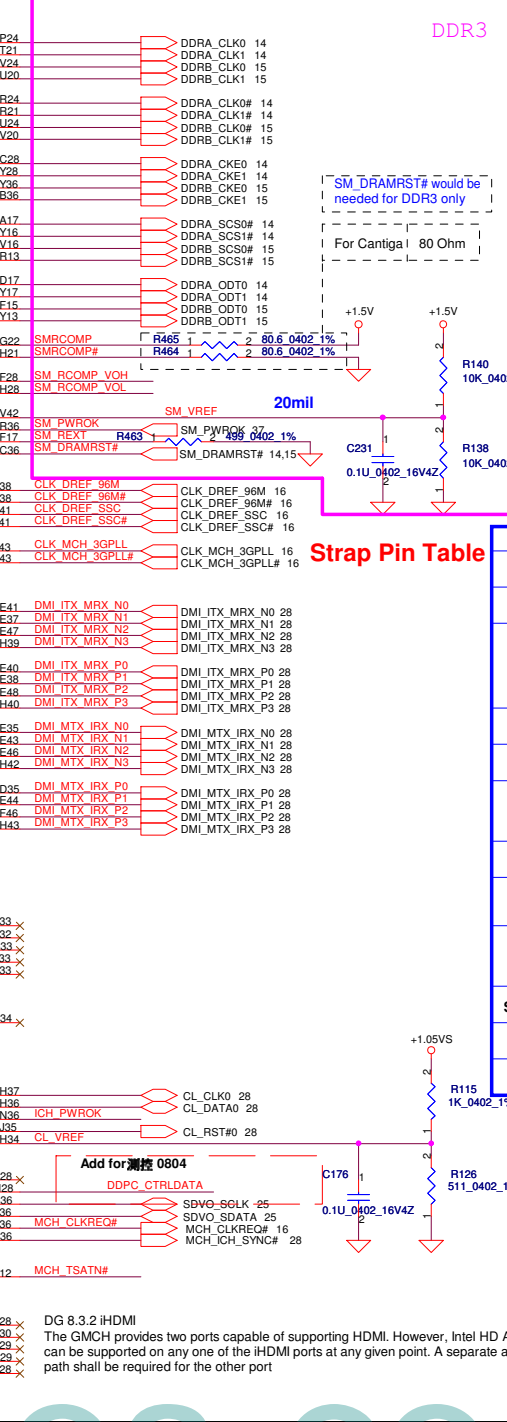
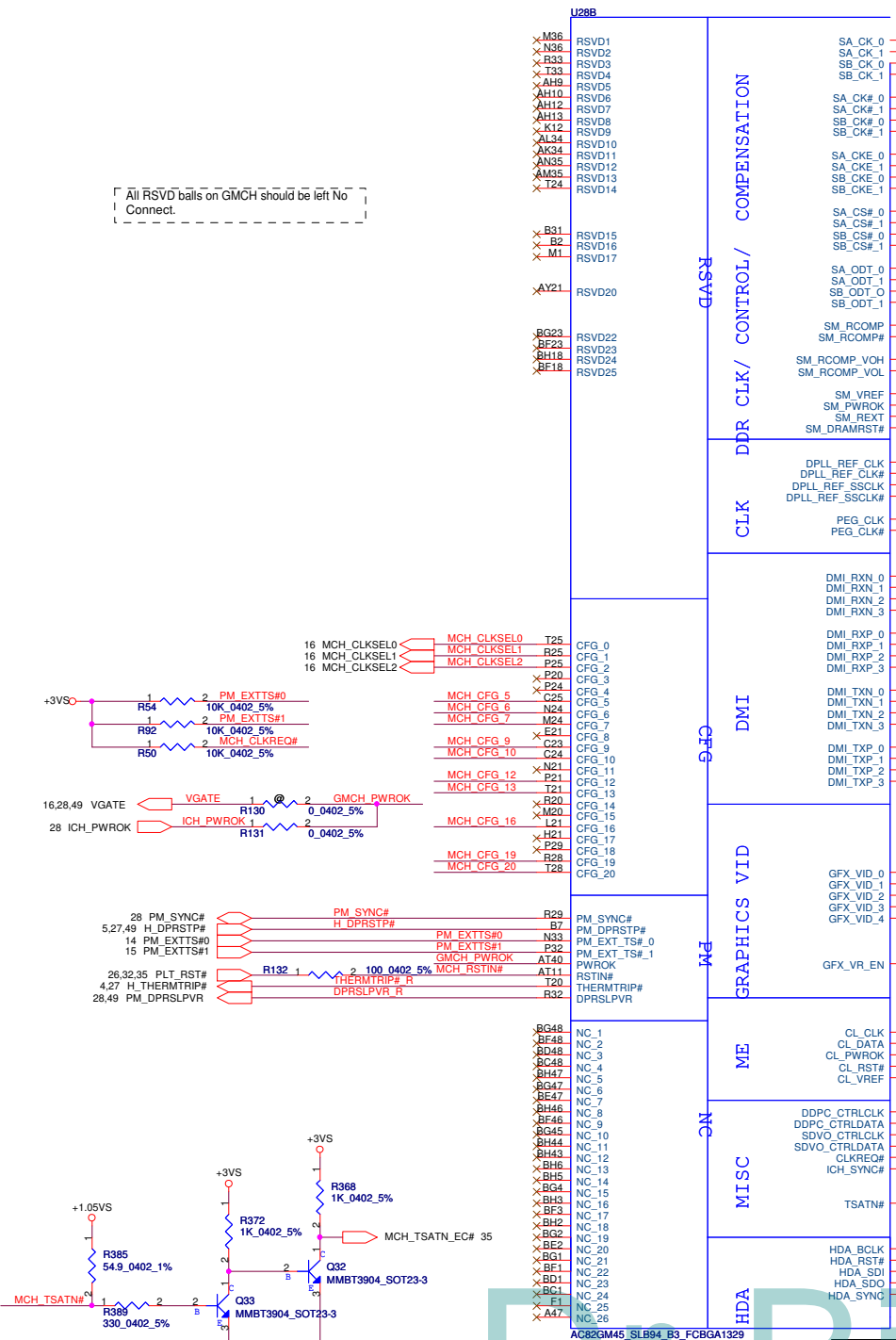
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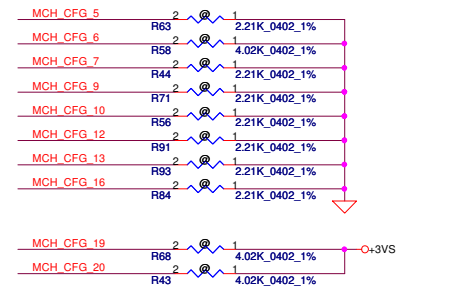
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All RSVD0 balls on GMCH should be left No Connect.



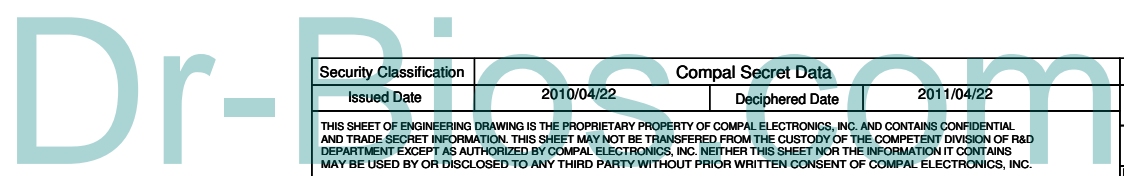
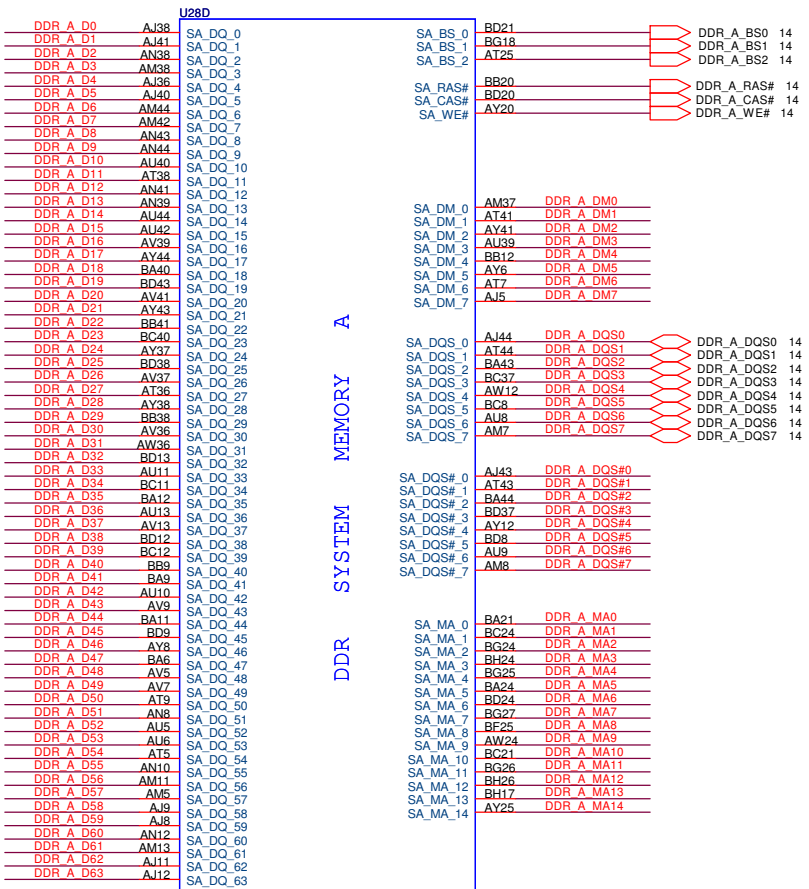
Strap Pin Table

CFG[2:0]	011 = FSB667 010 = FSB800 000 = FSB1067
CFG5	0 = DMI x 2 1 = DMI x 4 (Default)
CFG6	0 = ITPM Host Interface is enabled 1 = ITPM Host Interface is Disabled * (Default)
CFG7	0 = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel Management Engine Crypto TLS cipher suite with confidentiality * (default)
CFG9	0 = Lane Reversal Enable* (Default) 1 = Normal Operation
CFG10	0 = PCIe Loopback Enable 1 = Disable * (Default)
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation * (Default)
CFG16	0 = Dynamic ODT Disabled * (Default) 1 = Dynamic ODT Enabled
CFG19	0 = Normal Operation * (Default) 1 = DMI Lane Reversal Enable
CFG20 (PCIe/SDVO select)	0 = Only PCIe or SDVO is operational* (Default) 1 = PCIe/SDVO are operating simu.
SDVO_CTRLDATA	0 = No SDVO Card Present* (Default) 1 = SDVO Card Present
L_DDC_DATA	0 = LFP Disable * (Default) 1 = LFP Card Present; PCIe disable
DDPC_CTRLDATA	0 = Digital DisplayPort Disable* (Default) 1 = Digital DisplayPort Device Present



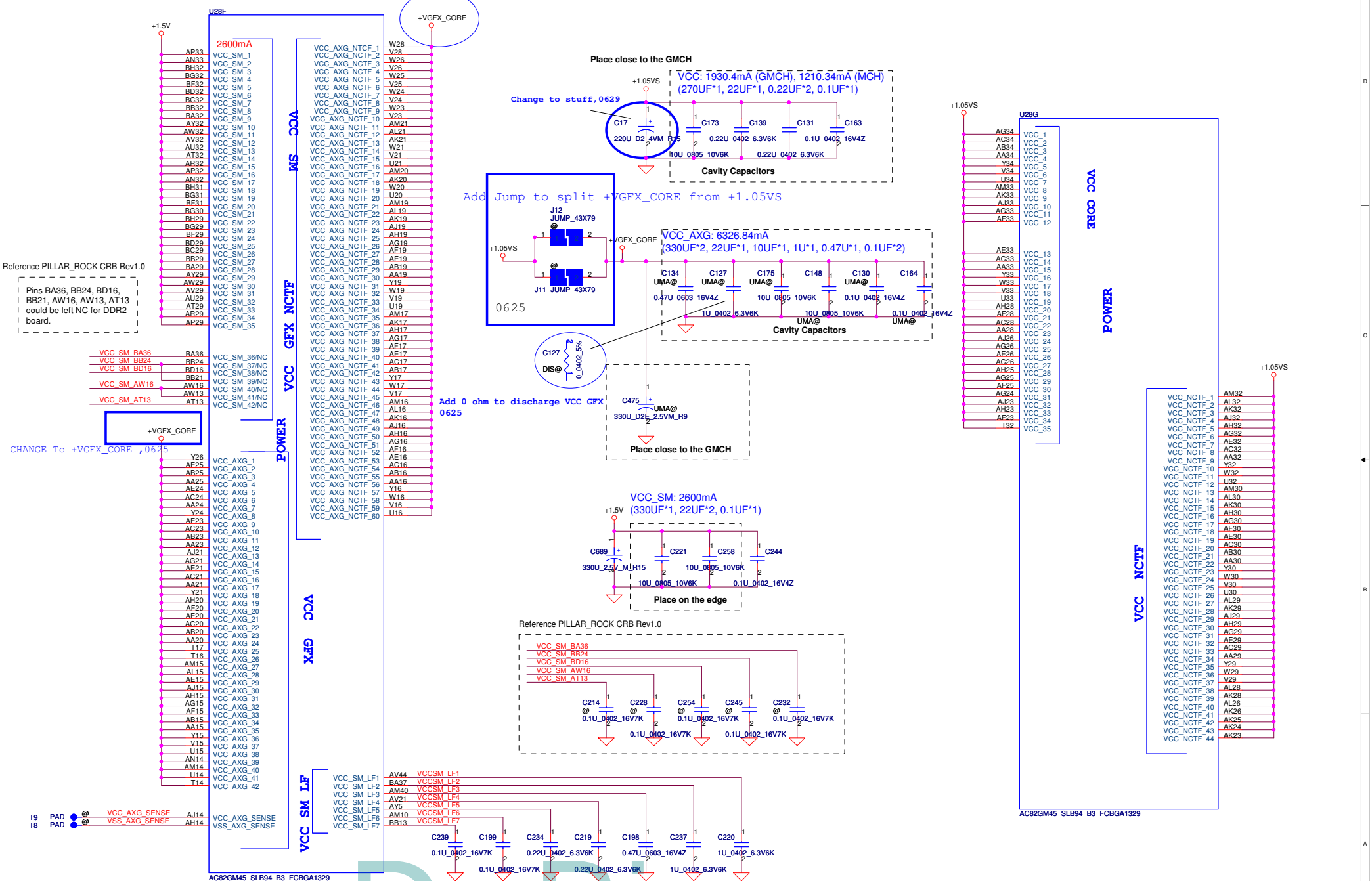
DG 8.3.2 iHDMI
The GMCH provides two ports capable of supporting HDMI. However, Intel HD Audio can be supported on any one of the iHDMI ports at any given point. A separate audio path shall be required for the other port

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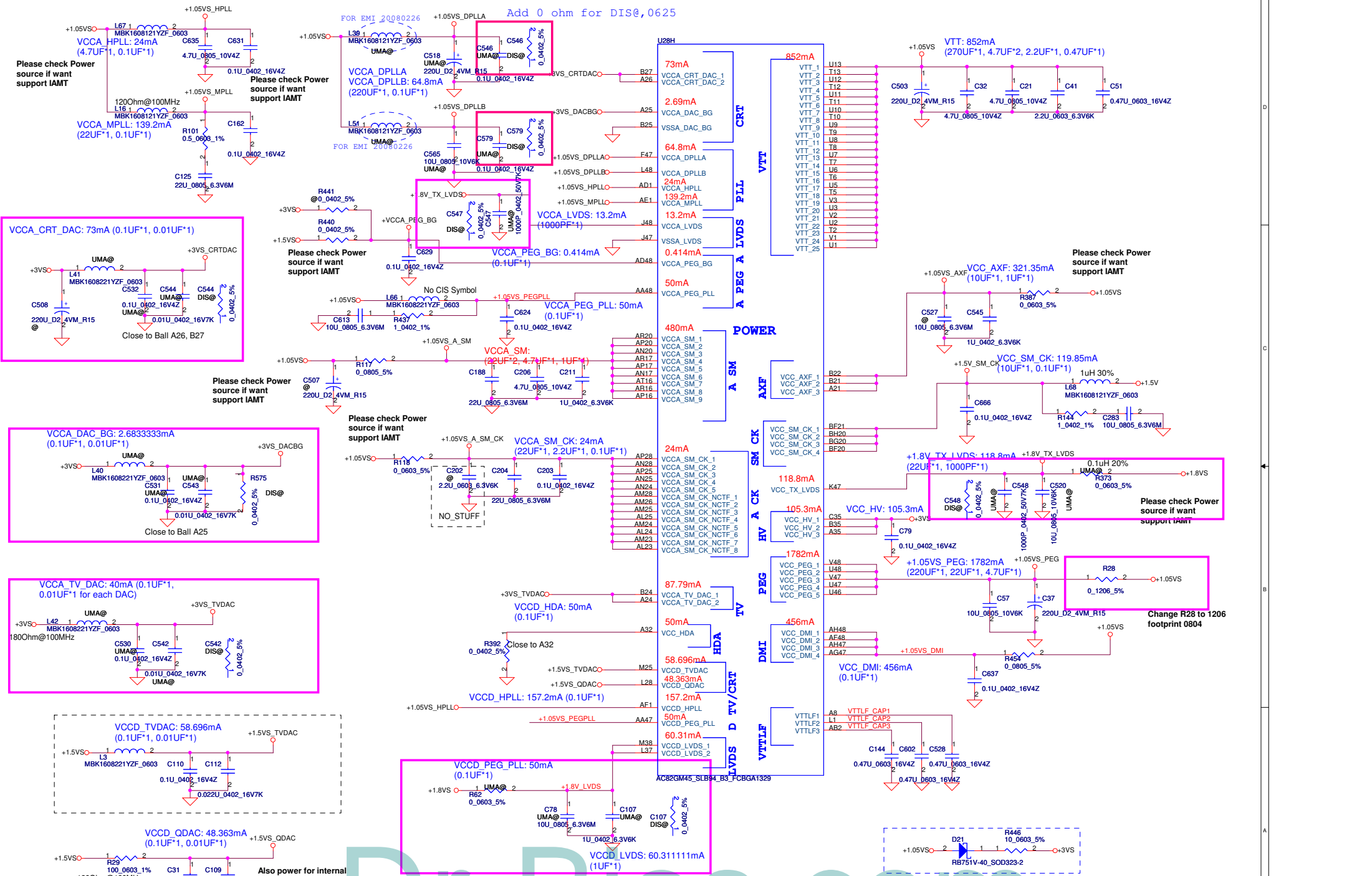
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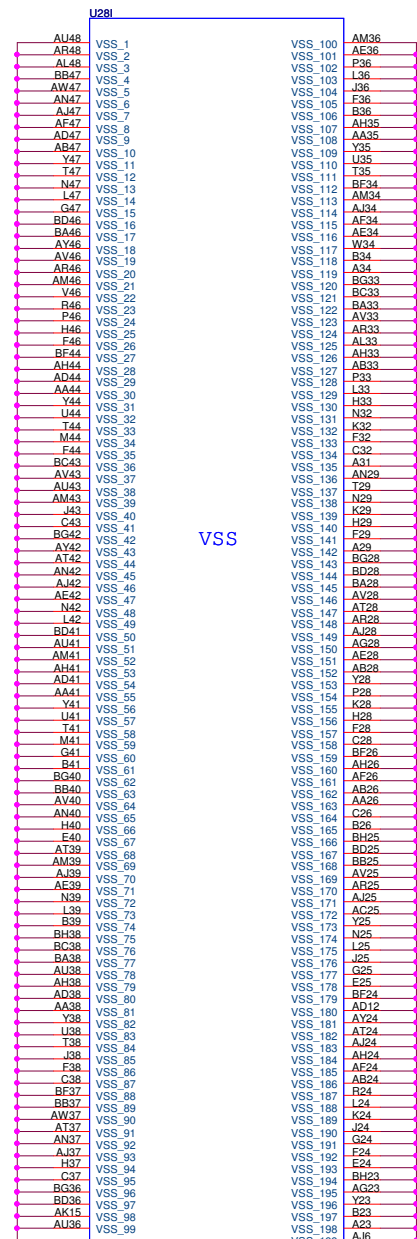
Change name to VCC GFX , 0625



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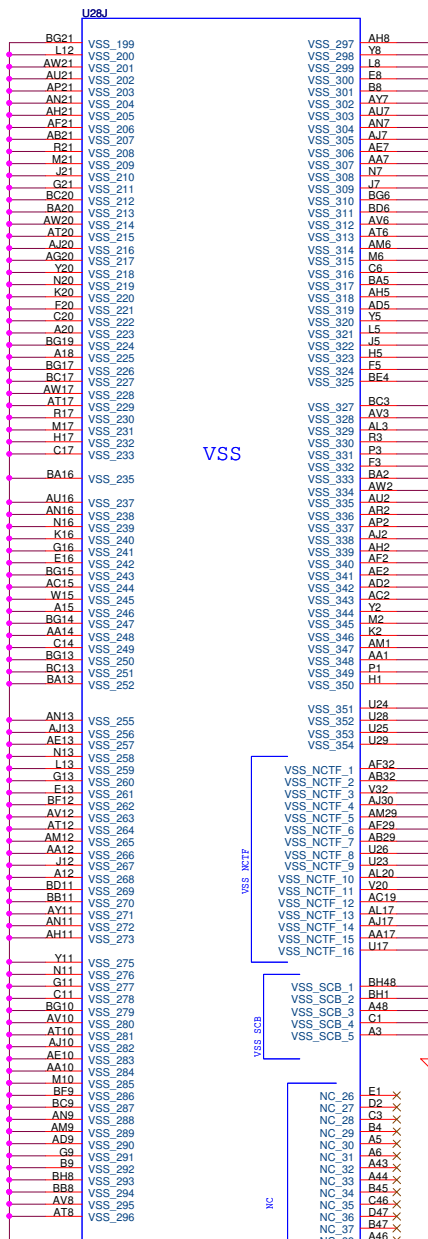
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Cantiga GMCH(5/7)-VCC			
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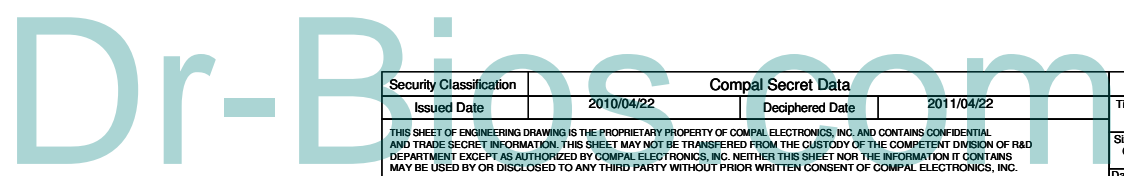
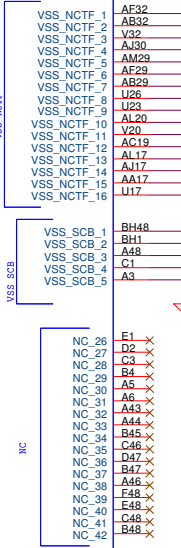
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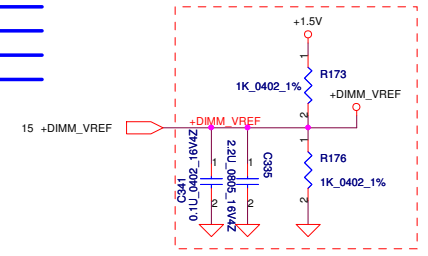
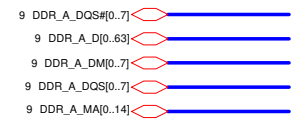
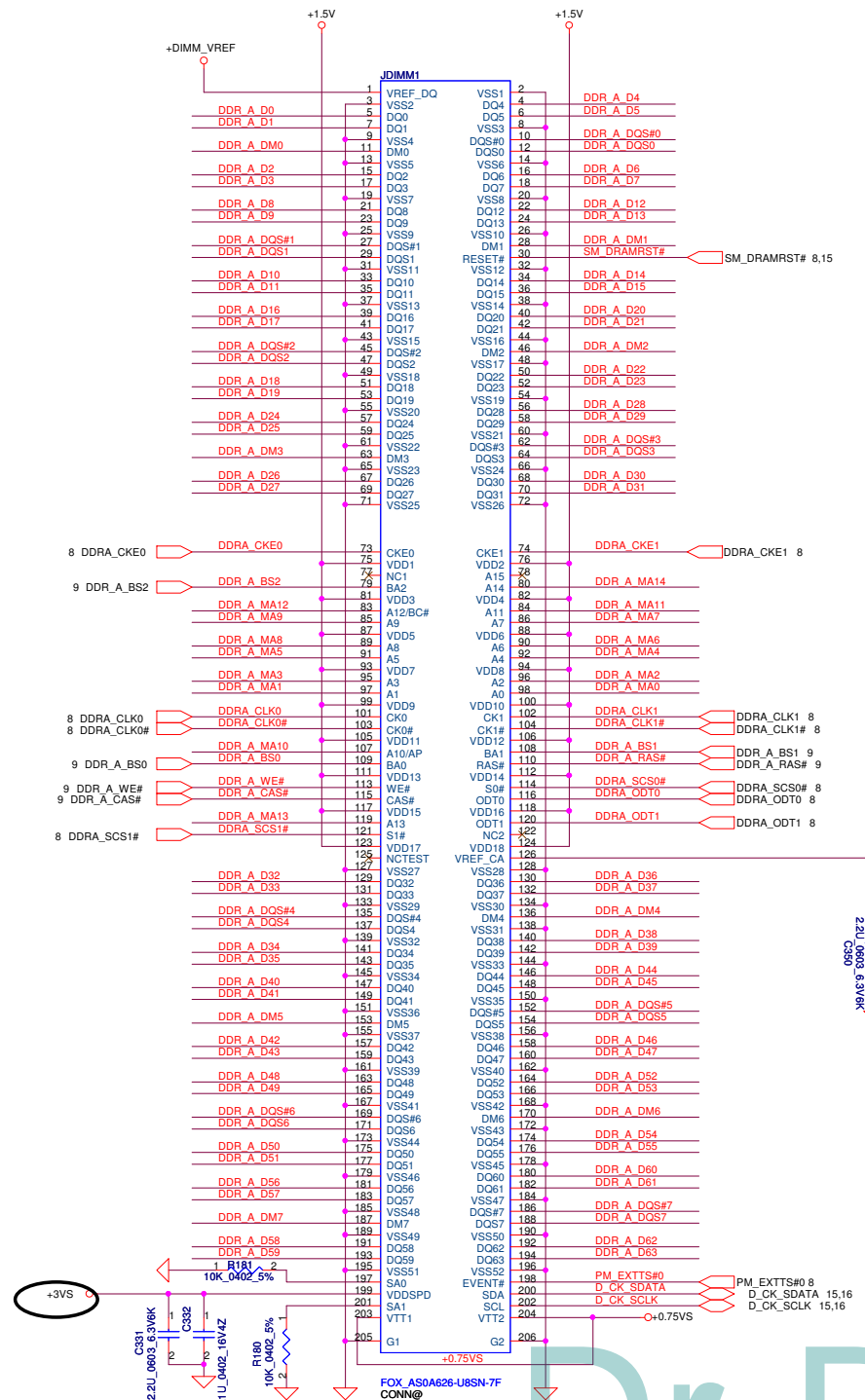


VSS

AC82GM45_SLB94_B3_FCBGA1329

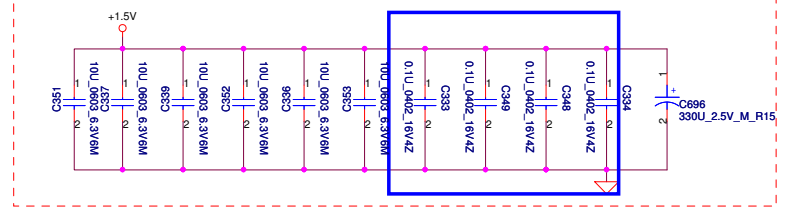


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Issued Date	2010/04/22	Deciphered Date	2011/04/22	Cantiga GMCH(1/7)-GTL	
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Customer				Document Number	0.2
Date				Thursday, July 29, 2010	Sheet 13 of 52

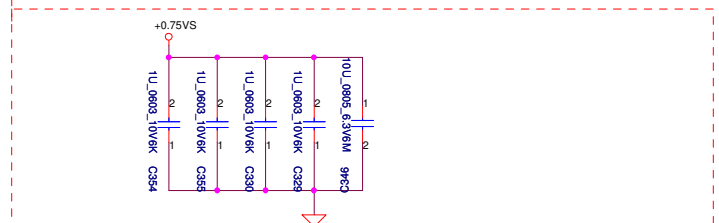


Layout Note:
Place near JDIMM2

Layout Note: Place these 4 Caps near Command and Control signals of DIMM

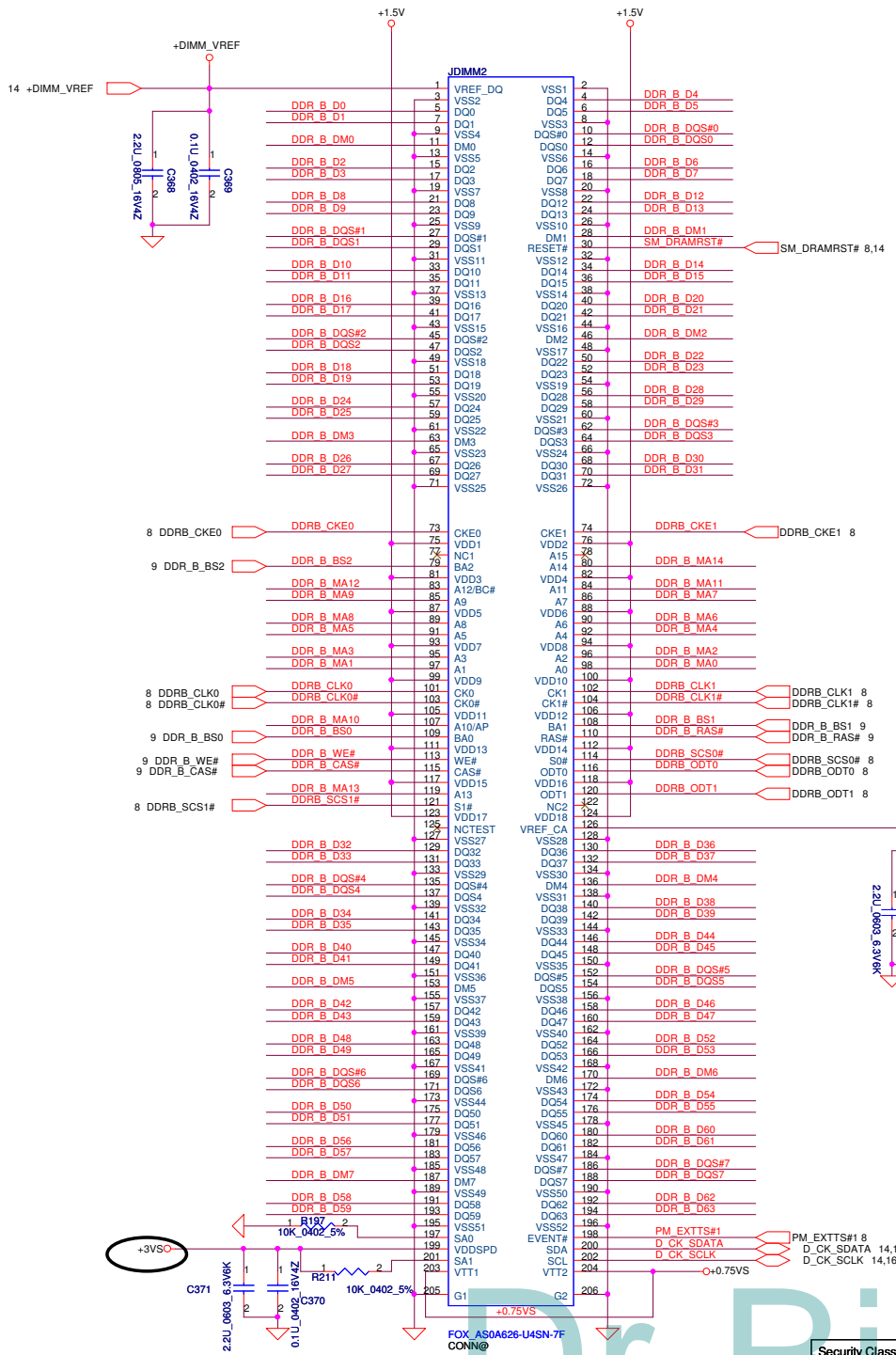


Layout Note:
Place near JDIMM2.203 & JDIMM2.204



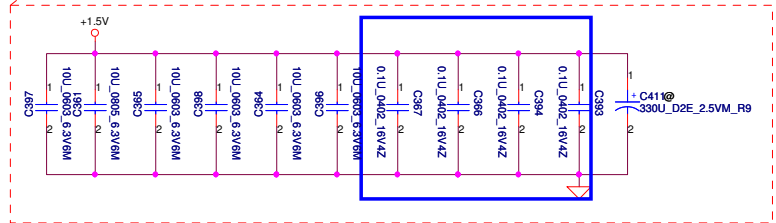
DIMM0 REV H:5.2mm (BOT)

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				PEW52 M/B LA-6632P Schematic	
				Date:	Wednesday, August 04, 2010
				Sheet	14 of 52

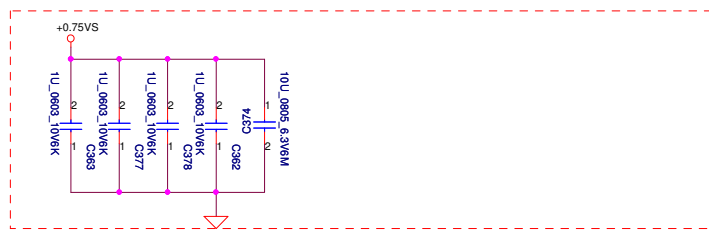


Layout Note:
Place near JDIMM1

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA



Layout Note:
Place near JDIMM1.203 & JDIMM1.204



DIMM1 REV H:9.2mm (BOT)

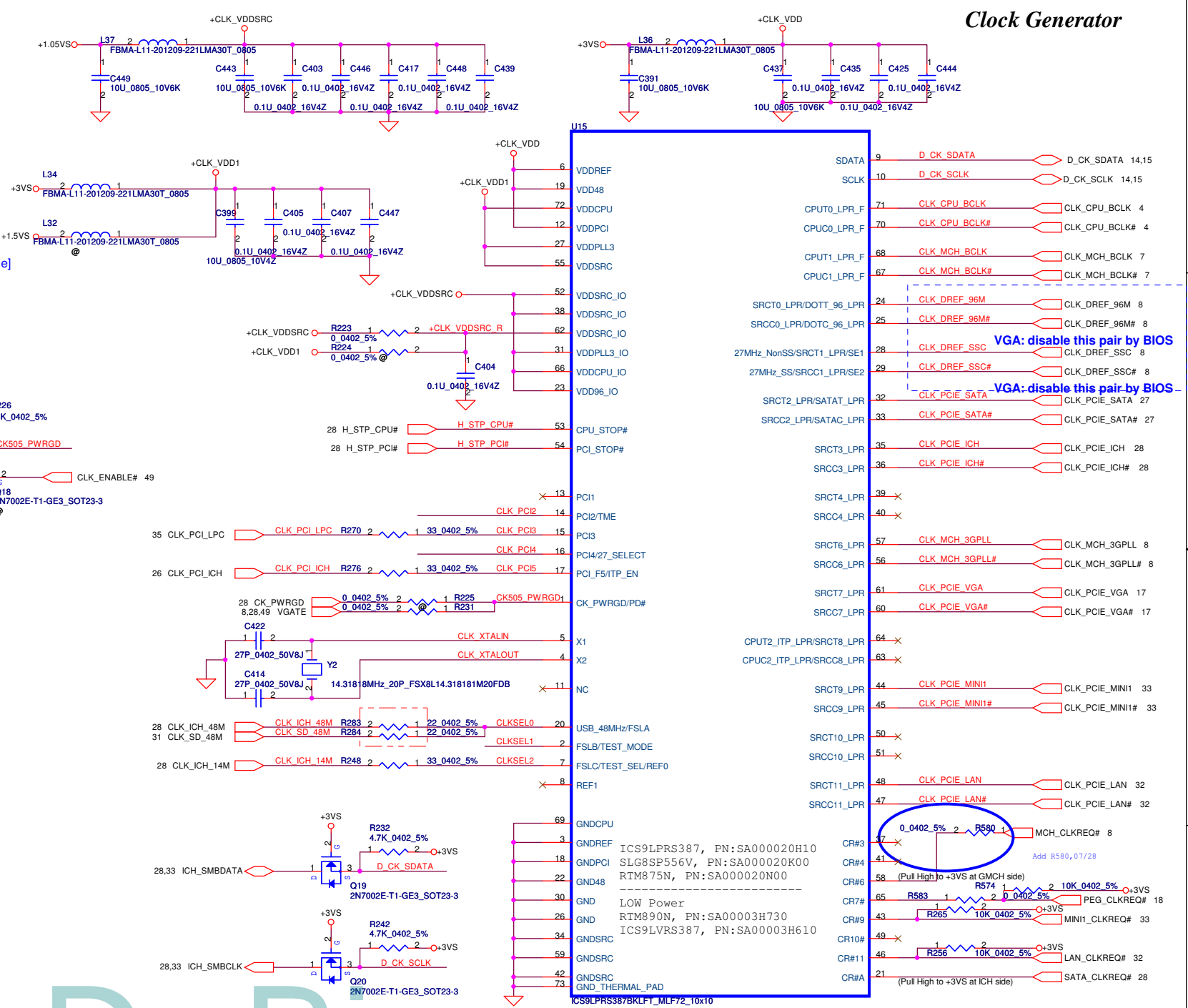
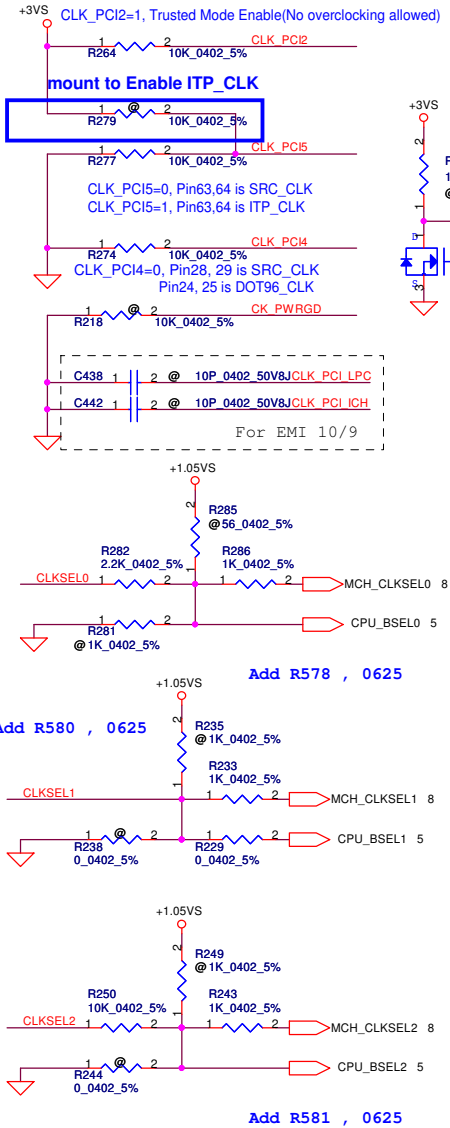
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Issued Date	2010/04/22	Deciphered Date	2011/04/22	DDRIII-SODIMM1	
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				Date:	Wednesday, August 04, 2010
				Sheet	15 of 52

FSLC	FSLB	FSLA	CPU MHz	SRC MHz	PCI MHz
0	0	0	266	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3

Table : ICS9LPRS387

CLK_REQ#	Control	Free-Run
CR#_10(WLAN)	PCIEX10	PCIEX0
CR#_6(MCH)	PCIEX6	PCIEX1
CR#_4(NEW CARD)	PCIEX4	
CR#_9(MINI CARDII)	PCIEX9	

SRC7(VGA_CLK): Discrete VGA[Enable] UMA[Disable]

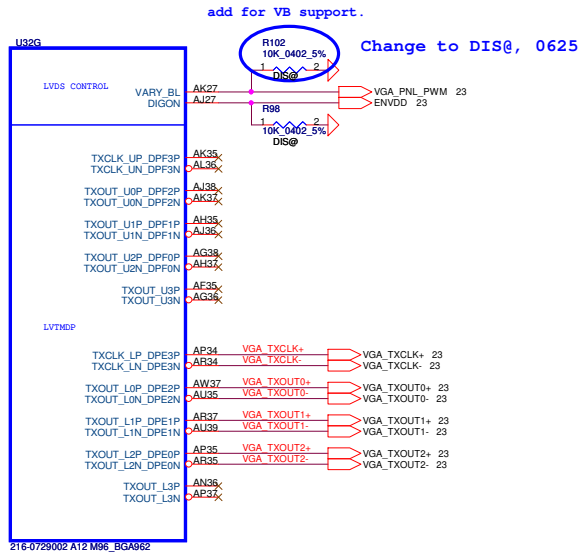
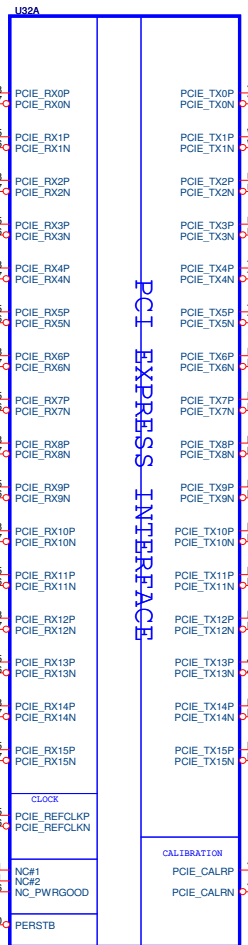


Clock Generator

Security Classification		Compal Secret Data	
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Compal Electronics, Inc.		
Title: Clock Generator (CK505)		
Size	Document Number	Rev
Customer	PEW52 M/B LA-6632P Schematic	0.2
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10 PCIE_GTX_C_MRX_P[0..15] (PCIE GTX C_MRX_P[0..15])
 10 PCIE_GTX_C_MRX_N[0..15] (PCIE GTX C_MRX_N[0..15])

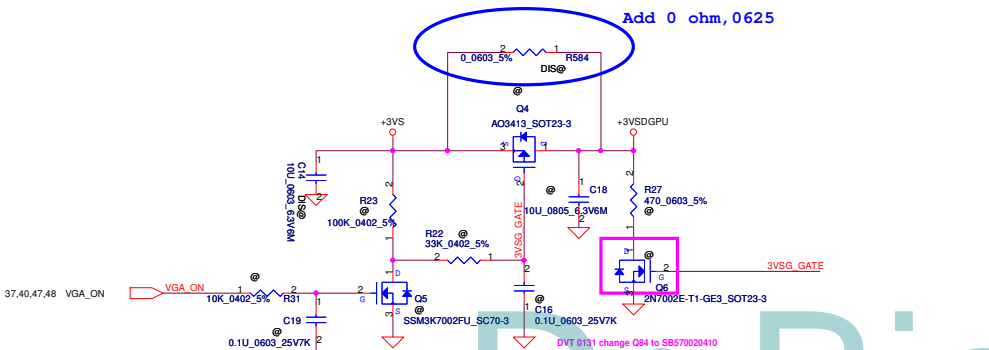


16 CLK_PCIE_VGA AB35
 16 CLK_PCIE_VGA# AA36C

For M96, AH16 is NC
 For Mahatten need PD
 NC#1 AK21
 NC#2 AH16

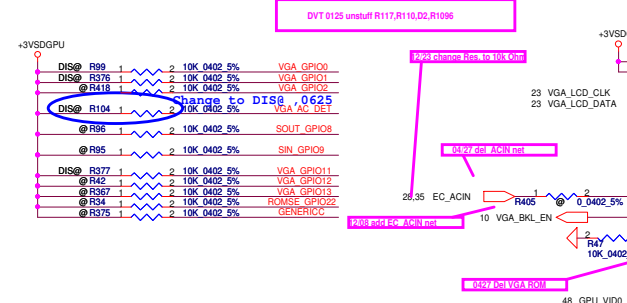
26 PLTRST_VGA# AA30C

Add 0 ohm, 0625

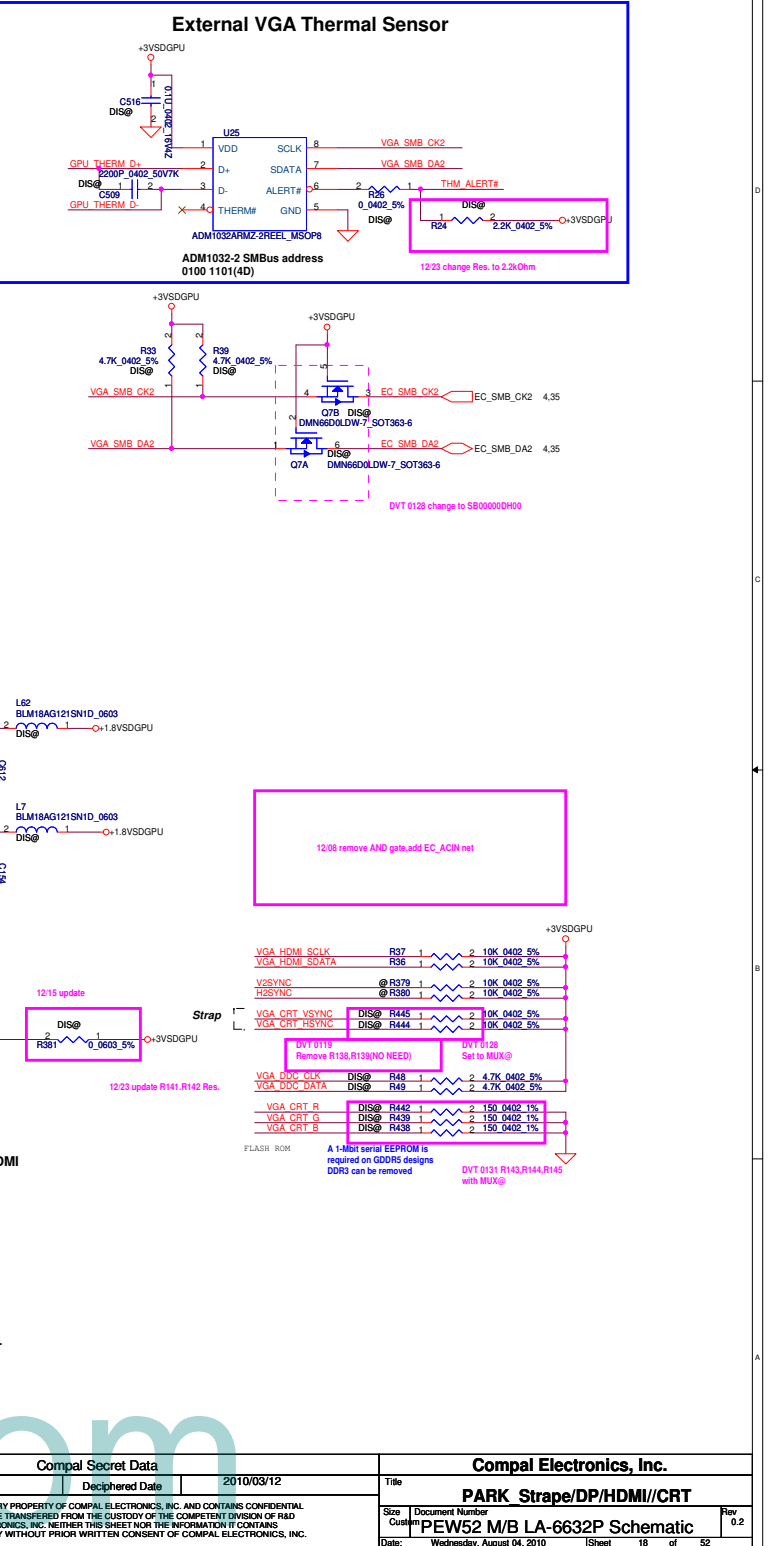
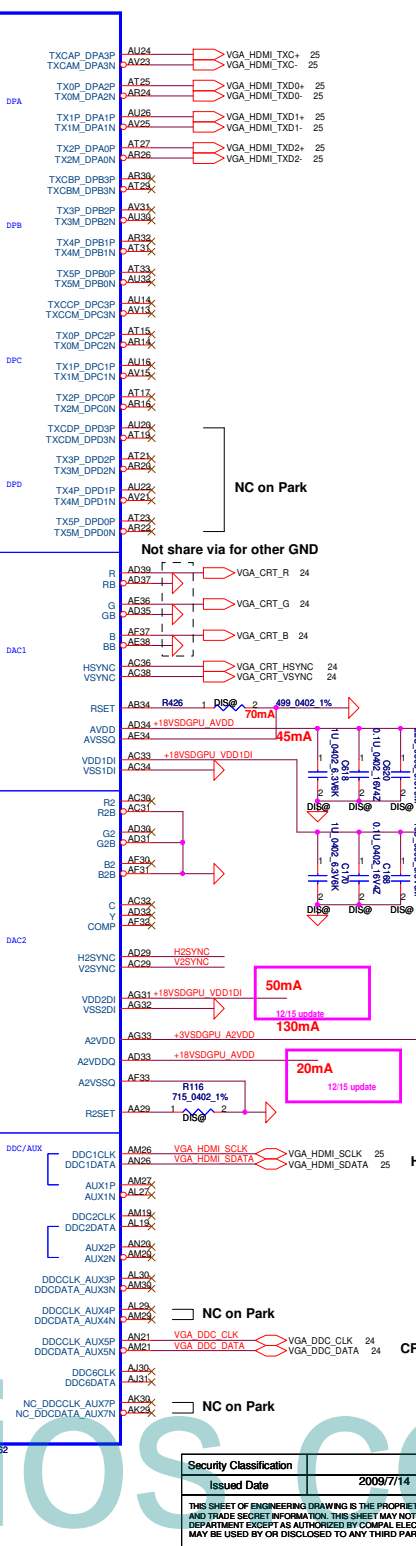
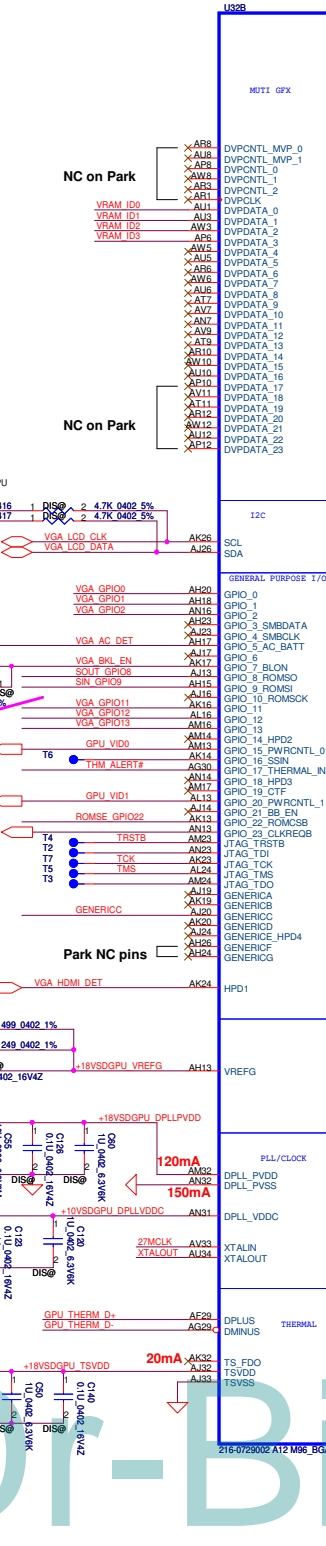
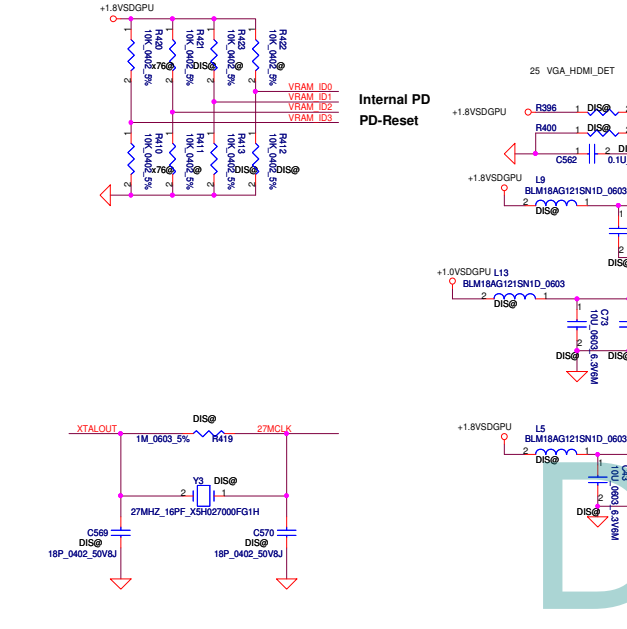


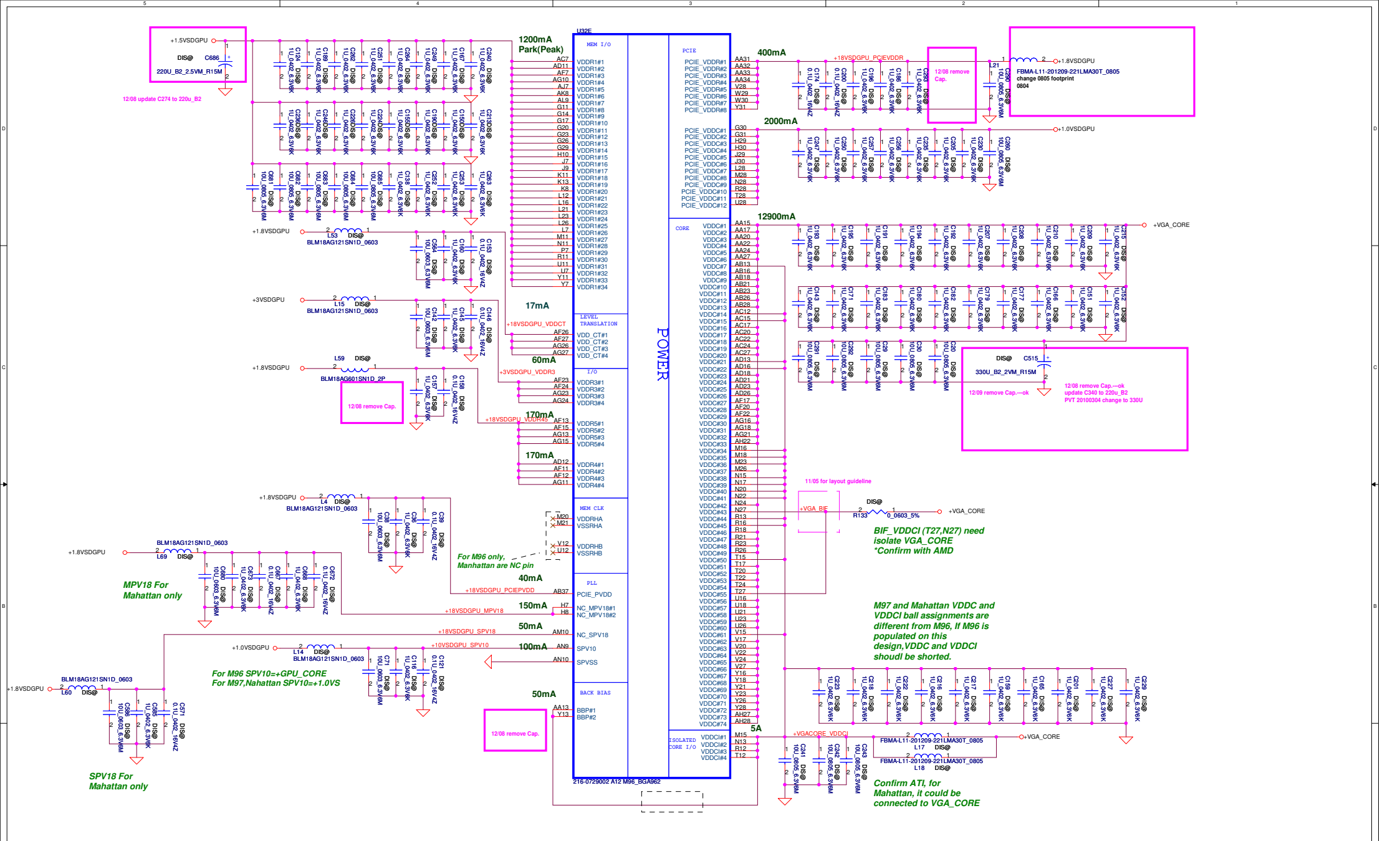
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/7/14	Deciphered Date	2010/03/12	Title	PARK_PCIE / LVDS
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				PEW5M	M/B LA-6632P Schematic
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Strap Name		Pin Straps description <all internal PD>	Setting
VIP_DEVICE_EN	V2SYNC	VIP Device Strap Enable indicates to the software driver 0: Driver would ignore the value sampled on VHAD_0 during reset 1: VHAD_0 to determine whether or not a VIP slave device	0
VGA_DIS	GPIO9	VGA Disable determines 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled (for mobile mode) 1: Tx de-emphasis enabled (Default setting for desktop)	1
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO13 GPIO12 GPIO11	GPIO13,12,11 [config 2,1,0] : a) If BIOS_ROM_EN = 1, then Config[2:0] defines the memory apertures CONFIG[2:0] 128 MB 000 256 MB 001 64 MB 010 b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size.	001
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0: Disable, 1: Enable	0
AUD[1] AUD[0]	HSYNC VSYNC	00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	11
BIF_GEN2_EN	GPIO2	0= Advertises the PCI-E device as 2.5 GT/s capable at power-on 1= Advertises the PCI-E device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	0
RESERVED	H2SYNC GPIO8 GPIO21	Internal use only. THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET. The pad may be left unconnected	

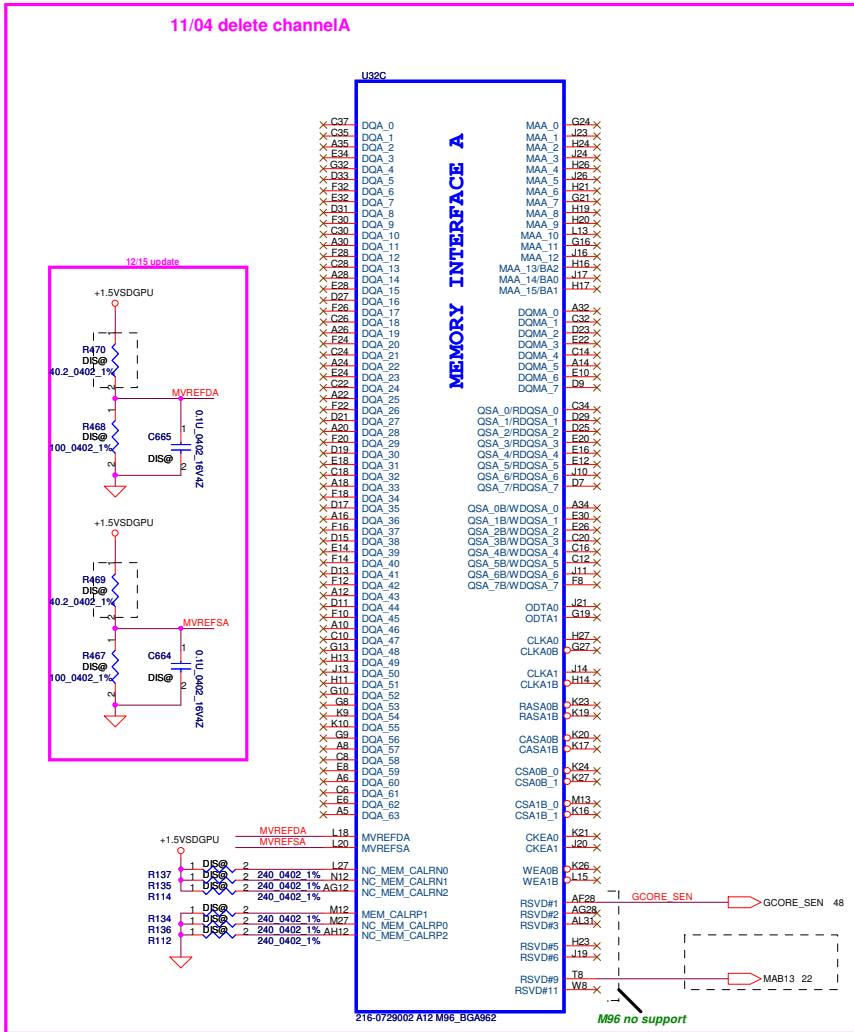


Park (XT)	Location	VRAM			
		VRAM_ID3	VRAM_ID2	VRAM_ID1	VRAM_ID0
64MX16 <4 pcs>	Samsung (SA000035720/K4W1G1646E-HC12)	0	1	0	0
	Hynix (SA000032420/H5TQ1G63BFR-12C)	1	0	0	0
128MX16 <4 pcs>	Samsung (SA00003M000/K4W2G1646B-HC12)	1	1	1	0
	Hynix (SA00003V500/H5TQ2G63BFR-12C)	1	1	1	1





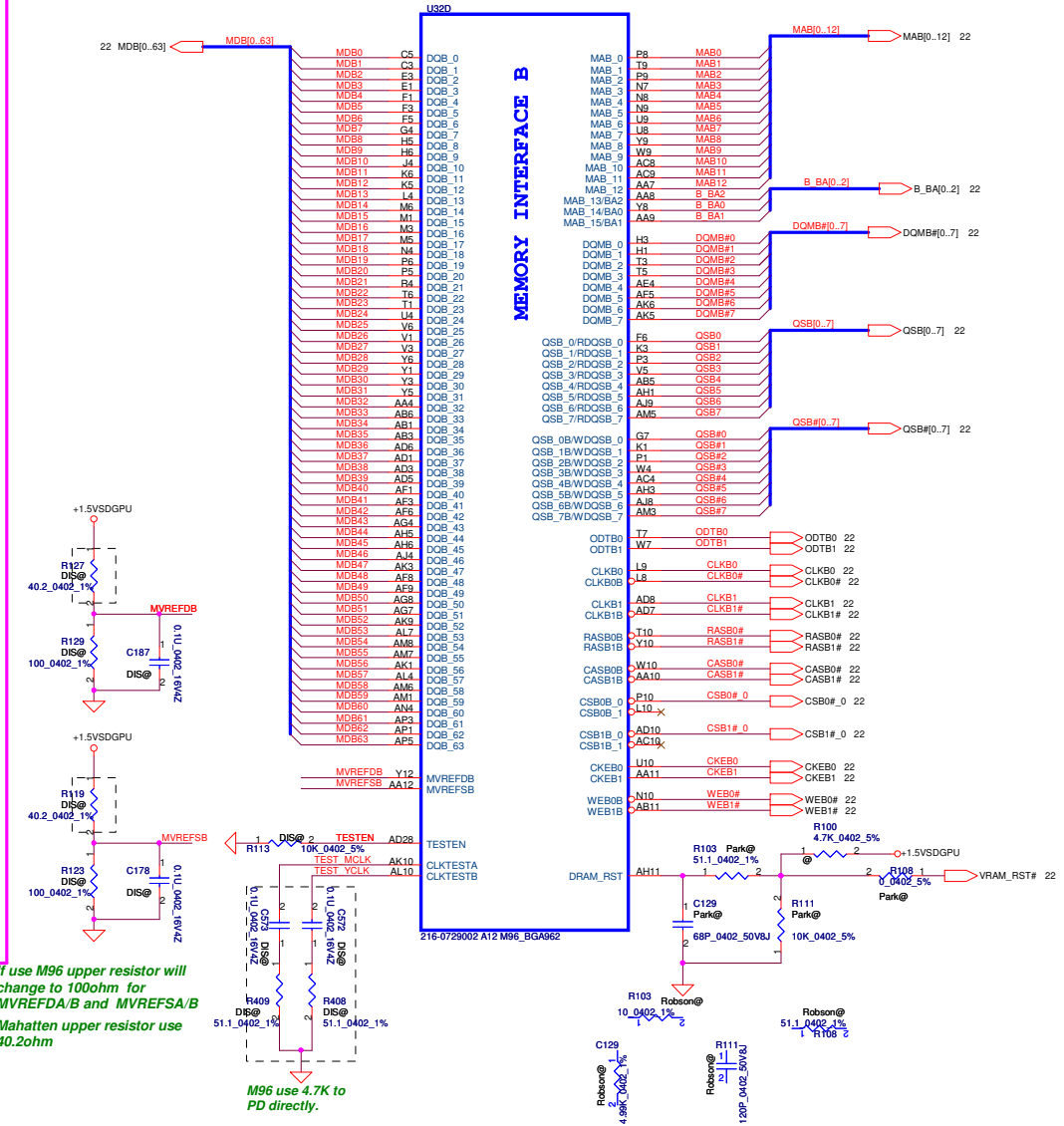
Park only support single channel memory (channel B only)



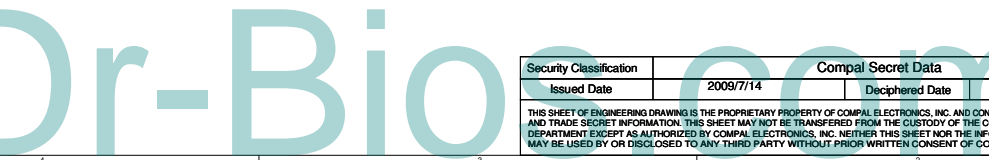
If use M96 upper resistor will change to 100ohm for MVREFDA/B and MVREFSA/B Mahatten upper resistor use 40.2ohm

In M97, Medison and Park, AF28 is FB_VDDC, AG28 is FB_VDDCI, AH29 is FB_GND. GCORE_SEN and FB_GND should route as differential pair Same as VDDCI_SEN and FB_GND

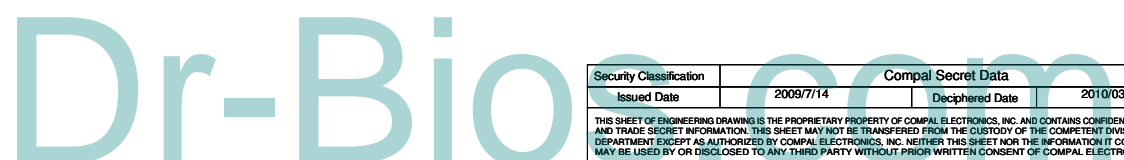
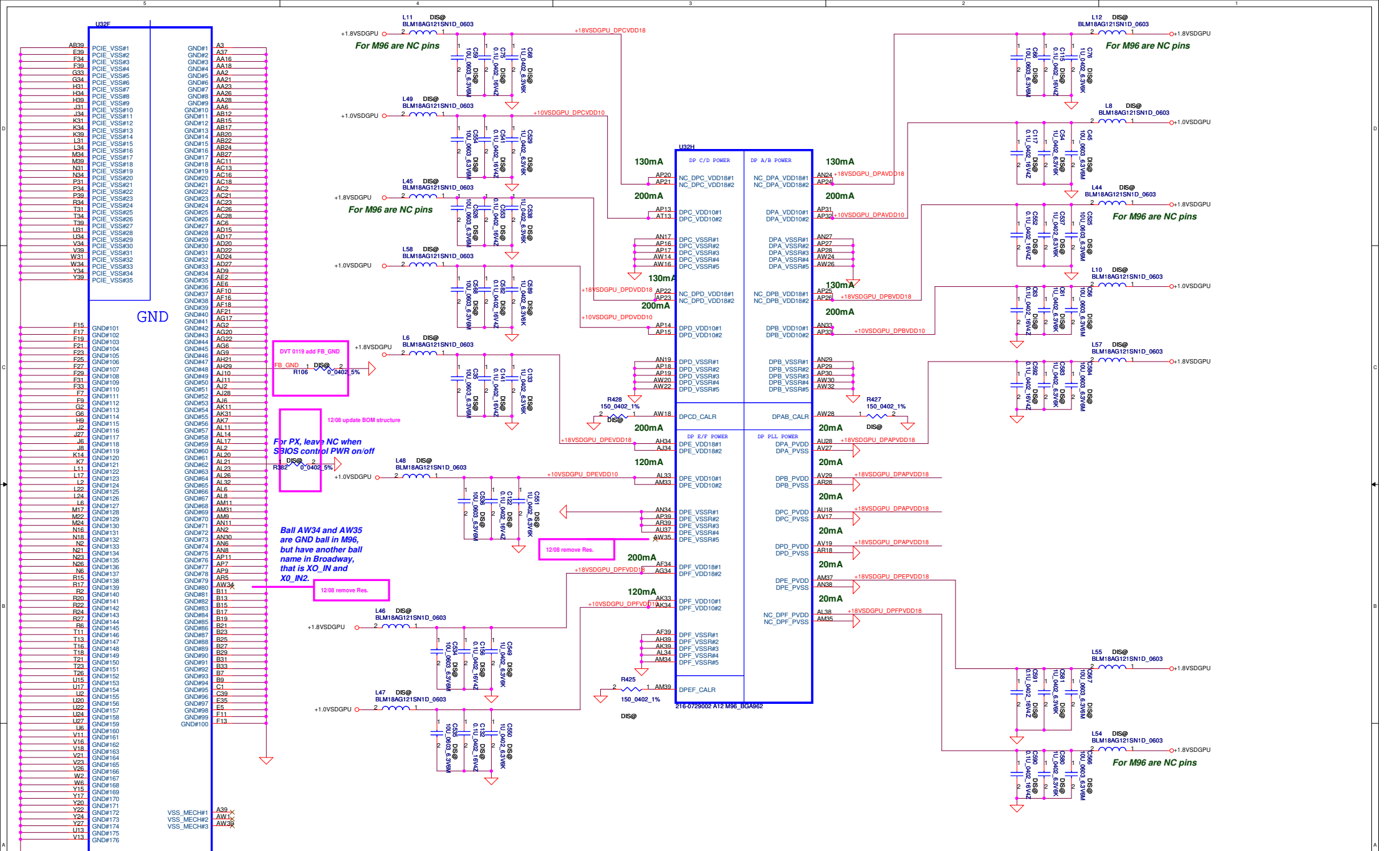
If use M96 upper resistor will change to 100ohm for MVREFDA/B and MVREFSA/B Mahatten upper resistor use 40.2ohm



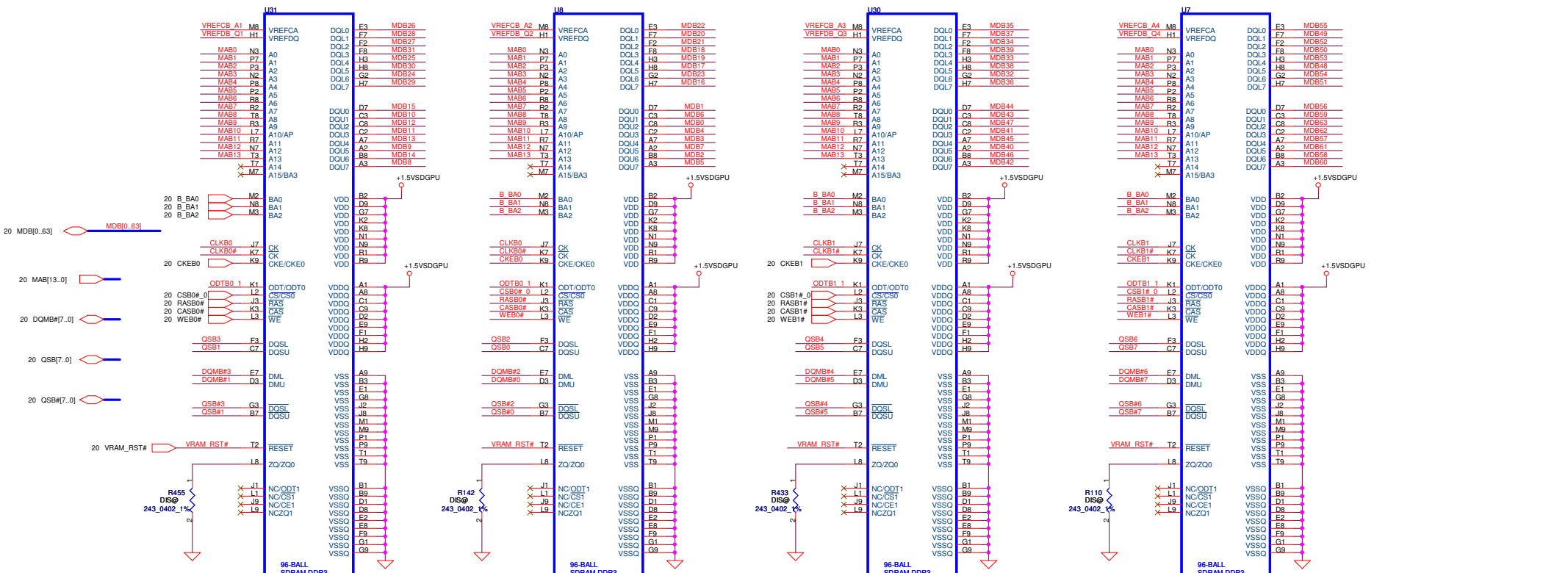
M96 use 4.7K to PD directly.



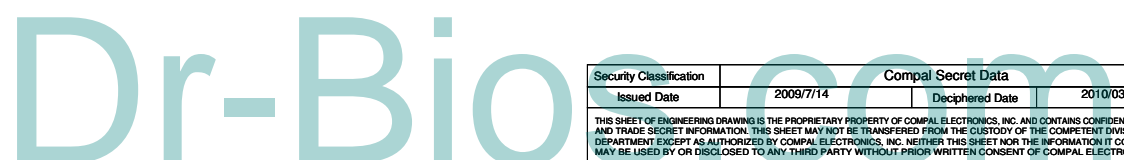
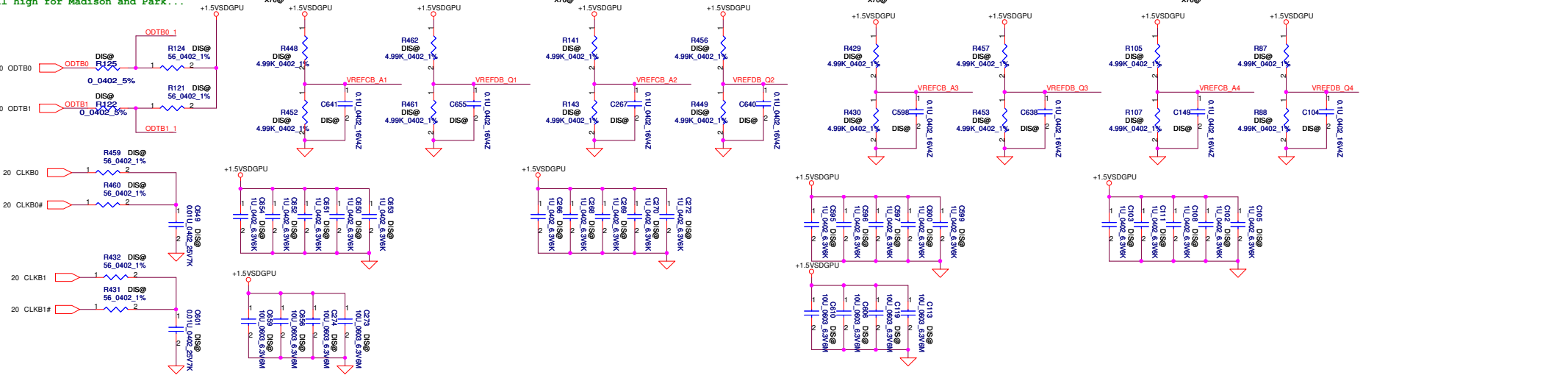
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Issued Date	2009/7/14		Deciphered Date		2010/03/12				PARK Memory		Customer Number			
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Date: Wednesday, August 04, 2010										Sheet		20	of	52



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Issued Date	2009/7/14	Deciphered Date	2010/03/12	Title	PARK Power/GND
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Size	Document Number	Rev			
	PEW52 M/B LA-6632P Schematic	0.2			
Date:	Thursday, July 29, 2010	Sheet	21	of 82	



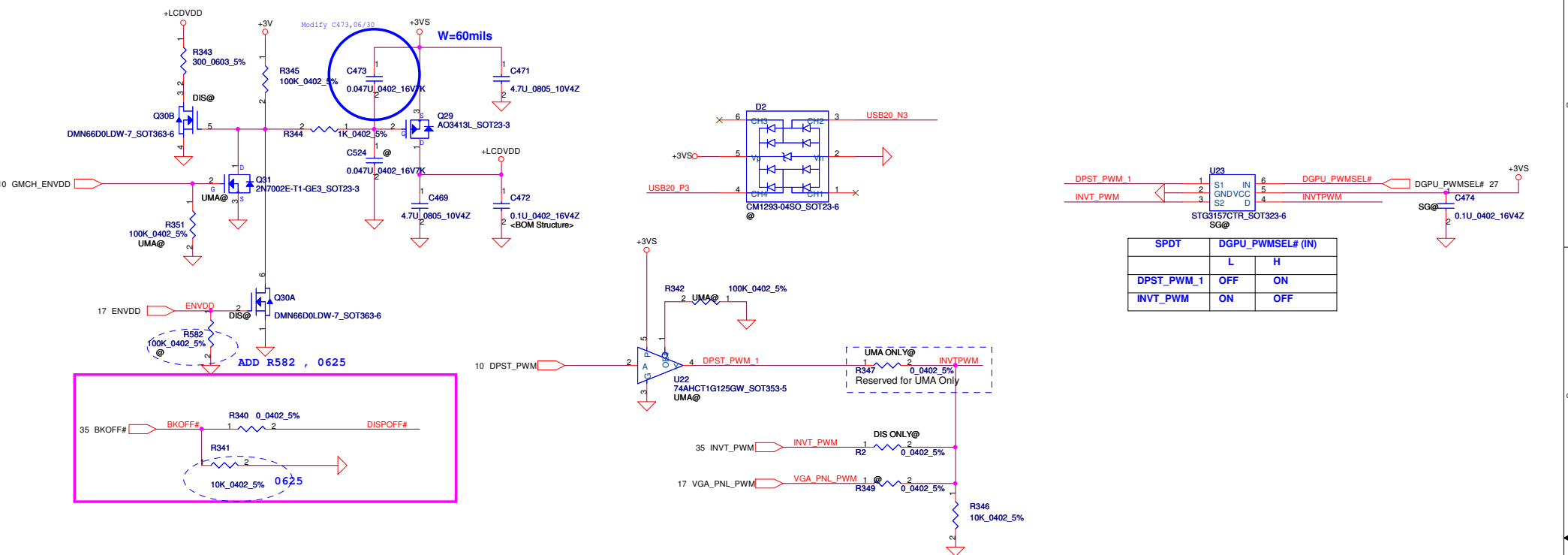
Pull high for Madison and Park...



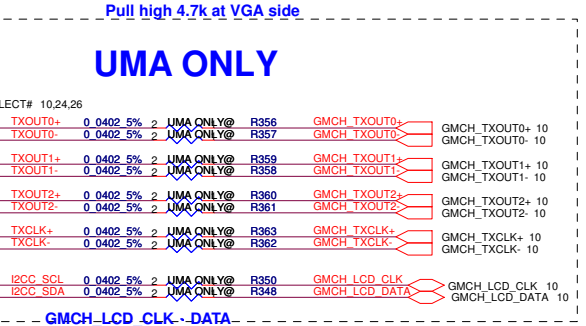
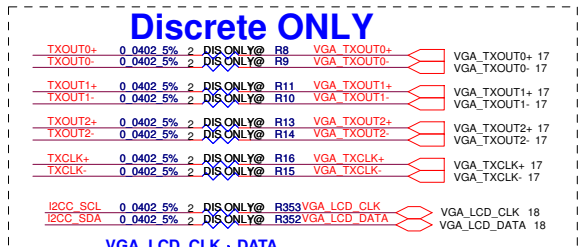
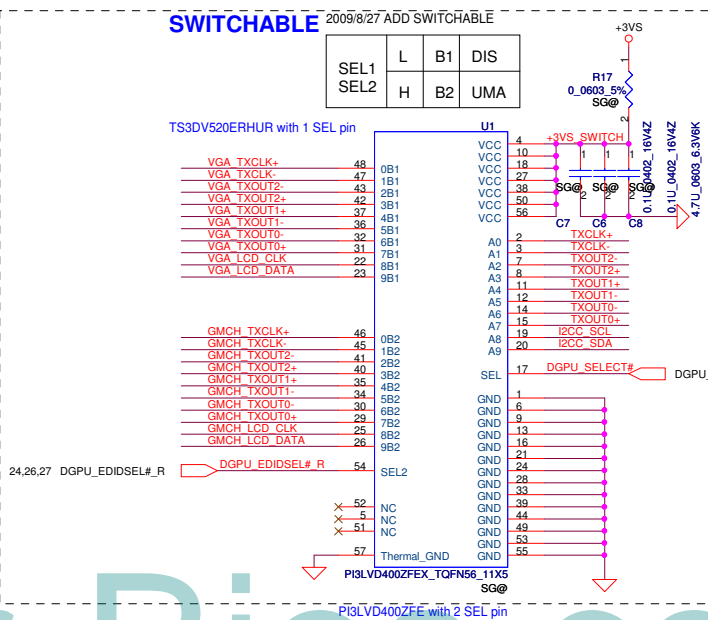
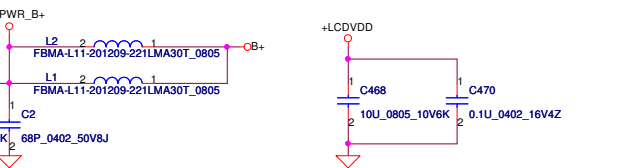
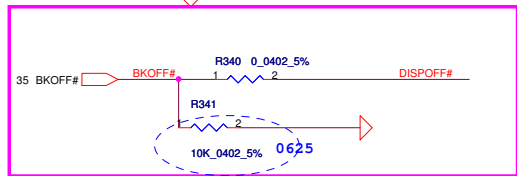
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Issued Date		Deciphered Date		VRAM DDR3 / Channel B	
2009/7/14		2010/03/12		Customer Number	
				PEW52 M/B LA-6632P Schematic	
				Date: Wednesday, August 04, 2010	
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LCD POWER CIRCUIT

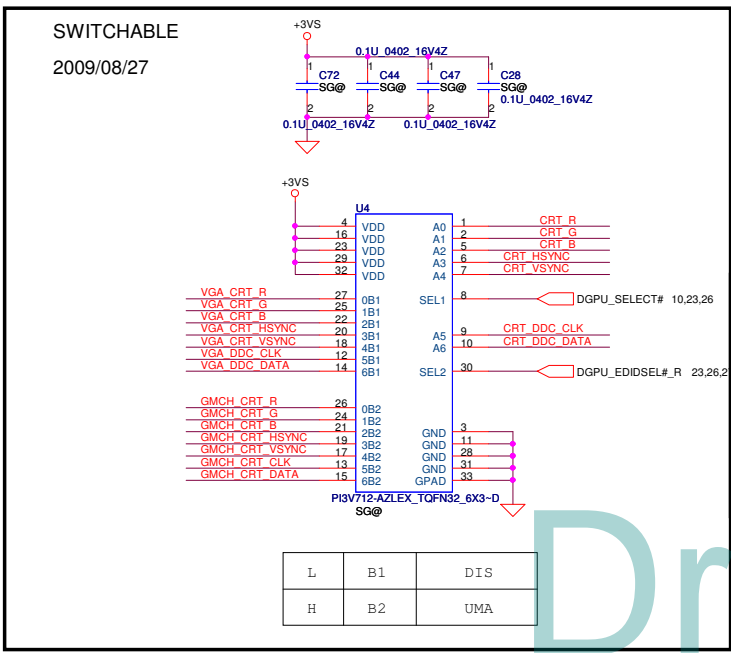
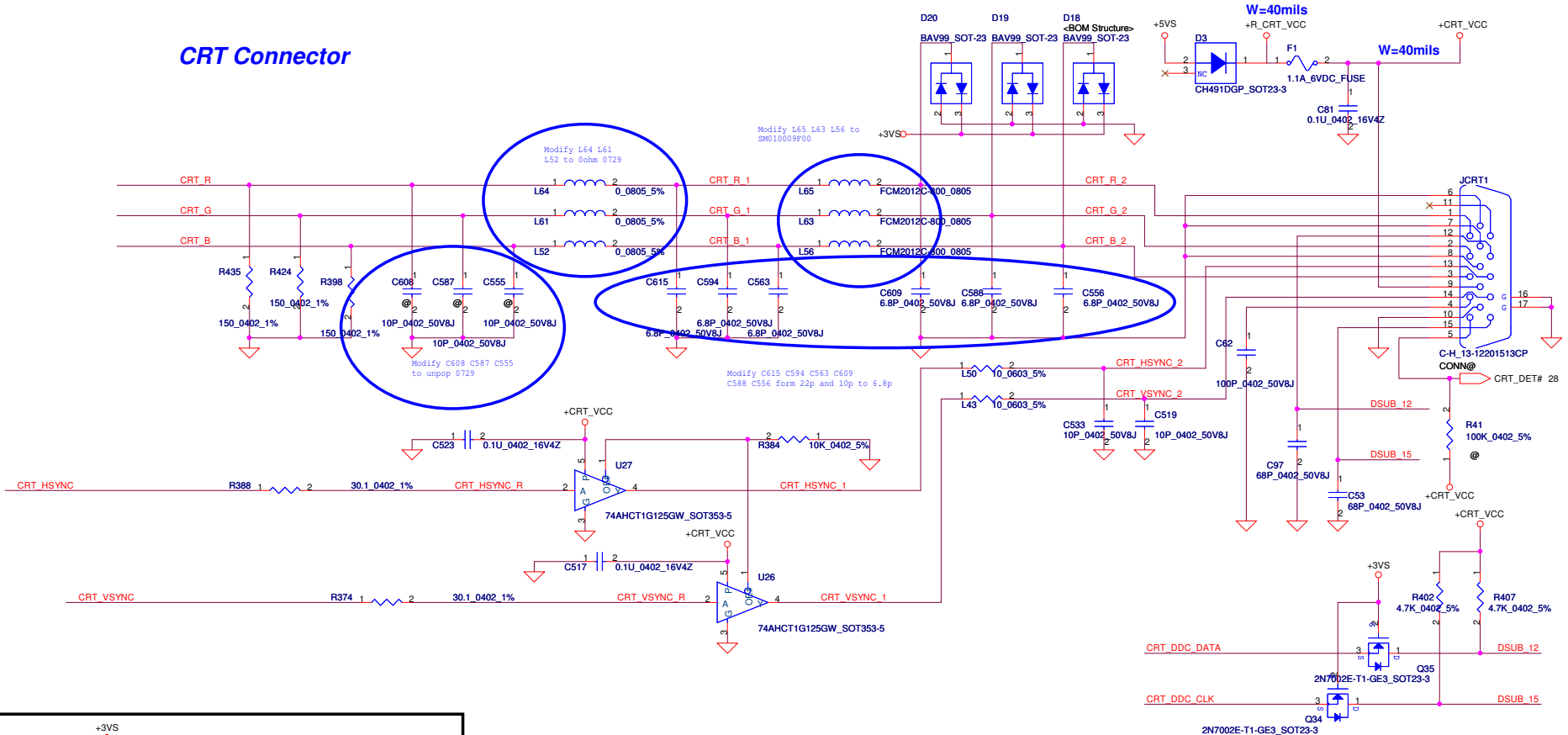


SPDT	DGPU_PWMSEL# (IN)
DPST_PWM_1	L
INVT_PWM	H
	OFF
	ON
	ON
	OFF
	OFF



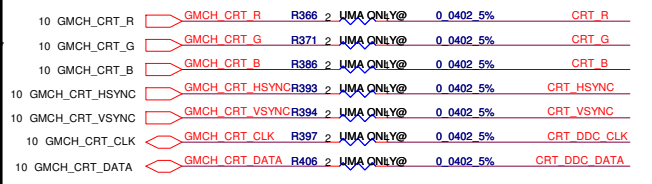
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Issued Date	2010/04/22	Deciphered Date	2011/04/22	Compal Electronics, Inc.
				LVDS Connector
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CRT Connector

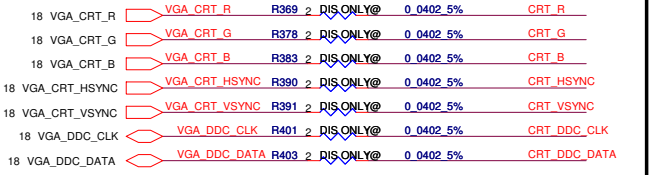


GMCH_CRT_CLK · DATA
Pull high 2.2k at NB side

UMA only

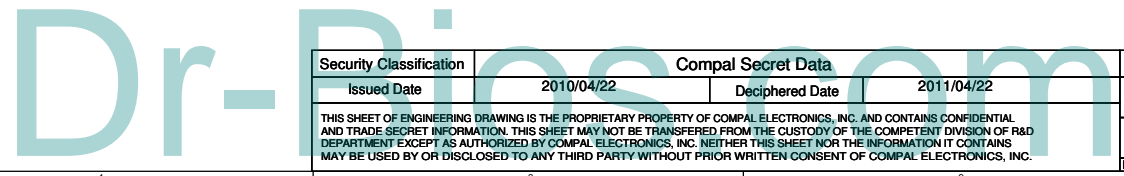
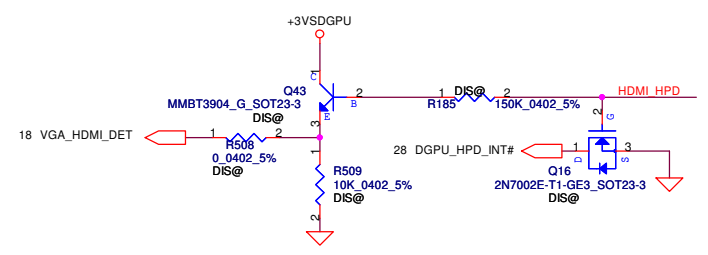
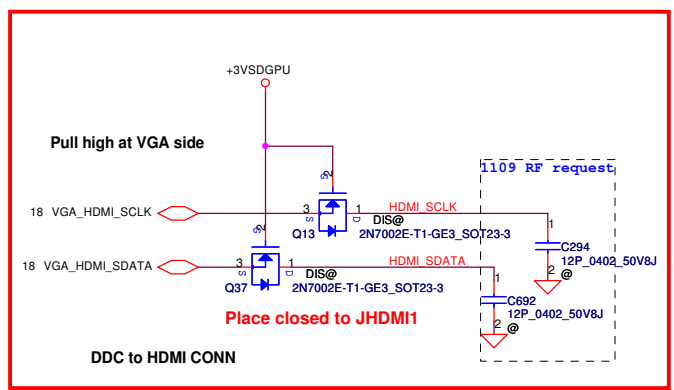
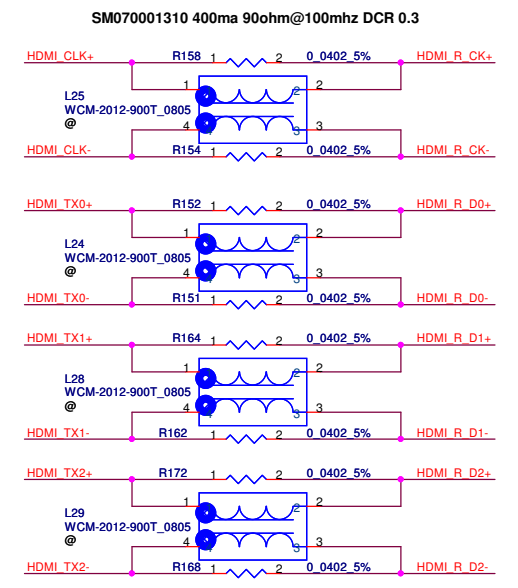
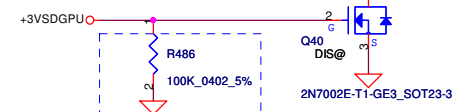
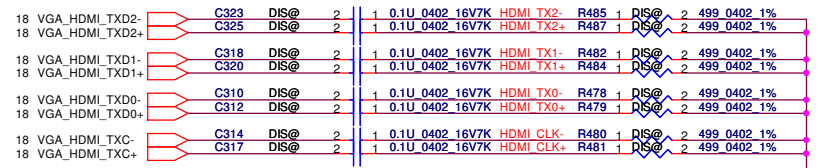
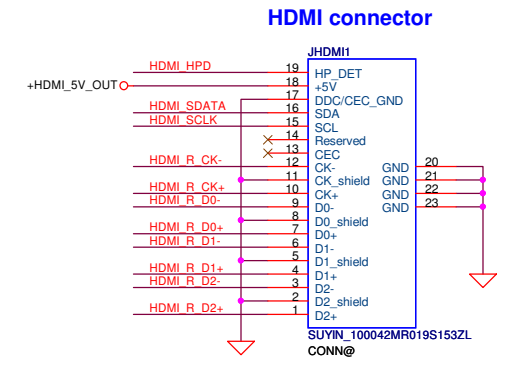
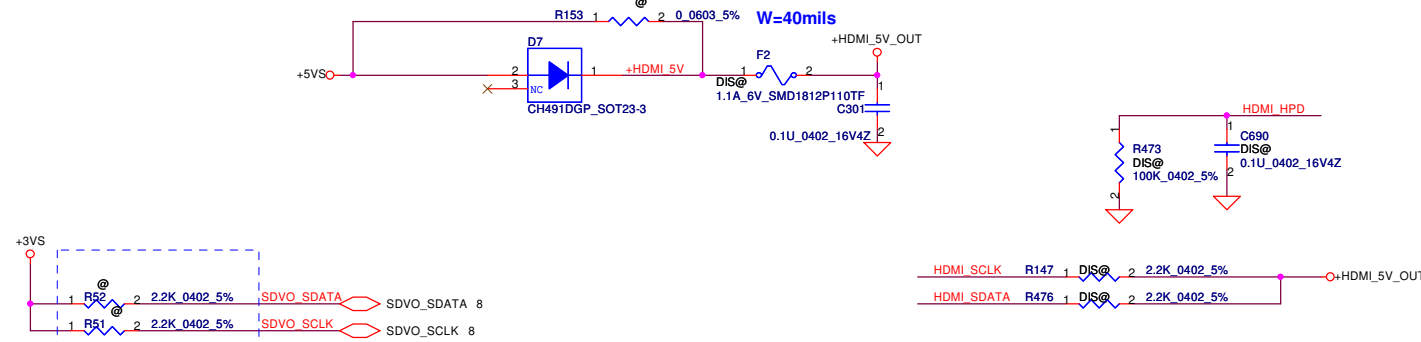


Discrete only

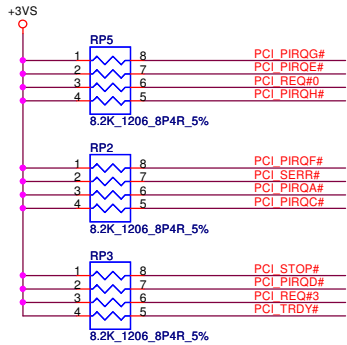
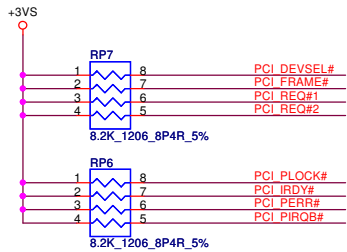


VGA_DDC_CLK · DATA
Pull high 4.7k at VGA side

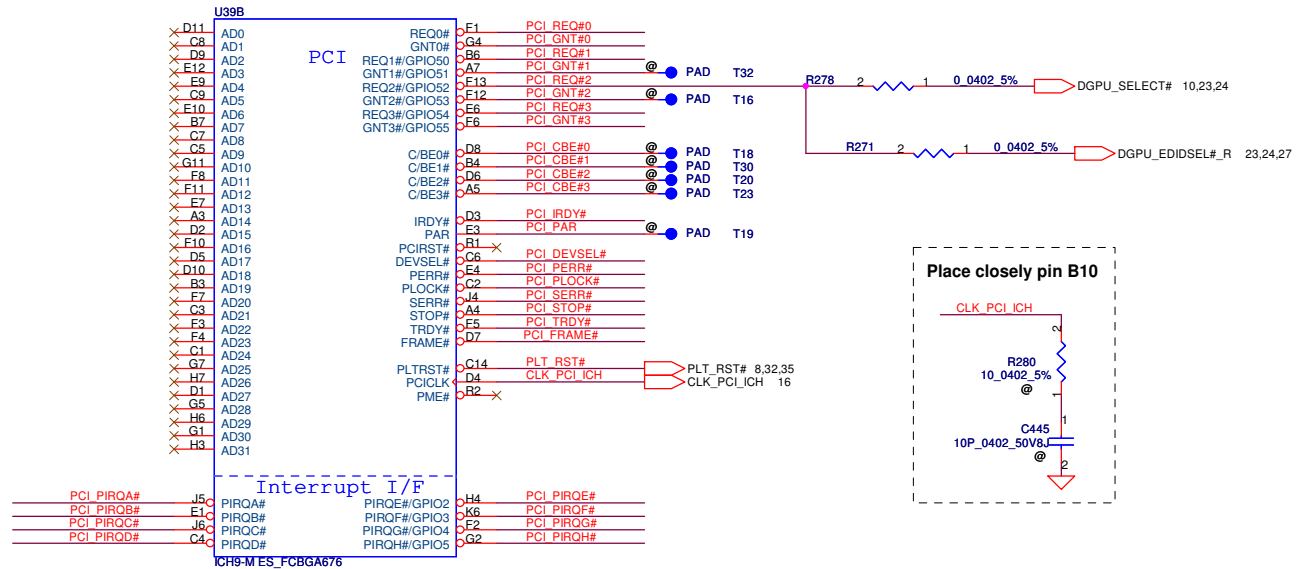
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Size B	Document Number	Date		Rev	
	PEW52 M/B LA-6632P Schematic	Wednesday, August 04, 2010		0.2	
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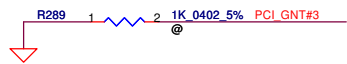
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/04/22	Deciphered Date	2011/04/22	Title	
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Size	Document Number	PEW52 M/B LA-6632P Schematic		Rev 0.2	
Date:	Wednesday, August 04, 2010	Sheet	25	of 52	



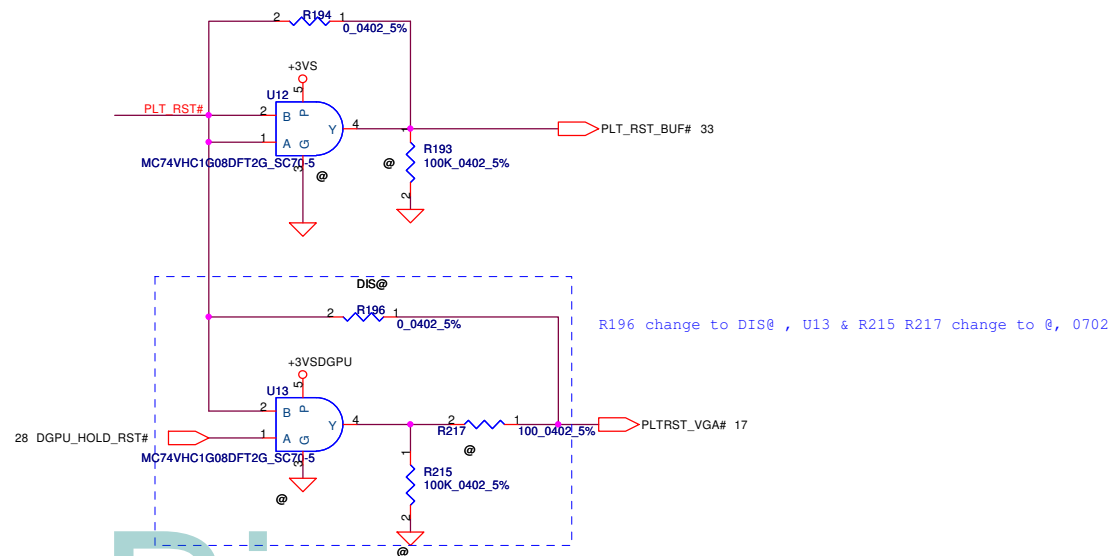
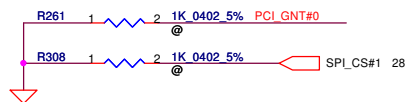
DMI for ESI-compatible operation
PCI_GNT#1 Low= DMI for ESI-compatible operation
 High= Default* (Internal pull-up)

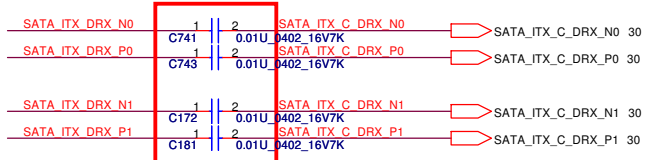
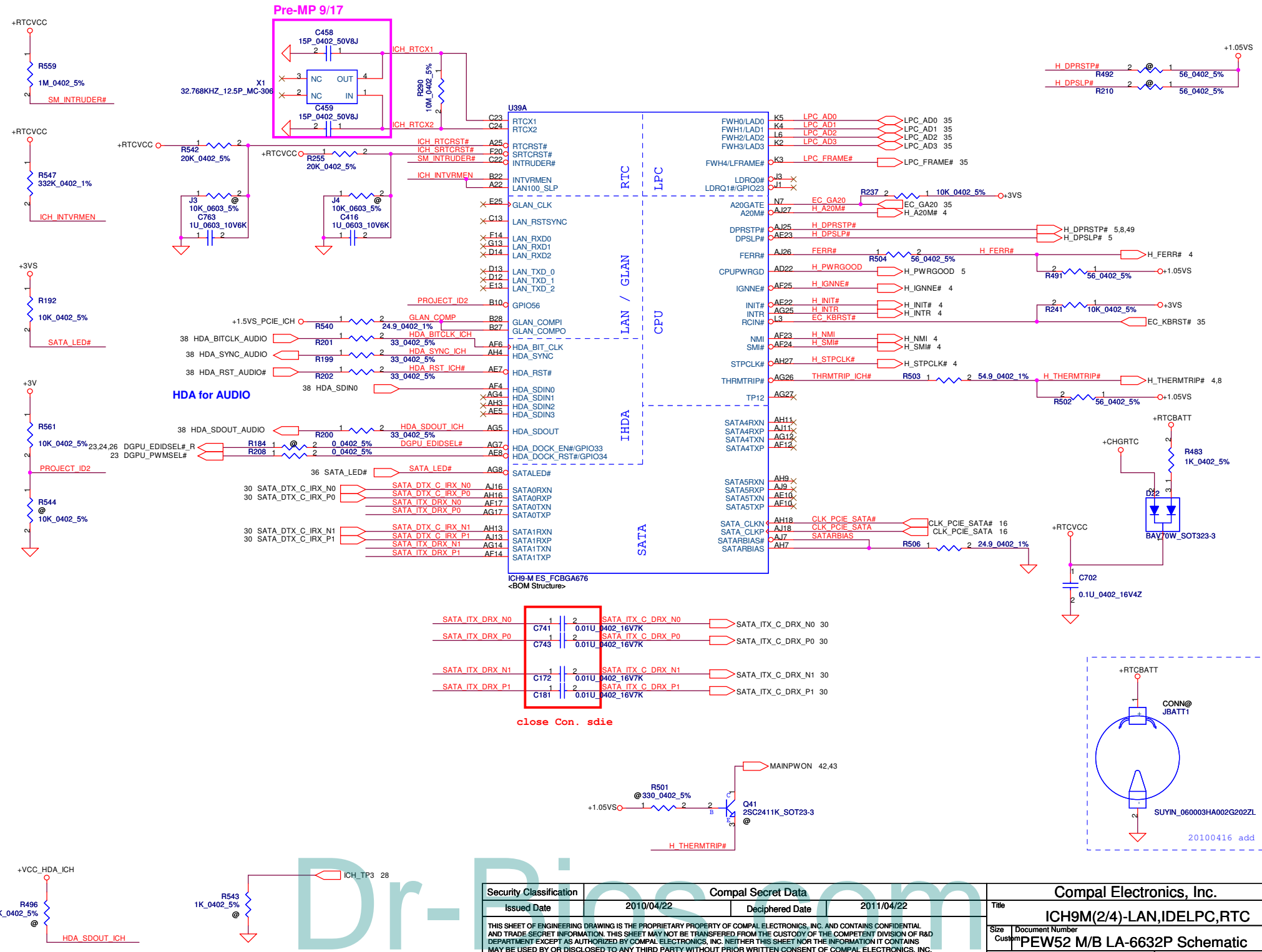


A16 Swap Override Strap
PCI_GNT#3 Low= A16 swap override Enable
 High= Default*

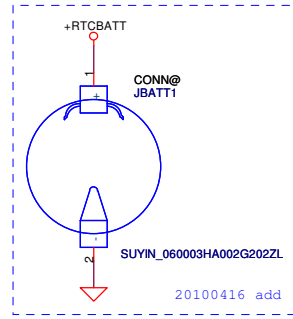
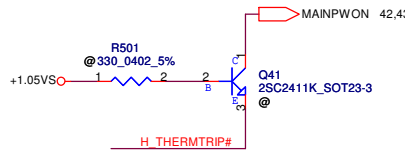


Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*

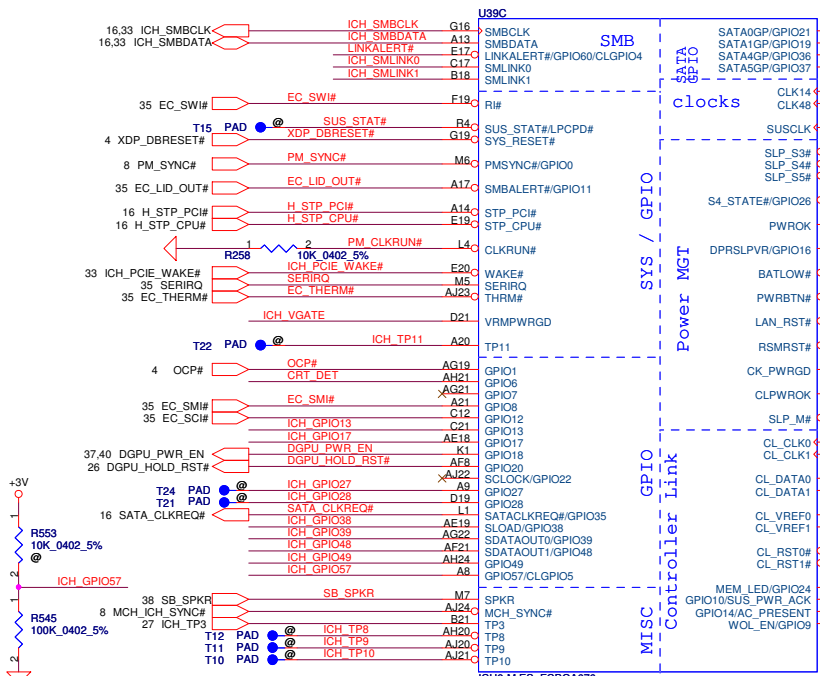
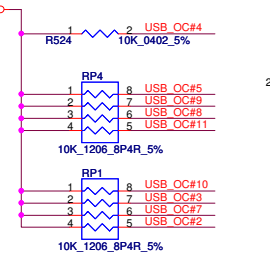
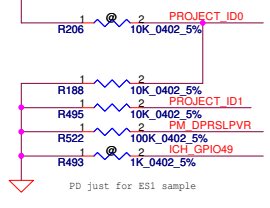
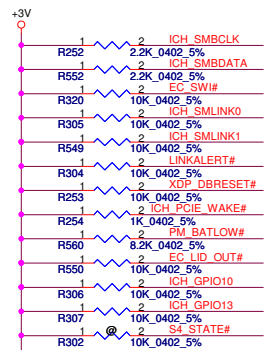
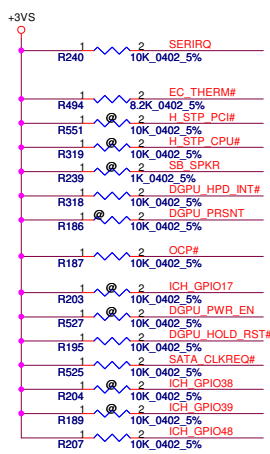




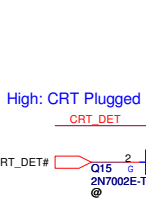
close Con. sdie



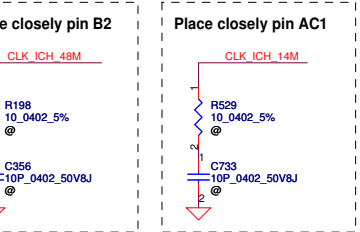
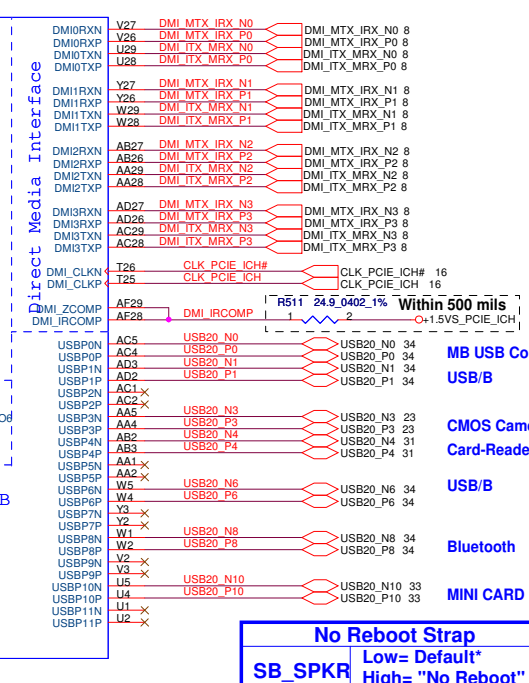
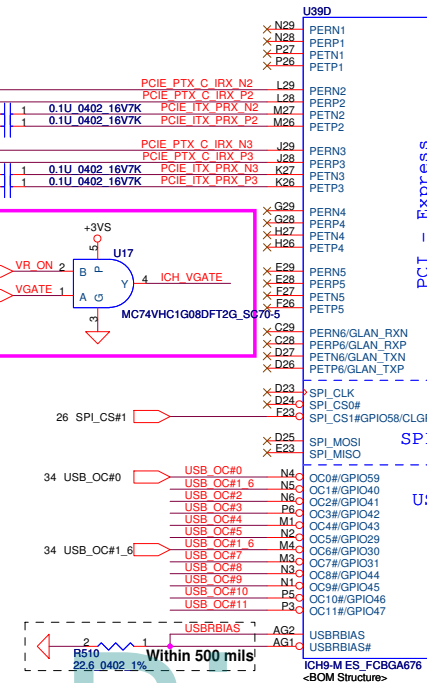
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/04/22	Deciphered Date	2011/04/22	Title	
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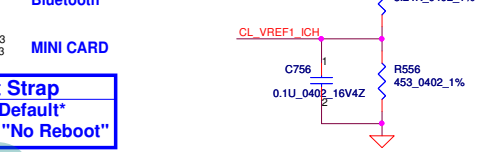
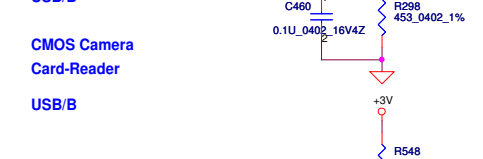
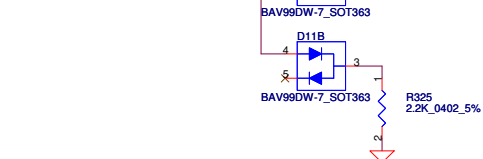
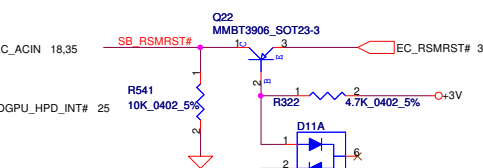
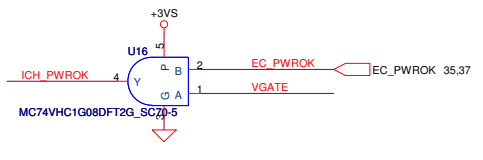
For MINI_CARD
 For PCIE LAN
 Change to Port 3 for SW Hsieh, York (TPE) request 20100426



	Project_ID0	Project_ID1	Project_ID2
UMA	0	0	0
DIS	0	0	1



No used Integrated LAN, connecting LAN_RST# to GND



No Reboot Strap
 Low= Default
 High= "No Reboot"
 SB_SPKR

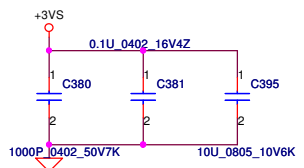
Internal TPM Strap
 Low= Disable*
 High= ITPM enable by MCH strap
 SPL_MOSI

DMI Termination Voltage
 Low= Desktop used
 High= Mobile* (Internal pull-up)
 GPIO49

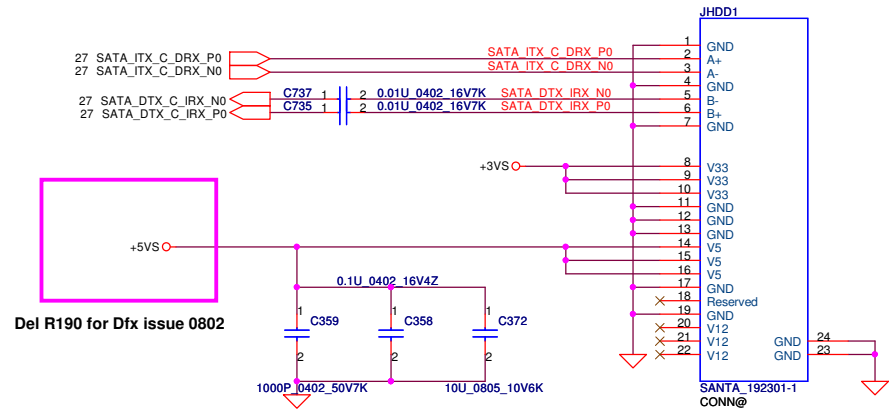
Security Classification	2010/04/22	Compal Secret Data	Deciphered Date	2011/04/22
Issued Date	2010/04/22	Deciphered Date	2011/04/22	

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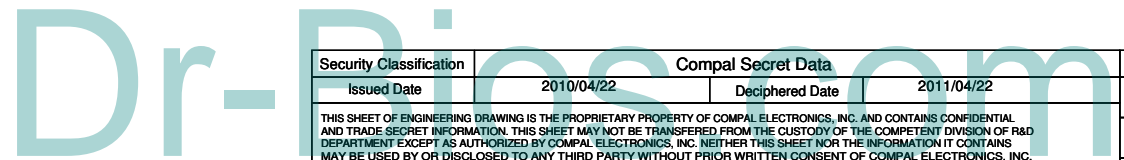
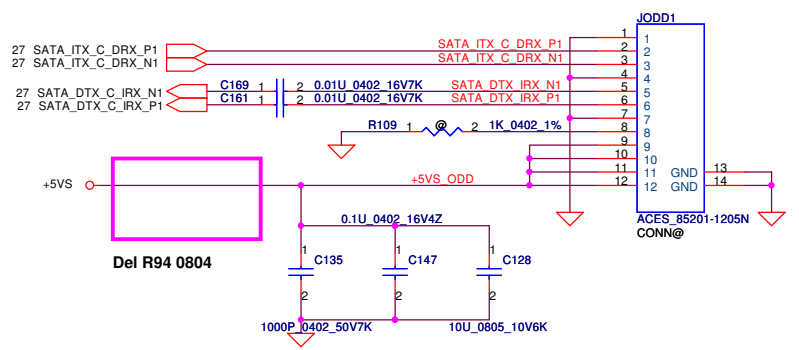
Compal Electronics, Inc.		
Title: ICH9M(3/4)-USB,GPIO,PCIE		
Size: Customer	Document Number: PEW52 M/B LA-6632P Schematic	Rev: 0.2
Date: Friday, August 06, 2010	Sheet: 28	of 52



SATA HDD Conn.

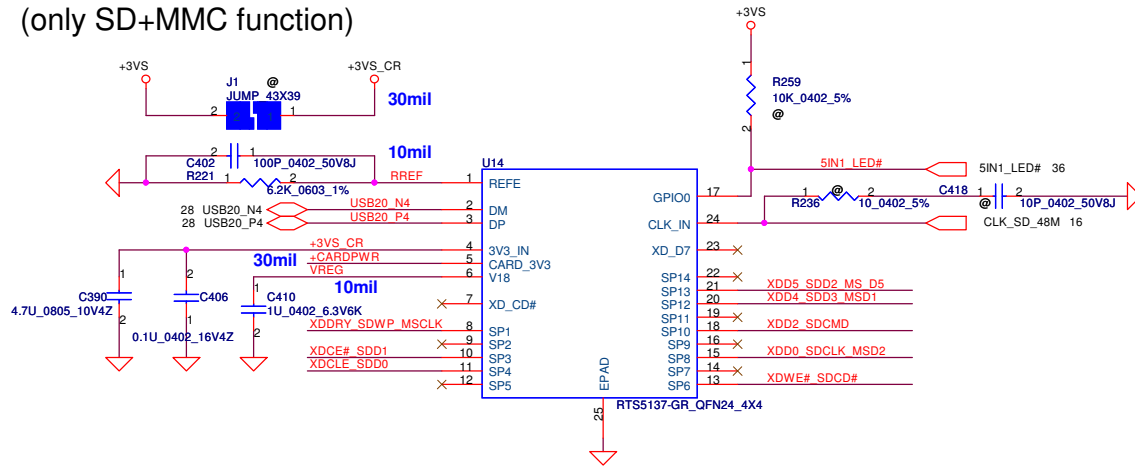


SATA ODD Conn.

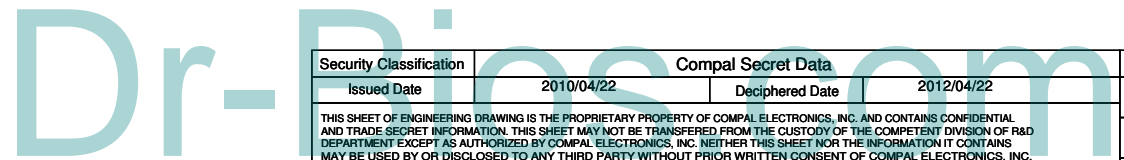
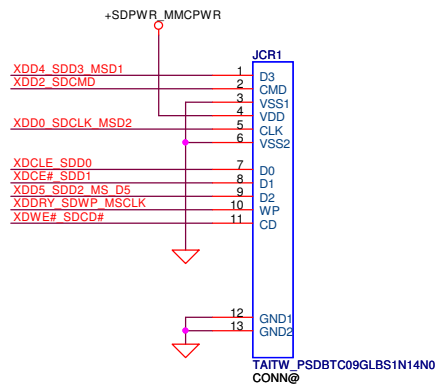
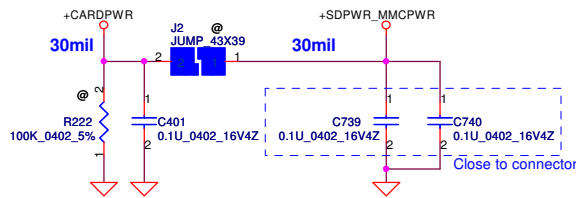


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Size	Document Number	Customer		Rev	0.2
Date:	Wednesday, August 04, 2010	Sheet	30	of	52

Card Reader RTS5138 / RTS5137 (only SD+MMC function)

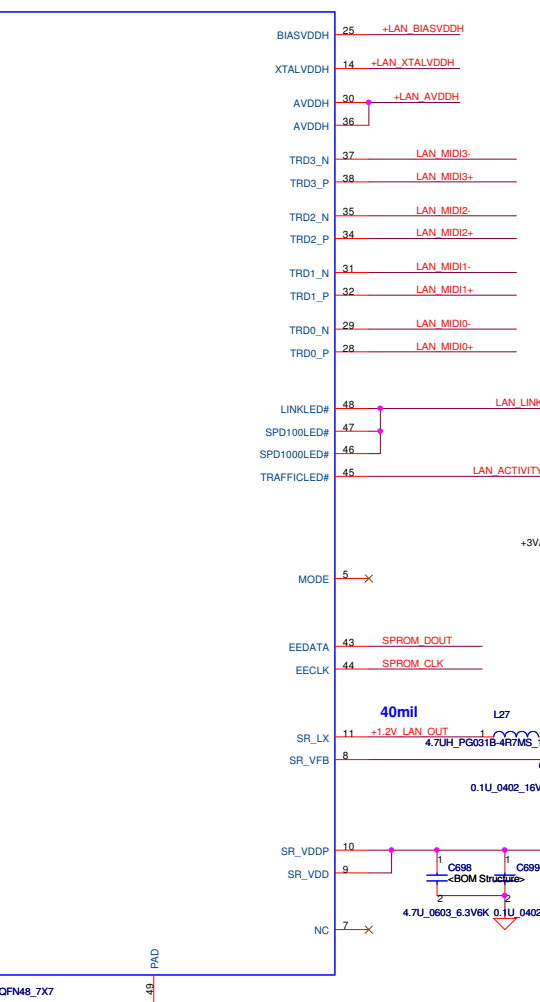
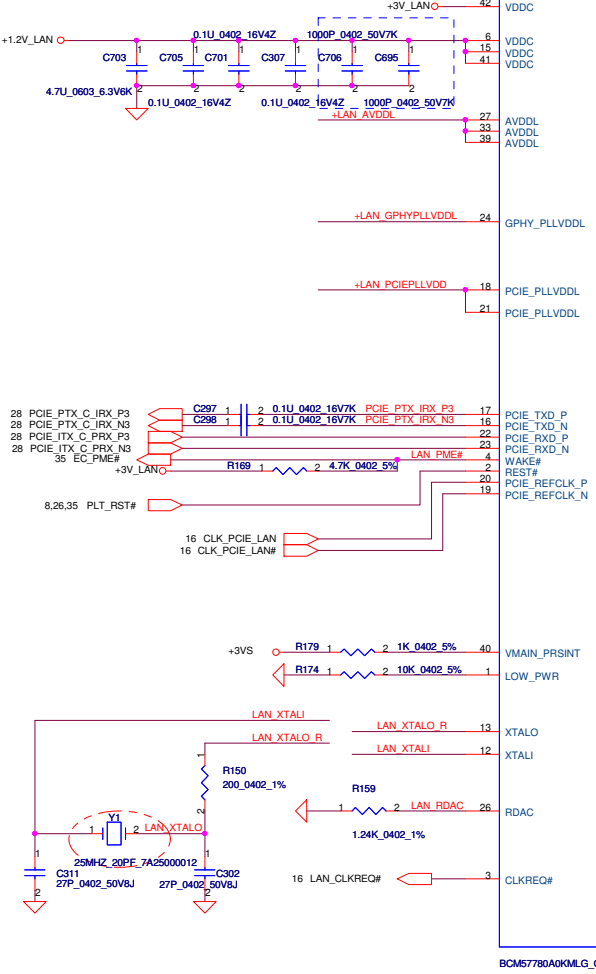


Card Reader Connector

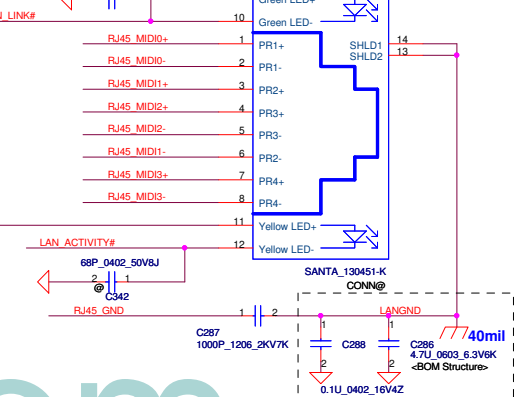
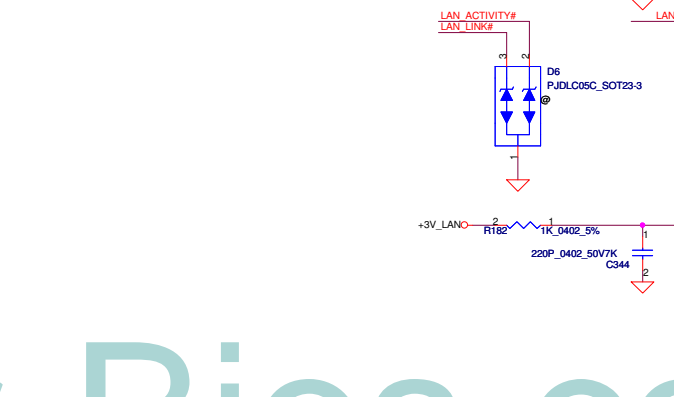
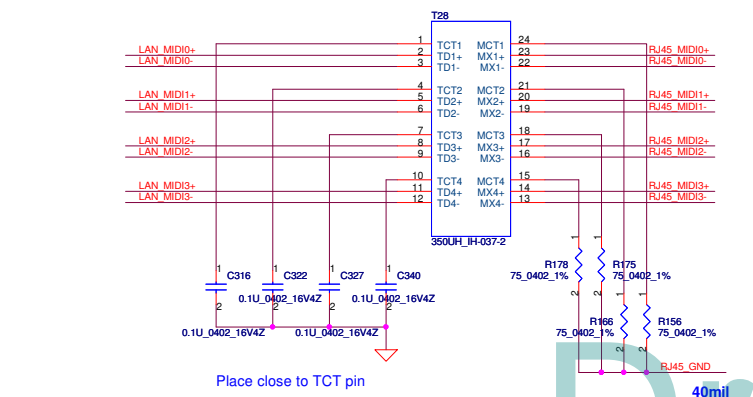
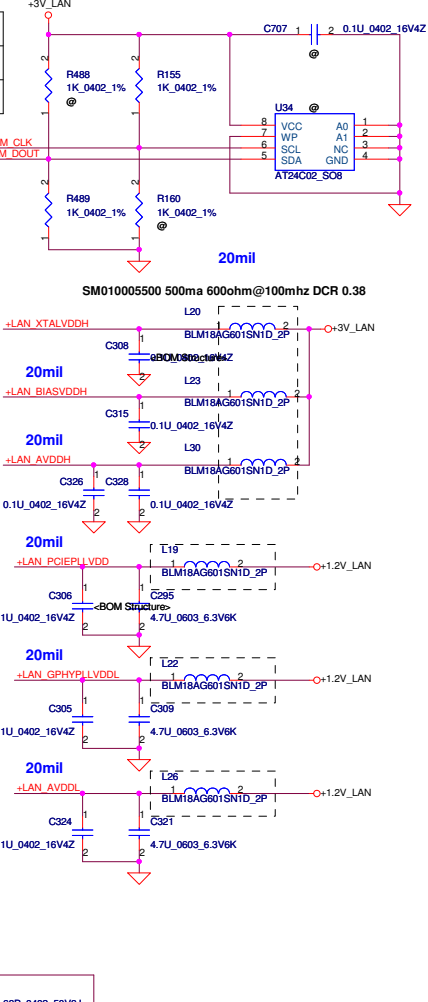


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091211 EMI add 1000P



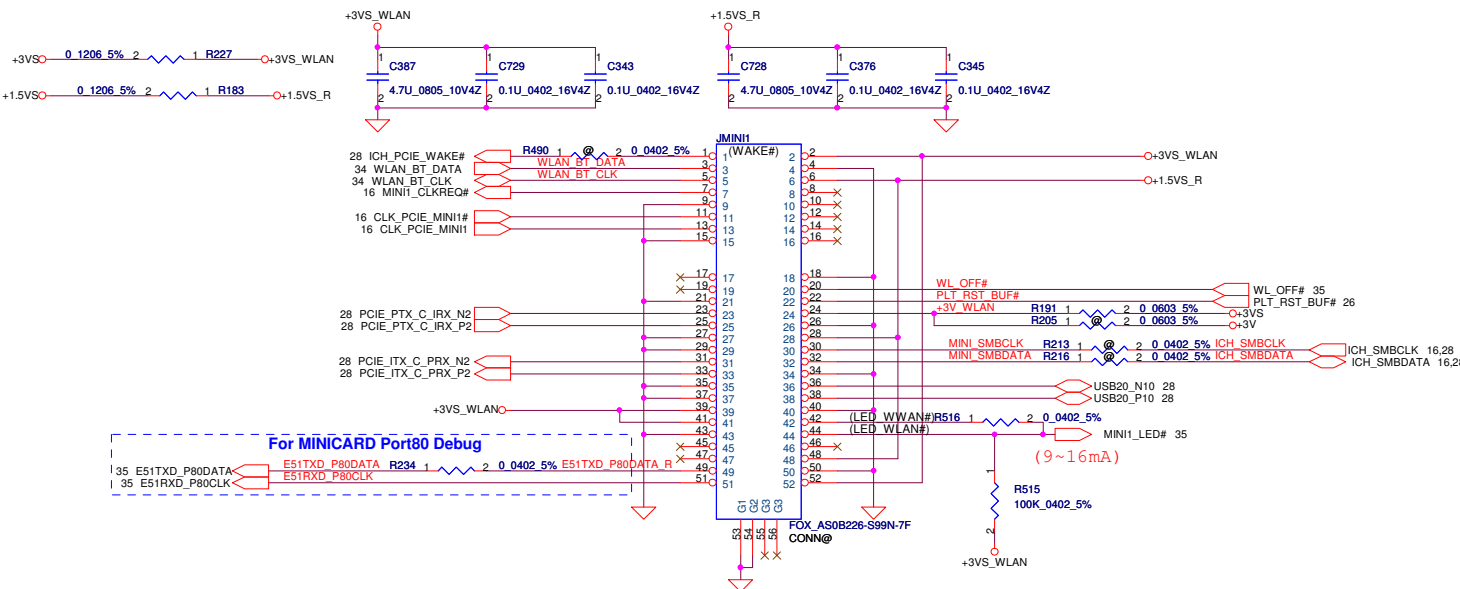
	SPROM_CLK (E2CLK)	SPROM_DOUT (E2DATA)
On chip	1	0
AT24C02	1	1



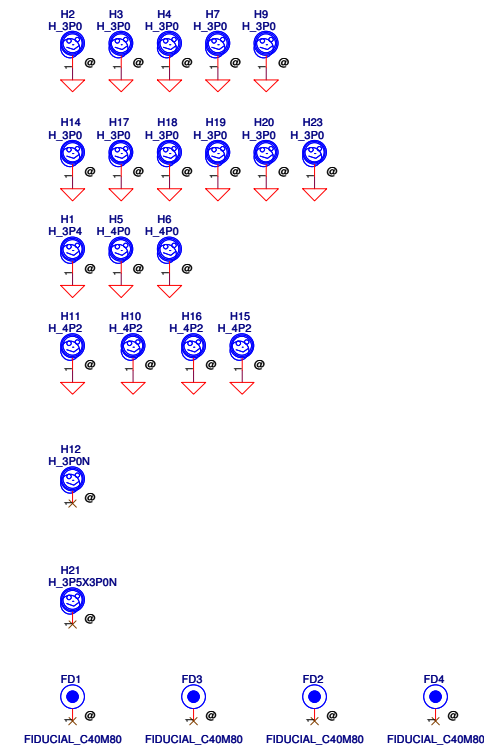
BOTH HAND: S X'FORM_GST5009-D LF LAN, SP050006B00
TIMAG:S X'FORM_IH-160 LAN , SP050006F00

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Size	Document Number	Customer	PEW52 M/B LA-6632P Schematic	Rev	0.2
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For Wireless LAN

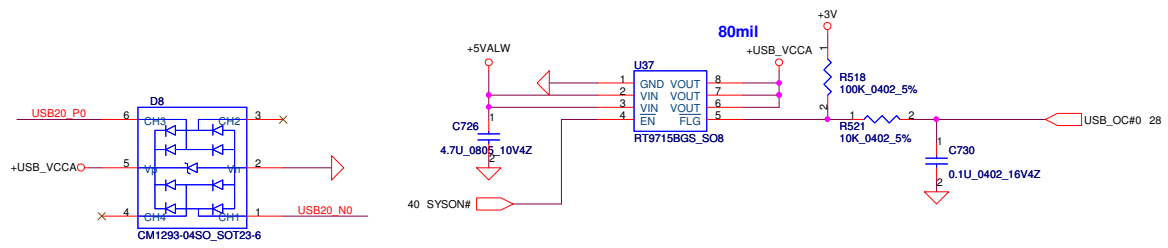


Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

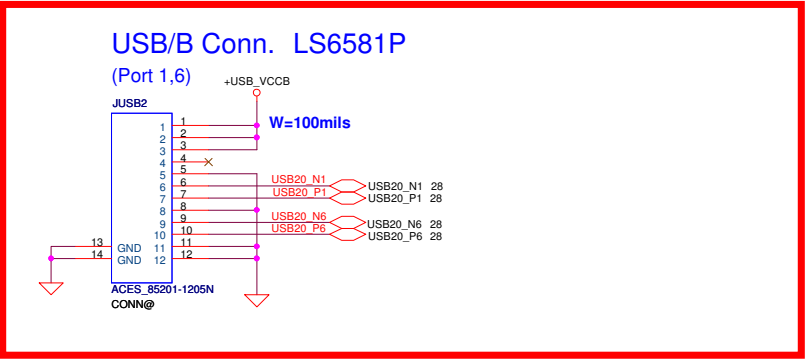
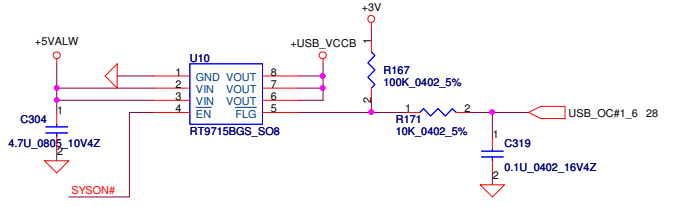
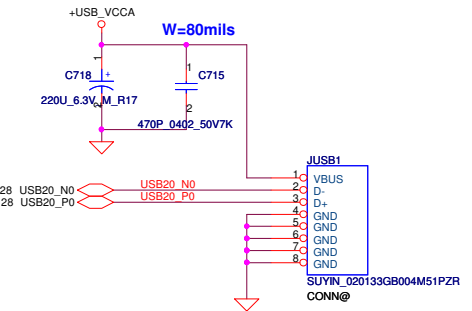


Dr-Bios.com

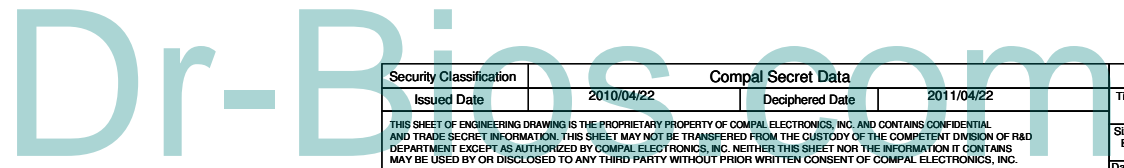
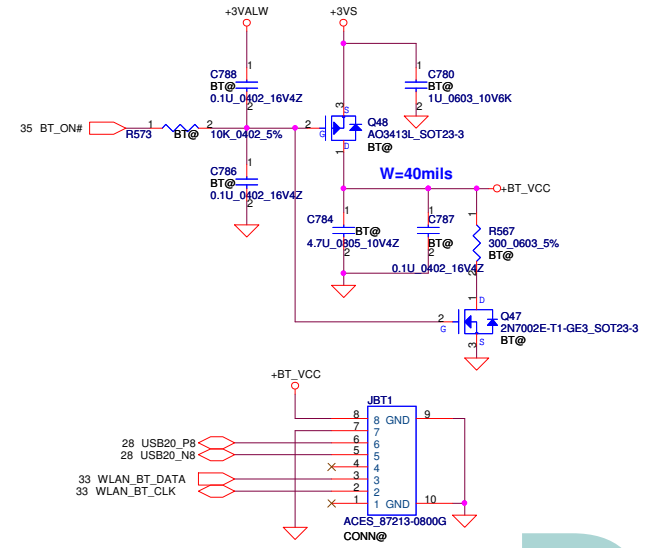
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Issued Date	2010/04/22	Deciphered Date	2011/04/22	Title MINI CARD (WLAN & TV-Tuner)	
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				Date	Wednesday, August 04, 2010
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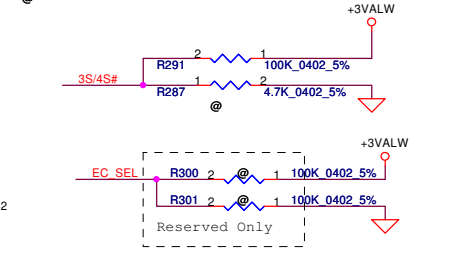
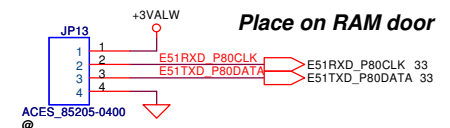
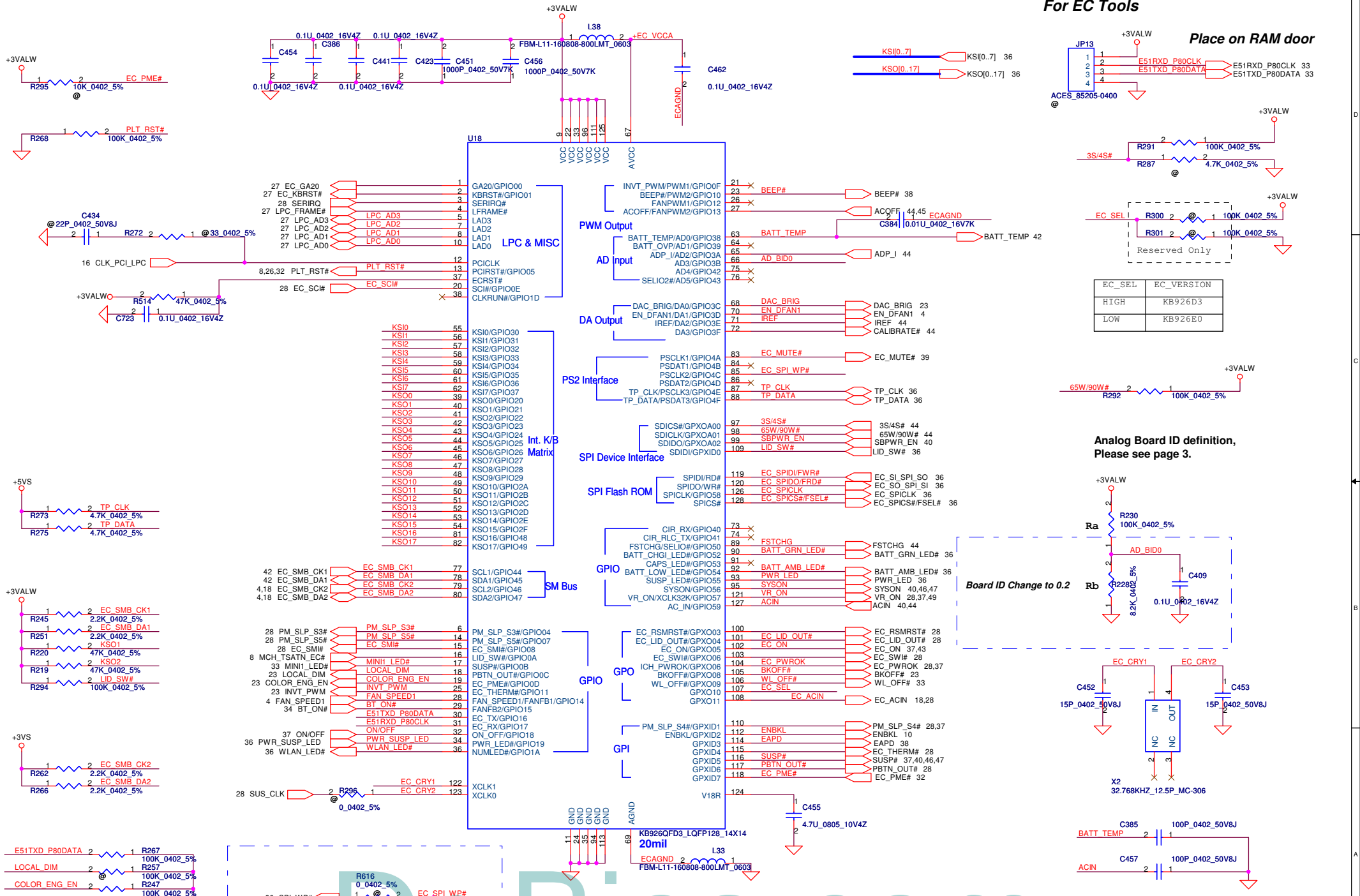
USB Conn.
(Port 0,1)



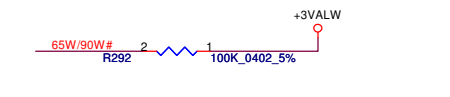
Bluetooth Conn.



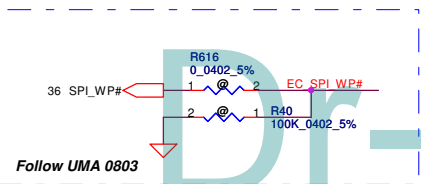
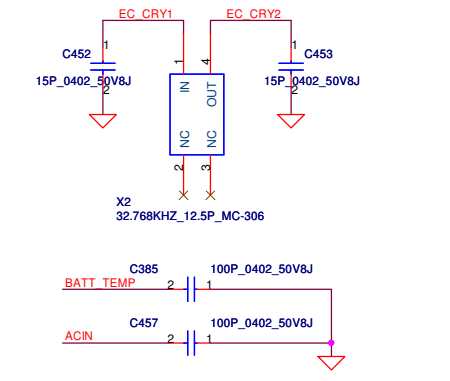
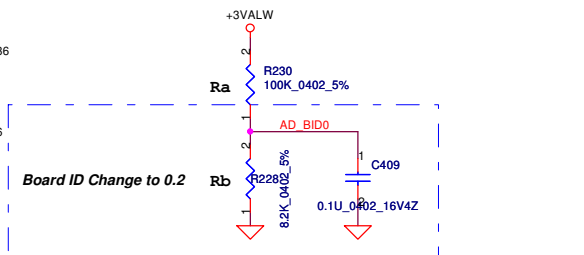
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				PEW52 M/B LA-6632P Schematic
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				Date: Wednesday, August 04, 2010
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EC_SEL	EC_VERSION
HIGH	KB926D3
LOW	KB926E0



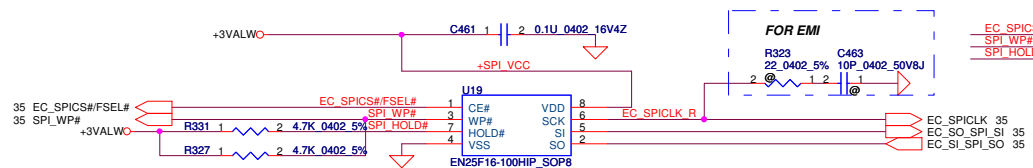
Analog Board ID definition, Please see page 3.



Follow UMA 0803

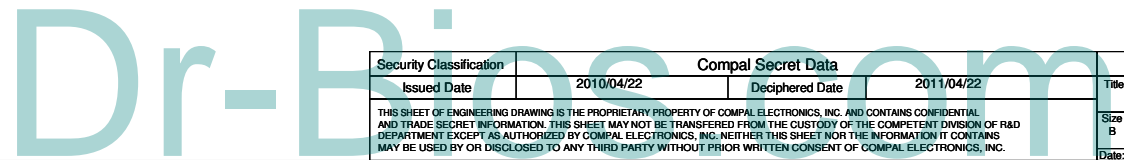
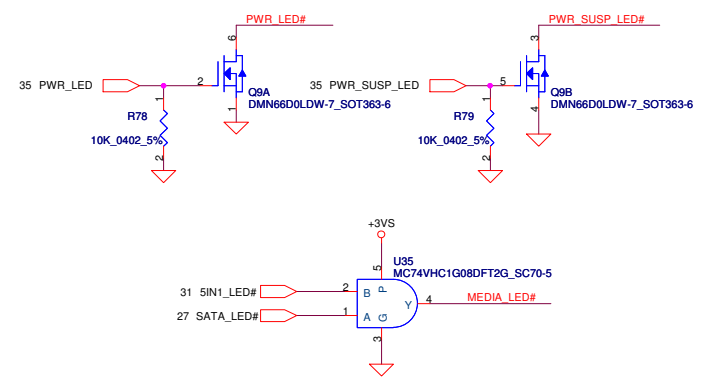
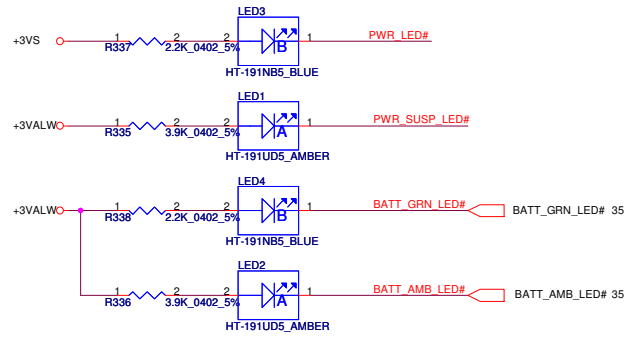
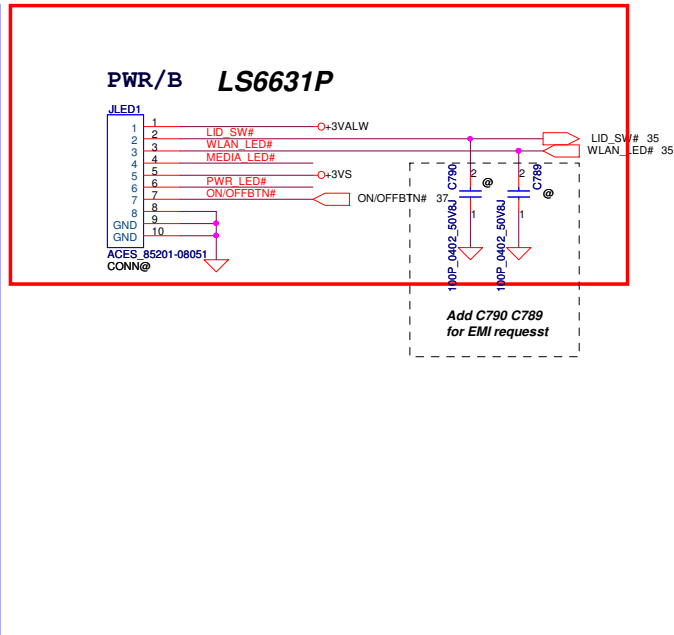
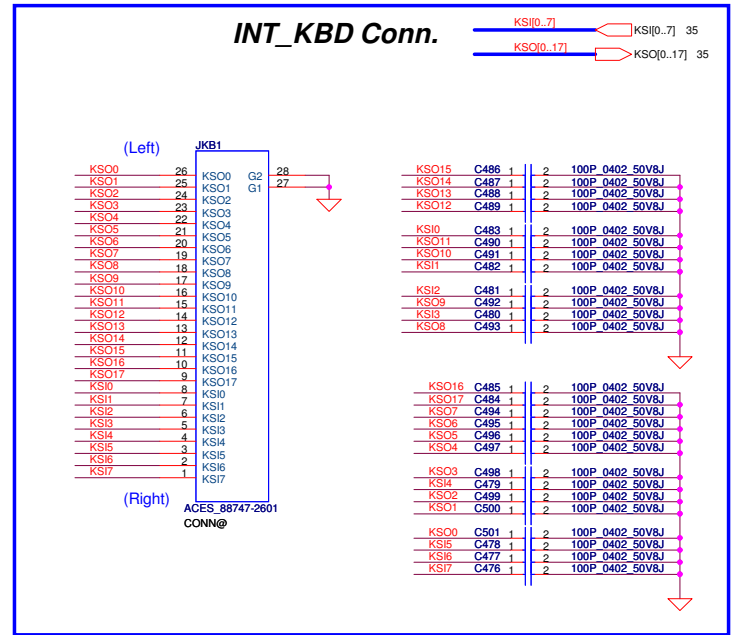
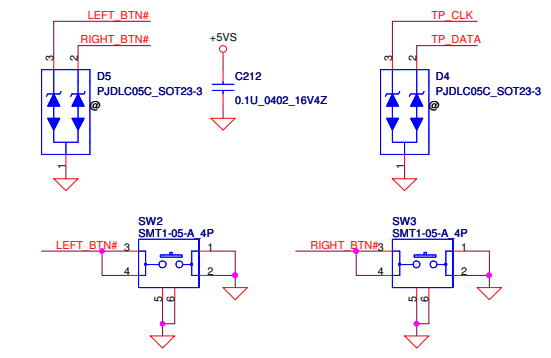
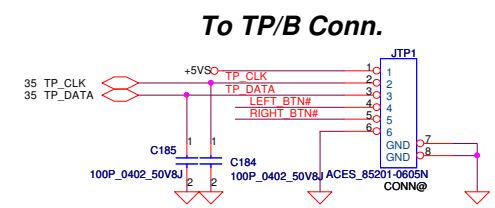
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Issued Date	2010/04/22	Deciphered Date	2011/04/22
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Title EC ENE KB926			
Size	Document Number	Rev	
B	PEW52 M/B LA-6632P Schematic	0.2	
Date:	Thursday, August 05, 2010	Sheet	35 of 52



ENE suggestion SPI Frequency over 66MHz
 SST: 50MHz
 MXIC: 70MHz
 ST: 40MHz

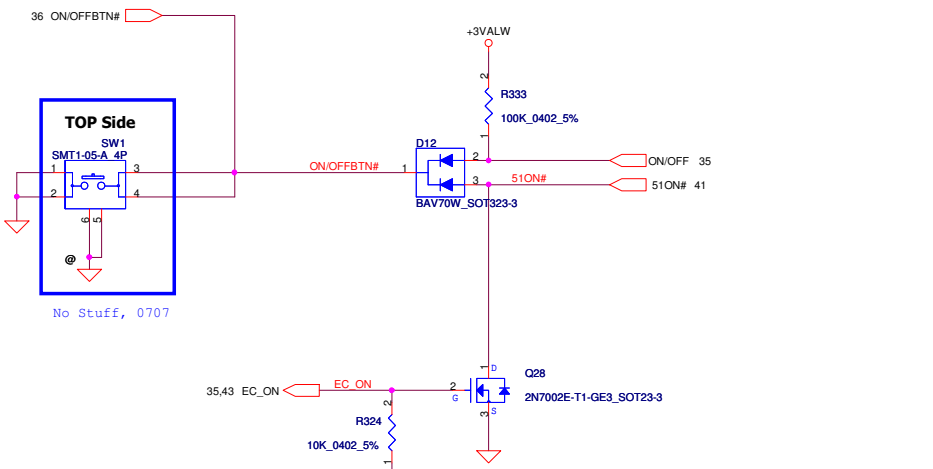
Reserved for BIOS simulator.
 Footprint S08



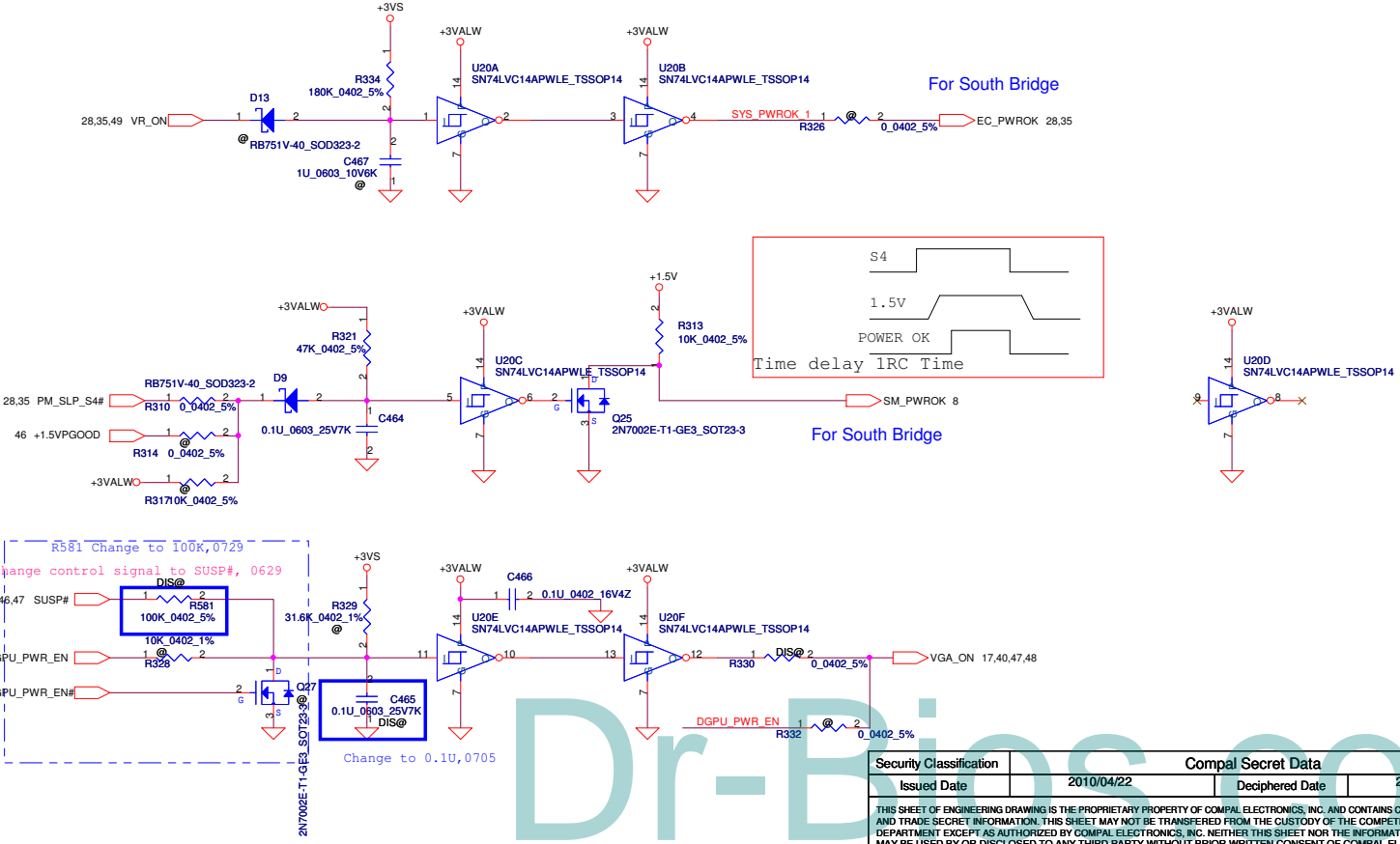
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/04/22	Deciphered Date	2011/04/22	Title
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Size	Document Number	Rev	Date	
B	PEW52 M/B LA-6632P Schematic	0.2	Friday, August 06, 2010	Sheet 36 of 52

Power Button

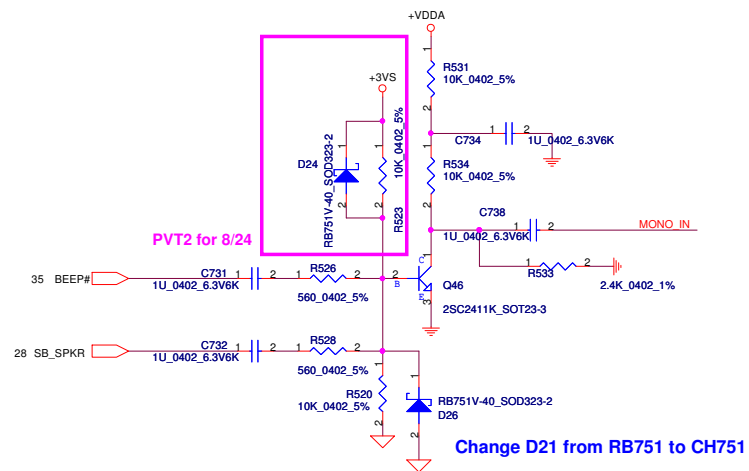
ON/OFF switch



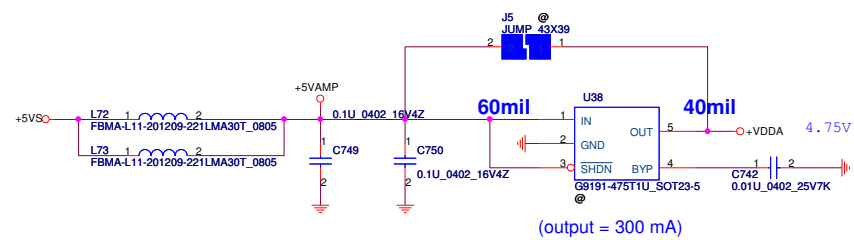
Power ON Circuit



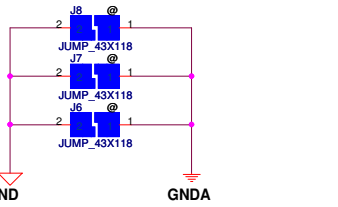
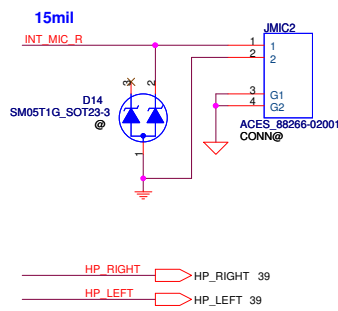
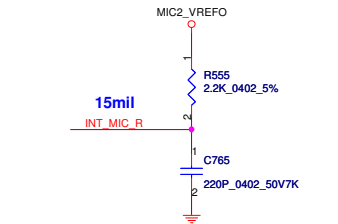
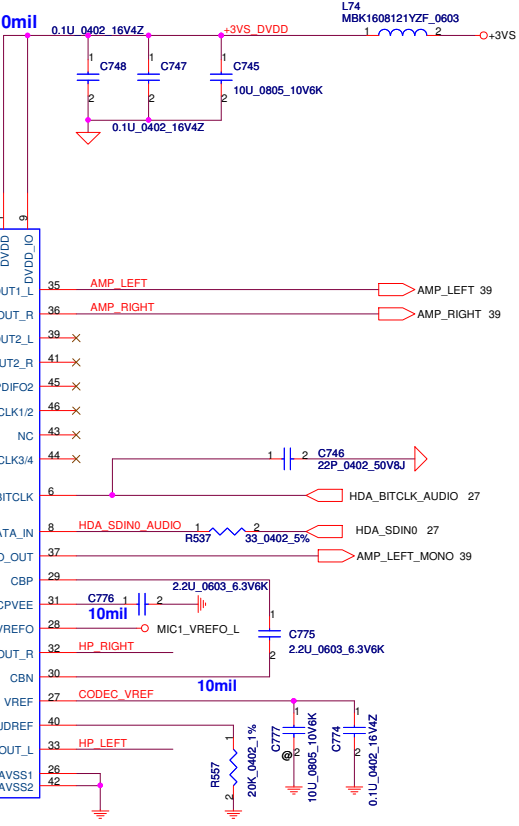
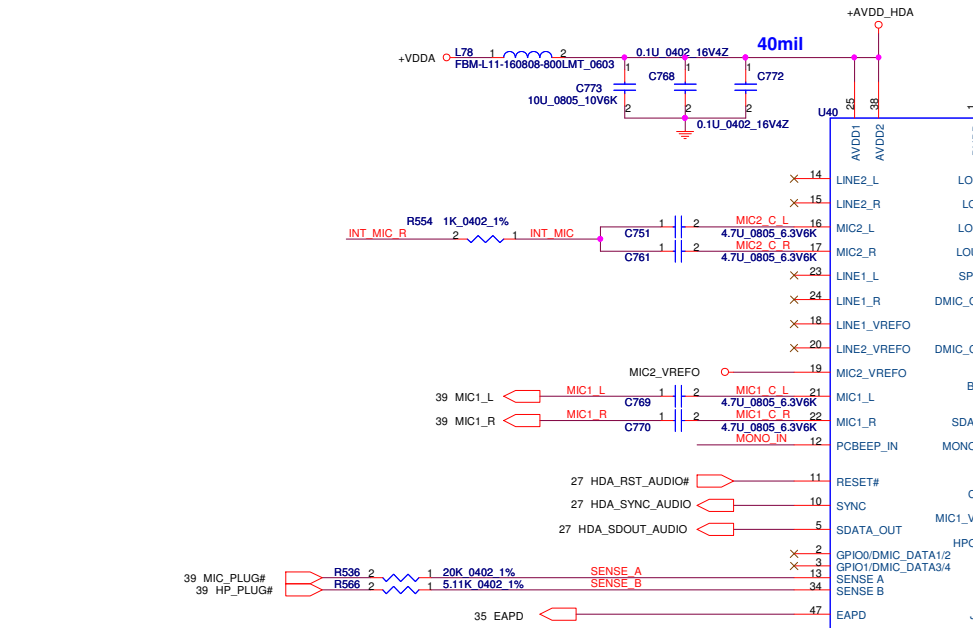
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/04/22	Deciphered Date	2011/04/22	Title	
				Power OK, Reset	
Size	Document Number	Date		Rev	
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				Sheet	52



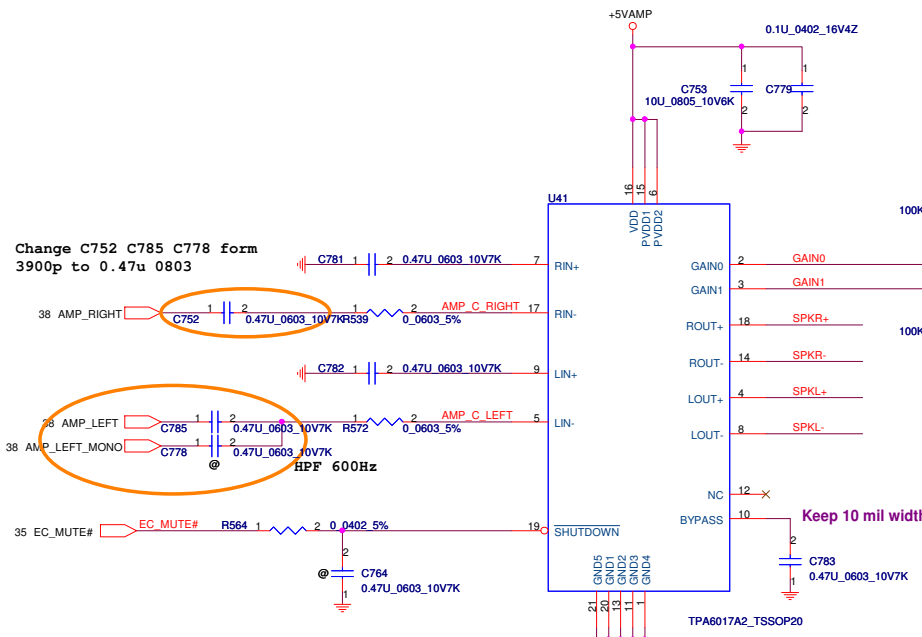
HD Audio Codec



(output = 300 mA)



Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	
	20K	PORT-B (PIN 21, 22)
	10K	
	5.1K	
SENSE B	39.2K	
	20K	
	10K	
	5.1K	PORT-H (PIN 32,33)

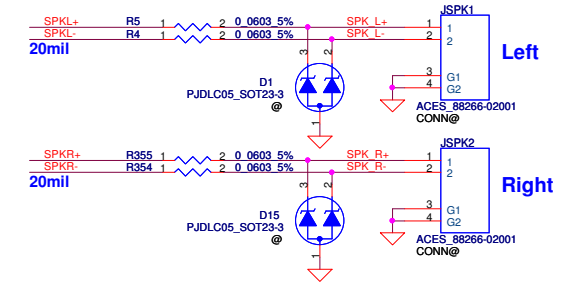


Change C752 C785 C778 form 3900p to 0.47u 0803

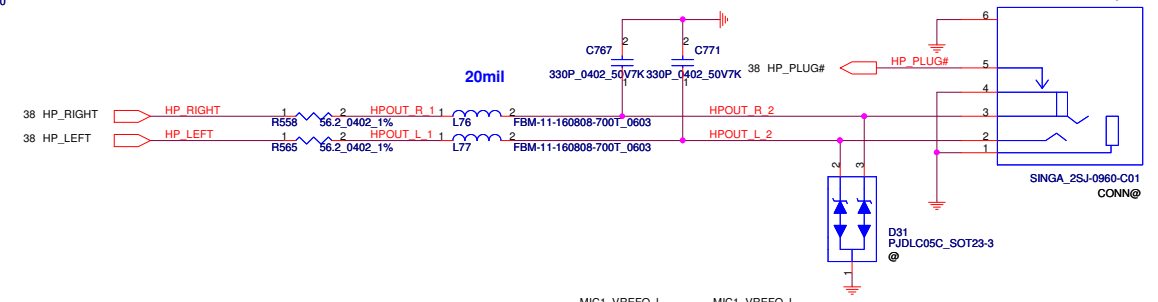
HPF 600Hz

Keep 10 mil width

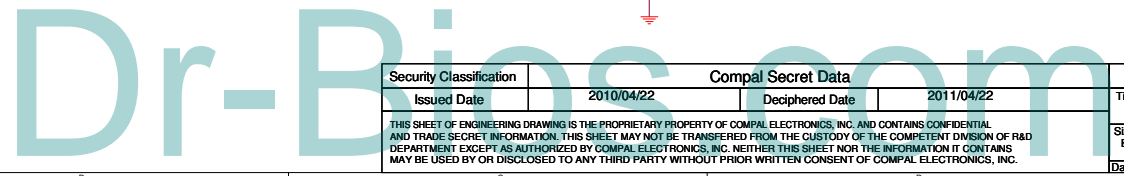
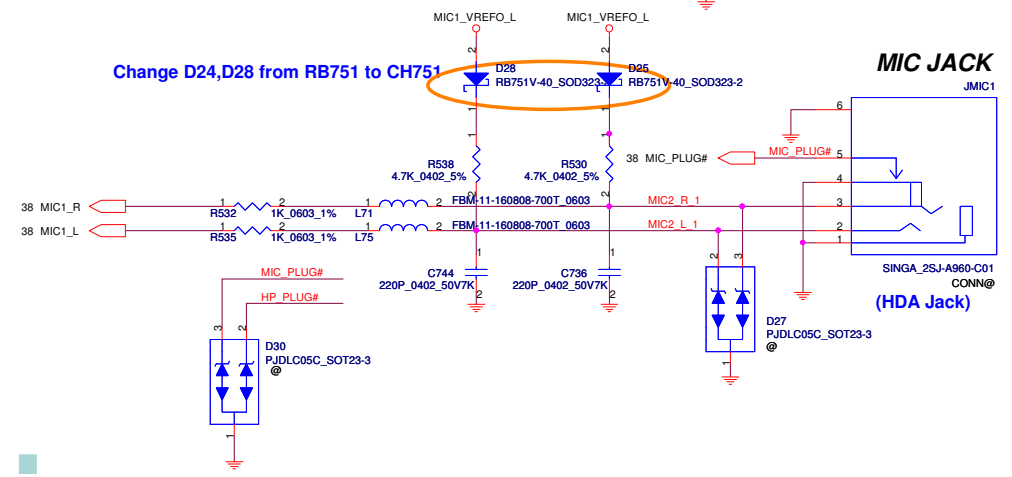
Int. Speaker Conn.



LINE Out/Headphone Out

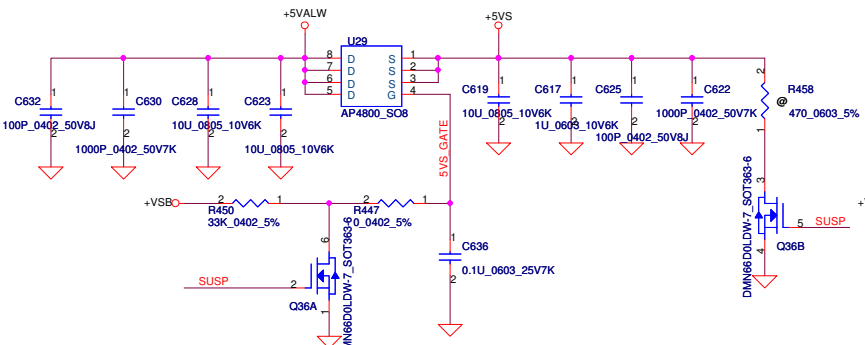


Change D24,D28 from RB751 to CH751

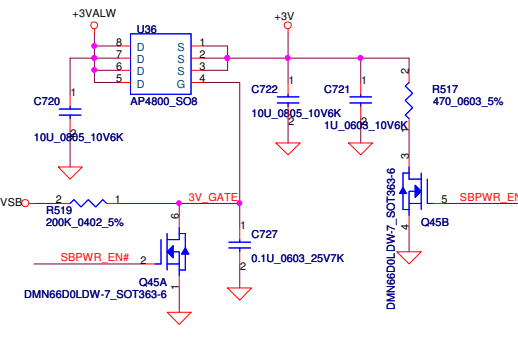


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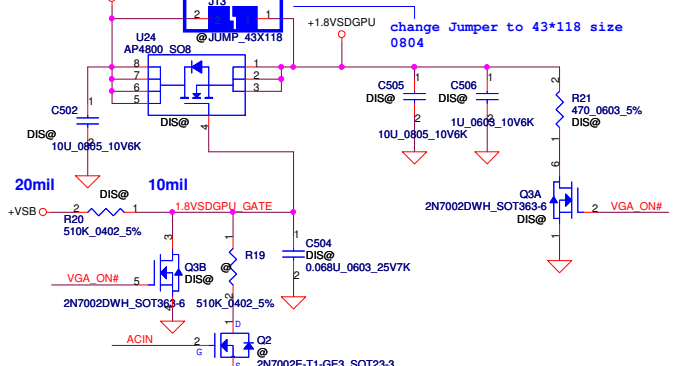
+5VALW TO +5VS



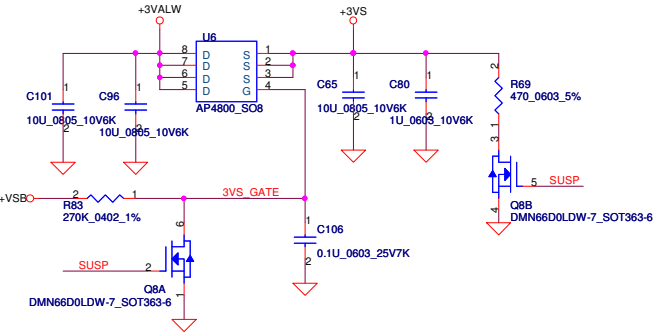
+3VALW TO +3V_SB(ICH8M AUX Power)



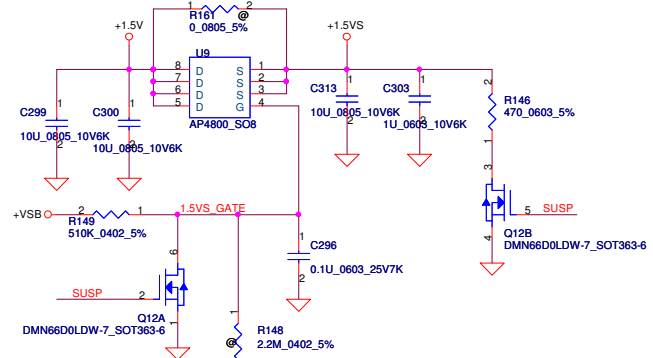
+1.8VS to +1.8VSDGPU for GPU



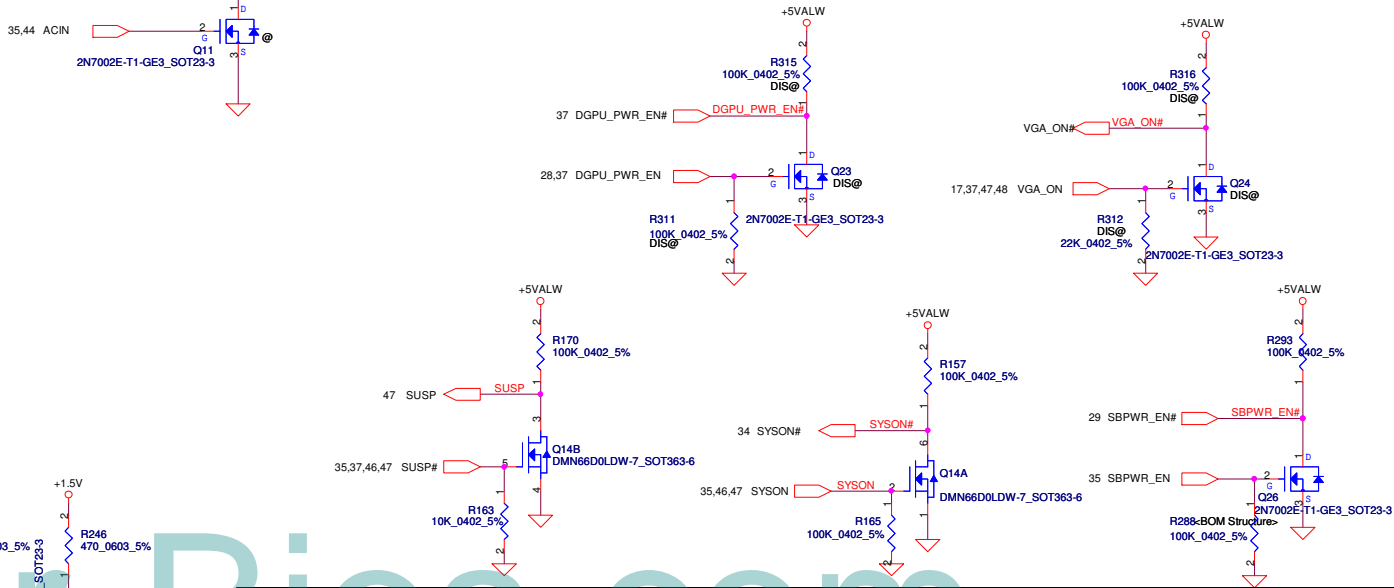
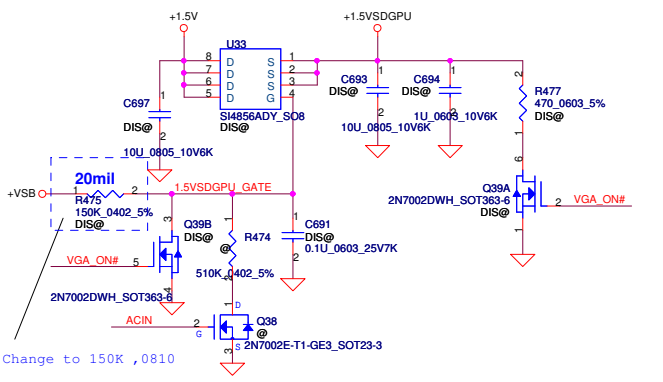
+3VALW TO +3VS



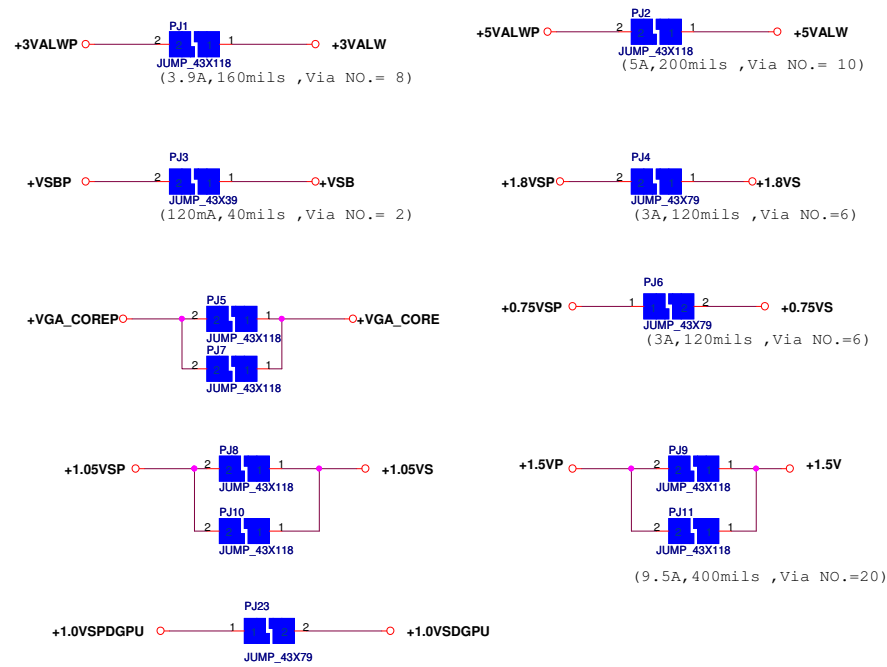
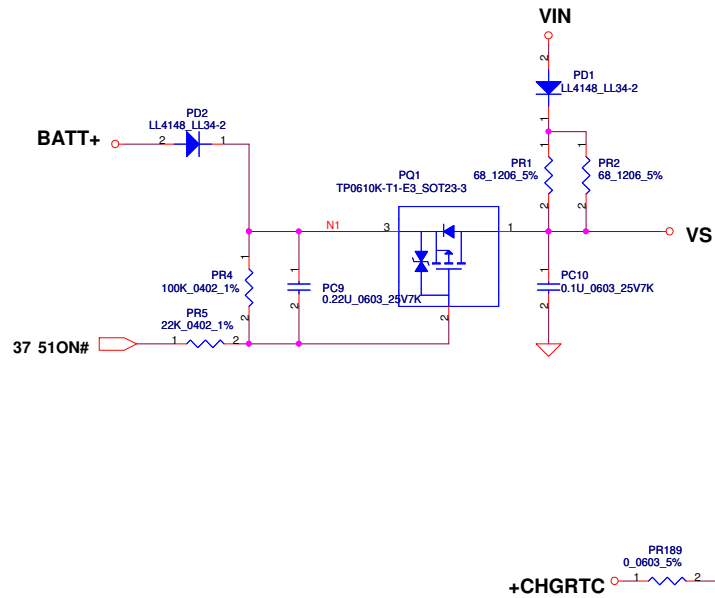
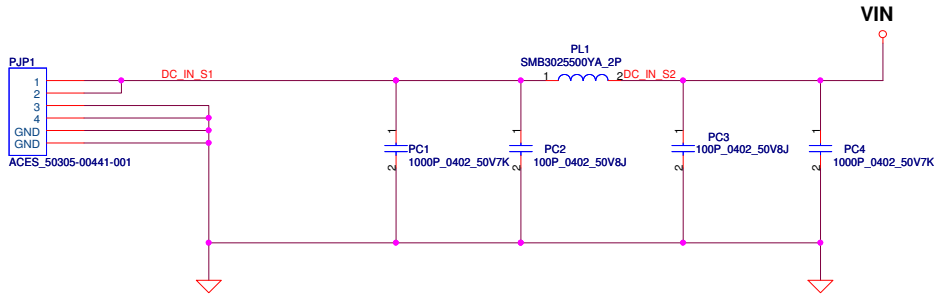
+1.5V to +1.5VS



+1.5V to +1.5VSDGPU for GPU

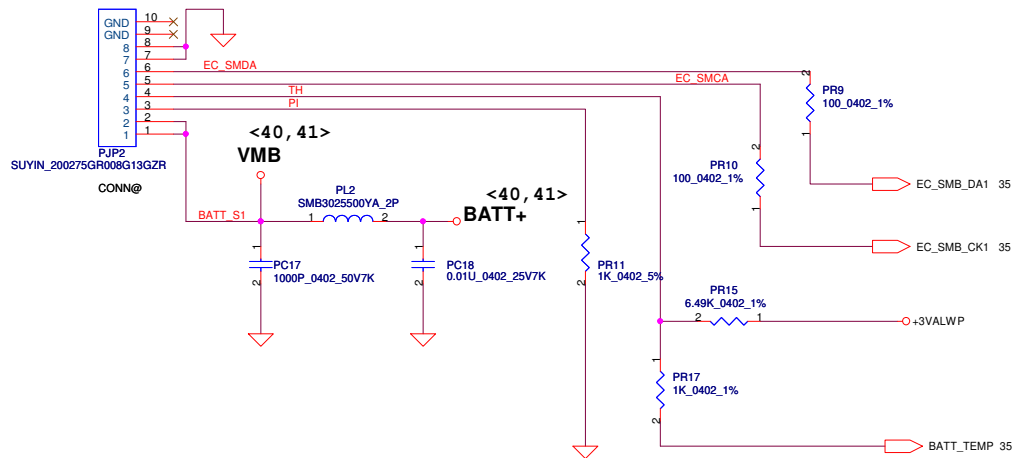


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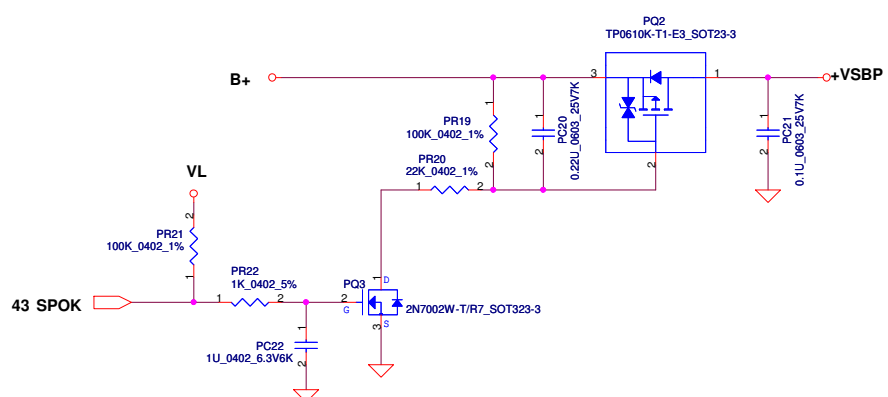
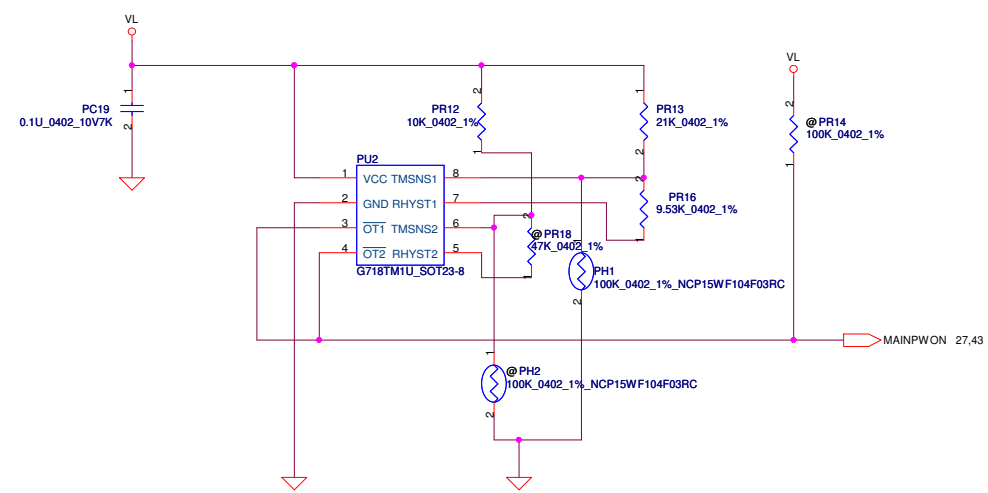


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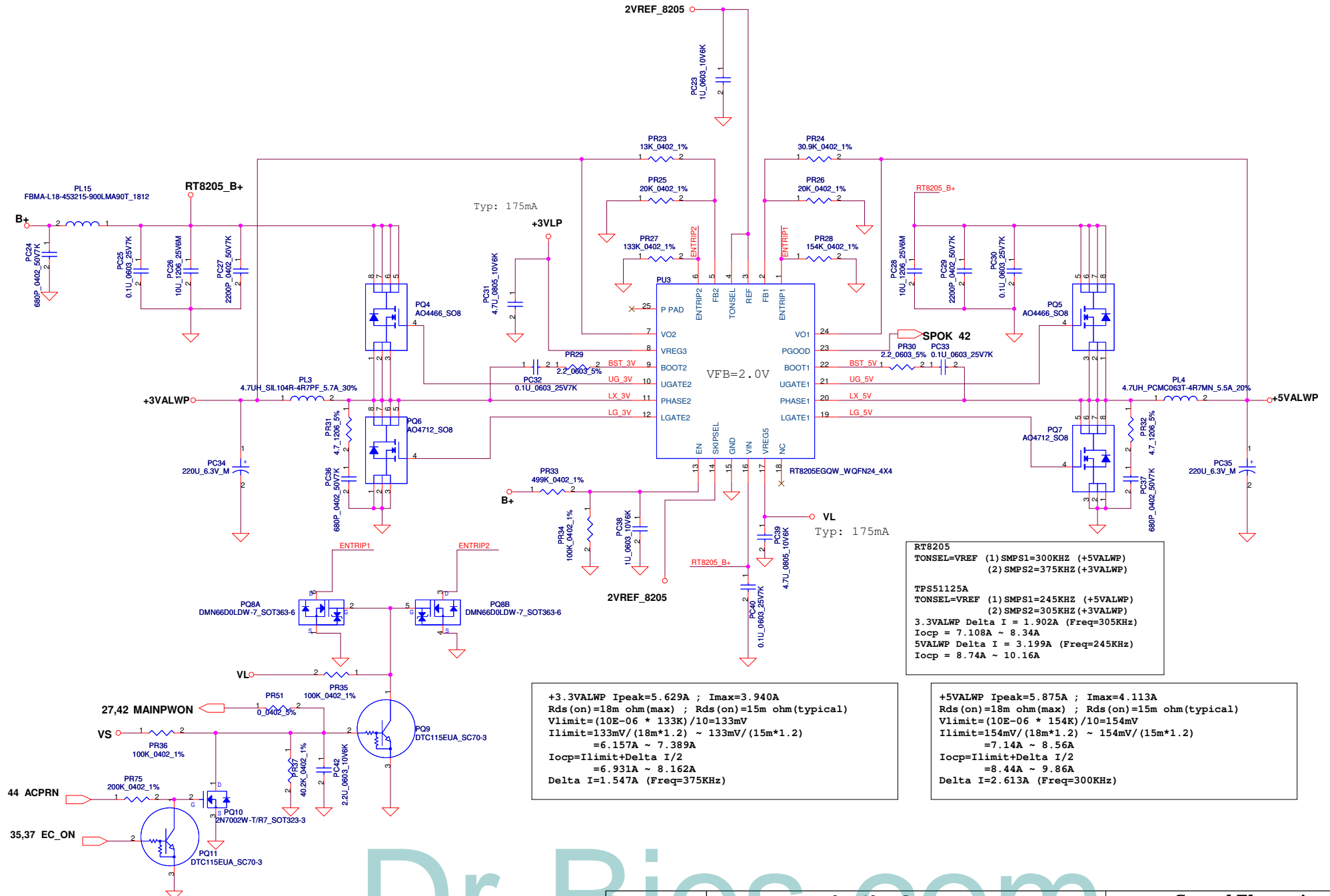
PH1 under CPU botten side :
 CPU thermal protection at 92 degree C
 Recovery at 56 degree C



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Note:
 Use TPS51125 IC can remove RTC refernece LDO
 Use TPS51427 IC must keep RTC refernece LDO



Typ: 175mA

VFB=2.0V

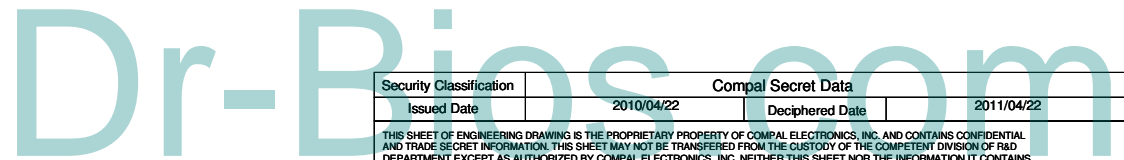
Typ: 175mA

RT8205
 TONSEL=VREF (1) SMPS1=300KHZ (+5VALWP)
 (2) SMPS2=375KHZ (+3VALWP)

TPS51125A
 TONSEL=VREF (1) SMPS1=245KHZ (+5VALWP)
 (2) SMPS2=305KHZ (+3VALWP)
 3.3VALWP Delta I = 1.902A (Freq=305KHz)
 Iocp = 7.108A ~ 8.34A
 5VALWP Delta I = 3.199A (Freq=245KHz)
 Iocp = 8.74A ~ 10.16A

+3.3VALWP Ipeak=5.629A ; Imax=3.940A
 Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
 Vlimit=(10E-06 * 133K)/10=133mV
 Ilimit=133mV/(18m*1.2) ~ 133mV/(15m*1.2)
 =6.157A ~ 7.389A
 Iocp=Ilimit+Delta I/2
 =6.931A ~ 8.162A
 Delta I=1.547A (Freq=375KHz)

+5VALWP Ipeak=5.875A ; Imax=4.113A
 Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
 Vlimit=(10E-06 * 154K)/10=154mV
 Ilimit=154mV/(18m*1.2) ~ 154mV/(15m*1.2)
 =7.14A ~ 8.56A
 Iocp=Ilimit+Delta I/2
 =8.44A ~ 9.86A
 Delta I=2.613A (Freq=300KHz)

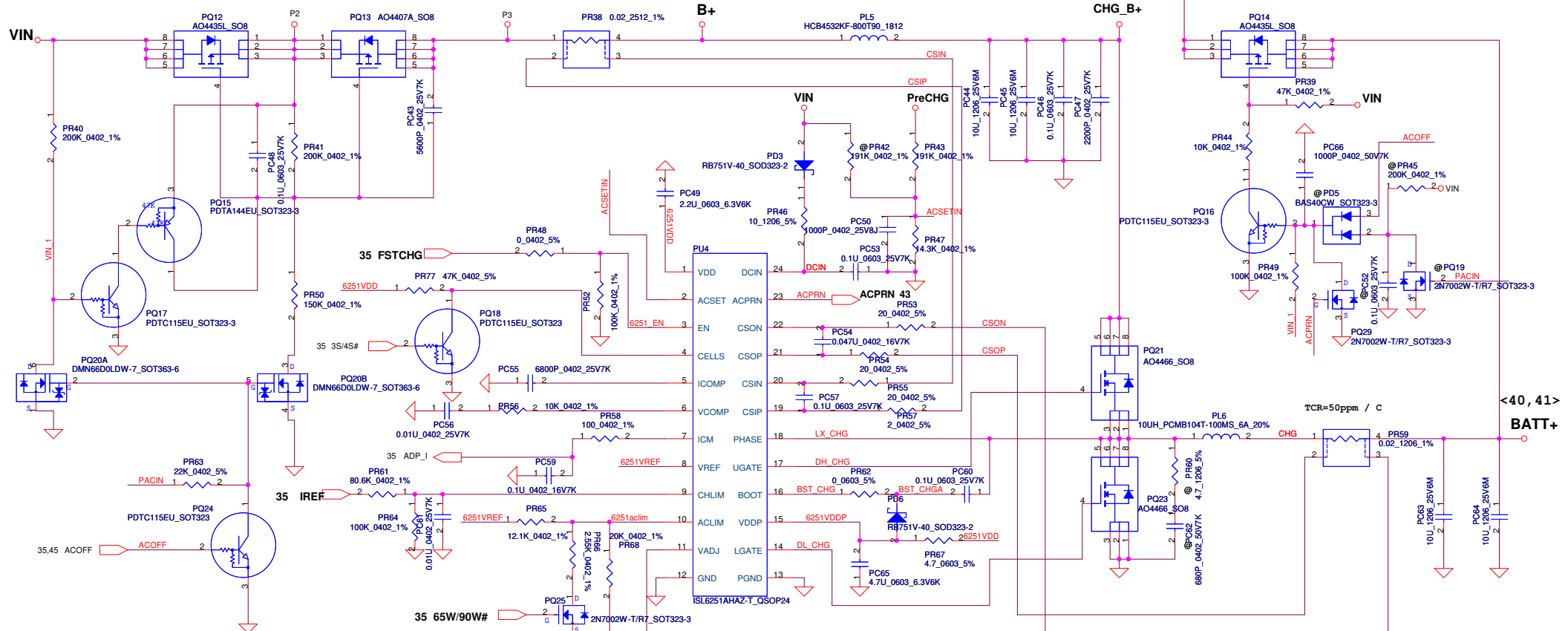


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Iada=0~4.74A (90W/19V=4.736A)
 Iada=0~3.42A (90W/19V=3.421A)

ADP_I = 19.9*Iadapter*Rsense

CP = 85%*Iada ; CP = 4.07A
 CP = 85%*Iada ; CP = 2.91A



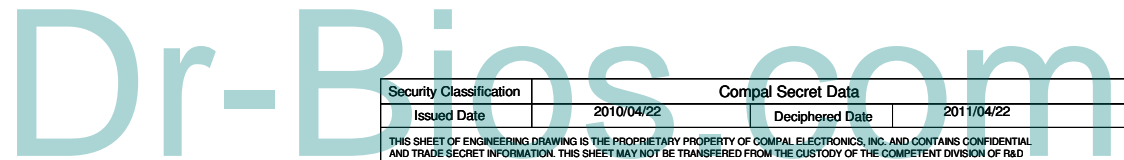
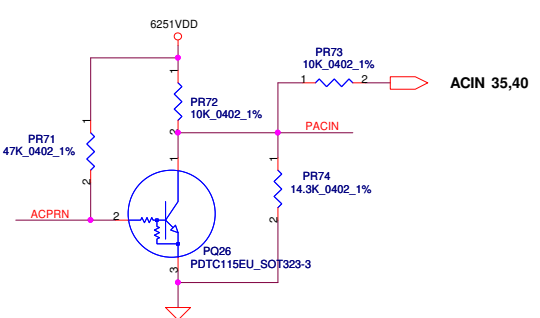
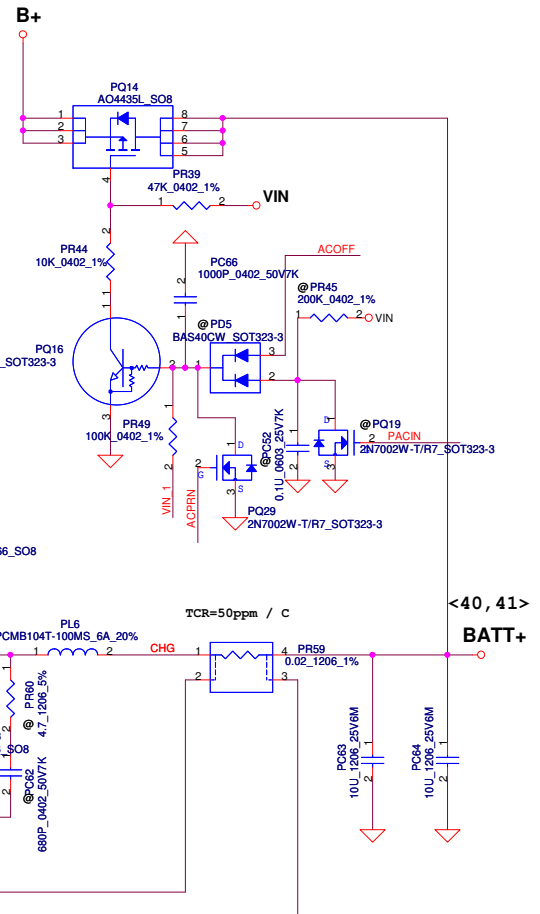
CP mode
 $I_{input} = (1/0.02) (0.05 * V_{ac1m} / 2.39 + 0.05)$
 where $V_{ac1m} = 1.502V$, $I_{input} = 4.07A$

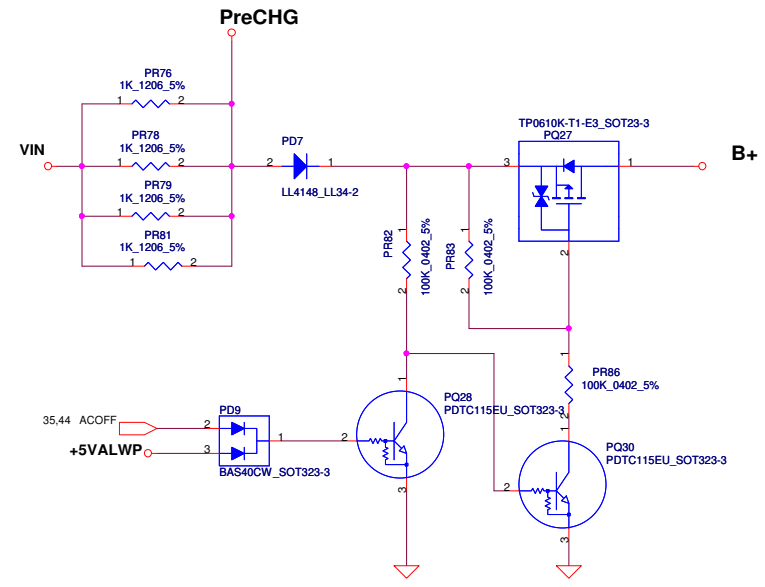
CC=0.6~4.48A
 $I_{REF} = 0.7224 * I_{charge}$
 $K_i = 0.7224$
 $I_{REF} = 0.43V \sim 3.24V$

K_i
 $V_{ch1m} = I_{ref} * (PR374 / (PR372 + PR374))$
 $= I_{ref} * (100K / (80.6K + 100K))$
 $= I_{ref} * 0.5537$
 $I_{charge} = (165mV / PR369) * (V_{ch1m} / 3.3V)$
 $= (165m / 20m) * (1/3.3V) * I_{ref} * 0.5537$
 $= 1.3842 * I_{ref}$
 $I_{ref} = 0.7224 * I_{charge} \Rightarrow K_i = 0.7224$

K_v
 $R_{internal} = 514K$ Rec=3K $R_1 = PR379 = 15.4K$ $R_2 = PR381 = 31.6K$
 $R = 514K // 31.6K // (15.4K + 3K) = 11.372K$
 $r = 514K // 514K // 31.6K = 28.14K$
 $V_{oc1} = 0.175 * V_{adj} + 3.99V$
 $4.2V = 0.175 * V_{adj} + 3.99V \Rightarrow V_{adj} = 1.2V$
 $V_{adj} = V_{ref} * (R / (R + 514K)) + CALIBRATE * (r / (r + 514K))$
 $1.1483 = CALIBRATE * 0.6046 \Rightarrow CALIBRATE = 1.899$
 $1.899 = (4.2 - (V_{oc1} + 0.175)) * R_v \Rightarrow R_v = (4.2 - 4.2 + 0.175) * R_v$
 $A = V_{ref} * (R / (R + 514K)) = 0.052$
 $R_v = 9.451$

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V





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VFB=0.75V
 $V_o = VFB * (1 + PR97 / PR98) = 0.75 * (1 + 5.9K / 5.76K) = 1.518V$
 $Fsw = 282KHz$

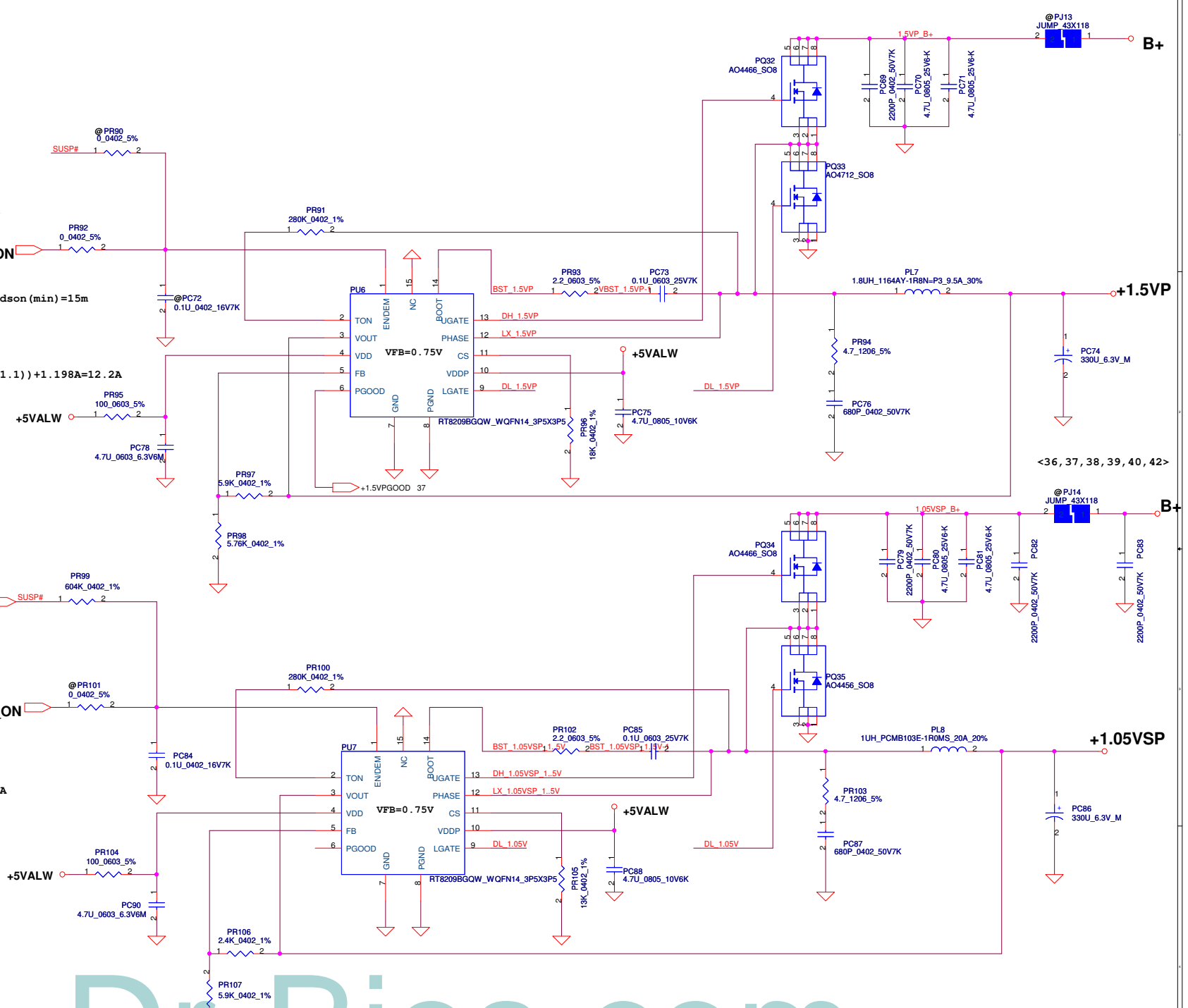
<Vo=1.5V> VFB=0.75V
 $V_o = VFB * (1 + PR116 / PR117) = 0.75 * (1 + 10K / 10K) = 1.5V$
 $Fsw = 262KHz$ Cout ESR=15m ohm Rds(on)=18m Rds(on)(min)=15m
 $I_{peak} = 11.3A$, $1.2I_{peak} = 13.56A$, $I_{max} = 7.91A$
 $\Delta I = ((19 - 1.5) * (1.5 / 19)) / (L * Fsw) = 2.3969A$
 $\Rightarrow 1/2 \Delta I = 1.198A$
 $V_{trip} = R_{trip} * I_{0uA} = 18K * 10uA = 0.18V$
 $I_{ocpmin} = V_{trip} / R_{ds(on)(max)} * 1.2 + 1.198$
 $= 0.18 / (0.018 * 1.3) + 1.198 = 9A$
 $I_{ocpmax} = (0.18 / (0.015 * 1.1)) + 1.198A = 12.2A$
 $I_{ocp} = 9 \sim 12.2A$

VFB=0.75V
 $V_o = VFB * (1 + PR108 / PR109) = 0.75 * (1 + 12K / 30K) = 1.05V$
 $T_{on} = 19 * e^{-12 * 143000} * ((2/3) * V_o + 100mV) / 19 + 50ns$
 $= 2.645e-7$ us
 $\Rightarrow V_o / V_{in} = D = T_{on} / T_s \Rightarrow T_s = 3.35us$
 $Fsw = 261KHz$ (by calculation tool)

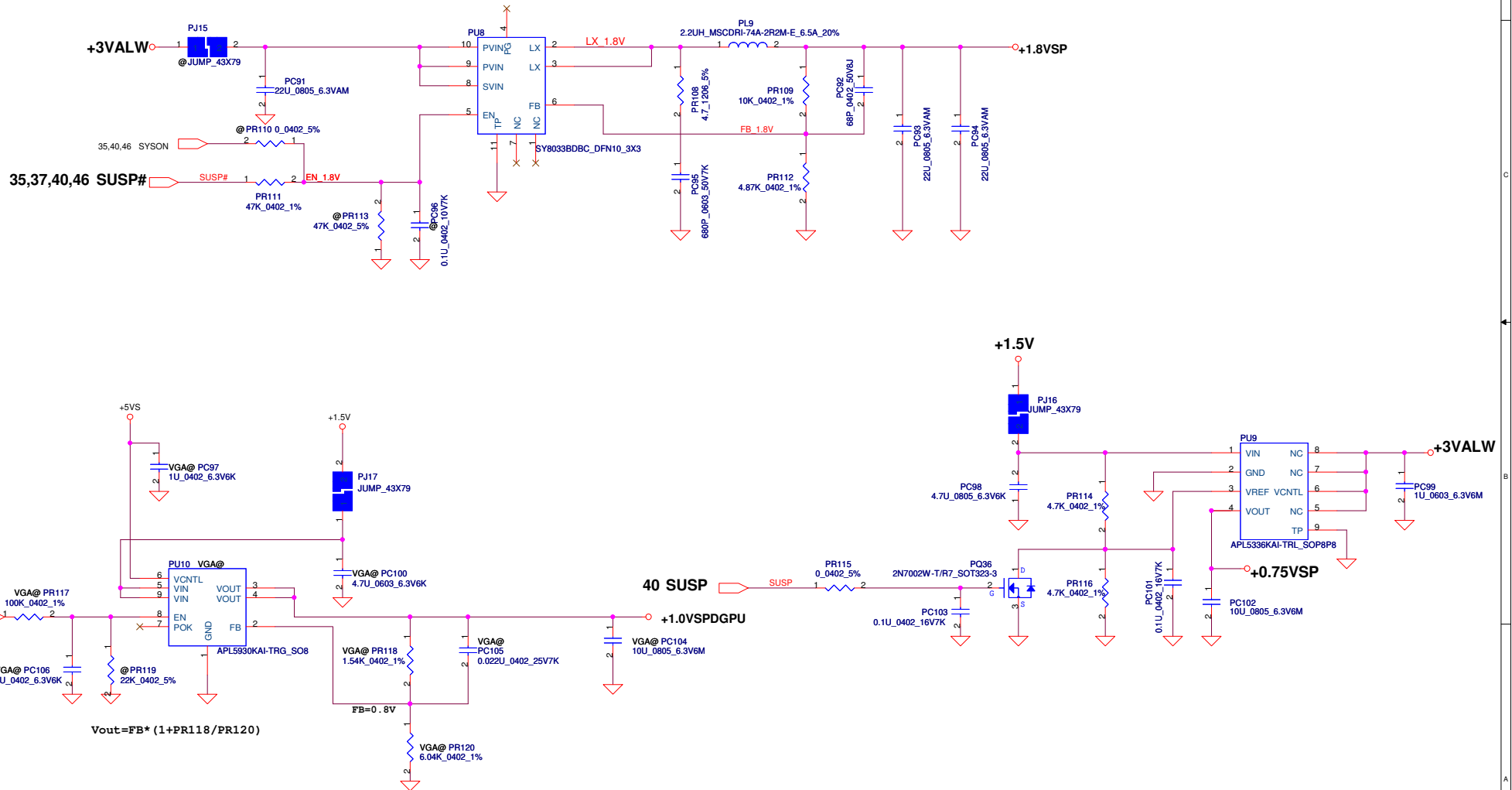
<Vo=1.05V> VFB=0.75V
 $V_o = VFB * (1 + PR108 / PR109) = 0.75 * (1 + 12K / 30K) = 1.05V$
 $Fsw = 261KHz$ Cout ESR=15m ohm Rds(on)(max.)=5.6m Rds(on)(min)=4.5m
 $I_{peak} = 14.9A$, $I_{max} = I_{peak} * 0.7 = 10.43A$ $I_{ocp} = 17.88A$
 $\Delta I = ((19 - 1.05) * (1.05 / 19)) / (L * Fsw) = 2.11A$
 $\Rightarrow 1/2 \Delta I = 1.055A$
 $V_{trip} = R_{trip} * I_{0uA} = 13K * 10uA = 0.13V$
 $I_{ocpmin} = V_{trip} / R_{ds(on)(max)} * 1.3 + 1.055$
 $= 0.13 / (0.056 * 1.3) + 1.055 = 18.95A$
 $I_{ocpmax} = (0.13 / (0.0045 * 1.1)) + 1.055A = 27.36A$
 $I_{ocp} = 18.95A \sim 27.36A$

35,40,47 SYSON

35,37,40,47 SUSP#

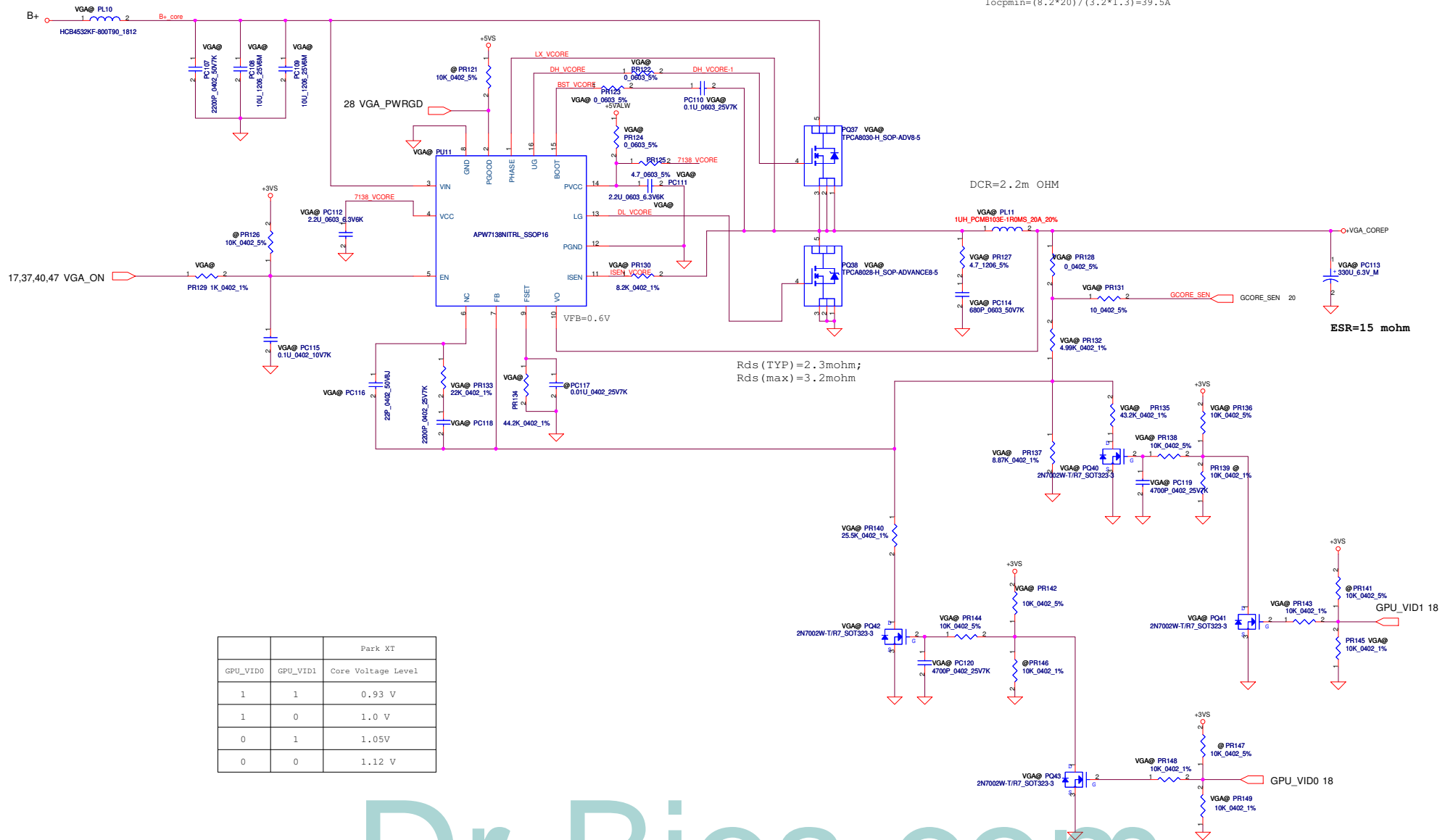


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VGA_CORE
 $F=1/(75\mu s-12*44.2)=300K$
 $I_{peak}=33A$ $I_{max}=23.1A$ $I_{ocp}=39.6A$
 $R_{senmax}=(3.2*1.3*35)/20=8.112$ Kohm choose
 $R_{sen}=8.2$ Kohm
 $I_{ocpmin}=(8.2*20)/(3.2*1.3)=39.5A$



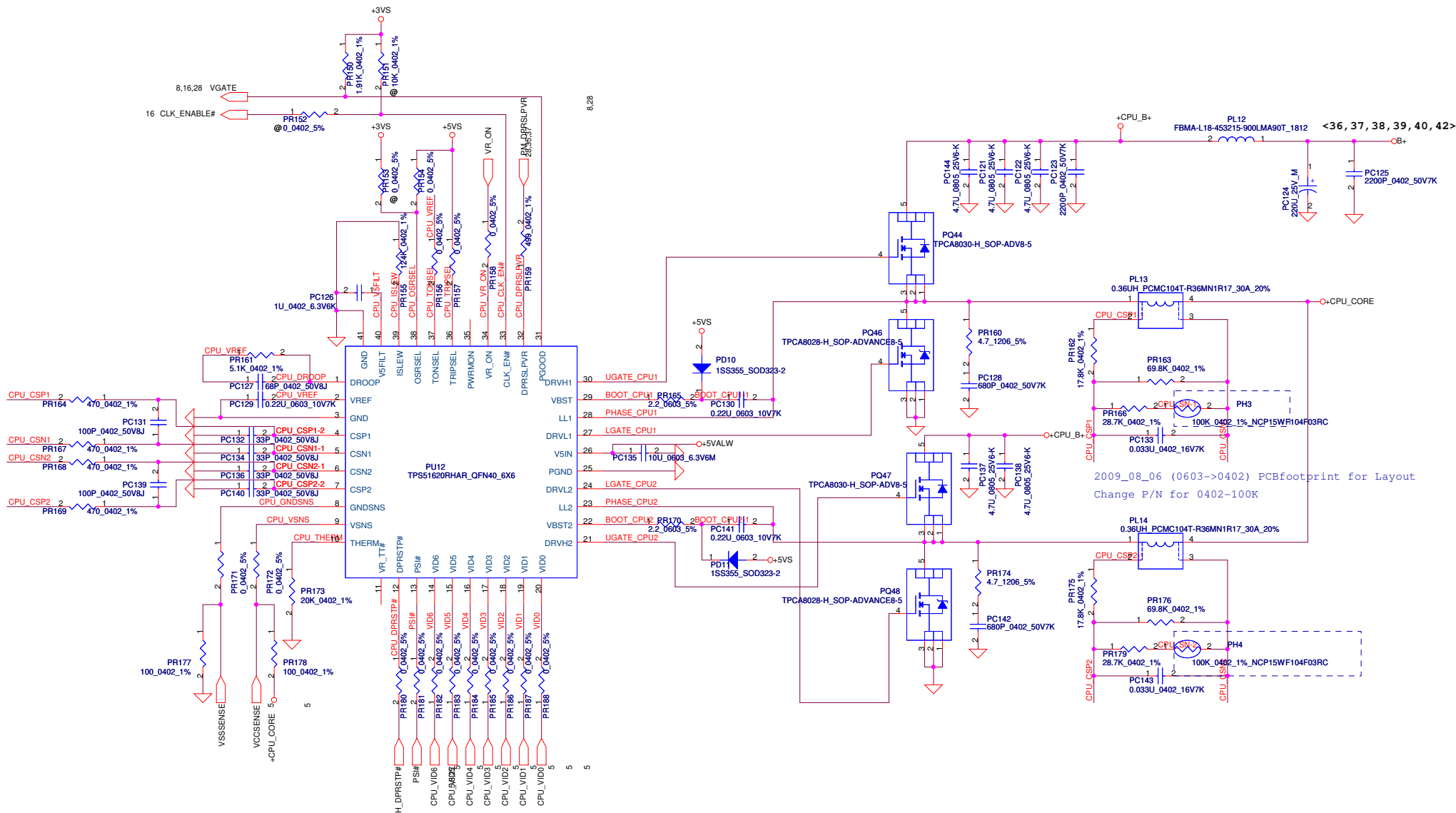
$R_{ds(TYP)} = 2.3\text{mohm}$;
 $R_{ds(max)} = 3.2\text{mohm}$

DCR = 2.2m OHM

ESR = 15 mohm

GPU_VID0	GPU_VID1	Core Voltage Level
1	1	0.93 V
1	0	1.0 V
0	1	1.05V
0	0	1.12 V





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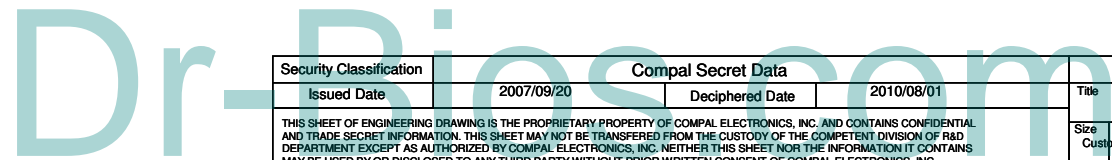
Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Change HW Enable sequency	HW sequency request	1	45	1.PR129---->1K 2.PR111---->47K 3.PR117---100K 4.PR99---604K	2009/08/25	PVT
3	regulate 5V voltage	HW request	1	45	PR24--->30.9K		
4							
5							
6							
7							
8							
9							
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A -->Modify item

- Page8: Add pull-low 0 ohm on CLK_DREF_96M, CLK_DREF_96M#
Add pull-low 0 ohm on CLK_DREF_SSC ,CLK_DREF_SSC#
- Page11: Add Jump to split out +VGFX_CORE from +1.05VS
Add 0 ohm to discharge VCC GFX on C127
- Page17: Add R584 to connect +3VS & +3SDGPU
Change R102 Bomstructure to DIS@
- Page23: Add R582 to pull-low ENVDD
stuff R341, add C473
- Page25: Change R51 R52 to UMA@
Stuff R486 for FAE request
- Page26: R196 change to DIS@
U13 & R215 R217 change to @
- Page37: Add R581
- Page40: Add J13 Jump



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