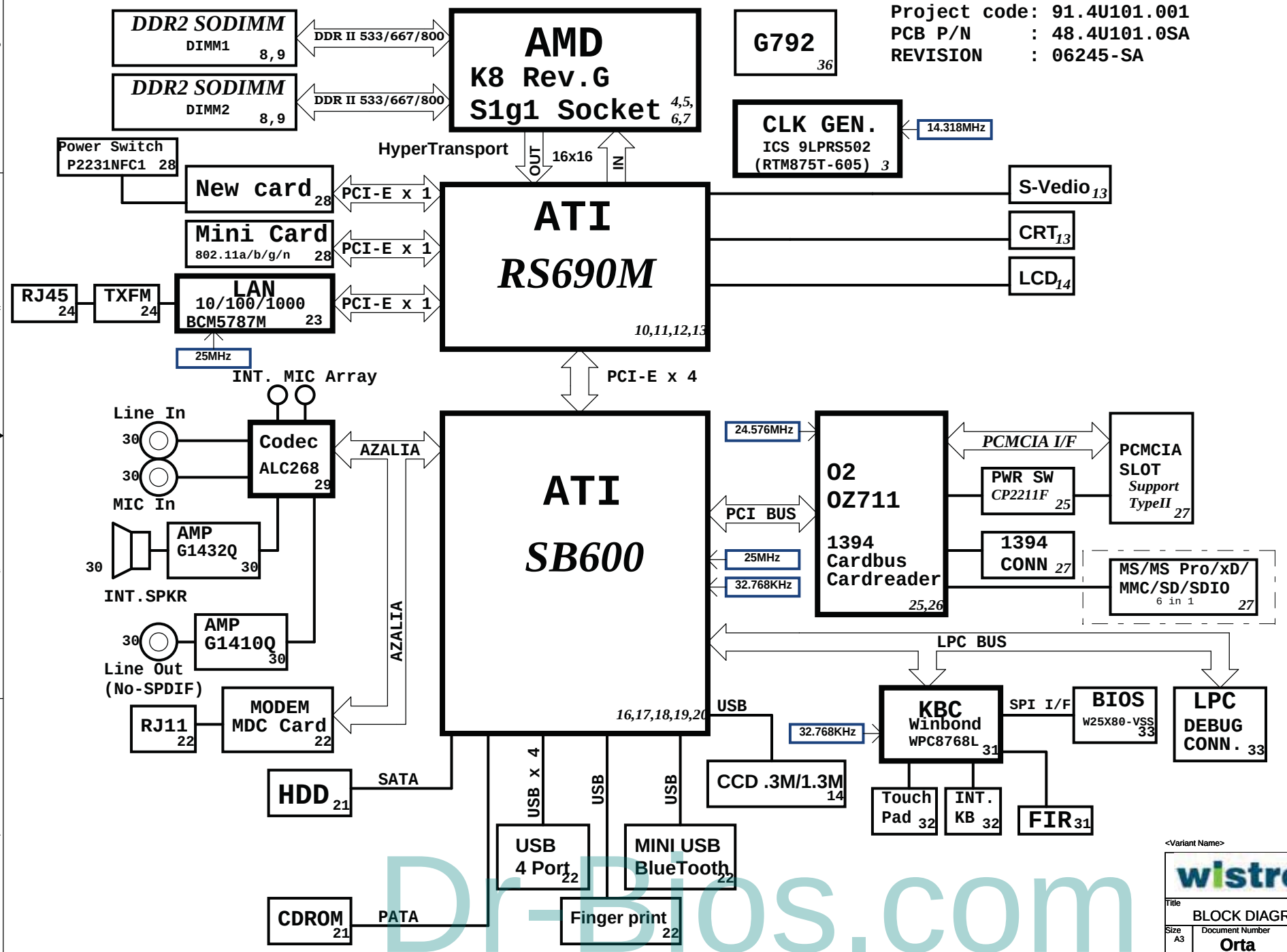
Orta Block Diagram



PCB Layer Stackup

L1: Signal 1
L2: VCC
L3: Inner Signal 2
L4: Inner Signal 3
L5: GND
L6: Signal 4

CPU V_CORE

INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	1D2V_S0 1D8V_S3

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	5V_S5 3D3V_S5

SYSTEM LDO

INPUT	OUTPUT
1D8V_S3	0D9V_S3

SYSTEM LDO

INPUT	OUTPUT
3D3V_S5 3D3V_S0 3D3V_S0	1D2V_S5 2D5V_S0 1D5V_S0

SYSTEM LDO

INPUT	OUTPUT
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

Battery Charger

INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: BLOCK DIAGRAM

Size: A3 | Document Number: Orta | Rev: SA

Date: Tuesday, December 12, 2006 | Sheet 1 of 46

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SA: 07/31/06 Start

SB change
power team
1.change L7, L9 to 68.1R510.10D
2.changge U12 to 84.04706.037
3.change R66 to 10K ohm

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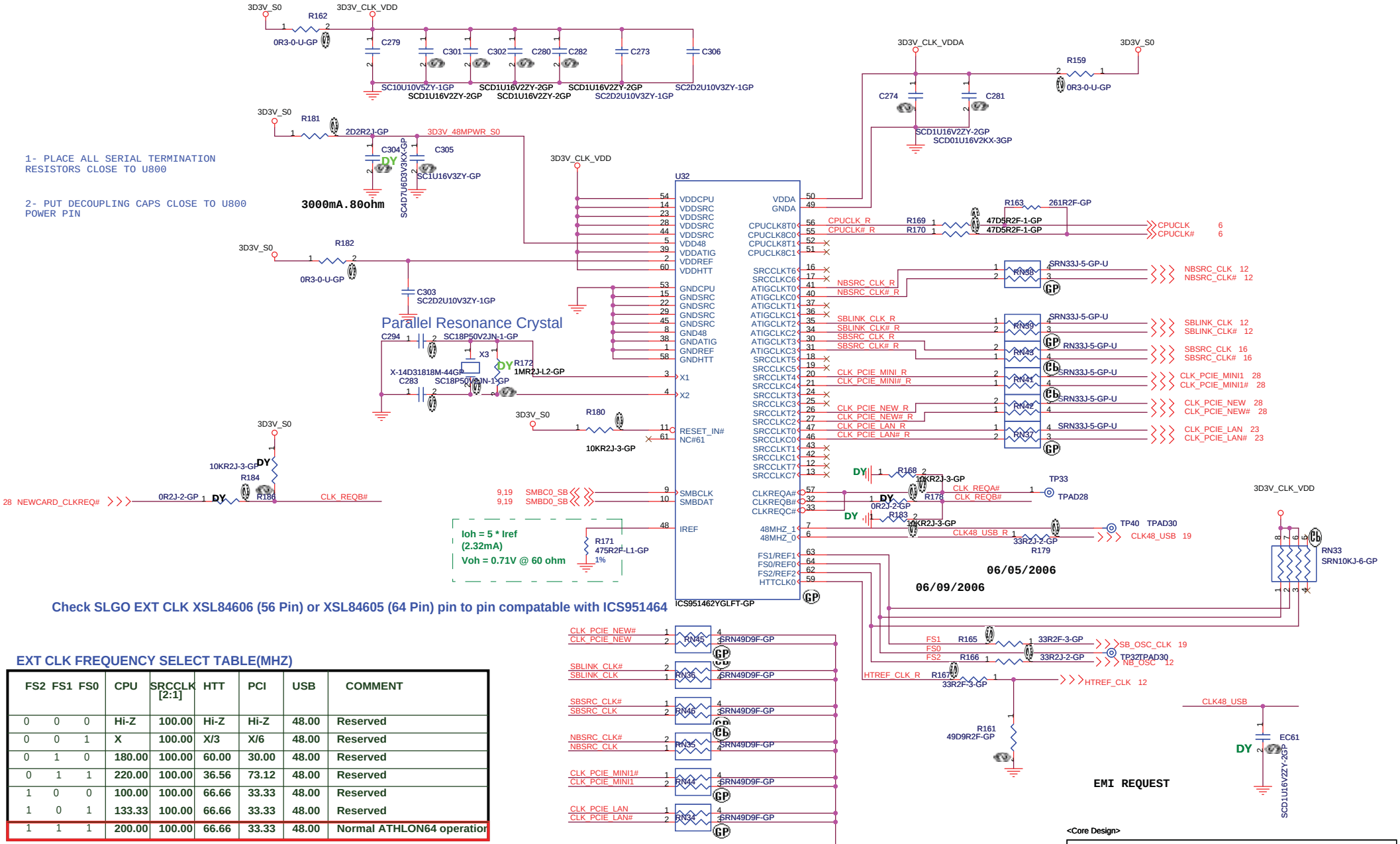
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHANGE HISTORY

Size	Document Number	Rev
A3	Orta	SA

Date: Tuesday, December 12, 2006 Sheet 2 of 46



Check SLGO EXT CLK XSL84606 (56 Pin) or XSL84605 (64 Pin) pin to pin compatable with ICS951464

EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation

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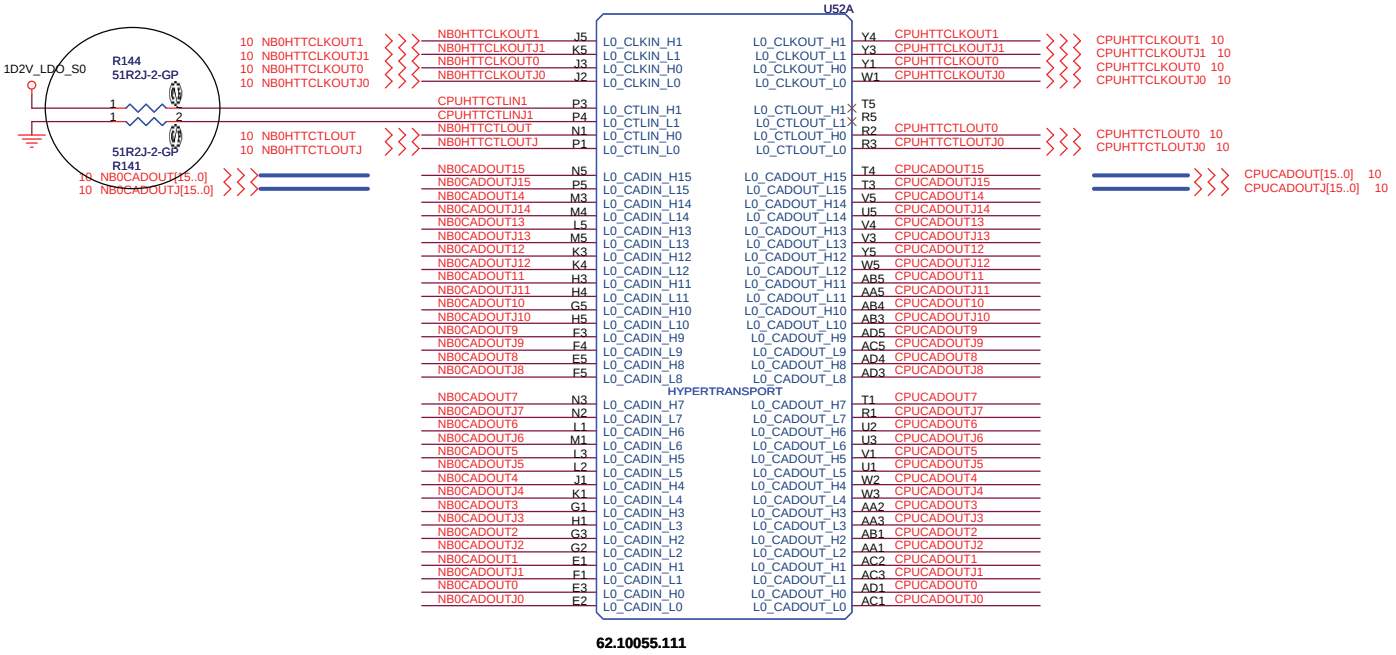
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CLKGEN_ICS951412

Size: A3 | Document Number: Orta | Rev: SA

Date: Tuesday, December 12, 2006 | Sheet 3 of 46



62.10055.111

<Core Design>

緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU(1/4)_HyperTransport I/F***

Size	Document Number	Rev
A3	Orta	SA

Date: Tuesday, December 12, 2006 Sheet 4 of 46

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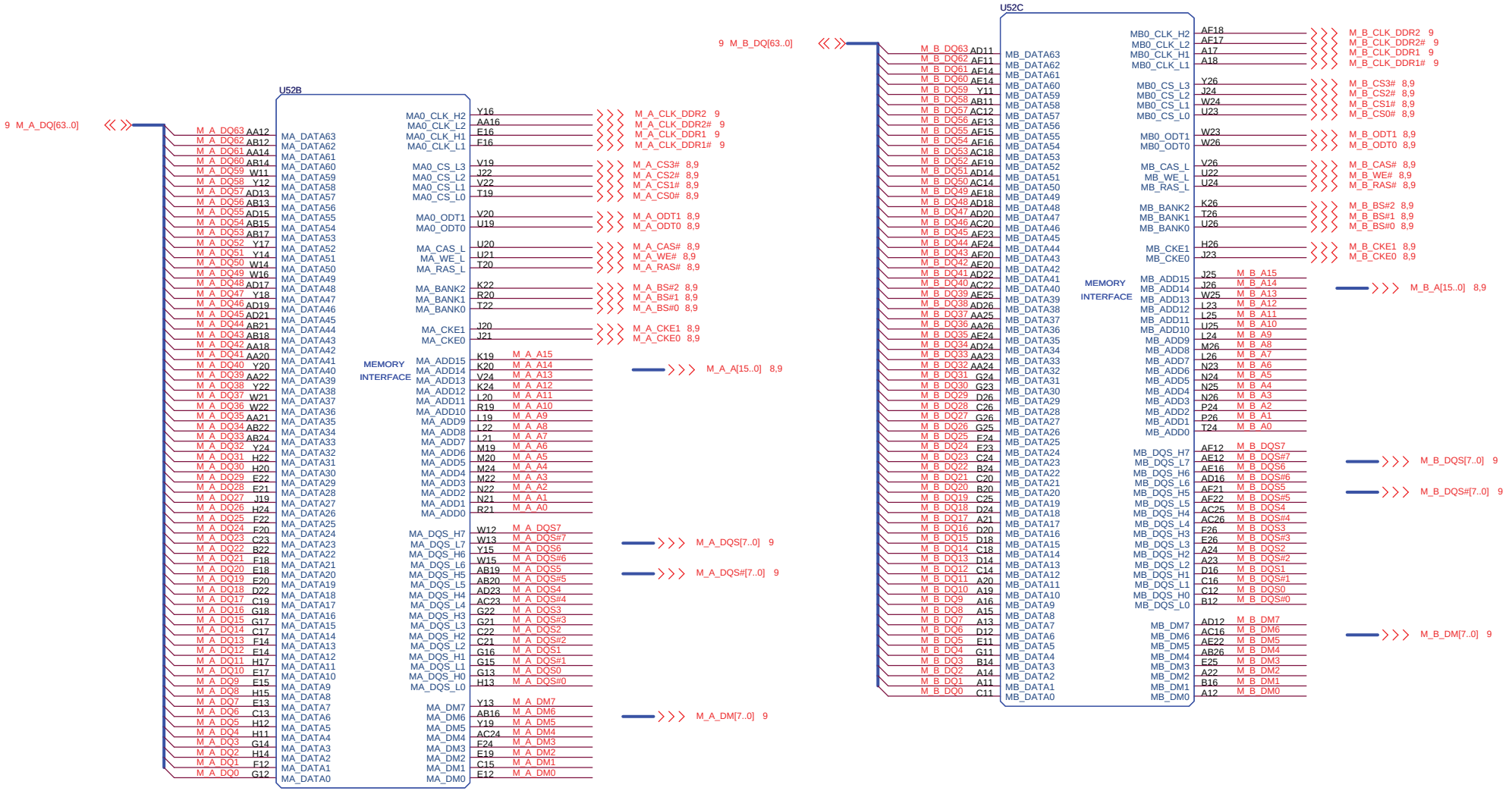

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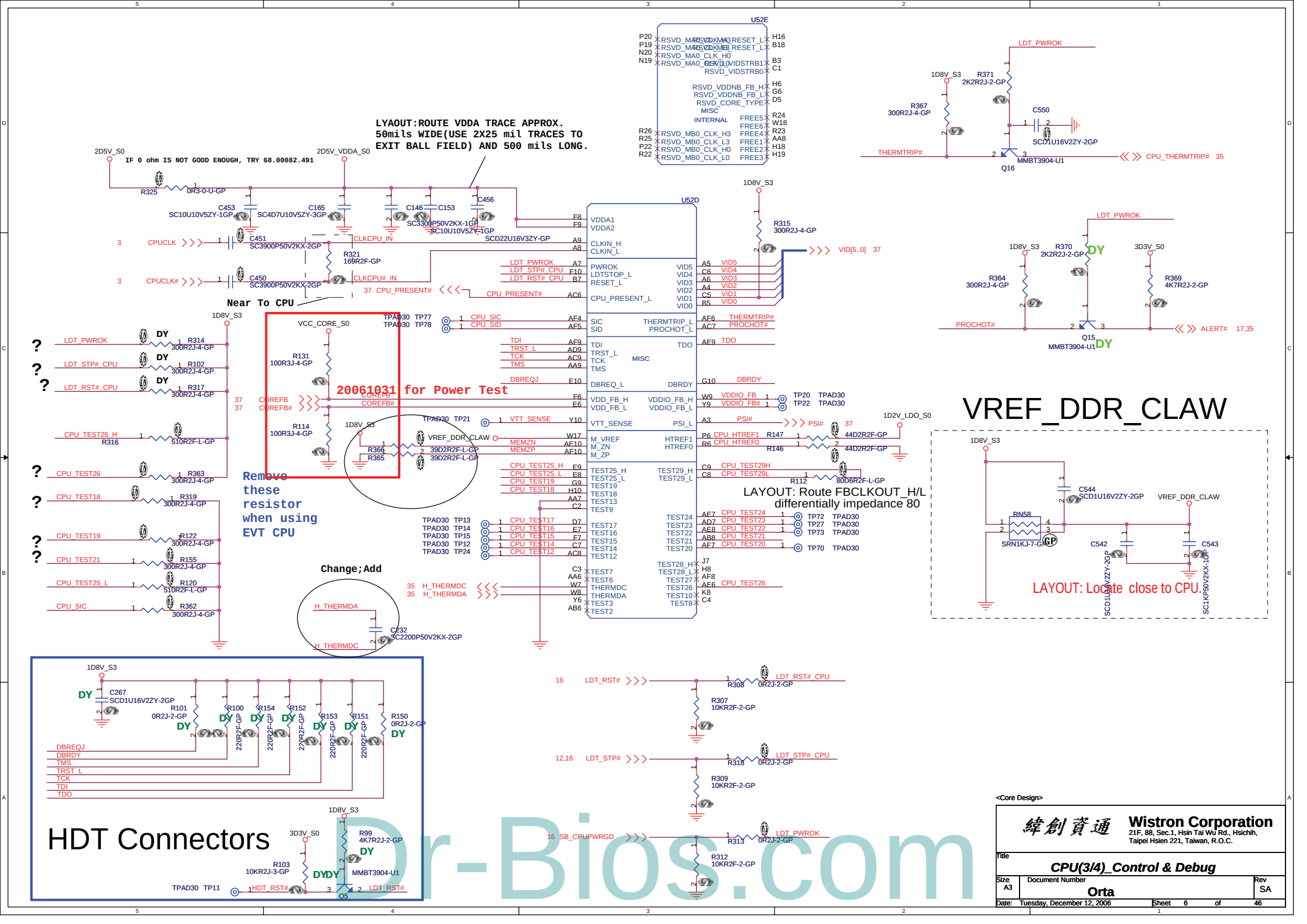
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(2/4)_DDR

Size: A3 | Document Number: Orta | Rev: SA

Date: Tuesday, December 12, 2006 | Sheet 5 of 46



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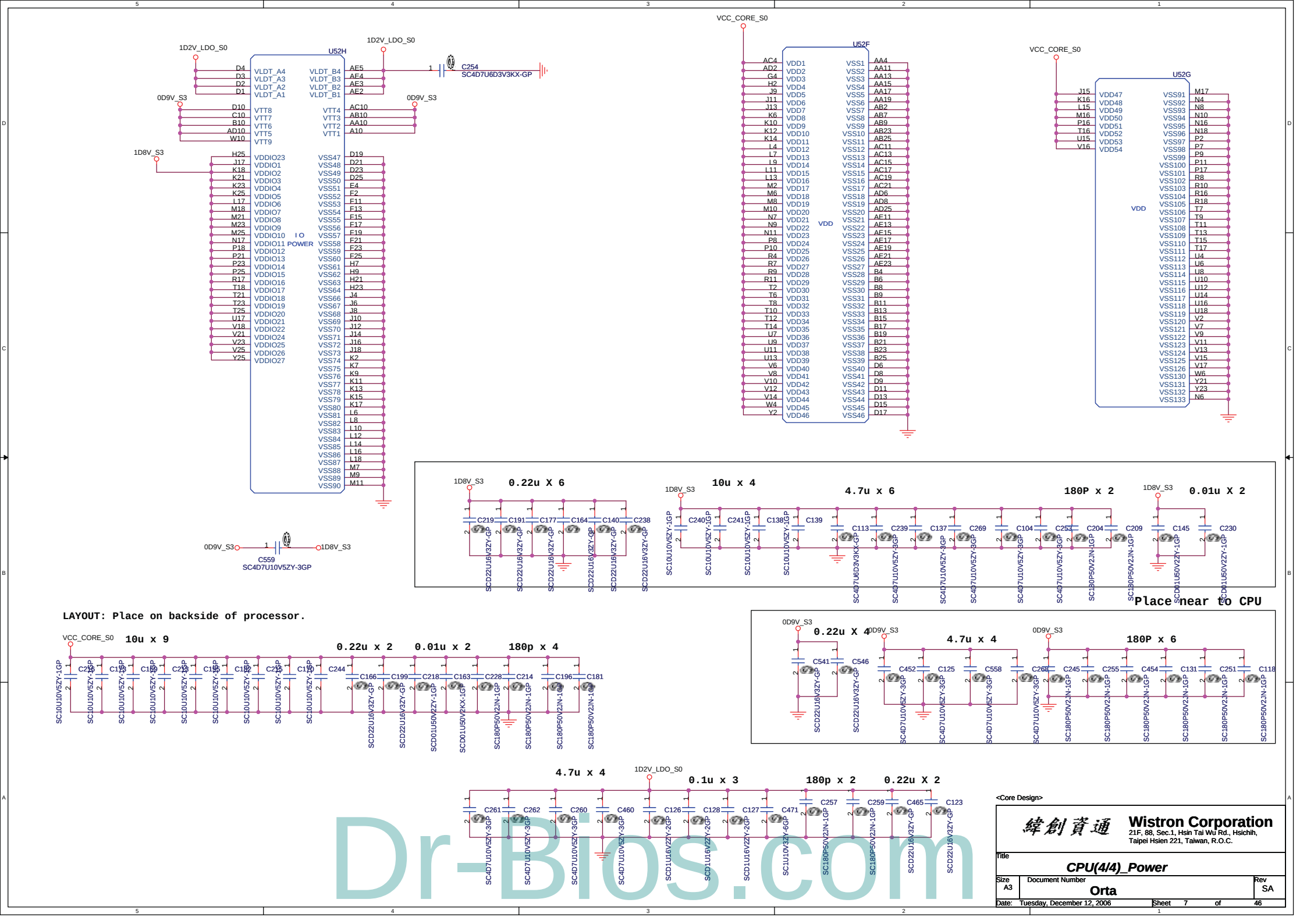
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(3/4)_Control & Debug
Size: A3 | Document Number: Orta | Rev: SA
Date: Tuesday, December 12, 2006 | Sheet 6 of 46


U52H
1D2V_LDO_S0
0D9V_S3
1D8V_S3
VLDT_A4
VLDT_A3
VLDT_A2
VLDT_A1
VLDT_B4
VLDT_B3
VLDT_B2
VLDT_B1
VTT8
VTT7
VTT6
VTT5
VTT9
VTT4
VTT3
VTT2
VTT1
VDDIO23
VDDIO1
VDDIO2
VDDIO3
VDDIO4
VDDIO5
VDDIO6
VDDIO7
VDDIO8
VDDIO9
VDDIO10
VDDIO11
VDDIO12
VDDIO13
VDDIO14
VDDIO15
VDDIO16
VDDIO17
VDDIO18
VDDIO19
VDDIO20
VDDIO21
VDDIO22
VDDIO24
VDDIO25
VDDIO26
VDDIO27
I O
POWER
VSS47
VSS48
VSS49
VSS50
VSS51
VSS52
VSS53
VSS54
VSS55
VSS56
VSS57
VSS58
VSS59
VSS60
VSS61
VSS62
VSS63
VSS64
VSS66
VSS67
VSS68
VSS69
VSS70
VSS71
VSS72
VSS73
VSS74
VSS75
VSS76
VSS77
VSS78
VSS79
VSS80
VSS81
VSS82
VSS83
VSS84
VSS85
VSS86
VSS87
VSS88
VSS89
VSS90
C254
SC4D7U6D3V3KX-GP
C559
SC4D7U10V5ZY-3GP
U52F
VCC_CORE_S0
VDD
VSS
U52G
VDD47
VDD48
VDD49
VDD50
VDD51
VDD52
VDD53
VDD54
VSS91
VSS92
VSS93
VSS94
VSS95
VSS96
VSS97
VSS98
VSS99
VSS100
VSS101
VSS102
VSS103
VSS104
VSS105
VSS106
VSS107
VSS108
VSS109
VSS110
VSS111
VSS112
VSS113
VSS114
VSS115
VSS116
VSS117
VSS118
VSS119
VSS120
VSS121
VSS122
VSS123
VSS124
VSS125
VSS126
VSS130
VSS131
VSS132
VSS133
0.22u X 6
10u x 4
4.7u x 6
180P x 2
0.01u X 2
Place near to CPU
LAYOUT: Place on backside of processor.
10u x 9
0.22u x 2
0.01u x 2
180p x 4
0.22u X 4
4.7u x 4
180P x 6
4.7u x 4
0.1u x 3
180p x 2
0.22u X 2
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU(4/4)_Power
Size
A3
Document Number
Orta
Rev
SA
Date: Tuesday, December 12, 2006
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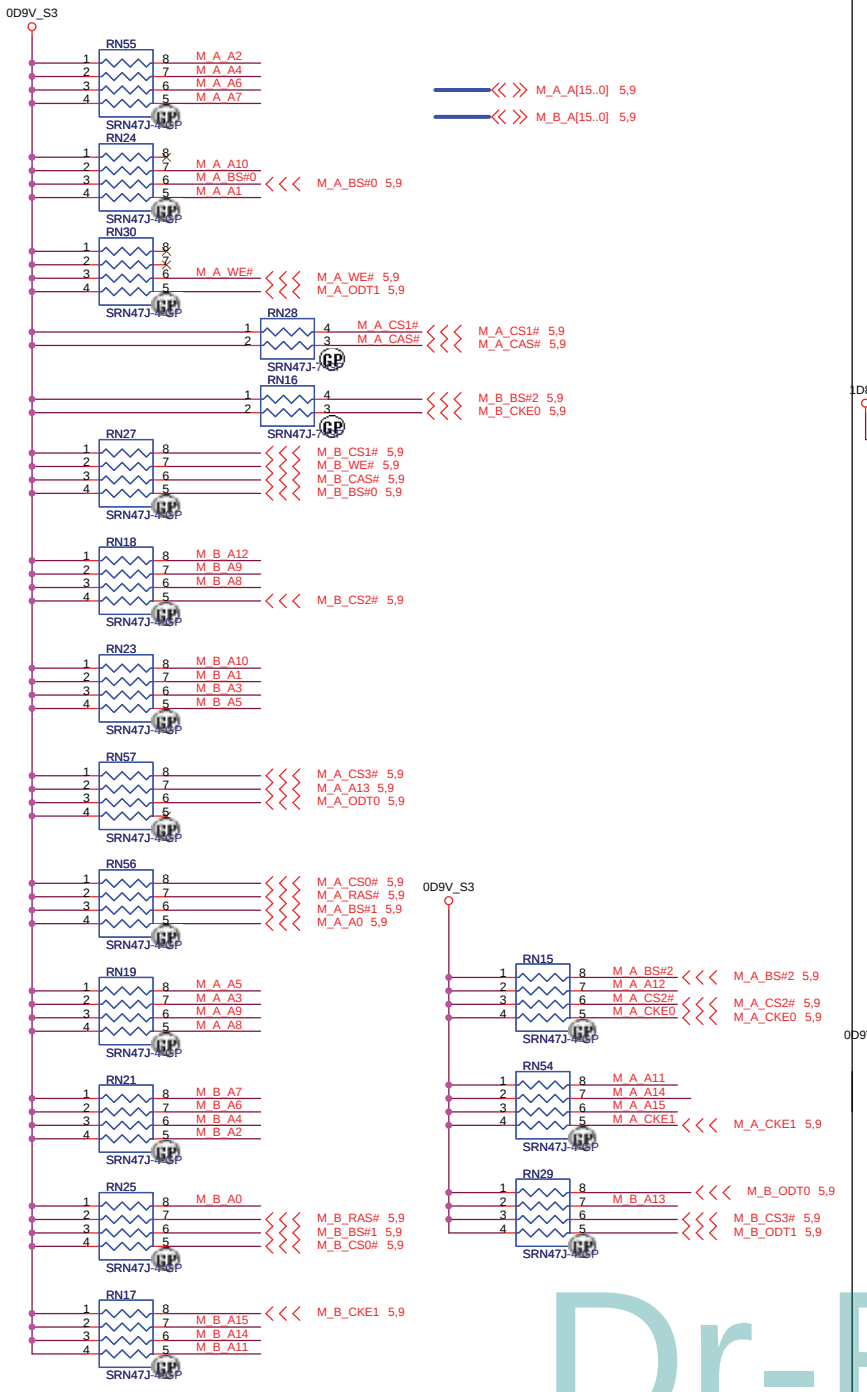
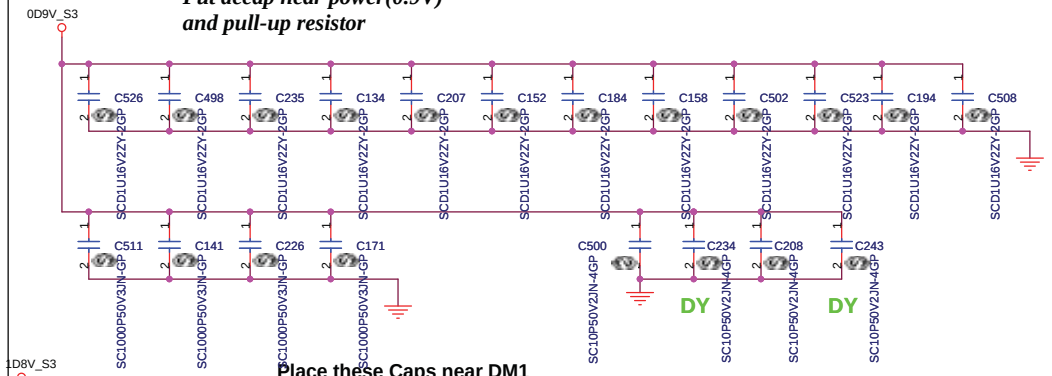
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

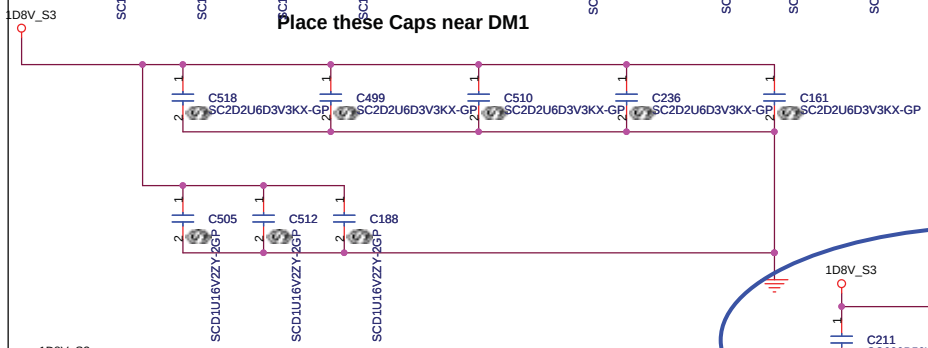


Decoupling Capacitor

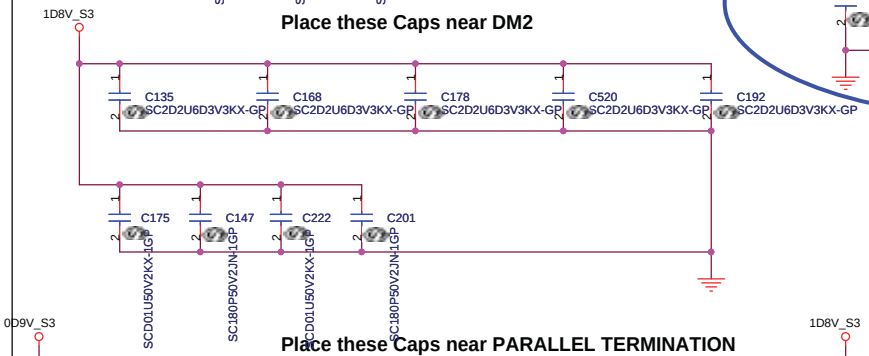
Put decap near power(0.9V) and pull-up resistor



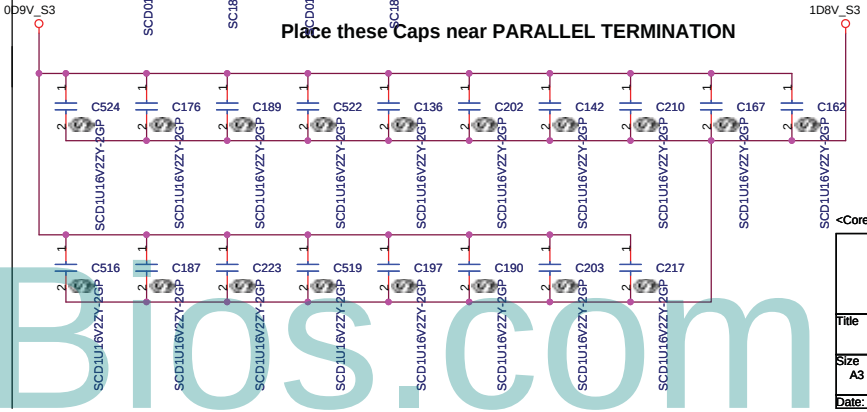
Place these Caps near DM1

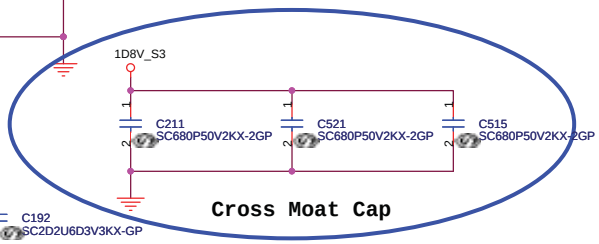


Place these Caps near DM2



Place these Caps near PARALLEL TERMINATION





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR DAMPING & TERMINATION

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A3	Orta	SA

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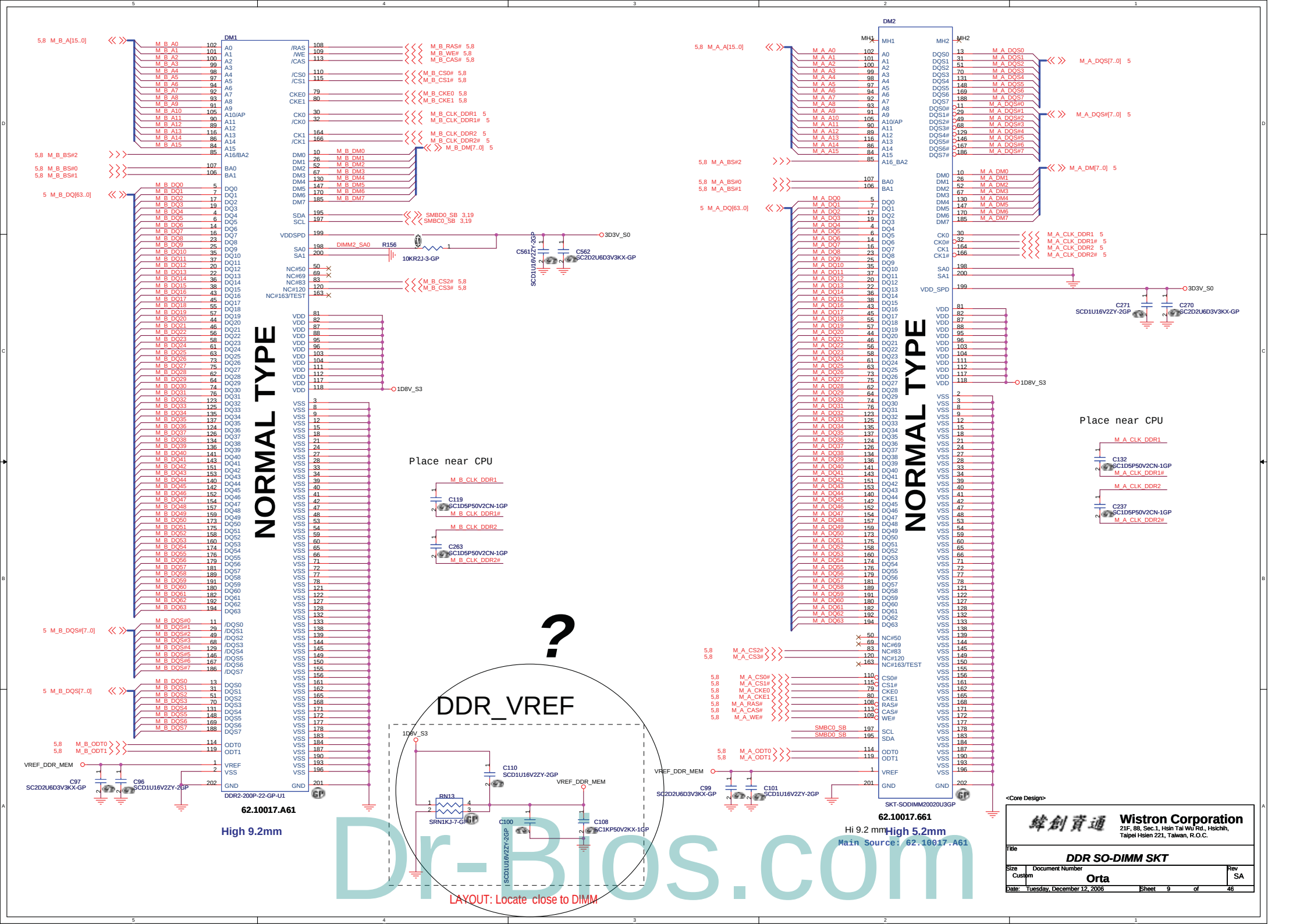
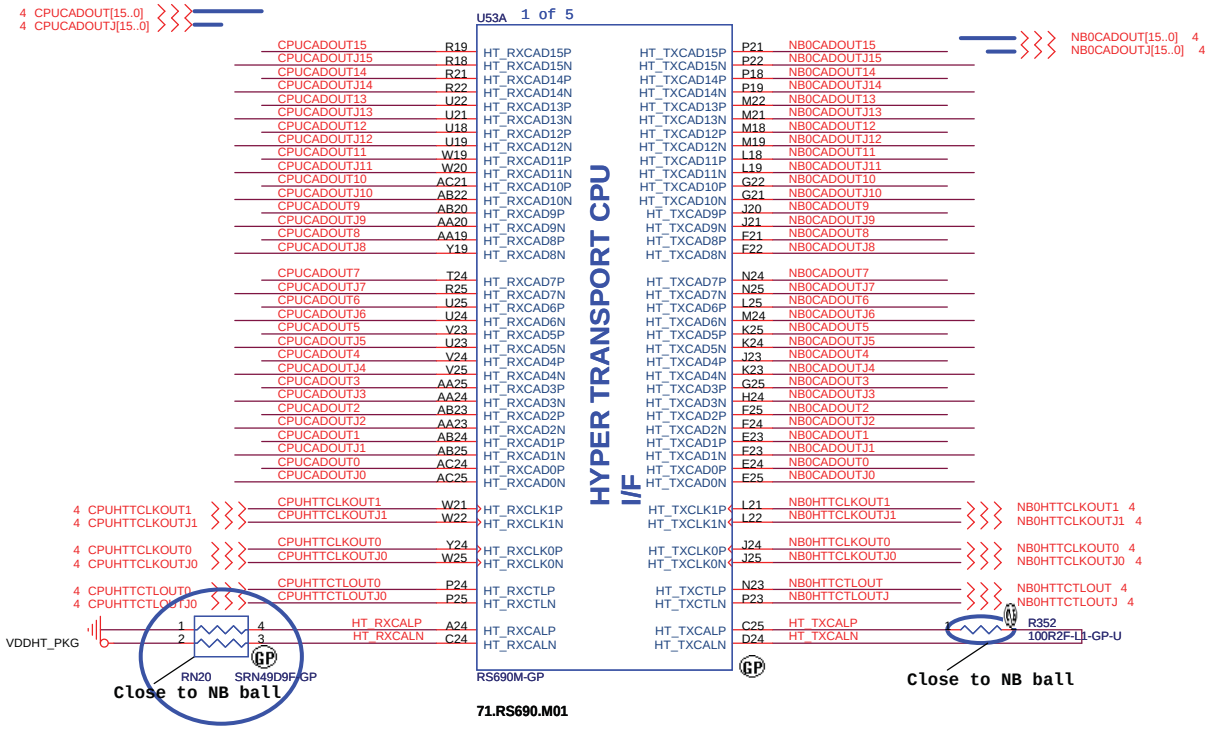

DM1
NORMAL TYPE
DDR2-200P-22-GP-U1
62.10017.A61
High 9.2mm
DM2
NORMAL TYPE
SKT-SODIMM20020U3GP
62.10017.661
Hi 9.2 mm
High 5.2mm
Main Source: 62.10017.A61
Place near CPU
Place near CPU
DDR_VREF
LAYOUT: Locate close to DIMM
Dr-Bios.com
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DDR SO-DIMM SKT
Orta
Tuesday, December 12, 2006

CLAW HAMMER TO NB

NB TO CLAW HAMMER



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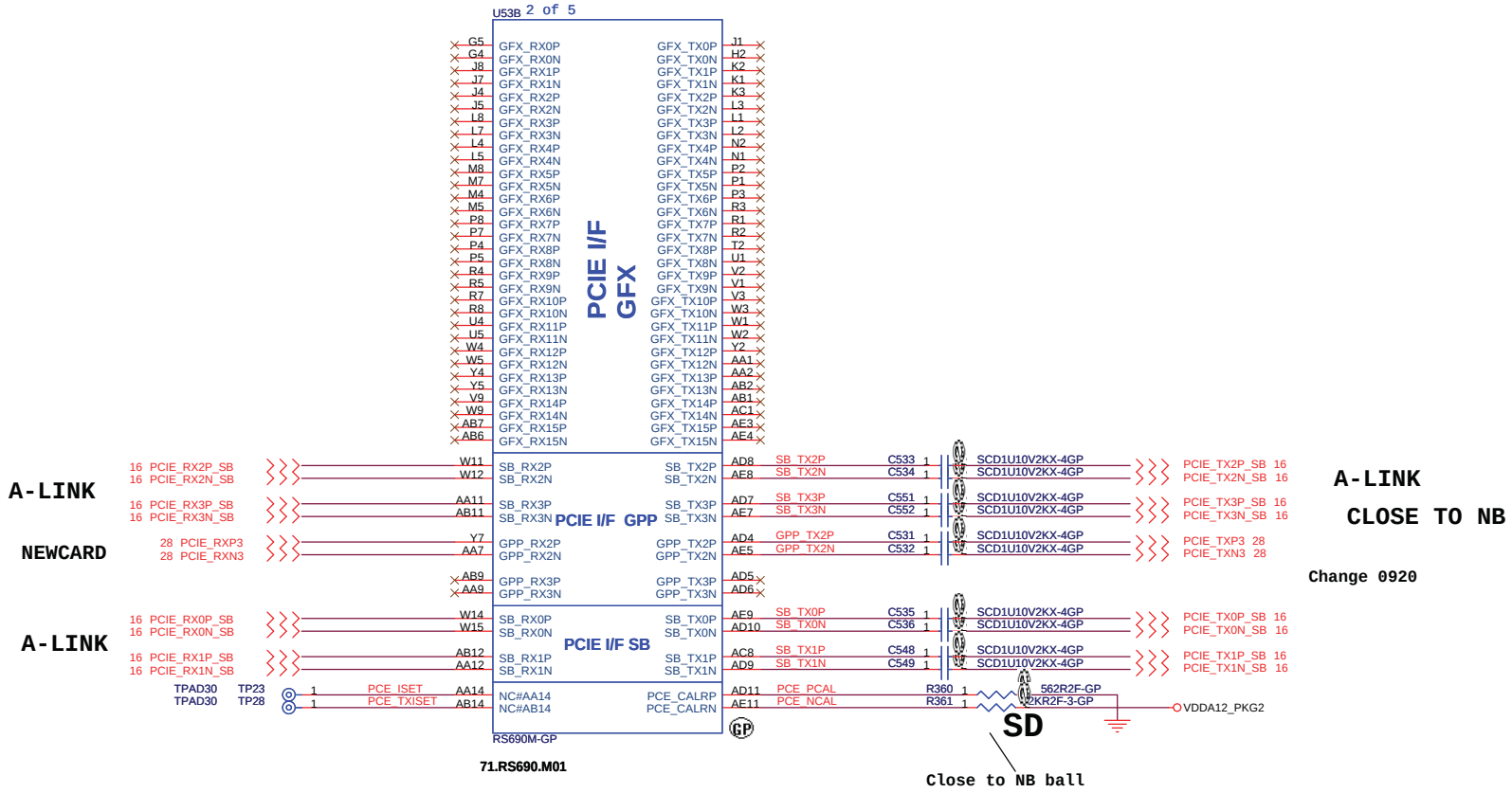
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NB-RS690M_HT

Size: A3 | Document Number: Orta | Rev: SA

Date: Tuesday, December 12, 2006 | Sheet 10 of 46



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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NB-RS690M_MEM/PCIE_LINK I/F

Size: A3 | Document Number: Orta | Rev: SA

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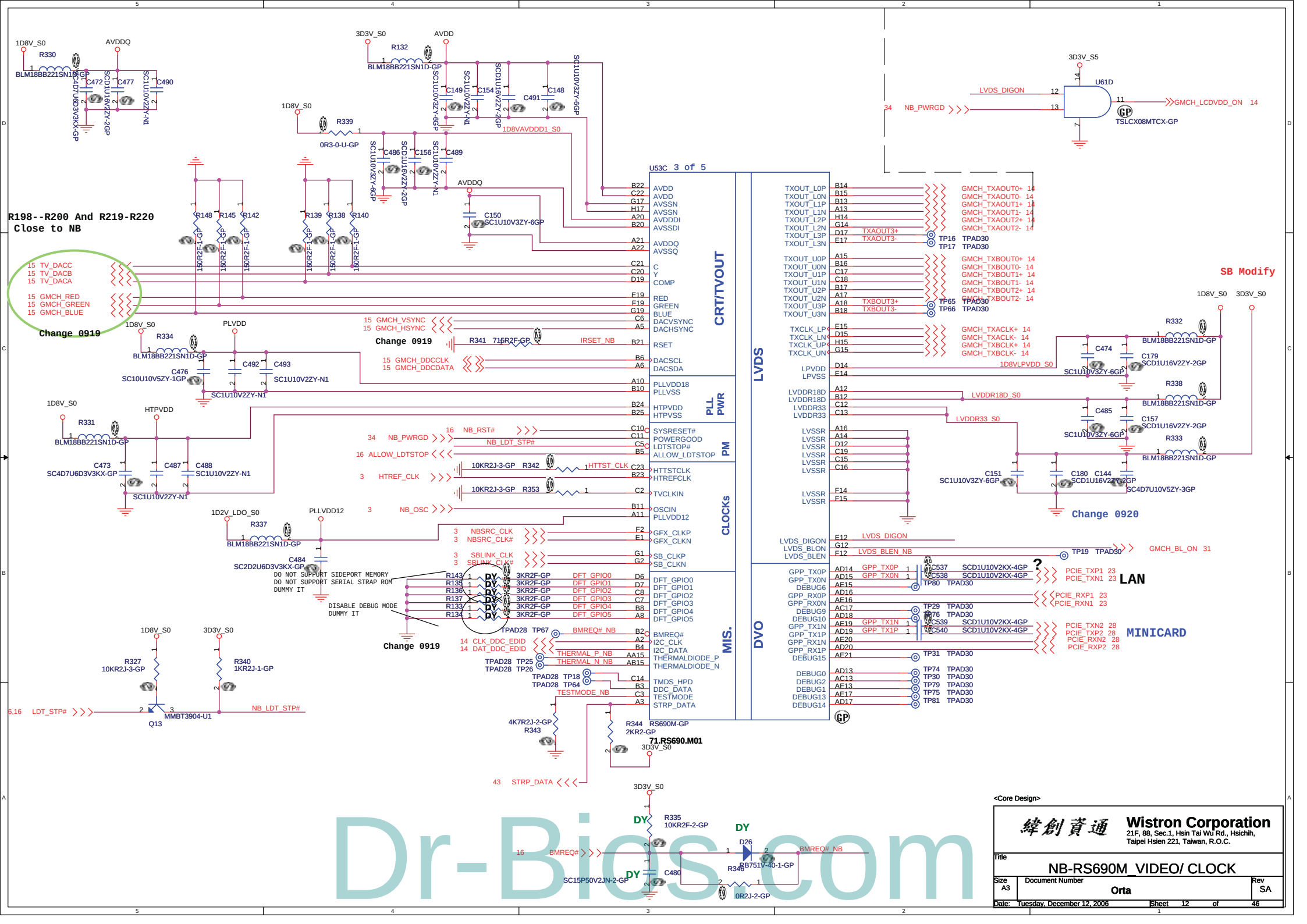

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NB-RS690M_VIDEO/ CLOCK

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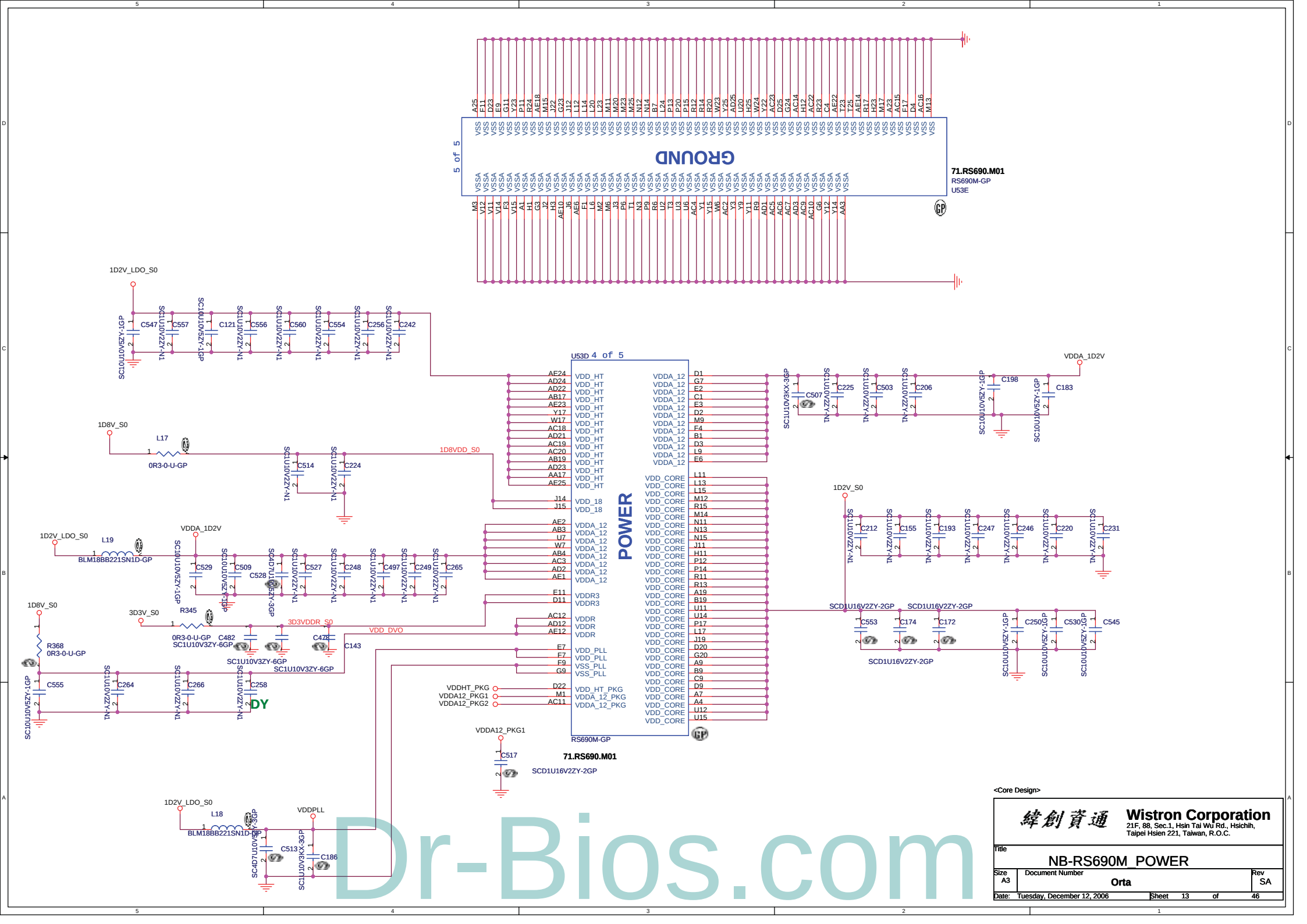
GROUND
5 of 5
71.RS690.M01
RS690M-GP
U53E
POWER
U53D 4 of 5
RS690M-GP
71.RS690.M01
1D2V_LDO_S0
1D8V_S0
3D3V_S0
VDDA_1D2V
1D2V_S0
1D8VDD_S0
3D3VDDR_S0
VDD_DVO
VDDPLL
VDDA12_PKG1
DY
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
NB-RS690M_POWER
Size A3
Document Number
Orta
Rev SA
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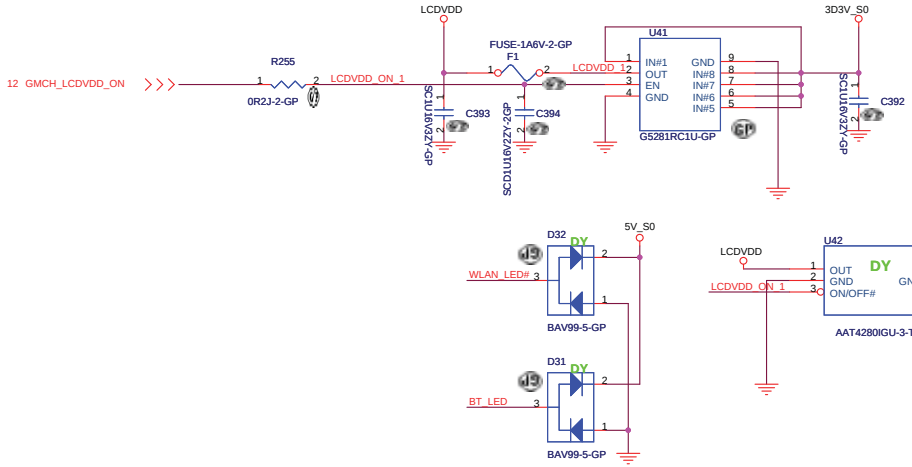
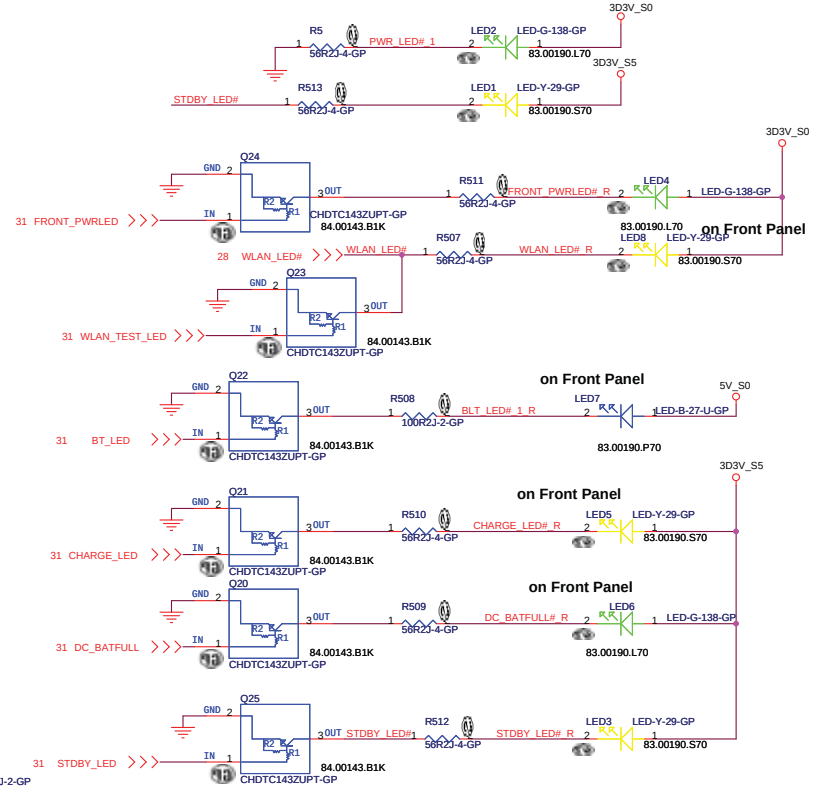
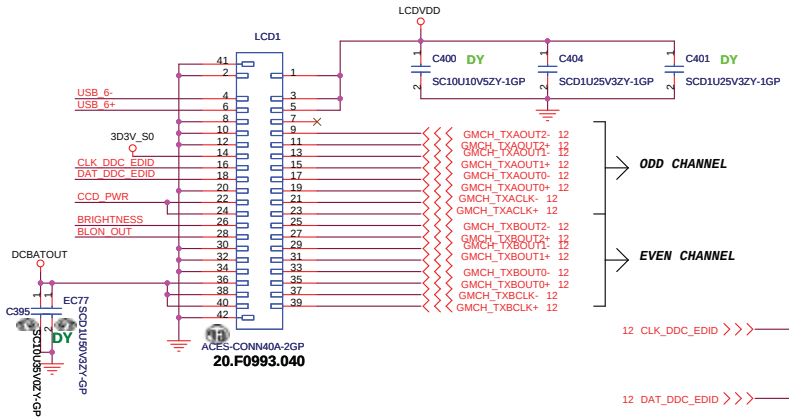
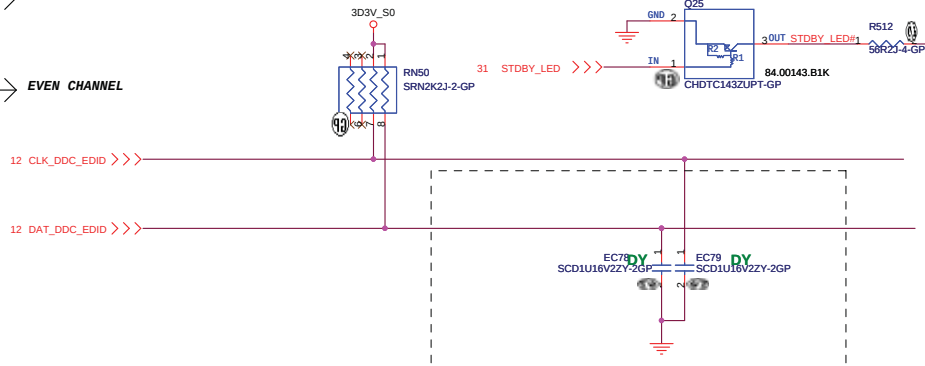
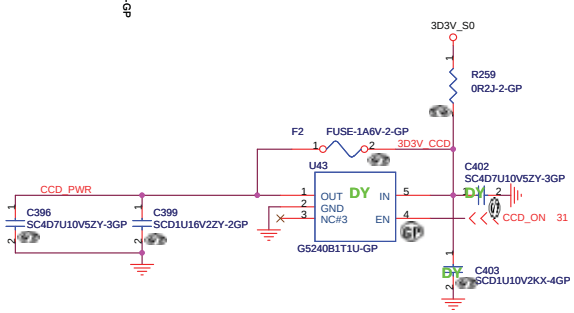
LCD/INVERTER CONN

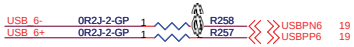


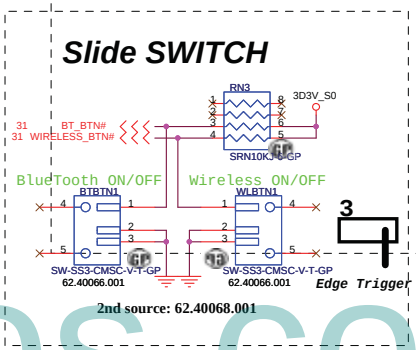




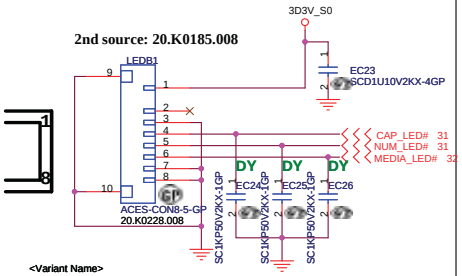








LED BD



<Variant Name>

蜂創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD CONN & LED

Size	Document Number	Rev
	Orta	SA

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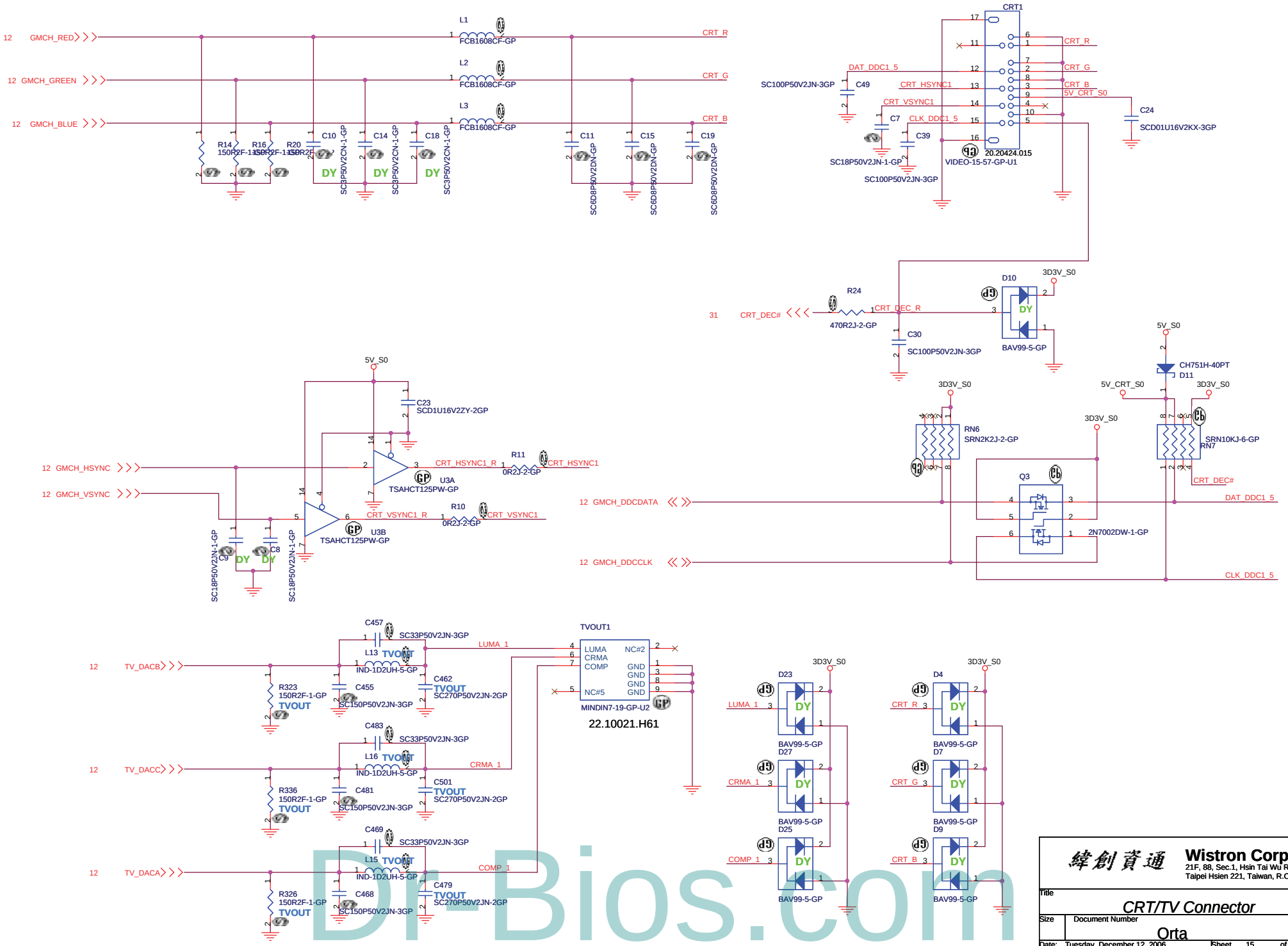

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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *CRT/TV Connector*

Size	Document Number	Rev
	Orta	SA

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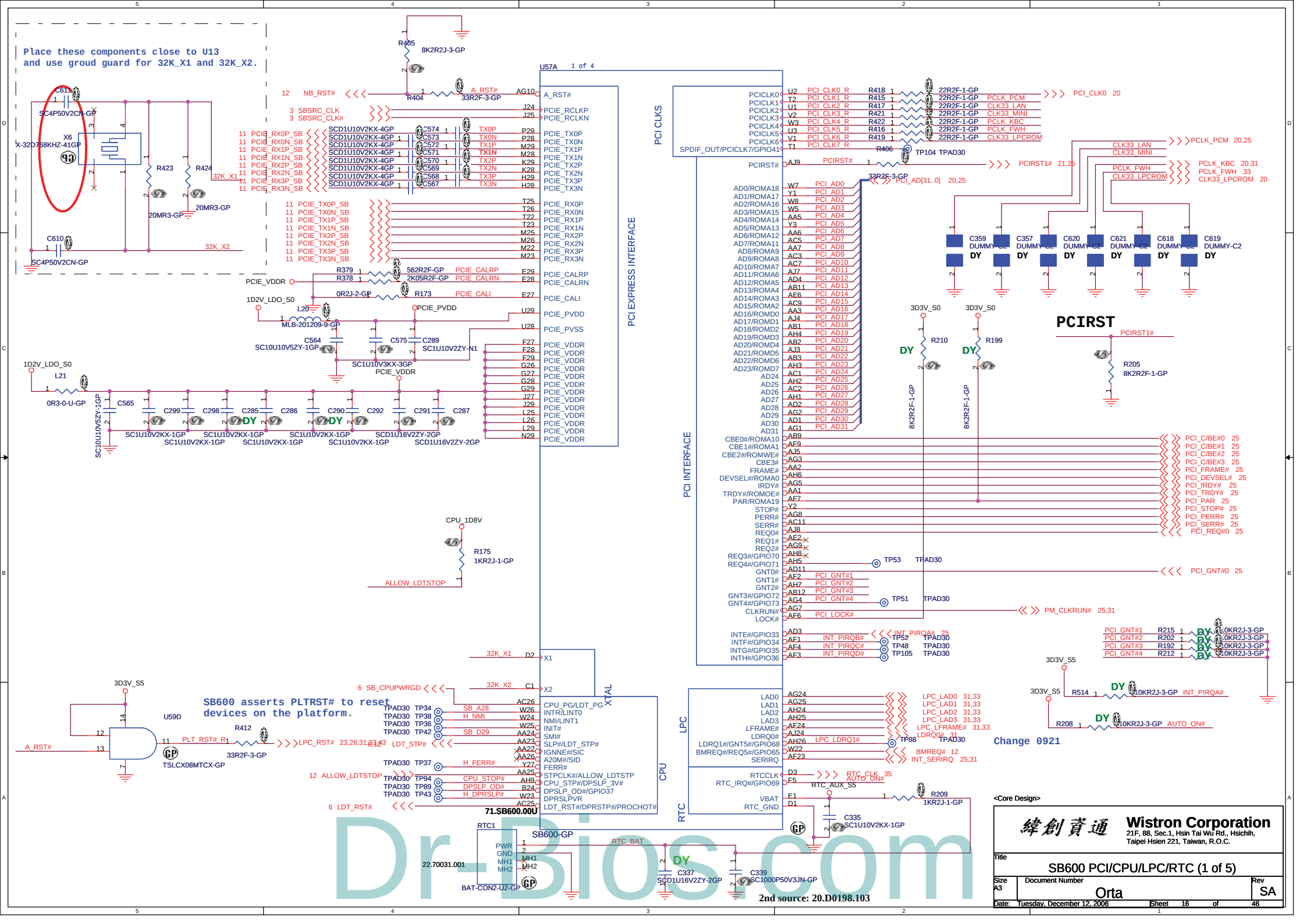
Place these components close to U13
and use groud guard for 32K_X1 and 32K_X2.
SB600 asserts PLTRST# to reset
devices on the platform.
PCIRST
Change 0921
U57A 1 of 4
PCI CLKS
PCI EXPRESS INTERFACE
PCI INTERFACE
LPC
CPU
RTC
XTAL
SB600-GP
71.SB600.00U
2nd source: 20.D0198.103
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
SB600 PCI/CPU/LPC/RTC (1 of 5)
Orta
Size A3
Rev SA
Date: Tuesday, December 12, 2006
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Dr-Bios.com

PLACE SATA AC DECOUPLING
CAPS CLOSE TO SB460

SCD01U50V2KX-1GP
SCD01U50V2KX-1GP
SCD01U50V2KX-1GP
SCD01U50V2KX-1GP

U57B 2 of 4

SATA_TXP0 SB AH21
SATA_TXN0 SB AJ21
SATA_RXN0 SB AH20
SATA_RXP0 SB AJ20

SATA_TX0+
SATA_TX0-
SATA_RX0-
SATA_RX0+
SATA_TX1+
SATA_TX1-
SATA_RX1-
SATA_RX1+
SATA_TX2+
SATA_TX2-
SATA_RX2-
SATA_RX2+
SATA_TX3+
SATA_TX3-
SATA_RX3-
SATA_RX3+
SATA_CAL
SATA_X1
SATA_X2
SATA_ACT#/GPIO67

SERIAL ATA

PLLVDD_SATA
PLLVDD_SATA
XTLVDD_SATA
AVDD_SATA
AVSS_SATA

SERIAL ATA POWER

SB600-GP

SATA

SATA_X1
R381
SATA_X2
10MR2J-L-GP
X5
XTAL-25MHZ-20GP
C582 SC10P50V2JN-4GP
C576 SC10P50V2JN-4GP

According to PA_IXP600AD9
Change C936 and C937 from 27P to 10P.

R397 1KR2F-3-GP
3D3V_S0
R191 10KR2J-3-GP
SATA_CAL
SATA_X1
SATA_X2
32 SATA_LED#

PLLVDD_ATA
XTLVDD_ATA
AVDD_SATA

ATA 66/100

IDE_IORDY AB29
IDE_IRQ AA28
IDE_A0 AA29
IDE_A1 AB27
IDE_A2 Y28
IDE_DACK# AB28
IDE_DRQ AC27
IDE_IOR# AC29
IDE_IOW# AC28
IDE_CS1# W28
IDE_CS3# W27

IDE_PDIORDY 21
INT_IRQ14 21
IDE_PDA0 21
IDE_PDA1 21
IDE_PDA2 21
IDE_PDDACK# 21
IDE_PDDREQ 21
IDE_PDIOR# 21
IDE_PDIOW# 21
IDE_PDCS1# 21
IDE_PDCS3# 21

IDE_D0/GPIO15 AD28
IDE_D1/GPIO16 AD26
IDE_D2/GPIO17 AE29
IDE_D3/GPIO18 AE27
IDE_D4/GPIO19 AG29
IDE_D5/GPIO20 AH28
IDE_D6/GPIO21 AJ28
IDE_D7/GPIO22 AJ27
IDE_D8/GPIO23 AH27
IDE_D9/GPIO24 AG27
IDE_D10/GPIO25 AG28
IDE_D11/GPIO26 AF28
IDE_D12/GPIO27 AF29
IDE_D13/GPIO28 AE28
IDE_D14/GPIO29 AD25
IDE_D15/GPIO30 AD29

IDE_PDD0 21
IDE_PDD1 21
IDE_PDD2 21
IDE_PDD3 21
IDE_PDD4 21
IDE_PDD5 21
IDE_PDD6 21
IDE_PDD7 21
IDE_PDD8 21
IDE_PDD9 21
IDE_PDD10 21
IDE_PDD11 21
IDE_PDD12 21
IDE_PDD13 21
IDE_PDD14 21
IDE_PDD15 21

SPI ROM

SPI_DI/GPIO12 J3
SPI_DO/GPIO11 J6
SPI_CLK/GPIO47 G3
SPI_HOLD#/GPIO31 G2
SPI_CS#/GPIO32 G6
LAN_RST#/GPIO13 C23
ROM_RST#/GPIO14 G5

TP54 TPAD30
TP45 TPAD30
TP50 TPAD30
TP101 TPAD30
TP46 TPAD30
TP41 TPAD30
TP47 TPAD30

HW MONITOR

FANOUT0/GPIO3 M4
FANOUT1/GPIO48 T3
FANOUT2/GPIO49 V4
FANIN0/GPIO50 N3
FANIN1/GPIO51 P2
FANIN2/GPIO52 W4
TEMP_COMM P5
TEMPIN0/GPIO61 P7
TEMPIN1/GPIO62 P8
TEMPIN2/GPIO63 T8
TEMPIN3/TALERT#/GPIO64 T7
ALERT# 6,35

VIN0/GPIO53 V5 PSW_CLR#
VIN1/GPIO54 L7 UMA_DIS
VIN2/GPIO55 M8 CLK_ID
VIN3/GPIO56 V6
VIN4/GPIO57 M6 FP_ID
VIN5/GPIO58 P4
VIN6/GPIO59 M7
VIN7/GPIO60 V7

FP_ID 32
FP_DETECT# 32

AVDD N1
AVSS M1

AVDD_HWM
R432 0R3-0-U-GP
3D3V_S0
C613 SCD1U16V2ZY-2GP
C614 SC2D2U6D3V3KX-GP
DY

3D3V_S0
R149 10KR2J-3-GP
FP_DETECT#
PSW_CLR#
G41 GAP-OPEN

0 => DIS
1 => UMA

3D3V_S0
R214 10KR2J-3-GP
R197 10KR2J-3-GP RTL
R198 10KR2J-3-GP DY
UMA_DIS
CLK_ID
FP_ID
R217 10KR2J-3-GP DY
R206 10KR2J-3-GP ICS
R207 10KR2J-3-GP DY
10KR2J-3-GP

71.SB600.00U

SATA

3D3V_S0 R187 0R3-0-U-GP
XTLVDD_ATA
EC117 SCD1U16V2ZY-2GP
C318 SC2D2U6D3V3KX-GP

1D2V_LDO_S0 R193 0R3-0-U-GP
PLLVDD_ATA
EC118 SCD1U16V2ZY-2GP
C320 SC2D2U6D3V3KX-GP

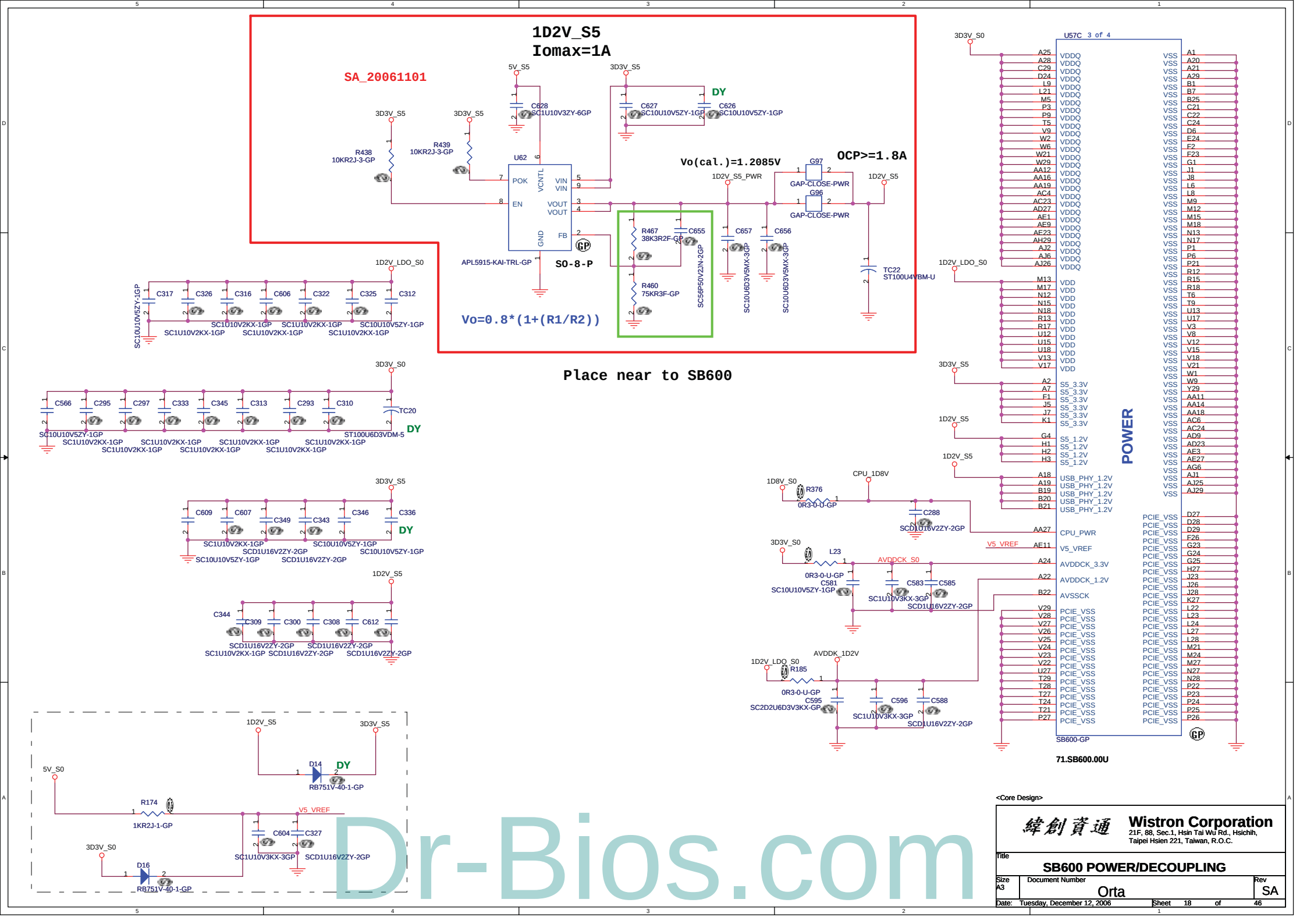
1D2V_LDO_S0 R177 0R3-0-U-GP
AVDD_SATA
EC114 SCD1U16V2ZY-2GP
C311 SC10U6D3V5KX-1GP
C307 SC10U6D3V5KX-1GP
EC63 SCD1U16V2ZY-2GP DY
EC65 SCD1U16V2ZY-2GP DY
EC62 SCD1U16V2ZY-2GP DY
EC60 SCD1U16V2ZY-2GP DY
EC64 SCD1U16V2ZY-2GP

<Core Design>

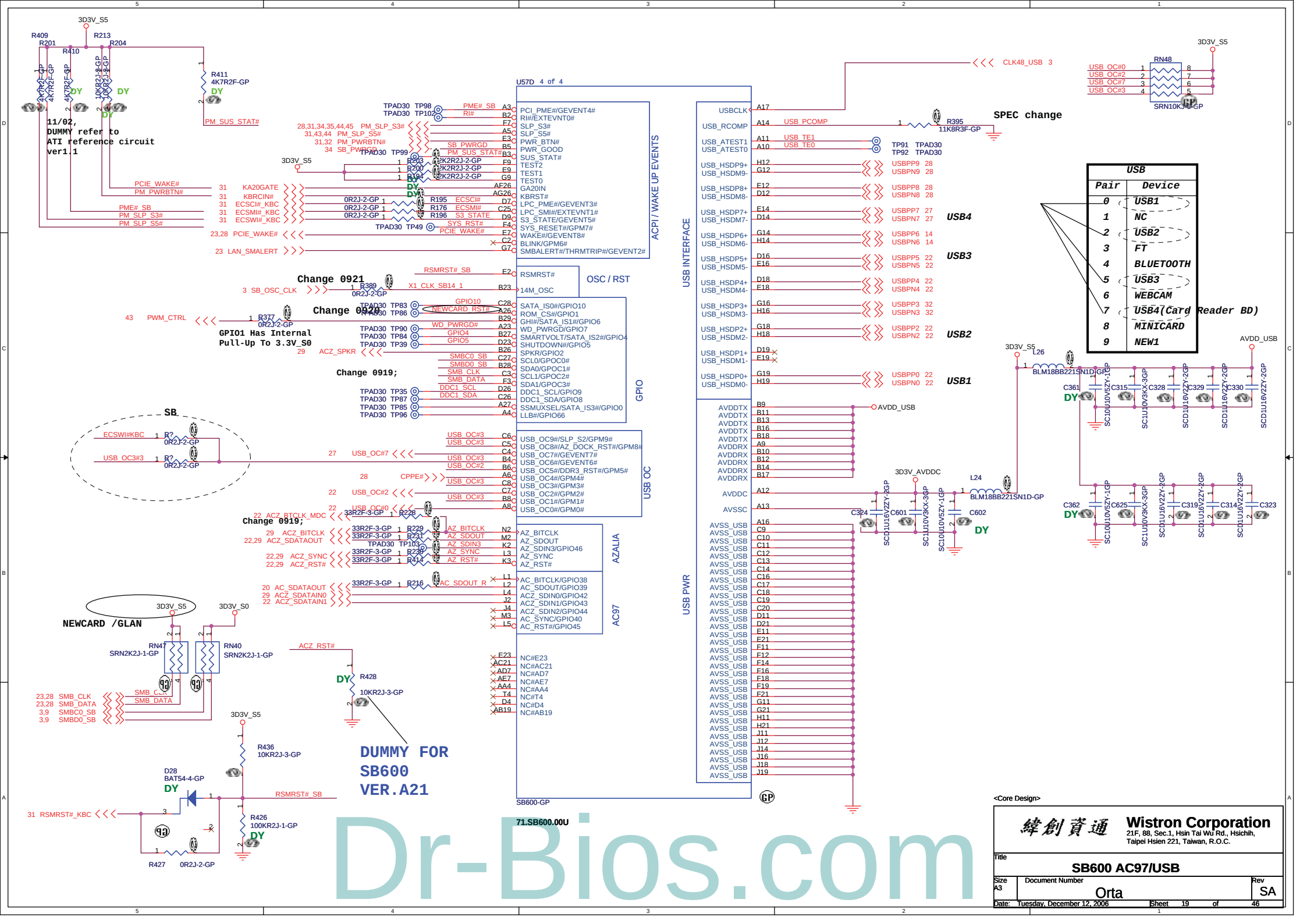
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

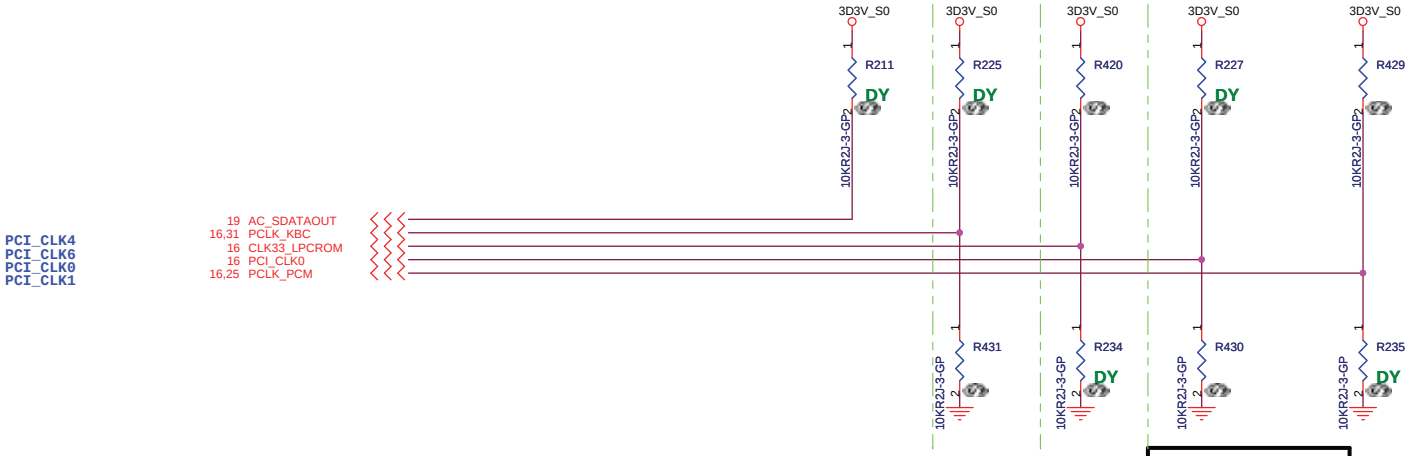
Title: SB600 ACPI/GPIO/SATA/IDE (2 of 5)
Size: A3
Document Number: Orta
Rev: SA
Date: Tuesday, December 12, 2006
Sheet 17 of 46

Dr-Bios.com


1D2V_S5
Iomax=1A
SA_20061101
Vo(cal.)=1.2085V
OCP>=1.8A
Vo=0.8*(1+(R1/R2))
Place near to SB600
SO-8-P
APL5915-KAI-TRL-GP
U62
U57C 3 of 4
POWER
SB600-GP
71.SB600.00U
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
SB600 POWER/DECOUPLING
Orta
Tuesday, December 12, 2006
Sheet 18 of 46

Dr-Bios.com

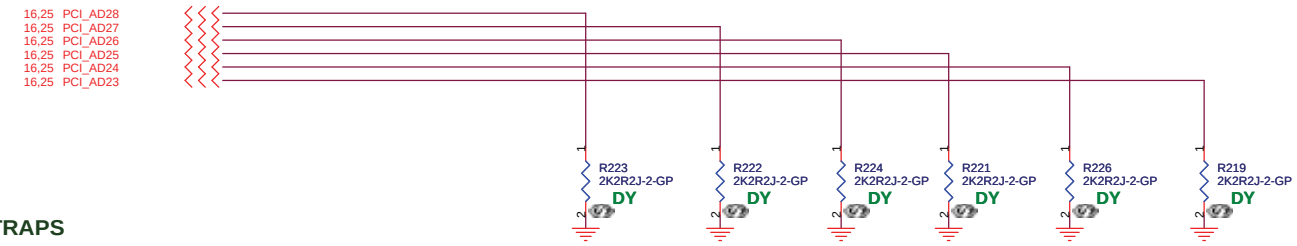

11/02,
DUMMY refer to
ATI reference circuit
ver1.1
Change 0921
Change 0920
GPIO1 Has Internal
Pull-Up To 3.3V_S0
Change 0919;
Change 0919;
SB
NEWCARD /GLAN
DUMMY FOR
SB600
VER.A21
SPEC change
USB
Pair Device
0 USB1
1 NC
2 USB2
3 FT
4 BLUETOOTH
5 USB3
6 WEBCAM
7 USB4(Card Reader BD)
8 MINICARD
9 NEW1
USB4
USB3
USB2
USB1
U57D 4 of 4
ACPI / WAKE UP EVENTS
USB INTERFACE
OSC / RST
GPIO
USB OC
AZALIA
AC97
USB PWR
SB600-GP
71.SB600.00U
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
SB600 AC97/USB
Size A3
Document Number
Orta
Rev SA
Date: Tuesday, December 12, 2006
Sheet 19 of 46
Dr-Bios.com



REQUIRED SYSTEM STRAPS

		SB600			
	AC_SDOUT	PCI_CLK4	PCI_CLK6	PCI_CLK0	PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM DEFAULT L, L = FWH ROM	
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	USE EXT. 48MHZ DEFAULT	CPU IF=P4		

SB600 HAS 15K INTERNAL PU FOR PCI_AD[23..28]



DEBUG STRAPS

		PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
STRAP HIGH		RESERVED	RESERVED	RESERVED	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOT FAIL TIMER DISABLE DEFAULT
STRAP LOW					USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOT FAIL TIMER ENABLE

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<Core Design>

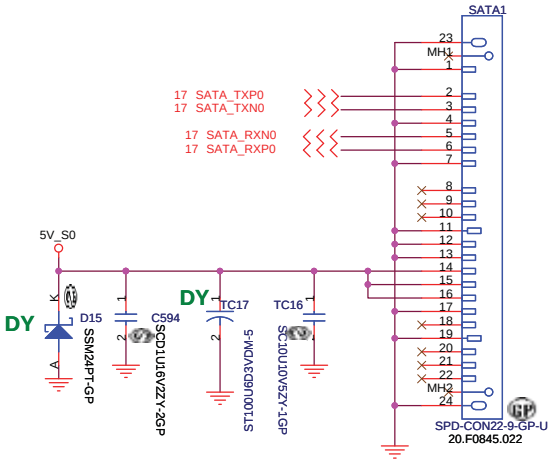
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SB600 STRAPPING PIN

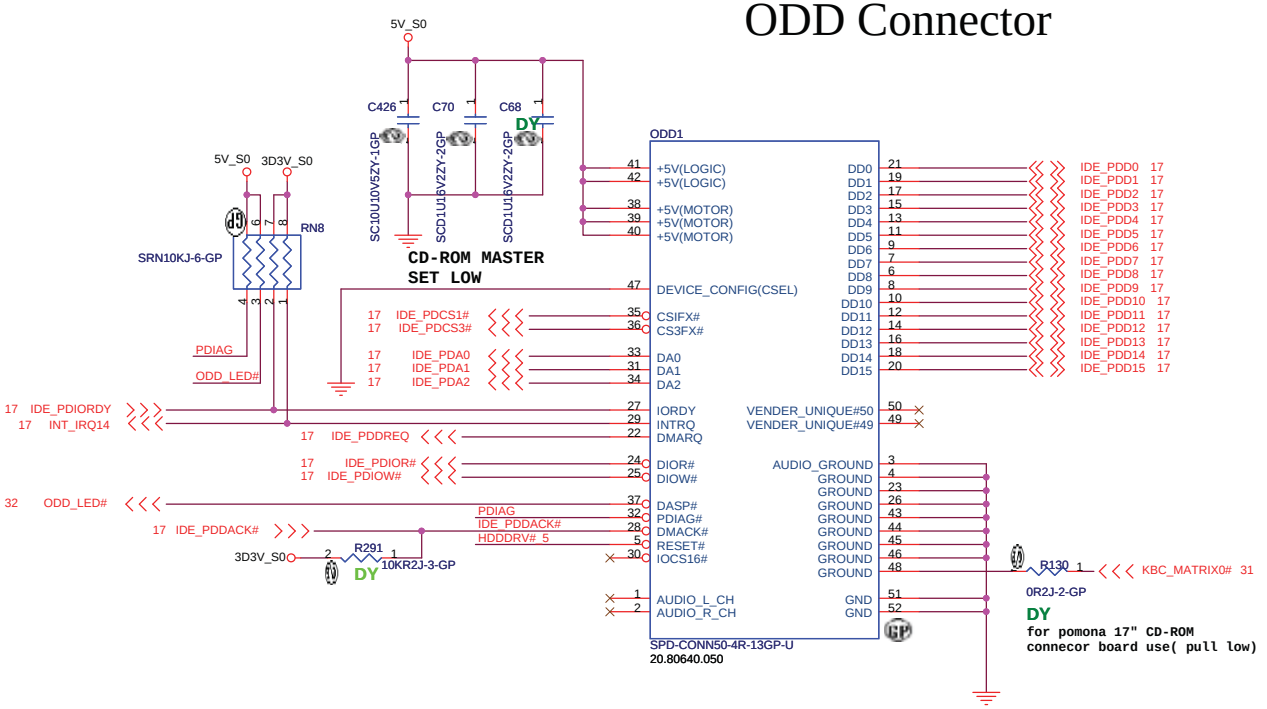
Size: A3 | Document Number: Orta | Rev: SA

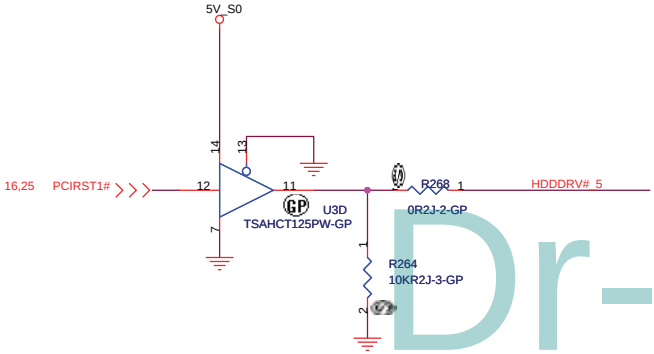
Date: Tuesday, December 12, 2006 | Sheet 20 of 46

SATA HD Connector



ODD Connector





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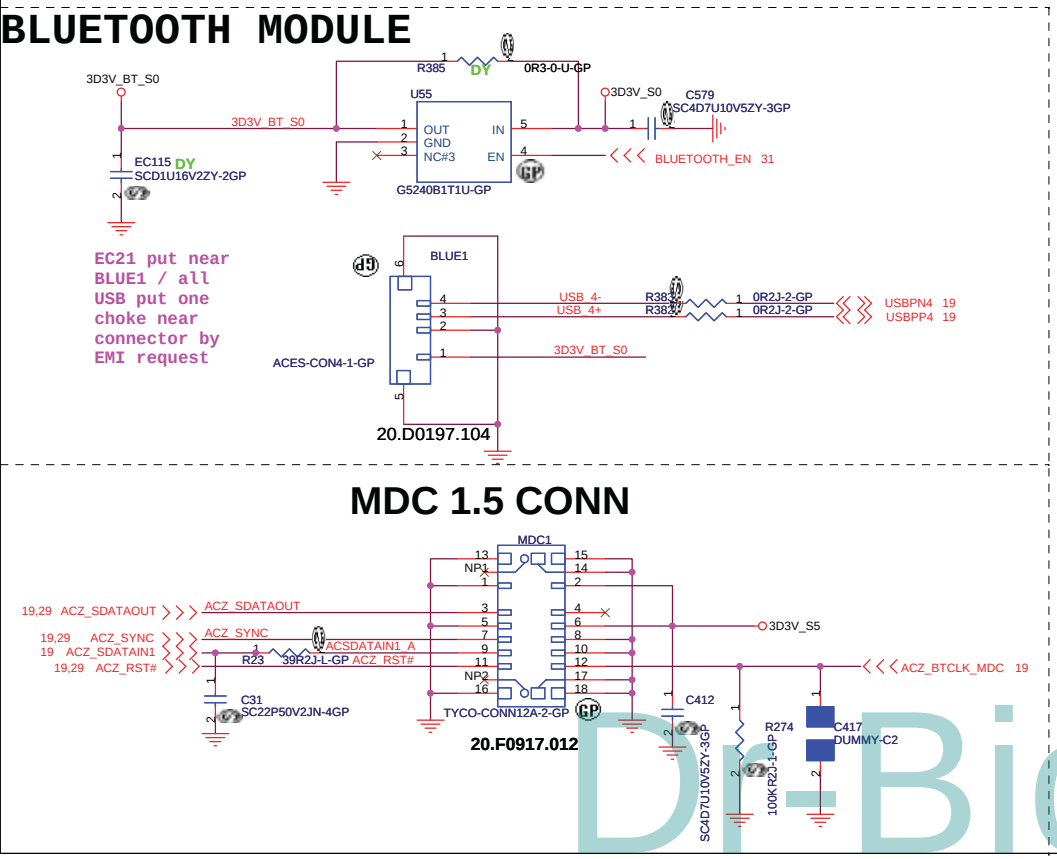
bom1

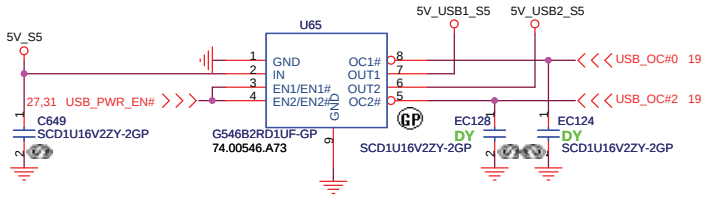
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

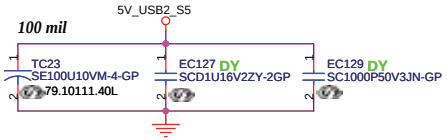
Title: ***HDD and CDROM***

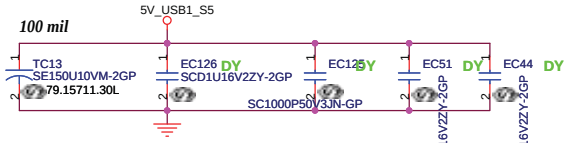
Size	Document Number	Rev
	Orta	SA

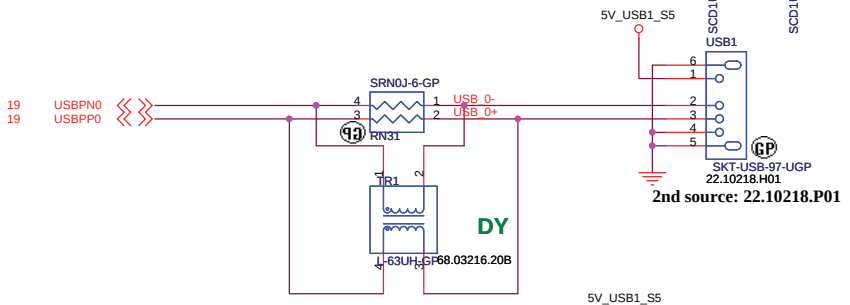
Date: Tuesday, December 12, 2006 Sheet 21 of 46

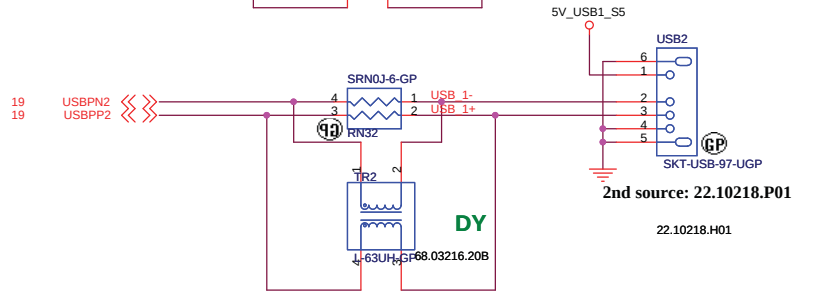


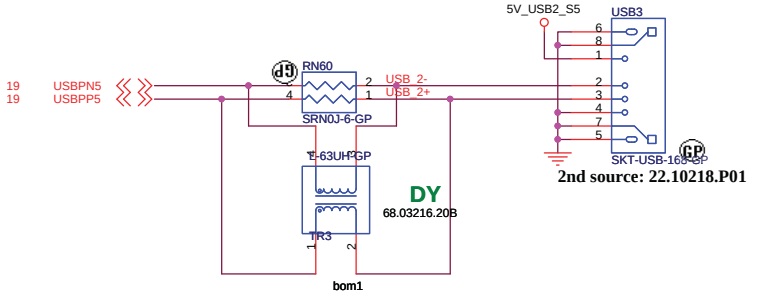












緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB / MDC / BLUETOOTH

Size	Document Number	Rev
	Orta	SA

Date: Tuesday, December 12, 2006 Sheet 22 of 46

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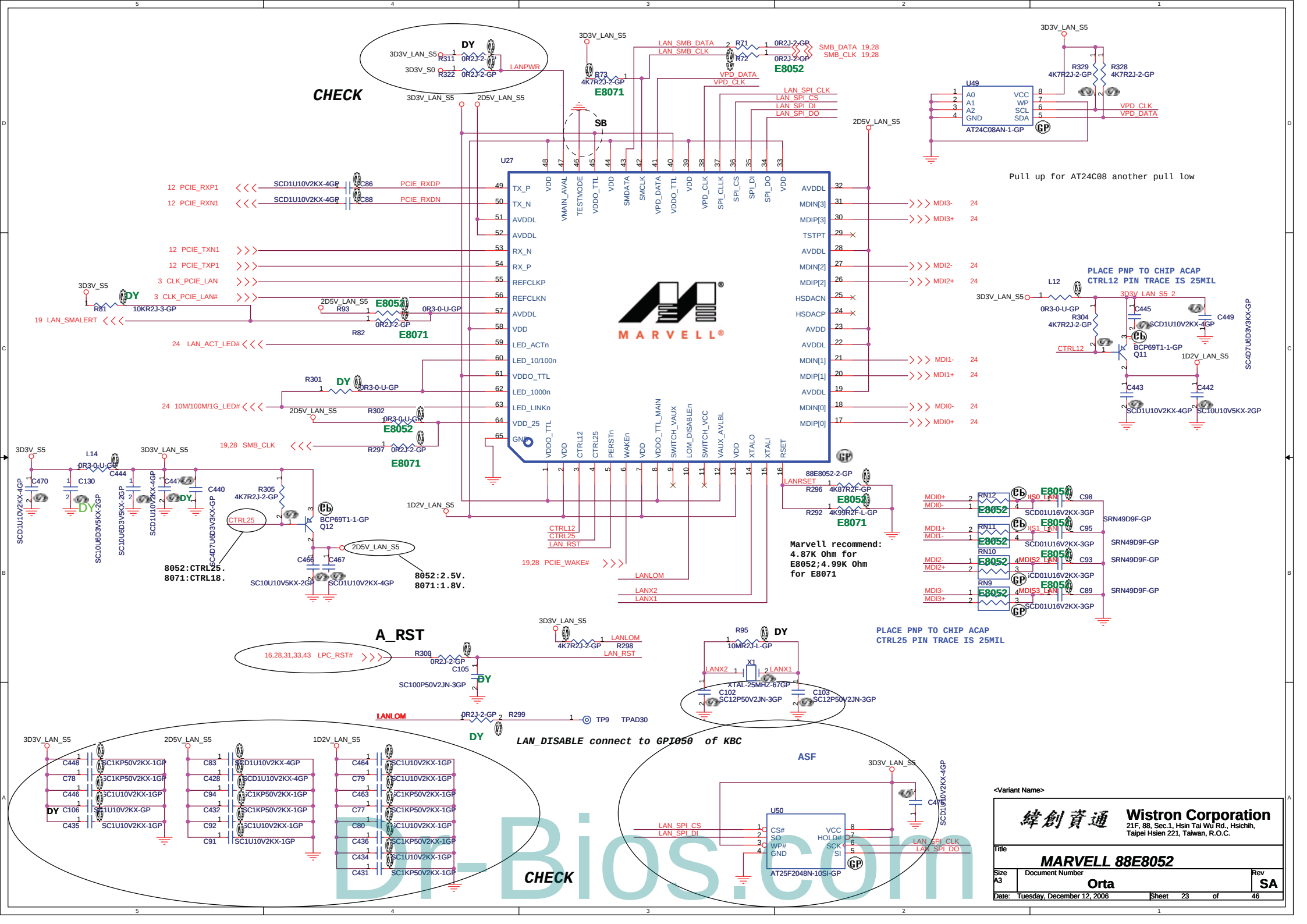
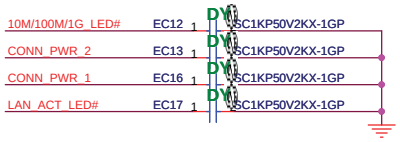
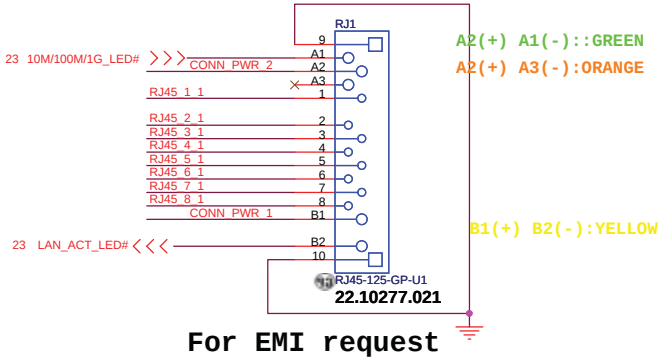
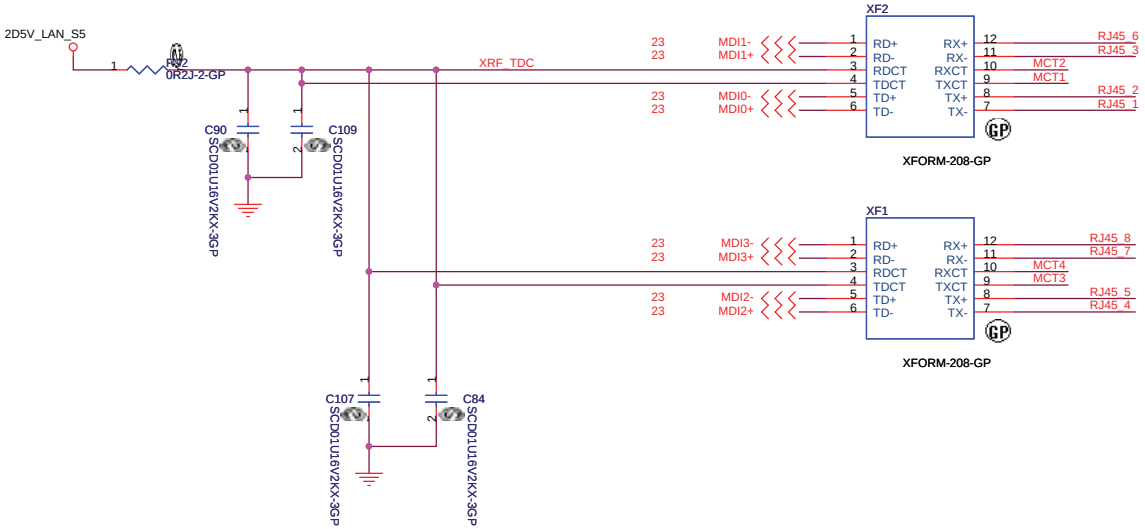

CHECK
SB
U27
MARVELL
Pull up for AT24C08 another pull low
PLACE PNP TO CHIP ACAP
CTRL12 PIN TRACE IS 25MIL
PLACE PNP TO CHIP ACAP
CTRL25 PIN TRACE IS 25MIL
8052:CTRL25.
8071:CTRL18.
8052:2.5V.
8071:1.8V.
Marvell recommend:
4.87K Ohm for
E8052;4.99K Ohm
for E8071
A_RST
LAN_DISABLE connect to GPI050 of KBC
ASF
CHECK
Dr-Bios.com
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
MARVELL 88E8052
Orta
Tuesday, December 12, 2006

LAN Connector

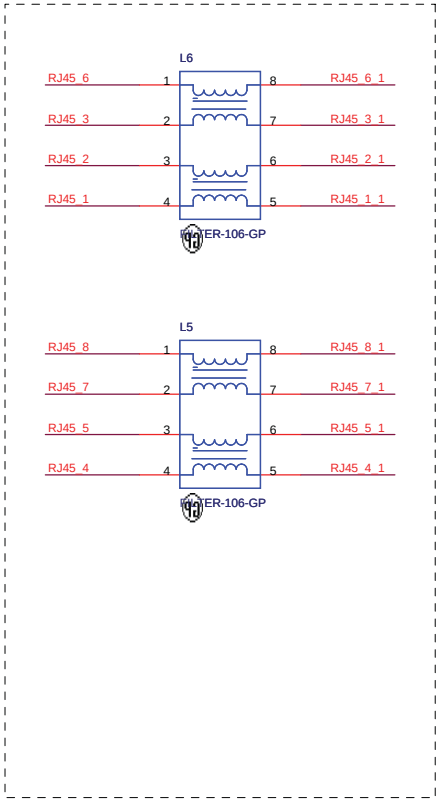




GIGA Lan Transformer



For EMI request

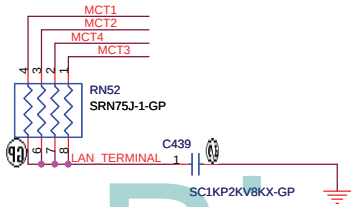


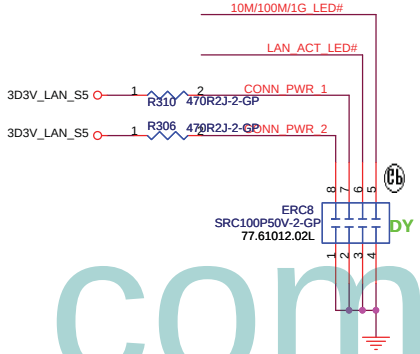
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6





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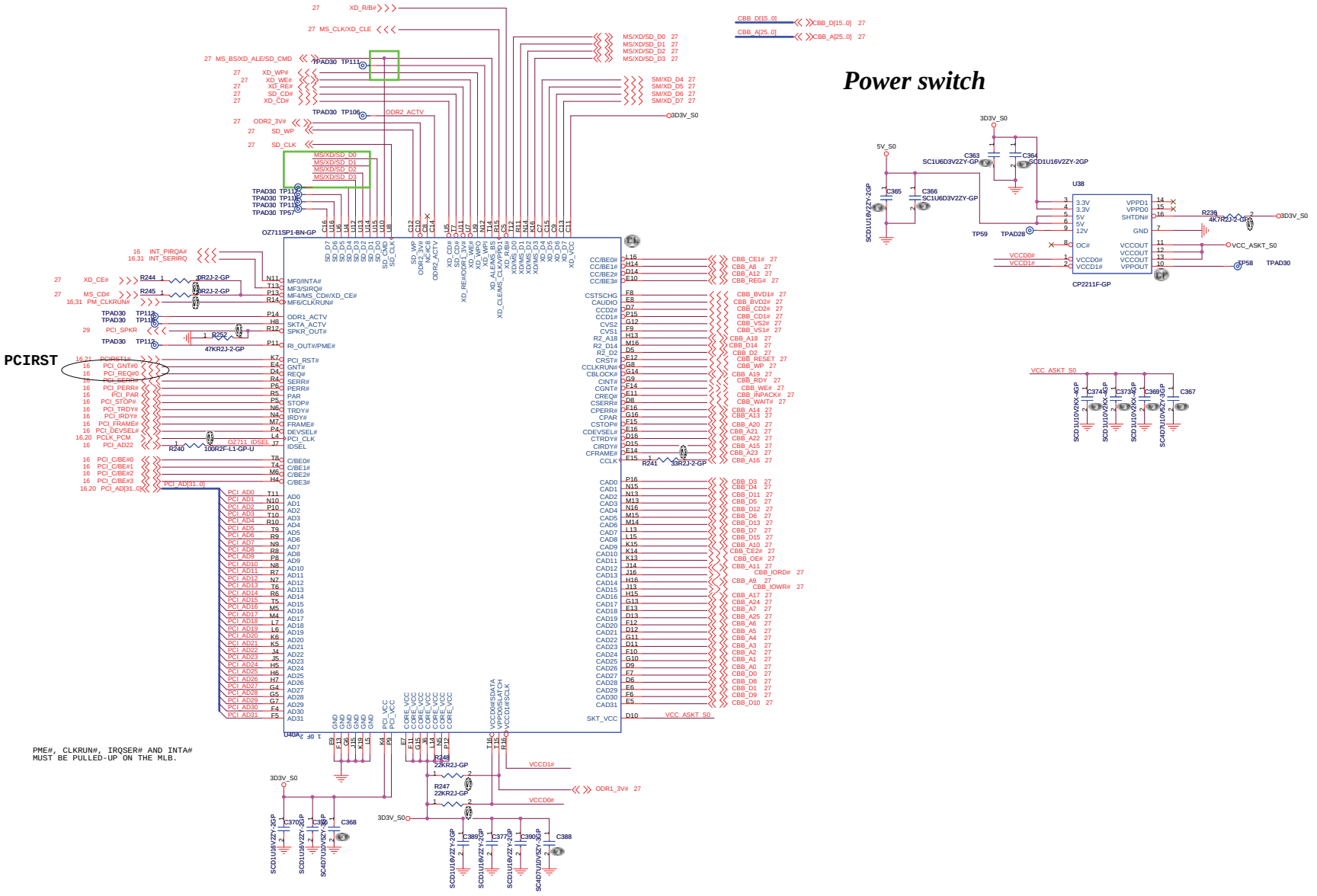
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN Connector**

Size: A3 | Document Number: **Orta** | Rev: **SA**

Date: Tuesday, December 12, 2006 | Sheet 24 of 46



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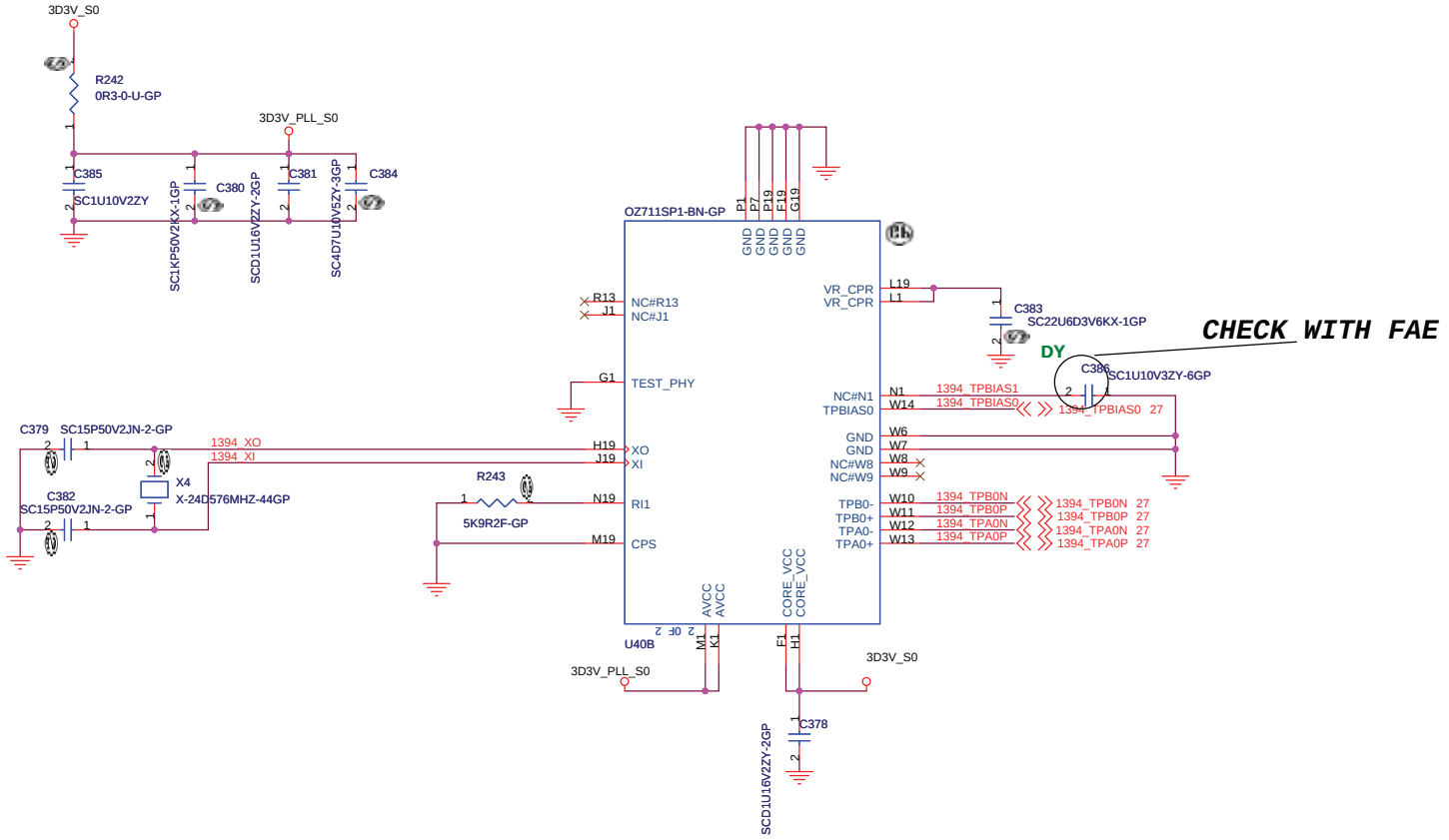
<variant_name>

蜂創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	OZ711SP1 (1 of 2)	
Size	Document Number: Orta	Rev: SA
Date: Tuesday, December 12, 2006	Sheet 25 of 46	



Dr-Bios.com

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *OZ711SP1 (2 of 2)*

Size	Document Number	Rev
	Orta	SA

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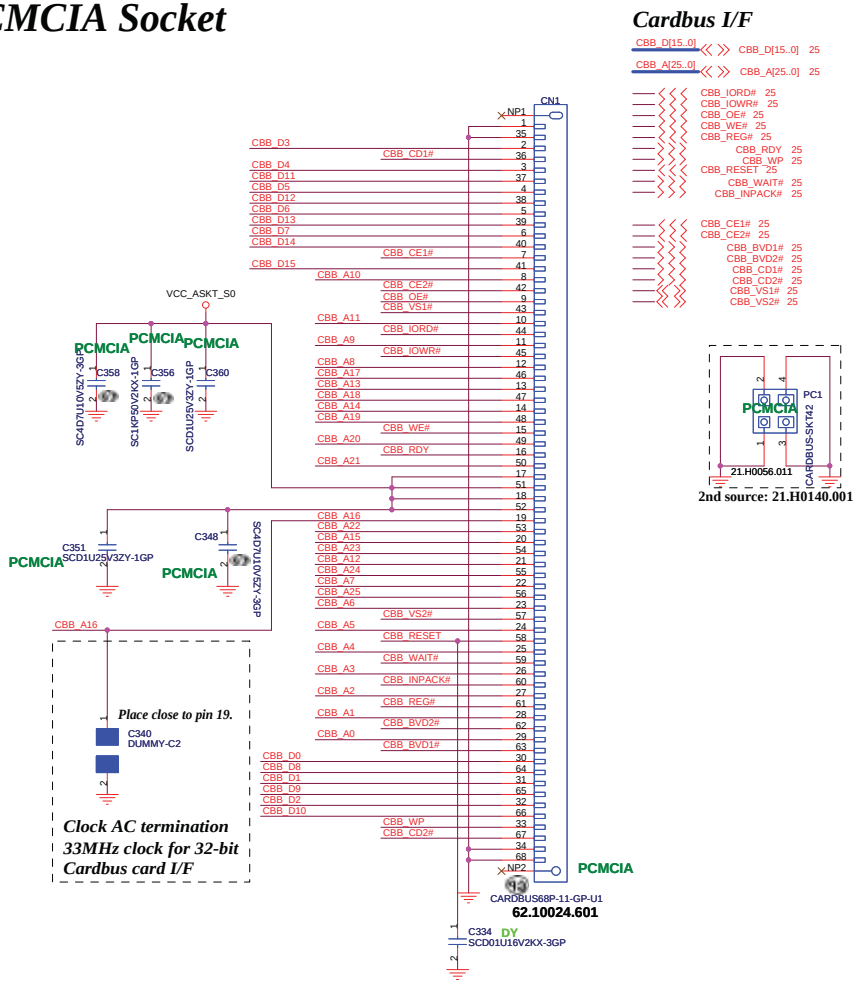
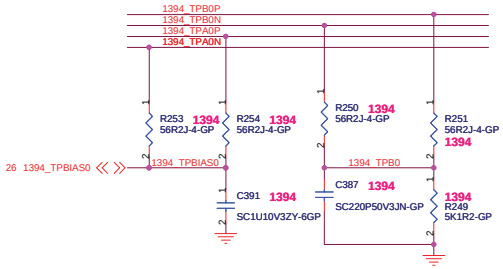
PCMCIA Socket

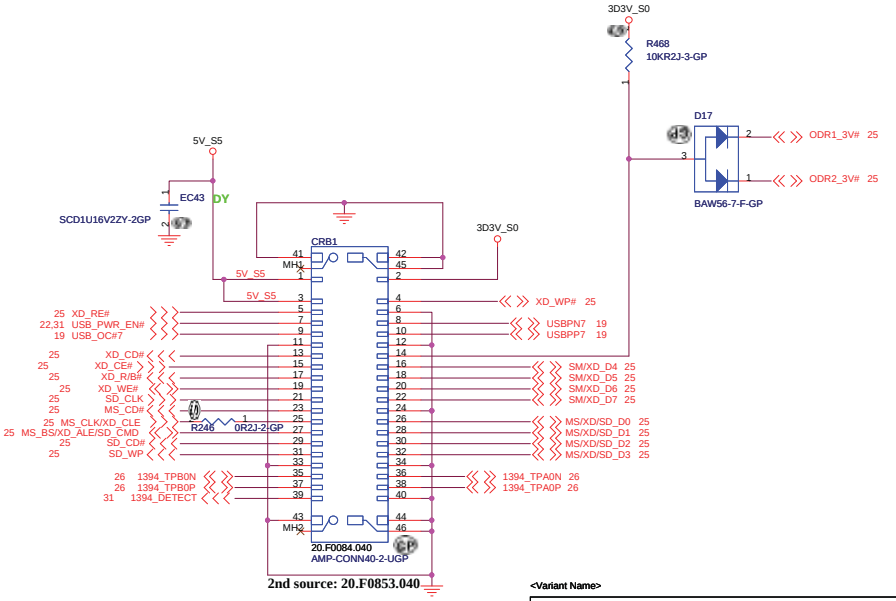


Cardbus I/F

2nd source: 21.H0140.001

CLOSE TO CHIP





XD
MS / MS PRO
SD / SD IO / MMC

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCMCIA / 1394 / CARD READER

Size	Document Number	Rev
	Orta	SA

Date: Tuesday, December 12, 2006 Sheet 27 of 46

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Mini Card Connector

NEWCARD Connector

SK1
NEW
CARDBUS-SKT70-GP-U
21.H0110.001

Reserve the symbol for bottom side connector

NEW1
FCI-CON26-5-GP
20.F0789.026

11 PCIE_TXP3
11 PCIE_TXN3
11 PCIE_RXP3
11 PCIE_RXN3
3 CLK_PCIE_NEW
3 CLK_PCIE_NEW#
19 CPPE#
3 NEWCARD_CLKREQ#
3D3V_NEW_S0
3D3V_NEW_LAN_S5
EC72
EC73
SCD1U10V2KX-4GP
19,23 PCIE_WAKE#
PCIE_WAKE# R
R239 0R2J-2-GP
1D5V_NEW_S0
RN49
SRN33J-5-GP-U
19,23 SMB_DATA
19,23 SMB_CLK
SMB_DATA_NEW
SMB_CLK_NEW
CONN_TP
CPUTSB#
TP108
TP109
TPS2231_PERST#
19 USBPP9
19 USBPN9

MINIC1
MINIPCI52P-1-GP-U
62.10043.331

3D3V_S5
1D5V_S0
3D3V_S0
5V_AUX_S5
1.5V
3.3V
+1.5V
+1.5V
+3.3V
+3.3VAUX
REFCLK+
REFCLK-
PERN0
PERP0
PETN0
PETP0
USB_D-
USB_D+
CLK_PCIE_MINI1 3
CLK_PCIE_MINI1# 3
PCIE_RXN2 12
PCIE_RXP2 12
PCIE_TXN2 12
PCIE_TXP2 12
USBPN8 19
USBPP8 19
SMB_CLK
SMB_DATA
WAKE#
CLKREQ#
PERST#
MINI_WAKE#
TP93
TPAD30
LPC_RST# 16,23,31,33,43
RESERVED#3
RESERVED#5
RESERVED#8
RESERVED#10
RESERVED#12
RESERVED#14
RESERVED#16
RESERVED#17
RESERVED#19
RESERVED#20
RESERVED#37
RESERVED#39
RESERVED#41
RESERVED#43
RESERVED#45
RESERVED#47
RESERVED#49
RESERVED#51
GND
19,23 SMB_CLK
19,23 SMB_DATA
R407 0R2J-2-GP
R408 0R2J-2-GP
TPAD30 TP95 UMI_PWR
UMI_DATA
UMI_CLK
TPAD30 TP97 UMI_RESET
TPAD30 TP100 UMI_VPP
31 E51_RxD
31 E51_TxD
31 WIRELESS_EN
R413 10KR2J-3-GP
TPAD30 TP55 LED_WWAN#
14 WLAN_LED#
LED_WLAN#
TP56 TPAD28 LED_WPAN#
LED_WWAN#
LED_WLAN#
LED_WPAN#

A_RST

WHEN DUMMY U19,R702 MUST STUFF

16,23,31,33,43 LPC_RST#
R232 0R2J-2-GP
NEW_PLT_RST1#
C355 SC100P50V2JN-3GP
3D3V_S5
R238 100KR2J-1-GP
R237 100KR2J-1-GP
CPPE#
CPUTSB#
TPS2231_PERST#
31,32,35 S5_ENABLE
1D5V_S0
1D5V_NEW_S0
3D3V_NEW_LAN_S5
U37
SYSRST#
CPPE#
CPUSB#
PERST#
SHDN#
3_3VIN
3_3VOUT
1_5VOUT
1_5VIN
AUXIN
AUXOUT
NC#4
NC#5
NC#13
NC#14
NC#16
STBY#
CLKEN
OC#
GND
P2231NFC1-GP
19,31,34,35,44,45 PM_SLP_S3#

Place near MINIC1
TC21 ST220U6D3VDM-13GP
C637 SC100U6D3V5MX-3GP
C624 SC1U16V3ZY-GP
C633 SCD1U16V2ZY-2GP
C630 SC100U6D3V5MX-3GP
C623 SC1U16V3ZY-GP
C605 SCD1U16V2ZY-2GP
C615 SCD1U16V2ZY-2GP
C617 SC100U6D3V5MX-3GP

C354 NEW SCD1U16V2ZY-2GP
Place them Near to Chip

C350 NEW SC1U16V3ZY-GP
C353 NEW SCD1U16V2ZY-2GP
C375 NEW SC1U16V3ZY-GP
C371 NEW SCD1U16V2ZY-2GP
C372 NEW SCD1U16V2ZY-2GP
Place them Near to Connector

CHECK WITH COLUMBIA

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bom1

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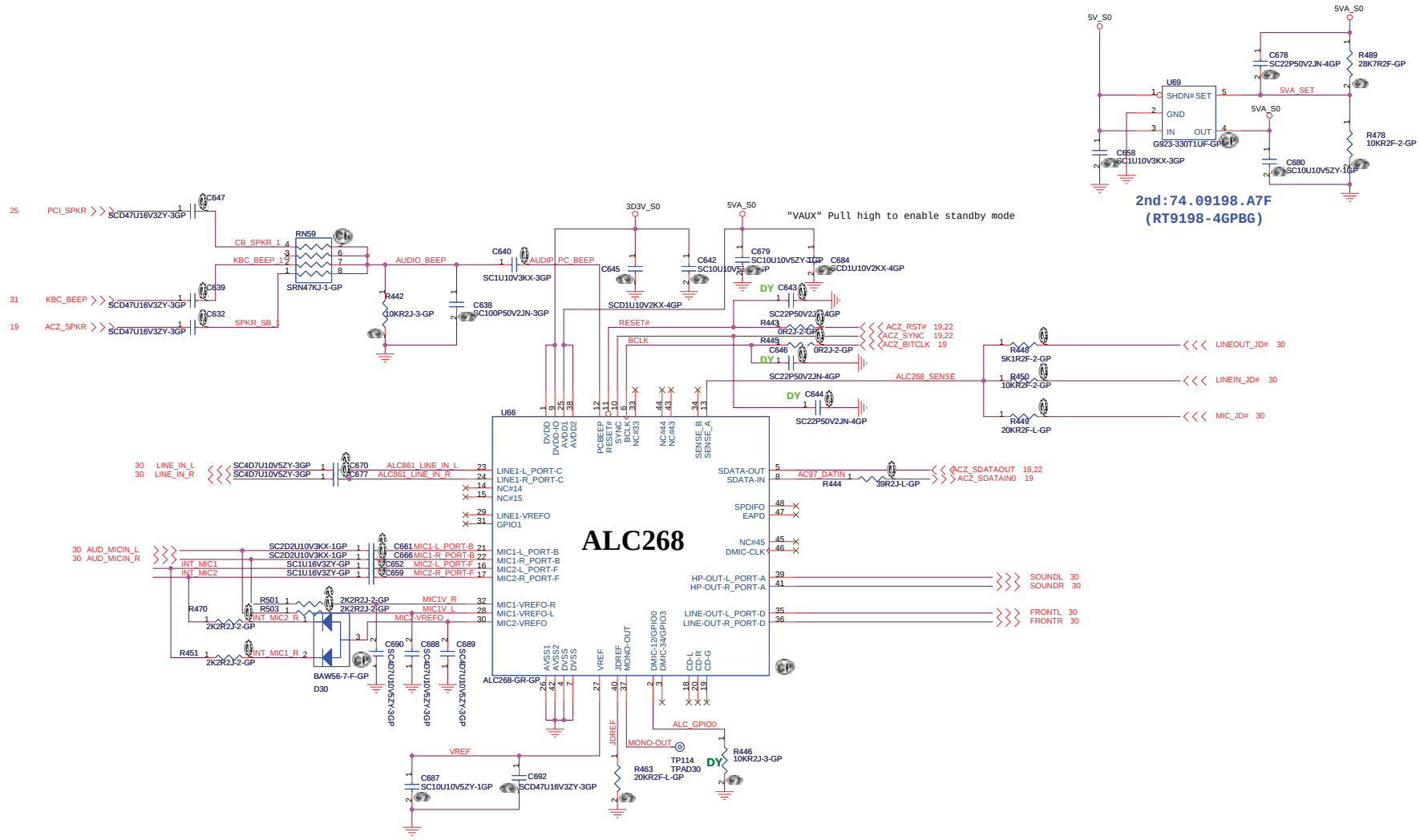
Title: MINI CARD / NEW CARD
Size: Document Number: Orta
Rev: SA
Date: Tuesday, December 12, 2006
Sheet 28 of 46



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<Variant Name>

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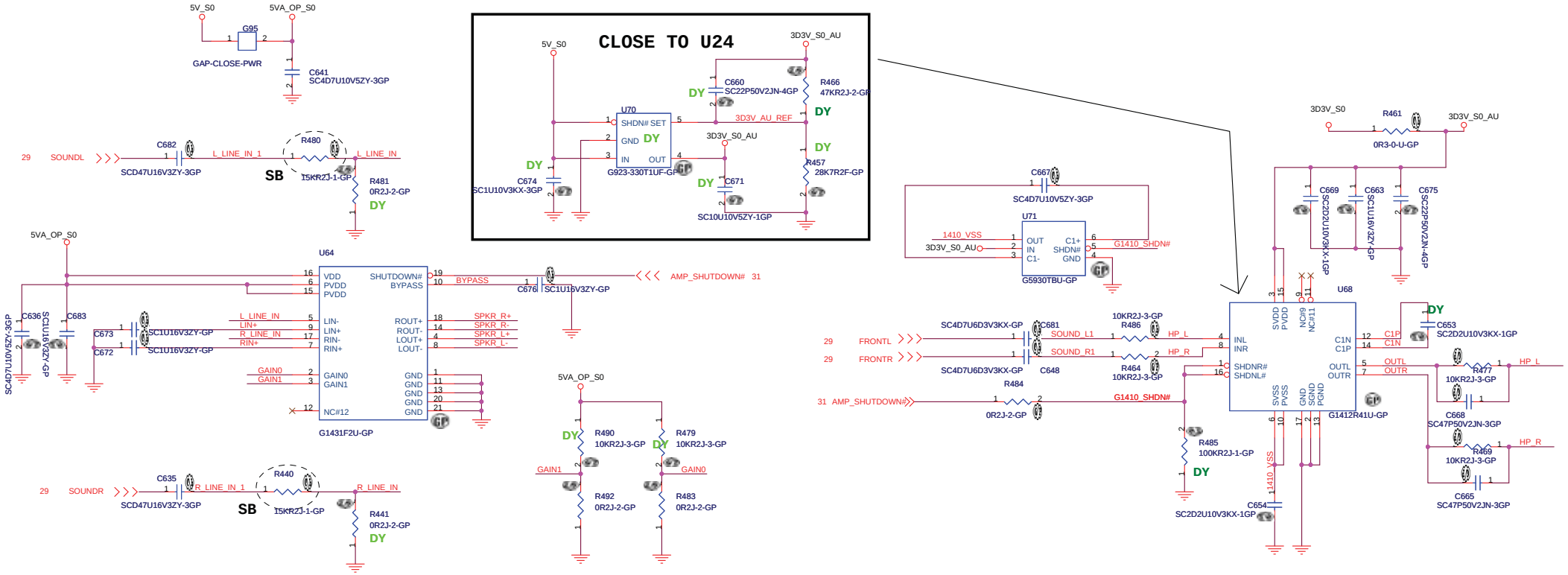
Title: AZALIA CODEC - ALC268

Size	Document Number	Rev
	Orta	SA

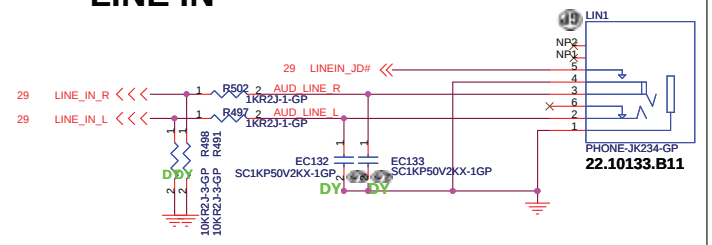
Date: Tuesday, December 12, 2006 Sheet 29 of 46

AUDIO OP AMPLIFIER

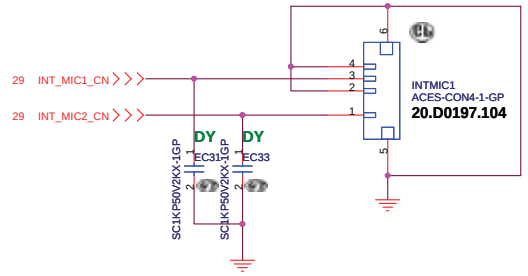
KBC_MUTE_GPIO8



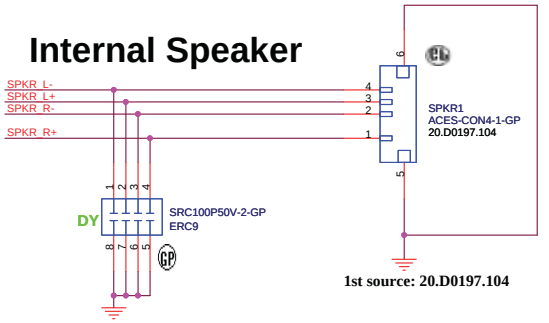
LINE IN



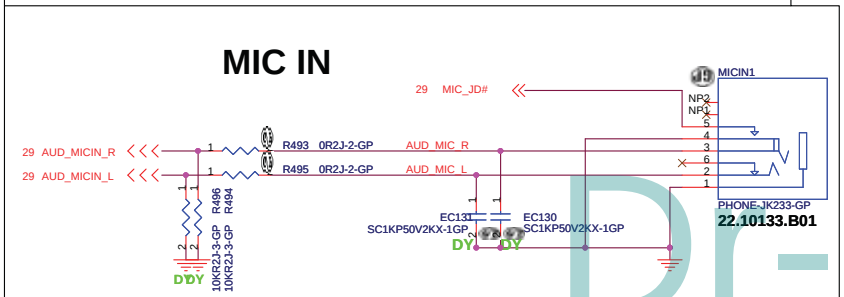
Internal Microphone



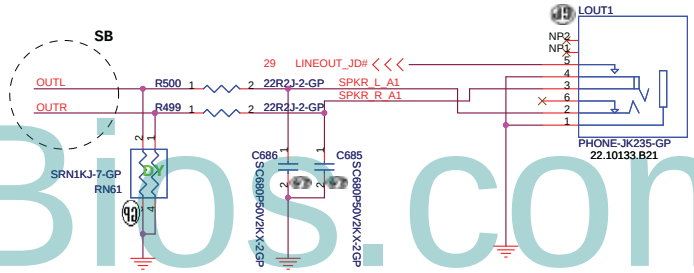
Internal Speaker



MIC IN



LINE OUT



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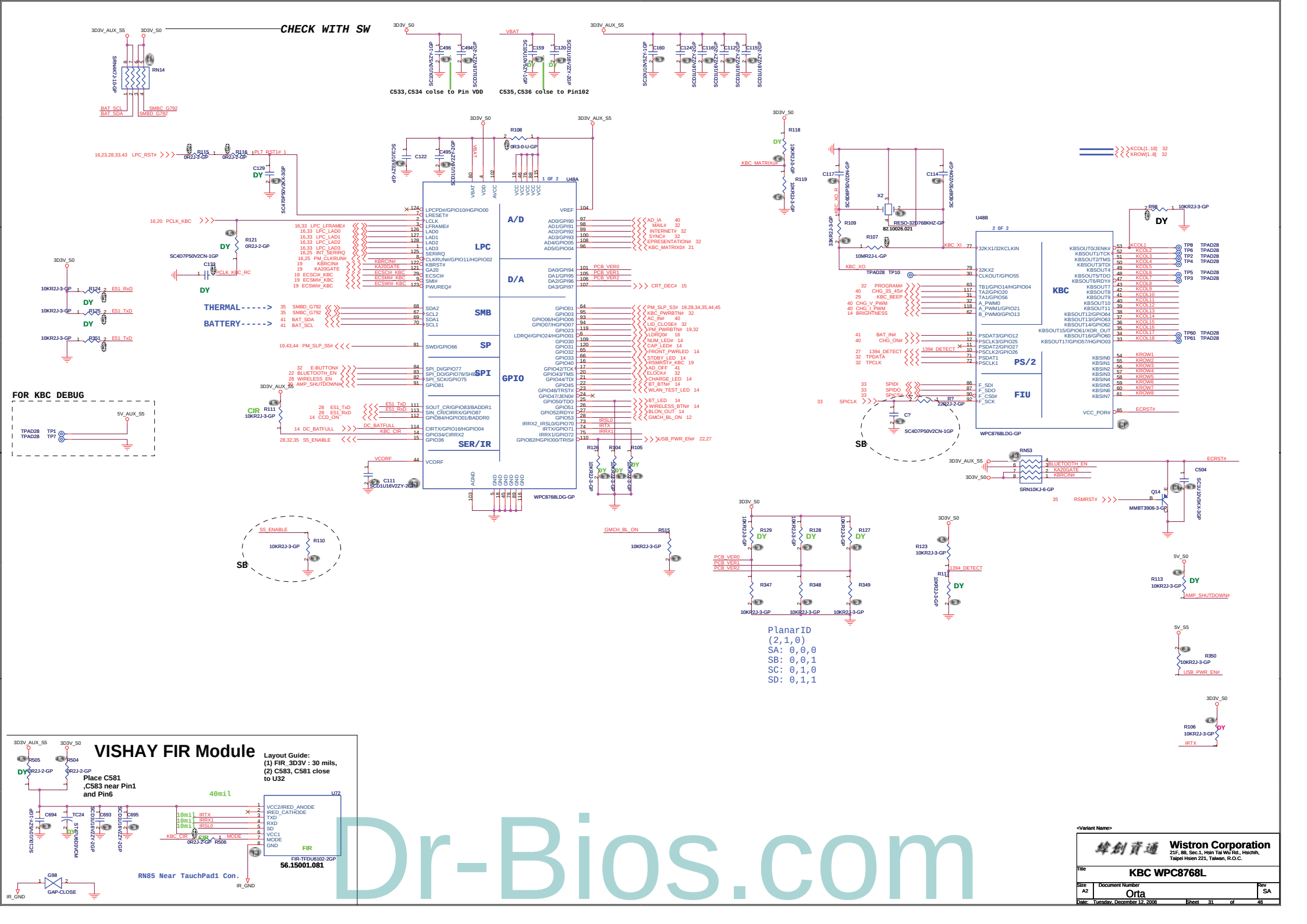
<variant_name>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	AUDIO AMP AND JACK	
Size	Document Number: Orta	Rev: SA
Date: Tuesday, December 12, 2006	Sheet 30 of 46	


CHECK WITH SW
C533,C534 colse to Pin VDD
C535,C536 colse to Pin102
FOR KBC DEBUG
THERMAL----->
BATTERY----->
PlanarID
(2,1,0)
SA: 0,0,0
SB: 0,0,1
SC: 0,1,0
SD: 0,1,1
VISHAY FIR Module
Layout Guide:
(1) FIR_3D3V : 30 mils,
(2) C583, C581 close
to U32
Place C581
,C583 near Pin1
and Pin6
40mil
RN85 Near TauchPad1 Con.
56.15001.081
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC WPC8768L
Orta
Tuesday, December 12, 2006
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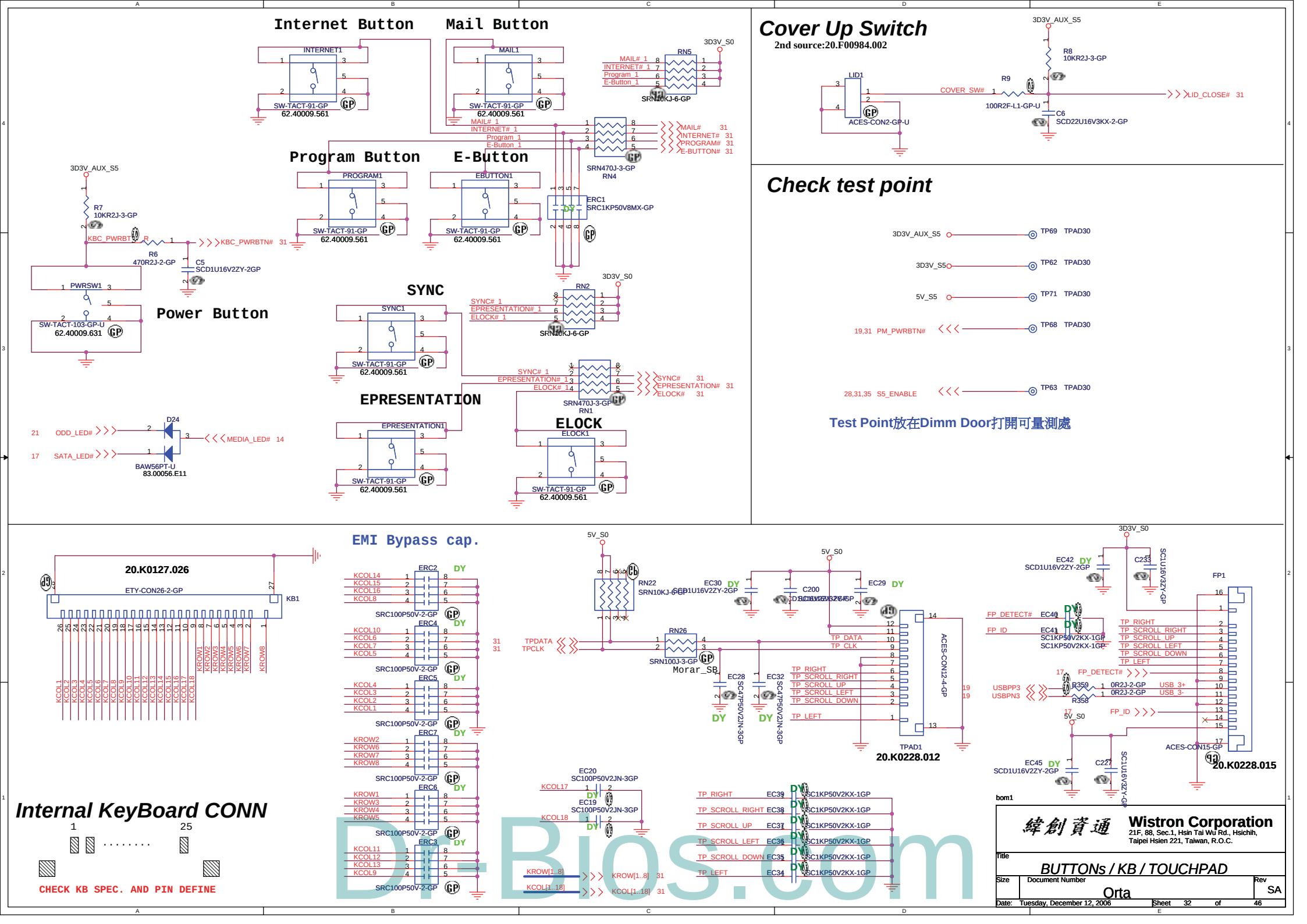
Internet Button
Mail Button
Program Button
E-Button
SYNC
EPRESENTATION
ELOCK
Power Button
Cover Up Switch
2nd source:20.F00984.002
Check test point
Test Point放在Dimm Door打開可量測處
EMI Bypass cap.
Internal KeyBoard CONN
CHECK KB SPEC. AND PIN DEFINE
20.K0127.026
20.K0228.012
20.K0228.015
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
BUTTONs / KB / TOUCHPAD
Orta
Tuesday, December 12, 2006
Sheet 32 of 46
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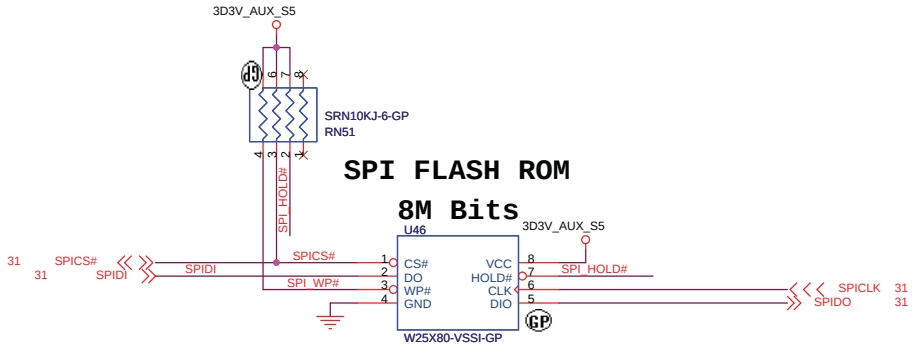
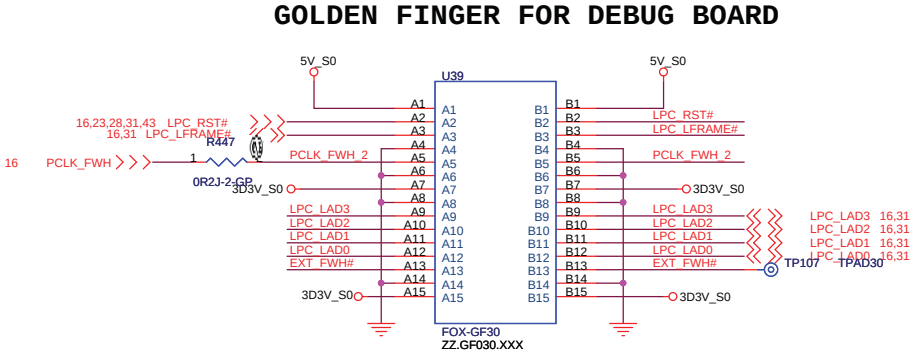


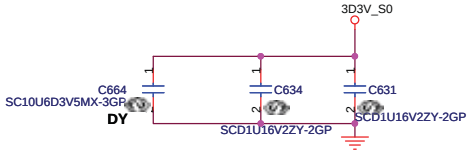


TOP VIEW

A15 (B1)
A14 (B2)
⋮ ⋮
A2 (B14)
A1 (B15)

(BOTTOM VIEW)

```
Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46
```



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<Core Design>

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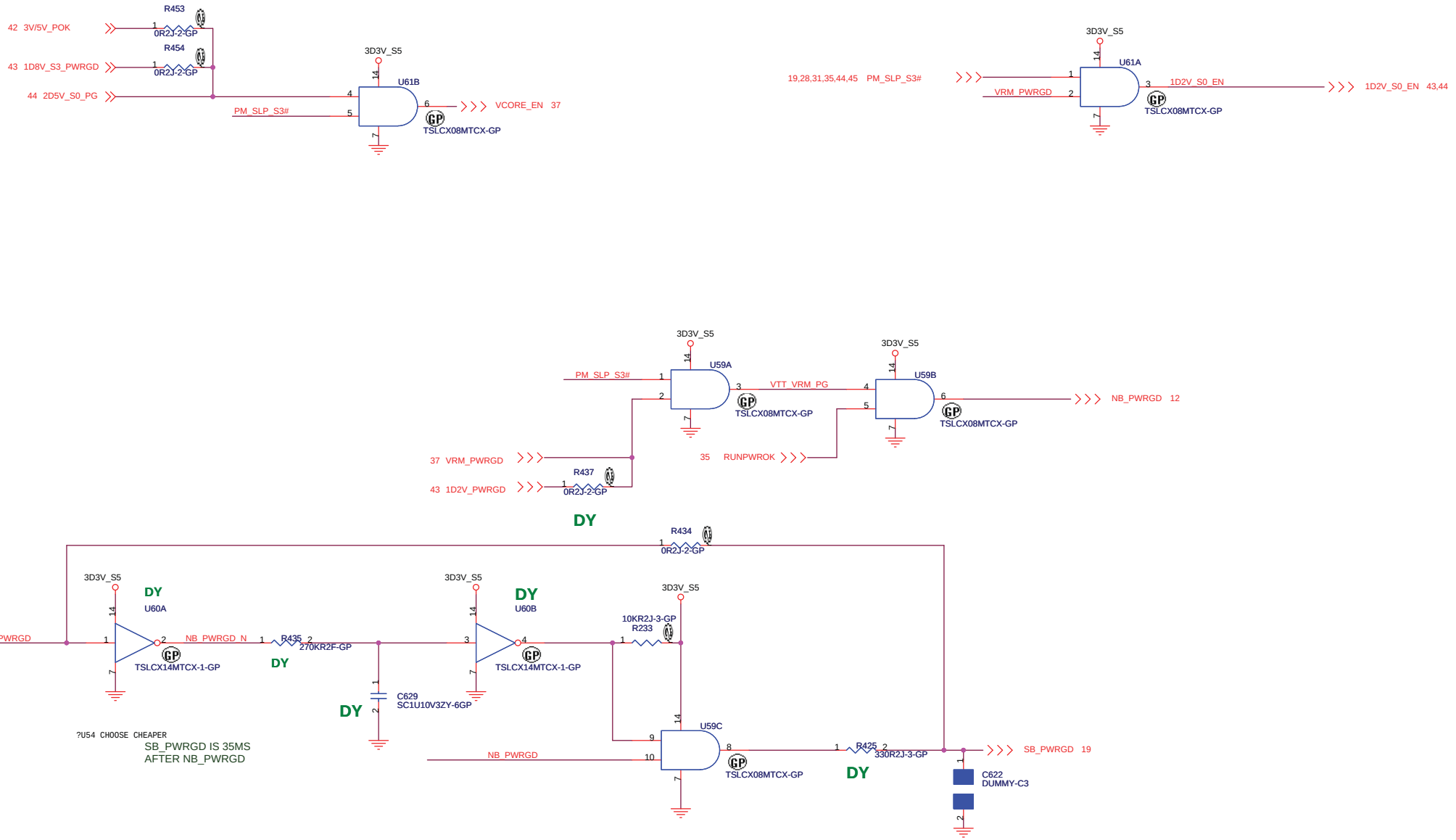
Taipei Hsien 221, Taiwan, R.O.C.

Title: BIOS

Size	Document Number	Rev
A3	Orta	SA

Date: Tuesday, December 12, 2006 Sheet 33 of 46



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<Core Design>

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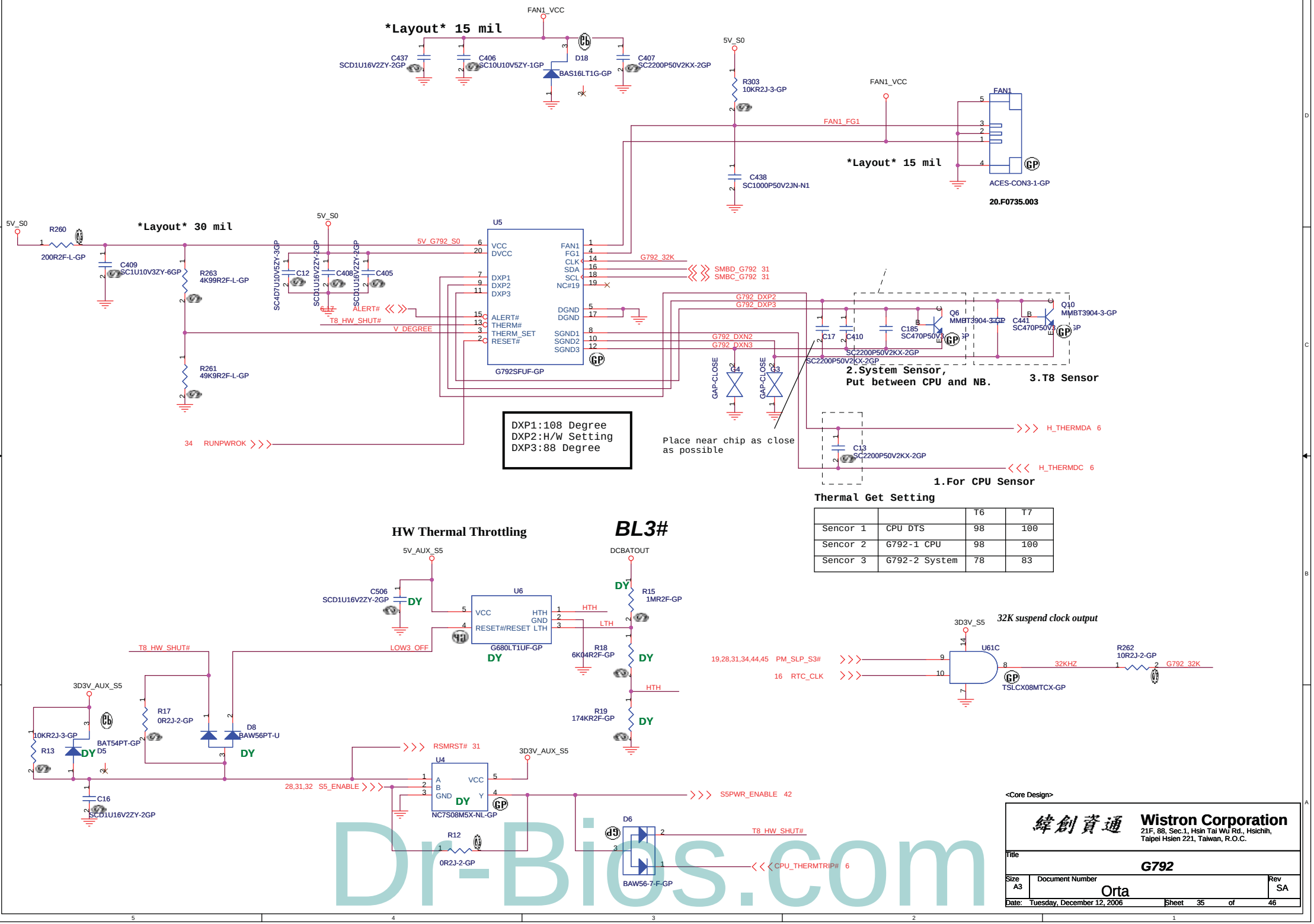
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWERGOOD&ENABLES(1/2)

Size	Document Number	Rev
A3	Orta	SA

Date: Tuesday, December 12, 2006 Sheet 34 of 46



		T6	T7
Sencor 1	CPU DTS	98	100
Sencor 2	G792-1 CPU	98	100
Sencor 3	G792-2 System	78	83

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<Core Design>

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Title: G792

Size: A3 | Document Number: Orta | Rev: SA

Date: Tuesday, December 12, 2006 | Sheet 35 of 46

CPU_CORE
ISL6264CRZ

VID0
VID1
VID2
VID3
VID4
VID5

VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
VID5(I / 3.3V)

Output Signal
VROK()

MAX8760_VRM

Output Power
VCC_CORE_PWR(O)

VCC_CORE_S0(Imax=35A)

VCORE_EN

Input Signal
EN (I / 3.3V)

COREFB
COREFB#

Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)

DCBATOUT
5V_S0
3D3V_S0

Input Power
VCC(I)
VCC(I)
VCC(I)

TI TPS51120
3D3V/5V

DCBATOUT_51120

Input Signal
51120_EN2 FOR 3.3V
51120_EN1 FOR 5.0V
VIN

Output Signal
PGOUT(OD / 5V)

Pull High (3D3V)

Input Power
VIN
REG5V_IN(I / 5V)

Output Power
5V(O)
3D3V(O)

5V_AUX_S5
3D3V_AUX_S5
5V_S5 (5.4A)
3D3V_S5 (4A)

2D5V_S0

3D3V_S0 → INPUT / OUT → 2D5V_S0

APL5913

1D8V_S5

3D3V_S5 → INPUT / OUT → 1D2V_S5

APL5332KAC-TRLGP

Adapter

AD_OFF
AD_JK
5V_AUX_S5

Input Signal
(I)

Output Signal
(O)

AD_IN

Input Power
VCC(I)
VCC(I)

Output Power
VCC(O)

AD+

Charger_ISL6255

CHARGE_OFF
BT_TH
BAT+SENSE
BT_SCL_5
BT_SDA_5
FLASH_GPIO1
FLASH_GPIO2
AC_IN

Input Signal
CLS (I / 3.3V)
THM (I / 3.3V)
BATT (I / 3.3V)
SCL (IO / 5V)
SDA (IO / 5V)
RESET#/PB5 (I/5V)
PB0/MOSI/AIN0
PB0/MOSI/AIN0

Output Signal
LDO (O / 5.4V)
XTAL2/PB4 (O/5V)
XTAL1/PB3 (O/5V)

AD_IN
CHARGE_LED#
BL2#

Output Power
VCC (O)
VCC (O)

DCBATOUT
BT+

Input Power
DCIN (I)

AD+

TI TPS51116
1.8V / 0.9V

PM_SLP_S5#

Input Signal
S5
S3

Output Signal
PGOOD(OD / 3.3V)

1D8V_S3_PG

Input Power
VCC(I)
VCC(I)

Output Power
VCC(O)
VCC(O)

1.8V_S3
0.9V_S3

DCBATOUT
5V_S5

ISL6268_1D2V

1D2V_S0_EN
5V_S5
DCBATOUT

Input Signal
SS_STBY1(I / 5V) FOR 1.2V

Input Power
VCC
VIN

Output Power
1D2V_PWR

1D2V (6.5A)

ISL6268_VGA_CORE

VGA_CORE_EN
5V_S5
DCBATOUT

Input Signal
SS_STBY1(I / 5V) FOR 1.2V

Input Power
VCC
VIN

Output Power
1D2V_PWR

VGA_CORE_S0 (15A)

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Title: **Power Block Diagram**

Size: A3 | Document Number: Orta | Rev: SA

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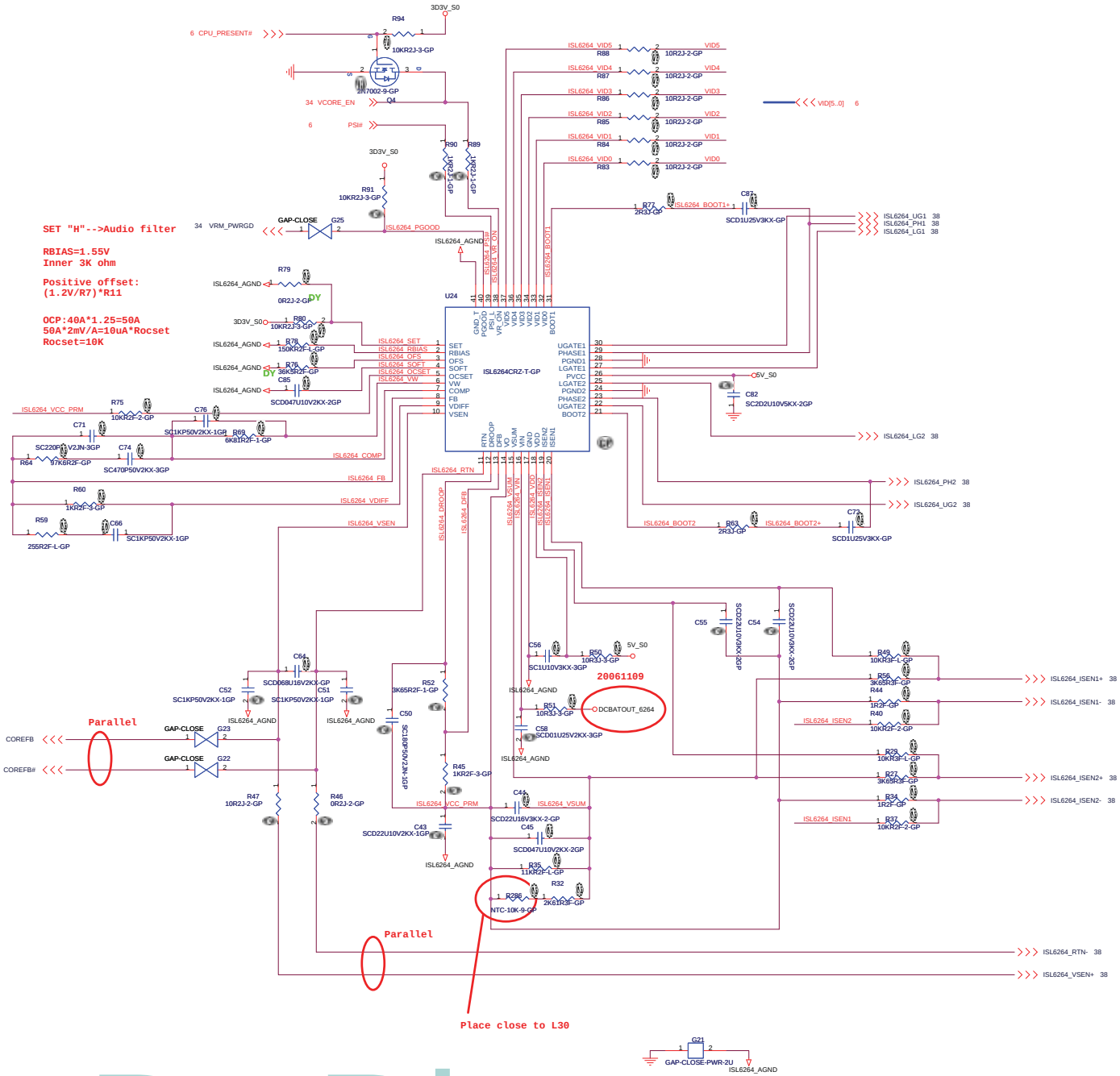
CPU_VCORE
VID=1.20V(25W)/1.15V(35W)
Iomax=21A(25W)/35A (35W)
OCP=40A~45A

TABLE 1. VOLTAGE IDENTIFICATION CODES

VID5	VID4	VID3	VID2	VID1	VID0	DAC
0	0	0	0	0	0	1.550
0	0	0	0	0	1	1.525
0	0	0	0	1	0	1.500
0	0	0	0	1	1	1.475
0	0	0	1	0	0	1.450
0	0	0	1	0	1	1.425
0	0	0	1	1	0	1.400
0	0	0	1	1	1	1.375
0	0	1	0	0	0	1.350
0	0	1	0	0	1	1.325
0	0	1	0	1	0	1.300
0	0	1	0	1	1	1.275
0	0	1	1	0	0	1.250
0	0	1	1	0	1	1.225
0	0	1	1	1	0	1.200
0	0	1	1	1	1	1.175
0	1	0	0	0	0	1.150
0	1	0	0	0	1	1.125
0	1	0	0	1	0	1.100
0	1	0	0	1	1	1.075
0	1	0	1	0	0	1.050
0	1	0	1	0	1	1.025
0	1	0	1	1	0	1.000
0	1	0	1	1	1	0.975
0	1	1	0	0	0	0.950
0	1	1	0	0	1	0.925
0	1	1	0	1	0	0.900
0	1	1	0	1	1	0.875
0	1	1	1	0	0	0.850
0	1	1	1	0	1	0.825
0	1	1	1	1	0	0.800
0	1	1	1	1	1	0.775
1	0	0	0	0	0	0.7625
1	0	0	0	0	1	0.75
1	0	0	0	1	0	0.7375
1	0	0	0	1	1	0.725
1	0	0	1	0	0	0.7125
1	0	0	1	0	1	0.7
1	1	1	1	1	1	0.375



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<Core Design>

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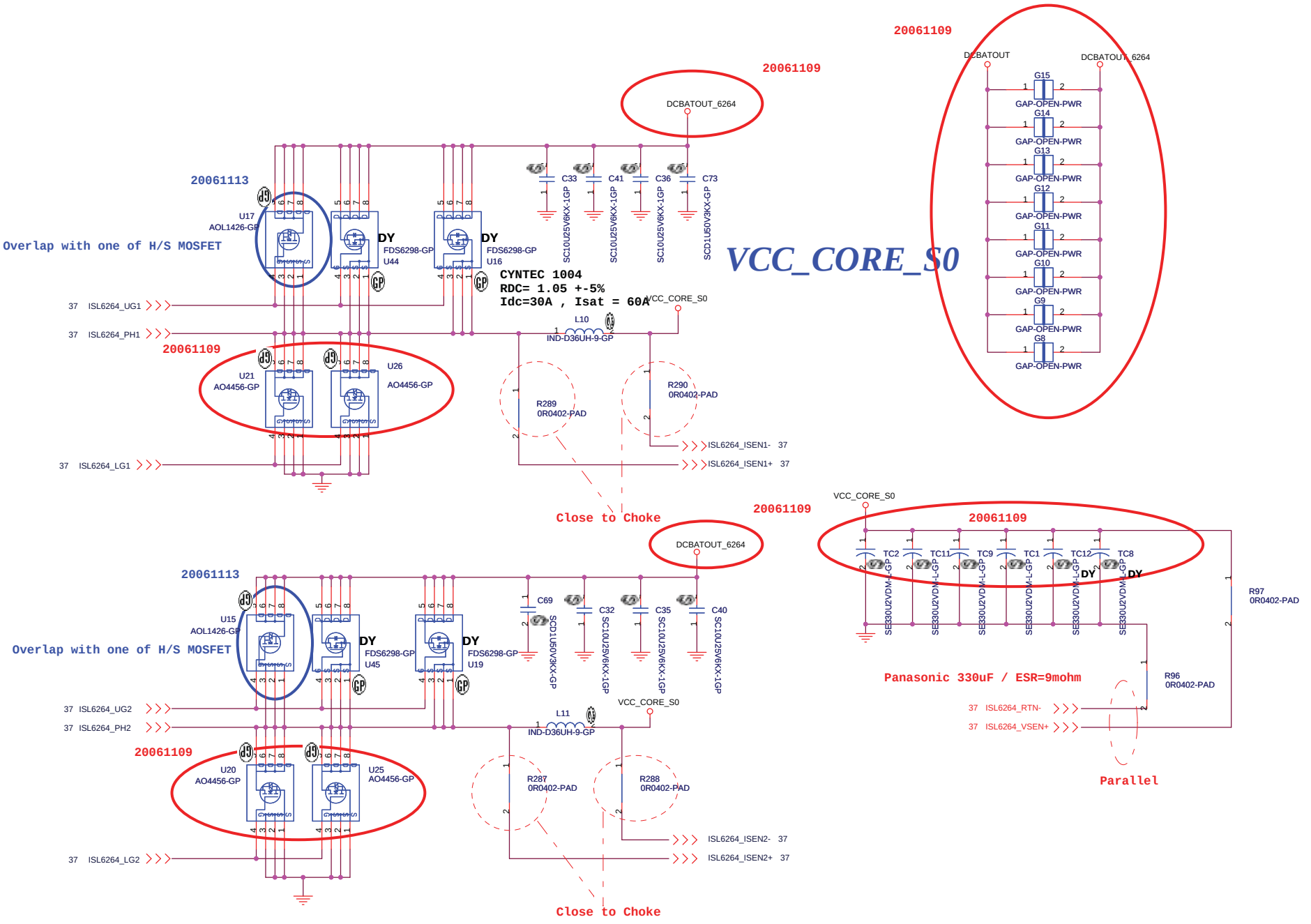
Title: CPU Vcore Power_1

Size: A2 | Document Number: Orta | Rev: SA

Date: Tuesday, December 12, 2006 | Sheet 37 of 46



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<Core Design>

Wistron Corporation
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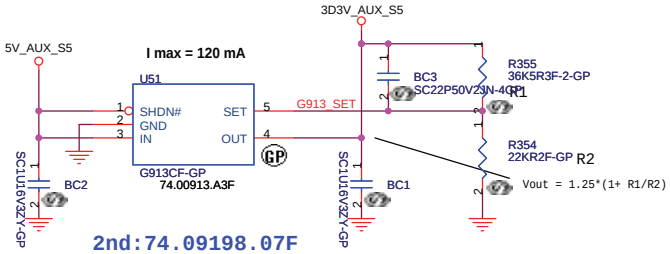
Title: CPU Vcore Power_2

Size: A3 | Document Number: Orta | Rev: SA

Date: Tuesday, December 12, 2006 | Sheet 38 of 46

Aux Power

3D3V_AUX_S5



2nd:74.09198.07F
(RT9198-33PBG)

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<Core Design>

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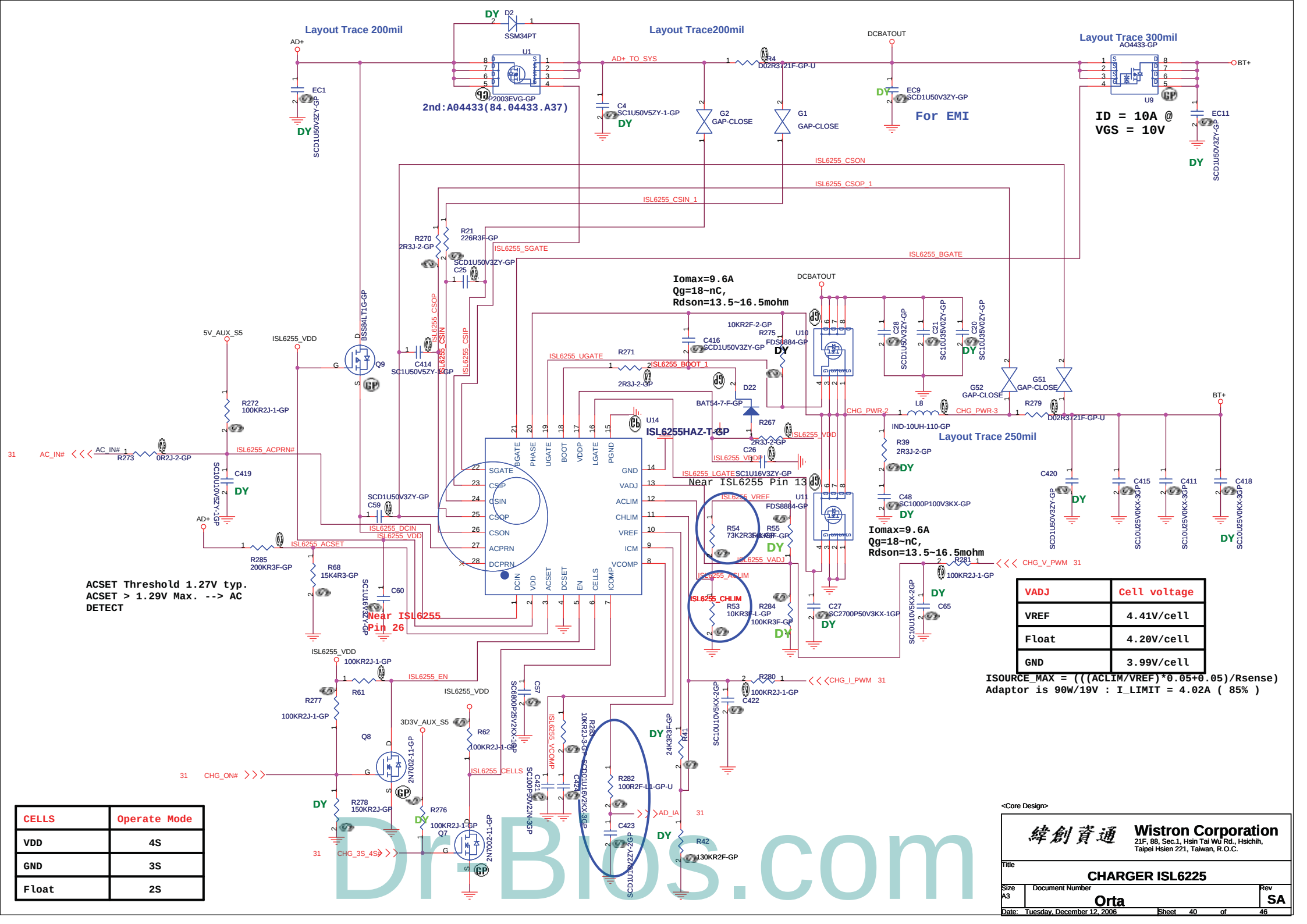
Title: ***3D3V_AUX***

Size	Document Number	Rev
A3	Orta	SA

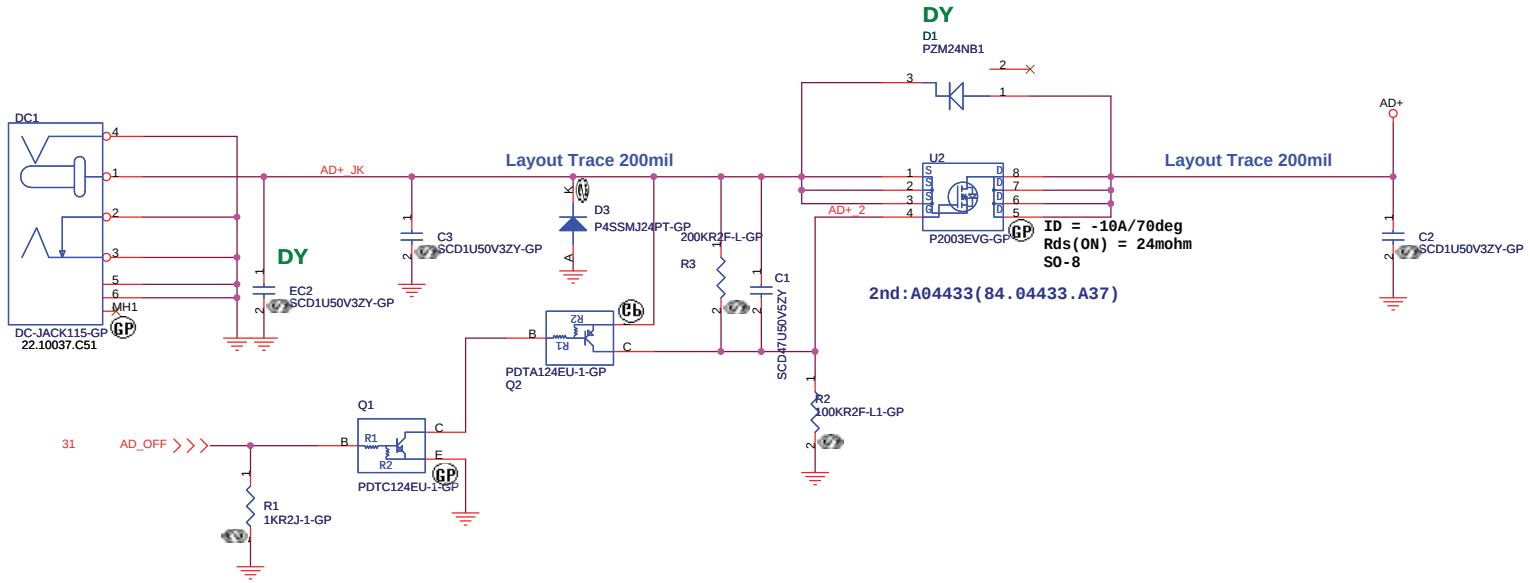
Date: Tuesday, December 12, 2006 Sheet 39 of 46



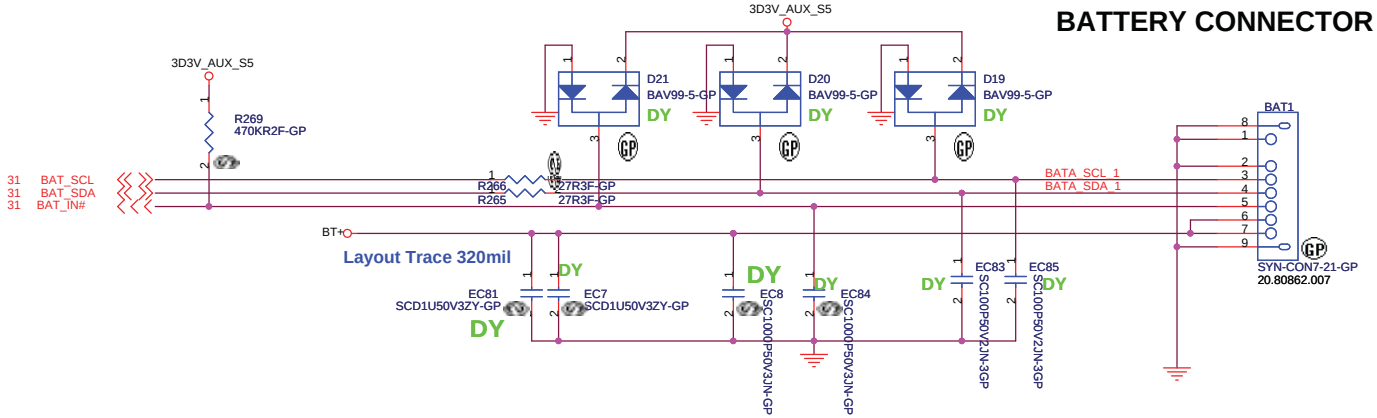
VADJ	Cell voltage
VREF	4.41V/cell
Float	4.20V/cell
GND	3.99V/cell

CELLS	Operate Mode
VDD	4S
GND	3S
Float	2S

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



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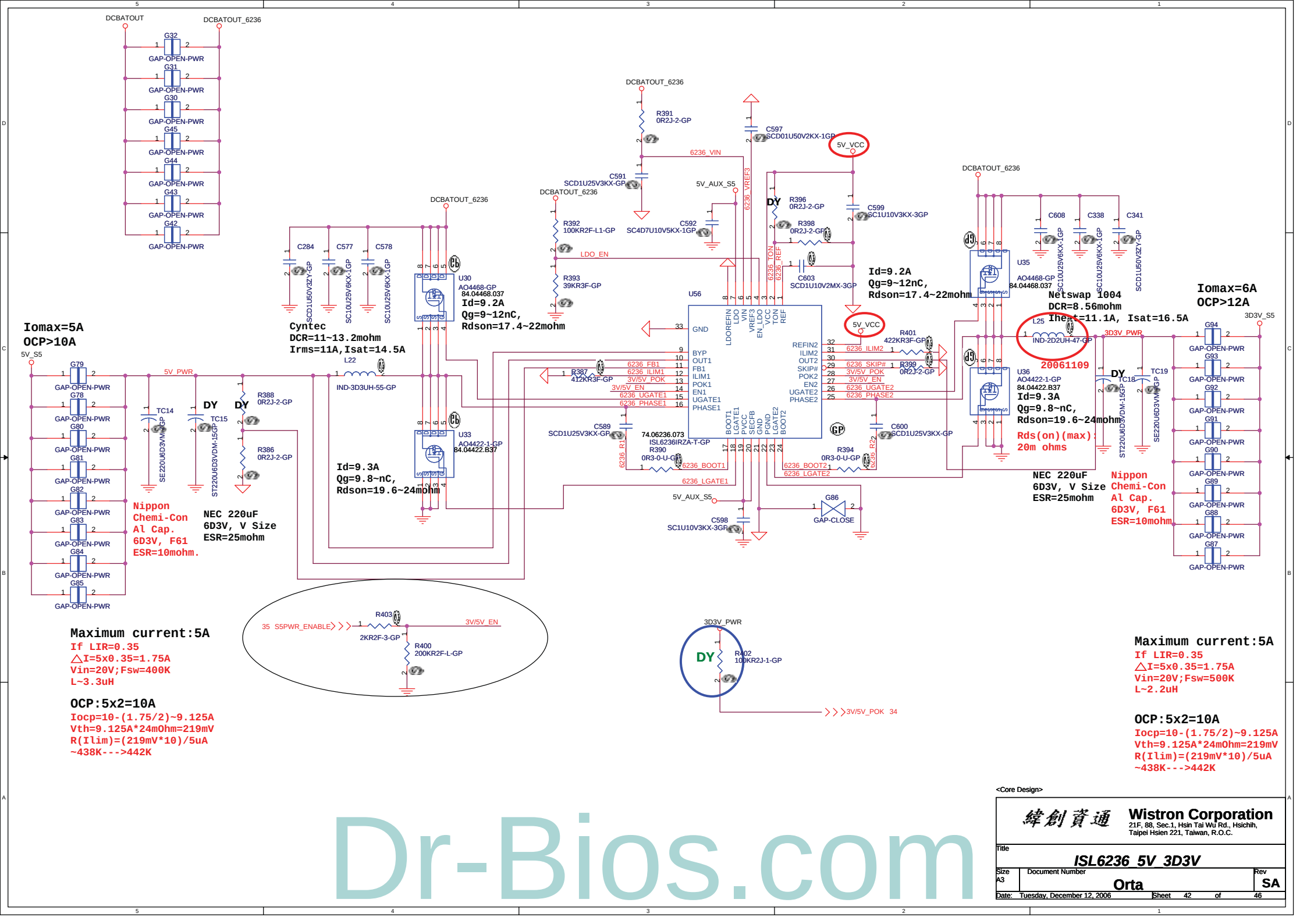
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AD/BATT CONN**

Size: A3 | Document Number: **Orta** | Rev: **SA**

Date: Tuesday, December 12, 2006 | Sheet 41 of 46


DCBATOUT
DCBATOUT_6236
G32 GAP-OPEN-PWR
G31 GAP-OPEN-PWR
G30 GAP-OPEN-PWR
G45 GAP-OPEN-PWR
G44 GAP-OPEN-PWR
G43 GAP-OPEN-PWR
G42 GAP-OPEN-PWR
Iomax=5A
OCP>10A
5V_S5
G79 GAP-OPEN-PWR
G78 GAP-OPEN-PWR
G80 GAP-OPEN-PWR
G81 GAP-OPEN-PWR
G82 GAP-OPEN-PWR
G83 GAP-OPEN-PWR
G84 GAP-OPEN-PWR
G85 GAP-OPEN-PWR
5V_PWR
TC14 SE220U6D3VM-GP
TC15 ST220U6D3VDM-15GP
DY
R388 0R2J-2-GP
R386 0R2J-2-GP
Nippon Chemi-Con Al Cap. 6D3V, F61 ESR=10mohm.
NEC 220uF 6D3V, V Size ESR=25mohm
L22
IND-3D3UH-55-GP
Cyntec DCR=11~13.2mohm Irms=11A,Isat=14.5A
C284 SCD1U50V3ZY-GP
C577 SC10U25V6KX-1GP
C578 SC10U25V6KX-1GP
U30 AO4468-GP 84.04468.037
Id=9.2A Qg=9~12nC, Rdson=17.4~22mohm
U33 AO4422-1-GP 84.04422.B37
Id=9.3A Qg=9.8~nC, Rdson=19.6~24mohm
R391 0R2J-2-GP
C591 SCD1U25V3KX-GP
R392 100KR2F-L1-GP
R393 39KR3F-GP
LDO_EN
C592 SC4D7U10V5KX-1GP
6236_VIN
C597 SCD01U50V2KX-1GP
5V_VCC
5V_AUX_S5
6236_VREF3
R396 0R2J-2-GP
R398 0R2J-2-GP
C599 SC1U10V3KX-3GP
C603 SCD1U10V2MX-3GP
6236_TON
6236_REF
U56
GND
LDOREFIN LDO VIN VREF3 EN_LDO VCC TON REF
BYP OUT1 FB1 ILIM1 POK1 EN1 UGATE1 PHASE1
REFIN2 ILIM2 OUT2 SKIP# POK2 EN2 UGATE2 PHASE2
BOOT1 LGATE1 PVCC SECFB GND PGND LGATE2 BOOT2
74.06236.073 ISL6236IRZA-T-GP
6236_FB1 6236_ILIM1 3V/5V_POK 3V/5V_EN 6236_UGATE1 6236_PHASE1
6236_SKIP# 6236_UGATE2 6236_PHASE2
R387 412KR3F-GP
R390 0R3-0-U-GP
R394 0R3-0-U-GP
R401 422KR3F-GP
R399 0R2J-2-GP
C589 SCD1U25V3KX-GP
C600 SCD1U25V3KX-GP
C598 SC1U10V3KX-3GP
6236_BOOT1
6236_LGATE1
6236_BOOT2
6236_LGATE2
G86 GAP-CLOSE
Id=9.2A Qg=9~12nC, Rdson=17.4~22mohm
Netswap 1004 DCR=8.56mohm Iheat=11.1A, Isat=16.5A
L25 IND-2D2UH-47-GP
20061109
U35 AO4468-GP 84.04468.037
C608 SC10U25V6KX-1GP
C338 SC10U25V6KX-1GP
C341 SCD1U50V3ZY-GP
U36 AO4422-1-GP 84.04422.B37
Id=9.3A Qg=9.8~nC, Rdson=19.6~24mohm
Rds(on)(max): 20m ohms
TC18 ST220U6D3VDM-15GP
TC19 SE220U6D3VM-GP
NEC 220uF 6D3V, V Size ESR=25mohm
Nippon Chemi-Con Al Cap. 6D3V, F61 ESR=10mohm
Iomax=6A
OCP>12A
3D3V_S5
3D3V_PWR
G94 G93 G92 G91 G90 G89 G88 G87 GAP-OPEN-PWR
35 S5PWR_ENABLE
R403 2KR2F-3-GP
R400 200KR2F-L-GP
3V/5V_EN
3D3V_PWR
R402 100KR2J-1-GP
3V/5V_POK 34
Maximum current:5A
If LIR=0.35
△I=5x0.35=1.75A
Vin=20V;Fsw=400K
L~3.3uH
OCP:5x2=10A
Iocp=10-(1.75/2)~9.125A
Vth=9.125A*24mOhm=219mV
R(Ilim)=(219mV*10)/5uA
~438K--->442K
Maximum current:5A
If LIR=0.35
△I=5x0.35=1.75A
Vin=20V;Fsw=500K
L~2.2uH
OCP:5x2=10A
Iocp=10-(1.75/2)~9.125A
Vth=9.125A*24mOhm=219mV
R(Ilim)=(219mV*10)/5uA
~438K--->442K
<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL6236_5V_3D3V
Size A3
Document Number
Orta
Rev SA
Date: Tuesday, December 12, 2006
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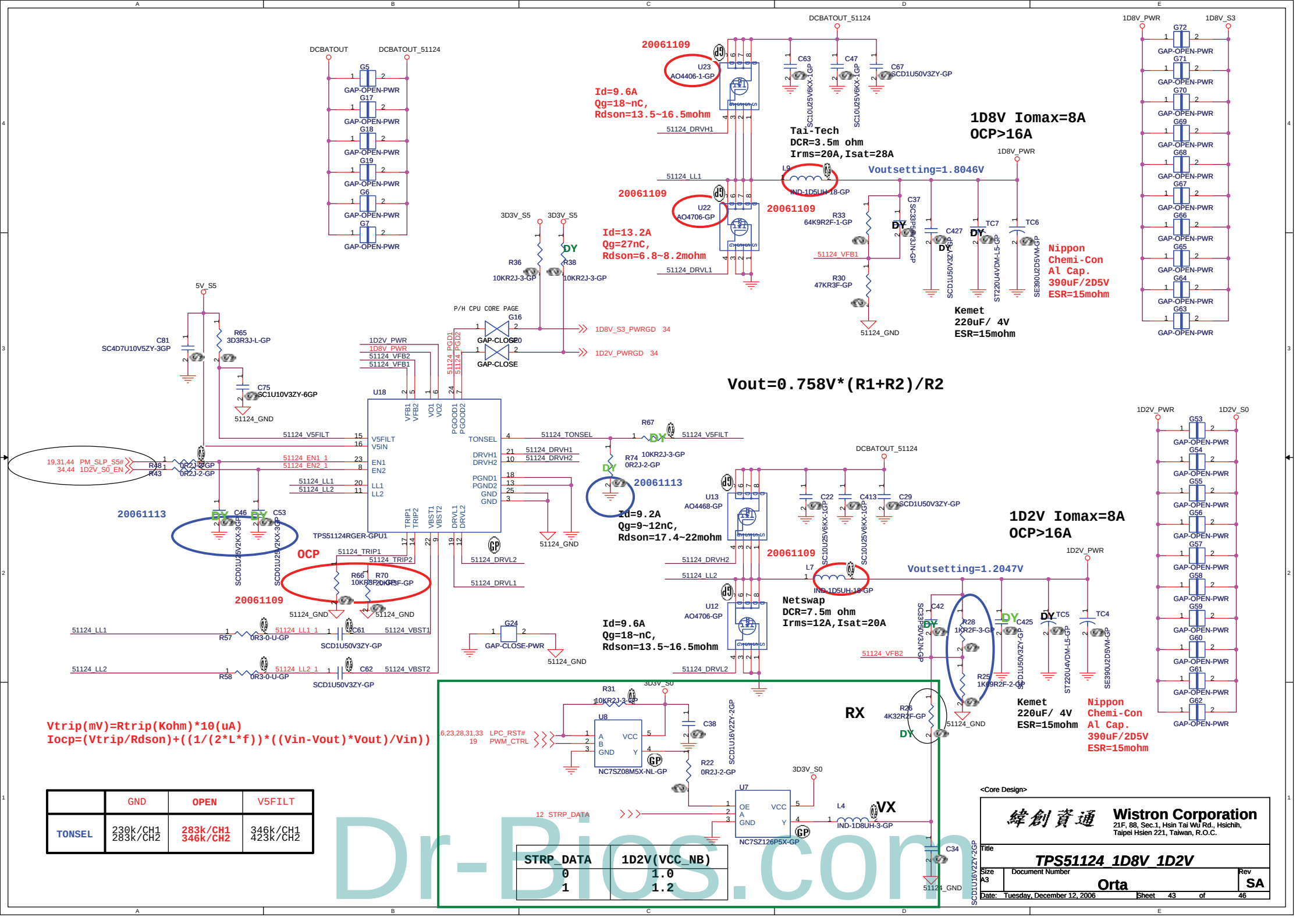
DCBATOUT
DCBATOUT_51124
GAP-OPEN-PWR
20061109
U23
AO4406-1-GP
Id=9.6A
Qg=18~nC,
Rdson=13.5~16.5mohm
51124_DRVH1
Tai-Tech
DCR=3.5m ohm
Irms=20A,Isat=28A
1D8V Iomax=8A
OCP>16A
51124_LL1
L9
IND-1D5UH-18-GP
Voutsetting=1.8046V
1D8V_PWR
20061109
U22
AO4706-GP
Id=13.2A
Qg=27nC,
Rdson=6.8~8.2mohm
51124_DRVL1
R33
64K9R2F-1-GP
51124_VFB1
R30
47KR3F-GP
51124_GND
Kemet
220uF/ 4V
ESR=15mohm
Nippon
Chemi-Con
Al Cap.
390uF/2D5V
ESR=15mohm
3D3V_S5
R36
10KR2J-3-GP
R38
10KR2J-3-GP
P/H CPU CORE PAGE
GAP-CLOSE
1D8V_S3_PWRGD 34
1D2V_PWRGD 34
5V_S5
R65
3D3R3J-L-GP
C81
SC4D7U10V5ZY-3GP
C75
SC1U10V3ZY-6GP
Vout=0.758V*(R1+R2)/R2
U18
TPS51124RGER-GPU1
51124_V5FILT
51124_TONSEL
R67
R74
10KR2J-3-GP
0R2J-2-GP
19,31,44 PM_SLP_S5#
34,44 1D2V_S0_EN
R48
R43
0R2J-2-GP
51124_EN1_1
51124_EN2_1
51124_LL1
51124_LL2
20061113
C46
C53
SCD01U25V2KX-3GP
OCP
51124_TRIP1
51124_TRIP2
R66
R70
10KR3F-GP
20061109
51124_VBST1
51124_VBST2
R57
R58
0R3-0-U-GP
SCD1U50V3ZY-GP
C61
C62
G24
GAP-CLOSE-PWR
20061113
Id=9.2A
Qg=9~12nC,
Rdson=17.4~22mohm
U13
AO4468-GP
20061109
U12
AO4706-GP
Id=9.6A
Qg=18~nC,
Rdson=13.5~16.5mohm
1D2V Iomax=8A
OCP>16A
Voutsetting=1.2047V
L7
IND-1D5UH-18-GP
Netswap
DCR=7.5m ohm
Irms=12A,Isat=20A
51124_VFB2
R28
1K02F-3-GP
R25
1K09R2F-2-GP
Kemet
220uF/ 4V
ESR=15mohm
Nippon
Chemi-Con
Al Cap.
390uF/2D5V
ESR=15mohm
RX
R26
4K32R2F-GP
VX
L4
IND-1D8UH-3-GP
R31
10KR2J-3-GP
U8
NC7SZ08M5X-NL-GP
C38
R22
0R2J-2-GP
U7
NC7SZ126P5X-GP
6,23,28,31,33 LPC_RST#
19 PWM_CTRL
12 STRP_DATA
3D3V_S0
C34
Vtrip(mV)=Rtrip(Kohm)*10(uA)
Iocp=(Vtrip/Rdson)+((1/(2*L*f))*((Vin-Vout)*Vout)/Vin))
TONSEL
GND
OPEN
V5FILT
230k/CH1
283k/CH2
283k/CH1
346k/CH2
346k/CH1
423k/CH2
STRP_DATA
1D2V(VCC_NB)
0
1.0
1
1.2
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<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
TPS51124_1D8V_1D2V
Size
A3
Document Number
Orta
Rev
SA
Date: Tuesday, December 12, 2006
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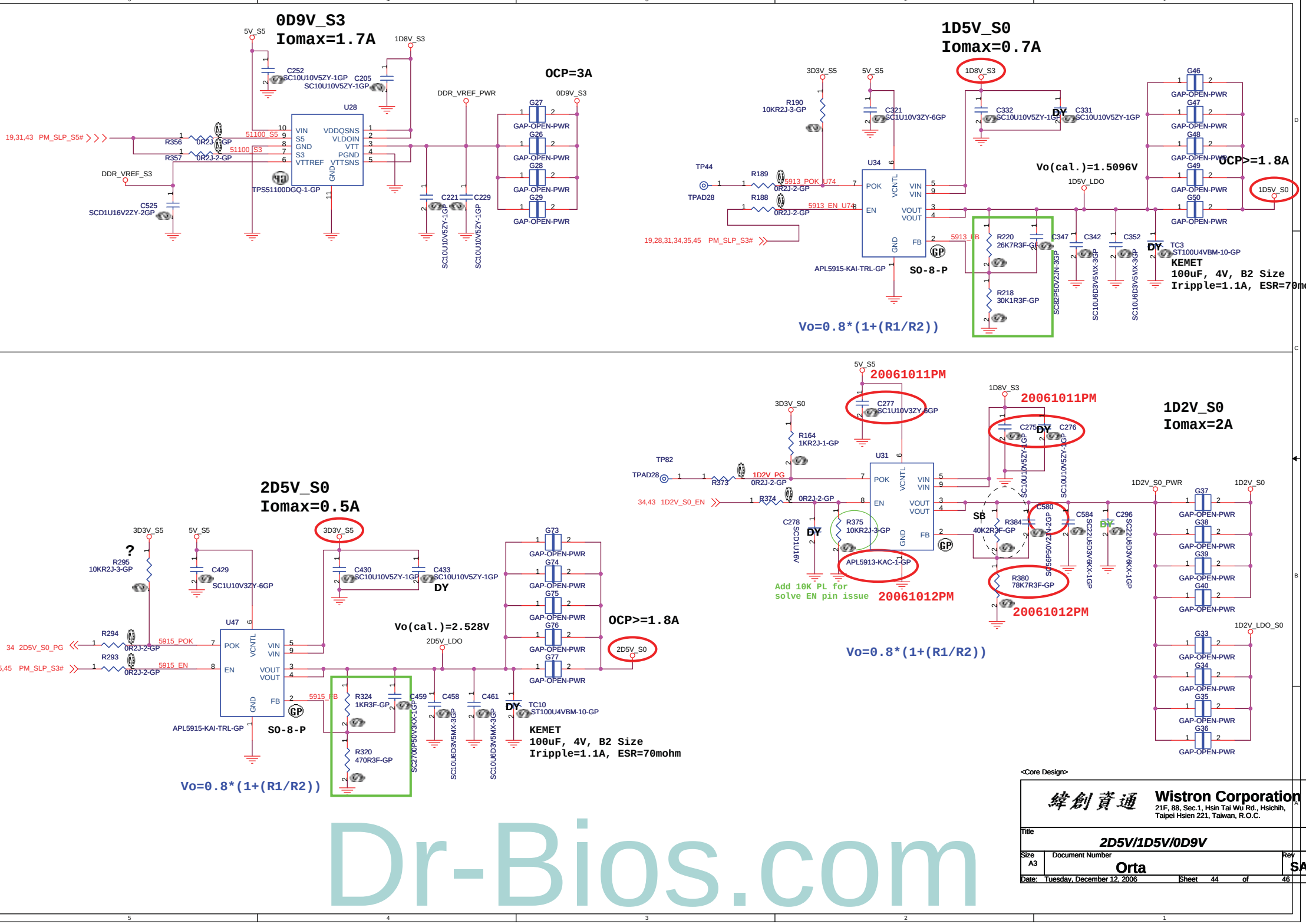
0D9V_S3
Iomax=1.7A
OCP=3A
5V_S5
1D8V_S3
C252
SC10U10V5ZY-1GP
C205
SC10U10V5ZY-1GP
U28
DDR_VREF_PWR
0D9V_S3
19,31,43 PM_SLP_S5#
R356
0R2J-1-GP
R357
0R2J-2-GP
51100_S5
51100_S3
VIN
S5
GND
S3
VTTREF
VDDQSNS
VLDOIN
VTT
PGND
VTTSNS
GND
DDR_VREF_S3
TPS51100DGQ-1-GP
C525
SCD1U16V2ZY-2GP
C221
C229
SC10U10V5ZY-1GP
SC10U10V5ZY-1GP
G27
G26
G28
G29
GAP-OPEN-PWR
1D5V_S0
Iomax=0.7A
3D3V_S5
5V_S5
1D8V_S3
R190
10KR2J-3-GP
C321
SC1U10V3ZY-6GP
C332
SC10U10V5ZY-1GP
DY
C331
SC10U10V5ZY-1GP
G46
G47
G48
G49
G50
GAP-OPEN-PWR
Vo(cal.)=1.5096V
OCP>=1.8A
1D5V_S0
TP44
TPAD28
R189
0R2J-2-GP
R188
0R2J-2-GP
5913_POK_U74
5913_EN_U74
U34
POK
EN
VCNTL
VIN
VOUT
GND
FB
19,28,31,34,35,45 PM_SLP_S3#
APL5915-KAI-TRL-GP
SO-8-P
5913_FB
R220
26K7R3F-GP
R218
30K1R3F-GP
SC82P50V2JN-3GP
1D5V_LDO
C347
C342
C352
SC10U6D3V5MX-3GP
SC10U6D3V5MX-3GP
TC3
ST100U4VBM-10-GP
KEMET
100uF, 4V, B2 Size
Iripple=1.1A, ESR=70moh
Vo=0.8*(1+(R1/R2))
2D5V_S0
Iomax=0.5A
3D3V_S5
5V_S5
3D3V_S5
R295
10KR2J-3-GP
C429
SC1U10V3ZY-6GP
C430
SC10U10V5ZY-1GP
C433
SC10U10V5ZY-1GP
DY
G73
G74
G75
G76
G77
GAP-OPEN-PWR
Vo(cal.)=2.528V
OCP>=1.8A
2D5V_S0
2D5V_LDO
U47
R294
0R2J-2-GP
R293
0R2J-2-GP
34 2D5V_S0_PG
35,45 PM_SLP_S3#
5915_POK
5915_EN
POK
EN
VCNTL
VIN
VOUT
GND
FB
APL5915-KAI-TRL-GP
SO-8-P
5915_FB
R324
1KR3F-GP
R320
470R3F-GP
C459
C458
C461
SC2700P50V3KX-1GP
SC10U6D3V5MX-3GP
SC10U6D3V5MX-3GP
TC10
ST100U4VBM-10-GP
KEMET
100uF, 4V, B2 Size
Iripple=1.1A, ESR=70mohm
Vo=0.8*(1+(R1/R2))
1D2V_S0
Iomax=2A
5V_S5
20061011PM
3D3V_S0
C277
SC1U10V3ZY-6GP
1D8V_S3
20061011PM
C275
DY
C276
SC10U10V5ZY-1GP
R164
1KR2J-1-GP
U31
TP82
TPAD28
R373
1D2V_PG
0R2J-2-GP
34,43 1D2V_S0_EN
R374
0R2J-2-GP
C278
SCD1U16V
DY
R375
10KR2J-3-GP
APL5913-KAC-1-GP
Add 10K PL for
solve EN pin issue
20061012PM
POK
EN
VCNTL
VIN
VOUT
GND
FB
SB
R384
40K2R3F-GP
C580
SC82P50V2JN-2GP
C584
SC22U6D3V6KX-1GP
DY
C296
SC22U6D3V6KX-1GP
R380
78K7R3F-GP
20061012PM
1D2V_S0_PWR
1D2V_S0
1D2V_LDO_S0
G37
G38
G39
G40
G33
G34
G35
G36
GAP-OPEN-PWR
Vo=0.8*(1+(R1/R2))
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
2D5V/1D5V/0D9V
Size
A3
Document Number
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Date: Tuesday, December 12, 2006
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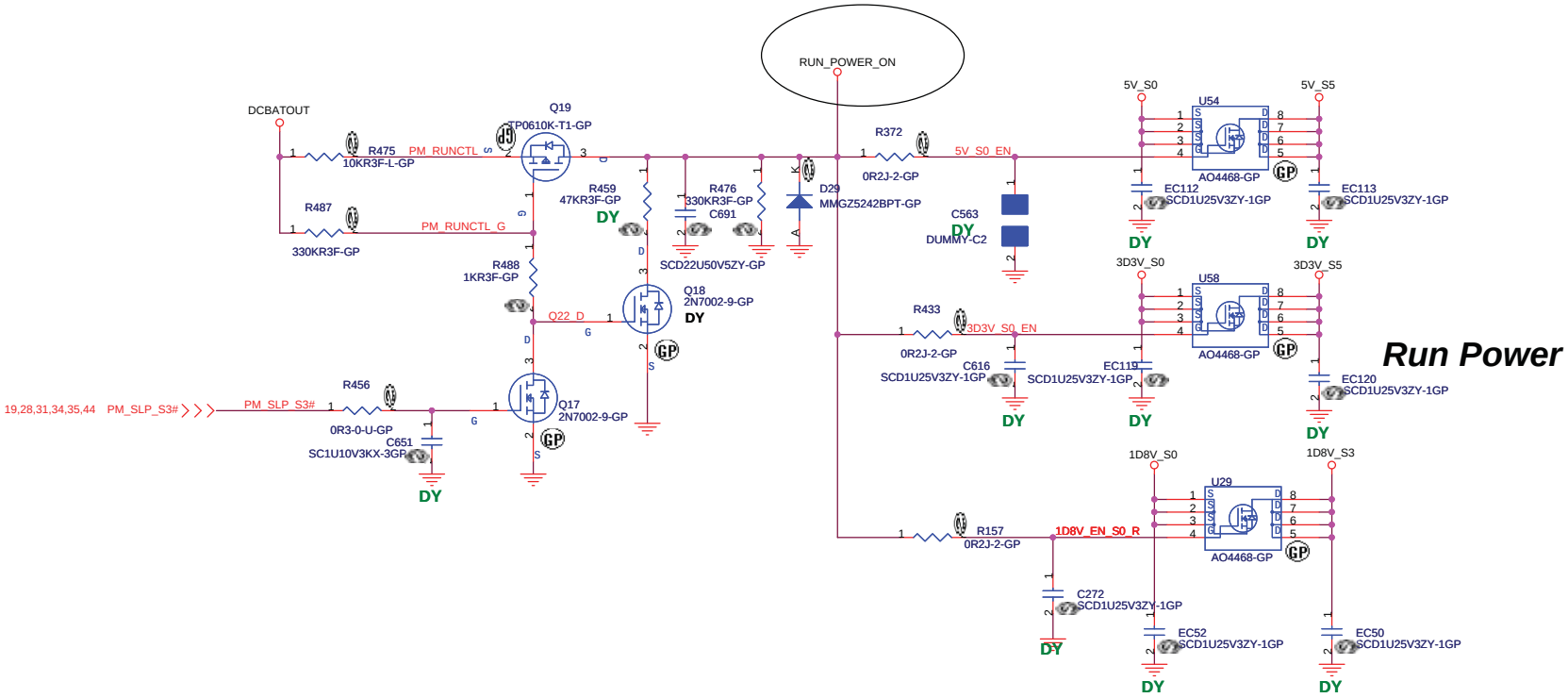
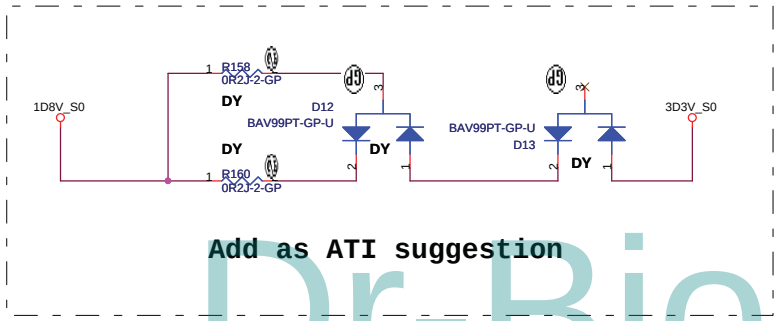


Run Power



Add as ATI suggestion

Power On Logic

<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **PWR CTL LOGIC / PWR PLANE**

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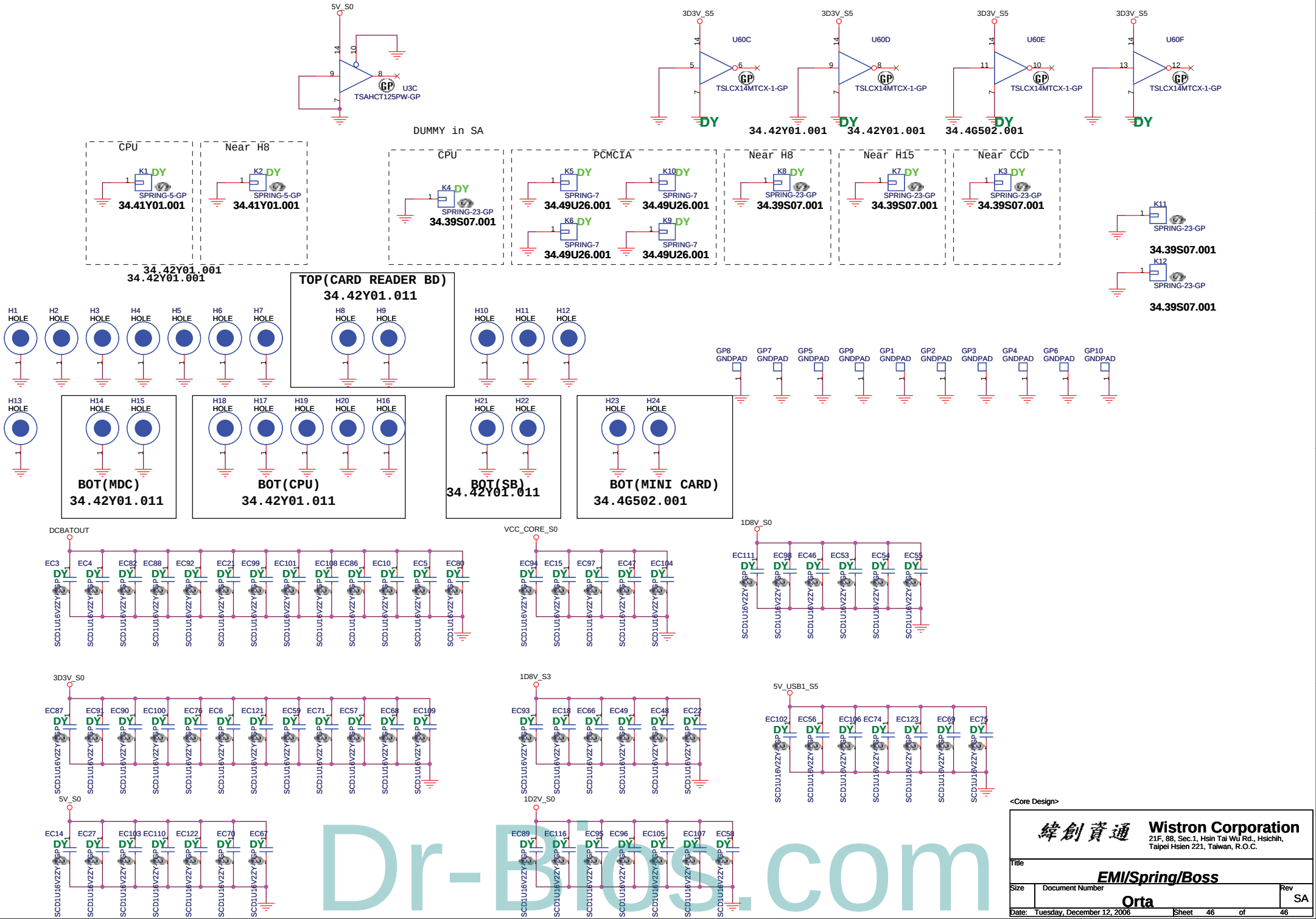

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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: EMI/Spring/Boss

Size | Document Number: Orta | Rev: SA

Date: Tuesday, December 12, 2006 | Sheet 46 of 46