

Compal Confidential

JALC0 Schematics Document

AMD Griffin Processor with RS780M+SB700

(With ATI MXM/B)

2008-9-11

REV: 2.0

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Issued Date	2007/09/14	Deciphered Date	2008/04/04	Title	SCHEMATICS, M/B S4182	
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail for SB	ON	ON	X
+3V_LAN	3.3V power rail for LAN	ON	ON	X
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
PCMCIA Card bus	AD17	0	PIRQE

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b
MXM GMT G781-1	1001 101X b

EC SM Bus2 address

Device	Address
ADI ADM1032	1001 100X b
CPU SB	1001 101X b

SB700 SM Bus 0 address

Device	Address
Clock Generator (ICS9LPRS365)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb
Minicard	
Minicard	
HDMI switch	

SB700 SM Bus 1 address

Device	Address
New card	
Lan	

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

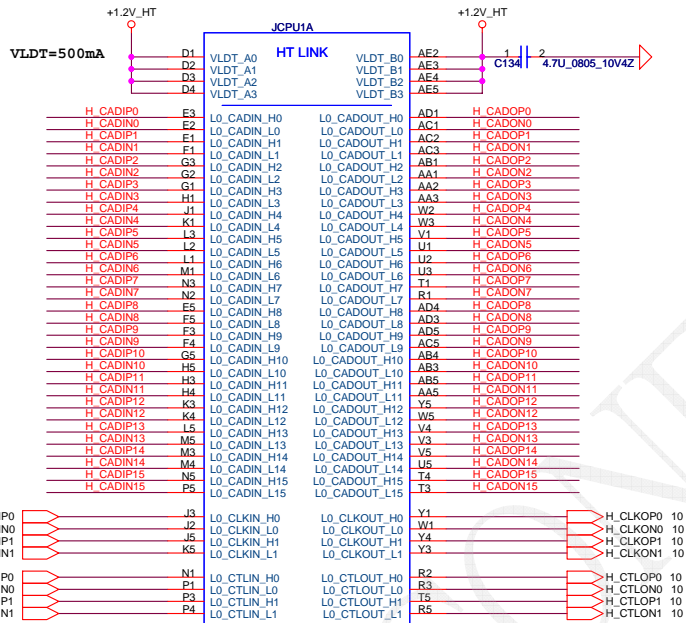
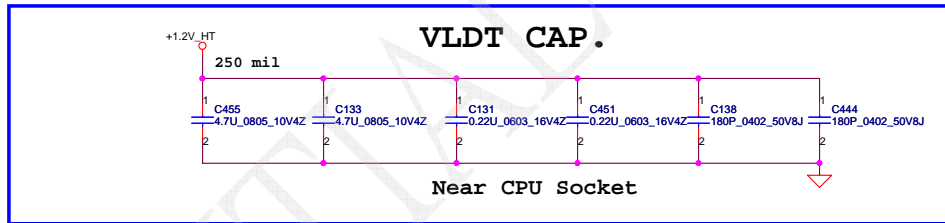
BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3, 0.4, 1.0
3	2.0
4	
5	
6	
7	

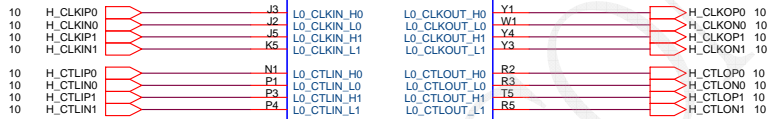
BTO Option Table

BTO Item	BOM Structure
	EEPROM@
	FLASH@
5787	5787@
5764	5764@
ALC888VC	888@
ALC268	ALC268@
with docking	Docking@
w/o docking	no docking@

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H_CADIP0	E3	L0_CADIN_H0	L0_CADOUT_H0	AD1	H_CADOP0
H_CADIN0	E2	L0_CADIN_L0	L0_CADOUT_L0	AC1	H_CADON0
H_CADIP1	F1	L0_CADIN_H1	L0_CADOUT_H1	AC2	H_CADOP1
H_CADIN1	F1	L0_CADIN_L1	L0_CADOUT_L1	AC3	H_CADON1
H_CADIP2	G3	L0_CADIN_H2	L0_CADOUT_H2	AB1	H_CADOP2
H_CADIN2	G2	L0_CADIN_L2	L0_CADOUT_L2	AA1	H_CADON2
H_CADIP3	G1	L0_CADIN_H3	L0_CADOUT_H3	AA2	H_CADOP3
H_CADIN3	H1	L0_CADIN_L3	L0_CADOUT_L3	AA3	H_CADON3
H_CADIP4	H1	L0_CADIN_H4	L0_CADOUT_H4	W2	H_CADOP4
H_CADIN4	K1	L0_CADIN_L4	L0_CADOUT_L4	W3	H_CADON4
H_CADIP5	L3	L0_CADIN_H5	L0_CADOUT_H5	V1	H_CADOP5
H_CADIN5	L2	L0_CADIN_L5	L0_CADOUT_L5	L1	H_CADON5
H_CADIP6	L1	L0_CADIN_H6	L0_CADOUT_H6	L12	H_CADOP6
H_CADIN6	M1	L0_CADIN_L6	L0_CADOUT_L6	L3	H_CADON6
H_CADIP7	N3	L0_CADIN_H7	L0_CADOUT_H7	T1	H_CADOP7
H_CADIN7	E5	L0_CADIN_L7	L0_CADOUT_L7	R1	H_CADON7
H_CADIP8	N2	L0_CADIN_H8	L0_CADOUT_H8	AD4	H_CADOP8
H_CADIN8	F5	L0_CADIN_L8	L0_CADOUT_L8	AD3	H_CADON8
H_CADIP9	F4	L0_CADIN_H9	L0_CADOUT_H9	AD5	H_CADOP9
H_CADIN9	F4	L0_CADIN_L9	L0_CADOUT_L9	AC5	H_CADON9
H_CADIP10	G5	L0_CADIN_H10	L0_CADOUT_H10	AB4	H_CADOP10
H_CADIN10	H5	L0_CADIN_L10	L0_CADOUT_L10	AB3	H_CADON10
H_CADIP11	H3	L0_CADIN_H11	L0_CADOUT_H11	AB5	H_CADOP11
H_CADIN11	H4	L0_CADIN_L11	L0_CADOUT_L11	AA5	H_CADON11
H_CADIP12	K3	L0_CADIN_H12	L0_CADOUT_H12	Y5	H_CADOP12
H_CADIN12	K4	L0_CADIN_L12	L0_CADOUT_L12	Y5	H_CADON12
H_CADIP13	L5	L0_CADIN_H13	L0_CADOUT_H13	W5	H_CADOP13
H_CADIN13	M5	L0_CADIN_L13	L0_CADOUT_L13	V4	H_CADON13
H_CADIP14	M3	L0_CADIN_H14	L0_CADOUT_H14	V3	H_CADOP14
H_CADIN14	M4	L0_CADIN_L14	L0_CADOUT_L14	V5	H_CADON14
H_CADIP15	N5	L0_CADIN_H15	L0_CADOUT_H15	U5	H_CADOP15
H_CADIN15	P5	L0_CADIN_L15	L0_CADOUT_L15	T4	H_CADON15
				T3	H_CADON15



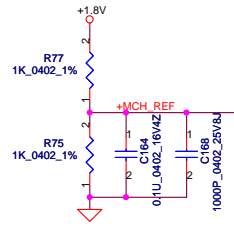
60900221006_B

Athlon 64 S1

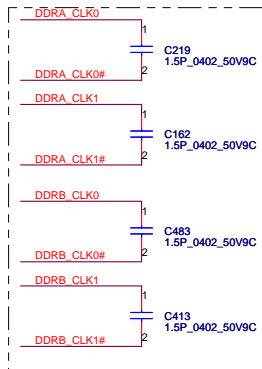
Processor Socket

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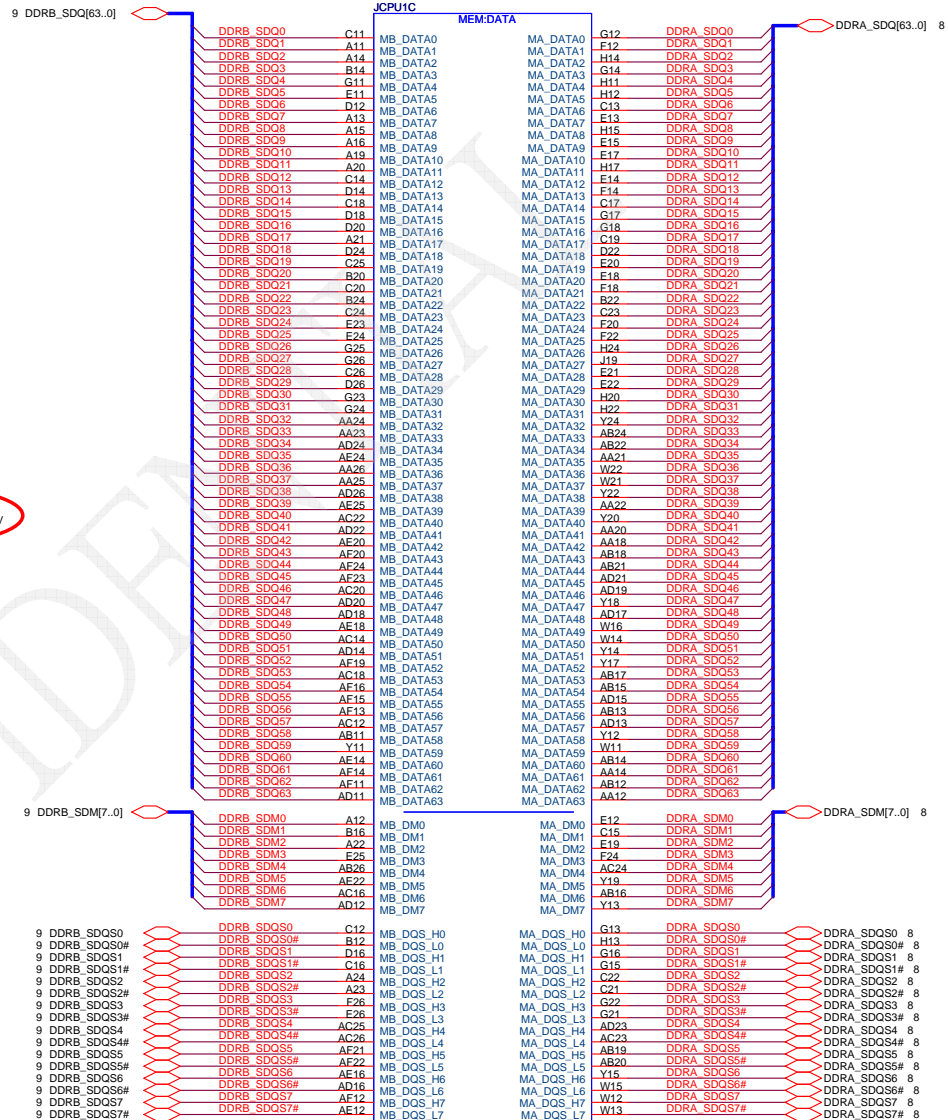
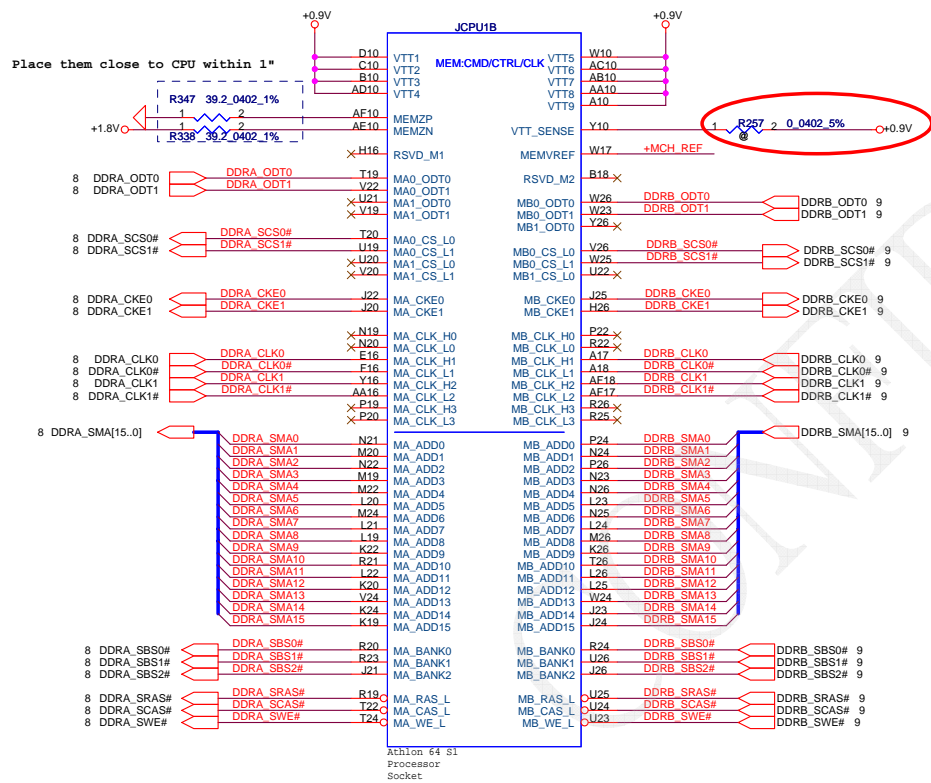
Processor DDR2 Memory Interface



PLACE CLOSE TO PROCESSOR
WITHIN 1.5 INCH



Place them close to CPU within 1"

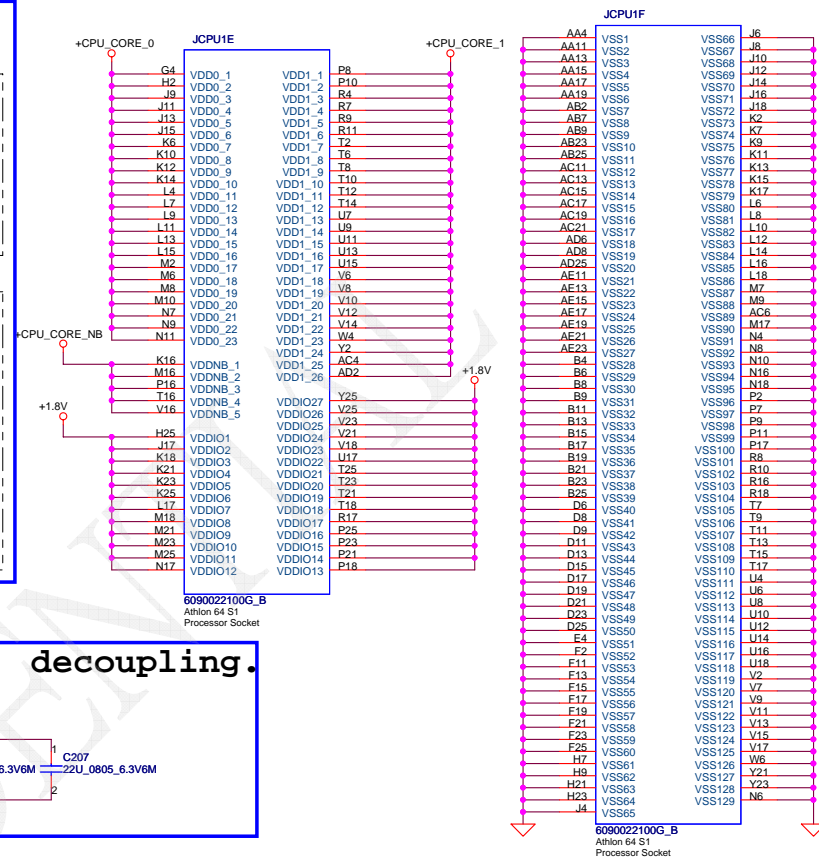
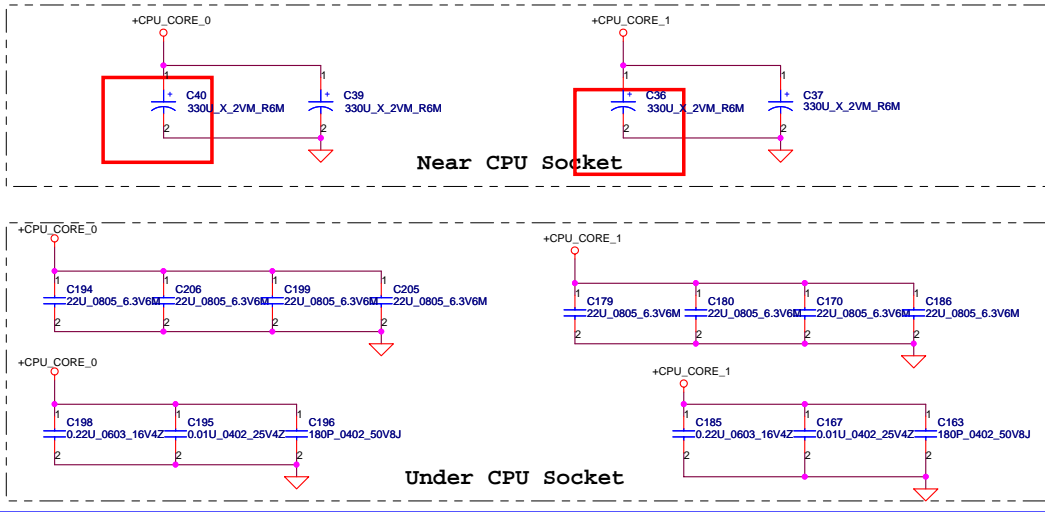


Athlon 64 S1
Processor
Socket

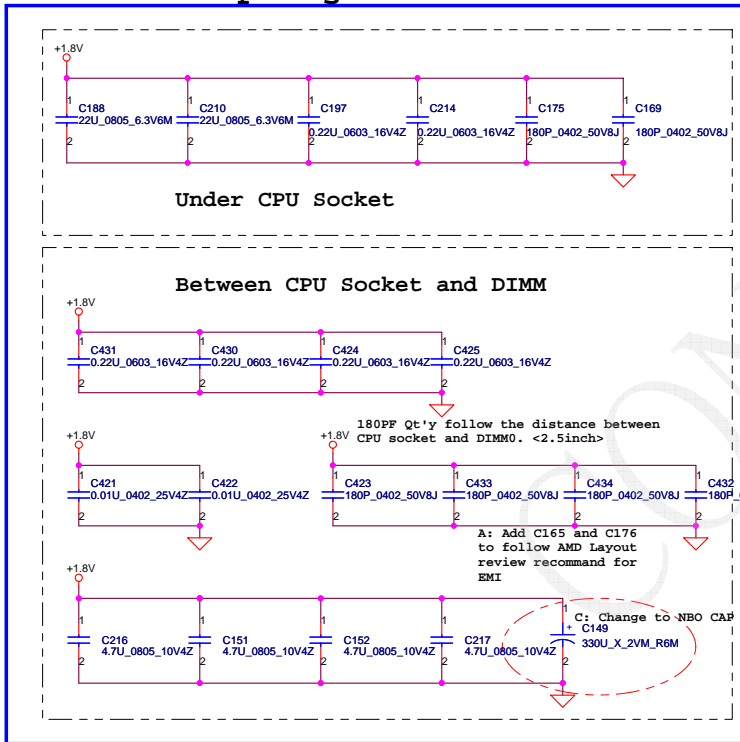
6090022100G_B
Athlon 64 S1
Processor Socket

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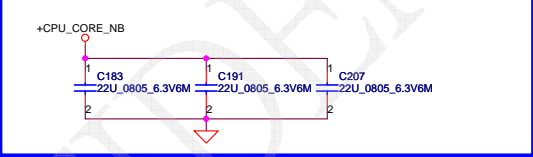
VDD(+CPU_CORE) decoupling.



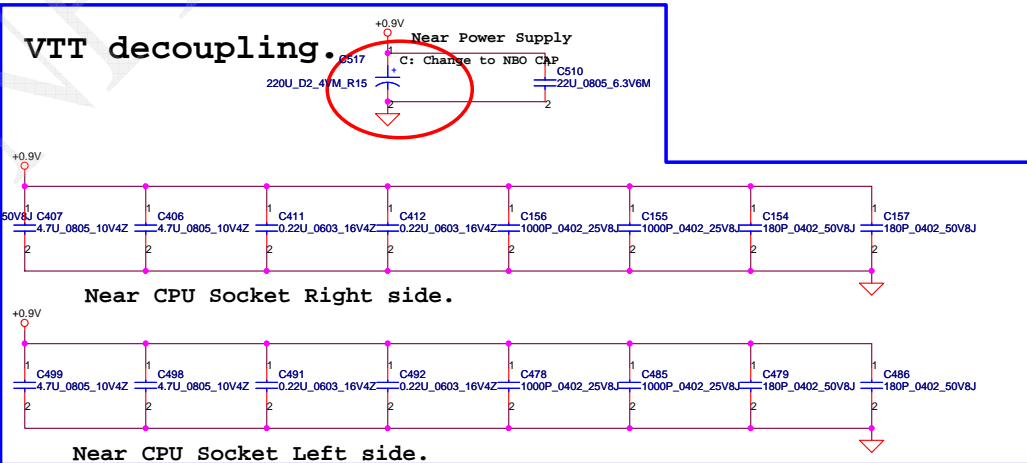
VDDIO decoupling.



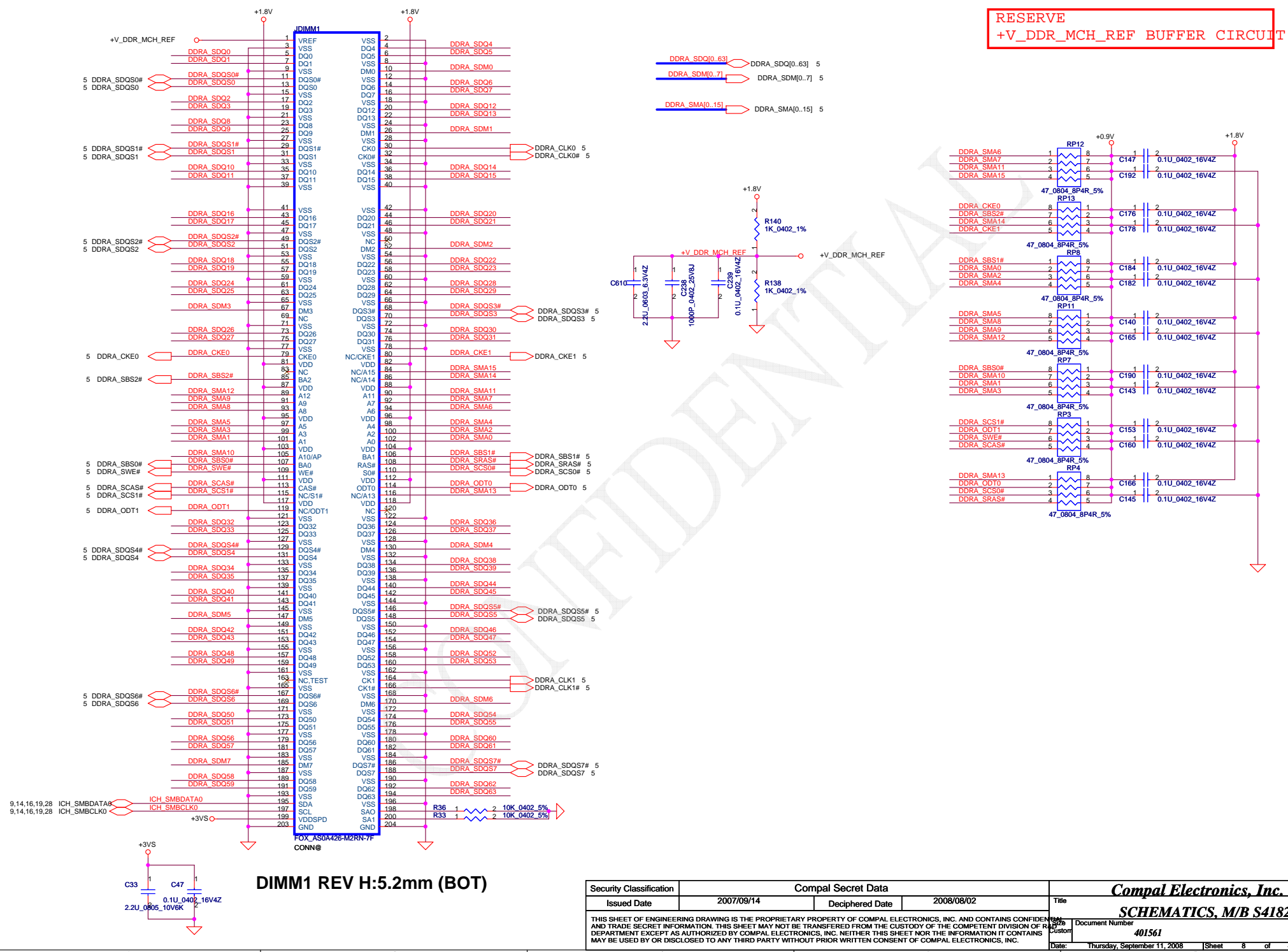
+CPU_CORE_NB decoupling.



VTT decoupling.



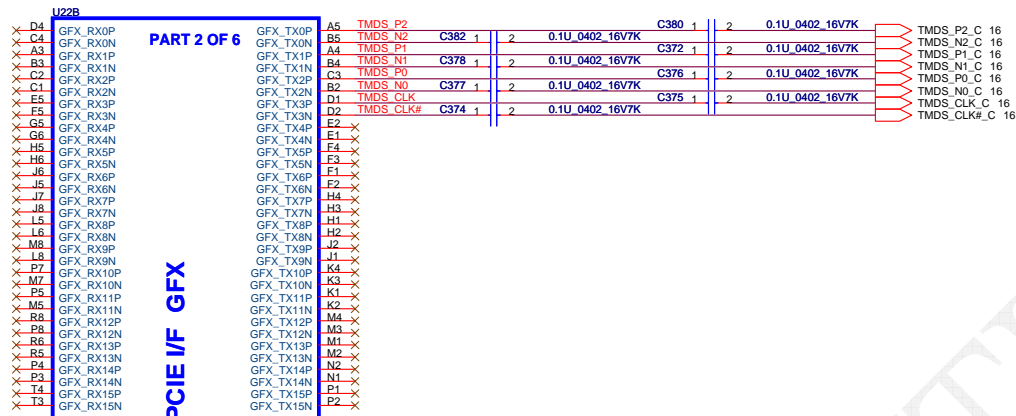
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RESERVE
+V_DDR_MCH_REF BUFFER CIRCUIT

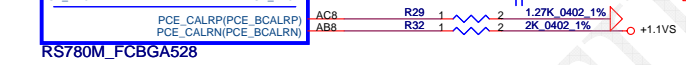
DIMM1 REV H:5.2mm (BOT)

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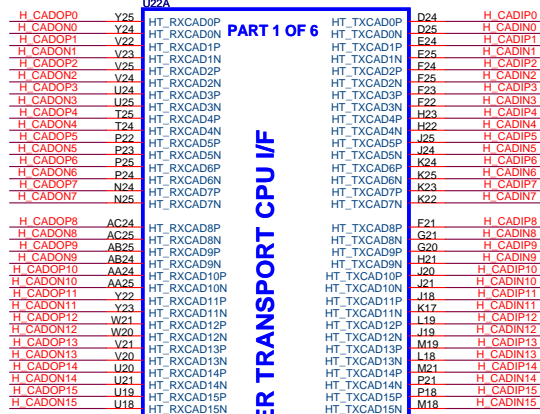
- 28 PCIE_PTX_C_IRX_P1
- 28 PCIE_PTX_C_IRX_N1
- 28 PCIE_PTX_C_IRX_P2
- 28 PCIE_PTX_C_IRX_N2
- 26 PCIE_PTX_C_IRX_P3
- 26 PCIE_PTX_C_IRX_N3
- 25 PCIE_PTX_C_IRX_P4
- 25 PCIE_PTX_C_IRX_N4

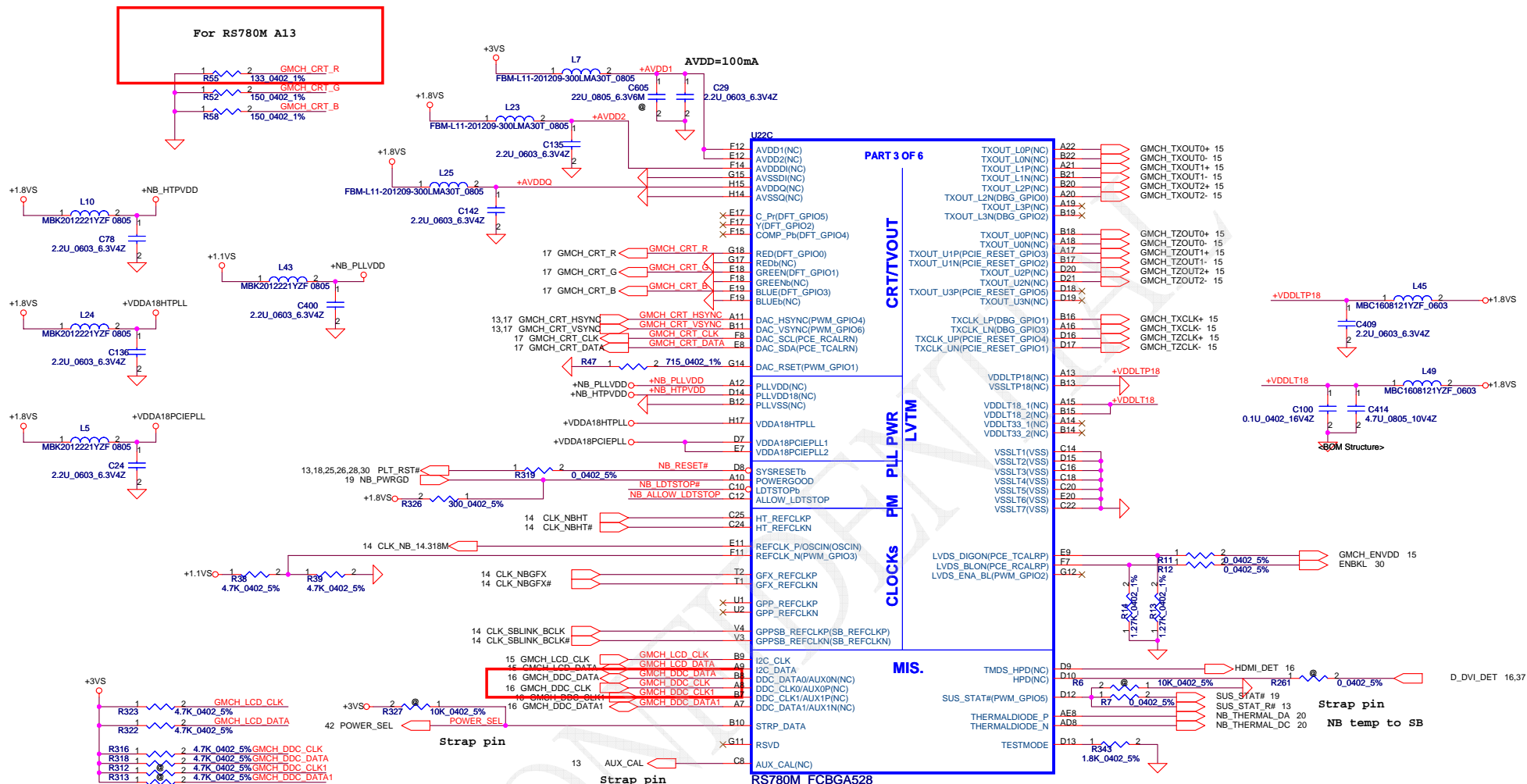
- 18 SB_RX0P
- 18 SB_RX0N
- 18 SB_RX1P
- 18 SB_RX1N
- 18 SB_RX2P
- 18 SB_RX2N
- 18 SB_RX3P
- 18 SB_RX3N



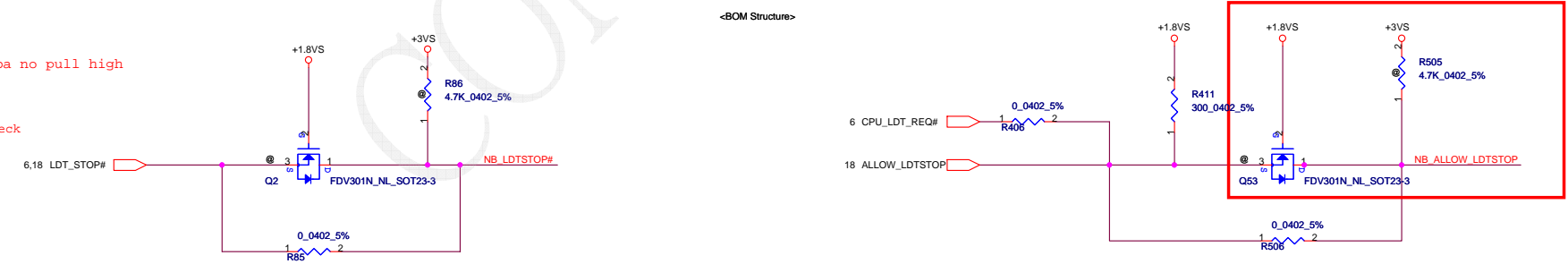
DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

- New Card
- TV Tuner
- WLAN
- GLAN
- Card Reader
- 4 H_CADON[0..15]
- 4 H_CADIN[0..15]

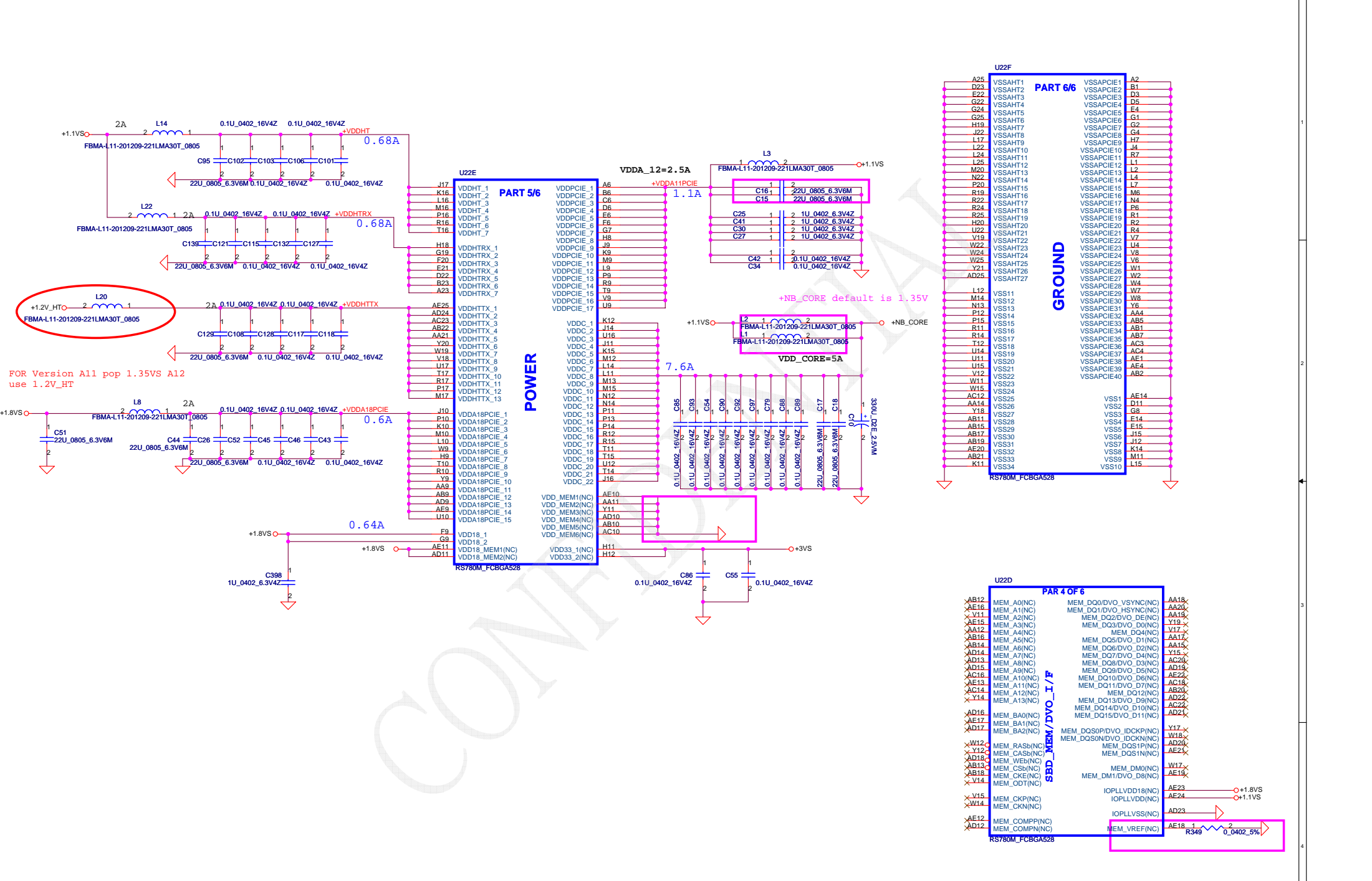




toshiba no pull high
AMD check



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FOR Version A11 pop 1.35VS A12 use 1.2V_HT

PART 6/6

GROUND

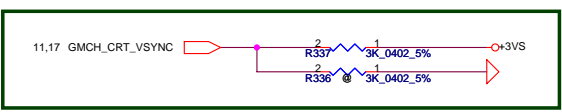
POWER

PAR 4 OF 6

SBD_MEM/DVO_I/F

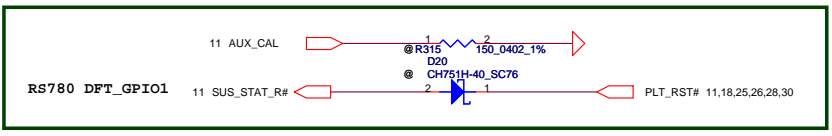
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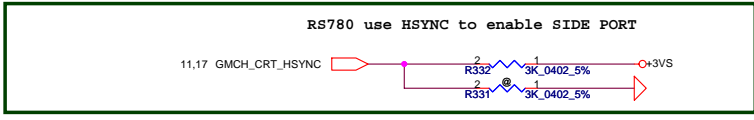
DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO. (VSYNC)
 1 : Disable (RS780)
 0 : Enable (Rs780)



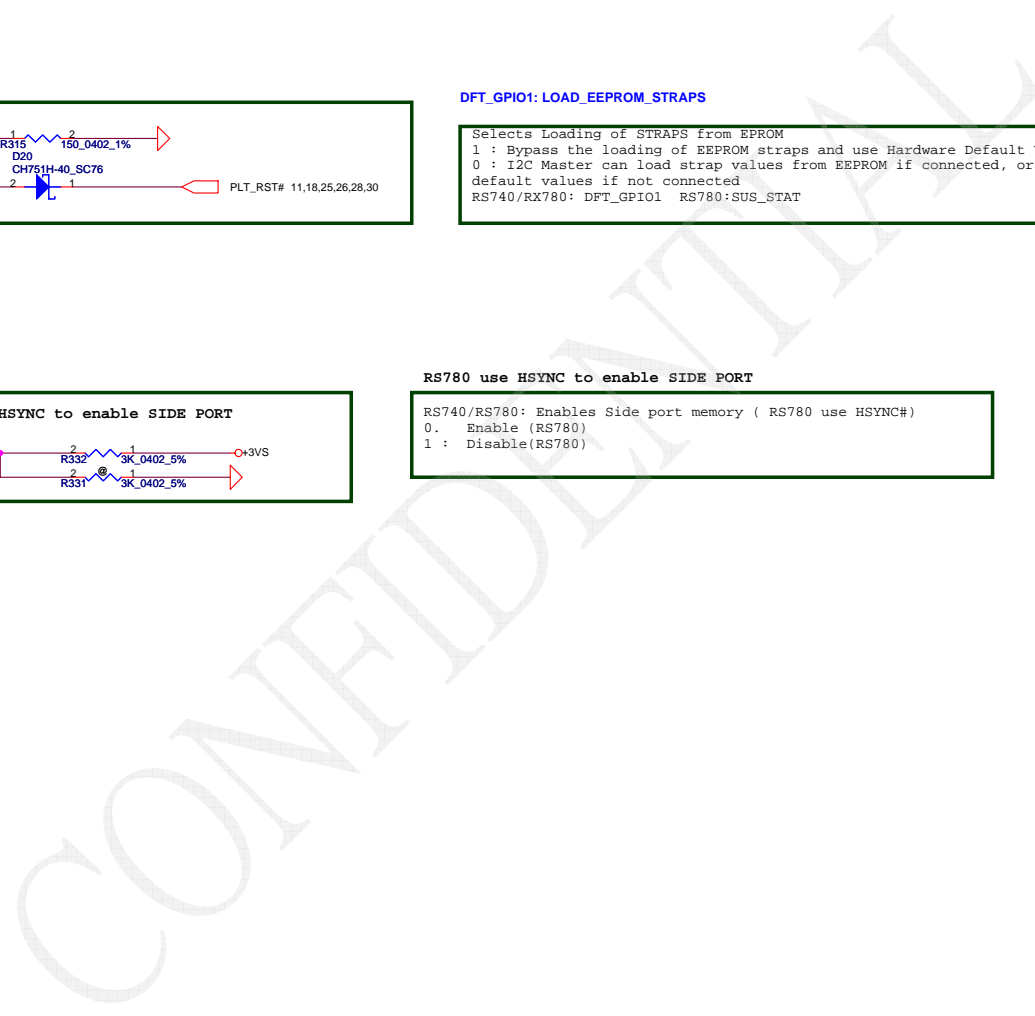
DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM
 1 : Bypass the loading of EEPROM straps and use Hardware Default Values
 0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected
 RS740/RX780: DFT_GPIO1 RS780:SUS_STAT

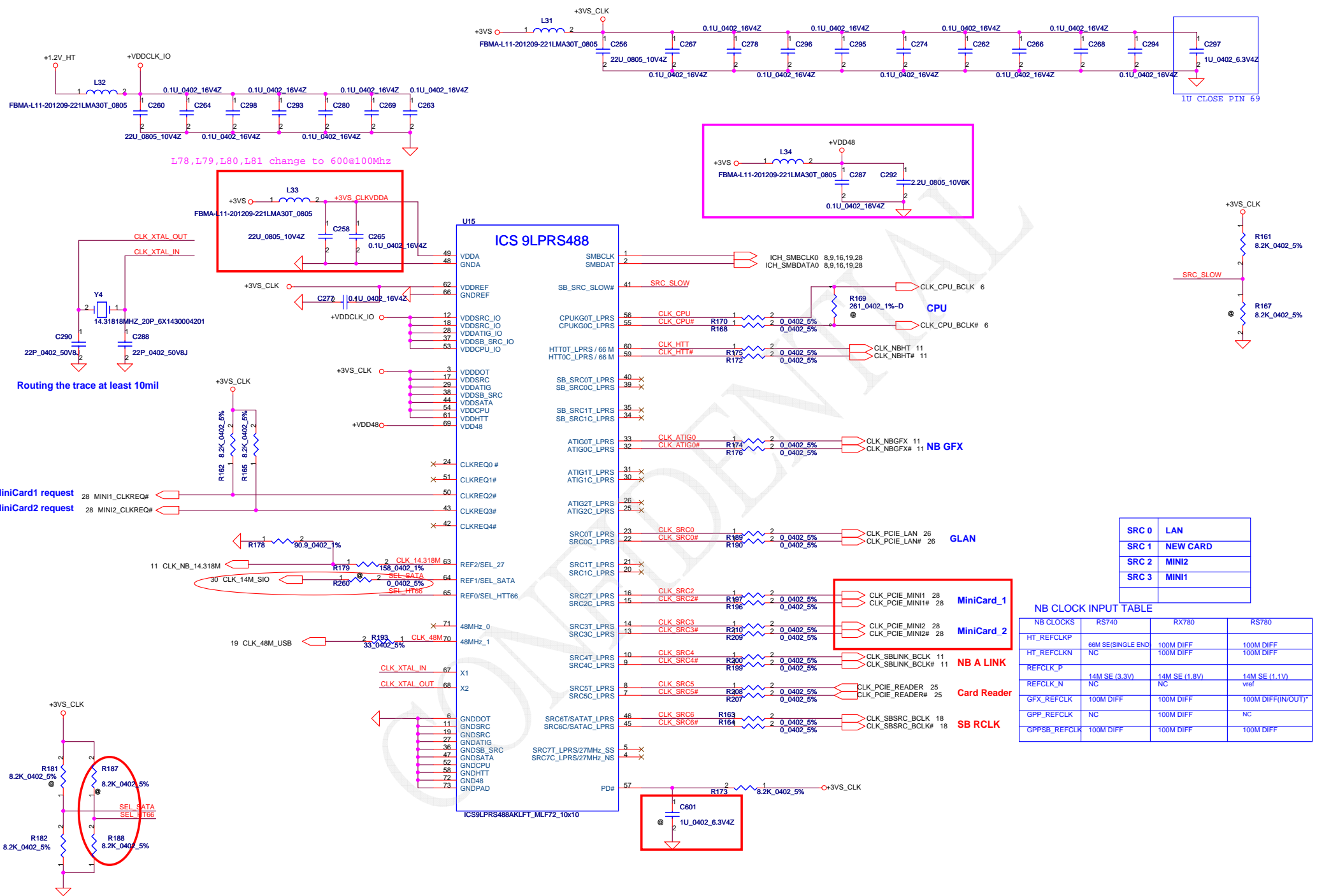


RS780 use HSYNC to enable SIDE PORT

RS740/RS780: Enables Side port memory (RS780 use HSYNC#)
 0 : Enable (RS780)
 1 : Disable(RS780)



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L78,L79,L80,L81 change to 600@100MHz

Routing the trace at least 10mil

MiniCard1 request
MiniCard2 request

SRC 0	LAN
SRC 1	NEW CARD
SRC 2	MINI2
SRC 3	MINI1

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	68M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)
GPP_REFCLK	NC	100M DIFF	NC
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

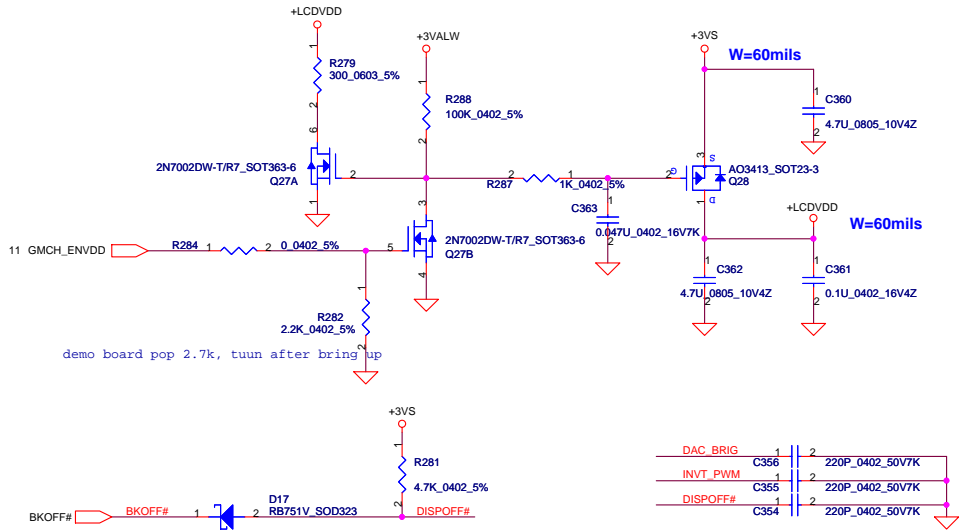
SEL_HTT66	1	configure as single-ended 66MHz output
	0*	configure as differential 100MHz output
SEL_SATA	1*	100M_SATA SRC6 output
	0	SPREAD 100M_SATA SRC6 output

* default

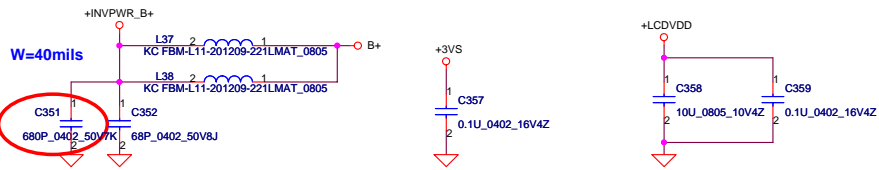
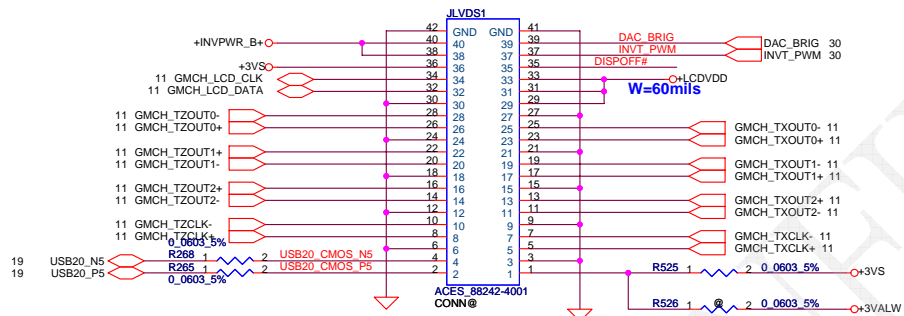
NB_OSC_14.318M	1	configure as 27M and 27M_SS output
	0*	configure as SRC 7 output

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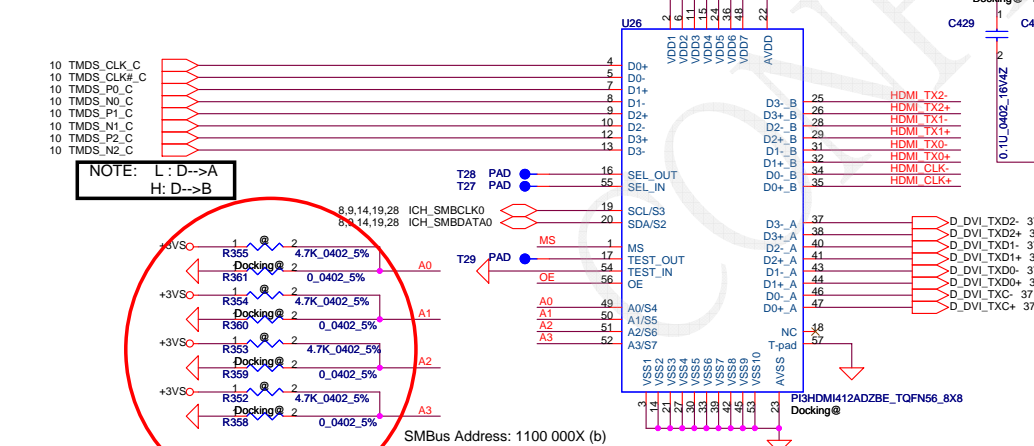
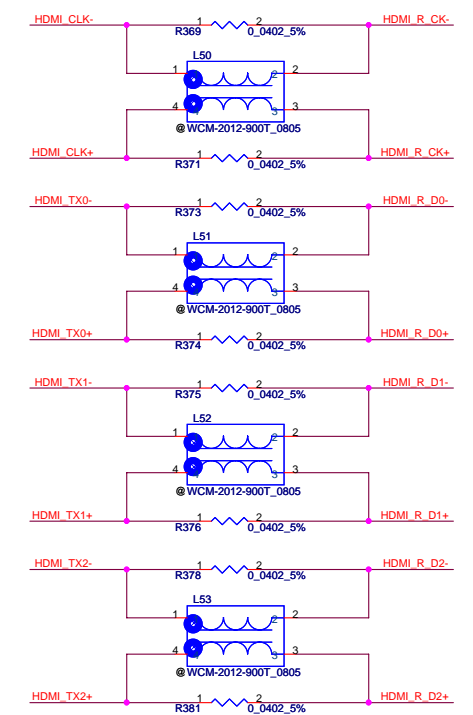
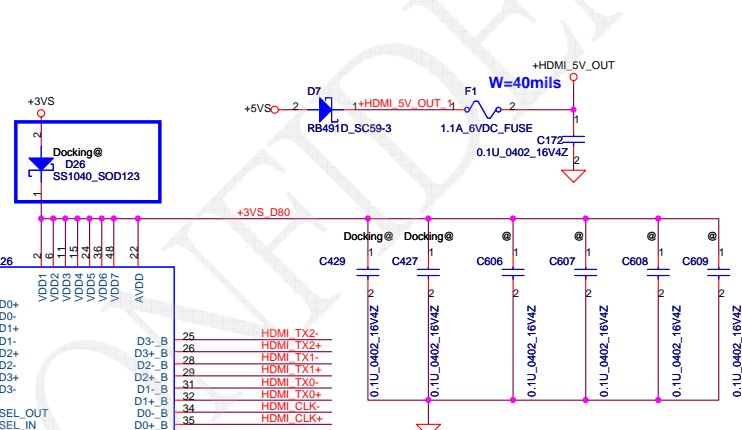
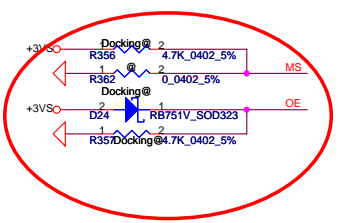
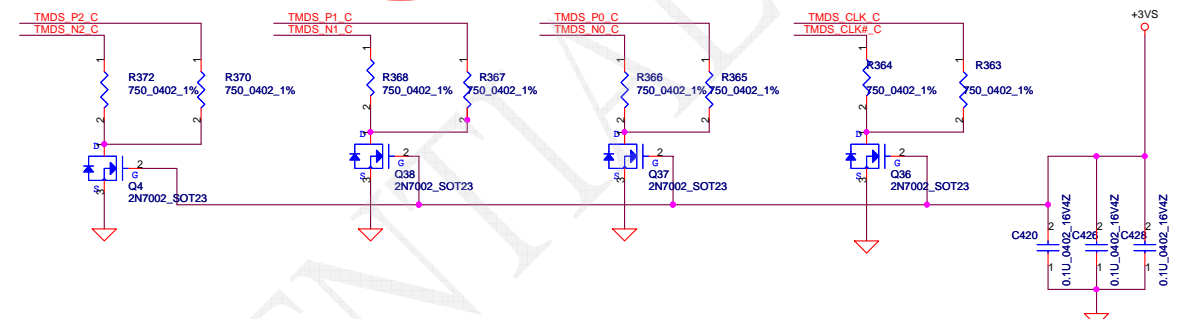
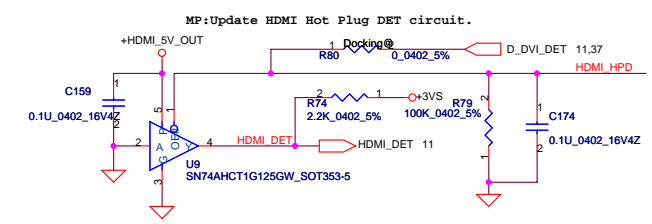
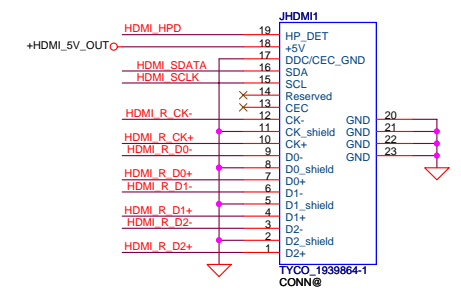
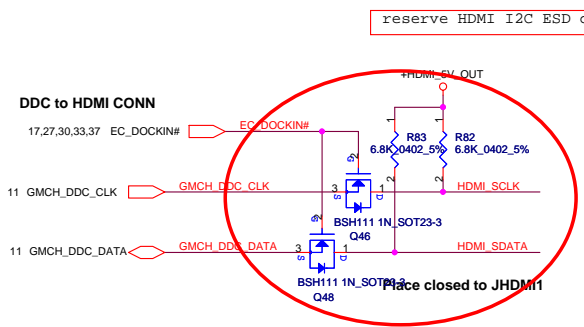
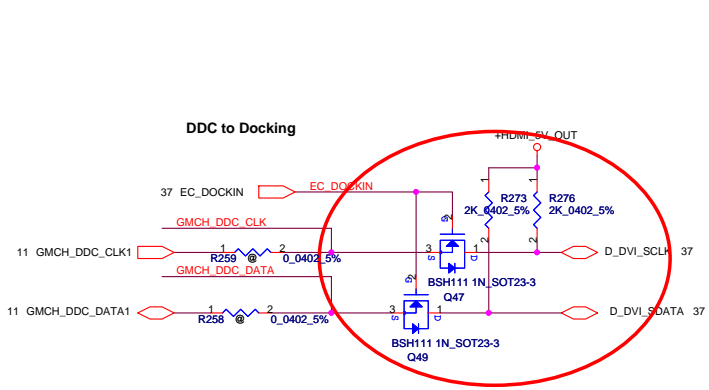
LCD POWER CIRCUIT



LCD/PANEL BD. Conn.



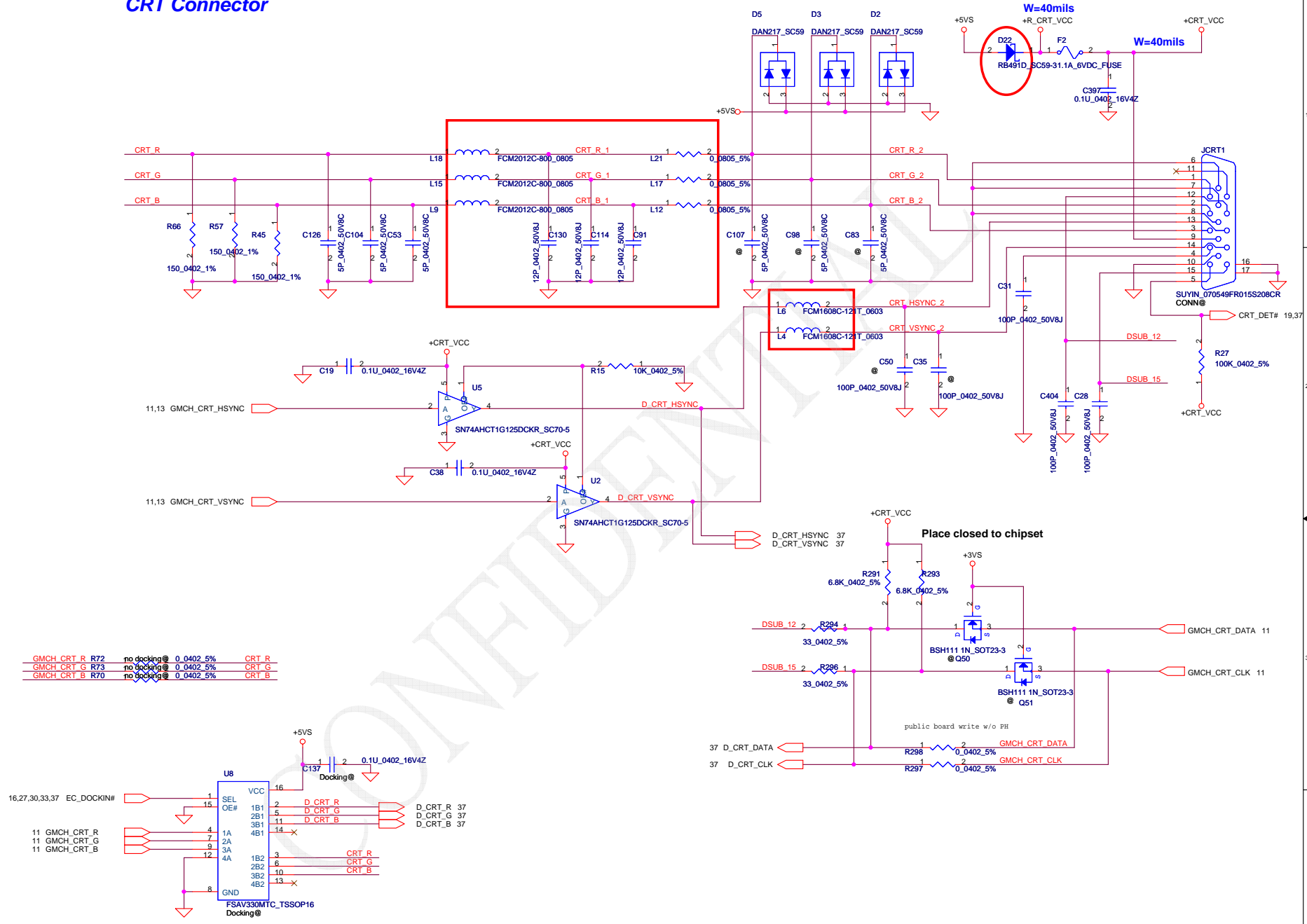
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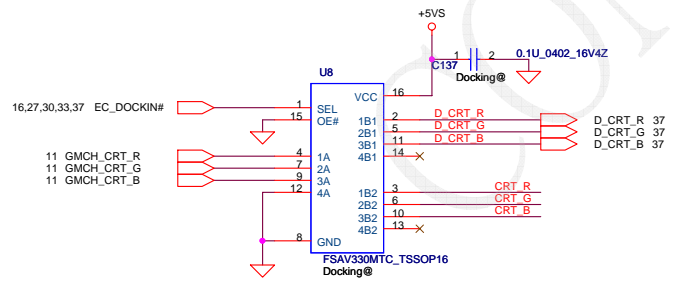
NOTE: L: D-->A
H: D-->B

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CRT Connector

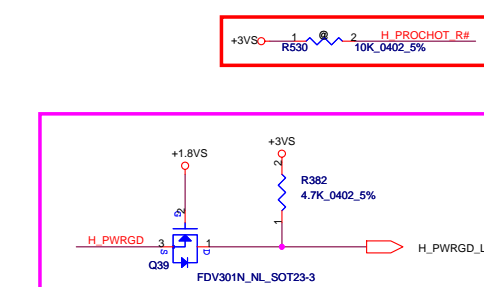
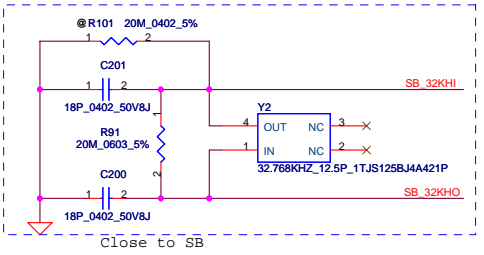
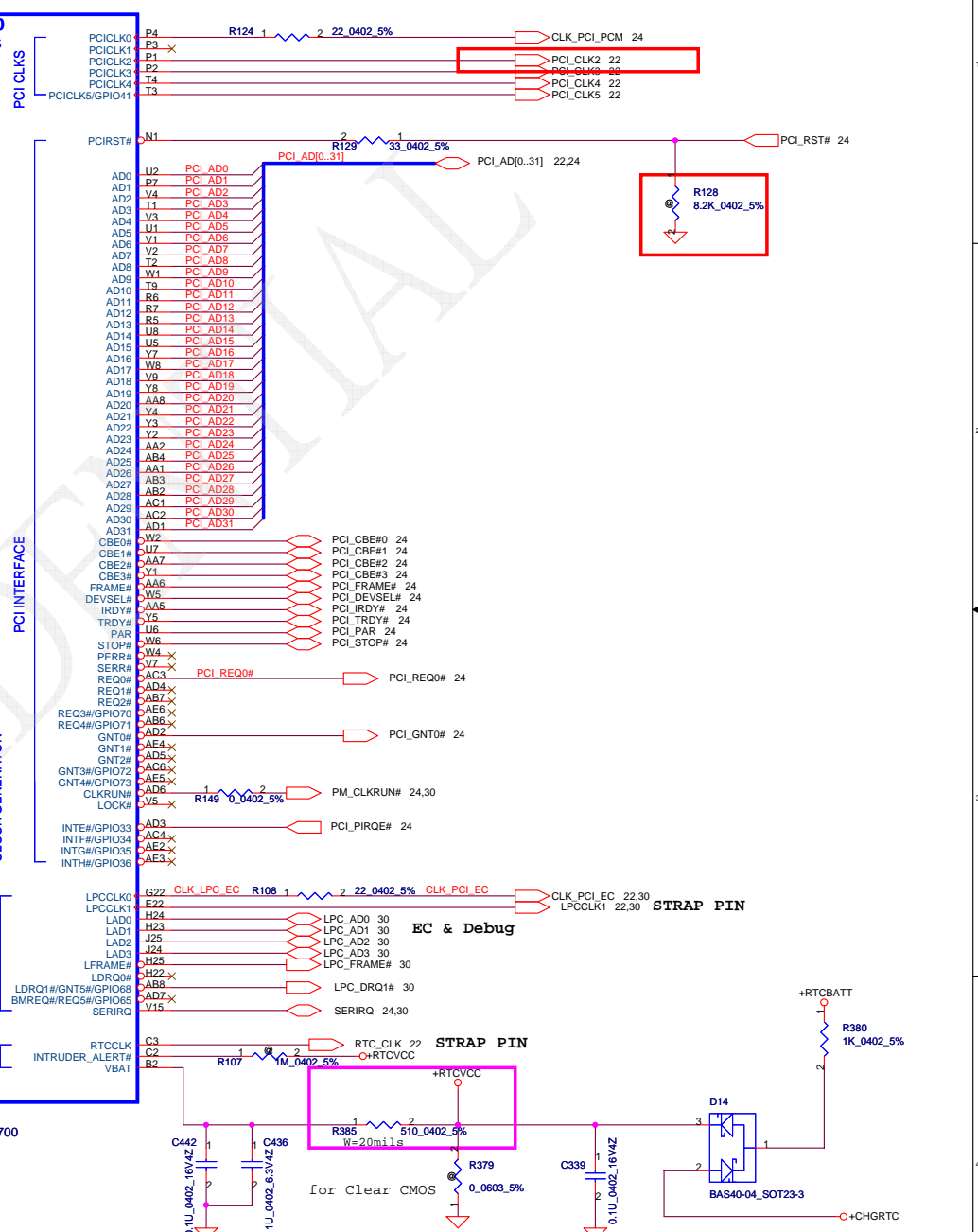
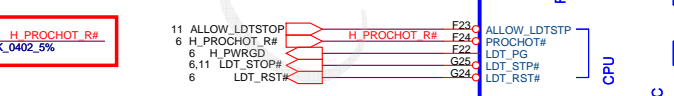
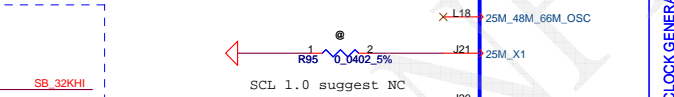
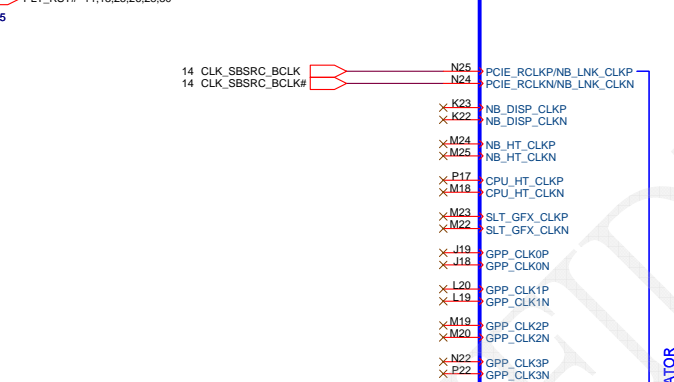
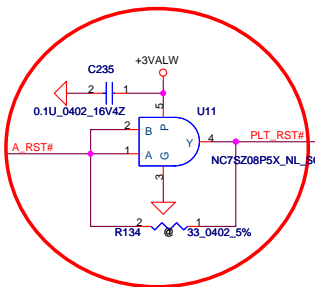
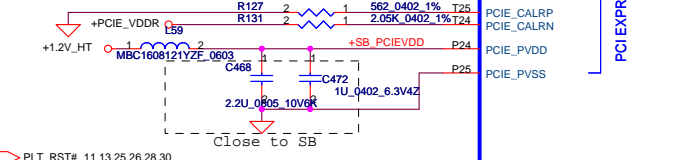
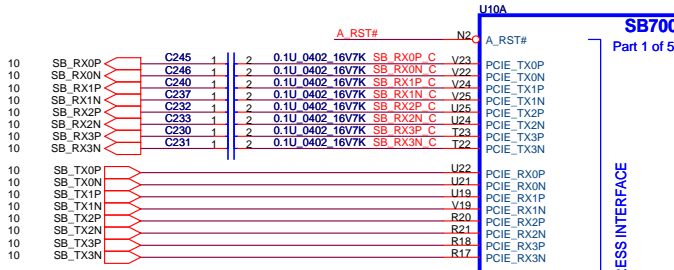
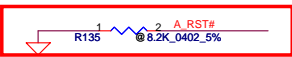


GMCH CRT_R R72	no docking@	0.0402_5%	CRT_R
GMCH CRT_G R73	no docking@	0.0402_5%	CRT_G
GMCH CRT_B R70	no docking@	0.0402_5%	CRT_B

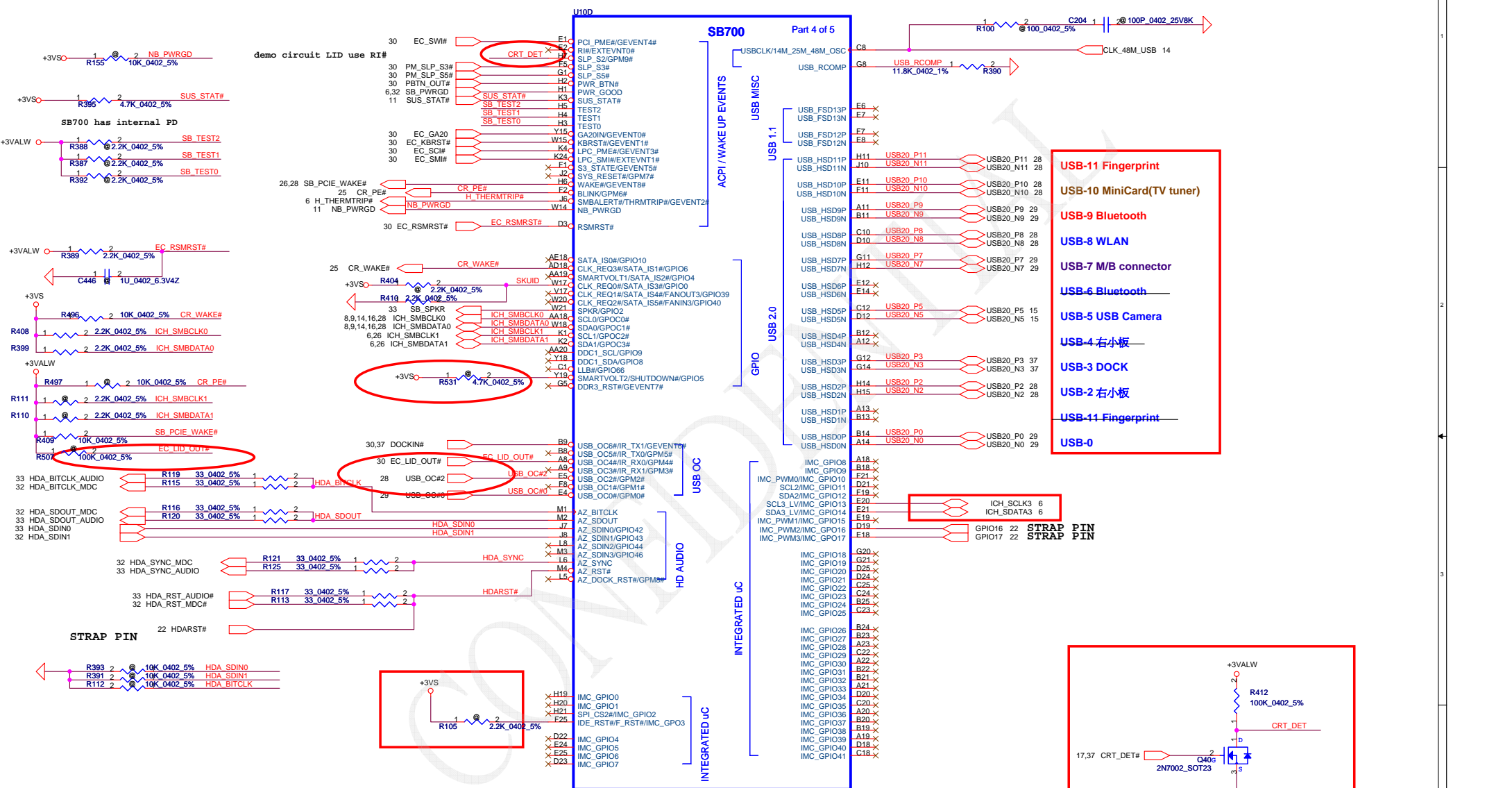


NOTE: L : A-->B1
H : A-->B2

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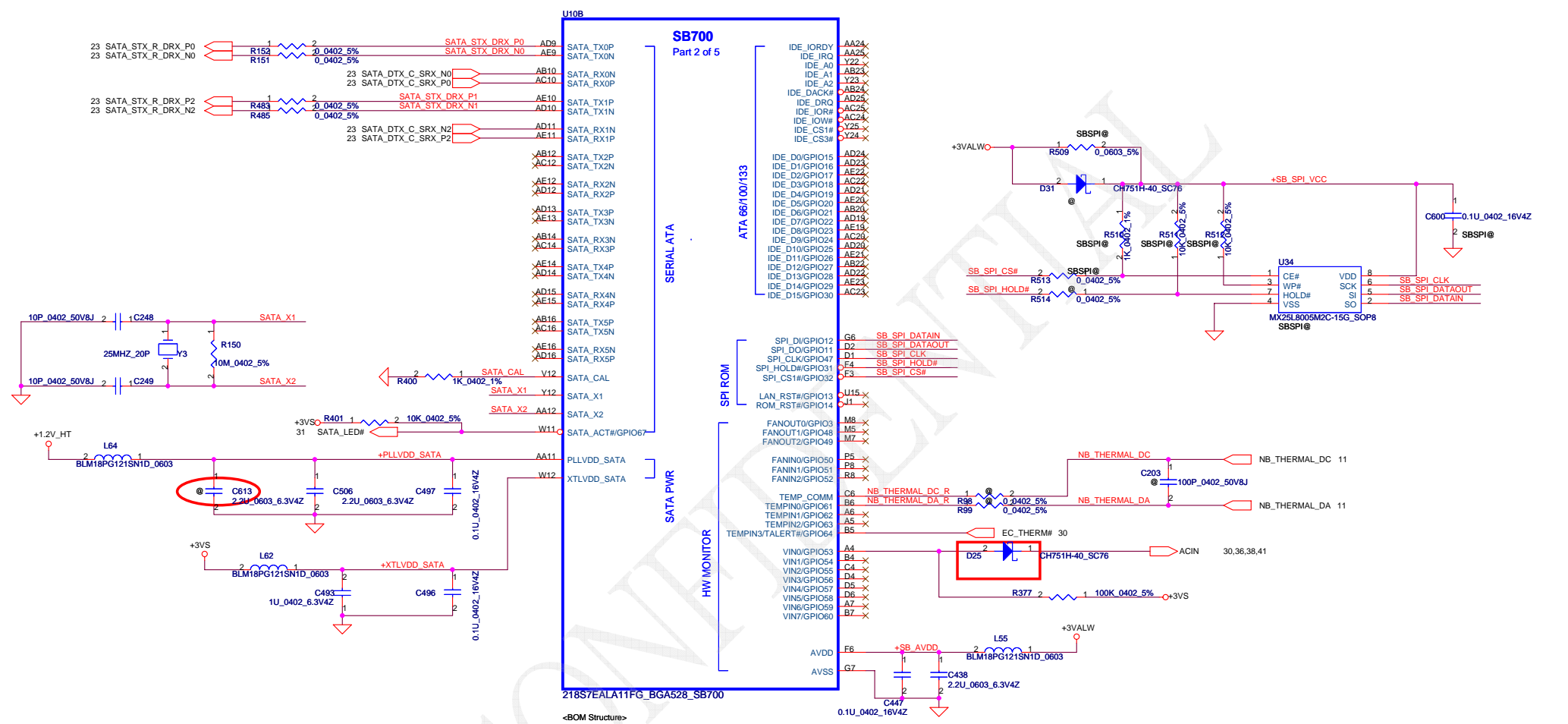
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21857EAL11FG_BGA528_SB700

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Compal Electronics, Inc.
SHEMATICS, M/B S4182



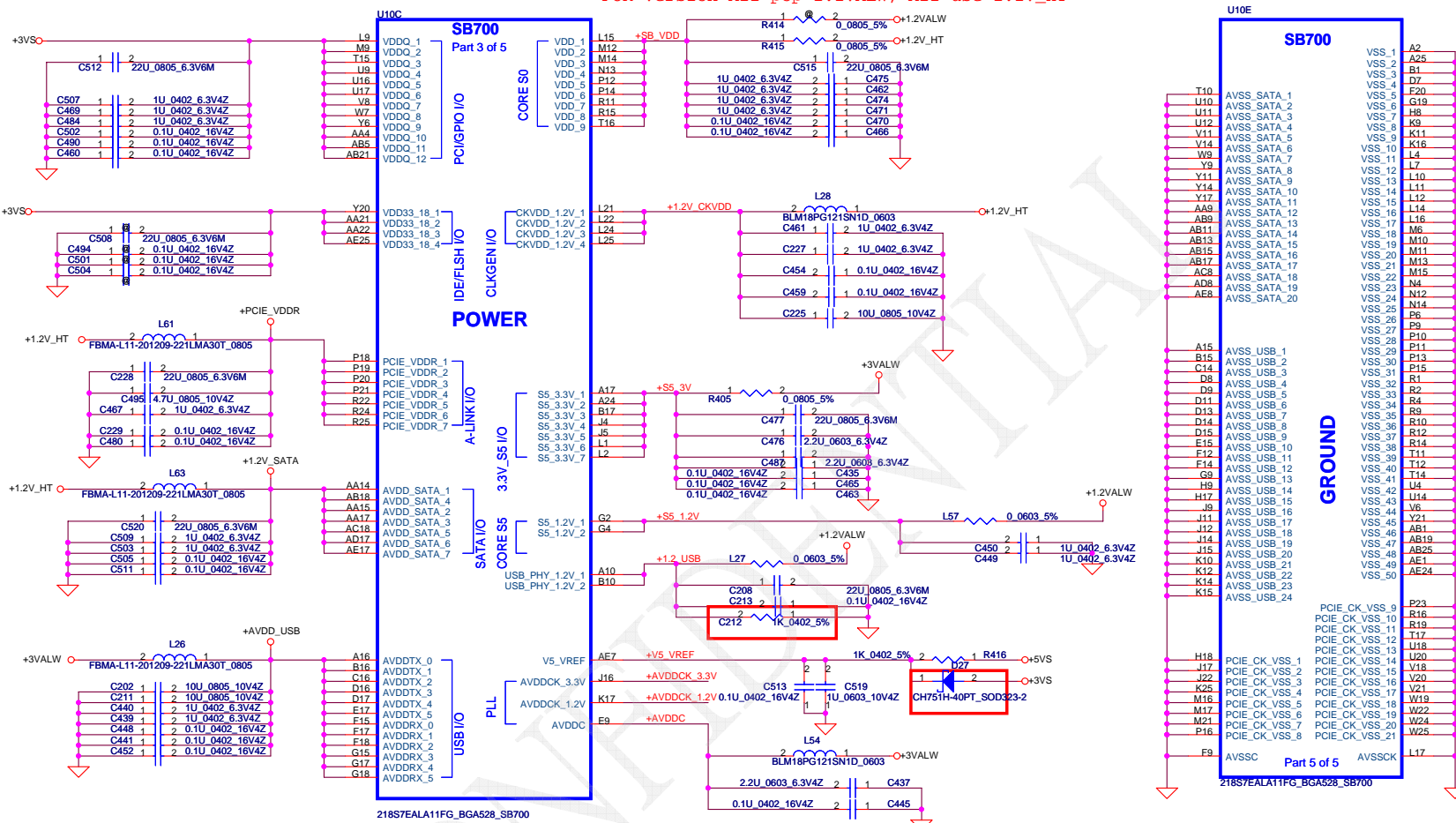
SB700
Part 2 of 5

SATA_TXOP	AD9	IDE_IORDY	AA24
SATA_TXON	AE9	IDE_IRO	AA25
SATA_RXON	AB10	IDE_A0	Y22
SATA_RXOP	AC10	IDE_A1	AB23
SATA_TX1P	AE10	IDE_A2	Y23
SATA_TX1N	AD10	IDE_DACK#	AB24
SATA_RX1N	AE11	IDE_DRQ	AD28
SATA_RX1P	AD11	IDE_IOR#	AC25
SATA_TX2P	AB12	IDE_IOW#	AC28
SATA_TX2N	AC12	IDE_CS#	Y26
SATA_RX2N	AE12	IDE_CS#	Y24
SATA_RX2P	AD12	IDE_D0/GPIO15	AD24
SATA_TX3P	AE13	IDE_D1/GPIO16	AD23
SATA_TX3N	AD13	IDE_D2/GPIO17	AE22
SATA_RX3N	AB14	IDE_D3/GPIO18	AC22
SATA_RX3P	AC14	IDE_D4/GPIO19	AD21
SATA_TX4P	AE14	IDE_D5/GPIO20	AE20
SATA_TX4N	AD14	IDE_D6/GPIO21	AD19
SATA_RX4N	AE15	IDE_D7/GPIO22	AD18
SATA_RX4P	AD15	IDE_D8/GPIO23	AE18
SATA_TX5P	AB16	IDE_D9/GPIO24	AD20
SATA_TX5N	AC16	IDE_D10/GPIO25	AC20
SATA_RX5N	AE16	IDE_D11/GPIO26	AE21
SATA_RX5P	AD16	IDE_D12/GPIO27	AB22
SATA_CAL	V12	IDE_D13/GPIO28	AE23
SATA_X1	Y12	IDE_D14/GPIO29	AC23
SATA_X2	Y12	IDE_D15/GPIO30	AC23
SATA_ACT#/GPIO6	W11	SPI_DI/GPIO12	G6
PLLVDD_SATA	AA11	SPI_DO/GPIO11	D2
XTLVDD_SATA	W12	SPI_CLK/GPIO47	D1
		SPI_HOLD#/GPIO31	E4
		SPI_CS1#/GPIO32	F3
		LAN_RST#/GPIO13	U15
		ROM_RST#/GPIO14	U1
		FANOUT0/GPIO3	M8
		FANOUT1/GPIO48	ME
		FANOUT2/GPIO49	M7
		FANIN0/GPIO50	P5
		FANIN1/GPIO51	P6
		FANIN2/GPIO52	R8
		TEMP_COMM	C6
		TEMPIN0/GPIO61	B6
		TEMPIN1/GPIO62	A6
		TEMPIN2/GPIO63	A5
		TEMPIN3/TALERT#/GPIO64	B5
		VIN0/GPIO53	A4
		VIN1/GPIO54	B4
		VIN2/GPIO55	C4
		VIN3/GPIO56	D4
		VIN4/GPIO57	D5
		VIN5/GPIO58	D6
		VIN6/GPIO59	A7
		VIN7/GPIO60	B7
		AVDD	F6
		AVSS	G7

218S7EALA11FG_BGA528_SB700
-<BOM Structure>

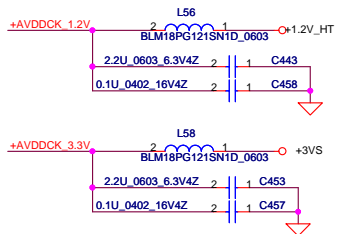
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FOR Version All pop 1.2VALW, A12 use 1.2V_HT



218S7EALA11FG_BGA528_SB700

<BOM Structure>



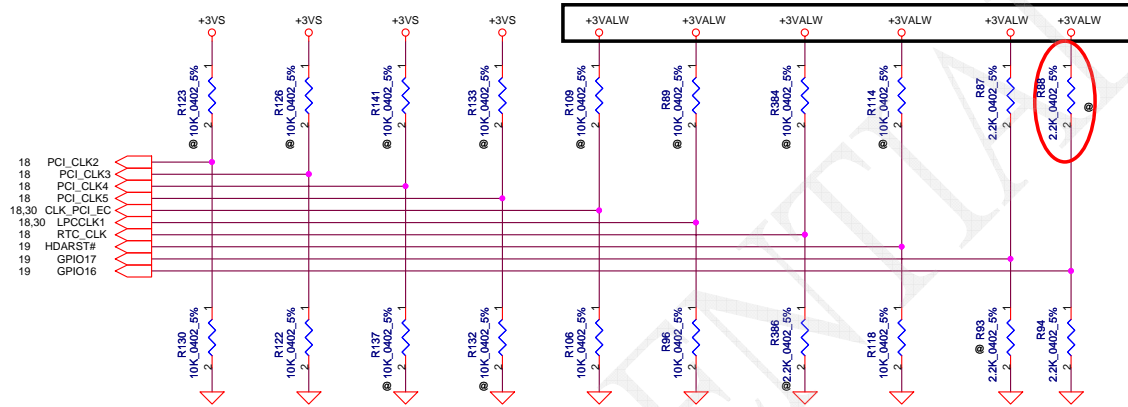
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SCHEMATICS, M/B S4182

REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

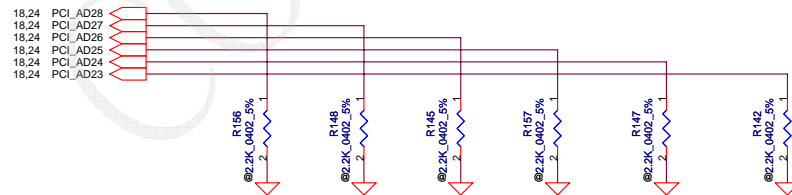
	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0 CLK_PCI_EC	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM	
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT	L,H = LPC ROM (Default L,NC) L,L = FWH ROM	



DEBUG STRAPS

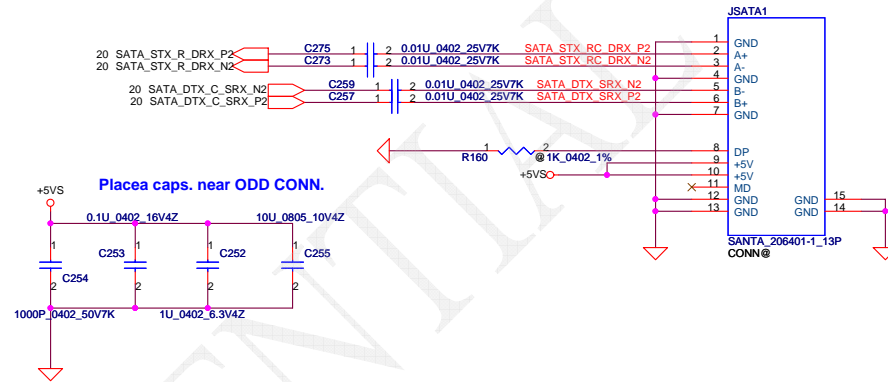
SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

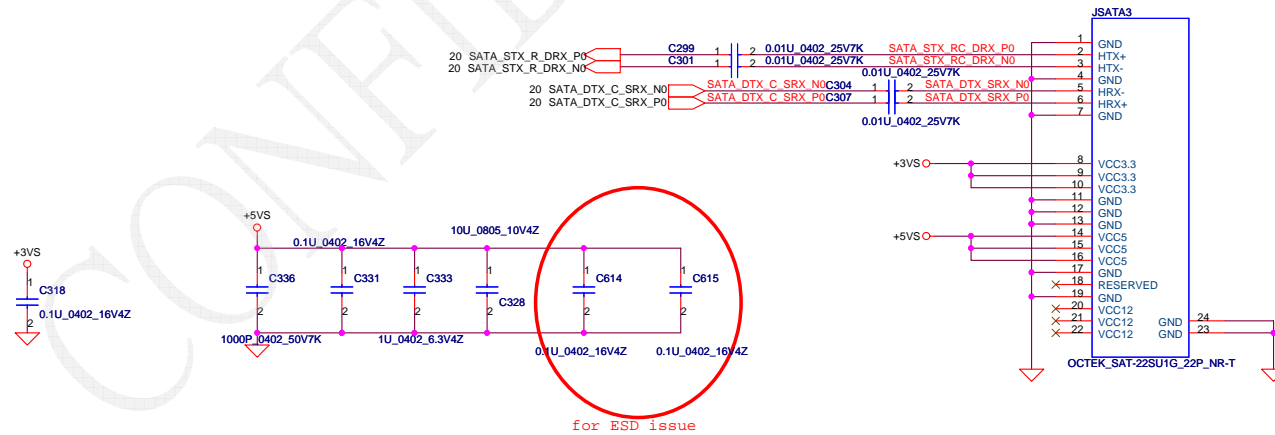


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SATA ODD Conn.



SATA HDD Conn.

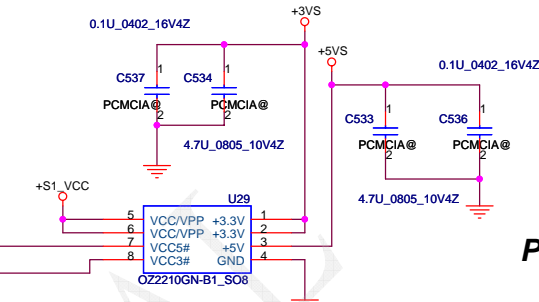
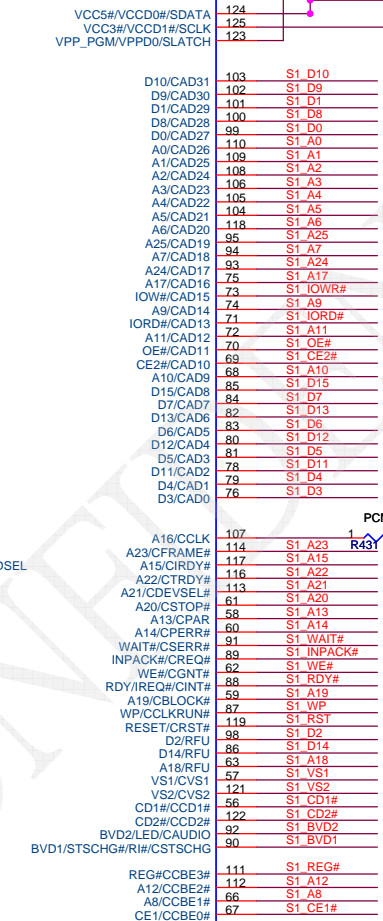
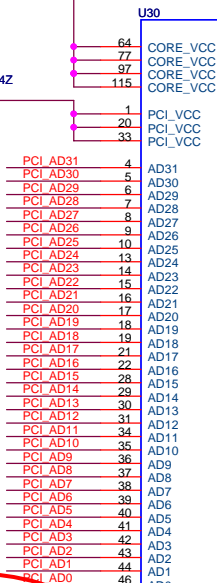
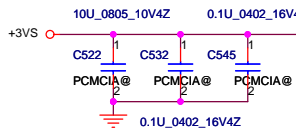
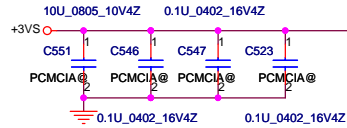


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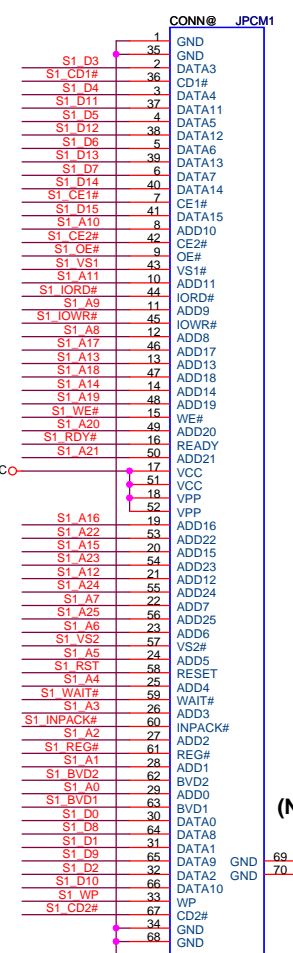
18,22 PCI_AD[0..31] PCI_AD[0..31]

18 PCI_CBE#[0..3] PCI_CBE#[0..3]

IDSEL SELECT POWER-ON-STRAPPING
(SEE NOTE & TABLE FOR OPTIONS)



PCMCIA Socket



4 IN 1 Socket (HDQ70)

SANTA_130601-7.LT

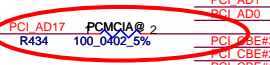
NOTE: IDSEL SELECTION!

THIS DEVICE UTILIZES A "SELECTABLE IDSEL" SCHEME. IDSEL CAN BE CONNECTED INTERNALLY TO ONE OF THREE PCI AD LINES OR EXTERNAL IDSEL SIGNAL.

22K TO 47K PULL-UP & PULL-DOWN RESISTORS ARE REQUIRED TO BE CONNECTED TO PINS 123 & 124 TO SELECT ONE OF THE 4 POSSIBLE IDSEL CONNECTIONS. THE TABLE BELOW SHOWS THE 4 POSSIBLE COMBINATIONS.

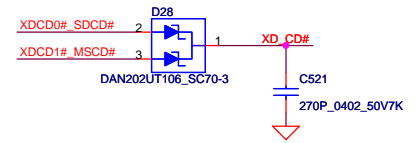
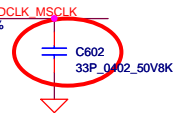
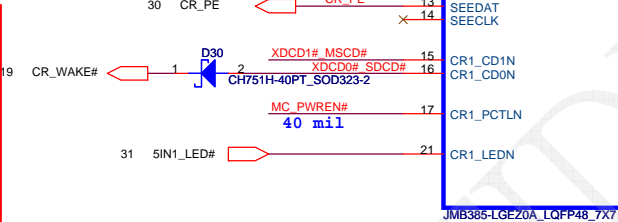
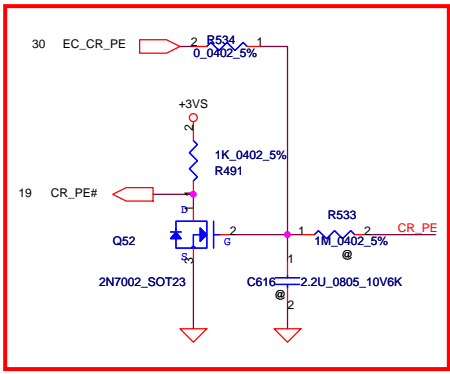
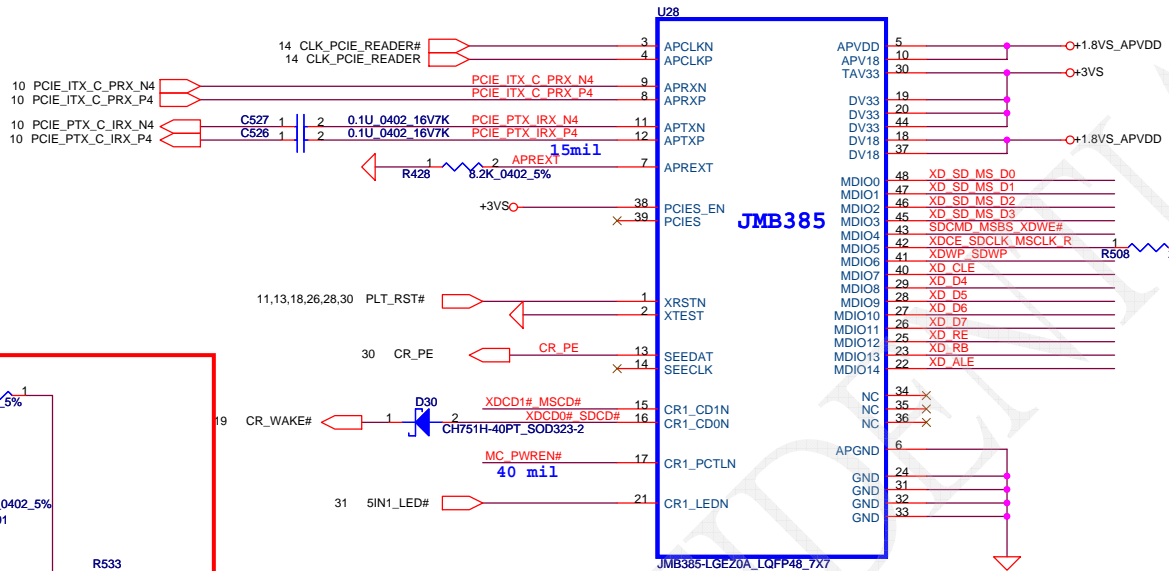
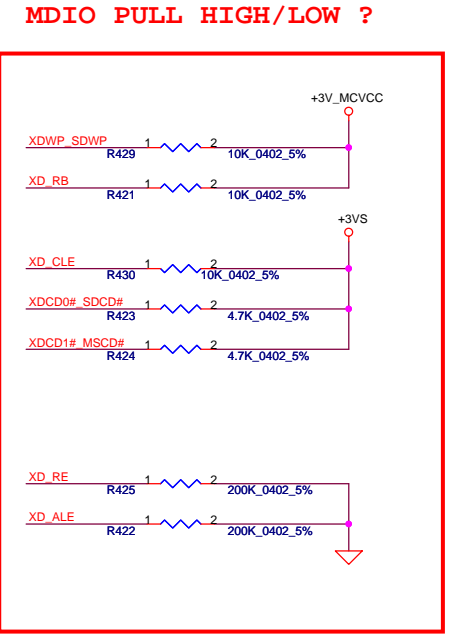
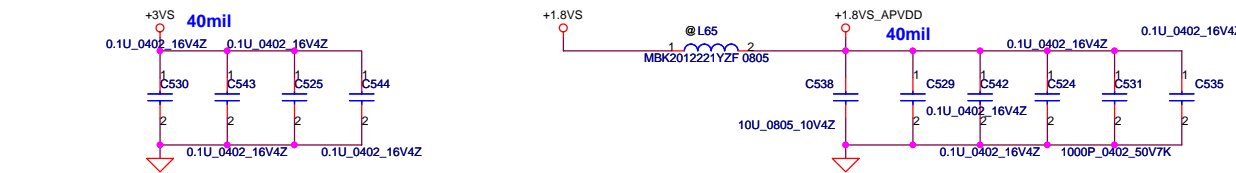
CONFIGURING IDSEL TO BE INTERNALLY CONNECTED ALLOWS FOR A FULL PARALLEL POWER MODE. IF AN EXTERNALLY CONNECTED IDSEL IS REQUIRED THEN AN INVERTER MUST BE CONNECTED TO VPP_PGM TO CREATE VPP_VCC.

VCC5# (124)	VPP_PGM (123)	IDSEL SELECT
DOWN	DOWN	AD18
DOWN	UP	AD20
UP	DOWN	AD25
UP	UP	INTA# F4



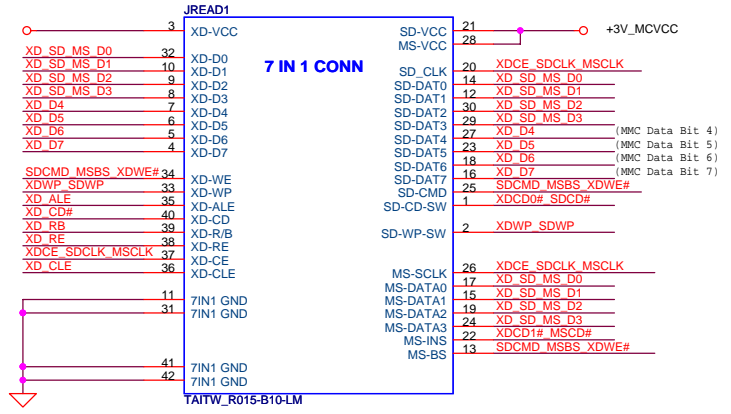
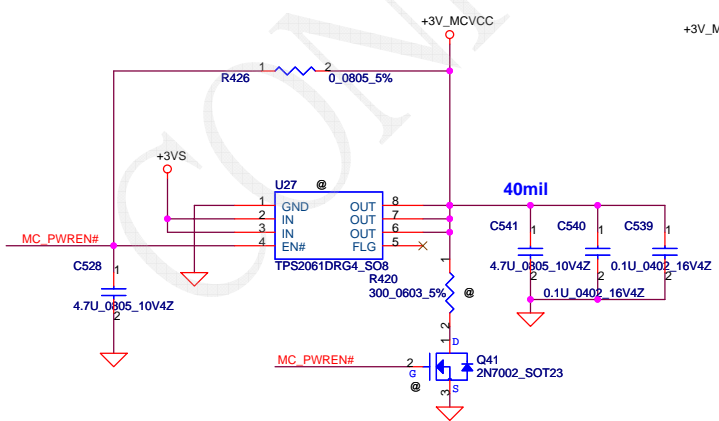
22K TO 47K PULL-UPS MUST BE PLACED ON INTA#, PME#, SERIRQ# & CLKRUN#.

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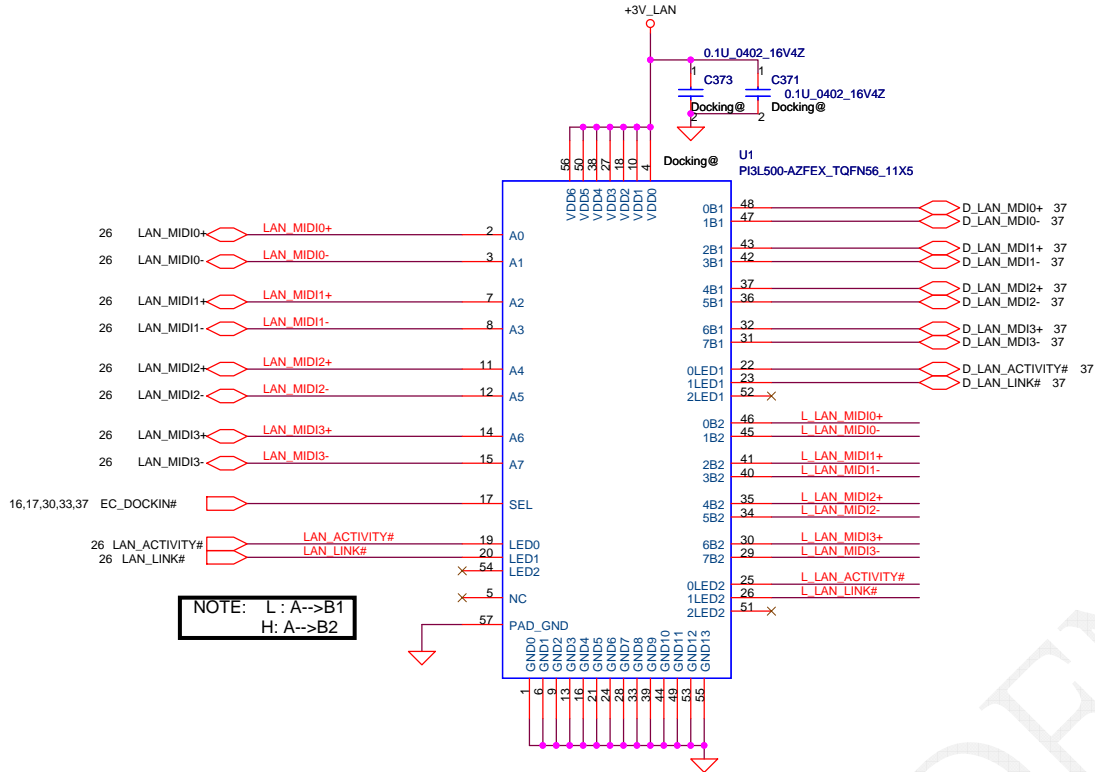


Memory Card Power Switch

4 IN 1 Socket Push Type(New)

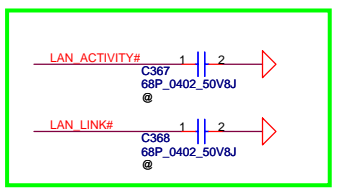
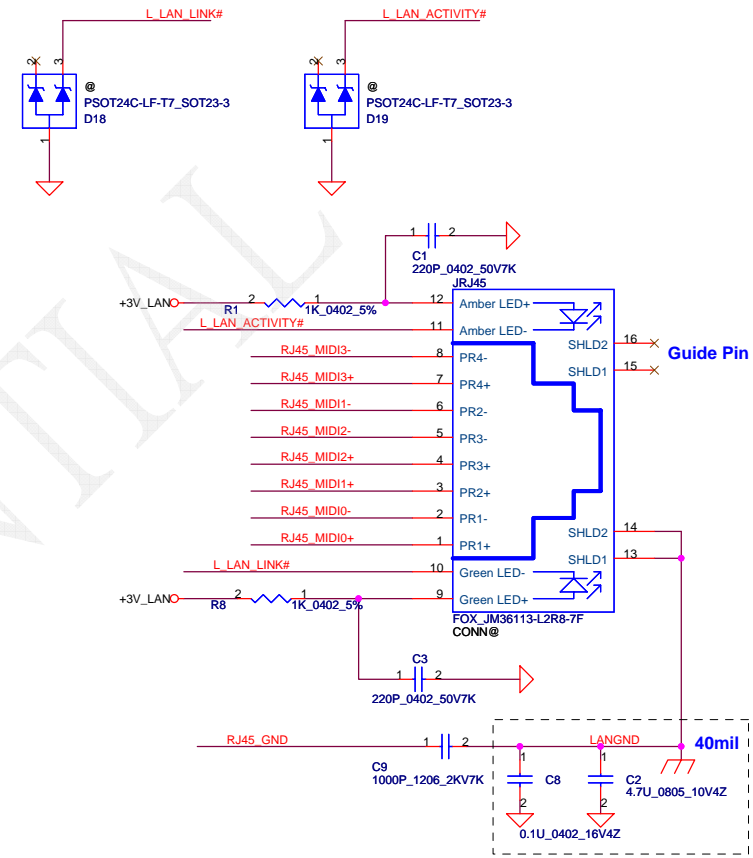
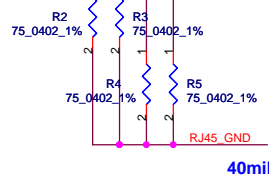
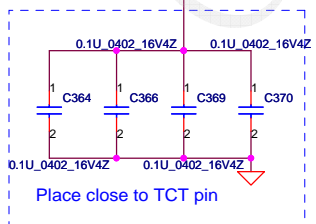
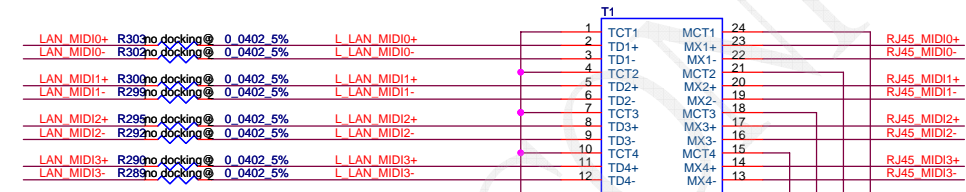


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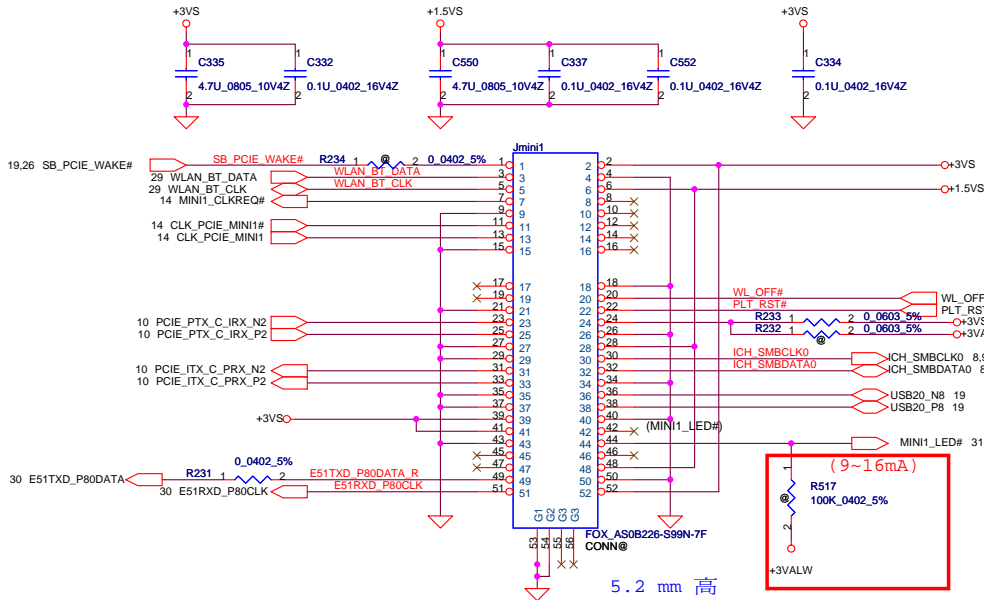
NOTE: L: A-->B1
H: A-->B2

LAN_ACTIVITY# R481 no docking@ 0.0402_5% L LAN_ACTIVITY#
LAN_LINK# R482 no docking@ 0.0402_5% L LAN_LINK#

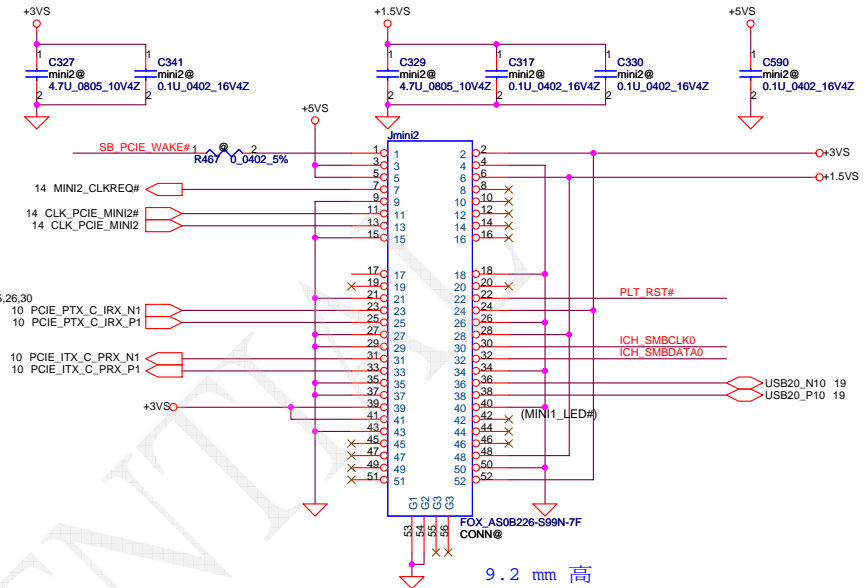


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For Wireless LAN

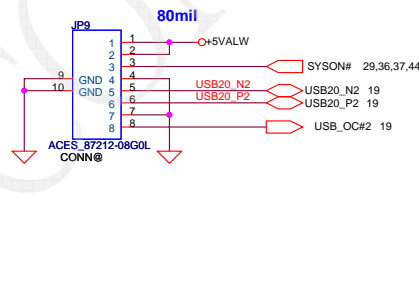


For TV-Tuner/HW MPEG

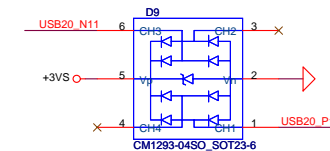
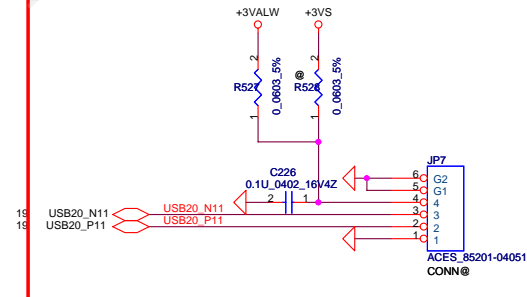


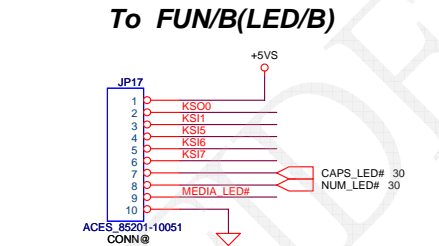
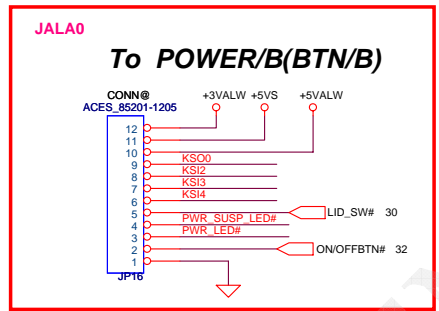
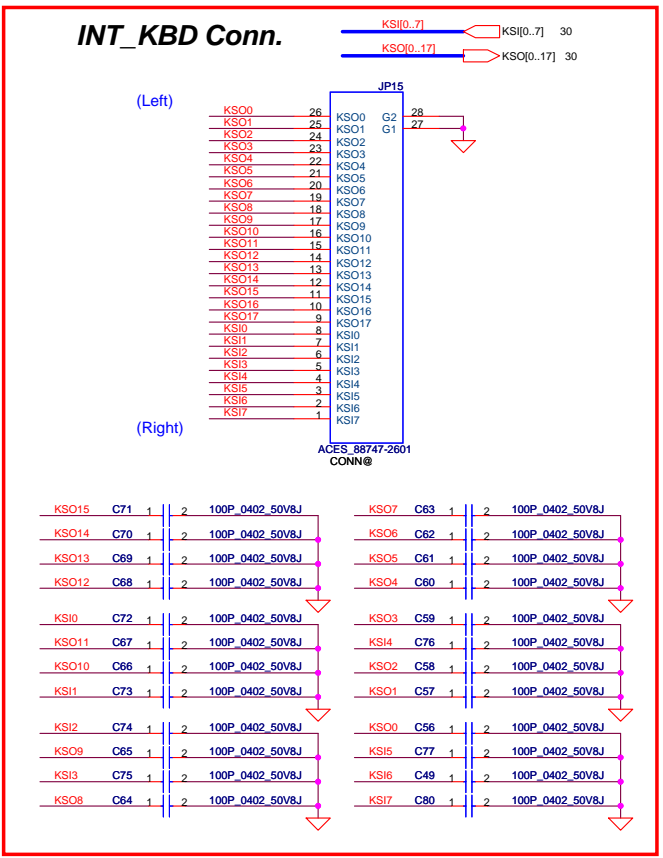
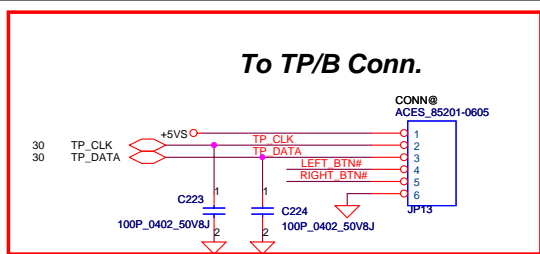
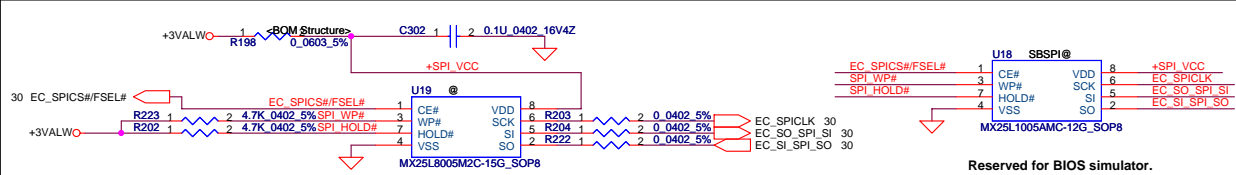
Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

To USB/B Connector

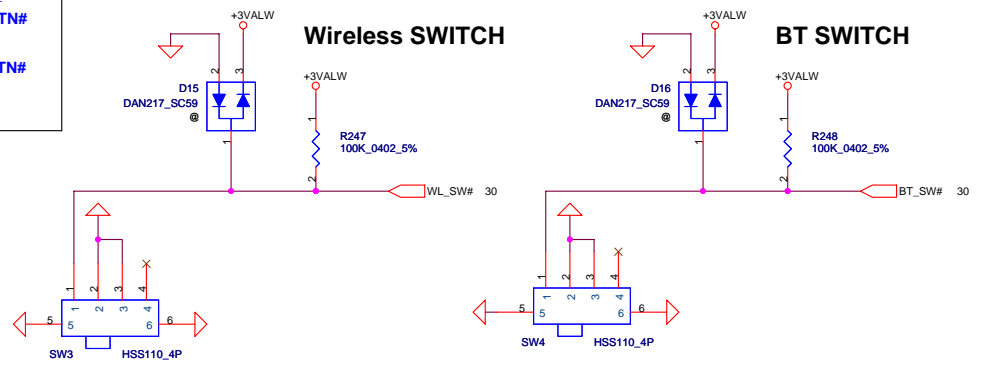
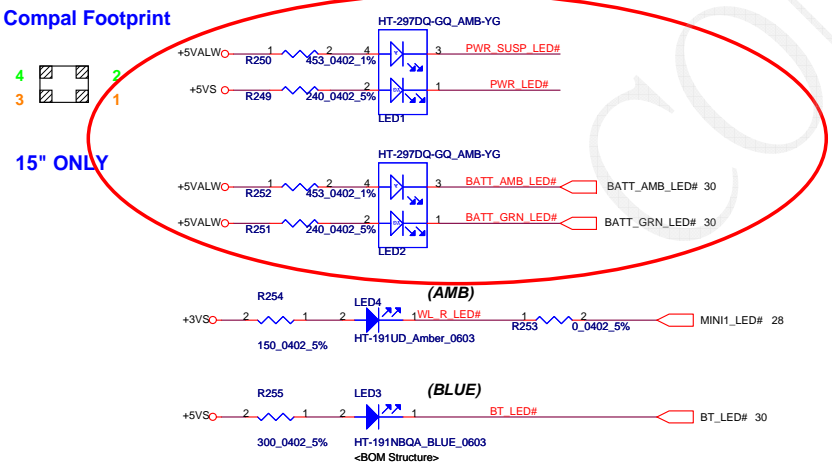
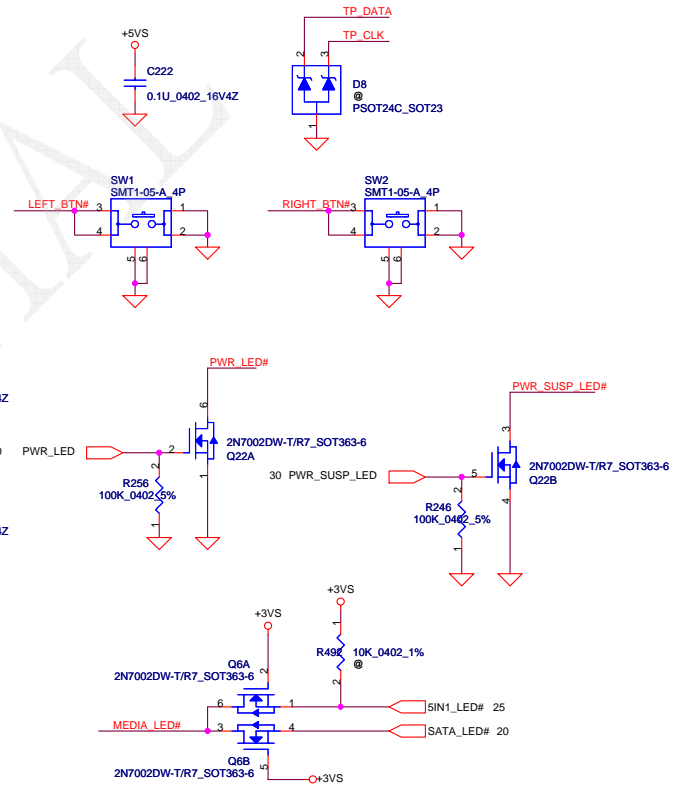


Fingerprint Conn





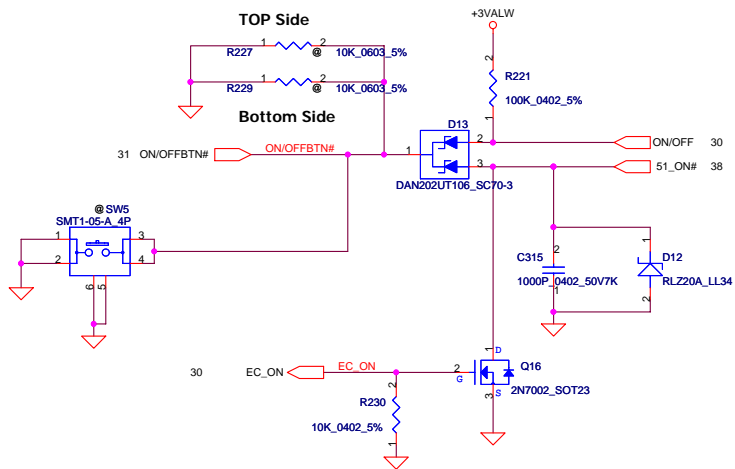
	KSO0
KSI1	PRESENTATION
KSI2	Program_BTN#
KSI3	EMAIL_BTN#
KSI4	IE_BTN#
KSI5	E-KEY_BTN#
KSI6	SYNC
KSI7	LOCK



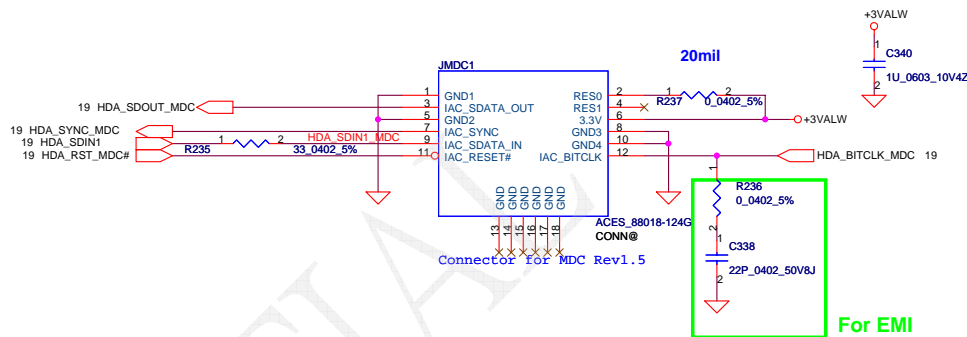
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Power Button

ON/OFF switch

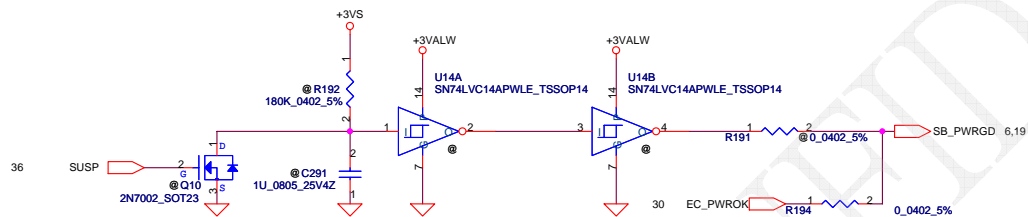


HDA MDC Conn.

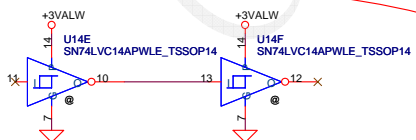
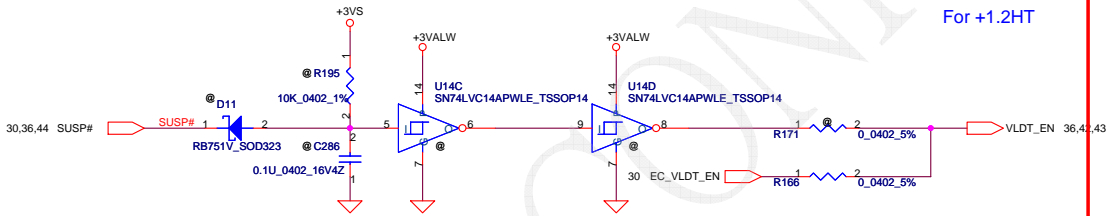


Power ON Circuit

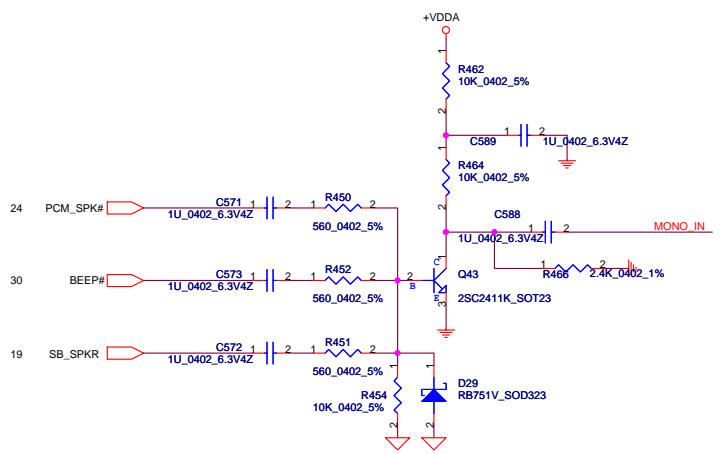
For South Bridge



For +1.2HT

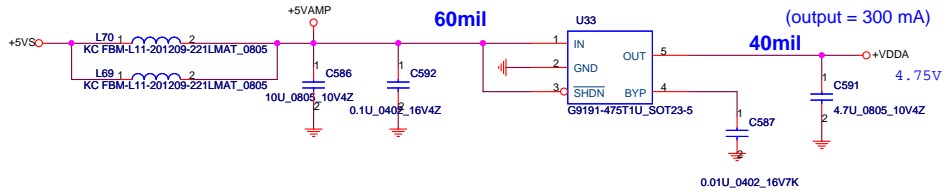


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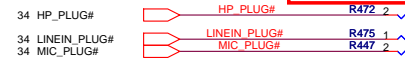
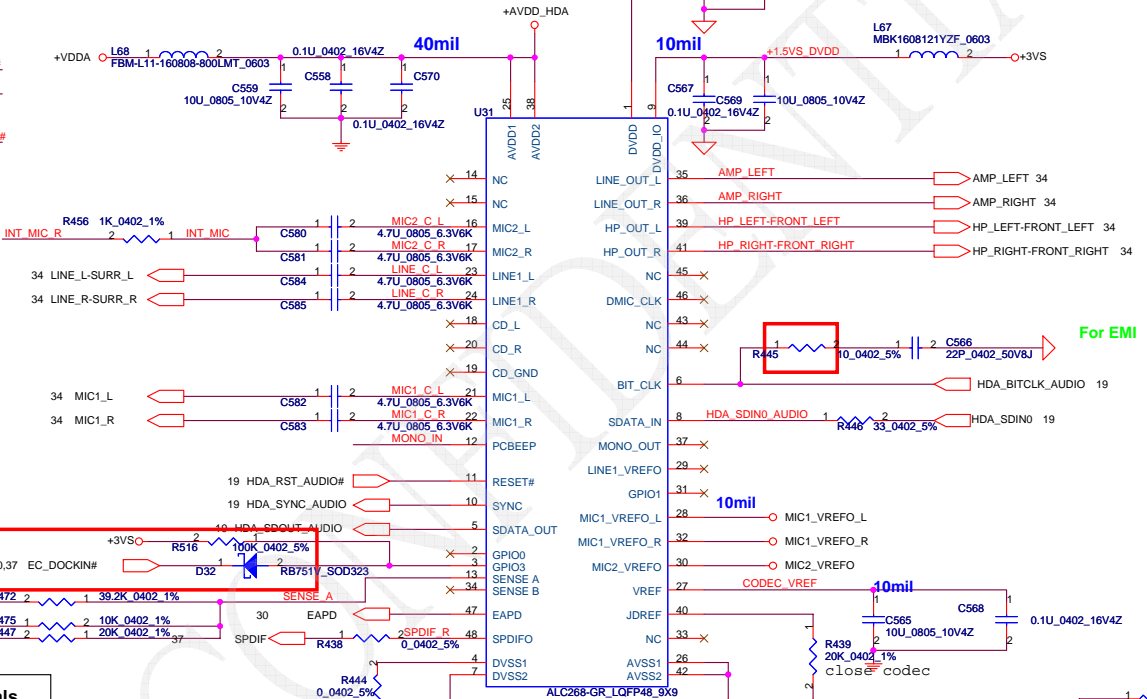


BOM Option

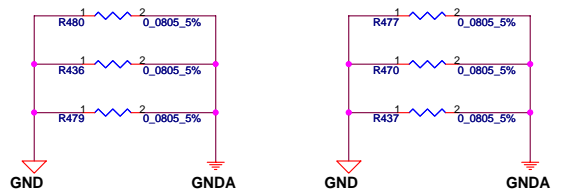
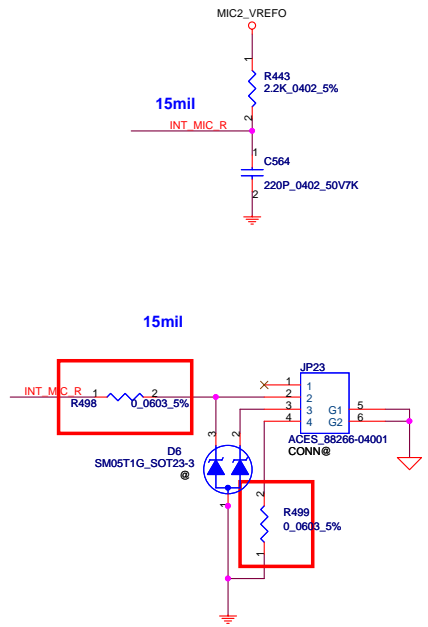
ALC268	268@
ALC888S-VC	888VC@



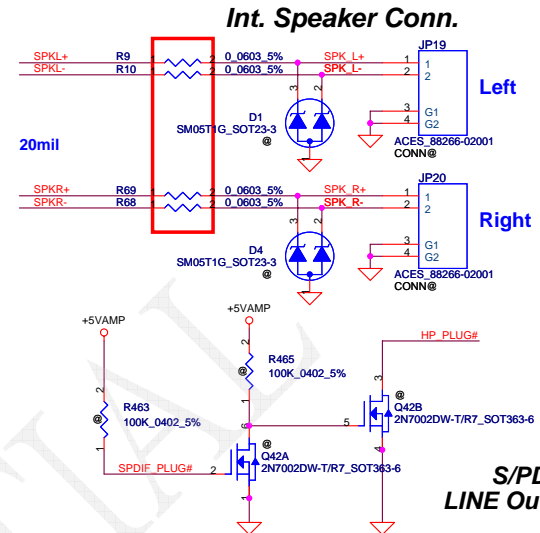
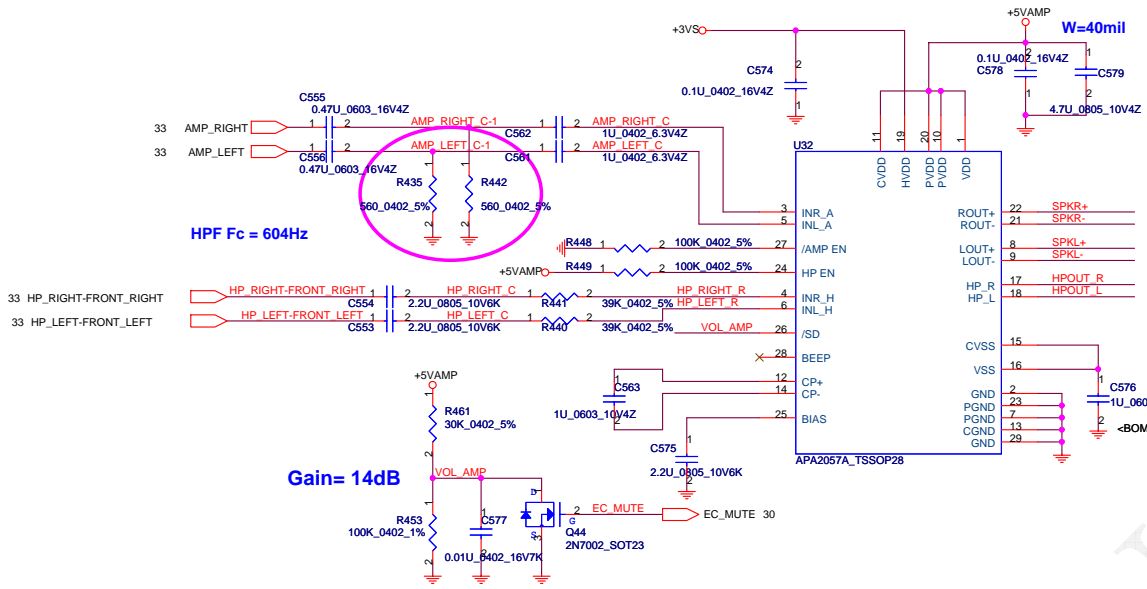
HD Audio Codec



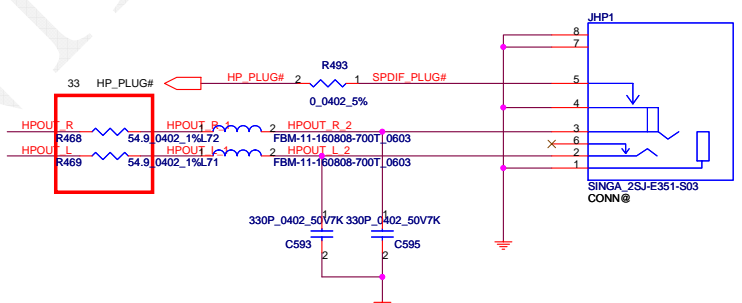
Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)



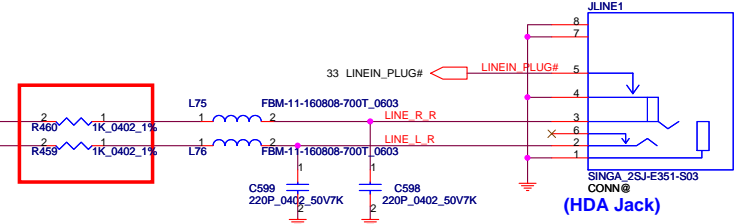
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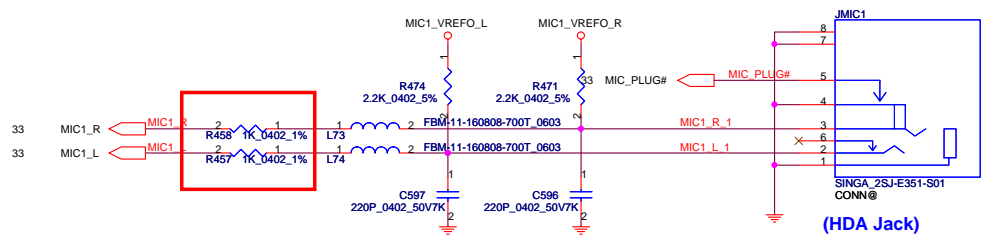
**S/PDIF Out JACK
LINE Out/Headphone Out**



LINE-IN JACK



MIC JACK



For Docking

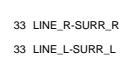
37 D_HPOUT_L \leftrightarrow D_HPOUT_L R278 Docking@ 47.0603.1% HPOUT_L
 37 D_HPOUT_R \leftrightarrow D_HPOUT_R R280 Docking@ 47.0603.1% HPOUT_R

For Docking

37 D_LINE_L \leftrightarrow D_LINE_L R274 Docking@ 47.0603.1% LINE_R-SURR_R
 37 D_LINE_R \leftrightarrow D_LINE_R R277 Docking@ 47.0603.1% LINE_L-SURR_L

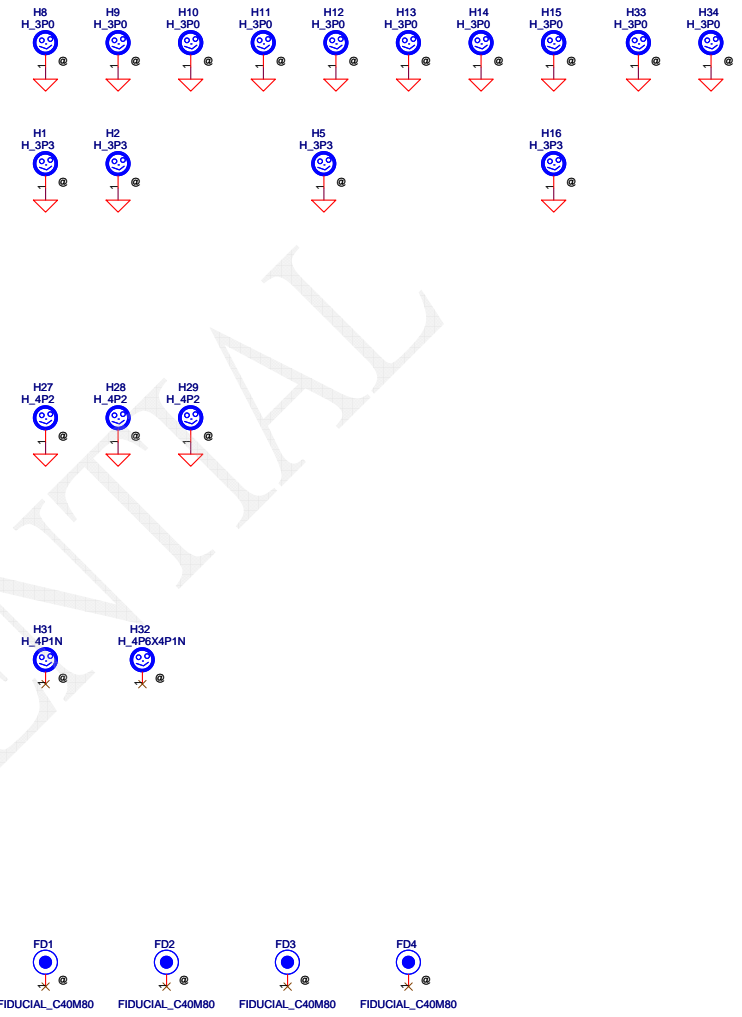
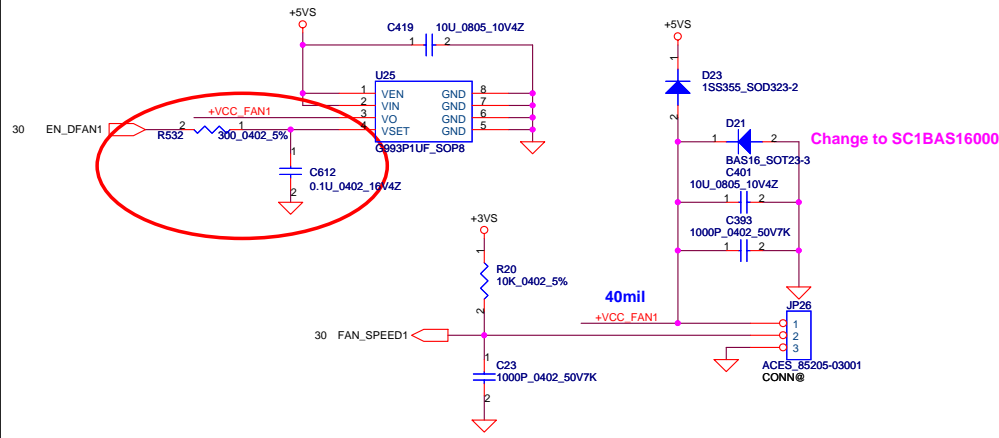
For Docking

37 D_MIC_L \leftrightarrow D_MIC_L R283 Docking@ 47.0603.1% MIC1_R
 37 D_MIC_R \leftrightarrow D_MIC_R R286 Docking@ 47.0603.1% MIC1_L



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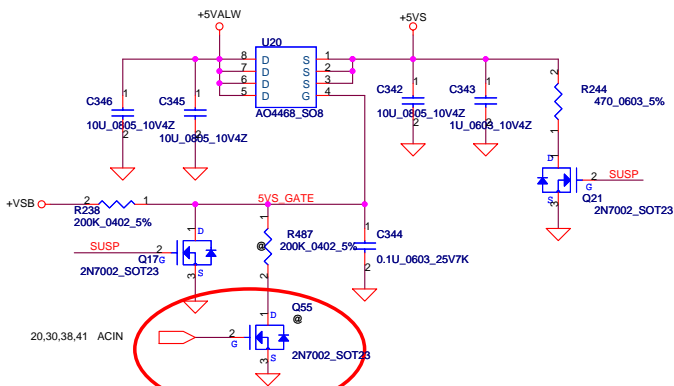
FAN1 Conn



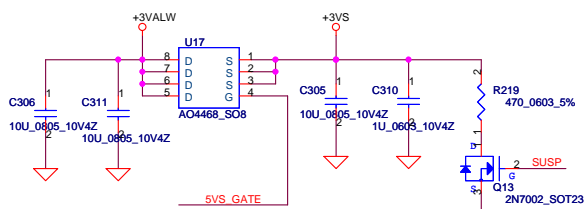
CONFIDENTIAL

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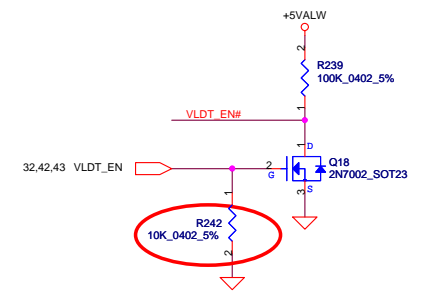
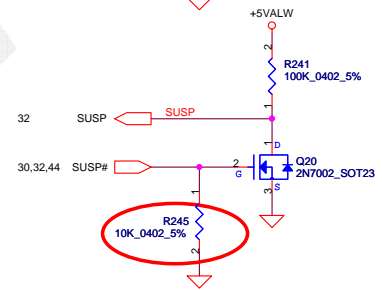
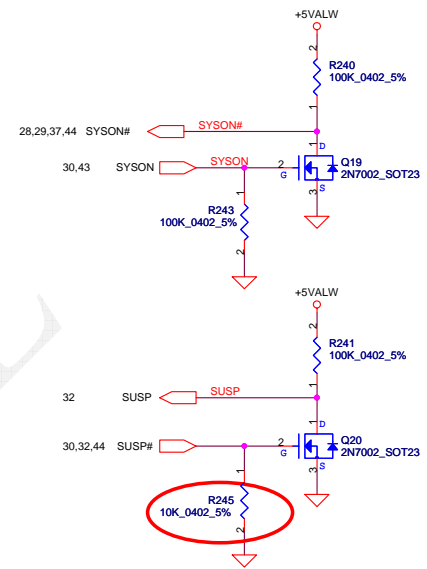
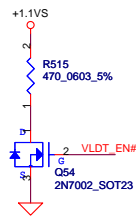
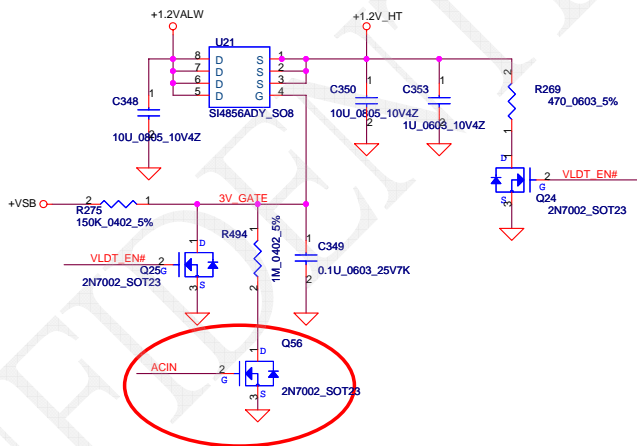
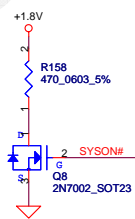
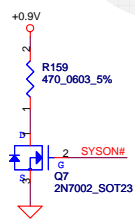
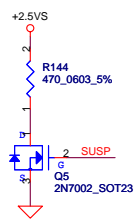
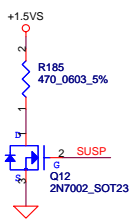
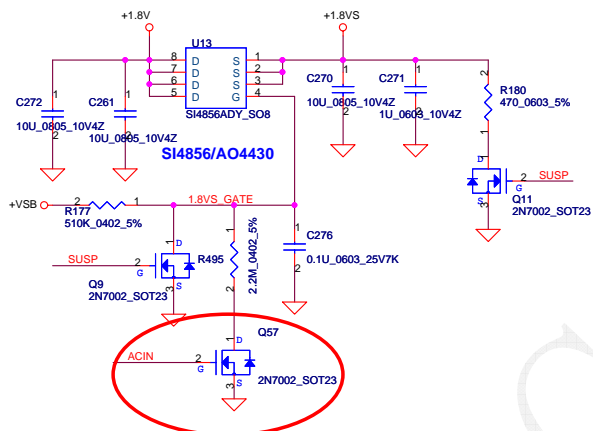
+5VALW TO +5VS



+3VALW TO +3VS

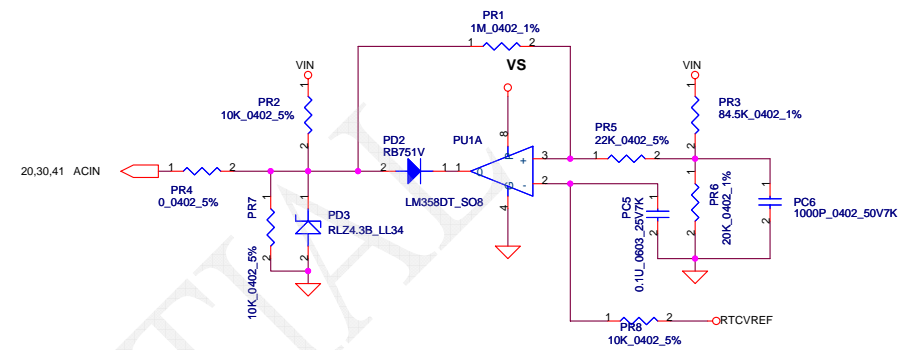
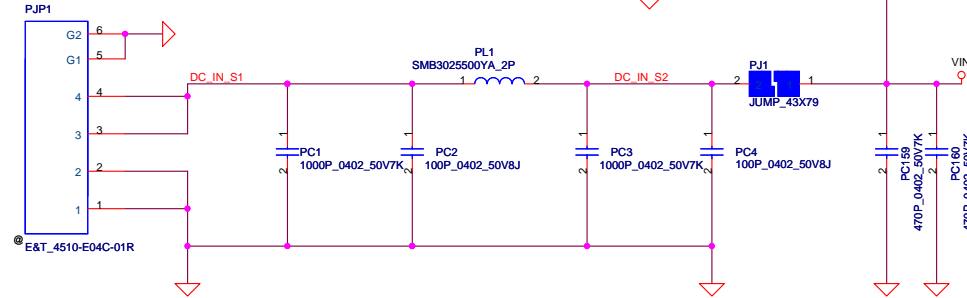


+1.8V to +1.8VS

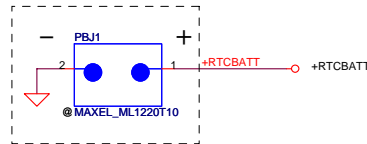


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SP02000EF00

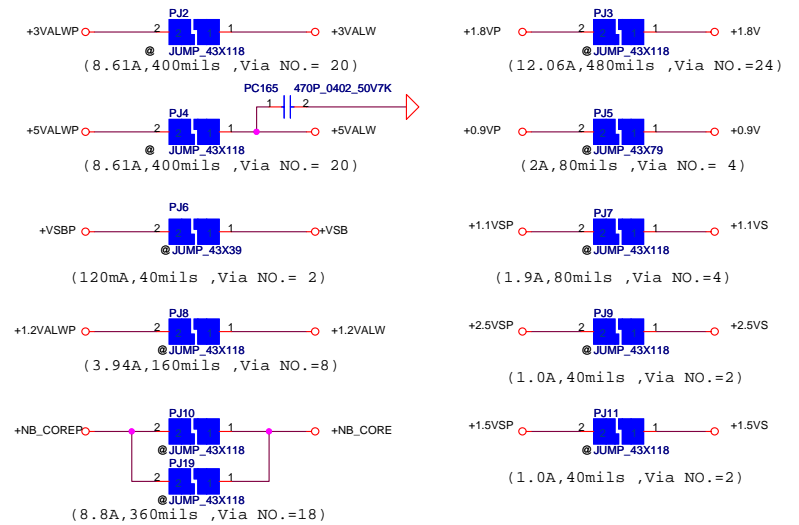
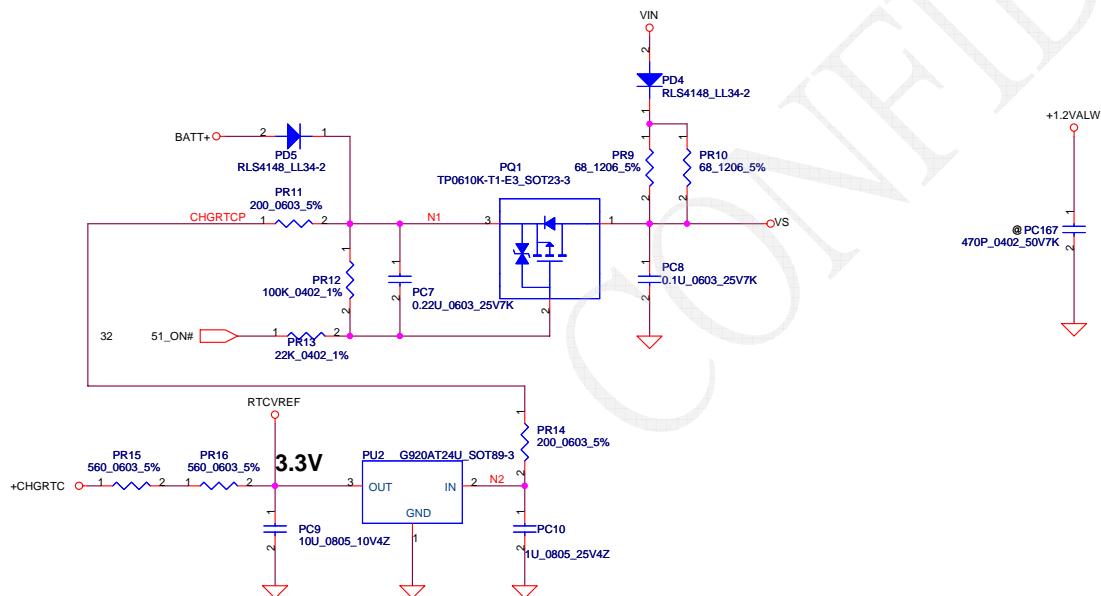


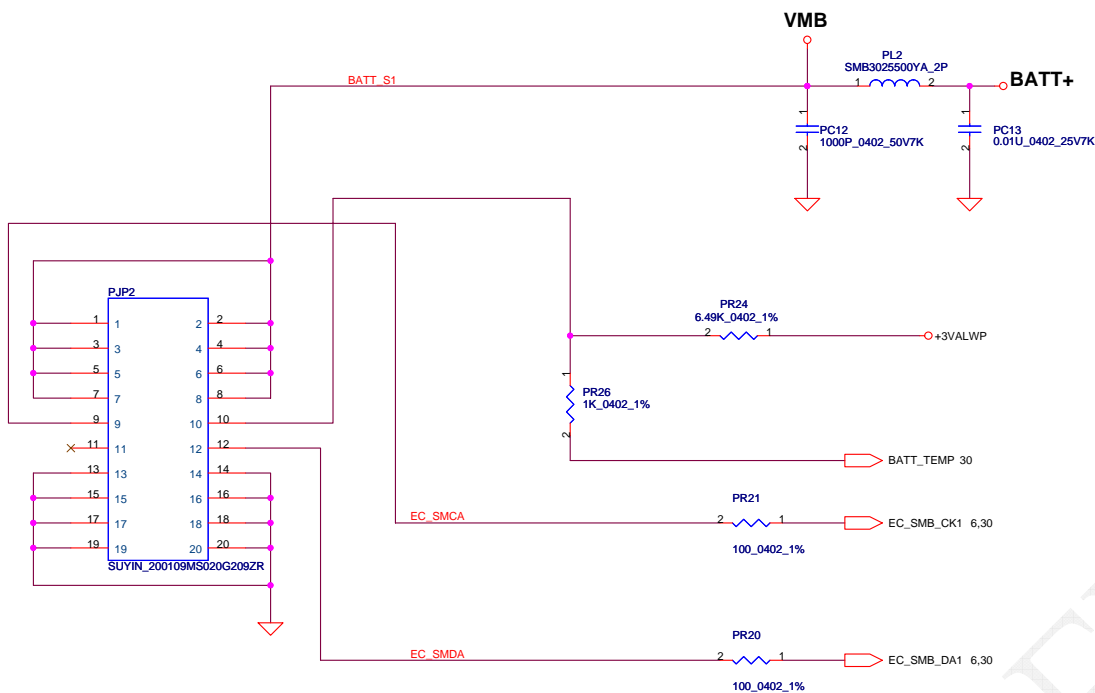
RTC Battery



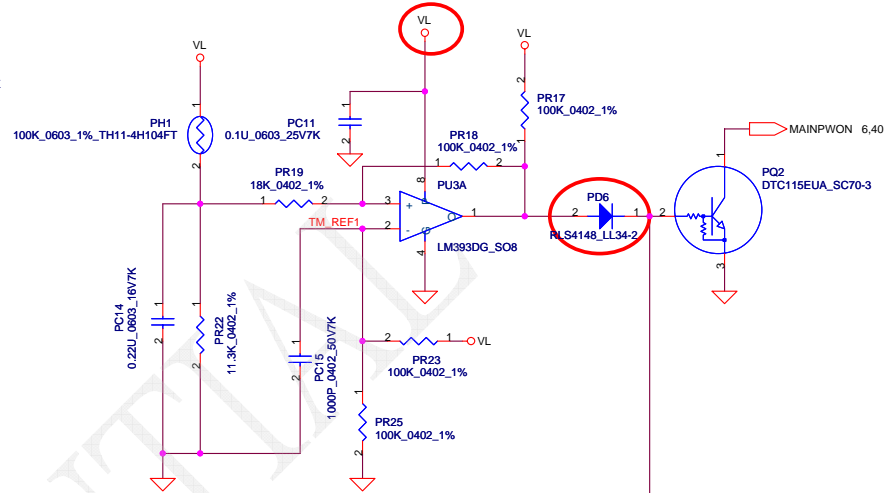
SP093MX000

Vin Detector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V

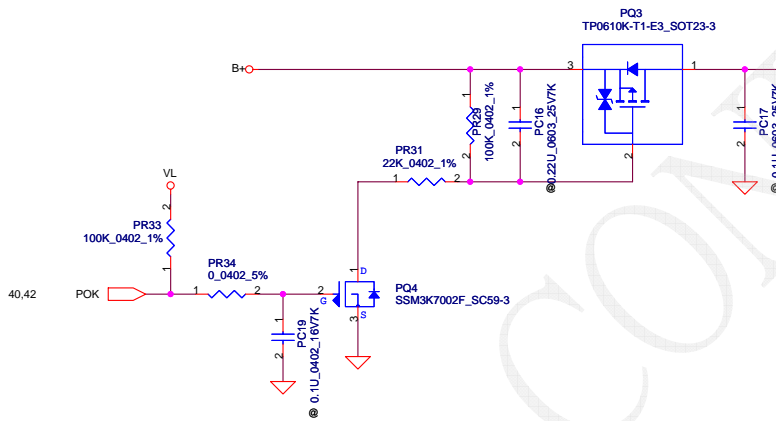
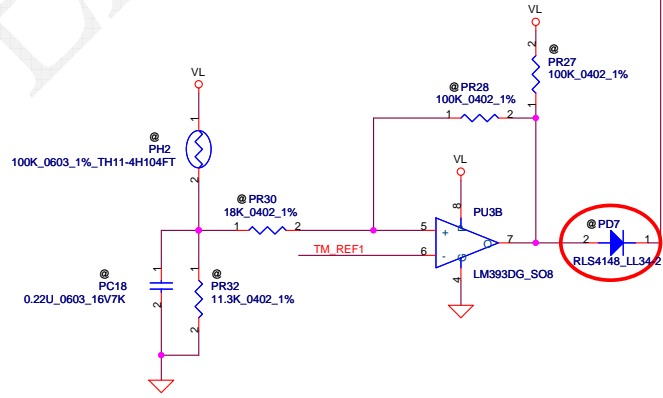




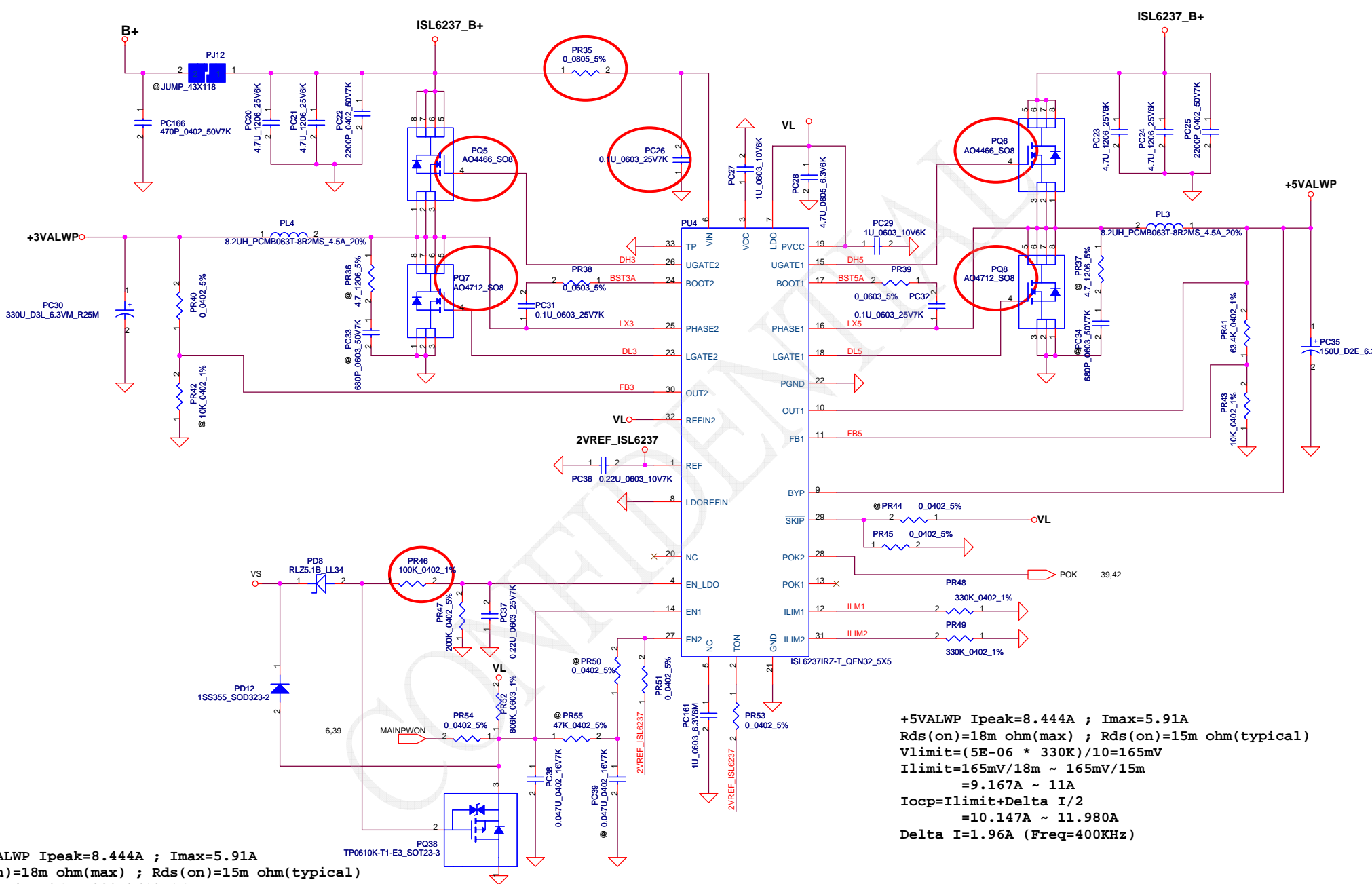
PH1 under CPU botten side :
 CPU thermal protection at 92 degree C
 Recovery at 56 degree C



PH2 near main Battery CONN :
 BAT. thermal protection at 92 degree C
 Recovery at 56 degree C



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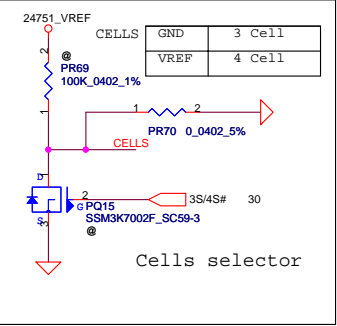


+3.3VALWP Ipeak=8.444A ; Imax=5.91A
 Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
 Vlimit=(5E-06 * 330K)/10=165mV
 Ilimit=165mV/18m ~ 165mV/15m
 =9.167A ~ 11A
 Iocp=Ilimit+Delta I/2
 =10.134A ~ 11.967A
 Delta I=1.934A (Freq=300KHz)

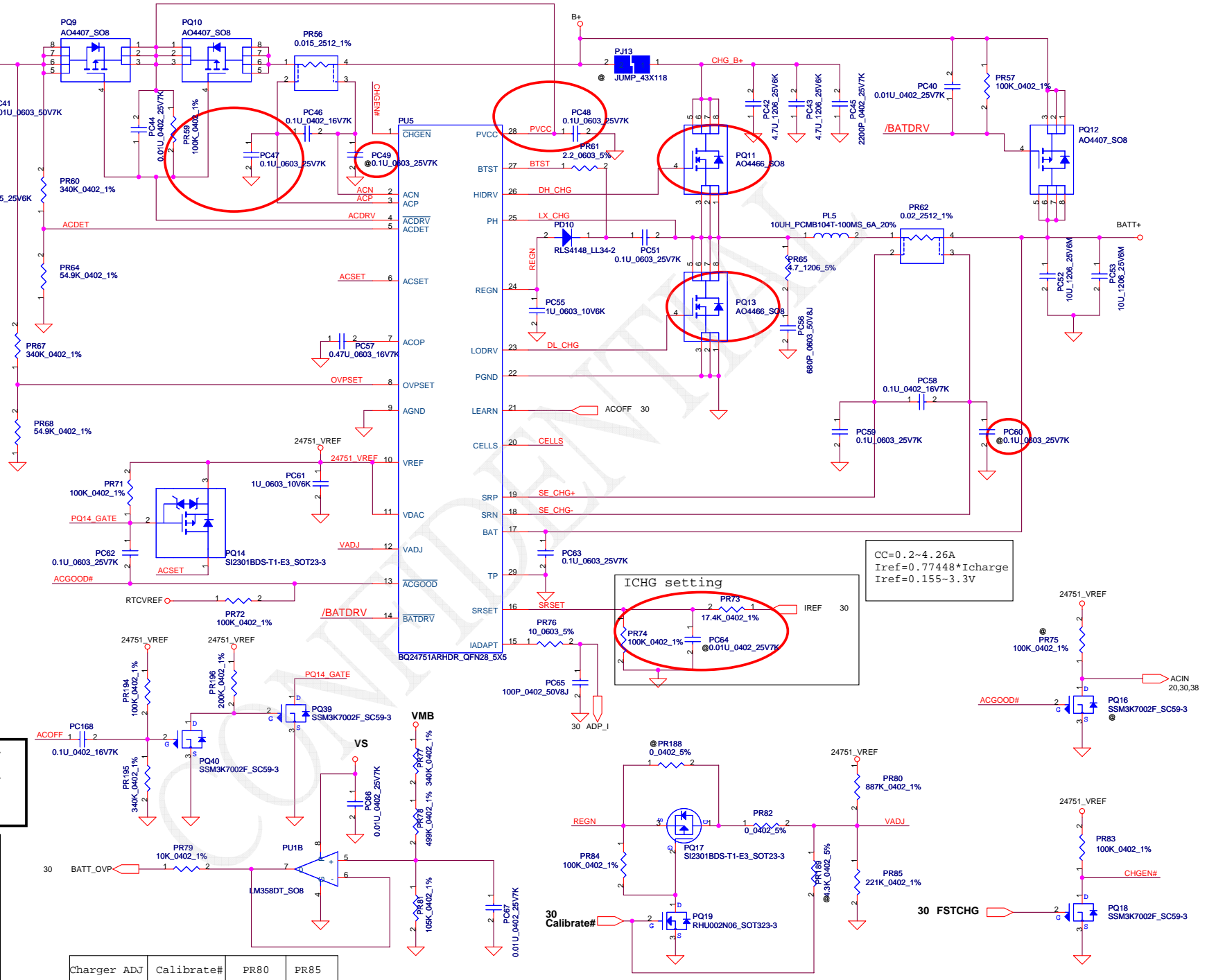
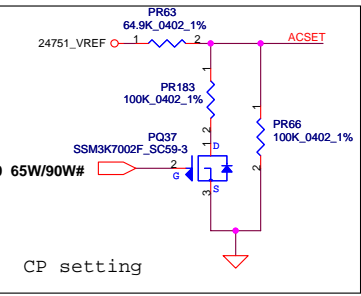
+5VALWP Ipeak=8.444A ; Imax=5.91A
 Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
 Vlimit=(5E-06 * 330K)/10=165mV
 Ilimit=165mV/18m ~ 165mV/15m
 =9.167A ~ 11A
 Iocp=Ilimit+Delta I/2
 =10.147A ~ 11.980A
 Delta I=1.96A (Freq=400KHz)

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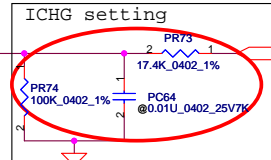
$I_{charge} = (V_{srset} / V_{vdac}) * (0.1 / PR36)$
 90W adapter
 $I_{adapter} = (V_{vacset} / V_{vdac}) * (0.1 / PR48) = 4.04A$
 65W adapter
 $I_{adapter} = (V_{vacset} / V_{vdac}) * (0.1 / PR48) = 2.90A$
 Input OVP : 22.3V
 Input UVP : 17.26V
 Fsw : 300KHz



LI-3S : 13.5V --- BATT-OVP=1.5V
LI-4S : 18V --- BATT-OVP=1.998V
BATT-OVP=0.111 * BATT+



CC=0.2~4.26A
 $I_{ref} = 0.77448 * I_{charge}$
 $I_{ref} = 0.155 \sim 3.3V$

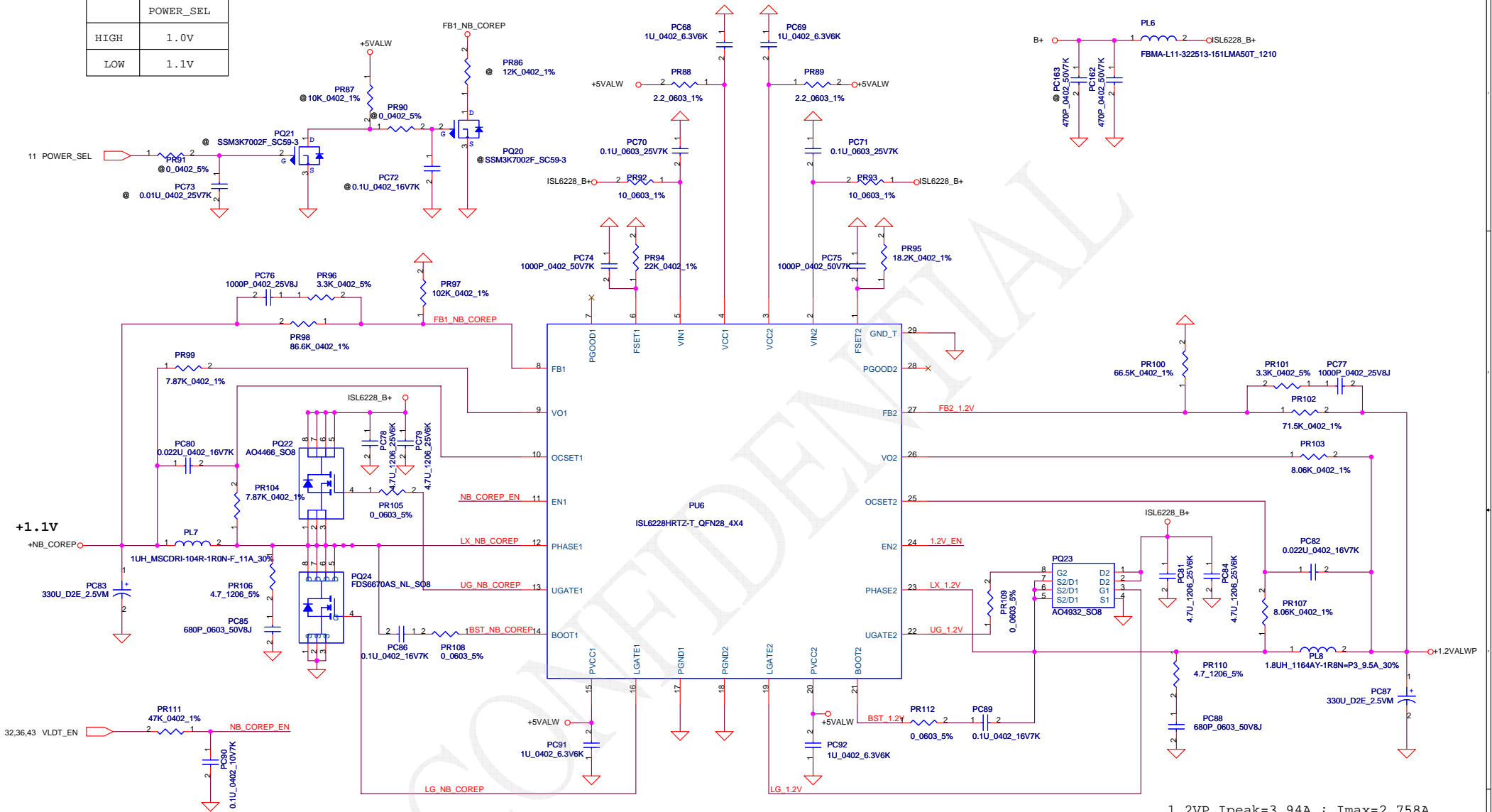


Charger ADJ	Calibrate#	PR80	PR85
4.0V	L	@	0
4.1V	L	887K	221K
4.2V	H	887K	221K

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	POWER_SEL
HIGH	1.0V
LOW	1.1V

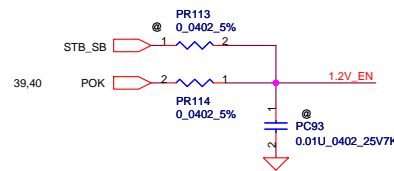


1.1VP Ipeak=8.9A ; Imax=6.23A
 DCR=6m ohm (max)
 $R_{ocset} = (I_{ocp} * DCR) / 10E-06 = 7.87K \text{ ohm}$
 $I_{ocp} = 10.089A (1.3 * DCR)$
 $C_{sen} = L / (R_{ocset} * DCR) = 0.022uF$

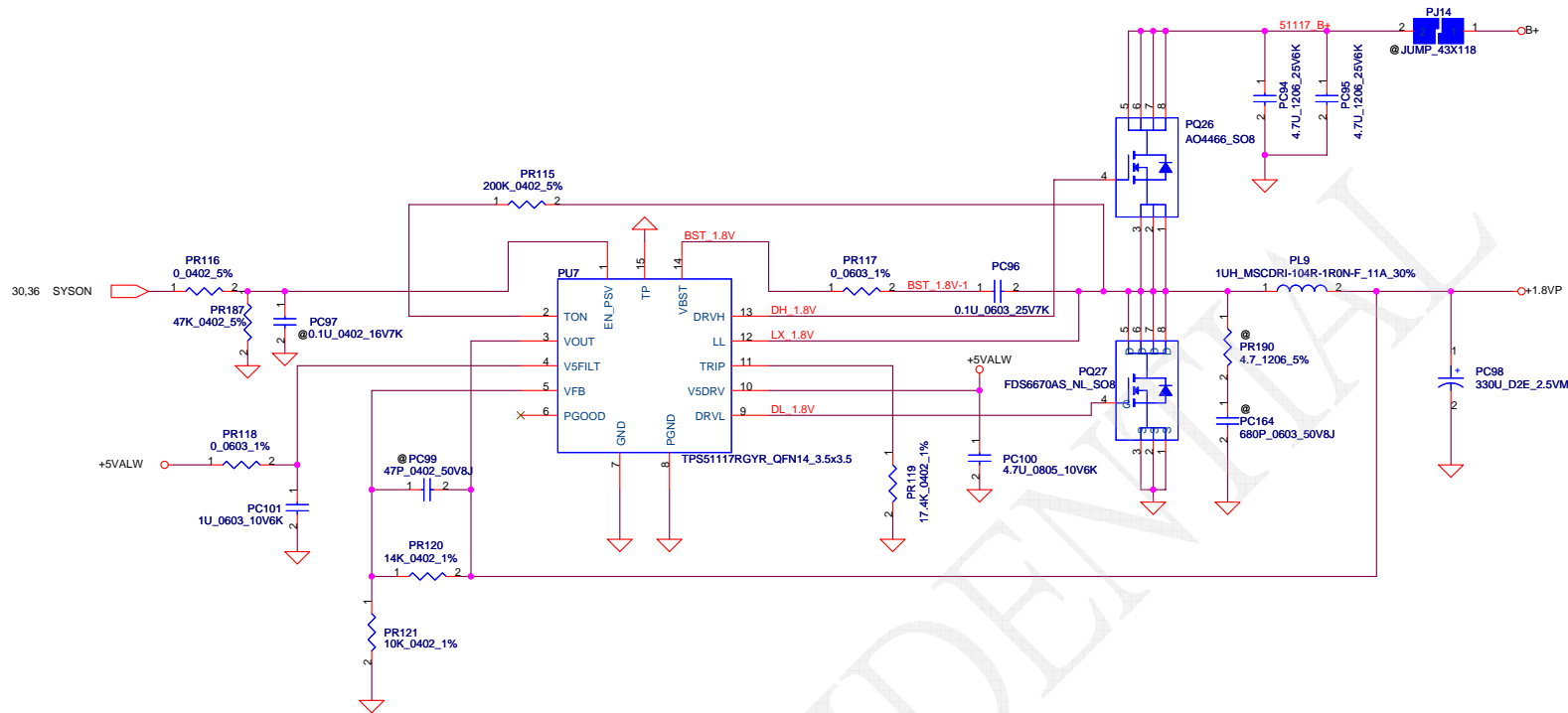
Freq=303KHz
 $R_{fset} = 1 / (1.5E-10 * Freq) = 22K$

1.2VP Ipeak=3.94A ; Imax=2.758A
 DCR=10m ohm (max)
 $R_{ocset} = (I_{ocp} * DCR) / 10E-06 = 8.06K \text{ ohm}$
 $I_{ocp} = 6.716A (1.2 * DCR)$
 $C_{sen} = L / (R_{ocset} * DCR) = 0.022uF$

Freq=366KHz
 $R_{fset} = 1 / (1.5E-10 * Freq) = 18.2K$

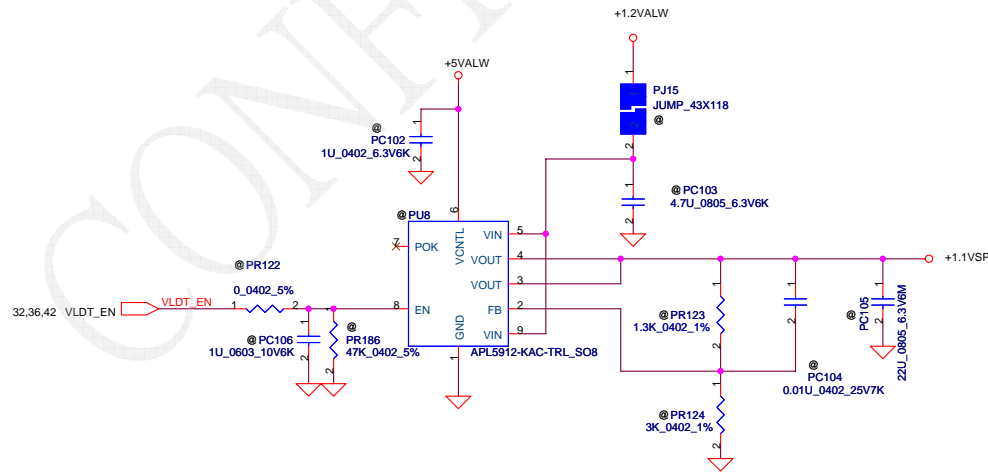


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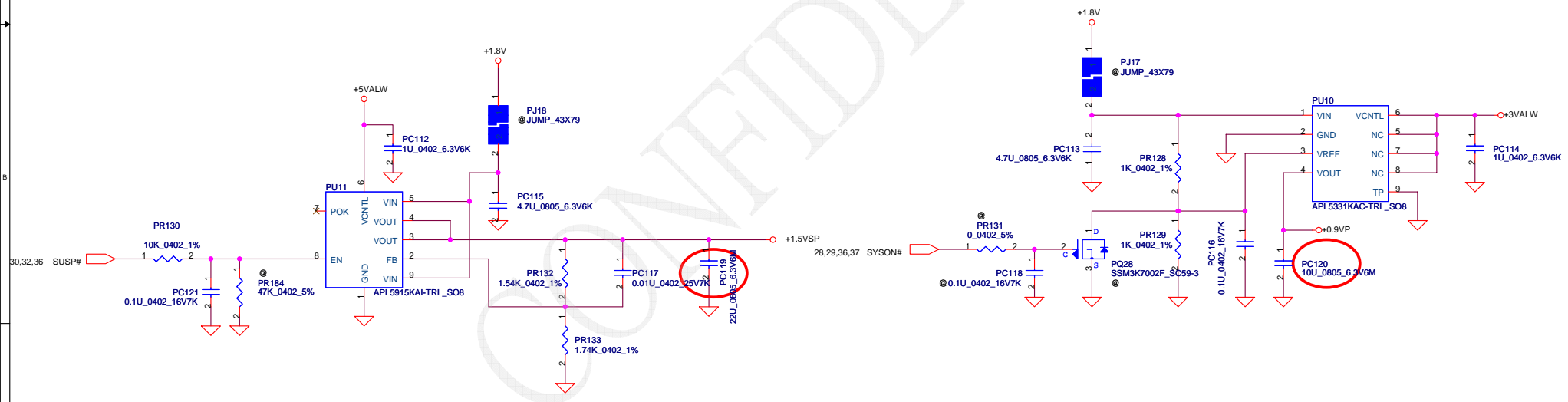
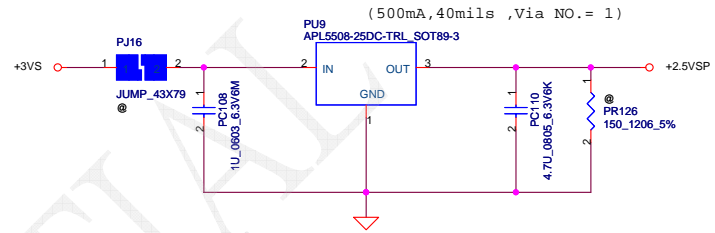


$V_{FB} = 0.75V$
 $V_o = V_{FB} * (1 + PR120 / PR121) = 1.8V$
 $T_{on} = 19E-12 * Ron * ((2/3) * V_o + 100mV) / (V_{in}) + 50ns = 3.1E-07$
 $Freq = 305KHz$

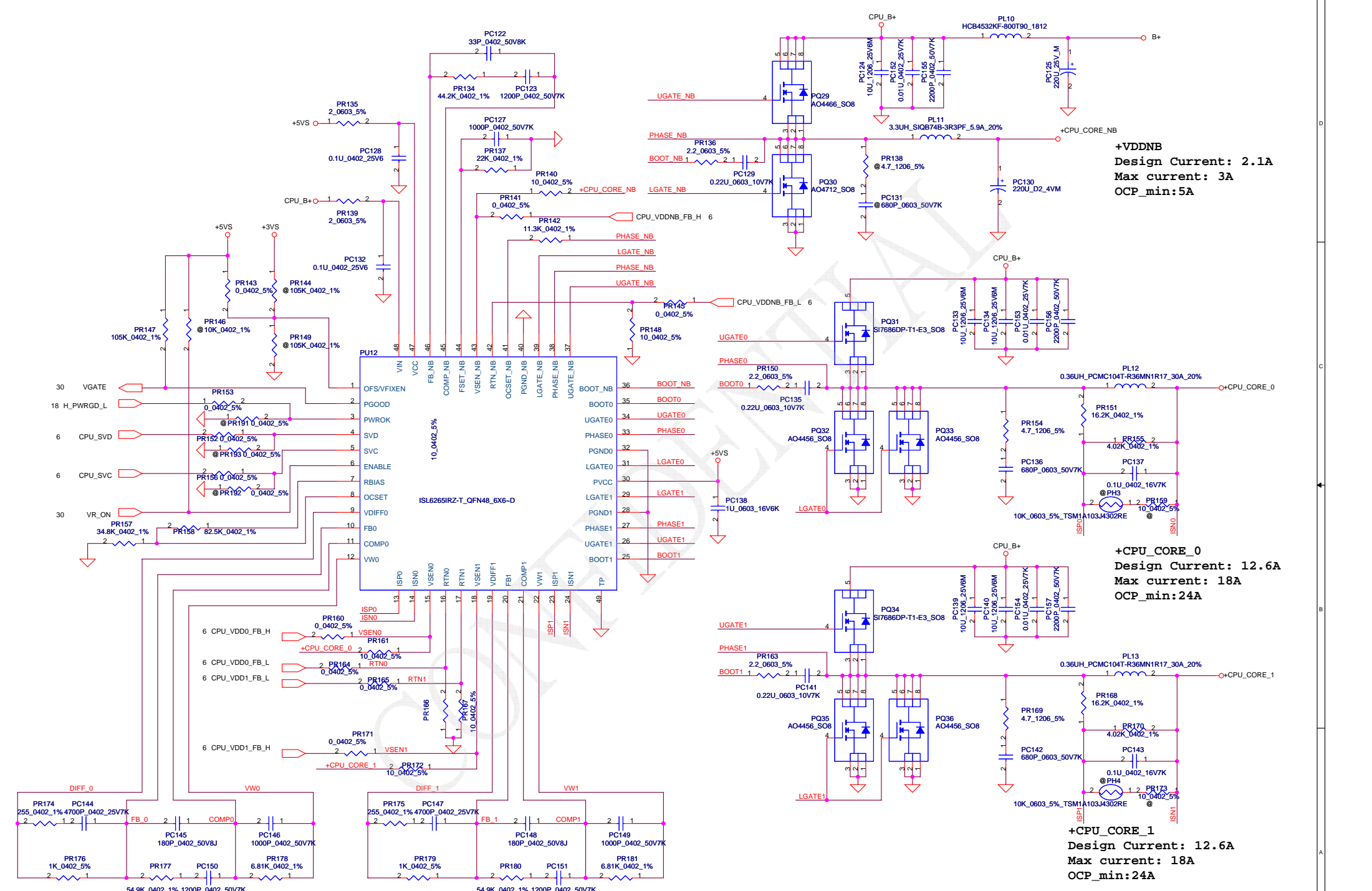
$C_{esr} = 15m \text{ ohm}$
 $I_{peak} = 12.6A$ $I_{max} = 8.82A$
 $\Delta I = ((19 - 1.8) * (1.8/19)) / (L * Freq) = 5.332A$
 $V_{trip} = R_{trip} * I_{0uA} = 0.24V$
 $I_{ocp_min} = V_{trip} / R_{ds_on_max} * 1.4 + 2.666 = 17.573A$
 $I_{ocp_max} = V_{trip} / R_{ds_on_typ} * 1.2 + 2.666 = 26.908A$
 $I_{ocp} = 17.573 - 26.908A$



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+VDDNB
 Design Current: 2.1A
 Max current: 3A
 OCP_min:5A

+CPU_CORE_0
 Design Current: 12.6A
 Max current: 18A
 OCP_min:24A

+CPU_CORE_1
 Design Current: 12.6A
 Max current: 18A
 OCP_min:24A

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NO DATE	PAGE	MODIFICATION LIST	PURPOSE
7/9	DCIN	Change PL1 to bead coil	link to SM010008E10
7/9	DCIN	Link RTC battery symbol	link to SP093MX0000
7/9	Battery conn	Change PL2 to bead coil	link to SM010008E10
7/9	Battery conn	Change PD3,PD4 to RLS4148	For low cost
7/9	Battery conn	Change PU2 pin8 to VL	Design change
7/9	Charger	Delete PU3 PVCC resistor and change PC26 to 1U	avoid PQ6 false turn-on when AC plug-in
7/9	Charger	Change PQ7,PQ9 to AO4466	For low cost
7/9	Charger	Change PU4 pin8 to +5VALW	Design change
7/9	Charger	Unpop PC28, PC37	avoid interfere by other signal
7/9	3V/5V	Change PR54 and PC51	Add design margine
7/9	3V/5V	Change MOSFET to AO4466+AO4712	For low cost
7/9	1.8V/1.5V	Change MOSFET to AO4466+AO4712	For low cost
7/9	1.8V/1.5V	Change PR75 to 2.2ohm	Design change
7/9	1.05V/1.25V/0.9V	Change MOSFET to AO4466+AO4712	For low cost
7/9	1.05V/1.25V/0.9V	Change PC94 to 330U	Decrease overshoot
7/9	1.05V/1.25V/0.9V	Change PU7 PVCC source to +5VS	Design change
7/9	1.05V/1.25V/0.9V	Change PC105,PC108 size to 0805	For low cost
7/9	CPU CORE	Change input MLCC to 4pcs	Design change
7/9	CPU CORE	Unpop PC111	Reserve for high frequency noise
7/10	Charger	Change PR38, PR39 and unpop PC32	increase resistor to reduce power loss on resistor divider
7/10	Charger	Change PR45, PR47 and unpop PC41	increase resistor to reduce power loss on resistor divider
7/10	Charger	Change PR43 to 100K	increase resistor to reduce power loss
7/10	3V/5V	Change PR65 to 100K_1%	Let BOM clear
7/10	Charger/0.9V	Change PQ4,PQ11,PQ12,PQ13,PQ24 to SB000009080	For low cost
8/1	Charger	Change PR30 to 0.015ohm and PR38 to 80.6K	Change over power protection point

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12/19		P.6	Change C500 p/n	common part
		P.6	R403, R402,R103 pull +1.8VS	
		P.6	unpop Q32, Q33,R344,R348,C410	voltage leakage issue
		P.6	CPU_test21, CPU_test24 pull low 300 ohm, CPU_DBREQ#pull high 300 ohm +1.8V	CPU issue
		P.7	C517 change p/n	common part
		P.11	U22.B8 and U22.A8 swap	HDMI I2C error
		P.11	R411 pull +1.8VS	voltage leakage issue
		P.12	POP L20 , Del L19 and +1.35V circuit	fixed chipset ver:All issue
		P.15	pop R187 , del R188	fixed system unstable issue
		P.16	C351 type change form 0603 to 0402	common part
		P.17	Q3, Q26 change to BSH111	common part
			R273,R276 change to 2K	DVI issue
			pop R80 , del R362,R357,R352,R353,R354,R355	common part
			change Q4,Q36,Q37,Q38 p/n	common part
		P.18	change D22 p/n	common part
			Change Q29 p/n	common part
		P.19	POP U11, C235, del R134	add driving
		P.20	add CR_PE# , CR_WAKE# net	JM385 D3e function
		P.21	Change CRT_det pin	for coding
		P.21	change R377 to 100k	for AC LED issue
		P.22	POP R413, Del R415	fixed chipset ver:All issue
		P.23	change R88 to 2.2k	fixed can't boot issue
		P.25	U30,46 connect to PCI_AD0, U30.127 connect to R434	fixed PCMCIA card issue
		P.26	add CR_PE# , CR_WAKE# net	JM385 D3e function
		P.26	DEL L65	use J385 internal power fn.
		P.27	del colayout 5787 circuit	for IEEE fail issue
		P.28	change T1 p/n	common part
		P.29	Del TV_therm net	no need in the circuit
		P.30	del USB_OC#1 net and C514, R413	no need in the circuit
		P.31	U16.76 as NC pin	no need in the circuit
		P.31	pop C284	for KB926 C0 version
		P.32	change SW3, SW4 p/n and circuit	ID desing change
		P.33	del R177 , pop R166	udpate sequency
		P.35	change C553,C554 to 2.2 u	for audio performance issue
		P.35	Change JHP1 connector package	ID desing change
		P.37	add R487,R494,R495	design change
		P.38	update docking pin define	common design
		P.38	del R271, change R272 to 0 ohm	for DVI detect issue

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1/31 P.6 POP CPU internal themal sensor schematic

1/31 P.11 change R55 to 133 ohm

1/31 P.14 Add C601

1/31 P.19 Change CRT_DET to U10.H7

1/31 P.33 Change R500 to D32, add R516

1/31 P.34 Change HP left and right chanel

1/31 P.36 reserve ACin sigal to power MOS

2/13 P.28 add R517 pull high at mini card

2/13 P.31 updated LED1, LED2 symbol

2/13 P.30 add R518 100k pull low on VR_ON

2/14 P.6 add R519, R520,521,522,R523,R524 in DTS

3/24 P.33 For EMI request,Change R445 to SD028100A80

3/24 P.12 Change C95,C139,C129,C44,C26,C15,C16,C17,C18 to SE000000I10 (22U)

3/24 P.19 change USB port

4/16 P.34 change R278,R280,R274,R277,R283,R286 to 47 ohm

4/16 P.6 reserve memhot# pull high

4/16 P.18 reserve proshot# pull high +3VS at S/B

4/16 P.19 reserve GPIO5 pull high at S/B

4/23 P.20 reserve R613

4/28 P.6 DTS unpop , del C410,R344, R348, R520,R522, Q32, Q33

4/28 P.6 del R528 , pop R527, change finger printer power

5/19 P.25 add R533,C616 delay circuit for ASF

5/19 P.23 add C614,C615 for ESD issue

6/2 P.30 board ID change

6/2 P.30 add CR_PE delay signal to card reader

7/21 P.7 add C149 and change to SGA00001Q80 for CRT issue

7/21 P.36 add Q56 , Q57 ; add R494 and change to SD028100480 ;
add R494 and change to SD028100480 ; add R4945 and change to SD028220480 for power issue

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