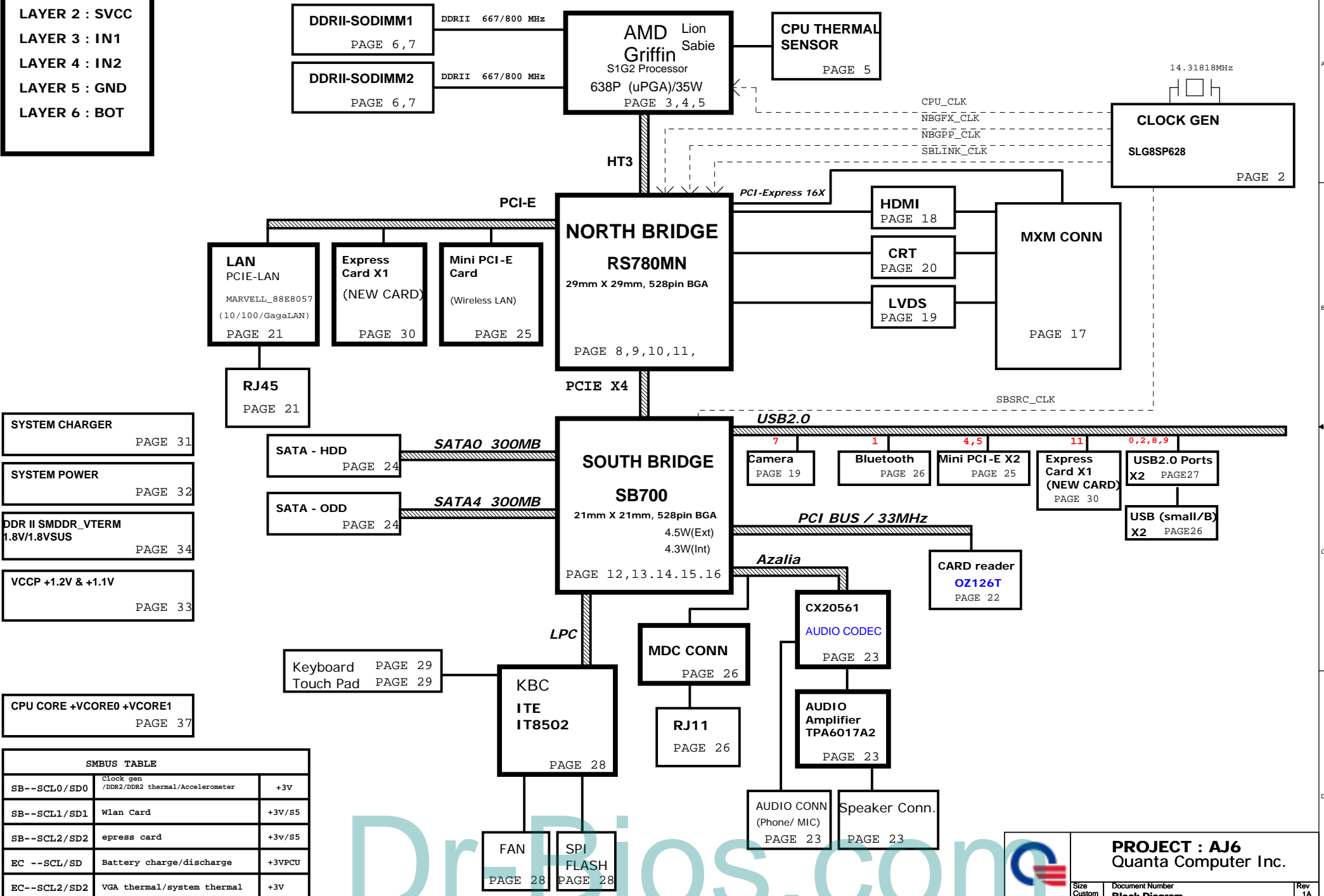


**PCB STACK UP**

- LAYER 1 : TOP
- LAYER 2 : SVCC
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : GND
- LAYER 6 : BOT

# AJ6 SYSTEM DIAGRAM



- SYSTEM CHARGER PAGE 31
- SYSTEM POWER PAGE 32
- DDR II SMD DR\_VTERM 1.8V/1.8VSUS PAGE 34
- VCCP +1.2V & +1.1V PAGE 33

CPU CORE +VCORE0 +VCORE1 PAGE 37

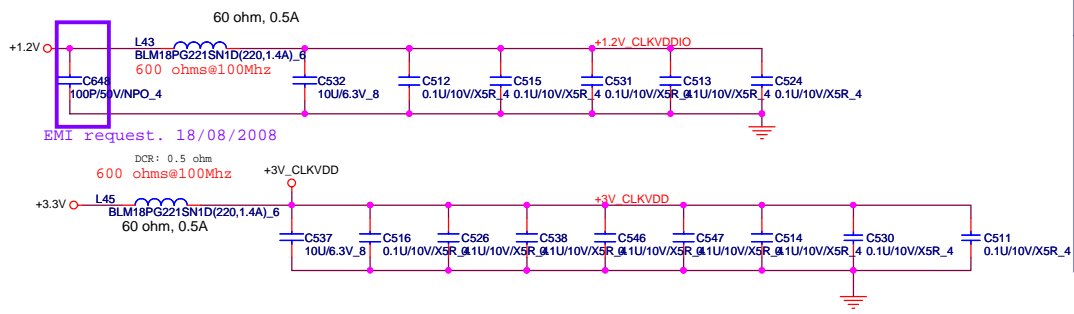
SMBUS TABLE		
SB--SCL0/SD0	Clock gen /DDR2/DDR2 thermal/Accelerometer	+3V
SB--SCL1/SD1	Wlan Card	+3V/S5
SB--SCL2/SD2	epress card	+3v/S5
EC --SCL/SD	Battery charge/discharge	+3VPCU
EC--SCL2/SD2	VGA thermal/system thermal	+3V

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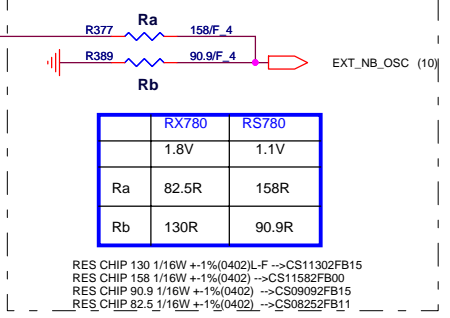
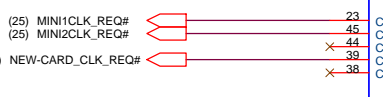
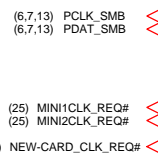
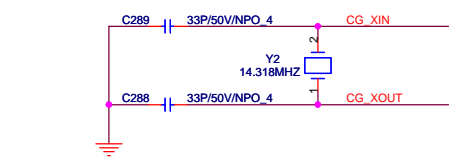
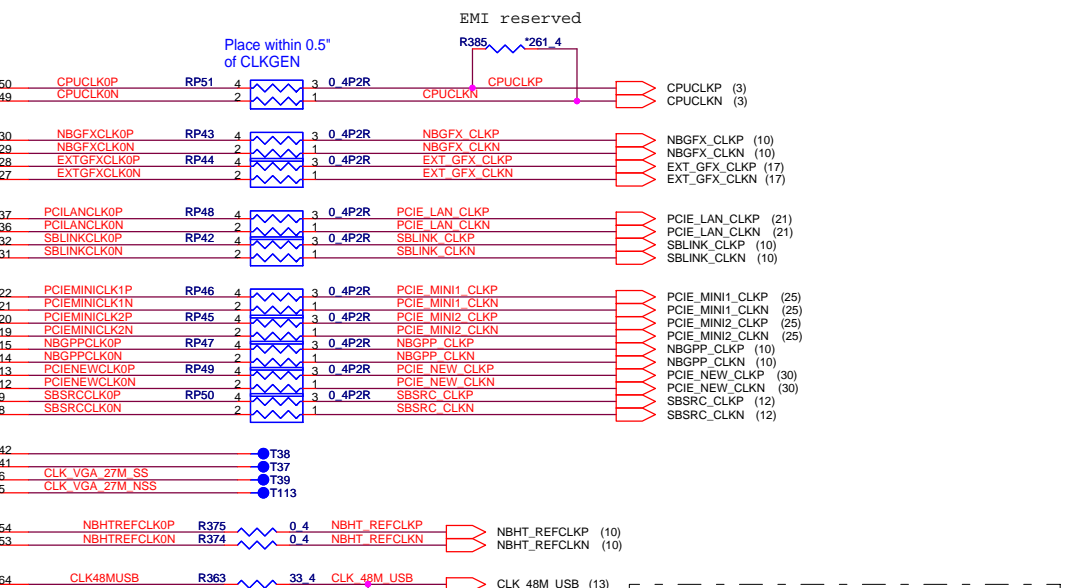
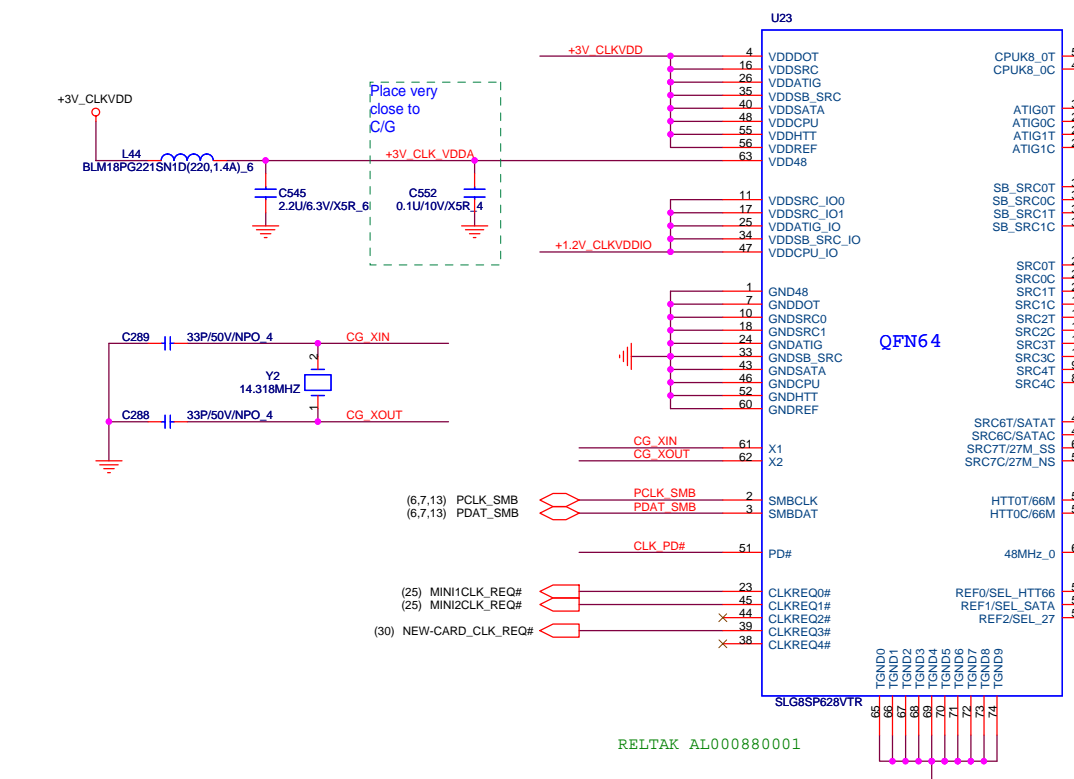
**PROJECT : AJ6**  
Quanta Computer Inc.

Size Custom	Document Number <b>Block Diagram</b>	Rev 1A
Date: Monday, August 18, 2008		Sheet 1 of 39

NB2/RD1



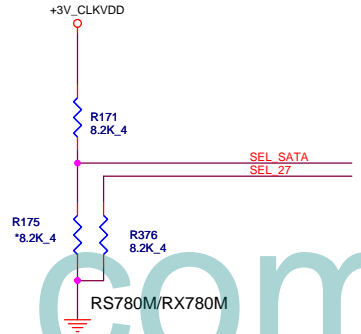
CLOCKS name	UMA	RS780	Clock pin function
NBGF_X_CLKP NBGF_X_CLKN	RP64 STUFF	RP64 STUFF	to NB for VGA reference clock
EXT_GFX_CLKP EXT_GFX_CLKN	RP5053 NC	RP5053 STUFF	to M86-M external reference clock
NBPPP_CLKP NBPPP_CLKN	RP70 STUFF	RP70 NC	to NB for RX780 for PCIEX2 interface reference clock only RS780 is internal share with AC-LINK clock, RS780 not need
SBLINK_CLKP SBLINK_CLKN	RP72 STUFF	RP72 STUFF	to NB for AC-LINK reference clock



Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

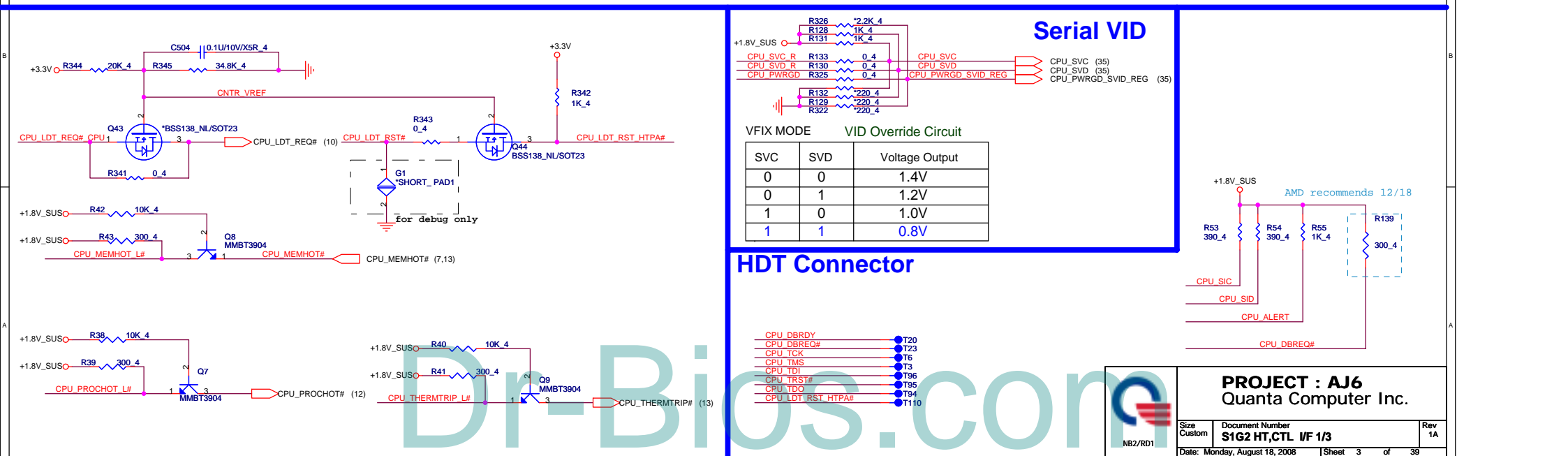
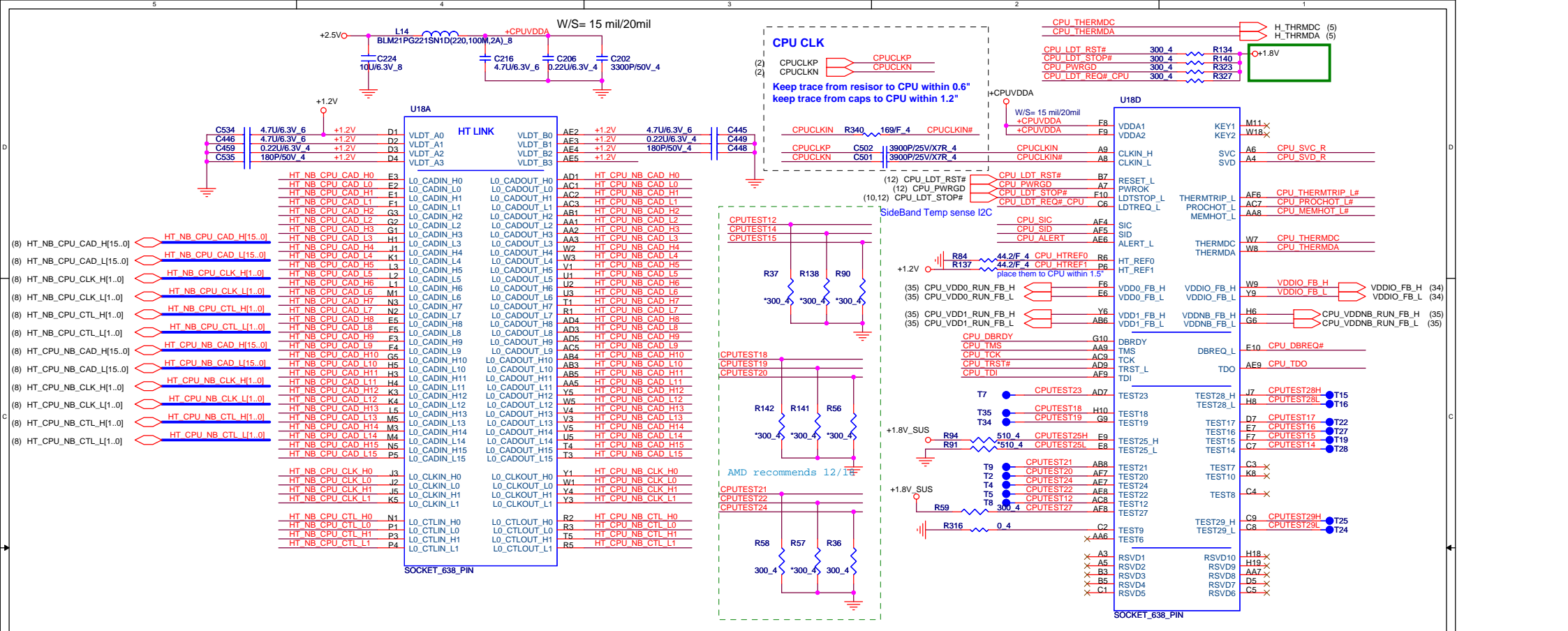
\* default

SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
SEL_HTT66	0*	100 MHz differential HTT clock
SEL_SATA	1*	100 MHz non-spreading differential SRC clock
SEL_SATA	0	100 MHz spreading differential SRC clock
SEL_27	1	27MHz and 27M_SS outputs
SEL_27	0*	100 MHz SRC clock

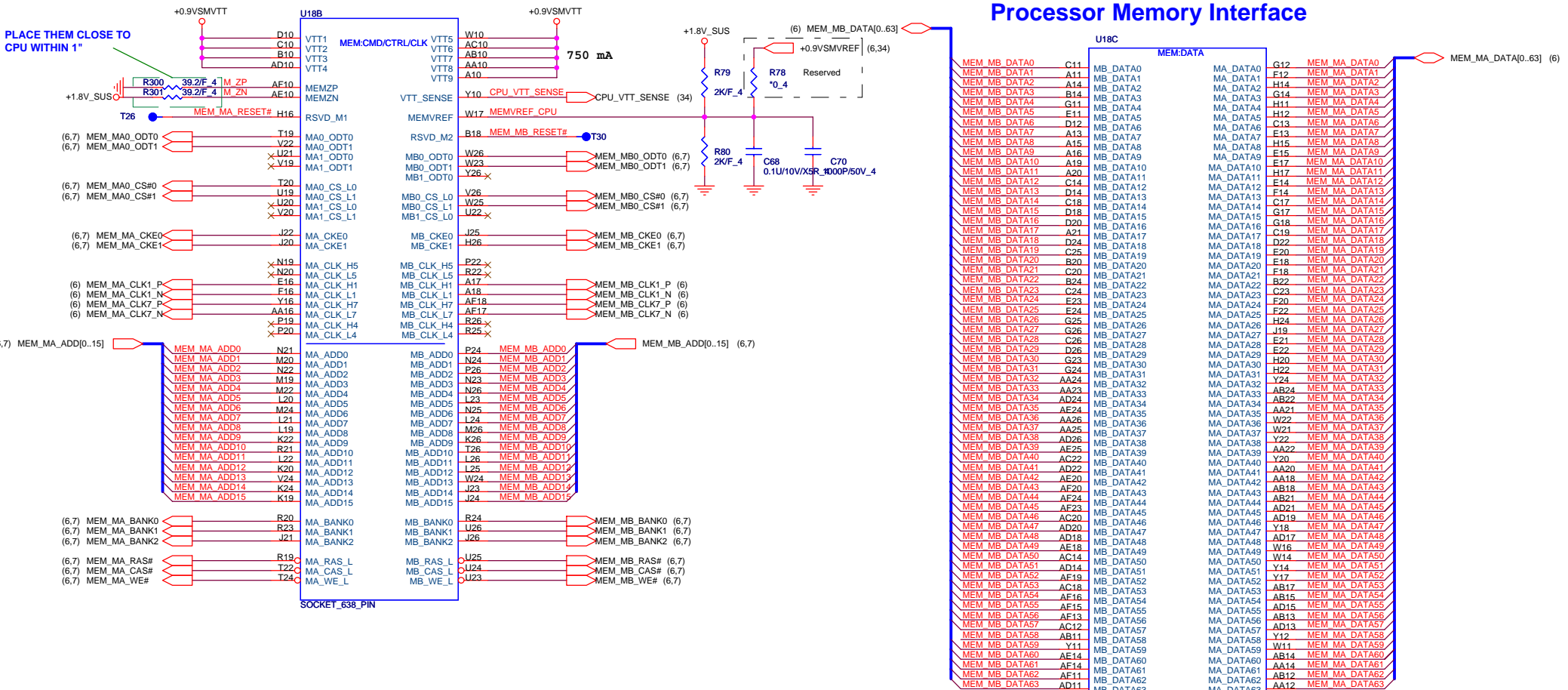


SLG8SP628VTR P/N : AL8SP628000  
 RTM880N-796 P/N : AL000880000



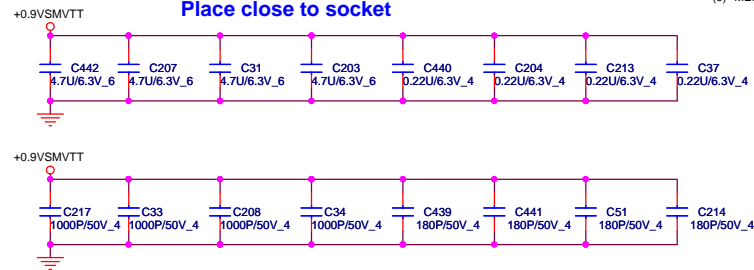


PLACE THEM CLOSE TO CPU WITHIN 1"

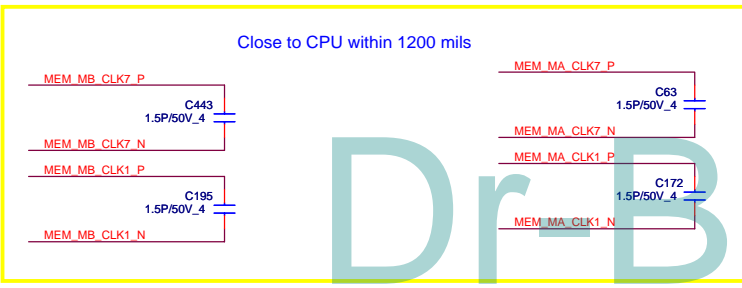


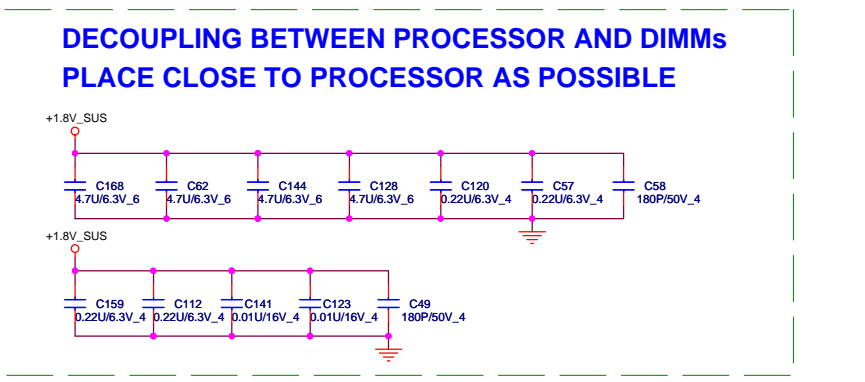
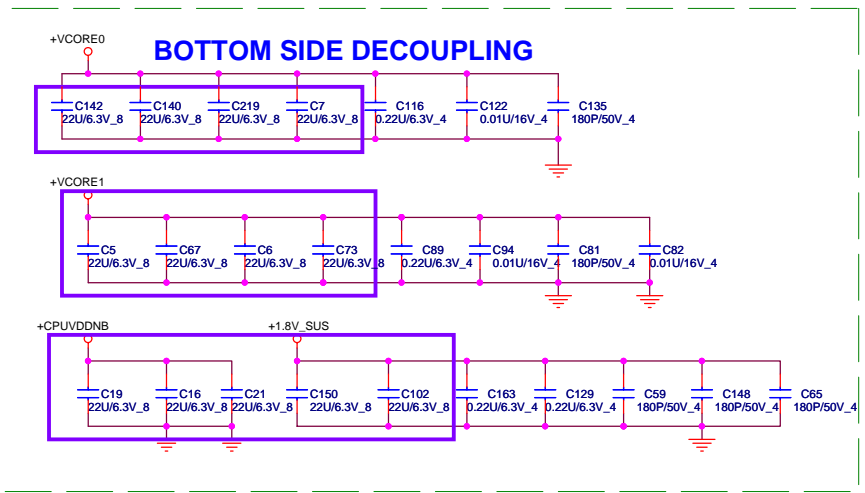
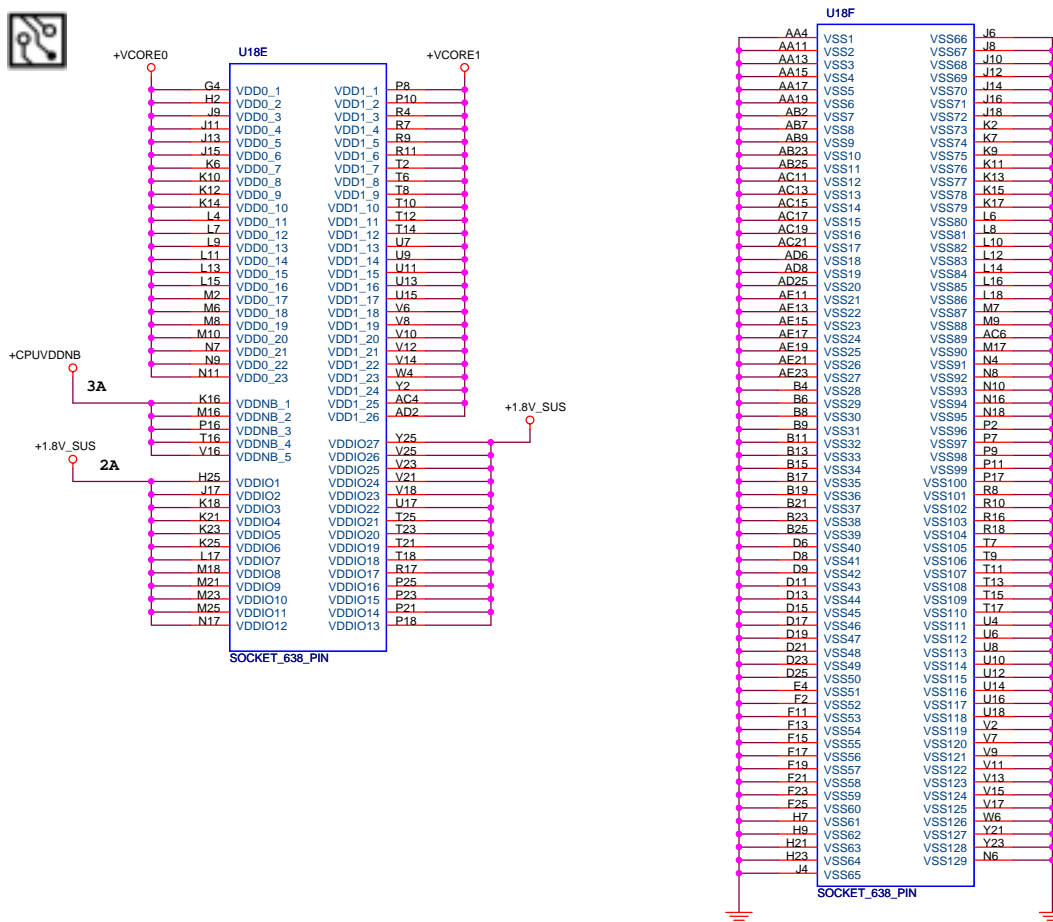
### Processor Memory Interface

Place close to socket

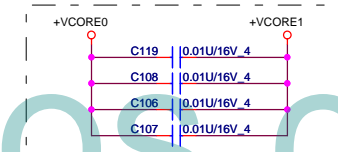
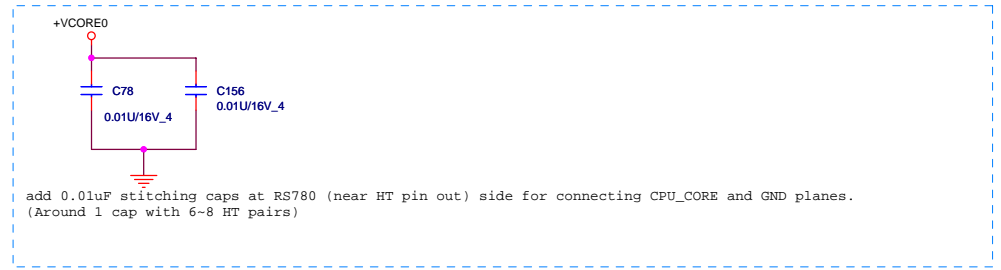
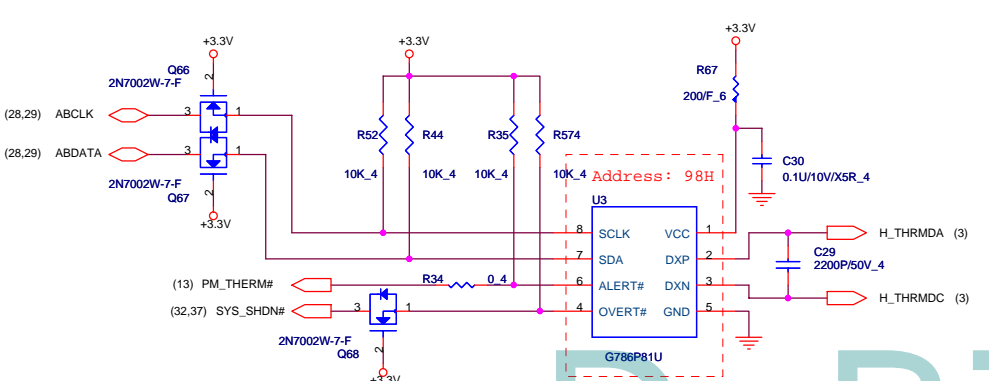


Close to CPU within 1200 mils





## PROCESSOR POWER AND GROUND

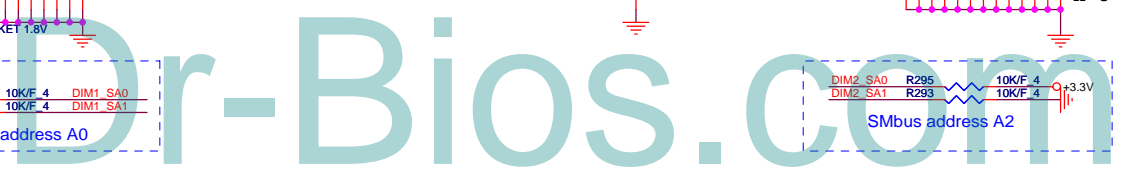
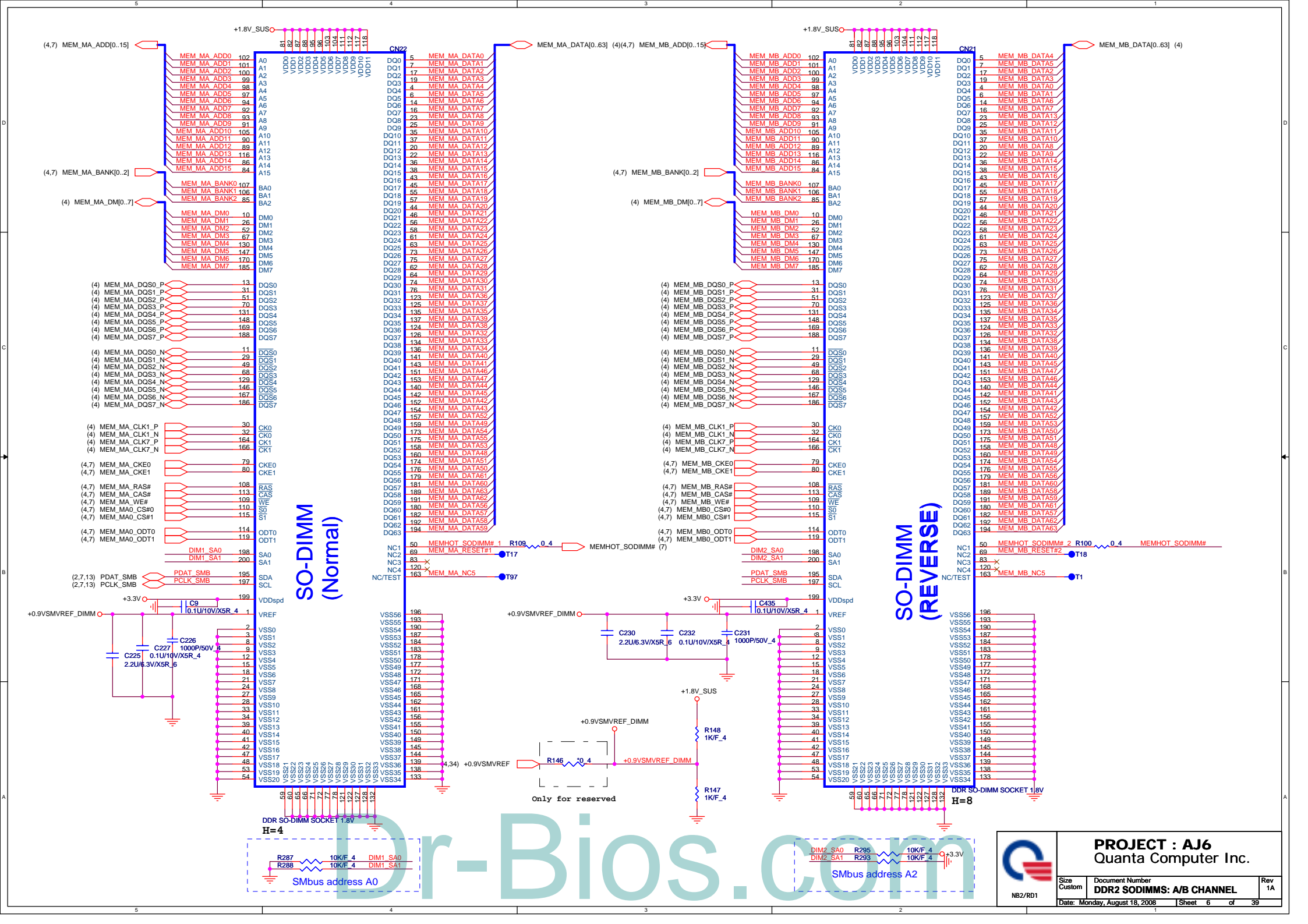


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For fix HyperTransport nets across plane splits

**PROJECT : AJ6**  
Quanta Computer Inc.





**PROJECT : AJ6**  
Quanta Computer Inc.

Size Custom Document Number **DDR2 SODIMMS: A/B CHANNEL** Rev 1A

Date: Monday, August 18, 2008 Sheet 6 of 39

NB2/RD1

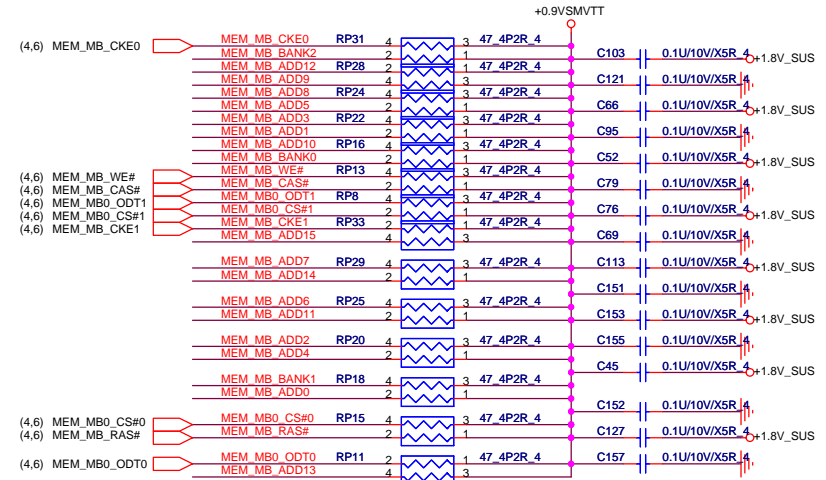
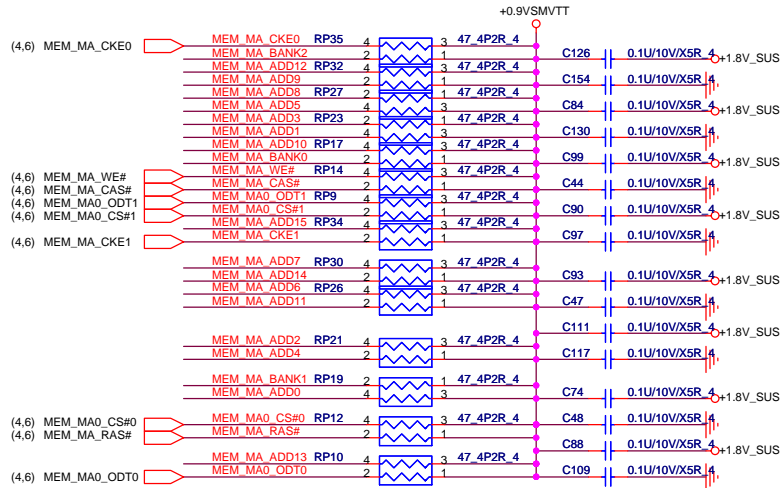


(4,6) MEM\_MA\_ADD[0..15] MEM\_MA\_ADD[0..15]

(4,6) MEM\_MA\_BANK[0..2] MEM\_MA\_BANK[0..2]

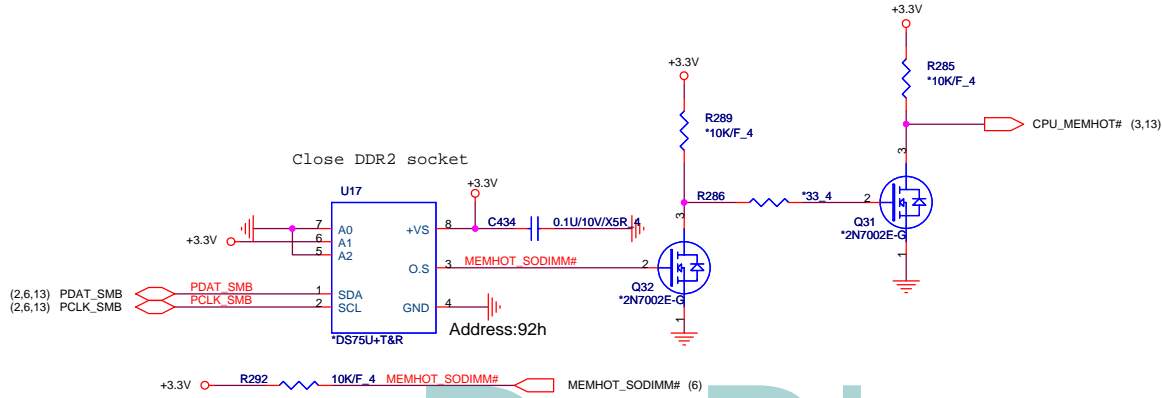
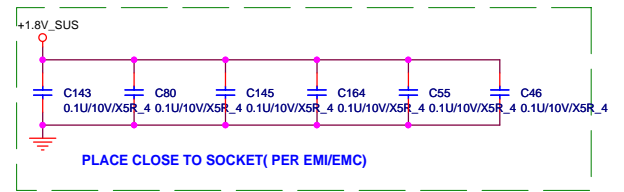
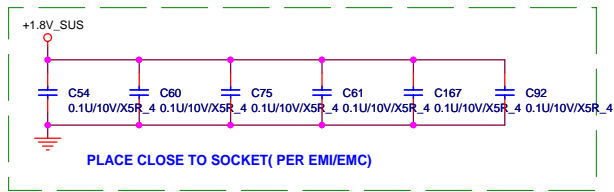
(4,6) MEM\_MB\_ADD[0..15] MEM\_MB\_ADD[0..15]

(4,6) MEM\_MB\_BANK[0..2] MEM\_MB\_BANK[0..2]



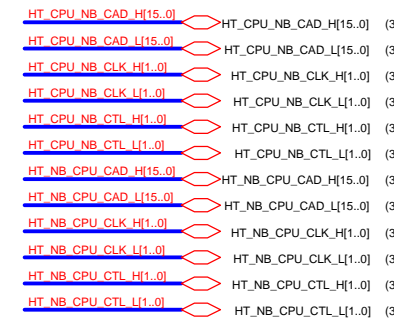
PLACE CLOSE TO PROCESSOR  
WITHIN 1.5 INCH

PLACE CLOSE TO PROCESSOR  
WITHIN 1.5 INCH



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PROJECT : AJ6  
Quanta Computer Inc.

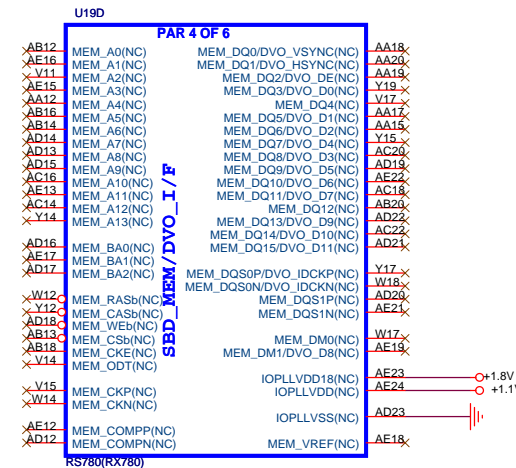


signals	RS780	RX780
HT_TXCALP	R641 300 ohm 1%	R641 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	R655 300 ohm 1%	R655 1.21k ohm 1%
HT_RXCALN		

RES CHIP 1.21K 1/16W +-1%(0402)  
P/N : CS21212FB18

RES CHIP 300 1/16W +-1%(0402)  
P/N : CS13002FB00

This block is for UMA RS780 only , RX780 NC



**PROJECT : AJ6**  
Quanta Computer Inc.

Size Custom	Document Number <b>RS780MN-HT LINK I/F 1/4</b>	Rev 1A
Date: Monday, August 18, 2008	Sheet 8	of 39

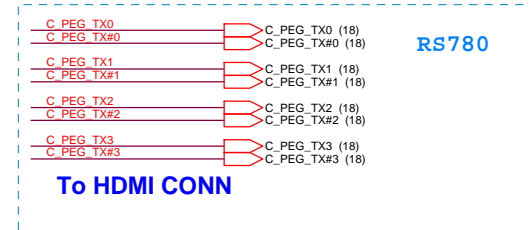
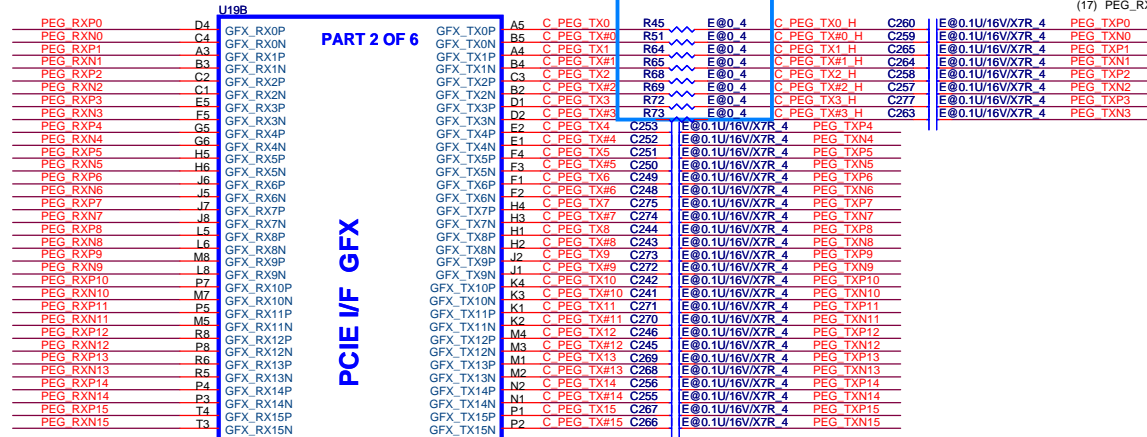
NB2/RD1



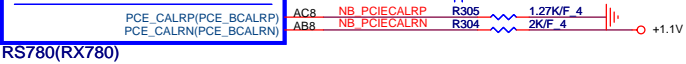
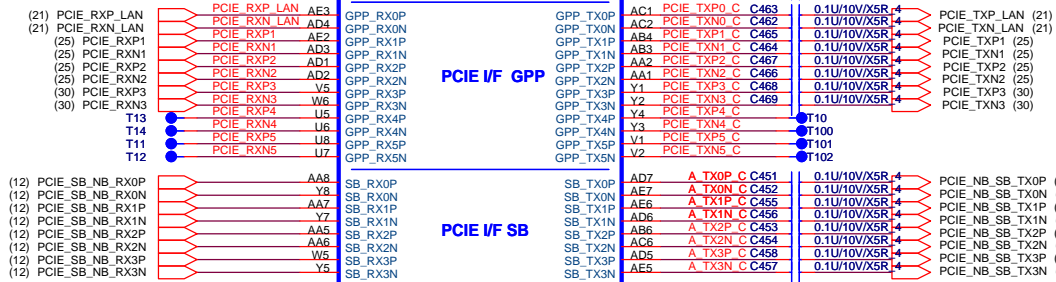
to solve the HDMI issue . 7/10



Close to North Bridge



- TO PCIE-LAN
- TO WLAN
- TO EPRESS CARD
- TO PCIE CARD READER

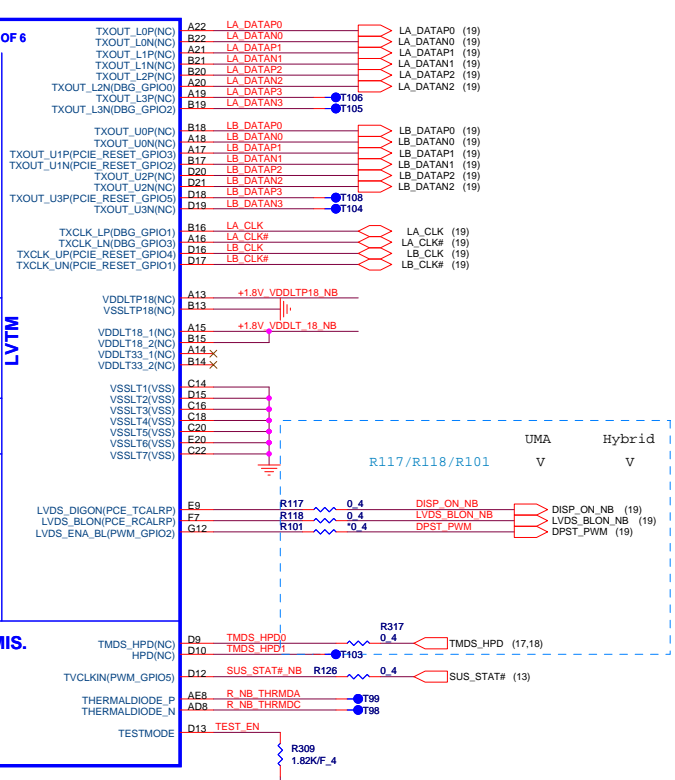
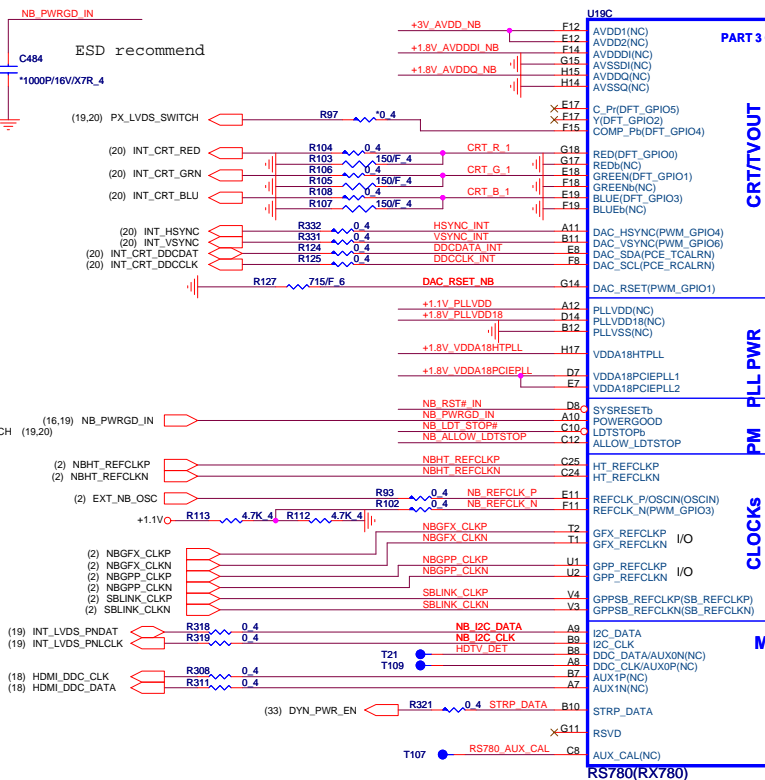
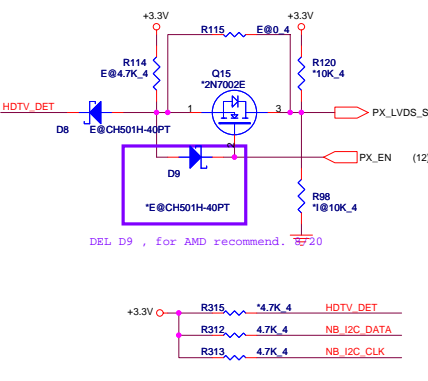
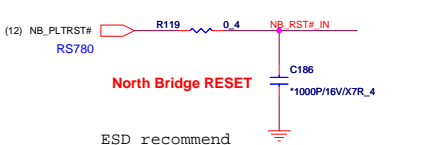


**RX780/RS740/RS780 difference table (PCIE LINK)**

	RX780/RS780
NB_PCIECALRP	1.27K (GND)
GPP4	GPP4
GPP5	GPP5

**RS780 Display Port Support (muxed on GFX)**

DP0	GFX_TX0, TX1, TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4, TX5, TX6 and TX7 AUX1 and HPD1



**RS780**

Enables Debug Bus access through memory T/O pads and GPIO.

0 : Enable RS780, Default  
1 : Disable RS780  
(RS780 use VSYNCH)

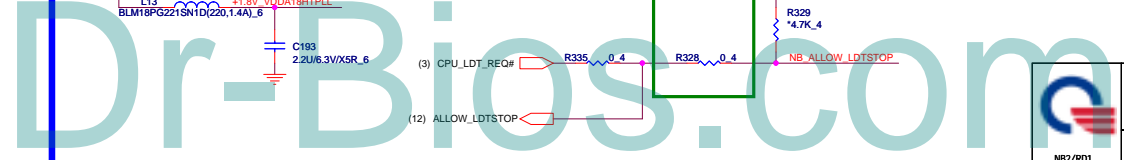
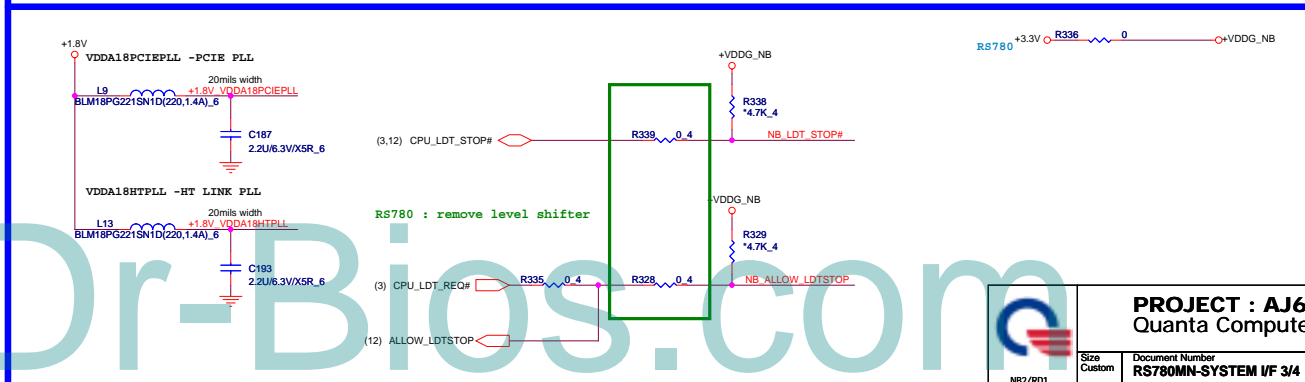
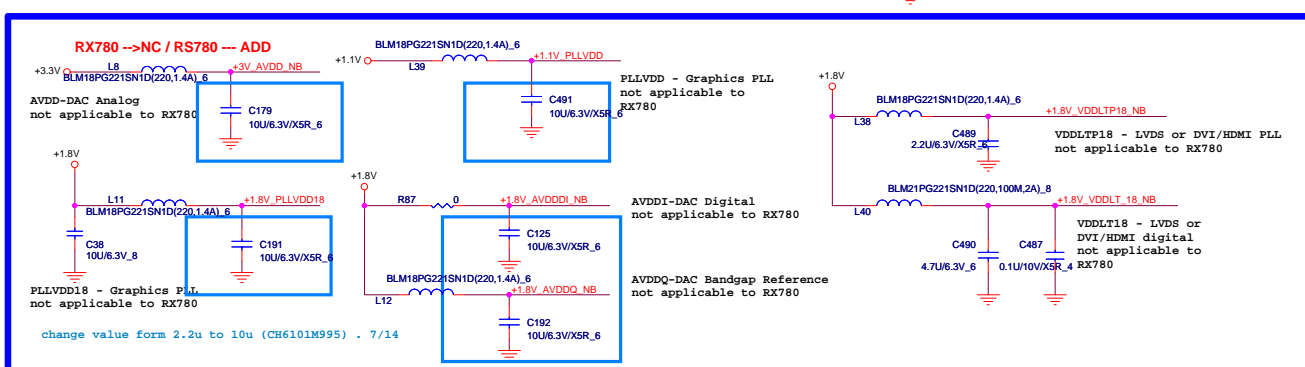
**RS780**

Indicates if memory Side port is available or not

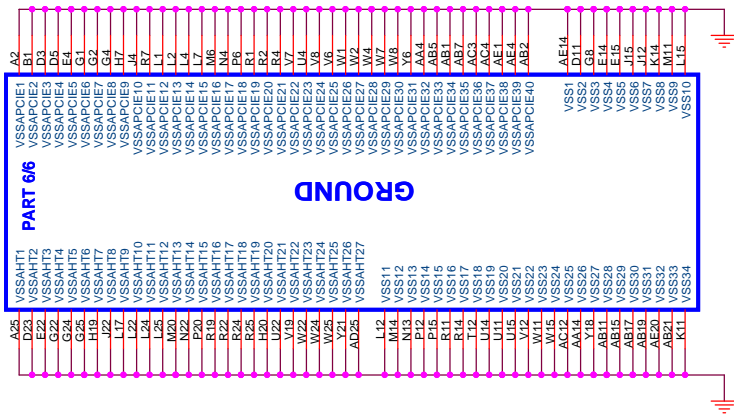
0 : available RS780, Default  
1 : Not available RS780  
(RS780 use HSYNCH)

**RS780/RX780**

For external EEPROM Debug only

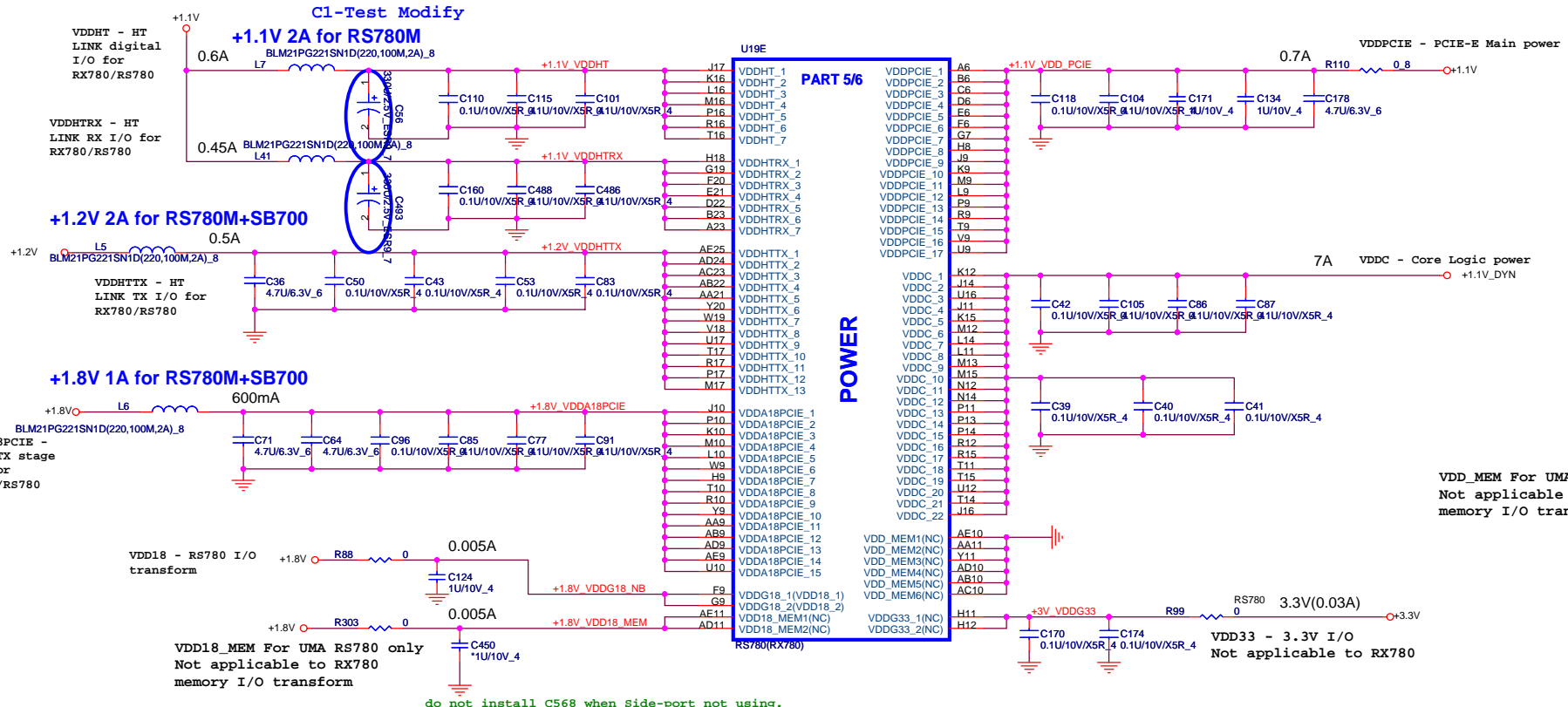


U19F



RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RX780	RS780	PIN NAME	RX780	RS780
VDDHT	+1.1V	+1.1V	IOPLLVD	NC	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	NC	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	NC	+1.8V
VDDG18	+1.8V	+1.8V	PLLVD	NC	+1.1V
VDD18_MEM	NC	+1.8V	PLLVD18	NC	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	NC	+1.8V/1.5V	VDDLTP18	NC	+1.8V
VDDG33	NC	+3.3V	VDDL18	NC	+1.8V
IOPLLVD18	NC	+1.8V	VDDL233	NC	NC



do not install C568 when Side-port not using.

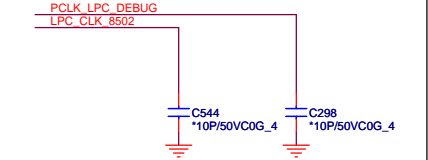
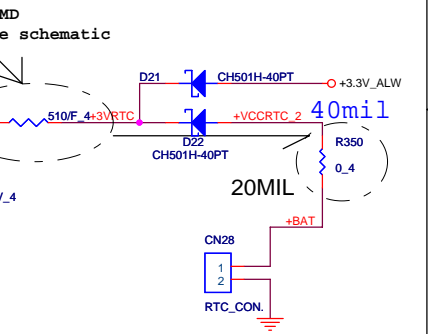
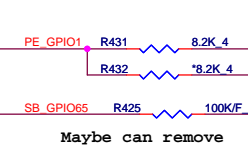
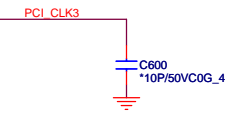
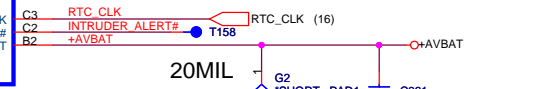
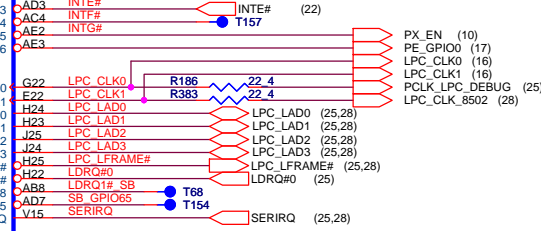
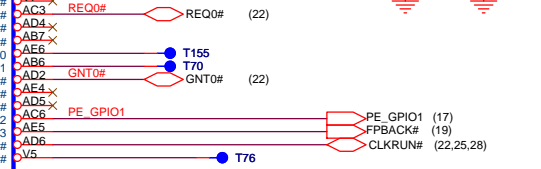
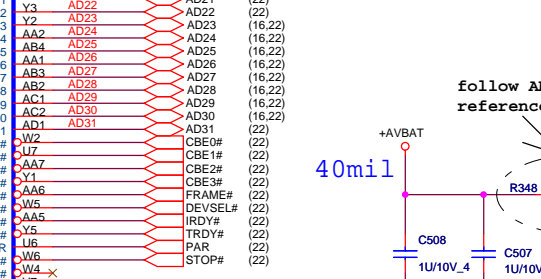
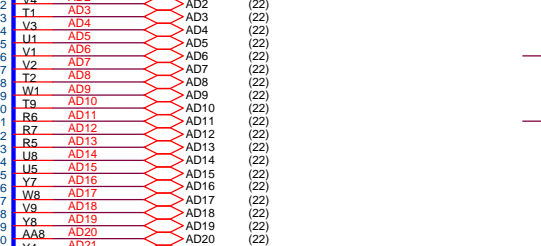
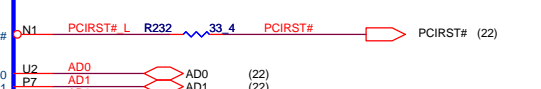
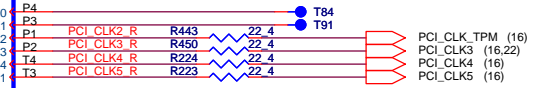
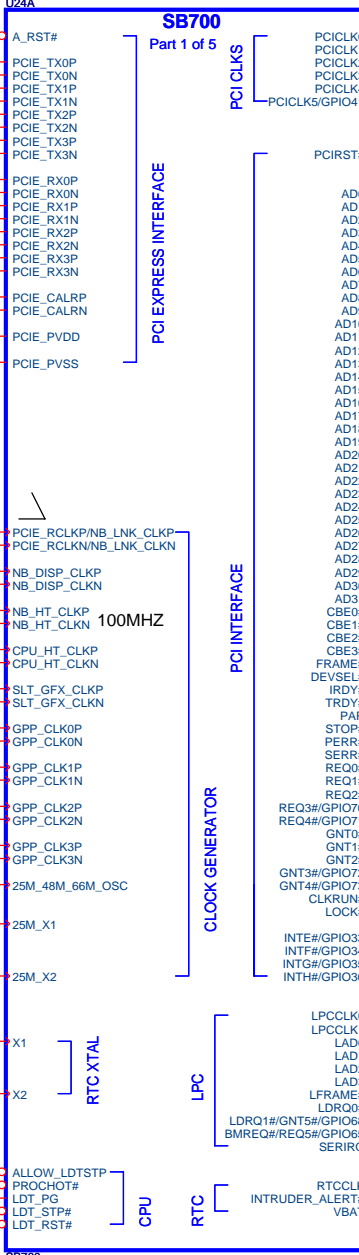
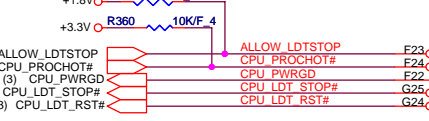
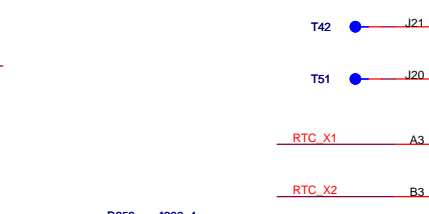
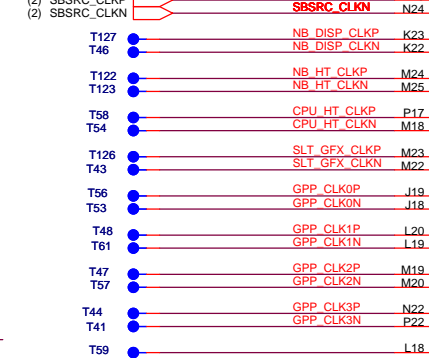
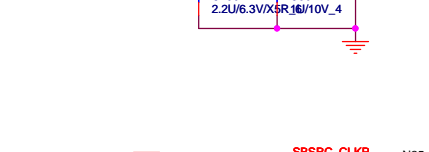
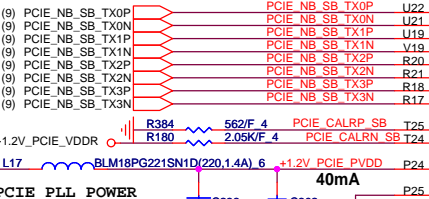
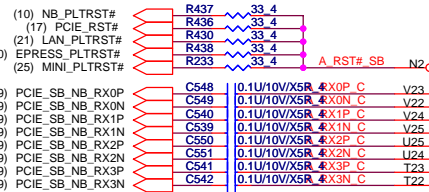
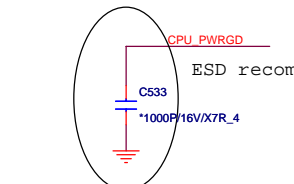
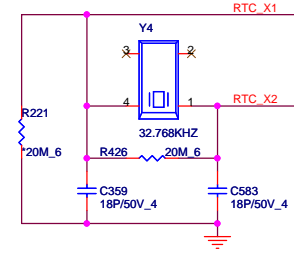
VDD MEM For UMA RS780 only  
Not applicable to RX780  
memory I/O transform

VDD33 - 3.3V I/O  
Not applicable to RX780

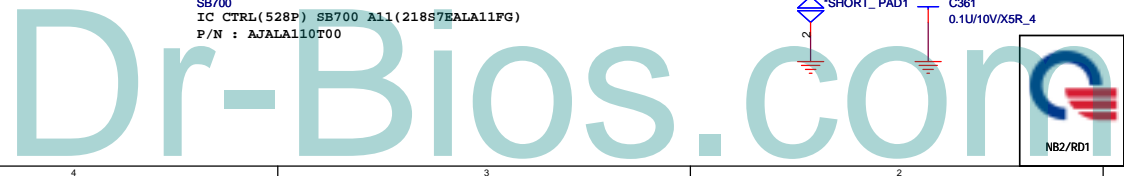


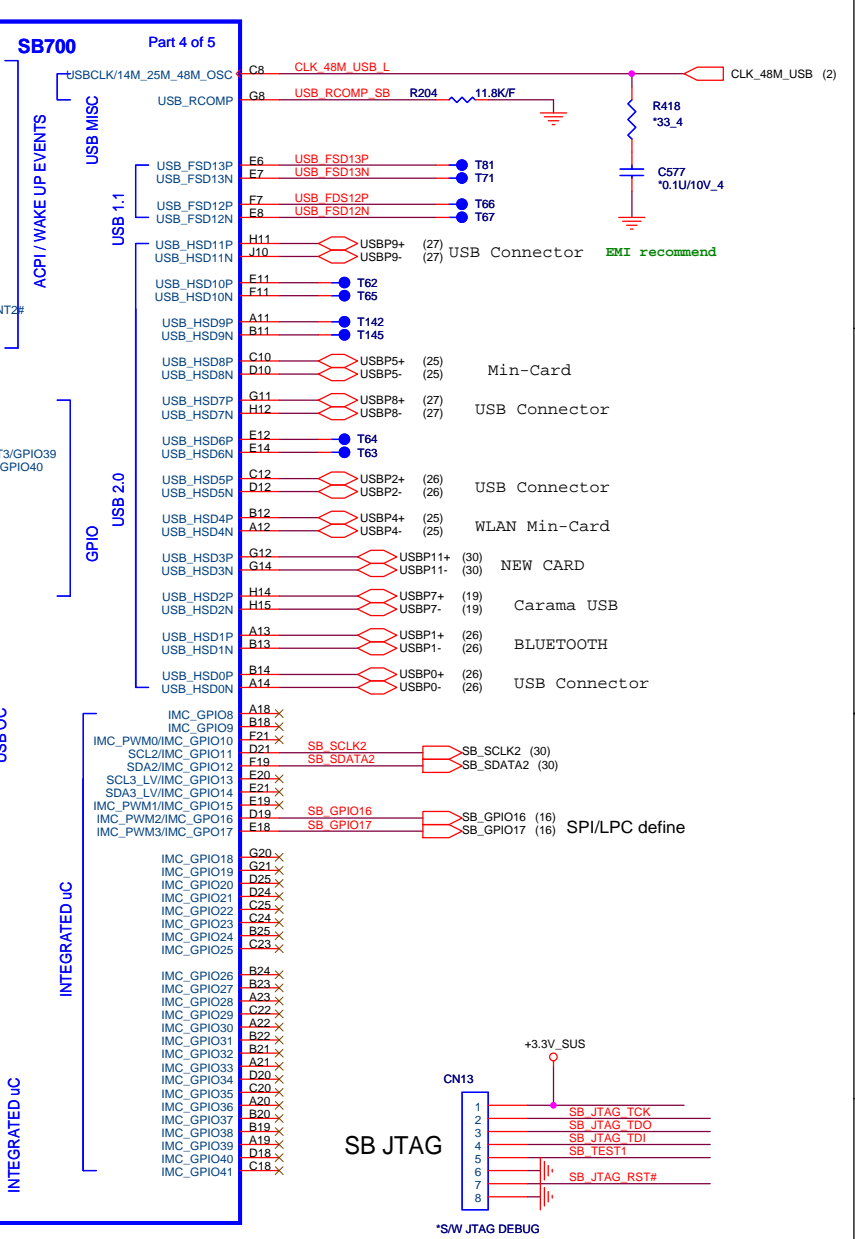
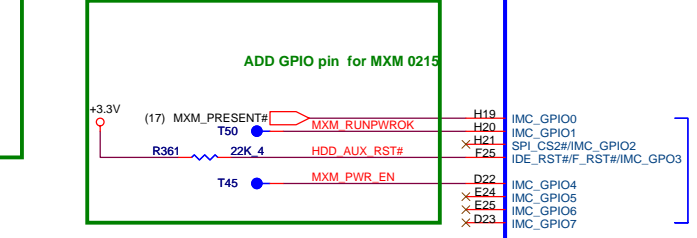
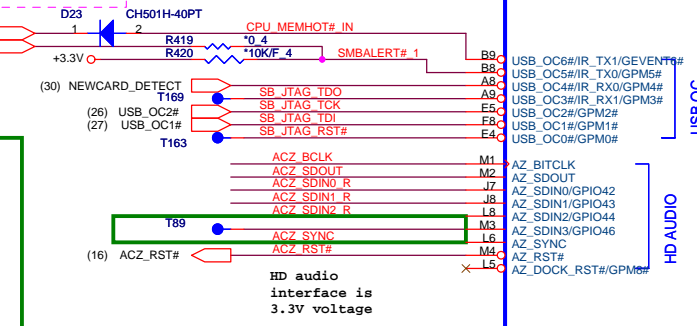
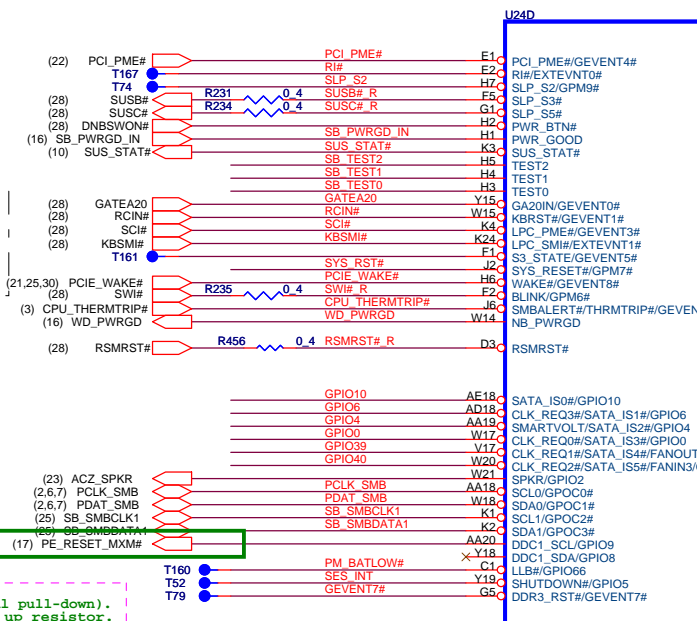
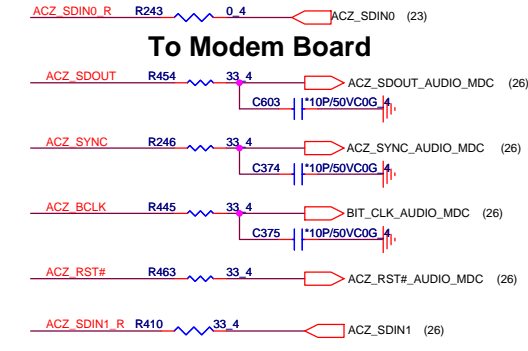
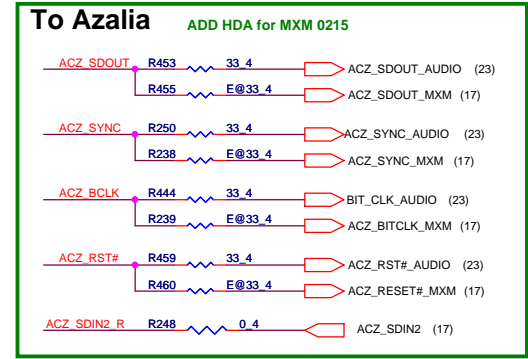
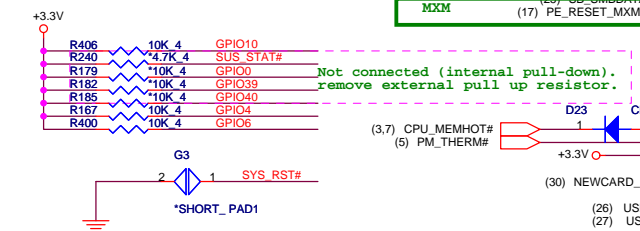
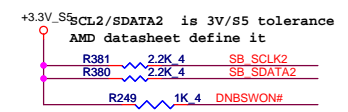
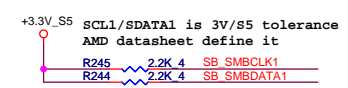
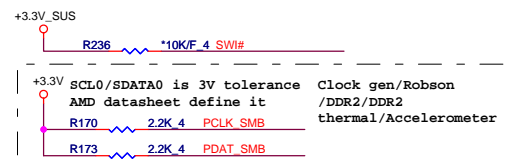
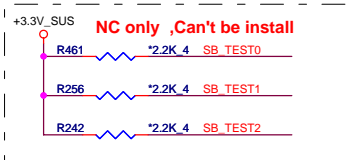
PROJECT : AJ6  
Quanta Computer Inc.

PLACE THESE  
PCIE AC  
COUPLING CAPS  
CLOSE TO U24

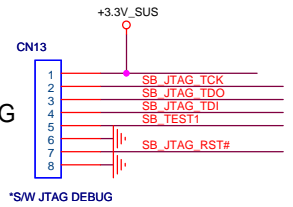


<b>PROJECT : AJ6</b> Quanta Computer Inc.		
Size Custom	Document Number <b>SB700-PCIE/PCU/LPC 1/4</b>	Rev 1A
Date: Monday, August 18, 2008	Sheet 12 of 39	





SB700



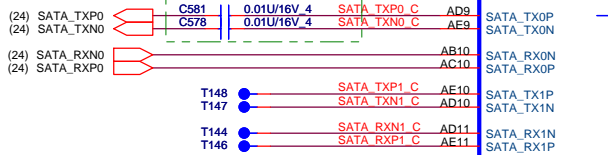
**PROJECT : AJ6**  
**Quanta Computer Inc.**

Size Custom	Document Number <b>SB700-ACPI/GPIO/USB 2/4</b>	Rev 1A
Date: Monday, August 18, 2008		Sheet 13 of 39



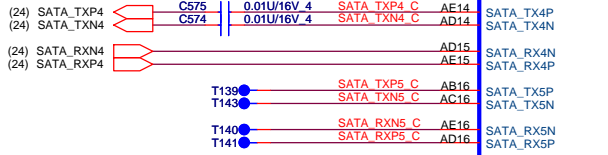
SATA PORT 0,1,2,3  
can support AHCI  
mode

**SATA1**



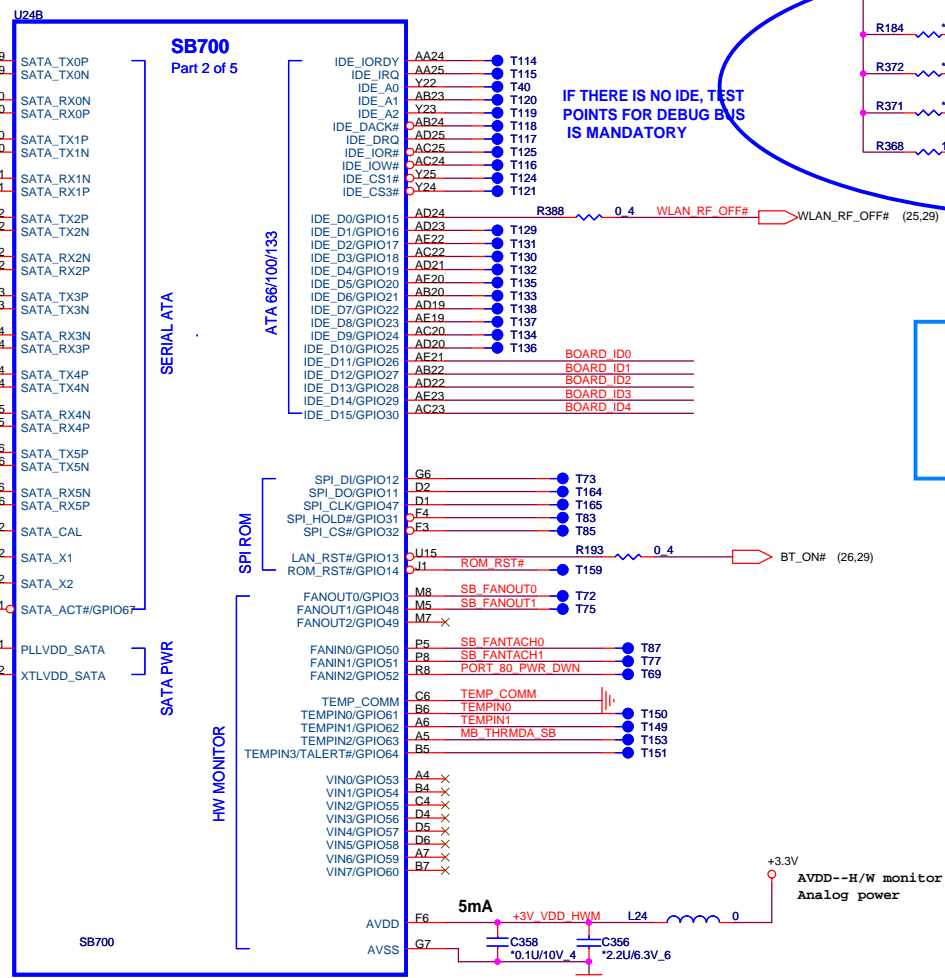
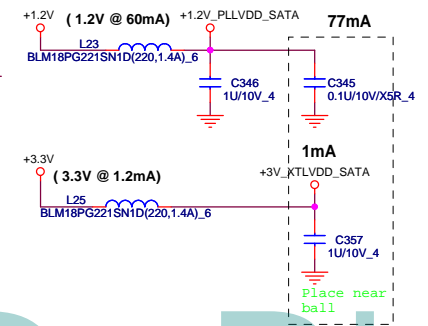
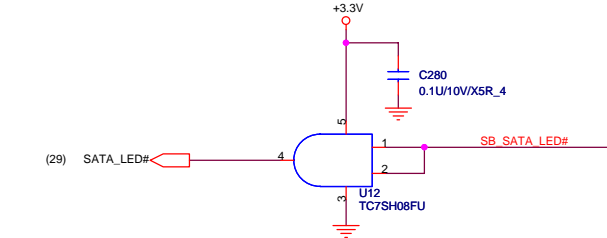
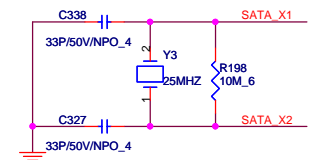
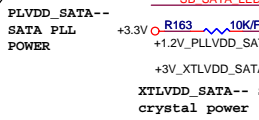
SATA PORT 4,5 are  
only support IDE  
mode

**SATA ODD**

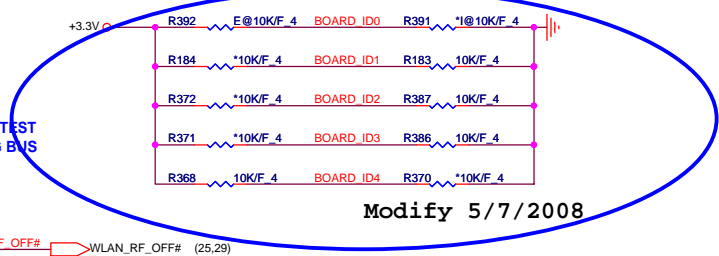


PLACE SATA AC COUPLING  
CAPS CLOSE TO SB700

NOTE:  
R201 IS 1K 1% FOR 25MHZ  
XTAL, 4.99K 1% FOR 100MHZ  
INTERNAL CLOCK



IF THERE IS NO IDE, TEST  
POINTS FOR DEBUG BUS  
IS MANDATORY



Modify 5/7/2008

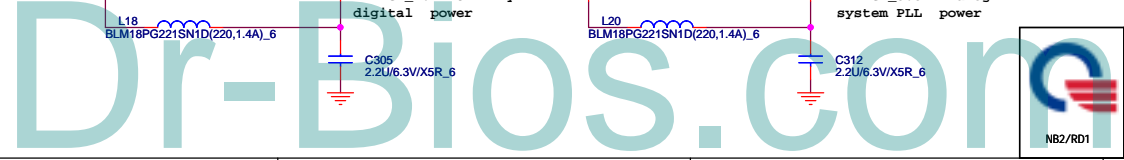
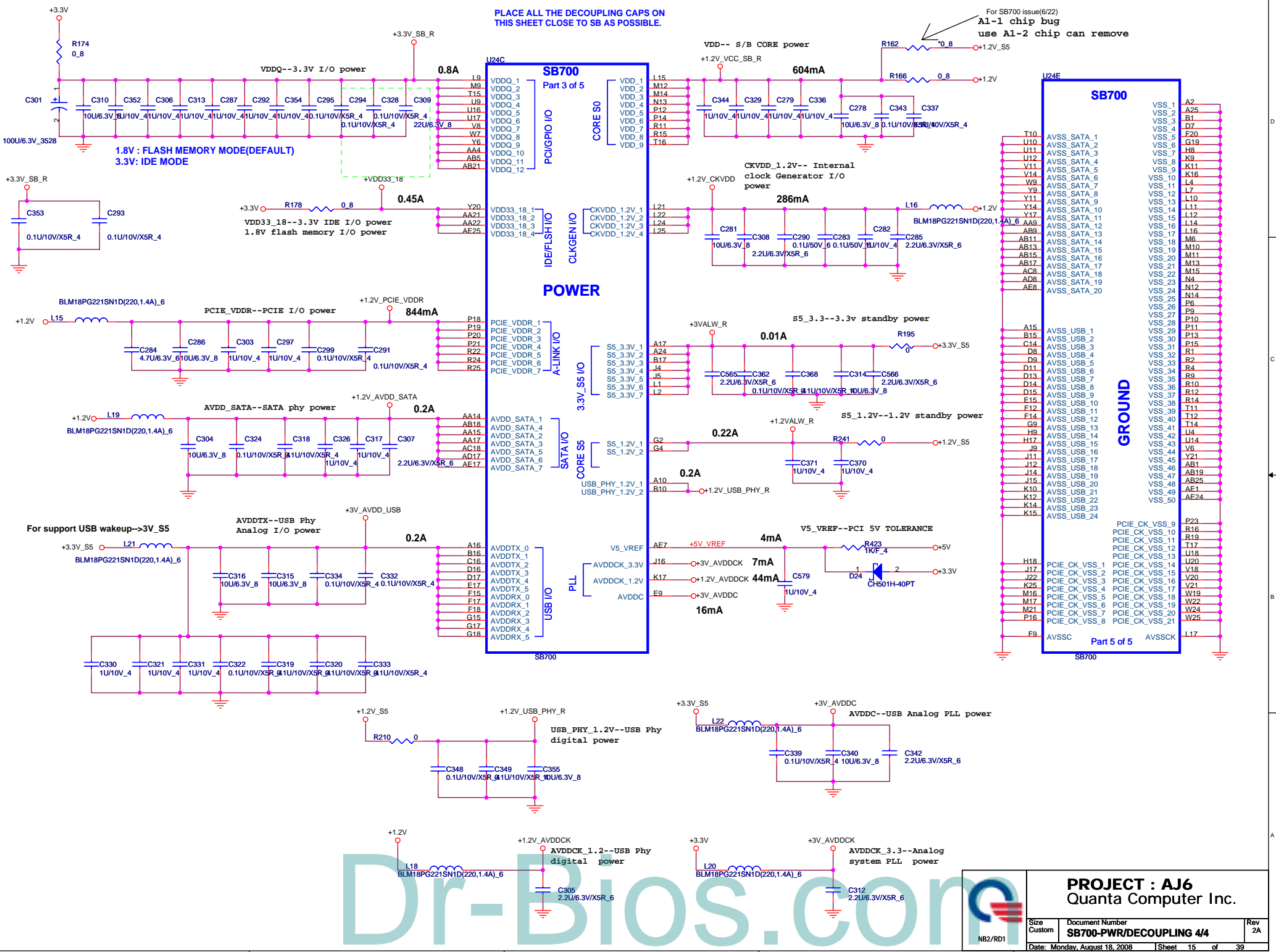
	UMA	MXM
ID0	0	1
ID1	0	0
ID2	0	0
ID3	0	0
ID4	1	1

change the board ID. 7/10



PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

For SB700 issue(6/22)  
A1-1 chip bug  
use A1-2 chip can remove



**PROJECT : AJ6**  
Quanta Computer Inc.

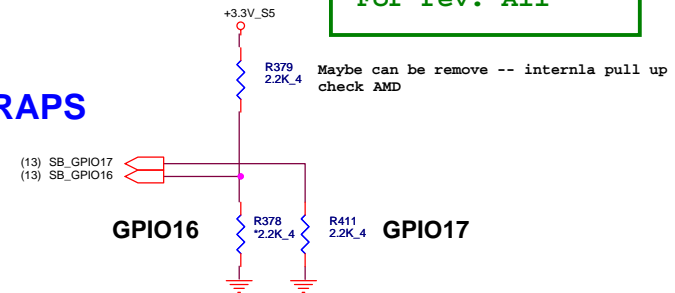
Size Custom	Document Number <b>SB700-PWR/DECOUPLING 4/4</b>	Rev 2A
Date: Monday, August 18, 2008		Sheet 15 of 39

NR2/RD1

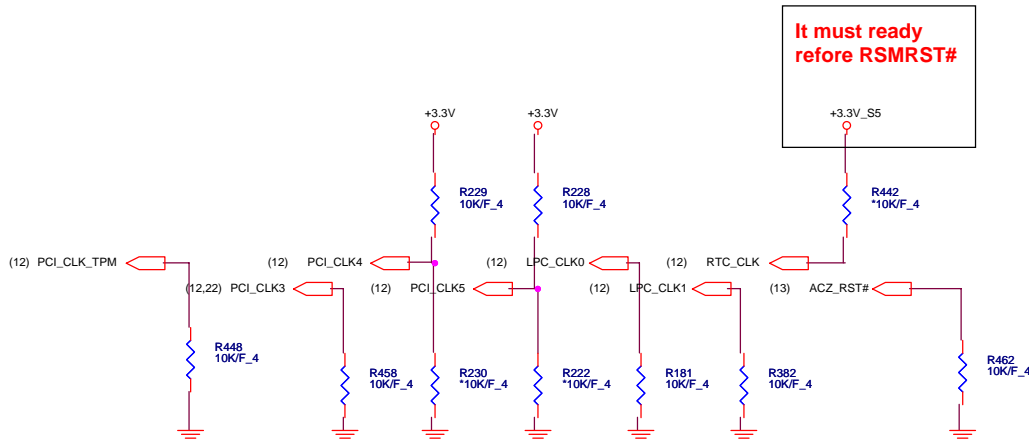
For rev. A11

It must ready before RSMRST#

REQUIRED STRAPS

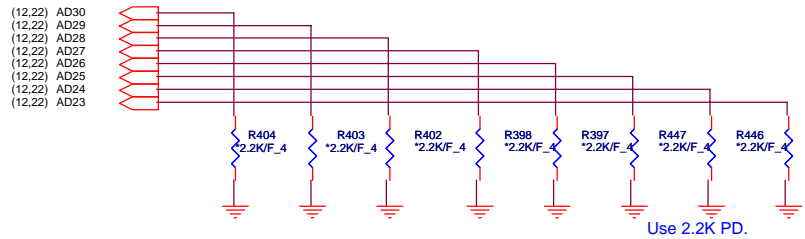


TYPE	GPIO16	GPIO17
FWH	L : 2.2K pull down	L : 2.2K pull down
LPC	NC	L : 2.2K pull down
SPI	L : 2.2K pull down	NC
RSVD	NC	NC



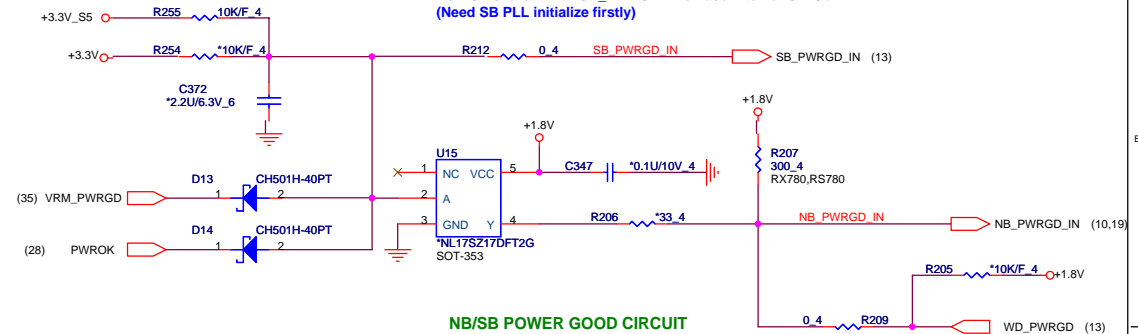
	PCI_CLK_TPM	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#
<b>PULL HIGH</b>	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED
<b>PULL LOW</b>	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT

DEBUG STRAPS SB700 HAS 15K INTERNAL PU FOR PCI\_AD[28:23]

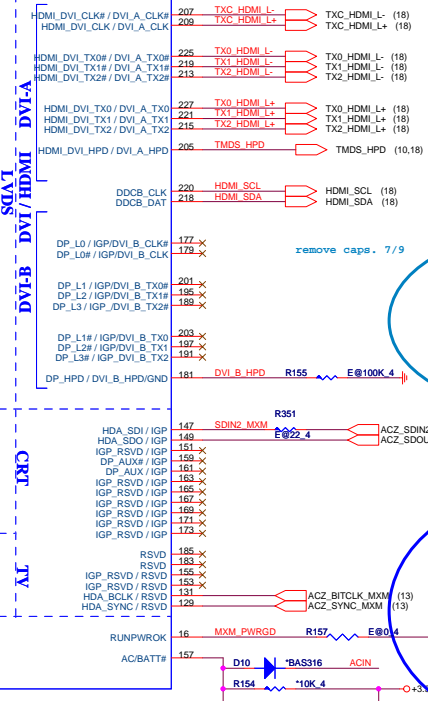
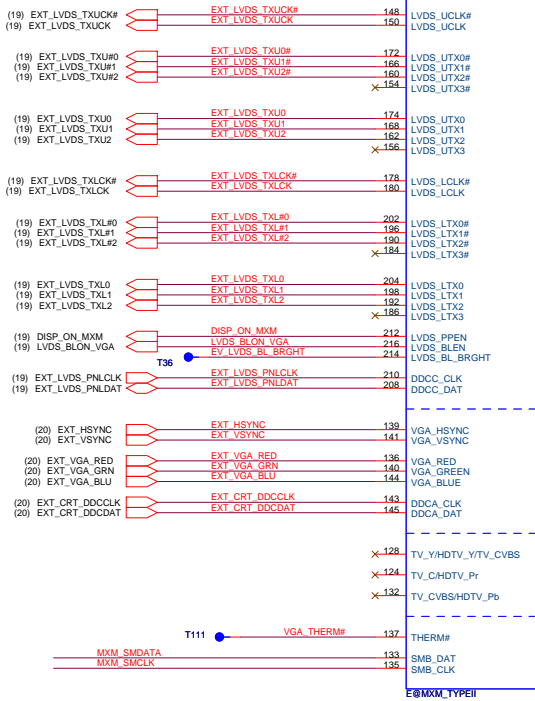


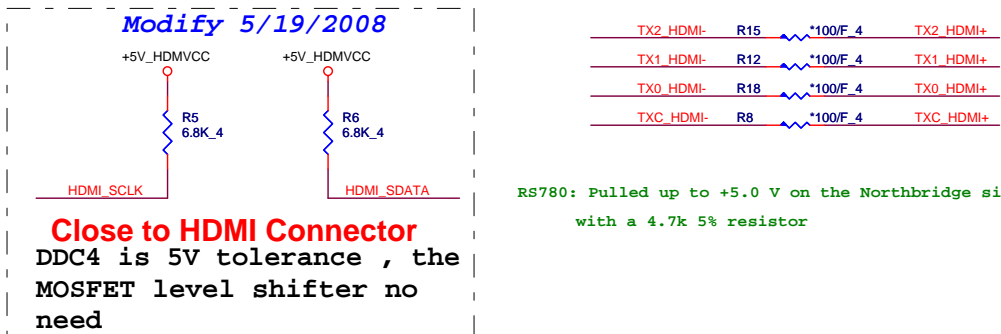
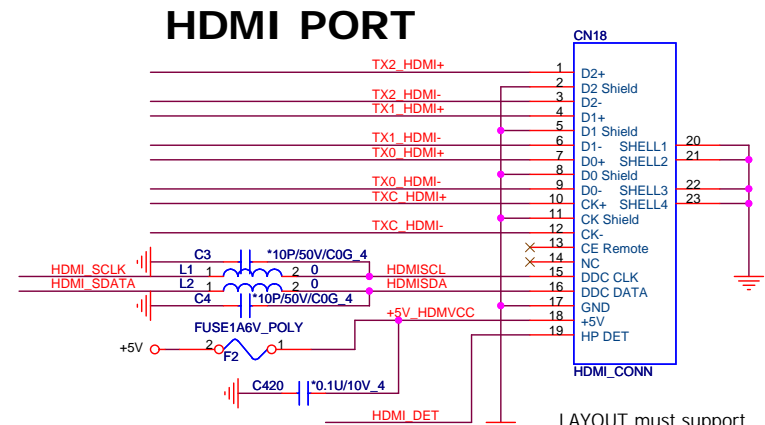
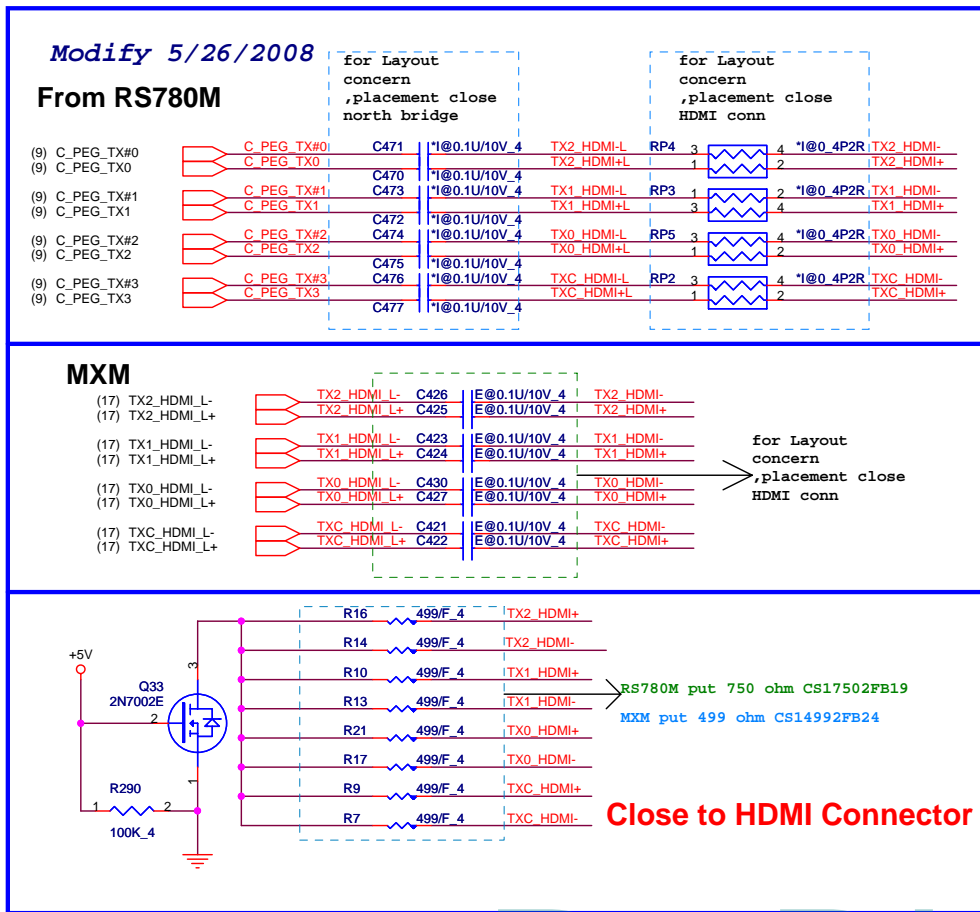
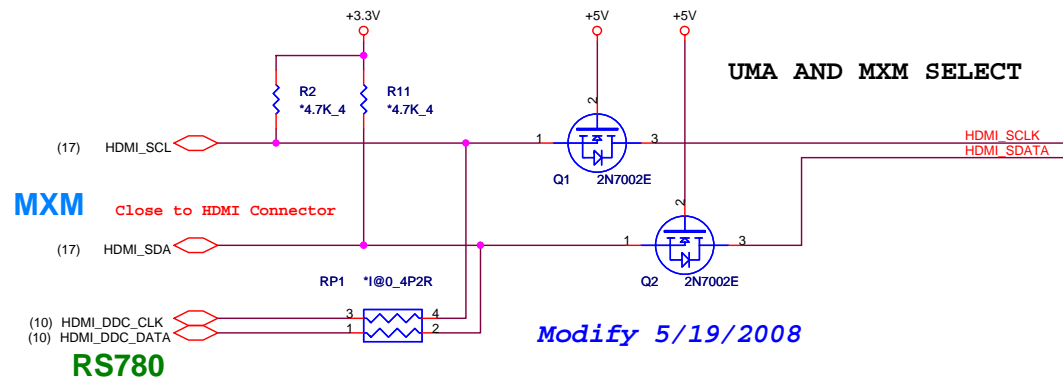
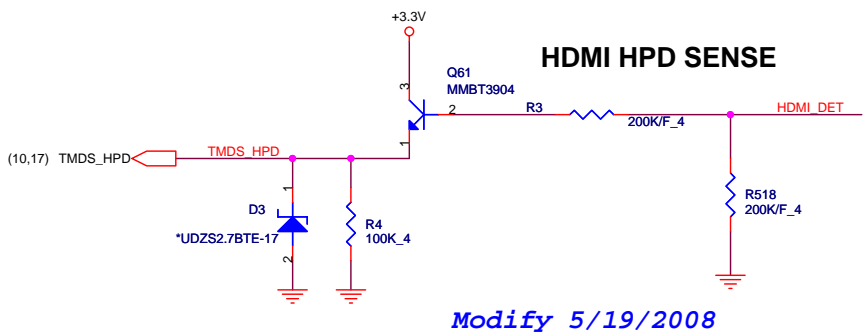
	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
<b>PULL HIGH</b>	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
<b>PULL LOW</b>	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

NB\_PWRGD\_IN:  
RS780/RX780 = 1.8V; RS740 = 3.3V  
Do NOT share it with SB\_PWRGD when use Internal Clk Gen  
(Need SB PLL initialize firstly)



- AL17SZ17000 IC(5P) NL17SZ17DFT2G(SOT-353) SOT-353
- ALUC1G17000 IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5) SOT23-5





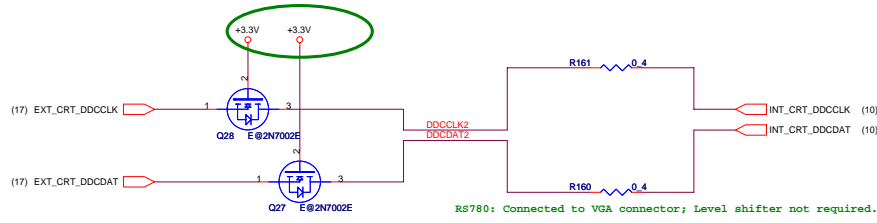
**PROJECT : AJ6**  
Quanta Computer Inc.

Size B	Document Number	Rev 2A
HDMI CONN		
Date: Monday, August 18, 2008		Sheet 18 of 39

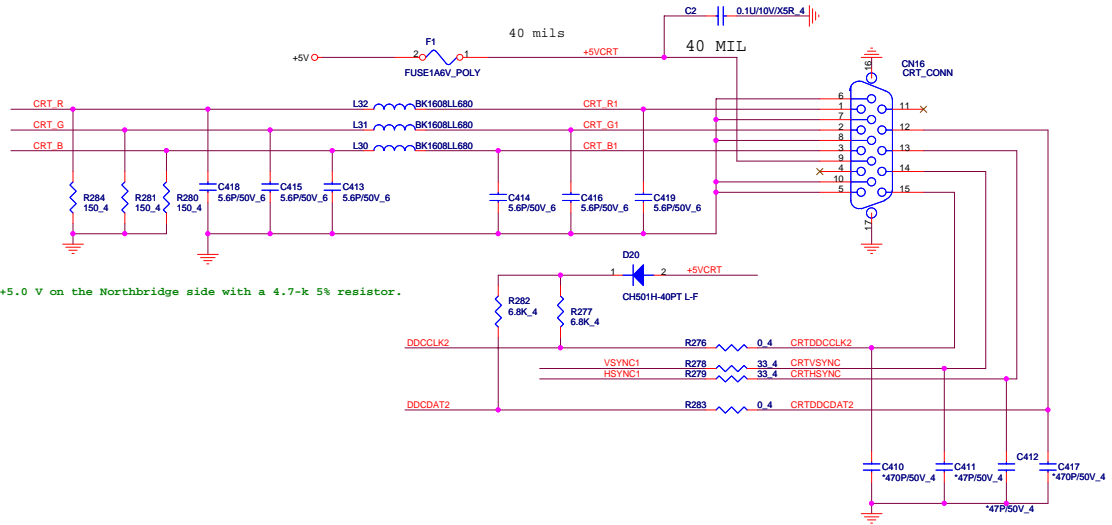
NB2/RD1



# CRT PORT



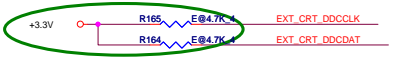
RS780: Connected to VGA connector; Level shifter not required.



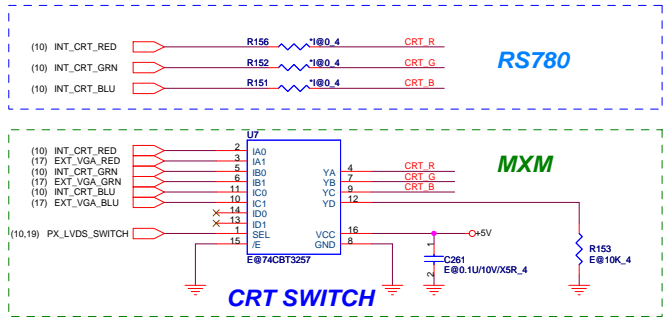
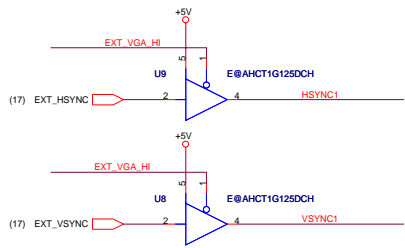
RS780: Pulled up to +5.0 V on the Northbridge side with a 4.7-k 5% resistor.

RS780 Hybrid

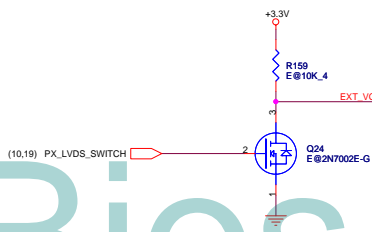
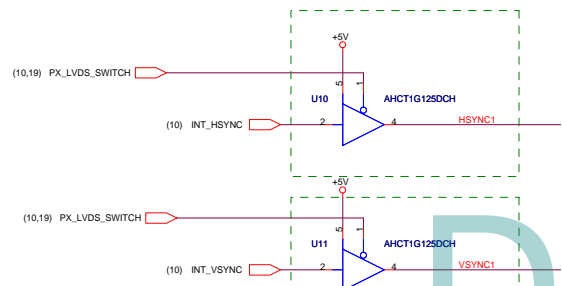
Q28, Q27	X	V
R165, R164	X	V



U9/U8 FOR RS780 ONLY  
U8/U9/U10/U11 FOR RS780+MXM HYBRID

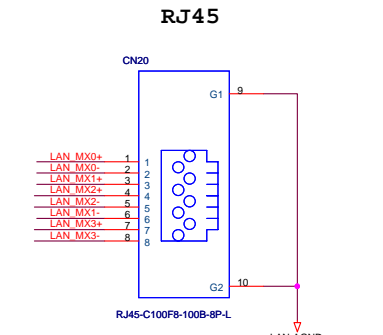
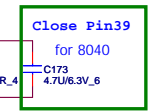
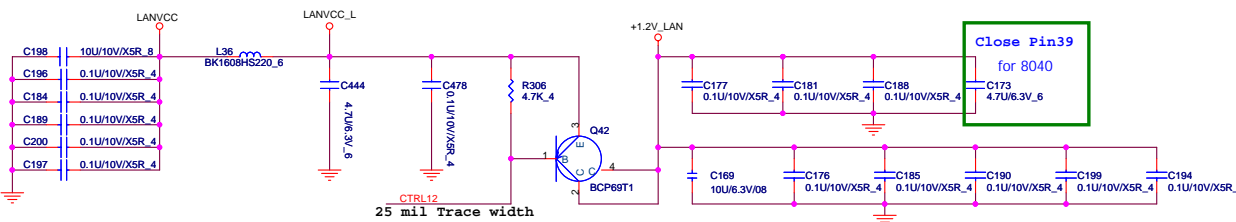
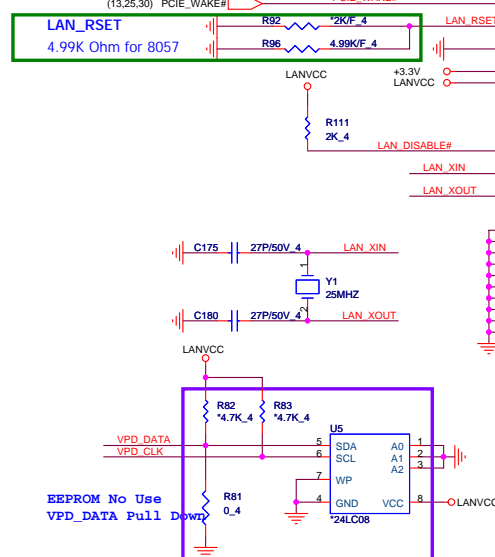
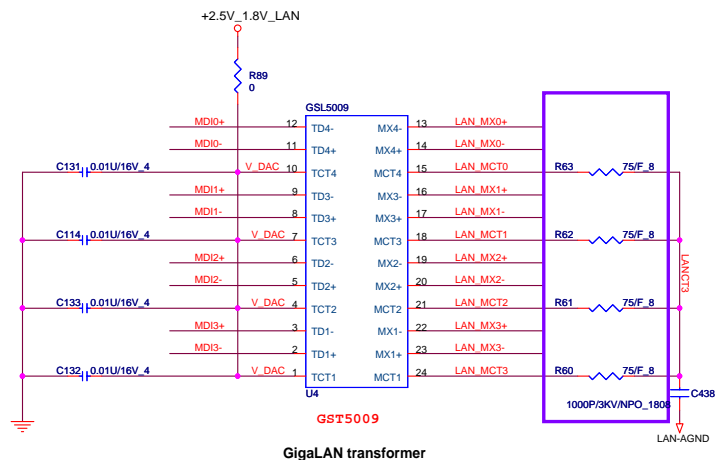
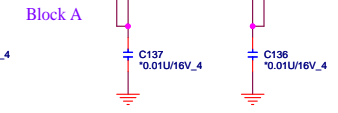
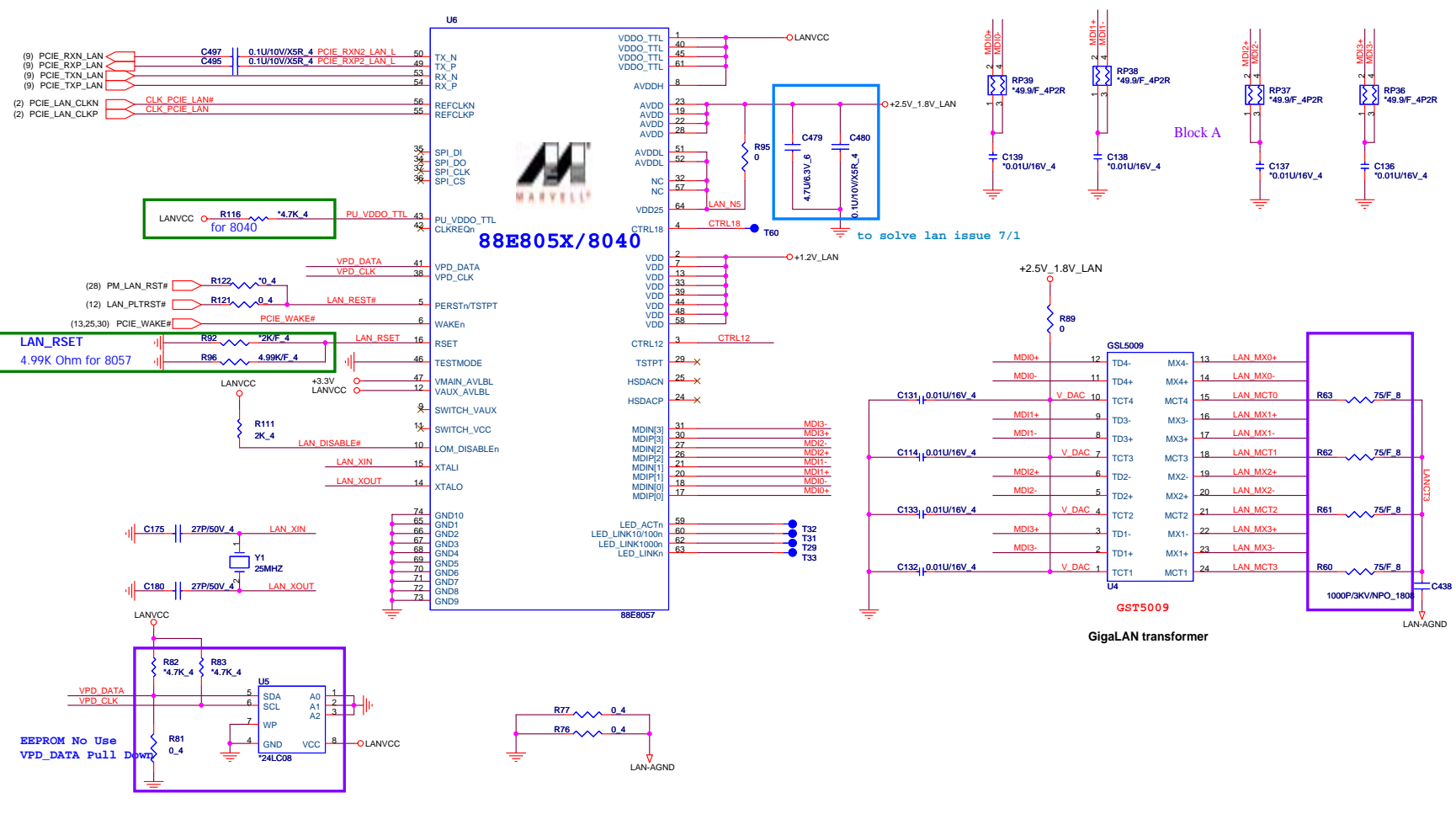


inputs	function
/E SET	
L L	Y - port 0
L H	Y - port 1
H X	Disconnect

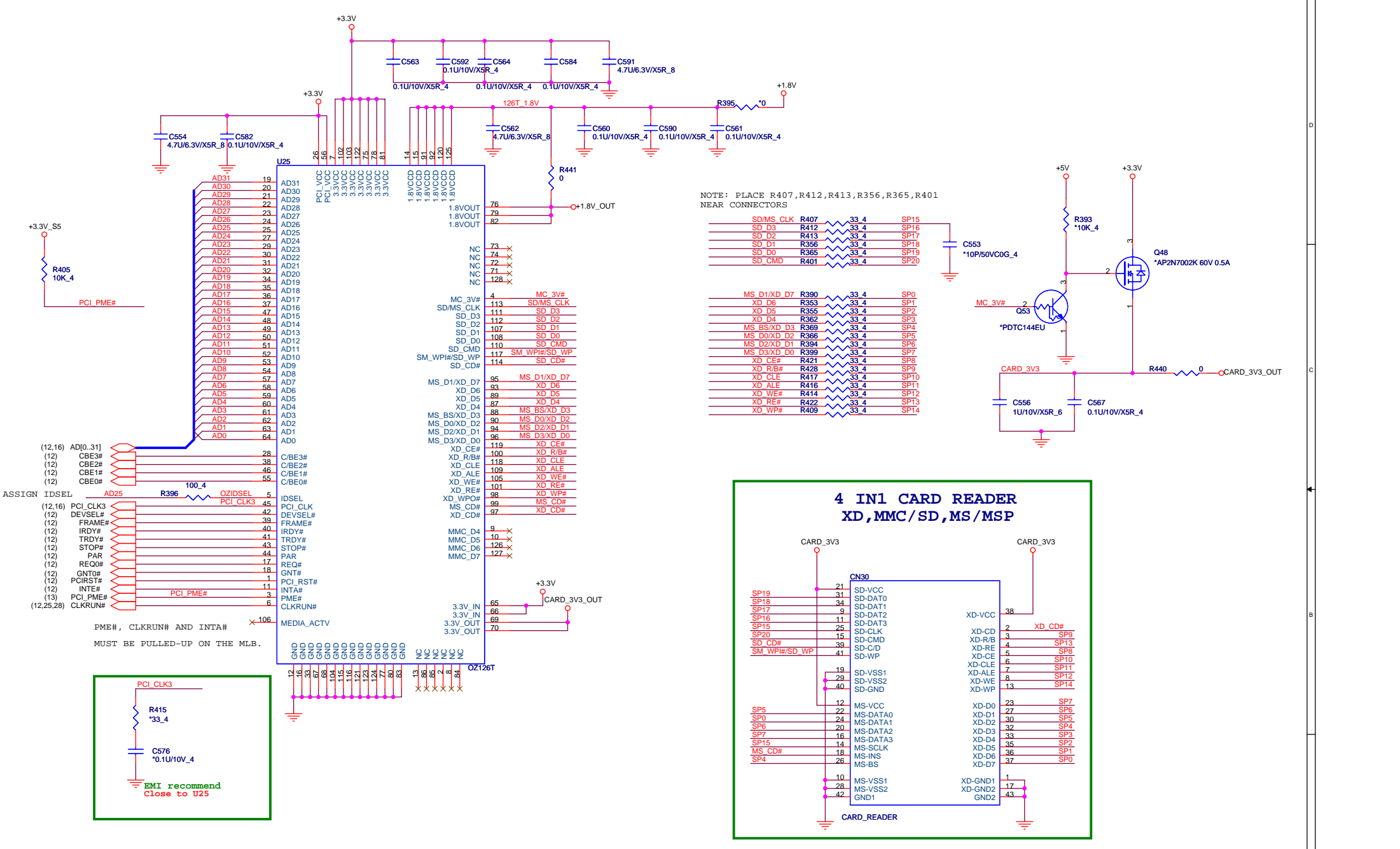


Dr-Bios.com



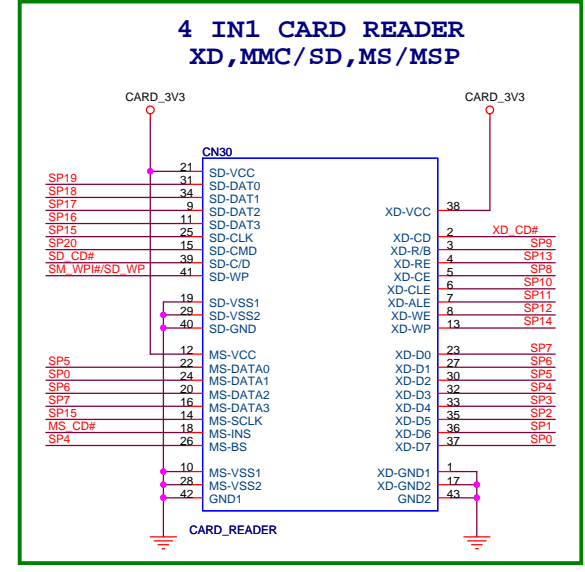


Dr-Bios.com



NOTE: PLACE R407, R412, R413, R356, R365, R401 NEAR CONNECTORS

SD/MS_CLK	R407	33.4	SP15
SD D3	R412	33.4	SP16
SD D2	R413	33.4	SP17
SD D1	R356	33.4	SP18
SD D0	R365	33.4	SP19
SD_CMD	R401	33.4	SP20
MS D1/XD D7	R390	33.4	SP0
XD D6	R353	33.4	SP1
XD D5	R355	33.4	SP2
XD D4	R362	33.4	SP3
MS BS/XD D3	R369	33.4	SP4
MS D0/XD D2	R366	33.4	SP5
MS D2/XD D1	R394	33.4	SP6
MS D3/XD D0	R399	33.4	SP7
XD CE#	R421	33.4	SP8
XD R/B#	R428	33.4	SP9
XD CLE	R417	33.4	SP10
XD ALE	R416	33.4	SP11
XD WE#	R414	33.4	SP12
XD RE#	R422	33.4	SP13
XD WP#	R409	33.4	SP14

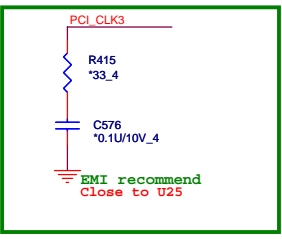


ASSIGN IDSEL

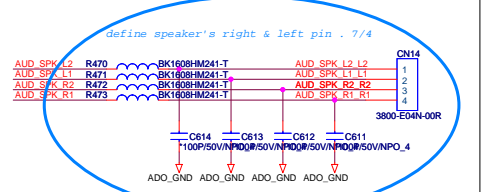
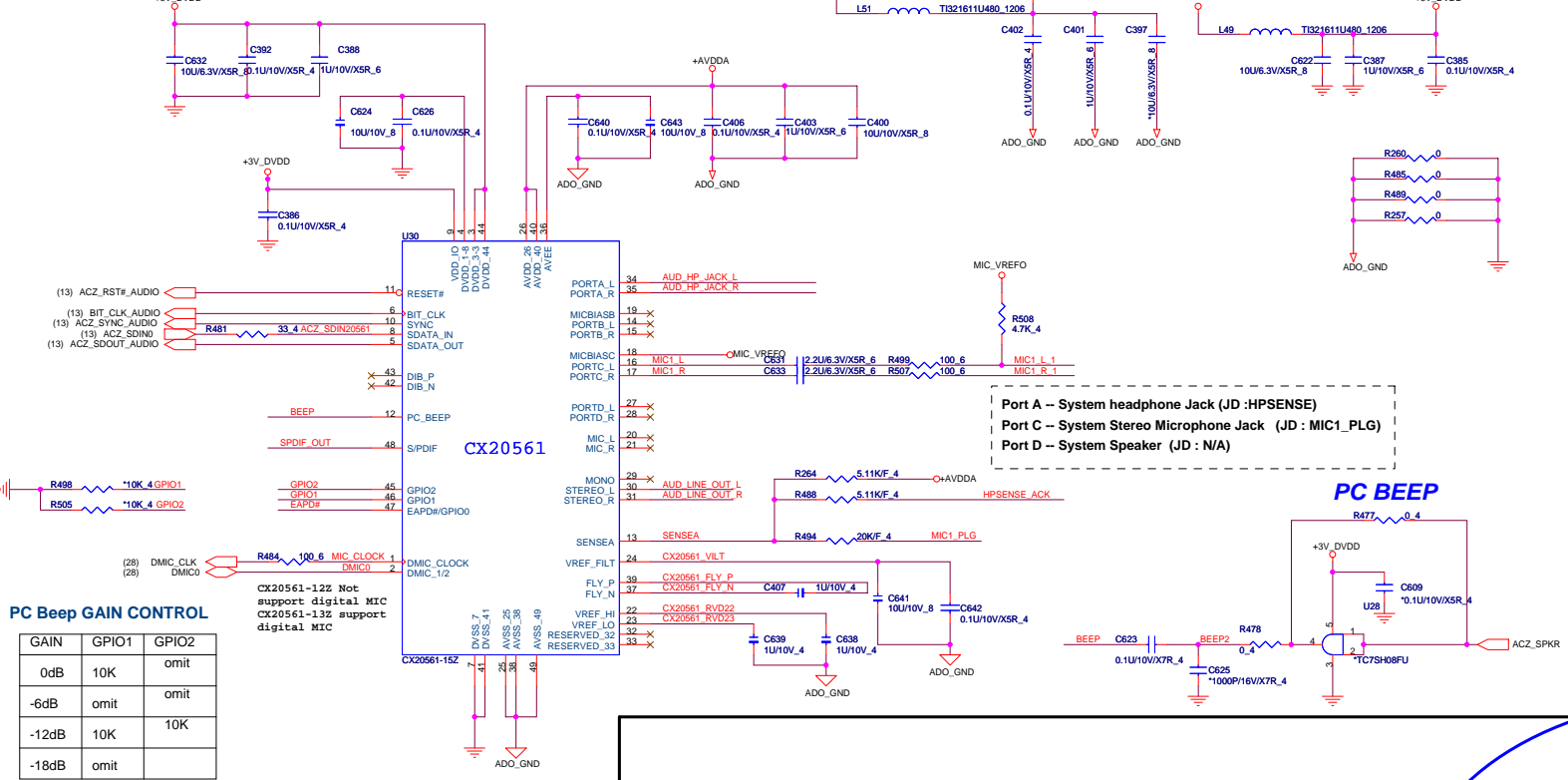
(12,16) AD[0..31]	AD25	100_4	OZIDSEL	5
(12) CBE3#			PCI_CLK3	45
(12) CBE2#			DEVSEL#	42
(12) CBE1#			FRAME#	39
(12) CBE0#			IRDY#	40
			TRDY#	41
			STOP#	43
			PAR	44
			REQ#	17
			GNT0#	18
			PCIRST#	1
			INTA#	11
(13) PCI PME#			PME#	3
(12,25,28) CLKRUN#			CLKRUN#	6

PME#, CLKRUN# AND INTA#  $\times 106$

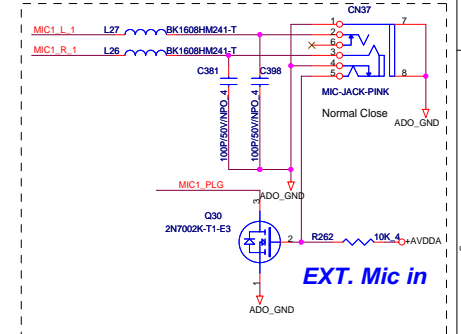
MUST BE PULLED-UP ON THE MLB.



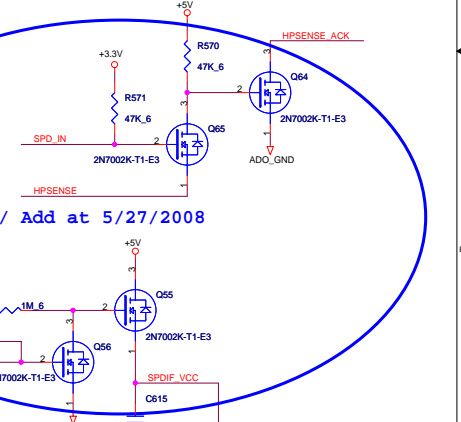
# (CX20561-15Z for QFN)



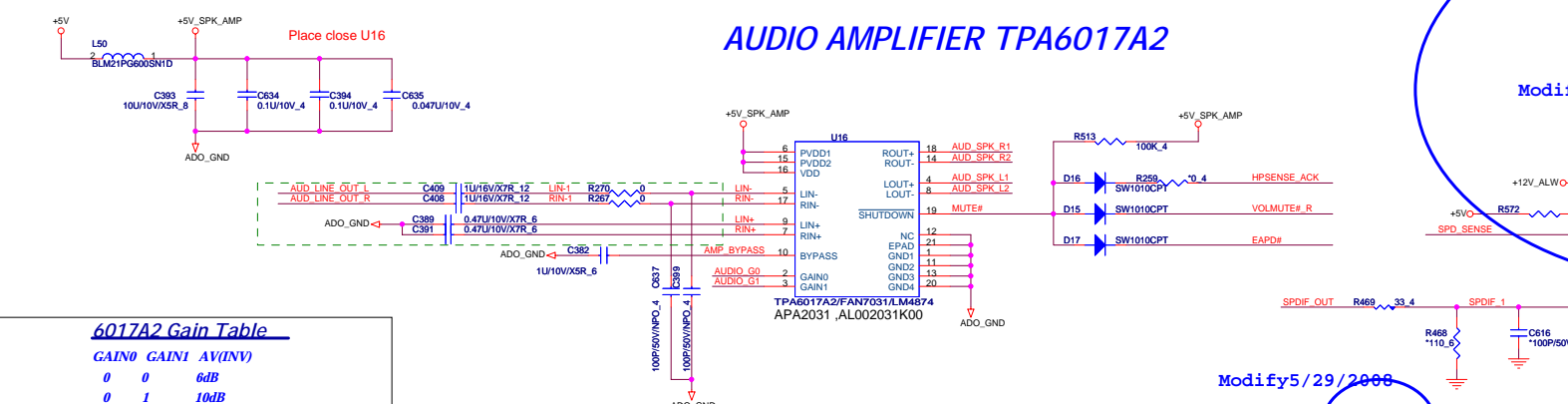
## Int. Stereo Speakers



## Headphone out + Spdif Out (normal open)



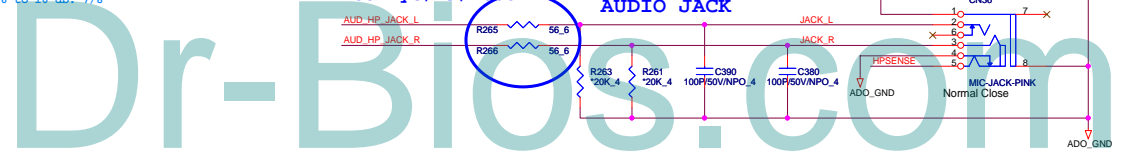
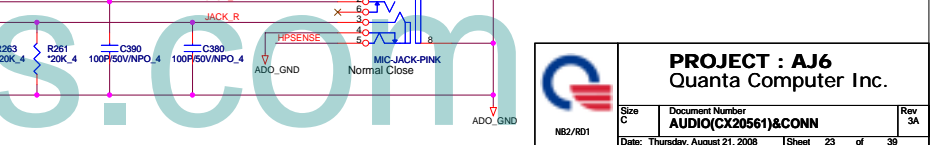
## AUDIO AMPLIFIER TPA6017A2



## Modify5/29/2008



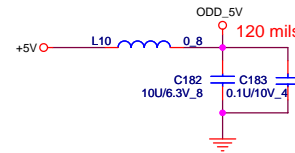
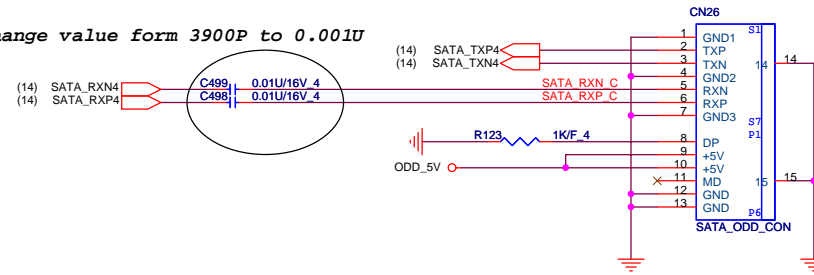
## AUDIO JACK



# SATA CD-ROM

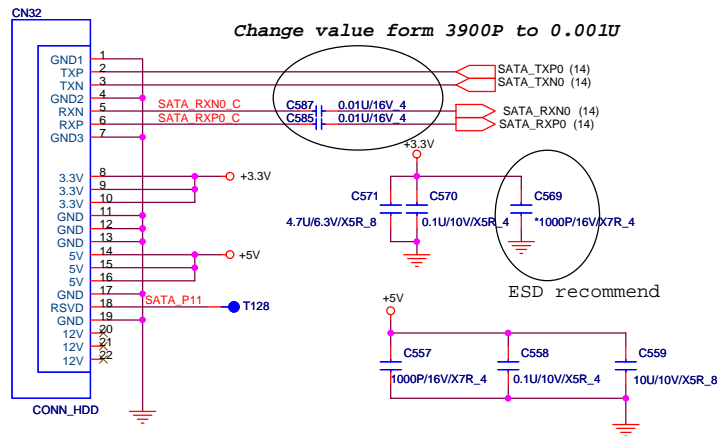
NEW PART check Pin define

Change value form 3900P to 0.001U

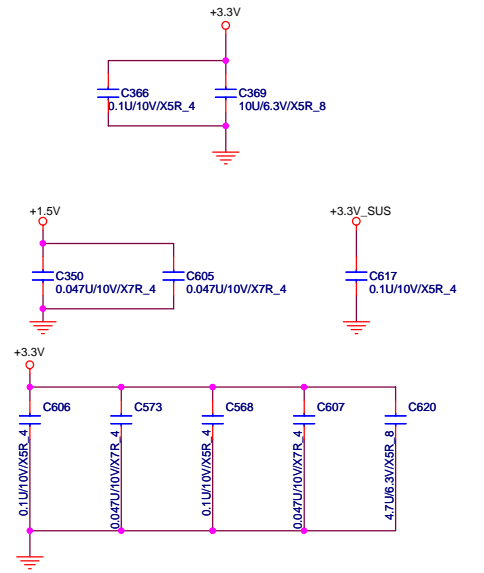
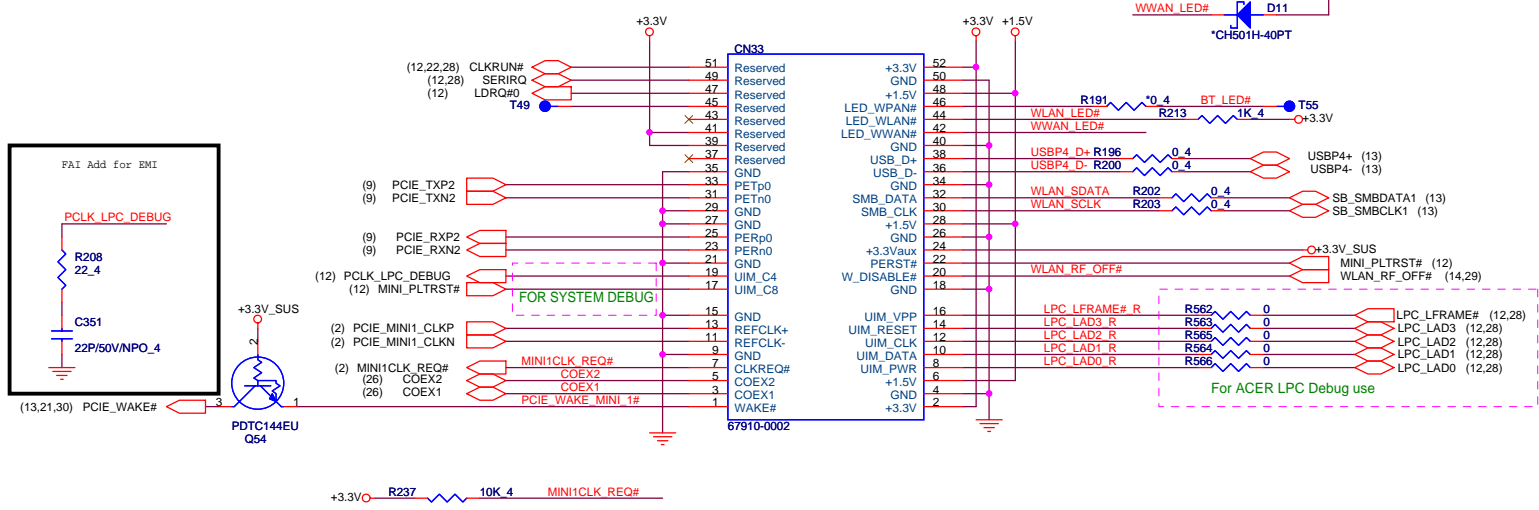


## SATA CONNECTOR

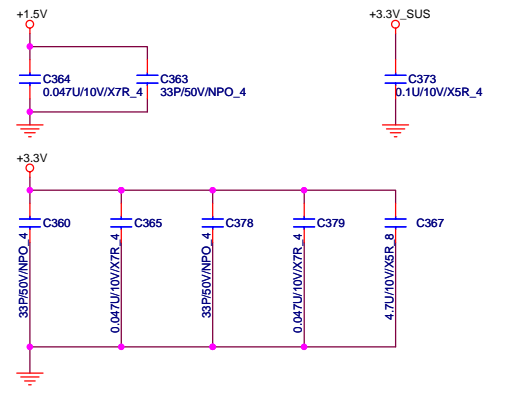
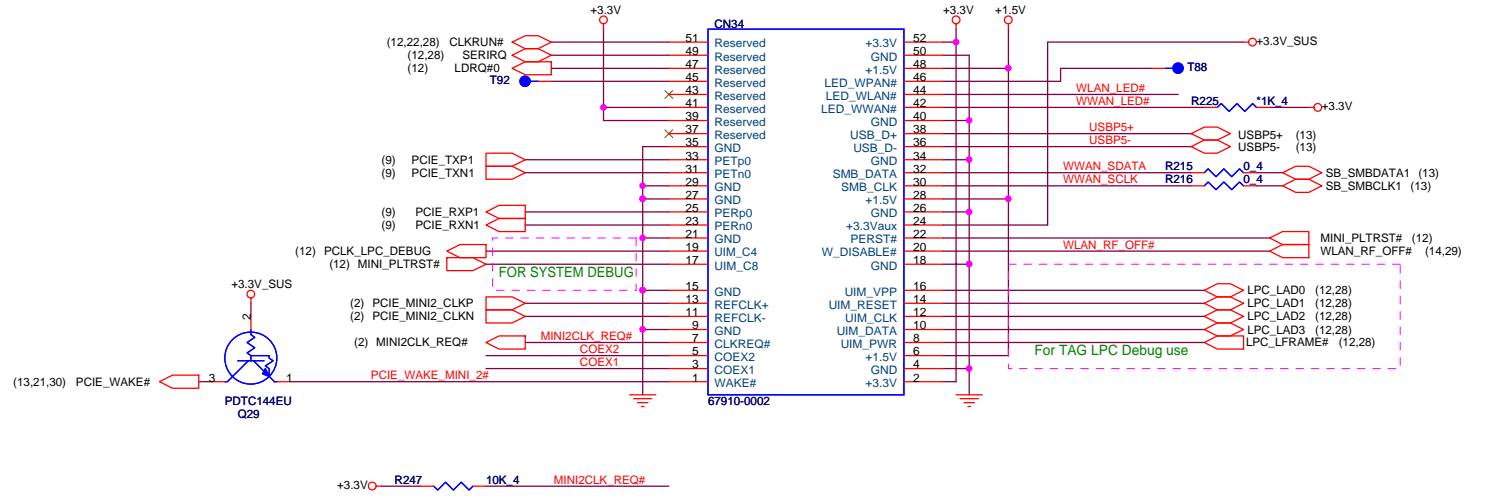
Change value form 3900P to 0.001U



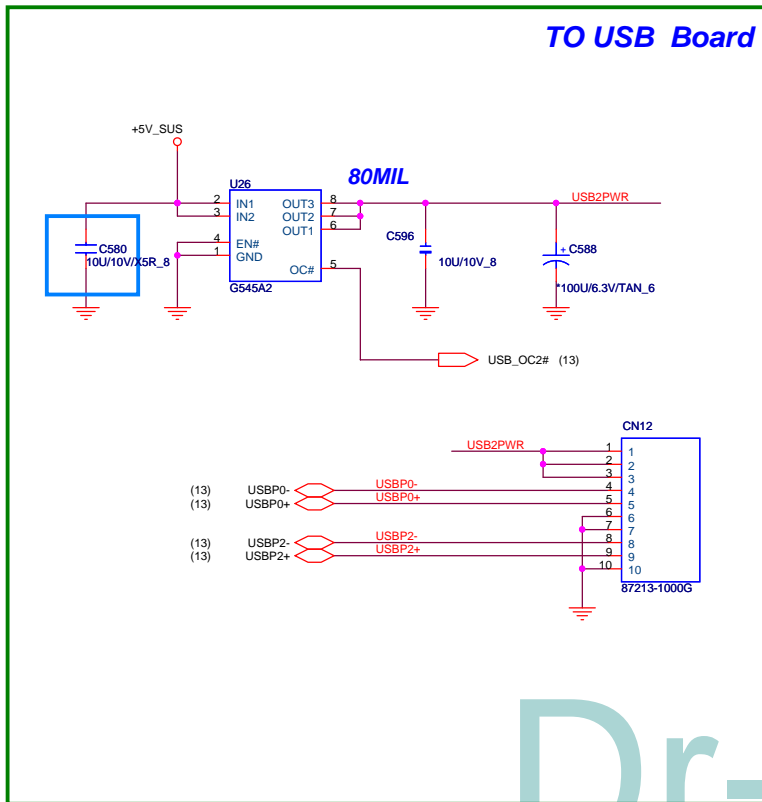
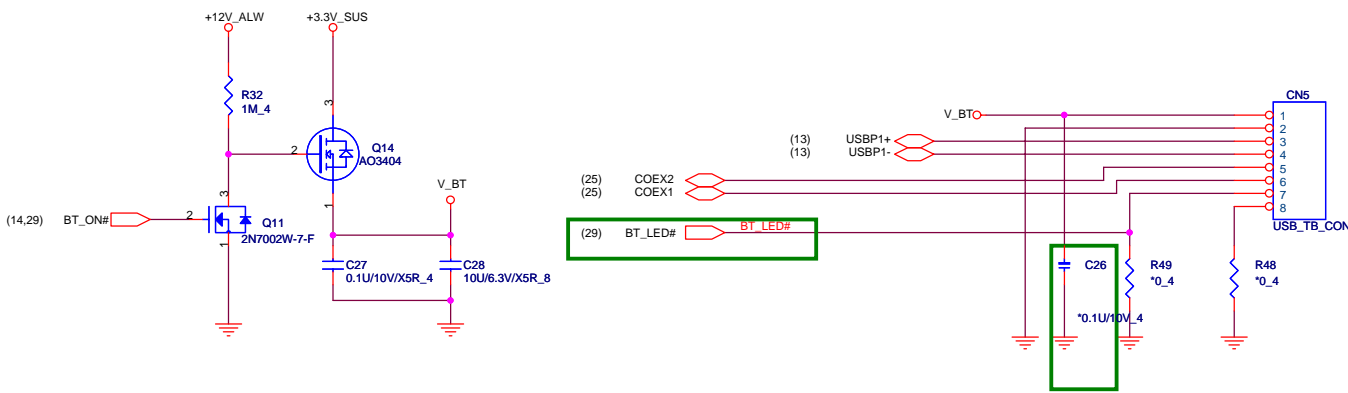
### MiniCard WLAN connector 1



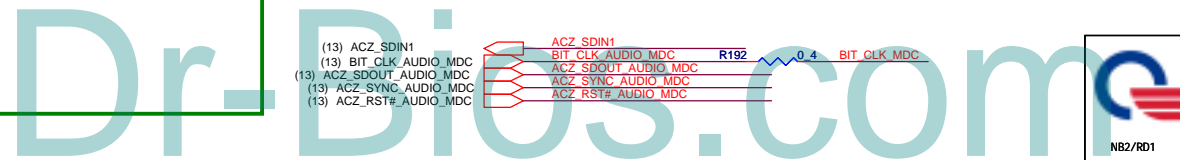
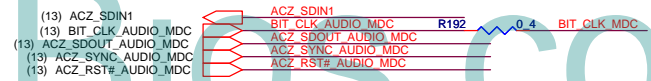
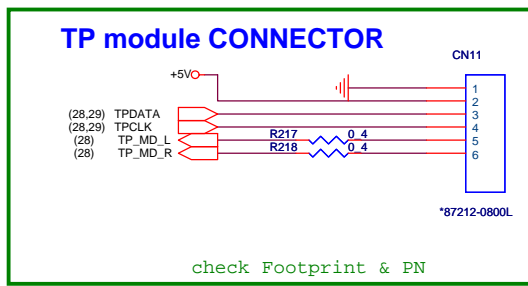
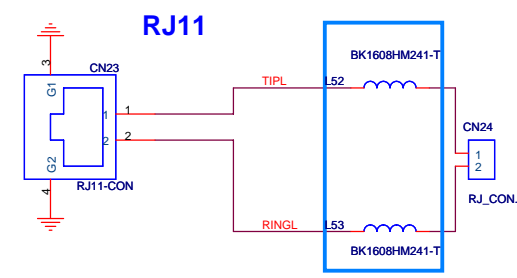
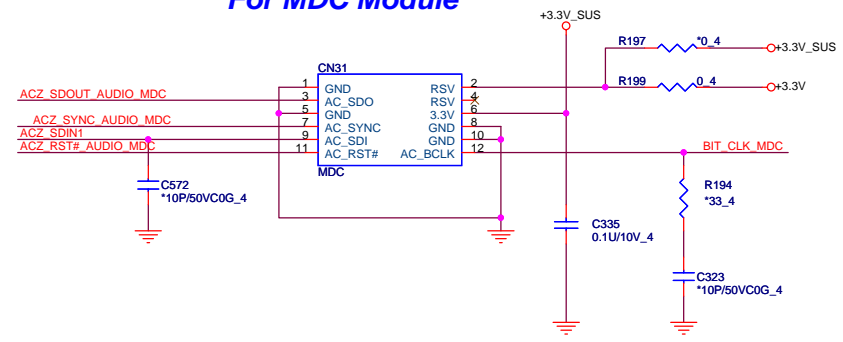
### MiniCard connector 2



# BLUETOOTH CONNECTOR

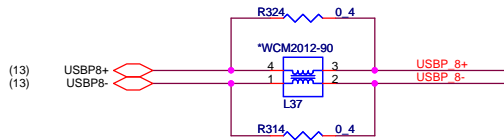
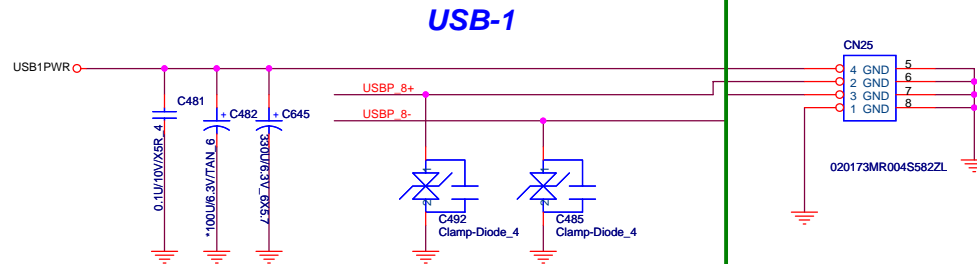
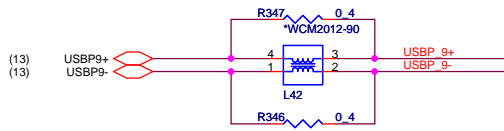
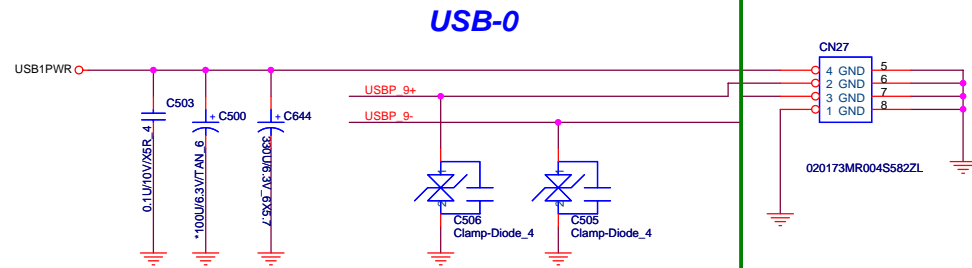
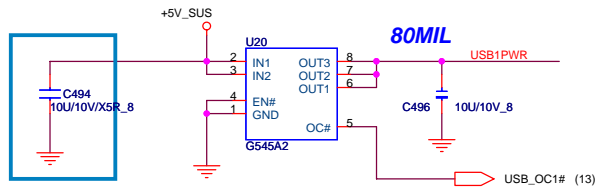


## For MDC Module

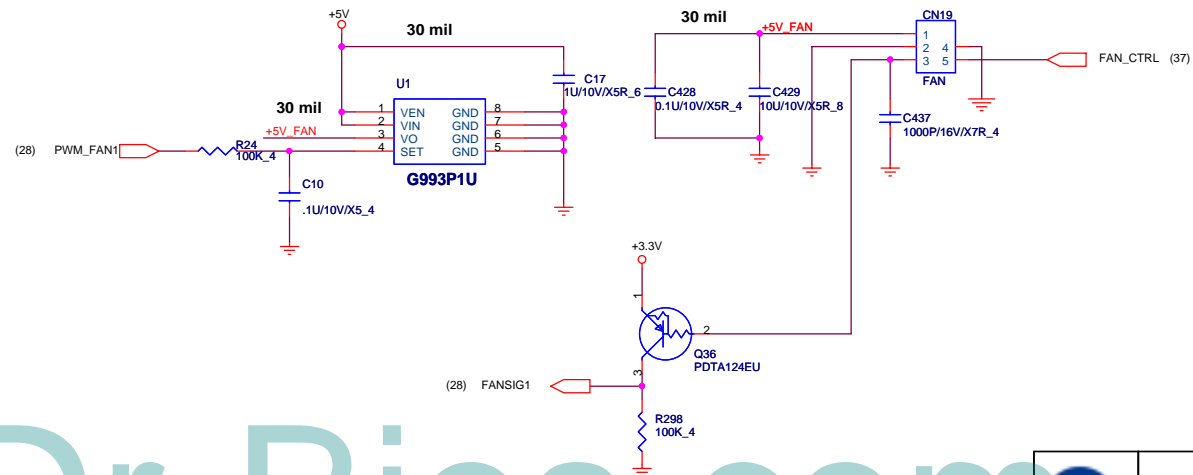


<b>PROJECT : AJ6</b> Quanta Computer Inc.		
Size Custom	Document Number <b>Bluetooth,RJ11, MDC,Small/B</b>	Rev 3A
NB2/RD1	Date: Thursday, August 21, 2008	Sheet 26 of 39



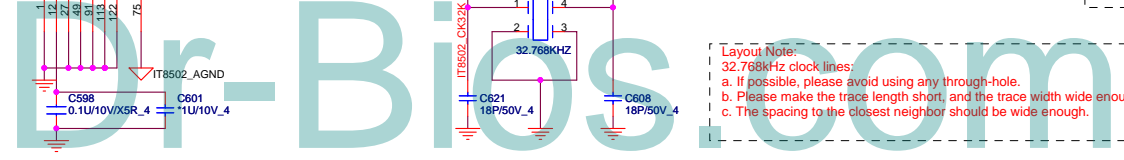
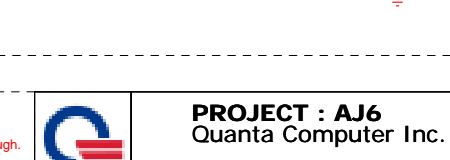
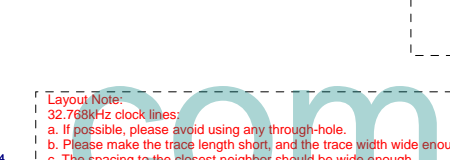
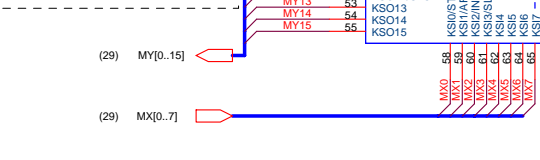
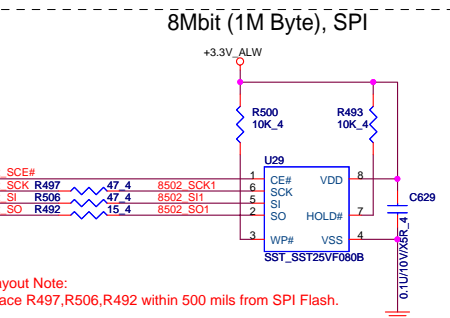
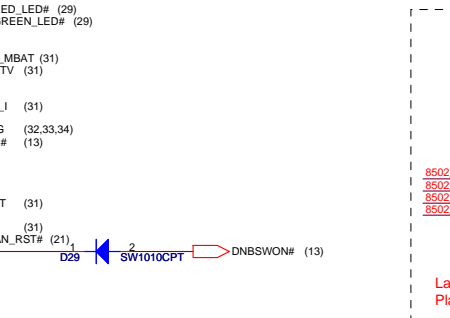
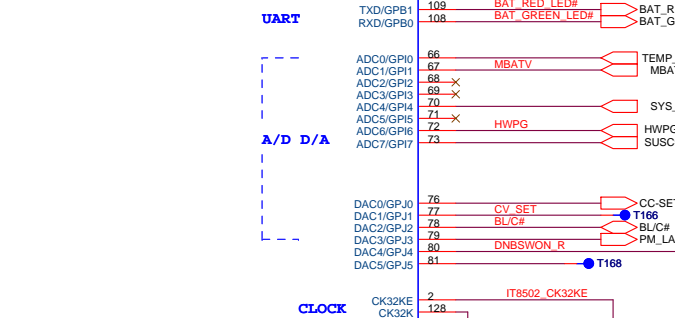
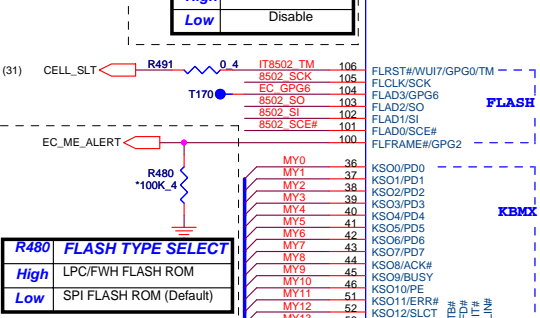
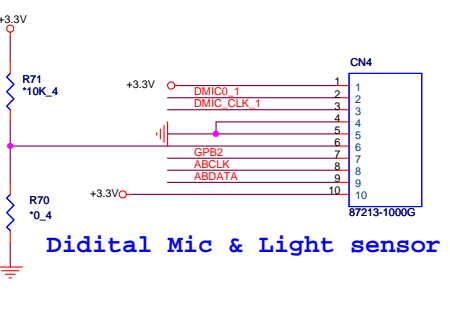
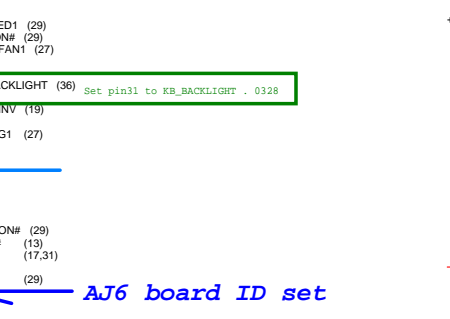
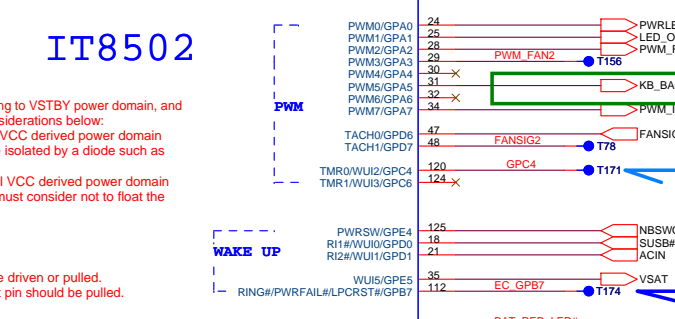
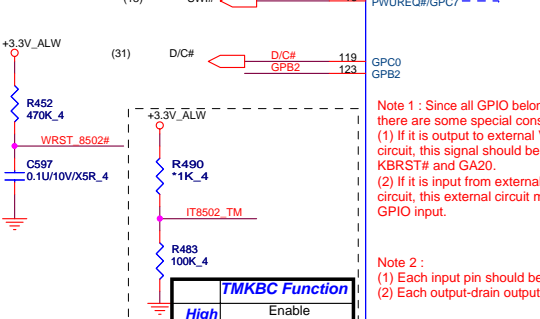
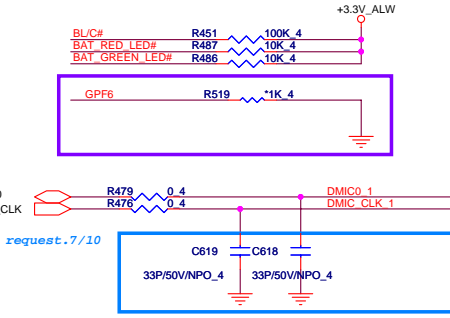
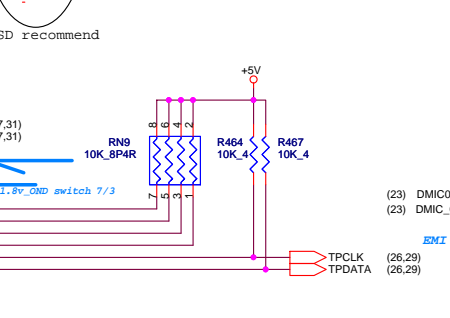
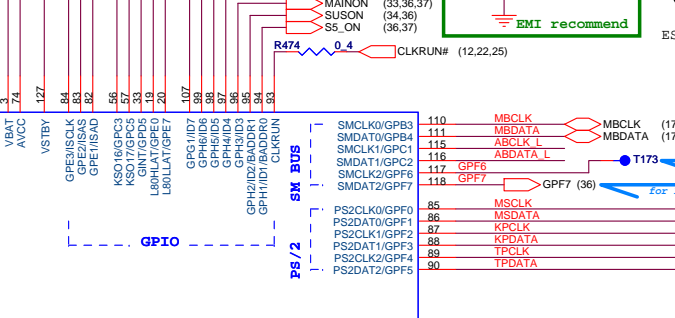
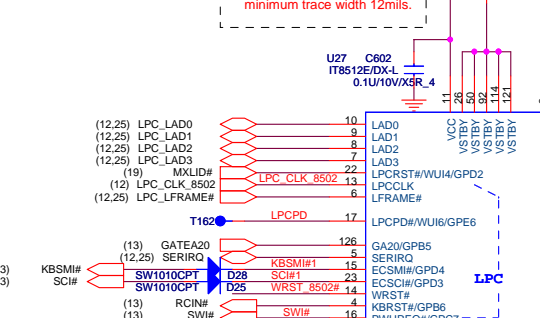
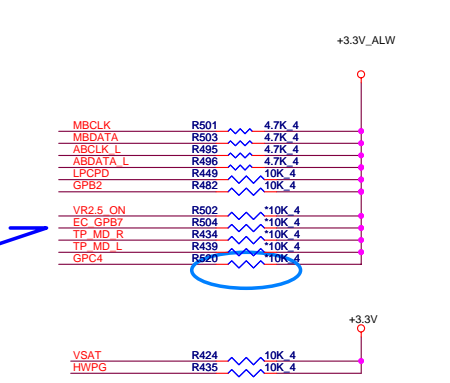
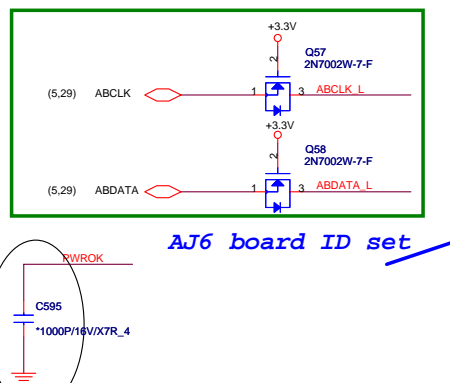
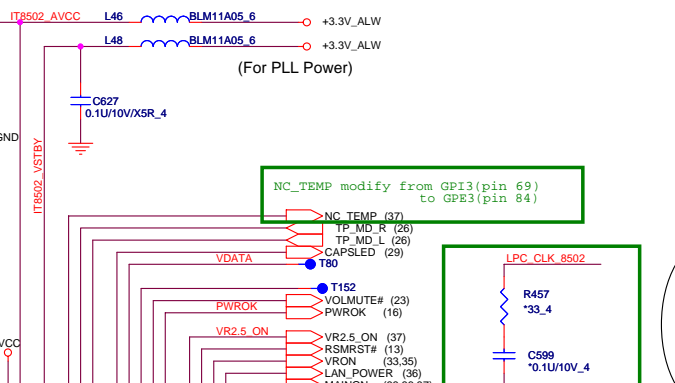
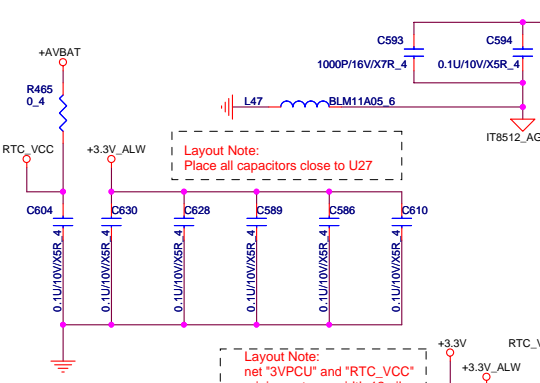
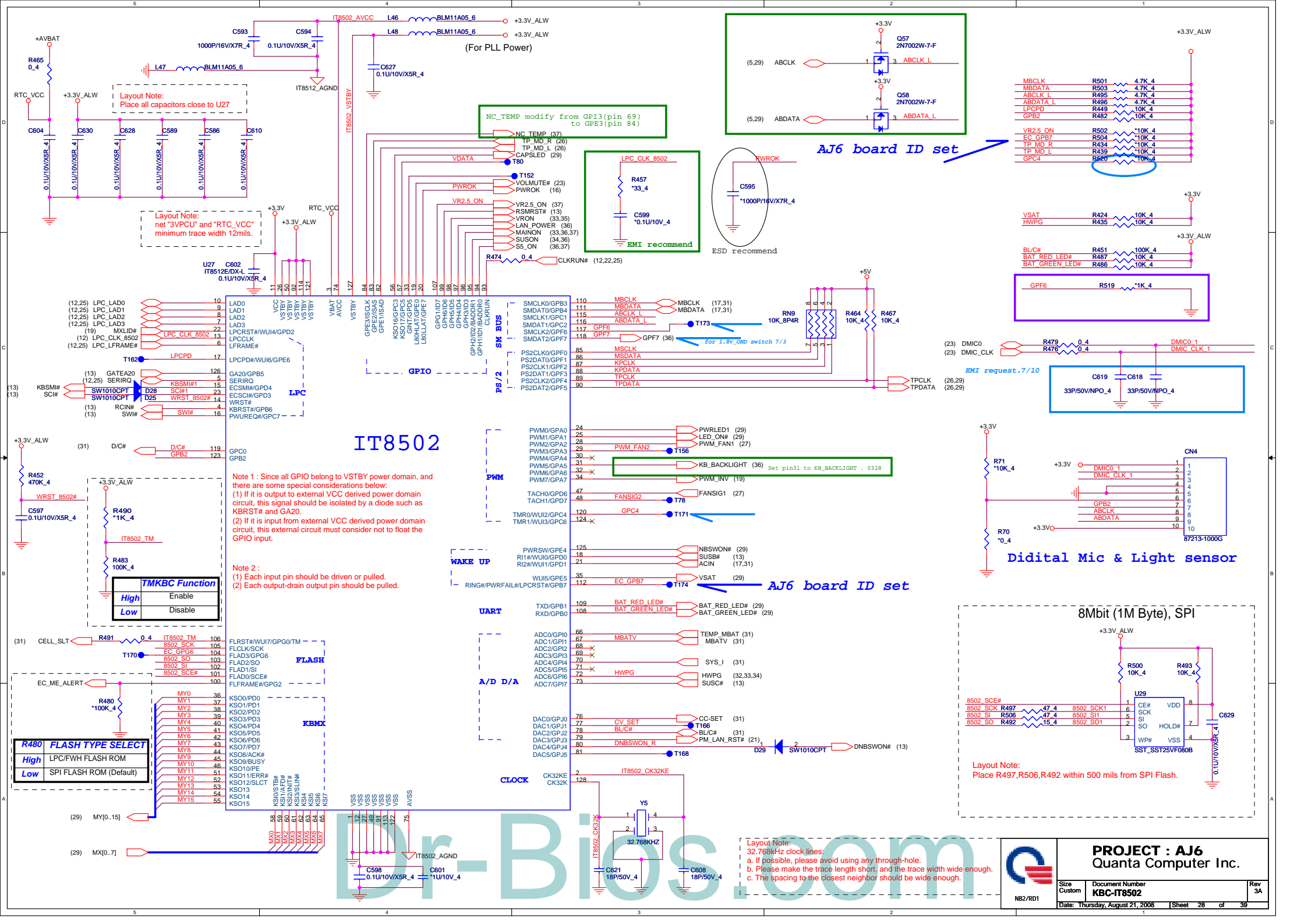


### CPU FAN

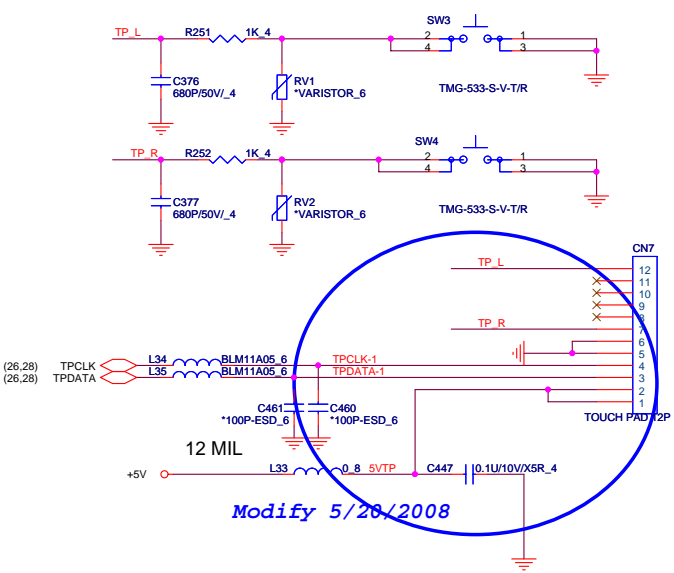


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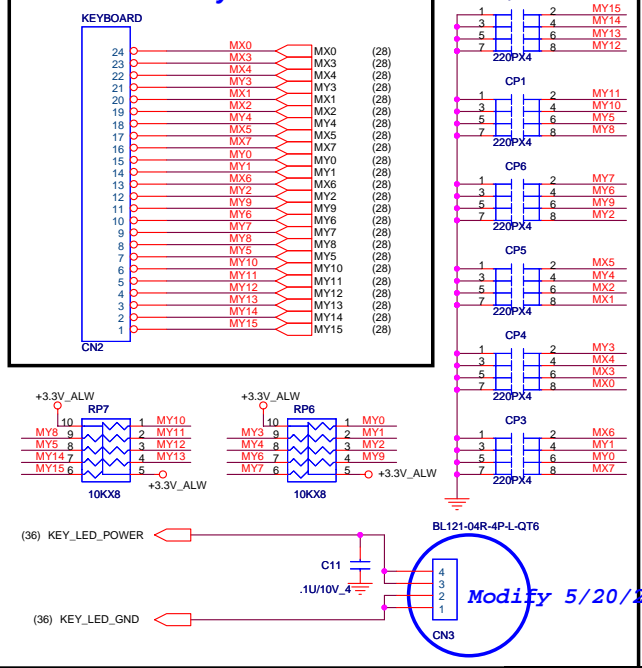
<b>PROJECT : AJ6</b> Quanta Computer Inc.		Rev 2A
Size Custom	Document Number <b>USB CONN X3ports</b>	
Date: Monday, August 18, 2008		Sheet 27 of 39



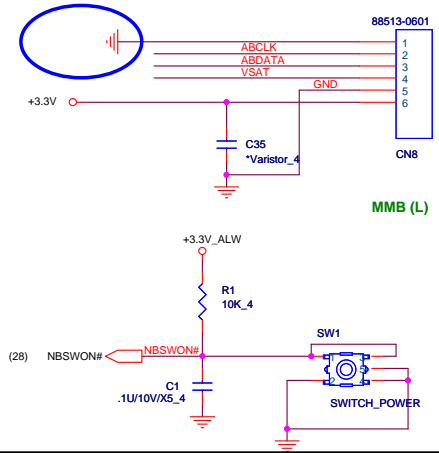
# TOUCHPAD SWITCH CONN



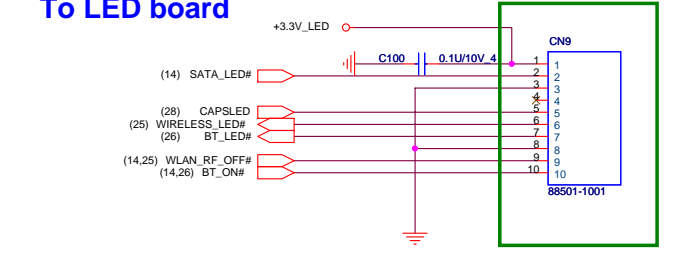
# KEYBOARD For New Keyboard use.



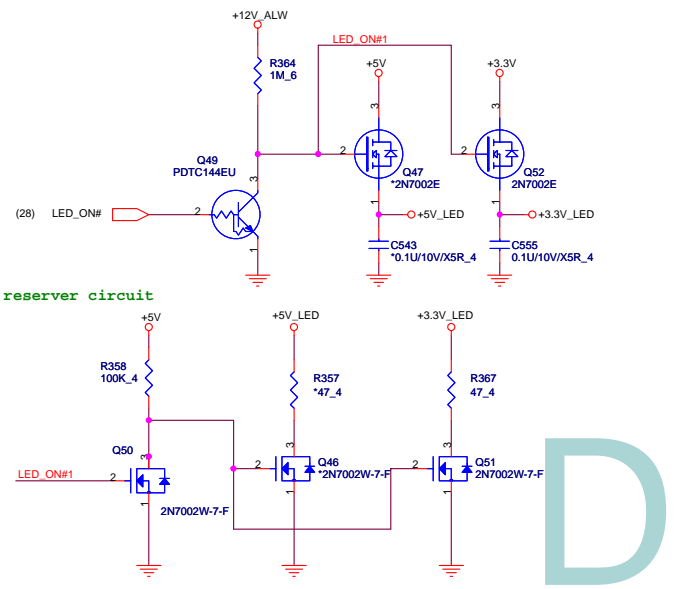
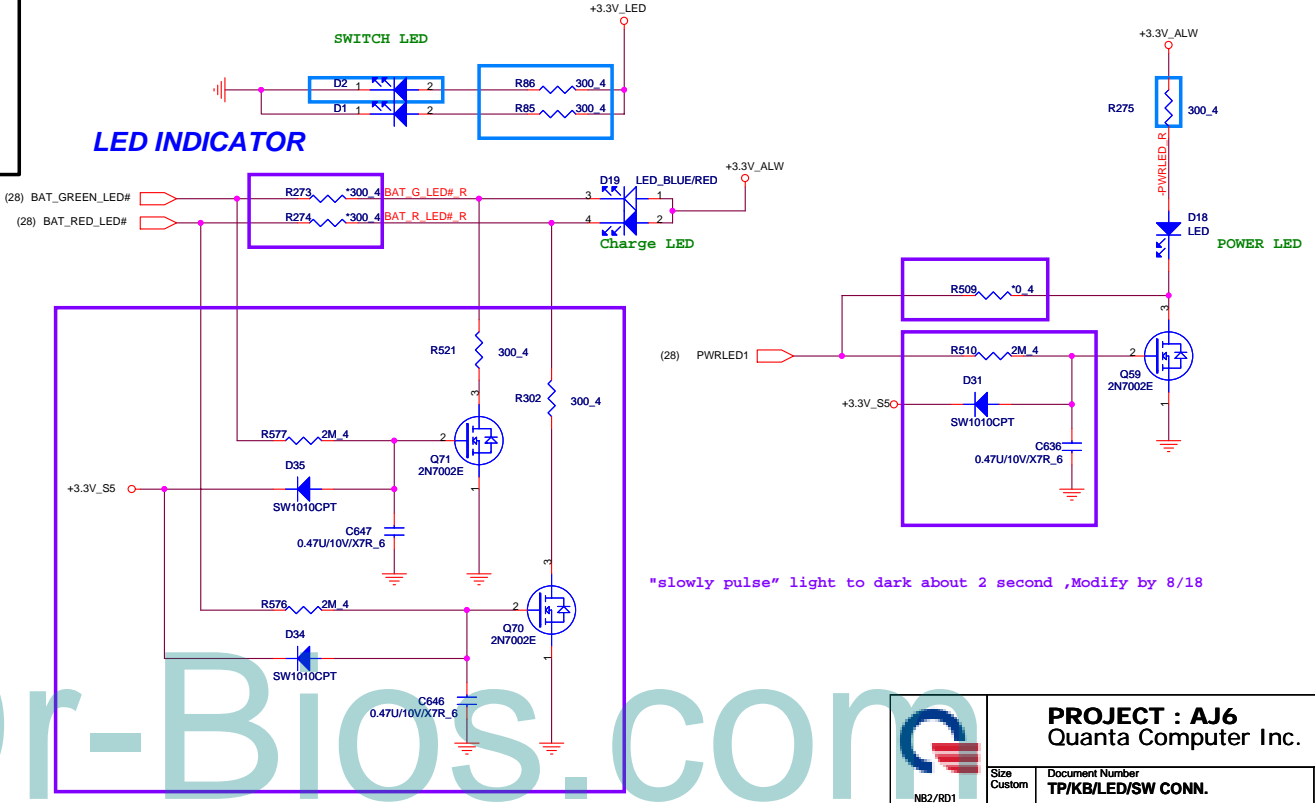
Modify 6/02/2008



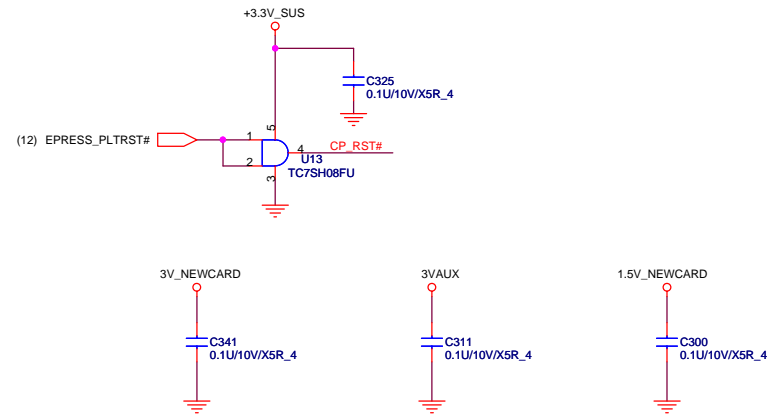
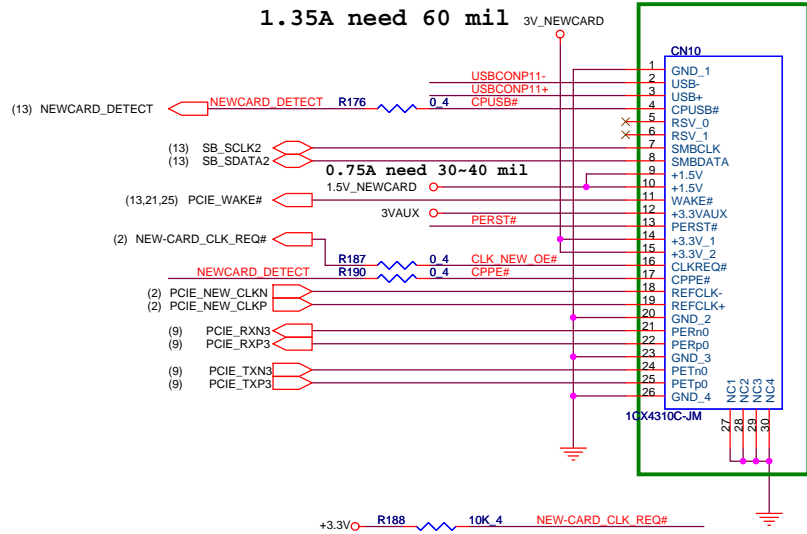
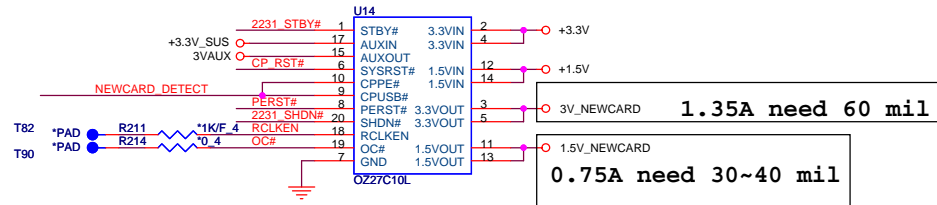
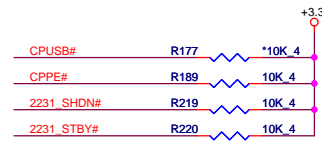
# To LED board



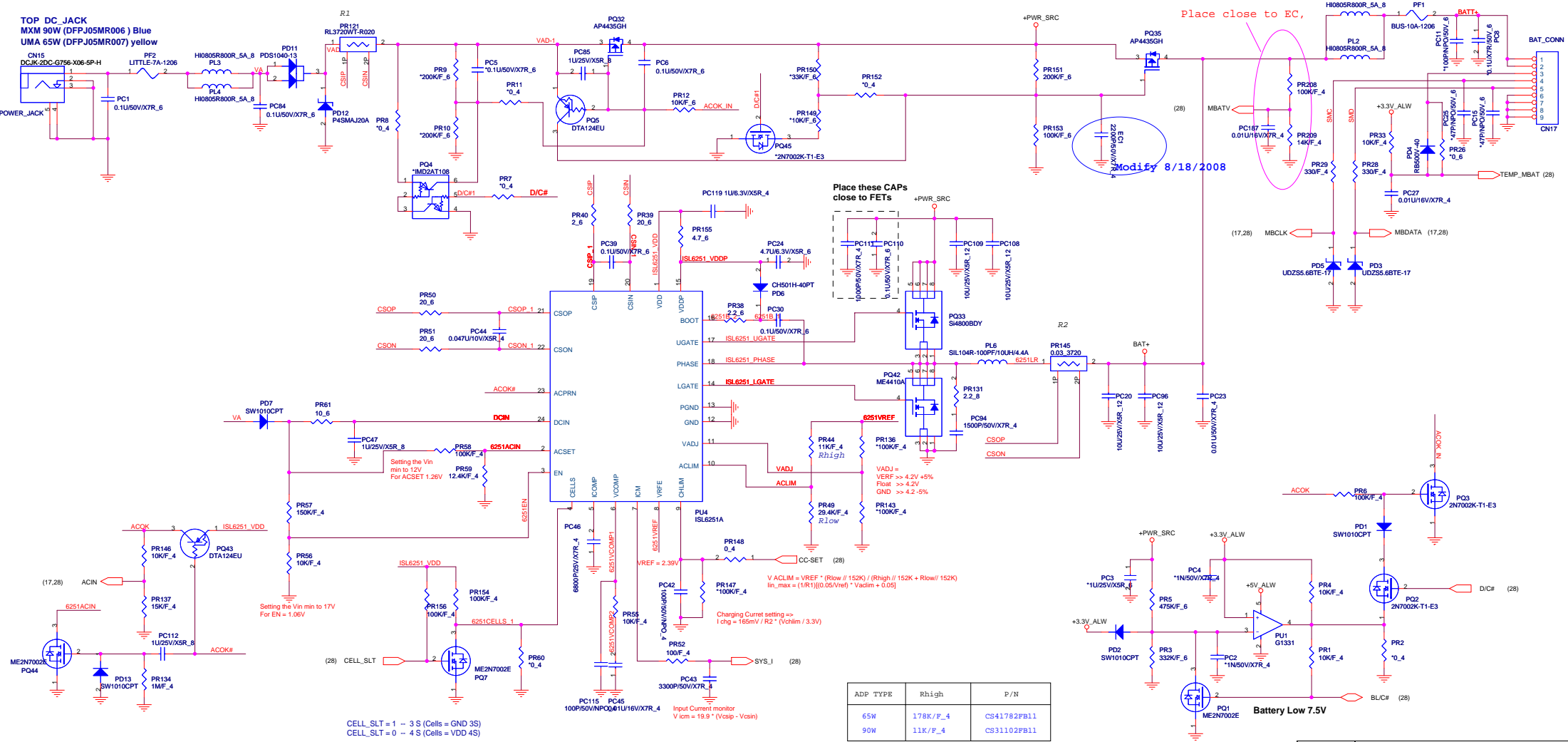
# LED INDICATOR



# NEWCARD



# BATTERY CHARGER



**PROJECT : AJ6**  
 Quanta Computer Inc.

Size: Custom  
 Document Number: **CHARGER (ISL6251)**  
 Rev: 3A

Date: Thursday, August 21, 2008  
 Sheet: 31 of 39





$Ton = 3.85p * R_{TON} * V_{OUT} / (V_{IN} - 0.5)$   
 $Frequency = V_{out} / (V_{IN} * TON)$

Add 5/30/2008

Place these CAPs close to FETs

**+1.2V**  
**15A**  
**S0-S1**

C-Test Modify

C-Test Modify

B-Test Modify

B-Test Modify

**2.0A**  
**S0-S1**

B-Test Modify

**+1.1V**  
**7.0A**  
**S0-S1**

C-Test Modify

$V_o = 0.75 (R1 + R2) / R2$   
 $R_{ILIM} = I_{LIMIT} * R_{sense} / 20uA$   
 Keep R2 higher than 10Kohm

$V_o = 0.75 (R1 + R2) / R2$

$V_{out1} = (1 + R1) / R2 * 0.5$

DYN_PWR_EN	High	Low
+1.1V_DYN	1.0	1.1



**PROJECT : AJ6**  
**Quanta Computer Inc.**

Size B	Document Number <b>+1.2V &amp; +1.1V(RT8204)</b>	Rev 2A
Date: Monday, August 18, 2008		Sheet 33 of 39

**+1.8VSUS**  
**18A**  
**S0-S3**

+1.8V\_SUS

C-Test Modify

$Ra = (V_{out} - 0.75) / 0.75 * Rb$   
Rb value from 100K to 300K ohm

Fix 1.8V Output  
FAI-Test Modify

Place these CAPS close to FETs

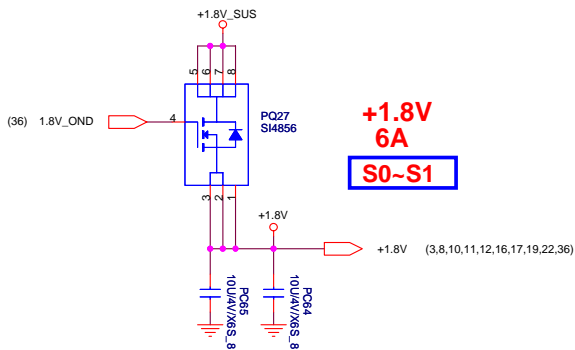
Rds(on) 7.25m ohm

B-Test modify

VDDIO\_FB\_H (3)  
Differential Pair  
VDDIO\_FB\_L (3)

$I_{lim}(Valley) = 10\mu A * R_{ILIM} / R_{DS\_ON}$   
For OCP set.

**+0.9VSMVT**  
**1.53A**  
**S0-S3**



**+1.8V**  
**6A**  
**S0-S1**

(4,6) +0.9VSMVREF

Mode	Discharge Mode
V5IN	No discharge
VDDQ	Tracking discharge
Gnd	Non-tracking discharge

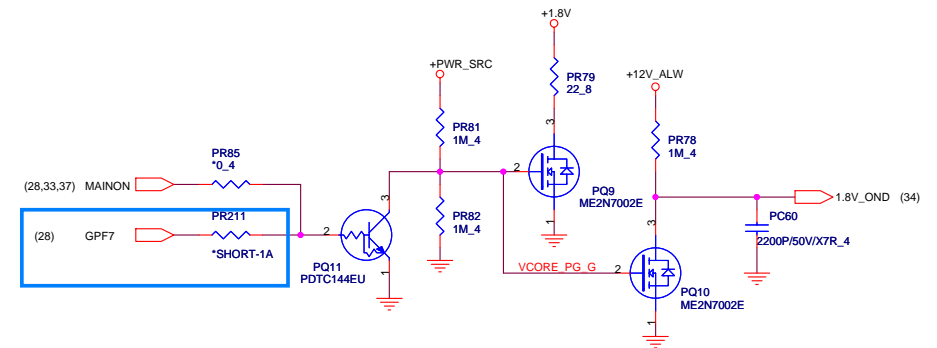
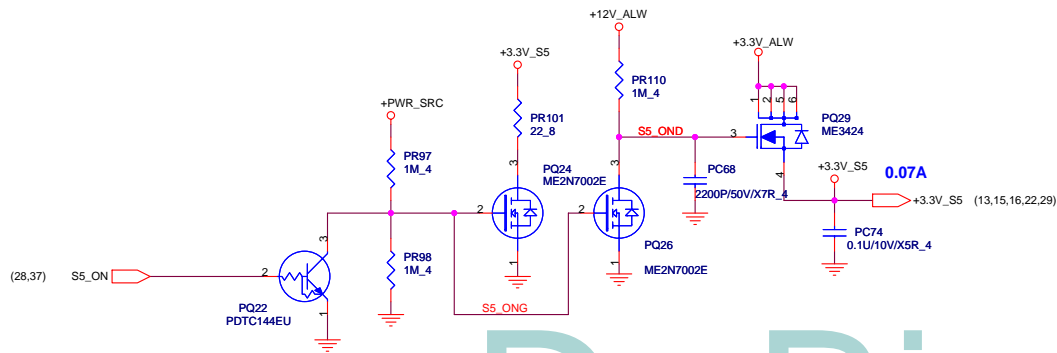
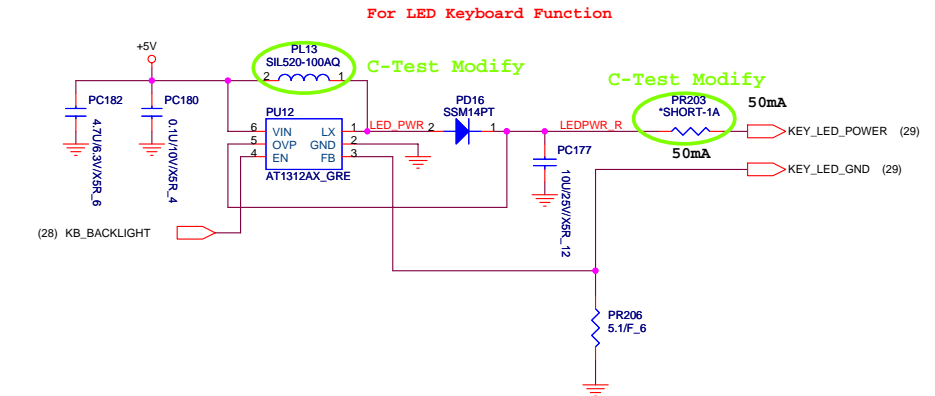
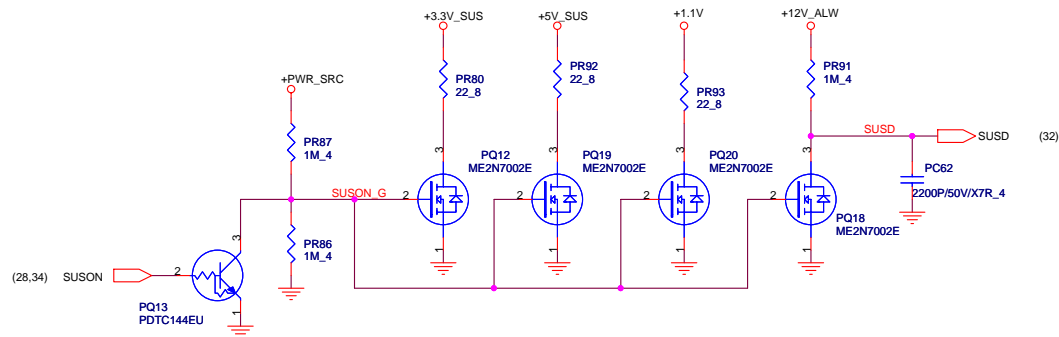
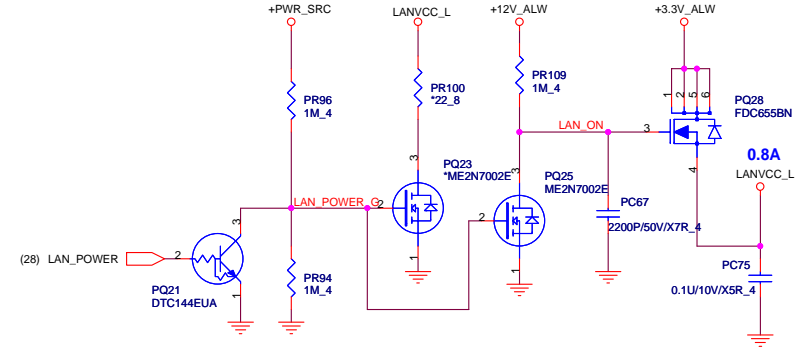
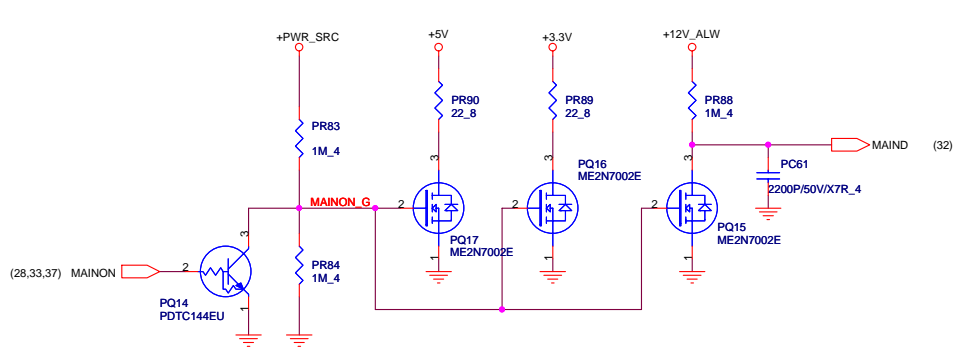
$V_{TRIP}(mV) = R_{TRIP}(Kohm) * 10(uA)$   
 $I_{OCP} = V_{trip} / R_{ds\_on} + I_{Ripple} / 2$

VDDQSET	VDDQ(V)	VTTREF and Vtt	Note
GND	2.5	$V_{\_vddqsns} / 2$	DDR
V5IN	1.8	$V_{\_vddqsns} / 2$	DDR2
FB	adjustable	$V_{\_VDDQSNS} / 2$	$1.5V < VDDQ < 3V$

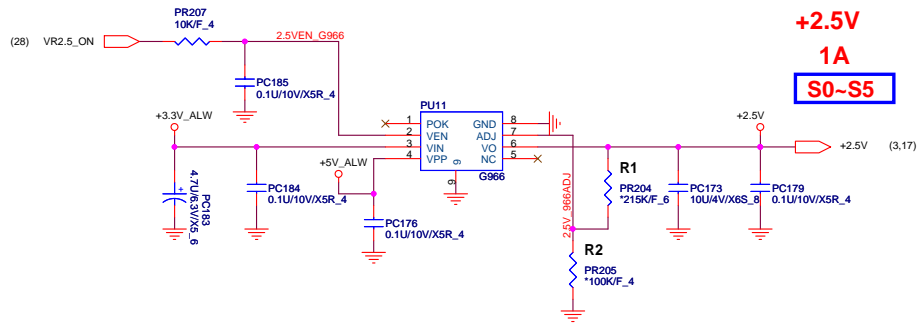
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	<b>PROJECT : AJ6</b>		Rev 2A
	Quanta Computer Inc.		
Size Custom	Document Number	1.8VSUS/DDR_VTER/+1.8V/2.5V	
Date: Tuesday, August 19, 2008	Sheet	34	of 39

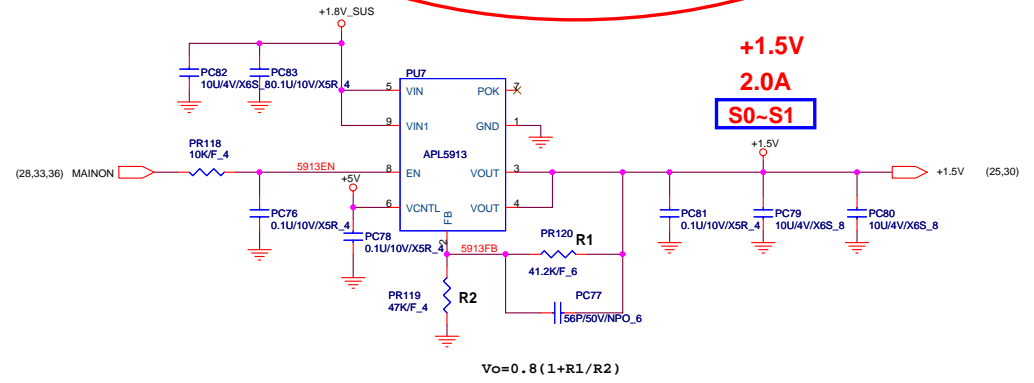
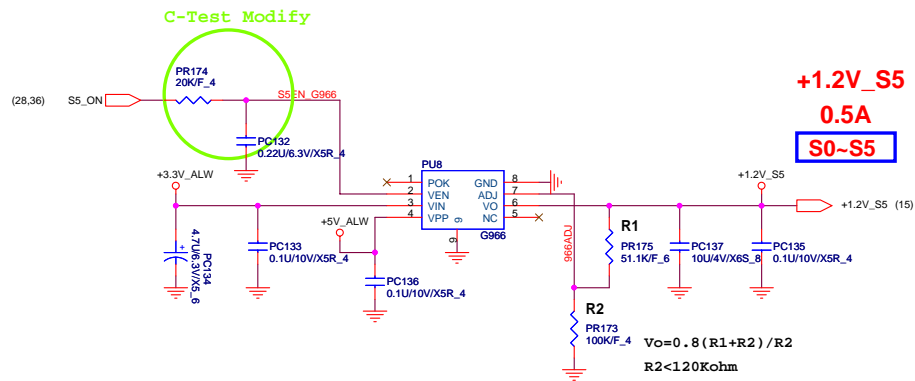
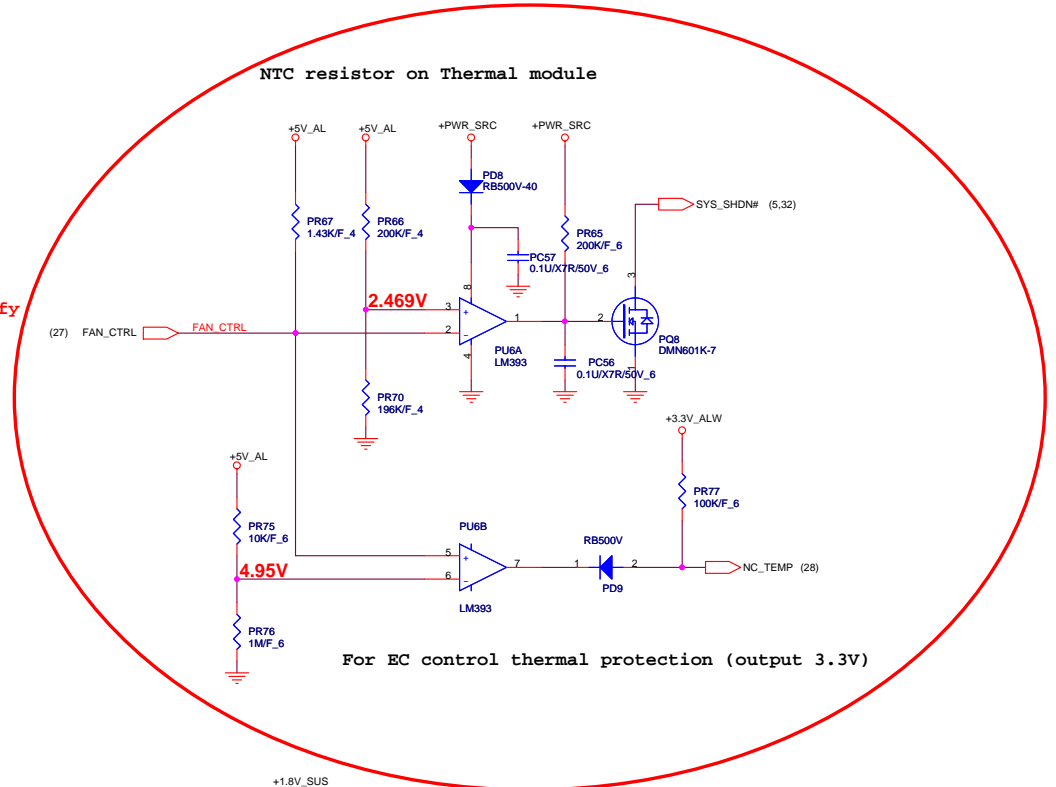





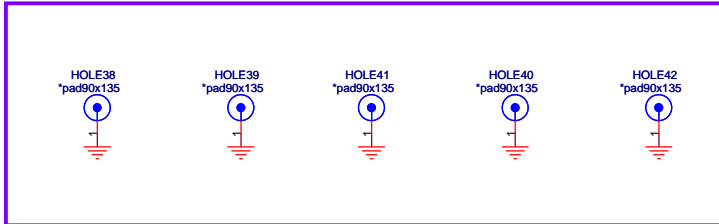
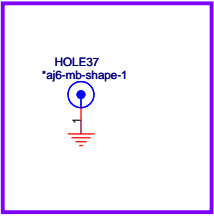
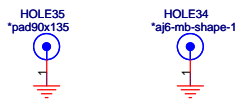
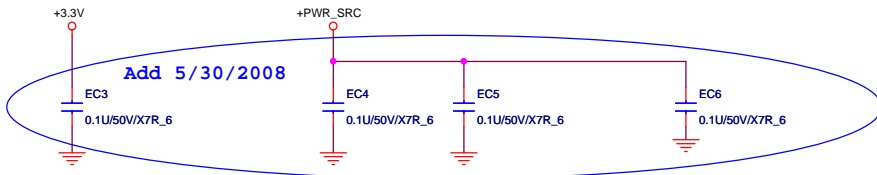
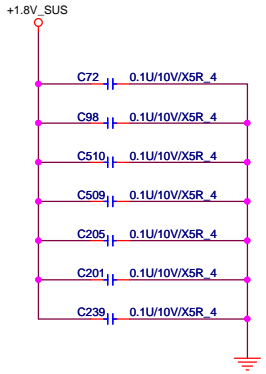
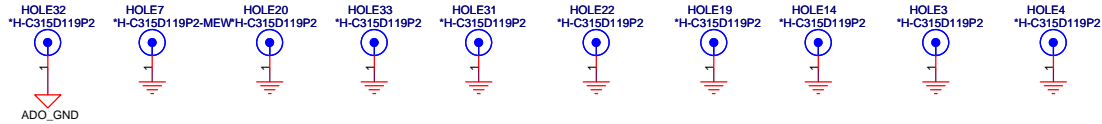
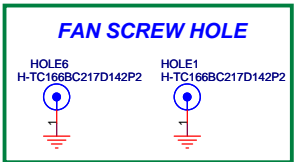
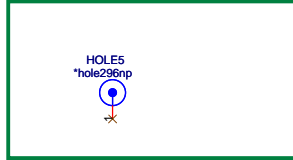
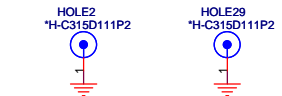
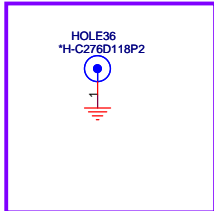
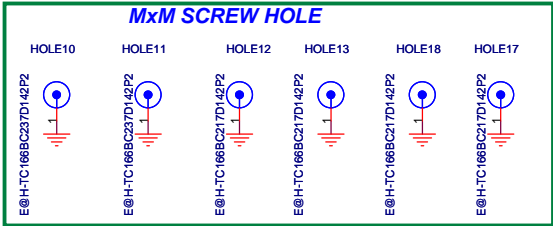
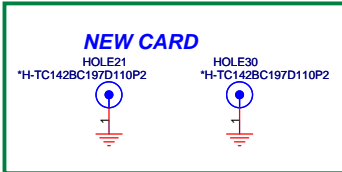
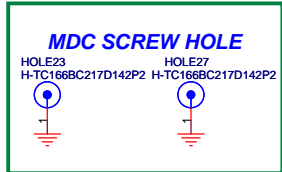
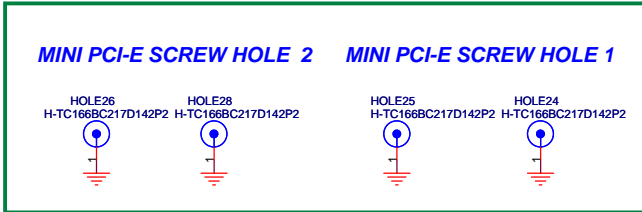
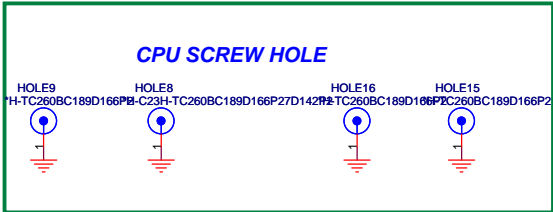
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B-Test Modify



 NB2/RD1	<b>PROJECT : AJ6</b> Quanta Computer Inc.		Rev 2A
	Size Custom Document Number <b>1.2V_S5/+1.5/+2.5V</b>	Date: Monday, August 18 2008	Sheet 37 of 39





MODEL: REV

### CHANGE LIST

PAGE	AJ6 MB	
	FROM	TO
1	1A	
2	1A	3B
3	1A	
4	1A	
5	2A	
6	1A	
7	1A	
8	1A	
9	3A	
10	3A	
11	1A	3B
12	1A	
13	1A	
14	3A	
15	2A	
16	1A	
17	3A	3B
18	2A	
19	3A	
20	1A	
21	3A	
22	1A	
23	3A	
24	3A	
25	2A	
26	3A	
27	2A	
28	3A	
29	3A	3B
30	1A	
31	3A	
32	2A	
33	2A	
34	2A	
35	2A	3B
36	2A	
37	2A	
38	2A	
39	3A	3B

1A **First release**

2A

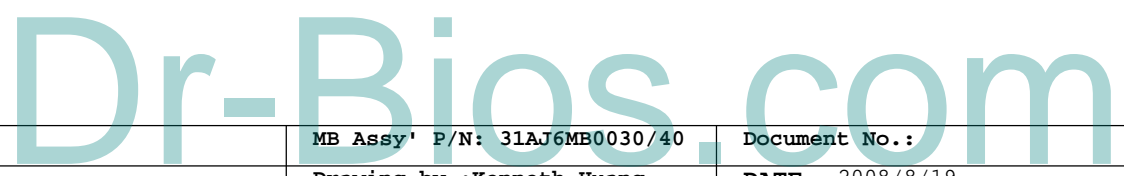
Page5:Add Q66,Q67 for EC drivinng / Add Q68,R574 & swap U3 pin4, pin6 for system shutdown  
Page9:Change PCIE CAP. from X5R to X7R & modify C\_PEG\_TX for UMA's HDMI detect issue  
Page10:Delet R115 for UMA SKU.  
Page15:Modify R83,R184,R368,R370,R371,R372,R,386,R387,R391,R392 for board ID / Chanhe C338,C327 for accuracy  
Page17:Add Q60,R517 for MXM discharge / Add R516,D32 for MXM timing / Modify C215,C210,C209,Q19,C238 for MXM power express /Add Q62,Q63 for MXM smbus  
Page18:Add Q61,R518 for HDMI HPD sense issue / modify Q1,Q2 for UMA HDMI smbus issue / delete D4,D5 & change R5,R6 value  
Page19:Modify & add Q69,C656,C657R567,R569 for LCD slight light issue / Add RP40 for MXM  
Page21:Add R95 for Lan chip power / change R60,R61,R62,R63 package  
Page23:Add Q64,Q65,R570,R571,R572 for SPDIF's LED issue / Change R271,R272,R265,R266 for volume issue /Change R473,R472,R471,R470 for EMI issue  
Page25:Add R562,R563,R564,R565,R566 for Acer LPC debug use / Add D12,R213 for WLAN LED  
Page26:Delete MODEM CAP. C166,C165  
Page27:Add C644,C645 for USB  
Page28:Modify U27 pin112 to AJ6 board ID setting / Swap pin98 & pin107 / Delete C601 for IT8502 issue /Change C621, C608 of value for accuracy  
Page29:Swap NC7,CN3 connector & modify circuit / Modify CN8 circuit / Delete R357 is no use  
Page32:Add a resister to connect PU9 pin1 and pin32 / Add PC160 in the circuit.  
Page33:Change PU5 PN from AL008204000 to AL08204001 / Change PR159 PN to CS23402FB08 / Add PR20, PC13, PC127 in the circuit / Delete PC117, PC123, PC121 in the circuit  
Page34:Change PR191 from 51.1K/F\_4 to 52.3K/F\_4 (CS35232FB10).  
Page35:Delete PC17, PC18 in the circuit / Add PC91 in the circuit  
Page36:Add PR90,PR89,PR80,PR92,PR93,PR101,PR79,PQ17,PQ16,PQ12,PQ19,PQ20,PQ24,PQ9 in the circuit for discharge  
Page37:Add PR67, PR66, PD8, PC57, PR65, PQ8, PC56, PU6, PR70, PR75, PR76, PD9, PR77 in the circuit for Acer thermal protection  
Page38:Add EC3,EC4,EC5,EC6 for EMI

3A

Page9:Add R45,R51,R64,R65,R68,R69,R72,E73 to solve the HDMI issue  
Page10 : for CRT fillicker, change C179,C191,C491,C125,C192 value from 2.2u to 10u.  
Page14 : change the board ID. 7/10  
Page17 : Duo to cost down, so to remove Q25 ,Q45 from MXM BOM.  
Page19 : add LCD panel circuit to fix white display when system boot up.  
Page21 : to solve the Lan issue, ADD C479,C480  
Page23 : change Gain from 15.6 to 10 db. 7/8  
Page24 : Change C498,C499 ,C585,C587 value form 3900P to 0.001U  
Page26 : to solve the EMI issue, ADD L52,L53  
Page28 : For EMI request. add C618,C619 7/10  
Page26 : to solve the EMI issue, ADD L52,L53  
Page29 : Change R509 PN from 2M to 0ohm. Change R85,R86,R275 ,R273,R274 to 300 ohm, Del D31& C636 & D2 from BOM  
Page26 : to solve the EMI issue, ADD L52,L53  
Page31 : PLL13 PN change to CV01014T201

3B

Page2 : ADD C648(CH11006JB00) , for EMI request ( +1.2v)  
Page11 :Change C56 and C493 from 4.7u/6.3V to 330u/2V (CH733RY8802) to solve" HIGH POWER NOSIE ISSUE"  
Page17 :Add C238 ( CC71004MZ81) to solve" HIGH POWER NOSIE ISSUE"  
Page29 :For slowly pulse" light to dark about 2 second, ADD R510,R576,R577, Q70,Q71,D34,D35 ,C636,C646,C647 ,R302 ,R521 ; DEL R273,R274,R509  
Page35 :Change PC90 and PC92 from 10u/25V to 27u/25V (CC62704MZ02) to solve" HIGH POWER NOSIE ISSUE"



Project :AJ6 MB  
Approved by : Johnny\_0

MB Assy' P/N: 31AJ6MB0030/40  
Drawing by :Kenneth Huang

Document No. :  
DATE: 2008/8/19

		<b>PROJECT : AJ6</b>	
		Quanta Computer Inc.	
Size Custom	Document Number	Rev 3B	
NB2/RD1		EC	
Date: Thursday, August 21, 2008		Sheet 39	of 39