

# Compal Confidential

## KBYF0 Schematics Document

AMD Griffin Processor with RS780M+SB700

(With ATI MXM/B)

2009-01-22

REV: 0.3

ZZZ1



PCB

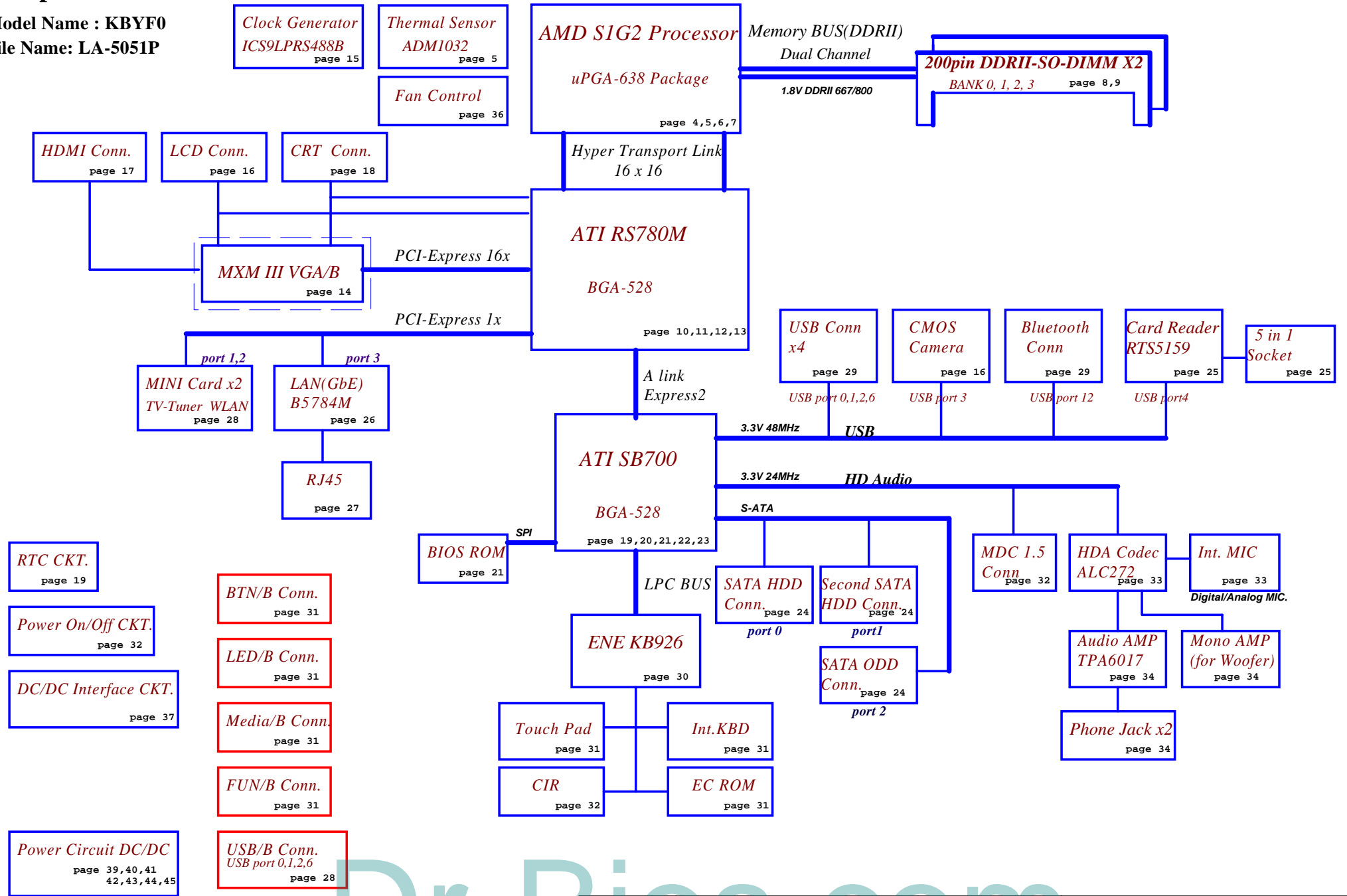
DA6000B600-\*

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Model Name : KBYF0  
File Name: LA-5051P



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### Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
B+	AC or battery power rail for power circuit.	NA	NA	NA
+CPU_CORE_0	Core voltage for CPU	ON	OFF	OFF
+CPU_CORE_1	Core voltage for CPU	ON	OFF	OFF
+CPU_CORE_NB	Core voltage for CPU	ON	OFF	OFF
+0.9V	0.9V switched power rail for DDR terminator	ON	ON	OFF
+1.1VS	1.05V switched power rail	ON	OFF	OFF
+1.2V_HT	1.25V switched power rail	ON	OFF	OFF
+NB_CORE	1.0V~1.1V switched power rail for NB VDDC	ON	OFF	OFF
+1.5VS	1.5V power rail for PCIE Card	ON	OFF	OFF
+1.8V	1.8V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA and MXM/B	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

### External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
--------	--------	-----------	------------

No PCI device

### EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADI ADM1032	1001 100X b
EEPROM(24C16/02)	1010 000X b	CPU SB	1001 101X b
MXM GMT G781-1	1001 101X b		

### EC SM Bus2 address

### SB700 SM Bus 0 address

Device	Address	Device	Address
Clock Generator (ICS9LPRS365)	1101 001Xb	Lan	
DDR DIMM0	1001 000Xb		
DDR DIMM2	1001 010Xb		
Minicard			
Minicard			

### SB700 SM Bus 1 address

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

### Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

### BOARD ID Table

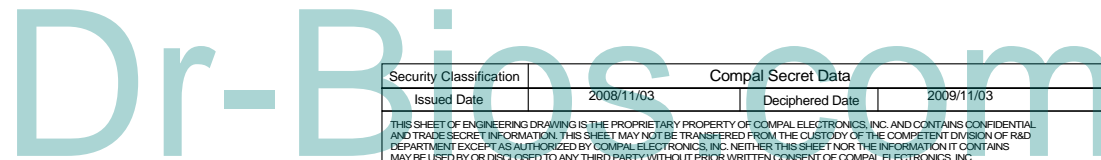
Board ID	PCB Revision
0	0.1
1	0.2
* 2	0.3 0.4 1.0
3	
4	
5	
6	
7	

### BTO Option Table

BTO Item	BOM Structure
Discrete	VGA@
UMA	UMA@

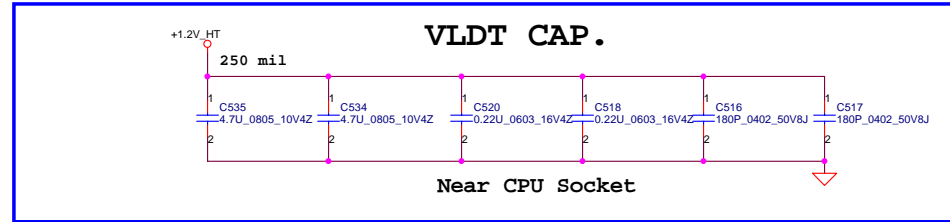
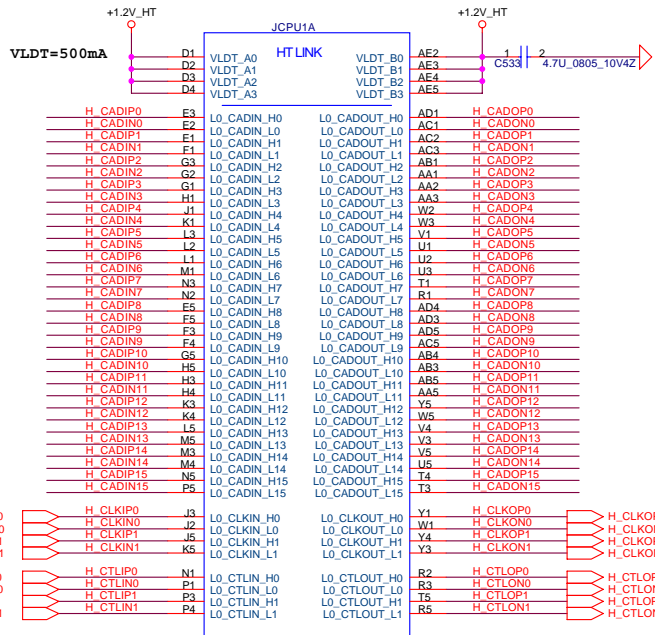
### PROJECT ID Table

Board ID	PROJECT
0	KBK0 (SJM70)
1	KBYF0 (SJV70)
2	
3	
4	
5	
6	
7	



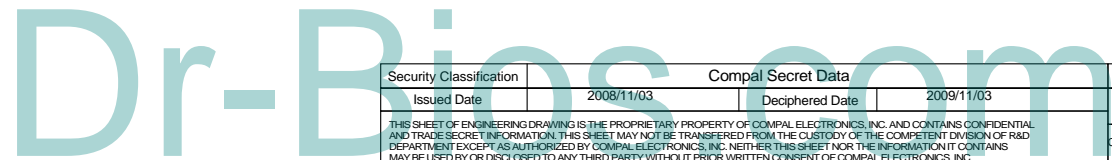
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 <10> H\_CADIN[0..15] H\_CADIN[0..15]

H\_CADOP[0..15] H\_CADOP[0..15] <10>  
 H\_CADON[0..15] H\_CADON[0..15] <10>



6090022100G\_B  
 Athlon 64 S1  
 Processor Socket  
 CONNN@

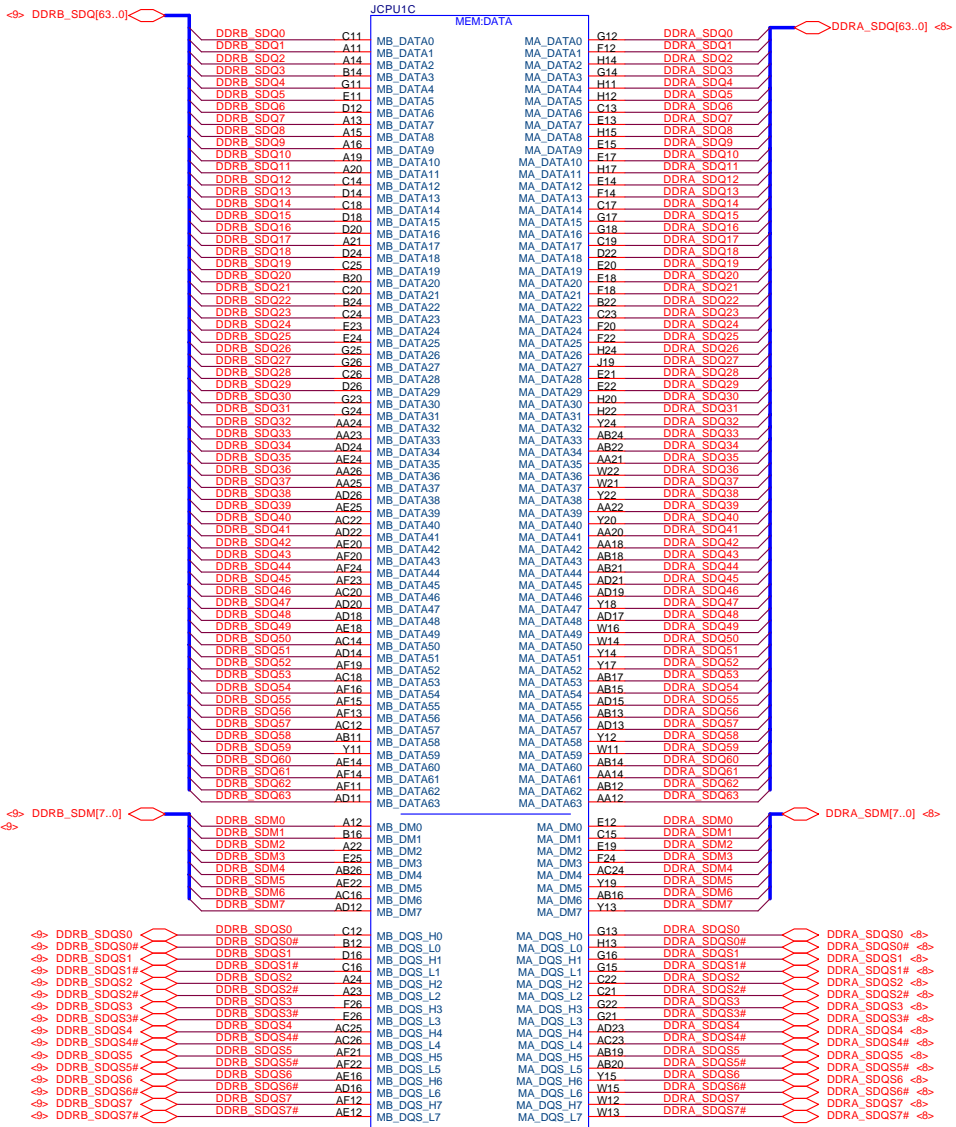
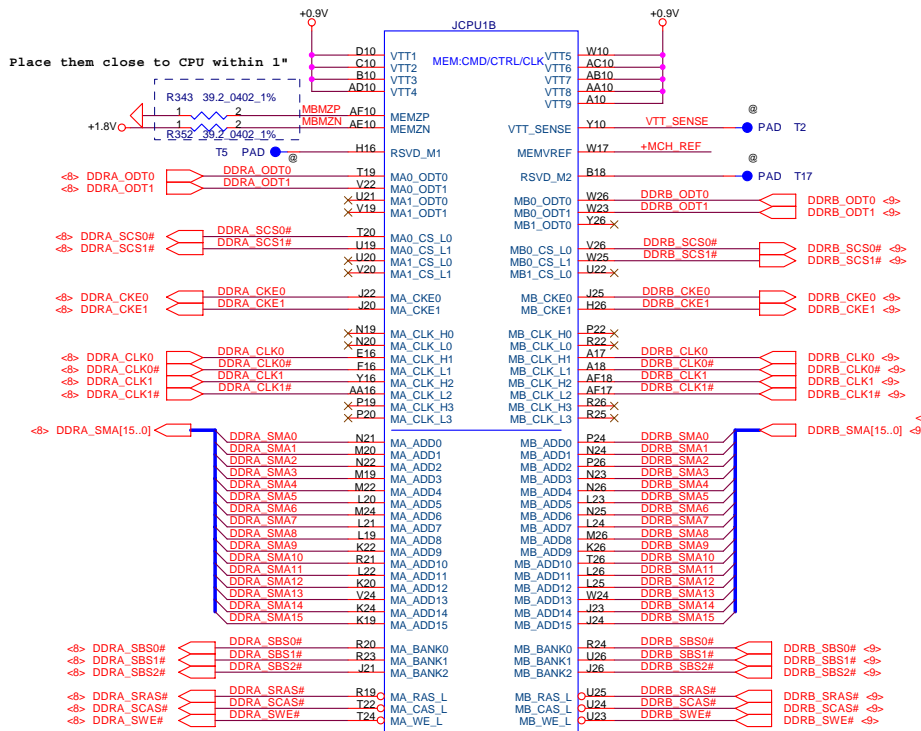
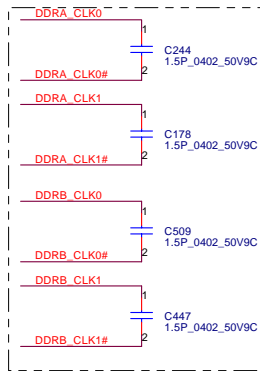
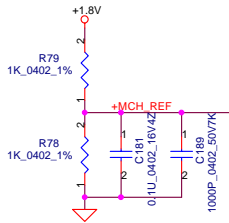
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 <10> H\_CLKIN0 H\_CLKIN0 J2 L0\_CLKIN\_L0 L0\_CLKOUT\_L0 W1 H\_CLKON0 H\_CLKON0 <10>  
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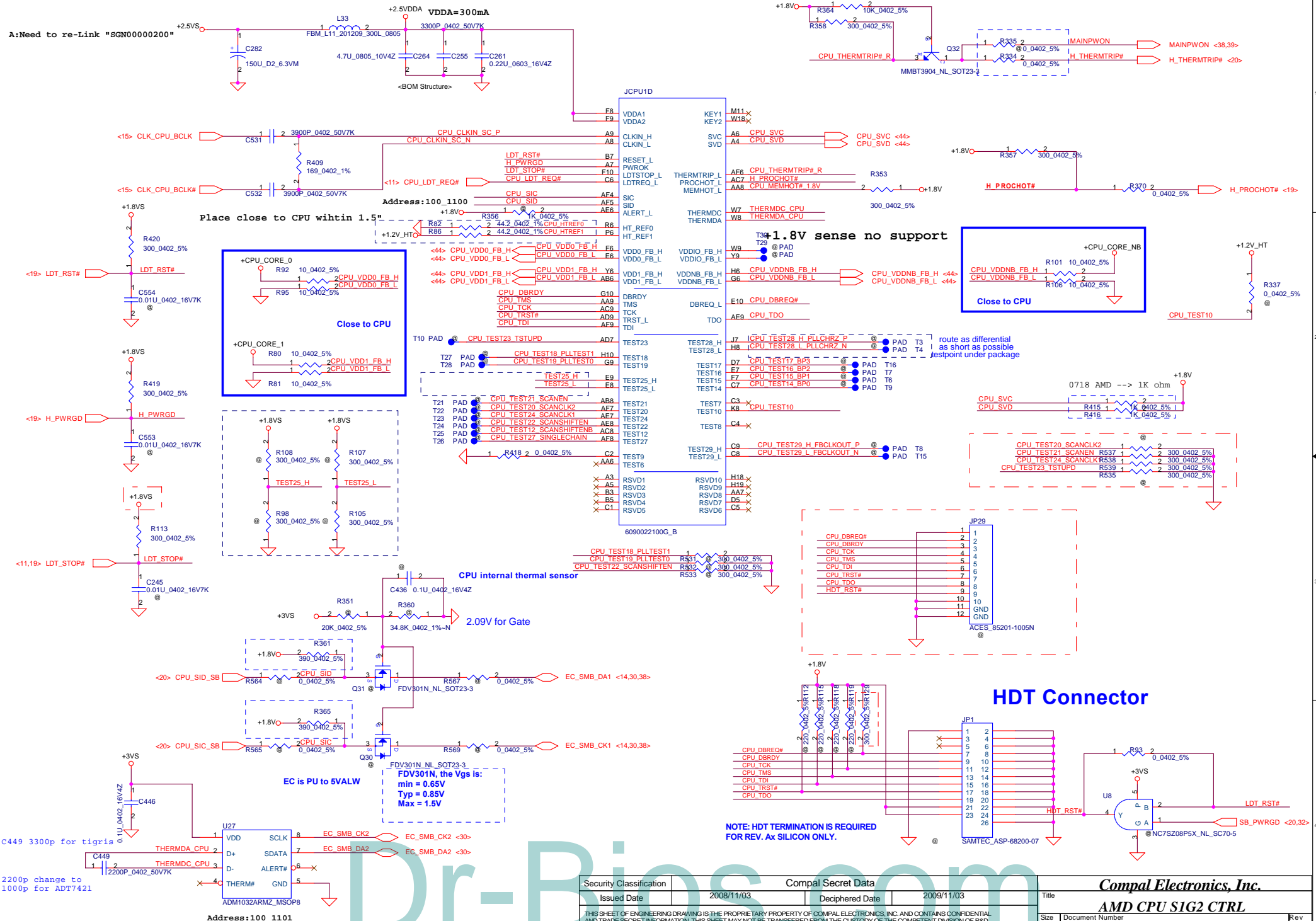


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# Processor DDR2 Memory Interface

PLACE CLOSE TO PROCESSOR  
WITHIN 1.5 INCH





A:Need to re-Link "SGN0000200"

Place close to CPU within 1.5"

CPU internal thermal sensor

HDT Connector

NOTE: HDT TERMINATION IS REQUIRED FOR REV. Ax SILICON ONLY.

C449 3300p for tigris  
2200p change to 1000p for ADT7421

Address:100\_1101

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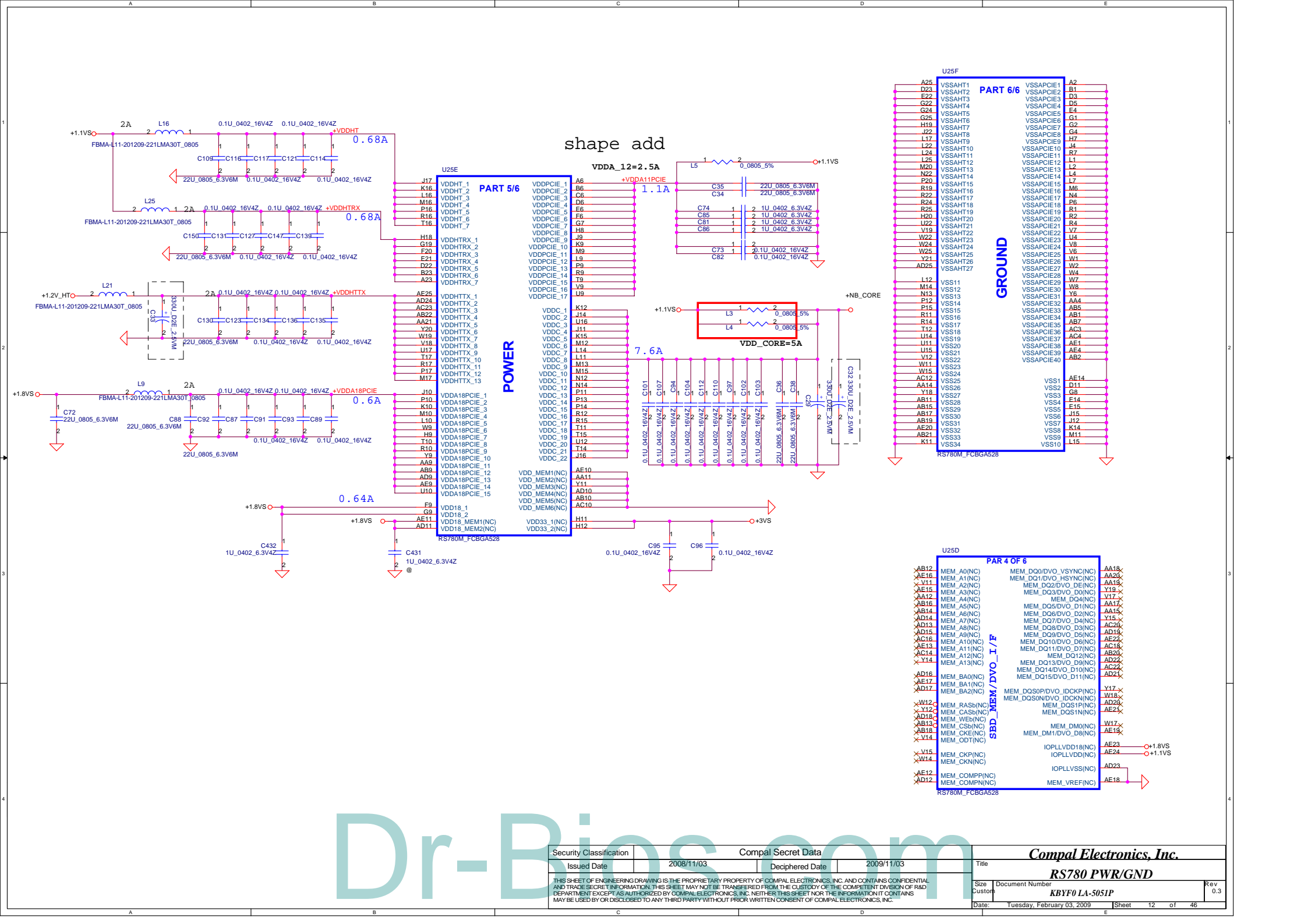










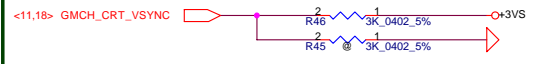


shape add

POWER

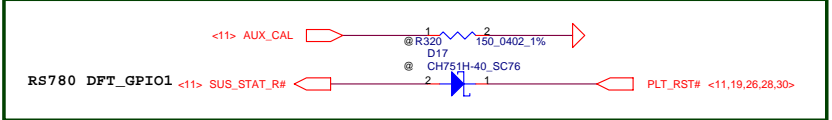
GROUND

Security Classification	Confidential		Title	Compal Electronics, Inc.	
Issued Date	2008/11/03	Deciphered Date	2009/11/03	RS780 PWR/GND	
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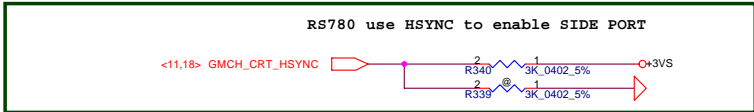
**DFT\_GPIO5:STRAP\_DEBUG\_BUS\_GPIO\_ENABLEb**

Enables the Test Debug Bus using GPIO. (VSYNC)  
 1 : Disable (RS780)  
 0 : Enable (RS780)



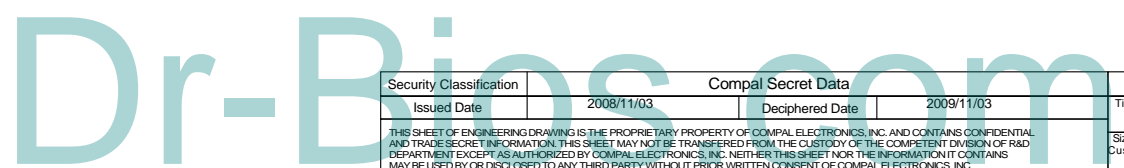
**DFT\_GPIO1:LOAD\_EEPROM\_STRAPS**

Selects Loading of STRAPS from EPROM  
 1 : Bypass the loading of EEPROM straps and use Hardware Default Values  
 0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected  
 RS740/RX780: DFT\_GPIO1 RS780:SUS\_STAT



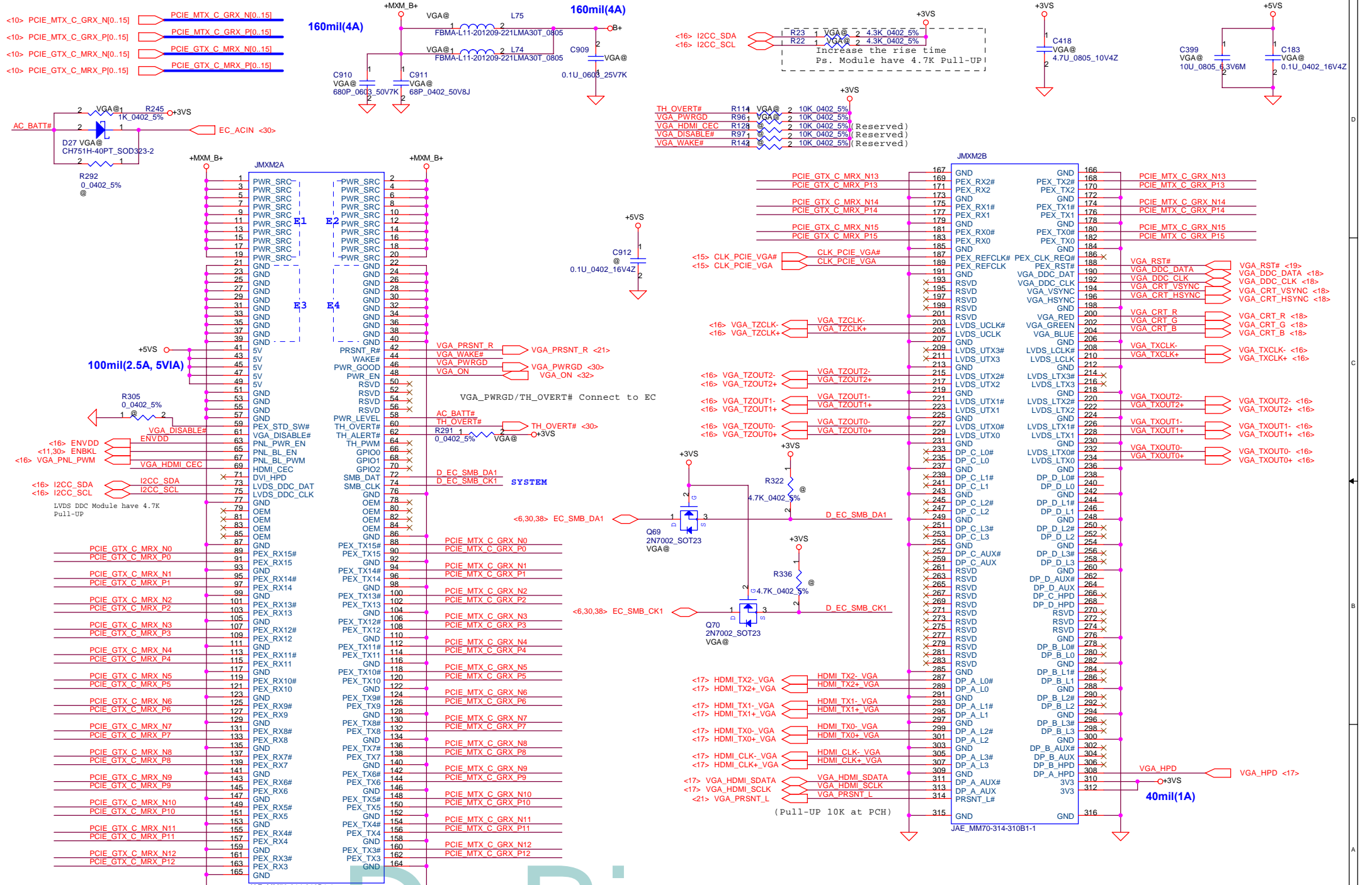
**RS780 use HSYNC to enable SIDE PORT**

RS740/RS780: Enables Side port memory ( RS780 use HSYNC#)  
 0 : Enable (RS780)  
 1 : Disable(RS780)

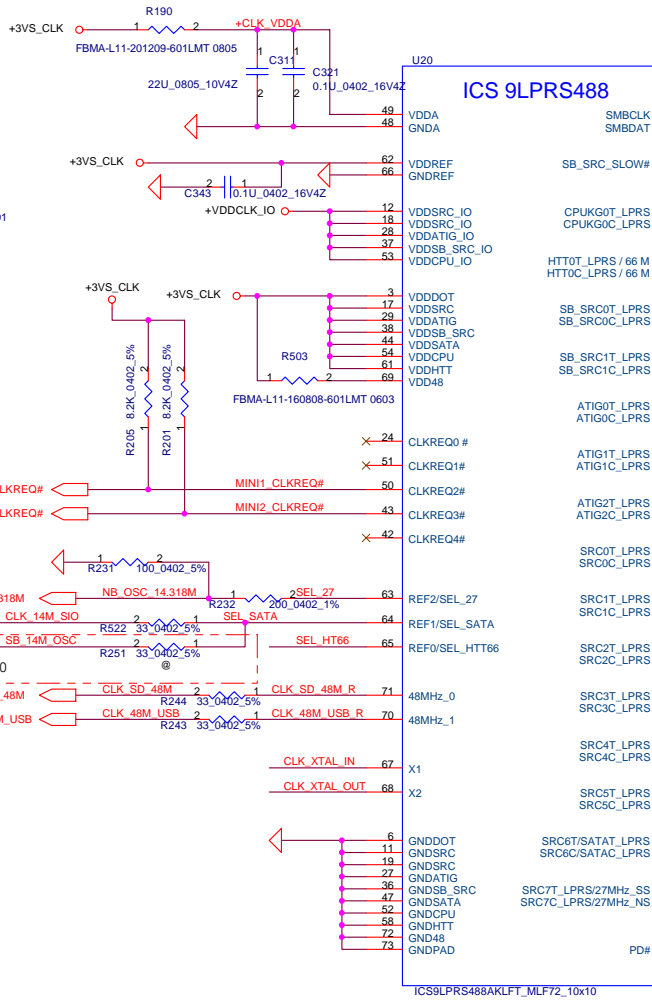
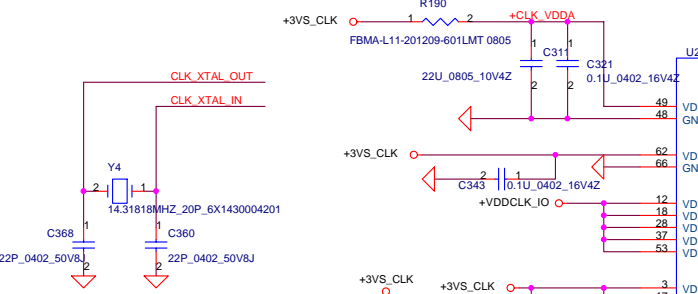
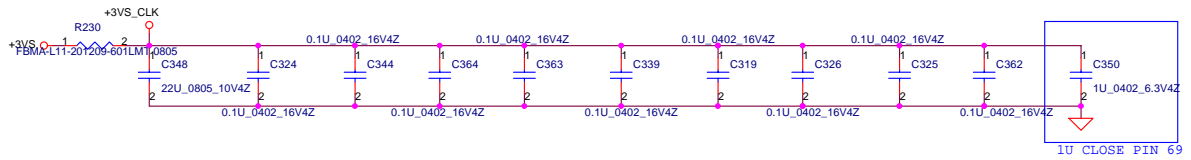
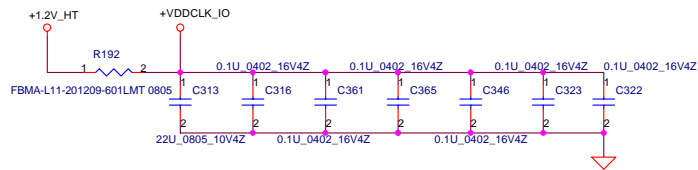


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REQ0# FOR SRC1  
REQ2# FOR SRC2  
REQ3# FOR SRC3

SRC 0	LAN
SRC 1	NEWCARD
SRC 2	MINI2
SRC 3	MINI1

NB GFX

VGA chip(Dis)

GLAN

MiniCard\_1

MiniCard\_2

NB A LINK

SB RCLK

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(N/OUT)
GPP_REFCLK	NC	100M DIFF	NC
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

SEL_HTT66	1	configure as single-ended 66MHz output
	0*	configure as differential 100MHz output
SEL_SATA	1*	100M SATA SRC6 output
	0	SPREAD 100M SATA SRC6 output

NB_OSC_14.318M	1	configure as 27M and 27M_SS output
	0*	configure as SRC 7 output

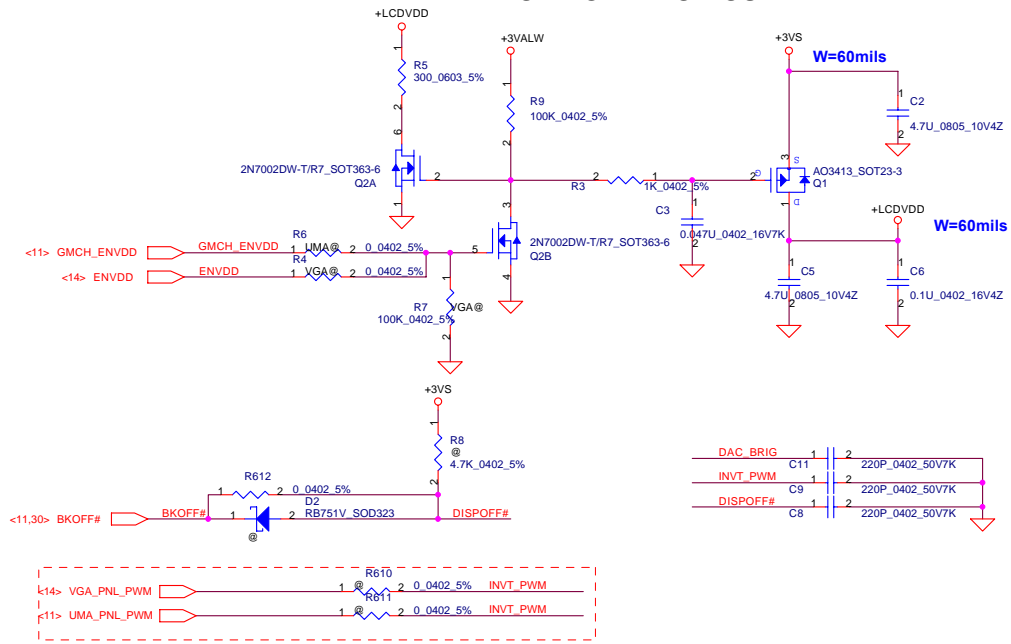
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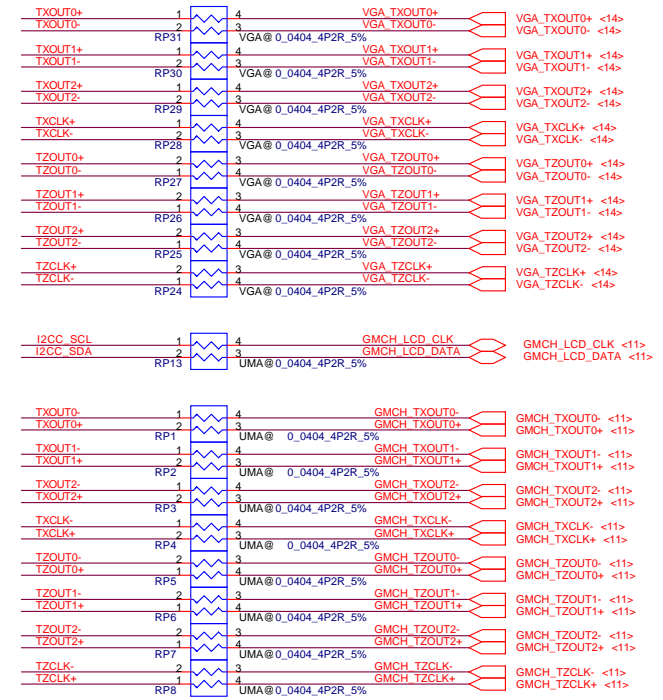
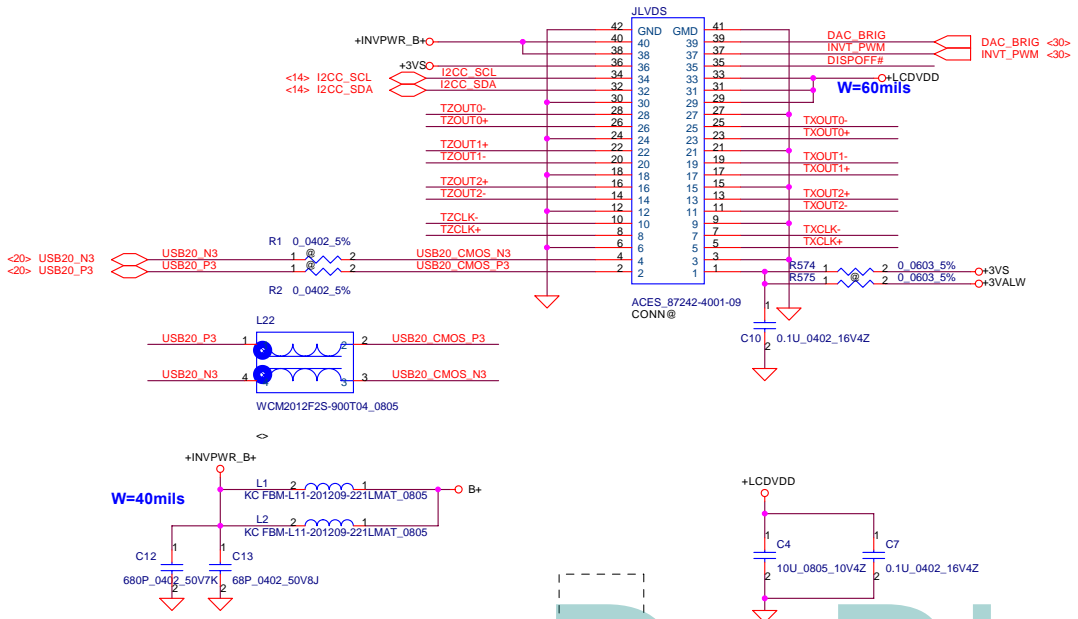
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Size	Document Number	Rev	
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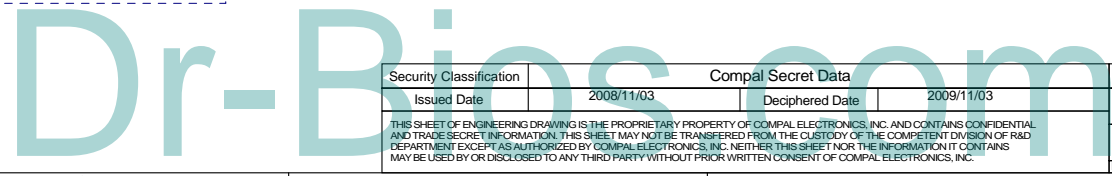
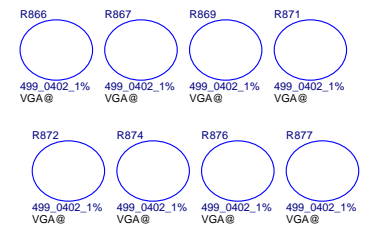
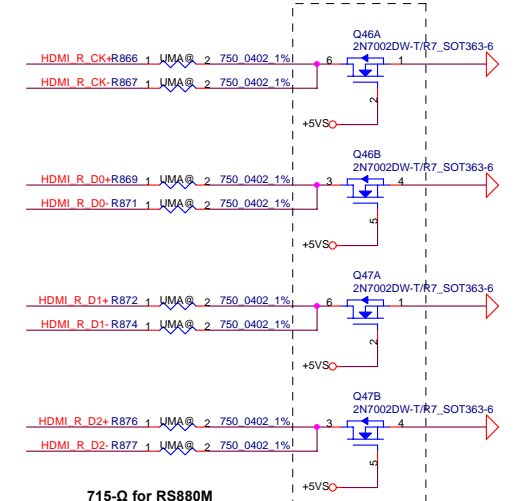
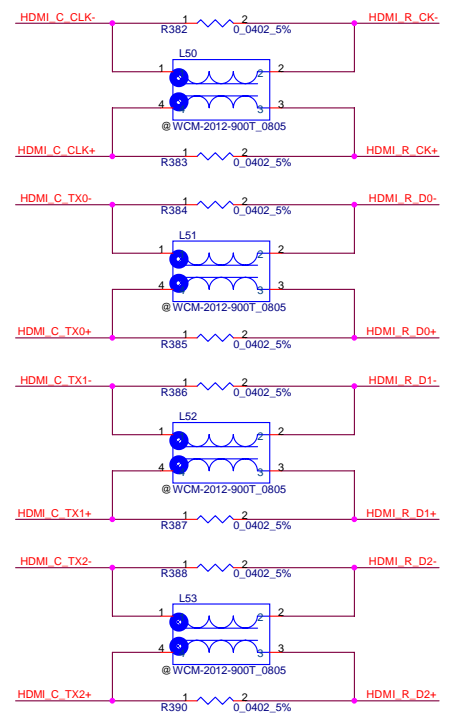
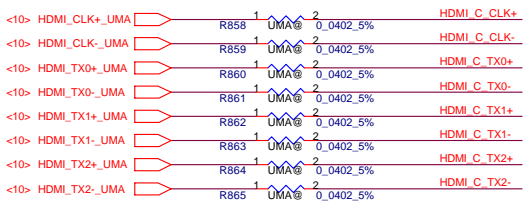
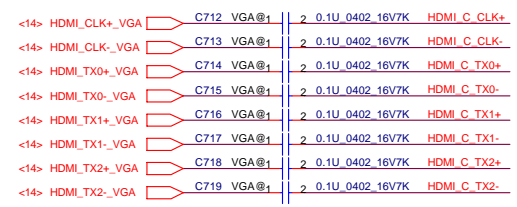
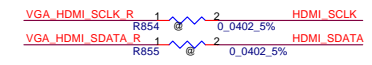
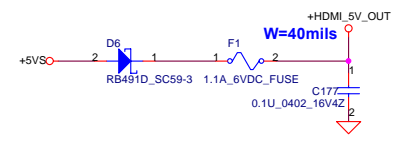
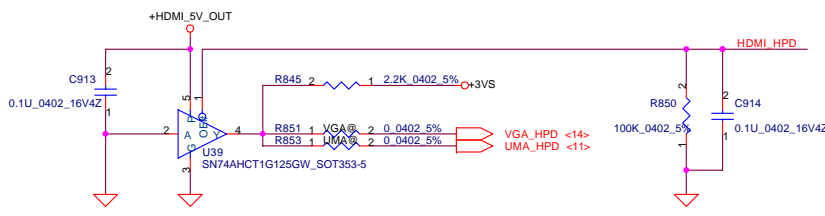
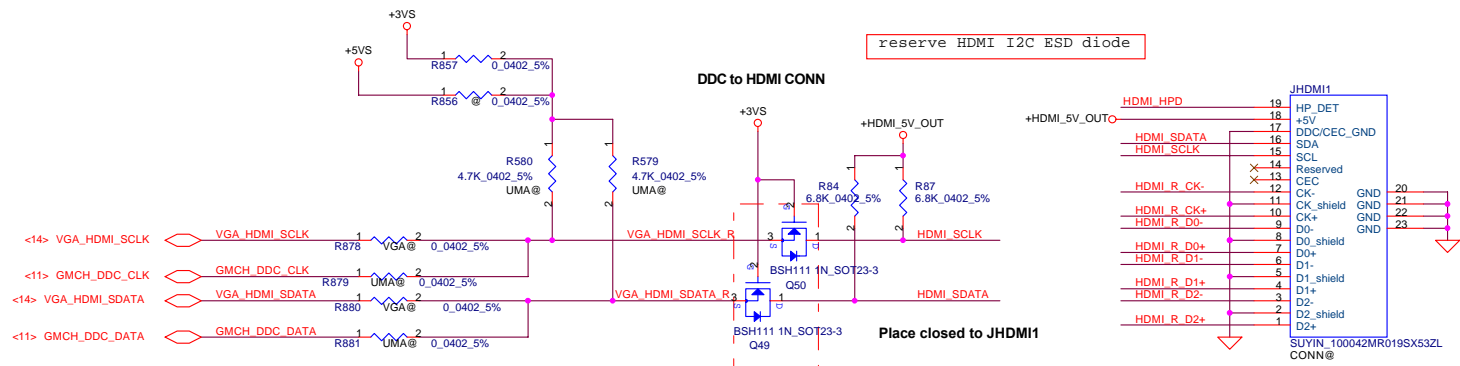
### LCD POWER CIRCUIT



### LCD/PANEL BD. Conn.

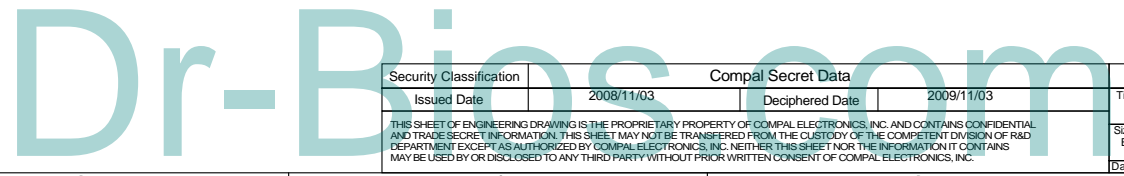
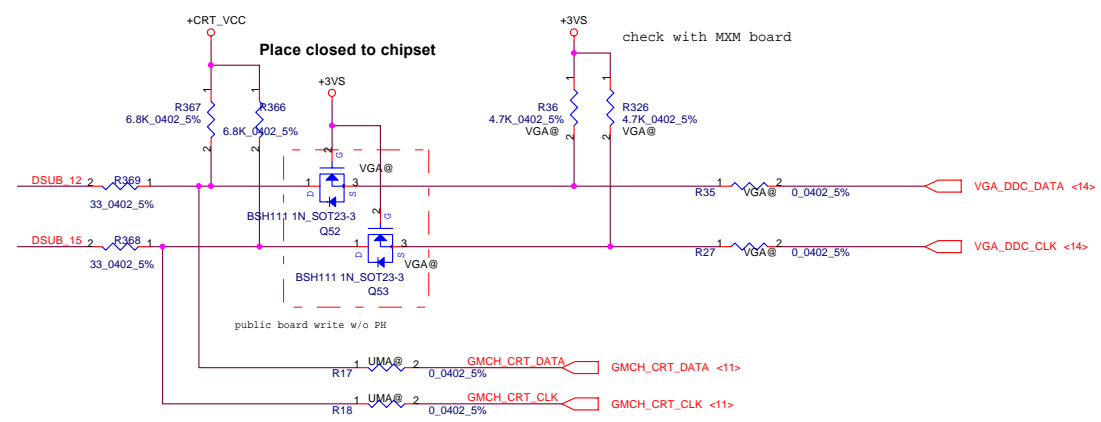
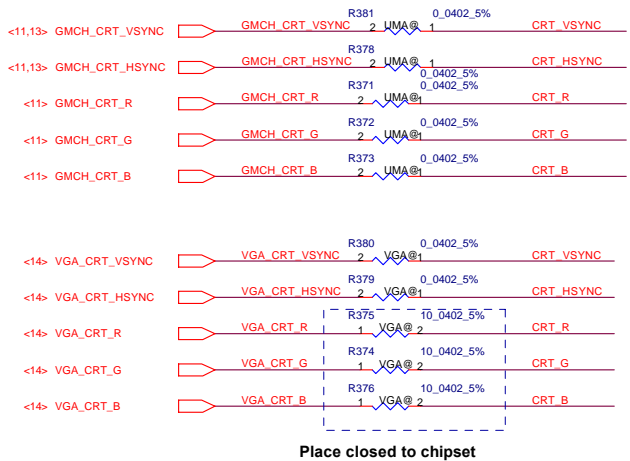
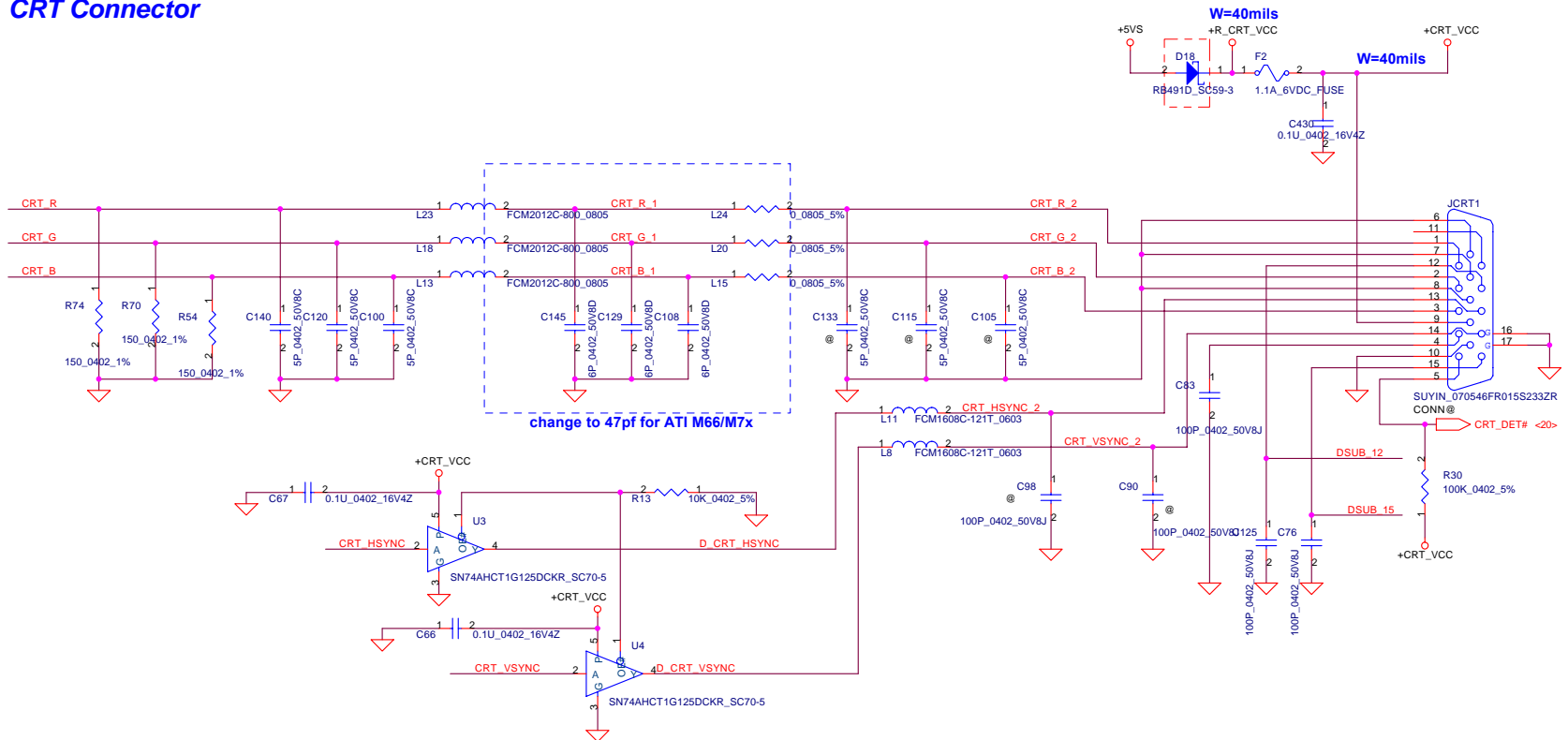


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Deciphered Date	2009/11/03	LVDS & DVI Connector	
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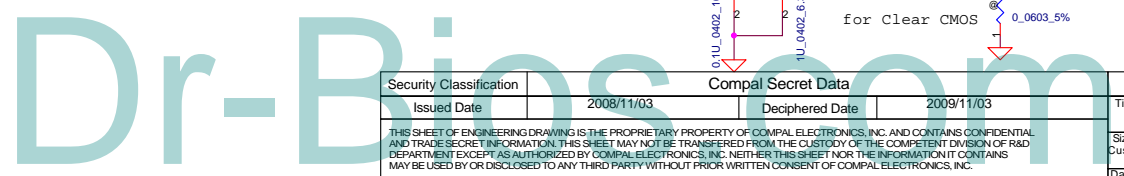
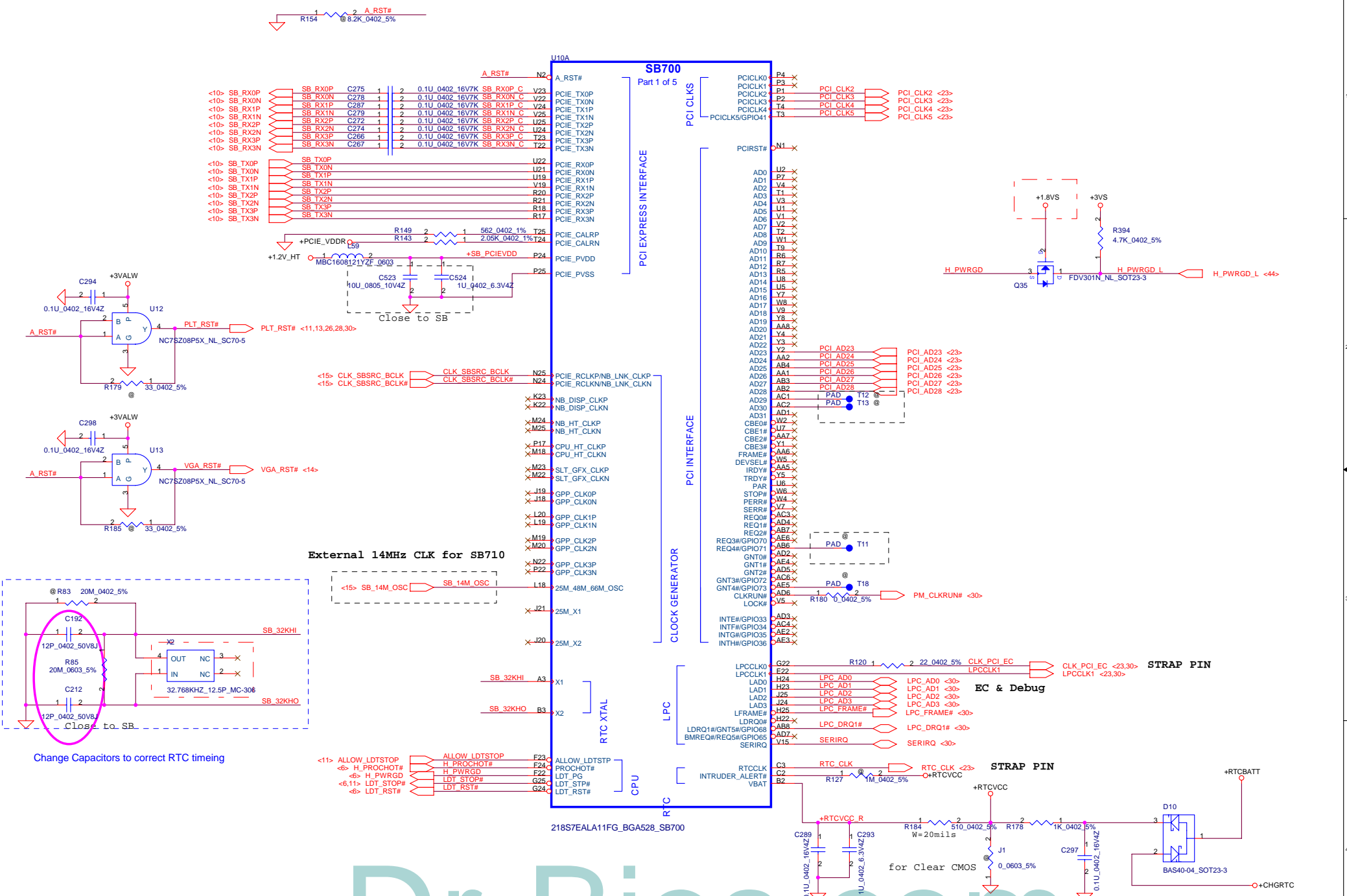


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Customer	KBYFO LA-5051P			Rev	0.3
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# CRT Connector



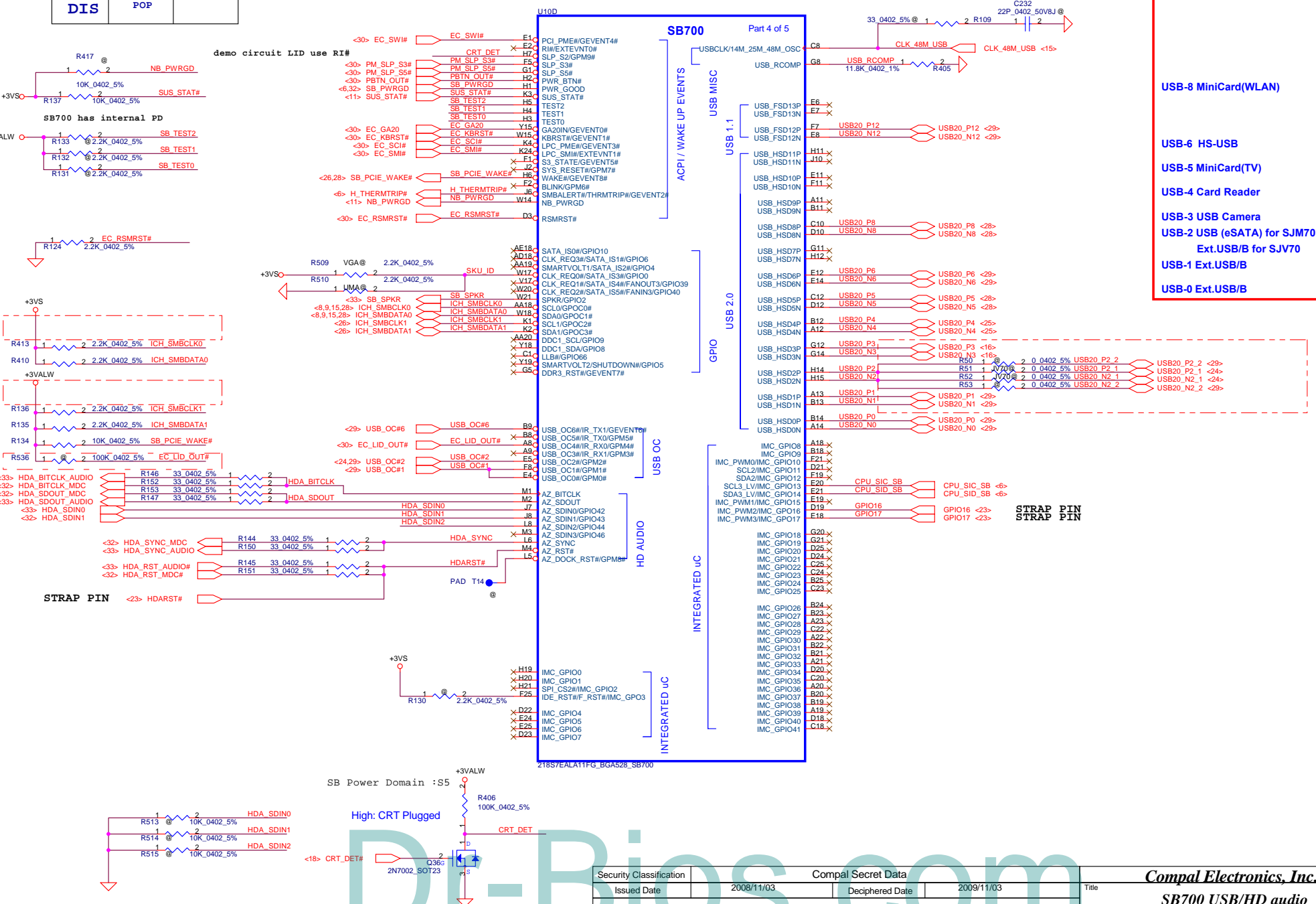
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Issued Date	2008/11/03	Deciphered Date	2009/11/03	Document Number
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				<b>KB7F0 LA-5051P</b>
				Rev
				0.3
		Date:	Tuesday, February 03, 2009	Sheet
				19 of 46

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SKU-ID	R509	R510
UMA		POP
DIS	POP	



- USB-12 Bluetooth
- USB-8 MiniCard(WLAN)
- USB-6 HS-USB
- USB-5 MiniCard(TV)
- USB-4 Card Reader
- USB-3 USB Camera
- USB-2 USB (eSATA) for SJW70  
Ext.USB/B for SJV70
- USB-1 Ext.USB/B
- USB-0 Ext.USB/B

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Title			Compal Electronics, Inc.		
Size			7000 USB/HD audio		
Document Number			KB70 LA-501P		
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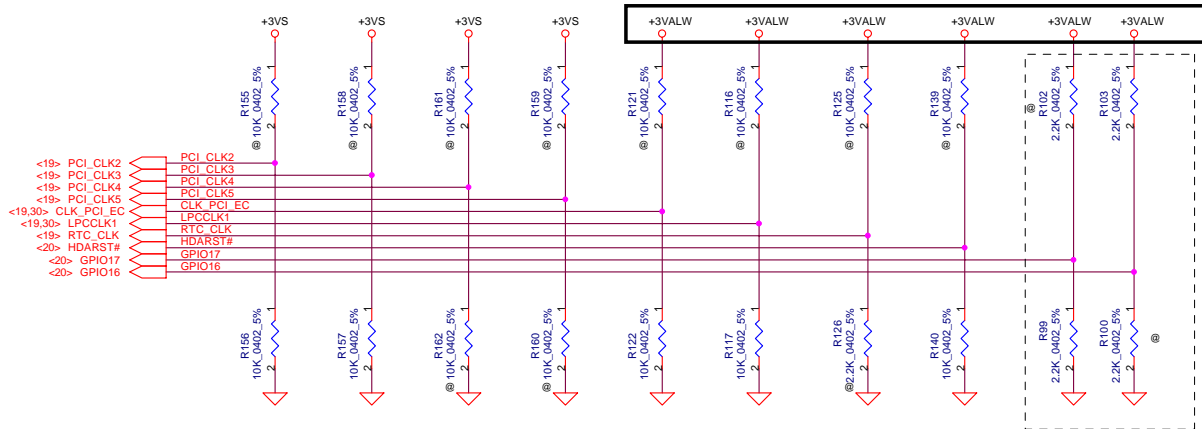




# REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC\_CLK

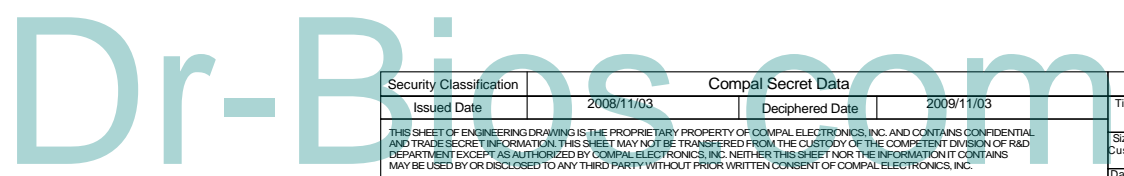
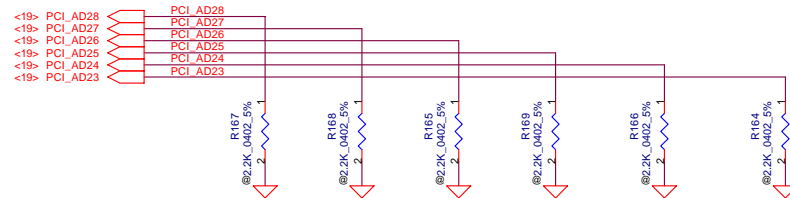
	PCI_CLK2 CLK_FCI_PCM	PCI_CLK3 CLK_FCI_DBG	PCI_CLK4	PCI_CLK5	LPC_CLK0 CLK_FCI_BC	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17	GP16
<b>PULL HIGH</b>	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	<b>INTERNAL RTC</b>  DEFAULT	EC ENABLED	Internal pull up H,H = Reserved HL = SPI ROM	
<b>PULL LOW</b>	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT		L,H = LPC ROM (Default L,NC) LL = FWH ROM



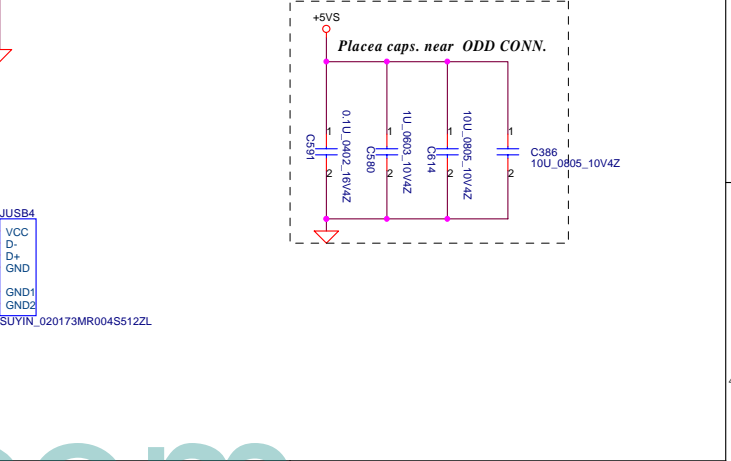
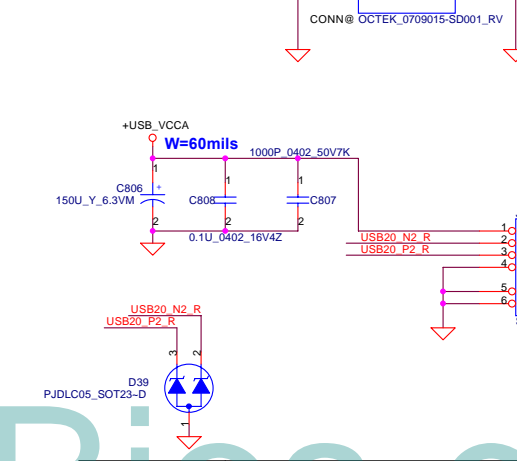
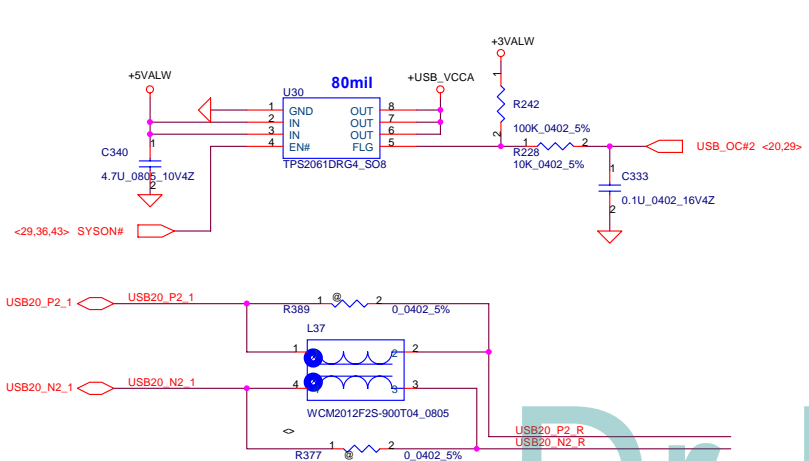
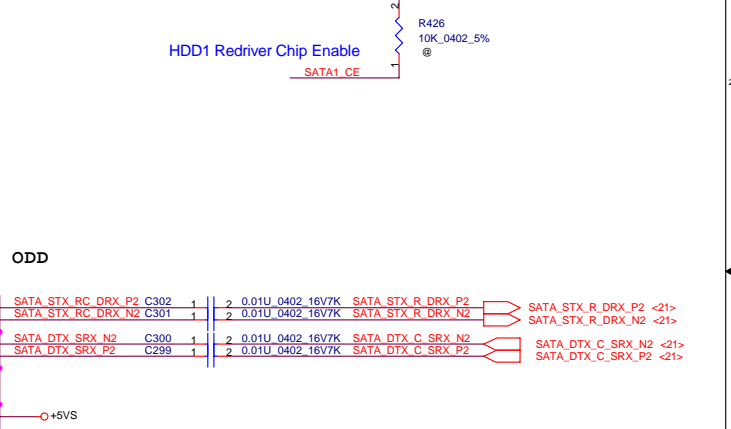
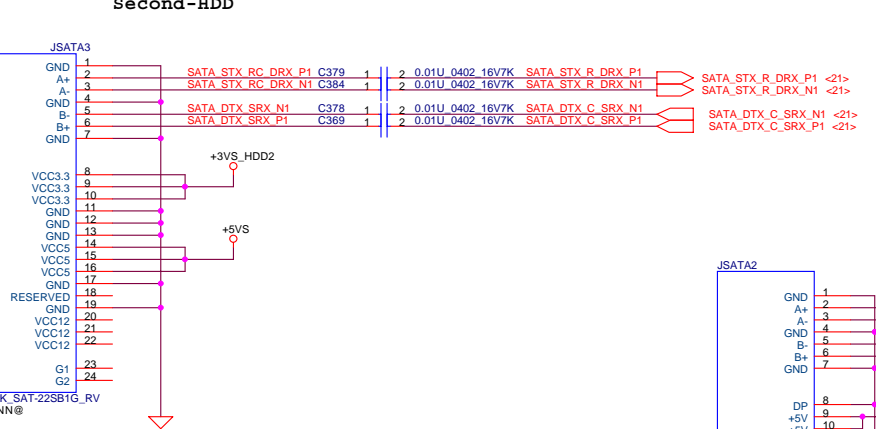
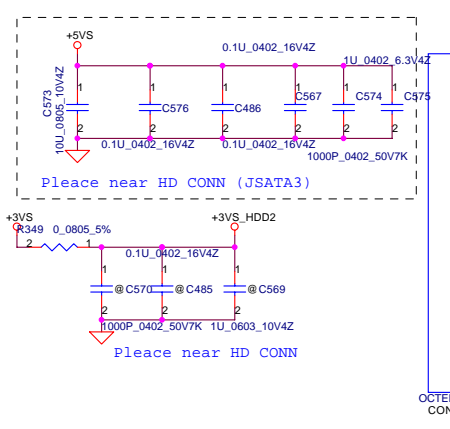
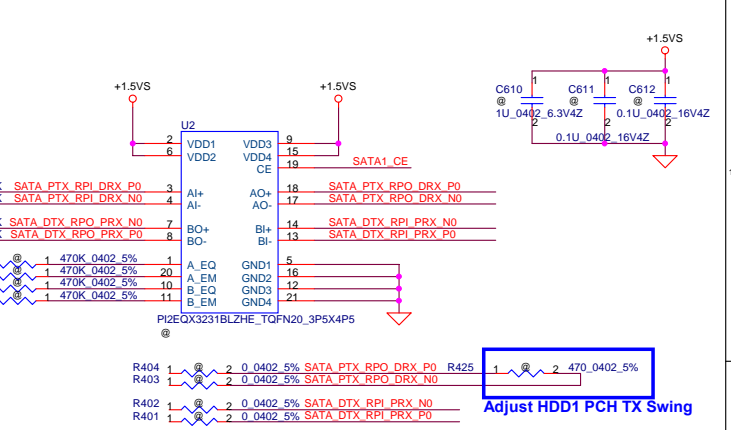
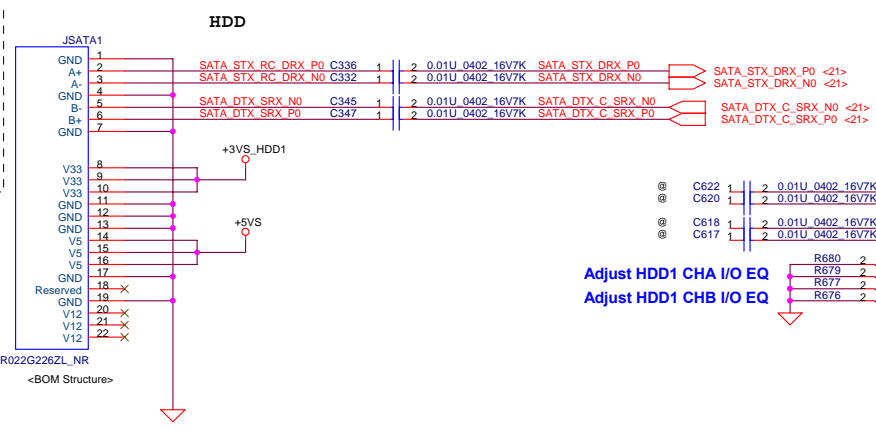
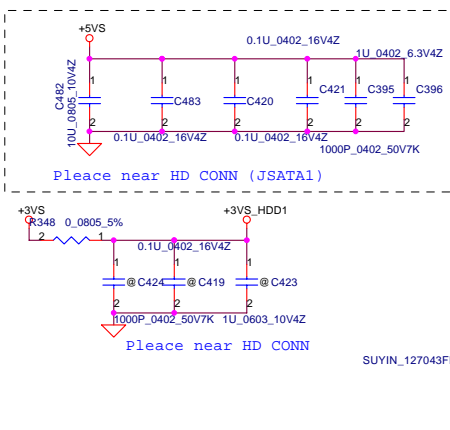
# DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI\_AD[28:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
<b>PULL HIGH</b>	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
<b>PULL LOW</b>	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

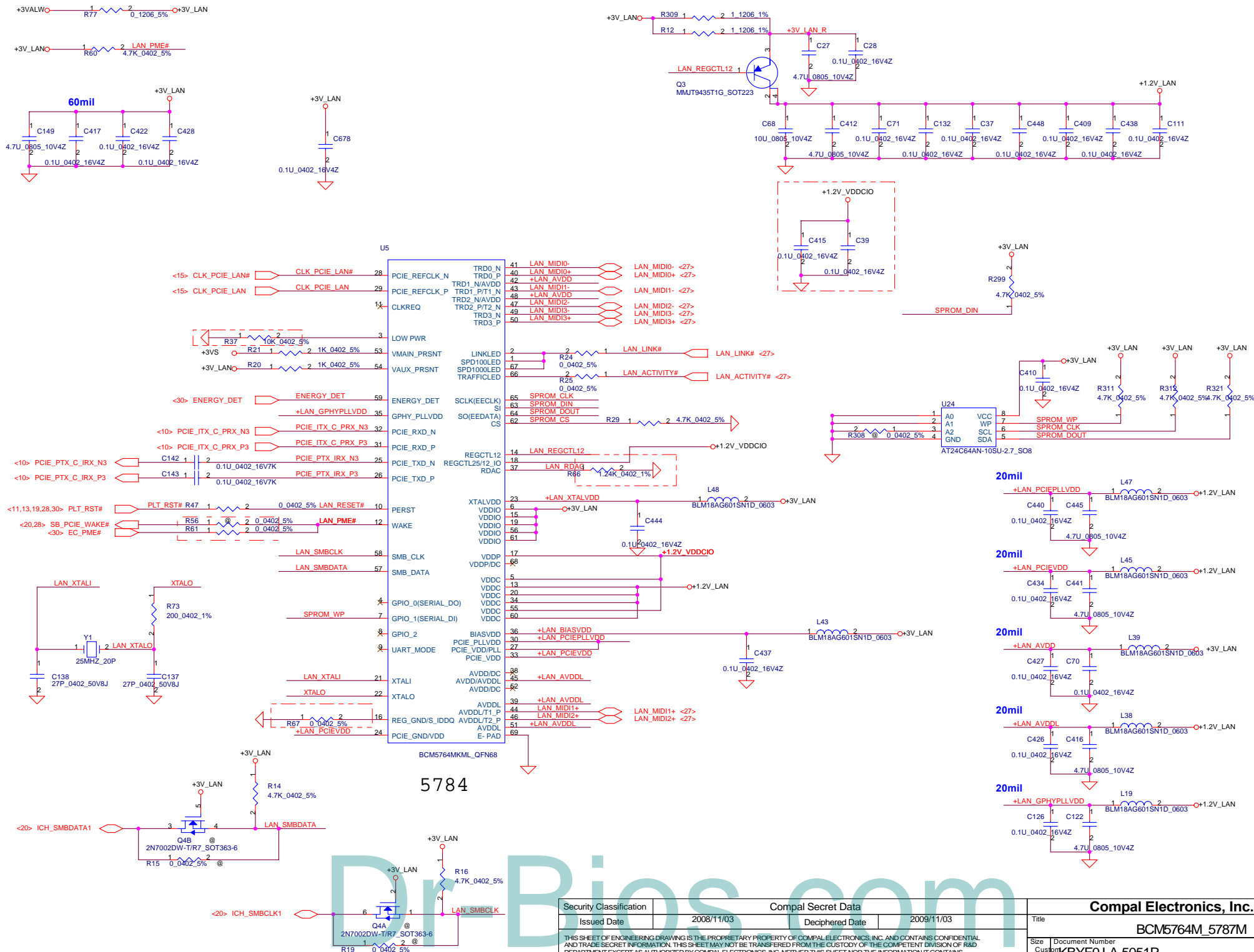


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Issued Date	2008/11/03	Deciphered Date	2009/11/03	SB700 STRAPS	
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Size B	Document Number	KBYF0 LA-5051P		Rev 0.3
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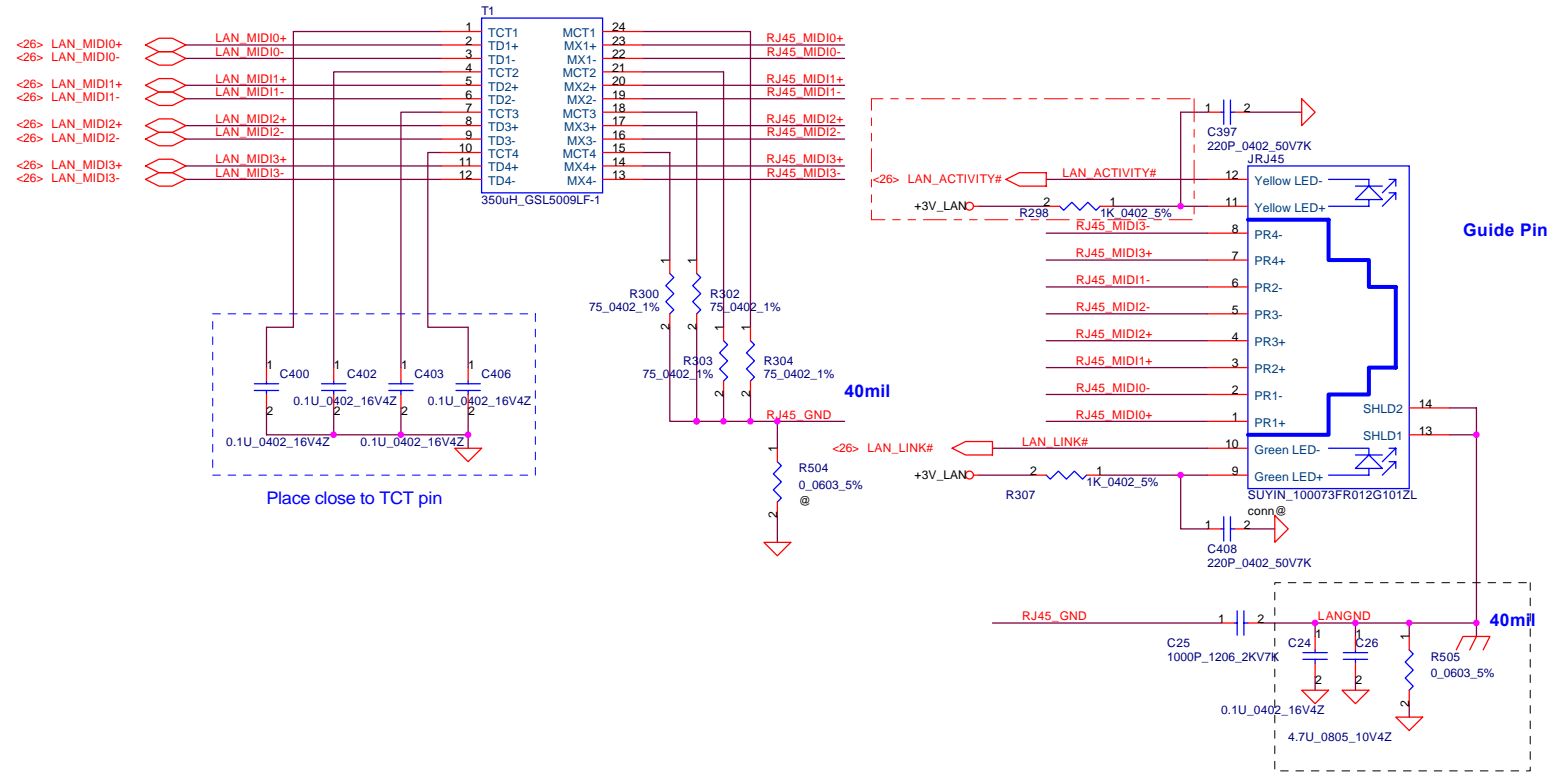




5784

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Compal Electronics, Inc.		
Title		
BCM5764M_5787M		
Size	Document Number	Rev
Custom	KUBYFO LA-5051P	0.3
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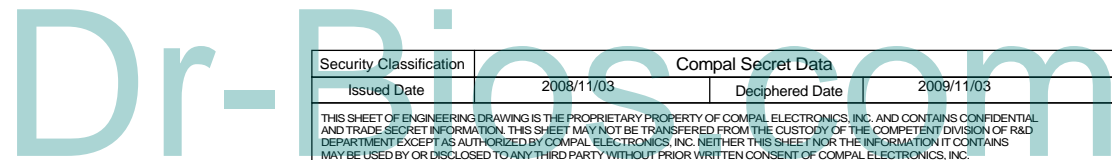


Place close to TCT pin

40mil

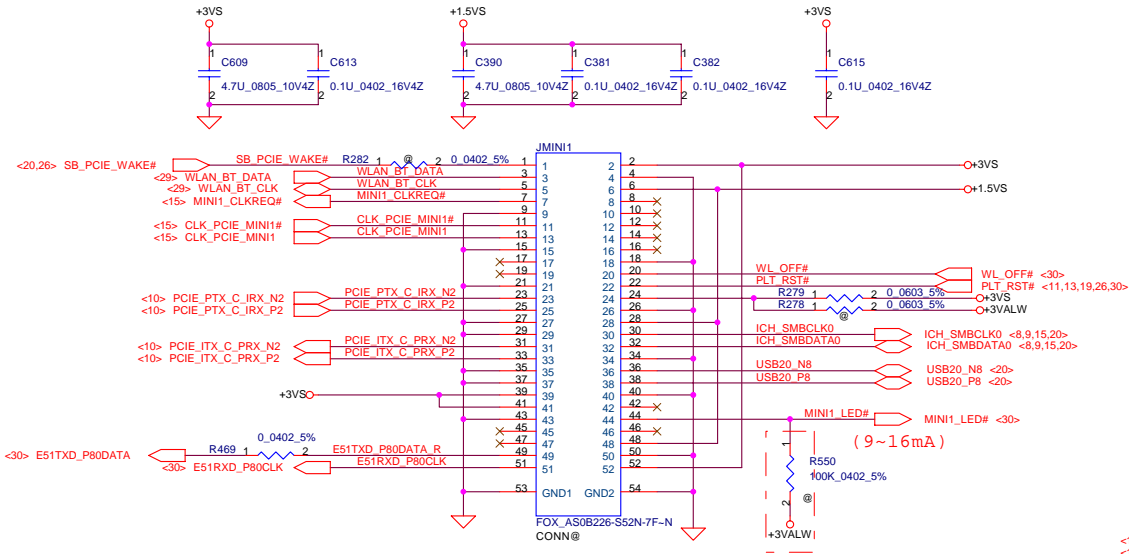
Guide Pin

For EMI



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Size	Document Number			Rev	
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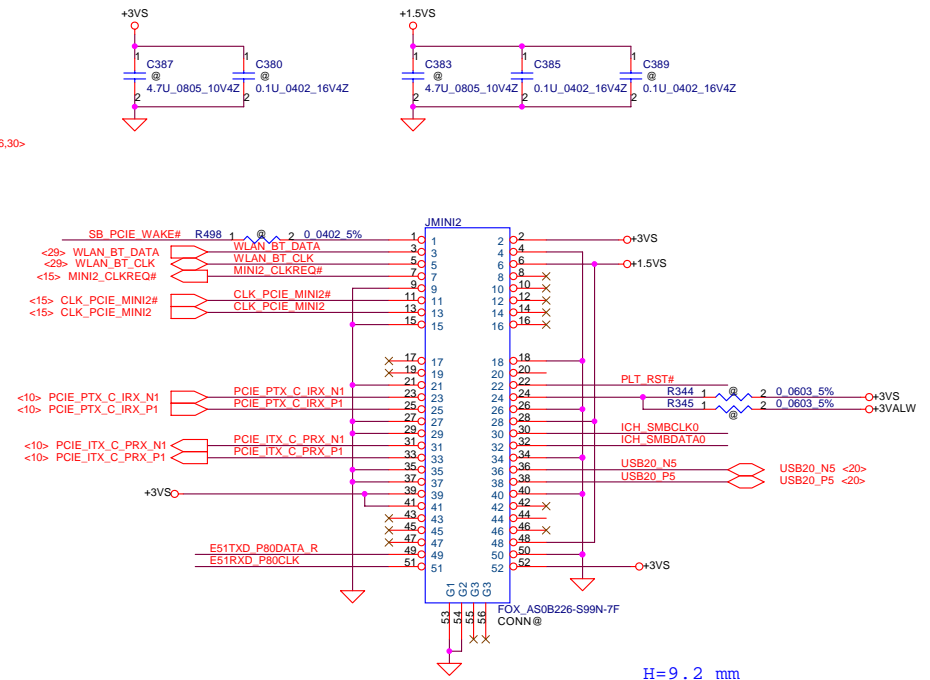
### For Wireless LAN



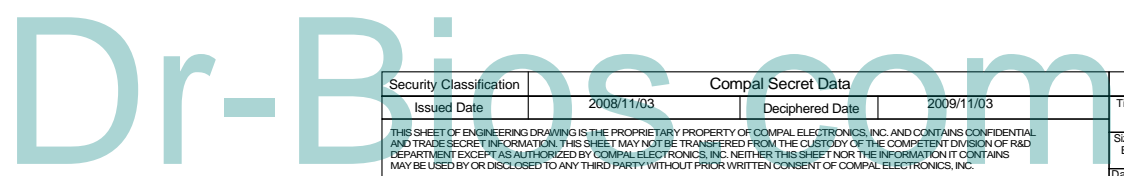
H=5.2 mm

Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

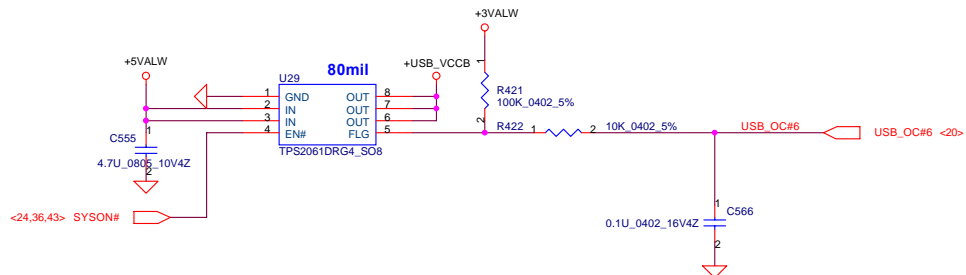
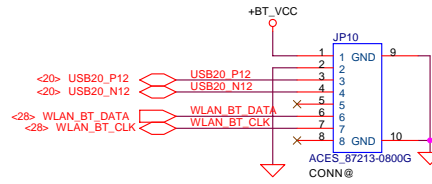
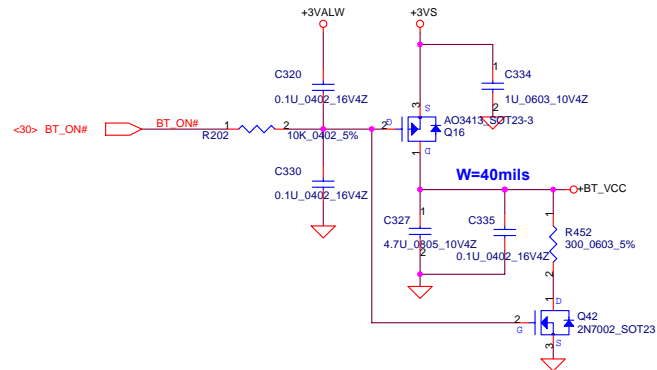
### For TV-Tuner/HW MPEG



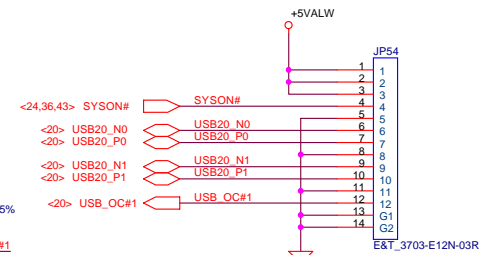
H=9.2 mm



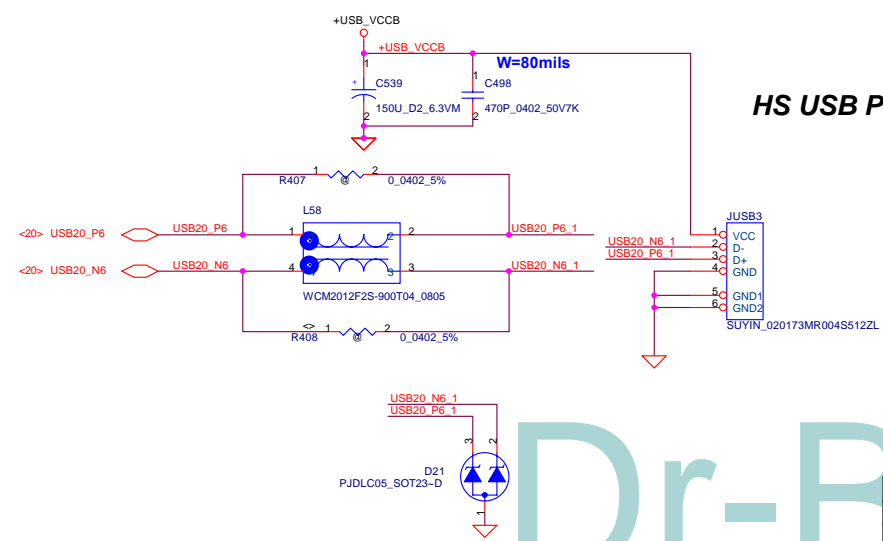
# Bluetooth Conn.



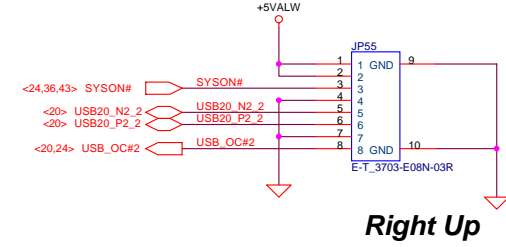
## 2 PORT



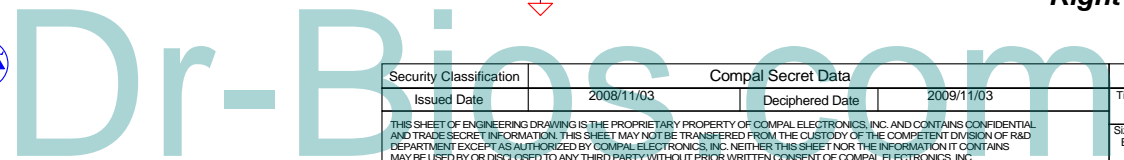
## HS USB PORT



## 1 PORT FOR JV70



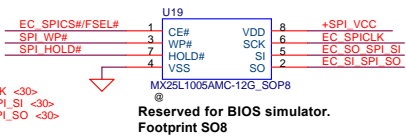
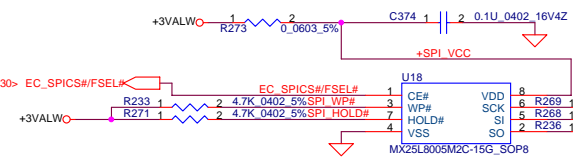
Right Up



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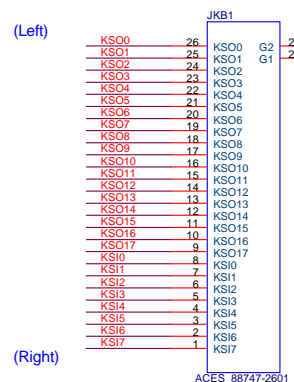
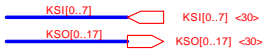




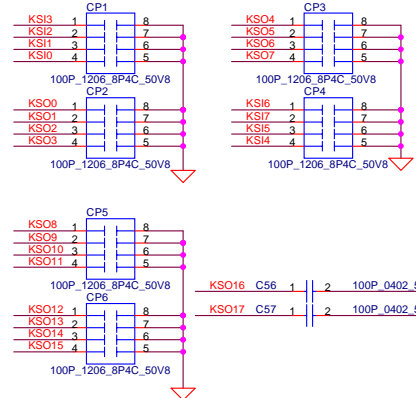


Reserved for BIOS simulator.  
Footprint S08

**INT\_KBD Conn.**

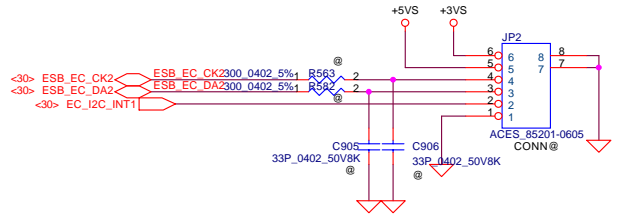


**For EMI**

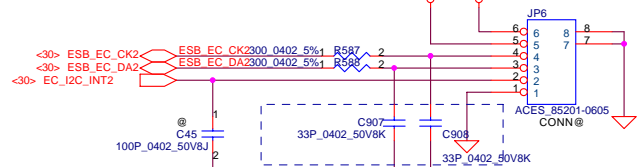


**To Media/B Conn.**

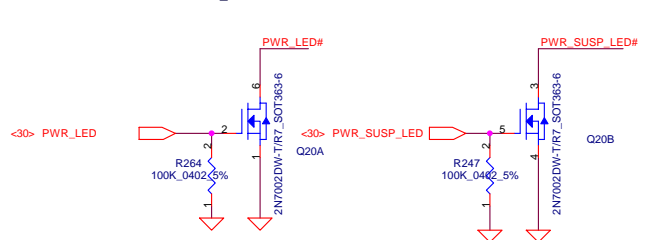
**CAP Sensor right JM70**



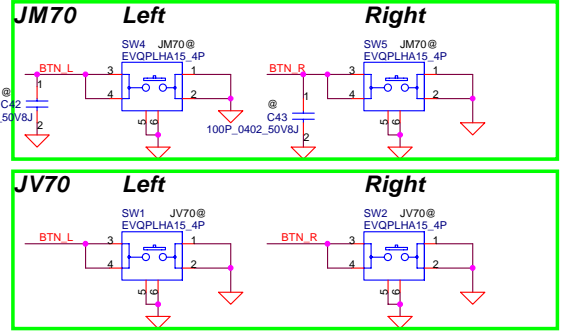
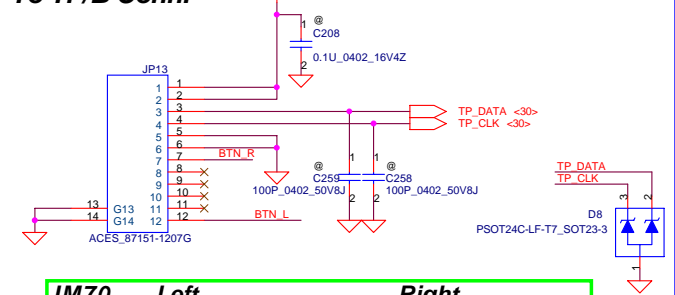
**CAP Sensor left for JM70**



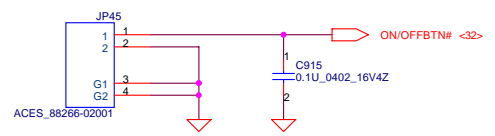
**CAP Sensor up for JV70**



**To TP/B Conn.**

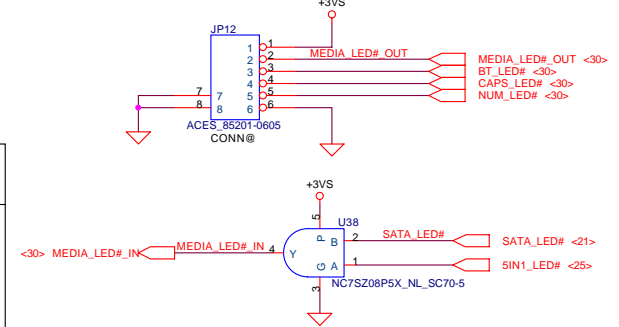


**TO POWER BTN/B for JV70**

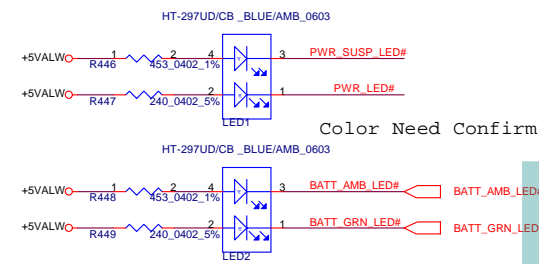


Need Check

**To LED/B Conn.**

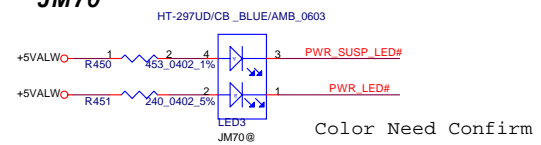


**JM70**



Color Need Confirm

**JM70**

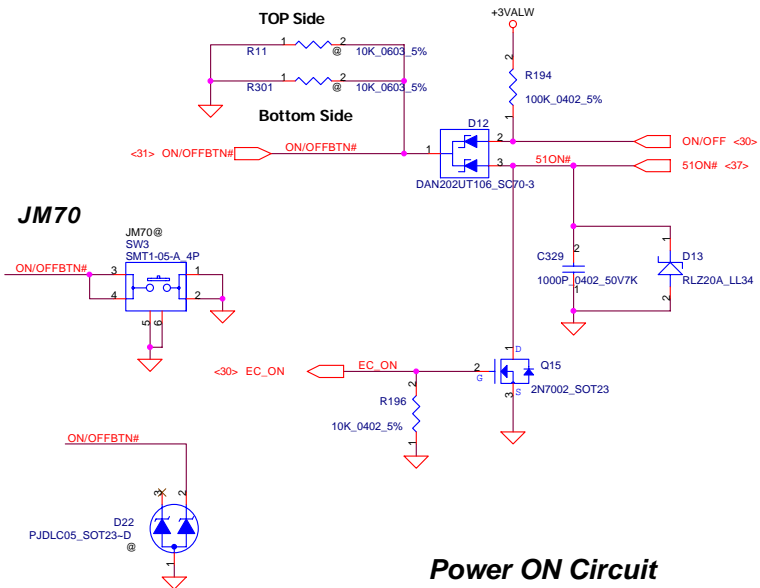


Color Need Confirm

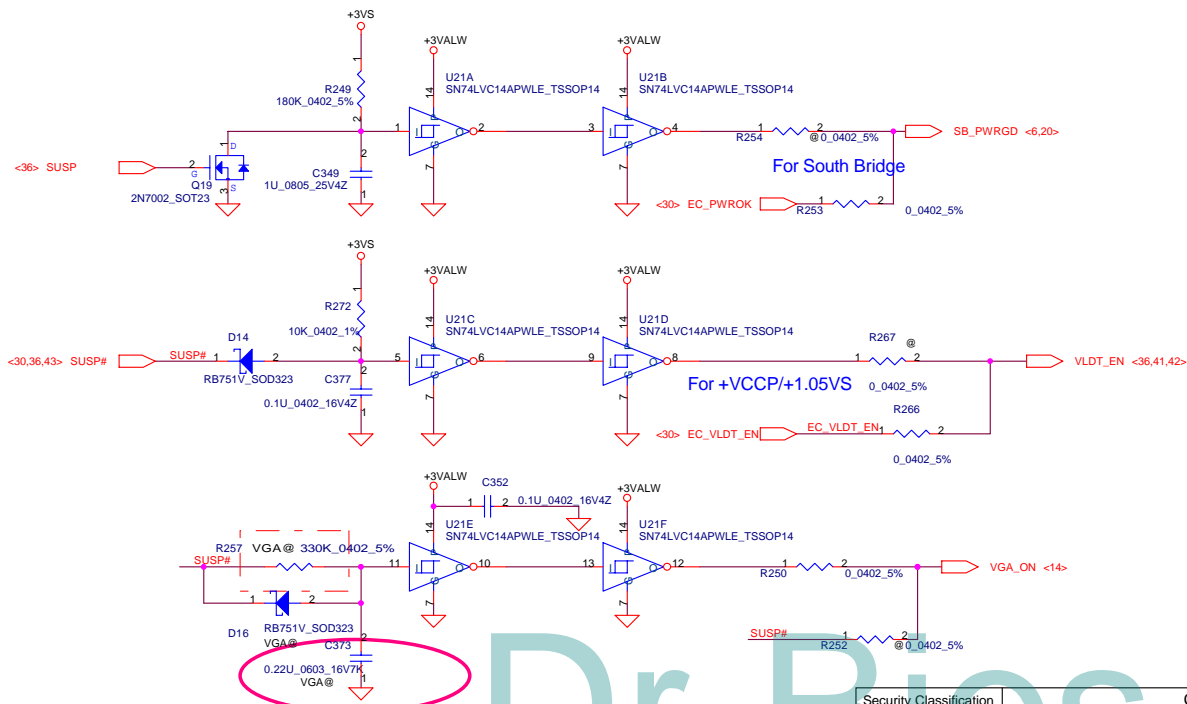
	JM70	JV70
1.	HDD	HDD
2.	BT_LED	BT_LED
3.	CAP_LED	NUM_LED
4.	NUM_LED	CAP_LED

### Power Button

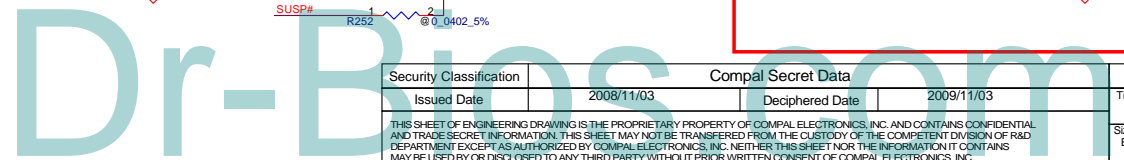
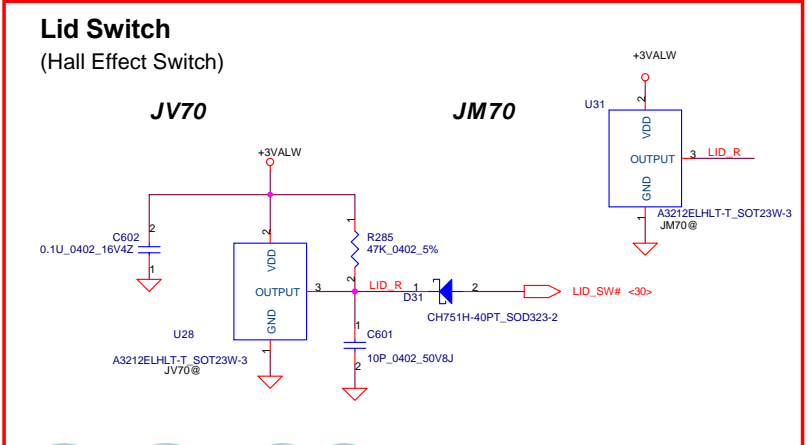
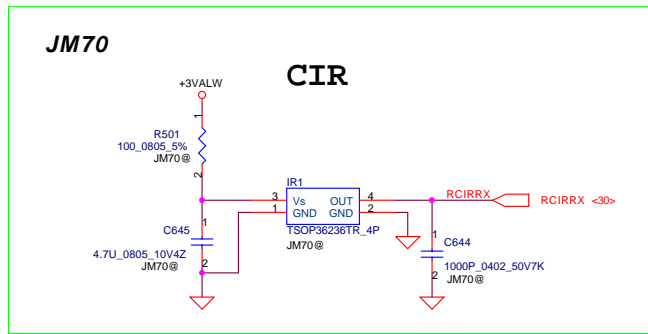
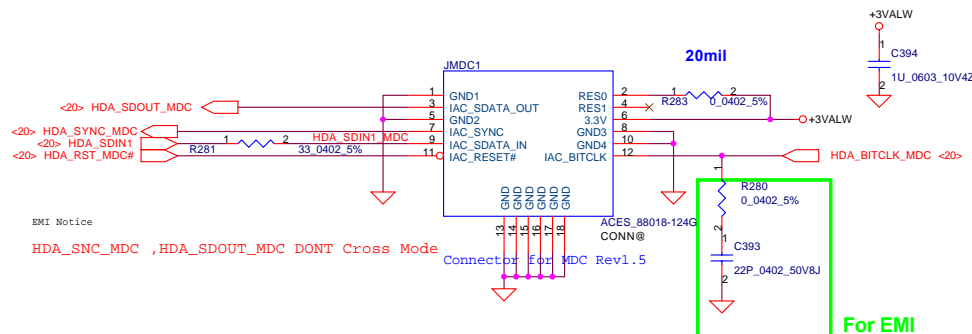
ON/OFF switch



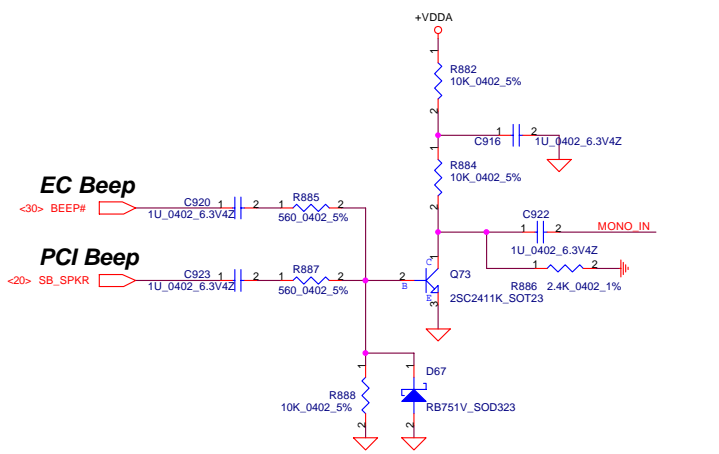
### Power ON Circuit



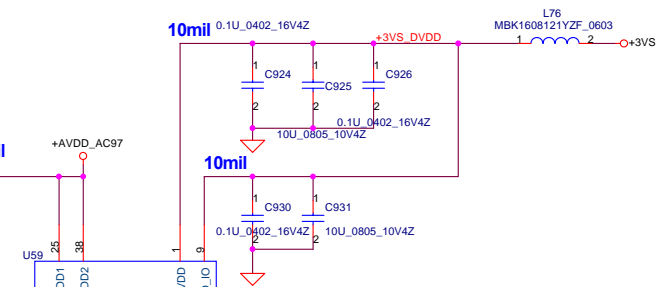
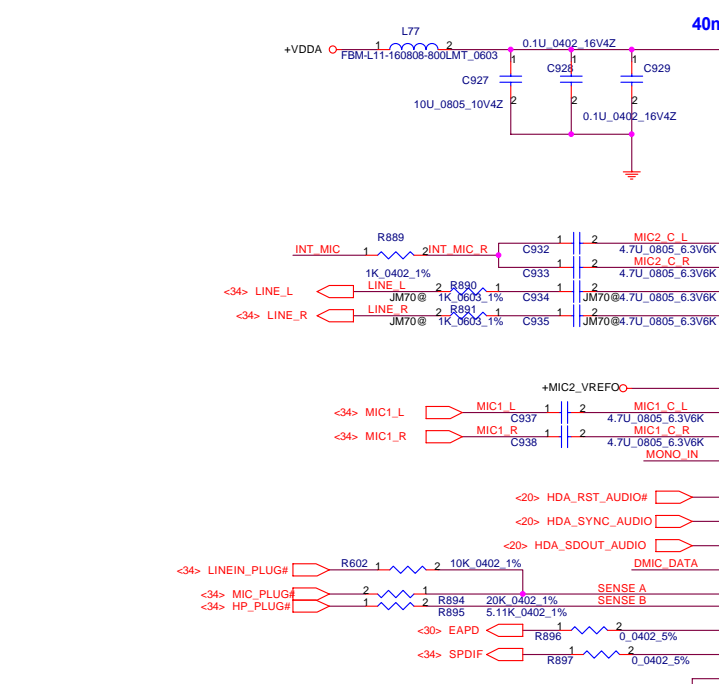
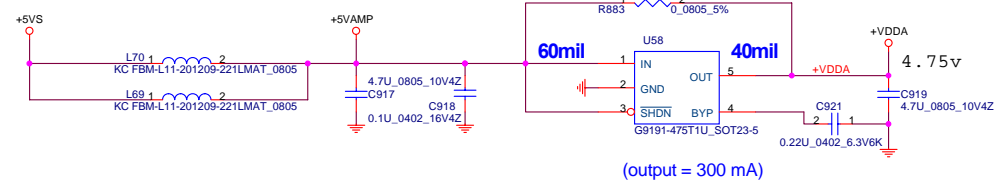
### HDA MDC Conn.



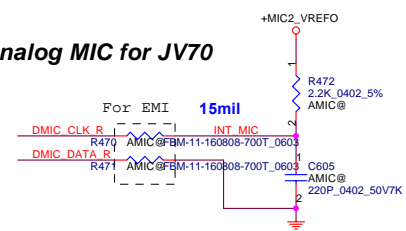
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Issued Date	2008/11/03	Deciphered Date	2009/11/03	Document Number
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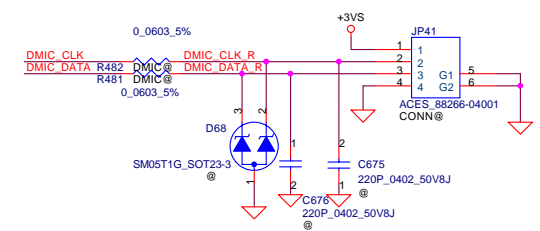
### HD Audio Codec



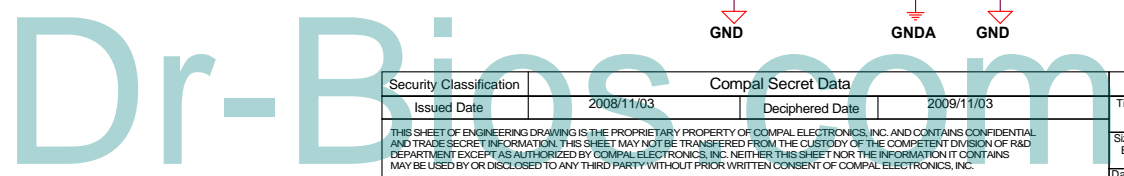
### Analog MIC for JV70



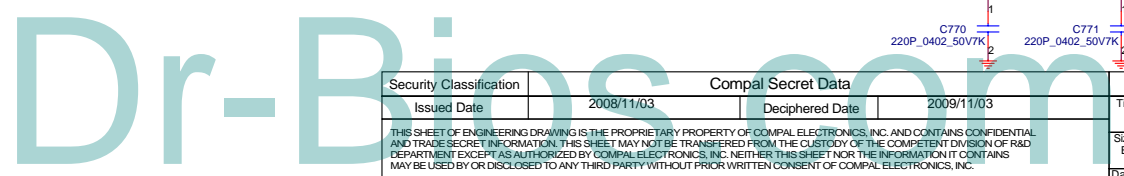
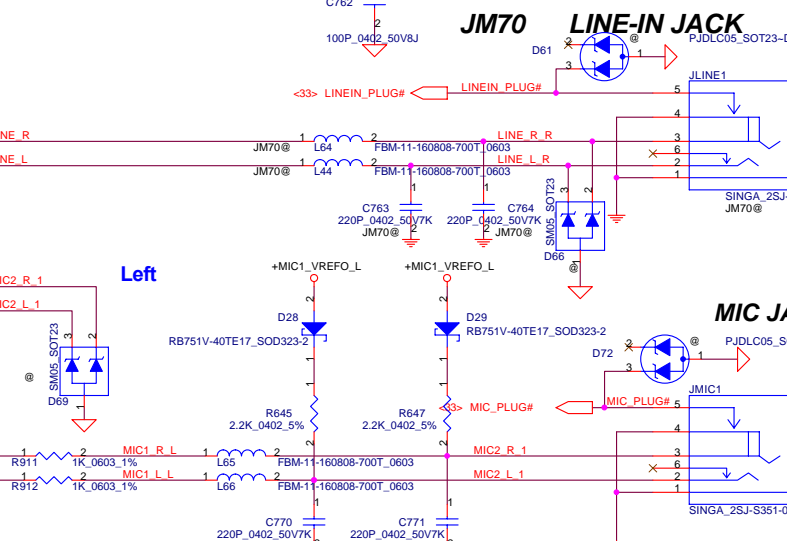
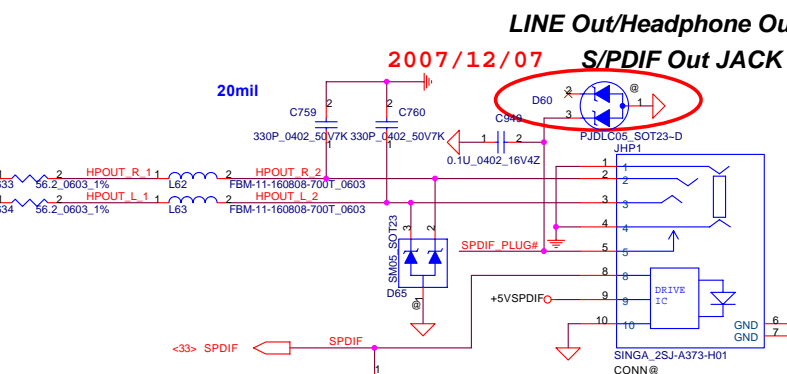
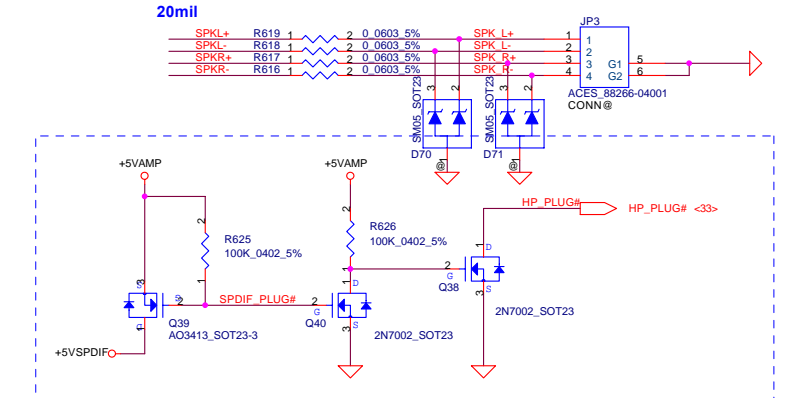
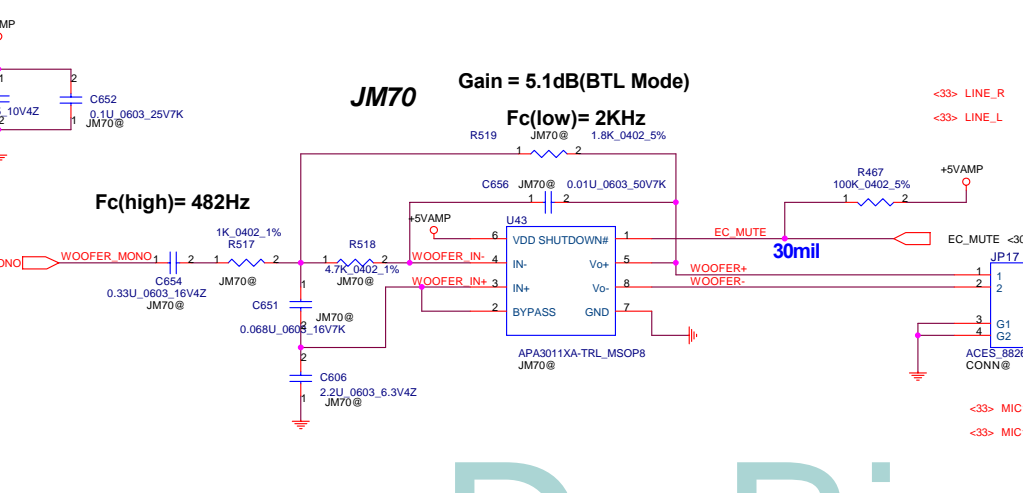
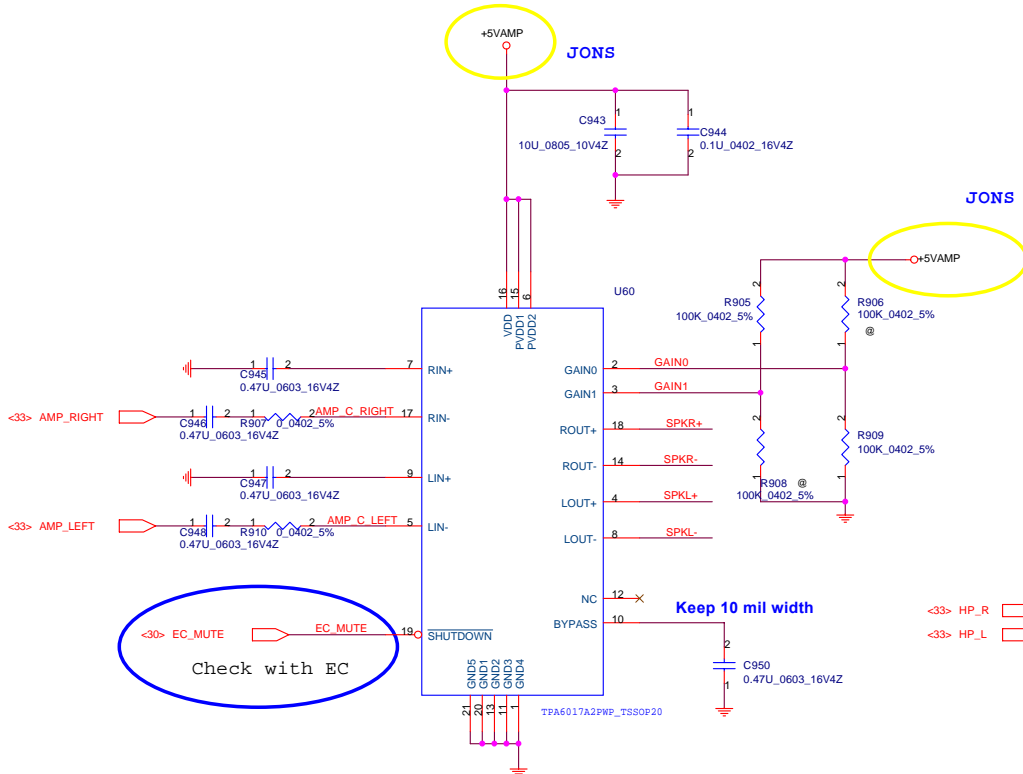
### Digital MIC for JM70 DMIC Conn.



Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

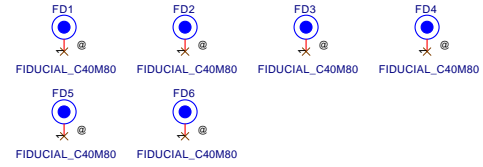
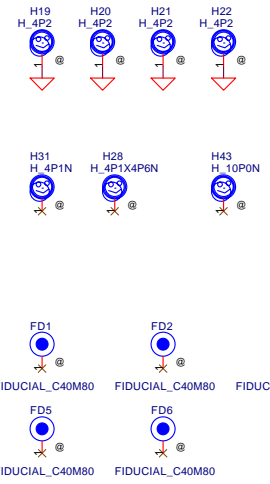
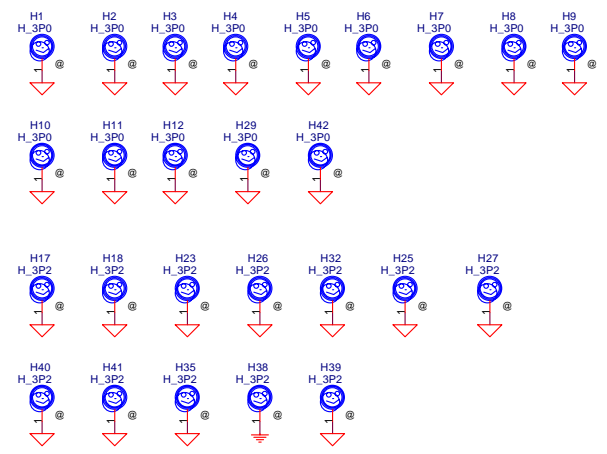
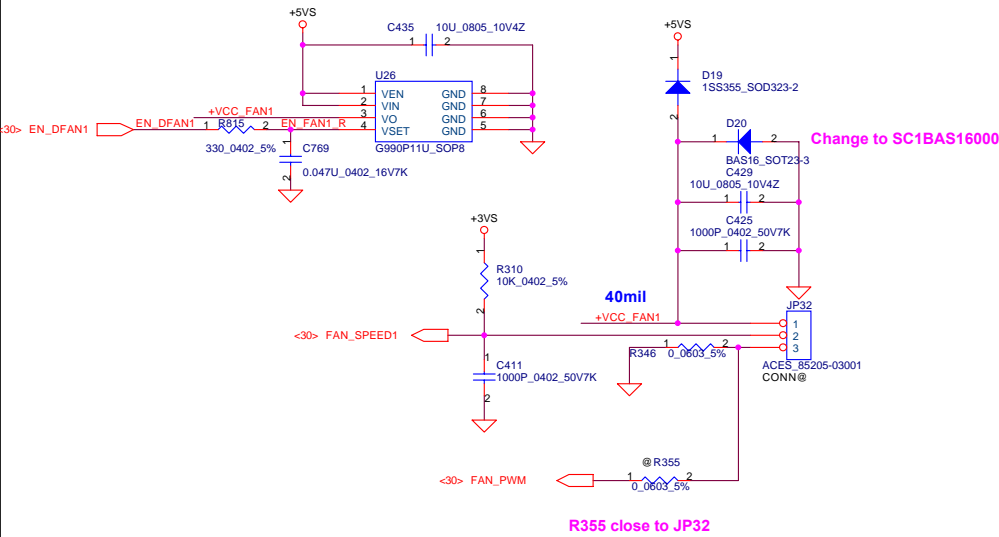


# Int. Speaker Conn.



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Size	B	Document Number	KBYP0 LA-5051P	
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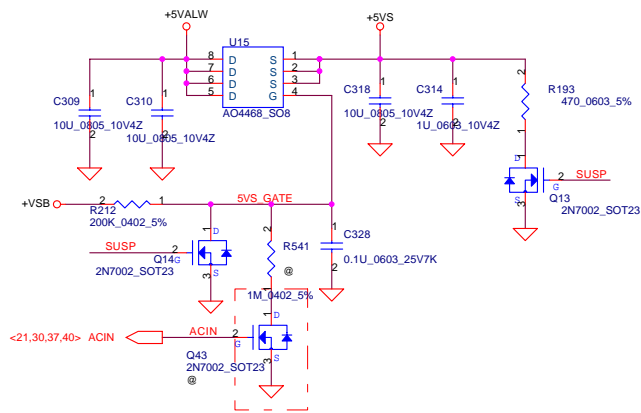
### FAN1 Conn



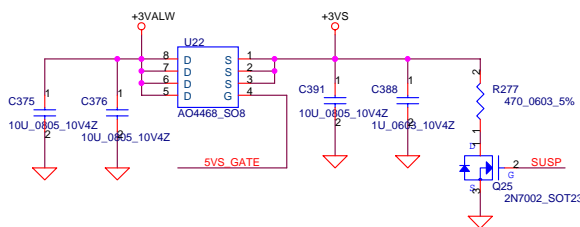
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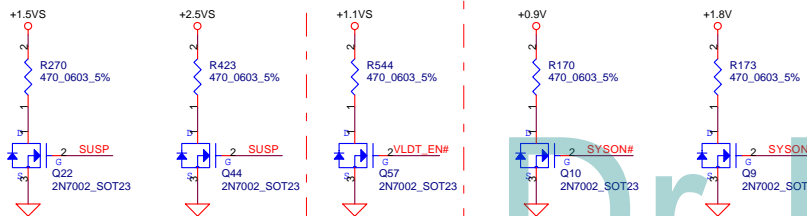
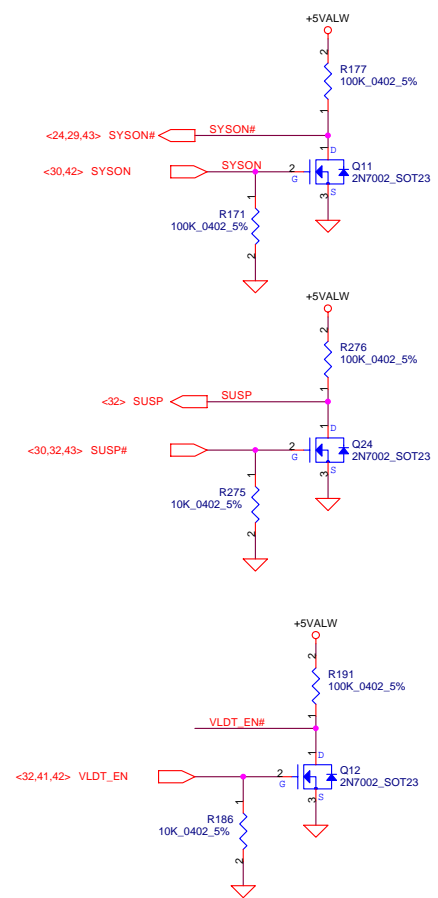
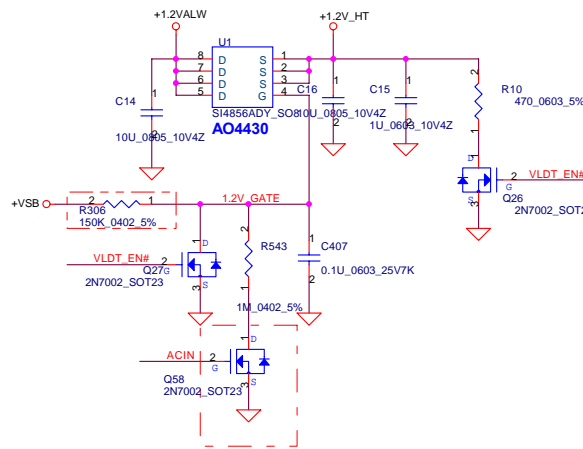
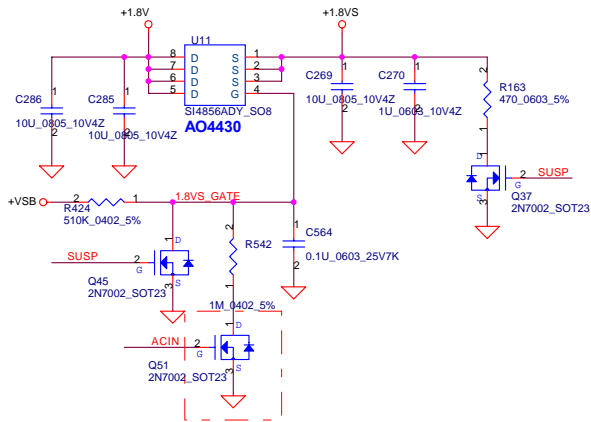
**+5VALW TO +5VS**



**+3VALW TO +3VS**

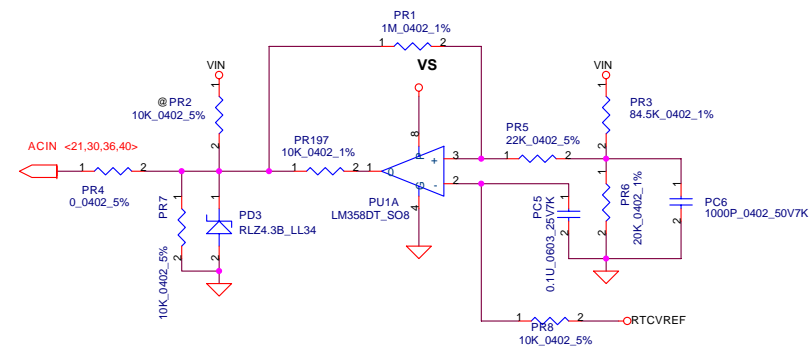
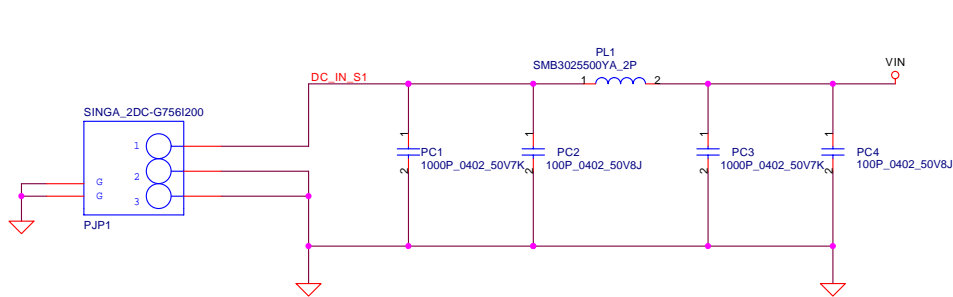


**+1.8V to +1.8VS**

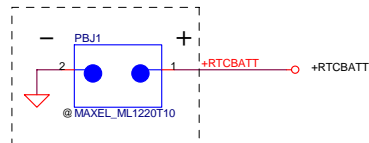


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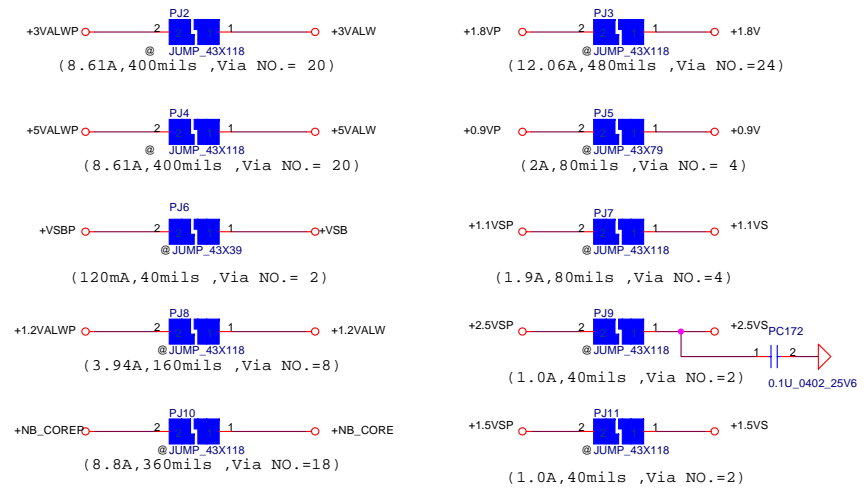
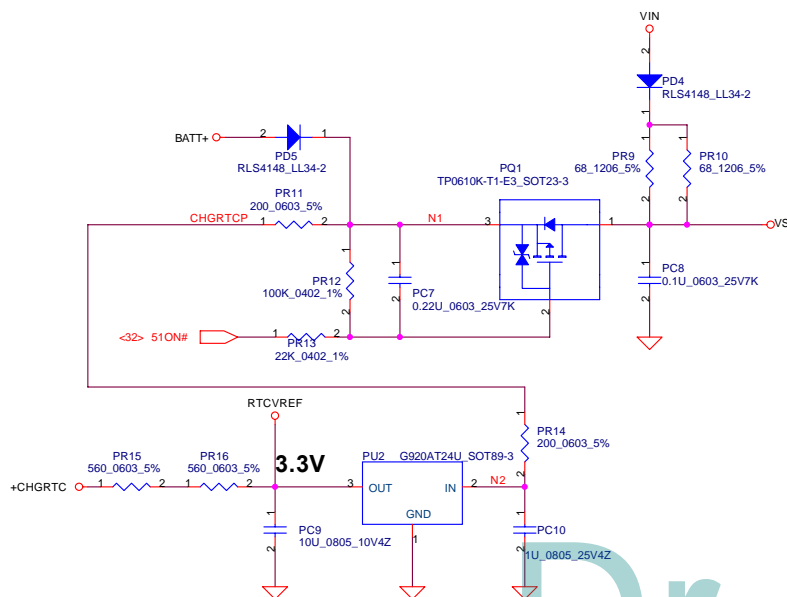


**RTC Battery**



SP093MX0000

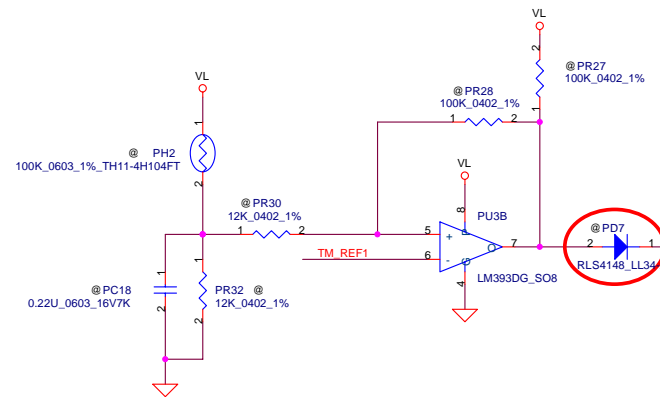
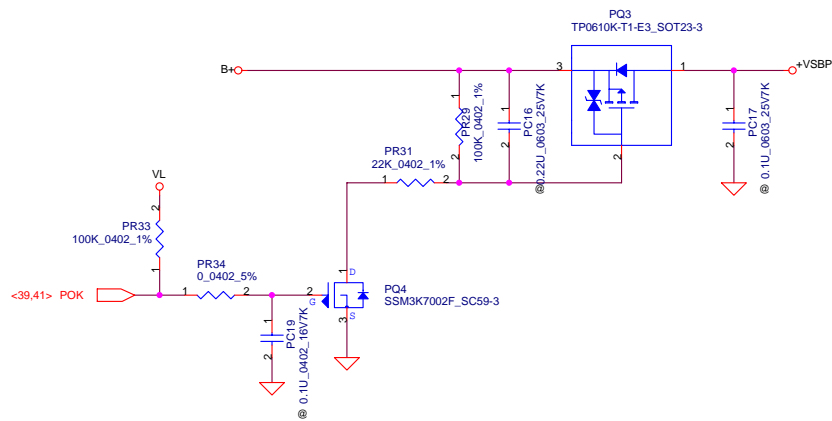
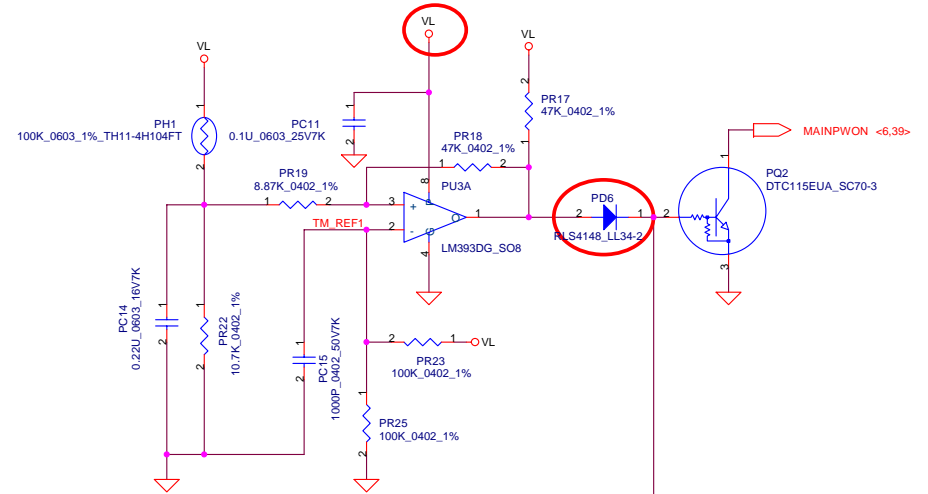
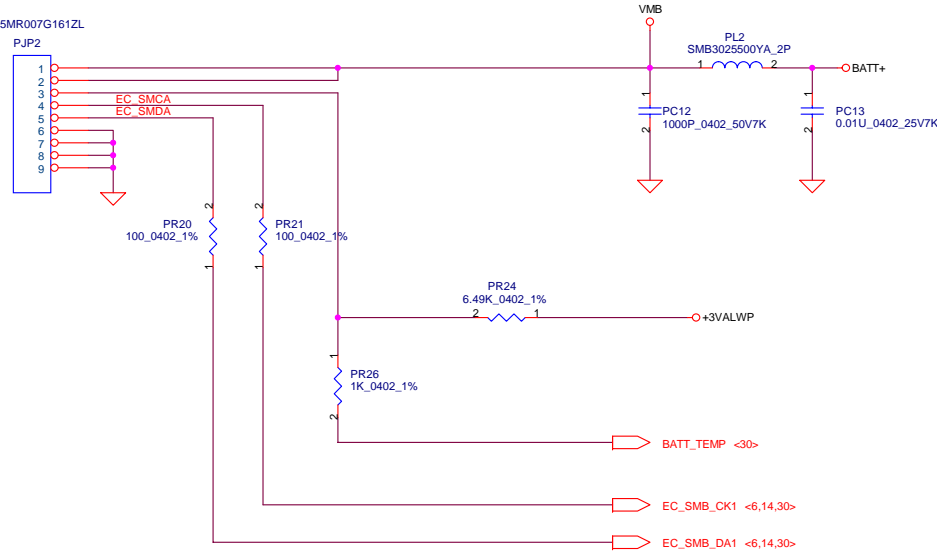
Vin Dectector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V



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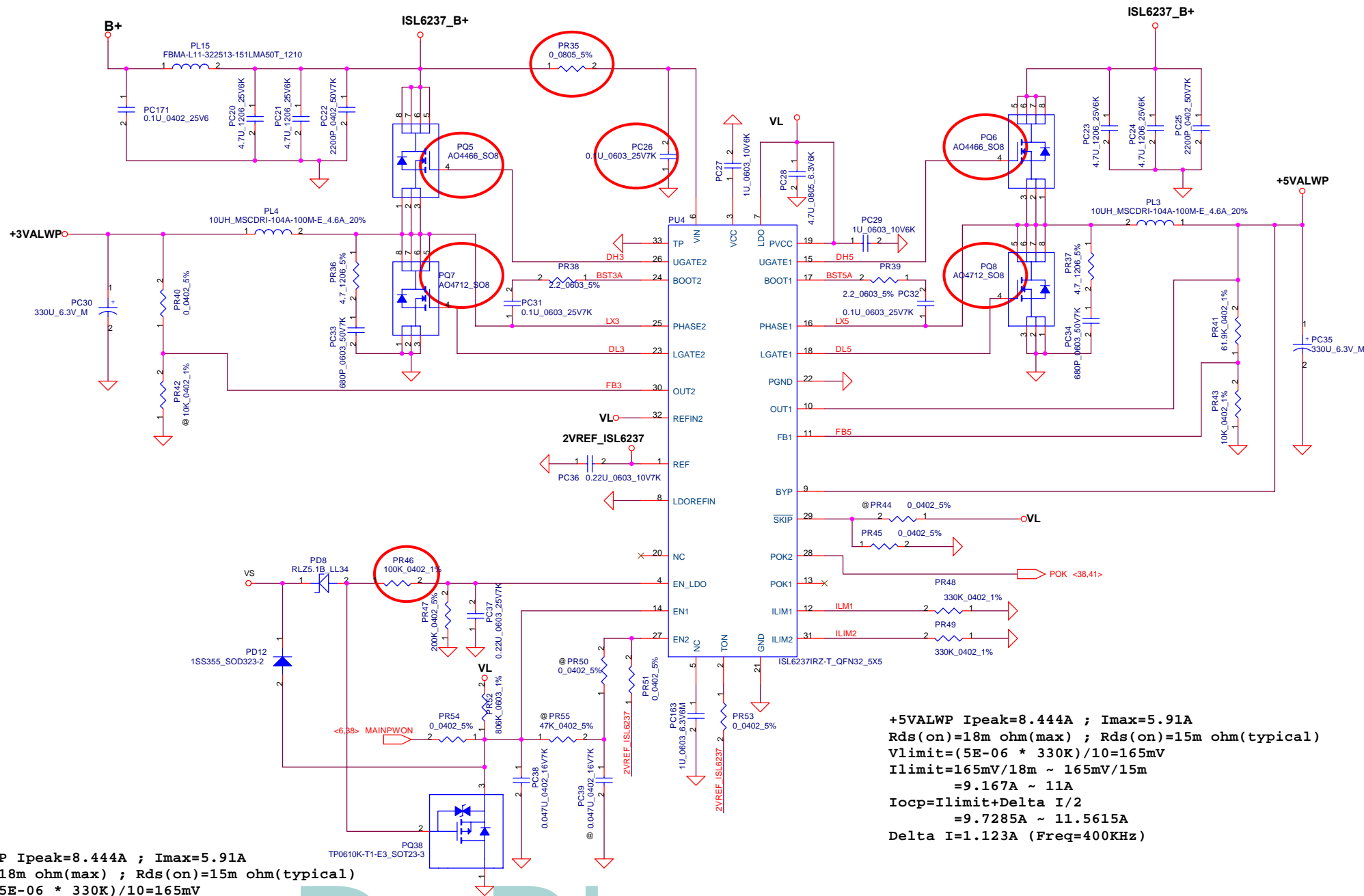
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SUYIN\_200275MR007G161ZL



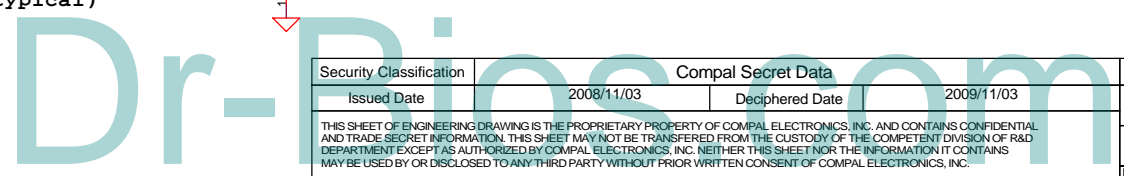
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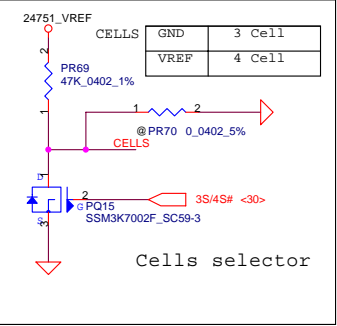
**+5VALWP Ipeak=8.444A ; Imax=5.91A**  
**Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)**  
**Vlimit=(5E-06 \* 330K)/10=165mV**  
**Ilimit=165mV/18m ~ 165mV/15m**  
**=9.167A ~ 11A**  
**Iocp=Ilimit+Delta I/2**  
**=9.7285A ~ 11.5615A**  
**Delta I=1.123A (Freq=400KHz)**

**+3.3VALWP Ipeak=8.444A ; Imax=5.91A**  
**Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)**  
**Vlimit=(5E-06 \* 330K)/10=165mV**  
**Ilimit=165mV/18m ~ 165mV/15m**  
**=9.167A ~ 11A**  
**Iocp=Ilimit+Delta I/2**  
**=9.721A ~ 11.554A**  
**Delta I=1.108A (Freq=300KHz)**

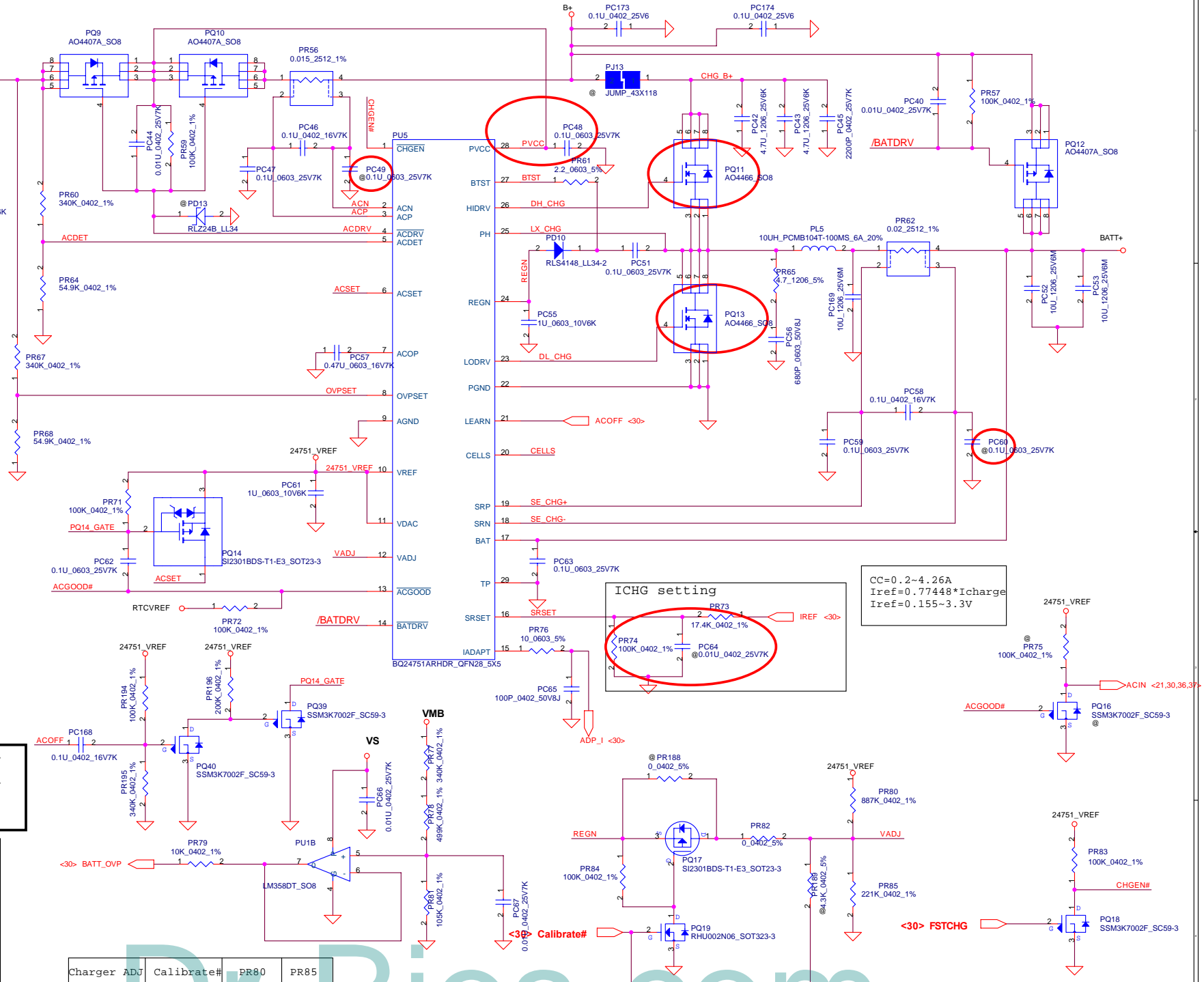
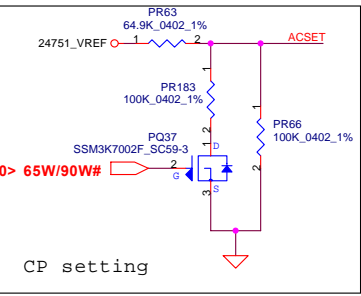


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$I_{charge} = (V_{rsset}/V_{vdac}) * (0.1/PR36)$   
 90W adapter  
 $I_{adapter} = (V_{acset}/V_{vdac}) * (0.1/PR48) = 4.04A$   
 65W adapter  
 $I_{adapter} = (V_{acset}/V_{vdac}) * (0.1/PR48) = 2.90A$   
 Input OVP : 22.3V  
 Input UVP : 17.26V  
 Fsw : 300KHz



**LI-3S : 13.5V --- BATT-OVP=1.5V**  
**LI-4S : 18V --- BATT-OVP=1.998V**  
**BATT-OVP=0.111\*BATT+**



**ICHG setting**  
 $I_{ref} = 0.77448 * I_{charge}$   
 $I_{ref} = 0.155 \sim 3.3V$

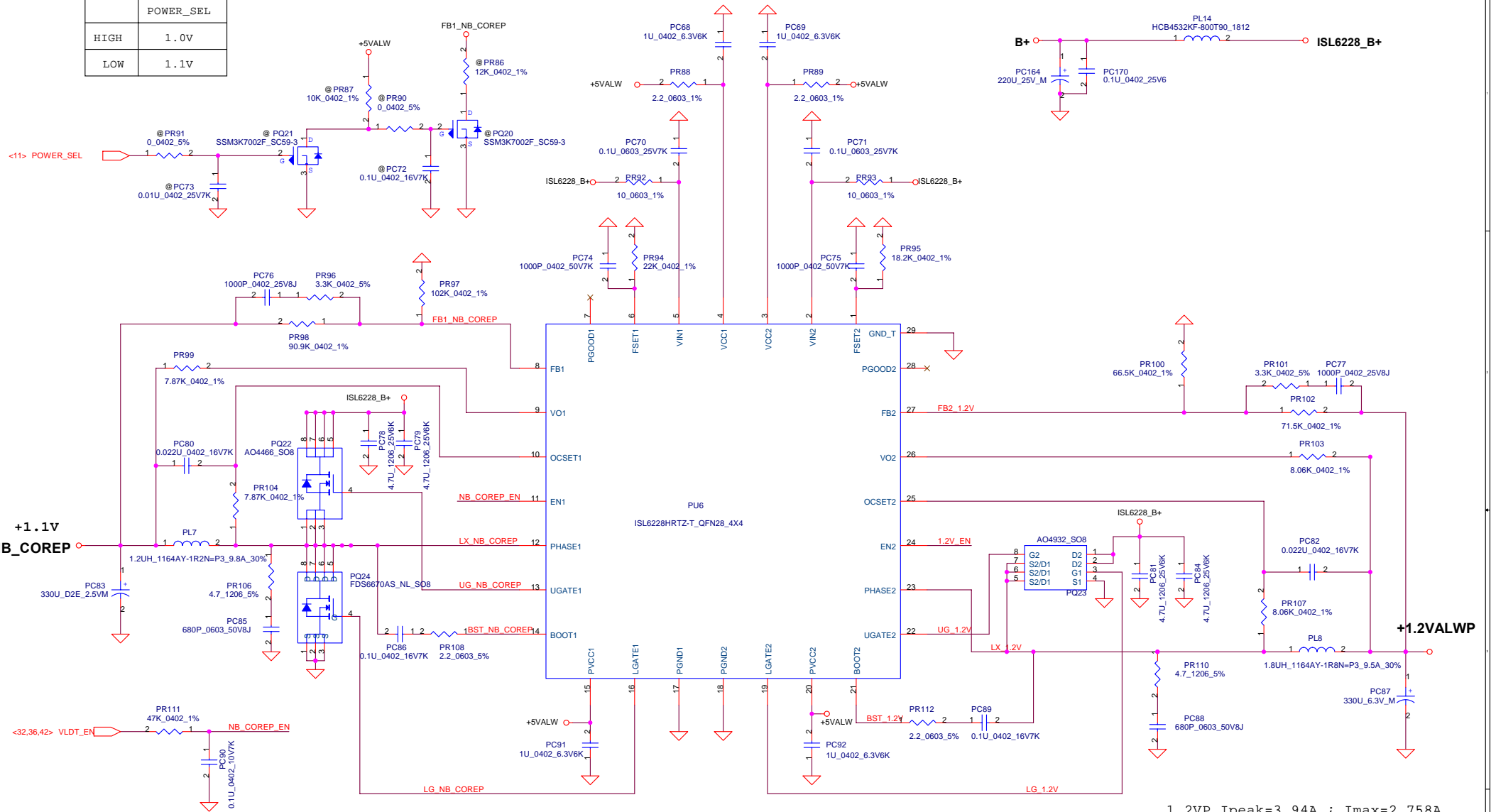
$CC = 0.2 \sim 4.26A$   
 $I_{ref} = 0.77448 * I_{charge}$   
 $I_{ref} = 0.155 \sim 3.3V$

Charger ADJ	Calibrate#	PR80	PR85
4.0V	L	@	0
4.1V	L	887K	221K
4.2V	H	887K	221K

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CHARGER			
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	POWER_SEL
HIGH	1.0V
LOW	1.1V

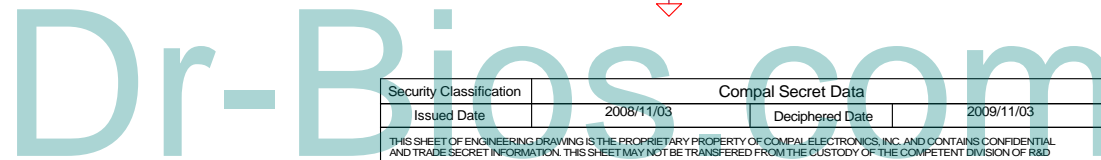
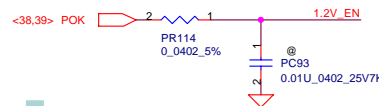


1.1VP Ipeak=8.9A ; Imax=6.23A  
 DCR=6m ohm (max)  
 $Rocset=(Iocp*DCR)/10E-06=7.68K\ ohm$   
 $Iocp=9.846A(1.3*DCR)$   
 $Csen=L/(Rocset*DCR)=0.022uF$

Freq=303KHz  
 $Rfset=1/(1.5E-10 * Freq)=22K$

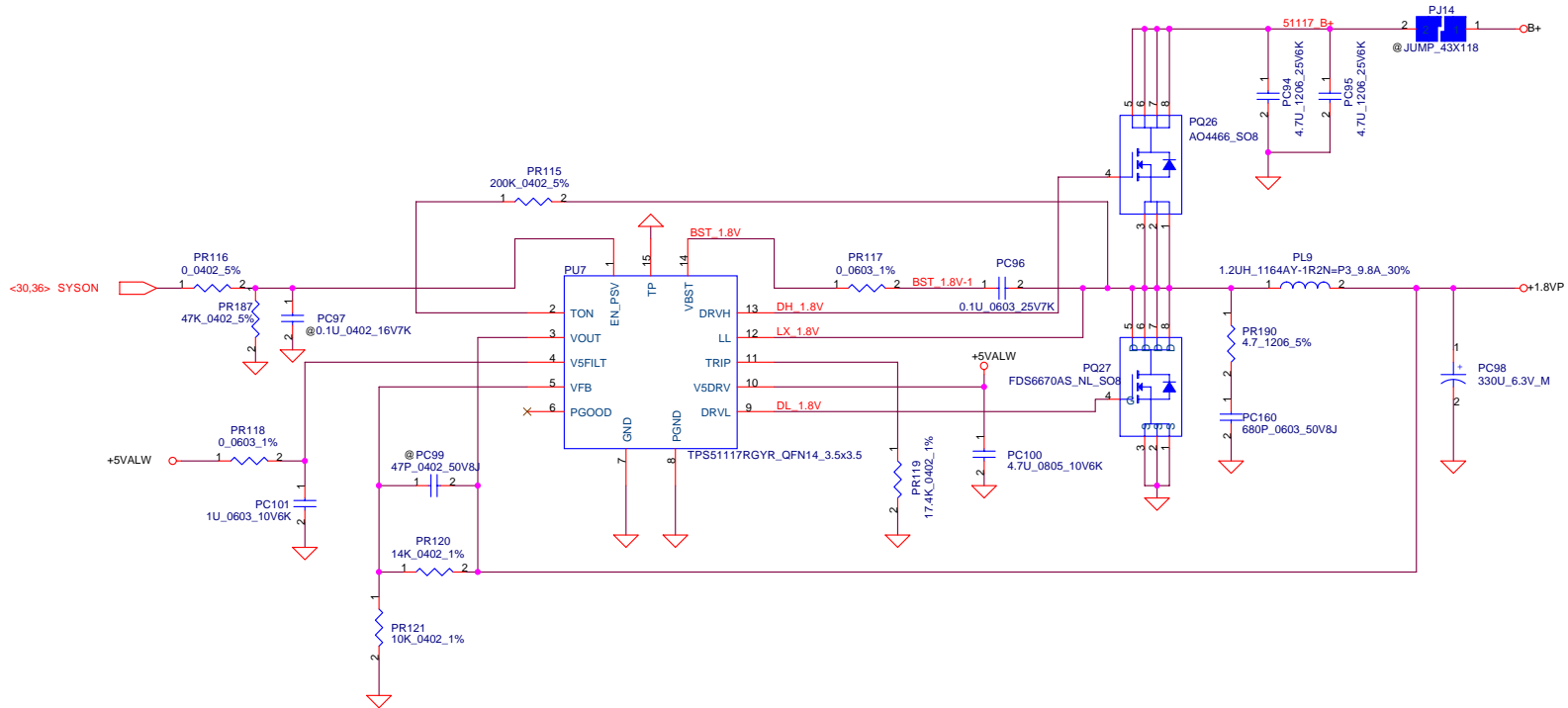
1.2VP Ipeak=3.94A ; Imax=2.758A  
 DCR=10m ohm (max)  
 $Rocset=(Iocp*DCR)/10E-06=6.65K\ ohm$   
 $Iocp=5.542A(1.2*DCR)$   
 $Csen=L/(Rocset*DCR)=0.027uF$

Freq=366KHz  
 $Rfset=1/(1.5E-10 * Freq)=18.2K$



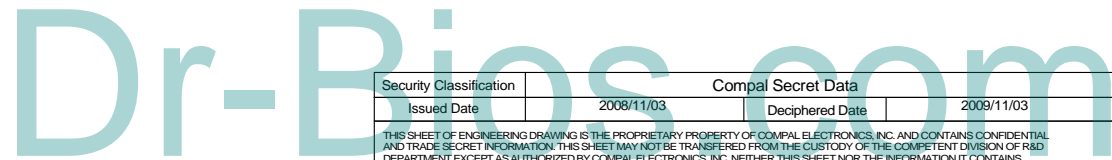
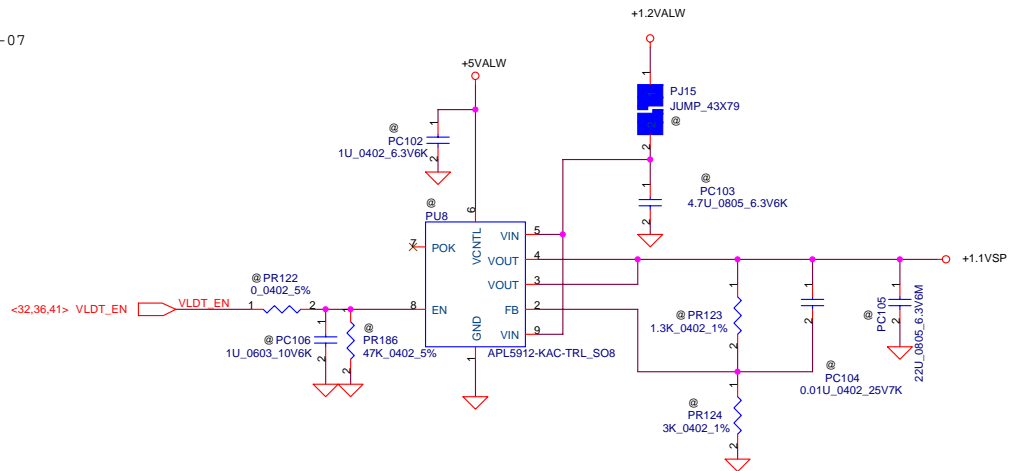
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Title		
NB_COREP / 1.2VSB		
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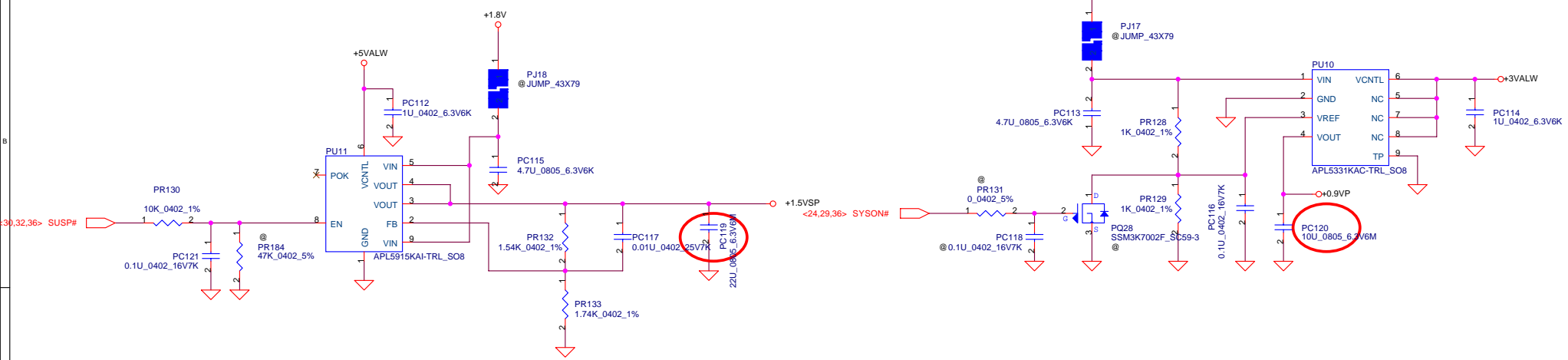
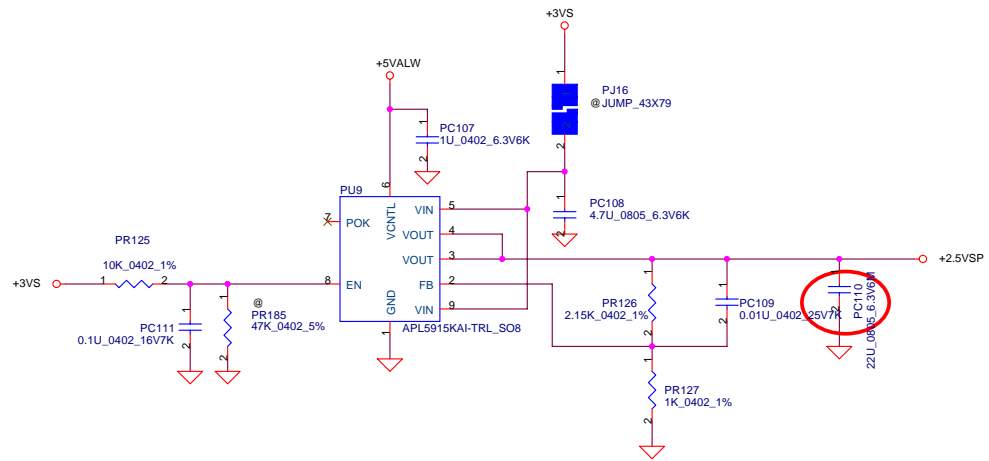


$V_{FB}=0.75V$   
 $V_o=V_{FB} \cdot (1 + PR120/PR121) = 1.8V$   
 $T_{on} = 19E-12 \cdot R_{on} \cdot ((2/3) \cdot V_o + 100mV) / (V_{in}) + 50ns = 3.1E-07$   
 $Freq = 305KHz$

$C_{esr} = 15m \text{ ohm}$   
 $I_{peak} = 12.6A \quad I_{max} = 8.82A$   
 $\Delta i = ((19-1.8) \cdot (1.8/19)) / (L \cdot Freq) = 5.332A$   
 $V_{trip} = R_{trip} \cdot I_{0uA} = 0.24V$   
 $I_{ocp-min} = V_{trip} / R_{ds(on)max} \cdot 1.4 + 2.666 = 17.573A$   
 $I_{ocp-max} = V_{trip} / R_{ds(on)typ} \cdot 1.2 + 2.666 = 26.908A$   
 $I_{ocp} = 17.573 - 26.908A$



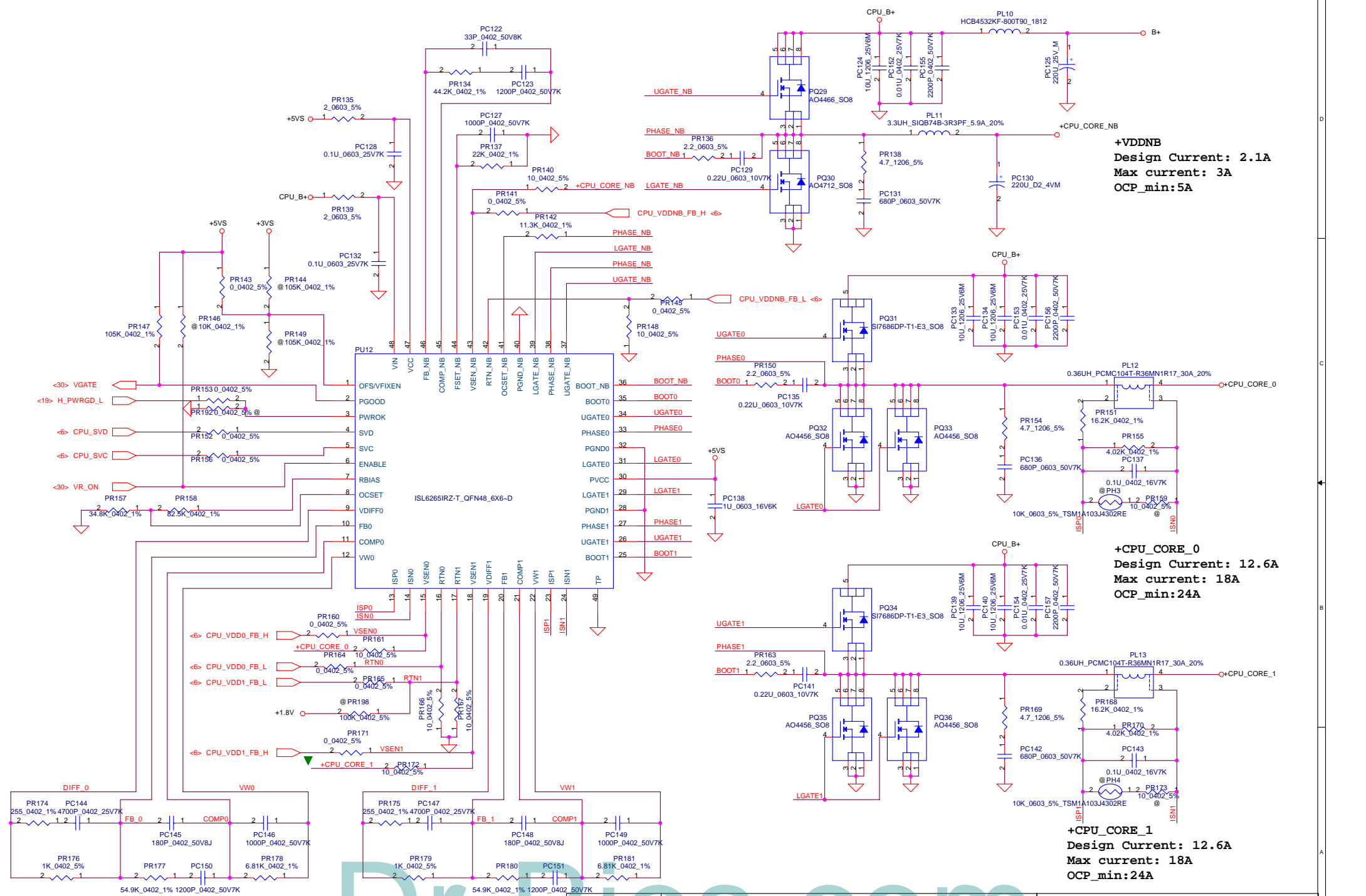
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				Document Number	
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**+VDDNB**  
**Design Current: 2.1A**  
**Max current: 3A**  
**OCp\_min:5A**

**+CPU\_CORE\_0**  
**Design Current: 12.6A**  
**Max current: 18A**  
**OCp\_min:24A**

**+CPU\_CORE\_1**  
**Design Current: 12.6A**  
**Max current: 18A**  
**OCp\_min:24A**

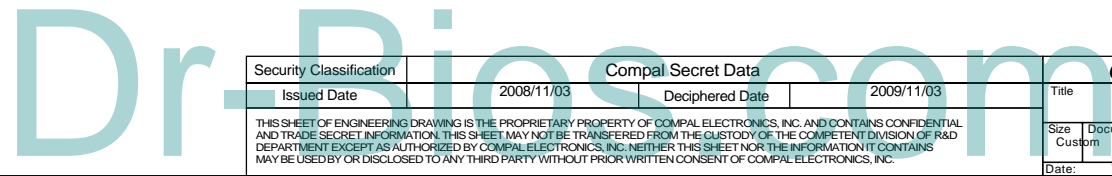
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Title		
+CPU_CORE		
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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	EMI request.	EMI request.	0.1	40	Change PR38, PR39, PR108, PR112, PR136, PR150, PR163 from SD013000080 to SD013220B80.	08, 12/24	to DVT
2	EMI request.	EMI request.	0.1	40	Add PC170, PC171, PC172, PC173, PC174 SE000000G880 S CER CAP 0.1U 25V K X5R 0402	08, 12/24	to DVT
3	EMI request.	EMI request.	0.1	39	Add PL15 SM010016410 S SUPPRE_ KC FBMA-L11-322513-151LMA50T	08, 12/24	to DVT
4	EMI request.	EMI request.	0.1	41	Add PL14 SM010018210 S SUPPRE_ TAI-TECH HCB4532KF -800T90 1812	08, 12/24	to DVT
5	Link CIS error.	Link CIS error.	0.1	40	Change PQ9, PQ10, PQ12 from SB944070000 S TR AO4407 1P SO8 W/D to SB000000DL00 S TR AO4407A 1P SO8	08, 12/24	to DVT
6	cost down	cost down	0.1	40	Change PC30 from SGA19331360 S POLY C 330U 6.3V M D3L ESR25M TPE H2.8 to SF000001G00 S_A-P_CAP 330U 6.3V M 6.3X5.7 LESR14M ME	08, 12/24	to DVT
7	cost down	cost down	0.1	40	Change PC35 from SGA20151320 S POLY C 150U 6.3V M D2E TPE ESR18 H1.8 to SF000001G00 S_A-P_CAP 330U 6.3V M 6.3X5.7 LESR14M ME	08, 12/24	to DVT
8	cost down	cost down	0.1	41, 42	Change PC87, PC98 from SGA19331D00 S POLY C 330U 2.5V D2 TPE LESR15M H1.8 to SF000001G00 S_A-P_CAP 330U 6.3V M 6.3X5.7 LESR14M ME	08, 12/24	to DVT
9	schematic update.	schematic update.	0.1	44	Delete PR198 SD028100380 S RES 1/16W 100K +-5% 0402	08, 12/24	to DVT
10	layout space too small.	layout space too small.	0.1	41	Change PQ23 from SB00000CG00 S TR AO4466 1N SO8 to SB00000BG00 S TR AO4932 2N SO8 Delete PQ25 SB00000AJ00 S TR AO4712 1N SO8	08, 12/24	to DVT
11							
12							
13							
14							
15							
16							
17							
18							



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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
12/17		p.12	L3,L4 change from bead to 0 Ohm	
12/17		P.17	Add R858~R865 for VGA HDMI	
12/17		P.18	R374,R375,R376 change from 0 ohm to 10 ohm	
12/17		P.20	R50 ,R53 change from JV70@ to @	
12/17		P.20	R51 ,R52 change from JM70@ to JV70@	
12/17		P.24	JP18 change from ESATA to USB port	
12/17		P.25	R396 change from 10K to 0 Ohm	
12/17		P.31	C905~C907 change from 0.1u to 33P	
12/17		P.31	U19 change from mount to @ ; U18 change from @ to mount	
12/17		P.32	D22 change from mount to @	
12/18		P.24	SATA re-driver IC reserved	
12/22		P.8	Add c124,c128,c151,c155,c55,c119,c113,c197 0.1uF	EMI request
12/22		P.30	Add c40 c41 100P	EMI request
12/22		P.30	Add c42,c43,c45	EMI request
12/22		P.37~p.45	upgrade PWR schematic	
12/22		P.30	Add C65 22uF for CRT flicker	
12/23		P.21	Delete R174,R175	
01/16		P.16	Add r611,r612 connect to INVT_PWM	Vari-Bright reserved
01/16		P.11	Add r347 connect to BKOFF#	Vari-Bright reserved
01/16		P.30	add r288 BKOFF# 4.7k pull low	

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