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Title: ***Cover Page***

Size	Document Number	Rev
A4	Brook_BH	-1M

Date: Wednesday, February 04, 2015 Sheet 1 of 106

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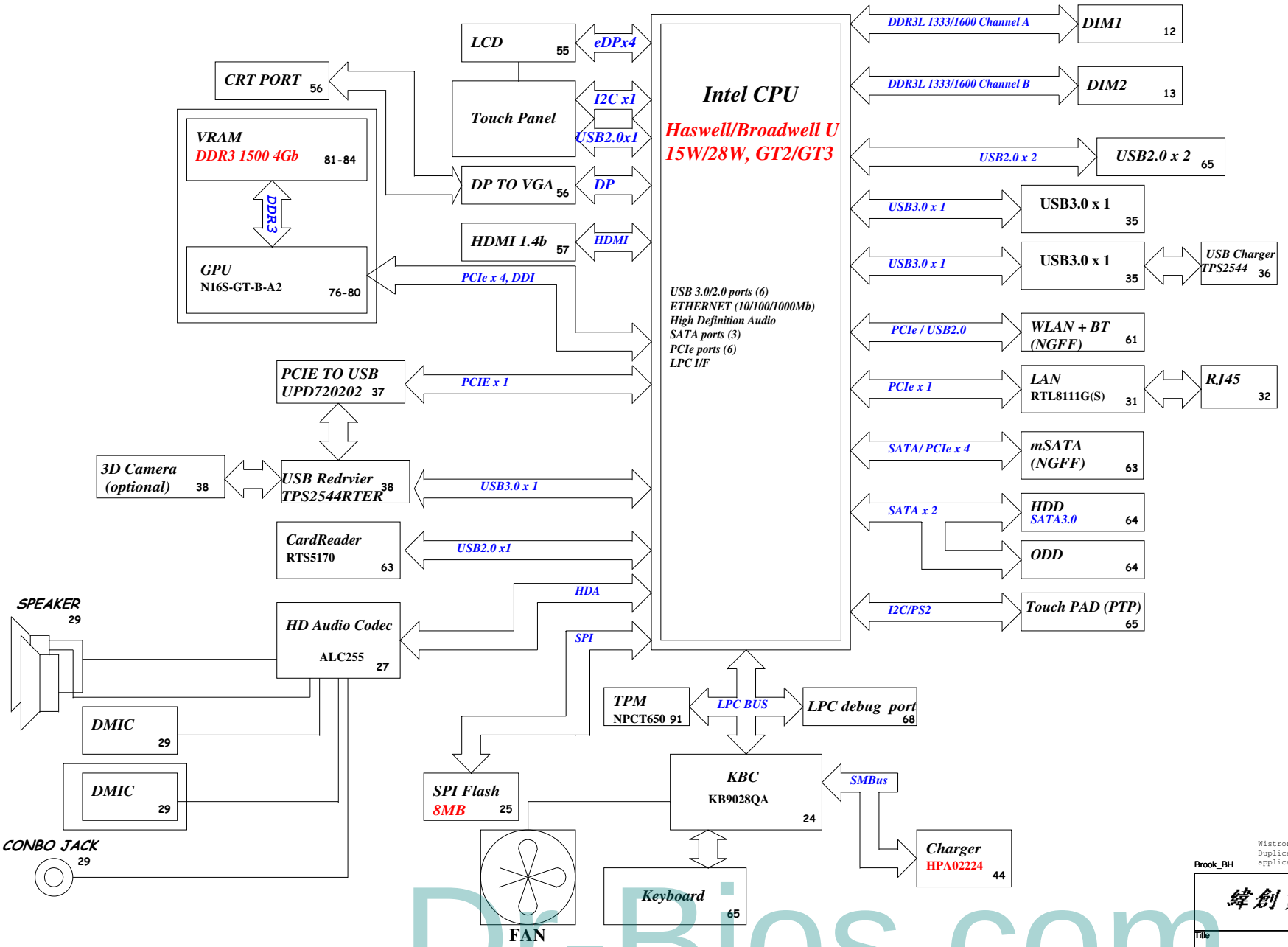
BROOK ULT Board Block Diagram

Project code : 4PD04X010001
PCB P/N : 14276
Revision : -1M



CHARGER HPA02224	44
INPUTS	OUTPUTS
DCBATOUT	BT+

SYSTEM DC/DC RT6575B	45
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5

CPU DC/DC RT6575B	46-47
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC TPS51716	48
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0

SYSTEM DC/DC RT8231	49
INPUTS	OUTPUTS
DCBATOUT	1D35V_S3

SYSTEM LDO S13390D15	51
INPUTS	OUTPUTS
3D3V_S5	1D3V_S5

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Title: Block Diagram

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Date: Wednesday, February 04, 2015 | Sheet 2 of 106

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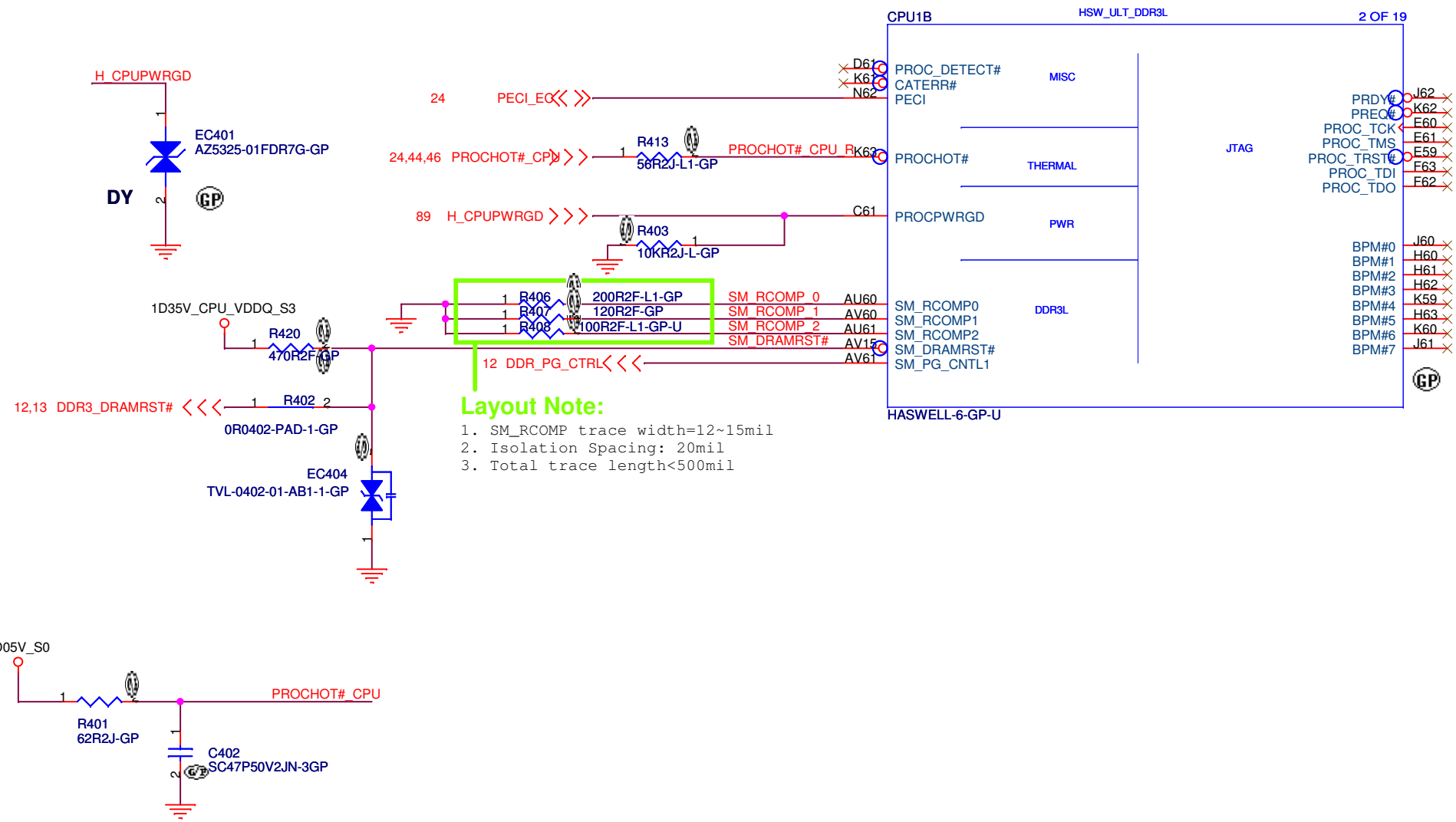

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Title: CPU (THERMAL/CLOCK/PM)

Size: A4 | Document Number: Brook_BH | Rev: -1M

Date: Wednesday, February 04, 2015 | Sheet 4 of 106

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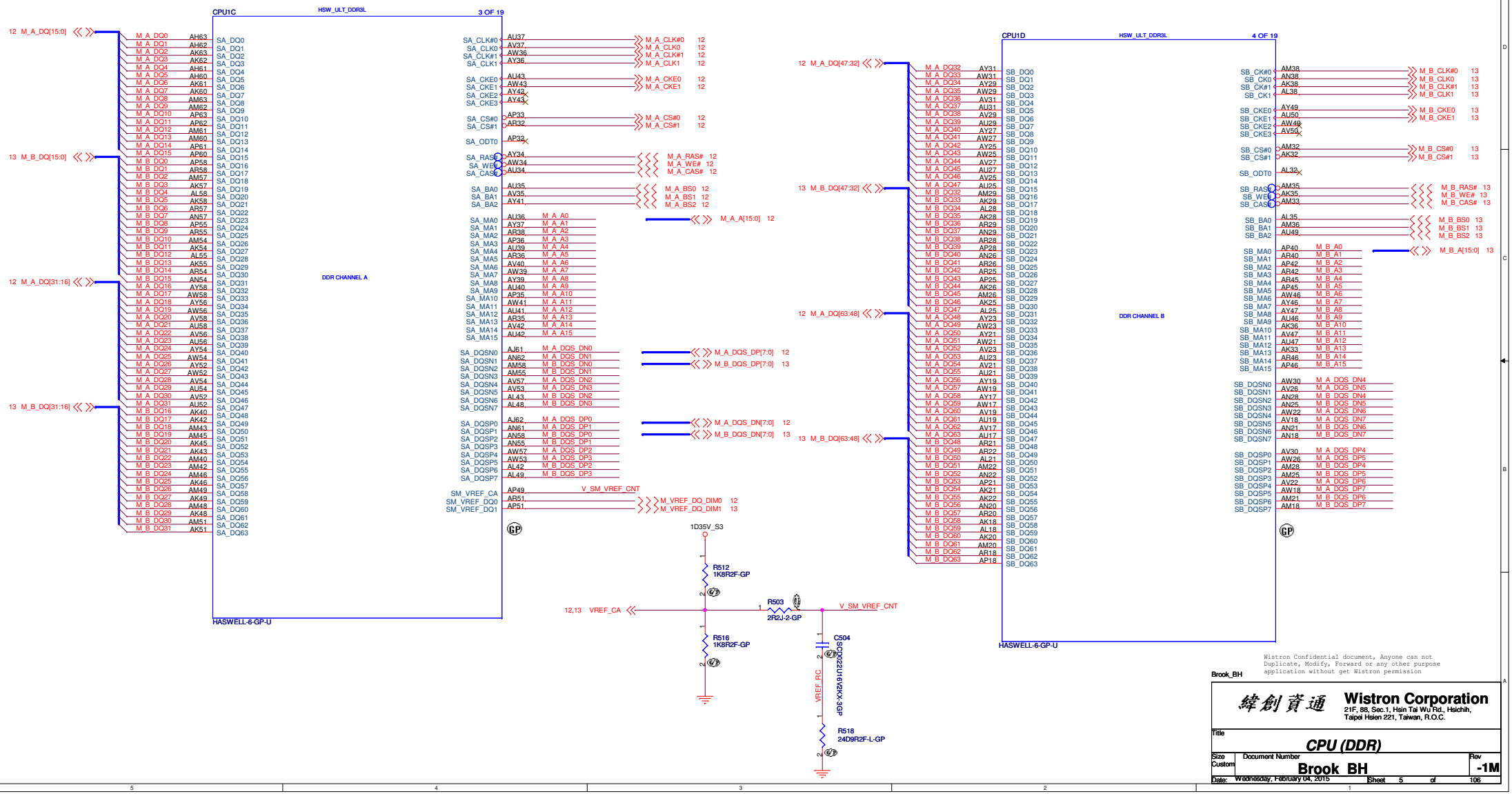
SSID = CPU



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Title: **CPU (DDR)**

Size	Document Number	Rev
Custom	Brook_BH	-1M

Date: Wednesday, February 04, 2015 Sheet 5 of 106

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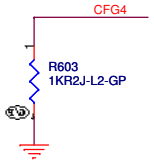
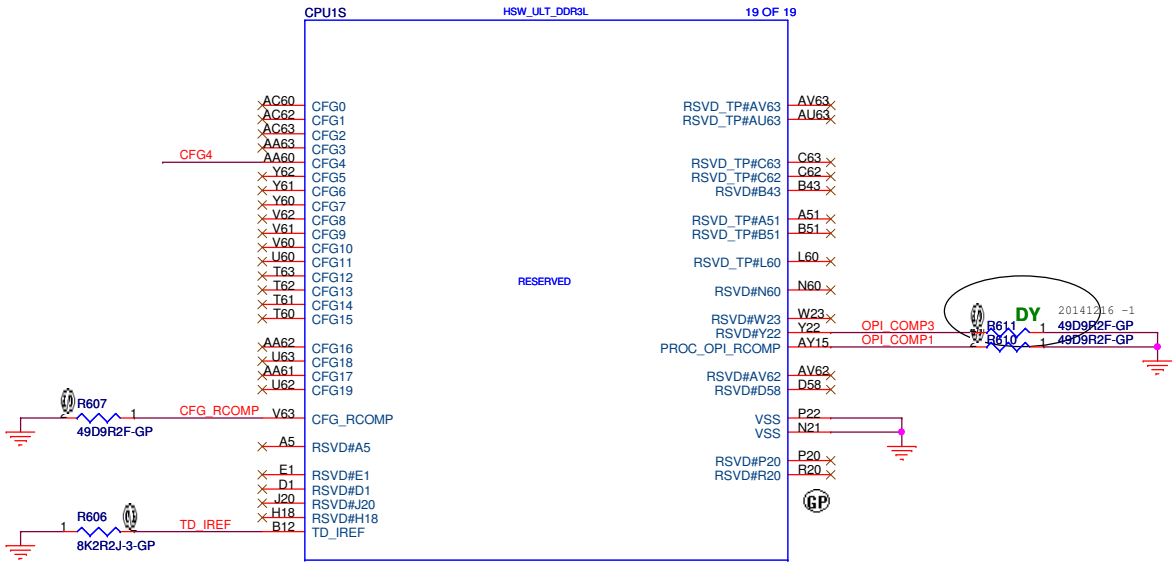
SSID = CPU

Pin Name	System Pull-up/Pull-down	Schematic Notes	✔
CFG[19:0]		Please refer to the *Crescent Bay and (??) Platforms - Debug Port Design Guide (DPDG)* .	

Note: Processor strap CFG[4] should be pulled low to enable embedded DisplayPort*

eDP Enable	
CFG4	1:Disable
	0:Enable





Signal Name	Description	Direction/ Buffer Type
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. • **CFG[3:0]:** Reserved configuration lane. A test point may be placed on the board for these lanes. • PCI Express* Static x16 Lane Numbering Reversal. — — • • **CFG[4]: eDP enable** — 1 = Disabled — 0 = Enabled • **[19:5]:** Reserved configuration lanes. A test point may be placed on the board for these lands.	I/O GTL
CFG_RCOMP	Configuration resistance compensation.	-
FC_x	FC signals are signals that are available for compatibility with other processors. A test point may be placed on the board for these lands. Refer to the appropriate platform design guide for implementation details.	

continued...

7.4 Reserved or Unused Signals

The following are the general types of reserved (RSVD) signals and connection guidelines:

- RSVD – these signals should not be connected
- RSVD_TP – these signals should be routed to a test point
- RSVD_NCTF – these signals are non-critical to function and may be left un-connected

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Title: **CPU (CFG)**

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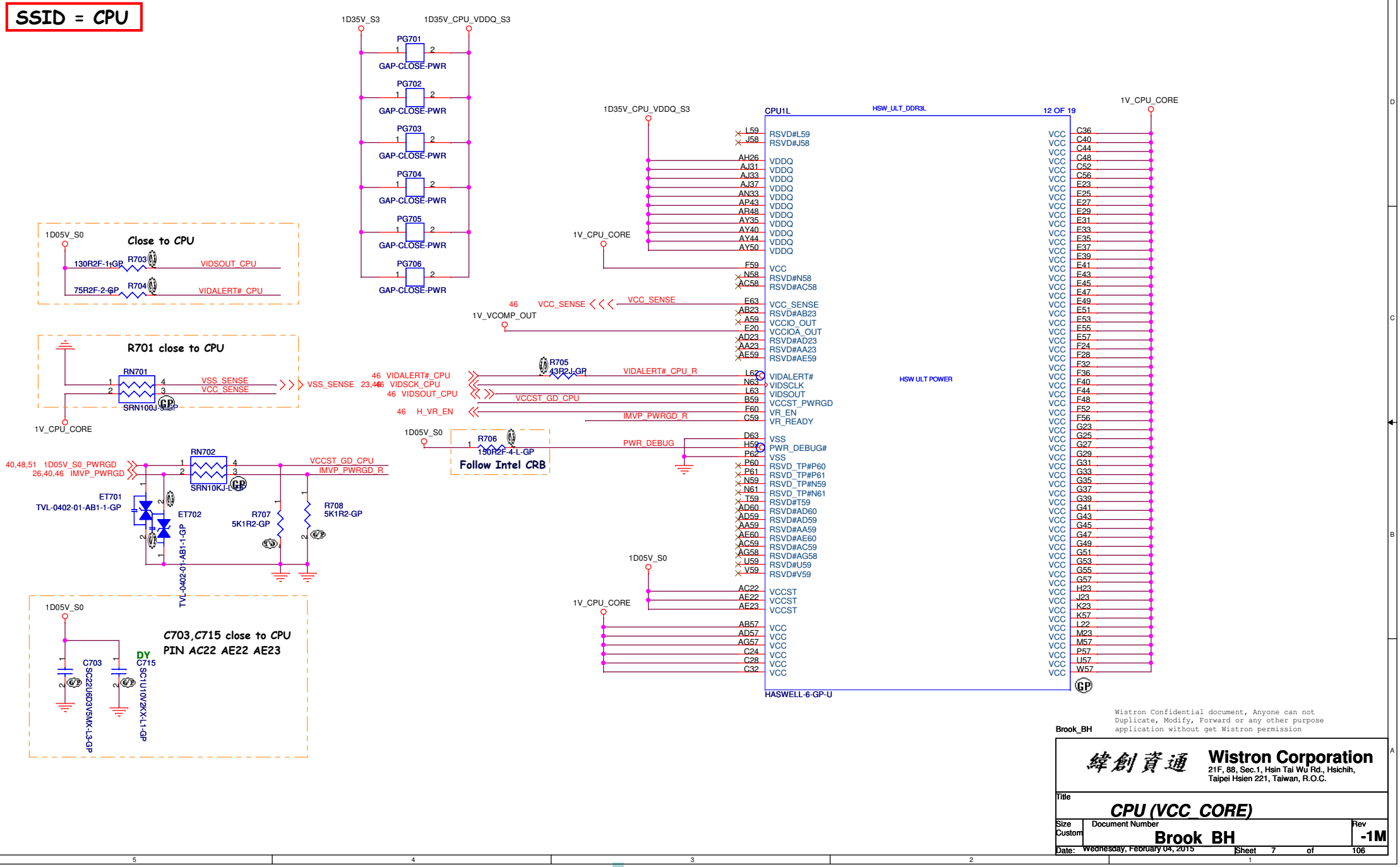
SSID = CPU



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Title: CPU (VCC_CORE)

Size	Document Number	Rev
Custom	Brook_BH	-1M

Date: Wednesday, February 04, 2015 Sheet 7 of 106

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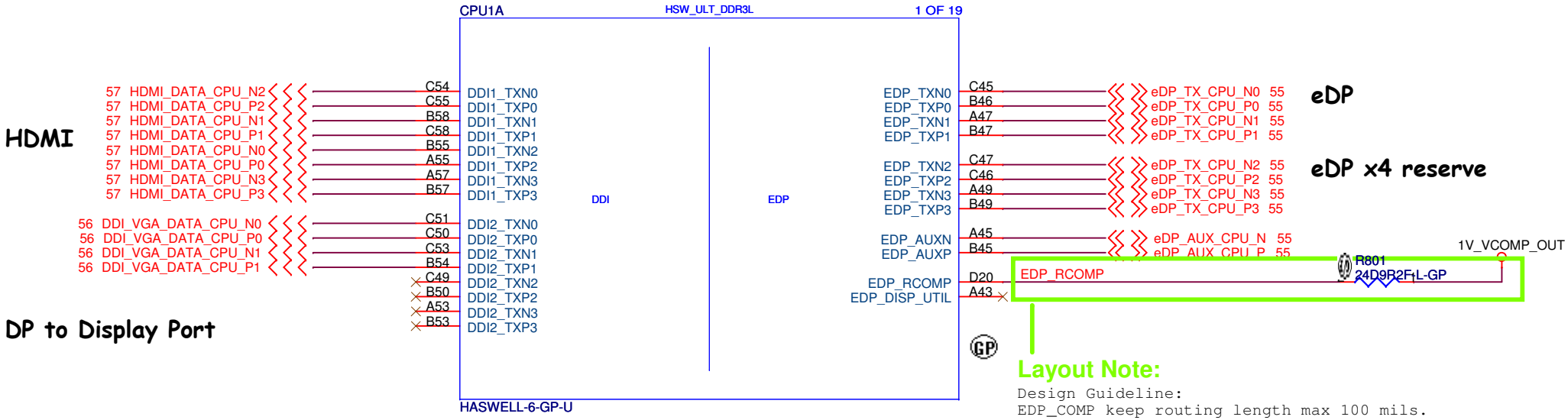
SSID = CPU



DP to Display Port

Layout Note:

Design Guideline:
EDP_COMP keep routing length max 100 mils.
Trace Width:20 mils.

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω ±1%	Max = 100 mils

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Title: CPU (DDI/EDP)

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1D35V_CPU_VDDQ_S3

Power current=3A

C1040 SC10U6D3V3MX-L-GP
C1035 SC10U6D3V3MX-L-GP DY
C1036 SC10U6D3V3MX-L-GP
C1037 SC10U6D3V3MX-L-GP
C1038 SC10U6D3V3MX-L-GP
C1039 SC10U6D3V3MX-L-GP

EC1006 SC2D2U10V3KX-L-GP
EC1007 SC2D2U10V3KX-L-GP
EC1008 SC2D2U10V3KX-L-GP
EC1009 SC2D2U10V3KX-L-GP

For Intel Recommend EE Part

1V_CPU_CORE

Power current=40A

PC1010 SC22U6D3V5MX-L3-GP
PC1009 SC22U6D3V5MX-L3-GP
PC1007 SC22U6D3V5MX-L3-GP
PC1006 SC22U6D3V5MX-L3-GP
PC1005 SC22U6D3V5MX-L3-GP
PC1002 SC22U6D3V5MX-L3-GP

PC1020 SC22U6D3V5MX-L3-GP
PC1019 SC22U6D3V5MX-L3-GP
PC1018 SC22U6D3V5MX-L3-GP
PC1017 SC22U6D3V5MX-L3-GP
PC1016 SC22U6D3V5MX-L3-GP
PC1015 SC22U6D3V5MX-L3-GP
PC1013 SC22U6D3V5MX-L3-GP
PC1012 SC22U6D3V5MX-L3-GP

1V_CPU_CORE

DY
EC1001 SC22U6D3V5MX-L3-GP
EC1002 SC22U6D3V5MX-L3-GP
EC1003 SC22U6D3V5MX-L3-GP
EC1004 SC22U6D3V5MX-L3-GP
EC1005 SC22U6D3V5MX-L3-GP
EC1016 SC22U6D3V5MX-L3-GP

1V_CPU_CORE

15WDY/28W
PT1001 ST220U2VDM-8-GP

1V_CPU_CORE

C1002 SC1U10V2KX-L1-GP
C1003 SC1U10V2KX-L1-GP
C1004 SC1U10V2KX-L1-GP
C1005 SC1U10V2KX-L1-GP

For Intel Recommend EE Part

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Title: CPU (Power CAP1)

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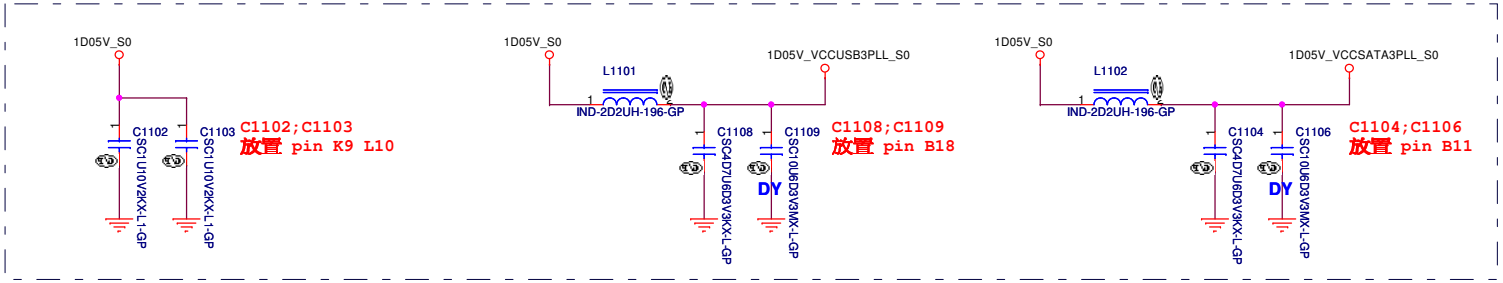
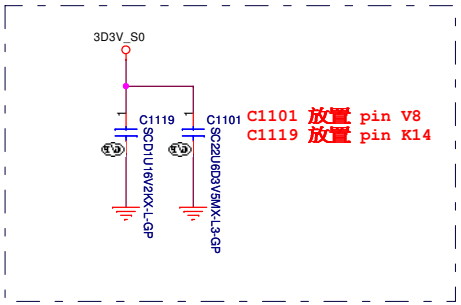
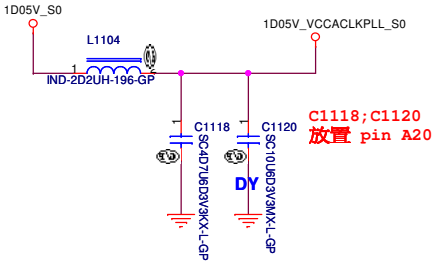
擺放電容的位置請參考 Page 21,每個位置如下

MAX: 3.074A

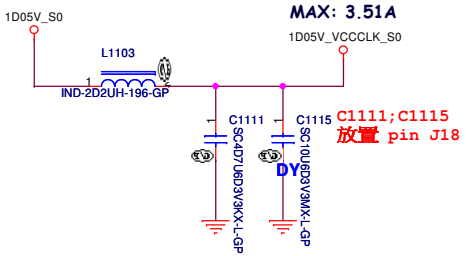


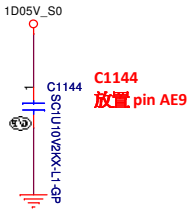
MAX: 0.285A

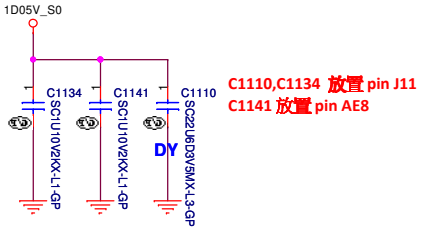


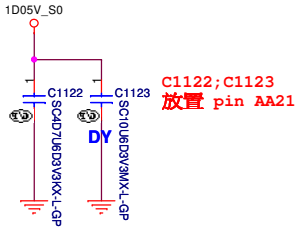


MAX: 3.51A









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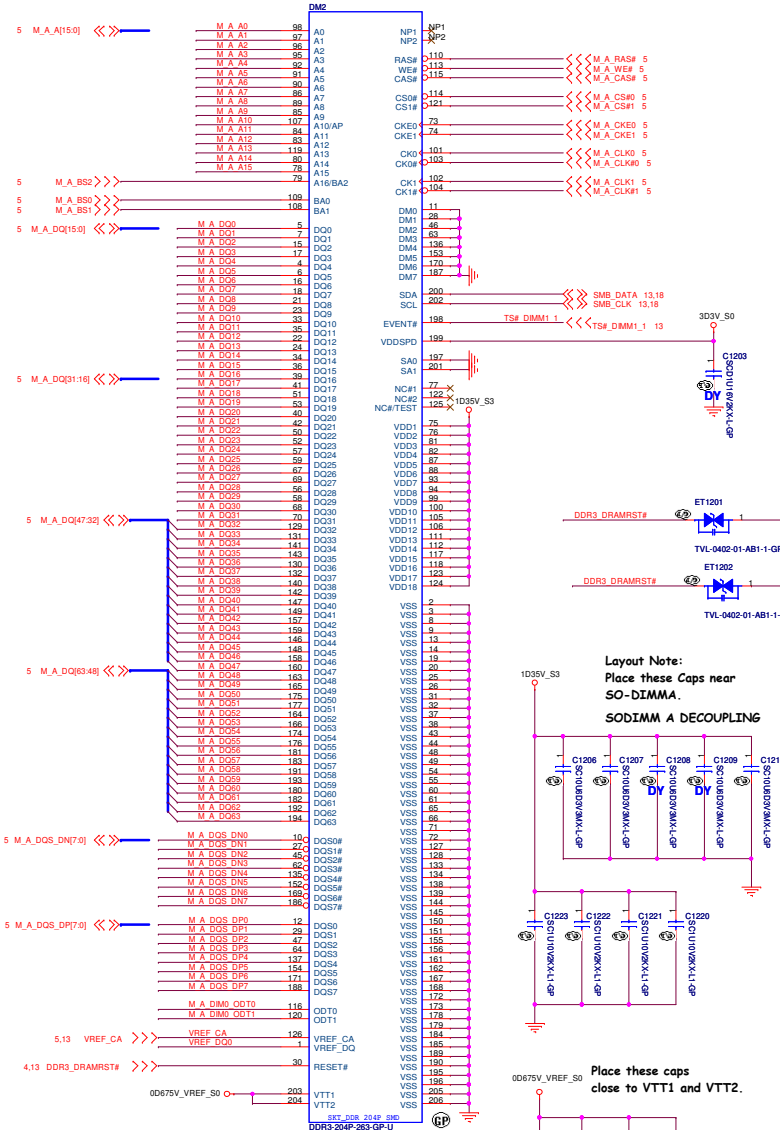
SSID = MEMORY

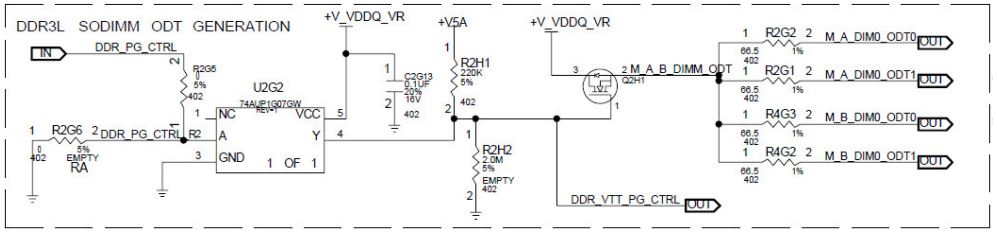


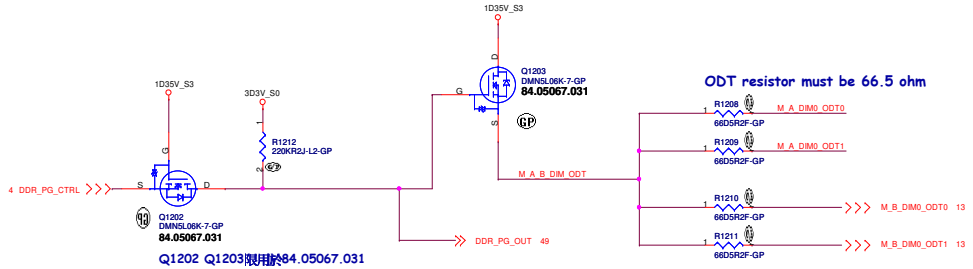
Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

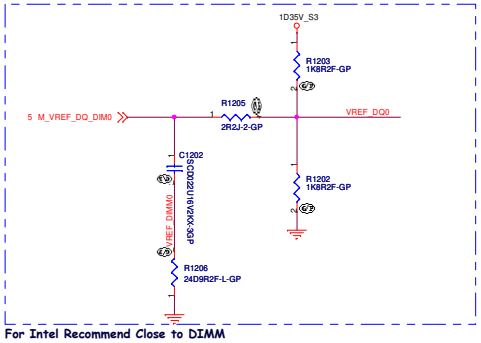
If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

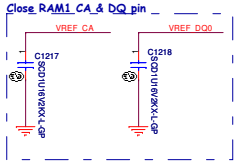
SODIMM Memory Connectivity and Topology
ODT Signal Connectivity and Support
For DDR3L SODIMM designs, Intel recommends ODT signals not to be routed between CPU and DIMM on platform, leave ODT at CPU as no-connect (open), and tie DIMM ODT to VDDQ through FET and resistor. The reason for this additional ODT-control circuitry on the platform is to save power dissipation by turning off VDDQ to VTT path during low power states, as ODT signal is terminated to VTT through RTT on SODIMM. The ODT value for DDR3L SODIMM 1-DPC platform will be encoded in the write command and use RTT_NOM = Off and RTT_WR = (60,120) Ohm.

- CPU ODT output would be NOCON
- SODIMM ODT input should be tied to VDDQ through a FET and a resistor to support low power states.









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Title: **DDR3-SODIMM1**
Size: A2 | Document Number: **Brook_BH** | Rev: **-1M**
Date: Wednesday, February 04, 2015 | Sheet 12 of 106

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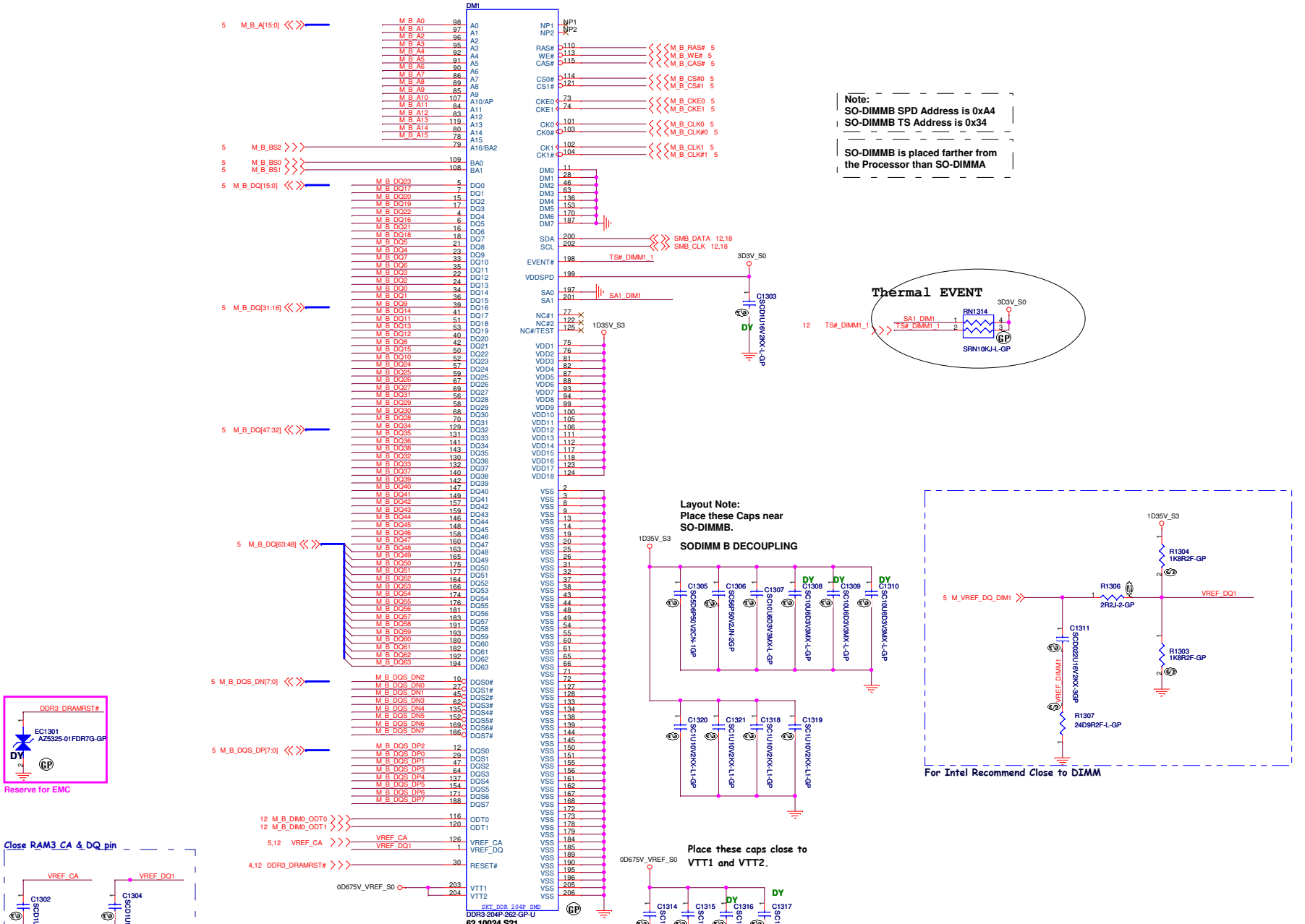
SSID = MEMORY



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Title: DDR3-SODIMM2

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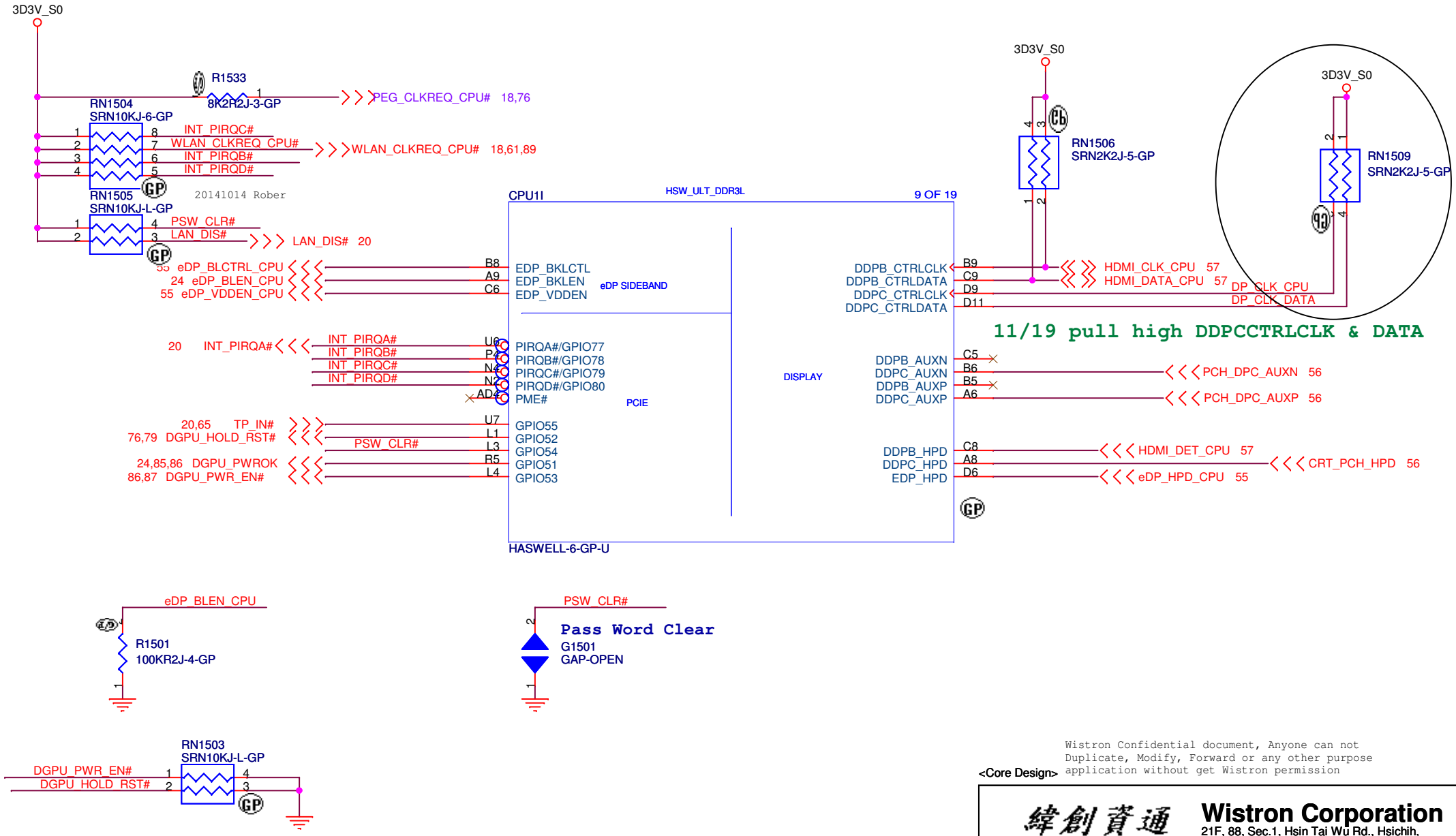

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<Core Design>

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Title: **CPU(EDP SIDEBAND/GPIO/DDI)**

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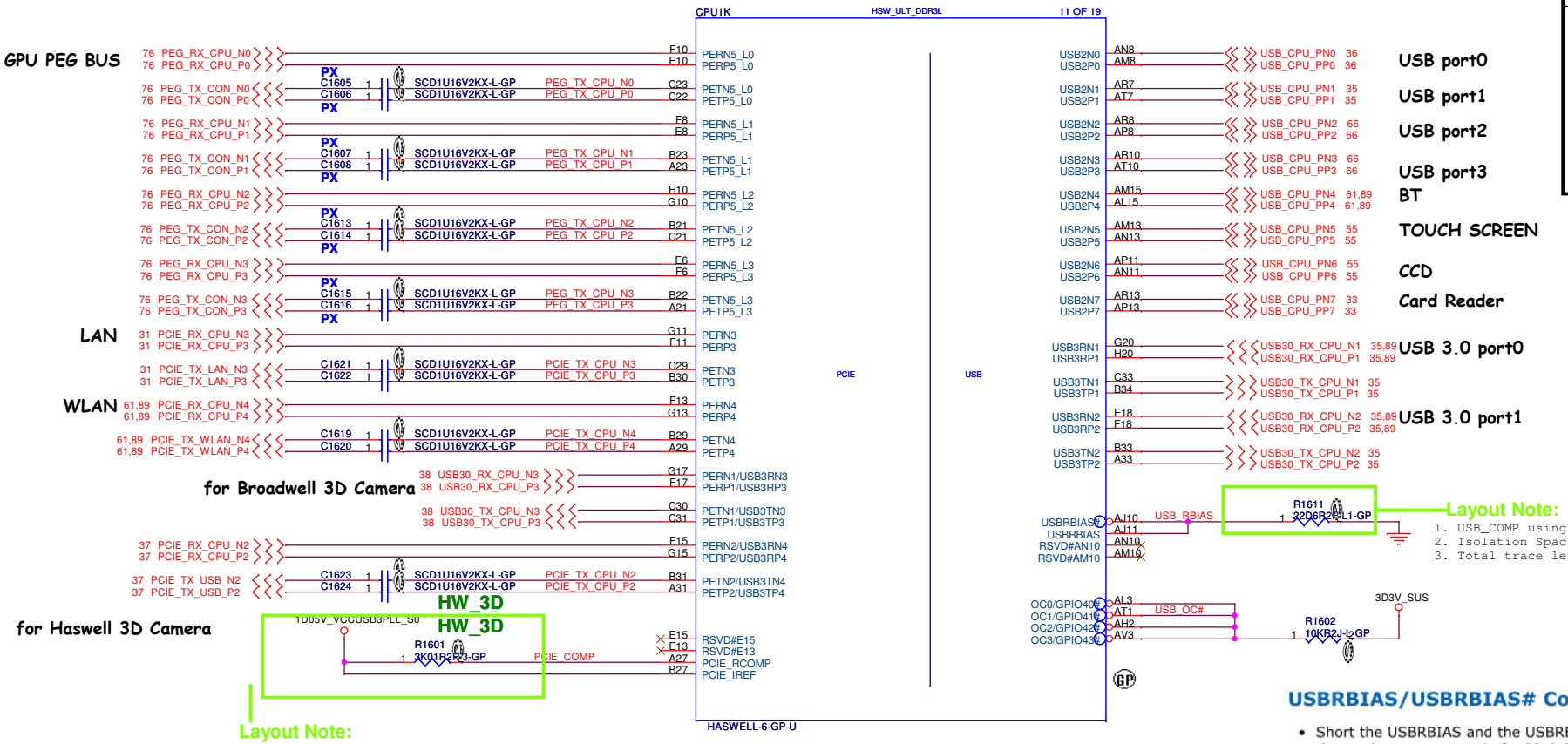

USB Table

Pair	Device
0	USB3.0 Port0
1	USB3.0 Port1
2	USB3.0 Port2
3	USB3.0 Port3
4	BT
5	TOUCH SCREEN
6	CCD
7	Card Reader

Layout Note:

1. USB_COMP using 50 ohm single-ended impedance
2. Isolation Spacing :15mil
3. Total trace length<500mil

Layout Note:

1. PCIE_RCOMP/ PCIE_IREF trace width=12~15mil
2. Isolation Spacing: 12mil
3. Total trace length<500mil

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
PCIE_RCOMP	4 mils min (breakout) 12-15 mils (trace) **Note:** Must maintain low DC resistance routing (<0.2 ohm).	At least 12 mils to any adjacent high speed I/O.	3k ohm ±1% pulled to VCCUSB3PLL.	Max total = 500 mils
PCIE_IREF	4 mils min (breakout) 12-15 mils (trace) **Note:** Must maintain low DC resistance routing (<0.2 ohm).	At least 12 mils to any adjacent high speed I/O.	No resistor. Must connect directly to VCCUSB3PLL.	Max total = 500 mils

USBRBIAS/USBRBIAS# Connection Guidelines

- Short the USBRBIAS and the USBRBIAS# pins at the package and then route on the top layer to one end of a 22.6 Ω ±1% resistor to ground (see Figure 15-2).
- Route signal using 50 ohm single-ended impedance and 500 mils (12.7-mm) max trace length and no longer than 450 mils to resistor.
- Avoid routing next to clock pins or under stitching capacitors. Recommended minimum spacing to other signal traces is 15 mils (0.381 mm).

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
PCIE_RCOMP	4 mils min (breakout) 12-15 mils (trace) **Note:** Must maintain low DC resistance routing (<0.2 ohm).	At least 12 mils to any adjacent high speed I/O.	3k ohm ±1% pulled to VCCUSB3PLL.	Max total = 500 mils
PCIE_IREF	4 mils min (breakout) 12-15 mils (trace) **Note:** Must maintain low DC resistance routing (<0.2 ohm).	At least 12 mils to any adjacent high speed I/O.	No resistor. Must connect directly to VCCUSB3PLL.	Max total = 500 mils

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Title: **CPU (PCI/USB)**

Size: A3 | Document Number: **Brook_BH** | Rev: **-1M**

Date: Wednesday, February 04, 2015 | Sheet 16 of 106

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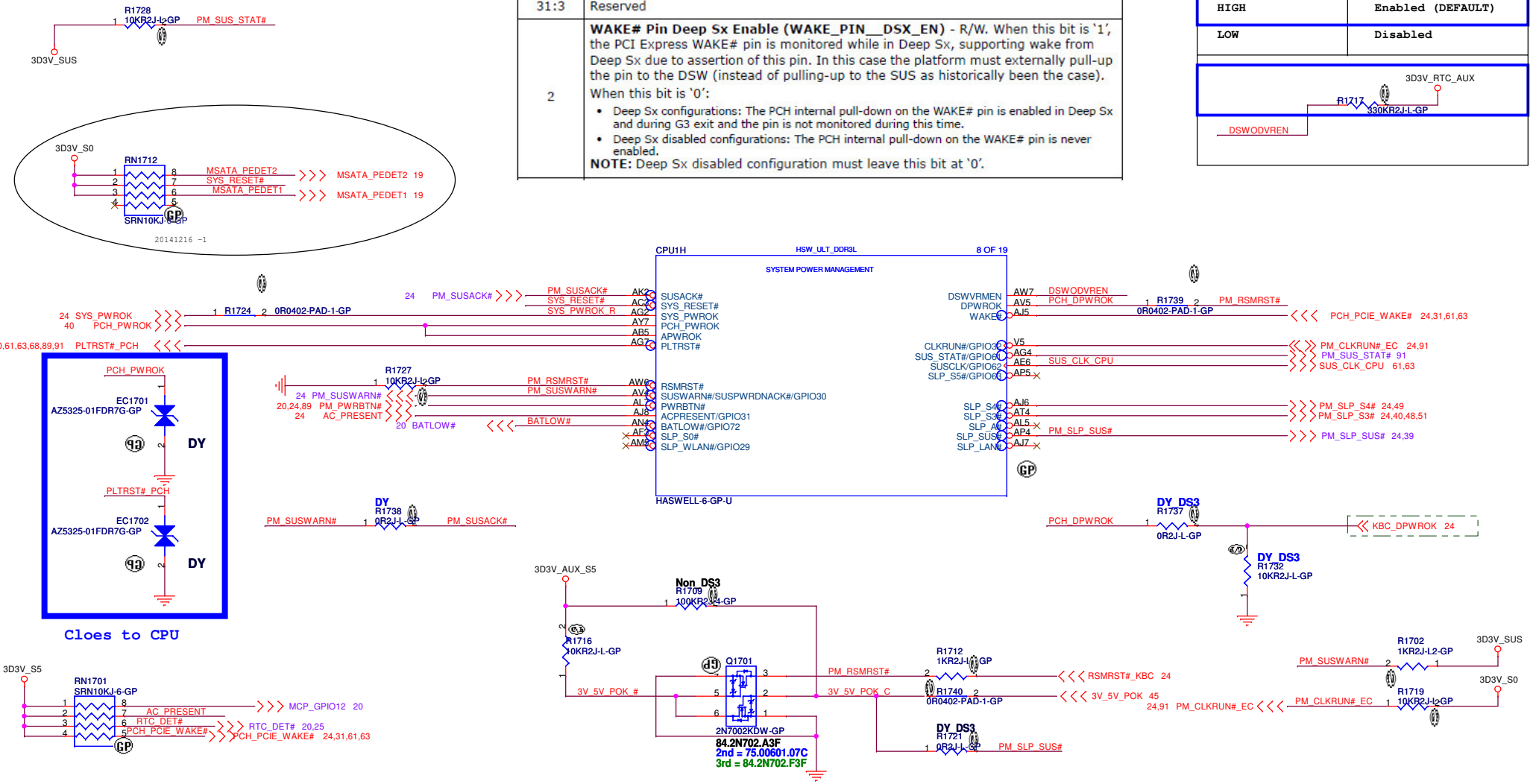
Bit	Description
31:3	Reserved
2	**WAKE# Pin Deep Sx Enable (WAKE_PIN___DSX_EN)** - R/W. When this bit is '1', the PCI Express WAKE# pin is monitored while in Deep Sx, supporting wake from Deep Sx due to assertion of this pin. In this case the platform must externally pull-up the pin to the DSW (instead of pulling-up to the SUS as historically been the case). When this bit is '0': • Deep Sx configurations: The PCH internal pull-down on the WAKE# pin is enabled in Deep Sx and during G3 exit and the pin is not monitored during this time. • Deep Sx disabled configurations: The PCH internal pull-down on the WAKE# pin is never enabled. **NOTE:** Deep Sx disabled configuration must leave this bit at '0'.

DSWODVREN – On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled



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Title: **CPU (DMI/FDI/PM)**

Size	Document Number	Rev
A3	Brook_BH	-1M

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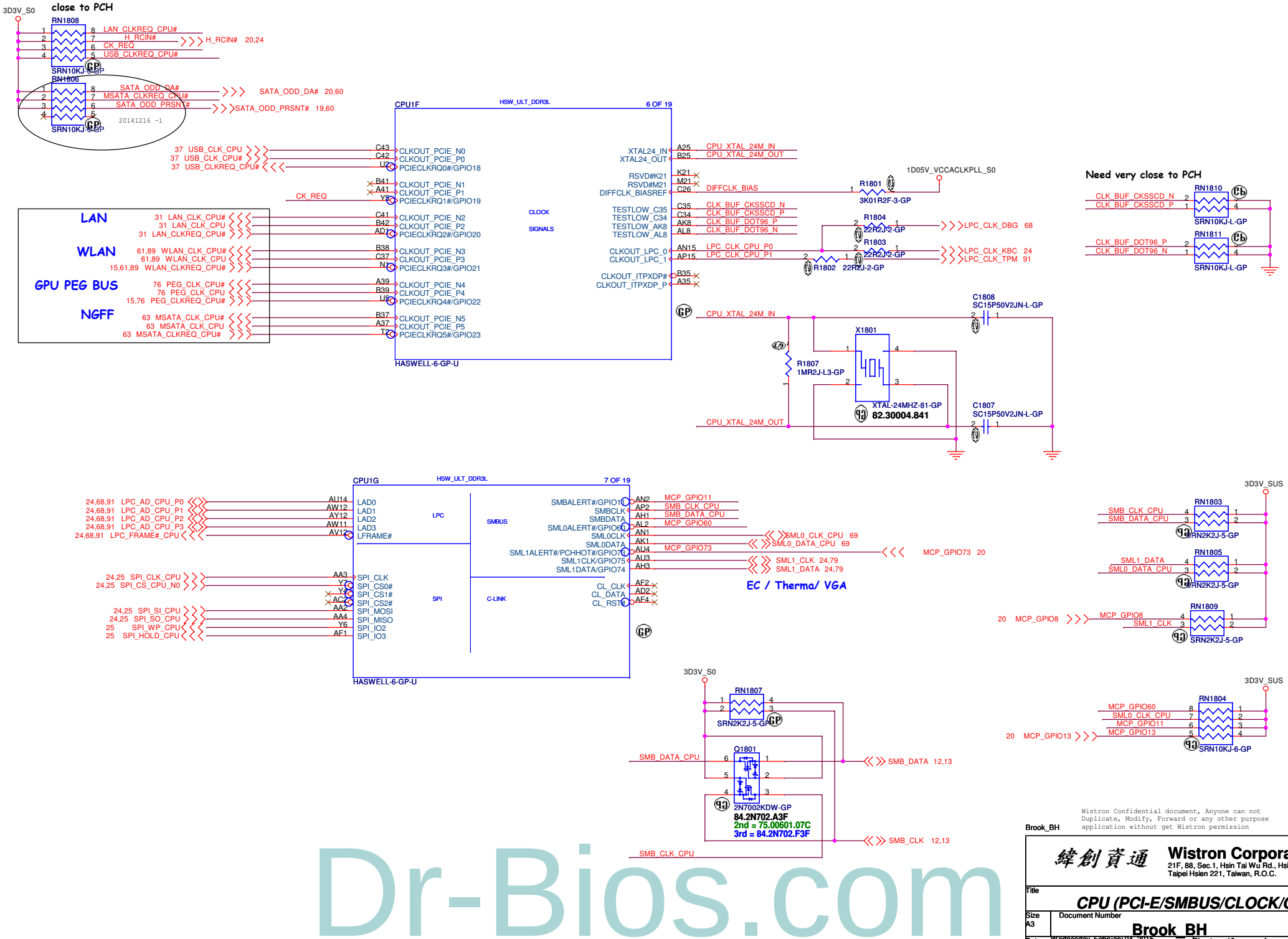

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Title: CPU (PCI-E/SMBUS/CLOCK/CL)

Size	Document Number	Rev
A3	Brook_BH	-1M

Date: Wednesday, February 04, 2015 Sheet 18 of 106

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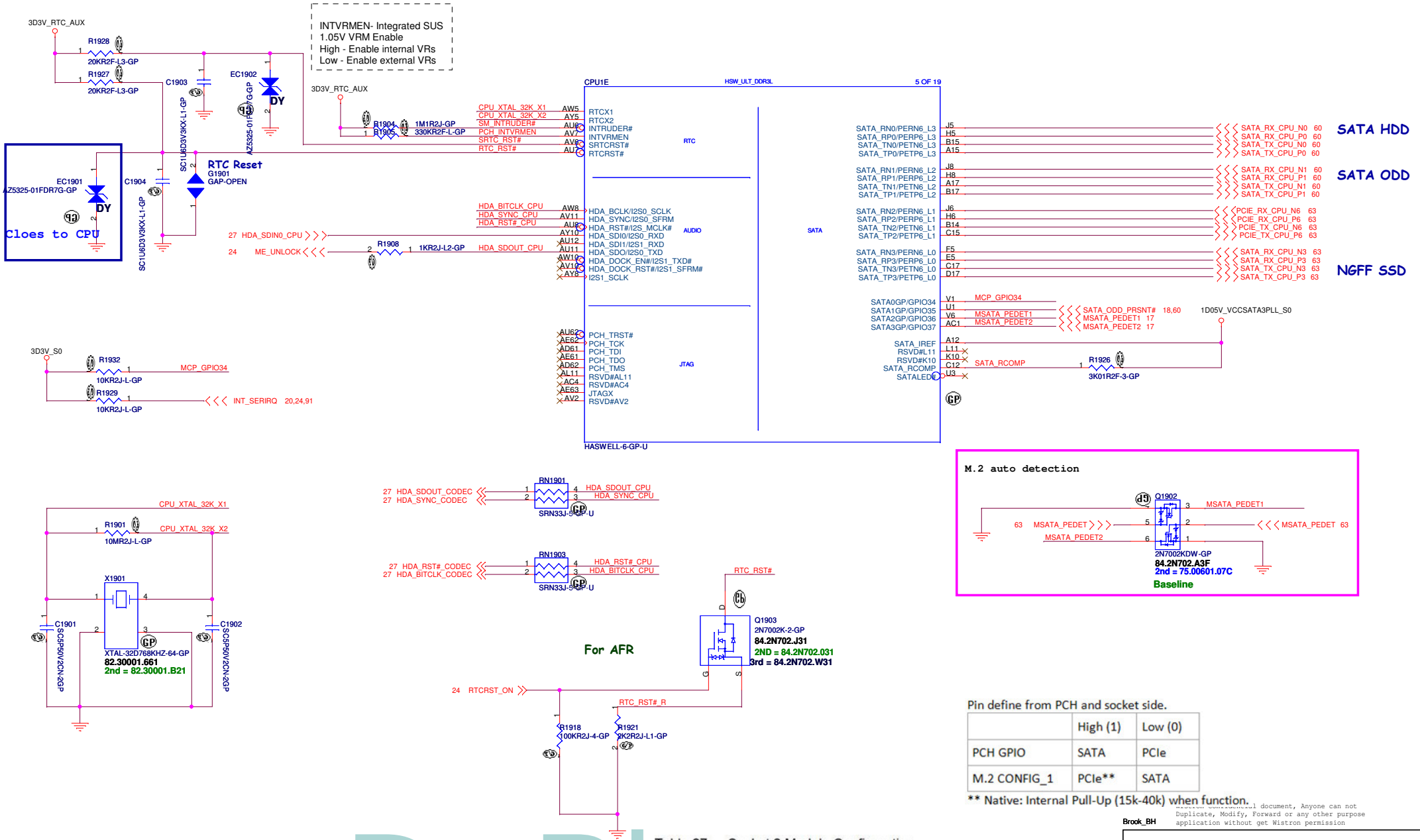

Pin define from PCH and socket side.

	High (1)	Low (0)
PCH GPIO	SATA	PCIe
M.2 CONFIG_1	PCIe**	SATA

** Native: Internal Pull-Up (15k-40k) when function.

Table 27. Socket 2 Module Configuration

State #	Module Configuration Decodes CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75	CONFIG_3 (Pin 1)	Module Type and Main Host Interface[1]	Port Configuration[2]
0	GND	GND	GND	GND	SSD – SATA	N/A
1	GND	N/C	GND	GND	SSD – PCIe	N/A

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Title: CPU (RTC/LPC/SATA/HDA)

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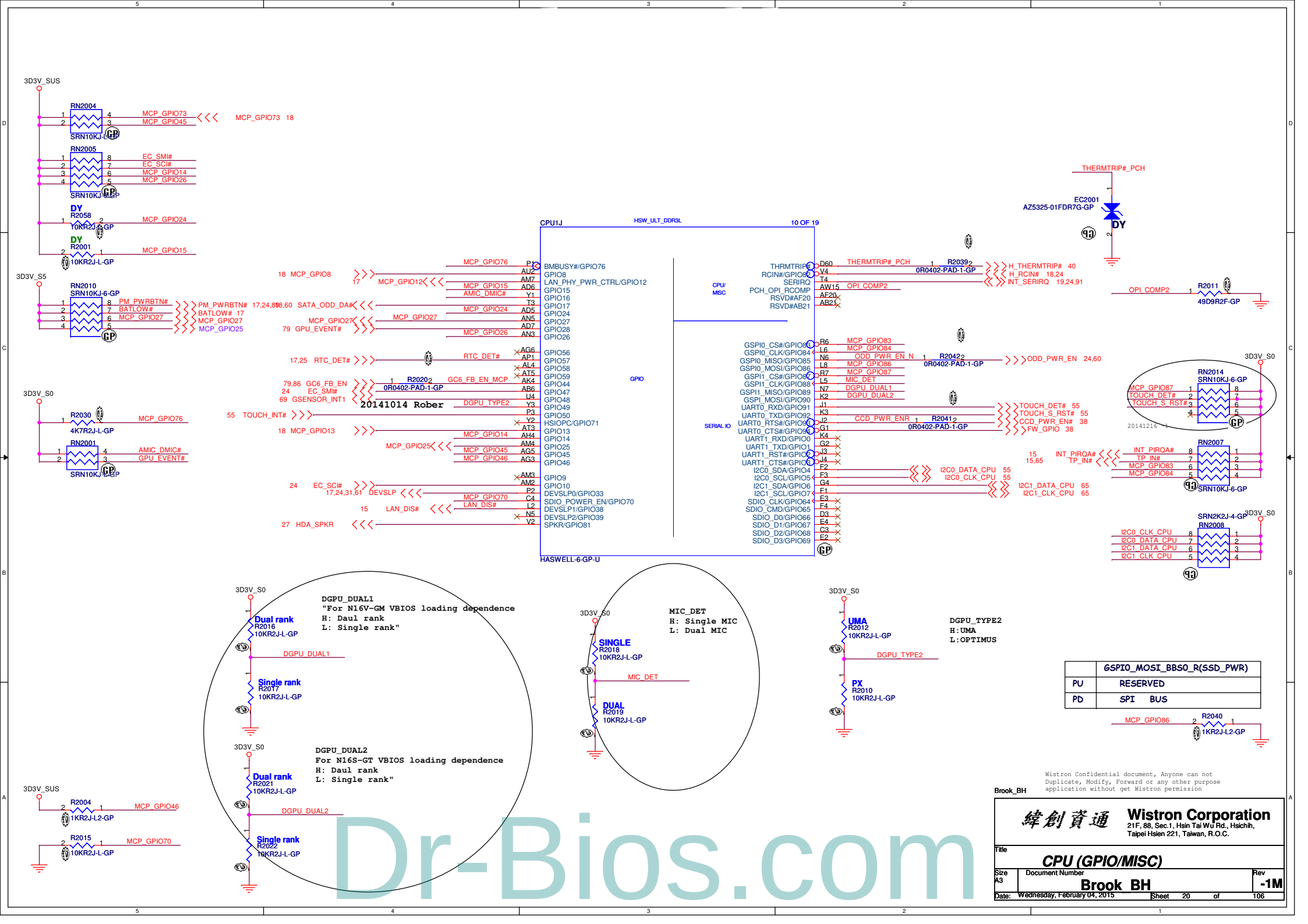
3D3V_SUS
RN2004
MCP_GPIO73
MCP_GPIO45
SRN10KJ-L-GP
RN2005
EC_SMI#
EC_SCI#
MCP_GPIO14
MCP_GPIO26
DY
R2058
MCP_GPIO24
R2001
MCP_GPIO15
3D3V_S5
RN2010
SRN10KJ-6-GP
PM_PWRBTN#
BATLOW#
MCP_GPIO27
MCP_GPIO25
3D3V_S0
R2030
4K7R2J-L-GP
MCP_GPIO76
RN2001
AMIC_DMIC#
GPU_EVENT#
CPU1J
HSW_ULT_DDR3L
10 OF 19
BMBUSY#/GPIO76
GPIO8
LAN_PHY_PWR_CTRL/GPIO12
GPIO15
GPIO16
GPIO17
GPIO24
GPIO27
GPIO28
GPIO26
GPIO56
GPIO57
GPIO58
GPIO59
GPIO44
GPIO47
GPIO48
GPIO49
GPIO50
HSIOPC/GPIO71
GPIO13
GPIO14
GPIO25
GPIO45
GPIO46
GPIO9
GPIO10
DEVSLP0/GPIO33
SDIO_POWER_EN/GPIO70
DEVSLP1/GPIO38
DEVSLP2/GPIO39
SPKR/GPIO81
GPIO
CPU MISC
SERIAL IO
THERMTRIP#
RCIN#/GPIO82
SERIRQ
PCH_OPI_RCOMP
RSVD#AF20
RSVD#AB21
GSPI0_CS#/GPIO83
GSPI0_CLK/GPIO84
GSPI0_MISO/GPIO85
GSPI0_MOSI/GPIO86
GSPI1_CS#/GPIO87
GSPI1_CLK/GPIO88
GSPI1_MISO/GPIO89
GSPI_MOSI/GPIO90
UART0_RXD/GPIO91
UART0_TXD/GPIO92
UART0_RTS#/GPIO93
UART0_CTS#/GPIO94
UART1_RXD/GPIO0
UART1_TXD/GPIO1
UART1_RST#/GPIO2
UART1_CTS#/GPIO3
I2C0_SDA/GPIO4
I2C0_SCL/GPIO5
I2C1_SDA/GPIO6
I2C1_SCL/GPIO7
SDIO_CLK/GPIO64
SDIO_CMD/GPIO65
SDIO_D0/GPIO66
SDIO_D1/GPIO67
SDIO_D2/GPIO68
SDIO_D3/GPIO69
HASWELL-6-GP-U
THERMTRIP#_PCH
EC2001
AZ5325-01FDR7G-GP
R2039
0R0402-PAD-1-GP
H_THERMTRIP# 40
H_RCIN# 18,24
INT_SERIRQ 19,24,91
OPI_COMP2
R2011
49D9R2F-GP
ODD_PWR_EN_N
R2042
ODD_PWR_EN 24,60
CCD_PWR_ENR
R2041
FW_GPIO 38
TOUCH_DET# 55
TOUCH_S_RST# 55
CCD_PWR_EN# 38
I2C0_DATA_CPU 55
I2C0_CLK_CPU 55
I2C1_DATA_CPU 65
I2C1_CLK_CPU 65
RN2014
SRN10KJ-6-GP
RN2007
SRN10KJ-6-GP
SRN2K2J-4-GP
RN2008
DGPU_DUAL1
"For N16V-GM VBIOS loading dependence
H: Daul rank
L: Single rank"
Dual rank
R2016
10KR2J-L-GP
DGPU_DUAL1
Single rank
R2017
10KR2J-L-GP
DGPU_DUAL2
For N16S-GT VBIOS loading dependence
H: Daul rank
L: Single rank"
Dual rank
R2021
10KR2J-L-GP
DGPU_DUAL2
Single rank
R2022
10KR2J-L-GP
MIC_DET
H: Single MIC
L: Dual MIC
SINGLE
R2018
10KR2J-L-GP
MIC_DET
DUAL
R2019
10KR2J-L-GP
DGPU_TYPE2
H:UMA
L:OPTIMUS
UMA
R2012
10KR2J-L-GP
DGPU_TYPE2
PX
R2010
10KR2J-L-GP
GSPIO_MOSI_BBSO_R(SSD_PWR)
PU RESERVED
PD SPI BUS
R2040
1KR2J-L2-GP
R2004
1KR2J-L2-GP
R2015
10KR2J-L-GP
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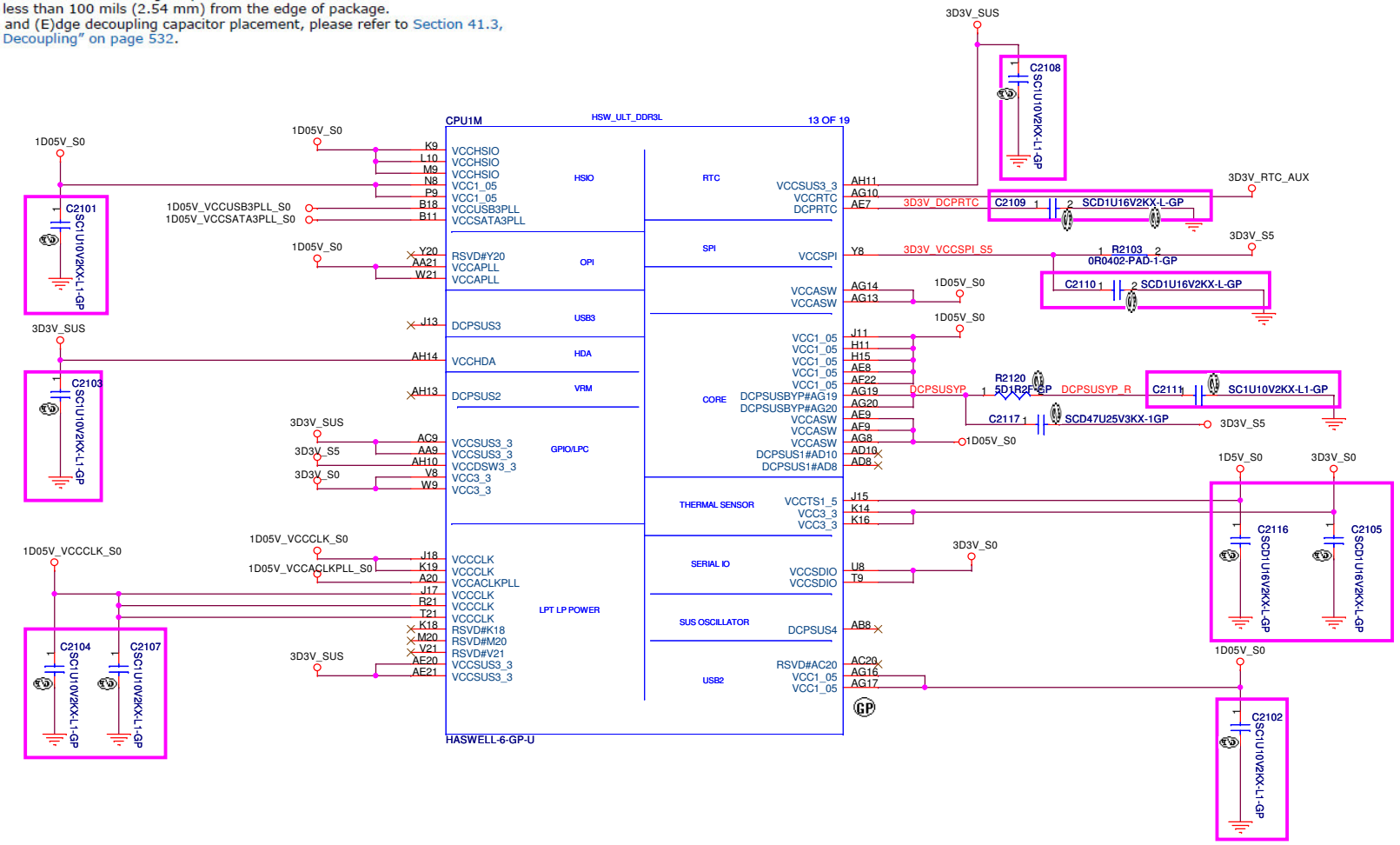
Notes:

1. Required only on external SUS.
2. Placeholder only. Does not need to be stuffed.
3. The following pins are not to be connected and be left floating. Test point is optional on these pins: AC20, Y20, K18, M20, V21.
4. Note that some decoupling capacitors are shared between more than 1 rail. Follow the "Place capacitors near balls" instructions above to ensure this sharing is optimized.
5. Capacitors should be placed less than 100 mils (2.54 mm) from the edge of package.
6. For description of (R)unway, and (E)dge decoupling capacitor placement, please refer to Section 41.3, "Loop Inductance Reduction Decoupling" on page 532.



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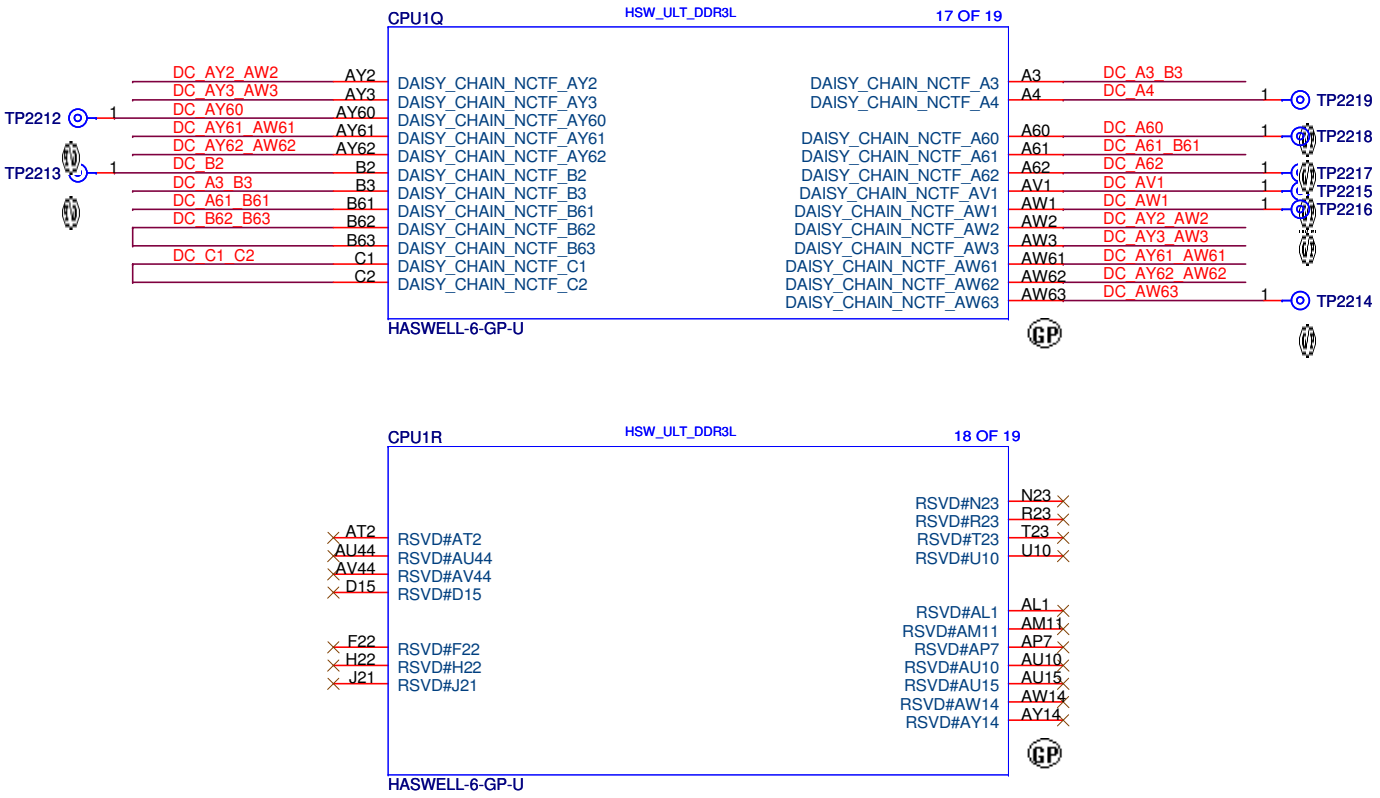

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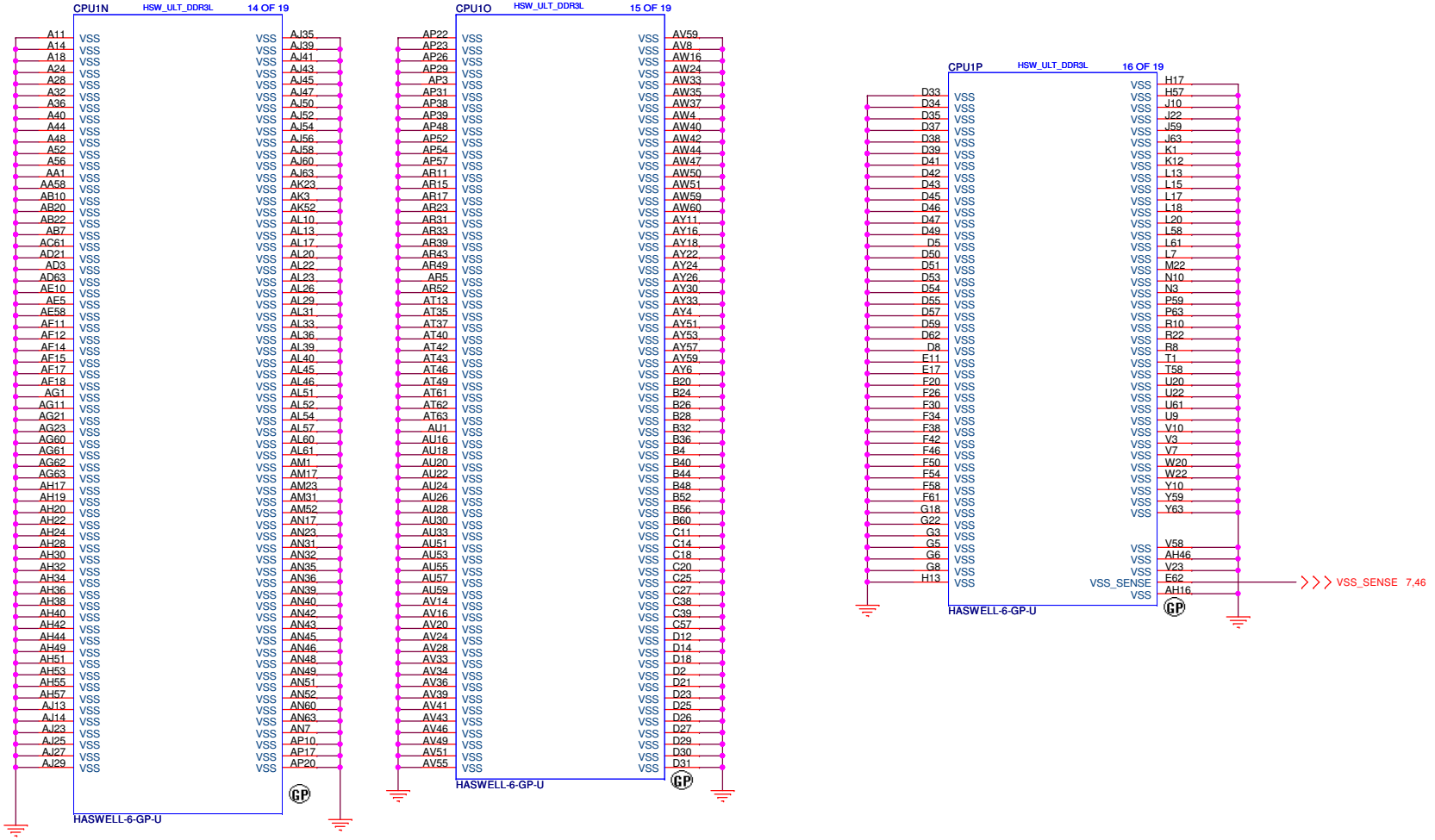

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SSID = KBC

VCC_LPC(Pin9)

Close to the EC

11/18 RN7904 to RN2404

OPMODE (Pin70)

LPC

GPIO0 High Active

2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031
3rd = 84.2N702.W31

Rober change 11/17

20141014 Rober

< ---CPU/GPU
< ---BATTER /CHARGER
< ---Touch Pad

MODEL_ID

MODEL_ID_AD	Pull-Low Register	Pull-High Register	Typical Voltage
Brook_H_UMA/Brook_SL_UMA	100.0 K	10.0 K	3.000 V
Brook_H_DIS/Brook_SL_DIS	100.0 K	20.0 K	2.750 V
Brook_B_UMA	100.0 K	33.0 K	2.481 V
Brook_B_DIS	100.0 K	47.0 K	2.245 V
Reserved for project use	100.0 K	64.9 K	2.001 V
Reserved for project use	100.0 K	76.8 K	1.867 V
Reserved for project use	100.0 K	100.0 K	1.650 V
Reserved for project use	100.0 K	143.0 K	1.358 V
Reserved for project use	100.0 K	174.0 K	1.204 V
Reserved for project use	100.0 K	215.0 K	1.048 V

ADT_TYPE_AD

ADT_TYPE_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	
65W	N/A	100.0 K	3.300 V		>= 3.000 V	
90W	100.0 K	N/A	0.000 V			< 0.150 V
30W	10.0 K	100.0 K	0.300 V	0.305 V	>= 0.150 V	< 0.425 V
45W	20.0 K	100.0 K	0.550 V	0.559 V	>= 0.425 V	< 0.684 V
120W	33.0 K	100.0 K	0.819 V	0.831 V	>= 0.684 V	< 0.937 V
135W	47.0 K	100.0 K	1.055 V	1.070 V	>= 0.937 V	< 1.177 V
150W	64.9 K	100.0 K	1.299 V	1.315 V	>= 1.177 V	< 1.366 V
Reserved	76.8 K	100.0 K	1.433 V	1.450 V	>= 1.366 V	< 1.542 V
Reserved	100.0 K	100.0 K	1.650 V	1.667 V	>= 1.542 V	< 1.842 V

PCB_VER_AD

PCB_VER_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	
SA	100.0 K	10.0 K	3.000 V	3.005 V	>= 2.875 V	
SB	100.0 K	20.0 K	2.750 V	2.759 V	>= 2.616 V	< 2.875 V
SC	100.0 K	33.0 K	2.481 V	2.493 V	>= 2.363 V	< 2.616 V
-1	100.0 K	47.0 K	2.245 V	2.259 V	>= 2.123 V	< 2.363 V
Reserved for project use	100.0 K	64.9 K	2.001 V	2.017 V	>= 1.934 V	< 2.123 V
Reserved for project use	100.0 K	76.8 K	1.867 V	1.883 V	>= 1.758 V	< 1.934 V
Reserved for project use	100.0 K	100.0 K	1.650 V	1.667 V	>= 1.504 V	< 1.758 V
Reserved for project use	100.0 K	143.0 K	1.358 V	1.374 V	>= 1.281 V	< 1.504 V
Reserved for project use	100.0 K	174.0 K	1.204 V	1.220 V	>= 1.126 V	< 1.281 V
Reserved for project use	100.0 K	215.0 K	1.048 V	1.062 V	>= 0.524 V	< 1.126 V

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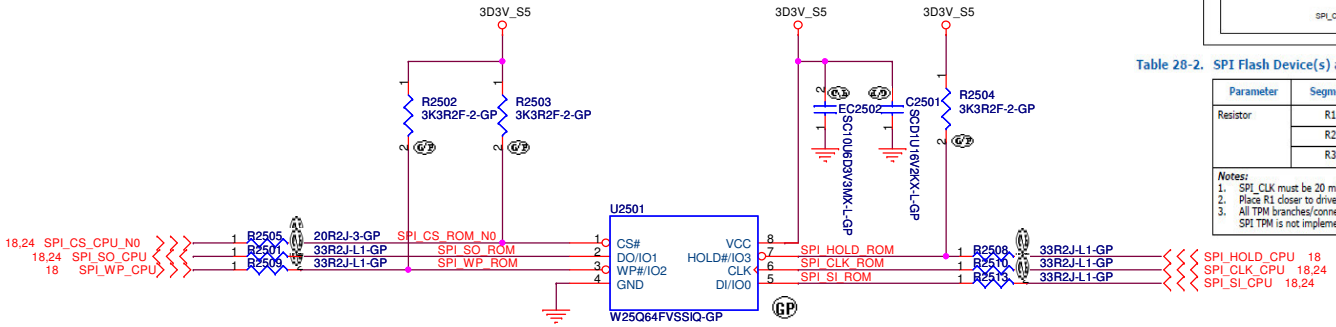
SSID = Flash.ROM

SPI FLASH ROM (8M byte) for PCH

SPI ROM Equal length need to less than 500mil

SPI FLASH ROM (8M byte)
1ST= 072.02564.0001(AMIC A25LQ64M)
2ND=072.25B64.0001(Gigadevice GD25B64BSIGR)

purge=72.25Q64.K01 (WINBOND W25Q64FVSSIQ)
72.25647.00A (MXIC MX25L6473EM2I)



72.25Q64.K01
2nd = 072.25B64.0001
3rd = 72.25Q64.R01

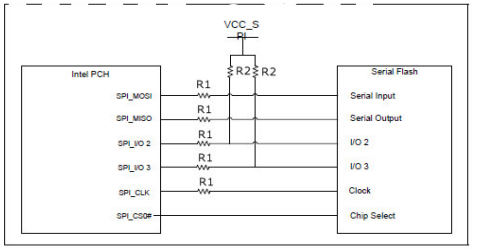
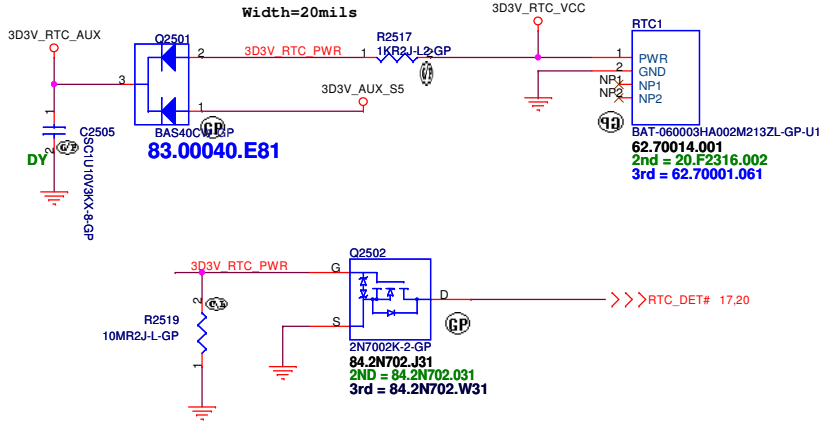


Table 28-2. SPI Flash Device(s) and TPM Routing Guideline (Sheet 2 of 2)

Parameter	Segment	Stackup	Unit	Routing Recommendation
Resistor	R1		ohm	15
	R2		ohm	1k
	R3		ohm	33

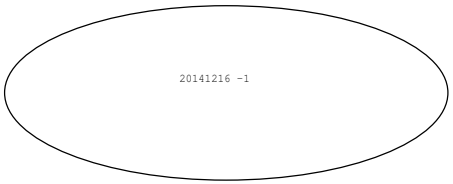
Notes:
1. SPI_CLK must be 20 mils spacing from any other high frequency (>1 GHz) signal.
2. Place R1 closer to driver side to effectively damping the undershoot and overshoot.
3. All TPM branches/connections (TPM_MOSI, TPM_MISO, TPM_CLK, and PCH_CS2#) can be left as NC if SPI TPM is not implemented.

SSID = RBAT



83.00040.E81
62.70014.001
2nd = 20.F2316.002
3rd = 62.70001.061

84.2N702.J31
2ND = 84.2N702.031
3rd = 84.2N702.W31



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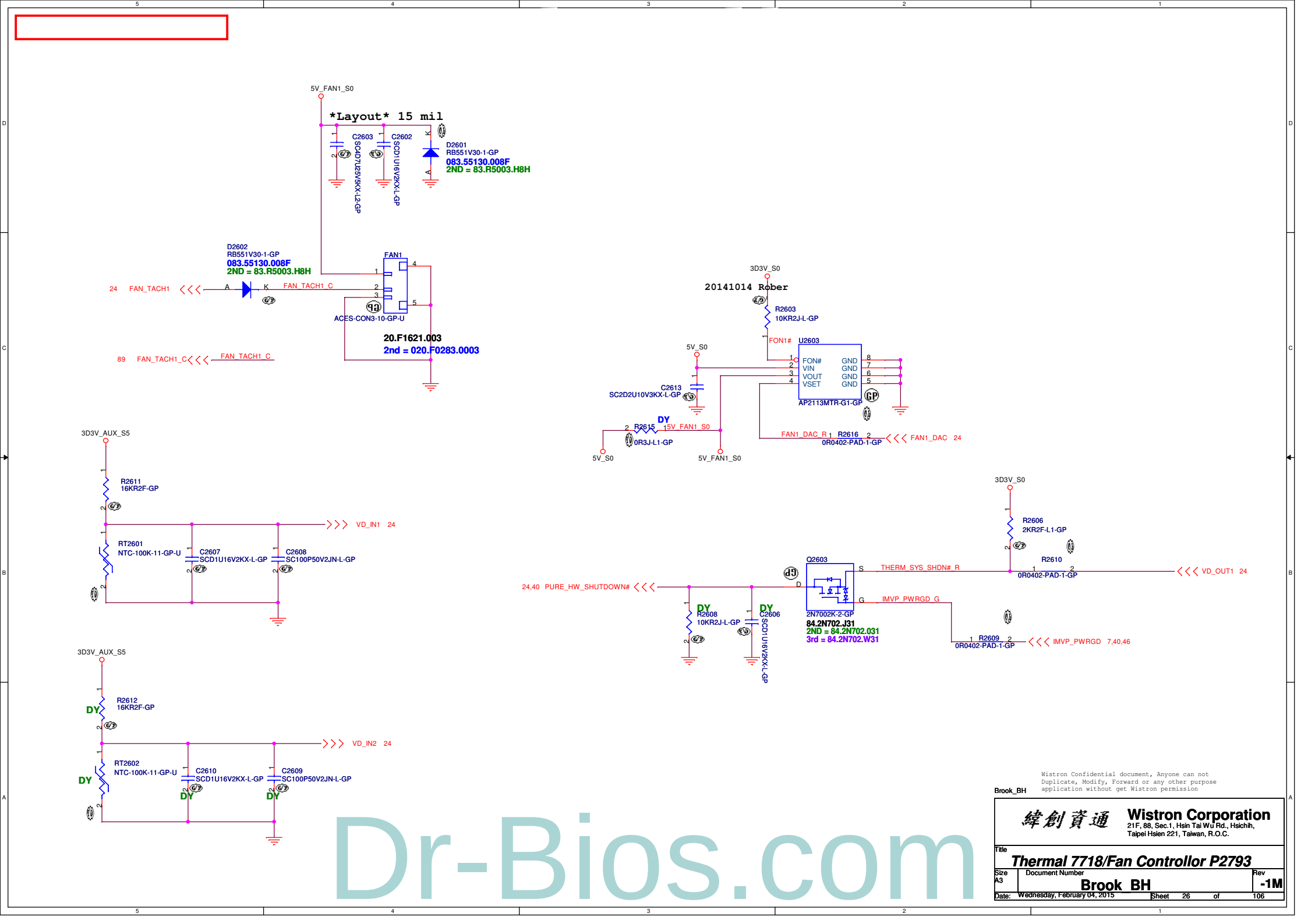

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SSID = AUDIO

AUD_AGND close to codec IC

placed nearby codec PIN12

Close to Pin46

Close to Pin41

Close pin36

Close pin40

Close to Pin1

Close to LOUT1

Close to LOUT1

Layout Note:
Place close to Pin 26

Layout Note:
Place close to Pin 13

Layout Note:

R2708 is need to connect.To prvent the beep sound

071.00255.0003

ALC255-CG-GP-U

Width>40mil, to improve Headpohone Crosstalk noise
Change it to sharp will be better.
Add 2 vias (>0.5A) when trace layer change.

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SSID = AUDIO

Speaker

27 AUD_SPK_L- EL2914 BLM15PX121SN1D-GP AUD_SPK1_L-_CON
27 AUD_SPK_L+ EL2915 BLM15PX121SN1D-GP AUD_SPK1_L+_CON
27 AUD_SPK_R- EL2916 BLM15PX121SN1D-GP AUD_SPK1_R-_CON
27 AUD_SPK_R+ EL2917 BLM15PX121SN1D-GP AUD_SPK1_R+_CON

EC2901 SC1KP50V2KX-L-1-GP
EC2902 SC1KP50V2KX-L-1-GP
EC2915 SC1KP50V2KX-L-1-GP
EC2920 SC1KP50V2KX-L-1-GP

SPK
AUD_SPK1_L-_CON
AUD_SPK1_L+_CON
AUD_SPK1_R-_CON
AUD_SPK1_R+_CON
ES-CON4-17-GP-U1

20.F1621.004
2nd = 020.F0155.0004

Layout Note:
Trace width=40mil

AUD_SPK1_L-_CON AUD_SPK1_L-_CON 89
AUD_SPK1_L+_CON AUD_SPK1_L+_CON 89
AUD_SPK1_R-_CON AUD_SPK1_R-_CON 89
AUD_SPK1_R+_CON AUD_SPK1_R+_CON 89

AFTP TESTPOINT

Combo Jack

R2910 0R0402-PAD-1-GP
AUD_HP1_JD#_R
Q2901
C2902
R2901 100KR2J-4-GP
2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031
SC10U6D3V3MX-L-GP
AUD_AGND
AUD_HP1_JD# 27

3D3V_S0
R2905 10KR2J-L-GP
AUD_HP1_JD#_TYPE
R2906 0R0402-PAD-1-GP
AUD_AGND
AUD_HP1_JD#_TYPE 89

0527_SB

27 RING2 AUD_HP1_JACK_L2 R2920 0R0402-PAD-1-GP ER2913 33D4R3F-GP
27 AUD_HP1_JACK_R2 SELEEVE R2921 0R0402-PAD-1-GP ER2912 33D4R3F-GP
20141216 -1

RING2_R
AUD_HP1_JD#_TYPE
AUD_HP1_JD#_R
AUD_HP1_JACK_R1
SELEEVE_R
AUD_HP1_JACK_L1
AUD1
AUDIO-JK506-GP-U
audio(IP/NK comb)
022.10002.0951

EC2923 EC2921 EC2922 EC2912 EC2913 EC2914 SC22P50V2JN-L-GP
AUD_AGND

AUD_HP1_JD#_R AUD_HP1_JD#_R 89
AUD_HP1_JACK_R1 AUD_HP1_JACK_R1 89
AUD_HP1_JACK_L1 AUD_HP1_JACK_L1 89
RING2_R RING2_R 89
SELEEVE_R SELEEVE_R 89
AUD_HP1_JD#_TYPE AUD_HP1_JD#_TYPE 89

AFTP TESTPOINT

DUAL
SINGLE
R2917 0R2J-L-GP
R2916 0R2J-L-GP
DUAL/SINGAL
DMIC_DATA_R
20141216 -1

MIC2
ENHANCE CS GND VDD DATA CLK
DMIC_DATA_CON_R
DMIC_CLK_CON_R
3D3V_S0
MICROPHONE-105-GP-U
082.40011.0001

MIC1
ENHANCE CS GND DUAL VDD DATA CLK
DMIC_DATA_R1
DMIC_CLK_CON_R1
3D3V_S0
MICROPHONE-105-GP-U
082.40011.0001

DMIC_CLK_CON_R R2909 0R0402-PAD-1-GP DMIC_CLK_CON 27
DMIC_DATA_CON_R R2911 0R0402-PAD-1-GP DMIC_DATA_CON 27
DMIC_CLK_CON_R1 0R2J-L-GP R2912 DMIC_CLK_CON
DY DY DY DUAL
EC2903 EC2904 EC2905
SC4D7P50V2BN-GP

DMIC_DATA_R
SINGLE
R2919 0R2J-L-GP

DMIC_DATA_R1 0R2J-L-GP R2913 DMIC_DATA_R
DY DUAL
EC2906
SC4D7P50V2BN-GP

DUAL MIC=082.40011.0001
SINGALE MIC=082.40011.0011
Single MIC 2nd=082.40002.0031

CLK_CON_MIC3
DATA_CON_MIC3
DY DY
EC2908 EC2907
SC4D7P50V2BN-GP

MIC3
3D3V_S0
CLK_CON_MIC3 R2914 0R0402-PAD-1-GP DMIC_CLK_CON 27
DATA_CON_MIC3 R2915 0R0402-PAD-1-GP DMIC_DATA_CON 27
PTWO-CON4-9-GP-U1
DY

11/30 SB

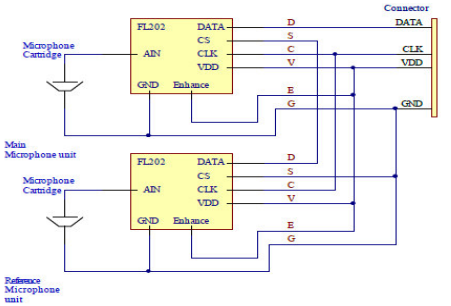

Figure 4 Schematic of NSM0410DT iSAM enhance array configuration (2 microphones array)

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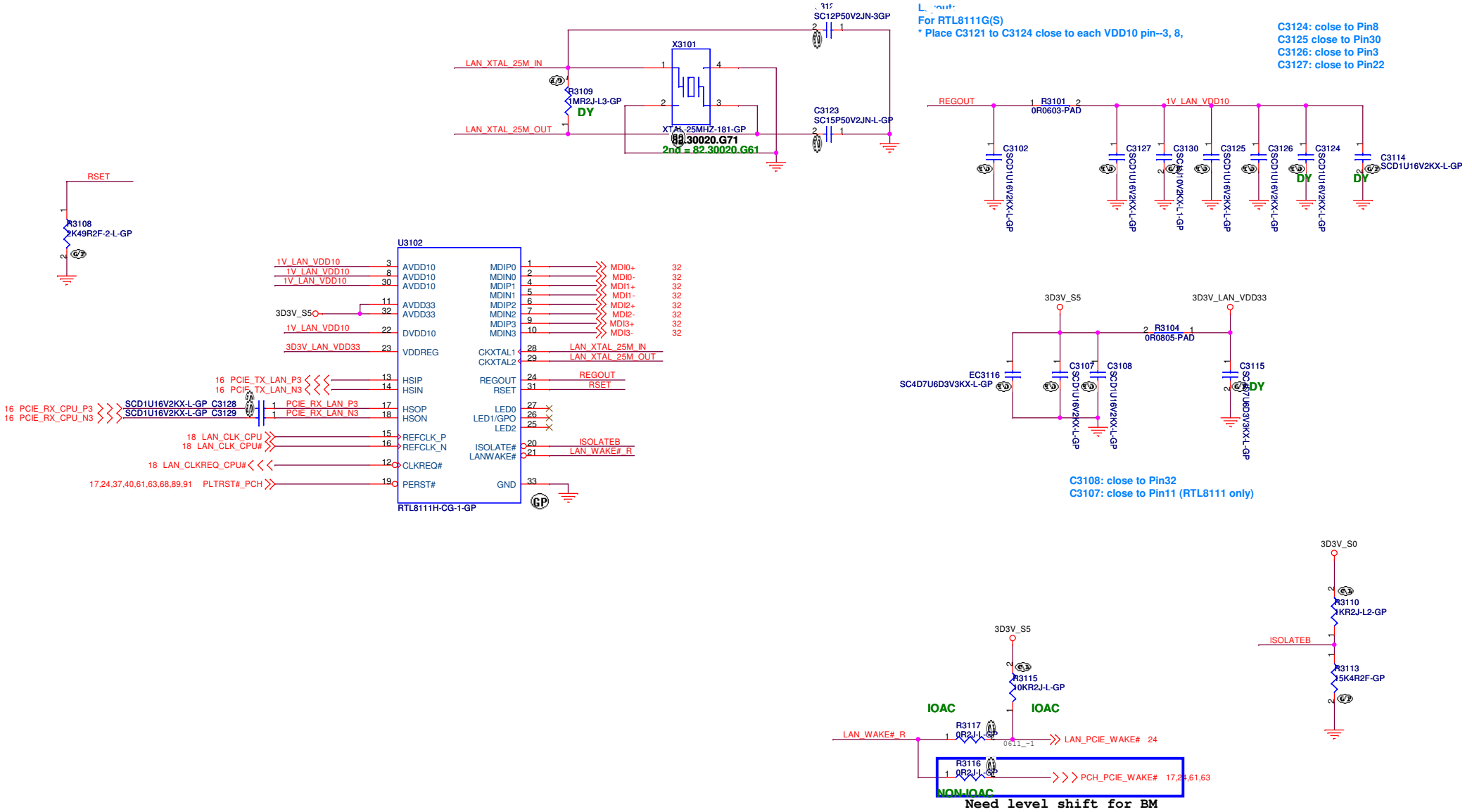

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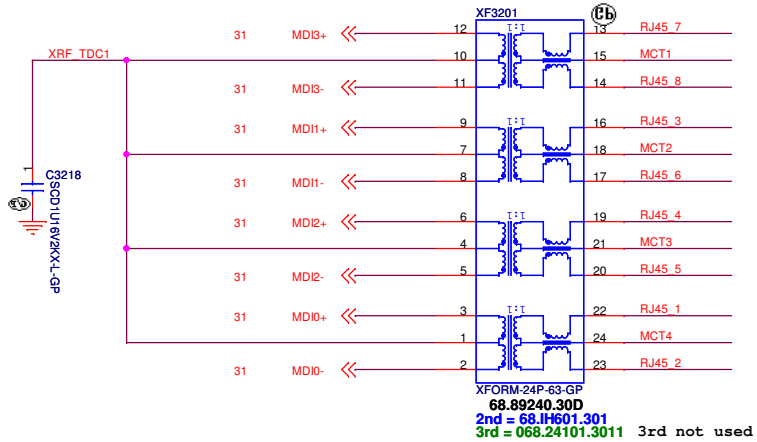
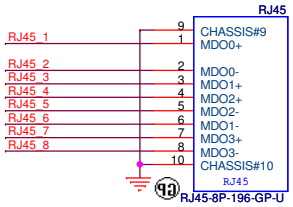
SSID = LAN



3rd not used



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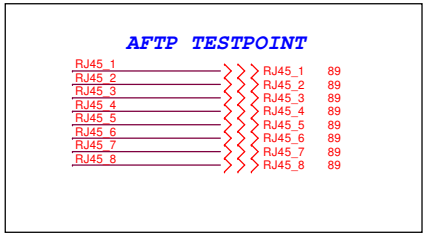

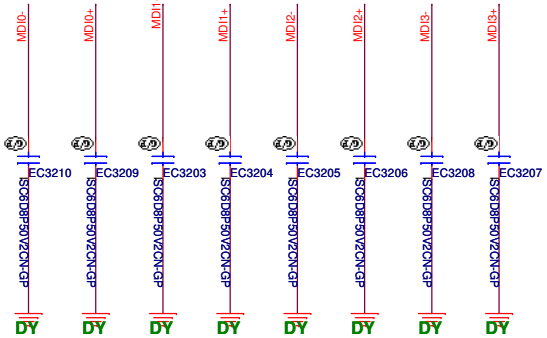

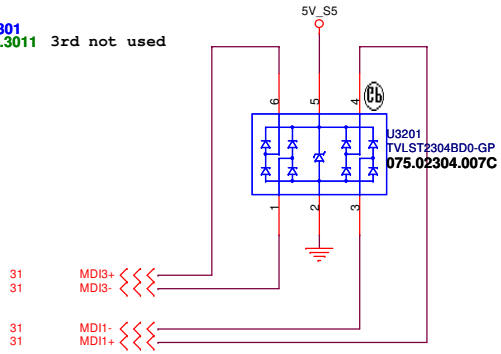

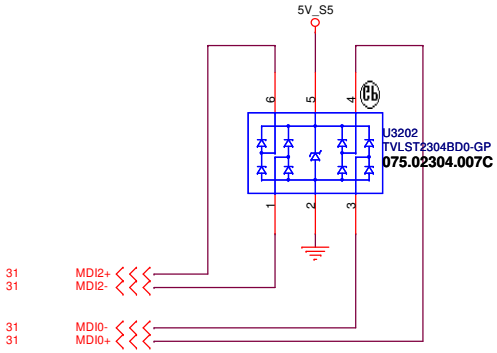

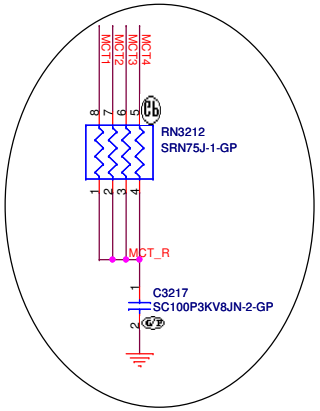

12/23 修改家電下鄉 PD

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Title: **(LAN+VGA) CONNECTOR**

Size	Document Number	Rev
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Date: Wednesday, February 04, 2015 Sheet 32 of 106

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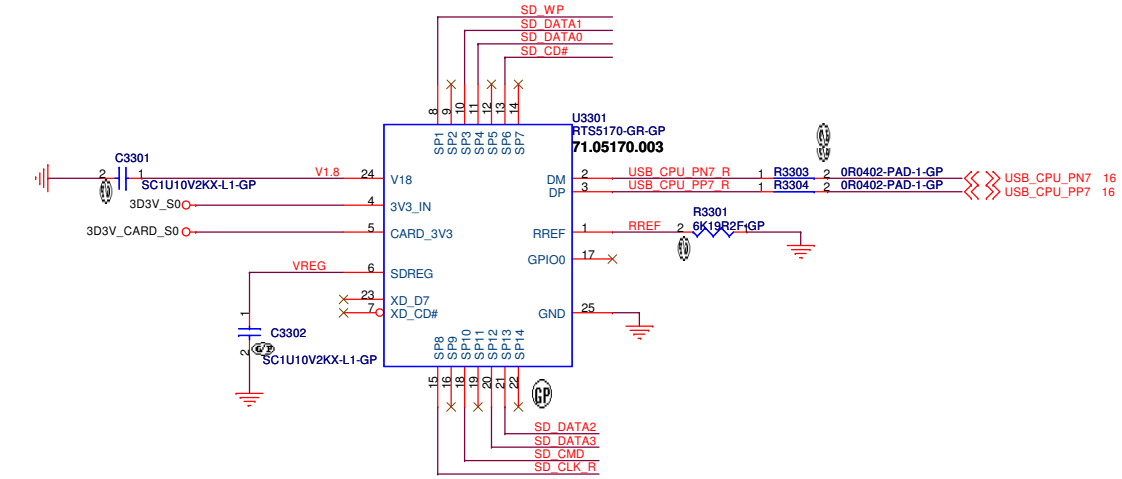

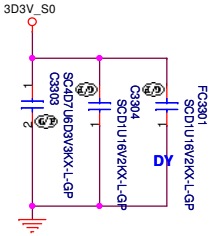

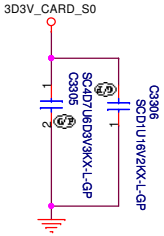

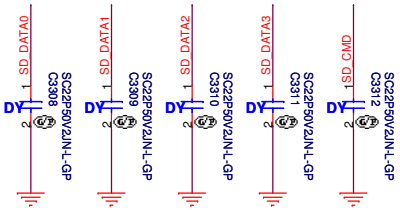

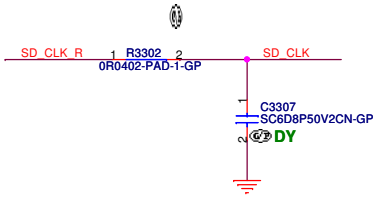

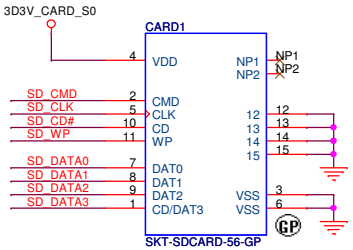

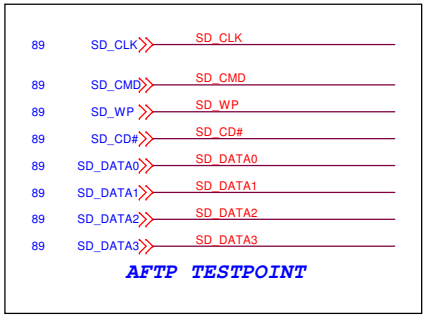

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Title: **Card Reader CONN (Reserved)**

Size	Document Number	Rev
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Date: Wednesday, February 04, 2015 Sheet 33 of 106

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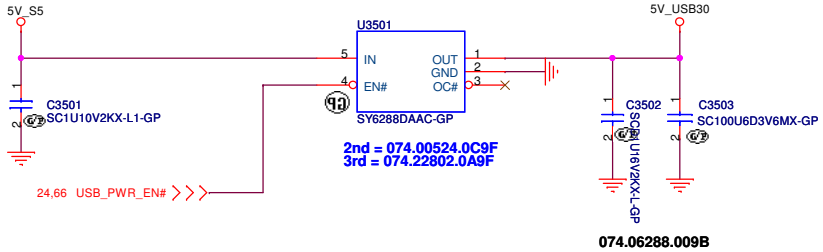
Low Active 2A



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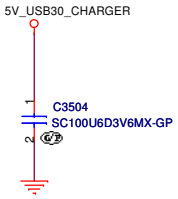
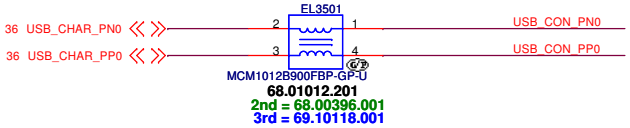


USB 3.0 Connector Pin definition		
1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	



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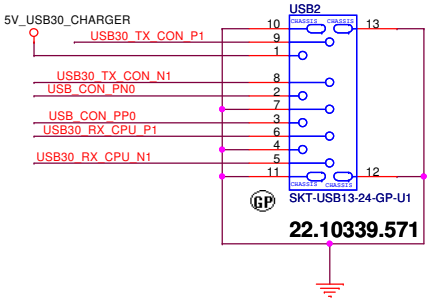

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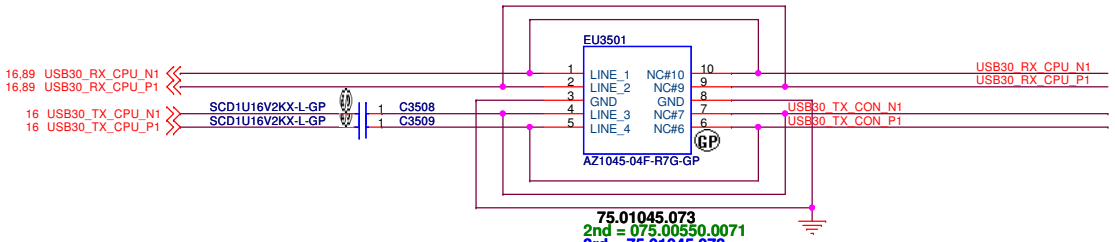

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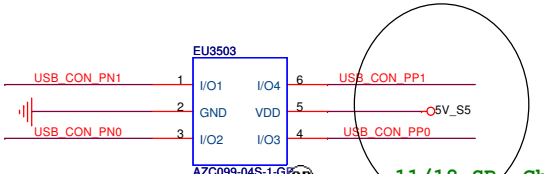

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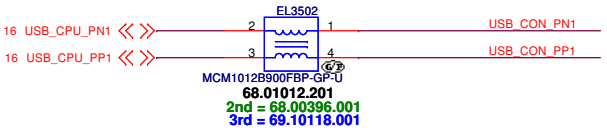
11/18 SB Change to 5V_S5

AFTP TESTPOINT

USB30_TX_CON_P1	USB30_TX_CON_P1 89
USB30_TX_CON_N1	USB30_TX_CON_N1 89
USB_CON_PN0	USB_CON_PN0 89
USB_CON_PP0	USB_CON_PP0 89
USB30_RX_CPU_P1	USB30_RX_CPU_P1 16,89
USB30_RX_CPU_N1	USB30_RX_CPU_N1 16,89
USB30_TX_CON_P2	USB30_TX_CON_P2 89
USB30_TX_CON_N2	USB30_TX_CON_N2 89
USB_CON_PN1	USB_CON_PN1 89
USB_CON_PP1	USB_CON_PP1 89
USB30_RX_CPU_P2	USB30_RX_CPU_P2 16,89
USB30_RX_CPU_N2	USB30_RX_CPU_N2 16,89



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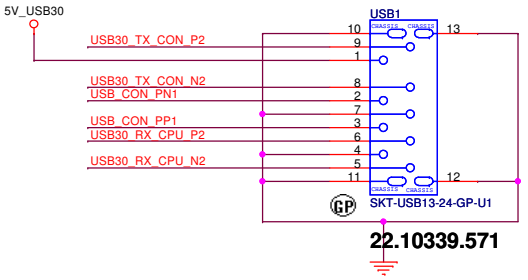

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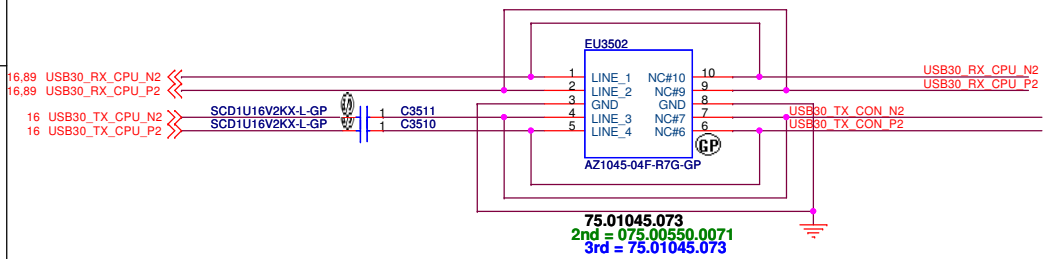

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Title: **USB_3.0**

Size	Document Number	Rev
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Date: Tuesday, February 10, 2015 Sheet 35 of 106

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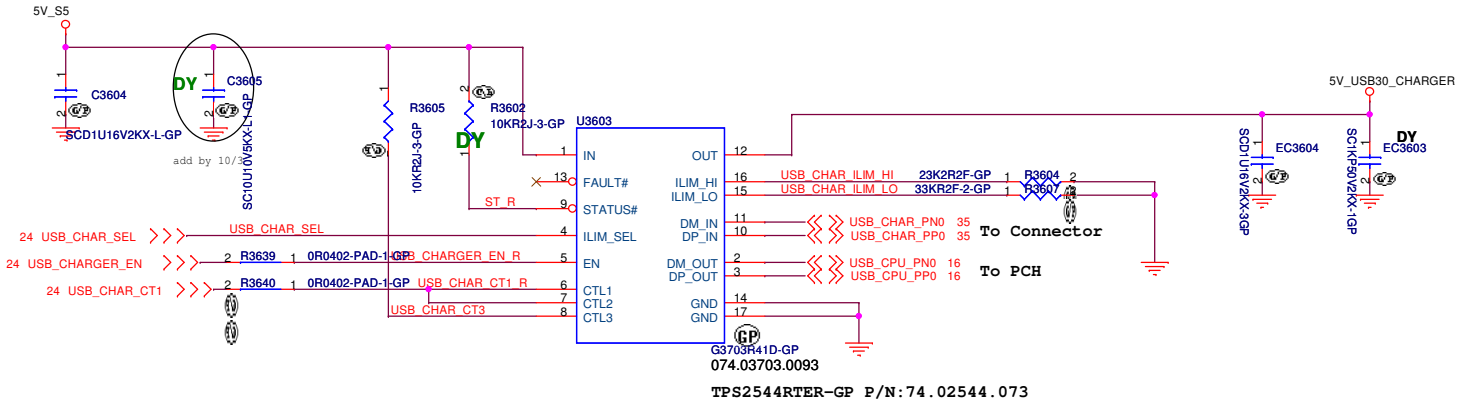

074.03703.0093

TPS2544RTER-GP P/N:74.02544.073

20150115 -1

	Device Control Pins			
Flow Line Condition	**CTL1**	**CTL2**	**CTL3**	**ILIM_SEL**
DCH	0	0	0	X
CDP	1	1	1	1
SDP2	1	1	1	0
SDP1	1	1	0	X
	0	1	0	X
DCP_SHORT	1	0	0	X
DCP_DIVIDER	1	0	1	X
DCP_Auto	0	0	1	0
	0	1	1	X

3.Electrical Safety for USB3.0 Port

2.0 A <= Measurement value <= 2.2 A : Pass

1.9 A <= Measurement value < 2.0 A or 2.2 A < Measurement value <= 2.4 A : Marginal

If this result is "Marginal", 4 more samples (Total 5 samples) must be measured for each port.

And it must be confirmed that the values of 5 samples can meet our requirement (1.9 A ~ 2.4 A).

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Title: **USB Charger**

Size: A3 | Document Number: **Brook_BH** | Rev: **-1M**

Date: Wednesday, February 04, 2015 | Sheet 36 of 106

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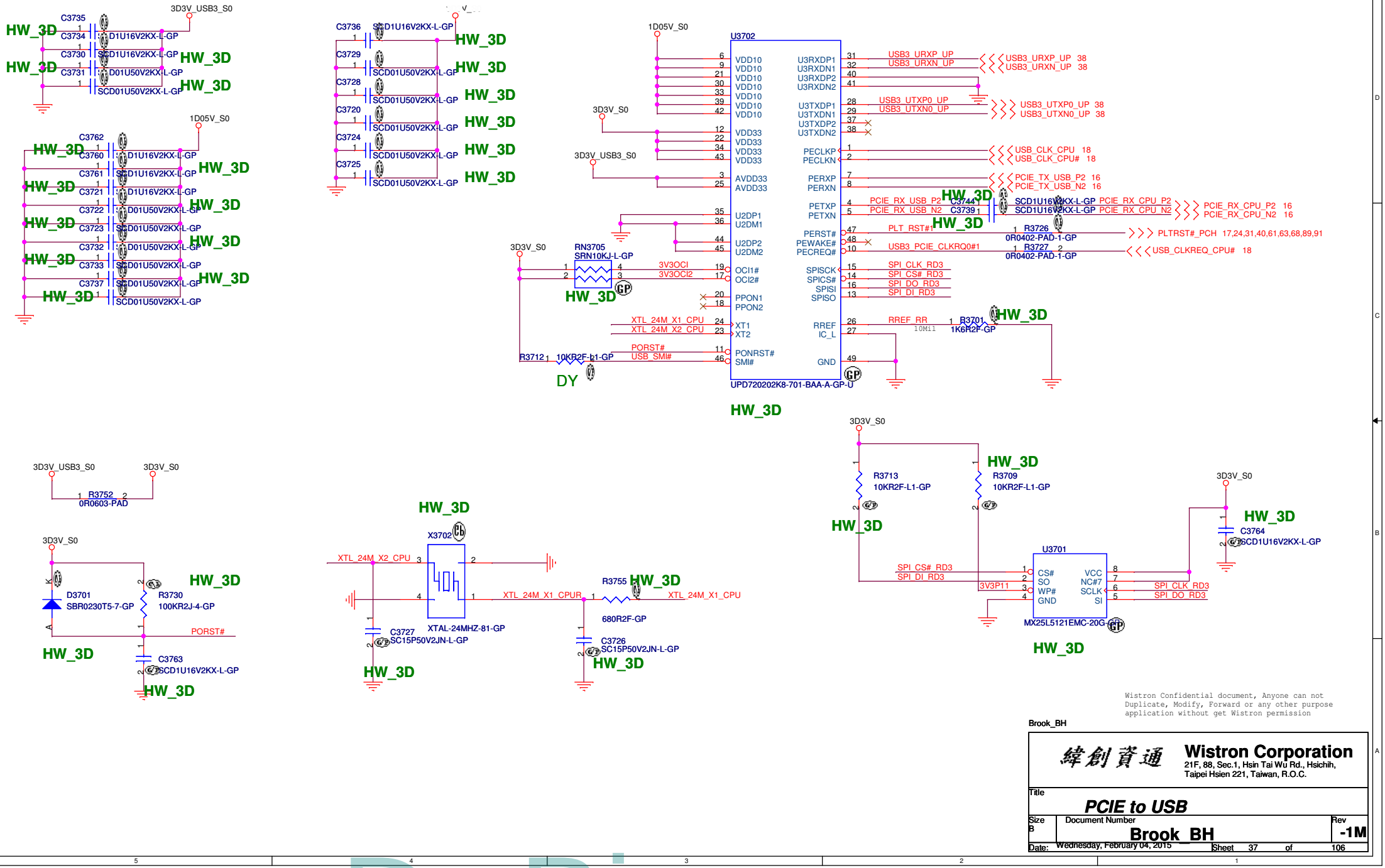

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Title: **PCIE to USB**

Size	Document Number	Rev
B	Brook_BH	-1M

Date: Wednesday, February 04, 2015 Sheet 37 of 106

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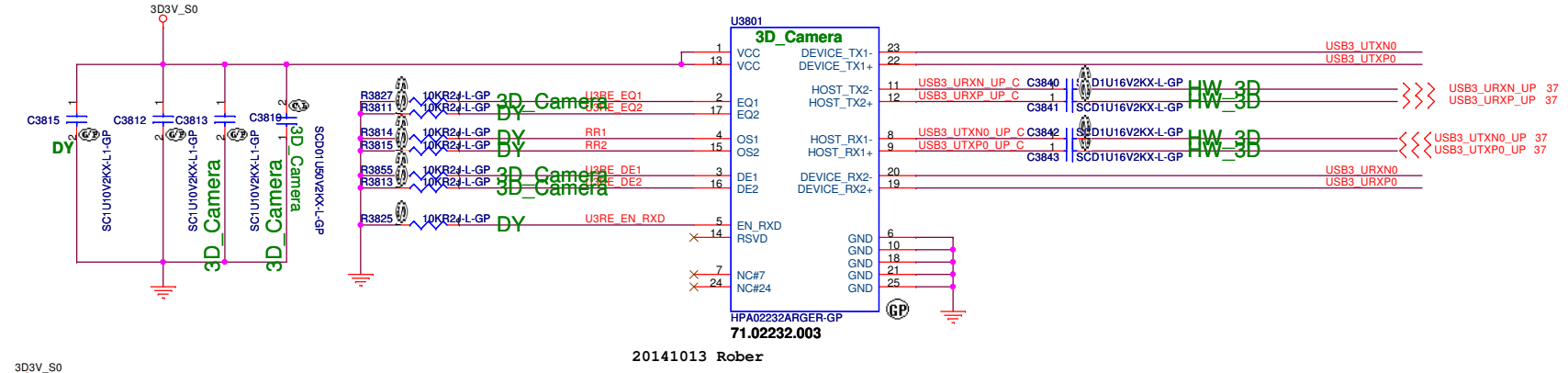
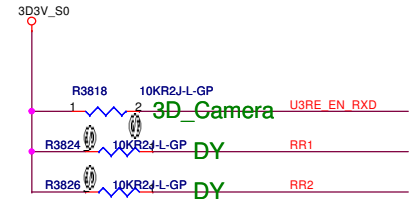
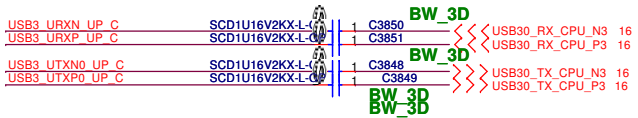
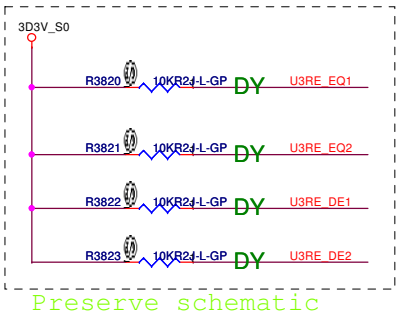
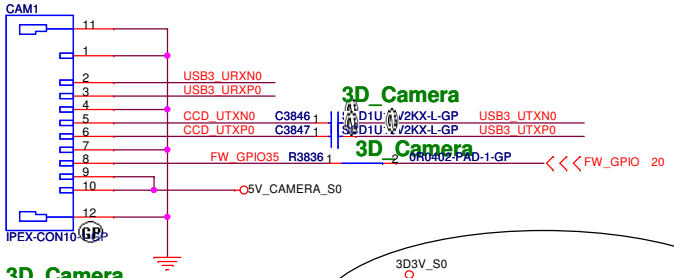




for Broadwell 3D Camera







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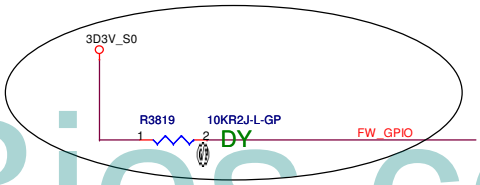
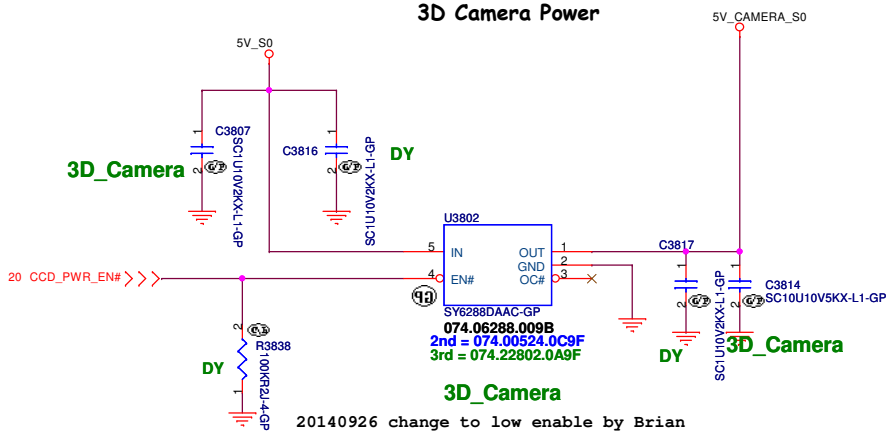


3D Camera Power



20140926 change to low enable by Brian

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Title: USB Redriver

Size: A3 | Document Number: Brook_BH | Rev: -1M

Date: Wednesday, February 04, 2015 | Sheet 38 of 106

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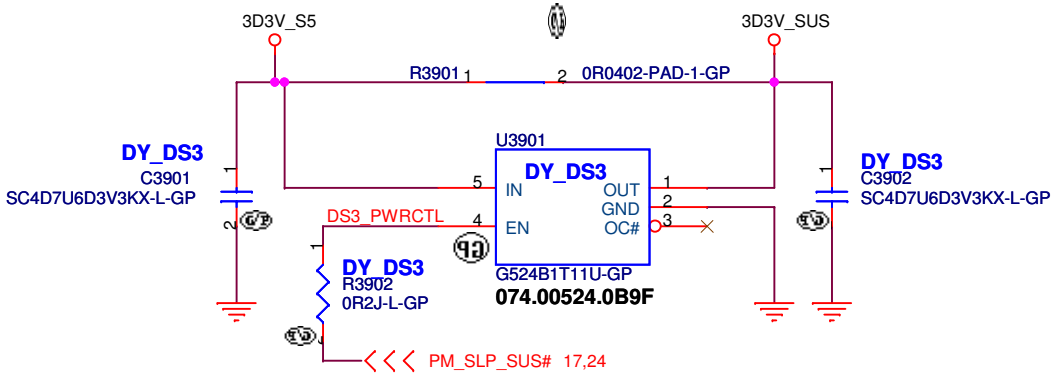

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Title: ***DS3***

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Date: Wednesday, February 04, 2015 Sheet 39 of 106

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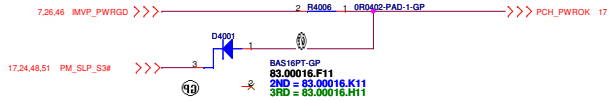
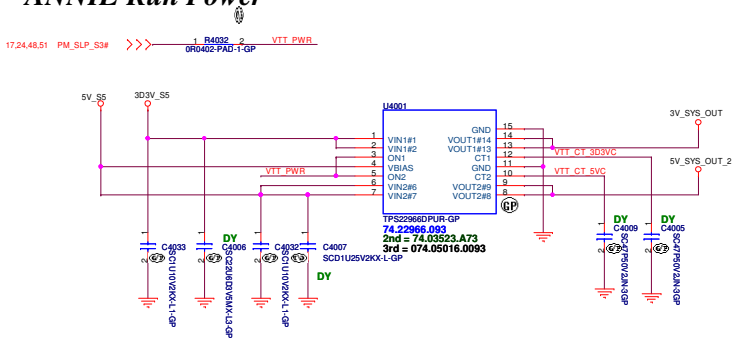
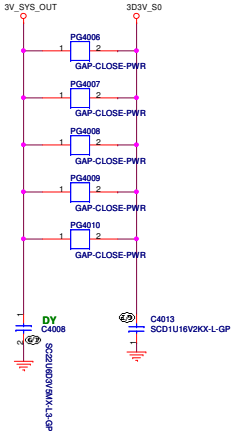
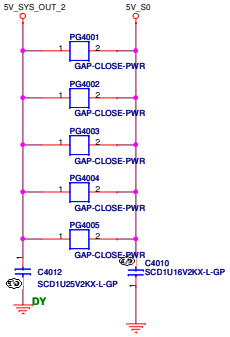
Power Sequence



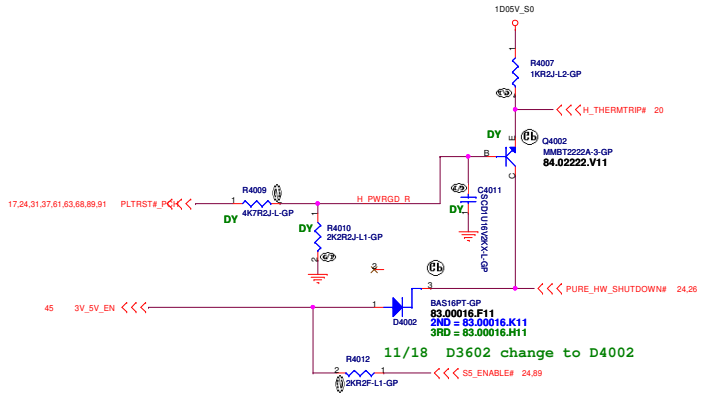
ANNIE Run Power

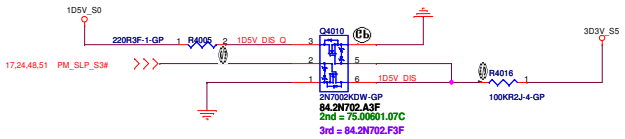






Discharge circuit





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Title: Connected Standby1

Size: A2 | Document Number: Brook_BH | Rev: -1M

Date: Wednesday, February 04, 2015 | Sheet 40 of 106

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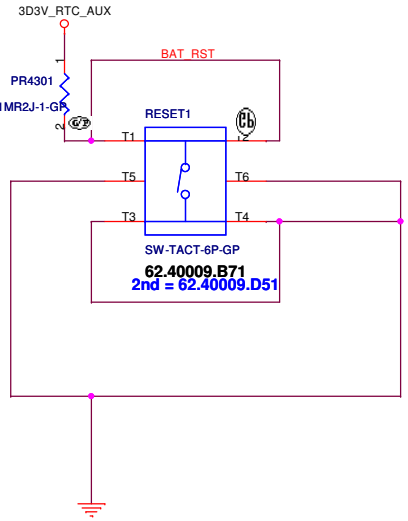
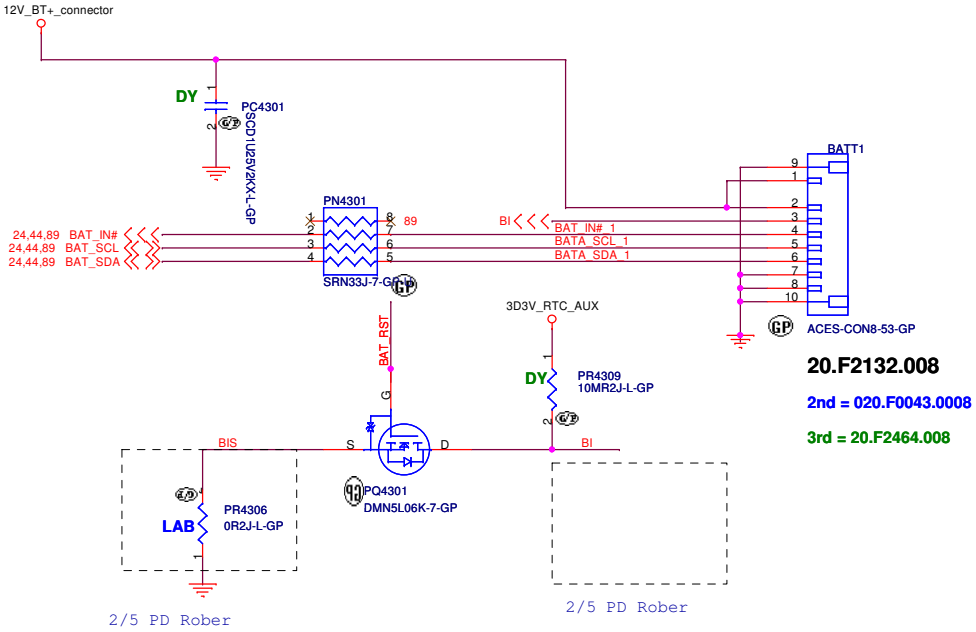
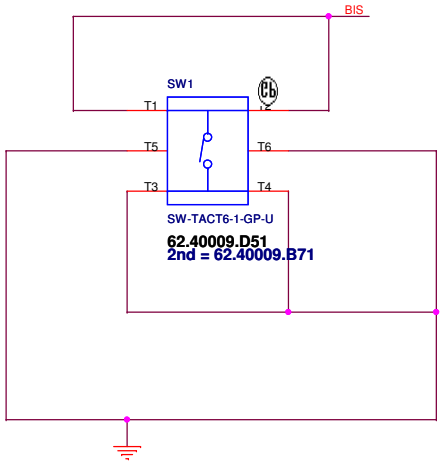
Battery Reset



Battery Connector

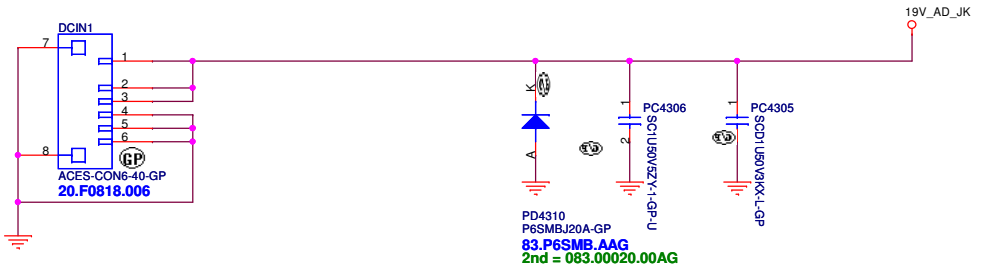


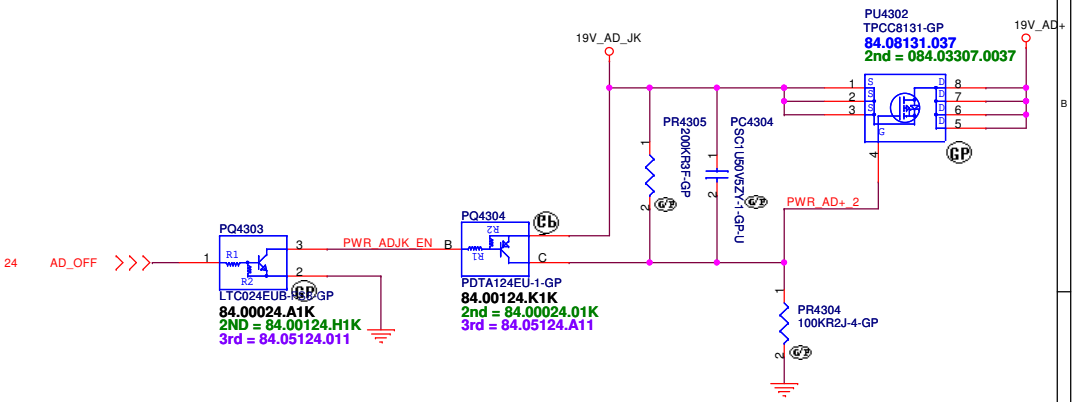
Battery Insert



ANNIE solution

Adaptor in to generate DCBATOUT





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Title	***DCIN JACK&BATT CONN***	
Size A3	Document Number **Brook_BH**	Rev **-1M**
Date: Thursday, February 05, 2015	Sheet 43 of 106	

SSID = Charger

	Star	PM_SLP_A#	Adaptor Current	AC_Protect current (85% x 120%)	AC_Protect Counter	PR4404 Sense resistor	Counter to Voltage	R1 PR4407	R2 PR4401
40W	AC + Battery	High	2.1	102%	2.142	20 m/Ohm	0.8568	41.2	100
45W	AC + Battery	High	2.37	102%	2.4174	20 m/Ohm	0.96696	60.4	100
65W	AC + Battery	High	3.42	102%	3.4884	10 m/Ohm	0.69768	86.2	100
90W	AC + Battery	High	4.74	102%	4.8348	10 m/Ohm	0.96696	60.4	100
120W	AC + Battery	High	6.32	102%	6.4301	10 m/Ohm	1.28728	113	100
135W	AC + Battery	High	7.1	102%	7.242	10 m/Ohm	1.4484	180	100

	45W	90W
PR4404	20m(64.R0205.7FL)	10m(64.R0105.7FL)
PR4407	60.4K(64.60425.6DL)	60.4K(64.60425.6DL)
PR4401	100K(64.10035.L3L)	100K(64.10035.L3L)

adapter 65W and 90W
AC mode (default:120%):
set up the value by PR4401 and PR4407

Add PR4838/PR4437
2011.0817

Deglicth Time Setting
125K -> Deglitch time : 5us
375K -> Deglitch time : 15us

CYNTEC, 7*7*3
DCR: 37~40mOhm
Idc : 5.5 A , Isat : 10A

Charger Current=1.4~3.6A

PU4404/PU4405 change to SIS412

Battery OCP	R3	R4
6 Cell (3S2P)	7A	105K	52.3K
4 Cell (4S1P)	4A	165K	52.3K

Battery UVP	R5	R6
6 Cell (3S2P)	9V	165K	71.5K
4 Cell (4S1P)	12V	110K	71.5K

Battery OVP	R7	R8
6 Cell (3S2P)	13.2V	90.9K	71.5K
4 Cell (4S1P)	17.6V	51.1K	71.5K

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Title: CHARGER_HPA02224
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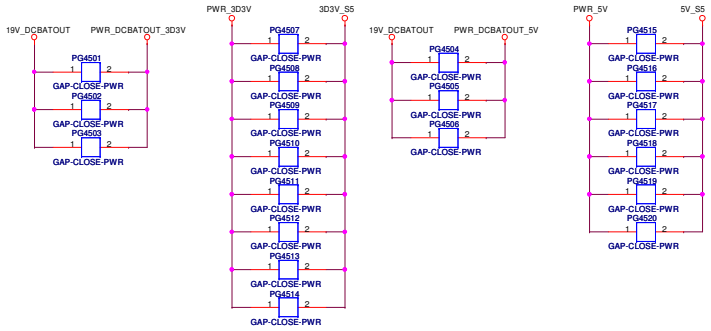
SSID = PWR.Plane.Regulator_3p3v5v



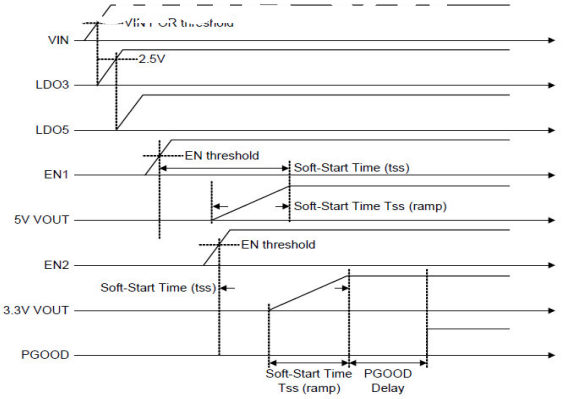
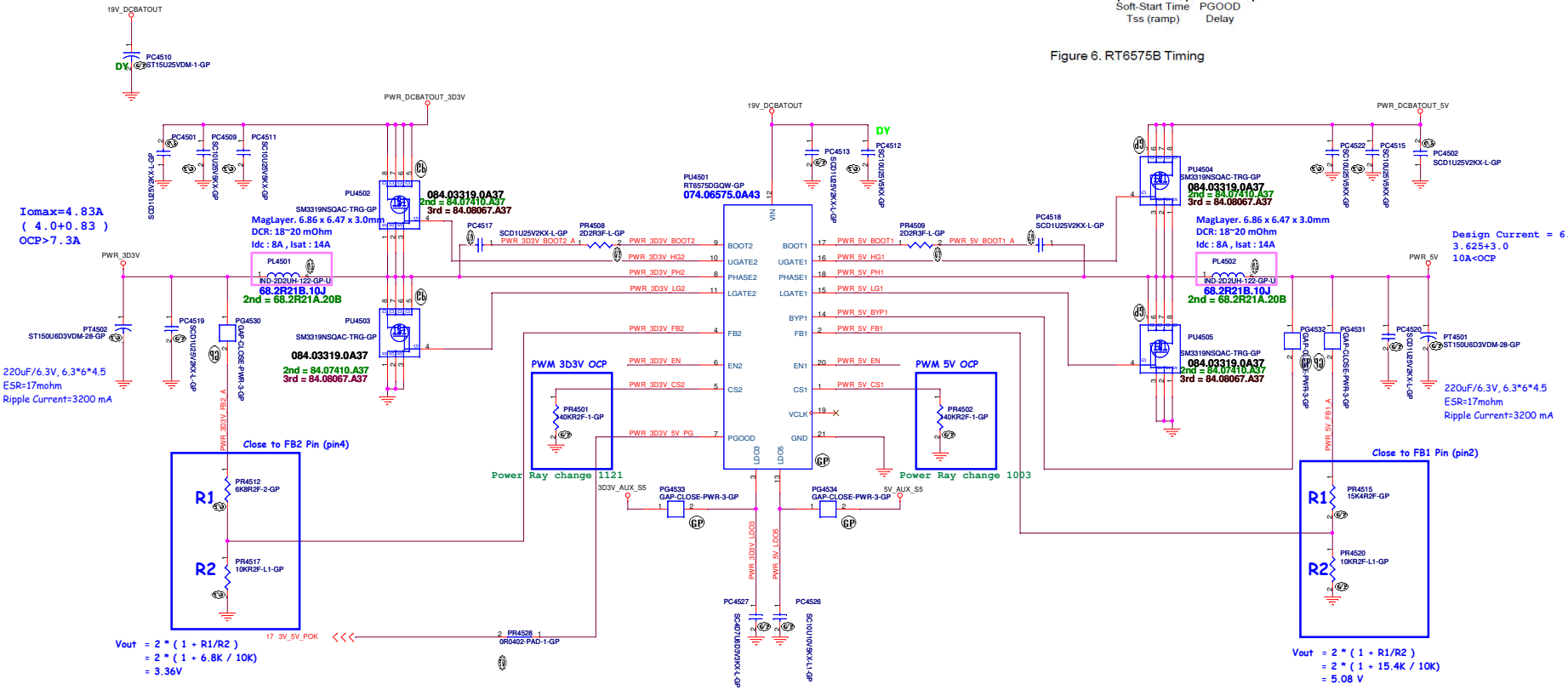
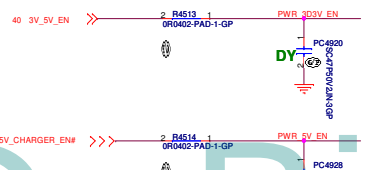


Figure 6. RT6575B Timing



11/18 R4913 and R4914 need to change R4513and R4514



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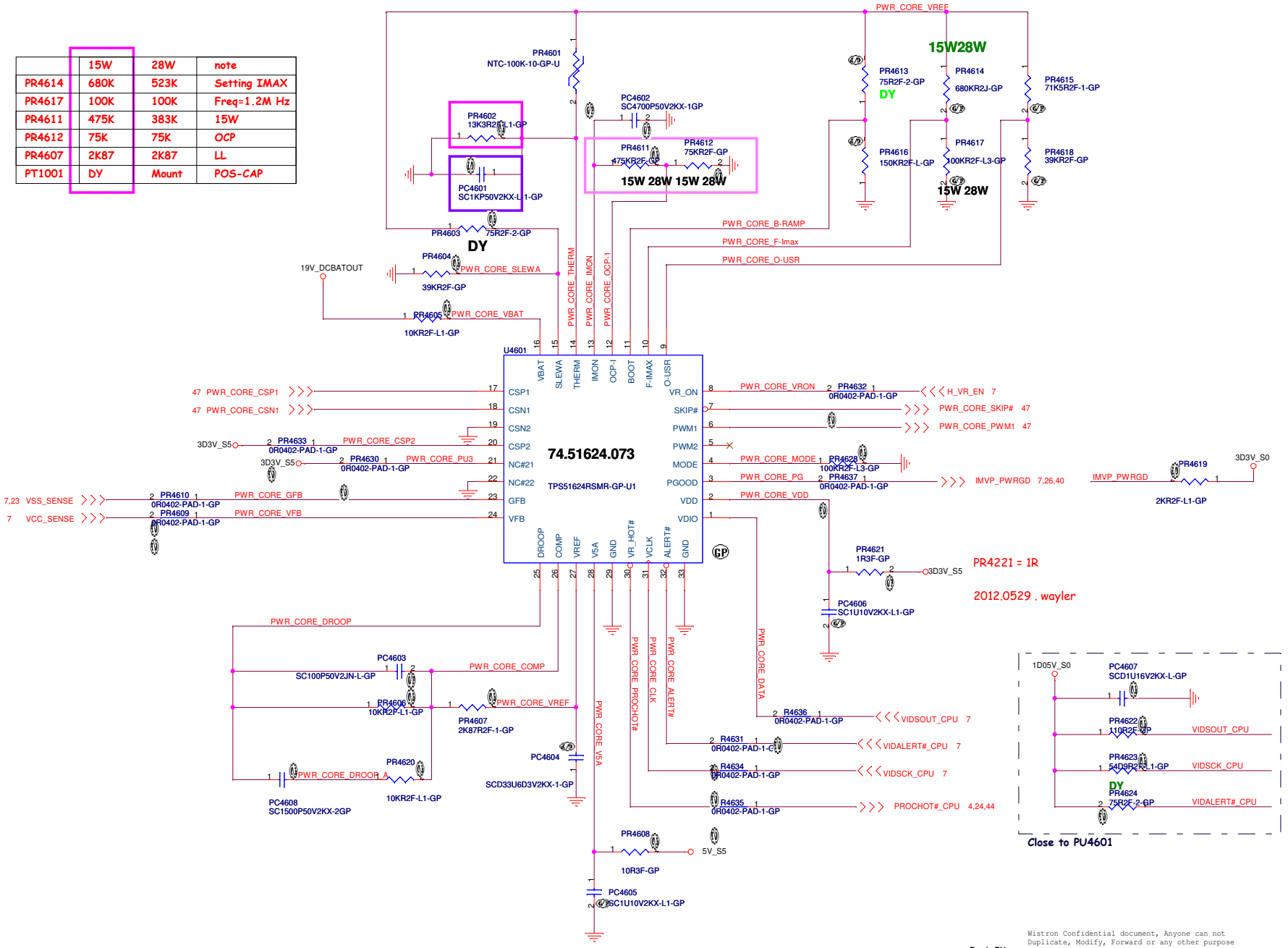
SSID = CPU.Regulator

	15W	28W	note
PR4614	680K	523K	Setting IMAX
PR4617	100K	100K	Freq=1.2M Hz
PR4611	475K	383K	15W
PR4612	75K	75K	OCP
PR4607	2K87	2K87	LL
PT1001	DY	Mount	POS-CAP



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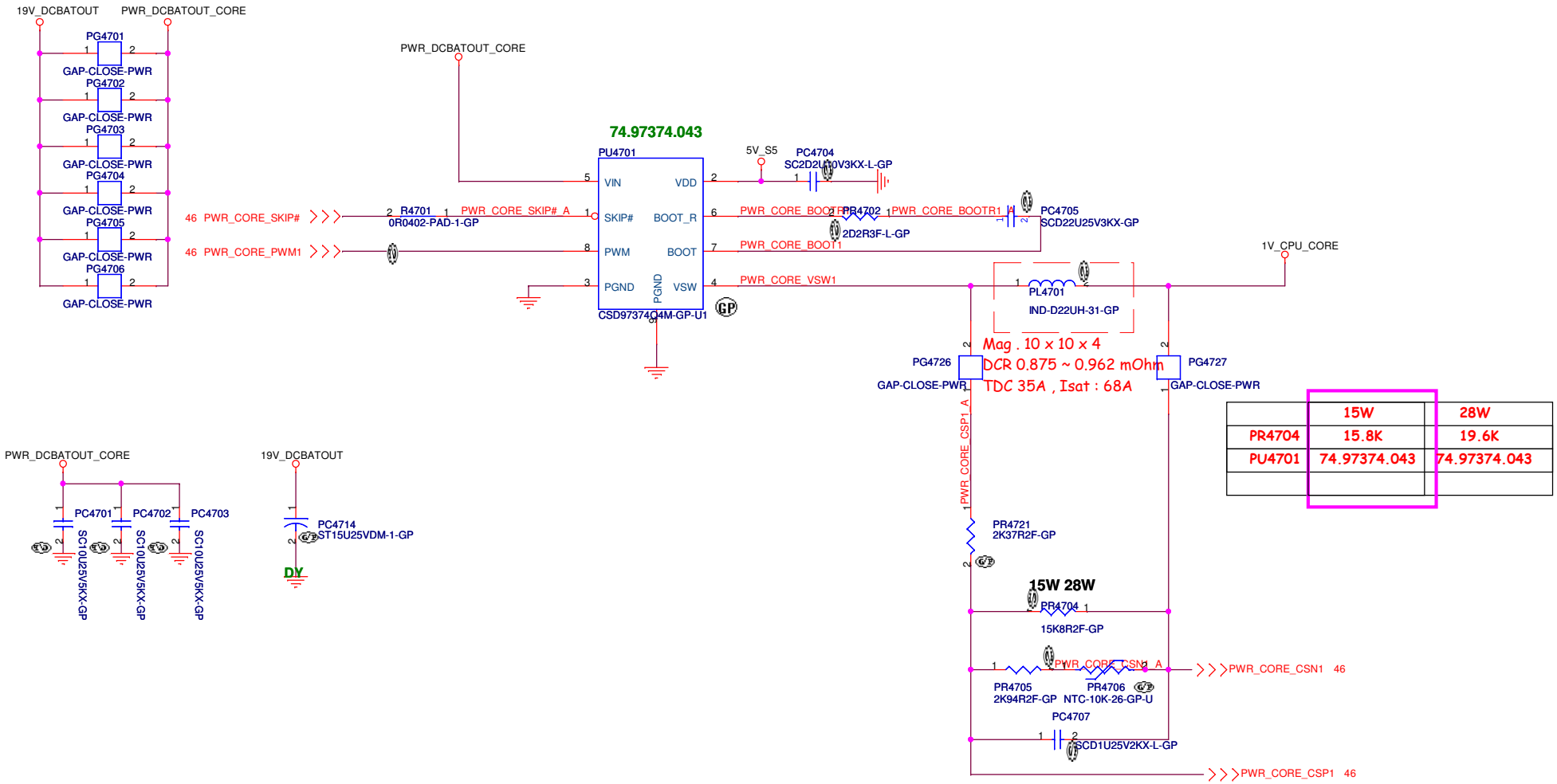

	15W	28W
PR4704	15.8K	19.6K
PU4701	74.97374.043	74.97374.043

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Title: TPS51624_CPUCORE(2/2)

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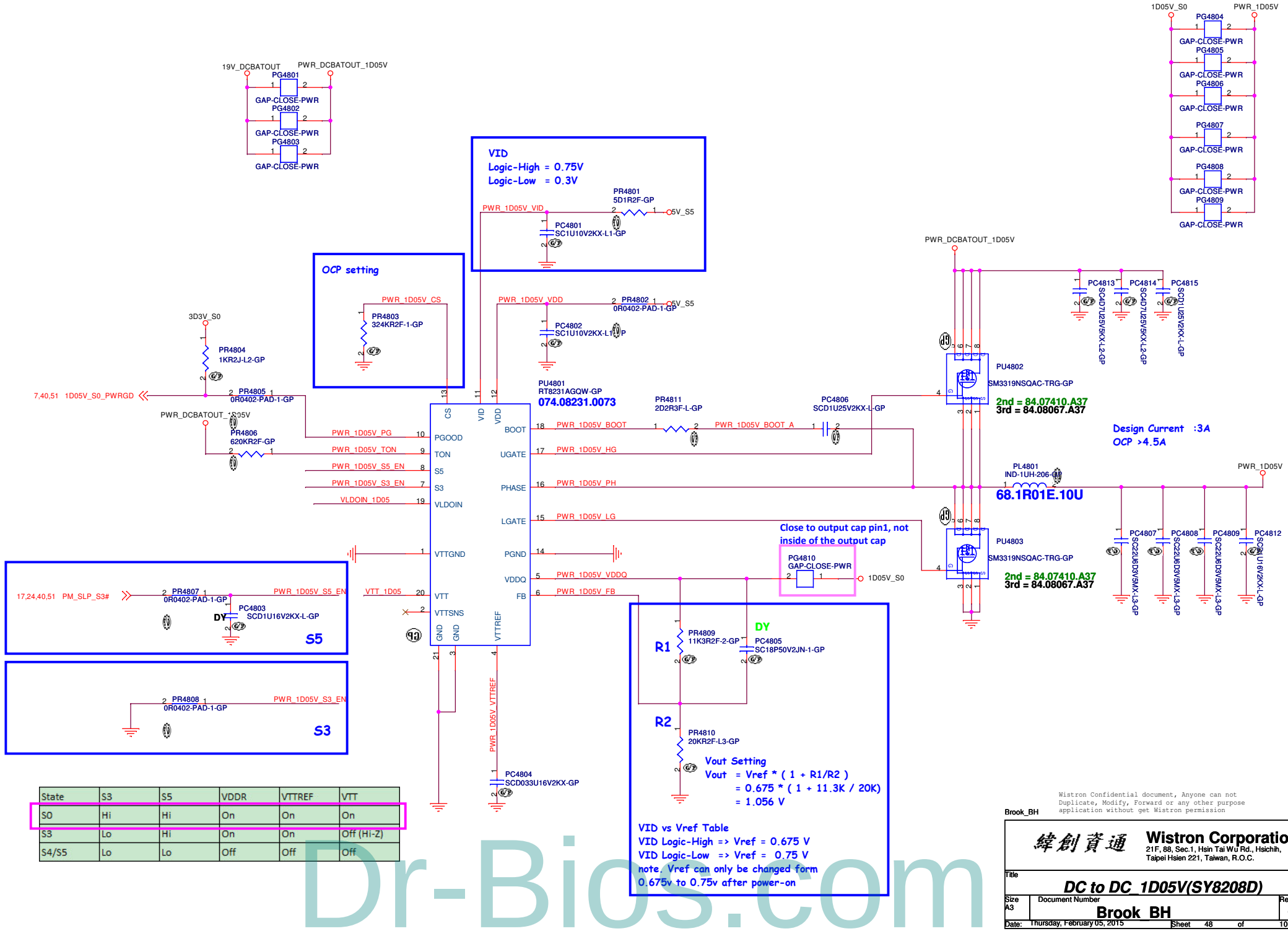

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

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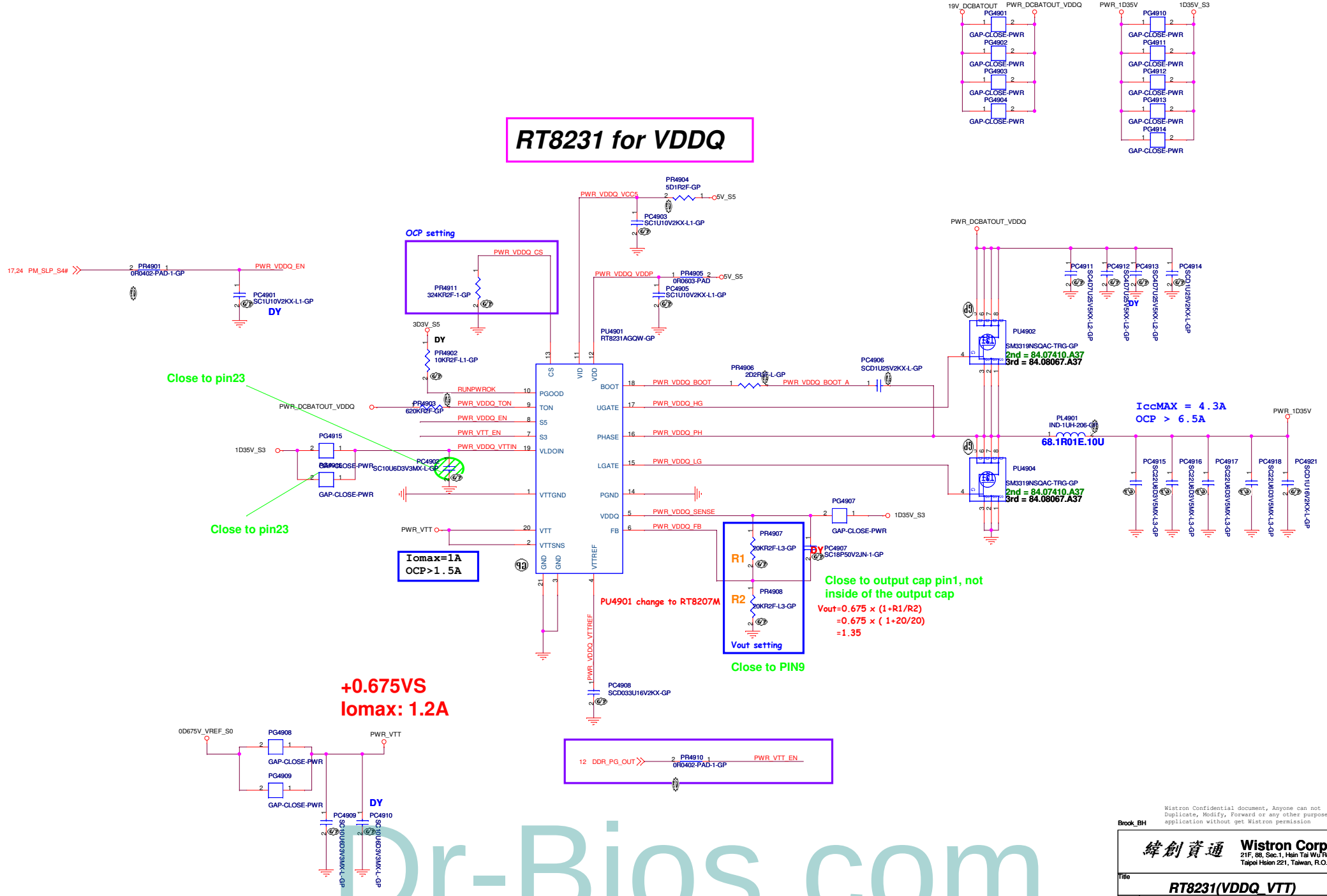
SSID = PWR.Plane.Regulator_1p2v0p6v

RT8231 for VDDQ



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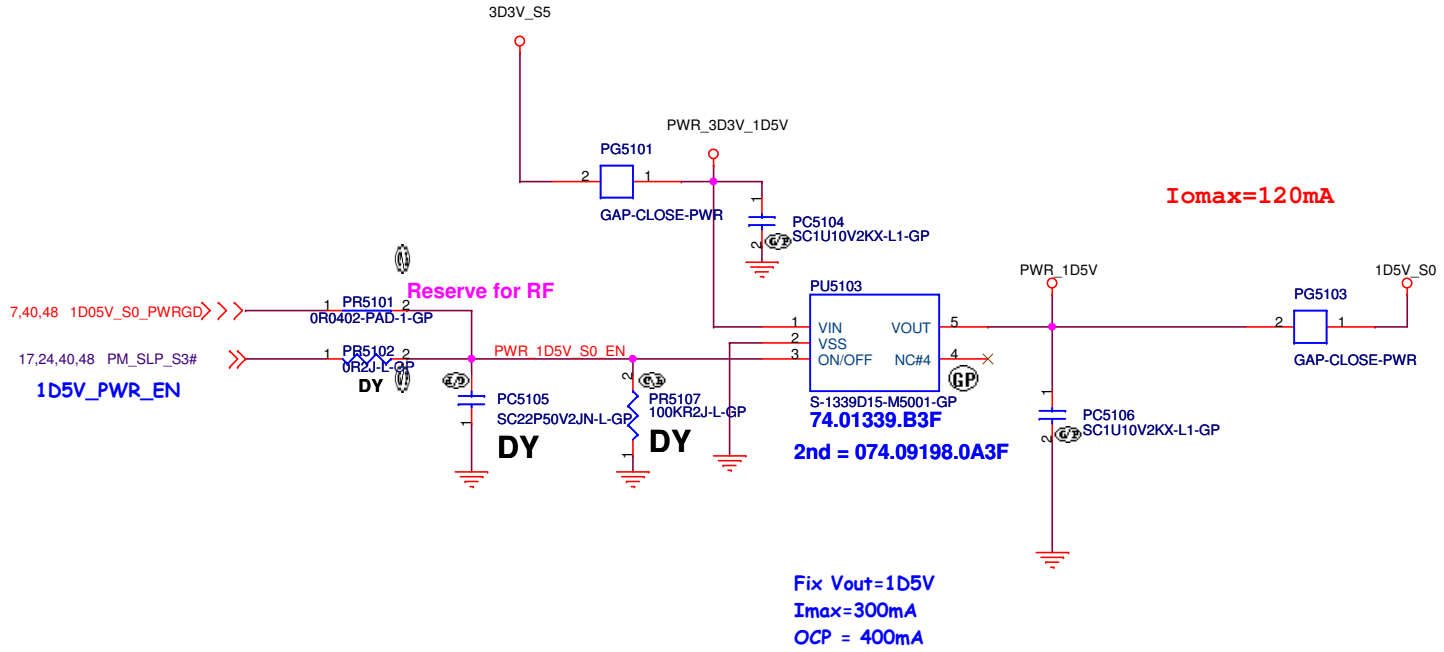
TLV70215 for 1D5V_S0
Enable=1.5V
Disable=0.4V



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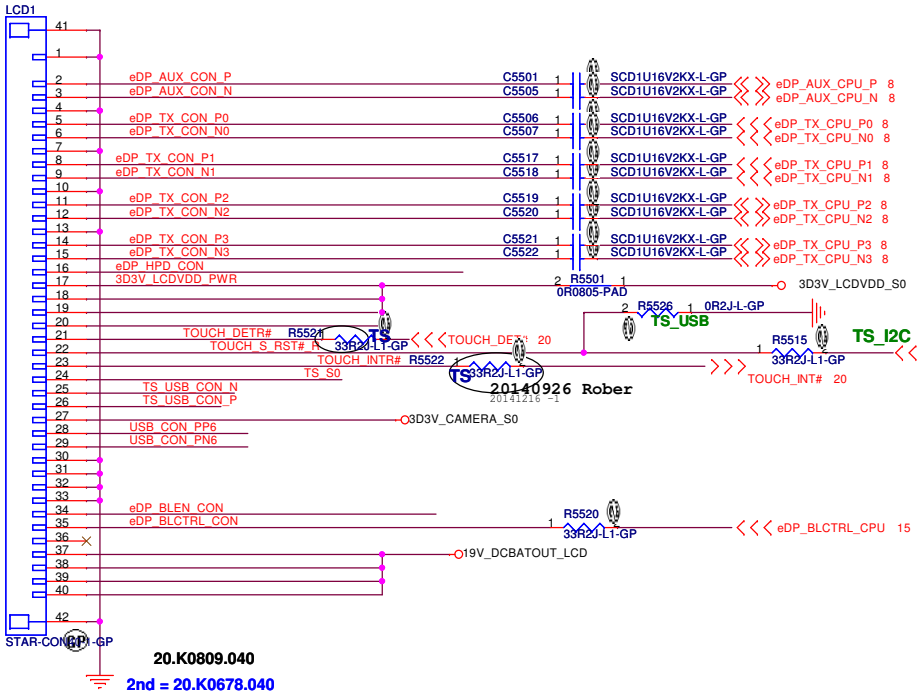
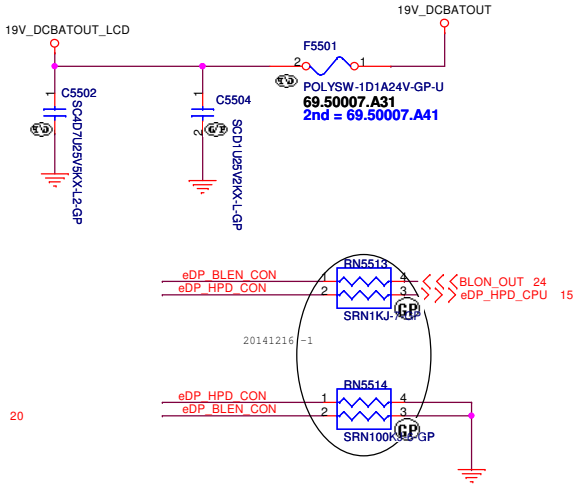
Main Func = LCD

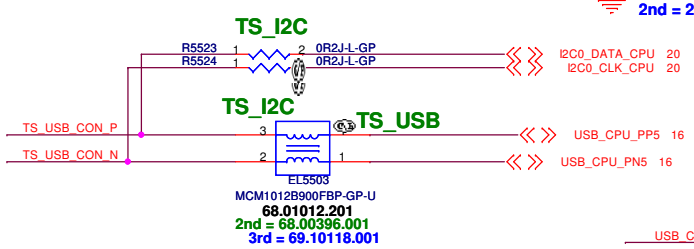
Pin count		EDP 4Lans+CCD
1	Display	GND
2		eDP_AUX_CON_P
3		eDP_AUX_CON_N
4		GND
5		eDP_TX_CON_P0
6		eDP_TX_CON_N0
7		GND
8		eDP_TX_CON_P1
9		eDP_TX_CON_N1
10		GND
11		eDP_TX_CON_P2
12		eDP_TX_CON_N2
13		GND
14		eDP_TX_CON_P3
15		eDP_TX_CON_N3
16		eDP_HPD_CON
17		LCDVDD(3V)
18		LCDVDD(3V)
19		LCDVDD(3V)
20		LCDVDD(3V)
21	Touch	TOUCH_DET#
22		TOUCH_GND/ TOUCH_RST
23		TOUCH_EN/ TOUCH_INT
24		Touch_PWR(3V/5V)
25		USB_PN6/ SCL
26		USB_PP6/ SDA
27	CCD	3D3V_CAMERA_S0
28		USB_CAMERA_P
29		USB_CAMERA_N
30	GND	GND
31		GND
32		GND
33		GND
34		
35		
36		
37	DCBATOUT	DCBATOUT_LCD
38		DCBATOUT_LCD
39		DCBATOUT_LCD
40		DCBATOUT_LCD

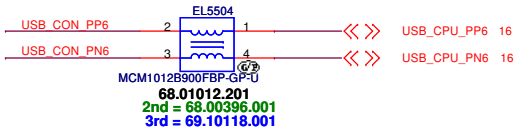


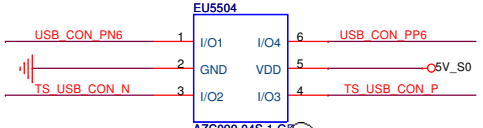
20.K0809.040
2nd = 20.K0678.040

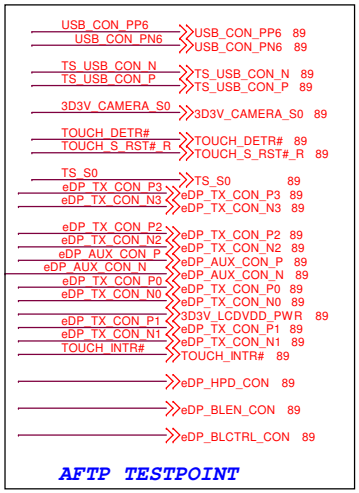
Inverter Power



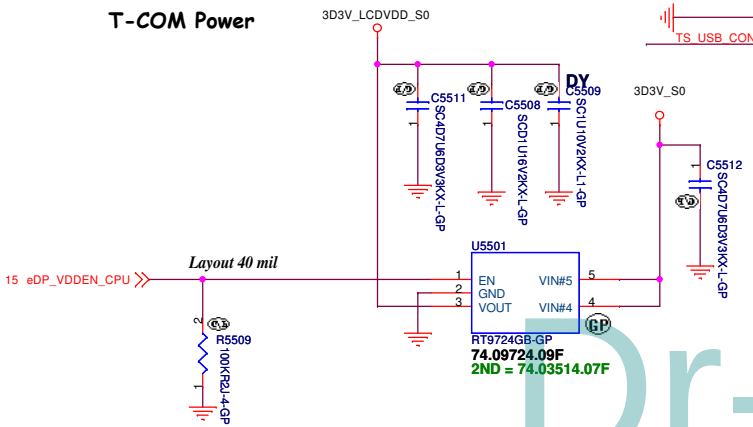




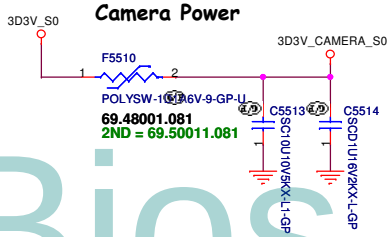




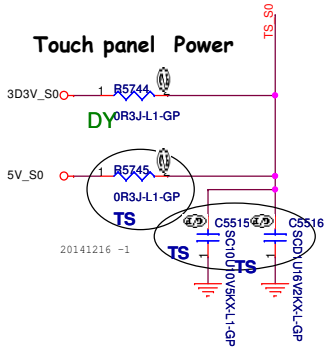
T-COM Power



Camera Power



Touch panel Power



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Title: LCD Connector

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SSID = Display

VGA RTD2168

Embedded LDO

Select VCCK_V12 source from external 1.2V or embedded LDO

3D3V_S0 — R5611 4K7R2J-L-GP — LDO_EN

C5603 SCD1U16V2KX-L-GP — 1D2V_VCCK_S0

20141013 Rober

close to pin25

LDO_EN(PIN21)	
0	1
VCCK_V12 from External 1.2V	VCCK_V12 from Embedded LDO

close to pin24

3D3V_AVCC_S0 — L5604 PBY100505T-600Y-N-GP — 3D3V_S0

C5618 SC10U10V5KX-L-GP, C5616 SCD1U16V2KX-L-GP, C5620 SCD1U16V2KX-L-GP

close to pin5

close to pin9

3D3V_DAC_S0 — L5605 PBY100505T-600Y-N-GP

C5619 SC10U10V5KX-L-GP, C5617 SCD1U16V2KX-L-GP, C5621 SCD1U16V2KX-L-GP

close to pin20

U5601 RTD2168-CGT-GP

3D3V_AVCC_S0	24 AVCC_33	HPD 1	CRT_HPD
1D2V_VCCK_S0	25 AVCC_12	SMB_SCL 2	SMB_SCL
	5 DVCC_33	SMB_SDA 3	SMB_SDA
3D3V_S0	20 DVCC_33	VGA_SCL 4	CRT_DDCCLK_CON
		VGA_SDA 6	CRT_DDCDATA_CON
1D2V_VCCK_S0	19 VCCK_12		
3D3V_DAC_S0	9 VDD_DAC_33	VSYNC 7	CRT_VSYNC
		HSYNC 8	CRT_HSYNC
LDO_EN	21 LDO_EN	RED_P 15	CRT_RED
		RED_N 16	
DP_AUX_CON_P	26 AUX_P	GREEN_P 12	CRT_GREEN
DP_AUX_CON_N	27 AUX_N	GREEN_N 13	
DDI_VGA_DATA_C_P0	29 LANE0P	BLUE_P 10	CRT_BLUE
DDI_VGA_DATA_C_N0	30 LANE0N	BLUE_N 11	
DDI_VGA_DATA_C_P1	31 LANE1P	POL1_SDA 22	POL1_SDA
DDI_VGA_DATA_C_N1	32 LANE1N	POL2_SCL 23	POL1_SCL
	17 XI/CKIN	GND_DAC 14	
	18 XO	GND 33	
RRX	28 RRX		

15 PCH_DPC_AUXP — C5615 SCD1U16V2KX-L-GP — DP_AUX_CON_P

15 PCH_DPC_AUXN — C5614 SCD1U16V2KX-L-GP — DP_AUX_CON_N

8 DDI_VGA_DATA_CPU_P0 — C5613 SCD1U16V2KX-L-GP — DDI_VGA_DATA_C_P0

8 DDI_VGA_DATA_CPU_N0 — C5612 SCD1U16V2KX-L-GP — DDI_VGA_DATA_C_N0

8 DDI_VGA_DATA_CPU_P1 — C5611 SCD1U16V2KX-L-GP — DDI_VGA_DATA_C_P1

8 DDI_VGA_DATA_CPU_N1 — C5610 SCD1U16V2KX-L-GP — DDI_VGA_DATA_C_N1

20140926 Rober

R5610 12KR2F-L-GP

20141013 Rober

RN5612 SRN4K7J-5-GP

20141216 -1

R5617 100KR2J-4-GP

CRT_RED — L5601 BLM18BB220SN-GP — CRT_RED_CON

C5604 SC10P50V2JN-L1-GP, C5605 SC10P50V2JN-L1-GP

CRT_GREEN — L5602 BLM18BB220SN-GP — CRT_GREEN_CON

C5606 SC10P50V2JN-L1-GP, C5607 SC10P50V2JN-L1-GP

CRT_BLUE — L5603 BLM18BB220SN-GP — CRT_BLUE_CON

C5608 SC10P50V2JN-L1-GP, C5609 SC10P50V2JN-L1-GP

RN5610 SRN150J-1-GP, RN5611 SRN150J-1-GP

those compoent need to close

L5601~3 change to 68.00084.B61

5V_CRT_S0 — 5V_HDMI_S0

D5601 CH551H-30PT-GP

83.R5003.C8F

2ND = 83.R5003.H8H

3rd = 83.5R003.08F

RN5601 SRN2K2J-5-GP

CRT_DDCDATA_CON, CRT_DDCCLK_CON

C5622 SCD1U16V2KX-L-GP, C5623 SC2D2U10V3KX-L-GP — 1D2V_VCCK_S0

close to pin19

CRT_VSYNC — R5605 36R2F-1-GP — CRT_VSYNC_CON — C5601 SC10P50V2JN-L1-GP

CRT_HSYNC — R5606 36R2F-1-GP — CRT_HSYNC_CON — C5602 SC10P50V2JN-L1-GP

CRT_DDCDATA_CON, CRT_DDCCLK_CON, CRT_RED_CON, CRT_GREEN_CON, CRT_BLUE_CON, CRT_VSYNC_CON, CRT_HSYNC_CON

AFTP TESTPOINT

Mode Configure Table(Power On Latch)

3D3V_S0 — R5613 4K7R2J-L-GP (DY) — POL1_SDA — R5614 4K7R2J-L-GP

3D3V_S0 — R5615 4K7R2J-L-GP — POL1_SCL — R5616 4K7R2J-L-GP (DY)

POL2_SCL(PIN23)	POL1_SDA(PIN22) 0	POL1_SDA(PIN22) 1
0	X	EP MODE
1	ROM ONLY MODE	EEPROM MODE

RTD2168 Supports three operation mode for systemdesign.
Reserve 4.7K resistor pull high/low for mode selection
ROM ONLY Mode: PIN22 pull low, PIN23 pull high
EP Mode: PIN22 pull high, PIN23 pull low
EEPROM Mode: PIN22 pull high, PIN23 pull high

EEPROM MODE

3D3V_S0 — U5602 CAT24C128YI-GT3-GP

A0, A1, A2, GND (DY), VCC, WP, SCL, SDA — POL1_SCL, POL1_SDA

VEDOR CHECK

In EEPROM mode,an additional EEPROM is needed. EEPROM should configure with following conditions. 1- EEPROM with a size of 16K-Byte
ROM or EEPROM mode: connect to PCH SMBUS
2- EEPROM device should be 2-byte addressing device
3- Slave address should configure as 0xA8

5V_CRT_S0 — C5632 SCD1U16V2KX-L-GP

CRT1 D-SUB-15-155-GP-U

CRT_DDCDATA_CON	12	VCC_CRT	9
CRT_DDCCLK_CON	15	DDCDATA_ID1	
		DDCCLK_ID3	
CRT_RED_CON	1	CRT_RED	
CRT_GREEN_CON	2	CRT_GREEN	
CRT_BLUE_CON	3	CRT_BLUE	
CRT_VSYNC_CON	14	VSYNC	
CRT_HSYNC_CON	13	HSYNC	
		NC#4	4
		NC#11	11
		GND	5
		GND	6
		GND	7
		GND	8
		GND	10
		GND	16
		GND	17

20.20984.015

2nd = 20.20938.015

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Title: VGA RTD2168

Size: A3 | Document Number: Brook_BH | Rev: -1M

Date: Thursday, February 12, 2015 | Sheet 56 of 106

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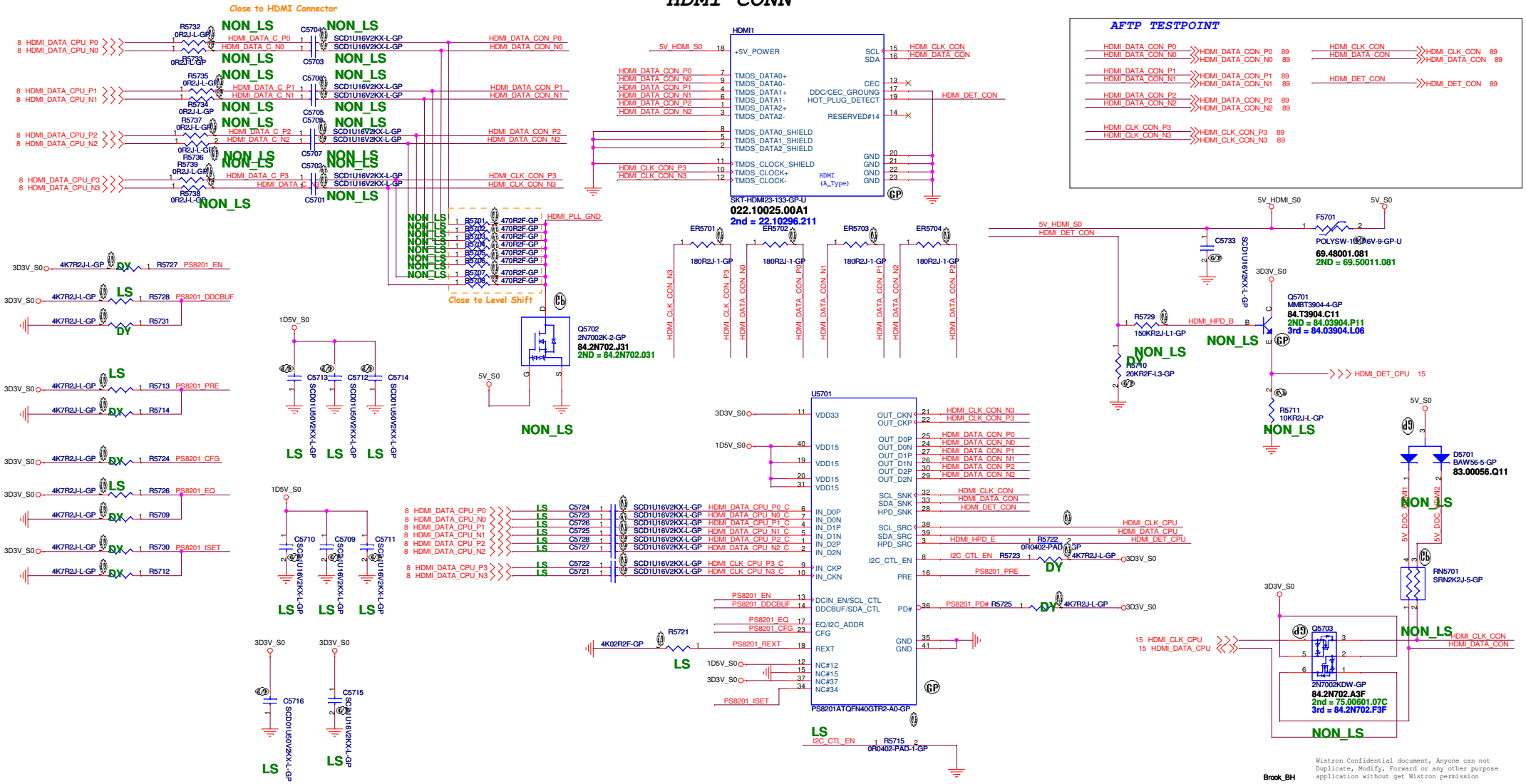
SSID = VIDEO

HDMI Level Shifter & CONN

HDMI CONN



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Title	HDMI Level Shifter&Conn	
Size: Custom	Document Number: Brook_BH	Rev: -1M
Date: Wednesday, February 04, 2015	Sheet 57 of 106	

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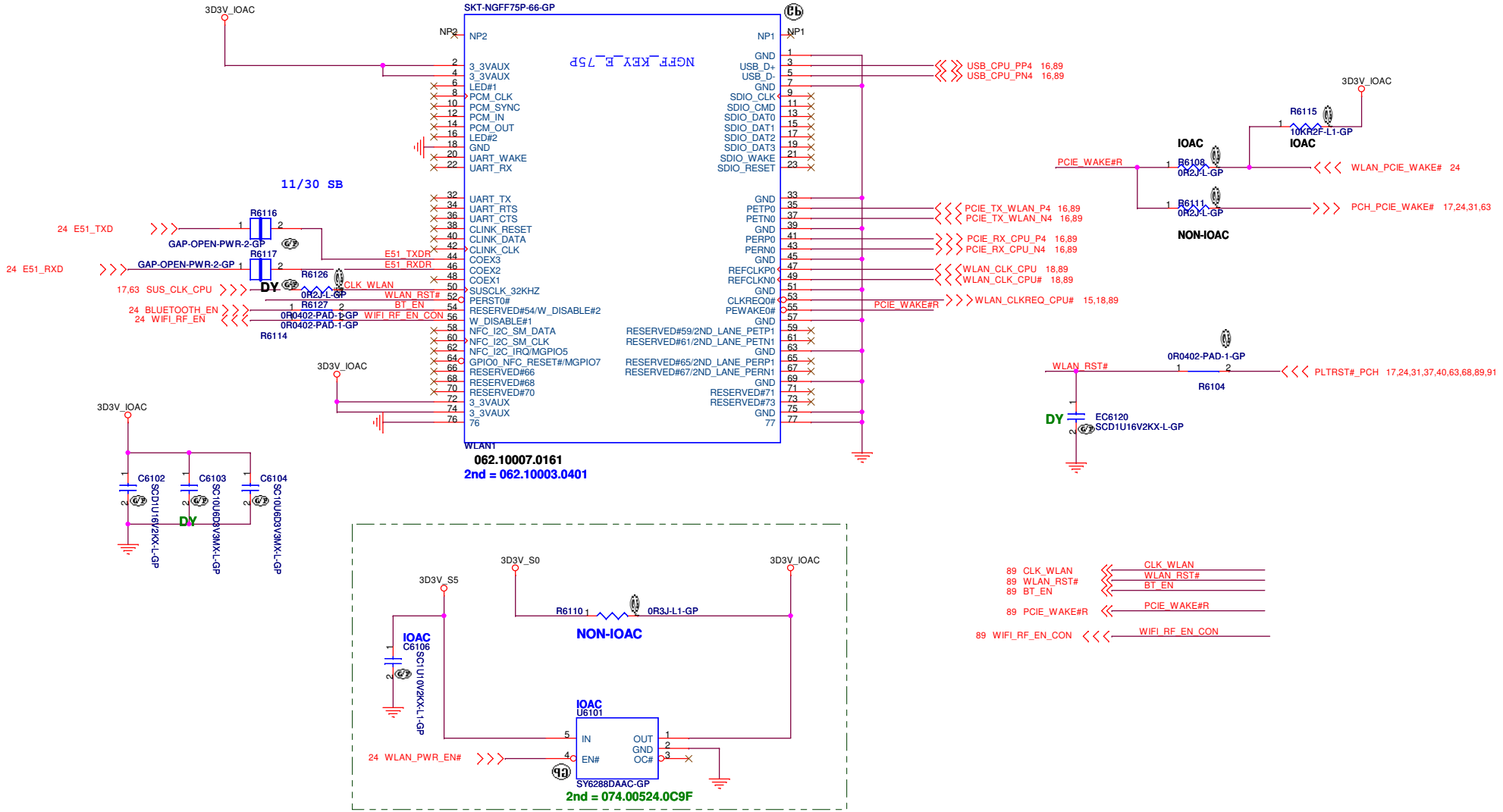
SSID = Wireless

Mini Card Connector(802.11a/b/g/n)



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Title: Mini Card WLAN

Size: A3 | Document Number: Brook BH | Rev: -1M

Date: Wednesday, February 11, 2015 | Sheet 61 of 106

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SSID = mSATA

Mini Card Connector(mSATA)

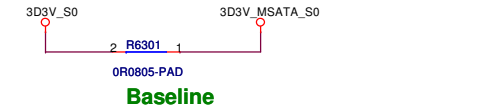
17.2.6 General Guidelines for mSATA (Gen 2 and Gen 3) Routing on SATA/PCIe muxed Ports

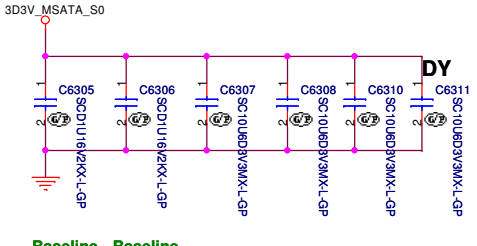
The below table summarizes the AC cap requirements on the motherboard when using the SATA/PCIe muxed ports.

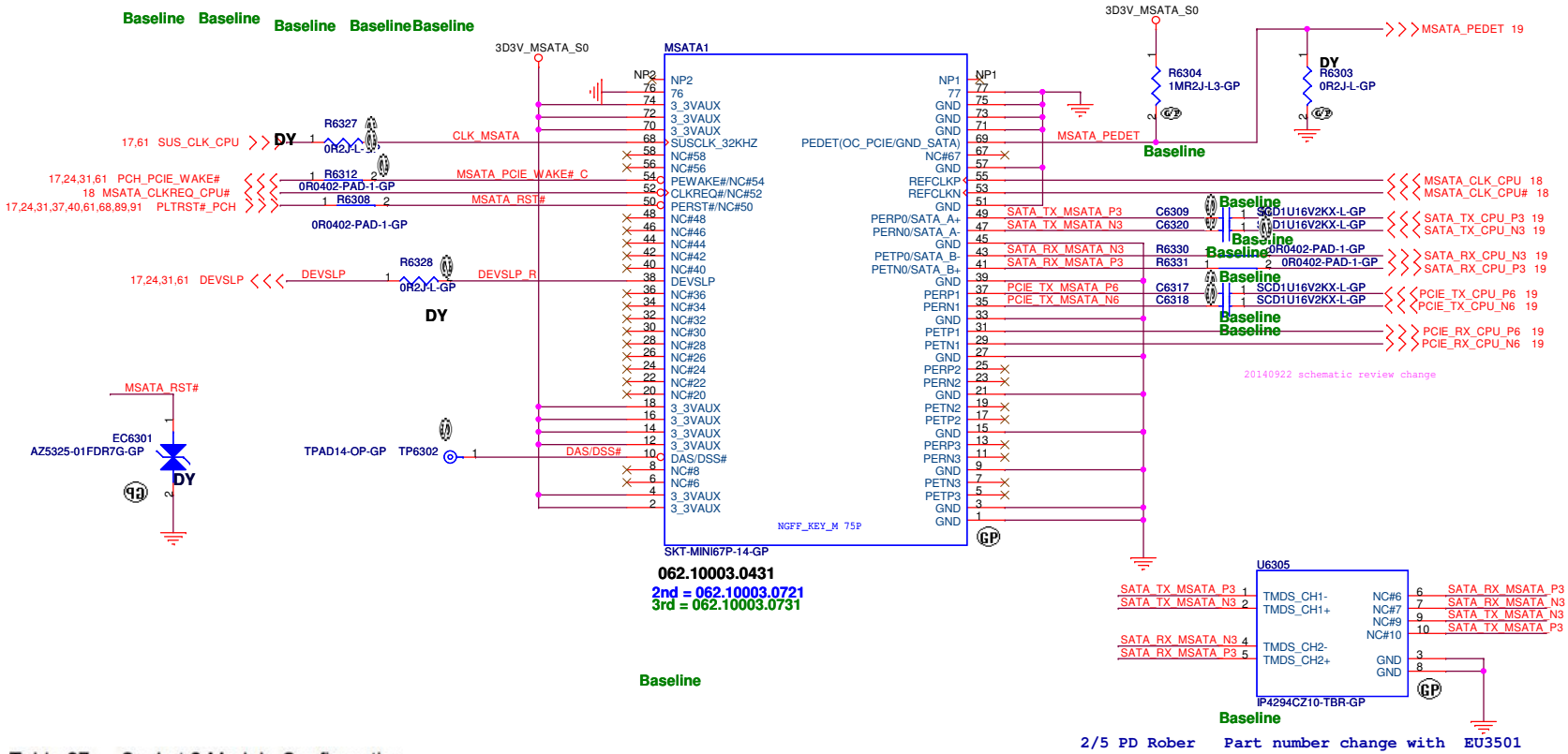
Table 17-6. SATA/PCIe Gen 2 and Gen 3 Capacitor Values

Condition	PCIe Only	SATA Only	PCIe/SATA
PCH Tx	100 nF	10 nF	100 nF
PCH Rx	None	10 nF[2]	None[3]

Notes:
1. For PCIe only application, please refer to the PCIe guidelines for details.
2. For SATA only application, both PCH Tx and PCH Rx channels need to have 10 nF caps on the motherboard. This option supports all SATA devices. However, the PCH Rx 10 nF capacitor can be removed if DC coupled ODDs/devices are NOT used.
3. For PCIe/SATA muxed application, a 100 nF AC cap is required on motherboards for PCH Tx channel and NO AC cap is required on motherboard for the PCH Rx channel. This option DOES NOT support DC coupled ODDs/Devices.







2/5 PD Rober Part number change with EU3501

Pin define from PCH and socket side.

	High (1)	Low (0)
PCH GPIO	SATA	PCIe
M.2 CONFIG_1	PCIe**	SATA

** Native: Internal Pull-Up (15k-40k) when function.

Table 27. Socket 2 Module Configuration

State #	Module Configuration Decodes CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75)	CONFIG_3 (Pin 1)	Module Type and Main Host Interface[1]	Port Configuration[2]
0	GND	GND	GND	GND	SSD – SATA	N/A
1	GND	N/C	GND	GND	SSD – PCIe	N/A

Pin define from PCH and socket side.

	High (1)	Low (0)
PCH GPIO	SATA	PCIe
M.2 CONFIG_1	PCIe**	SATA

** Native: Internal Pull-Up (15k-40k) when function.

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<Core Design>

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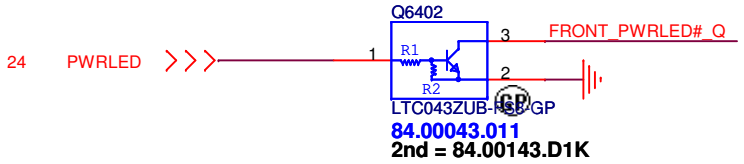
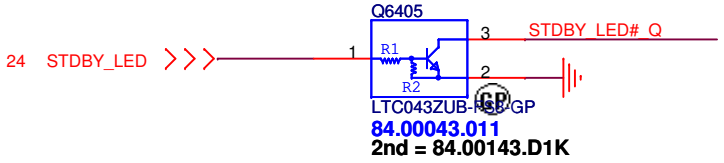
SSID = User.Interface

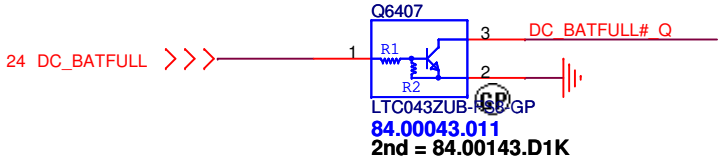
Power Button_LED



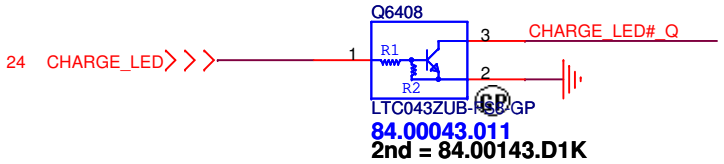
Power STDBY_LED

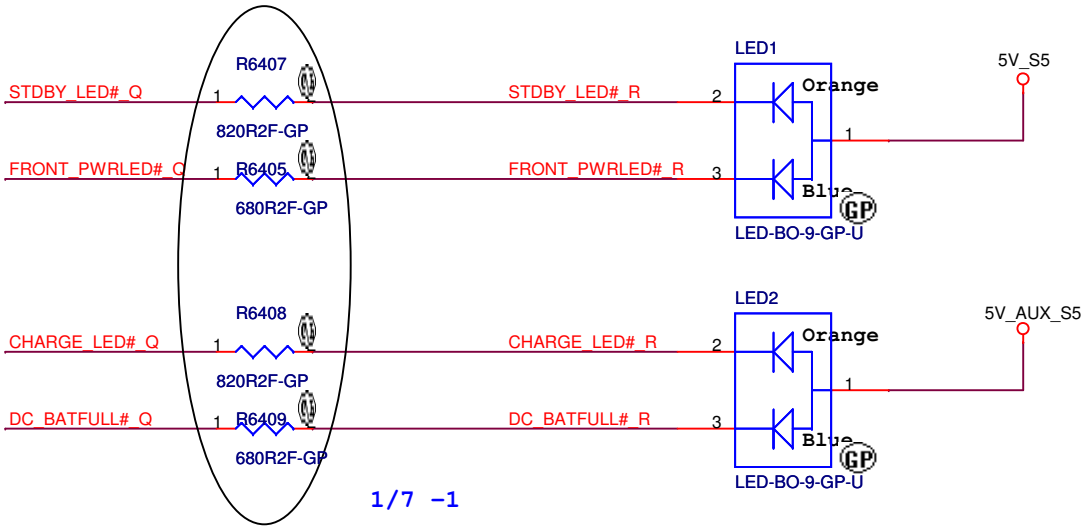


Battery LED2(DC_BATFULL)

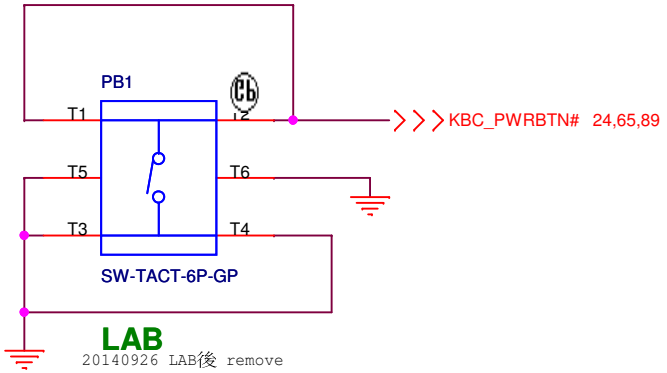


Battery LED1(CHARGE)





Power Button



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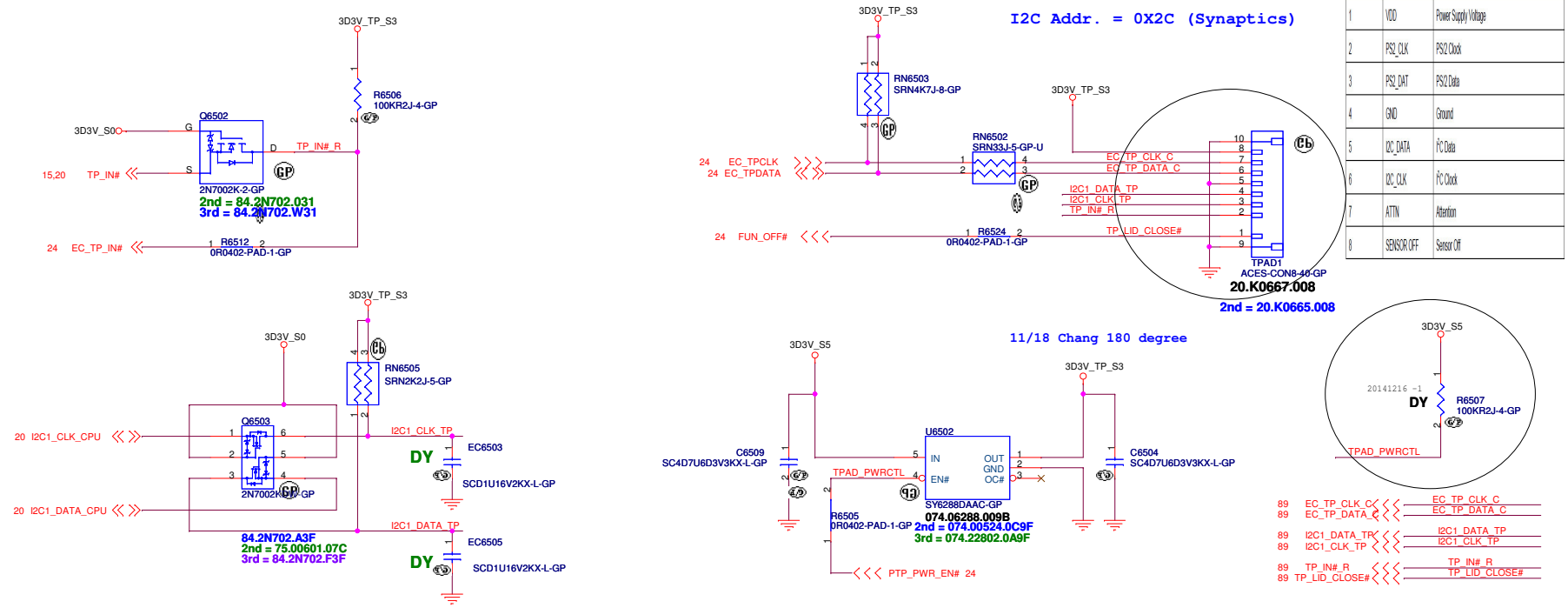
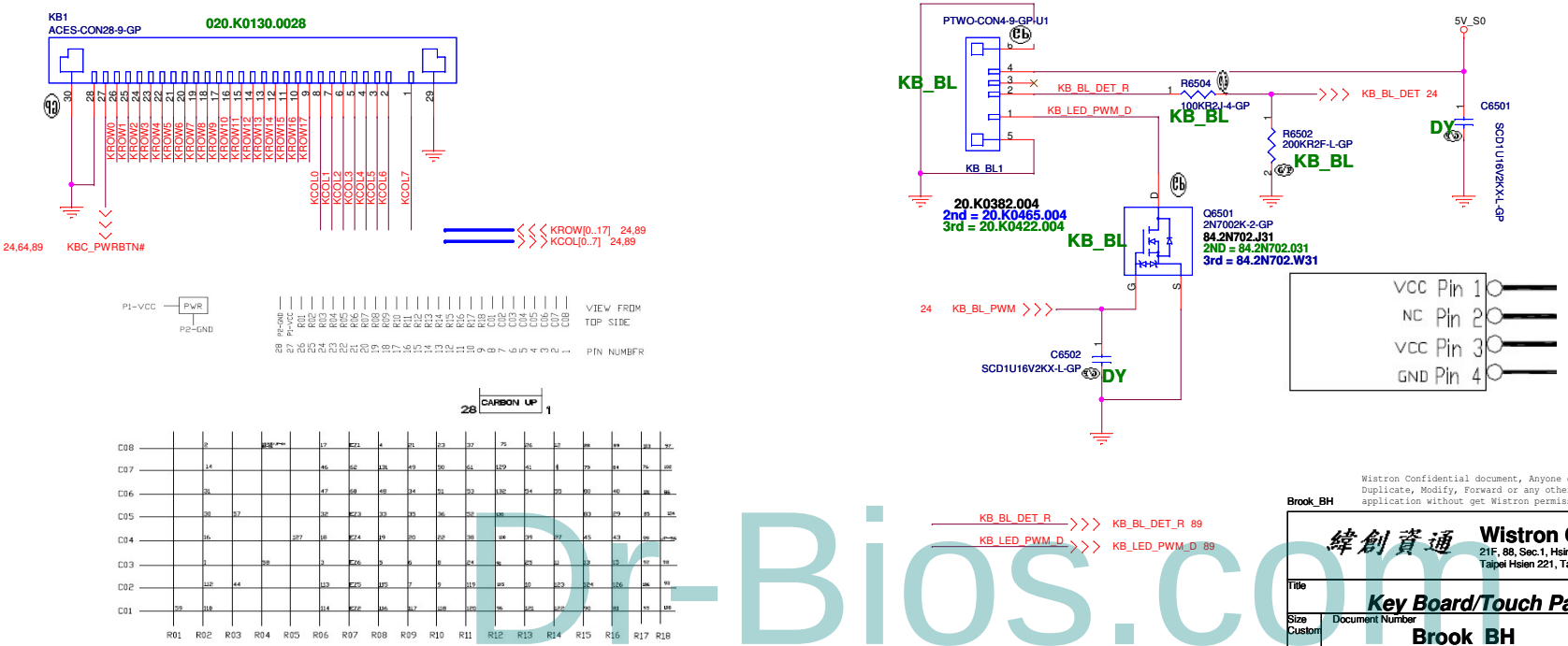
Touch Pad

I2C Addr. = 0X2C (Synaptics)

Pin Number	Pin Name	Description
1	VDD	Power Supply Voltage
2	PS2_CLK	PS/2 Clock
3	PS2_DAT	PS/2 Data
4	GND	Ground
5	I2C_DATA	I²C Data
6	I2C_CLK	I²C Clock
7	ATTN	Attention
8	SENSOR OFF	Sensor Off



Internal KeyBoard Connector



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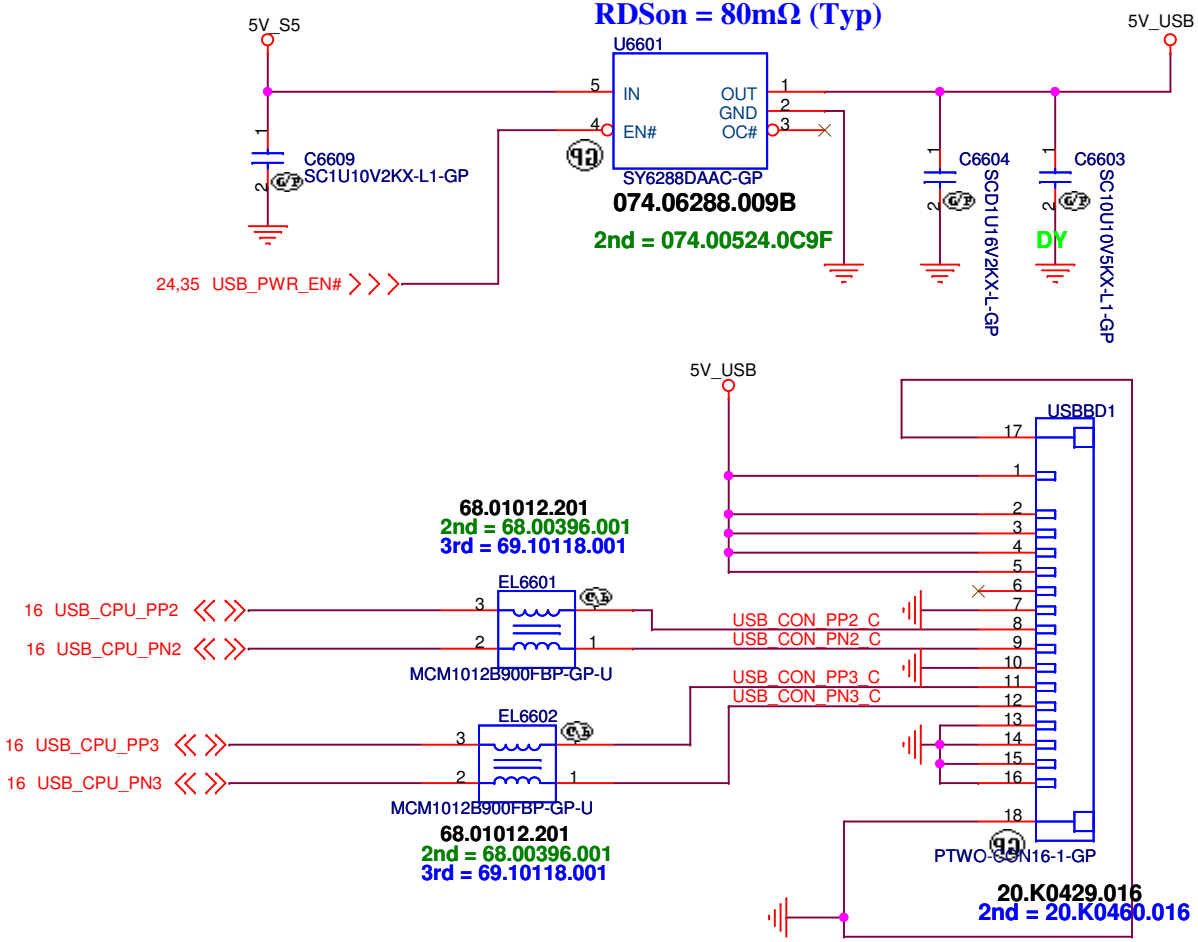

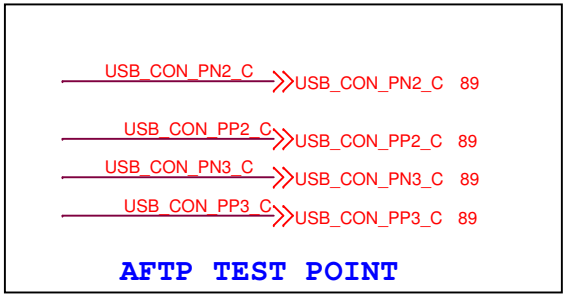

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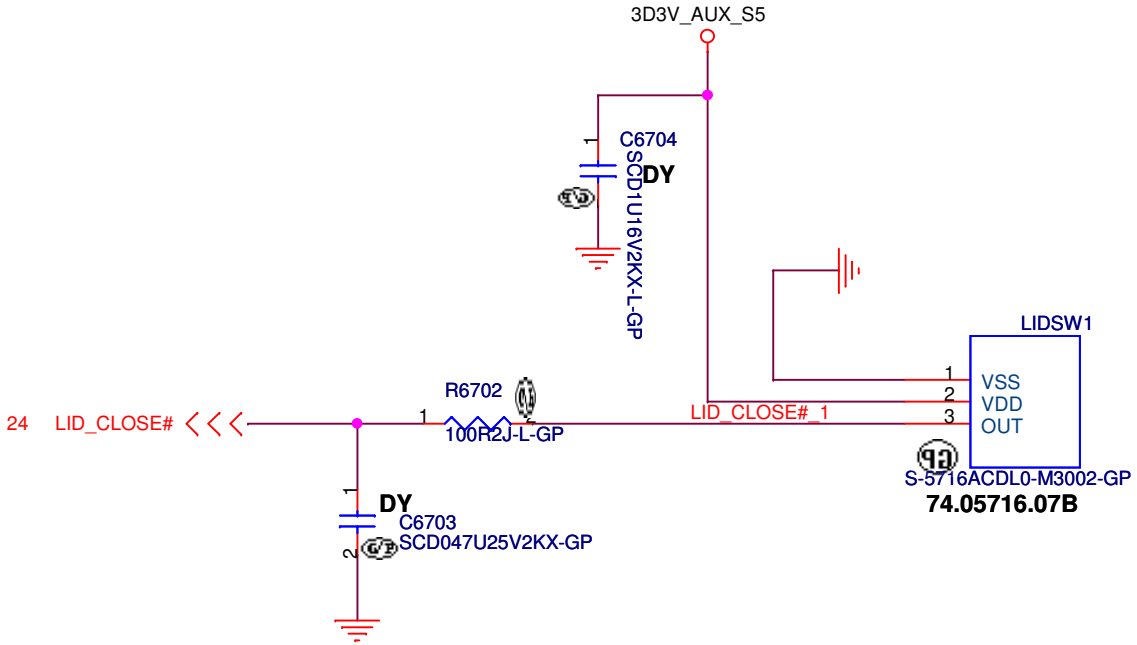

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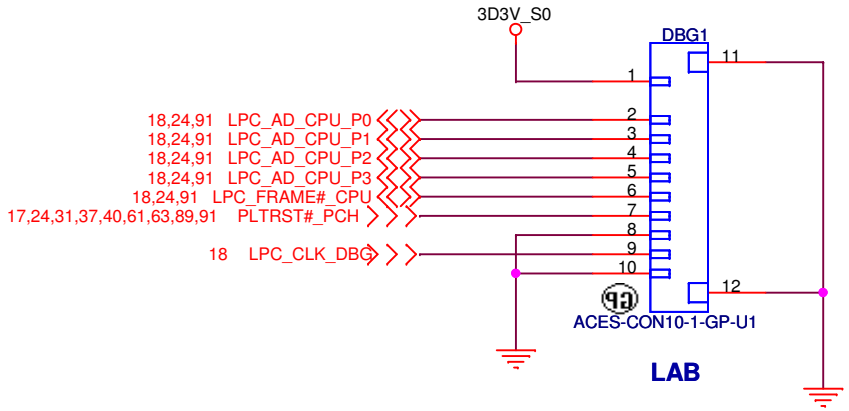

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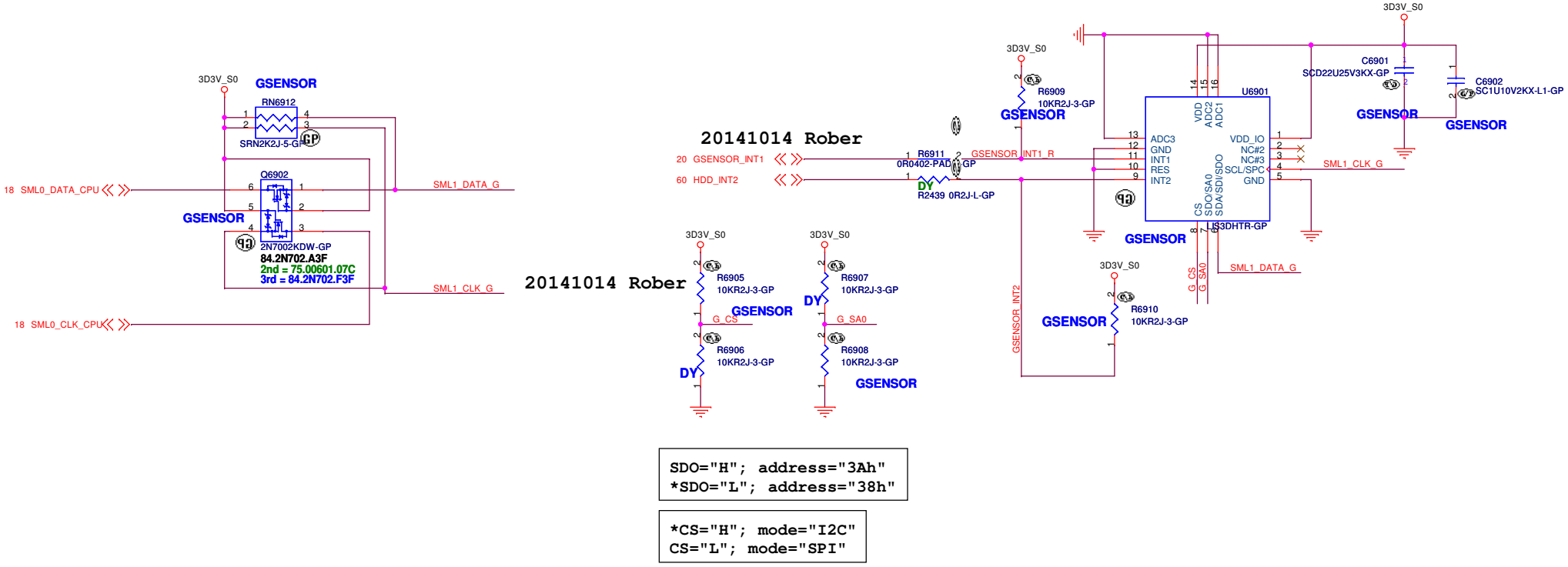
SSID = User.Interface

G Sensor

Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



SDO="H"; address="3Ah"
*SDO="L"; address="38h"

*CS="H"; mode="I2C"
CS="L"; mode="SPI"

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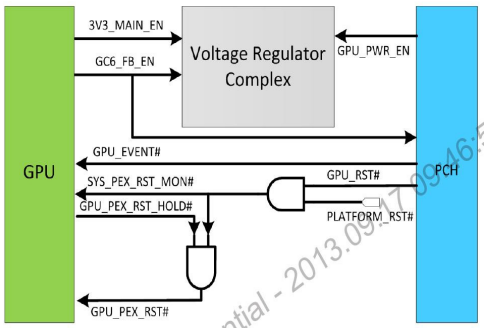

Figure 18-11. GC6 2.0 High-level Signal Connection Concept

3.4.2 PCI Express Power Decoupling and Filtering

Table 3-16. PEX_IOVDD/Q Power Rail Combined

GPU Package Type	Capacitor Type		Footprint	Population	Location
GB2B-64/ GB2-64	1.0 µF	X6S	0402	1	Under GPU
	4.7 µF	X6S	0603	1	Near GPU
	10 µF	X5R	0805	1	Midway between GPU and Power Supply
	22 µF	X5R	0805	1	Midway between GPU and Power Supply
GB4B-128 GB3B-256	1.0 µF	X6S	0402	4	Under GPU
	4.7 µF	X6S	0603	2	Near GPU
	10 µF	X5R	0805	4	Midway between GPU and Power Supply
	22 µF	X5R	0805	4	Midway between GPU and Power Supply

GPU Package Type	Capacitor Type		Footprint	Population	Location
GB2B-64/ GB2-64	1.0 µF	X6S	0402	1	Under GPU
	4.7 µF	X6S	0603	1	Near GPU
	10 µF	X5R	0805	1	Midway between GPU and Power Supply
	22 µF	X5R	0805	1	Midway between GPU and Power Supply

Power current=0.79A

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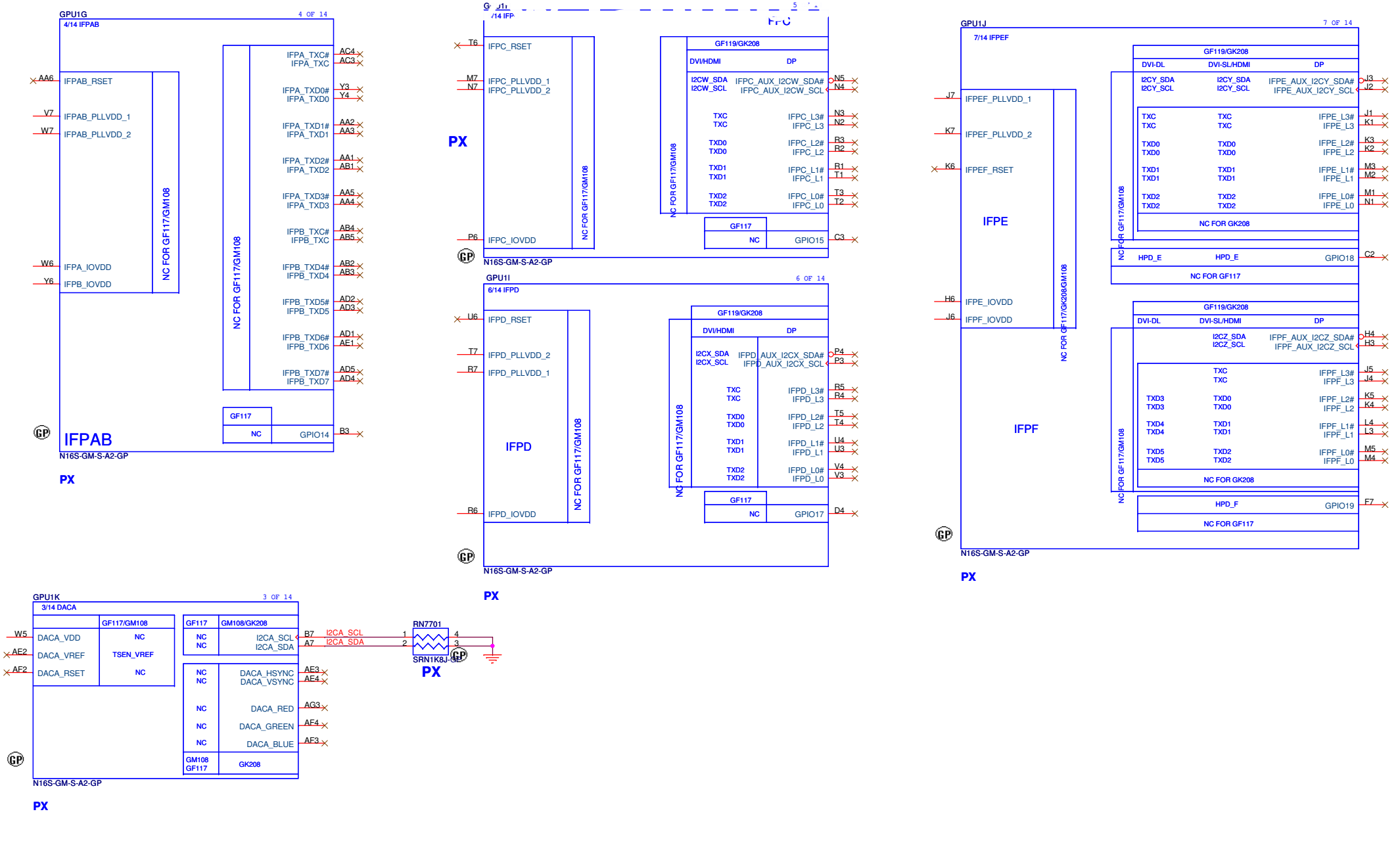

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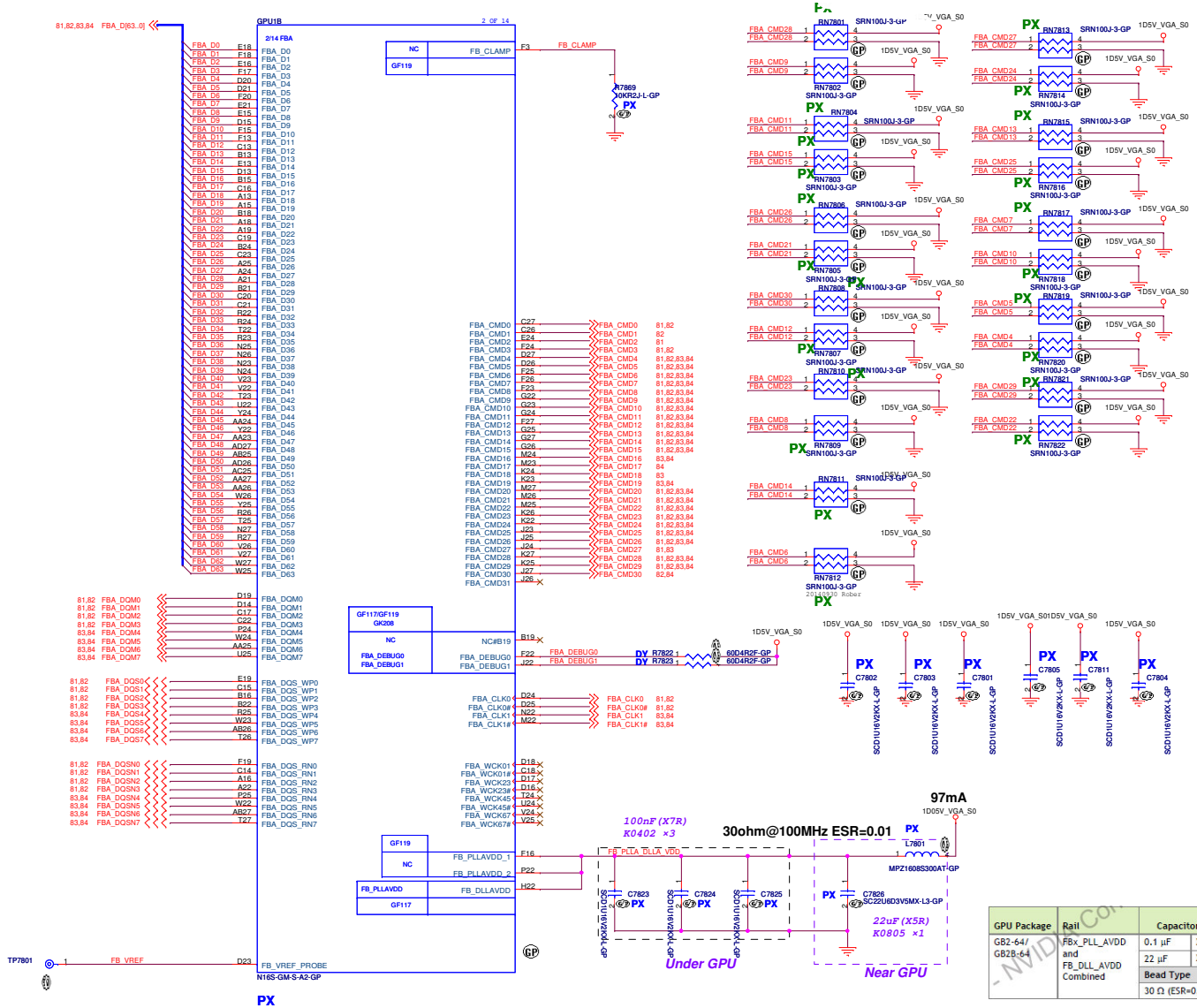


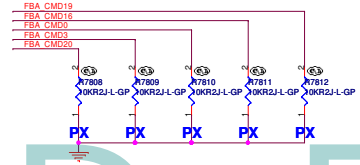
Table 6-4. Mode E Command Mapping

N16x DDR3 Mode E	Rank 0		Rank 1	
	Data Bits [31:0]	Data Bits [63:32]	Data Bits [31:0]	Data Bits [63:32]
FBx_CMD0	ODT		ODT	
FBx_CMD1			CS1*	
FBx_CMD2	CS0*			
FBx_CMD3	CKE		CKE	
FBx_CMD4	A9	A9	A11	A11
FBx_CMD5	A6	A6	A7	A7
FBx_CMD6	A3	A3	BA1	BA1
FBx_CMD7	A0	A0	A12	A12
FBx_CMD8	A8	A8	A8	A8
FBx_CMD9	A12	A12	A0	A0
FBx_CMD10	A1	A1	A2	A2
FBx_CMD11	RAS*	RAS*	RAS*	RAS*
FBx_CMD12	A13	A13	A14	A14
FBx_CMD13	BA1	BA1	A3	A3
FBx_CMD14	A14	A14	A13	A13
FBx_CMD15	CAS*	CAS*	CAS*	CAS*
FBx_CMD16		ODT		ODT
FBx_CMD17				CS1*
FBx_CMD18		CS0*		
FBx_CMD19		CKE		CKE
FBx_CMD20	RST	RST	RST	RST
FBx_CMD21	A7	A7	A6	A6
FBx_CMD22	A4	A4	A5	A5
FBx_CMD23	A11	A11	A9	A9
FBx_CMD24	A2	A2	A1	A1
FBx_CMD25	A10	A10	WE*	WE*
FBx_CMD26	A5	A5	A4	A4
FBx_CMD27	BA2	BA2		
FBx_CMD28	WE*	WE*	A10	A10
FBx_CMD29	BA0	BA0	BA0	BA0
FBx_CMD30		BA2	BA2	
FBx_CMD31				
FBx_CMD32				
FBx_CMD33[1]				
FBx_CMD34	DBG0[2]			
FBx_CMD35	DBG1[2]			

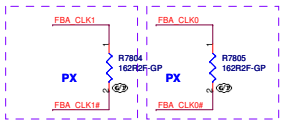
Notes:
1. Not available in GB2-64 and GB2B-64 packages.
2. GPU debug pins; not connected to DRAM. See section 6.1.11.

GPU Package	Rail	Capacitor Type		Footprint	Population	Location
GB2-64/ GB2B-64	FBx_PLL_AVDD and FB_DLL_AVDD Combined	0.1 µF	X7R	0402	2	Under GPU
		22 µF	X5R	0805	1	Near GPU
		Bead Type				
		30 Ω (ESR=0.010 Ω)		0603	1	Near GPU

Memory ODTx, CKEx and RST Termination



FBCLK Termination placed near each VRAM at board edge side



CHECK N16 Design guide P.98 Table 6-7

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Table 3-6. NVVDD Decoupling Footprint and Population

GPU Package Type	Capacitor Type		Footprint	Population		Location	Comments
GB2B-64 / GB2-64	4.7 µF	X6S	0603	10	10	Under GPU	
	1 µF	X6S	0402	4	4	Under GPU	
	47 µF	X5R	0805	1	1	Near GPU	
	22 µF	X5R	0805	1	1	Near GPU	
	4.7 µF	X5R	0805	5	5	Near GPU	
	330 µF	POS	7343	1	1	Near GPU	ESR ≤ 6 mΩ

Power current=26A

Power current=60mA

Power current=1.37A

Table 3-9. DDR3 GPU-Side FBVDD and FBVDDQ Combined Decoupling

GPU Package Type	Capacitor Type		Footprint		Population	Location
GB2B-64/GB2-64 DDR3	0.1µF	X7R	0402	2	2	Under GPU
	1 µF	X7R	0603	2	2	Under GPU
	4.7 µF	X6S	0603	2	2	Under GPU
	10 µF	X5R	0805	1	1	Near GPU
	22 µF	X5R	0805	1	1	Near GPU

CHECK N16 Design guide P.96 6.1.7 GPU Driver Calibration

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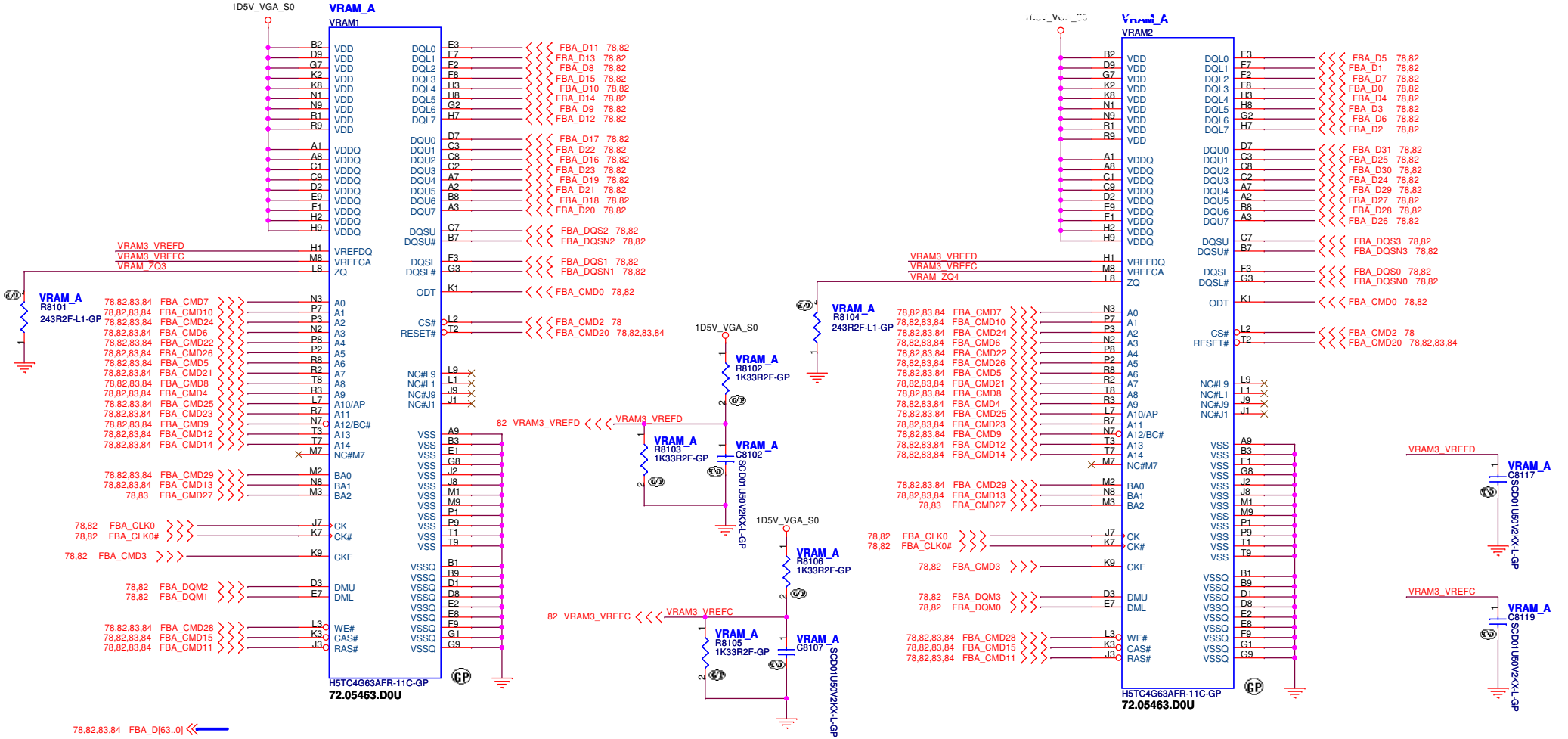
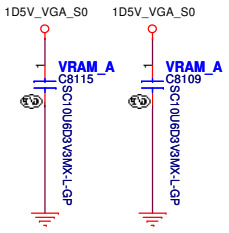




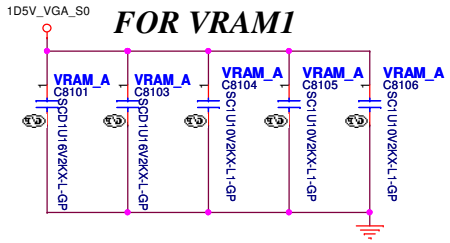
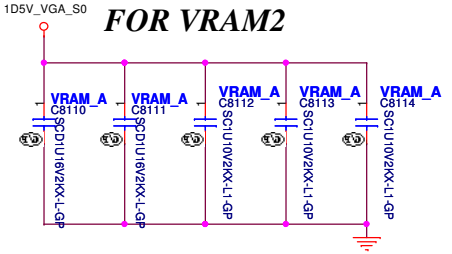
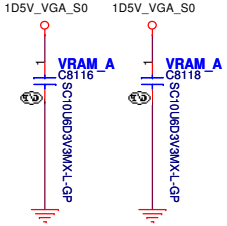


Table 3-11. DDR3 per Memory FBVDD/Q Decoupling

Capacitor Type			Population FBVDDQ	Population FBVDD	Location
FBVDD/Q Combinod					
0.1 µF	X7R	0402	2		Under DRAM
1.0 µF	X7R	0603	4		Under DRAM
10 µF	X5R	0805	0		Close to DRAM
FBVDD/Q Separate					
0.1 µF	X7R	0402	4	2	Under DRAM
1.0 µF	X7R	0603	3	1	Under DRAM
10 µF	X5R	0805	0	0	Close to DRAM

Note: *Location is close to DRAM for clamshell mode.





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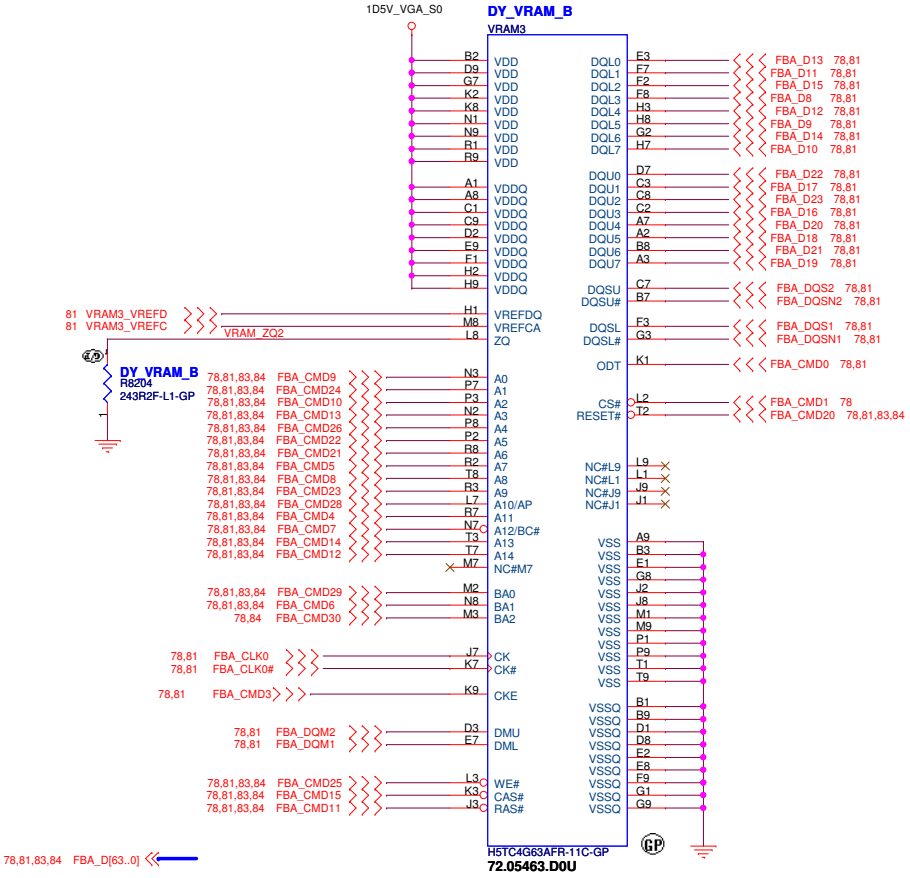

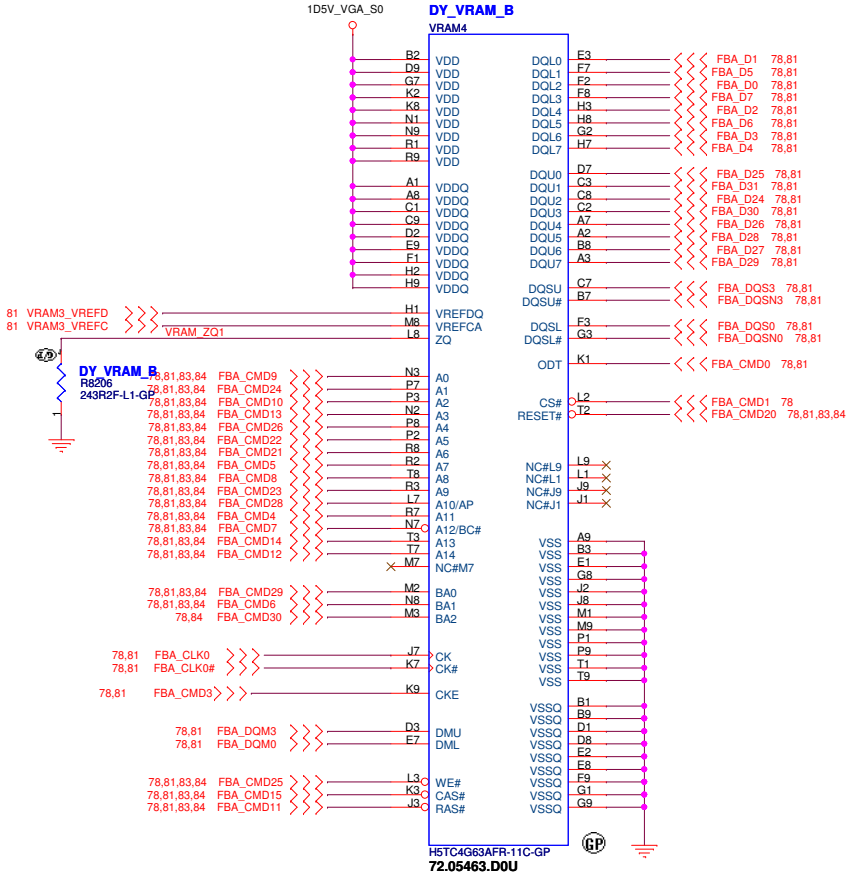

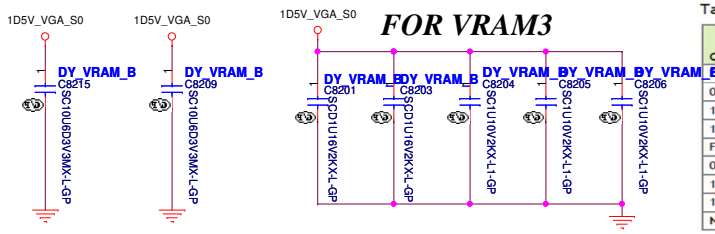

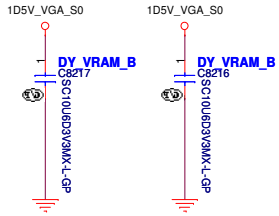

Table 3-11. DDR3 per Memory FBVDD/Q Decoupling

Capacitor Type			Population FBVDDQ	Population FBVDD	Location
FBVDD/Q Combined					
0.1 µF	X7R	0402	2		Under DRAM
1.0 µF	X7R	0603	4		Under DRAM
10 µF	X5R	0805	0		Close to DRAM
FBVDD/Q Separate					
0.1 µF	X7R	0402	4	2	Under DRAM
1.0 µF	X7R	0603	3	1	Under DRAM
10 µF	X5R	0805	0	0	Close to DRAM

Note: *Location is close to DRAM for clamshell mode.

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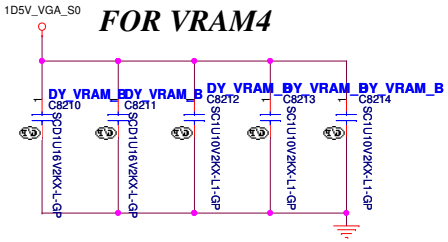

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Title: GPU-VRAM3,4 (2/4)

Size: Custom | Document Number: Brook_BH | Rev: -1M

Date: Wednesday, February 04, 2015 | Sheet 82 of 106

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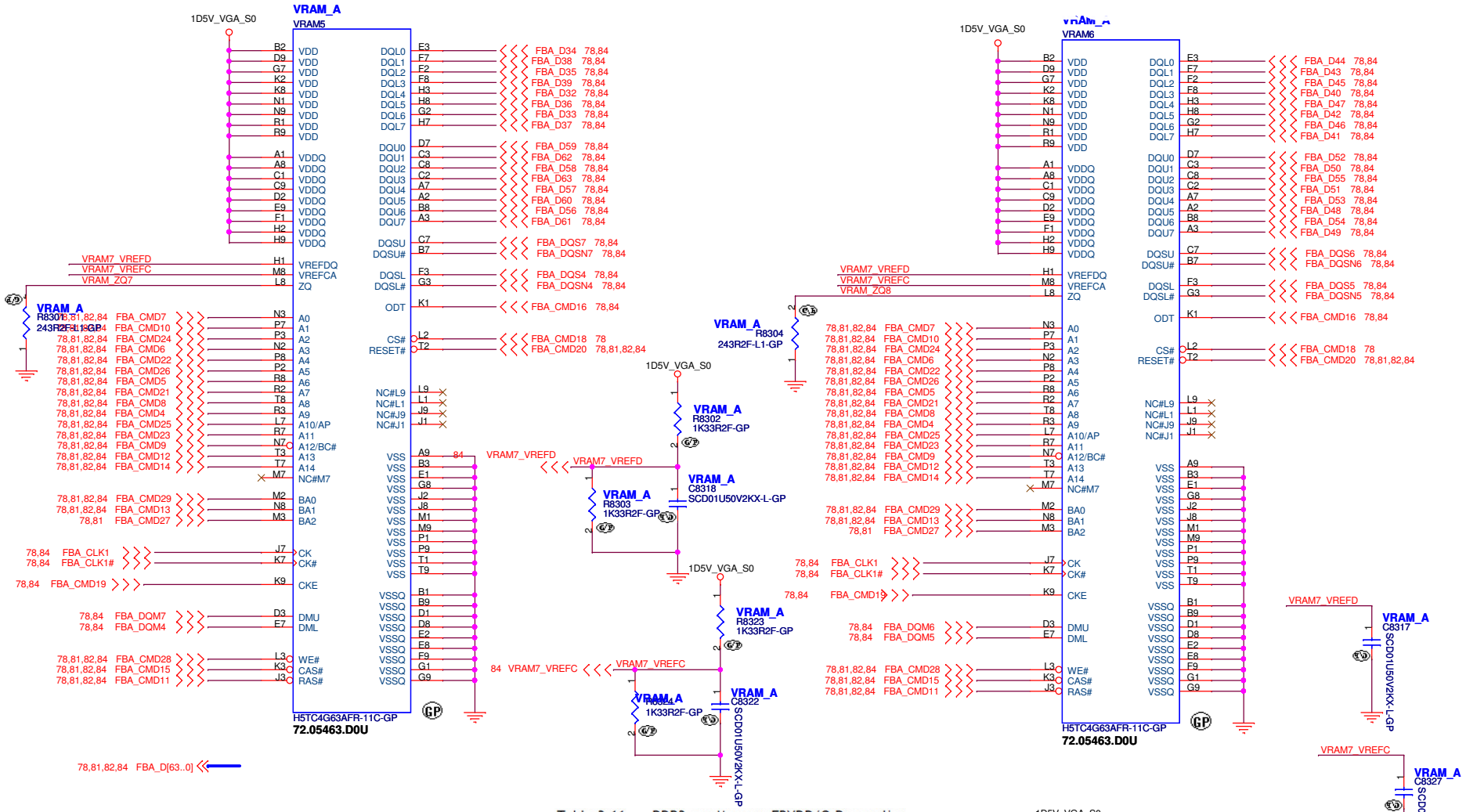

Table 3-11. DDR3 per Memory FBVDD/Q Decoupling

Capacitor Type			Population FBVDDQ	Population FBVDD	Location
FBVDD/Q Combined					
0.1 µF	X7R	0402	2		Under DRAM
1.0 µF	X7R	0603	4		Under DRAM
10 µF	X5R	0805	0		Close to DRAM
FBVDD/Q Separate					
0.1 µF	X7R	0402	4	2	Under DRAM
1.0 µF	X7R	0603	3	1	Under DRAM
10 µF	X5R	0805	0	0	Close to DRAM

Note: *Location is close to DRAM for clamshell mode.

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Title: GPU-VRAM7,8 (4/4)

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Date: Wednesday, February 04, 2015 | Sheet 83 of 106

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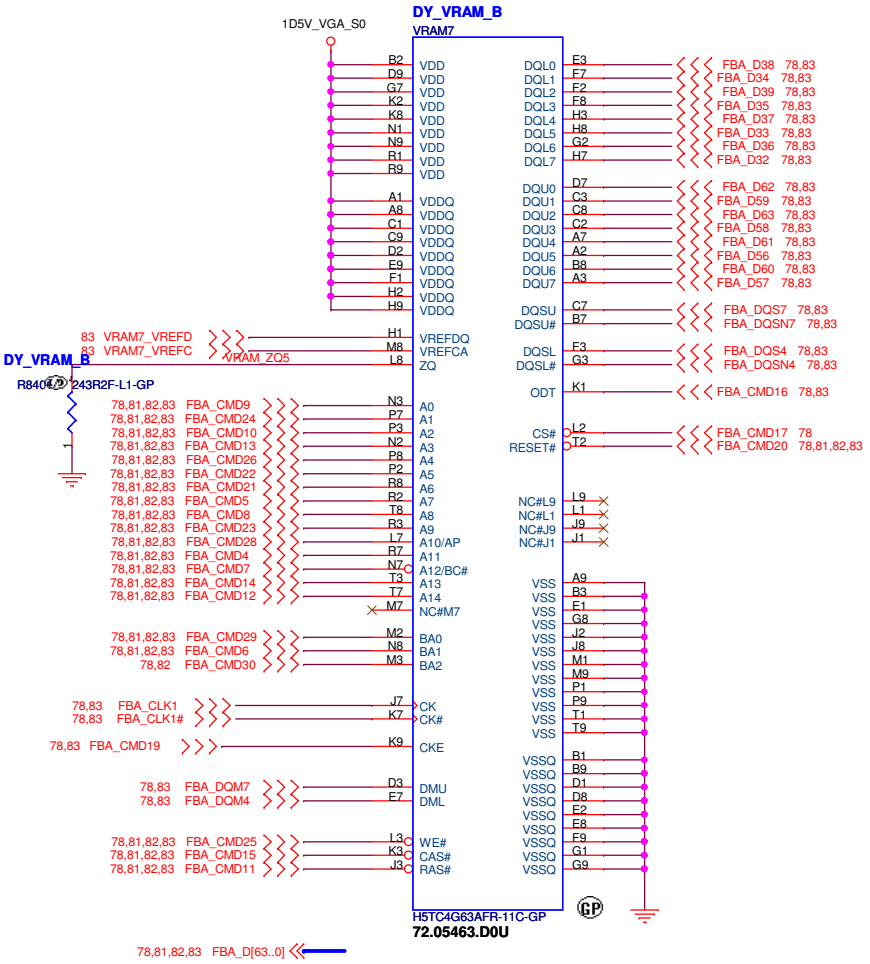

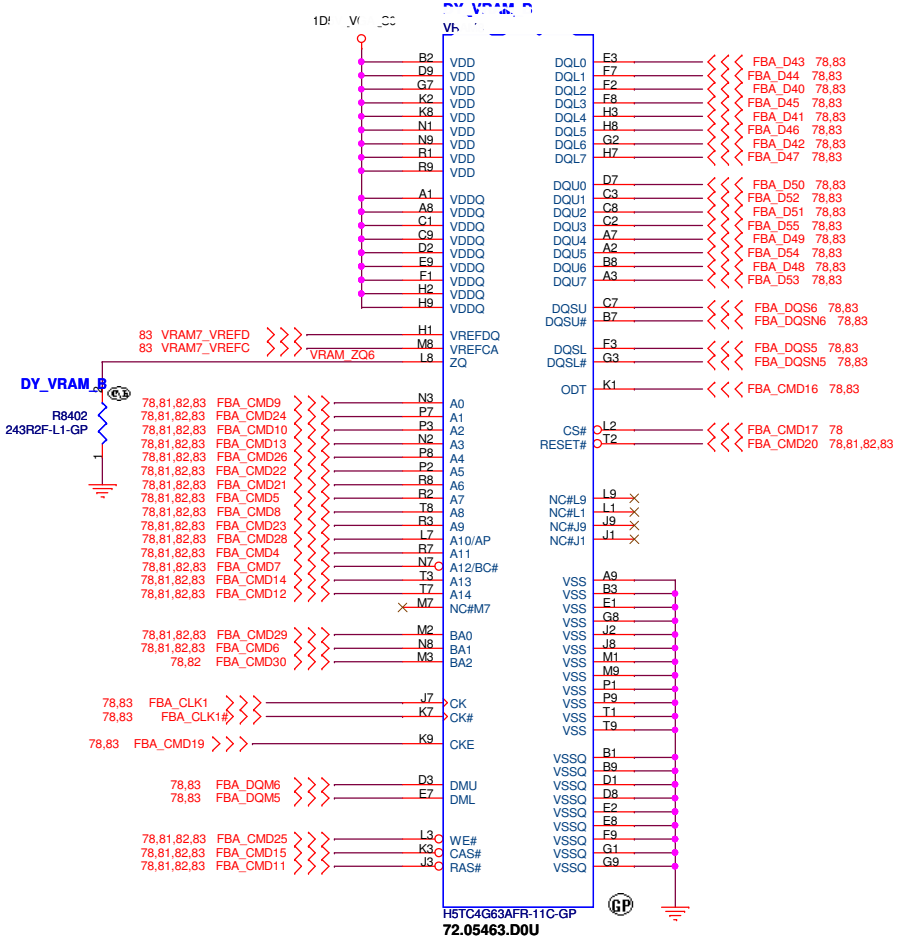

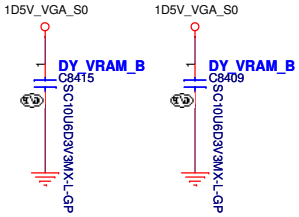

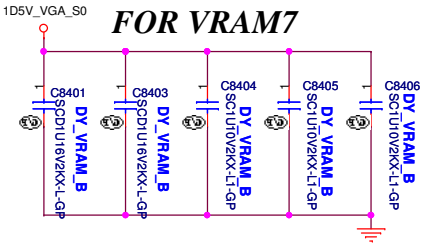

Table 3-11. DDR3 per Memory FBVDD/Q Decoupling

Capacitor Type			Population		Location
			FBVDDQ	FBVDD	
FBVDD/Q Combined					
0.1 µF	X7R	0402	2		Under DRAM
1.0 µF	X7R	0603	4		Under DRAM
10 µF	X5R	0805	0		Close to DRAM
FBVDD/Q Separato					
0.1 µF	X7R	0402	4	2	Under DRAM
1.0 µF	X7R	0603	3	1	Under DRAM
10 µF	X5R	0805	0	0	Close to DRAM

Note: *Location is close to DRAM for clamshell mode.

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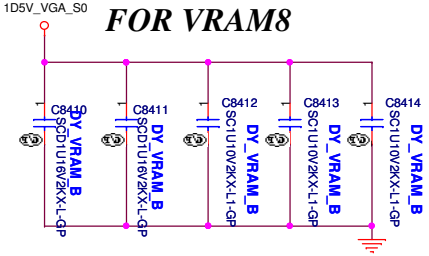

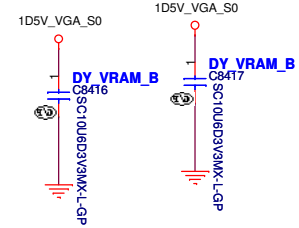

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Title: GPU-VRAM7,8 (4/4)

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Date: Wednesday, February 04, 2015 | Sheet 84 of 106

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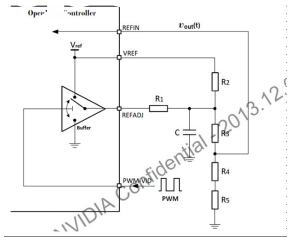
PWM-VID Spec and Component Values

PWM-VID Specification		Config A	Config B	Config C	Config D
Vmin	V	0.6	0.6	0.65	0.9
Vmax	V	1.2	1.2	1.15	1.15
Vboot	V	0.875	0.9	0.9	1.028
Voltage Step Vstep	mV	6.25	6.25	25	12.5
Number of Voltage Levels N	level	96	96	20	20
PWM Frequency F_{PWM}	MHz	1.125	1.125	0.676	0.676
PWM Minimum Pulse Width T_{DMIN}	ns	9.26	9.26	74	74
VID Transient Time T	us	<100	<100	<100	<100
Component Value					
R1 (1%)	KΩ	39	20	39	27
R2 (1%)	KΩ	39	20	30	7.5
R3 (1%)	KΩ	1.5	2	3	0
R4 (1%)	KΩ	30	18	24	6.2
R5 (1%)	KΩ	1.5	0	3	1.74
C	nF	1.5	2.7	1.8	5.6



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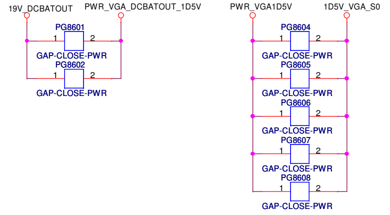
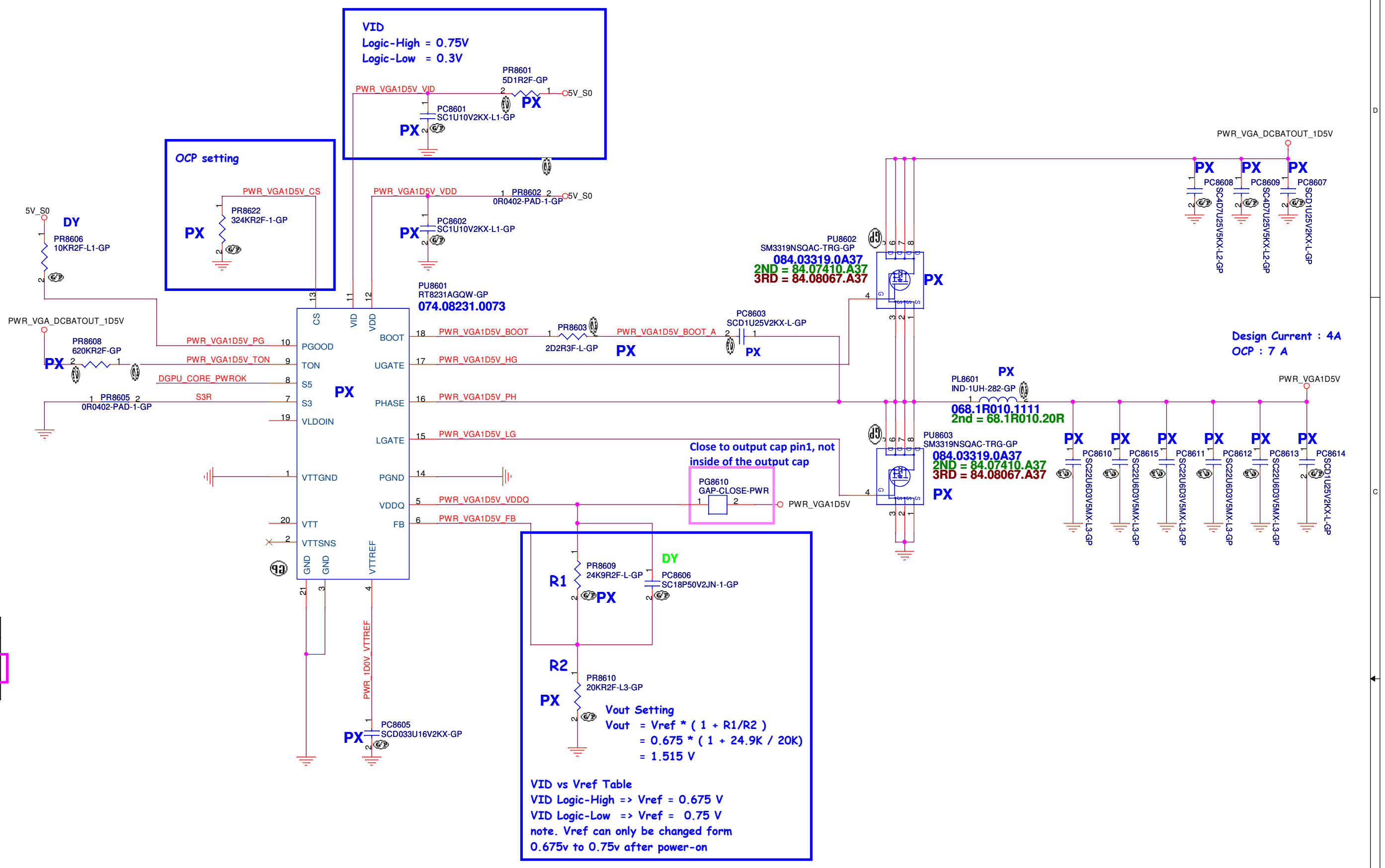
Title: RT8812A_VGA_CORE

Size	Document Number	Rev
Custom	Brook_BL	-1M

Date: Wednesday, February 04, 2015 Sheet 85 of 106

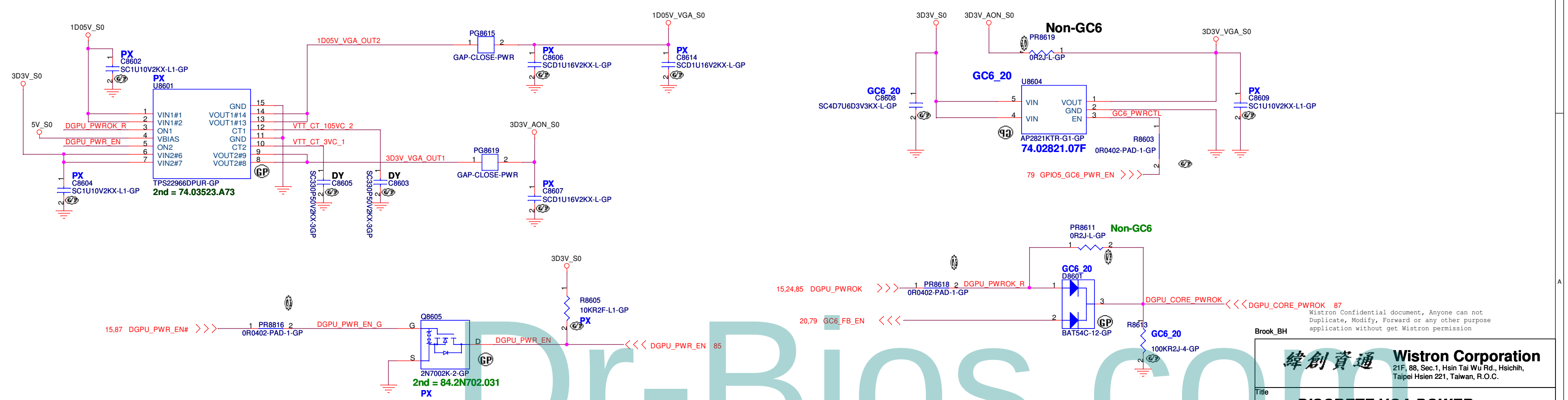




VID
Logic-High = 0.75V
Logic-Low = 0.3V
PR8601
5D1R2F-GP
PWR_VGA1D5V_VID
PC8601
SC1U10V2KX-L1-GP
OCP setting
PWR_VGA1D5V_CS
PR8622
324KR2F-1-GP
PWR_VGA1D5V_VDD
PR8602
0R0402-PAD-1-GP
PC8602
SC1U10V2KX-L1-GP
5V_S0
PR8606
10KR2F-L1-GP
PWR_VGA_DCBATOUT_1D5V
PR8608
620KR2F-GP
PWR_VGA1D5V_PG
PWR_VGA1D5V_TON
DGPU_CORE_PWROK
PR8605
0R0402-PAD-1-GP
S3R
PU8601
RT8231AGQW-GP
074.08231.0073
PGOOD
TON
S5
S3
VLDOIN
VTTGND
VTT
VTTSNS
BOOT
UGATE
PHASE
LGATE
PGND
VDDQ
FB
VTTREF
PWR_VGA1D5V_BOOT
PR8603
2D2R3F-L-GP
PWR_VGA1D5V_BOOT_A
PC8603
SCD1U25V2KX-L-GP
PWR_VGA1D5V_HG
PWR_VGA1D5V_PH
PWR_VGA1D5V_LG
PWR_VGA1D5V_VDDQ
PWR_VGA1D5V_FB
PU8602
SM3319NSQAC-TRG-GP
084.03319.0A37
2ND = 84.07410.A37
3RD = 84.08067.A37
PU8603
SM3319NSQAC-TRG-GP
084.03319.0A37
2ND = 84.07410.A37
3RD = 84.08067.A37
PL8601
IND-1UH-282-GP
068.1R010.1111
2nd = 68.1R010.20R
Design Current : 4A
OCP : 7 A
PWR_VGA1D5V
PC8608
PC8609
PC8607
PC8610
PC8615
PC8611
PC8612
PC8613
PC8614
Close to output cap pin1, not inside of the output cap
PG8610
GAP-CLOSE-PWR
R1
PR8609
24K9R2F-L-GP
PC8606
SC18P50V2JN-1-GP
R2
PR8610
20KR2F-L3-GP
Vout Setting
Vout = Vref * (1 + R1/R2)
= 0.675 * (1 + 24.9K / 20K)
= 1.515 V
VID vs Vref Table
VID Logic-High => Vref = 0.675 V
VID Logic-Low => Vref = 0.75 V
note. Vref can only be changed form
0.675v to 0.75v after power-on
PWR_1D0V_VTTREF
PC8605
SCD033U16V2KX-GP

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

3D3V_S0 to 3D3V_VGA_S0
1D05V_S0 to 1D05V_VGA_S0



1D05V_S0
3D3V_S0
C8602
SC1U10V2KX-L1-GP
U8601
5V_S0
DGPU_PWROK_R
DGPU_PWR_EN
VIN1#1
VIN1#2
ON1
VBIAS
ON2
VIN2#6
VIN2#7
GND
VOUT1#14
VOUT1#13
CT1
GND
CT2
VOUT2#9
VOUT2#8
TPS22966DPUR-GP
2nd = 74.03523.A73
C8604
SC1U10V2KX-L1-GP
1D05V_VGA_OUT2
VTT_CT_105VC_2
VTT_CT_3VC_1
3D3V_VGA_OUT1
C8605
C8603
PG8615
GAP-CLOSE-PWR
C8606
SCD1U16V2KX-L-GP
1D05V_VGA_S0
C8614
SCD1U16V2KX-L-GP
3D3V_AON_S0
PG8619
GAP-CLOSE-PWR
C8607
SCD1U16V2KX-L-GP
3D3V_S0
3D3V_AON_S0
Non-GC6
PR8619
0R2J-L-GP
3D3V_VGA_S0
GC6_20
C8608
SC4D7U6D3V3KX-L-GP
GC6_20
U8604
VIN
VIN
VOUT
GND
EN
AP2821KTR-G1-GP
74.02821.07F
GC6_PWRCTL
R8603
0R0402-PAD-1-GP
C8609
SC1U10V2KX-L1-GP
GPIO5_GC6_PWR_EN
PR8611
0R2J-L-GP
Non-GC6
GC6_20
D8601
DGPU_PWROK
PR8618
0R0402-PAD-1-GP
DGPU_PWROK_R
DGPU_CORE_PWROK
GC6_FB_EN
BAT54C-12-GP
R8613
GC6_20
100KR2J-4-GP
3D3V_S0
R8605
10KR2F-L1-GP
DGPU_PWR_EN#
PR8816
0R0402-PAD-1-GP
DGPU_PWR_EN_G
Q8605
DGPU_PWR_EN
2N7002K-2-GP
2nd = 84.2N702.031

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Title: DISCRETE VGA POWER

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Date: Thursday, February 05, 2015 | Sheet 86 of 106

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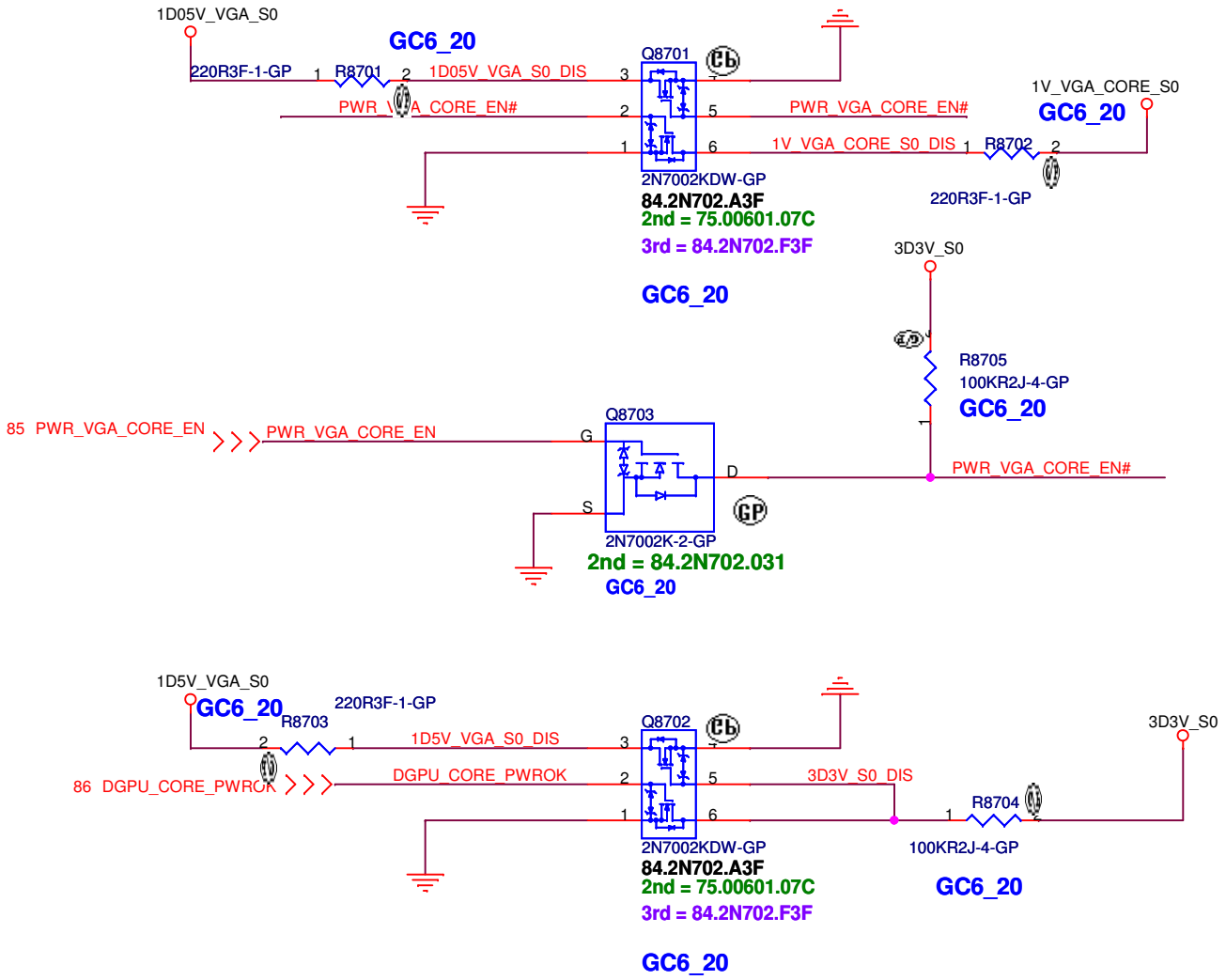

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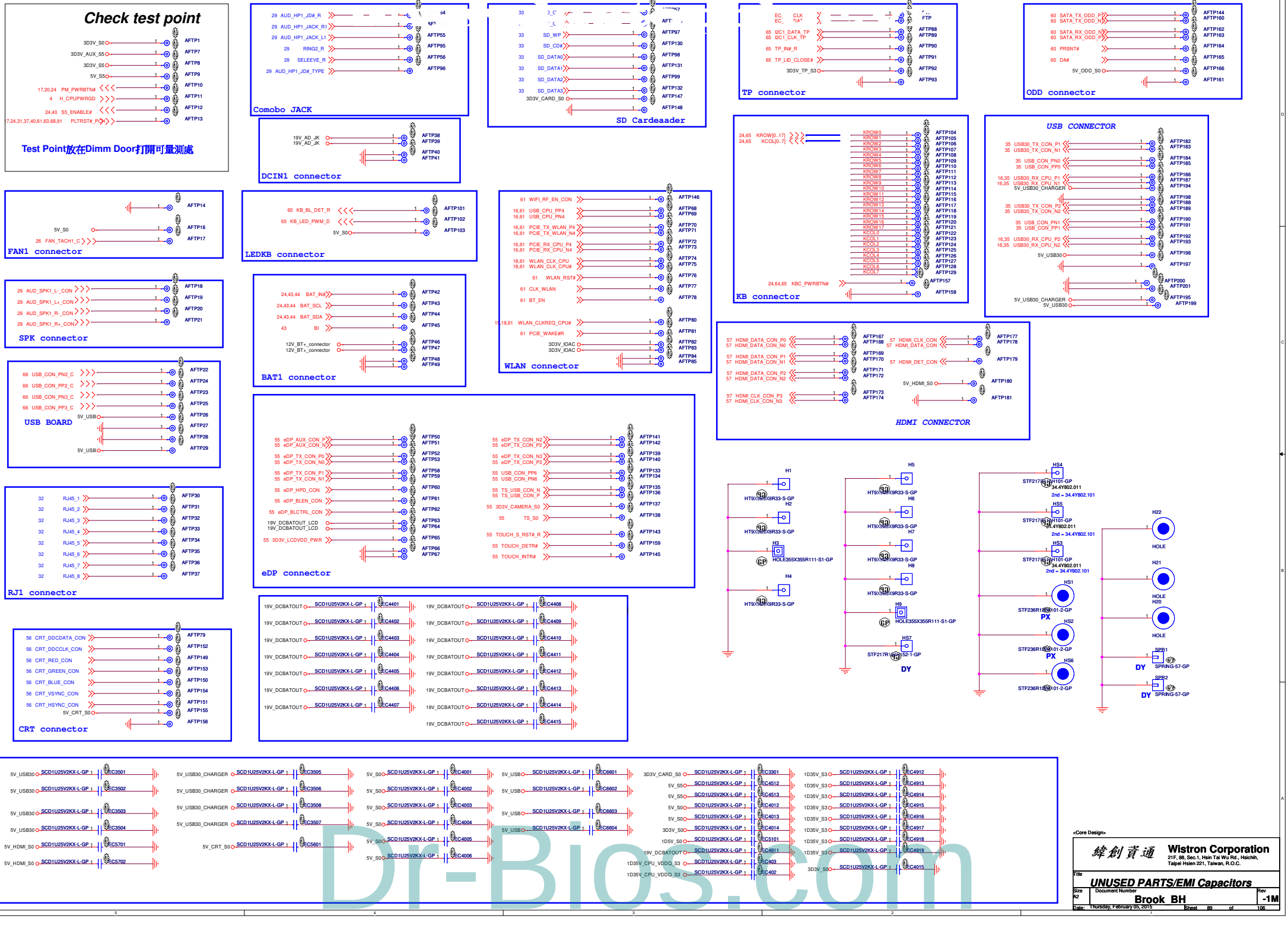
Check test point
3D3V_S0 AFTP1
3D3V_AUX_S5 AFTP7
3D3V_S5 AFTP8
5V_S5 AFTP9
17,20,24 PM_PWRBTN# AFTP10
4 H_CPUPWRGD AFTP11
24,40 S5_ENABLE# AFTP12
7,24,31,37,40,61,63,68,91 PLTRST#_P AFTP13
Test Point放在Dimm Door打開可量測處
Comobo JACK
AUD_HP1_JD#_R
AUD_HP1_JACK_R1
AUD_HP1_JACK_L1
RING2_R
SELEEVE_R
AUD_HP1_JD#_TYPE
SD Cardeaader
SD_WP
SD_CD#
SD_DATA0
SD_DATA1
SD_DATA2
SD_DATA3
3D3V_CARD_S0
TP connector
I2C1_DATA_TP
I2C1_CLK_TP
TP_INT_R
TP_LID_CLOSE#
3D3V_TP_S3
ODD connector
SATA_TX_ODD_P
SATA_TX_ODD_N
SATA_RX_ODD_N
SATA_RX_ODD_P
PRSNT#
DA#
5V_ODD_S0
DCIN1 connector
19V_AD_JK
FAN1 connector
5V_S0
FAN_TACH1_C
LEDKB connector
KB_BL_DET_R
KB_LED_PWM_D
KB connector
KROW[0..17]
KCOL[0..7]
KBC_PWRBTN#
USB CONNECTOR
USB30_TX_CON_P1
USB30_TX_CON_N1
USB_CON_PN0
USB_CON_PP0
USB30_RX_CPU_P1
USB30_RX_CPU_N1
5V_USB30_CHARGER
USB30_TX_CON_P2
USB30_TX_CON_N2
USB_CON_PN1
USB_CON_PP1
USB30_RX_CPU_P2
USB30_RX_CPU_N2
5V_USB30
SPK connector
AUD_SPK1_L-_CON
AUD_SPK1_L+_CON
AUD_SPK1_R-_CON
AUD_SPK1_R+_CON
BAT1 connector
BAT_IN#
BAT_SCL
BAT_SDA
BI
12V_BT+_connector
WLAN connector
WIFI_RF_EN_CON
USB_CPU_PP4
USB_CPU_PN4
PCIE_TX_WLAN_P4
PCIE_TX_WLAN_N4
PCIE_RX_CPU_P4
PCIE_RX_CPU_N4
WLAN_CLK_CPU
WLAN_CLK_CPU#
WLAN_RST#
CLK_WLAN
BT_EN
WLAN_CLKREQ_CPU#
PCIE_WAKE#R
3D3V_IOAC
HDMI CONNECTOR
HDMI_DATA_CON_P0
HDMI_DATA_CON_N0
HDMI_DATA_CON_P1
HDMI_DATA_CON_N1
HDMI_DATA_CON_P2
HDMI_DATA_CON_N2
HDMI_CLK_CON_P3
HDMI_CLK_CON_N3
HDMI_CLK_CON
HDMI_DET_CON
5V_HDMI_S0
USB BOARD
USB_CON_PN2_C
USB_CON_PP2_C
USB_CON_PN3_C
USB_CON_PP3_C
5V_USB
eDP connector
eDP_AUX_CON_P
eDP_AUX_CON_N
eDP_TX_CON_P0
eDP_TX_CON_N0
eDP_TX_CON_P1
eDP_TX_CON_N1
eDP_HPD_CON
eDP_BLEN_CON
eDP_BLCTRL_CON
19V_DCBATOUT_LCD
3D3V_LCDVDD_PWR
eDP_TX_CON_N2
eDP_TX_CON_P2
eDP_TX_CON_N3
eDP_TX_CON_P3
USB_CON_PP6
USB_CON_PN6
TS_USB_CON_N
TS_USB_CON_P
3D3V_CAMERA_S0
TS_S0
TOUCH_S_RST#_R
TOUCH_DETR#
TOUCH_INTR#
RJ1 connector
RJ45_1
RJ45_2
RJ45_3
RJ45_4
RJ45_5
RJ45_6
RJ45_7
RJ45_8
CRT connector
CRT_DDCDATA_CON
CRT_DDCCLK_CON
CRT_RED_CON
CRT_GREEN_CON
CRT_BLUE_CON
CRT_VSYNC_CON
CRT_HSYNC_CON
5V_CRT_S0
SCD1U25V2KX-L-GP
19V_DCBATOUT
5V_USB30
5V_USB30_CHARGER
5V_S0
5V_USB
3D3V_CARD_S0
5V_S5
5V_HDMI_S0
1D5V_S0
3D3V_S0
19V_DCBATOUT
1D35V_CPU_VDDQ_S3
1D35V_S3
3D3V_S0
HT9X355X9R33-S-GP
HOLE355X355R111-S1-GP
STF217R152-1-GP
STF236R101-2-GP
SPRING-57-GP
PX
DY
HOLE
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UNUSED PARTS/EMI Capacitors
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-1M
Thursday, February 05, 2015
Sheet 89 of 106

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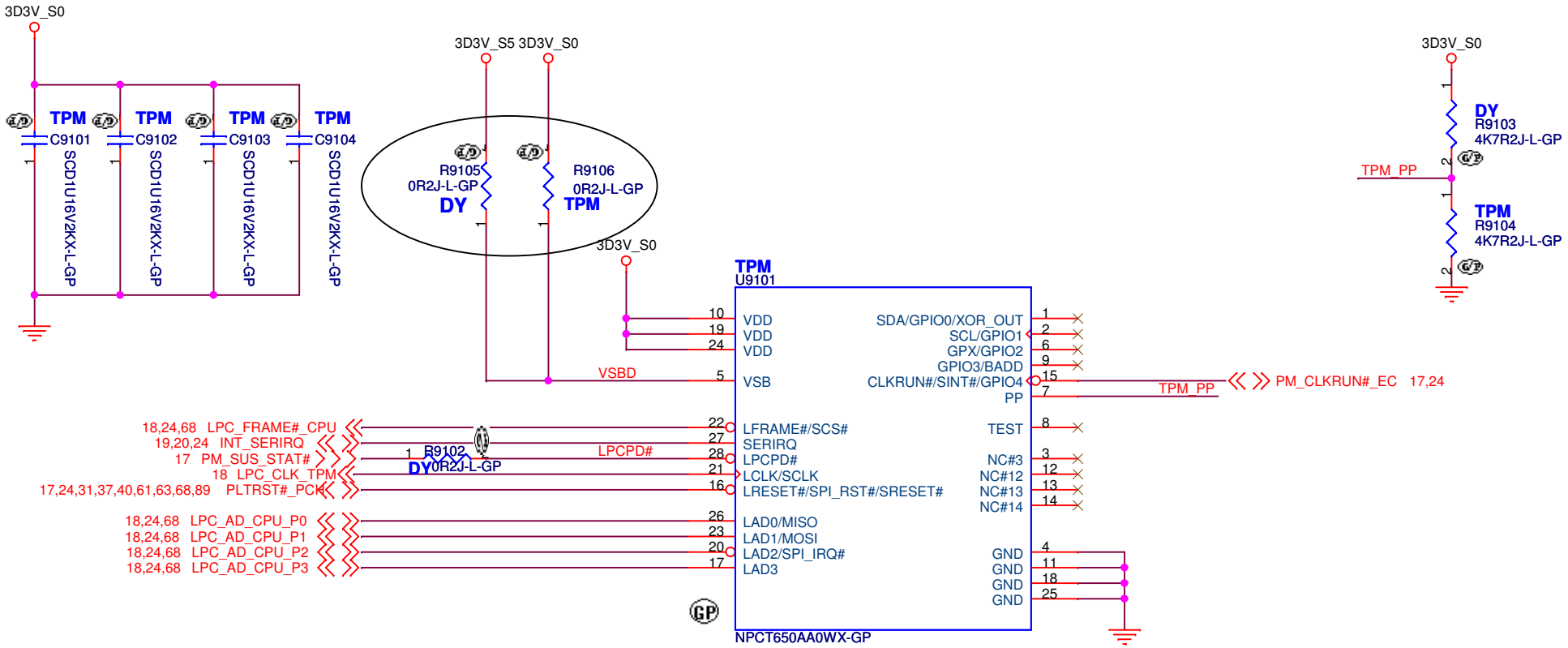

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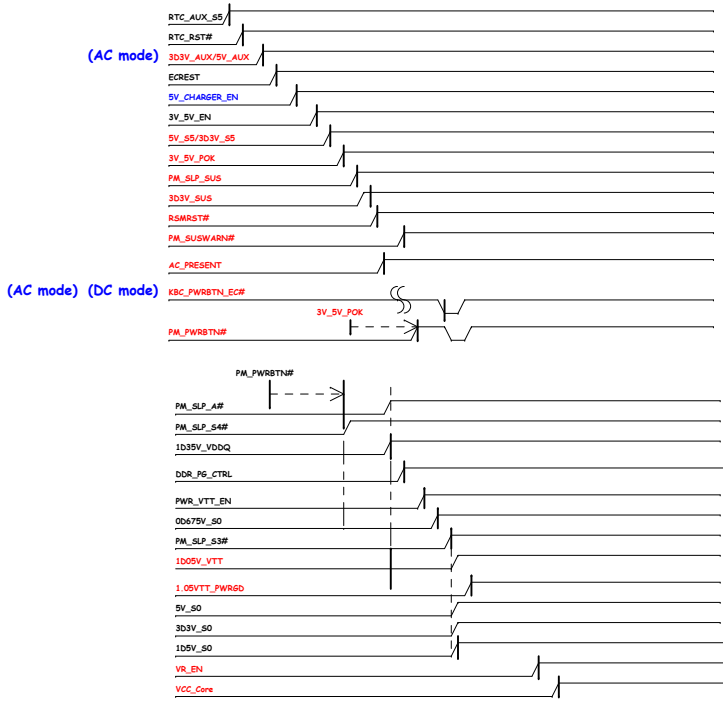
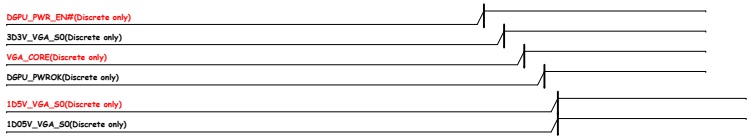
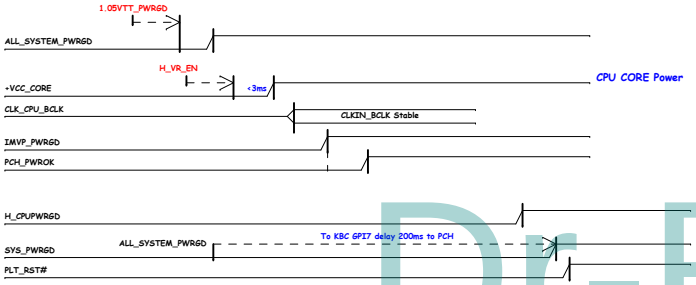
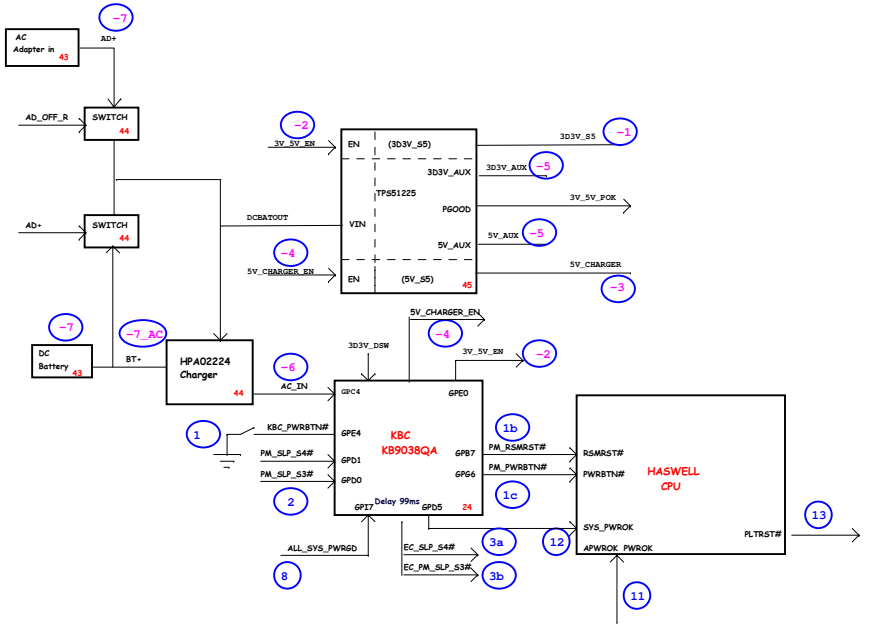
Intel-Power Up Sequence

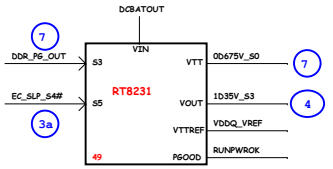


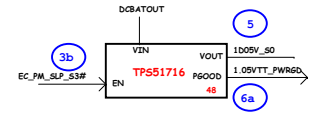


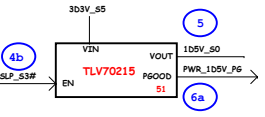


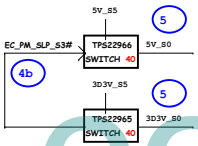
HASWELL POWER UP SEQUENCE DIAGRAM

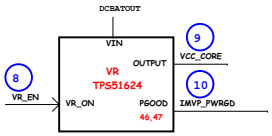


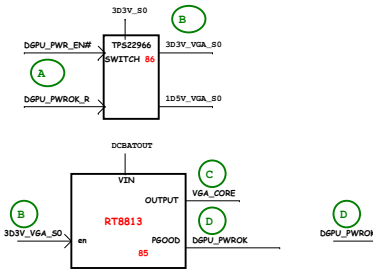












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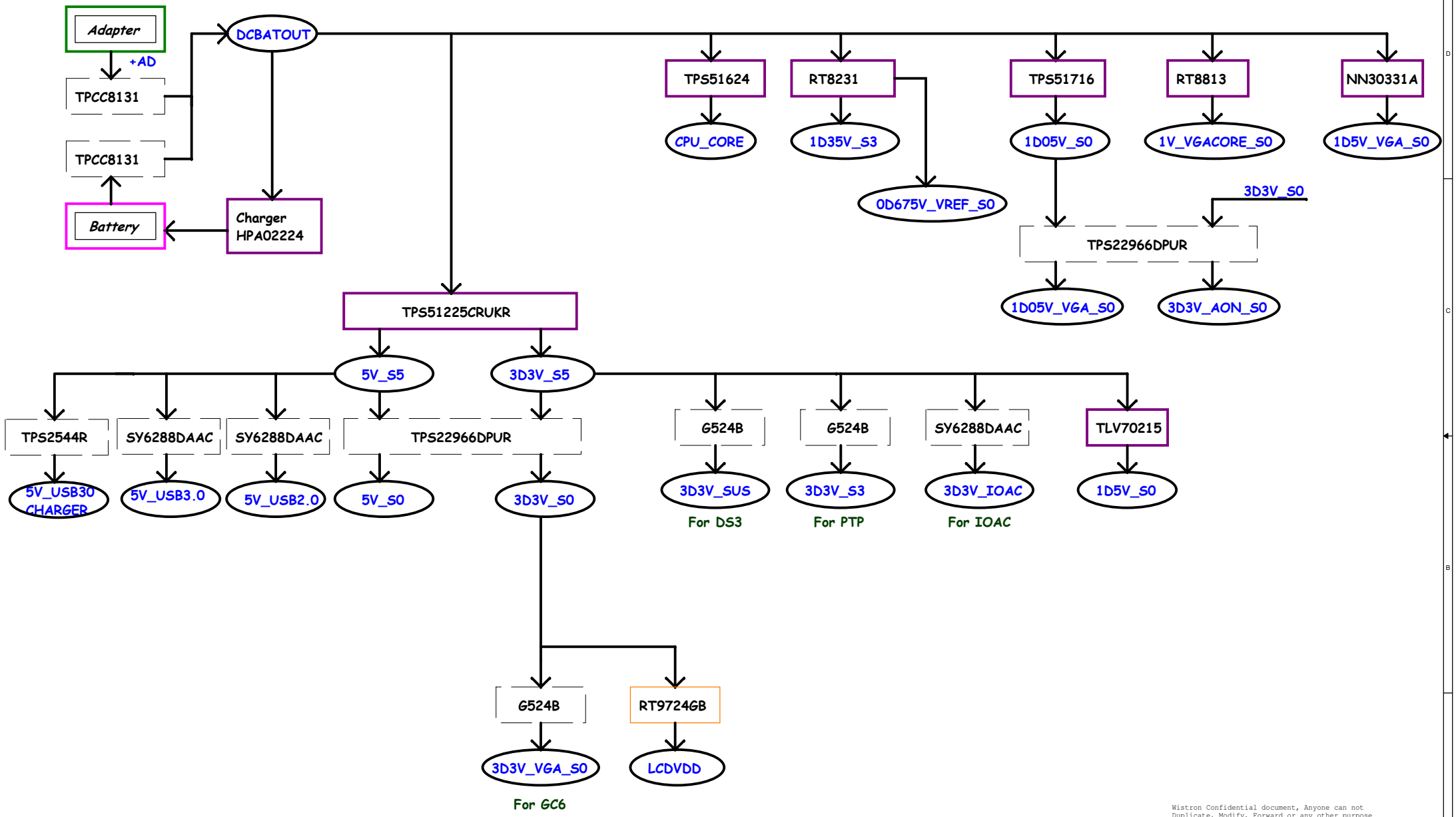

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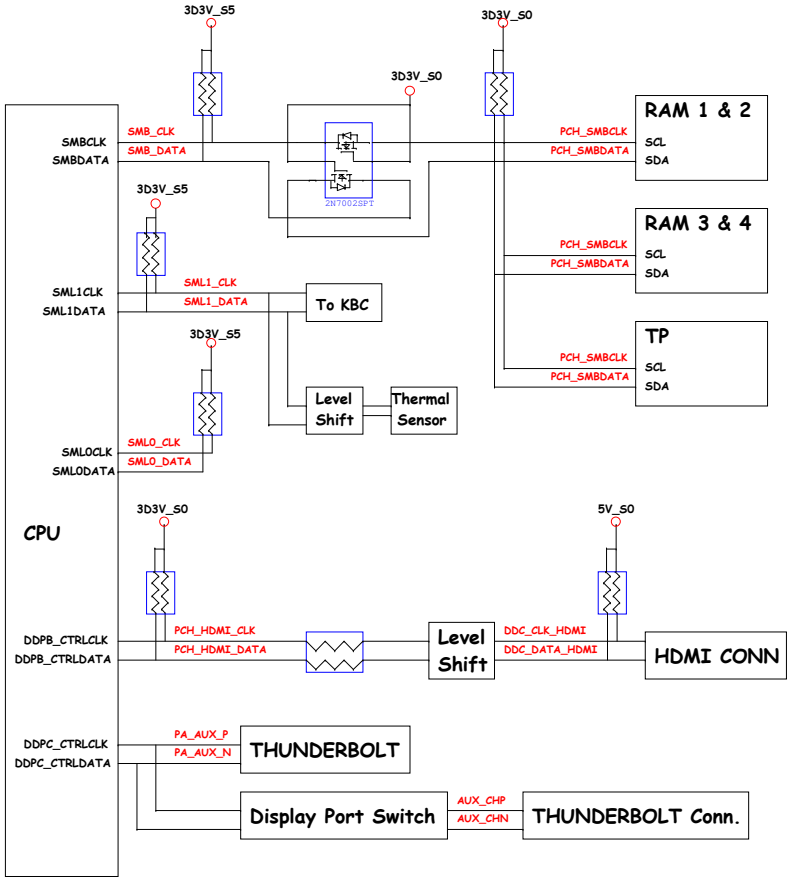
PCH SMBus Block Diagram



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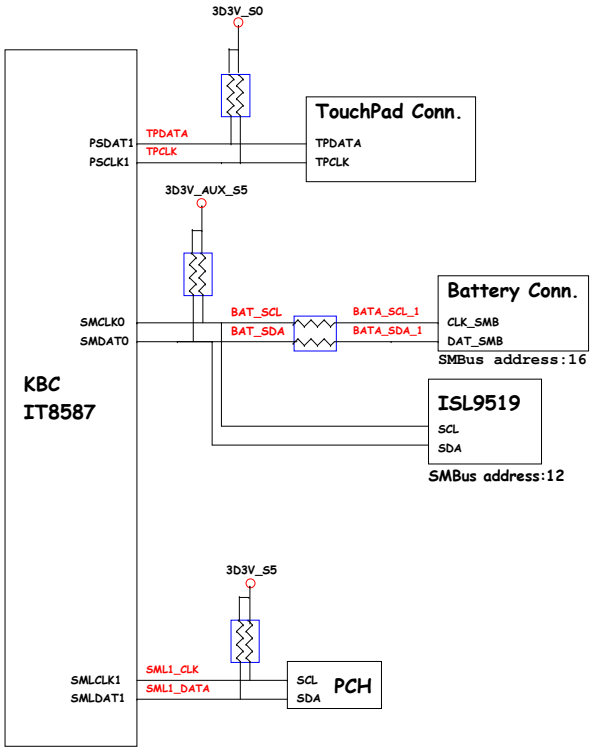

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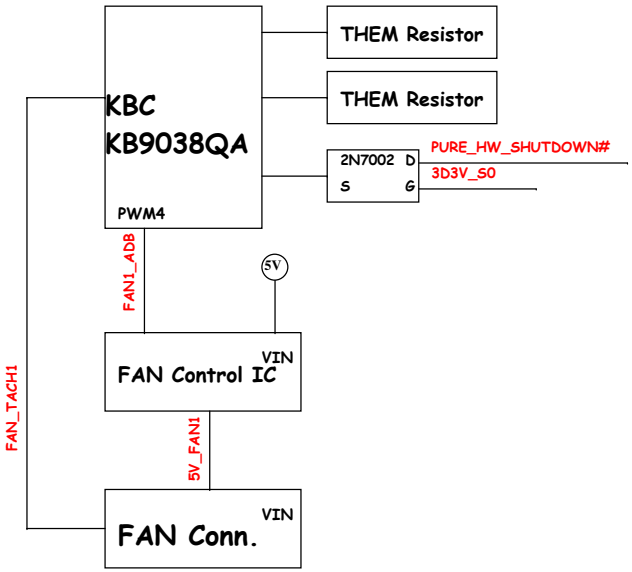
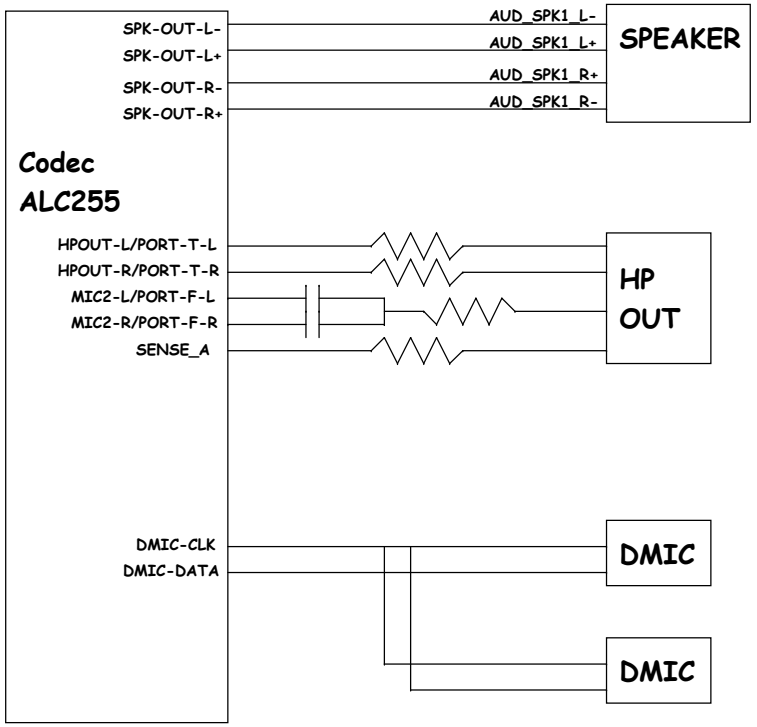
Thermal Block Diagram



Audio Block Diagram



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Title: **THERMAL/AUDIO BLOCK DIAGRAM**

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