31ZY8MB0000
ZY8 MB ASSY(DC/GM/MXM)ASSY W/O CPU
31ZY8MB0010
ZY8 MB ASSY(QC/GM/MXM)ASSY W/O CPU

ZY8 SYSTEM BLOCK DIAGRAM

DDR PWR TPS5116 P35
CHARGER ISL6251 P31
THERMAL PROTECTION P38
3/5V SYS PWR ISL6237 P32
2.5V/ 1.5V PWR DISCHARGER P37
CPU CORE PWR ISL6262A P33
POWER TREE P?
+1.05V RT8202 P34

X'TAL 14.318MHz
CLOCK GENERATOR
SELGO: SLG8SP513VTR P2

Penryn 479
uFCPGA P3, P4
DC/QC support

Thermal Sensor (NS LM95245) P3
Fan Driver (PWM Type) P29

FSB
667/800/1067 Mhz

HDMI Level Shift P19

DDR III
SO-DIMM 0
SO-DIMM 1
P16

Dual Channel DDR3
800/ 1066 MHz

NB
Cantiga
GM45
P5, P6, P7, P8, P9, P10, P11

PCIE
CRT
LVDS

MXM 3.0 P17

DISPLAY PORT
HDMI
CRT
LVDS

DISPLAY PORT P19
HDMI P19
CRT P18
LVDS P18

LVDS & CRT Switch P18

X4 DMI interface

HDD (SATA) *2 P22
ODD (SATA) P22

SATA0
SATA4
SATA1
SATA5
USB 2.0
Azalia

SB
ICH9M
PCIE-5 and USB9 are free.
P12,P13,P14,P15

X'TAL 32.768KHz

PCI-Express
PCIE-2
PCIE-1
PCIE-3
PCIE-4&6

USB1
New Card
USB1 P25
Mini Card
WLAN / TV
USB4 & 6 P21
USB4 & 6

X'TAL 25MHz

eSATA Conn.
USB0 P28
eSATA Buffer
(TI SN75LVCP412) P28
USB Port x 4
USB2, 3, 5 P28
Bluetooth
USB8 P29
CCD
USB11 P29
FingerPrint
USB9 P29

LPC

EC (WPC775C) P30
X'TAL 32.768KHz

IEEE1394 & Media Cardreader
(OZ888GS0LN) P26
IEEE1394a connector P26
Card Reader Connector P26

Broadcom Giga-LAN
(BCM5764/ BCM5784) P20
Transformer P20
RJ45 P20

Audio CODEC (ALC889X) P23

SPI ROM P30
Touch Pad P29
MMB P27
K/B COON. P29
CIR P30

Front Stereo Amp (G1453L/ 2W+2W) P24
Center Mono Amp (G1442/ 2W) P23
Rear Audio Amp & Head phone AN12947A P23,P24
Sub-Amplifier (MAX9737) P24

Front Speaker P24
Center Speaker P24
Speaker P24
S/PDIF P24
SUBWOOFER P24
Line in P24
MIC Jack P24
Int. D-MIC P18, P24

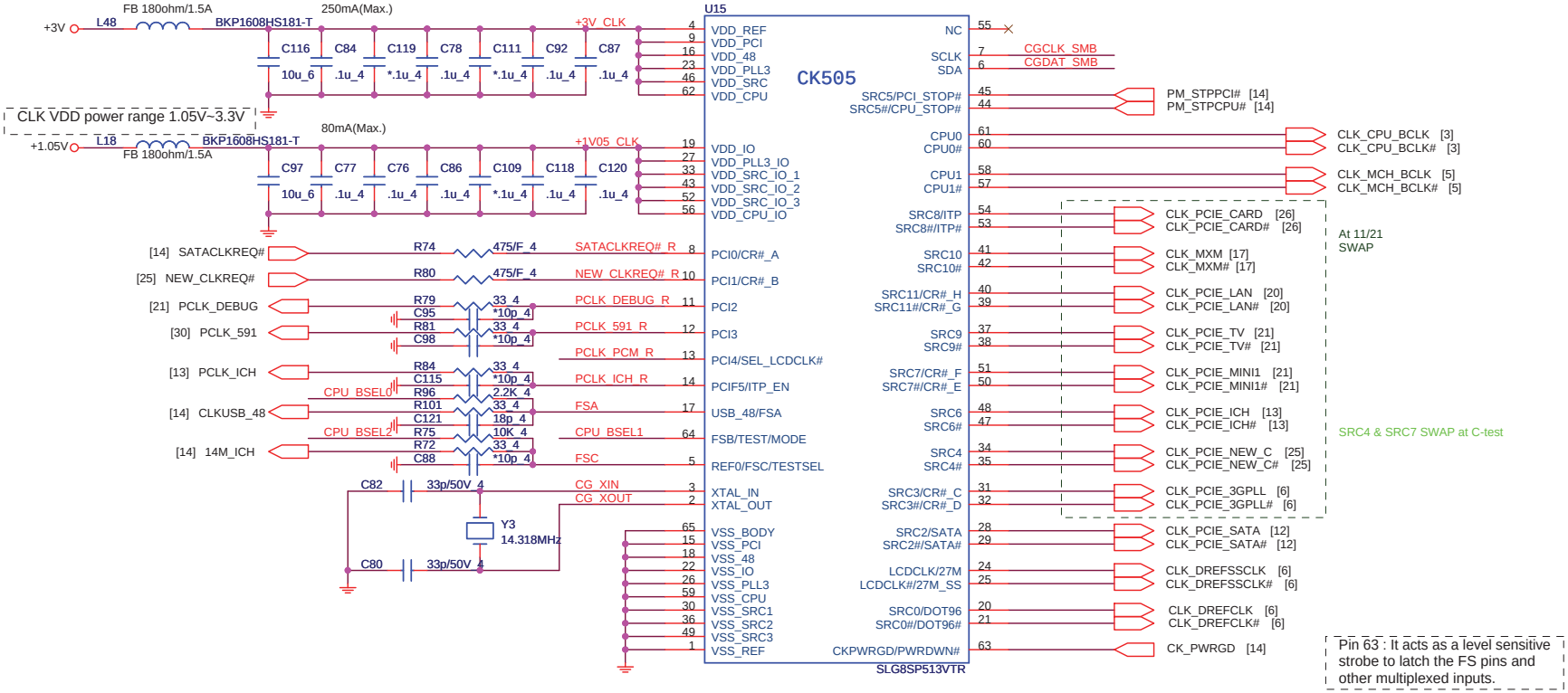
SSID: 019F and 019E
SVID: 1025

Quanta Computer Inc.
PROJECT : ZY8

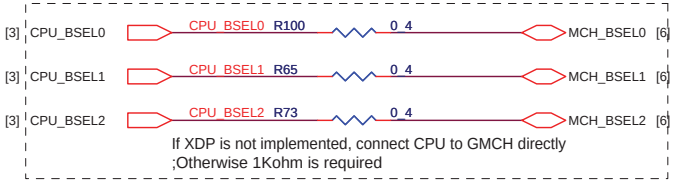
Size	Document Number	Rev
	ZY8 Block Diagram	2A

Date: Tuesday, December 30, 2008 Sheet 1 of 39

Clock Generator



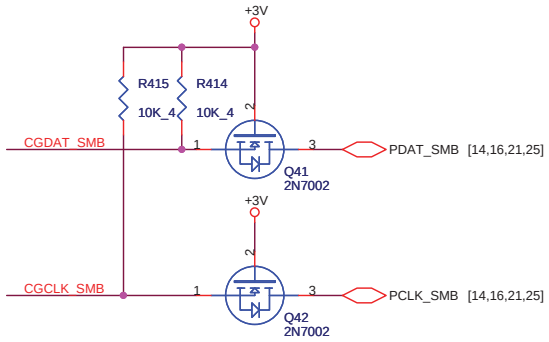
CPU Clock select



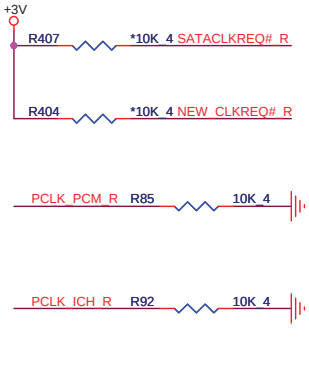
BSEL Frequency Select Table

FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz

SMBus



Strap table



Pin 8 : PCI_0 or CKREQ#_A selection
0 = PCI_0 output
1 = CKREQ#_A (Control SRC_0 & SRC_2)

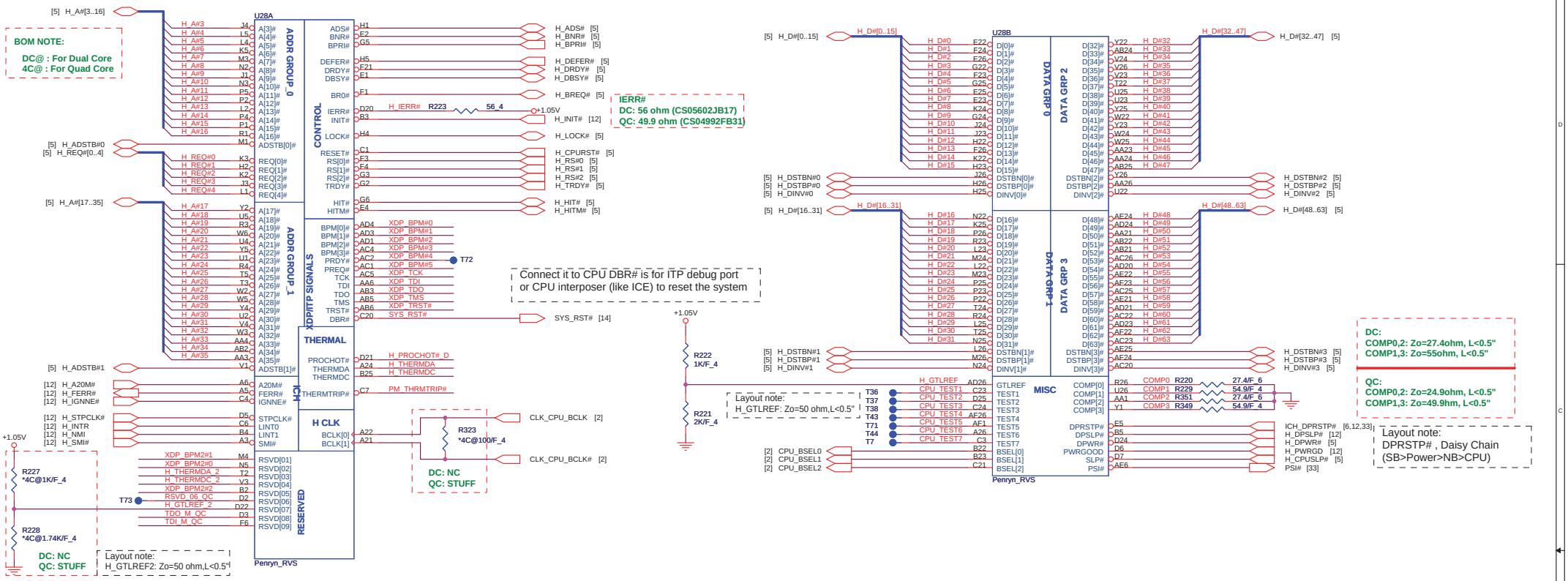
Pin 10 : PCI_1 or CKREQ#_B selection
0 = PCI_1 output
1 = CKREQ#_B (Control LCDCLK & SRC_4)

Pin 13 : For Pin 20/21 and 24/25 selection
0 = LCDCLK & DOT96 for internal graphic (Setting)
1 = 27M & 27M_SS &SRC_0 for external graphic

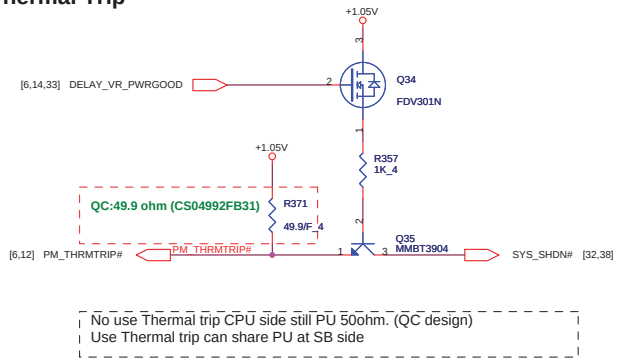
Pin 14 : For Pin 53/54 (CPU_ITP or SRC_8) selection
0 = SRC_8 (Setting)
1 = CPU_ITP

Quanta Computer Inc.
PROJECT : ZY8

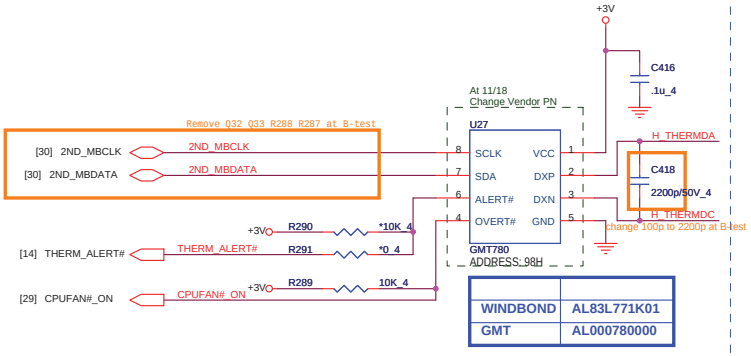
Size	Document Number	Rev
	CLOCK GENERATOR	2A
Date: Tuesday, February 17, 2009	Sheet 2 of 39	



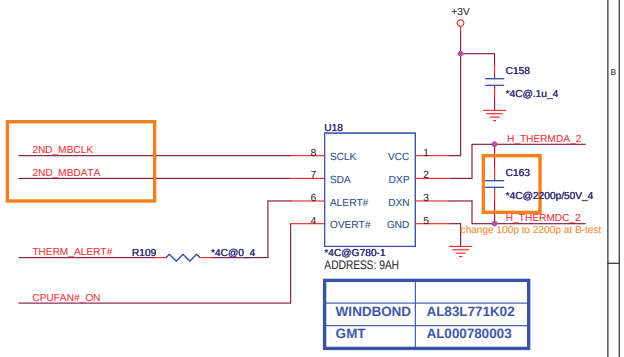
Thermal Trip



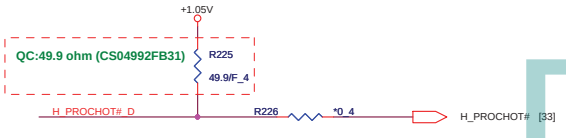
CPU #1 Thermal monitor



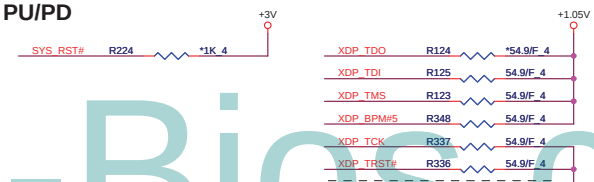
CPU #2 Thermal monitor

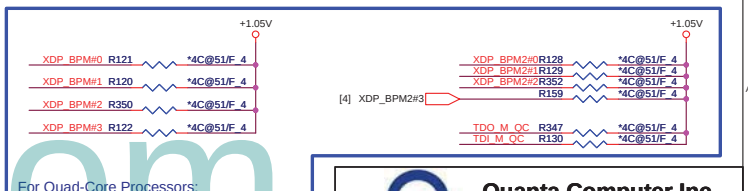


Processor hot

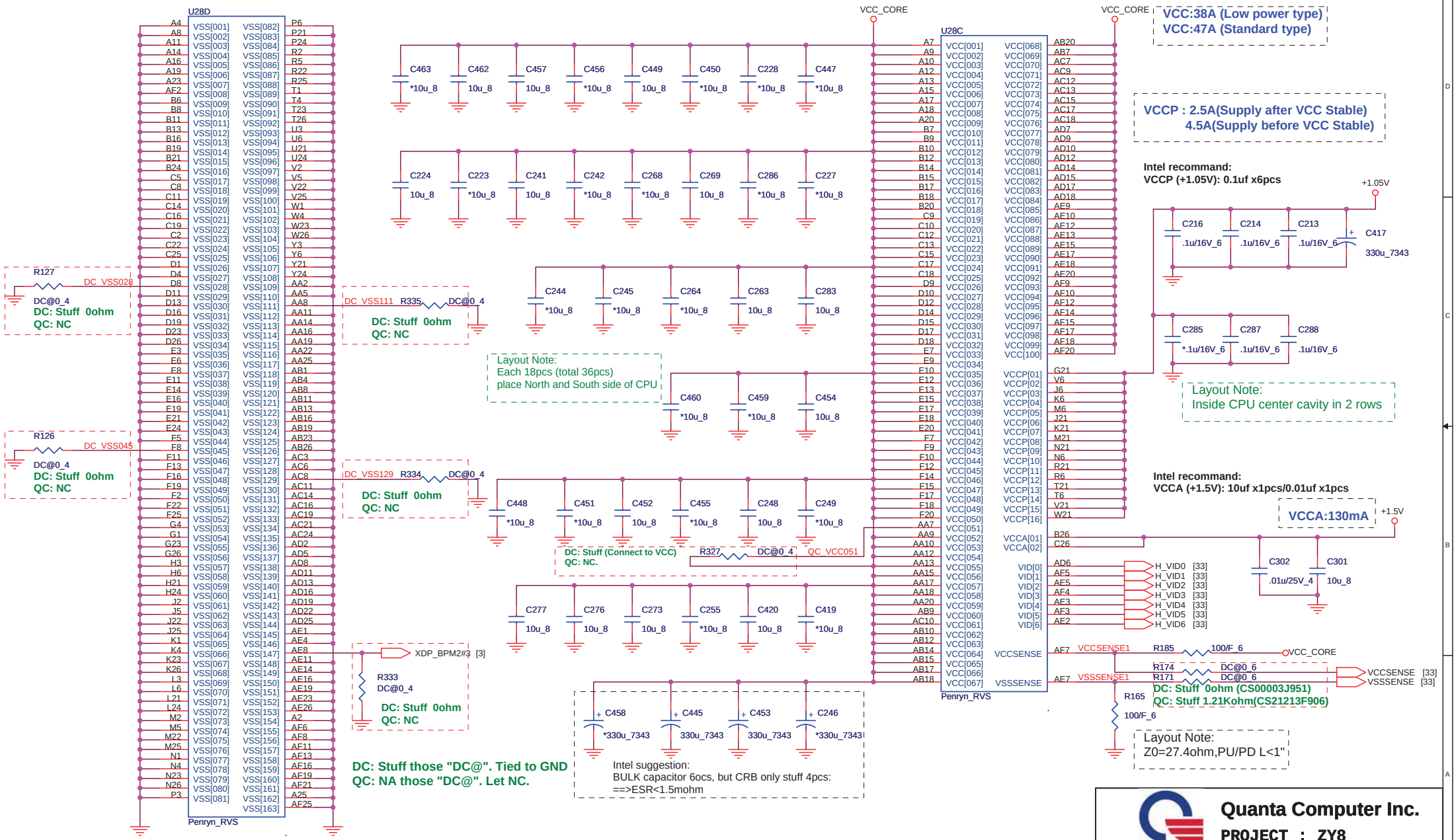


XDP PU/PD

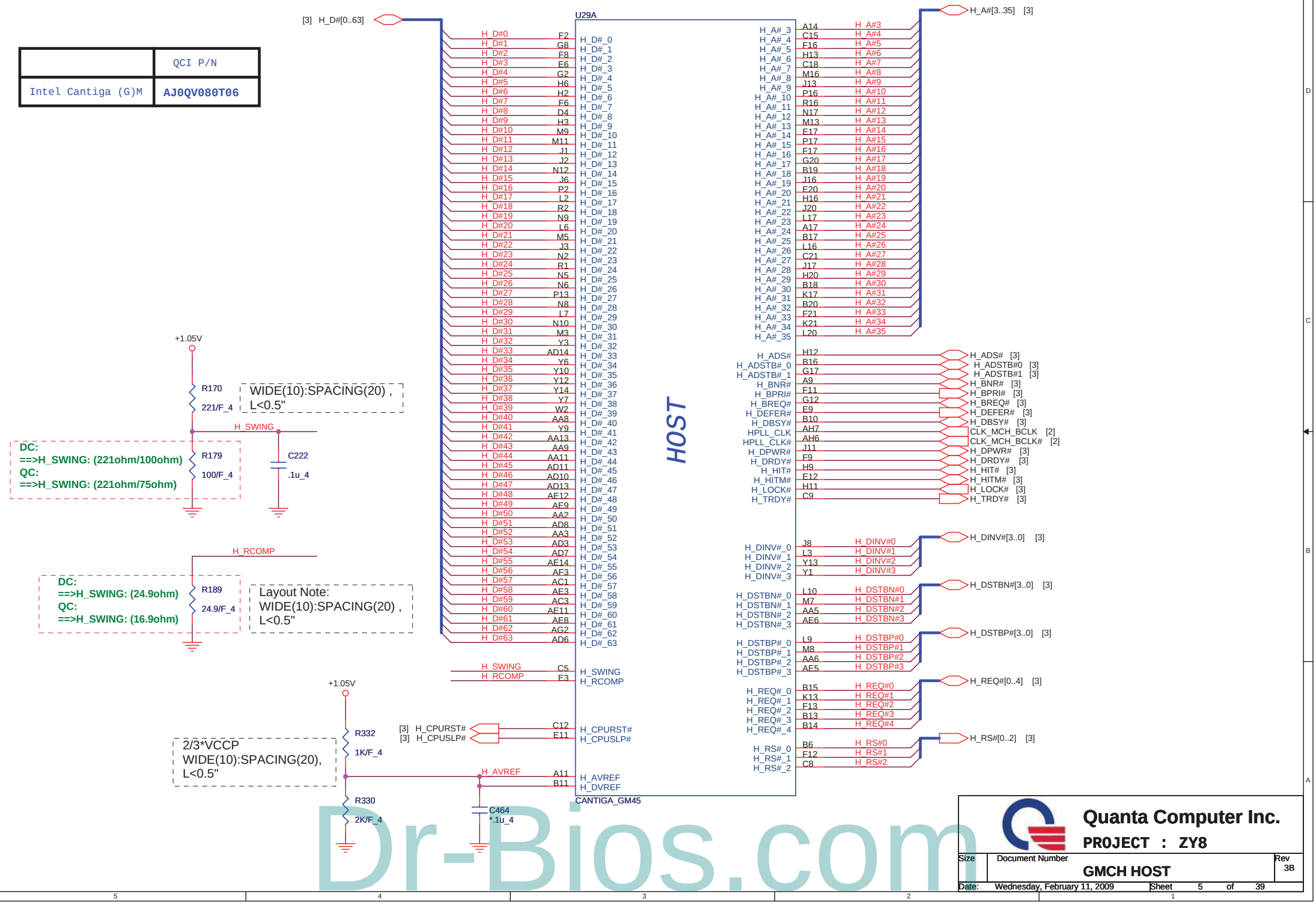




Quanta Computer Inc.	
PROJECT : ZY8	
Size	Document Number: CPU Host Bus
Rev	2A
Date: Friday, February 13, 2009	Sheet 3 of 39


U28D
Penryn_RVS
U28C
Penryn_RVS
VCC_CORE
VCC:38A (Low power type)
VCC:47A (Standard type)
VCCP : 2.5A(Supply after VCC Stable)
4.5A(Supply before VCC Stable)
Intel recommand:
VCCP (+1.05V): 0.1uf x6pcs
+1.05V
Layout Note:
Inside CPU center cavity in 2 rows
Intel recommand:
VCCA (+1.5V): 10uf x1pcs/0.01uf x1pcs
VCCA:130mA
+1.5V
Layout Note:
Each 18pcs (total 36pcs)
place North and South side of CPU
DC: Stuff 0ohm
QC: NC
DC: Stuff (Connect to VCC)
QC: NC.
DC: Stuff those "DC@". Tied to GND
QC: NA those "DC@". Let NC.
Intel suggestion:
BULK capacitor 6ocs, but CRB only stuff 4pcs:
==>ESR<1.5mohm
Layout Note:
Z0=27.4ohm,PU/PD L<1"
DC: Stuff 0ohm (CS00003J951)
QC: Stuff 1.21Kohm(CS21213F906)
Quanta Computer Inc.
PROJECT : ZY8
CPU Power
Size
Document Number
Rev 3B
Date: Wednesday, February 04, 2009
Sheet 4 of 39

	QCI P/N
Intel Cantiga (G)M	AJ0QV080T06



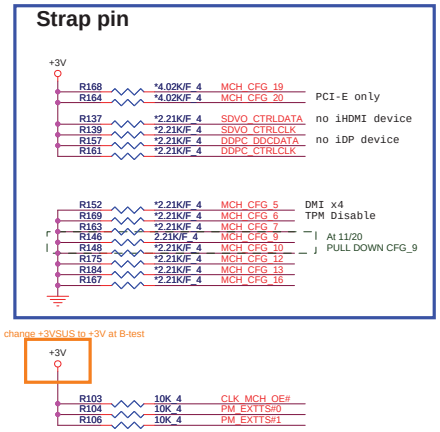
Quanta Computer Inc.
PROJECT : ZY8

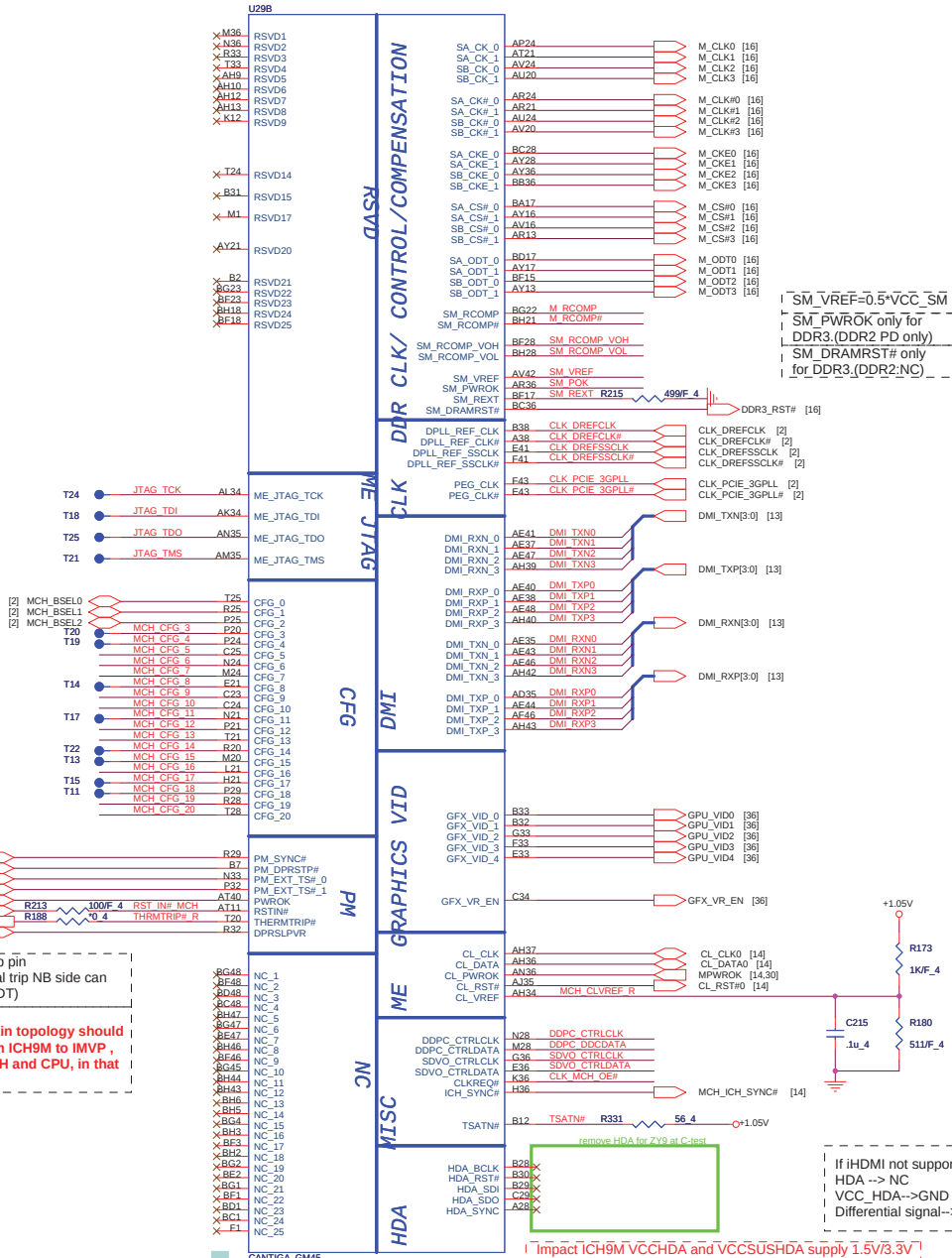
Size	Document Number	Rev
	GMCH HOST	3B
Date: Wednesday, February 11, 2009	Sheet 5 of 39	

Strap table

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	000= FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	iTPM Host Interface	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is disabled(Default)
CFG7	ME TLS Confidentiality	0 = AMT Firmware will use TLS cipher suite with no confidentiality 1 = AMT Firmware will use TLS cipher suite with confidentiality(Default)
CFG8	Reserved	
CFG9	PCIE Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG10	PCIE Loopback enable	0 = Enabled 1 = Disabled (Default)
CFG11	Reserved	
CFG12	ALLZ	0 = ALLZ mode enable 1 = disable(Default)
CFG13	XOR	0 = XOR mode enable 1 = disable(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal (Default) 1 = Lanes Reversed
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display port (SDVO/DP/iHDMI) or PCIE is operational (Default) 1 = Digital Display port (SDVO/DP/iHDMI) and PCIE are operating simultaneously via PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO/iHDMI Device Present(Default) 1 = SDVO/iHDMI Device present
DDPC_CTRLDATA	Digital Display Present	0 = Digital display(HDMI/DP) device absent(Default) 1 = Digital display(HDMI/DP) device present

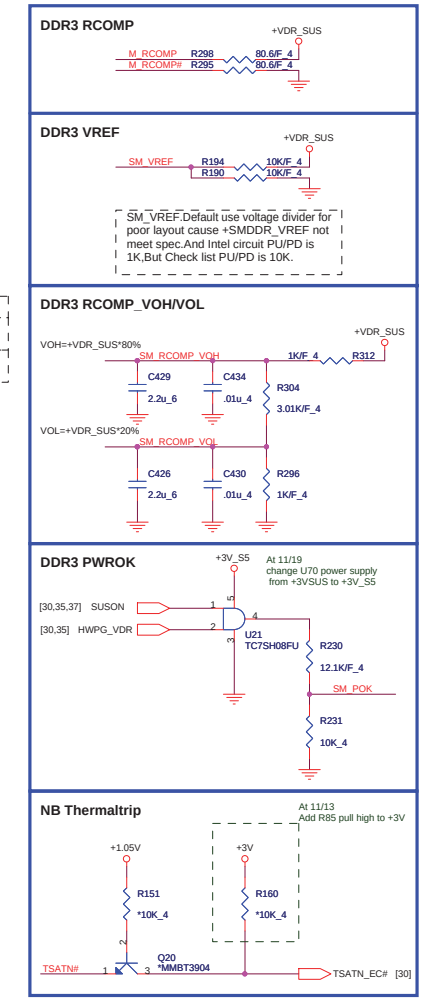
Strap pin





NB Thermal trip pin
No use Thermal trip NB side can NC.(NB has ODT)

PM_DPRSTP#
The Daisy chain topology should be routed from ICH9M to IMVP , then to (G)MCH and CPU, in that order.



CRB 1.0 : CL_VREF=0.355V (1K/511ohm)
DG 2.1 : CL_VREF=0.35V (1K/500ohm)

DDPC_CTRL for HDMI port C
SDVO_CTRL for HDMI port B

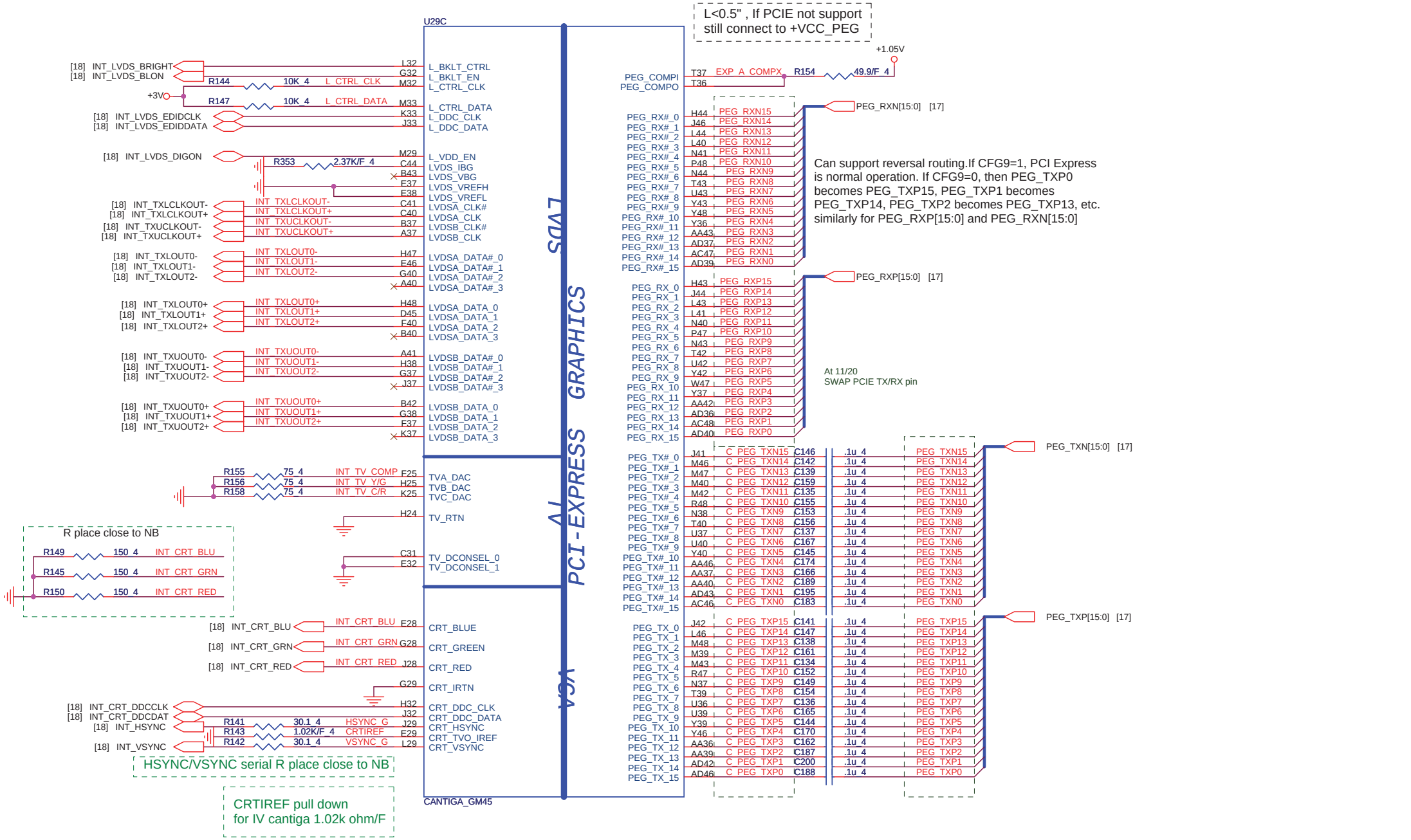
<Checklist ver0.8/DG2.1>
If TSATN# is not used, then it must be terminated with a 56-Ω pull-up resistor to VCCP.

If iHDMI not support
HDA --> NC
VCC_HDA-->GND
Differential signal-->NC

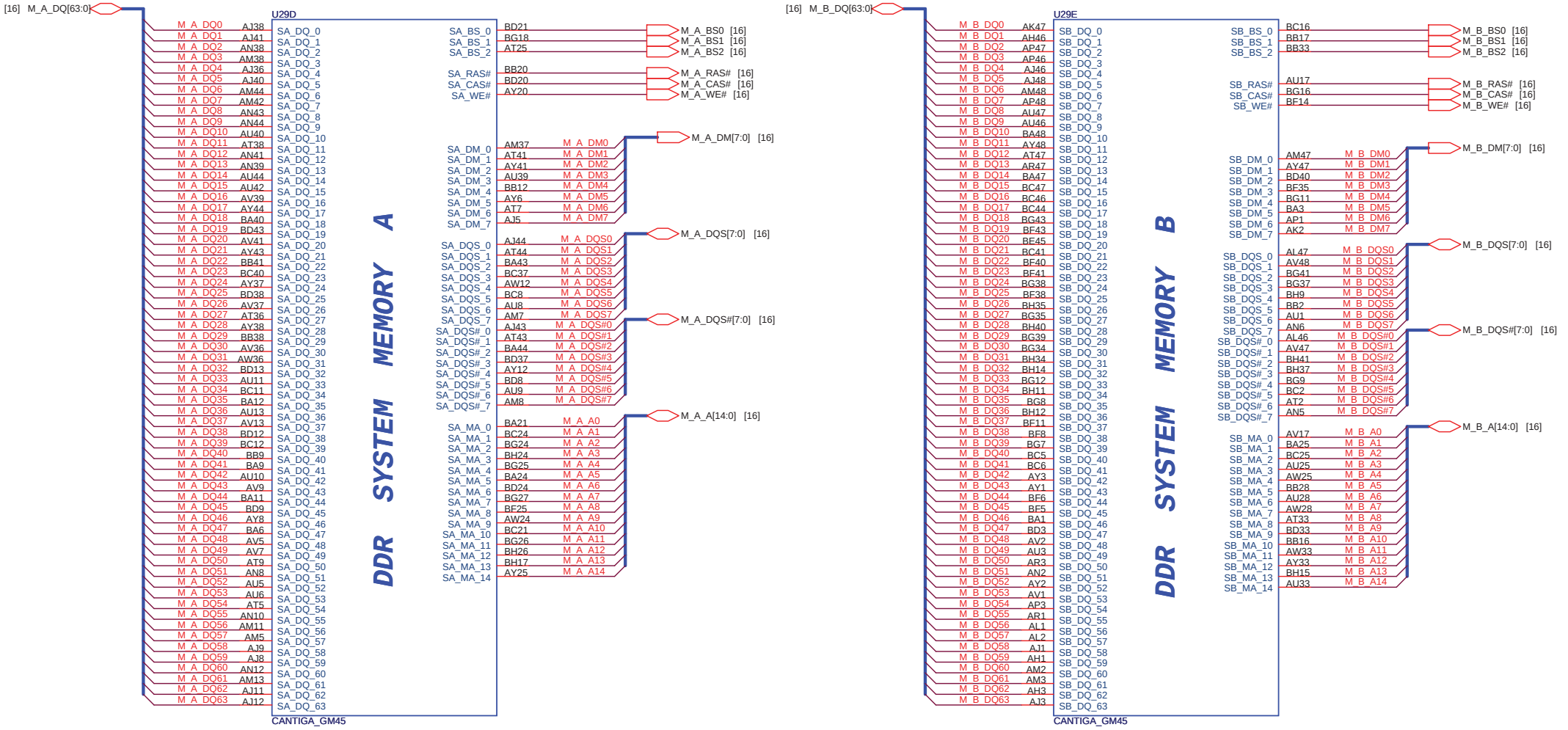
Impact ICH9M VCCHDA and VCCSUSHDA supply 1.5V/3.3V

NOTE:
If (G)MCH's HD Audio signals are connected to ICH9M for iHDMI, VCCHDA and VCCSUSHDA on ICH9M should be only on 1.5V. These power pins on ICH9M can be supplied with 3.3V if and only if (G)MCH's HDA is not connected to ICH9M. Consequently, only 1.5V audio/modem codecs can be used on the platform.

Quanta Computer Inc.
PROJECT : ZY8
Size | Document Number | Rev 3B
GMCH DMI
Date: Wednesday, February 11, 2009 | Sheet 6 of 39



Quanta Computer Inc.
PROJECT : ZY8
Size | Document Number: GMCH VGA/PEG | Rev 3B
Date: Wednesday, February 11, 2009 | Sheet 7 of 39

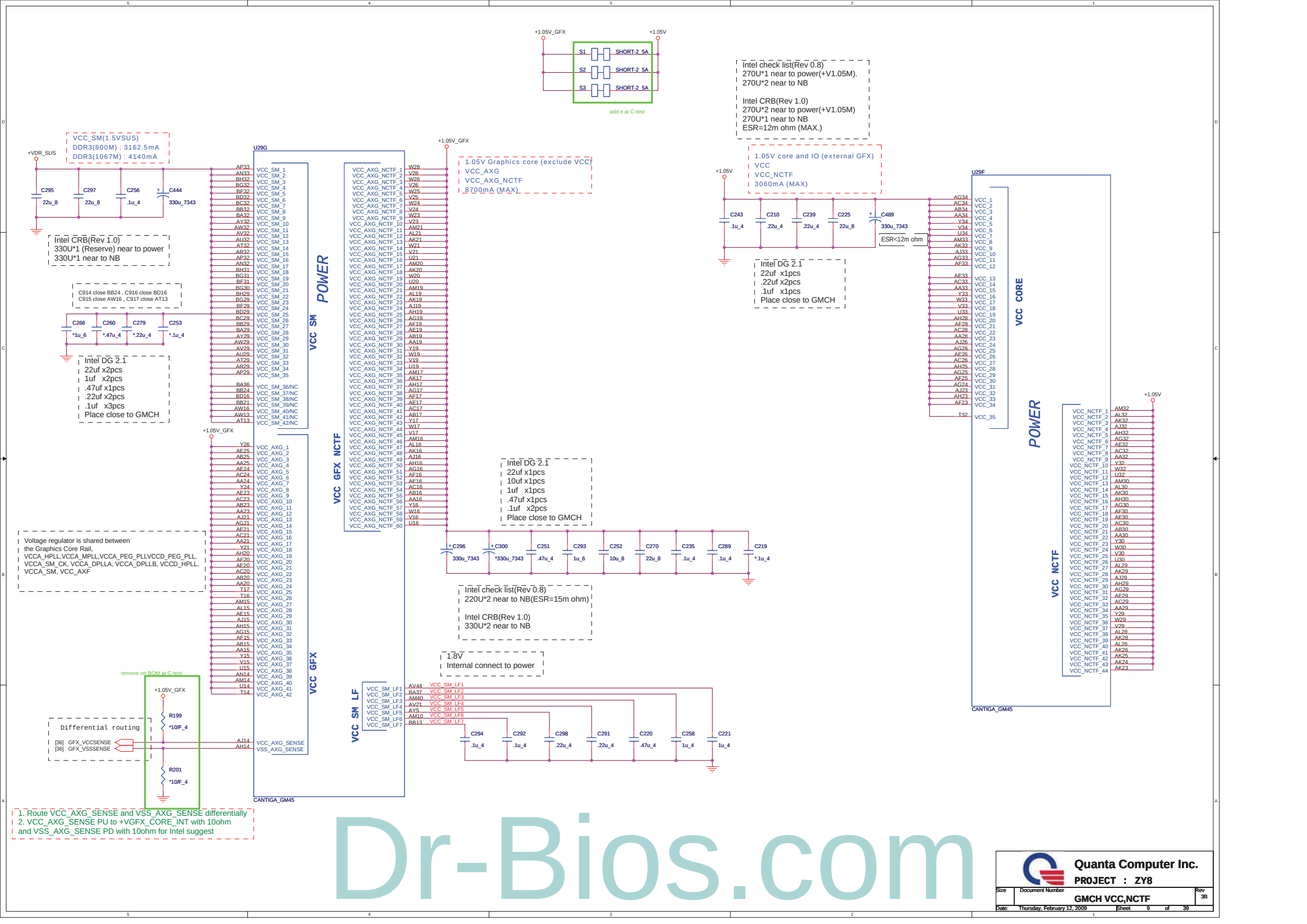


GMCH (CANTIGA)

Quanta Computer Inc.
PROJECT : ZY8

Size	Document Number	Rev
	GMCH DDR I/F	3B

Date: Wednesday, February 11, 2009 Sheet 8 of 39


+1.05V_GFX
+1.05V
S1
SHORT-2 5A
S2
SHORT-2 5A
S3
SHORT-2 5A
add it at C-test
Intel check list(Rev 0.8)
270U*1 near to power(+V1.05M).
270U*2 near to NB
Intel CRB(Rev 1.0)
270U*2 near to power(+V1.05M)
270U*1 near to NB
ESR=12m ohm (MAX.)
VCC_SM(1.5VSUS)
DDR3(800M) : 3162.5mA
DDR3(1067M) : 4140mA
+VDR_SUS
C295 22u_8
C297 22u_8
C256 .1u_4
C444 330u_7343
Intel CRB(Rev 1.0)
330U*1 (Reserve) near to power
330U*1 near to NB
C914 close BB24 , C916 close BD16
C915 close AW16 , C917 close AT13
C266 *1u_6
C260 *.47u_4
C279 *.22u_4
C253 *.1u_4
Intel DG 2.1
22uf x2pcs
1uf x2pcs
.47uf x1pcs
.22uf x2pcs
.1uf x3pcs
Place close to GMCH
U29G
VCC_SM_1
VCC_SM_2
VCC_SM_3
VCC_SM_4
VCC_SM_5
VCC_SM_6
VCC_SM_7
VCC_SM_8
VCC_SM_9
VCC_SM_10
VCC_SM_11
VCC_SM_12
VCC_SM_13
VCC_SM_14
VCC_SM_15
VCC_SM_16
VCC_SM_17
VCC_SM_18
VCC_SM_19
VCC_SM_20
VCC_SM_21
VCC_SM_22
VCC_SM_23
VCC_SM_24
VCC_SM_25
VCC_SM_26
VCC_SM_27
VCC_SM_28
VCC_SM_29
VCC_SM_30
VCC_SM_31
VCC_SM_32
VCC_SM_33
VCC_SM_34
VCC_SM_35
VCC_SM_36/NC
VCC_SM_37/NC
VCC_SM_38/NC
VCC_SM_39/NC
VCC_SM_40/NC
VCC_SM_41/NC
VCC_SM_42/NC
VCC SM
POWER
+1.05V_GFX
1.05V Graphics core (exclude VCC)
VCC_AXG
VCC_AXG_NCTF
8700mA (MAX)
VCC_AXG_NCTF_1
VCC_AXG_NCTF_2
VCC_AXG_NCTF_3
VCC_AXG_NCTF_4
VCC_AXG_NCTF_5
VCC_AXG_NCTF_6
VCC_AXG_NCTF_7
VCC_AXG_NCTF_8
VCC_AXG_NCTF_9
VCC_AXG_NCTF_10
VCC_AXG_NCTF_11
VCC_AXG_NCTF_12
VCC_AXG_NCTF_13
VCC_AXG_NCTF_14
VCC_AXG_NCTF_15
VCC_AXG_NCTF_16
VCC_AXG_NCTF_17
VCC_AXG_NCTF_18
VCC_AXG_NCTF_19
VCC_AXG_NCTF_20
VCC_AXG_NCTF_21
VCC_AXG_NCTF_22
VCC_AXG_NCTF_23
VCC_AXG_NCTF_24
VCC_AXG_NCTF_25
VCC_AXG_NCTF_26
VCC_AXG_NCTF_27
VCC_AXG_NCTF_28
VCC_AXG_NCTF_29
VCC_AXG_NCTF_30
VCC_AXG_NCTF_31
VCC_AXG_NCTF_32
VCC_AXG_NCTF_33
VCC_AXG_NCTF_34
VCC_AXG_NCTF_35
VCC_AXG_NCTF_36
VCC_AXG_NCTF_37
VCC_AXG_NCTF_38
VCC_AXG_NCTF_39
VCC_AXG_NCTF_40
VCC_AXG_NCTF_41
VCC_AXG_NCTF_42
VCC_AXG_NCTF_43
VCC_AXG_NCTF_44
VCC_AXG_NCTF_45
VCC_AXG_NCTF_46
VCC_AXG_NCTF_47
VCC_AXG_NCTF_48
VCC_AXG_NCTF_49
VCC_AXG_NCTF_50
VCC_AXG_NCTF_51
VCC_AXG_NCTF_52
VCC_AXG_NCTF_53
VCC_AXG_NCTF_54
VCC_AXG_NCTF_55
VCC_AXG_NCTF_56
VCC_AXG_NCTF_57
VCC_AXG_NCTF_58
VCC_AXG_NCTF_59
VCC_AXG_NCTF_60
VCC GFX NCTF
Intel DG 2.1
22uf x1pcs
10uf x1pcs
1uf x1pcs
.47uf x1pcs
.1uf x2pcs
Place close to GMCH
C296 330u_7343
C300 *330u_7343
C251 .47u_4
C293 1u_6
C252 10u_8
C270 22u_8
C235 .1u_4
C289 .1u_4
C219 *.1u_4
Intel check list(Rev 0.8)
220U*2 near to NB(ESR=15m ohm)
Intel CRB(Rev 1.0)
330U*2 near to NB
1.8V
Internal connect to power
VCC_SM_LF1
VCC_SM_LF2
VCC_SM_LF3
VCC_SM_LF4
VCC_SM_LF5
VCC_SM_LF6
VCC_SM_LF7
VCC SM LF
C294 .1u_4
C292 .1u_4
C298 .22u_4
C291 .22u_4
C220 .47u_4
C258 1u_4
C221 1u_4
1.05V core and IO (external GFX)
VCC
VCC_NCTF
3060mA (MAX)
+1.05V
C243 .1u_4
C210 .22u_4
C239 .22u_4
C225 22u_8
C489 330u_7343
ESR<12m ohm
Intel DG 2.1
22uf x1pcs
.22uf x2pcs
.1uf x1pcs
Place close to GMCH
U29F
VCC_1
VCC_2
VCC_3
VCC_4
VCC_5
VCC_6
VCC_7
VCC_8
VCC_9
VCC_10
VCC_11
VCC_12
VCC_13
VCC_14
VCC_15
VCC_16
VCC_17
VCC_18
VCC_19
VCC_20
VCC_21
VCC_22
VCC_23
VCC_24
VCC_25
VCC_26
VCC_27
VCC_28
VCC_29
VCC_30
VCC_31
VCC_32
VCC_33
VCC_34
VCC_35
VCC CORE
POWER
VCC_NCTF_1
VCC_NCTF_2
VCC_NCTF_3
VCC_NCTF_4
VCC_NCTF_5
VCC_NCTF_6
VCC_NCTF_7
VCC_NCTF_8
VCC_NCTF_9
VCC_NCTF_10
VCC_NCTF_11
VCC_NCTF_12
VCC_NCTF_13
VCC_NCTF_14
VCC_NCTF_15
VCC_NCTF_16
VCC_NCTF_17
VCC_NCTF_18
VCC_NCTF_19
VCC_NCTF_20
VCC_NCTF_21
VCC_NCTF_22
VCC_NCTF_23
VCC_NCTF_24
VCC_NCTF_25
VCC_NCTF_26
VCC_NCTF_27
VCC_NCTF_28
VCC_NCTF_29
VCC_NCTF_30
VCC_NCTF_31
VCC_NCTF_32
VCC_NCTF_33
VCC_NCTF_34
VCC_NCTF_35
VCC_NCTF_36
VCC_NCTF_37
VCC_NCTF_38
VCC_NCTF_39
VCC_NCTF_40
VCC_NCTF_41
VCC_NCTF_42
VCC_NCTF_43
VCC_NCTF_44
VCC NCTF
CANTIGA_GM45
Voltage regulator is shared between
the Graphics Core Rail,
VCCA_HPLL,VCCA_MPLL,VCCA_PEG_PLLVCCD_PEG_PLL,
VCCA_SM_CK, VCCA_DPLLA, VCCA_DPLLB, VCCD_HPLL,
VCCA_SM, VCC_AXF
remove on BOM at C-test
+1.05V_GFX
R199 *10/F_4
R201 *10/F_4
Differential routing
[36] GFX_VCCSENSE
[36] GFX_VSSSENSE
VCC_AXG_SENSE
VSS_AXG_SENSE
VCC GFX
CANTIGA_GM45
1. Route VCC_AXG_SENSE and VSS_AXG_SENSE differentially
2. VCC_AXG_SENSE PU to +VGFX_CORE_INT with 10ohm
and VSS_AXG_SENSE PD with 10ohm for Intel suggest
Dr-Bios.com
Quanta Computer Inc.
PROJECT : ZY8
Size
Document Number
GMCH VCC,NCTF
Rev 3B
Date: Thursday, February 12, 2009
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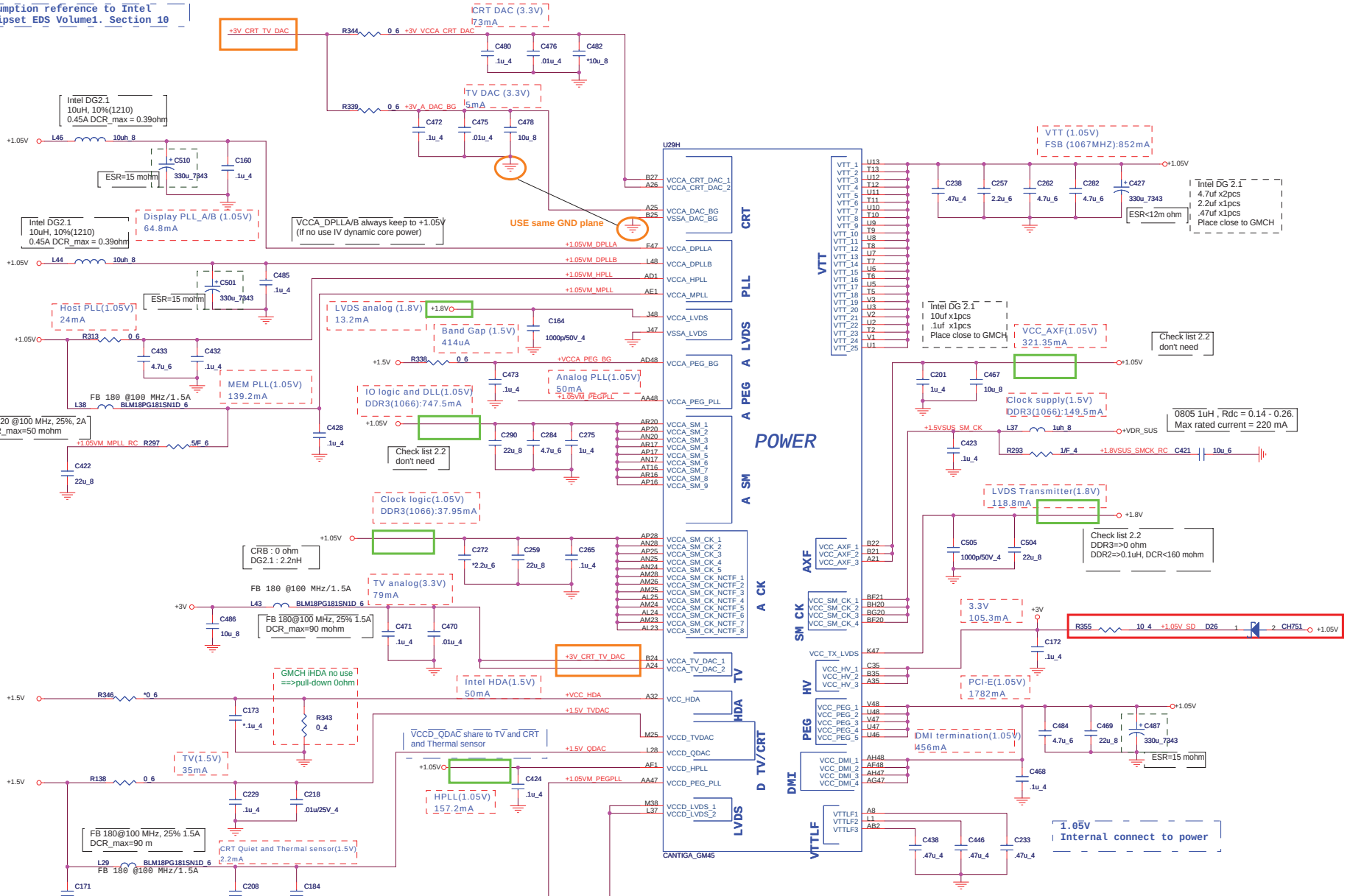
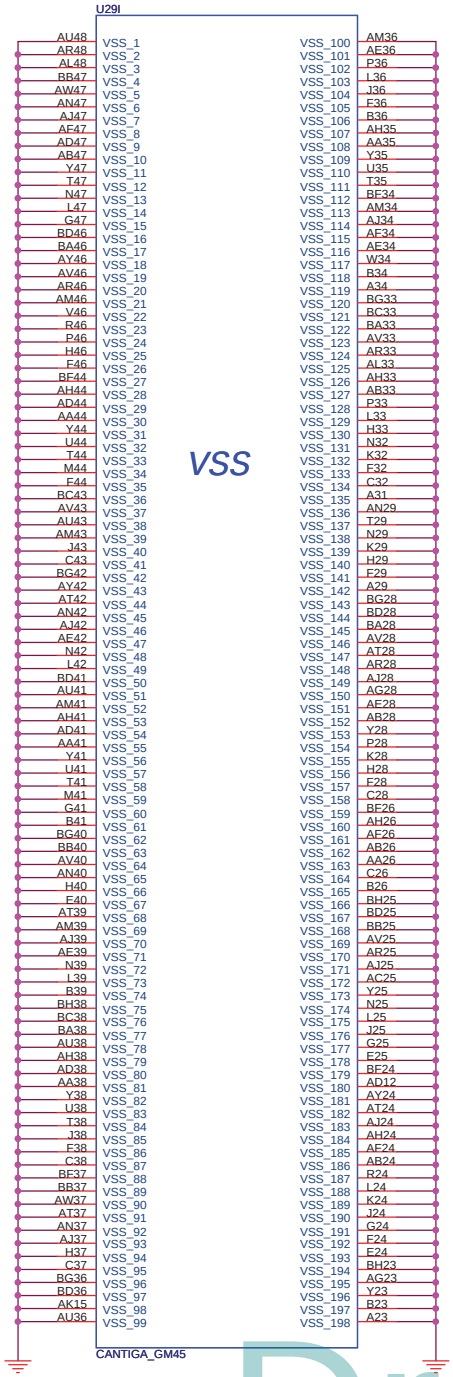
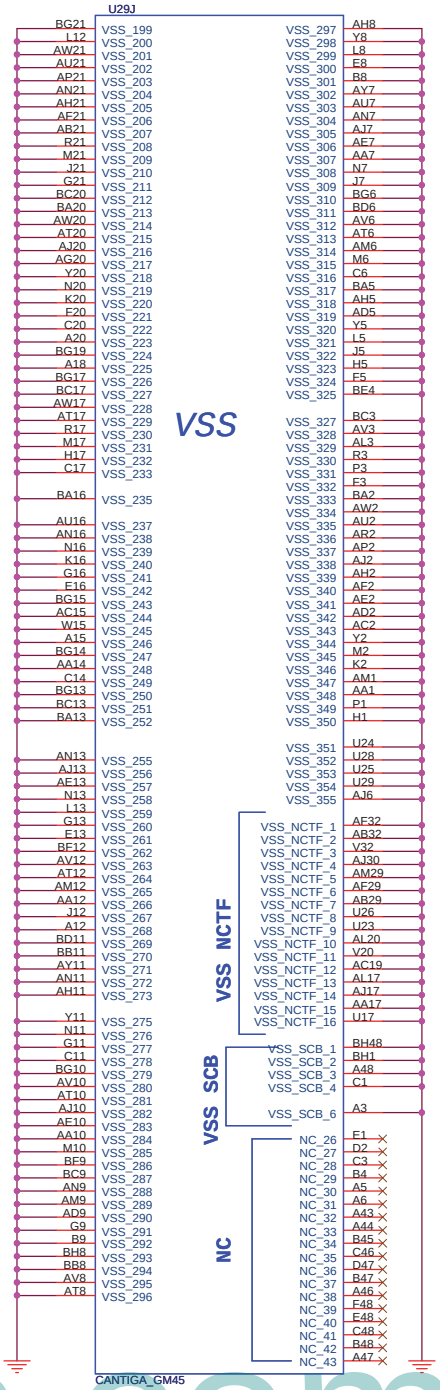
Power consumption reference to Intel Cantiga chipset EDS Volume1. Section 10



Quanta Computer Inc.
PROJECT : ZY8
Size | Document Number: GMCH POWER | Rev 3B
Date: Monday, February 16, 2009 | Sheet 10 of 39

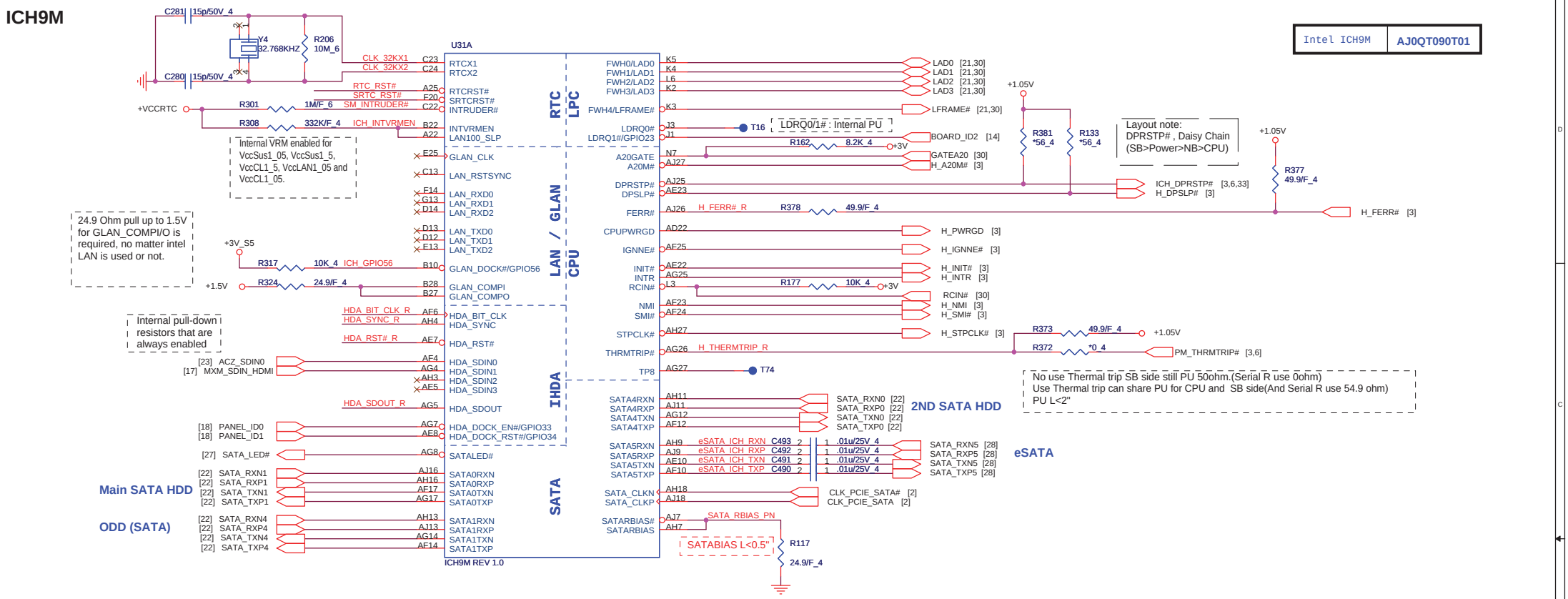




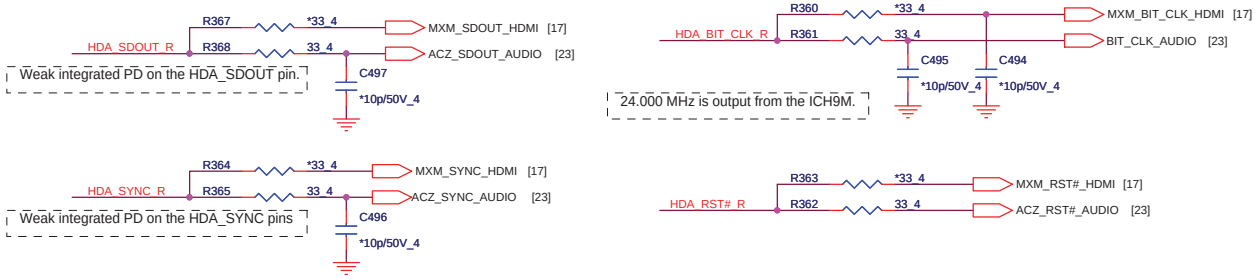
Quanta Computer Inc.

PROJECT : ZY8

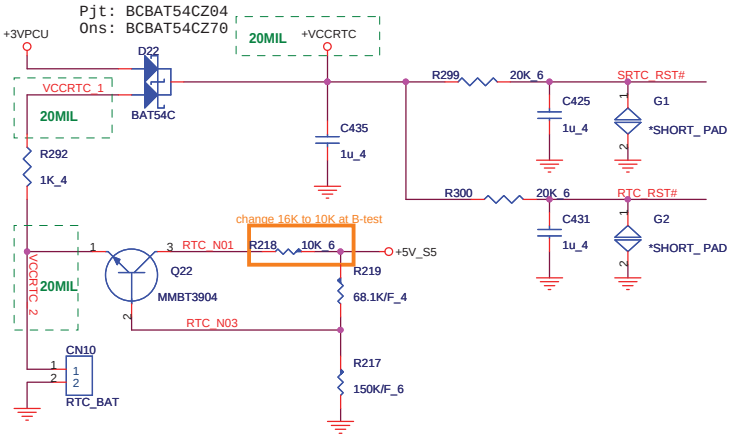
Size	Document Number	Rev
	GMCH VSS	3B
Date: Wednesday, February 11, 2009	Sheet 11 of 39	



HD Audio



RTC

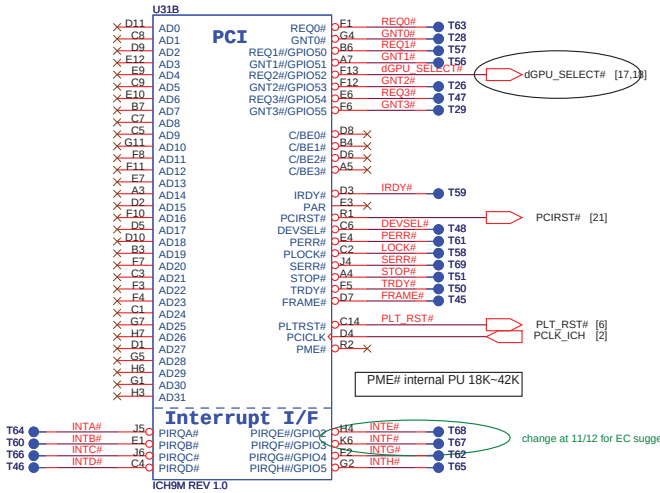


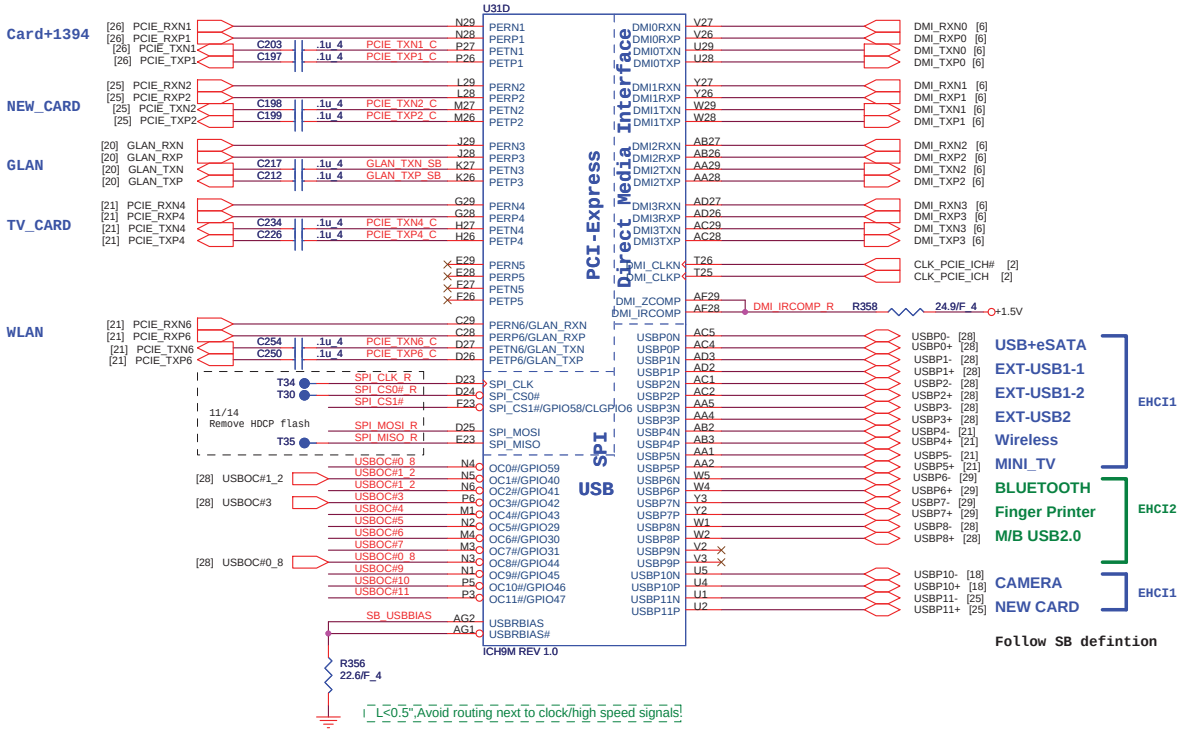
South Bridge Strap Pin (1/3)

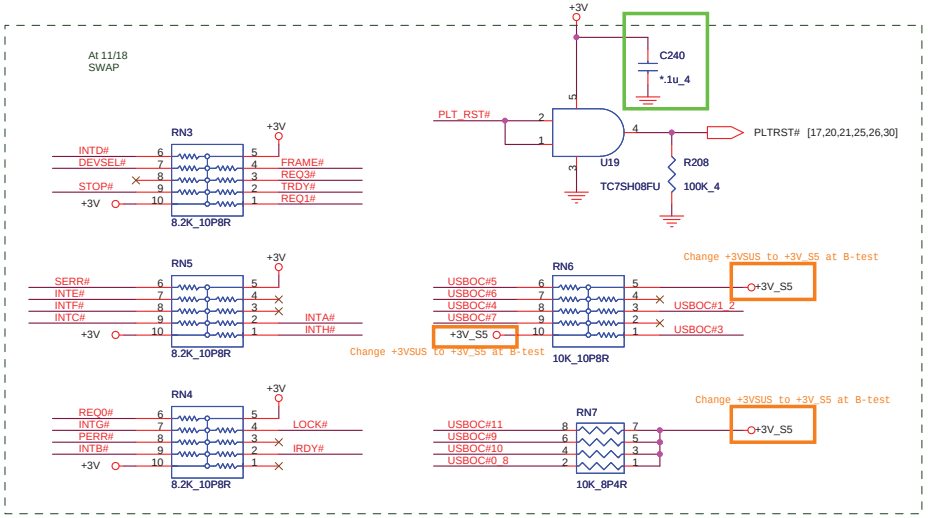
Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_DOCK_EN/ GPIO33	Flash Descriptor Security Override Strap	PWROK	0 = The Flash Descriptor Security will be overridden. 1 = The security measures defined in the Flash Descriptor will be in effect	This strap should only be enabled in manufacturing environments using an external pull-up resistor.
SATALED#	PCI Express Lane Reversal (Lanes 1-4)	PWROK	Internal PU	
TP3	XOR Chain Entrance	PWROK	ICH_TP3 / HDA_SDOUT: 0/0 RSVD; 0/1 Enter XOR Chain; 1/0 Normal opration(Default); 1/1 Set PCIE port config bit 1	
HDA_SDOUT	XOR Chain Entrance /PCI Express* Port Config 1 bit 1(Port 1-4)	PWROK		

Quanta Computer Inc.
PROJECT : ZY8
Size | Document Number: ICH9M HOST | Rev 3B
Date: Tuesday, February 10, 2009 | Sheet 12 of 39

ICH9M







South Bridge Strap Pin (2/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0	
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default	
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default	
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default	GNT3# R193 *1K_4
SPI_MOSI	Integrated TPM Enable	CLPWROK	0 = INT TPM disable(Default) 1 = INT TPM enable	SPI_MOSI_R R200 *20K_4 +3V_S5
GNT0#	Boot BIOS Selection 0	PWROK	PCI_GNT#0 / SPI_CS#1 / Boot Location 0 / 1 / SPI	GNT0# R186 *1K_4
SPI_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK	1 / 0 / PCI 1 / 1 / **LPC(Default)**	SPI_CS1# R191 *1K_4

Quanta Computer Inc.		
PROJECT : ZY8		
Size	Document Number	Rev
	ICH9M PCIE / PCI / USB	3B
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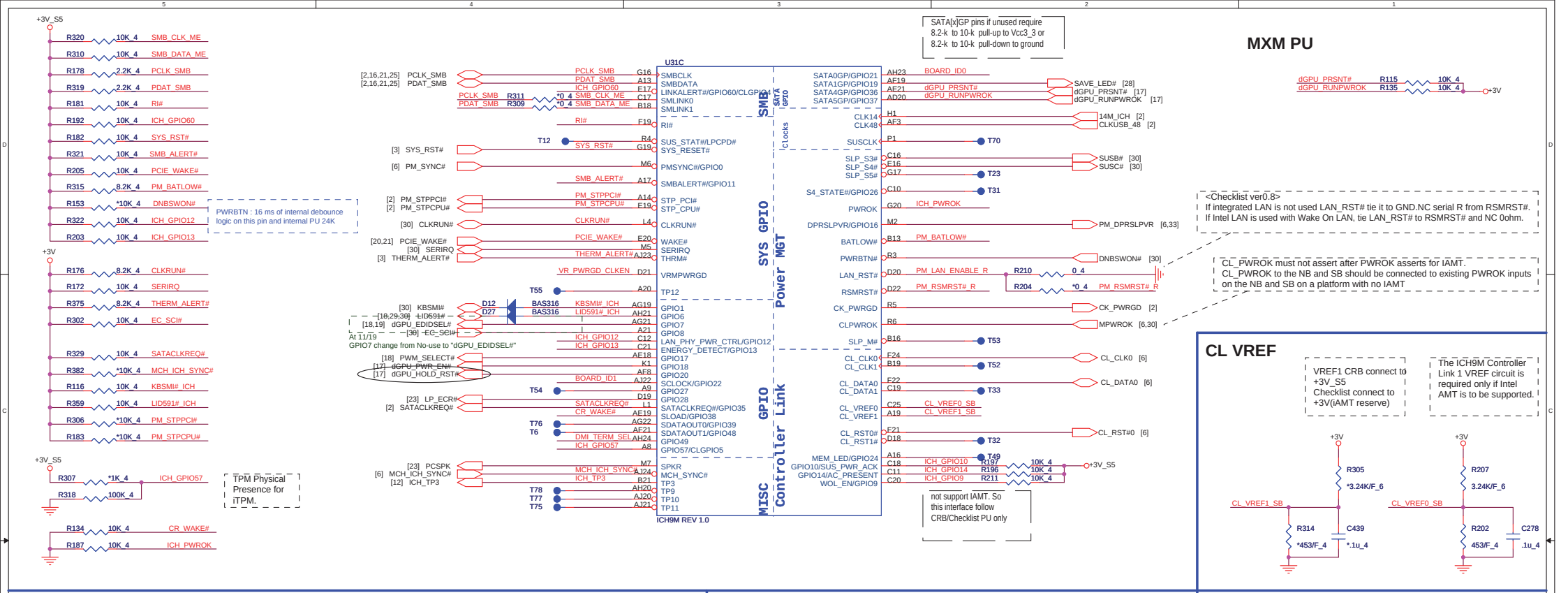
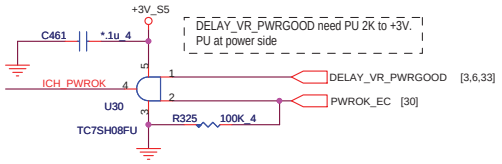


CL VREF

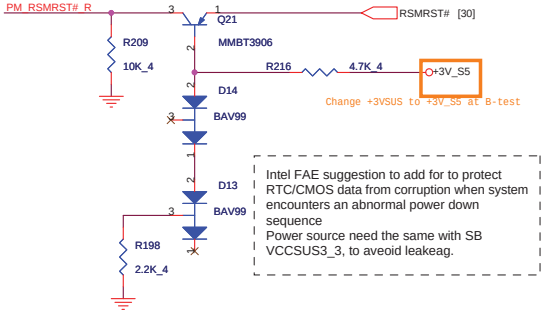
VREF1 CRB connect to +3V_S5
Checklist connect to +3V(iAMT reserve)

The ICH9M Controller Link 1 VREF circuit is required only if Intel AMT is to be supported.

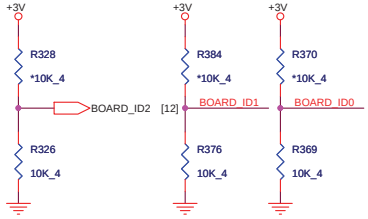
ICH PWROK



Resume RST



M/B ID

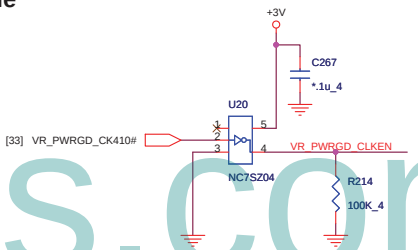


Board ID	ID2	ID1	ID0
default	0	0	0
	0	0	1
	0	1	0
	0	1	1
	1	0	0

South Bridge Strap Pin (3/3)

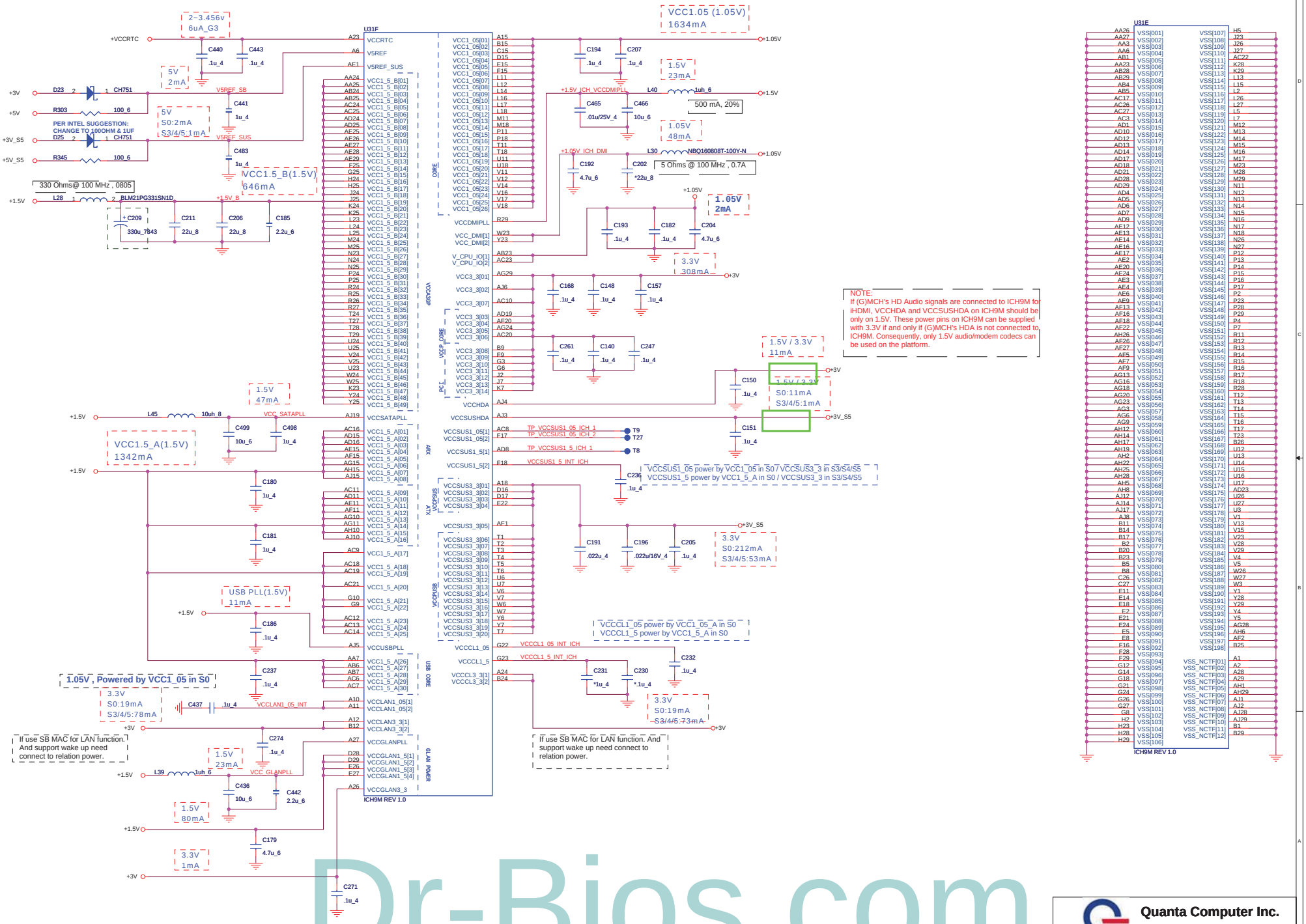
Pin Name	Strap description	Sampled	Configuration	PU/PD
GPIO20	Reserved	PWROK		
SPKR	No Reboot	PWROK	0 = Default 1 = No Reboot mode	PCSPK R166 *1K_4 +3V
GPIO49	DMI Termination Voltage	PWROK	0 = for desktop applications 1 = for mobile applications Internal PU	DMI_TERM_SEL R383 *1K_4

CLK Enable



Quanta Computer Inc.
PROJECT : ZY8
Size | Document Number | ICH9M GPIO | Rev 3B
Date: Monday, January 05, 2009 | Sheet 14 of 39

ICH9M



Quanta Computer Inc.
PROJECT : ZY8

Size	Document Number	Rev
	ICH9 POWER	3B

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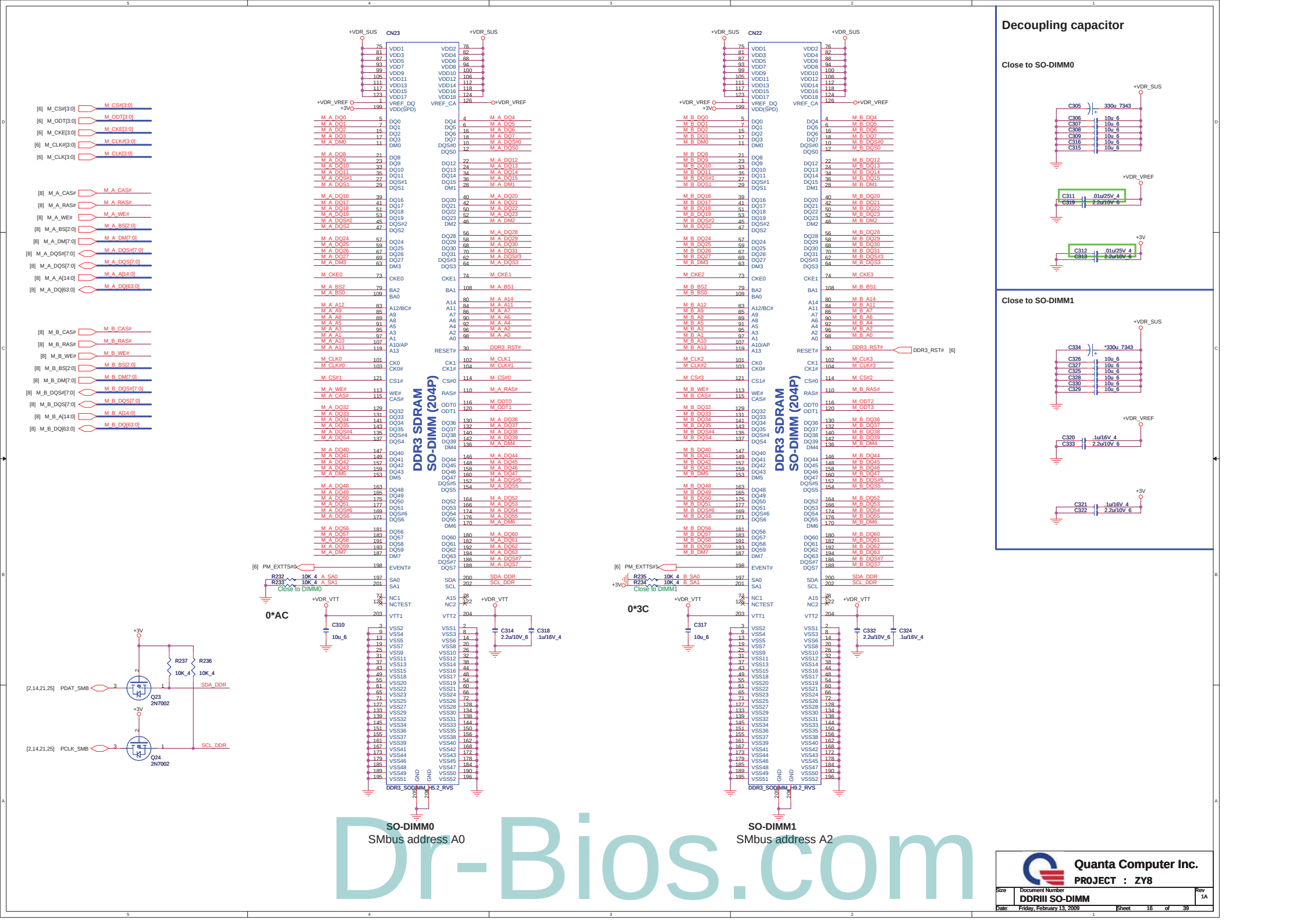

Decoupling capacitor
Close to SO-DIMM0
Close to SO-DIMM1
DDR3 SDRAM SO-DIMM (204P)
DDR3_SODIMM_H5.2_RVS
DDR3_SODIMM_H9.2_RVS
SO-DIMM0
SMbus address A0
SO-DIMM1
SMbus address A2
0*AC
0*3C
Close to DIMM0
Close to DIMM1
Quanta Computer Inc.
PROJECT : ZY8
DDRIII SO-DIMM
Friday, February 13, 2009
Sheet 16 of 39
Dr-Bios.com

MXM Module

dGPU_PRSNT#	Sku
Low	MXM
High	WO/ MXM

At 11/21
update MXM footprint to mxm-mm70-314-310b1-1-270p

CN25A

MXM3_2.0 CONNECTOR

CN25B

MXM3_2.0 CONNECTOR

PEX_Swing adjust

At 11/13
Modify Net Name

MXM3.0	n-Vidia	AMD
LVDS	LVDS	LVDS/Int. DP
DP_D	Int. DP	X
DP_A	HDMI	HDMI
DP_C	Ext. DP/DVI	Ext. DP/DVI
DP_B	N/A	N/A

MXM Reset

change to +3V at B-test

U36 TC7SH08FU

Thermo SMBus

change to 2N7002 at B-test

MXM VIN Power switch

dGPU_PWR_EN#	Behavior
Low	Enable dGPU PWR
High	Disable dGPU PWR

MXM 3V/5V Power switch

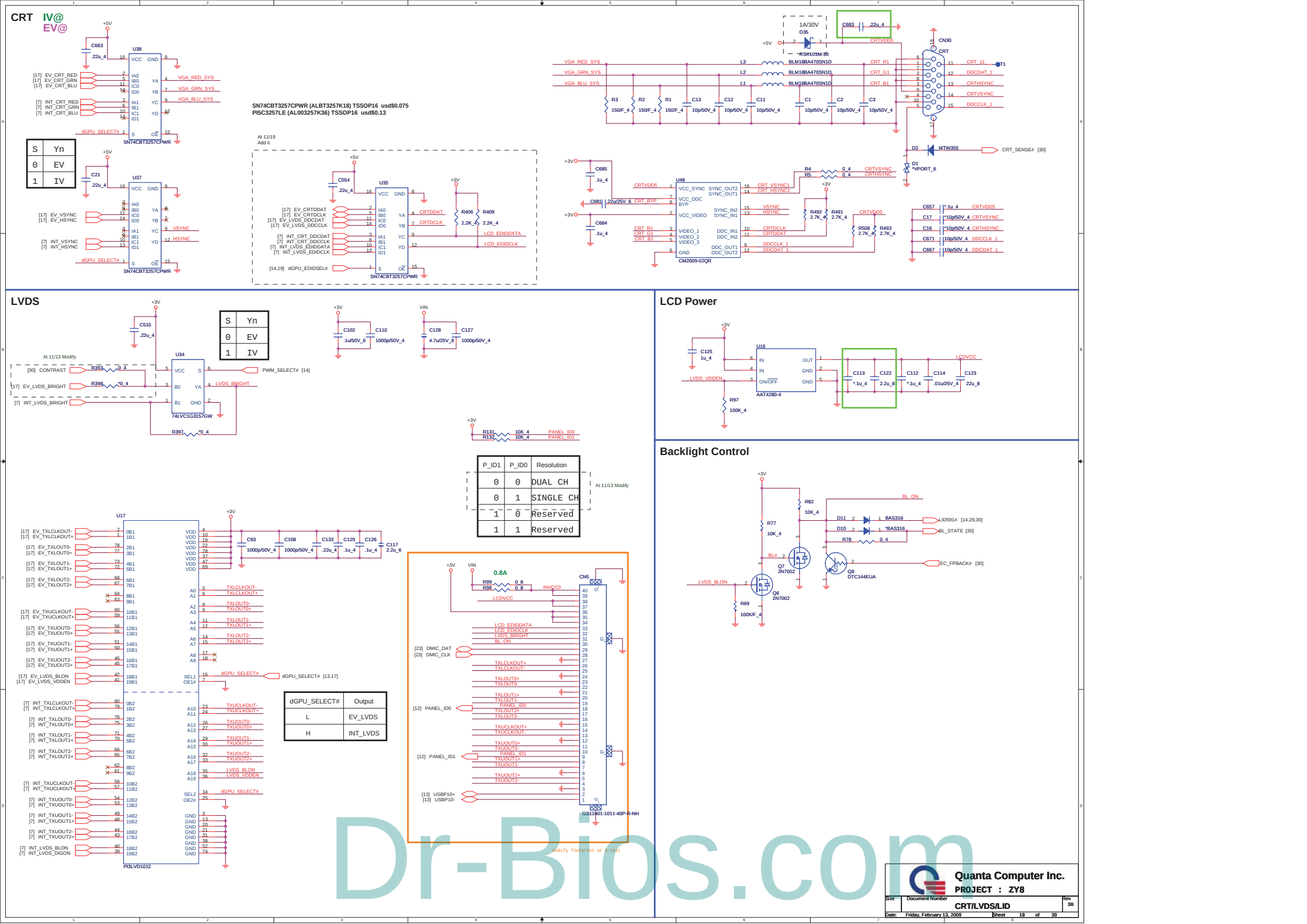
At 11/14 Add it

S	Yn
0	IA0
1	IA1

U13 *SN74CBT3257CPWR

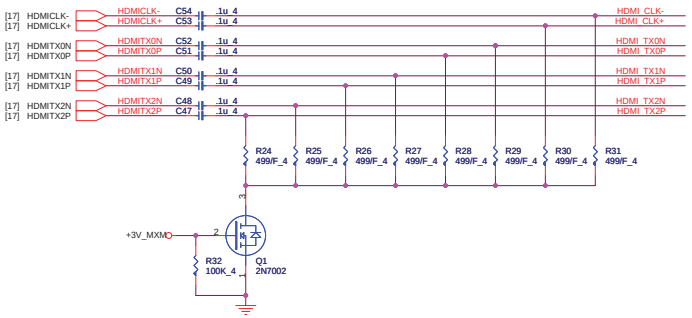
MXM use SPDIF output at B-test

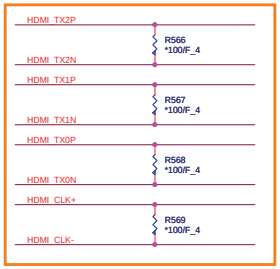
Quanta Computer Inc.
PROJECT : ZY8
Size: | Document Number: MXM3.0 | Rev: 3B
Date: Friday, February 13, 2009 | Sheet 17 of 39


CRT IV@ EV@
SN74CBT3257CPWR (ALBT3257K18) TSSOP16 usd$0.075
PI5C3257LE (AL003257K36) TSSOP16 usd$0.13
At 11/19 Add it
S Yn
0 EV
1 IV
LVDS
At 11/13 Modify
S Yn
0 EV
1 IV
74LVC1G3157GW
PI3LVD1012
P_ID1 P_ID0 Resolution
0 0 DUAL CH
0 1 SINGLE CH
1 0 Reserved
1 1 Reserved
At 11/13 Modify
dGPU_SELECT# Output
L EV_LVDS
H INT_LVDS
0.8A
GS12401-1011-40P-R-NH
modify footprint at B-test
LCD Power
AAT4280-4
Backlight Control
Quanta Computer Inc.
PROJECT : ZY8
CRT/LVDS/LID
Rev 3B
Date: Friday, February 13, 2009
Sheet 18 of 39

HDMI

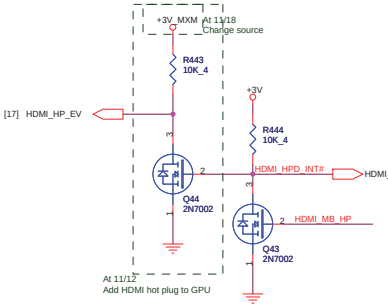
TMDS (DC-coupled)
DP(AC-coupled)



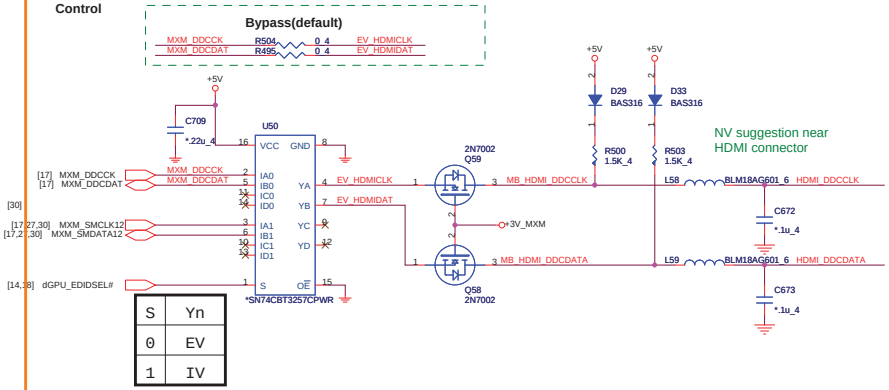


Close CN27

HDMI Hot-PLUG to SB and GPU

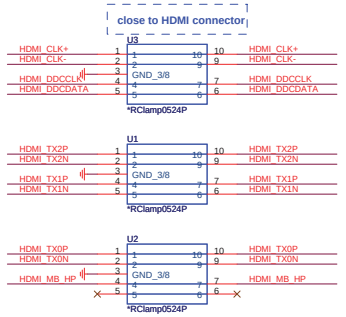


SDVO I2C Control

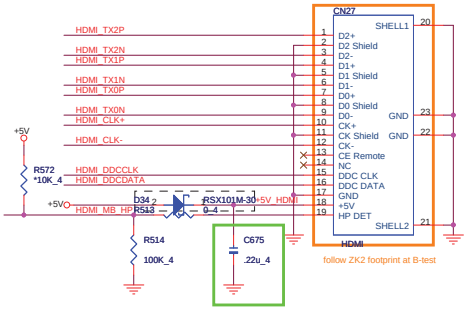


S	Yn
0	EV
1	IV

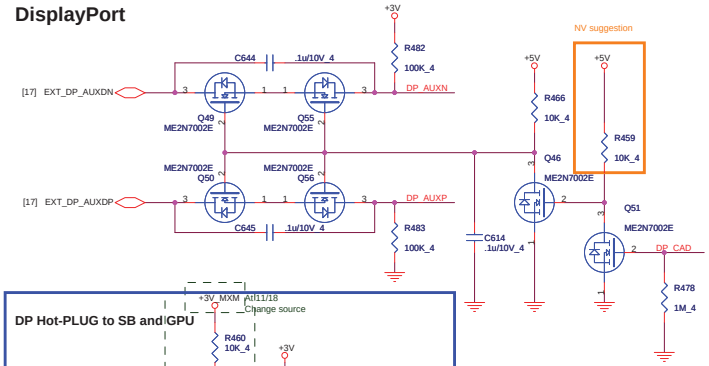
ESD Protect



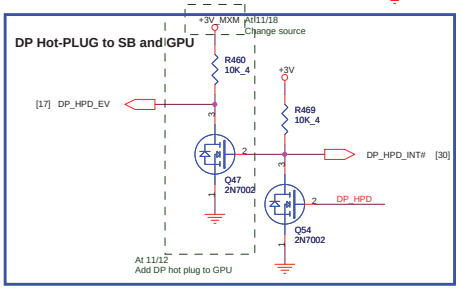
HDMI connector



DisplayPort

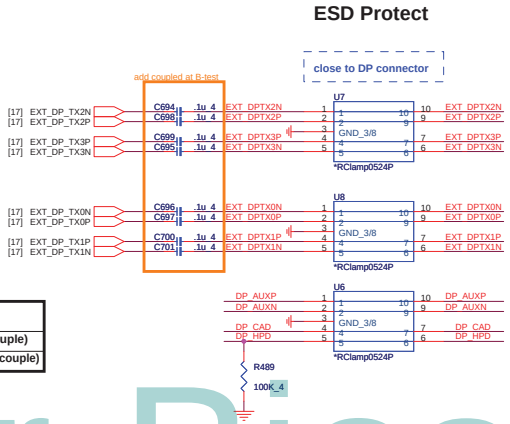


DP Hot-PLUG to SB and GPU



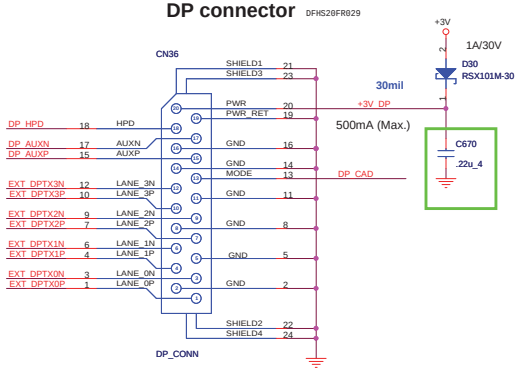
DP_CAD	Behavior
Low	DP signal (AC couple)
High	TMDS signal (DC couple)

ESD Protect



DP connector

DFHS20FR029



Quanta Computer Inc.
PROJECT : ZY8

Size	Document Number	Rev
	HDMI/DP	3B

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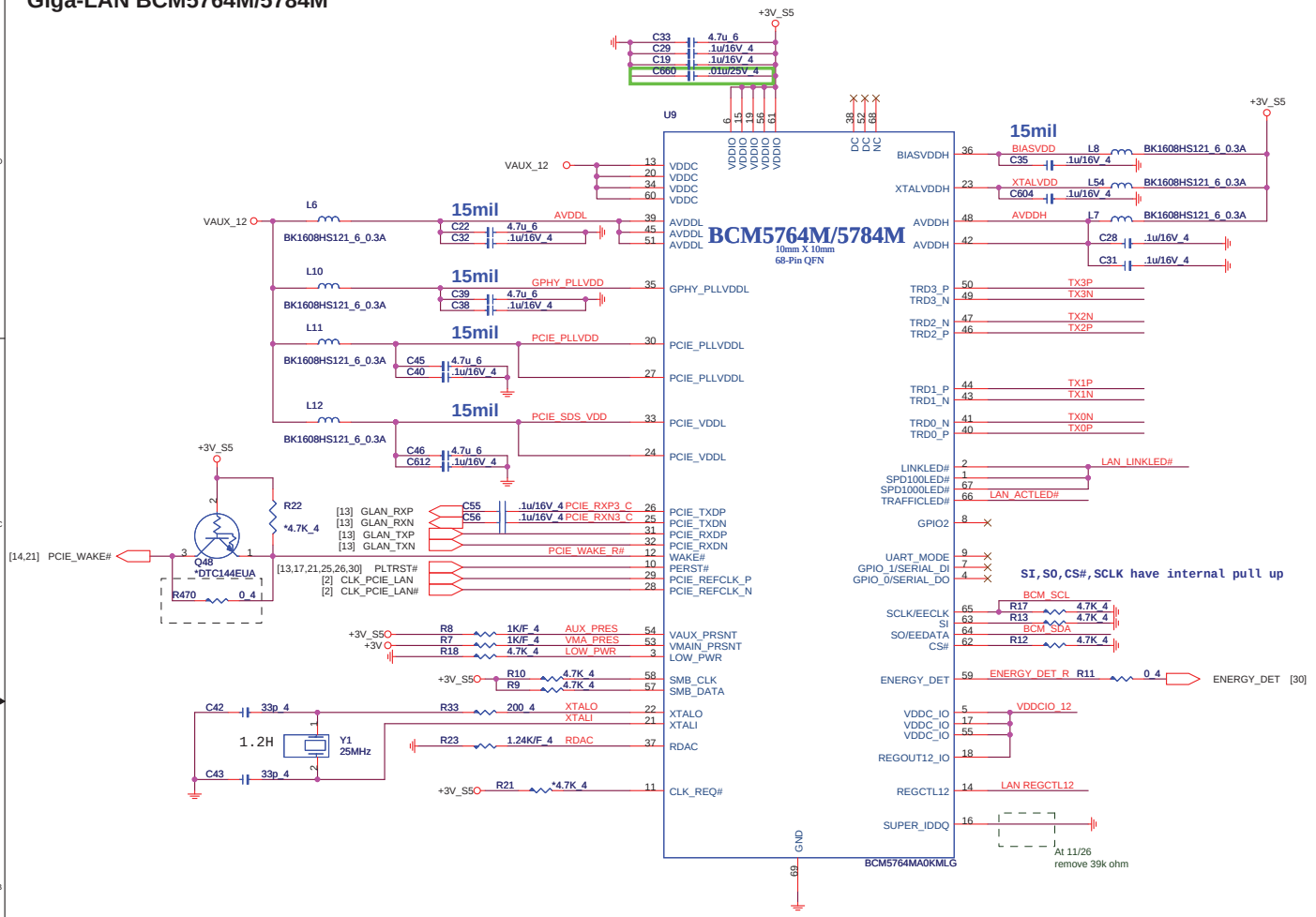
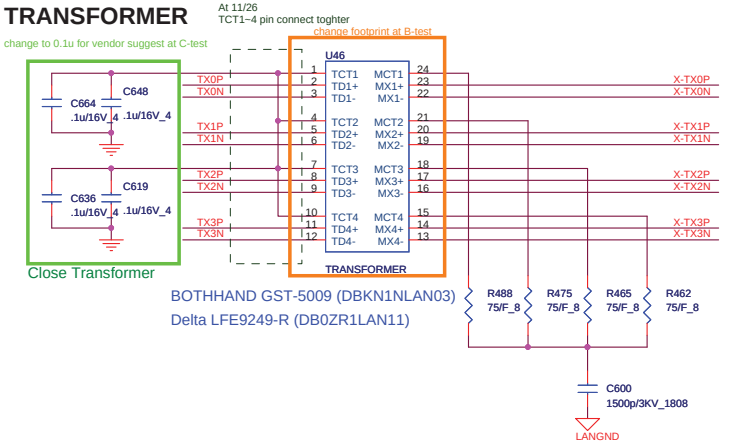
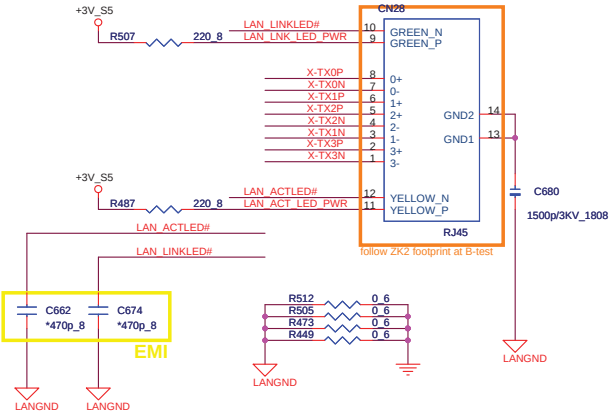
Giga-LAN BCM5764M/5784M



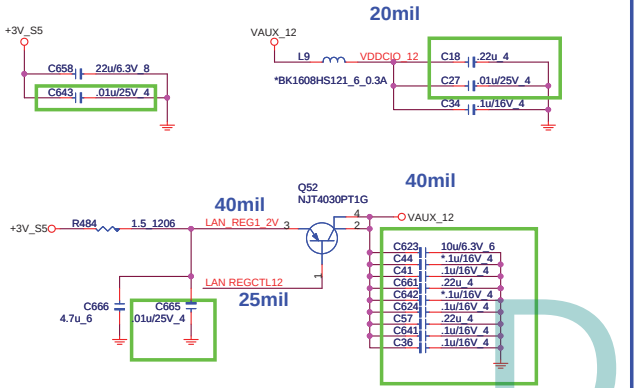
TRANSFORMER



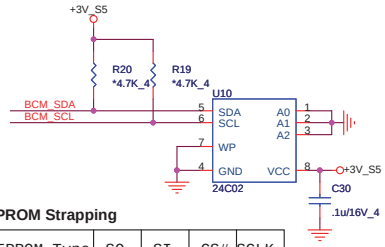
RJ45



LAN POWER



EEPROM



EEPROM Strapping

EEPROM Type	SO	SI	CS#	SCLK
24c02	1	0	0	0

Quanta Computer Inc.
PROJECT : ZY8
Size | Document Number: LAN (BCM5764M/5784M) | Rev 3B
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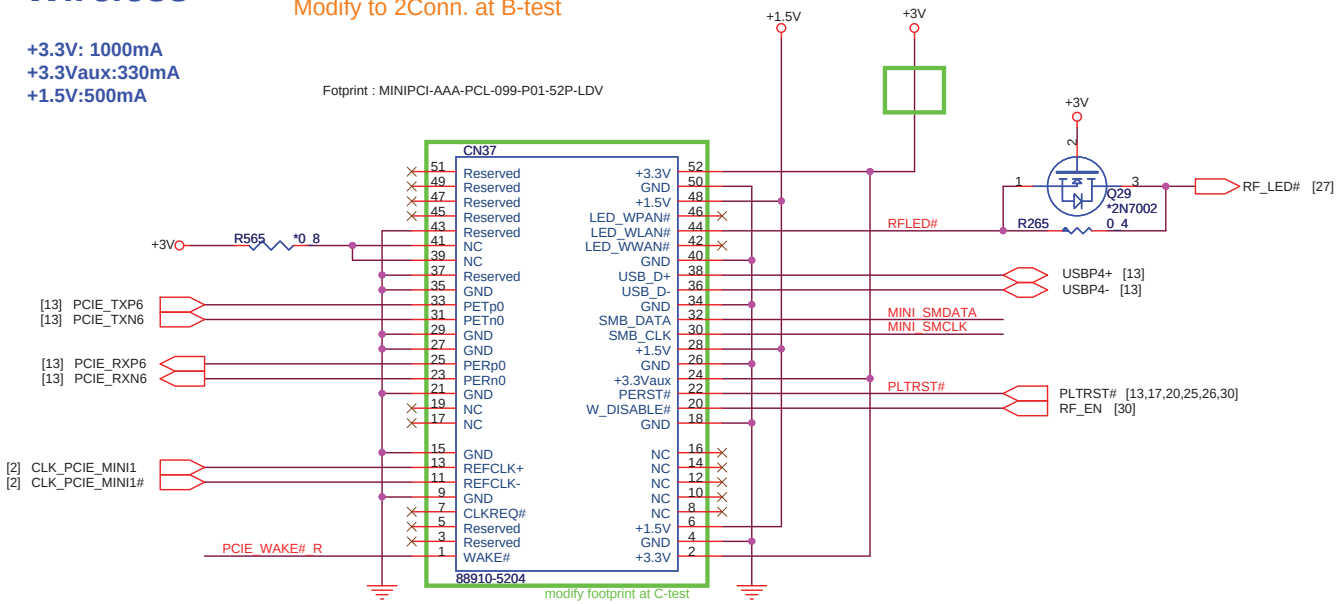
Wireless

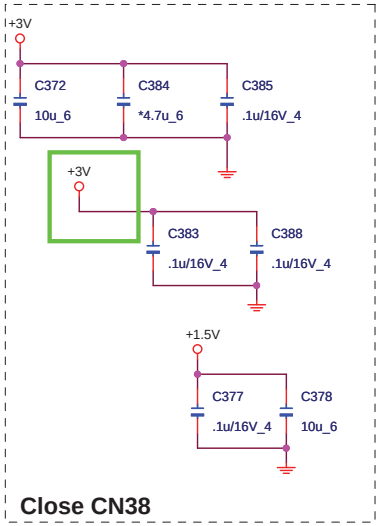
Modify to 2Conn. at B-test

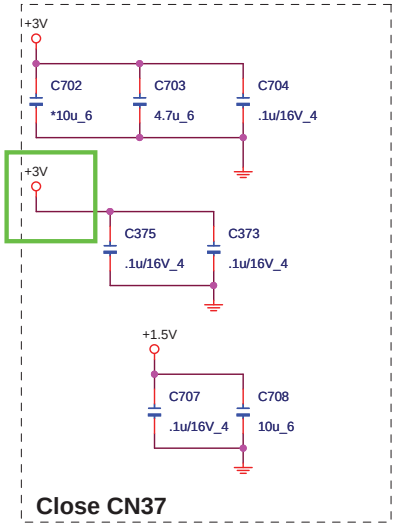
+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

Fotprint : MINIPCI-AAA-PCL-099-P01-52P-LDV

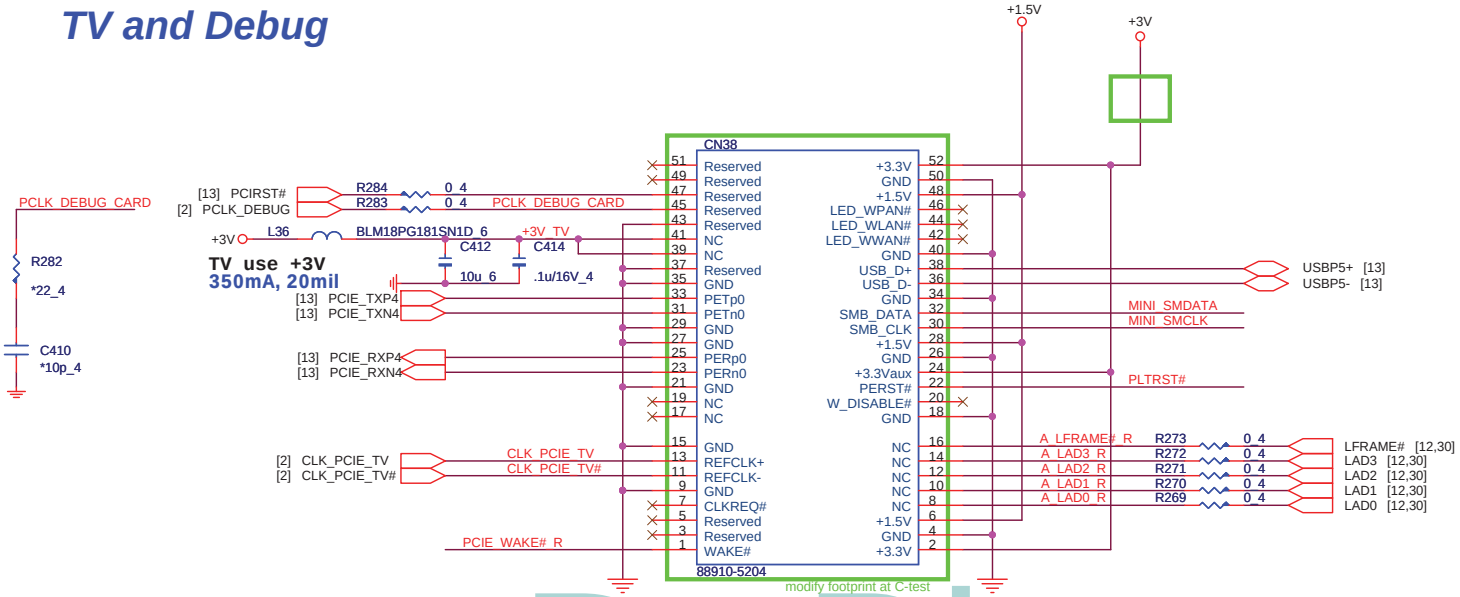


H=4

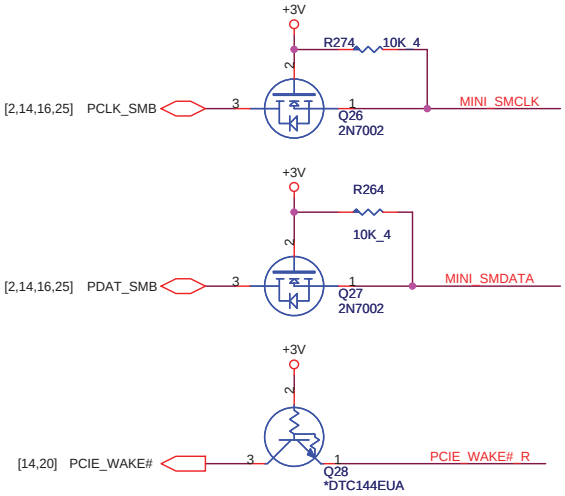




TV and Debug



H=9



Quanta Computer Inc.
PROJECT : ZY8

Size	Document Number	Rev
	MINI PCI-E card/TV	3B

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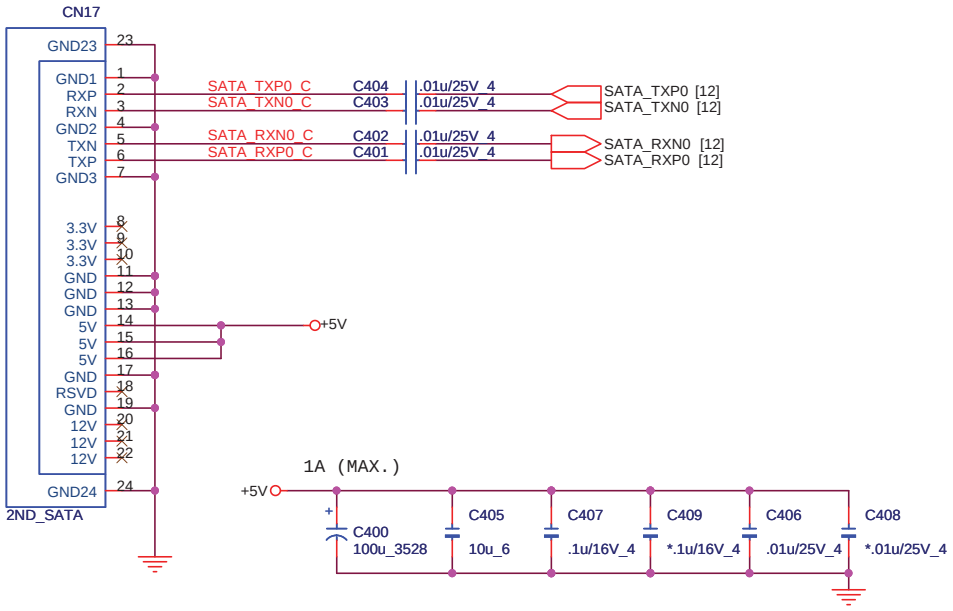
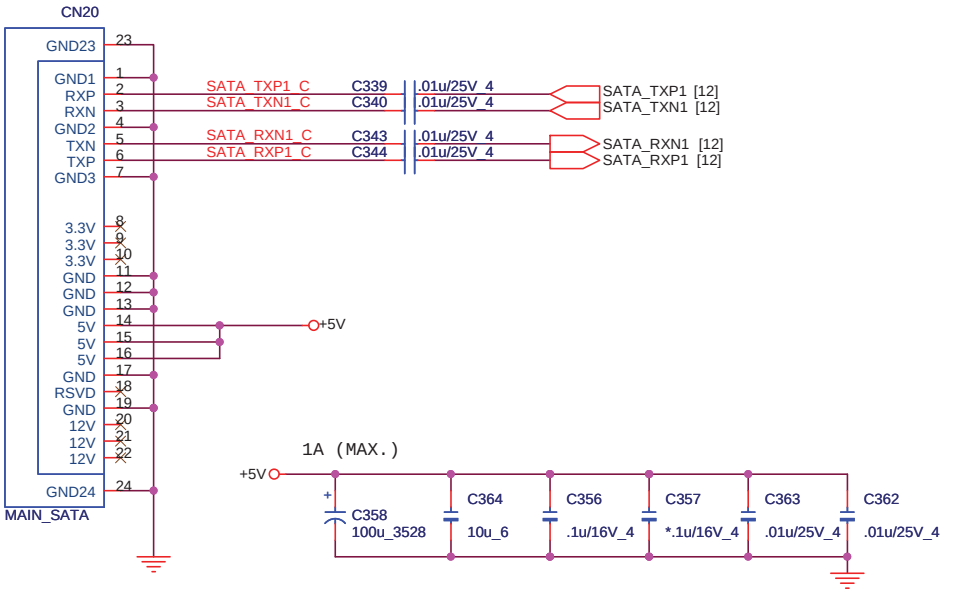
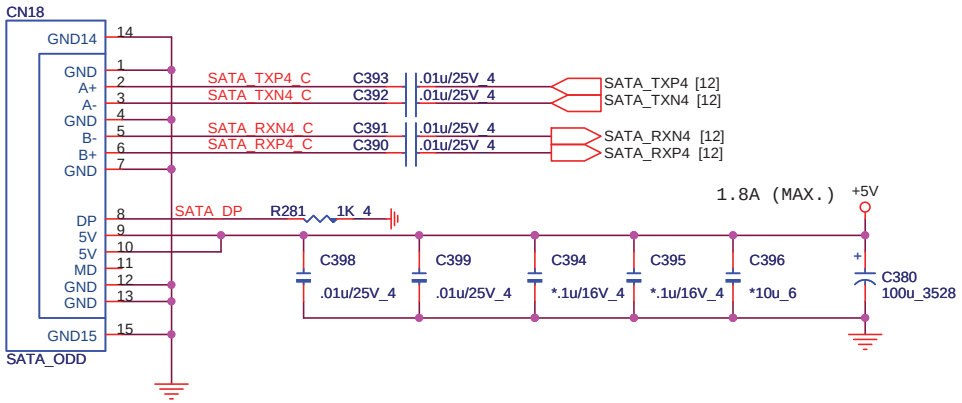
2nd SATA HDD (edge of board)



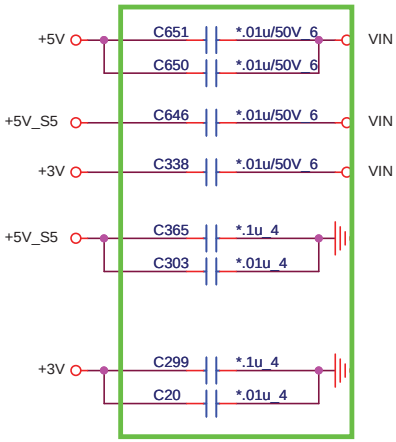
MAIN SATA HDD

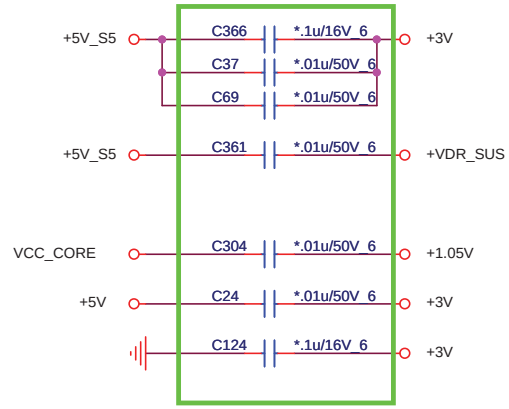


ODD (SATA)



EE RETURN-PATH CAPACITORS





Quanta Computer Inc.

PROJECT : ZY8

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	SATA-HDD/ODD	3B

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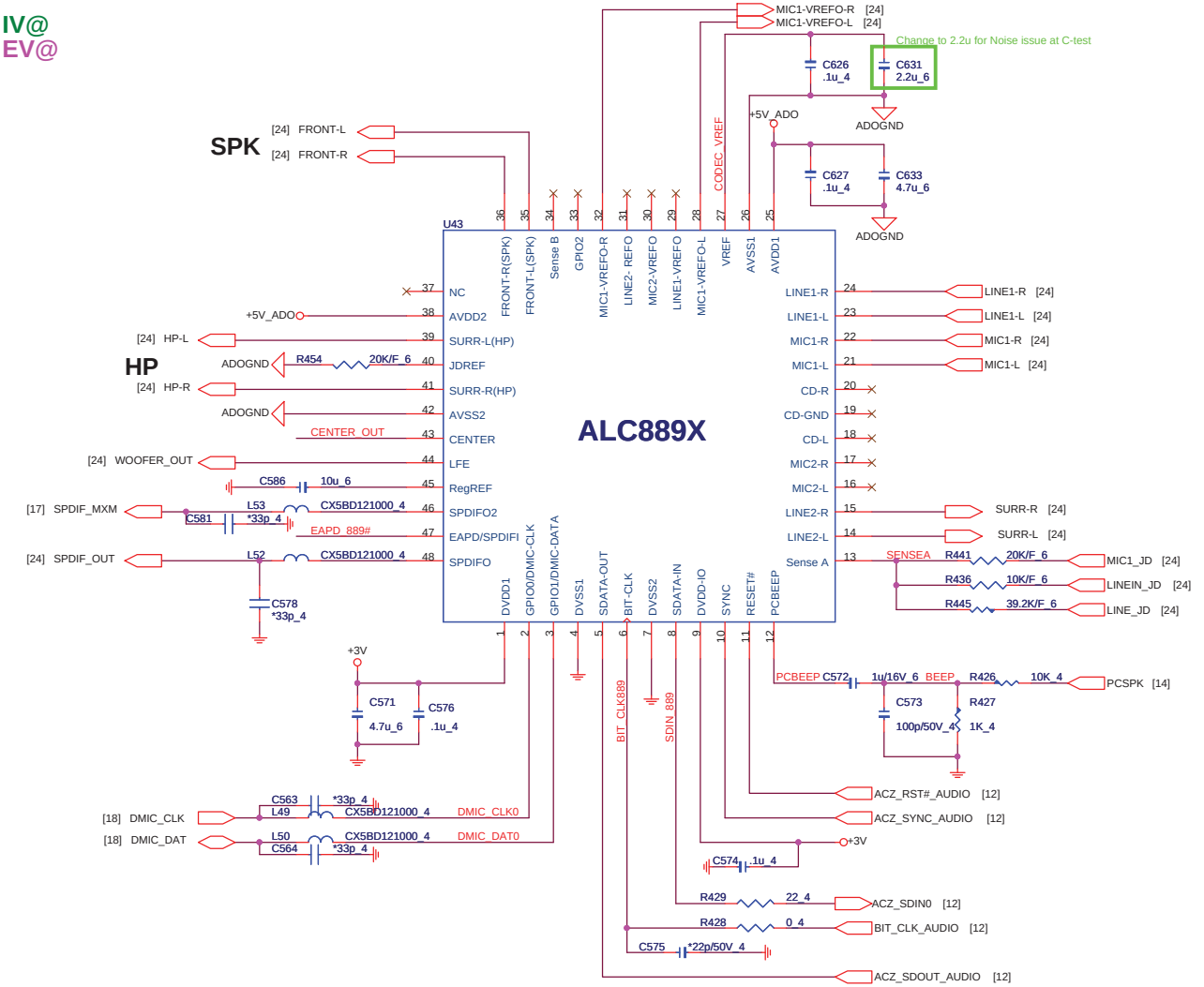
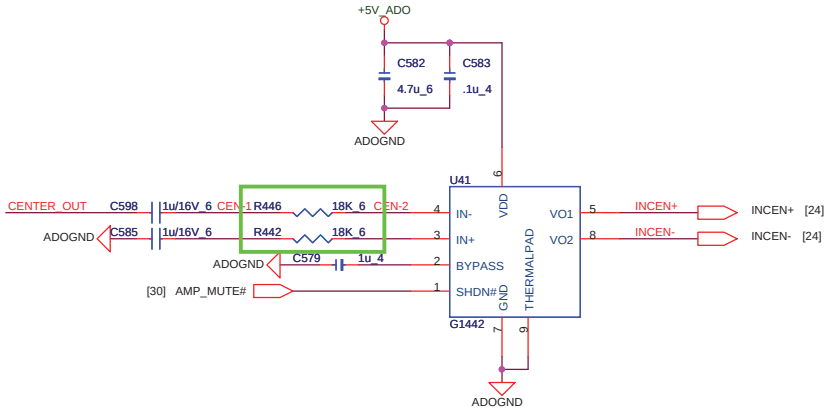
CODEC(ALC889X)

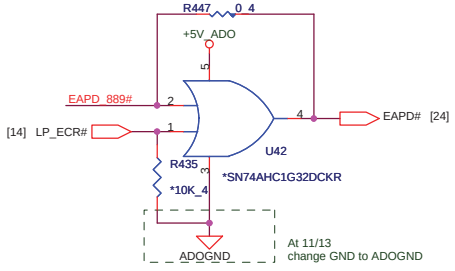
IV@
EV@



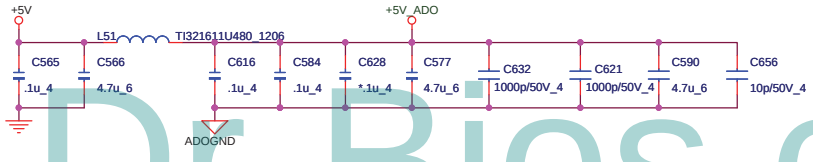
CENTER MONO



EAPD pin



CODEC/AMP Power



Quanta Computer Inc.
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	REALTEK ALC889X/MONO-AMP	3B
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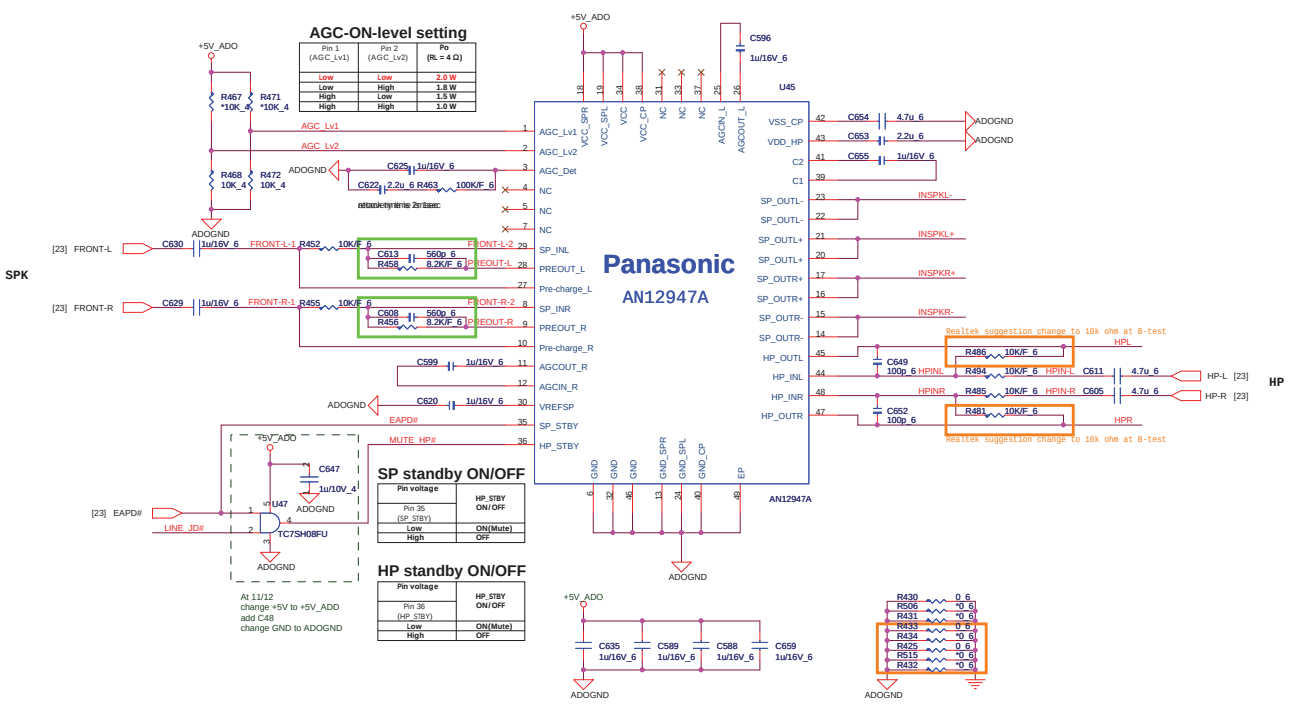
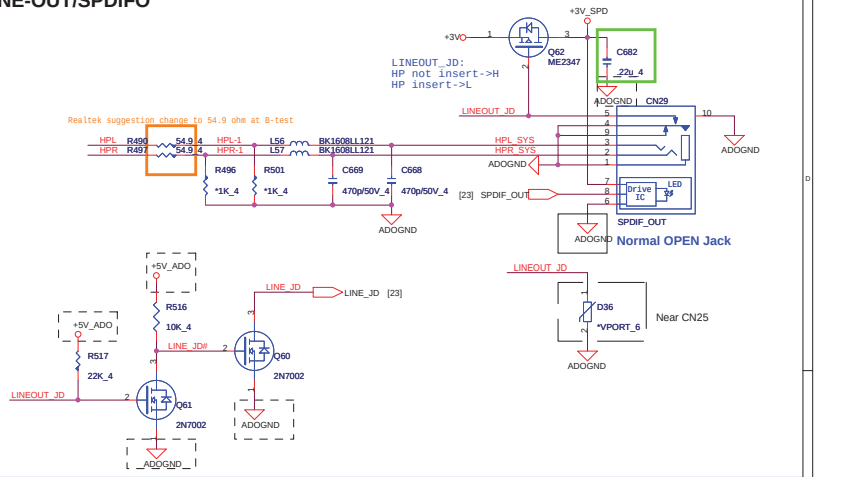
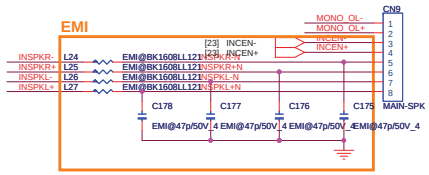
SPEAKER/HP AMP.



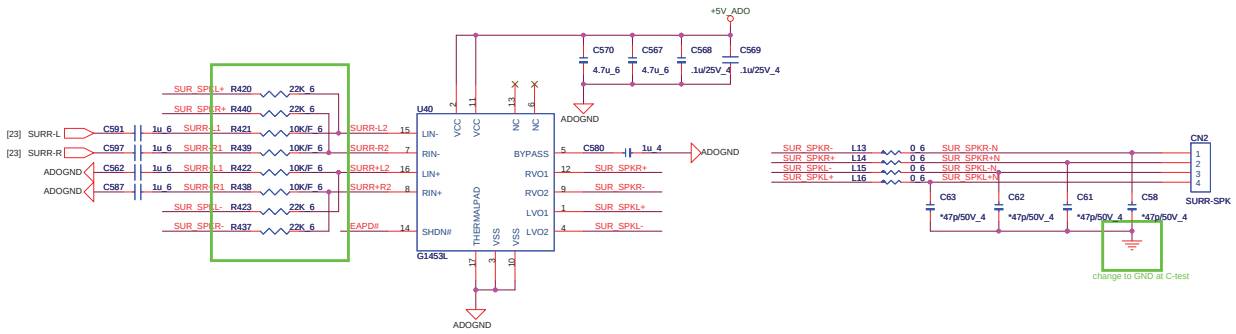
LINE-OUT/SPDIFO



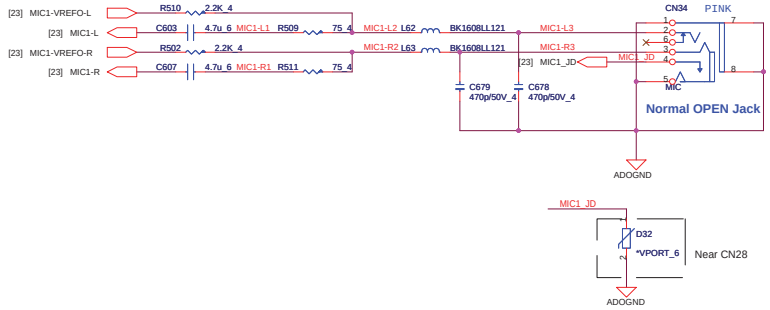
Main SPK/Center/Subwoofer



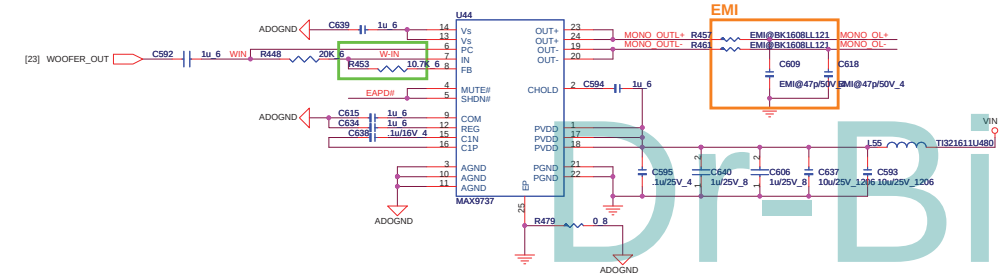
SURR-SPK



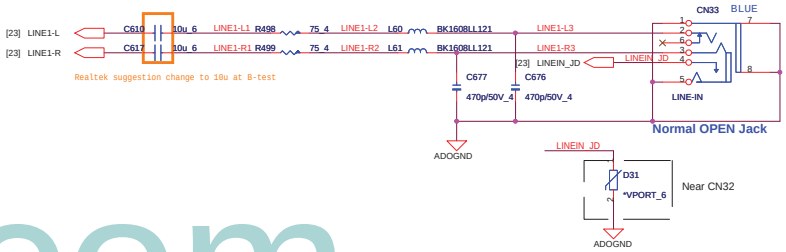
MIC



SUBWOOFER



LINE IN



Quanta Computer Inc.
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AMP/AUDIO JACK/WOOFER
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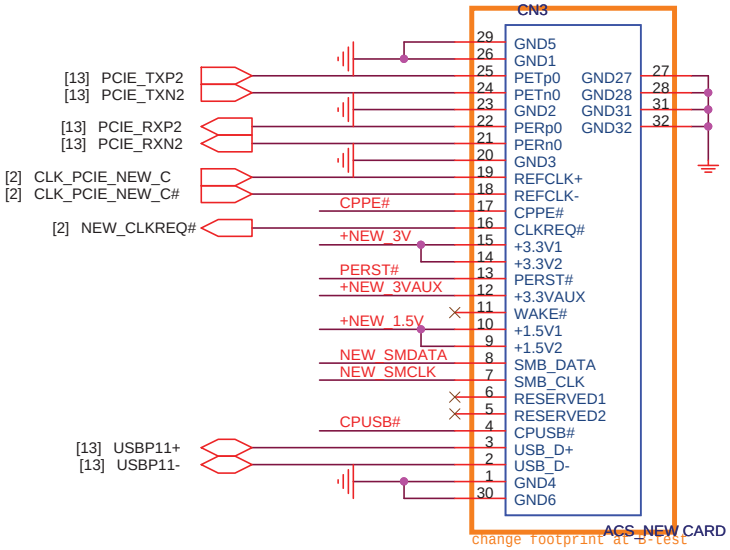
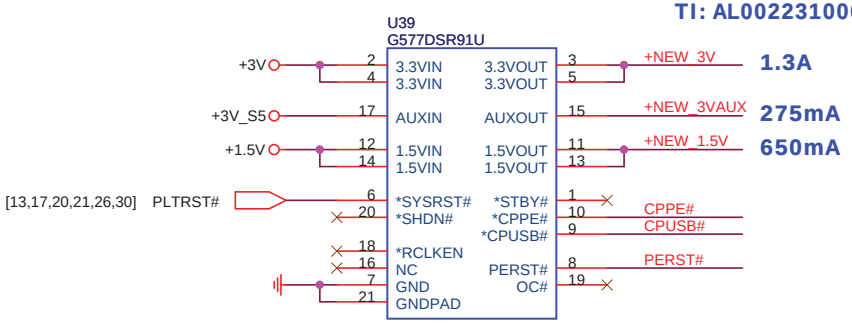
NEW CARD

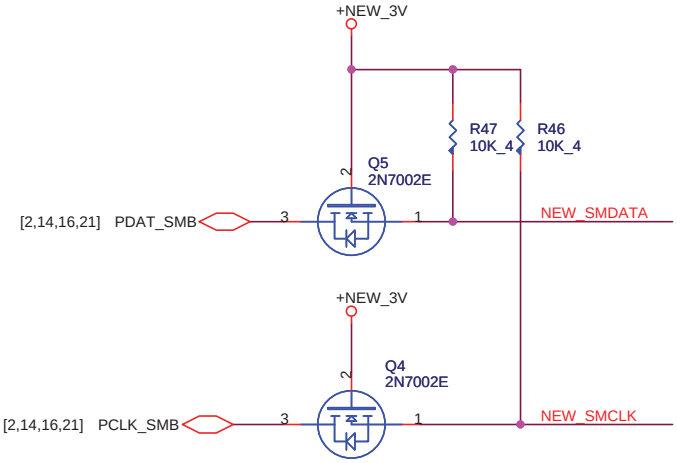


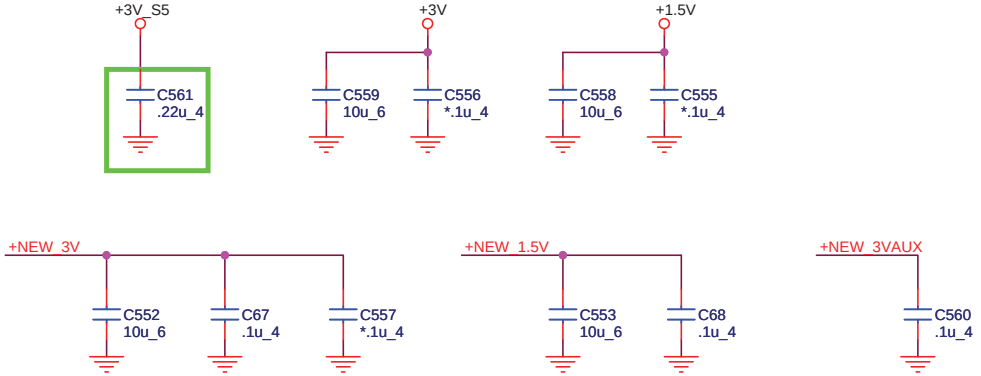
At 11/18
Change GMT cost down version.

NEW CARD'S POWER SWITCH

GMT: AL000577002
TI: AL002231000







Quanta Computer Inc.
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	NEW CARD	3B
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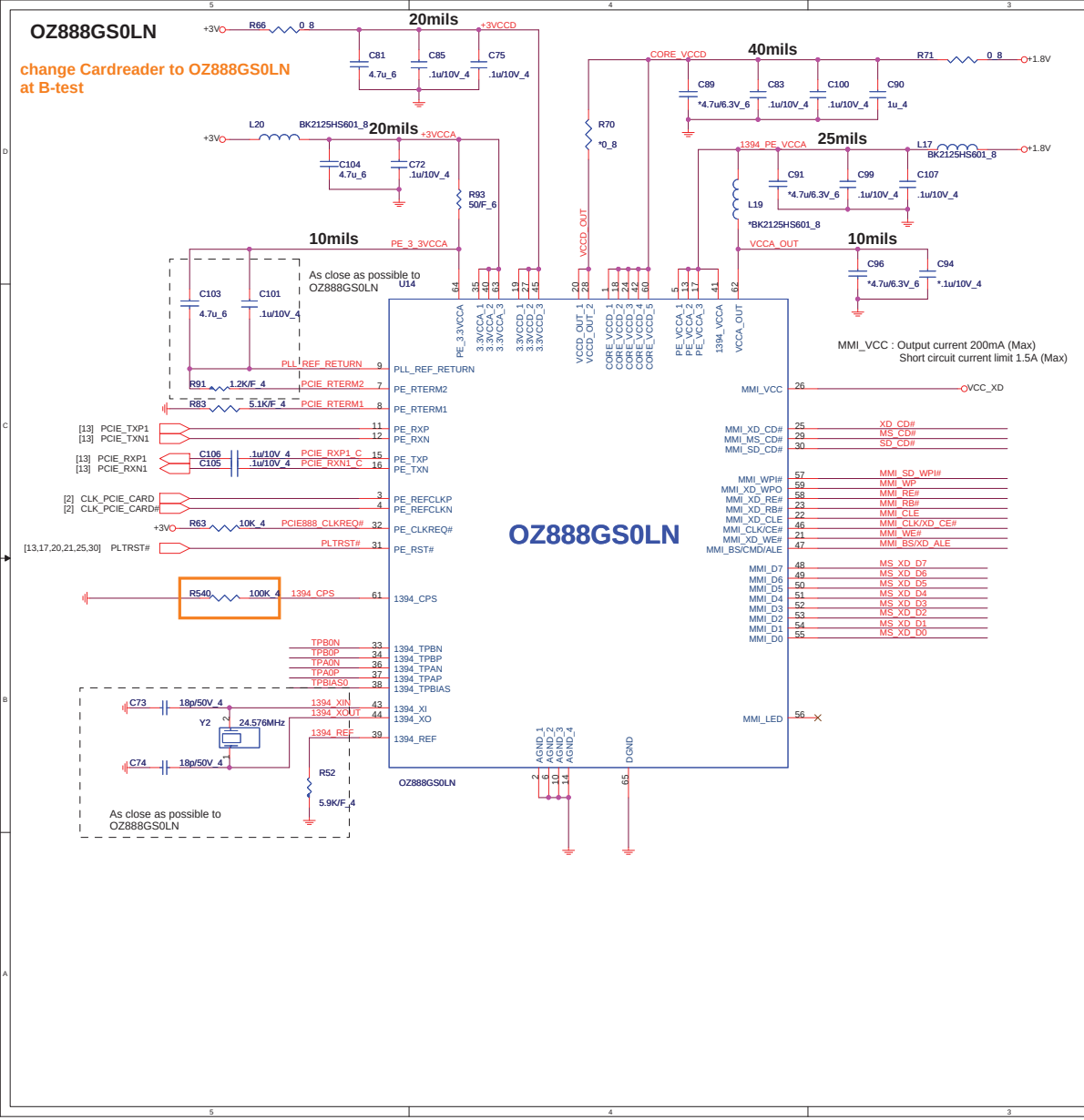

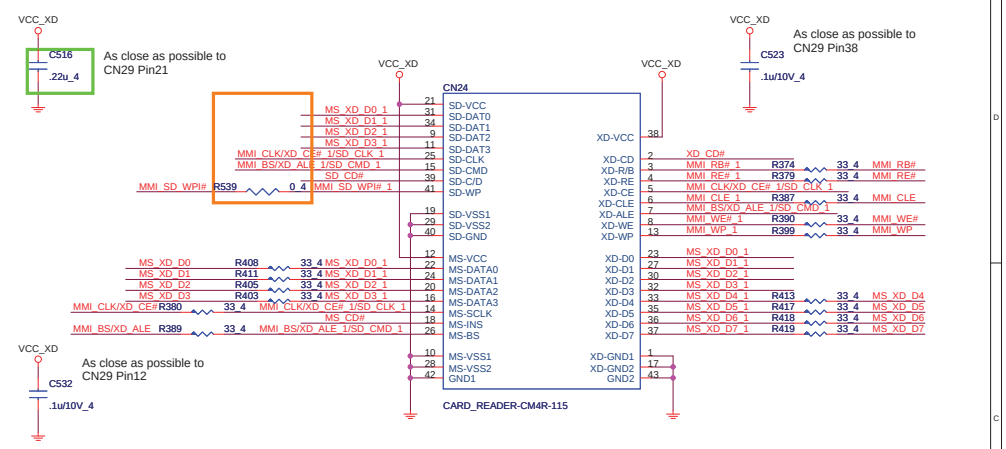

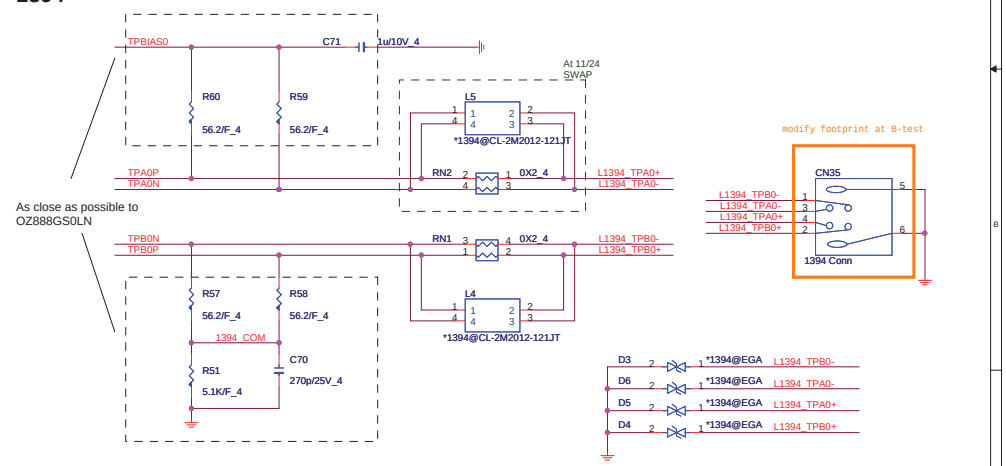

Quanta Computer Inc.

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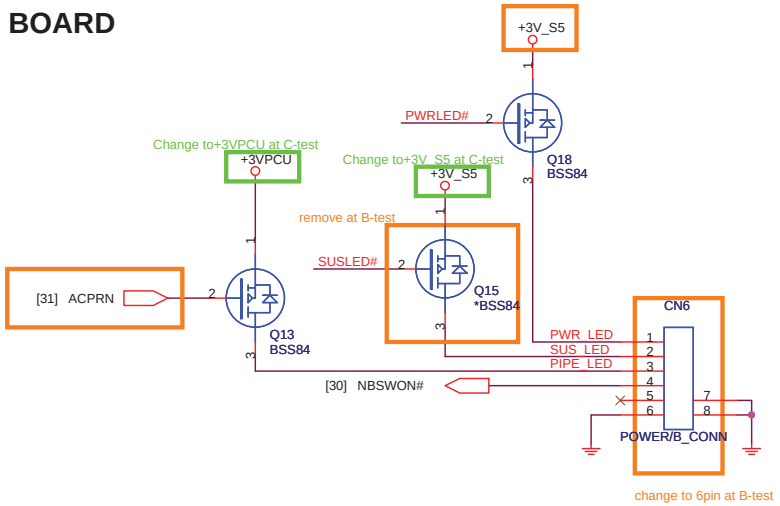
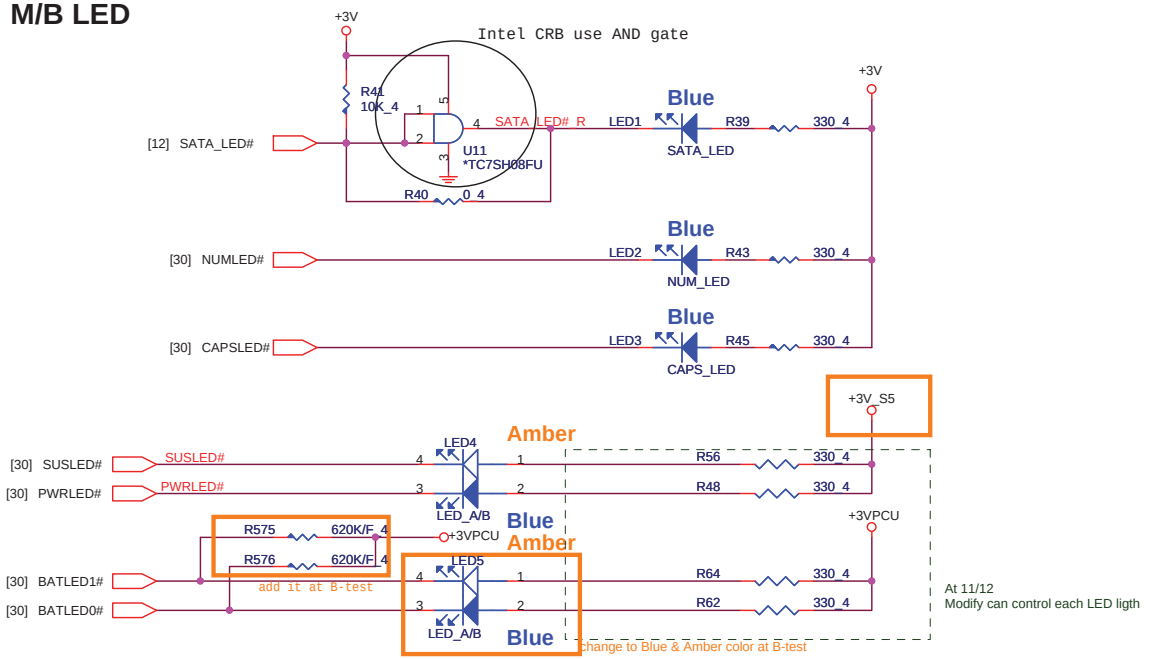
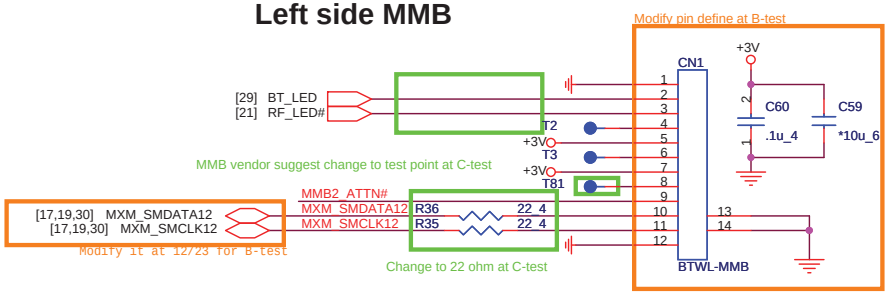
POWER BOARD



M/B LED

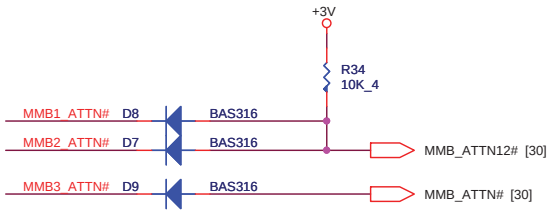


Left side MMB

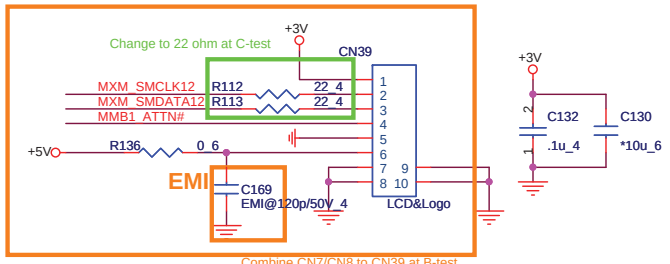


MXMCLK=MXM_SMCLK; MXMDATA=MXM_SMDATA12
MMB1 and MMB2 need add ISOLATE circuit where are on MXM page.

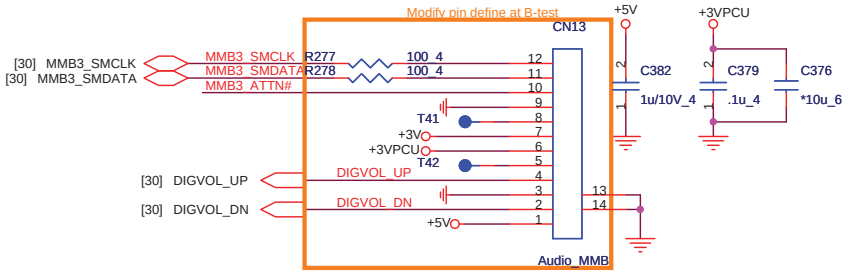
MMB Status



LCD BL_ON/OFF MMB & Backlight Logo LED



Right Side MMB



Quanta Computer Inc.		
PROJECT : ZY8		
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	POWER/MMB/LAUNCH/LED	3B
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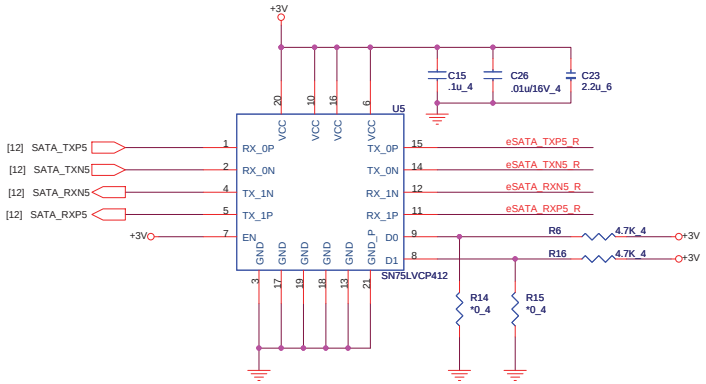
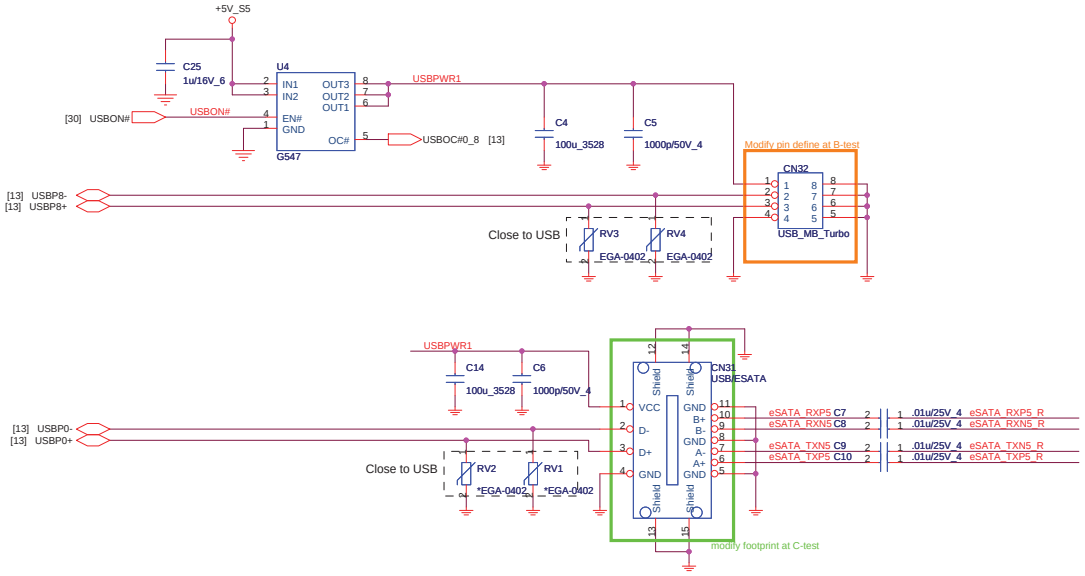
USB & ESATA

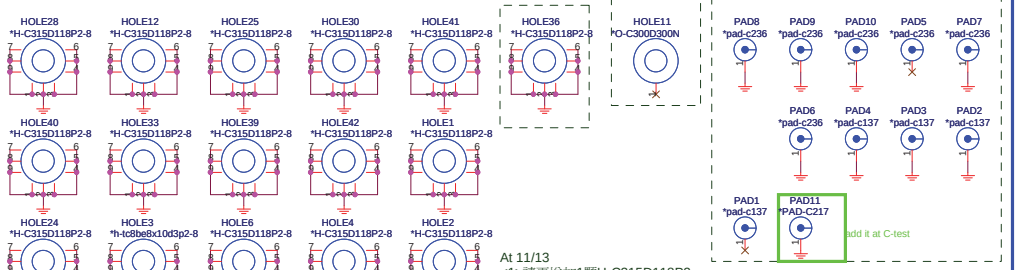


EN	D0	D1	CH-0	CH-1
0	X	X	Standby	Standby
1	0	0	0dB	0dB
1	1	0	Pre-emphasis (5dB)	0dB
1	0	1	0dB	Pre-emphasis (5dB)
1	1	1	Pre-emphasis (5dB)	Pre-emphasis (5dB)

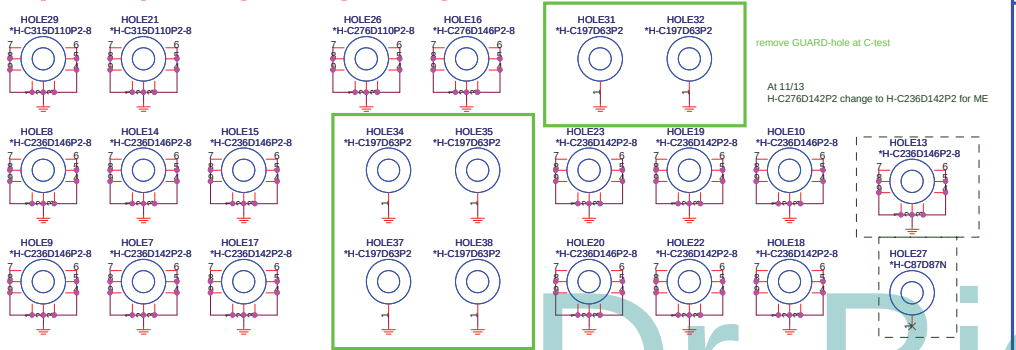


HOLES

At 11/13
change HOLE1~38 1PIN to 9PIN



At 11/13
<1>請再增加1顆H-C315D118P2
<2> HOLE22 請變更爲H-C236D142P2 (機構有改小)
<3>增加 1顆固定孔H-C87D87N ,(1788.00 944.00)



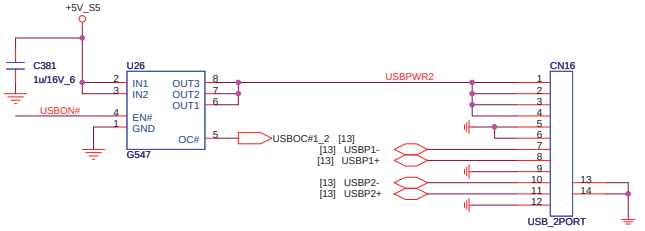
At 11/13
H-C276D142P2 change to H-C236D142P2 for ME

At 11/18
機構螺孔的部份變更如下
1.H-C236D142P2-8
=>HOLE23,HOLE24,HOLE25,HOLE31,HOLE32,HOLE33
2.H-C276D146P2-8
==>HOLE19,HOLE30,HOLE22,HOLE36
3.LAN CONN下方的螺孔未加上請, 增加一顆H-C276D118P2-8

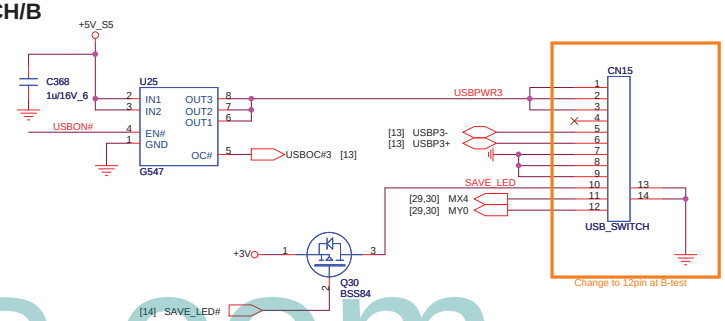
At 11/19
3.Sorry~ HOLE19,HOLE30,HOLE22,HOLE36
更作H-C276D146P2-8
請幫忙變更爲H-C236D146P2-8 才對

At 11/21
機構變更爲爲銅形狀兩個螺孔請幫忙修改footprint
HOLE41 和 HOLE12

USB_2PORT/B



USB_SWITCH/B



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	USB/eSATA	3B
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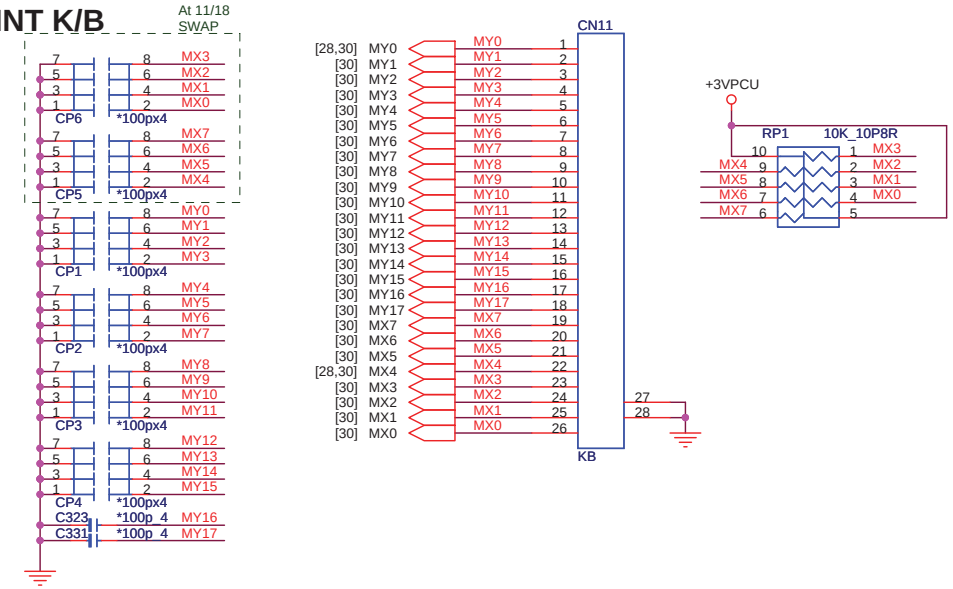
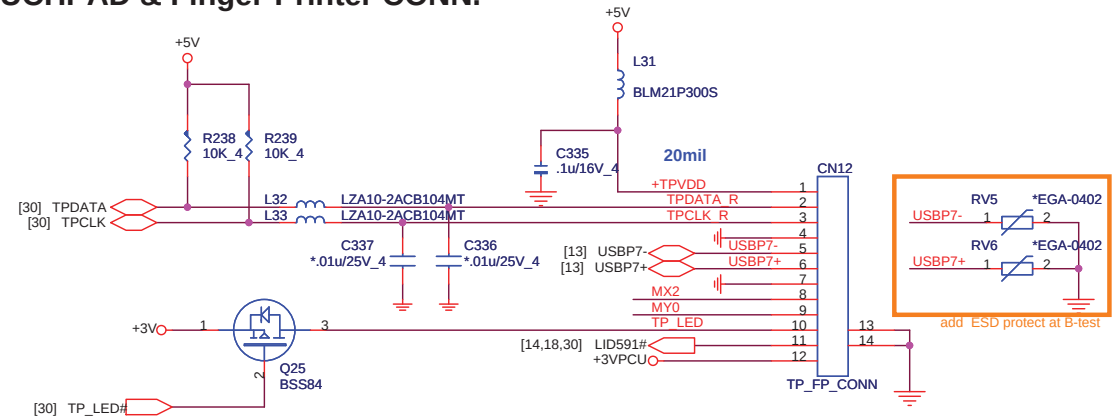
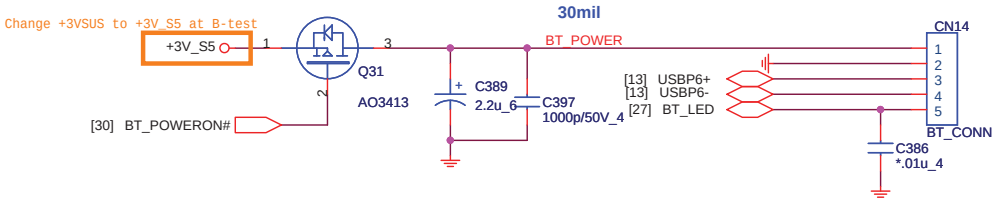
INT K/B



TOUCHPAD & Finger-Printer CONN.

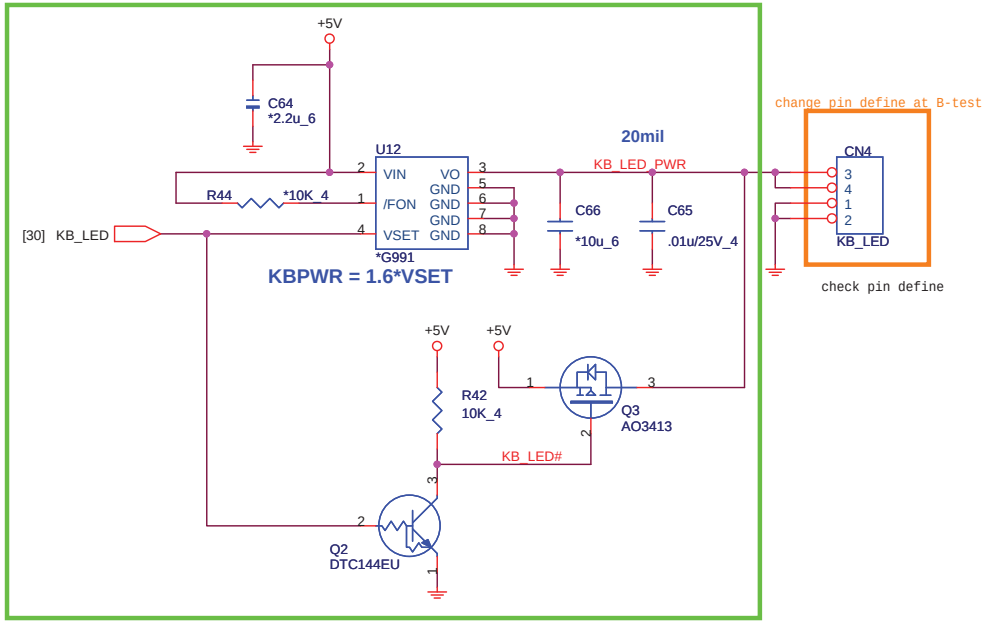


BLUETOOTH CONNECTOR

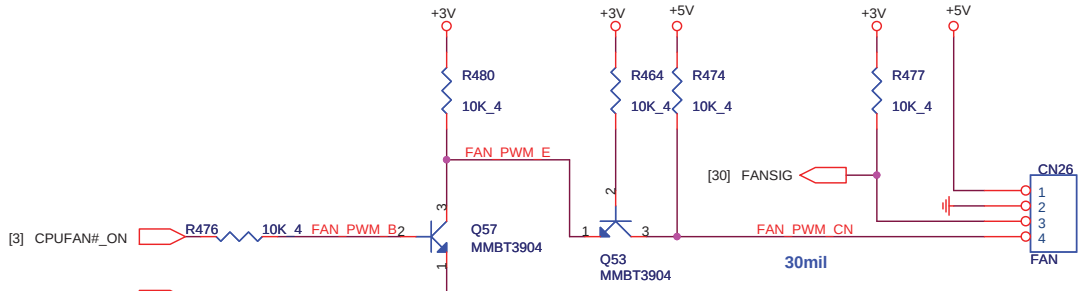


Keyboard LED control

Remove: U12, C64, R44, C66.
Stuff: Q3, R42, Q2
at C-test



CPU FAN



Quanta Computer Inc.

PROJECT : ZY8

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	KB/FAN/TP+FP/BT	3B

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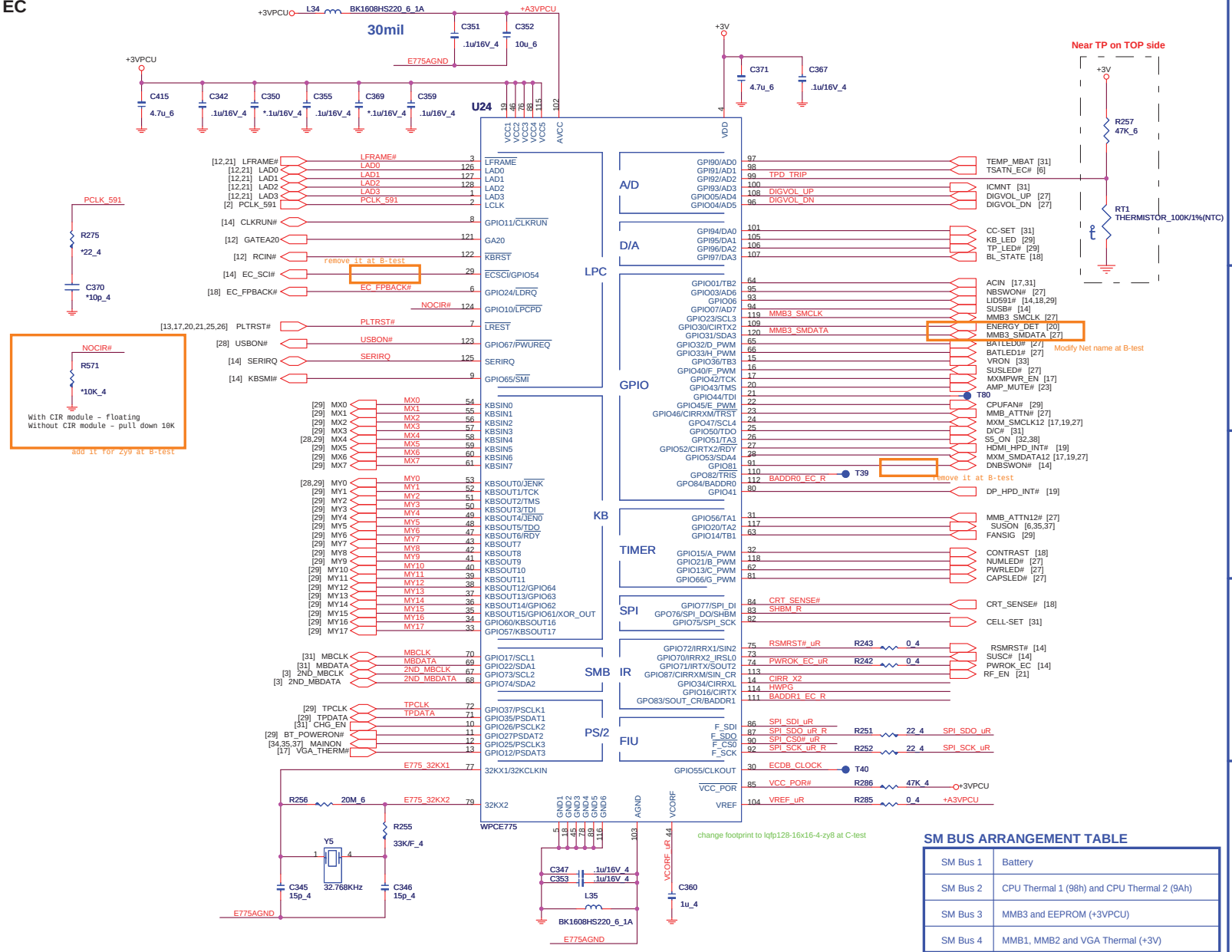
EC



I/O ADDRESS SETTING

BADDR1-0	I/O Address	
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

BADDR0 — BADDR0_EC_R — R260 — 10K_4
BADDR1 — BADDR1_EC_R — R259 — *10K_4
SHBM — SHBM_R — R249 — 10K_4

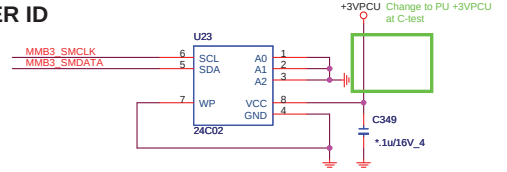
1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

SM BUS PU

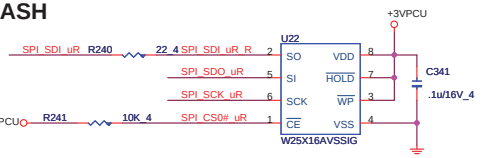
MBCLK	R248	10K_4
MBDATA	R247	10K_4
MMB3_SMCLK	R262	10K_4
MMB3_SMDATA	R263	10K_4
CRT_SENSE#	R250	*10K_4
2ND_MBCLK	R245	10K_4
2ND_MBDATA	R246	10K_4
MXM_SMCLK12	R268	10K_4
MXM_SMDATA12	R276	10K_4

change to 10K ohm,
2nd MBCLK/MBDATA and MXM_SMCLK12/MXM_SMDATA12 PU to +3V at B-test

ACER ID



SPI FLASH

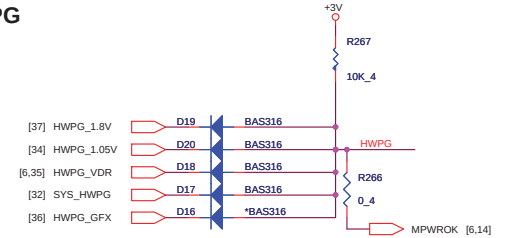


1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

At 11/24 add

Winbond	W25X16AVSSIG	AKE38ZP0N01
MXIC	MX25L1605AM2C-15G	AKE37FP0Z13
EON	EN25F16-100HIP	AKE38ZA0Q00
AMIC	A25L016	AKE38ZN0800

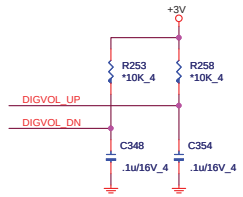
HWPG



SM BUS ARRANGEMENT TABLE

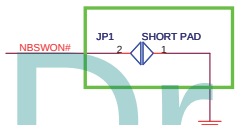
SM Bus 1	Battery
SM Bus 2	CPU Thermal 1 (98h) and CPU Thermal 2 (9Ah)
SM Bus 3	MMB3 and EEPROM (+3VPCU)
SM Bus 4	MMB1, MMB2 and VGA Thermal (+3V)

VR Cap.

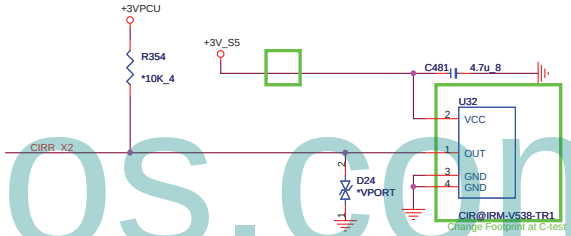


Place two near EC

POWER-ON Switch



CIR



INTERNAL KEYBOARD STRIP SET

Quanta Computer Inc.
PROJECT : ZY8

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	WPCE775C_0DG & FLASH	3B

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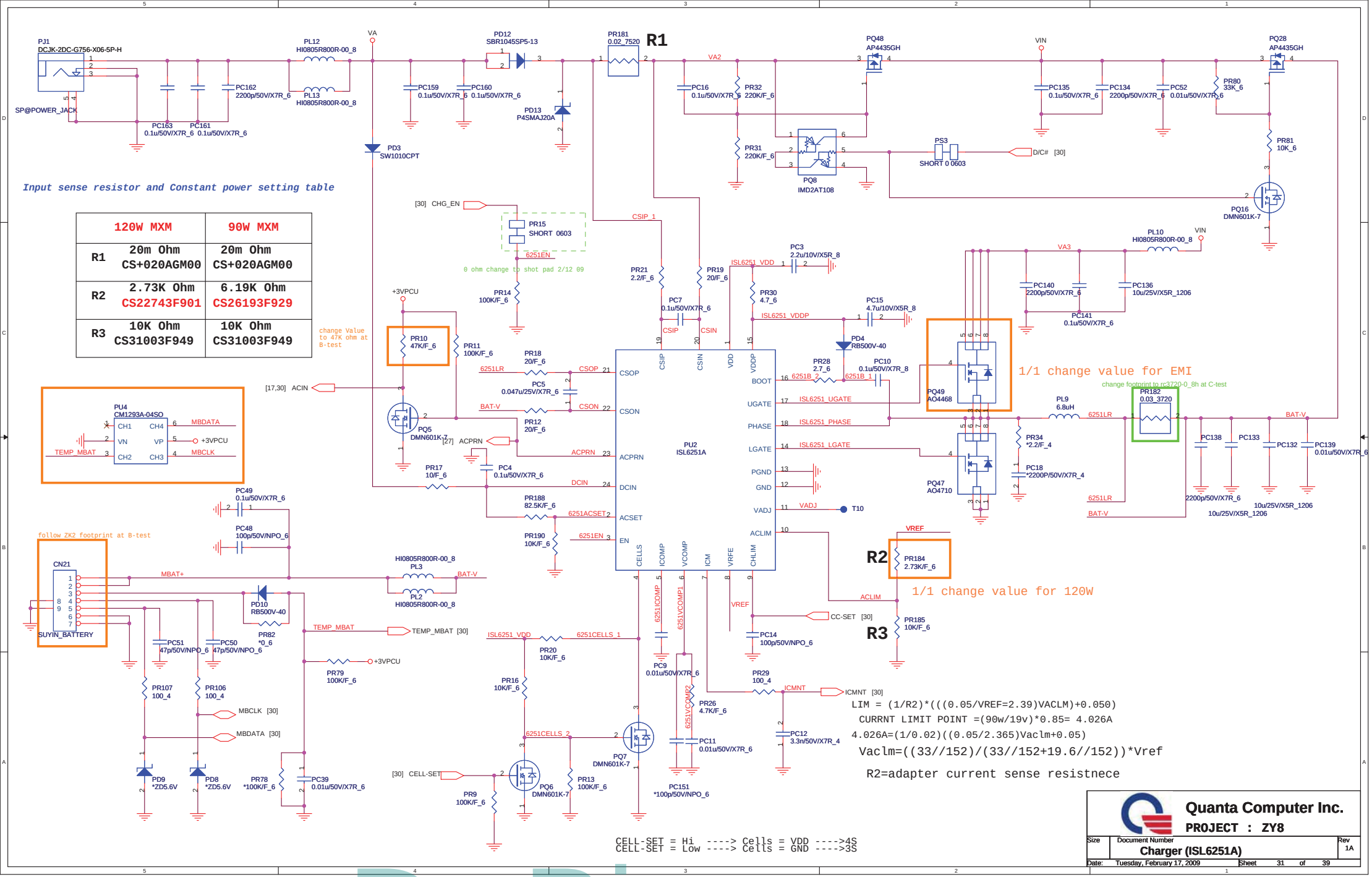
Input sense resistor and Constant power setting table
120W MXM
90W MXM
R1
20m Ohm CS+020AGM00
20m Ohm CS+020AGM00
R2
2.73K Ohm CS22743F901
6.19K Ohm CS26193F929
R3
10K Ohm CS31003F949
10K Ohm CS31003F949
change Value to 47K ohm at B-test
0 ohm change to shot pad 2/12 09
1/1 change value for EMI
change footprint to rc3720-0_8h at C-test
1/1 change value for 120W
follow ZK2 footprint at B-test
LIM = (1/R2)*(((0.05/VREF=2.39)VACLM)+0.050)
CURRNT LIMIT POINT =(90w/19v)*0.85= 4.026A
4.026A=(1/0.02)((0.05/2.365)Vaclm+0.05)
Vaclm=((33//152)/(33//152+19.6//152))*Vref
R2=adapter current sense resistnece
CELL-SET = Hi ----> Cells = VDD ---->4S
CELL-SET = Low ----> Cells = GND ---->3S
Quanta Computer Inc.
PROJECT : ZY8
Charger (ISL6251A)
Tuesday, February 17, 2009
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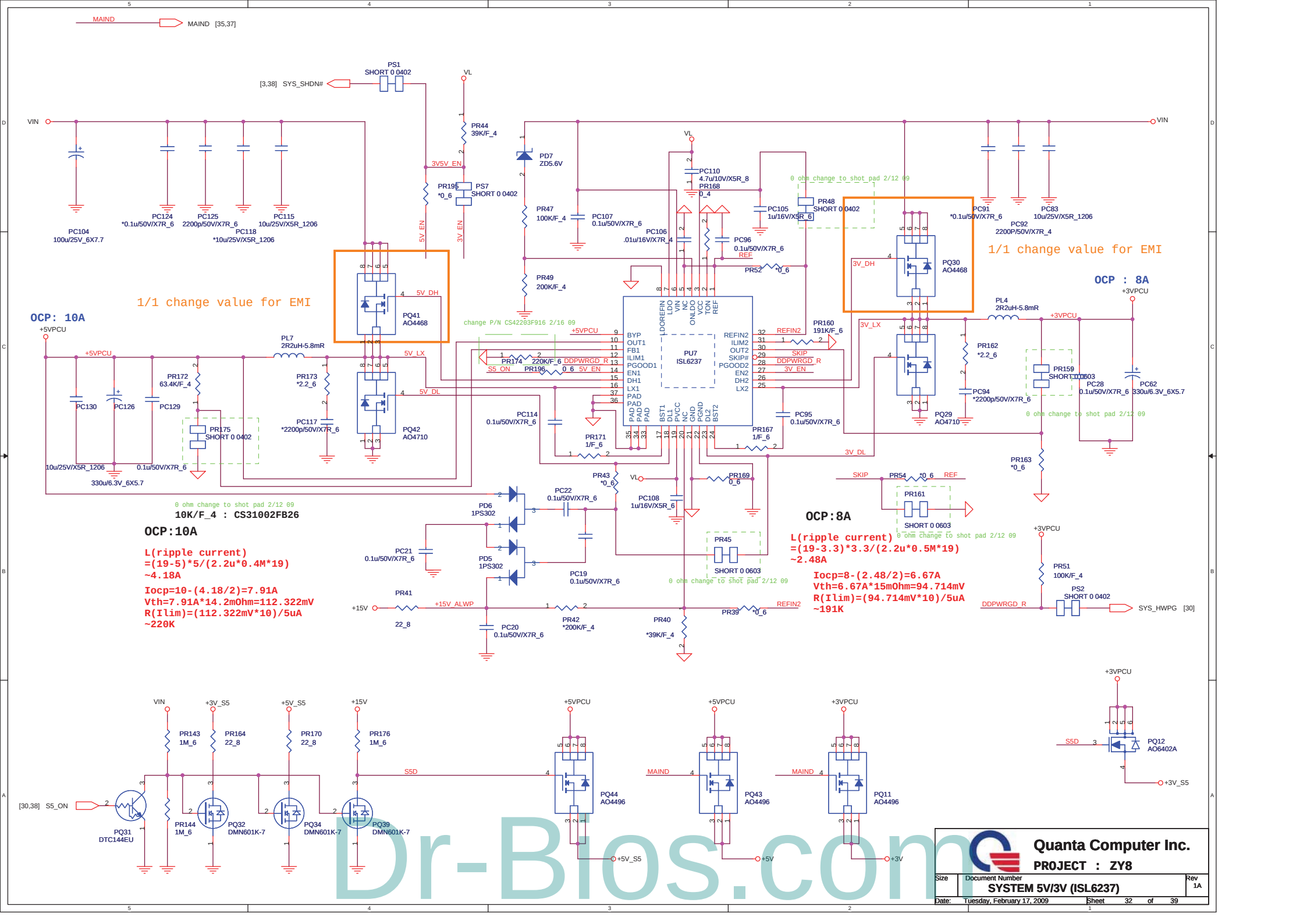
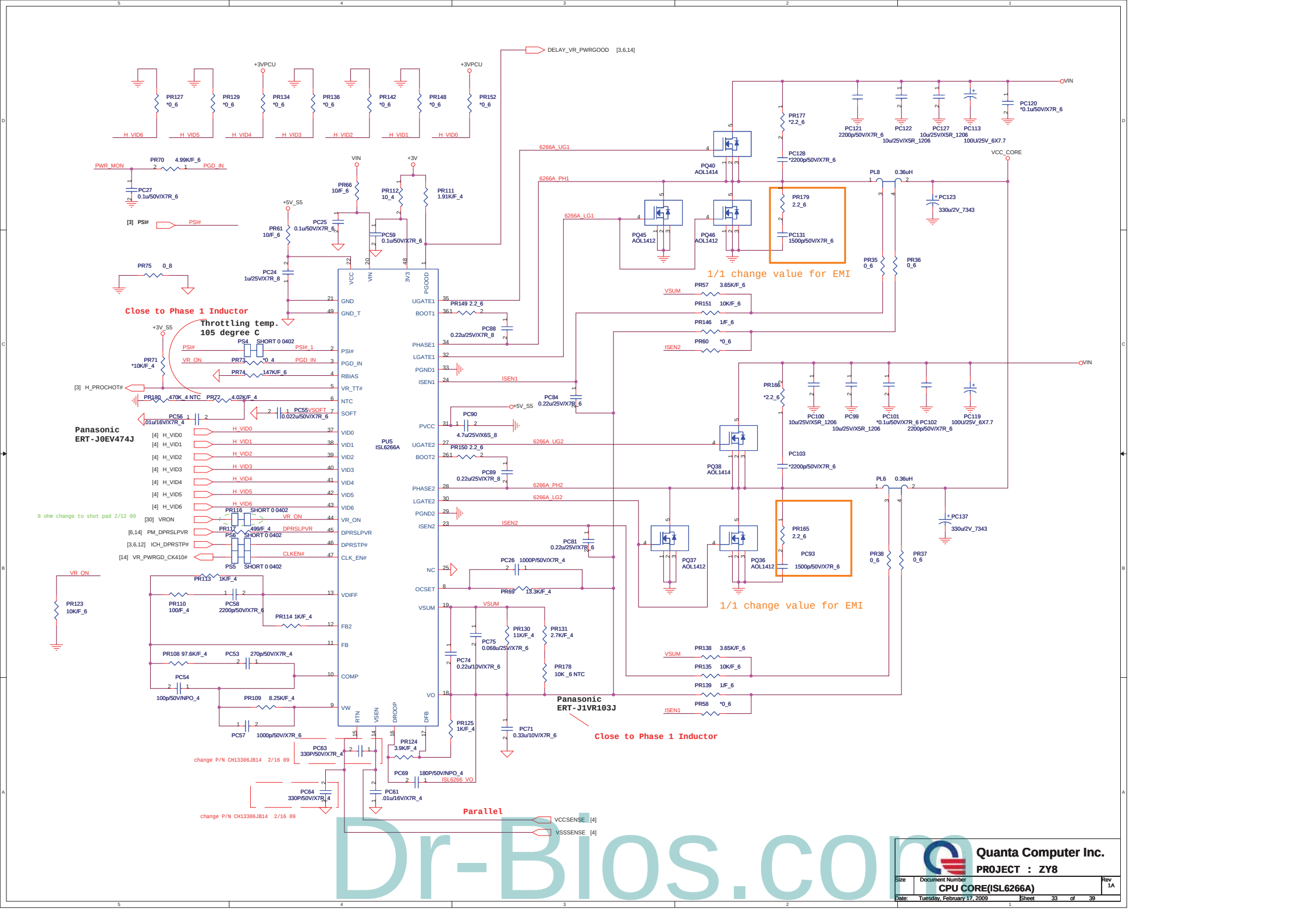
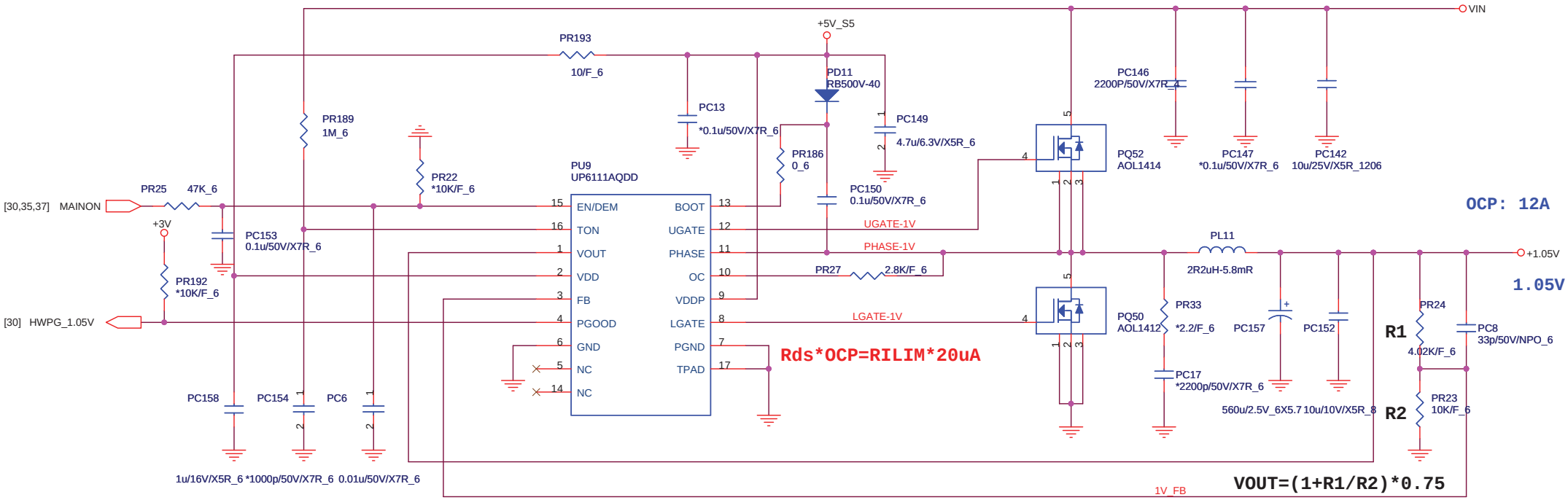

MAIND
MAIND [35,37]
PS1
SHORT 0 0402
[3,38] SYS_SHDN#
VL
VIN
PR44
39K/F_4
3V5V_EN
PR195
*0_6
PS7
SHORT 0 0402
PD7
ZD5.6V
PR47
100K/F_4
PC107
0.1u/50V/X7R_6
PR49
200K/F_4
PC104
100u/25V_6X7.7
PC124
*0.1u/50V/X7R_6
PC125
2200p/50V/X7R_6
PC118
*10u/25V/X5R_1206
PC115
10u/25V/X5R_1206
5V_EN
3V_EN
1/1 change value for EMI
PQ41
AO4468
5V_DH
OCP: 10A
+5VPCU
PL7
2R2uH-5.8mR
5V_LX
5V_DL
PR172
63.4K/F_4
PR173
*2.2_6
PC130
PC126
PC129
PR175
SHORT 0 0402
PC117
*2200p/50V/X7R_6
PQ42
AO4710
10u/25V/X5R_1206
0.1u/50V/X7R_6
330u/6.3V_6X5.7
change P/N CS42203F916 2/16 09
PU7
ISL6237
PR174
220K/F_6
DDPWRGD_R
S5_ON
PR196
0_6
5V_EN
PC114
0.1u/50V/X7R_6
PR171
1/F_6
PR43
*0_6
PC22
0.1u/50V/X7R_6
PD6
1PS302
PD5
1PS302
PC21
0.1u/50V/X7R_6
PC19
0.1u/50V/X7R_6
PR41
22_8
+15V
+15V_ALWP
PR42
*200K/F_4
PC20
0.1u/50V/X7R_6
PC108
1u/16V/X5R_6
PR169
0_6
PR45
SHORT 0 0603
PR40
*39K/F_4
PR39
*0_6
REFIN2
0 ohm change to shot pad 2/12 09
10K/F_4 : CS31002FB26
OCP:10A
L(ripple current)
=(19-5)*5/(2.2u*0.4M*19)
~4.18A
Iocp=10-(4.18/2)=7.91A
Vth=7.91A*14.2mOhm=112.322mV
R(Ilim)=(112.322mV*10)/5uA
~220K
PC110
4.7u/10V/X5R_8
PR168
0_4
PC105
1u/16V/X5R_6
PR48
SHORT 0 0402
PC106
.01u/16V/X7R_4
PC96
0.1u/50V/X7R_6
REF
PR52
*0_6
3V_DH
PQ30
AO4468
PC91
*0.1u/50V/X7R_6
PC92
2200P/50V/X7R_4
PC83
10u/25V/X5R_1206
1/1 change value for EMI
OCP : 8A
PL4
2R2uH-5.8mR
3V_LX
PR160
191K/F_6
PR162
*2.2_6
PC94
*2200p/50V/X7R_6
PR159
SHORT 0603
PC28
0.1u/50V/X7R_6
PC62
330u/6.3V_6X5.7
PQ29
AO4710
PC95
0.1u/50V/X7R_6
PR167
1/F_6
3V_DL
PR163
*0_6
SKIP
PR54
*0_6
PR161
SHORT 0 0603
OCP:8A
L(ripple current)
=(19-3.3)*3.3/(2.2u*0.5M*19)
~2.48A
Iocp=8-(2.48/2)=6.67A
Vth=6.67A*15mOhm=94.714mV
R(Ilim)=(94.714mV*10)/5uA
~191K
PR51
100K/F_4
PS2
SHORT 0 0402
DDPWRGD_R
SYS_HWPG [30]
[30,38] S5_ON
PR143
1M_6
PR164
22_8
PR170
22_8
PR176
1M_6
S5D
PQ31
DTC144EU
PR144
1M_6
PQ32
DMN601K-7
PQ34
DMN601K-7
PQ39
DMN601K-7
PQ44
AO4496
PQ43
AO4496
PQ11
AO4496
PQ12
AO6402A
+5V_S5
+5V
+3V
+3V_S5
Quanta Computer Inc.
PROJECT : ZY8
SYSTEM 5V/3V (ISL6237)
Size
Document Number
Rev
1A
Date: Tuesday, February 17, 2009
Sheet 32 of 39



Quanta Computer Inc.		
PROJECT : ZY8		
Size	Document Number: CPU CORE(ISL6266A)	Rev: 1A
Date: Tuesday, February 17, 2009	Sheet 33 of 39	



TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

AOL1412 Rdson=4.6mOhm

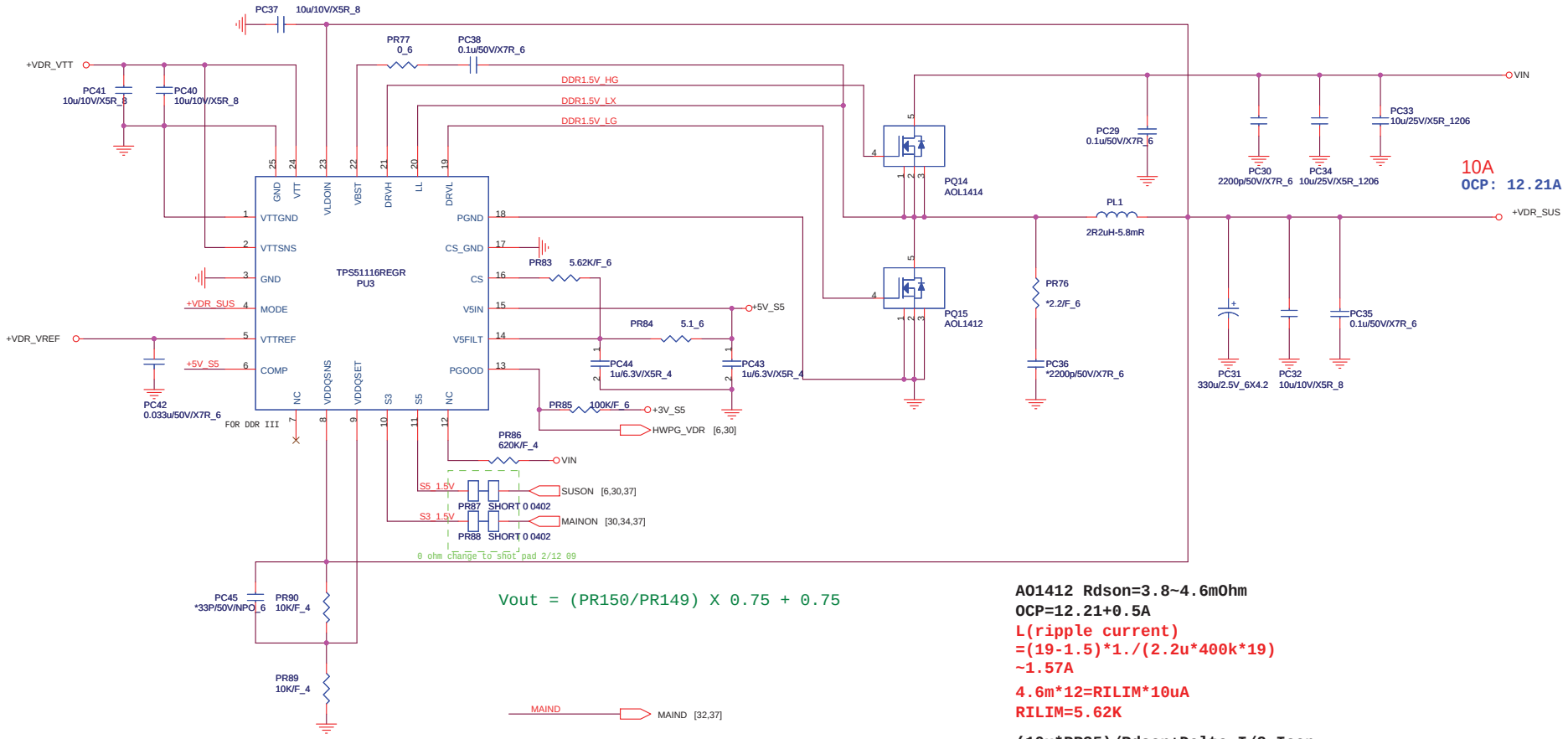
OCP=16-0.8A

L(ripple current)
=(19-1.05)*1.05/(1u*272k*19)
~3.646A

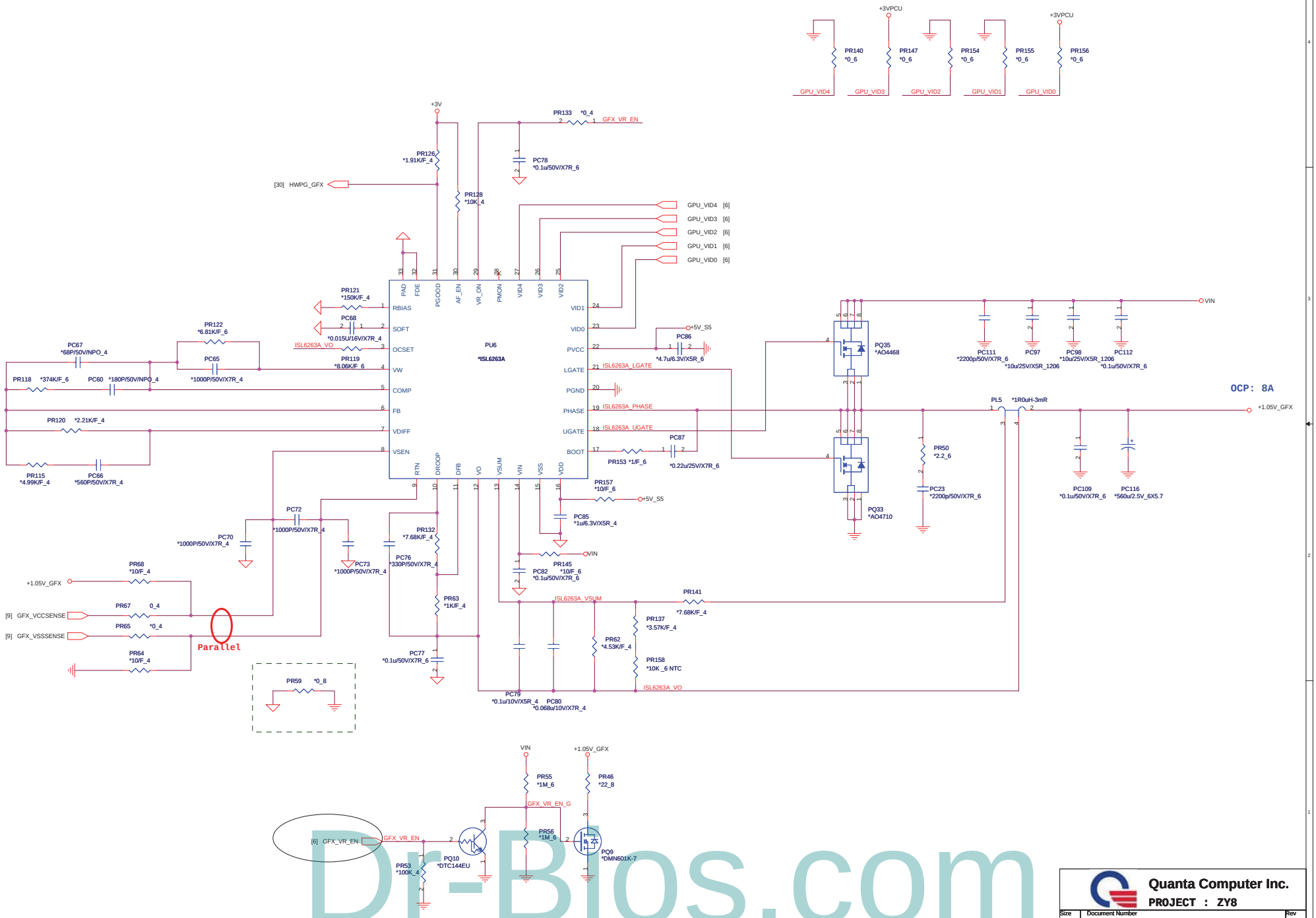
4.6m*12=RILIM*20uA

RILIM=2.76K--- 2.8K

Quanta Computer Inc.		
PROJECT : ZY8		
Size	Document Number: VCCP 1.05V(UP6111A)	Rev: 1A
Date: Tuesday, February 17, 2009	Sheet 34 of 39	

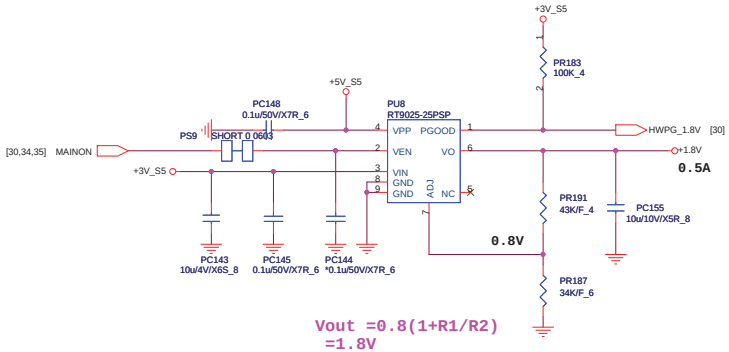


Quanta Computer Inc.		
PROJECT : ZY8		
Size	Document Number: DDR 1.8V(TPS51116)	Rev: 1A
Date: Tuesday, February 17, 2009	Sheet 35 of 39	

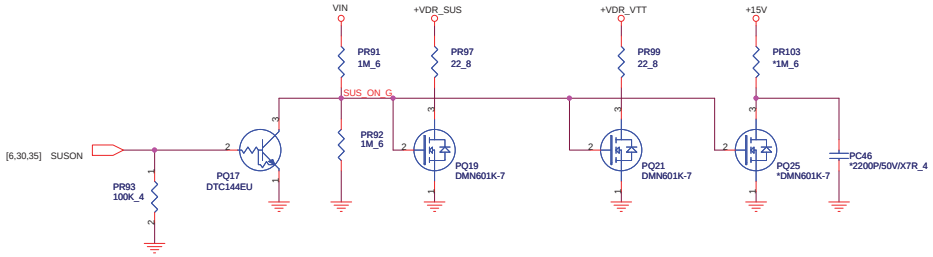


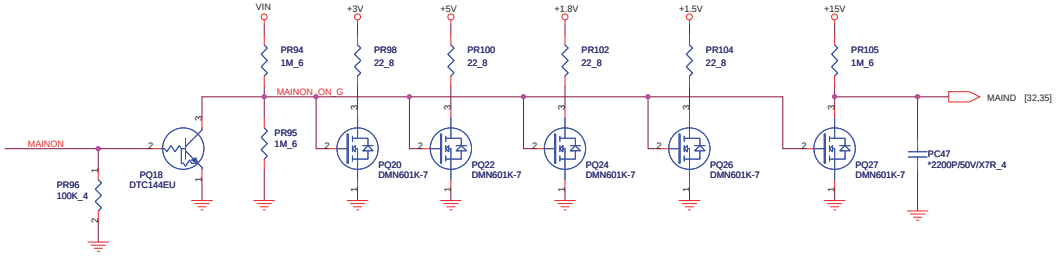
Quanta Computer Inc.
PROJECT : ZY8

Size	Document Number	Rev
	1.05V GFX (ISL6263A)	1A
Date: Tuesday, February 17, 2009	Sheet 36 of 39	



Vout =0.8(1+R1/R2)
=1.8V

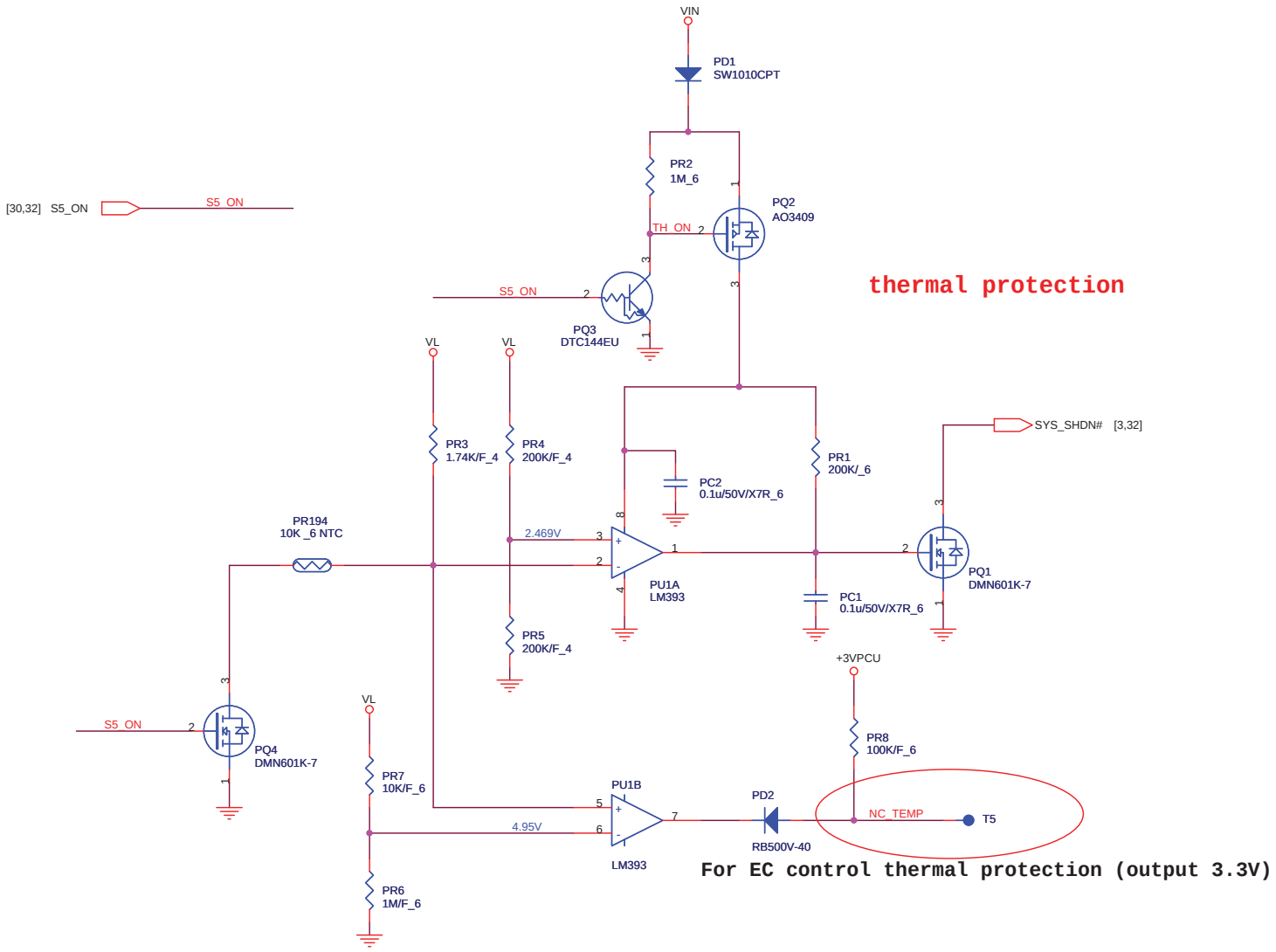




Quanta Computer Inc.
PROJECT : ZY8

Size	Document Number	Rev
	Discharge/1.5V	1A

Date: Tuesday, February 17, 2009 Sheet 37 of 39



Quanta Computer Inc.		
PROJECT : ZY8		
Size	Document Number: Thermal Protection	Rev: 1A
Date: Tuesday, February 17, 2009	Sheet 38 of 39	

CHANGE LIST

Model	REV	CHANGE LIST
ZY8 MB	1A	FIRST RELEASED: E20080?-???? (PCB: DA0ZY8MB6A0)
	2A	Page10 : Correct LVDS power of NorthBridge to +VDR_SUS Page12 : Change 32.768KHz (Y2) to normal type(H3.5) Change RTC battery connector type (CN34) to DFHD02MR311 Swap SATA port between port-1 (ODD) and port-4 (2ND HDD) Page3 :Remove Q32, Q33, R288,R287,R111 and R110 for Thermal monitor Page6 :Change PU power +3VSUS to +3V Add HDA function for ZY9 Page7 :Add HSYNC/VSYNC to GND for ZY9 MXM Page12 :Add HDA function for ZY9 Page17 :Add iHMDI function for ZY9 Change U33 power and Input Change U36 power Page19 :Add HDMI Level Shift for ZY9 Add Cap. for DP signal Change HDMI Conn footprint Page20 :Change transformer and RJ45 footprint Page21 :Change Conn pcs to Two pcs Page23 :Co-layout ALC888 for ZY9 Page25 :Change New Card Conn footprint Page26 :Change CardReader to OZ888GS0LN Page27 :Change Power Board Conn to 6 pin Change CN1 and CN13 pin define Combine LCD BL ON/OFF and Logo LED conn. to CN39 Page28 :Change USB CN32 pin define Change CN15 to 12pin Page29 :Add ESD protect for FP change PQ37 from BAM14140001 to BAM14120000 change PQ35, PQ30,PQ49 from BAM44960000 to BAM44680003 change PC131,PC93 from CH22206KB16 to CH21506K915 changePR184 from CS26193F929 to CH22743F901 PR179,PR165 mount PC112,PC109,PC120,PC101,PC147,PC156,PC91,PC29,PC35,PC135,PC160,PC159,PC141 un-mount change PU9 from AL0006111002 to AL008202001 change PU7 from AL006237000 to AL008206000 change PU3 from AL051116008 to AL008207000
	3A	
	3C	

MODEL: ZY8

FROM	To
X	1A
X	1A
1A	2A
1A	2A
1A	2A
1A	2A
1A	2A
1A	2A
1A	2A
1A	2A
1A	2A
1A	2A
1A	2A
1A	2A
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1A	2A
1A	2A
1A	2A
1A	2A
1A	2A
2A	3A
2A	3A
2A	3A
2A	3A
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3A	3B
3A	3B

Quanta Computer Inc.
PROJECT : ZY8

Size | Document Number: Change list | Rev 3B
Date: Monday, January 05, 2009 | Sheet 39 of 39

DOC NO.	PROJECT MODEL :	ZY8	APPROVED BY:		DATE:	2008/06/27
	PART NUMBER:		DRAWING BY:		REVISON:	1A