Newgate

Schematics Document

<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

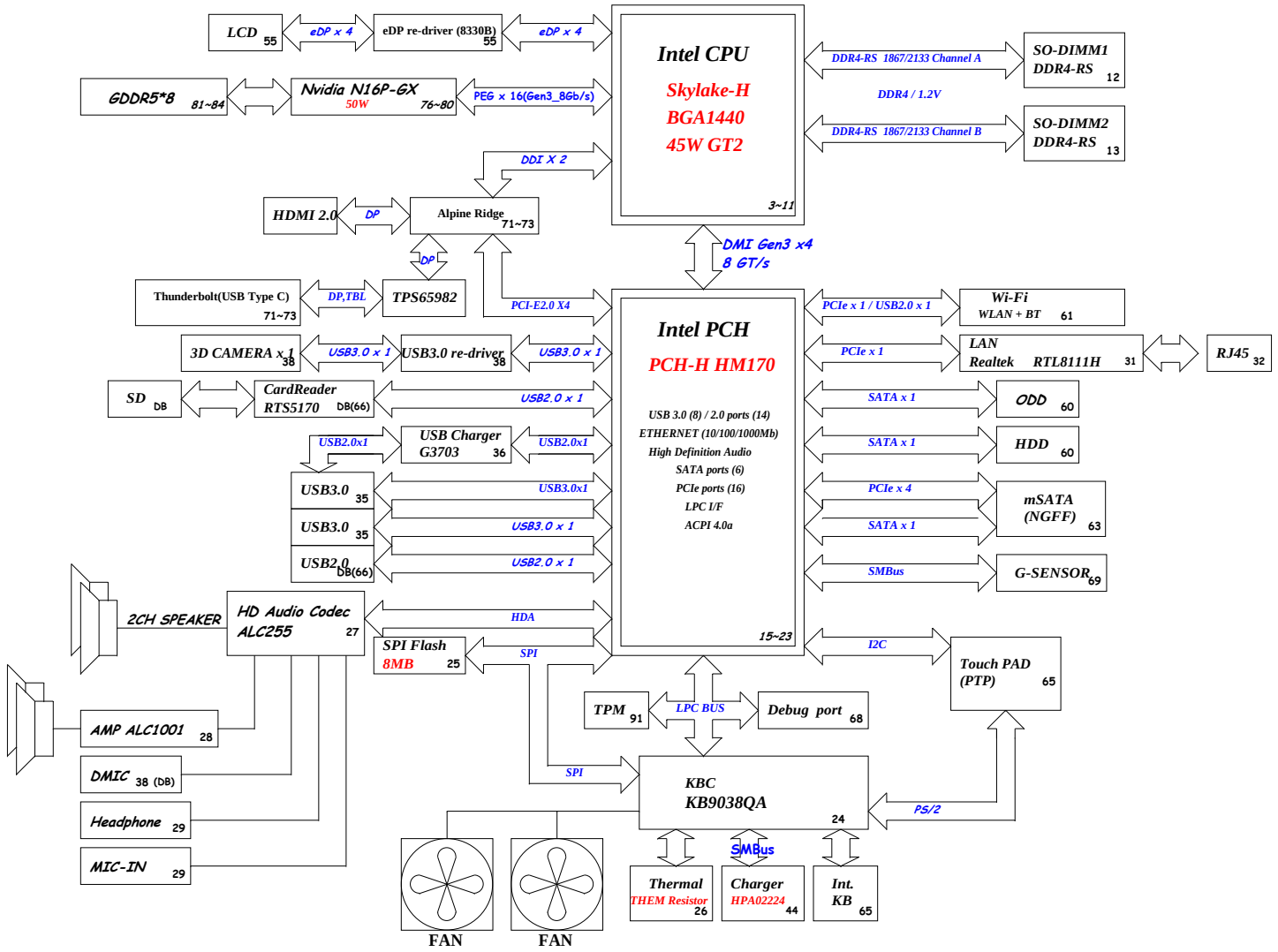
Title: ***Cover Page***

Size	Document Number	Rev
A	**Newgate**	**1M**

Date: Wednesday, August 12, 2015 Sheet 1 of 105

Newgate Board Block Diagram

Project code : 4PD06A010001
PCB P/N : 14307
Revision : 1M



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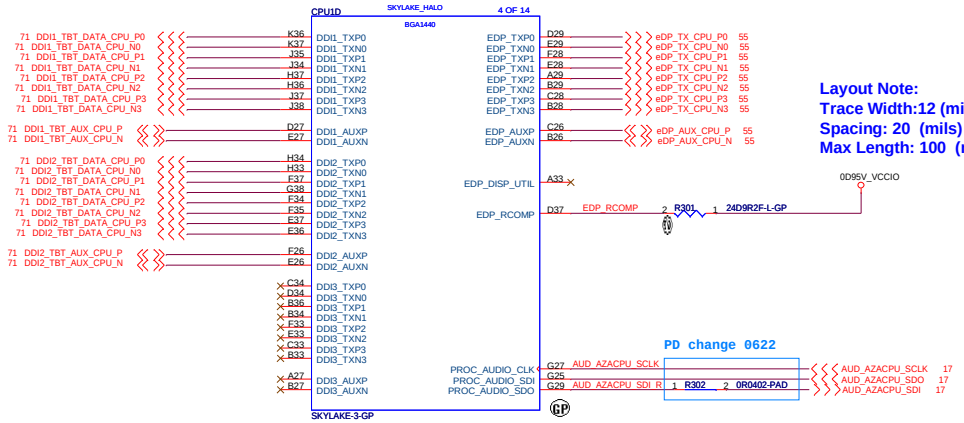
Title: Block Diagram

Size: C | Document Number: Newgate | Rev: 1M

Date: Wednesday, August 12, 2015 | Sheet 2 of 105

Royee 20150205 REVERSE PEG BUS for layout issue

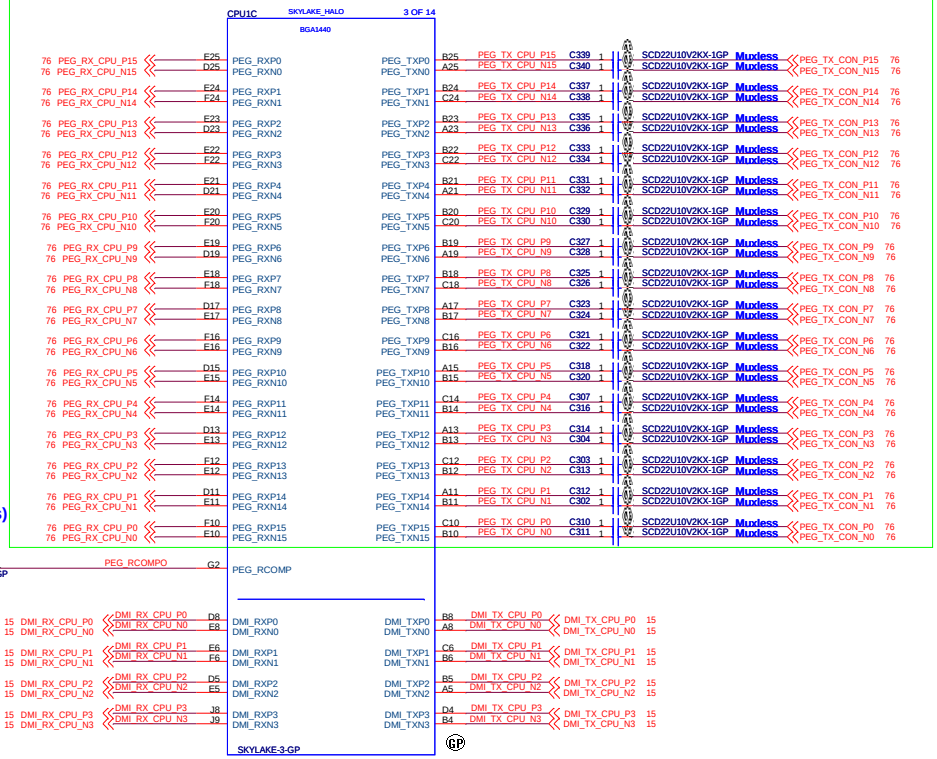
SSID = CPU



Layout Note:
Trace Width:12 (mils)
Spacing: 20 (mils)
Max Length: 100 (mils)

PD change 0622

Layout Note:
Trace Width:12 (mils)
Spacing: 15 (mils)
Max Length: 400 (mils)



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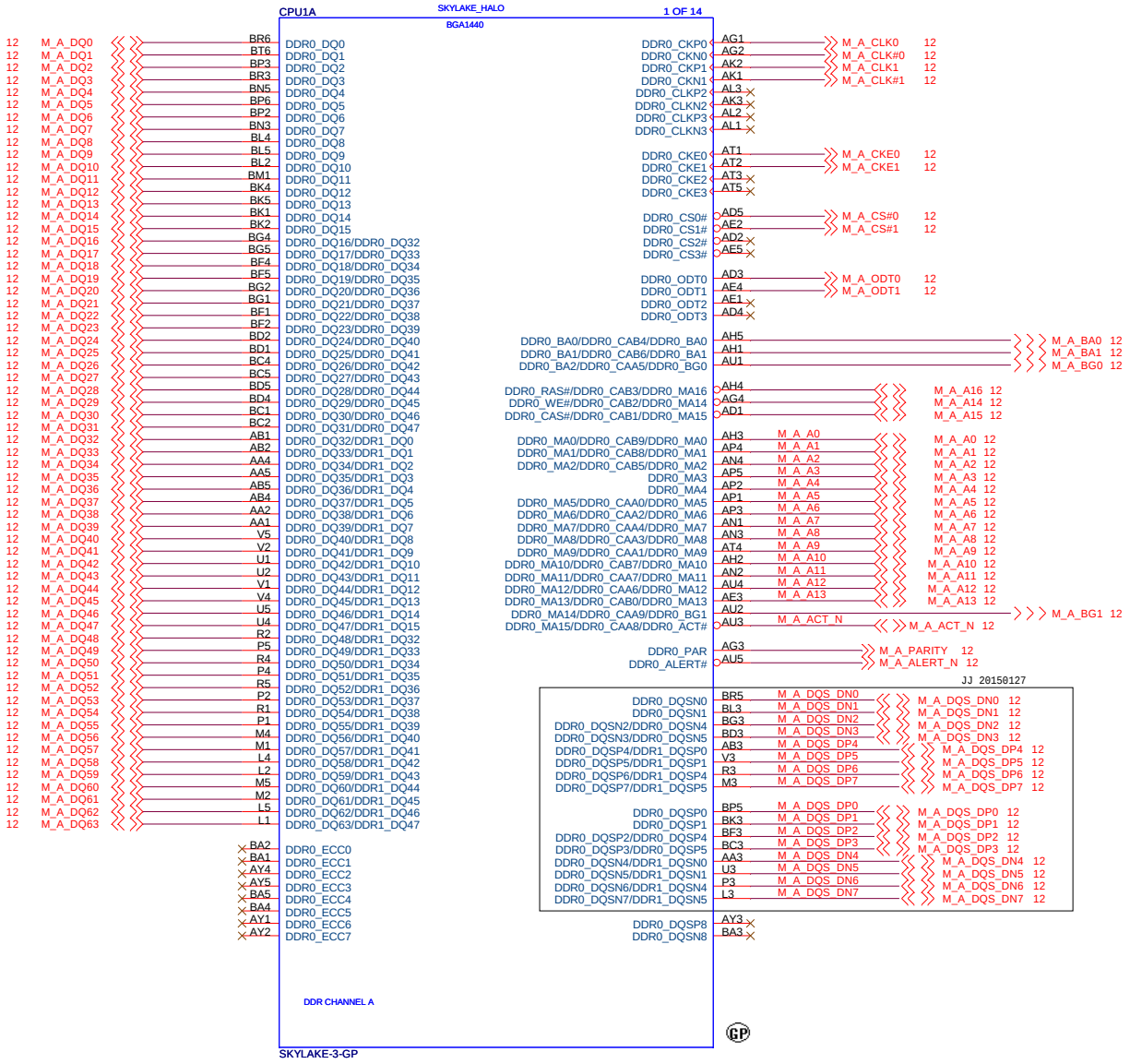
Title	**CPU (PCIE/DMI/FDI)**
Size: Custom	Document Number: **Newgate** Rev: **SA**
Date: Tuesday, August 18, 2015	Sheet 3 of 105



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Title: CPU_DDR_CHA

Size	Document Number	Rev
A3	Newgate	1M

Date: Tuesday, August 18, 2015 Sheet 4 of 105

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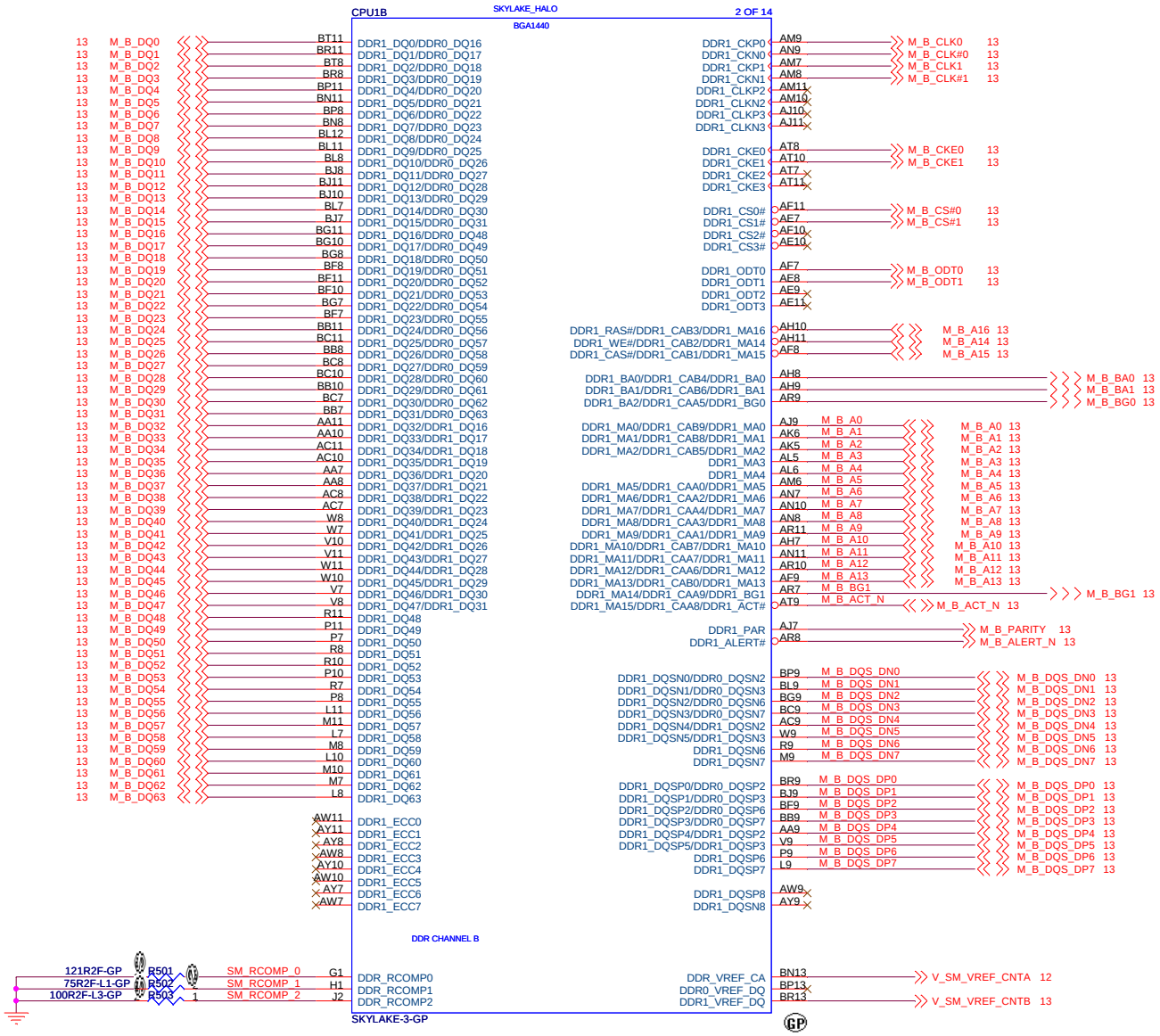

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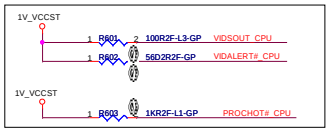
Title: CPU_DDR_CHB

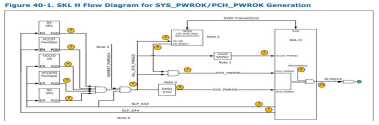
Size: A3 | Document Number: Newgate | Rev: 1M

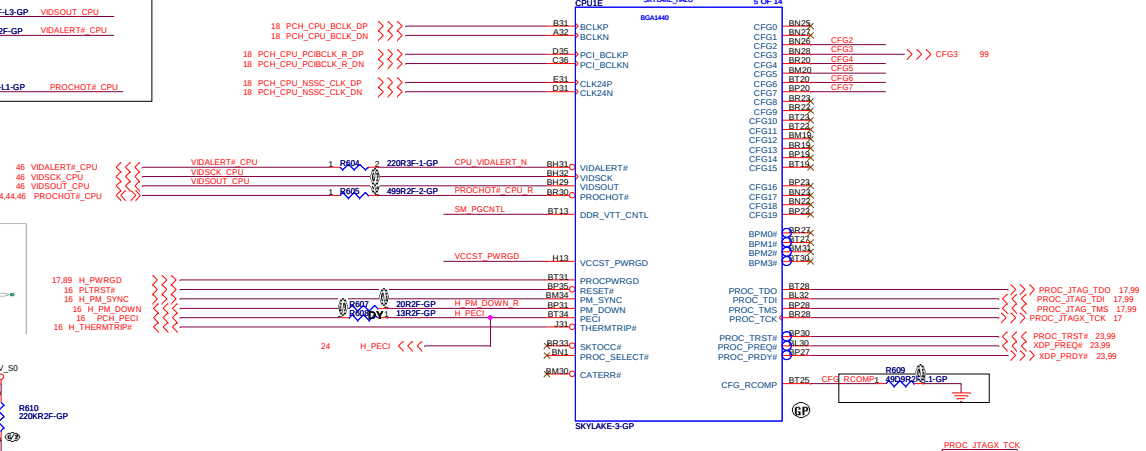
Date: Tuesday, August 18, 2015 | Sheet 5 of 105
</core_design>

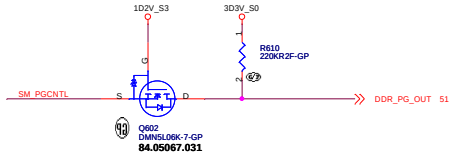
SSID = CPU

AROUND_CPU

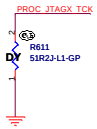


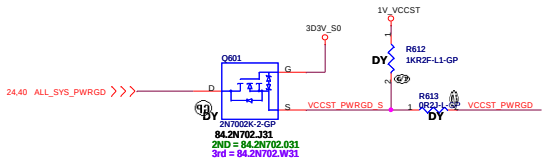






UN 0225





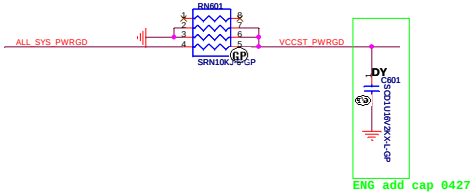


Table 6-8. Reset and Miscellaneous Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. Intel recommends placing test points on the board for CFG pins. • **CFG[0]:** Stall reset sequence after PCU PLL lock until de-asserted: – 1 = (Default) Normal Operation; No stall. – 0 = Stall. • **CFG[1]:** Reserved configuration lane. • **CFG[2]:** PCI Express* Static x16 Lane Numbering Reversal. – 1 = Normal operation – 0 = Lane numbers reversed. • **CFG[3]:** Reserved configuration lane. • **CFG[4]:** eDP enable: – 1 = Disabled. – 0 = Enabled. • **CFG[6:5]:** PCI Express* Bifurcation – 00 = 1 x8, 2 x4 PCI Express* – 01 = reserved – 10 = 2 x8 PCI Express* – 11 = 1 x16 PCI Express* • **CFG[7]:** PEG Training: – 1 = (default) PEG Train immediately following RESET# de assertion. – 0 = PEG Wait for BIOS for training. • **CFG[19:8]:** Reserved configuration lanes.	I/O	GTL	SE	All processor lines. CFG[2], CFG[6:5] and CFG[7] are relevant for H and S-processor line only and test point may be placed on the board for them.

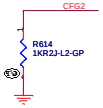
Processor Internal Pull-Up / Pull-Down Terminations

Processor Internal Pull-Up / Pull-Down Terminations

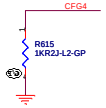
Signal Name	Pull Up/Pull Down	Rail	Value
BPM[3:0]	Pull Up	V_{CCIO}	16-60 Ω
PREQ#	Pull Up	V_{CCST}	3 kΩ
PROC_TDI	Pull Up	V_{CCSTG}[1]	3 kΩ
PROC_TMS	Pull Up	V_{CCSGT}[1]	3 kΩ
CFG[19:0]	Pull Up	V_{CCIO}	3 kΩ

Note:
1. For SKL-S it should be V_{CCST}

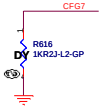
PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



eDP Enable	
CFG4	1:Disable 0:Enable



PEG Training	
CFG7	1:(default) PEG Train immediately following RESET# de assertion 0 = PEG Wait for BIOS for training.



PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

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Title: **CPU_CFG_CFG STRAP**

Size: A2 | Document Number: **Newgate** | Rev: **1M**

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1V_CPU_CORE
CPU1G
SKYLAKE_HALO
7 OF 14
BGA1440
AA13 AA31 AA32 AA33 AA34 AA35 AA36 AA37 AA38 AB29 AB30 AB31 AB32 AB35 AB36 AB37 AB38 AC13 AC14 AC29 AC30 AC31 AC32 AC33 AC34 AC35 AC36 AD13 AD14 AD31 AD32 AD33 AD34 AD35 AD36 AD37 AD38 AE13 AE14 AE30 AE31 AE32 AE35 AE36 AE37 AE38 AF35 AF36 AF37 AF38 K13 K14 L13 N13 N14 N30 N31 N32 N35 N36 N37 N38 P13
VCC
V32 V33 V34 V35 V36 V37 V38 W13 W14 W29 W30 W31 W32 W35 W36 W37 W38 Y29 Y30 Y31 Y32 Y33 Y34 Y35 Y36 L14 P29 P30 P31 P32 P33 P34 P35 P36 R13 R31 R32 R33 R34 R35 R36 R37 R38 T29 T30 T31 T32 T35 T36 T37 T38 U29 U30 U31 U32 U33 U34 U35 U36 V13 V14 V31 P14
SKYLAKE-3-GP
1V_CPU_CORE
VCC_SENSE
VSS_SENSE
AG37
AG38
VCCCORE_SENSE 46
VSSCORE_SENSE 46
JJ 20150130
CPU1J
SKYLAKE_HALO
10 OF 14
BGA1440
BJ17 BJ19 BJ20 BK17 BK19 BK20 BL16 BL17 BL18 BL19 BL20 BL21 BM17 BN17
VCCOPC
BJ23 BJ26 BJ27 BK23 BK26 BK27 BL23 BL24 BL25 BL26 BL27 BL28 BM24
RSVD#BJ23 RSVD#BJ26 RSVD#BJ27 RSVD#BK23 RSVD#BK26 RSVD#BK27 RSVD#BL23 RSVD#BL24 RSVD#BL25 RSVD#BL26 RSVD#BL27 RSVD#BL28 RSVD#BM24
BL15 BM16
VCCOPC_SENSE VSSOPC_SENSE
BL22 BM22
RSVD#BL22 RSVD#BM22
BP15 BR15 BT15
VCCEOPIO
BP16 BR16 BT16
RSVD#BP16 RSVD#BR16 RSVD#BT16
BN15 BM15
VCCEOPIO_SENSE VSSEOPIO_SENSE
BP17 BN16
RSVD#BP17 RSVD#BN16
BM14 BL14
VCC_OPC_1P8
BJ35 BJ36
RSVD#BJ35 RSVD#BJ36
AT13 AW13
ZVM# MSM#
AU13 AY13
ZVM2# MSM2#
BT29 BR25 BP25
OPC_RCOMP OPCE_RCOMP OPCE_RCOMP2
SKYLAKE-3-GP
<Core Design>
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Title
CPU_POWER1 (ASIC Power Bolck)
Size
Custom
Document Number
Newgate
Rev
1M
Date: Tuesday, August 18, 2015
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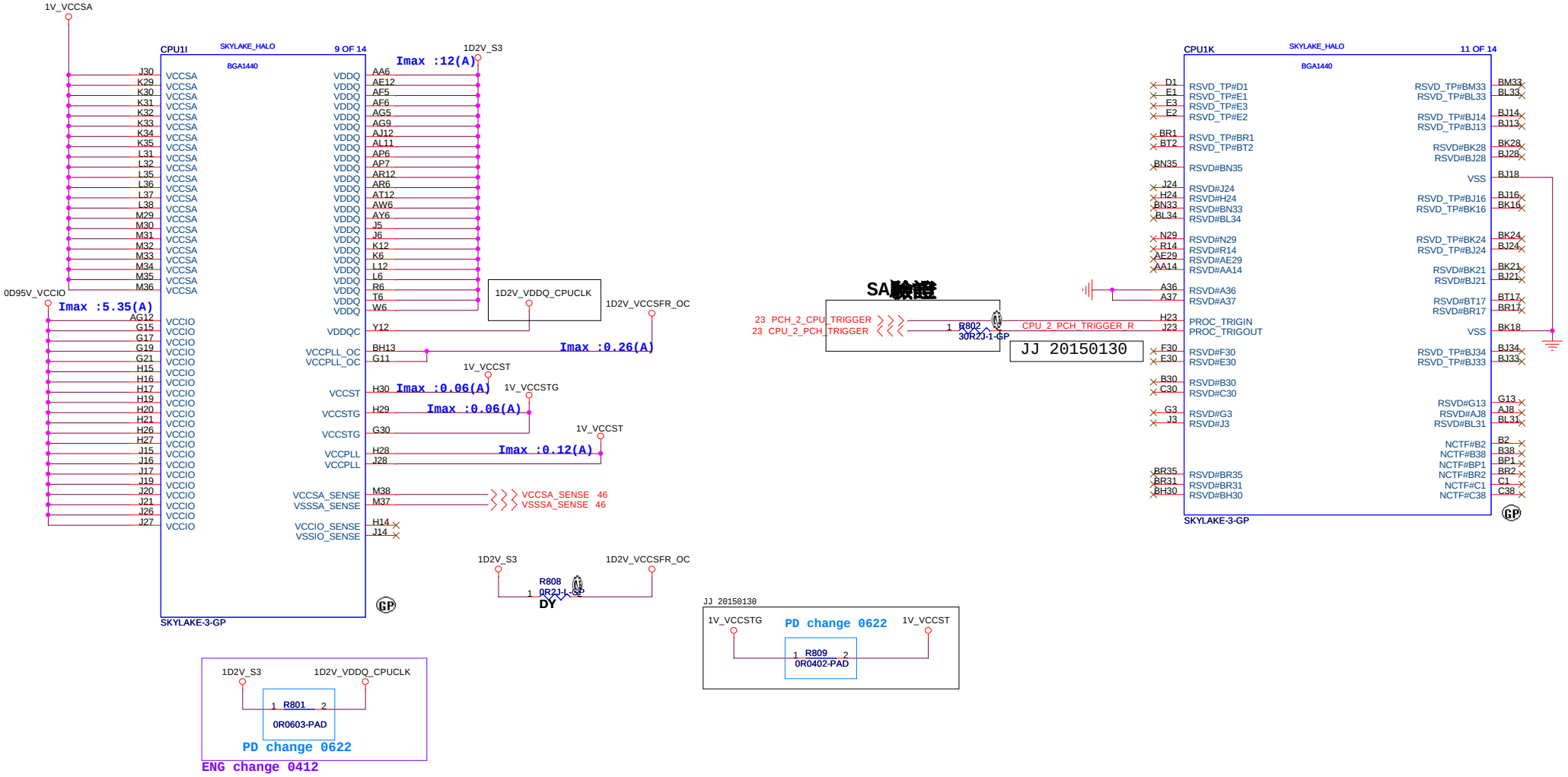
SSID = CPU



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Title: CPU_POWER2(ASIC Power Bolck)

Size: A3 | Document Number: Newgate | Rev: 1M

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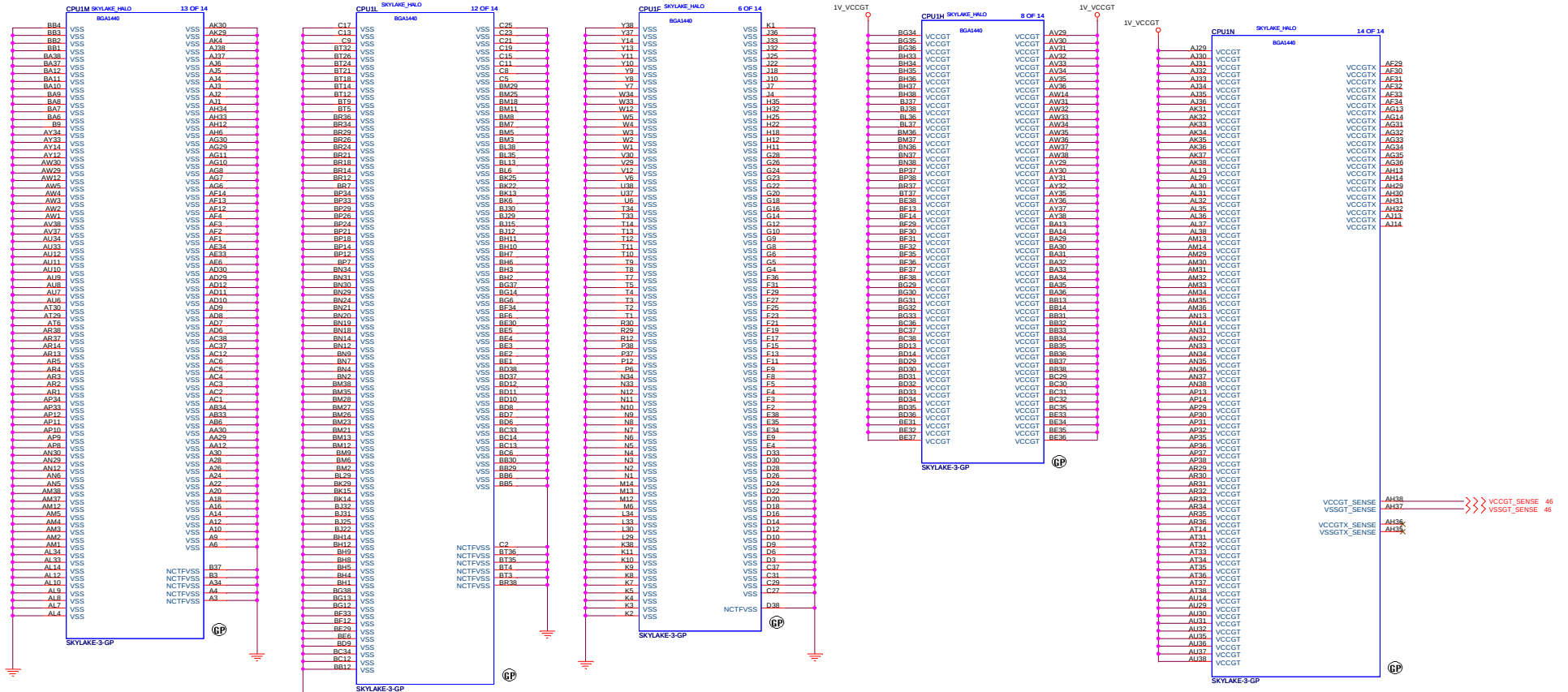
SSID = CPU



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Title: **CPU_POWER3(ASIC Power Bolck)**

Size: A2 | Document Number: **Newgate** | Rev: **1M**

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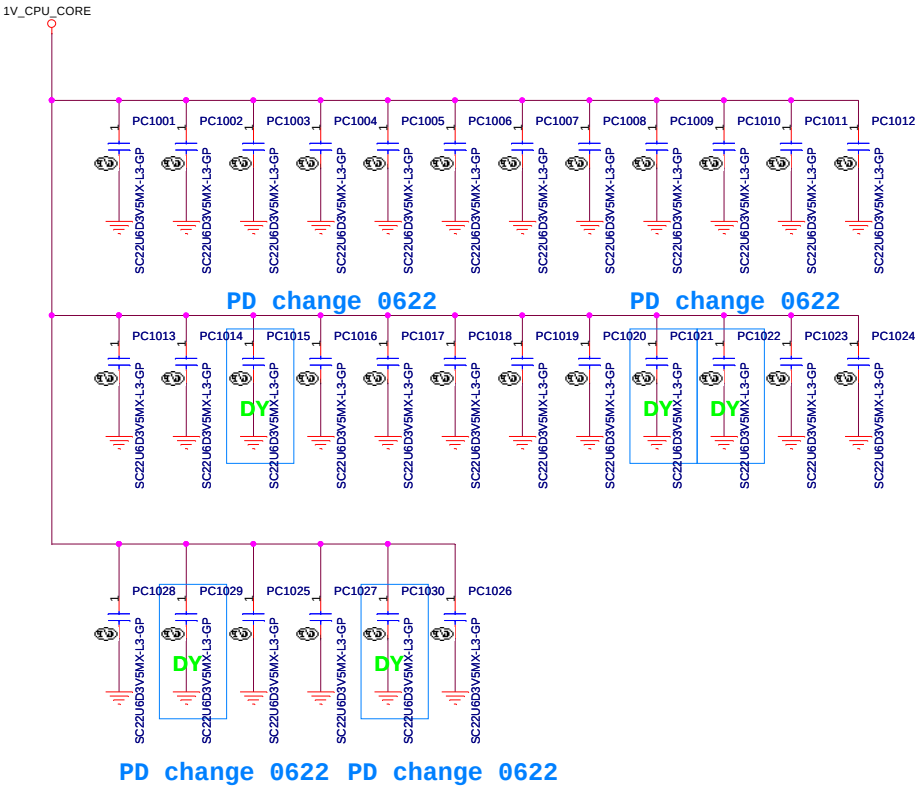
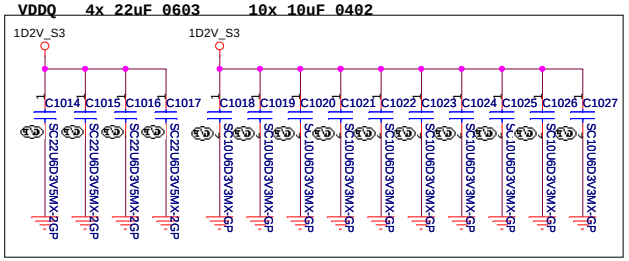
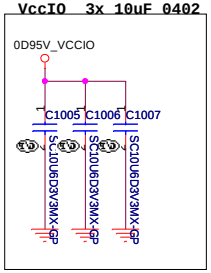
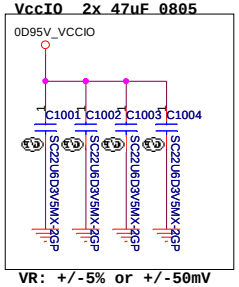
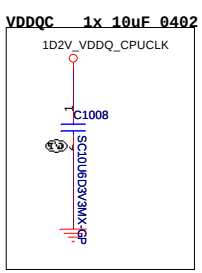
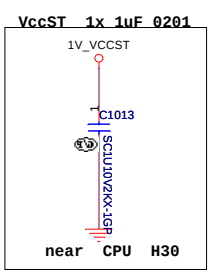




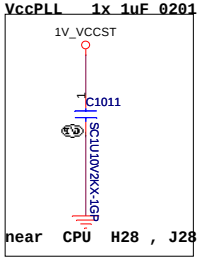


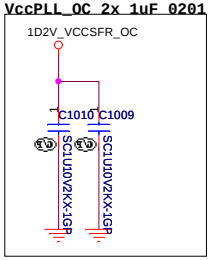


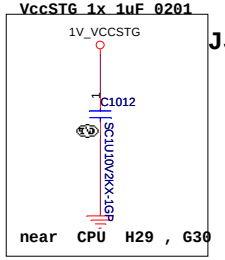




VR: +/-5% or +/-50mV
Place close to VR output







JJ 20150130

Decoupling Requirements for SKL H Processor (Sheet 2 of 2)

Domain	Board Edge cap	Backside cap	Notes
$V_{CC_{GT}}$	6x 47uF 0805		
		8x 22uF 0603	
		35x 10uF 0402	
		68x 1uF 0201	
$V_{CC_{GTx}}$	8x 22uF 0603		
		4x 10uF 0402	
		12x 1uF 0201	
$V_{CC_{SA}}$	1x 47uF 0805		
		1x 47uF 0805	
		7x 10uF 0402	
		3x 1uF 0201	
V_{DDQ}		4x 22uF 0603	Share supply with DRAM
		10x 10uF 0402	
V_{DDQC}		1x 10uF 0402	
$V_{CC_{IO}}$	2x 47uF 0805		VR: +/-5% or +/-50mV Place close to VR output
		3x 10uF 0402	
$V_{CC_{ST}}$		1x 1uF 0201	
$V_{CC_{STG}}$		1x 1uF 0201	Share supply with 1.0V PCH rail
$V_{CC_{PLL}}$		1x 1uF 0201	
$V_{CC_{PLL\_OC}}$		2x 1uF 0201	Supply from 1.2V V_{DDQ}
$V_{CC_{OPC}}$		10x 10uF 0402	VR: +/-5% or +/-50mV
$V_{CC_{EOPIO}}$		3x 10uF 0402	VR: +/-5% or +/-50mV

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Title: 010_CPU (Power CAP1)

Size: A3 | Document Number: Newgate | Rev: 1M

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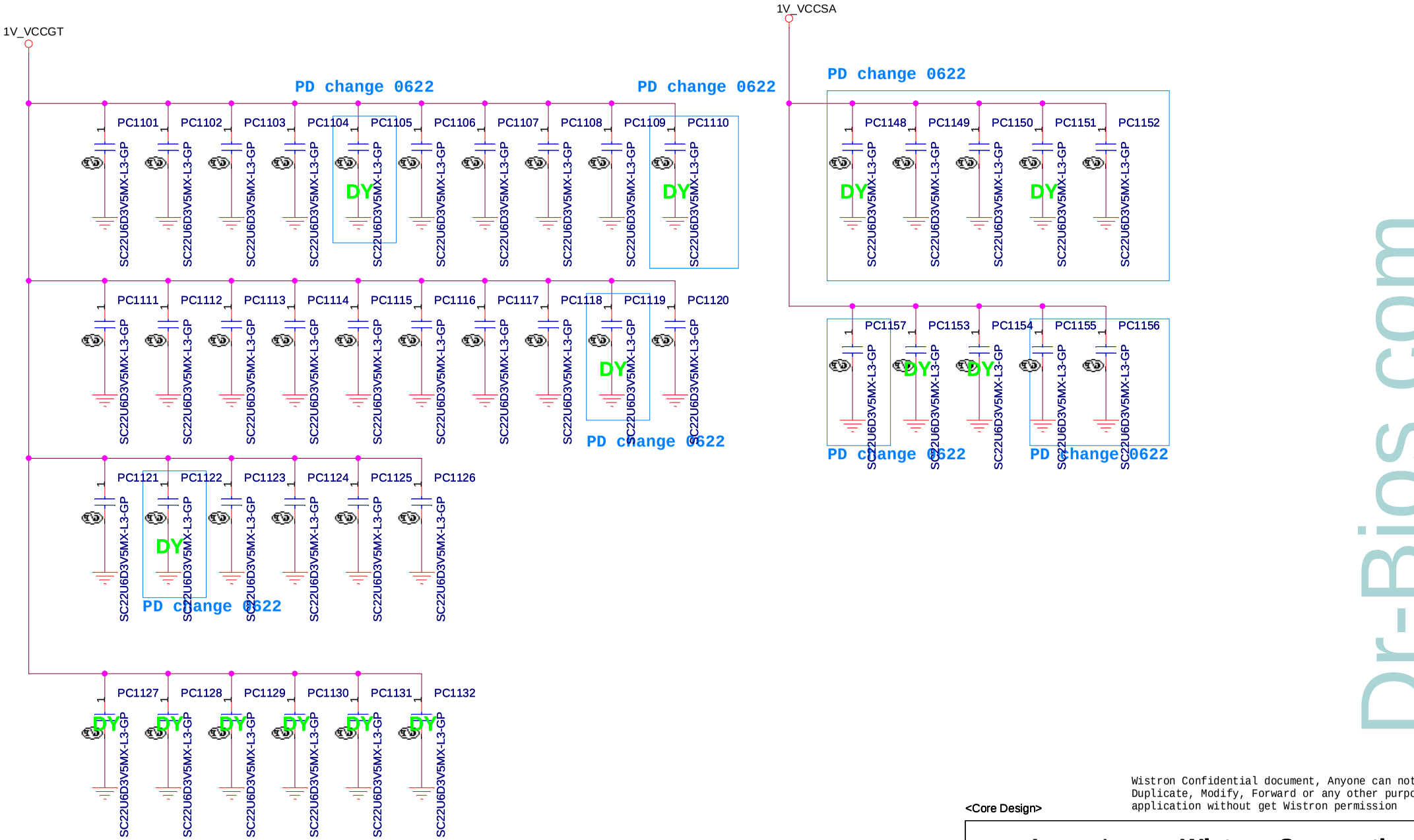

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Title: CPU (Power CAP2)

Size: A4 | Document Number: Newgate | Rev: 1M

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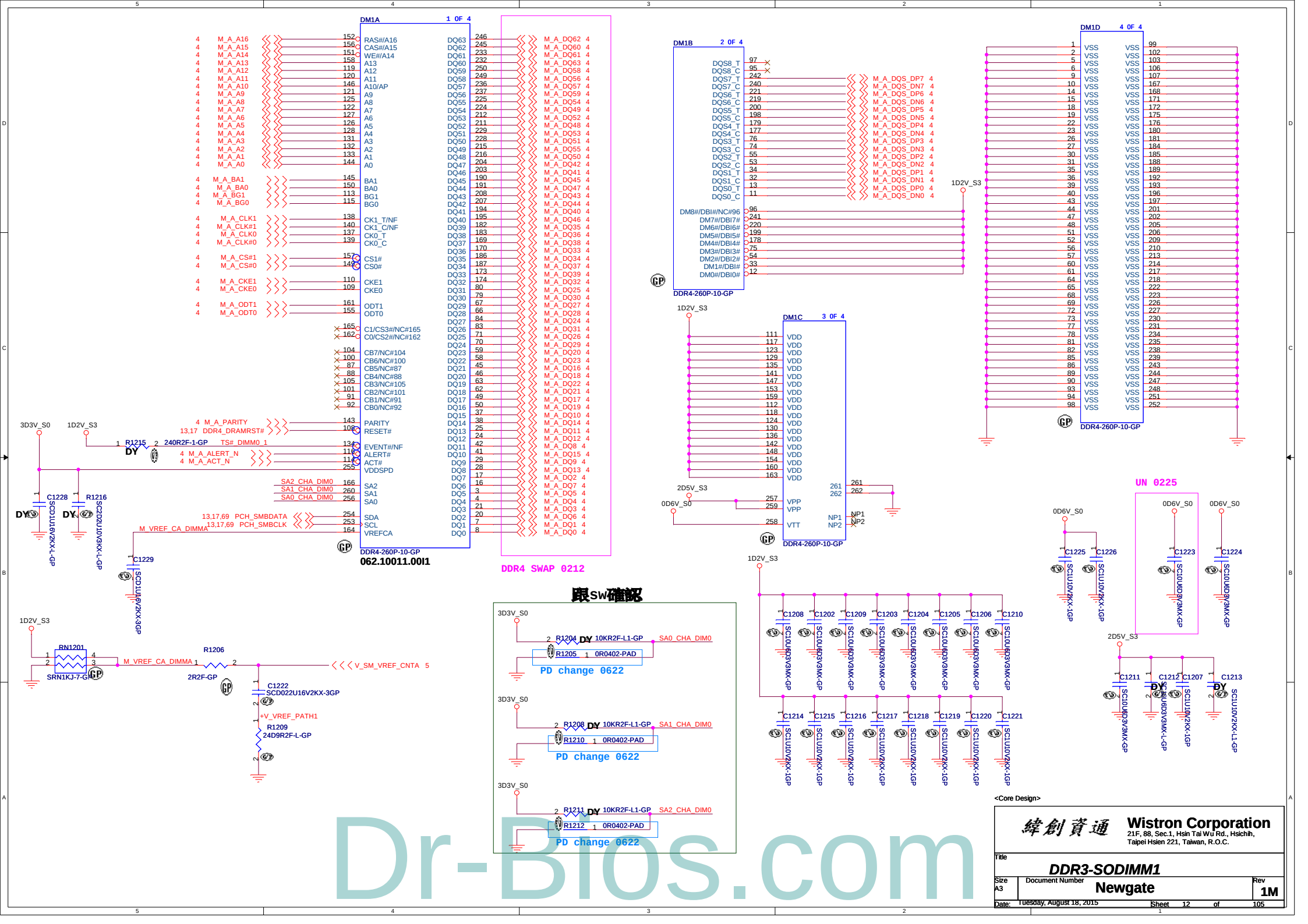
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1 OF 4
DDR4-260P-10-GP
062.10011.00I1
DDR4 SWAP 0212
DM1B
2 OF 4
DDR4-260P-10-GP
DM1C
3 OF 4
DDR4-260P-10-GP
DM1D
4 OF 4
DDR4-260P-10-GP
UN 0225
跟SW確認
PD change 0622
PD change 0622
PD change 0622
R1215 240R2F-1-GP
RN1201 SRN1KJ-7-GP
R1206 2R2F-GP
R1209 24D9R2F-L-GP
R1204 10KR2F-L1-GP
R1205 0R0402-PAD
R1208 10KR2F-L1-GP
R1210 0R0402-PAD
R1211 10KR2F-L1-GP
R1212 0R0402-PAD
<Core Design>
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Title
DDR3-SODIMM1
Size A3
Document Number Newgate
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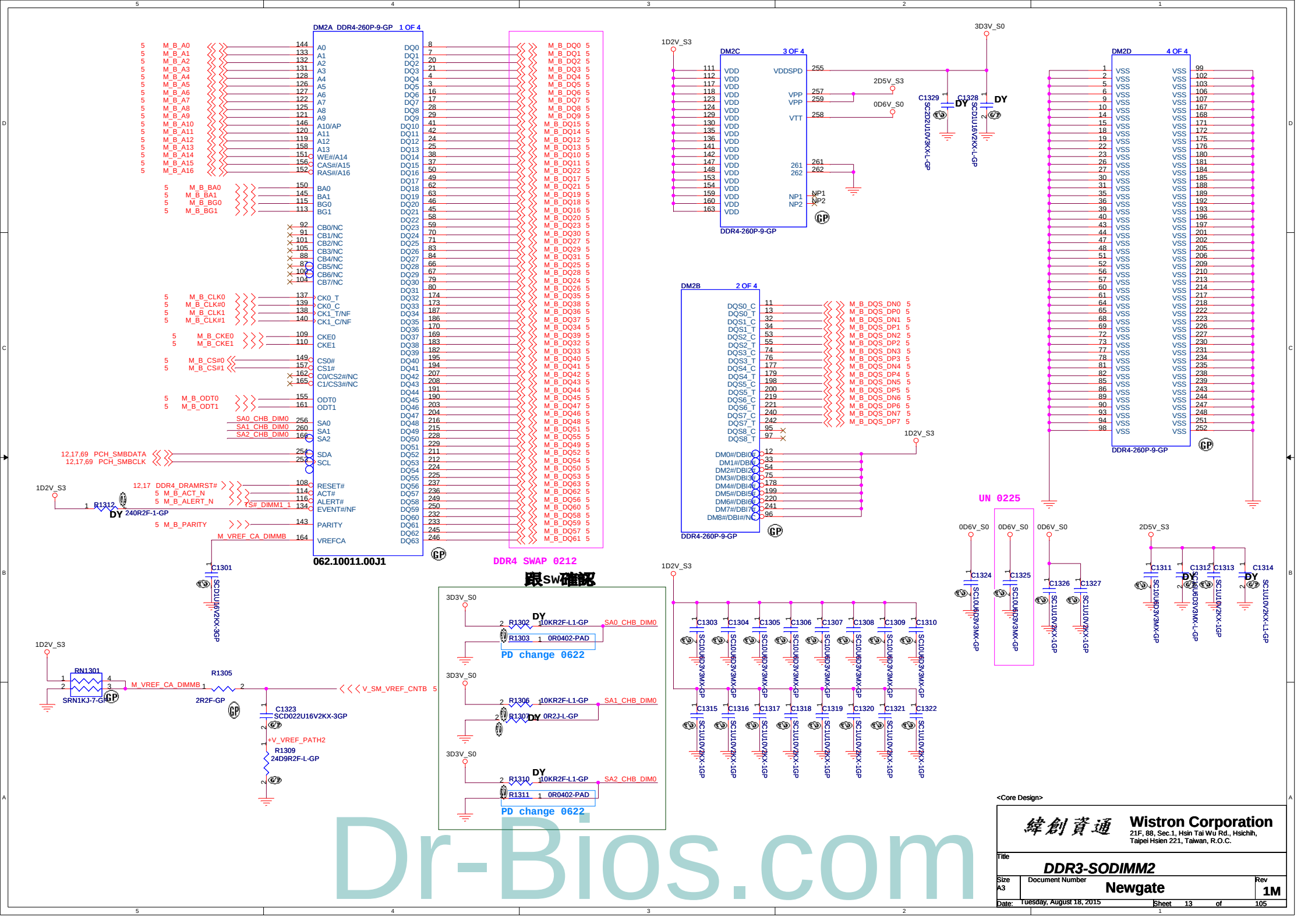

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Title: DDR3-SODIMM2
Size: A3
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Royee 20150204

PCH1A 1 OF 12

SPL PCH-H

22 SPI_SI_CPU
22 SPI_SO_CPU

Royee 20150204
PD change 0622

24,25 SPI_SI_ROM
24,25 SPI_SO_ROM
R1401 1 2 0R0402-PAD SPI_SI_CPU
R1402 1 2 0R0402-PAD SPI_SO_CPU

24,25 SPI_CS_CPU_N0
24,25 SPI_CLK_ROM
R1403 1 2 15R2F-2-GP SPI_CLK_CPU

22,25 SPI_IO2_ROM
22,25 SPI_IO3_ROM
R1404 1 2 0R0402-PAD SPI_IO2_CPU
R1405 1 2 0R0402-PAD SPI_IO3_CPU

Royee 20150204
PD change 0622

BD17 GPP_A11/PME#
AG15 RSVD_AG15
AG14 RSVD_AG14
AF17 RSVD_AF17
AE17 RSVD_AE17
AR19 TP5
AN17 TP4

Strap
BB29 SPI0_MOSI
BE30 SPI0_MISO
BD31 SPI0_CS0#
BC31 SPI0_CLK
AW31 SPI0_CS1#

Strap
BC29 SPI0_IO2
BD30 SPI0_IO3
AT31 SPI0_CS2#

Strap
AN36 GPP_D1/SPI1_CLK
AL39 GPP_D0/SPI1_CS#
AN41 GPP_D3/SPI1_MOSI
AN38 GPP_D2/SPI1_MISO
AH43 GPP_D22/SPI1_IO3
AG44 GPP_D21/SPI1_IO2

BB27 GPP_B13/PLTRST# → PLT_RST# 24,31,61,63,68,71,89,91

P43 GPP_G16/GSXCLK
R39 GPP_G12/GSXDOUT
R36 GPP_G13/GSXSLOAD
R42 GPP_G14/GSXDIN
R41 GPP_G15/GSXSRESET#

TBT_FORCE_PWR 71
TBT_PLUG_EVENT# 71

0217

change 0227

AF41 GPP_E3/CPU_GP0 → EC_SMI# 24
AE44 GPP_E7/CPU_GP1
BC23 GPP_B3/CPU_GP2 → TP_IN# 65
BD24 GPP_B4/CPU_GP3 → DGPU_HOLD_RST# 76,79

BC36 GPP_H18/SML4ALERT#
BE34 GPP_H17/SML4DATA
BD39 GPP_H16/SML4CLK
BB36 GPP_H15/SML3ALERT#
BA35 GPP_H14/SML3DATA
BC35 GPP_H13/SML3CLK
BD35 GPP_H12/SML2ALERT#
AW35 GPP_H11/SML2DATA
BD34 GPP_H10/SML2CLK

BE11 INTRUDER# → SM_INTRUDER#

SUNRISE-1-GP

R1408 10KR2F-L1-GP
2 1 DGPU_HOLD_RST#

delete 0225

3D3V_RTC_AUX
SM_INTRUDER# R1406 1MR2F-L1-GP

3D3V_S0
TP_IN# R1407 10KR2F-L1-GP
DY

change 0227

CHECK NEED PULL HIGH?
3D3V_S0
EC_SMI# R1409 10KR2F-L1-GP

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH_GPP1
Size: A4
Document Number: Newgate
Rev: 1M
Date: Tuesday, August 18, 2015
Sheet 14 of 105

SSID = PCH

PCH1B

2 OF 12

SUNRISE-1-GP

SPL PCH-H

DMI

USB 2.0

PCIe/USB 3

3 DMI_TX_CPU_N0 L27
3 DMI_TX_CPU_P0 N27
3 DMI_RX_CPU_N0 C27
3 DMI_RX_CPU_P0 B27
3 DMI_TX_CPU_N1 E24
3 DMI_TX_CPU_P1 G24
3 DMI_RX_CPU_N1 B28
3 DMI_RX_CPU_P1 A28
3 DMI_TX_CPU_N2 G27
3 DMI_RX_CPU_N2 E26
3 DMI_TX_CPU_P2 B29
3 DMI_RX_CPU_P2 C29
3 DMI_TX_CPU_N3 L29
3 DMI_RX_CPU_N3 K29
3 DMI_TX_CPU_P3 B30
3 DMI_RX_CPU_P3 A30

DMI_RXN0 DMI_RXP0 DMI_TXN0 DMI_TXP0 DMI_RXN1 DMI_RXP1 DMI_TXN1 DMI_TXP1 DMI_RXN2 DMI_RXP2 DMI_TXN2 DMI_TXP2 DMI_RXN3 DMI_RXP3 DMI_TXN3 DMI_TXP3

PEG_RCOMPN_CPU B18
PEG_RCOMPP_CPU C17
R1504 100R2F-L3-GP

PCIE_RCOMPN PCIE_RCOMPP

PCIE1_RXN/USB3_7_RXN H15
PCIE1_RXP/USB3_7_RXP G15
PCIE1_TXN/USB3_7_TXN A16
PCIE1_TXP/USB3_7_TXP B16
PCIE2_TXN/USB3_8_TXN B19
PCIE2_TXP/USB3_8_TXP C19
PCIE2_RXN/USB3_8_RXN E17
PCIE2_RXP/USB3_8_RXP G17
PCIE3_RXN/USB3_9_RXN L17
PCIE3_RXP/USB3_9_RXP K17
PCIE3_TXN/USB3_9_TXN B20
PCIE3_TXP/USB3_9_TXP C20
PCIE4_RXN/USB3_10_RXN E20
PCIE4_RXP/USB3_10_RXP G19
PCIE4_TXN/USB3_10_TXN B21
PCIE4_TXP/USB3_10_TXP A21
PCIE5_RXN K19
PCIE5_RXP L19
PCIE5_TXN D22
PCIE5_TXP C22
PCIE6_RXN G22
PCIE6_RXP E22
PCIE6_TXN B22
PCIE6_TXP A23
PCIE7_RXN L22
PCIE7_RXP K22
PCIE7_TXN C23
PCIE7_TXP B23
PCIE8_RXN K24
PCIE8_RXP L24
PCIE8_TXN C24
PCIE8_TXP B24

USB2N_1 AF5
USB2P_1 AG7
USB2N_2 AD5
USB2P_2 AD7
USB2N_3 AG8
USB2P_3 AG10
USB2N_4 AE1
USB2P_4 AE2
USB2N_5 AC2
USB2P_5 AC3
USB2N_6 AF2
USB2P_6 AF3
USB2N_7 AB3
USB2P_7 AB2
USB2N_8 AL8
USB2P_8 AL7
USB2N_9 AA1
USB2P_9 AA2
USB2N_10 AJ8
USB2P_10 AJ7
USB2N_11 W2
USB2P_11 W3
USB2N_12 AD3
USB2P_12 AD2
USB2N_13 V2
USB2P_13 V1
USB2N_14 AJ11
USB2P_14 AJ13

USB_PCH_PN1 36
USB_PCH_PP1 36
USB_PCH_PN2 35
USB_PCH_PP2 35
USB3.0 Port 1 USB Charger
USB3.0 Port 2(USB2.0)

Port change 0224

USB_PCH_PN6 66
USB_PCH_PP6 66
USB_PCH_PN7 61,89
USB_PCH_PP7 61,89
USB2.0 (DB)
Bluetooth

USB_PCH_PN9 38
USB_PCH_PP9 38
USB_PCH_PN10 66
USB_PCH_PP10 66
CCD
Card reader

3D3V_S5

R1510 10KR2F-L1-GP

GPP_E9/USB2_OC0# AD43 USB2_OC
GPP_E10/USB2_OC1# AD42
GPP_E11/USB2_OC2# AD39
GPP_E12/USB2_OC3# AC44
GPP_F15/USB2_OCB_4 Y43
GPP_F16/USB2_OCB_5 Y41
GPP_F17/USB2_OCB_6 W44
GPP_F18/USB2_OCB_7 W43

R1509 113R2F-GP

USB2_COMP AG3 USBCOMP
USB2_VBUSSENSE AD10 USB2_VBUSSENSE
RSVD_AB13 AB13
USB2_ID AG2 USB2_ID

GPD7/RSVD BD14

JJ 2015/01/27

RN1501 SRN1KJ-7-GP

USB2_VBUSSENSE 1 4
USB2_ID 2 3

Delete WIGIG 0204

WIGIG
WIFI
LAN

61,89 PCIE_RX_PCH_N3
61,89 PCIE_RX_PCH_P3
61 PCIE_TX_PCH_N3
61 PCIE_TX_PCH_P3
31 PCIE_RX_PCH_N4
31 PCIE_RX_PCH_P4
31 PCIE_TX_PCH_N4
31 PCIE_TX_PCH_P4
71 PCIE_RX_PCH_N5
71 PCIE_RX_PCH_P5

JJ 20150129

71 PCIE_TX_CON_N5 C1503 1 TBT SCD22U10V1KX-GP PCIE_TX_PCH_N5
71 PCIE_TX_CON_P5 C1504 1 TBT SCD22U10V1KX-GP PCIE_TX_PCH_P5

71 PCIE_RX_PCH_N6
71 PCIE_RX_PCH_P6
71 PCIE_TX_CON_N6 C1505 1 TBT SCD22U10V1KX-GP PCIE_TX_PCH_N6
71 PCIE_TX_CON_P6 C1506 1 TBT SCD22U10V1KX-GP PCIE_TX_PCH_P6

71 PCIE_RX_PCH_N7
71 PCIE_RX_PCH_P7
71 PCIE_TX_CON_N7 C1509 1 TBT SCD22U10V1KX-GP PCIE_TX_PCH_N7
71 PCIE_TX_CON_P7 C1510 1 TBT SCD22U10V1KX-GP PCIE_TX_PCH_P7

71 PCIE_RX_PCH_N8
71 PCIE_RX_PCH_P8
71 PCIE_TX_CON_N8 C1507 1 TBT SCD22U10V1KX-GP PCIE_TX_PCH_N8
71 PCIE_TX_CON_P8 C1508 1 TBT SCD22U10V1KX-GP PCIE_TX_PCH_P8

Alpine-Ridge

ENG change 0416

USB Table

Pair	Device
1	USB3.0 Port 1(USB2.0) Charger
2	USB3.0 Port 2(USB2.0)
3	
4	
5	USB2.0
6	
7	Bluetooth
8	Touch Screen
9	CCD
10	Card reader
11	Finger Printer
12	
13	
14	

<Core Design>

緯創資通 Wistron Corporation
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Title: PCH_PCIE_DMI_USB

Size: A3 | Document Number: Newgate | Rev: 1M

Date: Tuesday, August 18, 2015 | Sheet 15 of 105

SSID = PCH

Delete WIGIG 0204

change 0227

change 0227

UN 0225

PCH1C

3 OF 12

SPL PCH-H

CLINK

FAN

PCIe/SATA

HOST

SUNRISE-1-GP

MSATA

MSATA

MSATA

HDD

ODD

eDP

<Core Design>

AROUND PCH

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	PCH_PCIE_SATA
Size A4	Document Number Newgate
Rev	1M
Date: Tuesday, August 18, 2015	Sheet 16 of 105

SSID = PCH

RTC Reset

change 0226 SWAP 0303

DM1 & 2

G-SENSOR

EC & GPU

PD change 0622

JJ 20150127

JJ 20150130

ENG change 0417

ENG SUS_CLK_CPU delete 0421

delete 0225

For AFR

UN 0225

SUNRISE-1-GP

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH_HDA_GPP1_JTAG

Size: A2 | Document Number: Newgate | Rev: 1M

Date: Tuesday, August 18, 2015 | Sheet 17 of 105

SSID = PCH

MP change 0807
(not change net name)

PCH1F 6 OF 12

SUNRISE-1-GP

GPIO REVIEW CHECK

delete 0227

GPIO REVIEW CHECK

DEVSLP_PCH 63

ENG change 0416

TPM

POWER modify 0223 SWAP 0303

DY

CHECK WITH SW(VGA)

ENG change 0417

PCH1G 7 OF 12

SUNRISE-1-GP

PEG CLOCK CHECK WITH SW

CHECK P and N

Delete WIGIG 0204

ENG 0412 change

<Core Design>

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Title: PCH_USB3_CLOCK

Size: A3 | Document Number: Newgate | Rev: 1M

Date: Tuesday, August 18, 2015 | Sheet 18 of 105

SSID = PCH

PCH1E 5 OF 12 SPL PCH-H SUNRISE-1-GP

Delete 0225

71 DDI1_TBT_HPD_CPU
71 DDI2_TBT_HPD_CPU
AW4 GPP_I0/DDPB_HPD0
AV2 GPP_I1/DDPC_HPD1
AV4 GPP_I2/DDPD_HPD2
BA4 GPP_I3/DDPE_HPD3
Strap GPP_I7/DDPC_CTRLCLK
GPP_I8/DDPC_CTRLDATA
Strap GPP_I5/DDPB_CTRLCLK
GPP_I6/DDPB_CTRLDATA
Strap GPP_I9/DDPD_CTRLCLK
GPP_I10/DDPD_CTRLDATA
BB8 BD6 BA5 BC4 BE5 BE6
DDI2_TBT_DATA_CPU 22
DDI1_TBT_CLK_CPU 71
DDI1_TBT_DATA_CPU 71
DDPD_DATA_CPU 22
55 eDP_HPD_CPU
BD7 GPP_I4/EDP_HPD
GPP_F14 Y44
GPP_F23 V44
GPP_F22 W39
GPP_G23 L43
GPP_G22 L44
GPP_G21 U35
GPP_G20 R35
GPP_H23 BD36

R1904 10KR2F-L1-GP
DGPU_PWR_EN#

JJ 20150127
PSW_CLR#
Pass Word Clear
G1901
GAP-OPEN

3D3V_S5
RN1904 SRN10KJ-5-GP
RTC_DET#
GPU_EVENT#

JJ 20150130
3D3V_S0
PSW_CLR#
R1906 10KR2F-L1-GP

3D3V_S0
RN1901 SRN2K2J-5-GP
I2C1_CLK_CPU
I2C1_DATA_CPU
Royee 20150202

PCH1K 11 OF 12 SPL PCH-H SUNRISE-1-GP

22 GPP_B22/GSPI1_MOSI
86 DGPU_PWR_EN#
PSW_CLR#
25 RTC_DET#
AT29 GPP_B22/GSPI1_MOSI
AR29 GPP_B21/GSPI1_MISO
AV29 GPP_B20/GSPI1_CLK
BC27 GPP_B19/GSPI1_CS#
Strap

22 GPP_B18/GSPI0_MOSI
79 GPU_EVENT#
38 CCD_PWR_EN
BD28 GPP_B18/GSPI0_MOSI
BD27 GPP_B17/GSPI0_MISO
AW27 GPP_B16/GSPI0_CLK
AR24 GPP_B15/GSPI0_CS#
Strap

ENG change 0412

AV44 GPP_C9/UART0_TXD
BA41 GPP_C8/UART0_RXD
AU44 GPP_C11/UART0_CTS#
AV43 GPP_C10/UART0_RTS#

ENG change 0427

AU41 GPP_C15/UART1_CTS#/ISH_UART1_CTS#
AT44 GPP_C14/UART1_RTS#/ISH_UART1_RTS#
AT43 GPP_C13/UART1_TXD/ISH_UART1_TXD
AU43 GPP_C12/UART1_RXD/ISH_UART1_RXD

LPSS_UART2_CTS# AN43 GPP_C23/UART2_CTS#
LPSS_UART2_RTS# AN44 GPP_C22/UART2_RTS#
LPSS_UART2_TXD AR39 GPP_C21/UART2_TXD
LPSS_UART2_RXD AR45 GPP_C20/UART2_RXD

TOUCH PAD
65 I2C1_CLK_CPU
65 I2C1_DATA_CPU
AR41 GPP_C19/I2C1_SCL
AR44 GPP_C18/I2C1_SDA
AR38 GPP_C17/I2C0_SCL
AT42 GPP_C16/I2C0_SDA

JJ 20150130
AM44 GPP_D4/ISH_I2C2_SDA
AJ44 GPP_D23/ISH_I2C2_SCL

GPP_D9 AL44
GPP_D10 AL36
GPP_D11 AL35
GPP_D12 AJ39

CHECK NEED PULL HIGH?
LAB 測試腳

GPP_D16/ISH_UART0_CTS# AJ43
GPP_D15/ISH_UART0_RTS# AL43
GPP_D14/ISH_UART0_TXD AK44
GPP_D13/ISH_UART0_RXD AK45

JJ 20150130

GPP_H20/ISH_I2C0_SCL BC38
GPP_H19/ISH_I2C0_SDA BB38
GPP_H22/ISH_I2C1_SCL BD38
GPP_H21/ISH_I2C1_SDA BE39

GPP_A23/ISH_GP5 BC22
GPP_A22/ISH_GP4 BD18
GPP_A21/ISH_GP3 BE21
GPP_A20/ISH_GP2 BD22
GPP_A19/ISH_GP1 BD21
GPP_A18/ISH_GP0 BB22
GPP_A17/ISH_GP7 BC19
TBT_PRESENT# GSENSOR_INT# 69

ENG change 0412

3D3V_S5
R1908 10KR2J-3-GP DY
TBT_PRESENT#
R1907 10KR2J-3-GP TBT
ENG change 0412

TBT_PRESENT#	HIGH	LOW
	NON TBT	WITH TBT

3D3V_S0
R1903 49K9R2F-L-GP DEBUG LPSS_UART2_CTS#
R1909 49K9R2F-L-GP DEBUG LPSS_UART2_RTS#
R1910 49K9R2F-L-GP DEBUG LPSS_UART2_TXD
R1911 49K9R2F-L-GP DEBUG LPSS_UART2_RXD

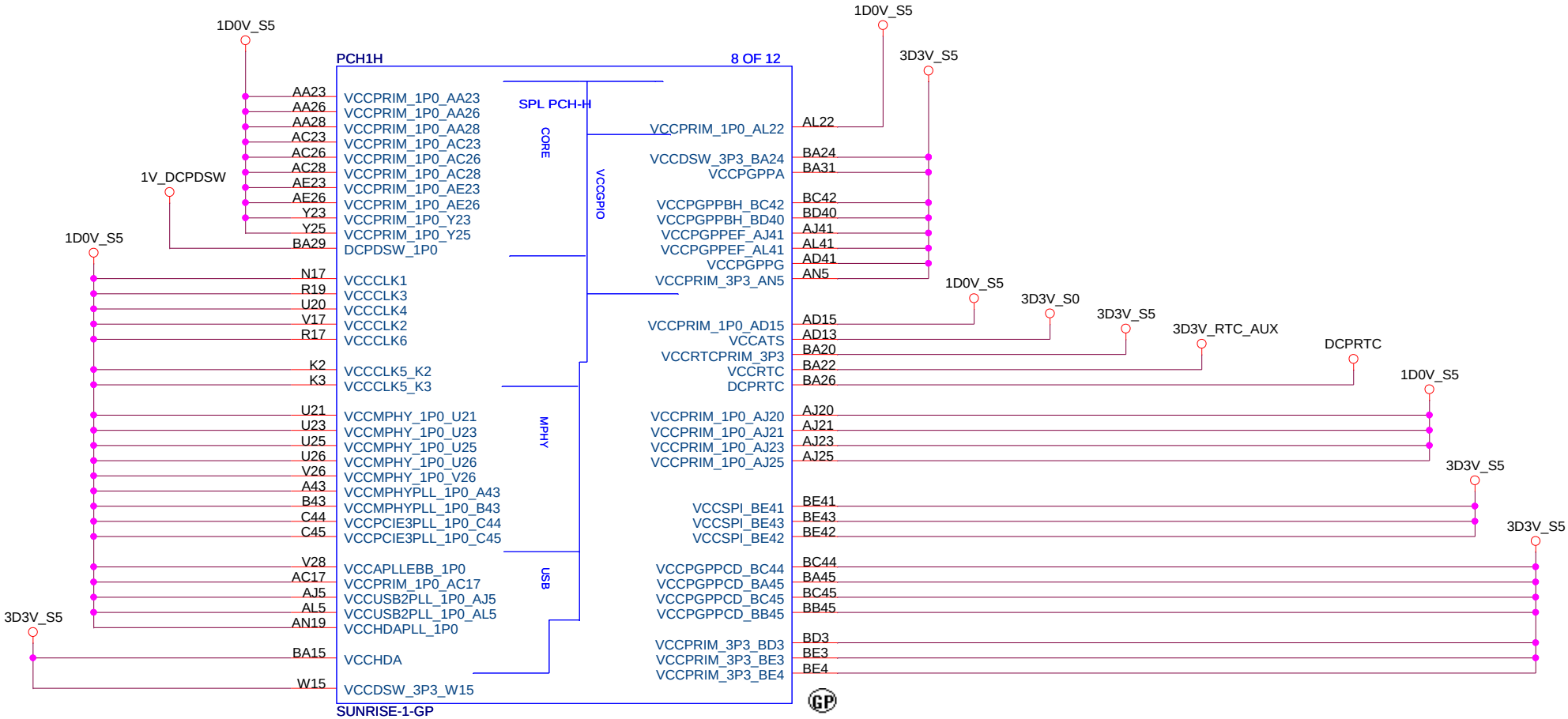
5V_S5
DEBUG2 DEBUG
LPSS_UART2_TXD
LPSS_UART2_RXD
20.F1897.004
ACES-CON4-37-GP
ENG change property 0505

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH_GPP2_GPP3
Size: A3 Document Number: Newgate Rev: 1M
Date: Tuesday, August 18, 2015 Sheet 19 of 105

SSID = PCH



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

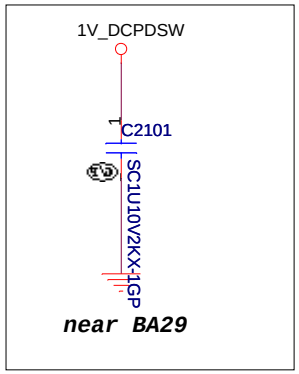
Title: PCH_POWER_VCCPRIM_VCCMPHY

Size	Document Number	Rev
A4	Newgate	1M

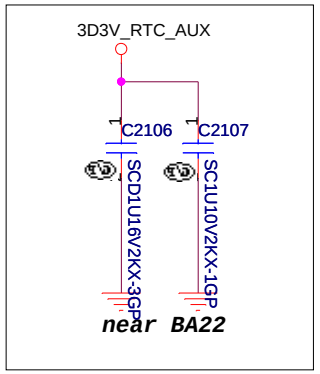
Date: Wednesday, August 12, 2015 Sheet 20 of 105

SSID = PCH

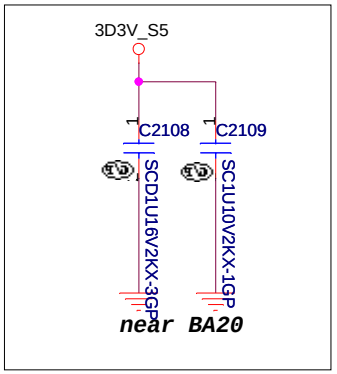
DcpDSW
1x 1uF



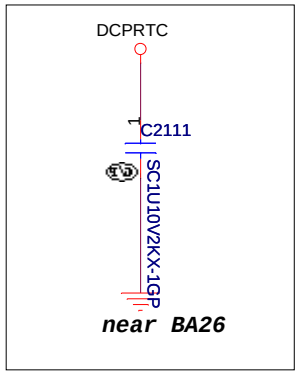
VccRTC
1x1 uF 1x0.1 uF



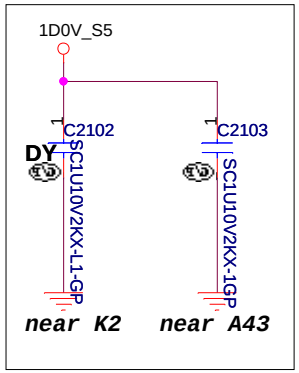
VccRTCPRIM
1x1 uF 1x0.1 uF



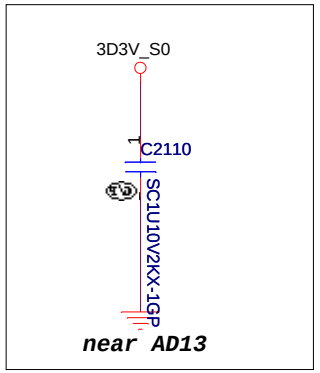
DcpRTC
1x 0.1uF



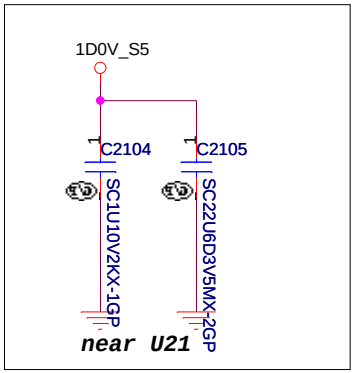
VccMPHYPLL / VccPCIE3PLL
1x1 uF



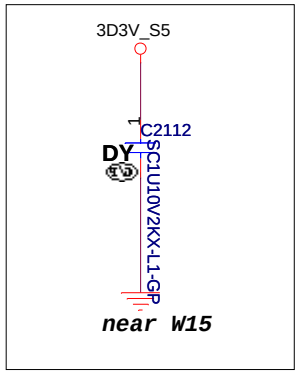
VccATS
1x1 uF



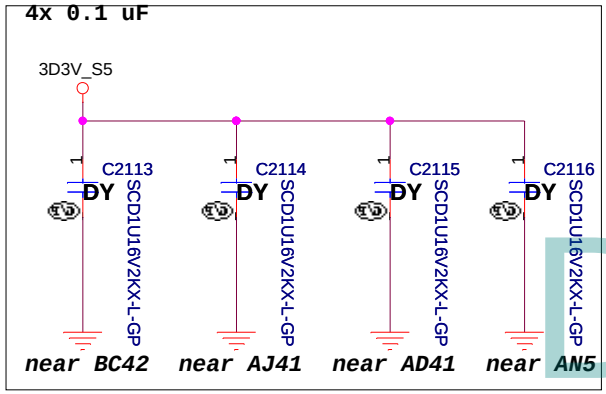
VccMPHY / VccPRIM / VccAPLLEBB
1x1 uF 1x22 uF



VccDSW
1x 1uF



VccPGPPBCH / VccPGPPEF / VccPGPPG
/ VccPRIM
4x 0.1 uF



Decoupling and Power Connection Requirements for SKL S/H PCH (DT / AIO) (Sheet 1 of 2)

Voltage Supply	Area	PCH Pins sharing power rail	Value	Size	Quantity	Placement type (R)umney / (E)dge	Place capacitor(s) near ball(s)
V1.0A	VccMPHY VccPRIM VccAPLLEBB	U21, U23, U25, U26, V26, AC17, V28	1 uF	0402	1	E (<3 mm)	U21
			22 uF	0805	1	E (<5 mm)	
	VccMPHYPLL VccPCIE3PLL	A43, B43, C44, C45	1 uF	0402	1	E (<5 mm)	A43
	VccCLK5	K2, K3	1 uF	0402	1	E (<5 mm)	K2 (Note 1)
	VccCLK (1,2,3,4,6)	N17, R19, U20, V17, R17	-	-	-	-	-
	VccUSB2PLL VccHDAPLL	AJ5, AL5, AN19	-	-	-	-	-
	VccPRIM	AL22	-	-	-	-	-
	VccPRIM	AD15	-	-	-	-	-
	VccPRIM	AJ20, AJ21, AJ23, AJ25	-	-	-	-	-
	VccPRIM	AA23, AA26, AA28, AC23, AC26, AC28, AE23, AE26, Y23, Y25	-	-	-	-	-
V1.0DSW	DcpDSW	BA29	1 uF	0402	1	E (<5 mm)	BA29
V1.8A/ V3.3A	VccPGPPBCH	BC42, BD40	0.1 uF	0402	1	E (<3 mm)	BC42 (Note 1)
	VccPGPPEF	AJ41, AL41	0.1 uF	0402	1	E (<3 mm)	AJ41 (Note 1)
	VccPGPPG	AD41	0.1 uF	0402	1	E (<3 mm)	AD41 (Note 1)
	VccPRIM	AN5	0.1 uF	0402	1	E (<3 mm)	AN5 (Note 1)
	VccPGPPA	BA31	-	-	-	-	-
	VccSPI	BE41, BE42, BE43	-	-	-	-	-
	VccPGPPD	BC44, BA45, BC45, BB45	-	-	-	-	-
V1.8A/ V1.85/ V3.3S	VccATS	AD13	1 uF	0402	1	E (<5 mm)	AD13
V1.5A/ V1.8A/ V3.3A	VccHDA	BA15	-	-	-	-	-
V3.3A	VccRTCPRIM	BA20	1 uF	0402	1	E (<5 mm)	BA20
			0.1 uF	0402	1	E (<3 mm)	
	VccPRIM	BD3, BE3, BE4	-	-	-	-	-
V3.3RTC	VccRTC	BA22	1 uF	0402	1	E (<5 mm)	BA22
			0.1 uF	0402	1	E (<3 mm)	
V3.3DSW	VccDSW	W15	1 uF	0401	1	E (<3 mm)	W15 (Note 1)
	VccDSW	BA24	-	-	-	-	-
PCH Internal VRM	DcpRTC	BA26	0.1 uF	0402	1	E (<5 mm)	BA26

<Core Design>

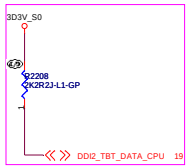
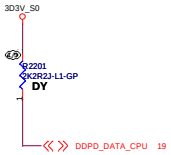
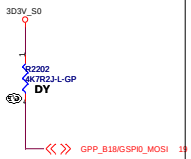
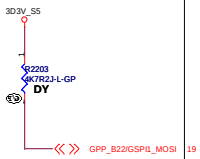
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

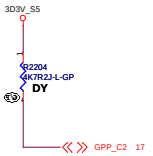
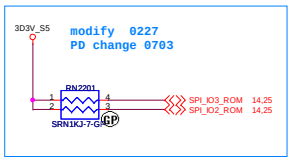
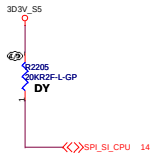
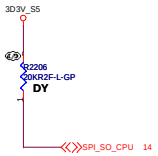
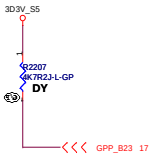
Title: PCH_POWER_CAP1

Size: A4 | Document Number: Newgate | Rev: 1M

Date: Wednesday, August 12, 2015 | Sheet 21 of 105

SSID = PCH

Description	Display Port B Detected	Display Port C Detected	Display Port D Detected	No reboot	Boot BIOS strap bit BBS	Flash descriptor security override	ESPI FLASH SHARING MODE
GPIO	GPP_I6	GPP_I8	GPP_I10	GPP_B18	GPP_B22	HDA_SDO	GPP_H12
Schematic	Pull up at p.71 RN7101	change 0225 					
High	Detected	Detected	Detected	Enable	LPC	Disable	1:SLAVE ATTACEHD FLASH SHARING ESPI FLASH SHARING MODE
Low	Not Detected	Not Detected	Not Detected	Disable	SPI	Enable	0: MASTER ATTACHED FLASH SHARING
	internal pull-down	internal pull-down	internal pull-down	internal pull-down	internal pull-down	internal pull-down	internal pull-down

Description	Top Swap Override	eSPI or LPC	TLS Confi-dentiality	Reserved	Reserved	Reserved	Reserved	Reserved
GPIO	GPP_B14	GPP_C5	GPP_C2	SPI0_IO3	SPI0_IO2	SPI0_MOSI	SPI0_MISO	GPP_B23
Schematic								
High	Enable	eSPI	Enable					
Low	Disable	LPC	Disable					
	internal pull-down	internal pull-down	internal pull-down	internal pull-up	internal pull-up	internal pull-up	internal pull-up	internal pull-down

<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH_STRAP

Size: A2 | Document Number: Newgate | Rev: 1M

Date: Tuesday, August 18, 2015 | Sheet 22 of 105

SSID = PCH

PCH1I 9 OF 12

SPL PCH-H

AC18	VSS	VSS	AR5
AN4	VSS	VSS	AR7
AN10	VSS	VSS	U15
BE14	VSS	VSS	AL4
BE18	VSS	VSS	AE29
BE23	VSS	VSS	AE4
BE28	VSS	VSS	AE42
BE32	VSS	VSS	AF18
BE37	VSS	VSS	AF20
BE40	VSS	VSS	AF21
BE9	VSS	VSS	AF23
C10	VSS	VSS	AF25
C2	VSS	VSS	AF26
C28	VSS	VSS	AF28
C37	VSS	VSS	AF29
J7	VSS	VSS	AG11
K10	VSS	VSS	AG13
K27	VSS	VSS	AG31
K33	VSS	VSS	AG32
K36	VSS	VSS	AG33
K4	VSS	VSS	AG38
K42	VSS	VSS	AG4
K43	VSS	VSS	AH1
L12	VSS	VSS	AH17
L13	VSS	VSS	AH18
L15	VSS	VSS	AH20
L4	VSS	VSS	AH21
L41	VSS	VSS	AH23
L8	VSS	VSS	AH25
M35	VSS	VSS	AH26
M42	VSS	VSS	AH28
N10	VSS	VSS	AH29
N15	VSS	VSS	AH45
N19	VSS	VSS	AJ10
N22	VSS	VSS	AJ14
N24	VSS	VSS	AJ15
N35	VSS	VSS	AJ17
N36	VSS	VSS	AJ18
N4	VSS	VSS	AJ26
N41	VSS	VSS	AJ28
N5	VSS	VSS	AJ29
P17	VSS	VSS	AJ31
P19	VSS	VSS	AJ32
P22	VSS	VSS	AJ36
P45	VSS	VSS	AK4
R10	VSS	VSS	AK42
R14	VSS	VSS	AU7
R22	VSS	VSS	AV17
R29	VSS	VSS	AV24
R33	VSS	VSS	AV27
R38	VSS	VSS	AV31
R5	VSS	VSS	AV33
T1	VSS	VSS	AV6
T2	VSS	VSS	AW13
T4	VSS	VSS	AW19
Y18	VSS	VSS	AW29
Y20	VSS	VSS	AW37
Y21	VSS	VSS	AW9
Y26	VSS	VSS	AY38
Y28	VSS	VSS	AY45
Y29	VSS	VSS	B25
A18	VSS	VSS	B3
A25	VSS	VSS	B37
A32	VSS	VSS	B40
A37	VSS	VSS	B6
AA17	VSS	VSS	BA1
AA18	VSS	VSS	BB11
AA20	VSS	VSS	BB16
AA21	VSS	VSS	BB21
AA25	VSS	VSS	BB25
AA29	VSS	VSS	BB30
AA4	VSS	VSS	BB34
AA42	VSS	VSS	BC2
AB10	VSS	VSS	BD43

SUNRISE-1-GP

PCH1L 12 OF 12

SPL PCH-H

C42	VSS	VSS	AB11
D10	VSS	VSS	AB7
D12	VSS	VSS	AB14
D15	VSS	VSS	AB31
D16	VSS	VSS	AB32
D17	VSS	VSS	AB38
D19	VSS	VSS	AB4
D21	VSS	VSS	AB5
D24	VSS	VSS	AC1
D25	VSS	VSS	AC20
D27	VSS	VSS	AC21
D29	VSS	VSS	AC25
D30	VSS	VSS	AC29
D31	VSS	VSS	AC45
D33	VSS	VSS	AB8
D35	VSS	VSS	AD11
D36	VSS	VSS	AD14
E13	VSS	VSS	AB15
E15	VSS	VSS	AD32
E31	VSS	VSS	AD33
E33	VSS	VSS	AD36
F44	VSS	VSS	AD4
F8	VSS	VSS	AD8
G42	VSS	VSS	AE18
G9	VSS	VSS	AE20
H17	VSS	VSS	AE21
H19	VSS	VSS	AE25
H22	VSS	VSS	AE28
H24	VSS	VSS	AL10
H27	VSS	VSS	AL11
H29	VSS	VSS	AL13
H3	VSS	VSS	AL17
H35	VSS	VSS	AL19
J10	VSS	VSS	AL24
J11	VSS	VSS	AL29
J3	VSS	VSS	AL32
J39	VSS	VSS	AL33
J5	VSS	VSS	AL38
T42	VSS	VSS	AM15
U10	VSS	VSS	AM17
U11	VSS	VSS	AM19
U14	VSS	VSS	AM22
U17	VSS	VSS	AM24
U18	VSS	VSS	AM27
U28	VSS	VSS	AM29
U29	VSS	VSS	AM45
U31	VSS	VSS	AN11
U32	VSS	VSS	AN22
U33	VSS	VSS	AN27
U38	VSS	VSS	AN31
U4	VSS	VSS	AN39
U8	VSS	VSS	AN7
V18	VSS	VSS	AN8
V20	VSS	VSS	AP11
V21	VSS	VSS	AP4
V23	VSS	VSS	AR33
V25	VSS	VSS	AR34
V29	VSS	VSS	AR42
V3	VSS	VSS	AR9
V45	VSS	VSS	AT10
W14	VSS	VSS	AT15
W31	VSS	VSS	AT36
W32	VSS	VSS	AT9
W33	VSS	VSS	AU1
W38	VSS	VSS	AU35
W4	VSS	VSS	AU36
W8	VSS	VSS	AU39
Y17	VSS	VSS	AU45
	VSS	VSS	C4

SUNRISE-1-GP

PCH1J 10 OF 12

SPL PCH-H

BD2	VSS_BD2	RSVD_AR22	AR22
BD45	VSS_BD45	RSVD_W13	W13
BD44	VSS_BD44	RSVD_U13	U13
BE44	VSS_BE44	RSVD_P31	P31
D45	VSS_D45	RSVD_N31	N31
A42	VSS_A42	RSVD_P27	P27
B45	VSS_B45	RSVD_R27	R27
B44	VSS_B44	RSVD_N29	N29
A4	VSS_A4	RSVD_P29	P29
A3	VSS_A3	RSVD_AN29	AN29
B2	VSS_B2	RSVD_R24	R24
A2	VSS_A2	RSVD_P24	P24
B1	VSS_B1		
BB1	VSS_BB1		
BC1	VSS_BC1		
A44	VSS_A44		
C1	RSVD_C1		
D1	RSVD_D1		

		PREQ#	AT3
		PRDY#	AT4
		CPU_TRST#	AY5
		PCH_TRIGOUT	AL2
		PCH_TRIGIN	AK1

PCH_2_CPU_TRIGGER_R — R2301 1 — 30R2J-1-GP

XDP_PREQ# 6,99
XDP_PRDY# 6,99
PROC_TRST# 6,99
PCH_2_CPU_TRIGGER 8
CPU_2_PCH_TRIGGER 8

SUNRISE-1-GP

SA驗證

<Core Design>

緯創資通 Wistron Corporation
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Title: PCH_RSVD_VSS

Size: B | Document Number: Newgate | Rev: 1M

Date: Tuesday, August 18, 2015 | Sheet 23 of 105

SSID = KBC

071.09028.000G

Royee 20150204

9028 hasn't 0313

OPMODE (Pin71): PU (Default:eSPI)
OPMODE(Default/Internal PU):

EC9028	ASM(LPC)
EC9038	DY(eSPI)

ENG change 0412

modify 0227

PD change 0622

ENG change 0423 (USB_CHAR_CT2)
ENG change 0427 (TBTA_MRESET)

PD change 0706

Touch Pad modify 0227

---CPU/GPU
< -BATTER /CHARGER

SYS_PWROK(S0_PWR_GOOD) ==DELAY 100ms

Change R2428 and pic 0223

UN 0225

PCB_VER_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	
SA	100.0K	10.0K	3.000 V	3.005 V	>= 2.875 V	
SB	100.0K	20.0K	2.750 V	2.759 V	>= 2.619 V	< 2.875 V
SC	100.0K	33.0K	2.481 V	2.493 V	>= 2.363 V	< 2.619 V
-1	100.0K	47.0K	2.245 V	2.259 V	>= 2.123 V	< 2.363 V
-1M	100.0 K	64.9 K	2.001 V	2.011 V	>= 1.834 V	< 2.123 V
Reserved for project use	100.0K	76.8K	1.867 V	1.883 V	>= 1.758 V	< 1.834 V
Reserved for project use	100.0K	100.0K	1.650 V	1.667 V	>= 1.504 V	< 1.758 V
Reserved for project use	100.0K	143.0K	1.358 V	1.374 V	>= 1.261 V	< 1.504 V
Reserved for project use	100.0K	174.0K	1.204 V	1.220 V	>= 1.126 V	< 1.261 V
Reserved for project use	100.0K	215.0K	1.048 V	1.062 V	>= 0.924 V	< 1.126 V

ADT_TYPE_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	
65W	N/A	100.0 K	0.000 V		>= 0.000 V	
90W	100.0 K	N/A	0.000 V			< 0.150 V
30W	10.0 K	100.0 K	0.300 V	0.305 V	>= 0.150 V	< 0.425 V
45W	20.0 K	100.0 K	0.550 V	0.559 V	>= 0.425 V	< 0.684 V
120W	33.0 K	100.0 K	0.819 V	0.831 V	>= 0.684 V	< 0.957 V
135W	47.0 K	100.0 K	1.055 V	1.070 V	>= 0.957 V	< 1.177 V
150W	64.9 K	100.0 K	1.298 V	1.319 V	>= 1.177 V	< 1.366 V
Reserved	76.8 K	100.0 K	1.493 V	1.490 V	>= 1.366 V	< 1.542 V
Reserved	100.0 K	100.0 K	1.650 V	1.667 V	>= 1.542 V	< 1.842 V

MODEL_ID_AD	Pull-Low Register	Pull-High Register	Typical Voltage
Rayleigh-SL_UMA	100.0 K	10.0 K	3.000 V
Rayleigh-SL_945M	100.0 K	20.0 K	2.750 V
Rayleigh-SL_950M	100.0 K	33.0 K	2.481 V
Rayleigh-SLS_960M	100.0 K	47.0 K	2.245 V
Newgate-SLS_945M	100.0 K	64.9 K	2.001 V
Newgate-SLS_950M	100.0 K	76.8 K	1.867 V
Newgate-SLS_960M	100.0 K	100.0 K	1.650 V
Reserved for project use	100.0 K	143.0 K	1.358 V
Reserved for project use	100.0 K	174.0 K	1.204 V
Reserved for project use	100.0 K	215.0 K	1.048 V

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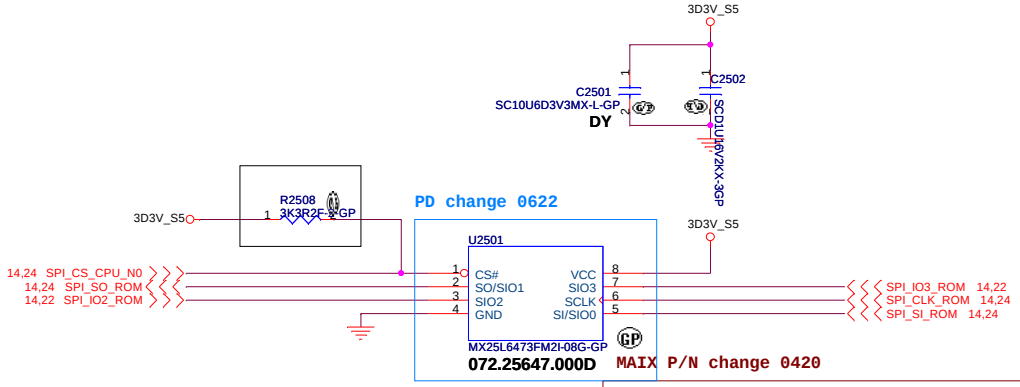
File: KBC_ENE_KB9028_KB9038_
Size: A1 | Document Number: Newgate | Rev: 1M
Date: Tuesday, August 18, 2015 | Sheet 24 of 105

SSID = Flash.ROM

SPI FLASH ROM (8M byte) for PCH



SPI FLASH ROM (8M byte) for PCH

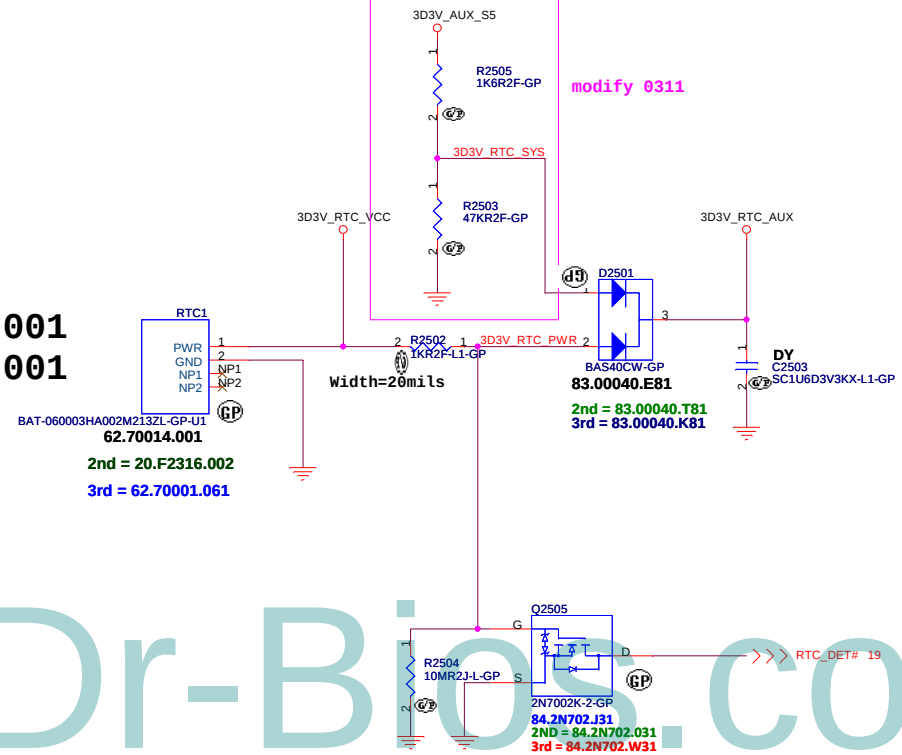
SPI ROM Equal length need to less than 500mil

SPI FLASH ROM (8M byte)

1st = 072.25647.000D (MXIC MX25L6473FM2I-08G)
2nd= 072.25Q64.0F01 (MICRON N25Q064A13ESED0F)
3rd= 72.25Q64.K01 (WINBOND W25Q64FVSSIQ)

Main Func = RTC

RTC BATTERY
1st= 23.22065.001
2nd= 23.20068.001



<Core Design>

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Title: Flash(KBC+PCH)/RTC

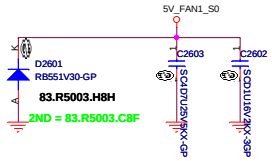
Size: A3 | Document Number: Newgate | Rev: 1M

Date: Tuesday, August 18, 2015 | Sheet 25 of 105

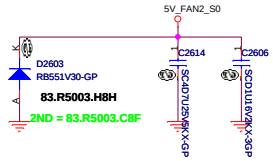
SSID = Thermal

ADB (Active Dusting Blower) function

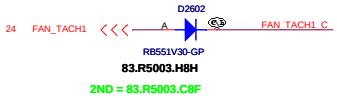
Layout 15 mil

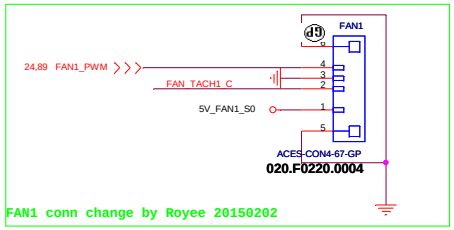


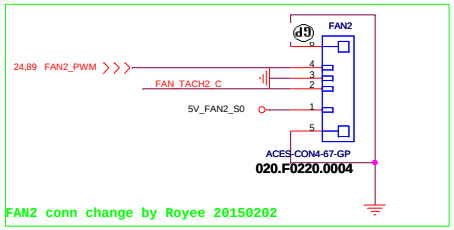
Layout 15 mil



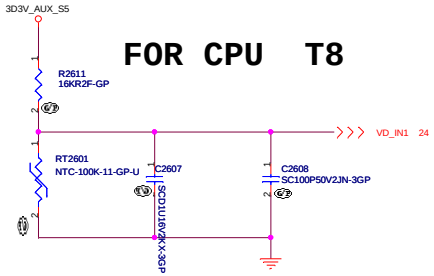
AFTP TESTPOINT

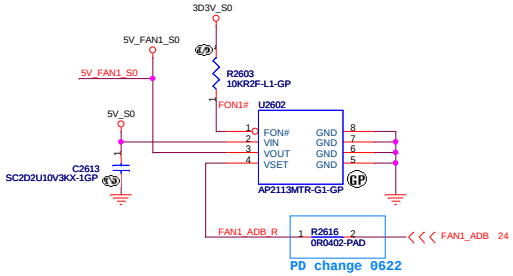


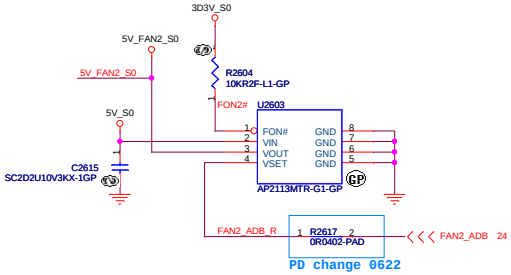


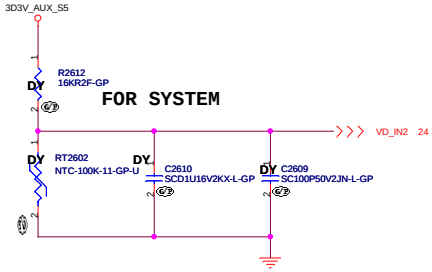


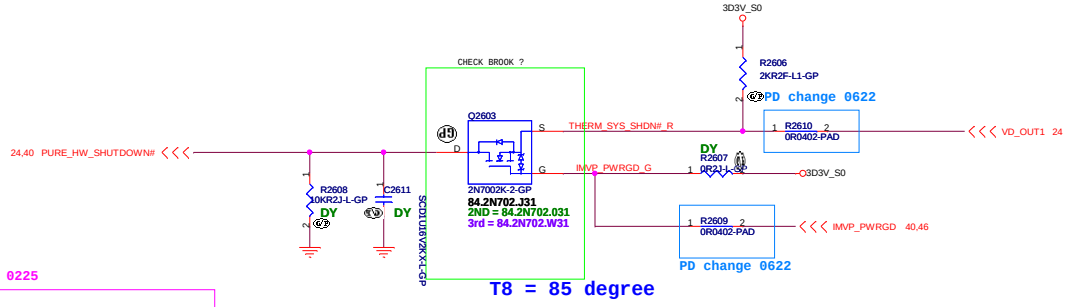
FOR CPU T8











UN 0225

T8 = 85 degree

<Core Design>

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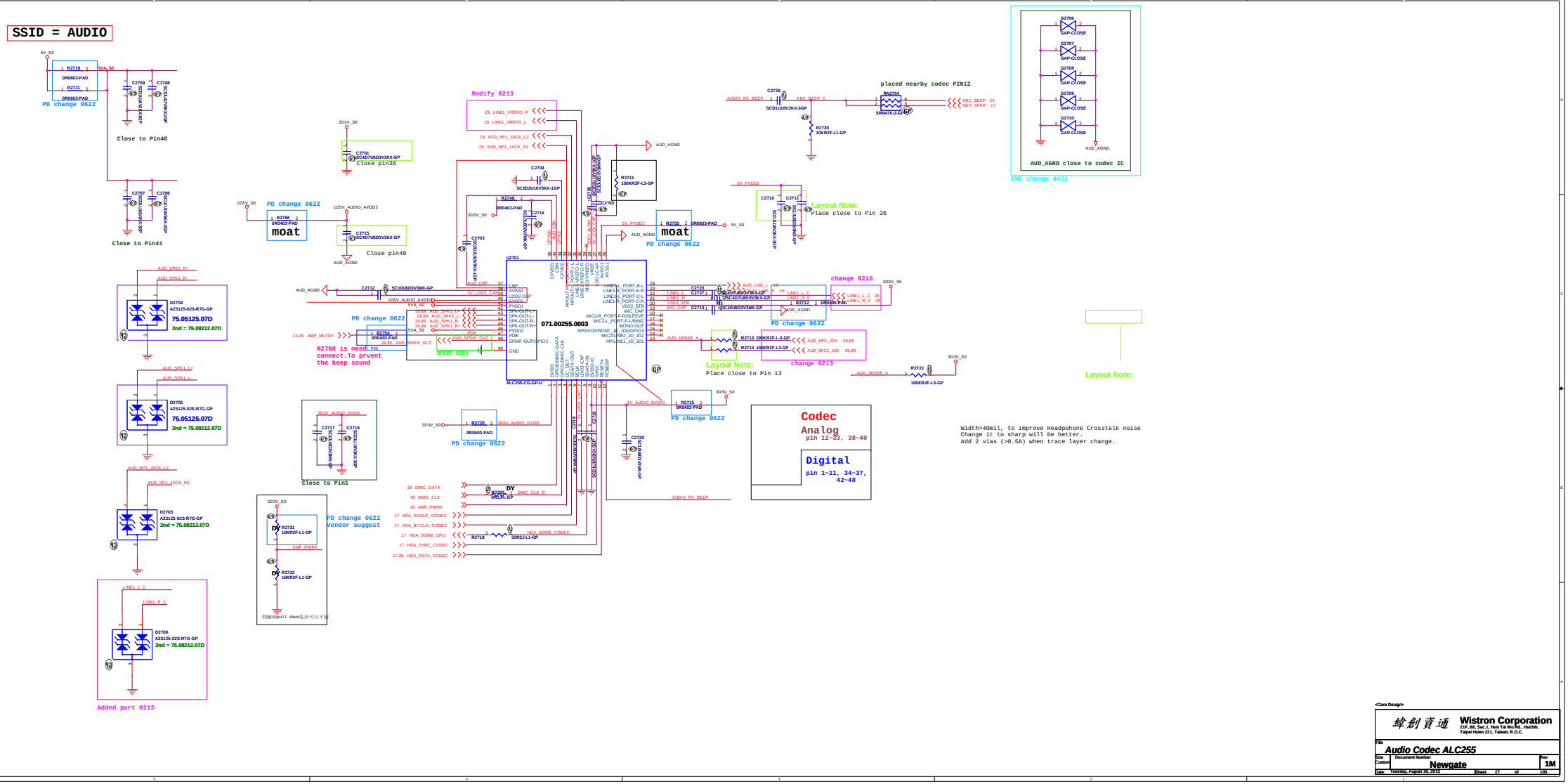
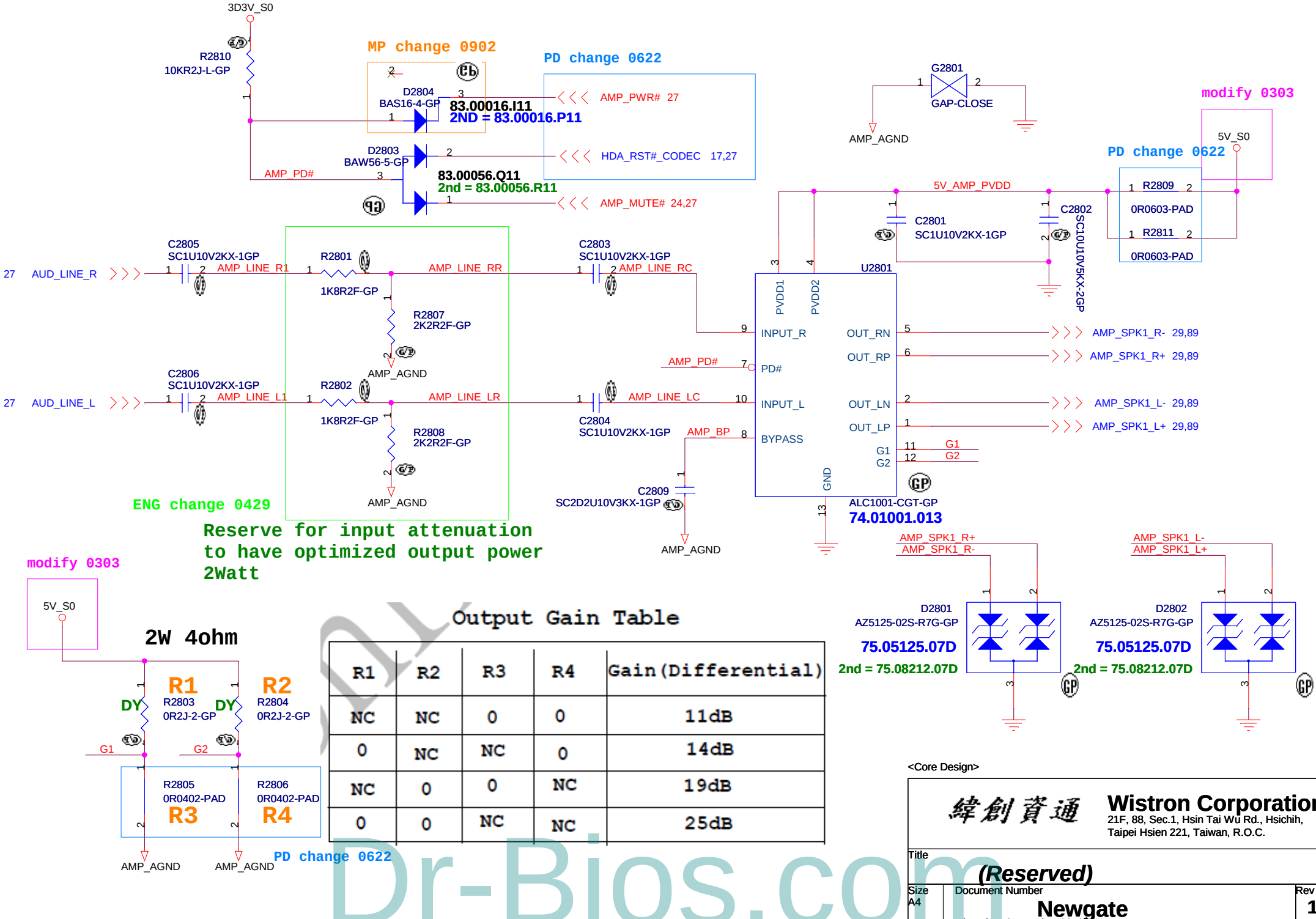
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal T8 and FAN

Size: Custom | Document Number: Newgate | Rev: 1M

Date: Tuesday, August 18, 2015 | Sheet 26 of 105


SSID = AUDIO
PD change 0622
Close to Pin46
Close to Pin41
Modify 0213
Close pin36
Close pin40
moat
placed nearby codec PIN12
AUD_AGND close to codec IC
ENG change 0421
Layout Note:
Place close to Pin 26
change 0216
change 0213
Layout Note:
Place close to Pin 13
Layout Note:
R2708 is need to connect.To prvent the beep sound
SPDIF 0203
071.00255.0003
ALC255-CG-GP-U
Close to Pin1
PD change 0622
Vendor suggest
Added part 0213
Codec
Analog
pin 12~33, 38~40
Digital
pin 1~11, 34~37, 42~48
Width>40mil, to improve Headpohone Crosstalk noise
Change it to sharp will be better.
Add 2 vias (>0.5A) when trace layer change.
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Audio Codec ALC255
Newgate
1M
Tuesday, August 18, 2015
27
105



Output Gain Table

R1	R2	R3	R4	Gain(Differential)
NC	NC	0	0	11dB
0	NC	NC	0	14dB
NC	0	0	NC	19dB
0	0	NC	NC	25dB

<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***(Reserved)***

Size: A4 | Document Number: **Newgate** | Rev: **1M**

Date: Wednesday, September 02, 2015 | Sheet 28 of 105

SSID = AUDIO

Check speaker spec and confirm 2nd with ME 0302

Speaker

28,89 AMP_SPK1_L-
28,89 AMP_SPK1_L+
27,89 AUD_SPK1_L-
27,89 AUD_SPK1_L+
28,89 AMP_SPK1_R-
28,89 AMP_SPK1_R+
27,89 AUD_SPK1_R-
27,89 AUD_SPK1_R+

12/17

Layout Note:
Trace width=40mil

EC2906 EC2905 EC2904 EC2903 EC2916 EC2917 EC2918 EC2919
DY
SC1KP50V2KX-1-GP

SPK1
ACES-CON8-12-GP-U1
20.F0818.008
1nd = 20.F0818.008

AMP_SPK1_L- <<< AMP_SPK1_L- 28,89
AMP_SPK1_L+ <<< AMP_SPK1_L+ 28,89
AUD_SPK1_L- <<< AUD_SPK1_L- 27,89
AUD_SPK1_L+ <<< AUD_SPK1_L+ 27,89
AMP_SPK1_R- <<< AMP_SPK1_R- 28,89
AMP_SPK1_R+ <<< AMP_SPK1_R+ 28,89
AUD_SPK1_R- <<< AUD_SPK1_R- 27,89
AUD_SPK1_R+ <<< AUD_SPK1_R+ 27,89

AFTP TESTPOINT

AUD_HP1_JACK_R2_OUT <<< AUD_HP1_JACK_R2_OUT 89
AUD_HP1_JACK_L2_OUT <<< AUD_HP1_JACK_L2_OUT 89
LINE1_L_IN <<< LINE1_L_IN 89
LINE1_R_IN <<< LINE1_R_IN 89
5V_SPDIF_S0 <<< 5V_SPDIF_S0 89
AUD_SPDIF_OUT <<< AUD_SPDIF_OUT 27,89

ENG add AFTP 0430
AFTP TESTPOINT

5V_S0 — C2920 DY SCD1U16V2ZY-2GP
AUD_HP1_JD#
U2901 SY6288DAAC-GP
IN EN# OUT GND OC#
074.06288.009B
2nd = 074.00524.0C9F
3rd = 074.02822.009F
5V_SPDIF_S0
C2921 SCD1U16V2ZY-2GP DY
R2903 DY 0R2J-2-GP

ENG change 0412

LINE OUT

ENG change 0504
PD change 0622
ENG connector change 0504

27 AUD_HP1_JACK_R2
27 AUD_HP1_JACK_L2
R2904 63D4R3F-GP AUD_HP1_JACK_R2_R
R2905 63D4R3F-GP AUD_HP1_JACK_L2_R
R2908 0R0402-PAD
R2909 0R0402-PAD
AUD_HP1_JACK_R2_OUT
AUD_HP1_JACK_L2_OUT
27,89 AUD_HP1_JD#
5V_SPDIF_S0
27,89 AUD_SPDIF_OUT
C2922 DY SC100P50V2JN-3GP
C2923 DY SC100P50V2JN-3GP
AUD_AGND
SPDIF1
M6 M1 M4 M5 M7
LED
DRIVE IC
A B C 8 9
TX
AUDIO-JK530-GP-U
022.10033.0011

SCHEMATIC
M6 M1 M4 M5 M7
LED DRIVE IC Tx
A GND B VCC C Vin

MIC IN

ENG connector change 0504
PD change 0622

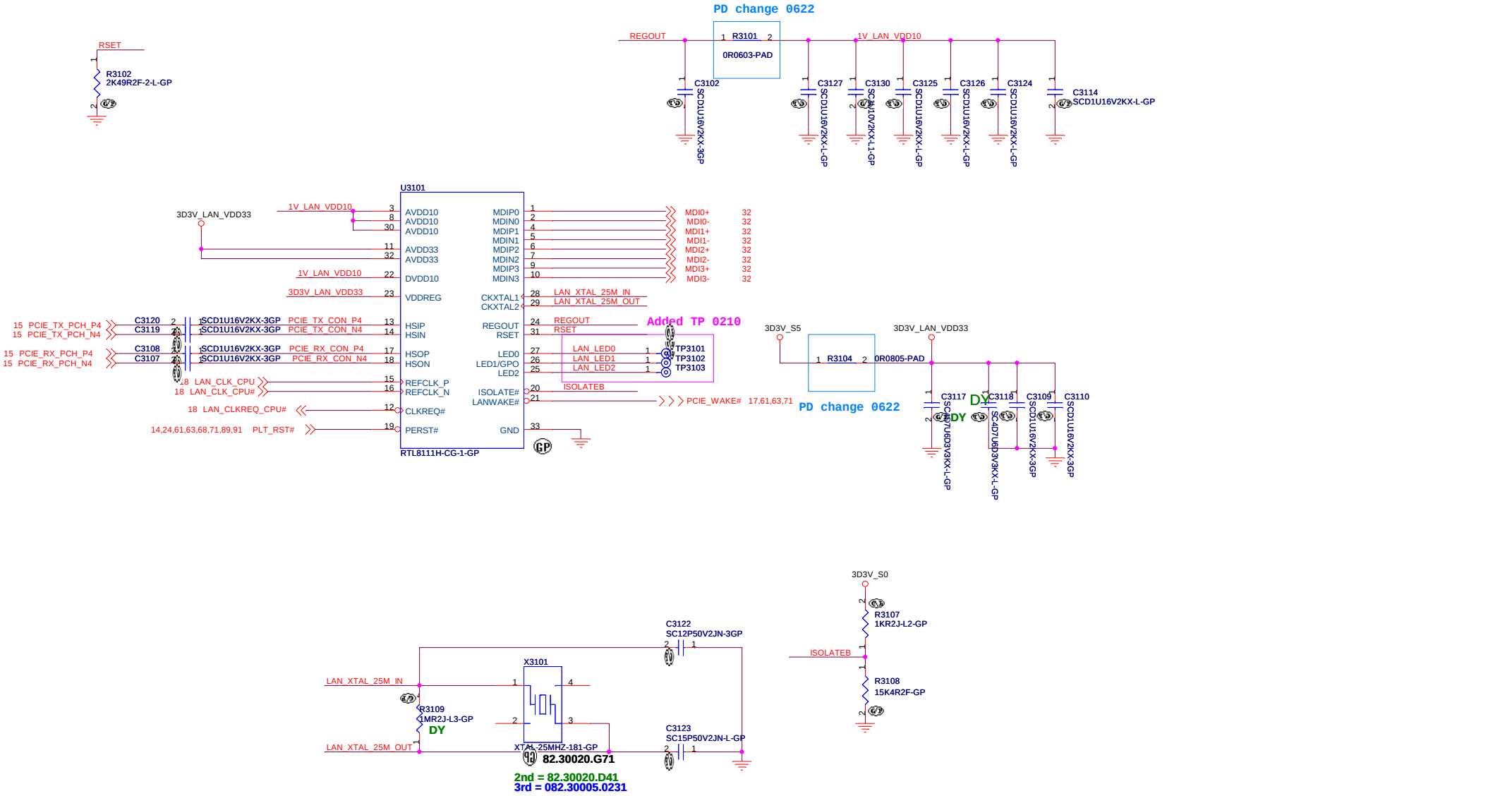
27 LINE1_VREFO_L
27 LINE1_VREFO_R
27 LINE1_L_C
27 LINE1_R_C
R2906 2K2R2J-L1-GP
R2907 2K2R2J-L1-GP
R2901 1KR2F-L1-GP
R2902 1KR2F-L1-GP
LINE1_L_R
LINE1_R_R
R2910 0R0402-PAD
R2911 0R0402-PAD
LINE1_L_IN
LINE1_R_IN
27,89 AUD_MIC1_JD#
C2924 DY SC100P50V2JN-3GP
C2925 DY SC100P50V2JN-3GP
AUD_AGND
MICIN1
M5 M4 M3 M1 MP MQ NP1 NP2
AUDIO-JK528-GP-U1
022.10002.00J1

SCHEMATIC | SCHEMATIC (PLUG IN)
M5 M4 M3 M1 MP MQ

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Speaker/ALC255
Size: Custom
Document Number: Newgate
Rev: 1M
Date: Tuesday, August 18, 2015
Sheet 29 of 105



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

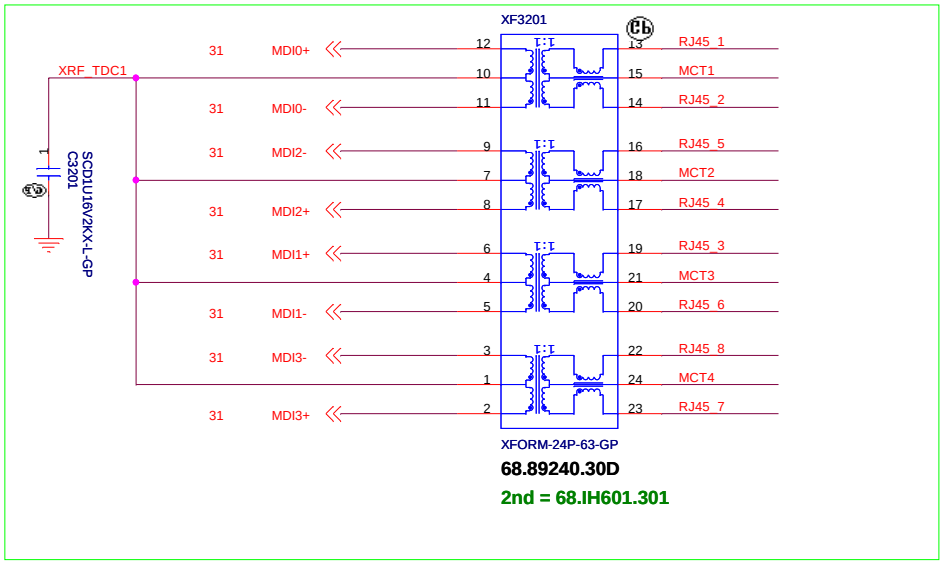
Title: LAN(RTL8111)

Size: A3 | Document Number: Newgate | Rev: 1M

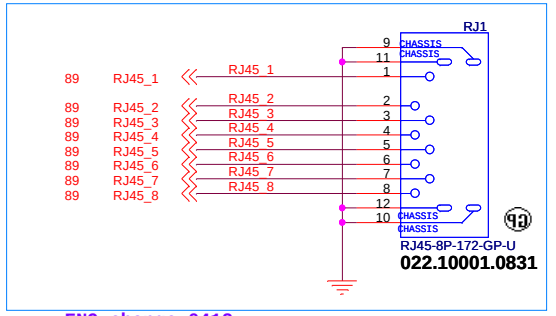
Date: Tuesday, August 18, 2015 | Sheet 31 of 105

SSID = LAN

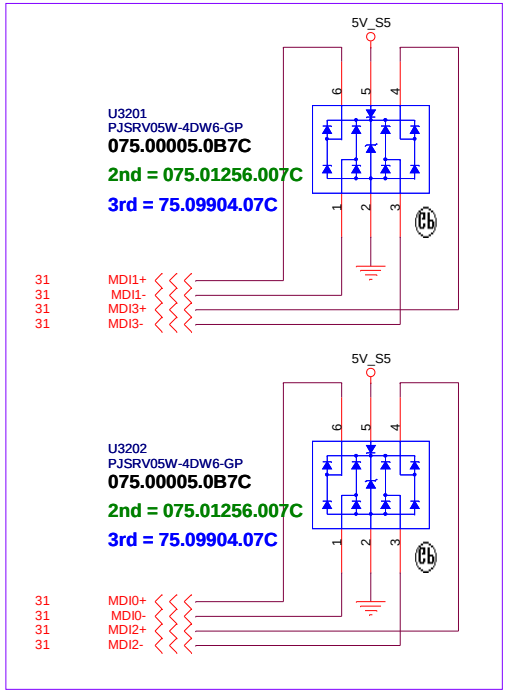
part change 0430



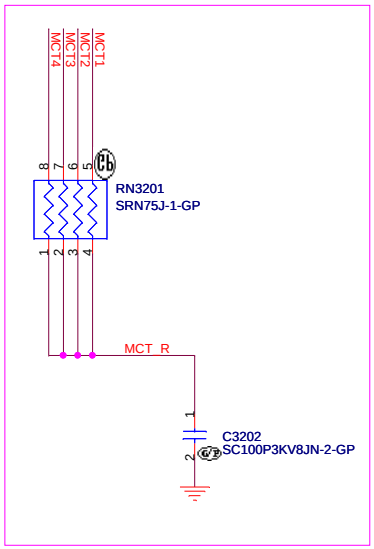
PD change 0624

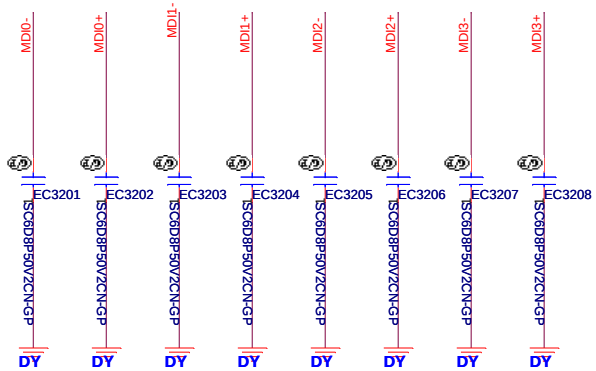


ENG change 0412



SWAP 0228





<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *RJ45+Transformer*		
Size: B	Document Number: Newgate	Rev: 1M
Date: Tuesday, August 18, 2015	Sheet 32 of 105	

Low Active 2A

5V_S5 → C3501 SC1U10V2KX-L1-GP

U3501 SY6288DAAC-GP (IN, EN#, OUT, GND, OC#)

5V_USB30 → C3502 SC1U16V2KX-L-GP, C3503 SC100U6D3V6MX-GP

24,66 USB_PWR_EN#

074.06288.009B
2nd = 074.00524.0C9F
3rd = 074.02822.009F

AFTP TESTPOINT

USB30_RX_CON_N1 89
USB30_RX_CON_P1 89
USB30_TX_CON_N1 89
USB30_TX_CON_P1 89
USB_CON_PN1 89
USB_CON_PP1 89
USB30_RX_CON_N2 89
USB30_RX_CON_P2 89
USB30_TX_CON_N2 89
USB30_TX_CON_P2 89
USB_CON_PN2 89
USB_CON_PP2 89

Close to USB1 0416

5V_USB30_CHARGER → C3504 SC100U6D3V6MX-GP

USB 3.0 Connector Pin definition

1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	

JJ 20150127

18 USB30_RX_CPU_N1 → FR3501 0R0402-PAD → USB30_RX_CON_N1
18 USB30_RX_CPU_P1 → FR3502 0R0402-PAD → USB30_RX_CON_P1

PD change 0701

FC3516 SCLP50V2CN-1GP DY, FC3503 SCLP50V2CN-1GP DY

18 USB30_TX_CPU_N1 → C3508 SCD1U16V2KX-L-GP → USB30_TX_N1_R → FR3504 0R0402-PAD → USB30_TX_CON_N1
18 USB30_TX_CPU_P1 → C3509 SCD1U16V2KX-L-GP → USB30_TX_P1_R → FR3506 0R0402-PAD → USB30_TX_CON_P1

PD change 0701

FC3505 SCLP50V2CN-1GP DY, FC3507 SCLP50V2CN-1GP DY

EU3501 PJE5UFN10A-GP

USB30_RX_CON_N1 ← 1, USB30_RX_CON_P1 ← 2, USB30_TX_CON_N1 ← 4, USB30_TX_CON_P1 ← 5

075.00510.0073
2nd = 075.00550.0071
3rd = 75.01045.073

EL3501 MCM1012B900FBP-GP-U

36 USB_CHAR_PP1 → USB_CON_PP1
36 USB_CHAR_PN1 → USB_CON_PN1

68.01012.201
2nd = 68.00396.001
3rd = 69.10118.001

EU3503 PJSRV05W-4DW6-GP

USB_CON_PN2 ↔ USB_CON_PP2
USB_CON_PN1 ↔ USB_CON_PP1
5V_S5

075.00005.0B7C
2nd = 075.01256.007C
3rd = 75.09904.07C

USB3.0 conn change by Royee 20150202
PD change 0624

5V_USB30_CHARGER → USB1 SKT-USB13-72-GP-U

USB_CON_PN1 ↔ USB_CON_PN1
USB_CON_PP1 ↔ USB_CON_PP1
USB30_RX_CON_N1 ↔ USB30_RX_CON_N1
USB30_RX_CON_P1 ↔ USB30_RX_CON_P1
USB30_TX_CON_N1 ↔ USB30_TX_CON_N1
USB30_TX_CON_P1 ↔ USB30_TX_CON_P1
VBUS, D-, D+, STDA_SSRX-, STDA_SSRX+, STDA_SSTX-, STDA_SSTX+, GND_DRAIN, GND

22.10341.711
2nd = 22.10339.I41

5V_USB30 → USB2 SKT-USB13-72-GP-U

USB_CON_PN2 ↔ USB_CON_PN2
USB_CON_PP2 ↔ USB_CON_PP2
USB30_RX_CON_N2 ↔ USB30_RX_CON_N2
USB30_RX_CON_P2 ↔ USB30_RX_CON_P2
USB30_TX_CON_N2 ↔ USB30_TX_CON_N2
USB30_TX_CON_P2 ↔ USB30_TX_CON_P2
VBUS, D-, D+, STDA_SSRX-, STDA_SSRX+, STDA_SSTX-, STDA_SSTX+, GND_DRAIN, GND

22.10341.711
2nd = 22.10339.I41

JJ 20150127

PD change 0701

18 USB30_RX_CPU_N2 → FR3508 0R0402-PAD → USB30_RX_CON_N2
18 USB30_RX_CPU_P2 → FR3510 0R0402-PAD → USB30_RX_CON_P2

FC3509 SCLP50V2CN-1GP DY, FC3511 SCLP50V2CN-1GP DY

PD change 0701

18 USB30_TX_CPU_N2 → C3511 SCD1U16V2KX-L-GP → USB30_TX_N2_R → FR3512 0R0402-PAD → USB30_TX_CON_N2
18 USB30_TX_CPU_P2 → C3510 SCD1U16V2KX-L-GP → USB30_TX_P2_R → FR3514 0R0402-PAD → USB30_TX_CON_P2

FC3513 SCLP50V2CN-1GP DY, FC3515 SCLP50V2CN-1GP DY

15 USB_PCH_PN2 → USB_CON_PN2
15 USB_PCH_PP2 → USB_CON_PP2

EL3502 MCM1012B900FBP-GP-U

68.01012.201
2nd = 68.00396.001
3rd = 69.10118.001

EU3502 PJE5UFN10A-GP

USB30_RX_CON_N2 ← 1, USB30_RX_CON_P2 ← 2, USB30_TX_CON_N2 ← 4, USB30_TX_CON_P2 ← 5

075.00510.0073
2nd = 075.00550.0071
3rd = 75.01045.073

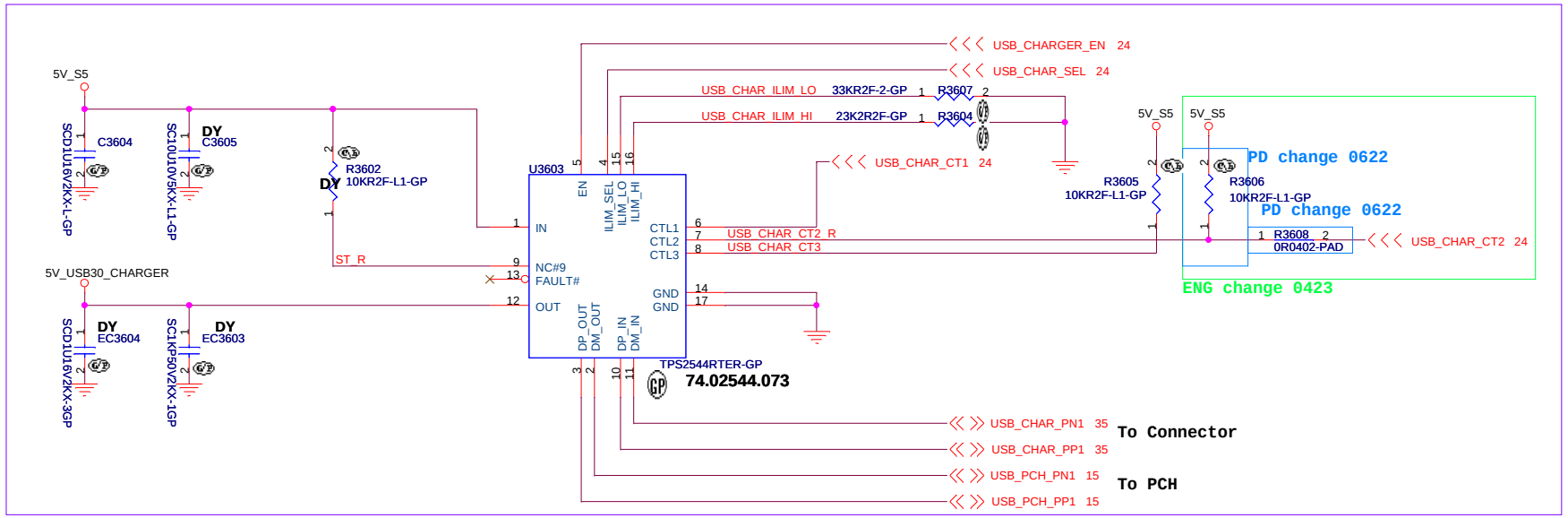
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB3.0 CONN

Size: A3 | Document Number: Newgate | Rev: 1M

Date: Tuesday, August 18, 2015 | Sheet 35 of 105



ENG change 0412

Table 2. Truth Table

CTL1	CTL2	CTL3	ILIM_ SEL	MODE	Current Limit Setting	Status Output	Notice
0	0	0	0	Discharge	NA	OFF	OUT held low
0	0	0	1	Discharge	NA	OFF	
0	0	1	0	DCP_Auto	ILIM_HI	OFF	Data lines disconnected
0	0	1	1	DCP_Auto	ILIM_HI	DCP	Data lines disconnected Load Detect function active
0	1	0	0	SDP1	ILIM_LO	OFF	Data lines connected
0	1	0	1	SDP1	ILIM_HI	OFF	
0	1	1	0	DCP_Auto	ILIM_LO	OFF	Data lines disconnected
0	1	1	1	DCP_Auto	ILIM_HI	DCP	Data lines disconnected Load Detect function active
1	0	0	0	DCP_Shorted	ILIM_LO	OFF	Device forced to stay in DCP BC1.2
1	0	0	1	DCP_Shorted	ILIM_HI	OFF	Charging mode
1	0	1	0	DCP/Divider1	ILIM_LO	OFF	Device forced to stay in DCP divider1
1	0	1	1	DCP/Divider1	ILIM_HI	OFF	Charging mode
1	1	0	0	SDP1	ILIM_LO	OFF	Data lines connected
1	1	0	1	SDP1	ILIM_HI	OFF	
1	1	1	0	SDP2	ILIM_LO	OFF	
1	1	1	1	CDP	ILIM_HI	CDP	Data lines disconnected Load Detect function active

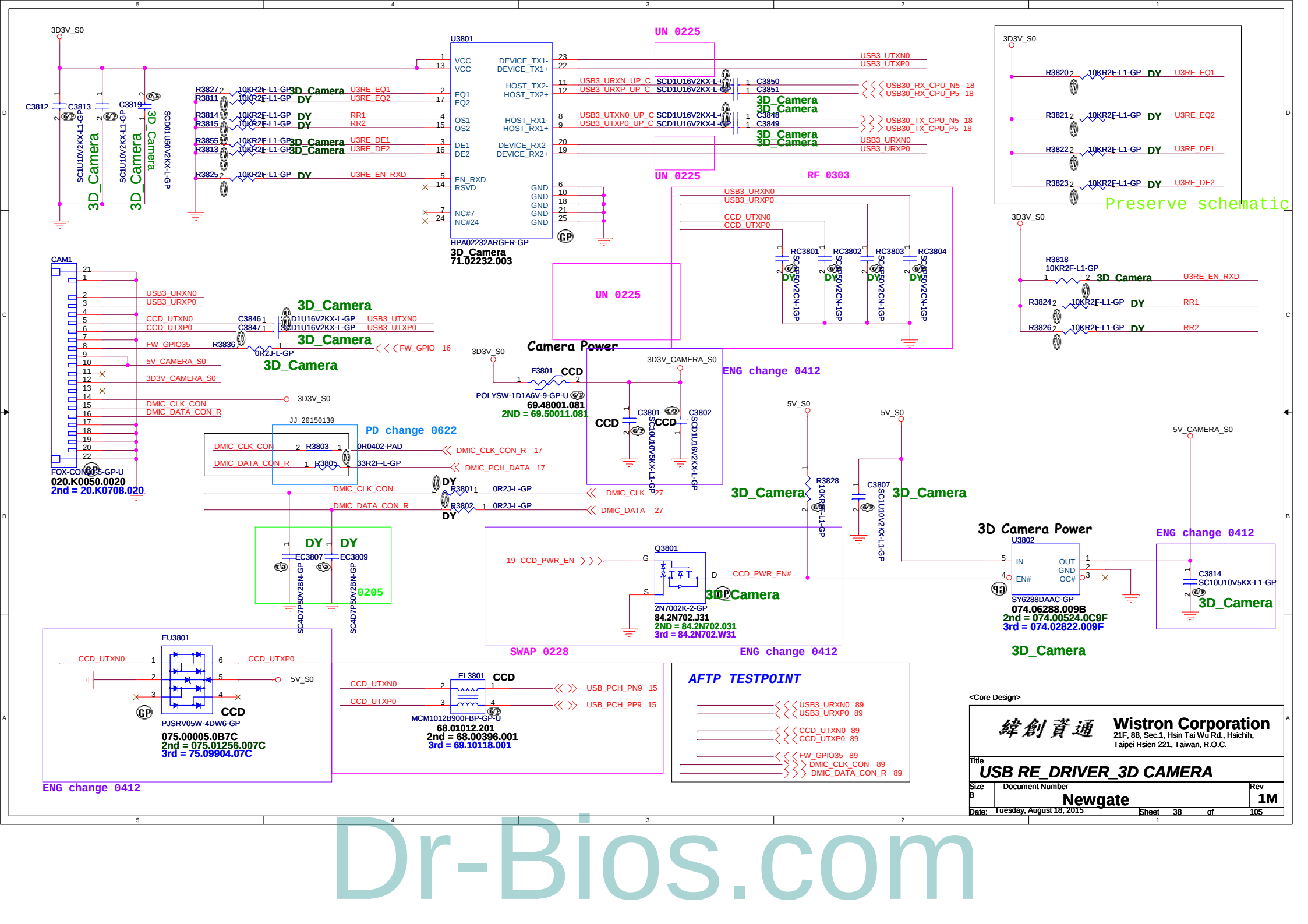
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

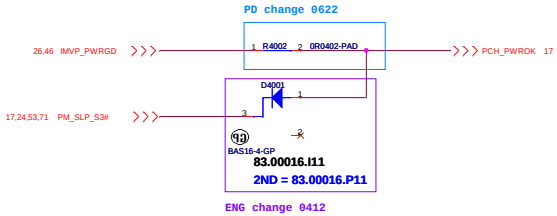
Title: **USB CHARGER**

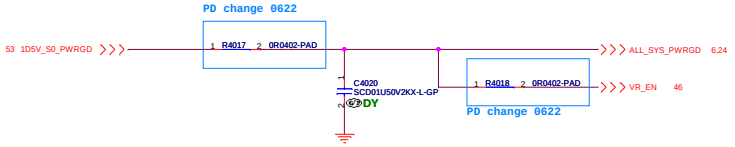
Size: B | Document Number: **Newgate** | Rev: **1M**

Date: Tuesday, August 18, 2015 | Sheet 36 of 105

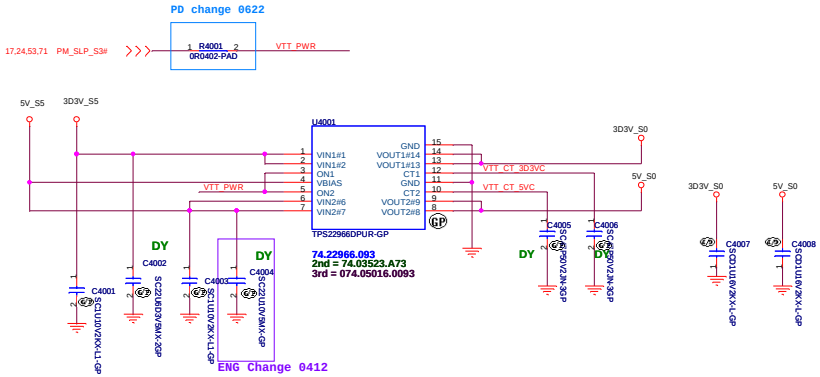

3D3V_S0
U3801
HPA02232ARGER-GP
3D_Camera
71.02232.003
UN 0225
RF 0303
Preserve schematic
CAM1
FOX-CONN-GP-U
020.K0050.0020
2nd = 20.K0708.020
Camera Power
3D3V_CAMERA_S0
ENG change 0412
PD change 0622
JJ 20150130
5V_S0
3D Camera Power
U3802
SY6288DAAC-GP
074.06288.009B
2nd = 074.00524.0C9F
3rd = 074.02822.009F
5V_CAMERA_S0
Q3801
2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031
3rd = 84.2N702.W31
SWAP 0228
EU3801
PJSRV05W-4DW6-GP
075.00005.0B7C
2nd = 075.01256.007C
3rd = 75.09904.07C
EL3801
MCM1012B900FBP-GP-U
68.01012.201
2nd = 68.00396.001
3rd = 69.10118.001
AFTP TESTPOINT
0205
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
USB RE_DRIVER_3D CAMERA
Size B
Document Number
Newgate
Rev 1M
Date: Tuesday, August 18, 2015
Sheet 38 of 105

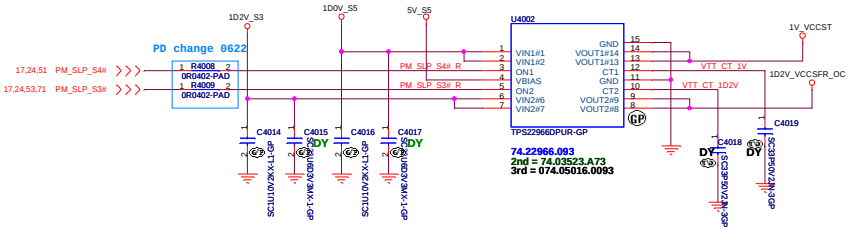
Power Sequence

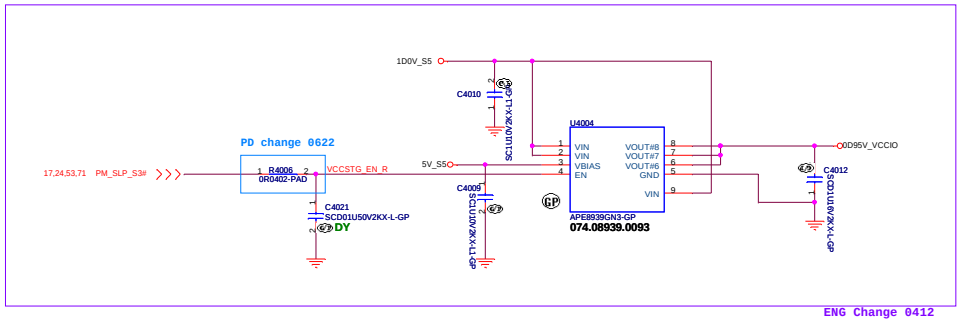


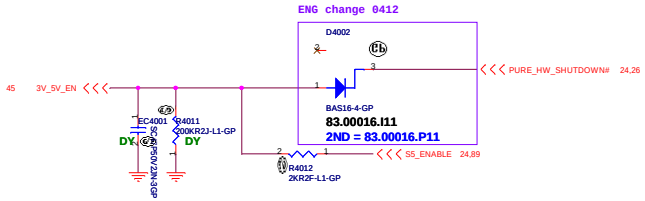


ANNIE Run Power









<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable & SEQUENCE

Size: A2 | Document Number: Newgate | Rev: 1M

Date: Tuesday, August 18, 2015 | Sheet 40 of 105

UN 0225

12V_BT+_connector

PC4304
SCD1U25V2KX-L-GP

PD change 0626 update symbol

BAT1

ACES-CON10-38-GP-U2
20.F2133.010

PN4301

24,44 BAT_IN#
24,44 BAT_SCL
24,44 BAT_SDA

BAT_IN#_1
BAT_SCL_1
BAT_SDA_1

BI

SRN33J-7-GP-U

PD4303
MMSZ5232BS-GP
83.5R603.Q3F
DY
2ND = 83.5R603.K3F
3RD = 83.5R603.D3F

PD4302
AZ5125-02S-R7G-GP
DY
2nd = 75.08212.07D

Battery Reset

RST1 conn change by Royee 20150202

3D3V_RTC_AUX

PR4310
1MR2J-L-GP

BI_RST

RST1
SW-TACT-124-GP

62.40078.001
2nd = 62.40009.D71
3rd = 62.40089.441

ENG change 0412
DY 0421

3D3V_RTC_AUX

PR4309
10MR2J-L-GP
DY

BI

Q4301
DMN5L06K-7-GP

BI_RST

DY
PR4307
0R2J-L-GP

BIS

ENG change 0416

Battery Insert

BTSW1 conn change by Royee 20150202
PD change 0624

BIS

BTSW1

SW-TACT-5P-GP

AFTP TESTPOINT

89 BI
89 BAT_IN#_1
89 BAT_SCL_1
89 BAT_SDA_1

BI
BAT_IN#_1
BAT_SCL_1
BAT_SDA_1

ANNIE solution

Adaptor in to generate DCBATOUT

DCIN1

ACES-CONN12S-2-GP
20.F2434.006
2nd = 20.F2383.006

PD4301
P6SMBJ20A-GP
83.P6SMB.AAG
2nd = 083.00020.00AG

PC4302
SC1U50V5ZY-1-GP-U

AD_JK

PC4305
SCD1U50V3KX-L-GP

ENG change 0412

24 AD_OFF

PQ4304

LTC024EUB-FS8-GP
84.00024.A1K
2ND = 84.00124.H1K
3rd = 84.00124.V1K

PWR_ADJK_EN

PQ4305

LTA024EUB-FS8-GP
84.00024.01K
2nd = 84.02303.01K

ENG change 0421

AD_JK

ENG change 0412

PR4305
200KR3F-GP

PC4306
SC1U50V5ZY-1-GP-U

PWR_AD+_2

PU4302
TPCC8103-GP
84.08103.037
2nd = 084.03335.0037

19V_AD+

2nd change 0421

PR4304
100KR2F-L3-GP

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC IN / BATT Conn

Size: A3 | Document Number: Newgate | Rev: 1M

Date: Tuesday, August 18, 2015 | Sheet 43 of 105

SSID = Charger

Adaptor			Protect	Sense	Amplifer		R1	R2
Watt	Current	Persent	Current	Resistor	Ratio	IADP	PR4407	PR4401
135.00 W	6.92 A	102%	7.06 A	10 m Ohm	40	2.62 V	137 K	100 K
120.00 W	6.15 A	102%	6.28 A	10 m Ohm	40	2.51 V	110 K	100 K
90.00 W	4.62 A	102%	4.71 A	10 m Ohm	40	1.00 V	50 K	100 K

Charger Current=1.4~3.6A

CYNTEC, 7*7*3
DCR: 37~40mOhm
Idc : 5.5 A , Isat : 10A

Total Power Setting

Royee 20150204

SMBuS

Royee 20150204

net change 0223

IDCHG : Dischange detect current :
= 8 or 16 x (Vsrn - Vsrp)

IADP : AC adapter detect current :
= 20 or 40 x (Vacp - Vacn) / 10mohm

PMON : Total system power

UN 0225

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER HPA02224

Size: Custom | Document Number: Newgate | Rev: 1M

Date: Wednesday, September 02, 2015 | Sheet 44 of 105

20141022 Jack

MP change 0814

RF 0412

close to PU4504

Add 3rd 0423

1st = 84.00920.037
2nd = 84.03664.037
3rd = 075.06994.0073

Design Current : 9.67A
OCP : 13.5A

MagLayer. 6.86 x 6.47 x 3.0mm
DCR: 18~20 mOhm
Idc : 8A , Isat : 14A

2ND = 84.08067.A37
2ND = 84.08065.B37
2ND change 0423

MagLayer. 6.86 x 6.47 x 3.0mm
DCR: 18~20 mOhm
Idc : 8A , Isat : 14A

Design Current : 11A
OCP : 16A

RF 0303

close to PL4502

close to PL4501

Close to FB2 Pin (pin4)

MP change 0804(PD EC)

Vout = 2 * (1 + R1/R2)
= 2 * (1 + 6.8K / 10K)
= 3.36V

ENG change 0412

PD change 0622

PWM 3D3V OCP

PWM 5V OCP

PD change 0625

Close to FB1 Pin (pin2)

Vout = 2 * (1 + R1/R2)
= 2 * (1 + 15.8K / 10K)
= 5.16 V

ENG change R4515 value 0504B

PWM 5V En

PD change 0622

PWM 3D3V En

PD change 0622

Vin POR threshold , Rising :4.6 V ; Failing : 3.7 V
EN threshold Logic-High : 1.6 V
EN threshold Logic-Low : 0.4 V

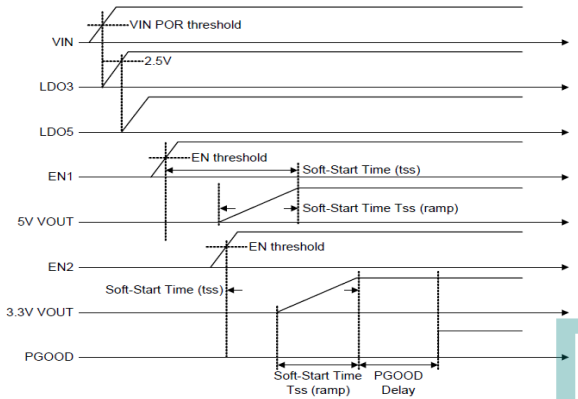


Figure 6. RT6575B Timing

<Core Design>

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Title: RT6575D_5V/3D3V

Size: A2 | Document Number: Newgate | Rev: 1M

Date: Tuesday, August 18, 2015 | Sheet 45 of 105

PROG1 - PR4612 : 110K -> VBOOT 0V / Slew Rate : 30mV/us / VRA:IA,VR2:GT,VR3:SA
PROG2 - PR4613 : 34K -> VRA IMAX:70A / VRA 2 Phase
PROG3 - PR4614 : 16K9 -> VRB IMAX:50A / VRB 2 Phase
PROG4 - PR4615 : 182K -> Droop Active / VRA & VRB FREQ 750KHz
PROG5 - PR4616 : 121K -> VRC IMAX 13A / VRC FREQ 750KHz

JJ 20150202

ISL95855HRTZ-GP

Title	ISL95855_CPU_VCORE(1/3)
Size	A2
Document Number	Newgate
Rev	1M
Date:	Wednesday, September 02, 2015
Sheet	46 of 105

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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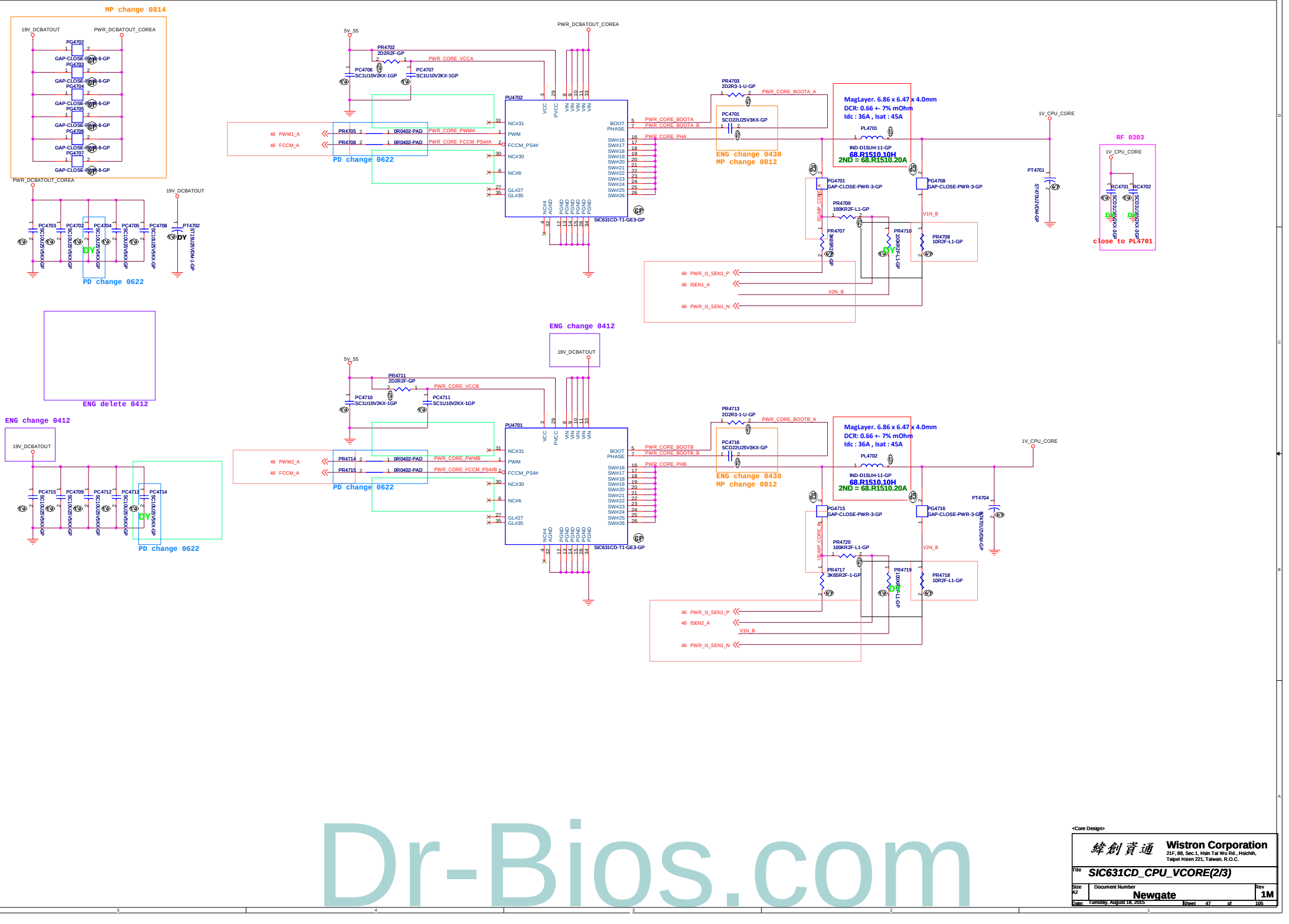

<Core Design>

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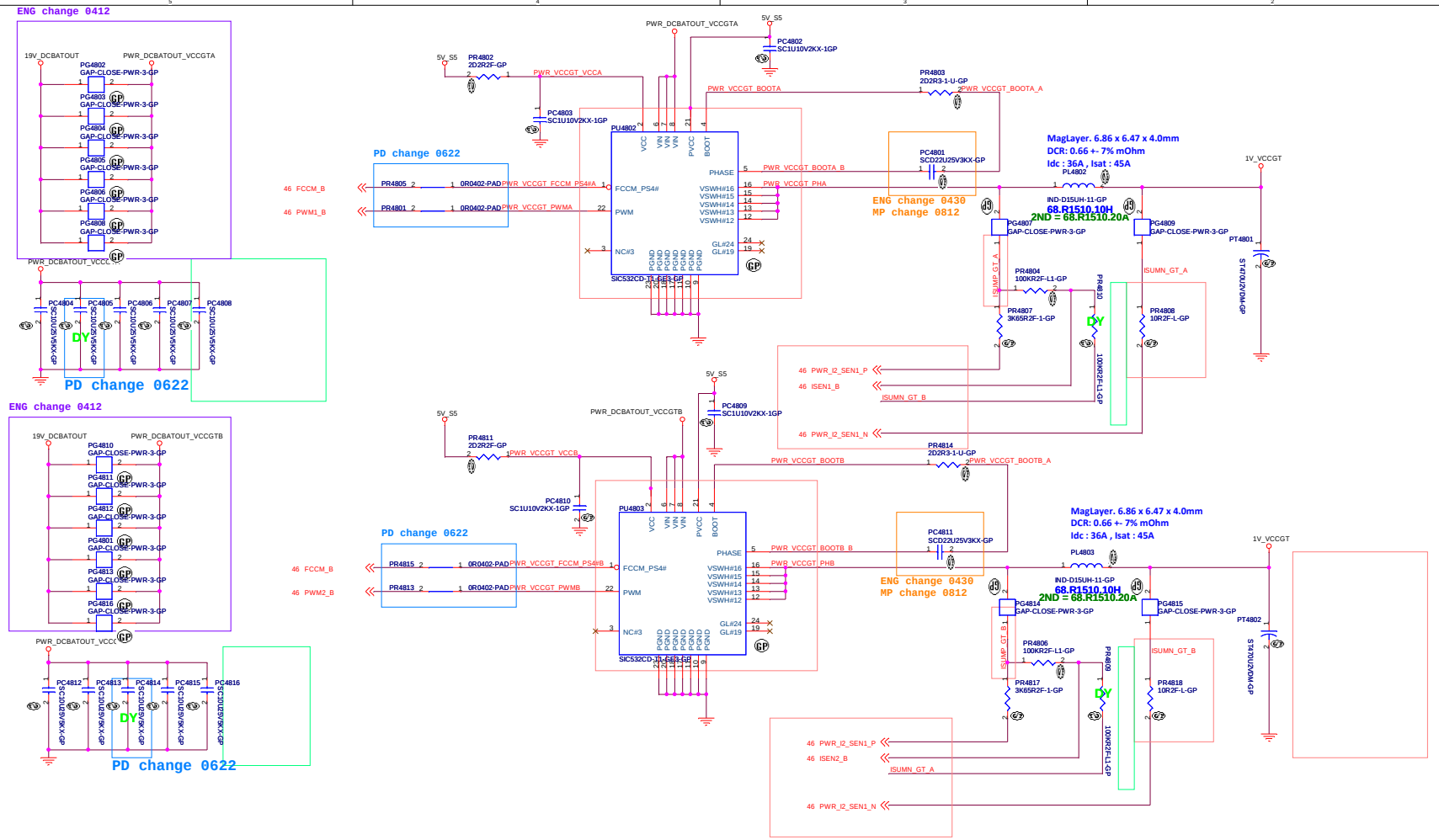
Title: SIC631CD_CPU_VCORE(2/3)

Size: A2 | Document Number: Newgate | Rev: 1M

Date: Tuesday, August 18, 2015 | Sheet 47 of 105



<Core Design>

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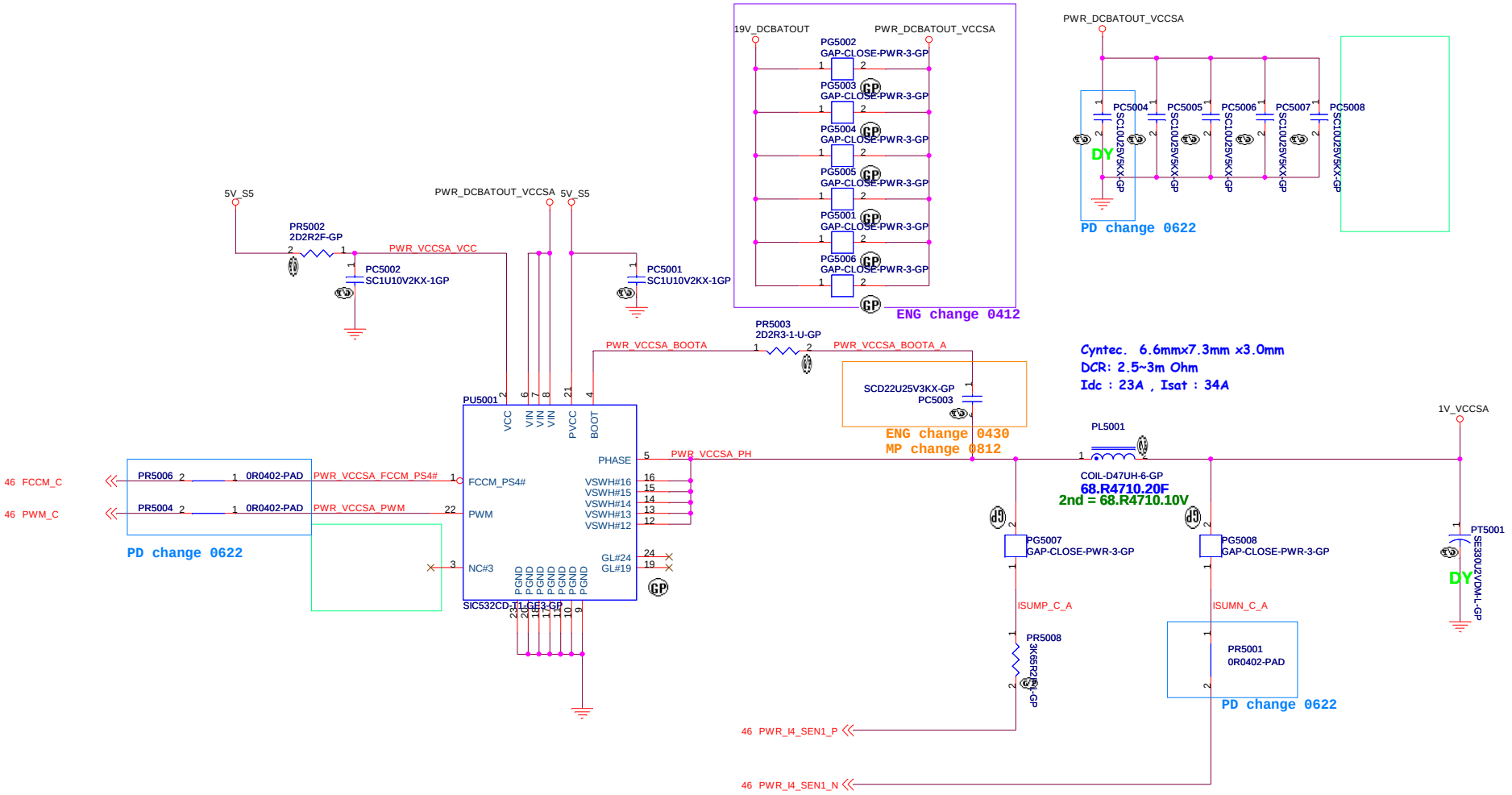
Title: SIC631CD_CPU_VCORE(2/3)

Size: A2 | Document Number: Newgate | Rev: 1M

Date: Tuesday, August 18, 2015 | Sheet 48 of 105



<Core Design>

Wistron Corporation
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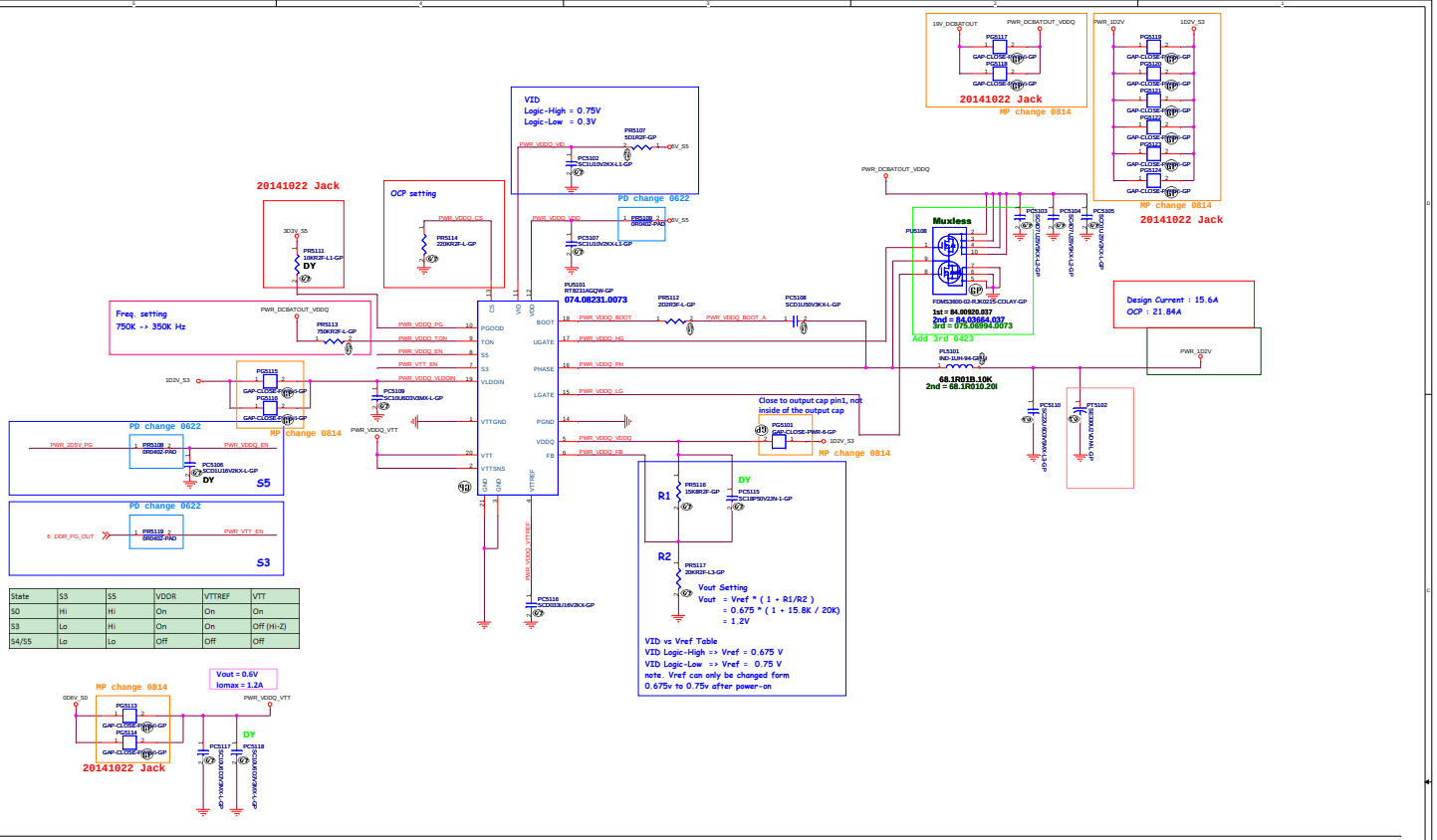
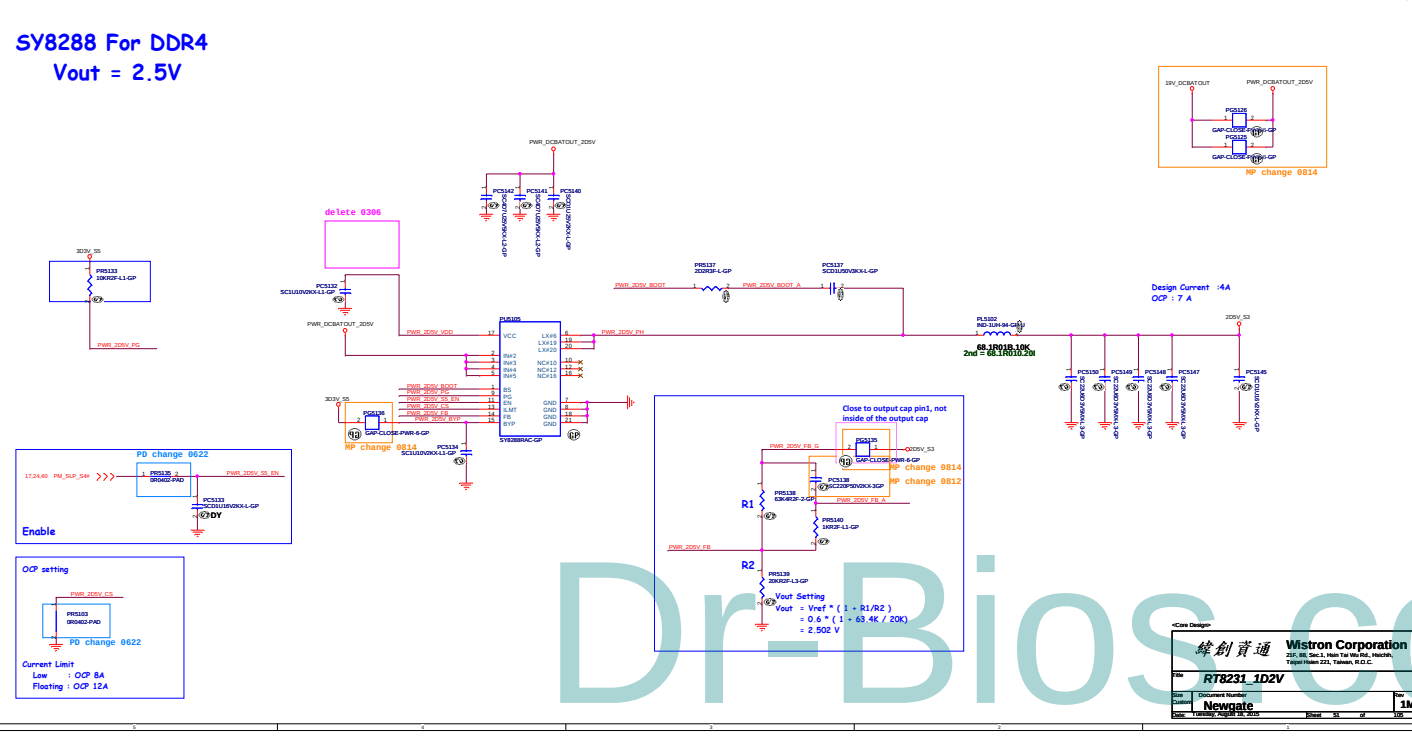
Title: SIC631CD_VCCSA

Size: A3 | Document Number: Newgate | Rev: 1M

Date: Tuesday, August 18, 2015 | Sheet 50 of 105



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off



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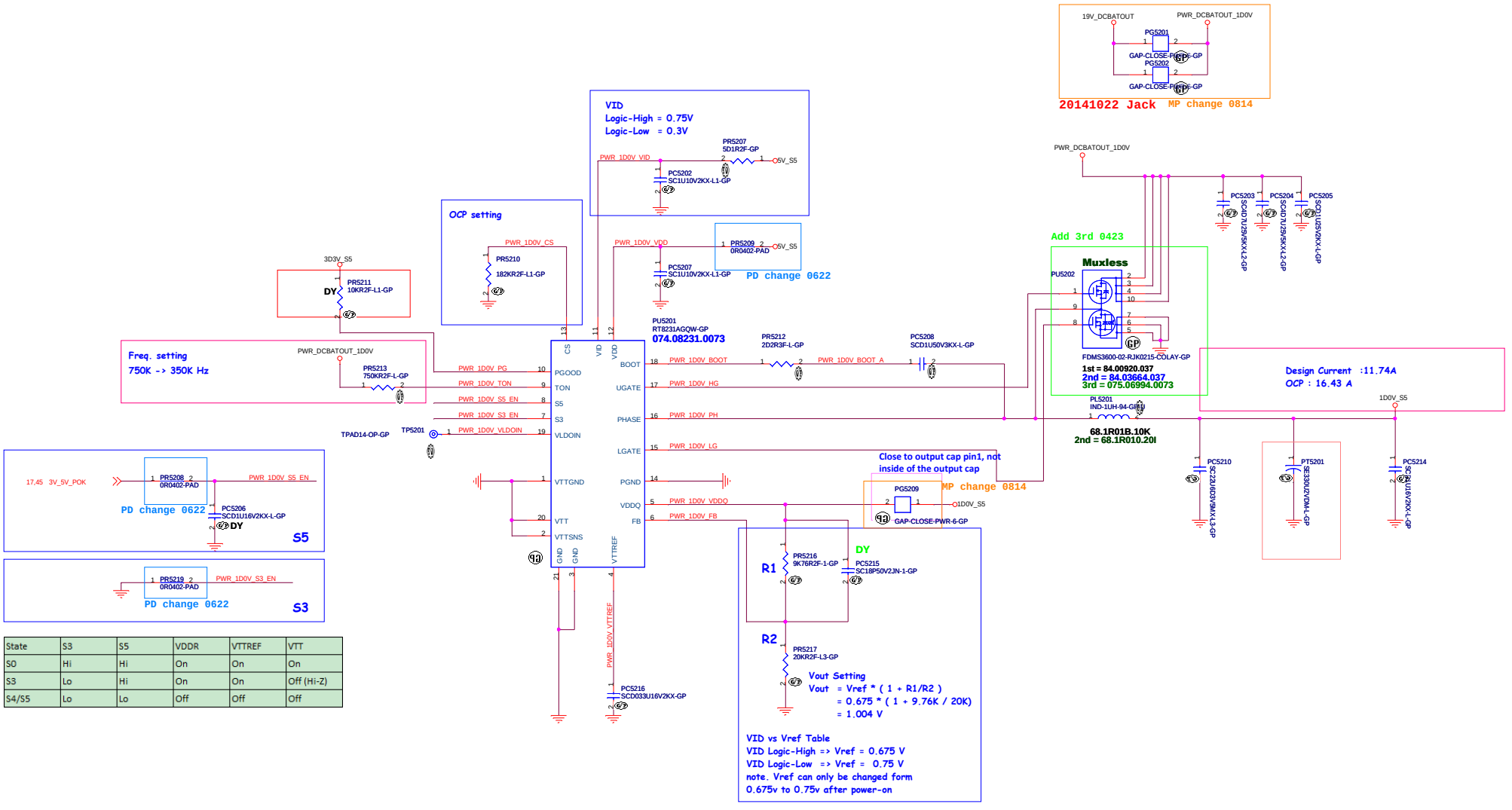
Title: RT8231_1D2V
Size: Custom | Document Number: Newgate | Rev: 1M
Date: Tuesday, August 18, 2015 | Sheet 51 of 105



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

<Core Design>

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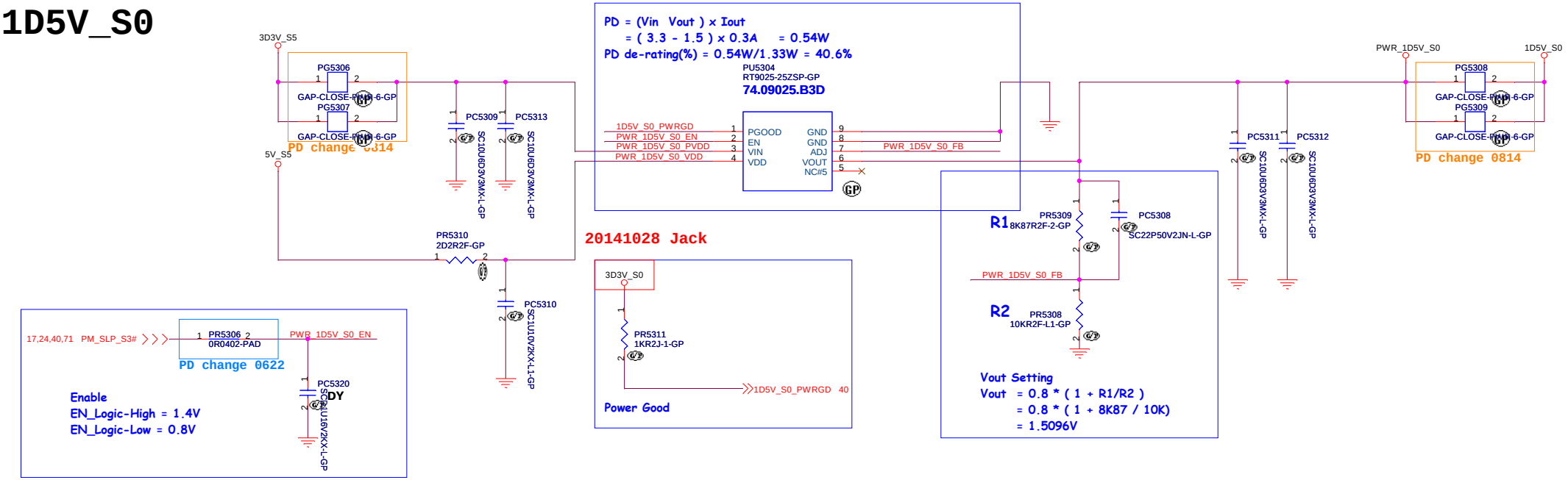
Title: RT8231_1D0V

Size: C | Document Number: Newgate | Rev: 1M

Date: Tuesday, August 18, 2015 | Sheet 52 of 105

1D5V_S0



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Title: RT9025_1D5V
Size: A3
Document Number: Newgate
Rev: 1M
Date: Tuesday, August 18, 2015
Sheet 53 of 105

eDP conn change by Royee 20150202

PD change 0622

Delete by Royee 20150202

PD change 0626

Inverter Power

20.K0809.040
2nd = 020.K0144.0040
3rd = 20.K0678.040

69.50007.A31
2nd = 69.50007.A41

AFTP TESTPOINT

MP change 0814

T-COM Power

74.22966.093
2nd = 74.03523.A73
3rd = 074.05016.0093

MP change 0902

Delete touch panel Power by Royee 20150202

Delete USB P8 and I2C0 by Royee 20150202

modify 0227

Swap0306

CHECK FAE

UN 0225

modify 0304 swap 0303

delete 0225

JJ 20150127

CHECK FAE

ADDR_EQ	3	3-level Input	I²C Target Address Select and EQ Configuration Input. If the I²C bus is used, this input setting selects the I²C target address, as described in Table 7. This input also configures the input EQ to the device, as described in Table 5.

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Title: EOPIO/EDRAM Power

Size: Custom | Document Number: Newgate | Rev: 1M

Date: Wednesday, September 02, 2015 | Sheet 55 of 105

SSID = VIDEO

HDMI Level Shifter & CONNECTOR

71 HDMI_CLK_CON_N3
71 HDMI_CLK_CON_P3
71 HDMI_DATA_CON_N0
71 HDMI_DATA_CON_P0
71 HDMI_DATA_CON_N1
71 HDMI_DATA_CON_P1
71 HDMI_DATA_CON_N2
71 HDMI_DATA_CON_P2

HDMI_CLK_CON_N3
HDMI_CLK_CON_P3
HDMI_DATA_CON_N0
HDMI_DATA_CON_P0
HDMI_DATA_CON_N1
HDMI_DATA_CON_P1
HDMI_DATA_CON_N2
HDMI_DATA_CON_P2

Change from 470 to 475 0204

R5701 475R2F-L1-GP
R5704 475R2F-L1-GP
R5706 475R2F-L1-GP
R5707 475R2F-L1-GP
R5709 475R2F-L1-GP
R5710 475R2F-L1-GP
R5711 475R2F-L1-GP
R5708 475R2F-L1-GP

HDMI_PLL_GND

Change TBT 0209

3D3V_S0

Q5702
2N7002K-2-GP
84.2N702.J31
2nd = 84.2N702.031
3rd = 84.2N702.W31

5V_S0

D5701
BAW56-5-GP
83.00056.Q11
2nd = 83.00056.R11

5V_DDC_HDMI1
5V_DDC_HDMI2

RN5701
SRN2K2J-5-GP

3D3V_S0

71 TBT_HDMI_DDC_CLK
71 TBT_HDMI_DDC_DATA

Q5703
2N7002KDW-GP
84.2N702.A3F
2nd = 75.00601.07C
3rd = 075.01660.007C

HDMI_CLK_CON
HDMI_DATA_CON

Change TBT 0209

3D3V_S0

R5717
1MR2F-L-GP

Q5701
2N7002K-2-GP
84.2N702.J31
2nd = 84.2N702.031
3rd = 84.2N702.W31

71 TBT_SRC_HPD

HDMI_DET_CON

R5718
20KR2F-L3-GP

HDMI_CLK_CON_N3
ER5701 180R2J-1-GP DY
HDMI_CLK_CON_P3

HDMI_DATA_CON_N0
ER5702 180R2J-1-GP DY
HDMI_DATA_CON_P0

HDMI_DATA_CON_N1
ER5703 180R2J-1-GP DY
HDMI_DATA_CON_P1

HDMI_DATA_CON_N2
ER5704 180R2J-1-GP DY
HDMI_DATA_CON_P2

5V_S0
F5702
POLYSW-1D1A6V-9-GP-U
5V_HDMI_S0

C5702
SCD1U25V2KX-L-GP

HDMI CONN

HDMI1

+5V_POWER
TMDS_DATA0+
TMDS_DATA0-
TMDS_DATA1+
TMDS_DATA1-
TMDS_DATA2+
TMDS_DATA2-
TMDS_DATA0_SHIELD
TMDS_DATA1_SHIELD
TMDS_DATA2_SHIELD
TMDS_CLOCK_SHIELD
TMDS_CLOCK+
TMDS_CLOCK-
SCL
SDA
CEC
DDC/CEC_GROUNG
HOT_PLUG_DETECT
RESERVED#14
GND
GND
GND
GND
HDMI (A_Type)

HDMI_DATA_CON_P0
HDMI_DATA_CON_N0
HDMI_DATA_CON_P1
HDMI_DATA_CON_N1
HDMI_DATA_CON_P2
HDMI_DATA_CON_N2
HDMI_CLK_CON_P3
HDMI_CLK_CON_N3
HDMI_CLK_CON
HDMI_DATA_CON
HDMI_DET_CON

SKT-HDMI23-131-GP-U
022.10025.0091
2nd = 022.10025.0061

HDMI conn change by Royee 20150202
PD change 0624

<Core Design>

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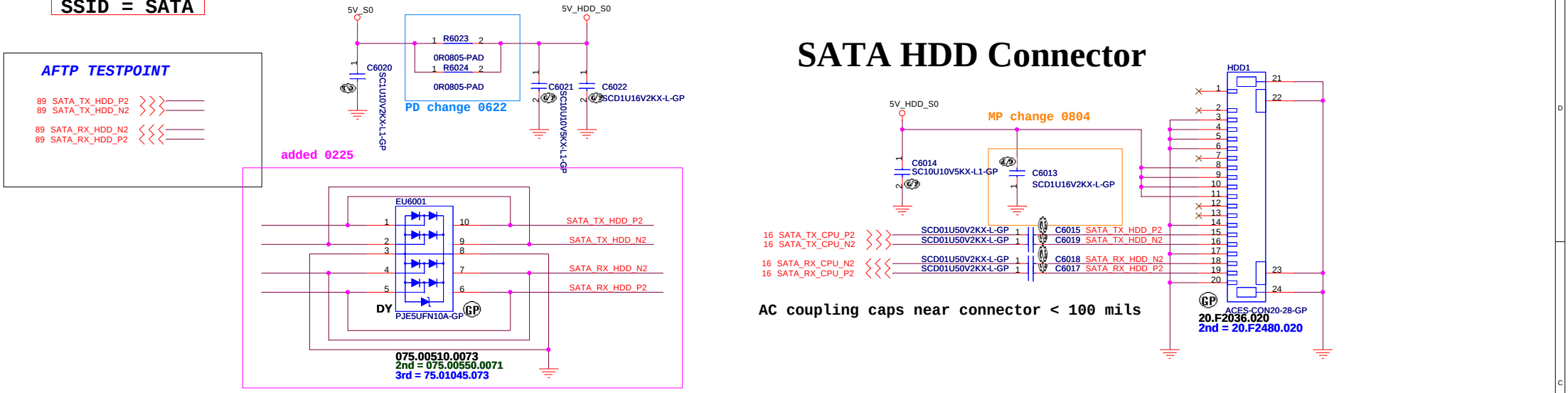
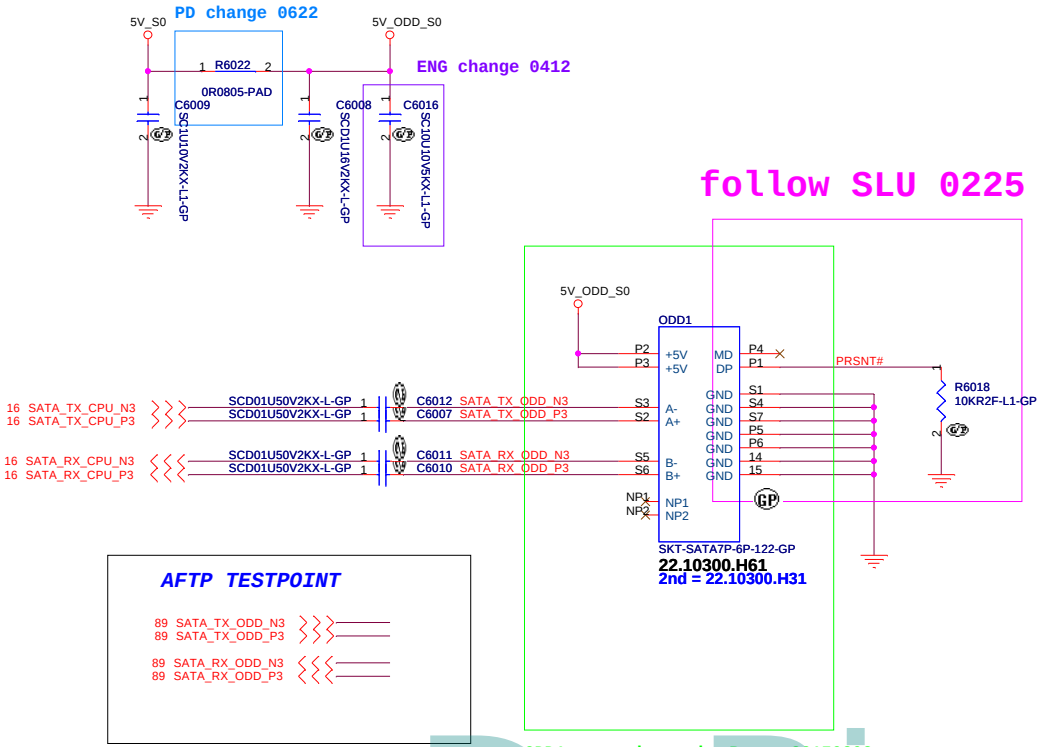
Title: HDMI Level Shifter/Conn
Size: Custom
Document Number: Newgate
Rev: 1M
Date: Tuesday, August 18, 2015
Sheet 57 of 105

SSID = SATA

SATA HDD Connector





PIN DEFINE	CONN	FFC
GND	P5/P6	20
GND		19
GND		18
ODD_DA	P4	17
NC		16
5V	P2/P3	15
5V		14
5V		13
5V		12
5V		11
5V		10
NC		9
PRSNT	P1	8
GND	S7	7
RXP	S6	6
RXN	S5	5
GND	S4	4
TXN	S3	3
TXP	S2	2
GND	S1	1

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Title: HDD/ODD

Size: A3 | Document Number: Newgate | Rev: 1M

Date: Tuesday, August 18, 2015 | Sheet 60 of 105

SSID = Wireless/ Wigig

NGFF Connector (802.11a/b/g/n)

WLAN conn change by Royee 20150202

PD change 0622

3D3V_S0 — R6105 0R0805-PAD — 3D3V_IOAC

modify 0302

3D3V_IOAC

Delete WIGIG 0204

PD change 0622

24 WIFI_RF_EN
24,89 BLUETOOTH_EN
14,24,31,63,68,71,89,91 PLT_RST#

R6101 1KR2J-L2-GP WIFI_RF_EN_CON
R6102 0R0402-PAD WLAN_RST#

ENG delete 0412

24 E51_RXD
24 E51_TXD

R6116 0R0402-PAD E51_RXD_R
R6117 0R0402-PAD E51_TXD_R

PD change 0622

WLAN1

76	76	77	77
74	3_3VAUX	GND	75
72	3_3VAUX	RESERVED#73	73
70	RESERVED#70	RESERVED#71	71
68	RESERVED#68	GND	69
66	RESERVED#66	RESERVED#67/2ND_LANE_PERN1	67
64	GPIO0_NFC_RESET#/MGPIO7	RESERVED#65/2ND_LANE_PERP1	65
62	NFC_I2C_IRQ/MGPIO5	GND	63
60	NFC_I2C_SM_CLK	RESERVED#61/2ND_LANE_PETN1	61
58	NFC_I2C_SM_DATA	RESERVED#59/2ND_LANE_PETP1	59
56	W_DISABLE#1	GND	57
54	RESERVED#54/W_DISABLE#2	PEWAKE#	55
52	PERST0#	CLKREQ0#	53
50	SUSCLK_32KHZ	GND	51
48	COEX1	REFCLKN0	49
46	COEX2	REFCLKP0	47
44	COEX3	GND	45
42	CLINK_CLK	PERN0	43
40	CLINK_DATA	PERP0	41
38	CLINK_RESET	GND	39
36	UART_CTS	PETN0	37
34	UART_RTS	PETP0	35
32	UART_TX	GND	33
22	UART_RX	SDIO_RESET	23
20	UART_WAKE	SDIO_WAKE	21
18	GND	SDIO_DAT3	19
16	LED#2	SDIO_DAT2	17
14	PCM_OUT	SDIO_DAT1	15
12	PCM_IN	SDIO_DAT0	13
10	PCM_SYNC	SDIO_CMD	11
8	PCM_CLK	SDIO_CLK	9
6	LED#1	GND	7
4	3_3VAUX	USB_D-	5
2	3_3VAUX	USB_D+	3
		GND	1
NP2	NP2	NP1	NP1

NGFF_KEY_E_75P

SKT-MINI75P-8-GP

062.10007.0241
2nd = 062.10007.0511
3rd = 062.10007.0291
4th = 062.10007.0371

Delete WIGIG 0204

PD change 0622

PCIE_WAKE# WLAN — R6107 0R0402-PAD

PCIE_WAKE# 17,31,63,71
WLAN_CLKREQ_CPU# 18,89

WLAN_CLK_CPU# 18,89
WLAN_CLK_CPU 18,89

PCIE_RX_PCH_N3 15,89
PCIE_RX_PCH_P3 15,89

PCIE_TX_CON_N3 — C6105 SCD22U10V2KX-L1-GP — PCIE_TX_PCH_N3 15
PCIE_TX_CON_P3 — C6106 SCD22U10V2KX-L1-GP — PCIE_TX_PCH_P3 15

USB_PCH_PN7 15,89
USB_PCH_PP7 15,89

3D3V_IOAC

C8101 SCD1U16V2KX-L-GP
C8102 SCD1U6D3V3MX-L-GP
C8103 SCD1U16V2KX-L-GP

UN 0225

AFTP TESTPOINT

PCIE_WAKE#_WLAN 89
WLAN_CLKREQ_CPU# 18,89

WLAN_CLK_CPU# 18,89
WLAN_CLK_CPU 18,89

PCIE_RX_PCH_N3 15,89
PCIE_RX_PCH_P3 15,89

PCIE_TX_CON_N3 89
PCIE_TX_CON_P3 89

USB_PCH_PN7 15,89
USB_PCH_PP7 15,89

WIFI_RF_EN_CON 89
BLUETOOTH_EN 24,89
WLAN_RST# 89

E51_RXD_R 89
E51_TXD_R 89

<Core Design>

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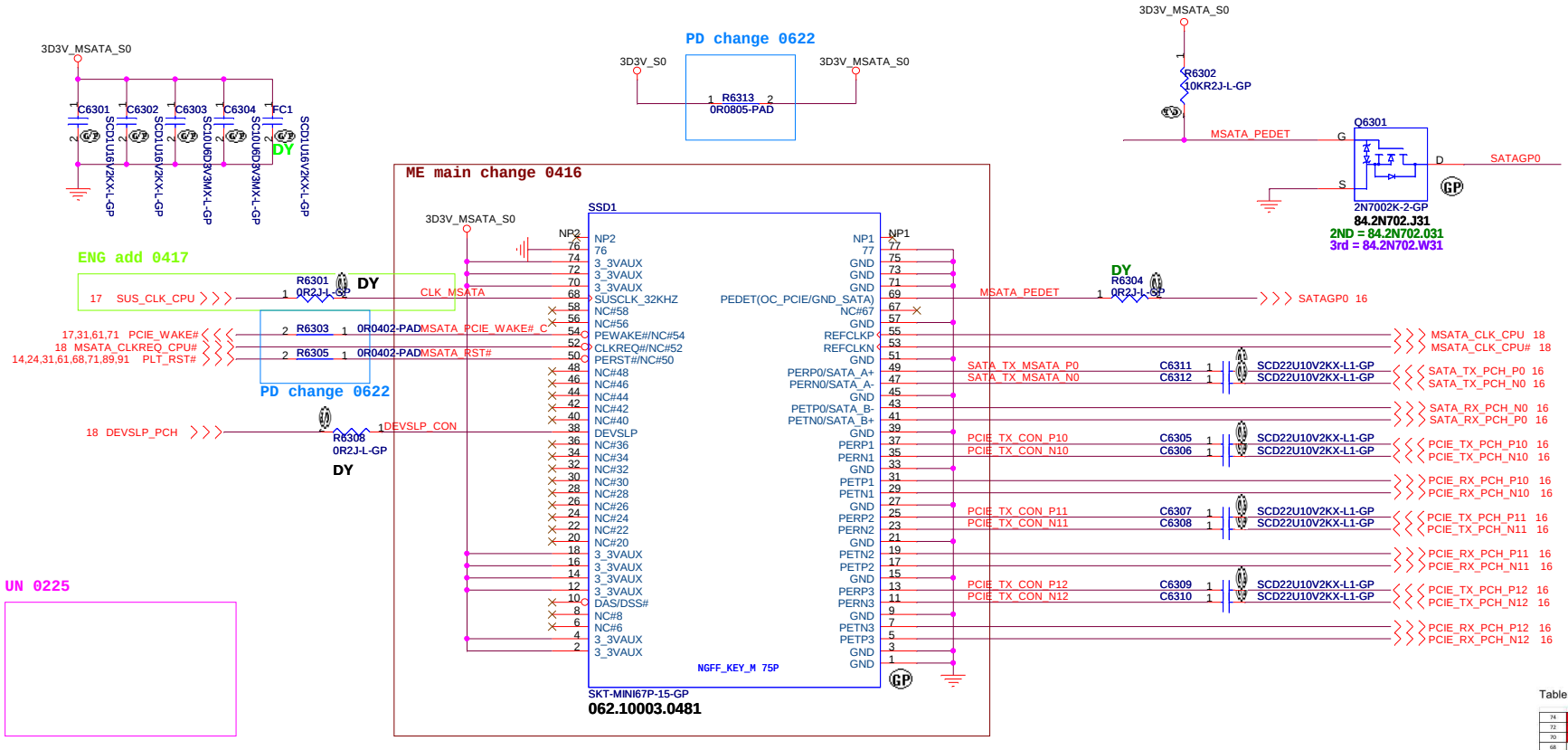
Title: Mini card-WLAN

Size: Custom | Document Number: Newgate | Rev: 1M

Date: Tuesday, August 18, 2015 | Sheet 61 of 105

Mini Card Connector (NGFF m-SATA)

SSID = m-SATA



UN 0225

Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

Table 34-5. SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[2]	None	None[3]

Notes:

1. Design Constraint: For PCIe only application, please refer to the PCIe guidelines for details.
2. Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the 10 nF capacitor on Rx can be removed if DC coupled ODDs / devices are NOT used.
3. Design Constraint: For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
4. Design Constraint: For PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
5. Design Constraints, Required: Refer to the Chapter 3, "General Differential Design Guidelines"" along with the additional guidelines in this section for all design optimization guidelines.

<Core Design>

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Title: **SSD-NGFF**

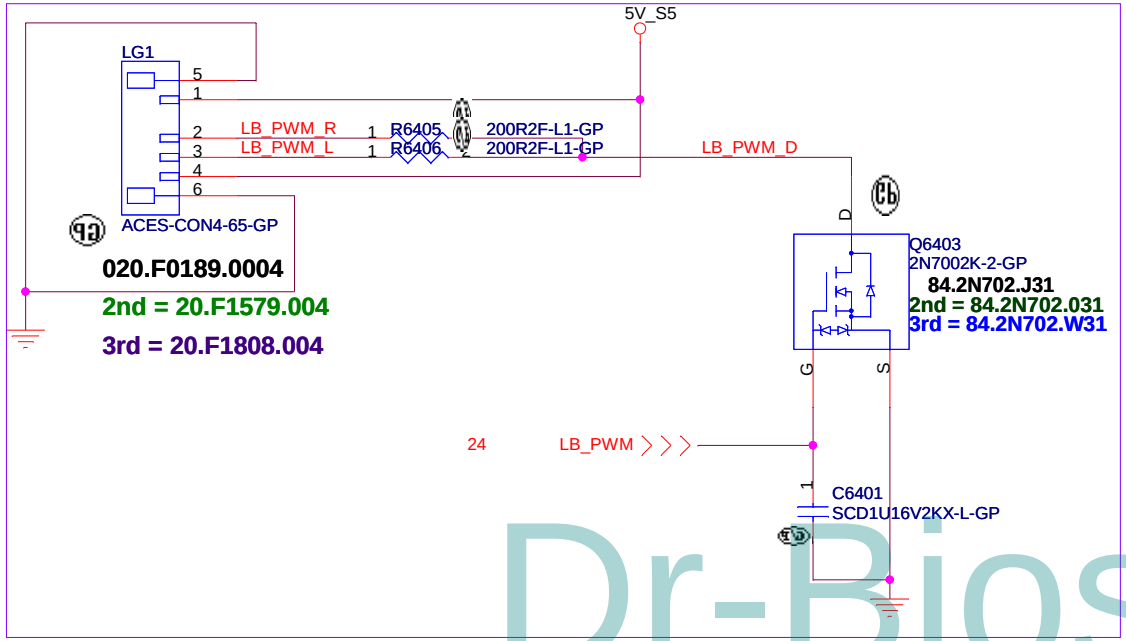
Size: A3 | Document Number: **Newgate** | Rev: **1M**

Date: Tuesday, August 18, 2015 | Sheet 63 of 105

SSID = User.Interface

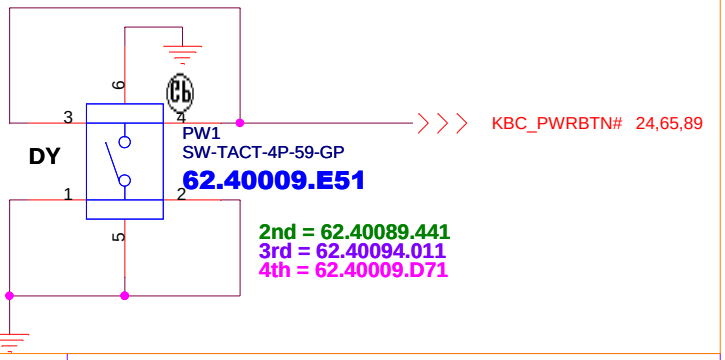
ENG change 0412

LG1 conn ENG change 0412

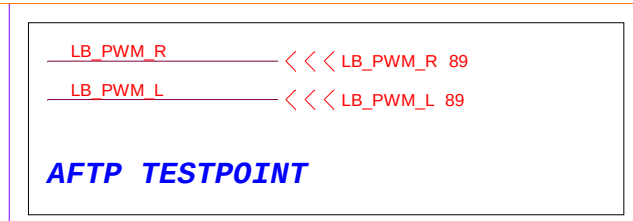


MP change 0804

Power Button



ENG change 0412

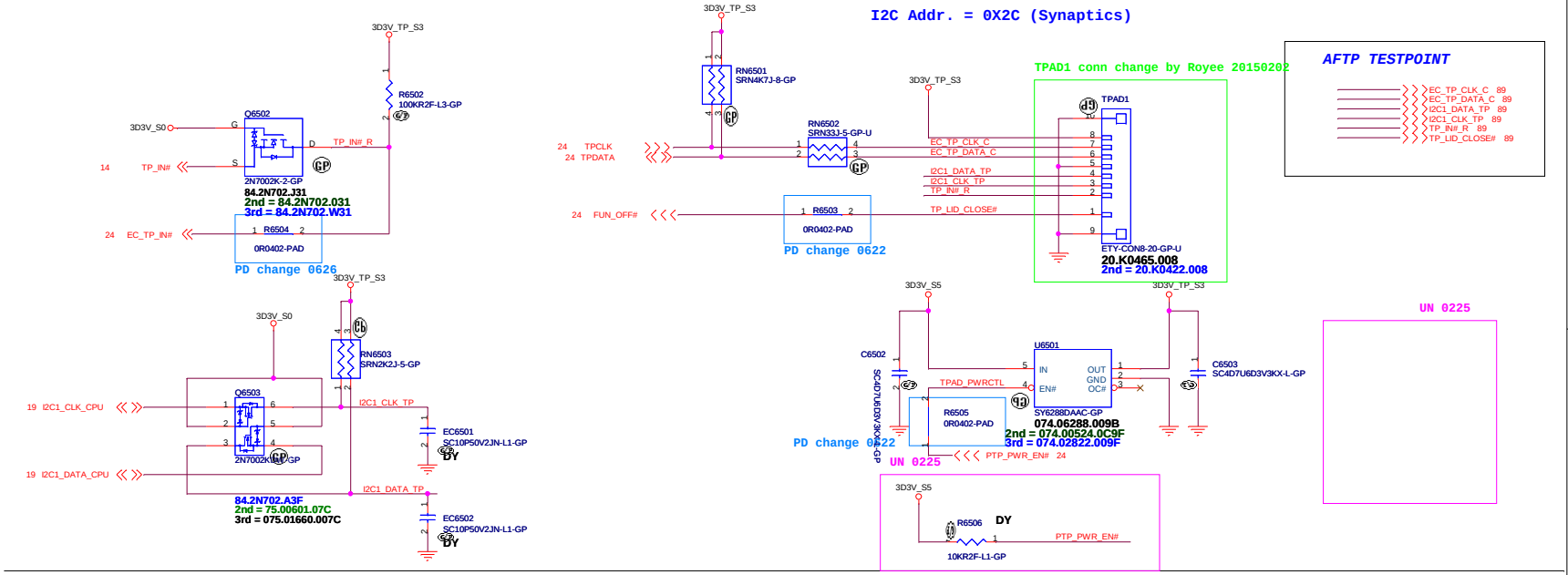


<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: LED Bard/Power Button		
Size: A4	Document Number: Newgate	Rev: 1M
Date: Tuesday, August 18, 2015	Sheet 64 of 105	

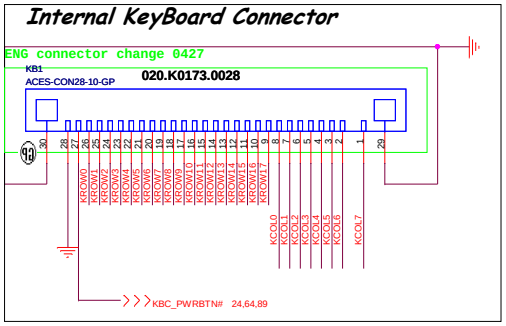
Precision Touch Pad

I2C Addr. = 0X2C (Synaptics)

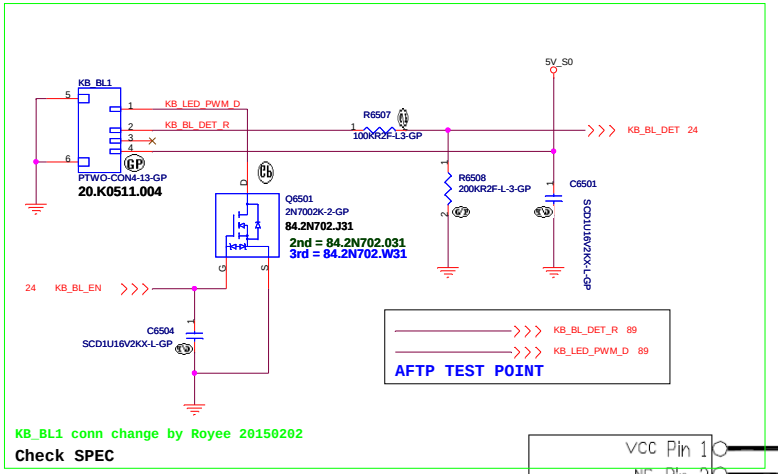


UN 0225

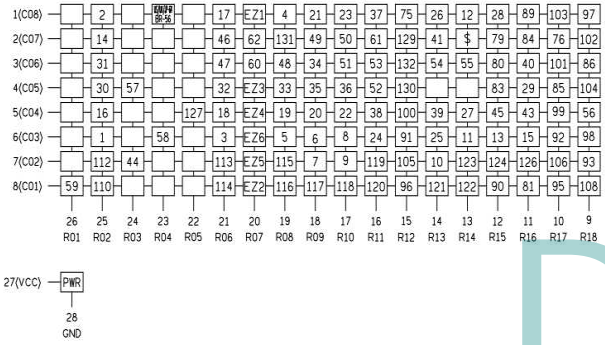
Internal KeyBoard Connector

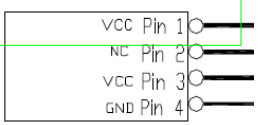


CHECK WITH SPEC



KROW[0..17] 24,89
KCOL[0..7] 24,89





UN 0225

<Core Design>

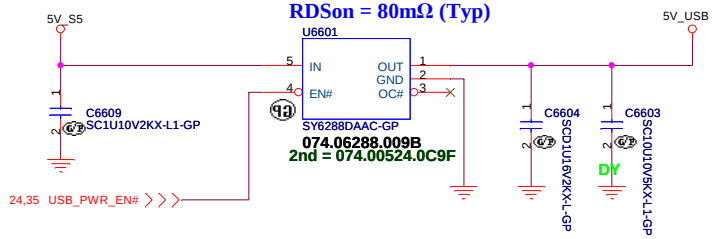
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: LED Bard / Power Button

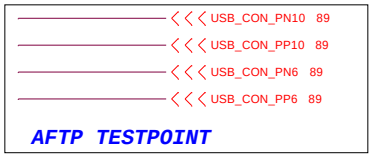
Size: Custom | Document Number: Newgate | Rev: 1M

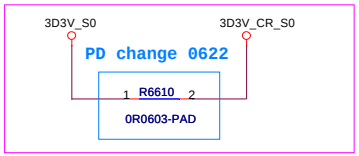
Date: Tuesday, August 18, 2015 | Sheet 65 of 105

Low Active 2A
RDSon = 80mΩ (Typ)

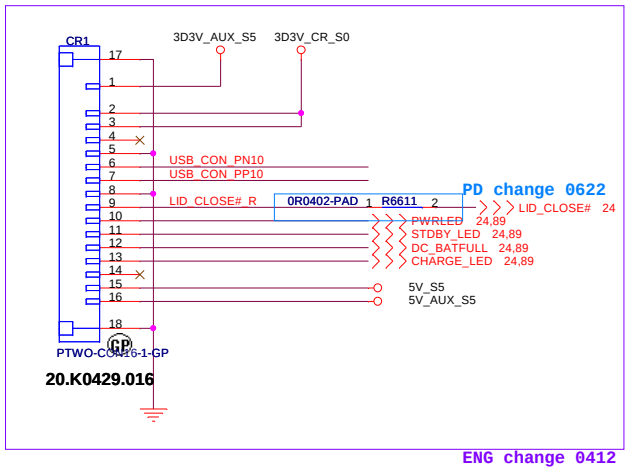


Added 0303

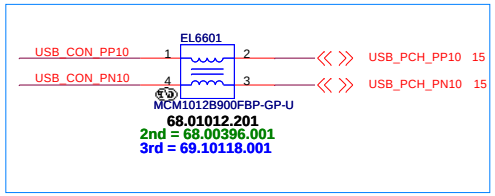




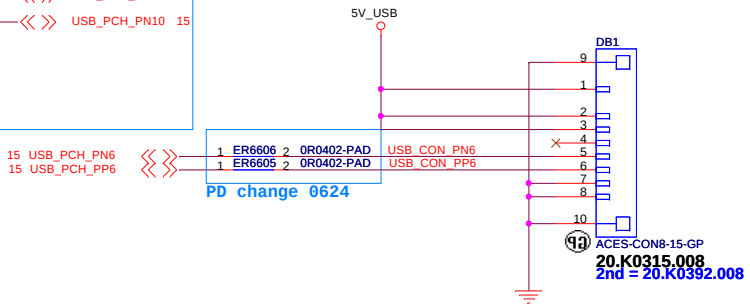
Card Reader

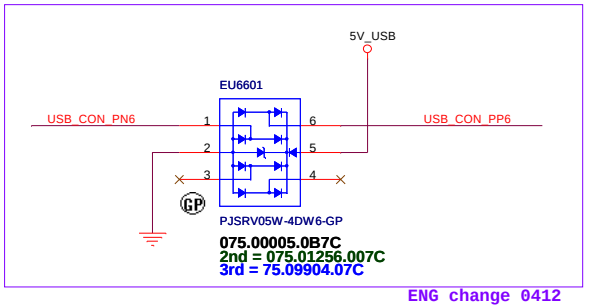


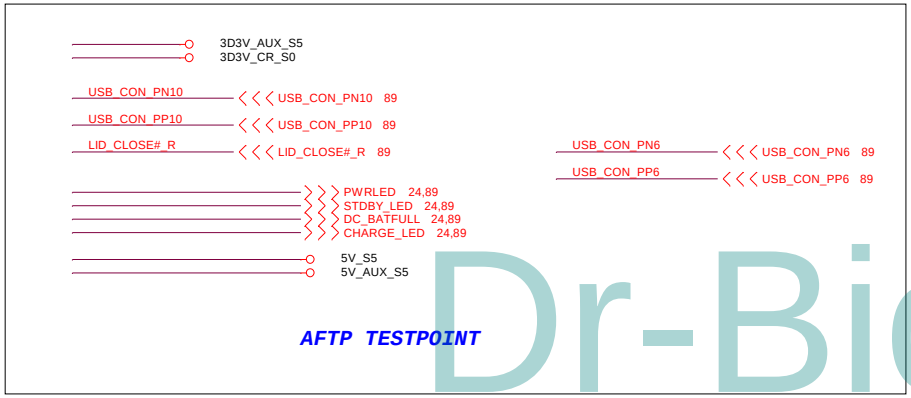
PD change 0626



USB2.0





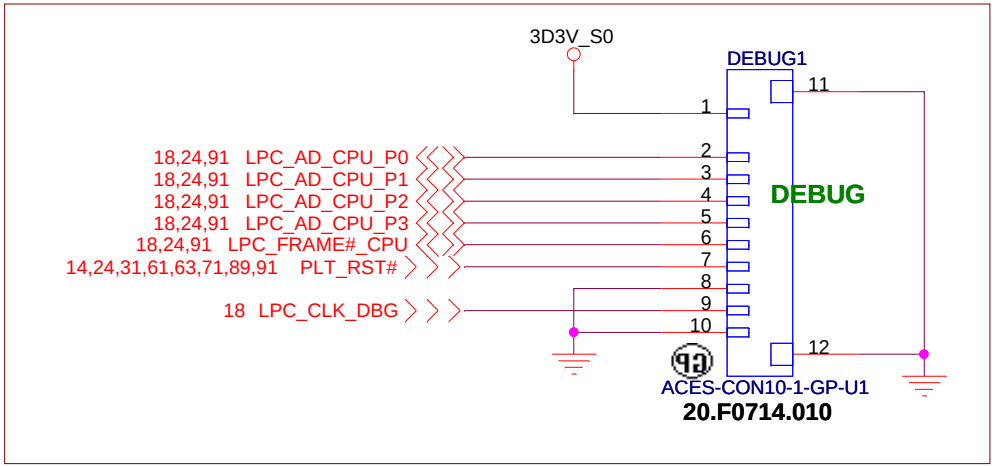


<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board Connector
Size: A3
Document Number: Newgate
Rev: 1M
Date: Tuesday, August 18, 2015
Sheet 66 of 105

ENG change 0416



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Debug connector***

Size	Document Number	Rev
A	**Newgate**	**1M**

Date: Tuesday, August 18, 2015 Sheet 68 of 105

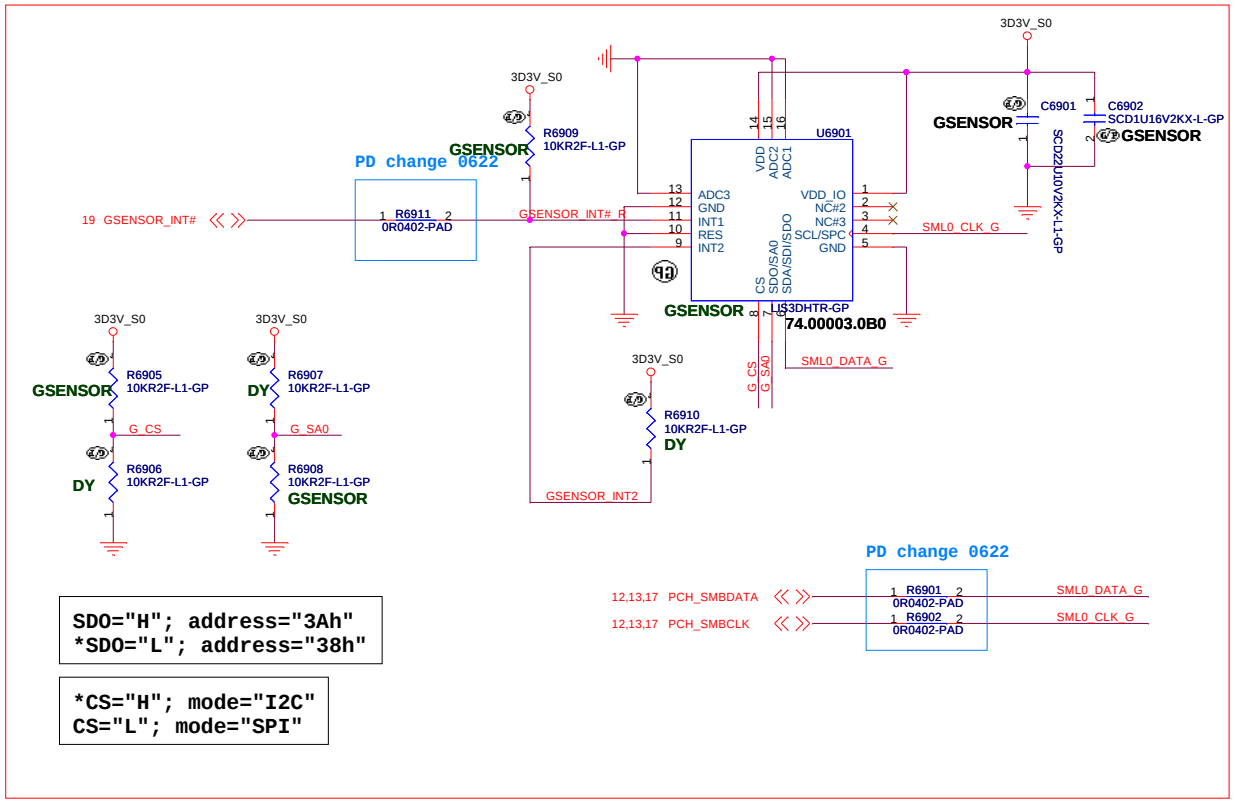
SSID = User.Interface

G Sensor

Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

CHECK WITH MICK

change 0225



SDO="H"; address="3Ah"
*SDO="L"; address="38h"

*CS="H"; mode="I2C"
CS="L"; mode="SPI"

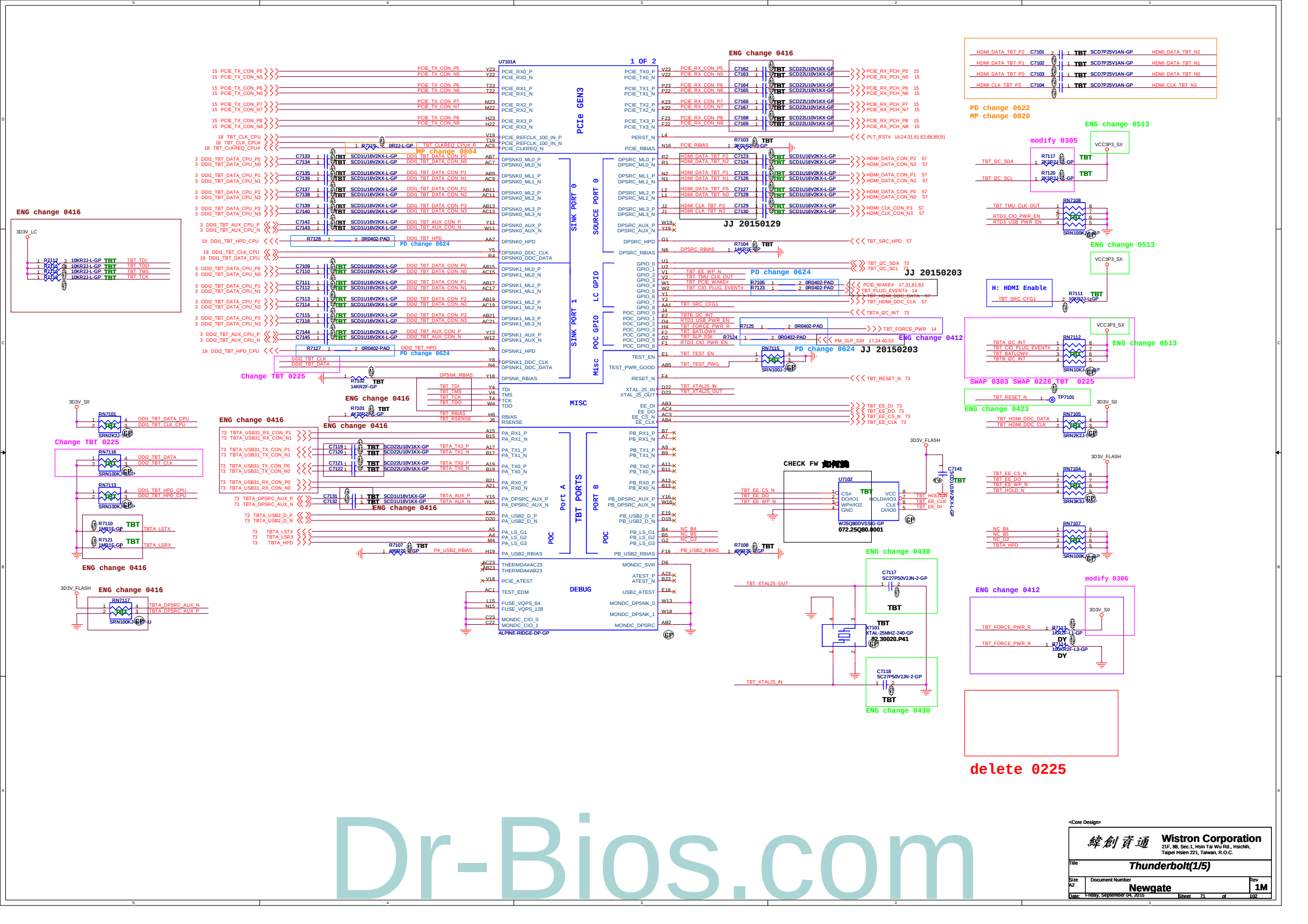
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: G-SENSOR

Size: A3 | Document Number: Newgate | Rev: 1M

Date: Tuesday, August 18, 2015 | Sheet 69 of 105

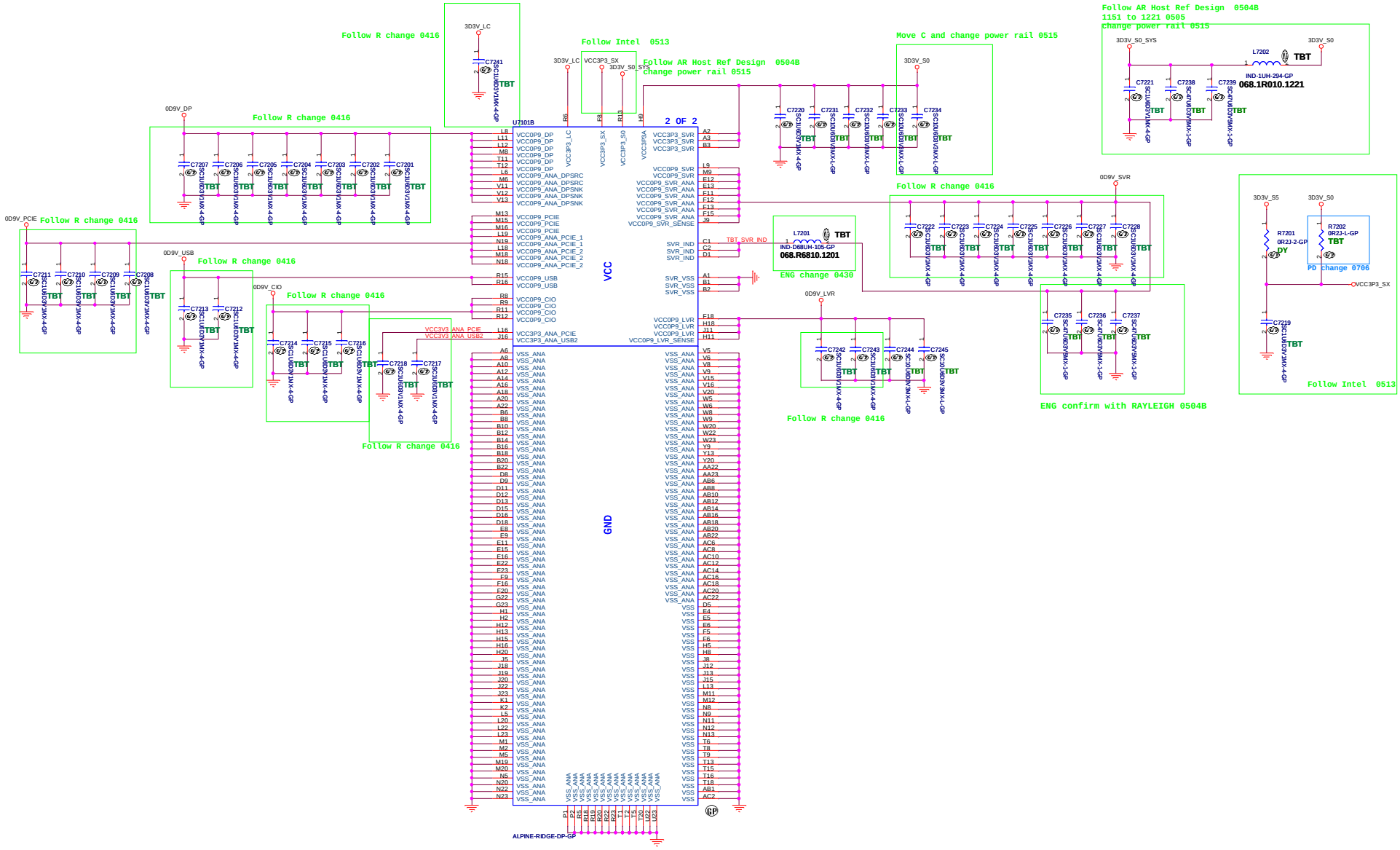


<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thunderbolt(1/5)

Size: A2 | Document Number: Newgate | Rev: 1M

Date: Friday, September 04, 2015 | Sheet 71 of 102



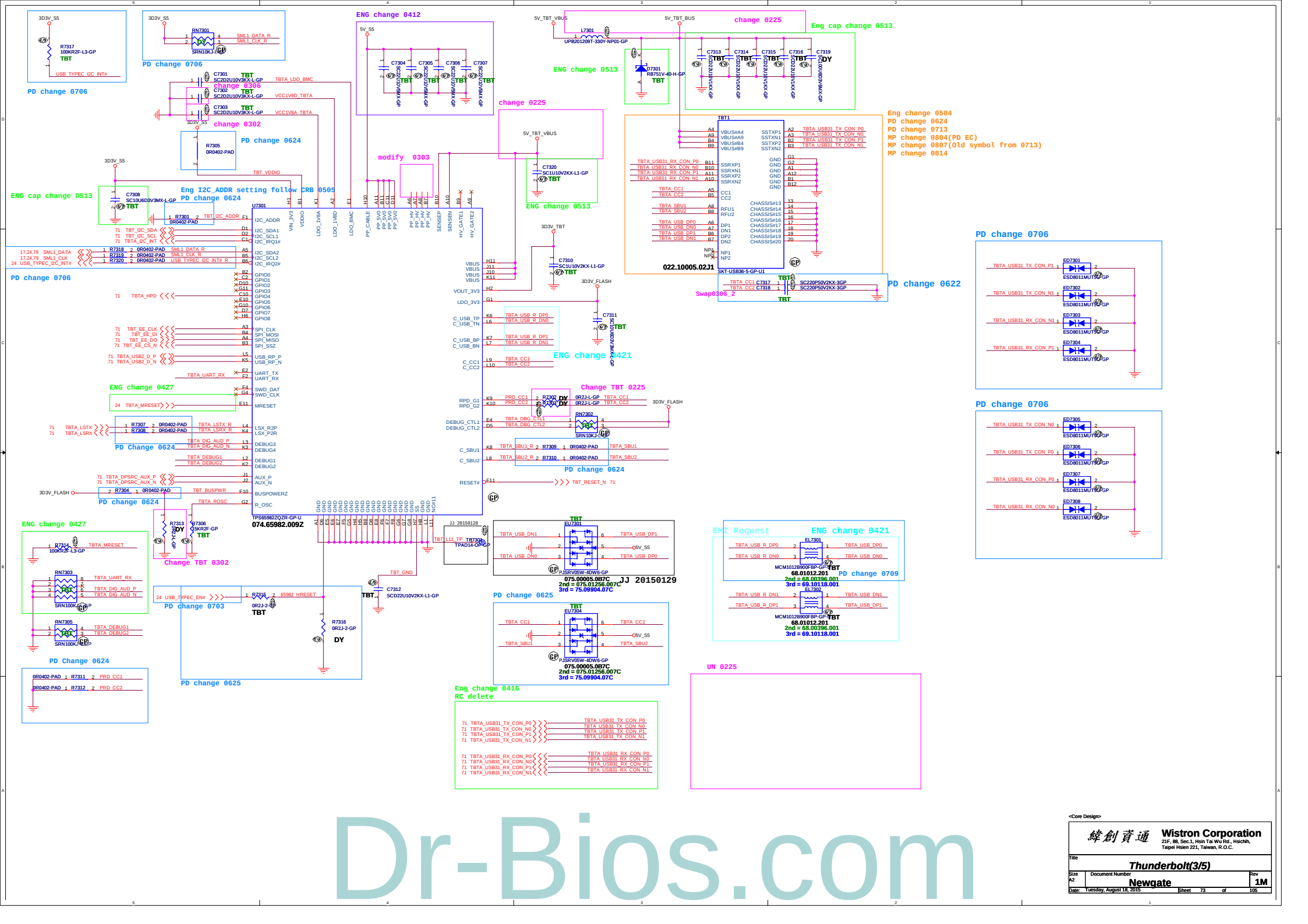
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thunderbolt(2/5)

Size: A2 | Document Number: Newgate | Rev: 1M

Date: Wednesday, August 12, 2015 | Sheet 72 of 105


ENG change 0412
change 0225
Eng cap change 0513
ENG change 0513
Eng change 0504
PD change 0624
PD change 0713
MP change 0804(PD EC)
MP change 0807(Old symbol from 0713)
MP change 0814
PD change 0706
change 0306
change 0302
PD change 0624
modify 0303
Eng I2C_ADDR setting follow CRB 0505
PD change 0624
ENG change 0513
PD change 0622
Swap0306_2
022.10005.02J1
SKT-USB36-5-GP-U1
ENG change 0421
Change TBT 0225
PD change 0624
ENG change 0427
PD Change 0624
Change TBT 0302
PD change 0703
PD change 0625
ENG change 0427
PD Change 0624
PD change 0625
ENG change 0421
PD change 0709
EMI Request
UN 0225
Eng change 0416
RC delete
U7301
TPS65982ZQZR-GP-U
074.65982.009Z
EU7301
EU7304
EL7301
EL7302
075.00005.0B7C
2nd = 075.01256.007C
3rd = 75.09904.07C
JJ 20150129
68.01012.201
2nd = 68.00396.001
3rd = 69.10118.001
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Thunderbolt(3/5)
Newgate
1M
Tuesday, August 18, 2015
73
105

UN 0225

14,79 DGPU_HOLD_RST# → R7603 0R2J-L-GP → VGA_RST#

NON_GC6

3D3V_AON_S0 → R7604 10KR2J-L-GP Muxless

Q7601 2N7002K-2-GP

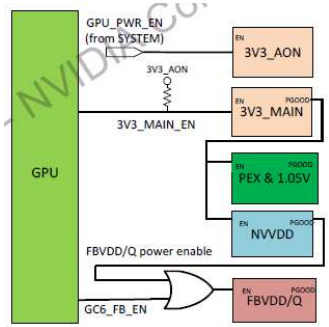
18 PEG_CLKREQ_CPU# → D

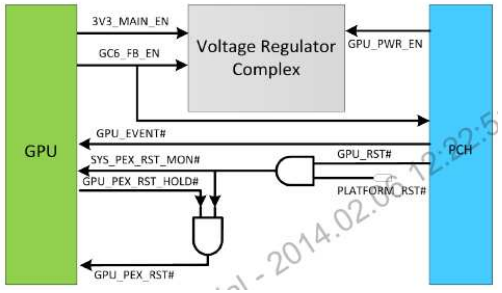
84.2N702.J31
2ND = 84.2N702.031
3rd = 84.2N702.W31

S → 79 VGA_RST#

PEG_CLKREQ_dGPU# AK12

18 PEG_CLK_CPU
18 PEG_CLK_CPU#





VGA1A — 1 OF 17

3 PEG_RX_CPU_P0 / 3 PEG_RX_CPU_N0	C7601 / C7606 SCD22U10V2KX-L1-GP Muxless	PEG_RX_CON_P0 / PEG_RX_CON_N0	AK14 / AJ14
3 PEG_TX_CON_P0 / 3 PEG_TX_CON_N0			AN12 / AM12
3 PEG_RX_CPU_P1 / 3 PEG_RX_CPU_N1	C7607 / C7608 SCD22U10V2KX-L1-GP Muxless	PEG_RX_CON_P1 / PEG_RX_CON_N1	AH14 / AG14
3 PEG_TX_CON_P1 / 3 PEG_TX_CON_N1			AN14 / AM14
3 PEG_RX_CPU_P2 / 3 PEG_RX_CPU_N2	C7613 / C7614 SCD22U10V2KX-L1-GP Muxless	PEG_RX_CON_P2 / PEG_RX_CON_N2	AK15 / AJ15
3 PEG_TX_CON_P2 / 3 PEG_TX_CON_N2			AP14 / AP15
3 PEG_RX_CPU_P3 / 3 PEG_RX_CPU_N3	C7615 / C7616 SCD22U10V2KX-L1-GP Muxless	PEG_RX_CON_P3 / PEG_RX_CON_N3	AL16 / AK16
3 PEG_TX_CON_P3 / 3 PEG_TX_CON_N3			AN15 / AM15
3 PEG_RX_CPU_P4 / 3 PEG_RX_CPU_N4	C7617 / C7618 SCD22U10V2KX-L1-GP Muxless	PEG_RX_CON_P4 / PEG_RX_CON_N4	AK17 / AJ17
3 PEG_TX_CON_P4 / 3 PEG_TX_CON_N4			AN17 / AM17
3 PEG_RX_CPU_P5 / 3 PEG_RX_CPU_N5	C7619 / C7620 SCD22U10V2KX-L1-GP Muxless	PEG_RX_CON_P5 / PEG_RX_CON_N5	AH17 / AG17
3 PEG_TX_CON_P5 / 3 PEG_TX_CON_N5			AP17 / AP18
3 PEG_RX_CPU_P6 / 3 PEG_RX_CPU_N6	C7621 / C7622 SCD22U10V2KX-L1-GP Muxless	PEG_RX_CON_P6 / PEG_RX_CON_N6	AK18 / AJ18
3 PEG_TX_CON_P6 / 3 PEG_TX_CON_N6			AN18 / AM18
3 PEG_RX_CPU_P7 / 3 PEG_RX_CPU_N7	C7625 / C7626 SCD22U10V2KX-L1-GP Muxless	PEG_RX_CON_P7 / PEG_RX_CON_N7	AL19 / AK19
3 PEG_TX_CON_P7 / 3 PEG_TX_CON_N7			AN20 / AM20
3 PEG_RX_CPU_P8 / 3 PEG_RX_CPU_N8	C7627 / C7628 SCD22U10V2KX-L1-GP Muxless	PEG_RX_CON_P8 / PEG_RX_CON_N8	AK20 / AJ20
3 PEG_TX_CON_P8 / 3 PEG_TX_CON_N8			AP20 / AP21
3 PEG_RX_CPU_P9 / 3 PEG_RX_CPU_N9	C7629 / C7630 SCD22U10V2KX-L1-GP Muxless	PEG_RX_CON_P9 / PEG_RX_CON_N9	AH20 / AG20
3 PEG_TX_CON_P9 / 3 PEG_TX_CON_N9			AN21 / AM21
3 PEG_RX_CPU_P10 / 3 PEG_RX_CPU_N10	C7631 / C7632 SCD22U10V2KX-L1-GP Muxless	PEG_RX_CON_P10 / PEG_RX_CON_N10	AK21 / AJ21
3 PEG_TX_CON_P10 / 3 PEG_TX_CON_N10			AN23 / AM23
3 PEG_RX_CPU_P11 / 3 PEG_RX_CPU_N11	C7633 / C7634 SCD22U10V2KX-L1-GP Muxless	PEG_RX_CON_P11 / PEG_RX_CON_N11	AL22 / AK22
3 PEG_TX_CON_P11 / 3 PEG_TX_CON_N11			AP23 / AP24
3 PEG_RX_CPU_P12 / 3 PEG_RX_CPU_N12	C7635 / C7636 SCD22U10V2KX-L1-GP Muxless	PEG_RX_CON_P12 / PEG_RX_CON_N12	AK23 / AJ23
3 PEG_TX_CON_P12 / 3 PEG_TX_CON_N12			AN24 / AM24
3 PEG_RX_CPU_P13 / 3 PEG_RX_CPU_N13	C7637 / C7638 SCD22U10V2KX-L1-GP Muxless	PEG_RX_CON_P13 / PEG_RX_CON_N13	AH23 / AG23
3 PEG_TX_CON_P13 / 3 PEG_TX_CON_N13			AN26 / AM26
3 PEG_RX_CPU_P14 / 3 PEG_RX_CPU_N14	C7639 / C7640 SCD22U10V2KX-L1-GP Muxless	PEG_RX_CON_P14 / PEG_RX_CON_N14	AK24 / AJ24
3 PEG_TX_CON_P14 / 3 PEG_TX_CON_N14			AP26 / AP27
3 PEG_RX_CPU_P15 / 3 PEG_RX_CPU_N15	C7644 / C7645 SCD22U10V2KX-L1-GP Muxless	PEG_RX_CON_P15 / PEG_RX_CON_N15	AL25 / AK25
3 PEG_TX_CON_P15 / 3 PEG_TX_CON_N15			AN27 / AM27

VGA1A signals:

PEX_WAKE#	AJ11
PEX_RST#	AJ12
PEX_CLKREQ#	AK12
PEX_REFCLK	AL13
PEX_REFCLK#	AK13
PEX_TX0 / PEX_TX0#	AK14 / AJ14
PEX_RX0 / PEX_RX0#	AN12 / AM12
PEX_TX1 / PEX_TX1#	AH14 / AG14
PEX_RX1 / PEX_RX1#	AN14 / AM14
PEX_TX2 / PEX_TX2#	AK15 / AJ15
PEX_RX2 / PEX_RX2#	AP14 / AP15
PEX_TX3 / PEX_TX3#	AL16 / AK16
PEX_RX3 / PEX_RX3#	AN15 / AM15
PEX_TX4 / PEX_TX4#	AK17 / AJ17
PEX_RX4 / PEX_RX4#	AN17 / AM17
PEX_TX5 / PEX_TX5#	AH17 / AG17
PEX_RX5 / PEX_RX5#	AP17 / AP18
PEX_TX6 / PEX_TX6#	AK18 / AJ18
PEX_RX6 / PEX_RX6#	AN18 / AM18
PEX_TX7 / PEX_TX7#	AL19 / AK19
PEX_RX7 / PEX_RX7#	AN20 / AM20
PEX_TX8 / PEX_TX8#	AK20 / AJ20
PEX_RX8 / PEX_RX8#	AP20 / AP21
PEX_TX9 / PEX_TX9#	AH20 / AG20
PEX_RX9 / PEX_RX9#	AN21 / AM21
PEX_TX10 / PEX_TX10#	AK21 / AJ21
PEX_RX10 / PEX_RX10#	AN23 / AM23
PEX_TX11 / PEX_TX11#	AL22 / AK22
PEX_RX11 / PEX_RX11#	AP23 / AP24
PEX_TX12 / PEX_TX12#	AK23 / AJ23
PEX_RX12 / PEX_RX12#	AN24 / AM24
PEX_TX13 / PEX_TX13#	AH23 / AG23
PEX_RX13 / PEX_RX13#	AN26 / AM26
PEX_TX14 / PEX_TX14#	AK24 / AJ24
PEX_RX14 / PEX_RX14#	AP26 / AP27
PEX_TX15 / PEX_TX15#	AL25 / AK25
PEX_RX15 / PEX_RX15#	AN27 / AM27

N15P-GT-A2-GP

071.0N15P.000U
Muxless

PEX_IOVDD_1..6 AG19 AG21 AG22 AG24 AH21 AH25
PEX_IOVDDQ_1..14 AG13 AG15 AG16 AG18 AG25 AH15 AH18 AH26 AH27 AJ27 AK27 AL27 AM28 AN28

1D05V_VGA_S0

Muxless SC407U6D3V3KX-L1-GP C7602 / C7603 SCD1U10V2KX-L1-GP
Muxless SC10U6D3V3MX-L-GP C7604 / C7605
Muxless SC407U6D3V3KX-L1-GP C7609 / C7610 SCD1U10V2KX-L1-GP
Muxless SC10U6D3V3MX-L-GP C7611 / C7612

Place under GPU
Place near GPU

3D3V_AON_S0

PEX_PLL_HVDD AH12
PEX_SVDD_3V3 AG12

Muxless SC407U6D3V3KX-L1-GP C7623 / C7624 SCD1U10V2KX-L1-GP

Place near GPU

VDD_SENSE L4 → NVVDD_SENSE 85
GND_SENSE L5 → NVGND_SENSE 85

NC#P8 P8

DY
200R2F-L1-GP
PEX_TSTCLK_OUT AJ26 → VGAPEX_AJ26 → R7605
PEX_TSTCLK_OUT# AK26 → VGAPEX_AK26

Place near AG26

PEX_PLLVDD AG26

Muxless SC407U6D3V3KX-L1-GP C7641 / C7642 SCD1U10V2KX-L1-GP
Muxless SC10U6D3V3MX-L-GP C7643

Place near GPU

TESTMODE AK11 TESTMODE → R7606 10KR2J-L-GP Muxless

PEX_TERMP AP29 PEX_TERMP → R7607 2K49R2F-2-L-GP Muxless

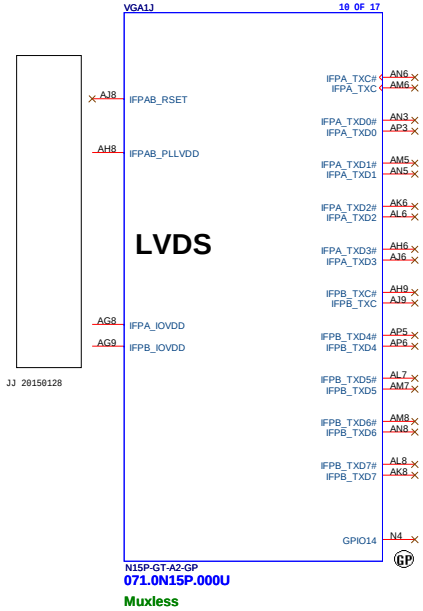
<Core Design>

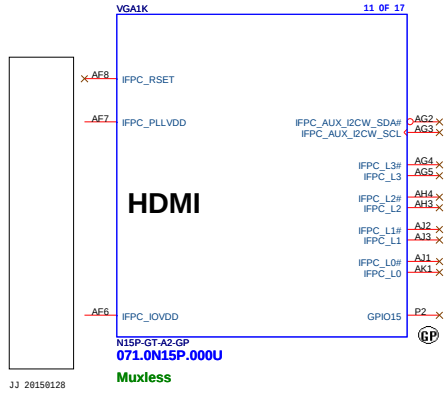
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

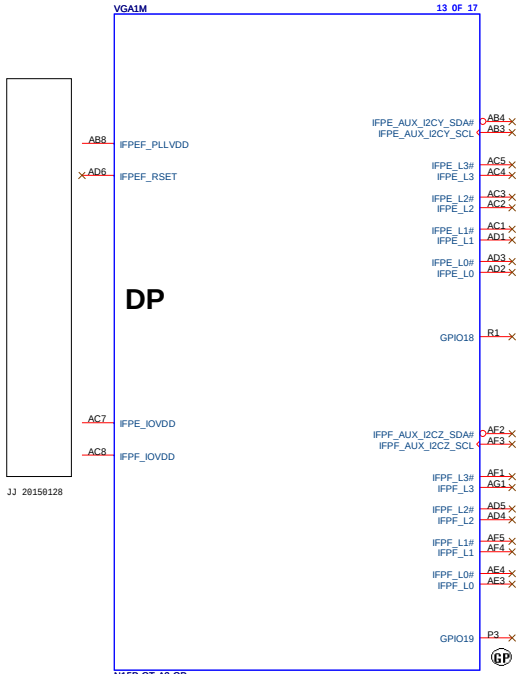
Title: GPU_840M_PEG (1/5)

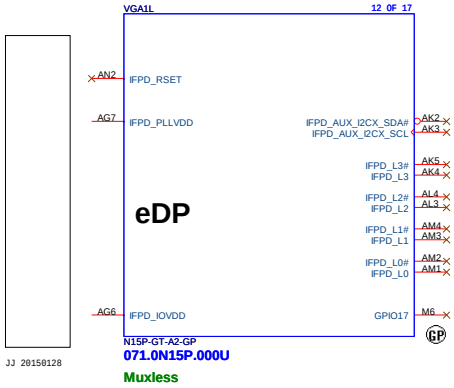
Size: Custom | Document Number: Newgate | Rev: 1M

Date: Tuesday, August 18, 2015 | Sheet 76 of 105









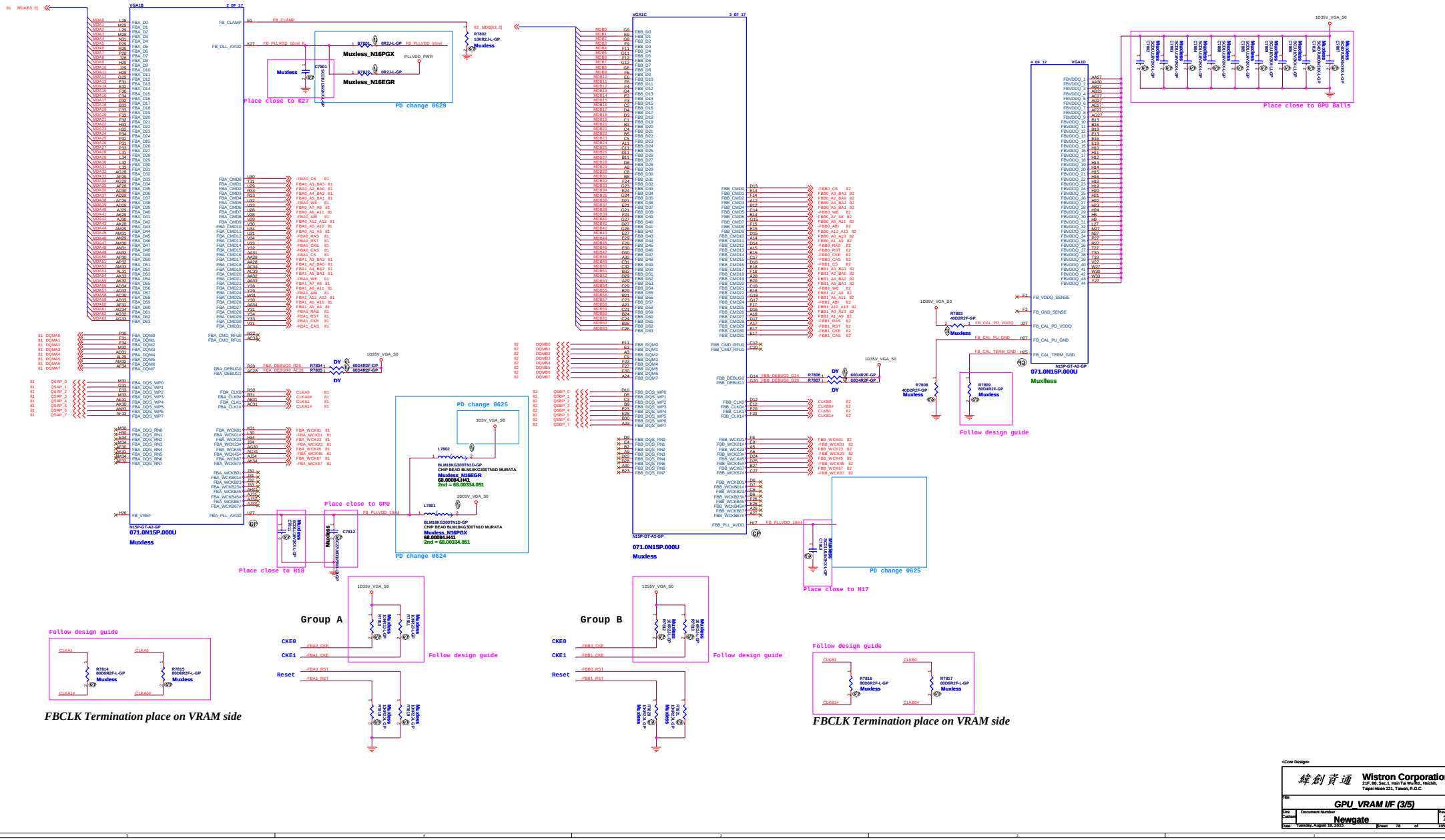
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_DIGITALOUT (2/5)

Size: Custom | Document Number: Newgate | Rev: 1M

Date: Tuesday, August 18, 2015 | Sheet 77 of 105


VGA1B
2 OF 17
VGA1C
3 OF 17
VGA1D
4 OF 17
N15P-GT-A2-GP
071.0N15P.000U
Muxless
Muxless_N16PGX
Muxless_N16EGR
PD change 0629
PD change 0625
PD change 0624
Place close to K27
Place close to GPU
Place close to H18
Place close to H17
Place close to GPU Balls
Follow design guide
Group A
Group B
CKE0
CKE1
Reset
FBCLK Termination place on VRAM side
Wistron Corporation
GPU_VRAM I/F (3/5)
Newgate
1M
Tuesday, August 18, 2015

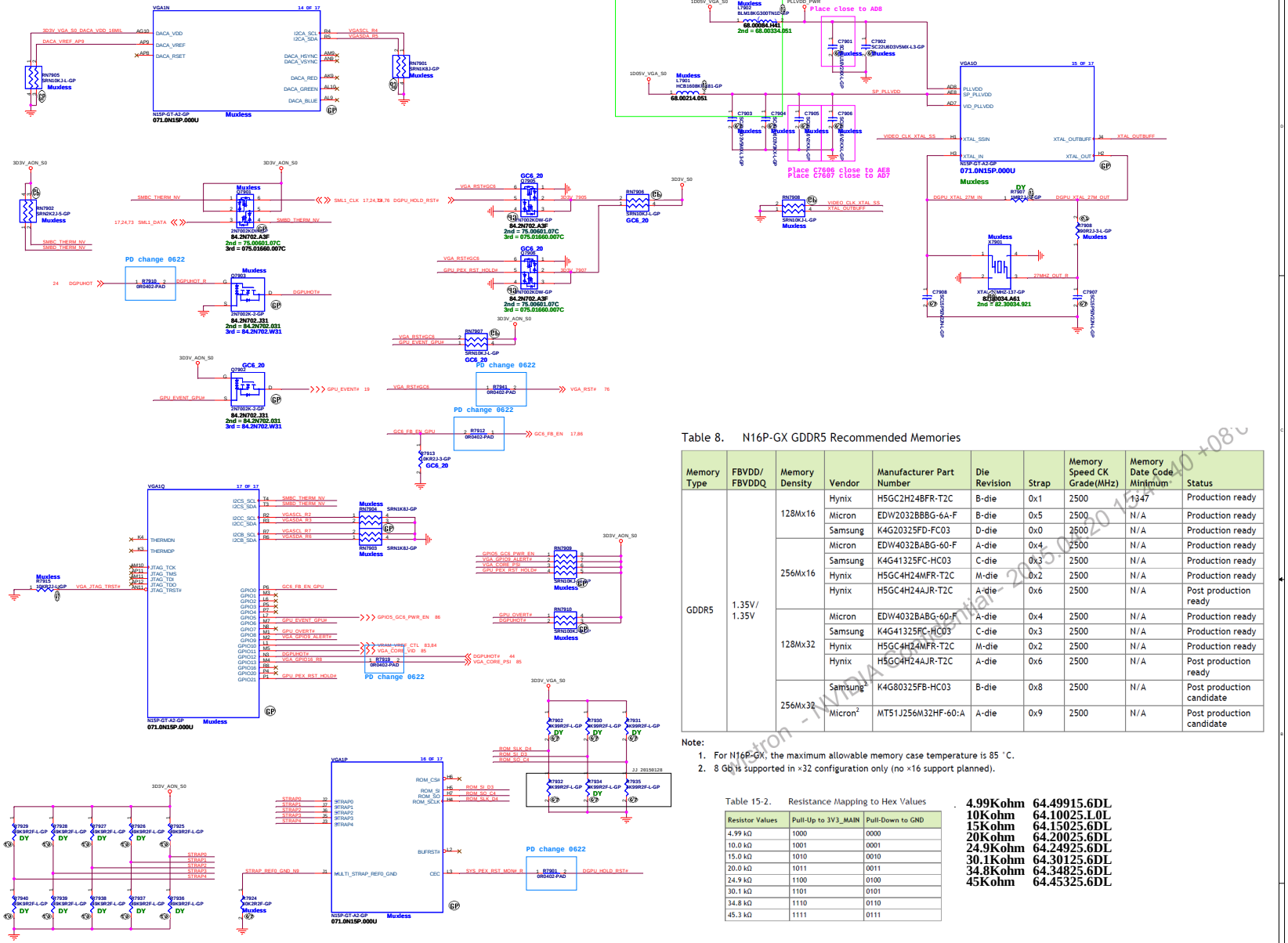


Table 8. N16P-GX GDDR5 Recommended Memories

Memory Type	FBVDD/ FBVDDQ	Memory Density	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed CK Grade(MHz)	Memory Date Code Minimum	Status
GDDR5	1.35V/ 1.35V	128Mx16	Hynix	H5GC2H24BFR-T2C	B-die	0x1	2500	1347	Production ready
			Micron	EDW2032BBBG-6A-F	B-die	0x5	2500	N/A	Production ready
			Samsung	K4G20325FD-FC03	D-die	0x0	2500	N/A	Production ready
		256Mx16	Micron	EDW4032BABG-60-F	A-die	0x4	2500	N/A	Production ready
			Samsung	K4G41325FC-HC03	C-die	0x3	2500	N/A	Production ready
			Hynix	H5GC4H24MFR-T2C	M-die	0x2	2500	N/A	Production ready
			Hynix	H5GC4H24AJR-T2C	A-die	0x6	2500	N/A	Post production ready
		128Mx32	Micron	EDW4032BABG-60-F	A-die	0x4	2500	N/A	Production ready
			Samsung	K4G41325FC-HC03	C-die	0x3	2500	N/A	Production ready
			Hynix	H5GC4H24MFR-T2C	M-die	0x2	2500	N/A	Production ready
			Hynix	H5GC4H24AJR-T2C	A-die	0x6	2500	N/A	Post production ready
		256Mx32	Samsung[2]	K4G80325FB-HC03	B-die	0x8	2500	N/A	Post production candidate
			Micron[2]	MT51J256M32HF-60:A	A-die	0x9	2500	N/A	Post production candidate

Note:
1. For N16P-GX, the maximum allowable memory case temperature is 85 °C.
2. 8 Gb is supported in ×32 configuration only (no ×16 support planned).

Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

4.99Kohm	64.49915.6DL
10Kohm	64.10025.L0L
15Kohm	64.15025.6DL
20Kohm	64.20025.6DL
24.9Kohm	64.24925.6DL
30.1Kohm	64.30125.6DL
34.8Kohm	64.34825.6DL
45Kohm	64.45325.6DL

Table 15-3. GB2B-64 and GB4B-128 Multi-level Mode Strapping

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	Keep foot print for pull-up to 3V3_AOH and pull-down to GND and stuff 50kΩ pull-up.			
STRAP1 STRAP2 STRAP3 STRAP4	Keep foot print for pull-up to 3V3_AOH and pull-down to GND for forward compatibility.			

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Title: GPU_GPIO/STRAP	
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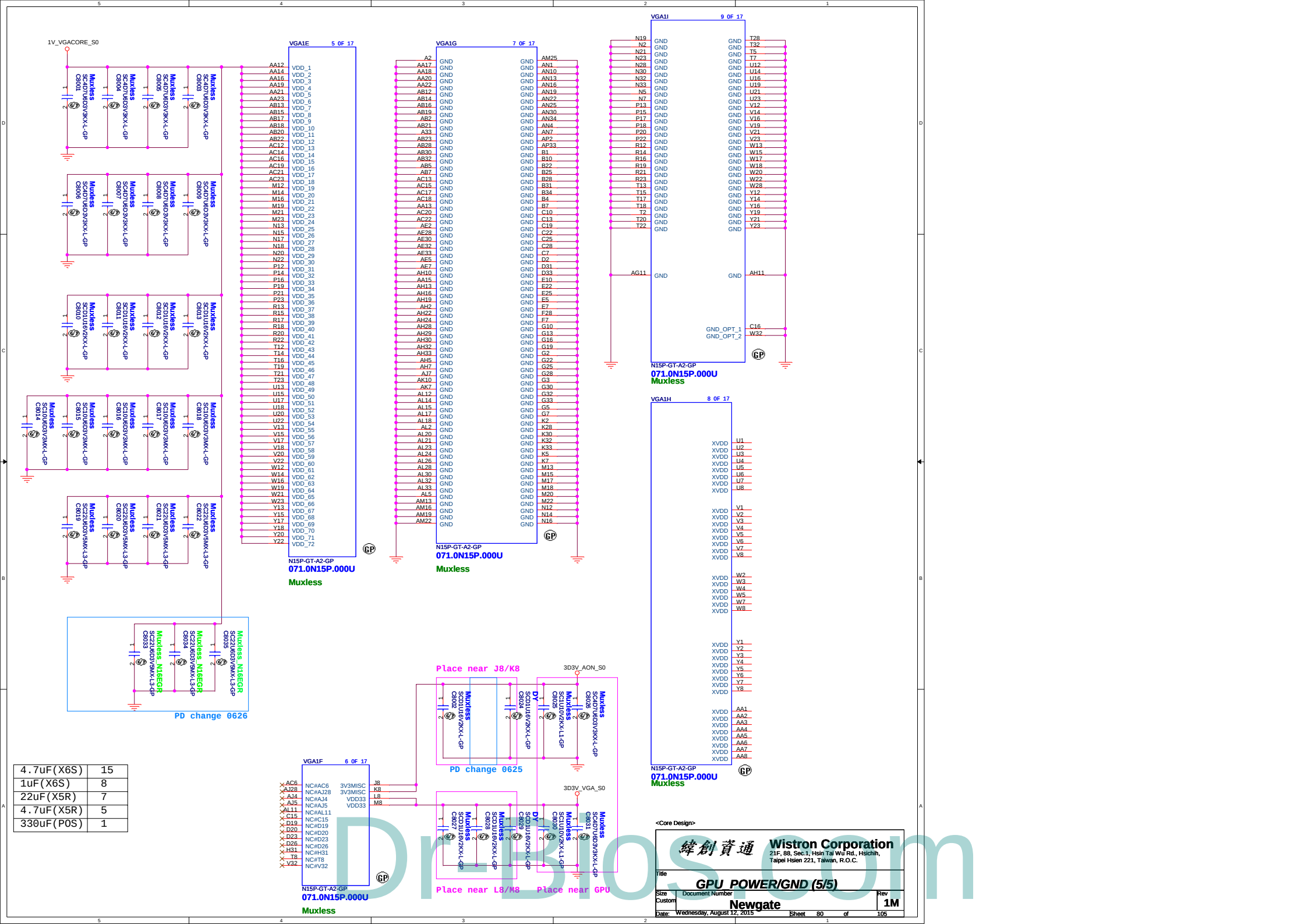

4.7uF(X6S)	15
1uF(X6S)	8
22uF(X5R)	7
4.7uF(X5R)	5
330uF(POS)	1

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Title: GPU_POWER/GND (5/5)

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TABLE
GDDR5 VIDEO MEMORY 72.05224.A0U 72.20325.B0U

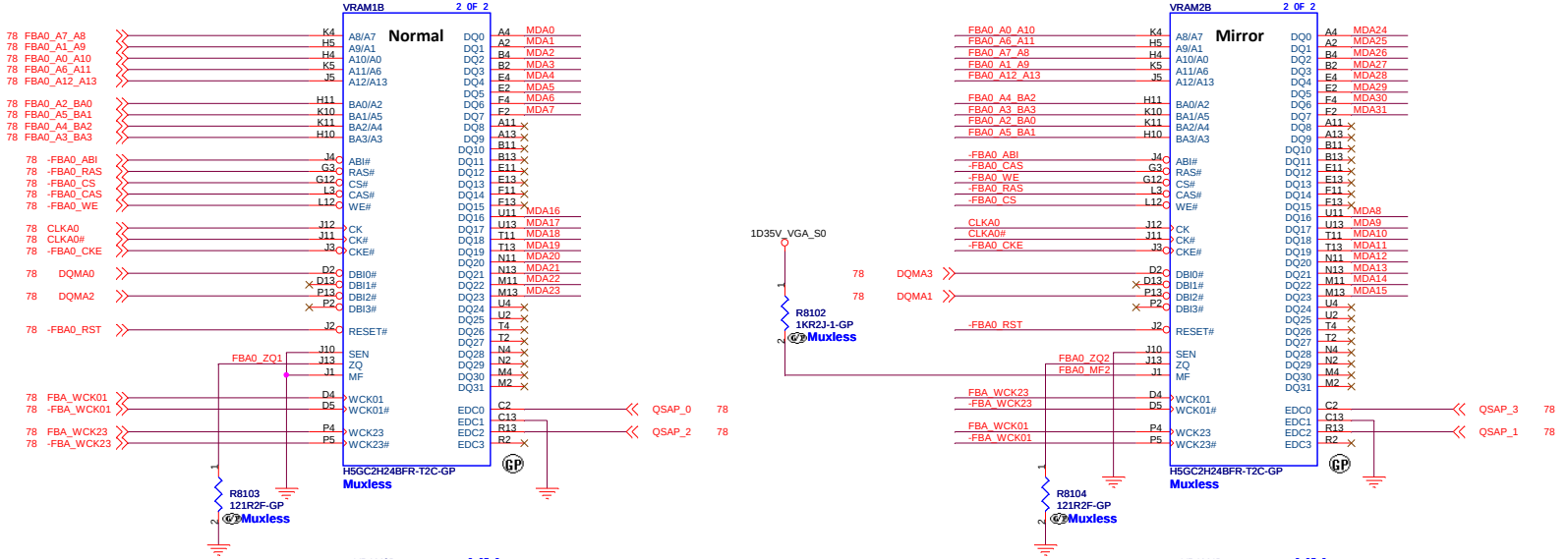
	HYNIX 2GBITS (64Mx32)	SAMSUNG 2GBITS (64Mx32)	HYNIX 4GBITS (128Mx32)	SAMSUNG 4GBITS (128Mx32)
U91 U92 U93 U94 U95 U96 U97 U98	H5GQ2H24AFR-T2C	K4G20325FD-FC04	H5GC4H24MFR (tentative)	K4G41325FC-HC03 (tentative)

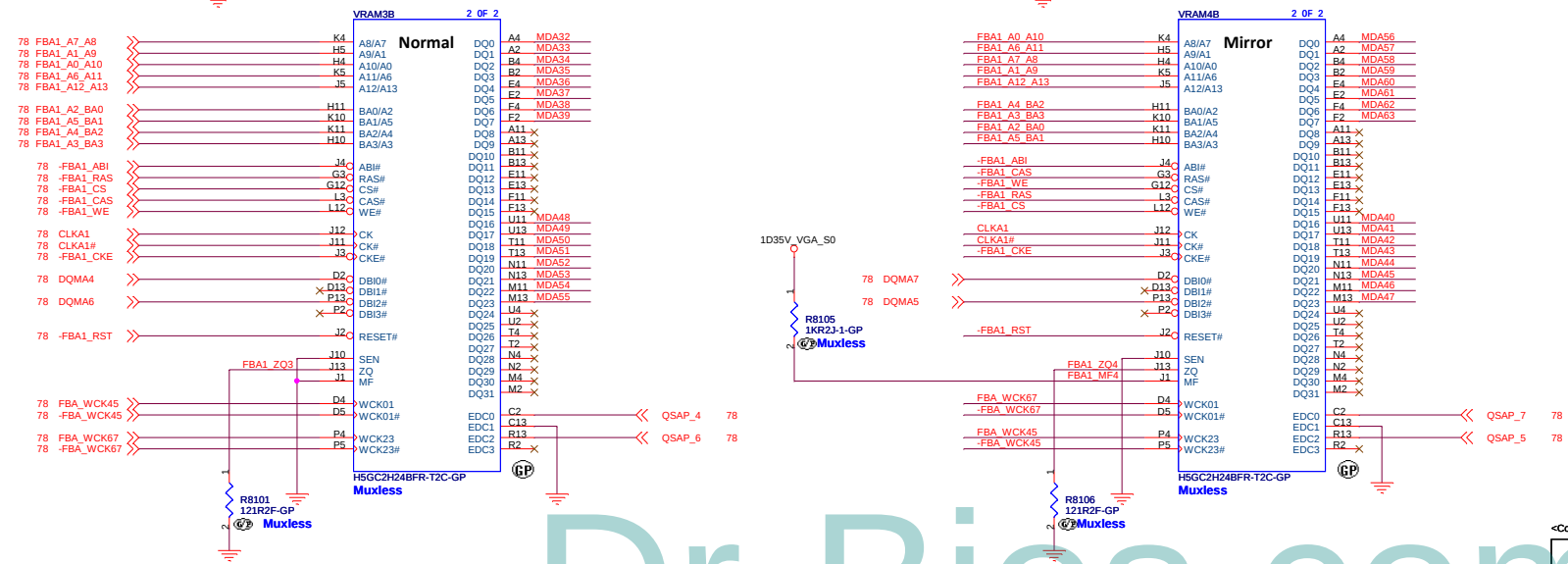
LOGIC

CHECK PM AVL

FB CMD mapping Mode H -N15P-GX GDDR5

MDA[63..0] 78





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Title: *VRAM 1,2 (1/4)*

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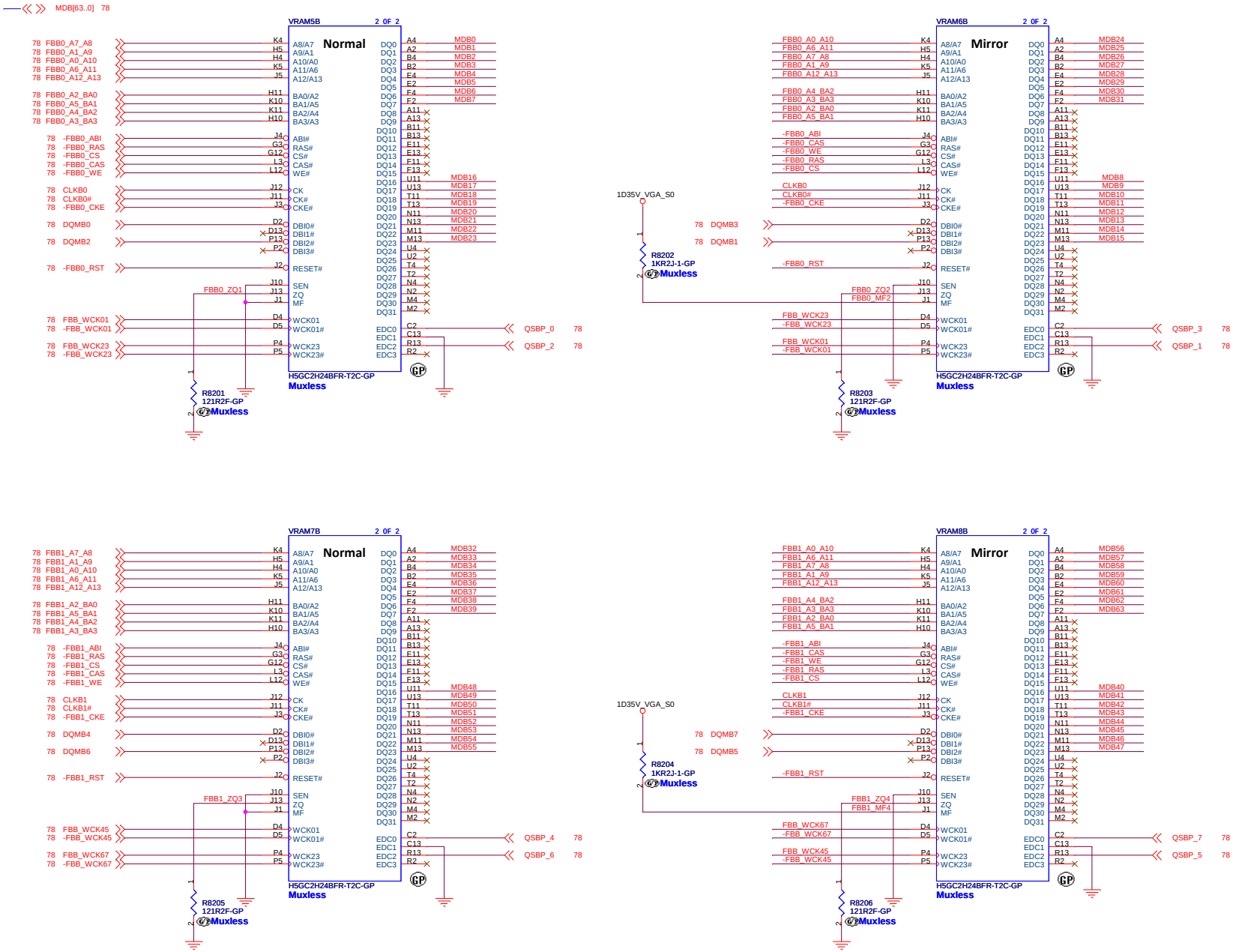

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Title: VRAM 3,4 (2/4)

Size: Custom | Document Number: Newgate | Rev: 1M

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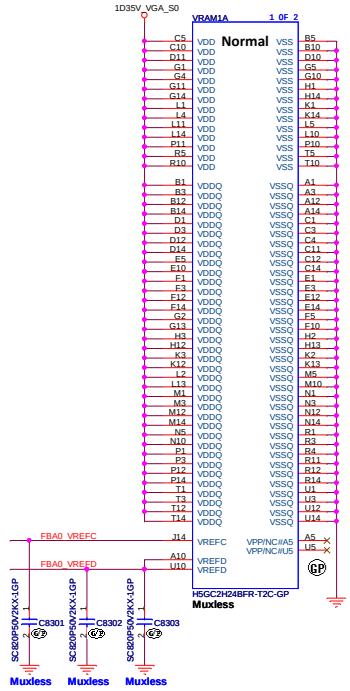

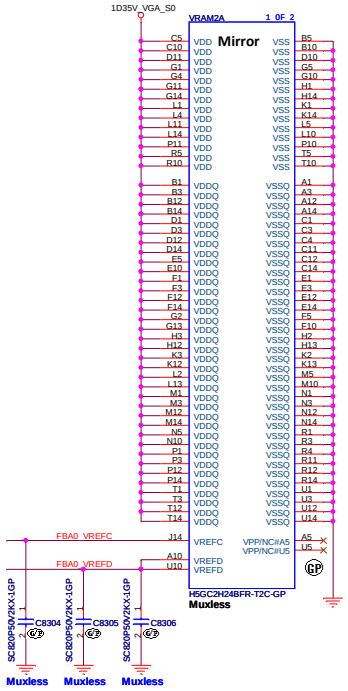

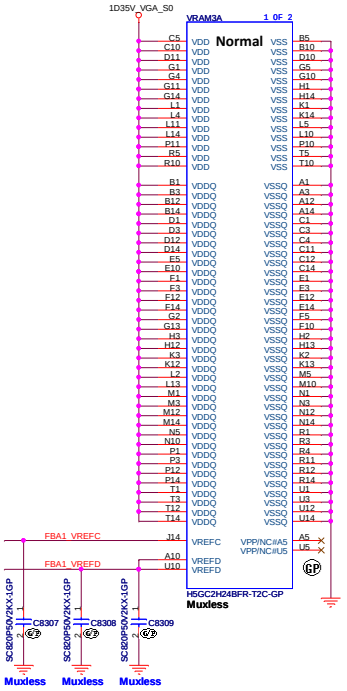

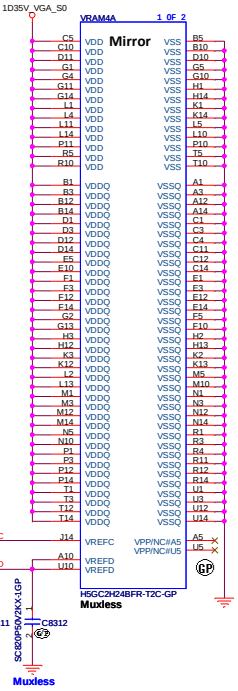

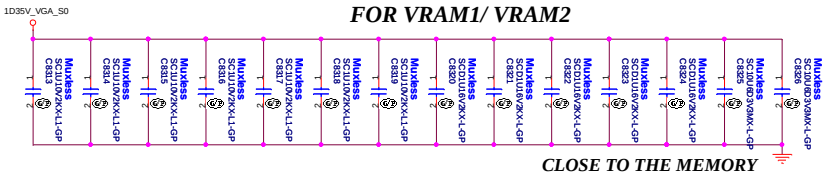

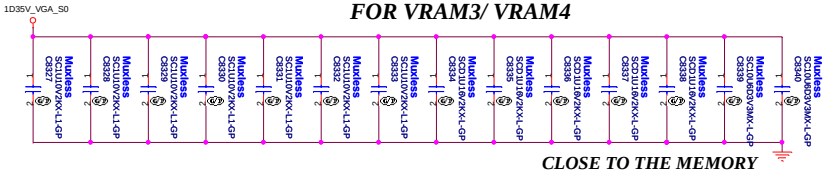

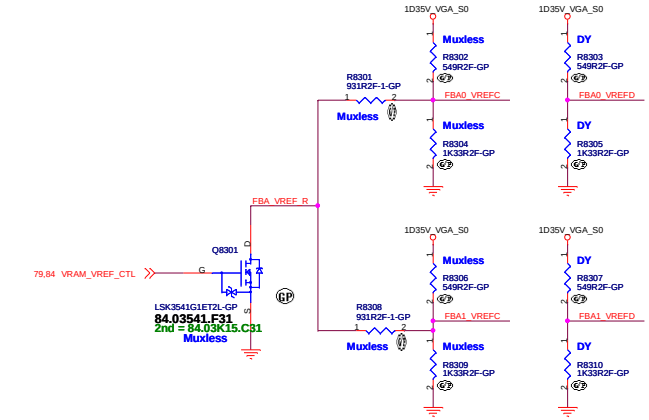

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Title: VRAM 5,6 (3/4)

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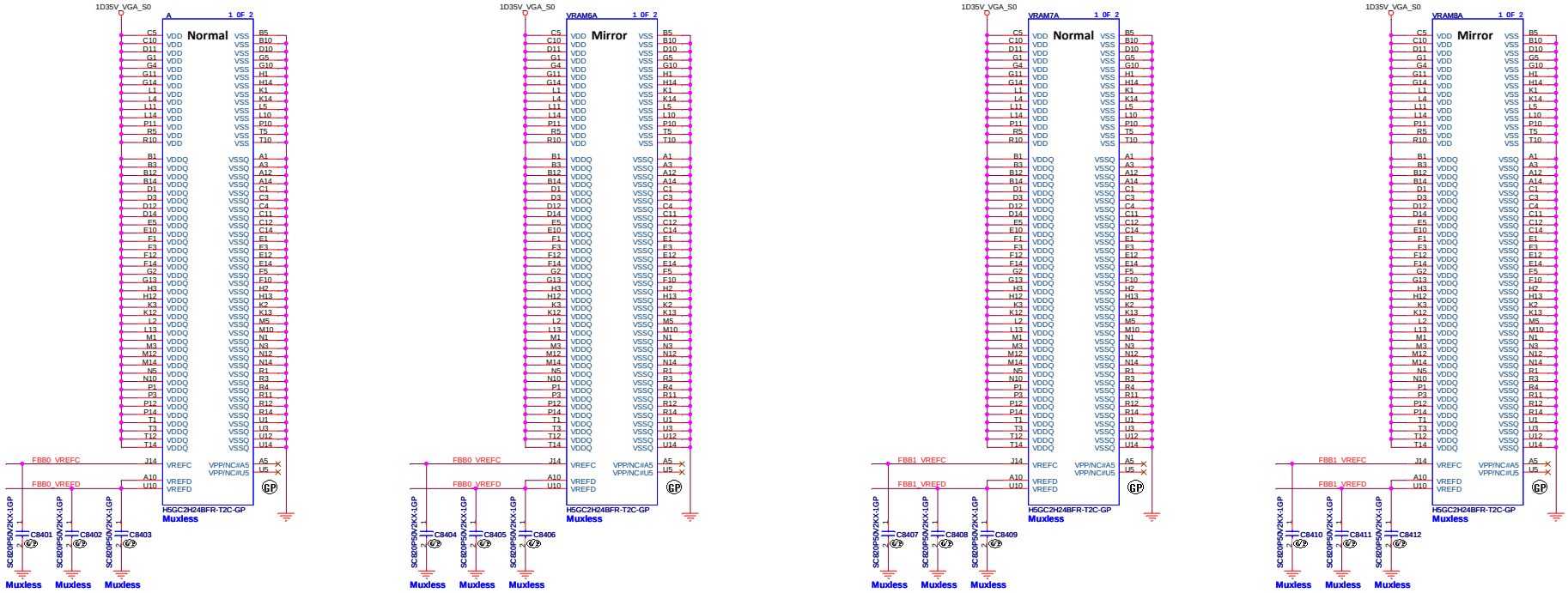
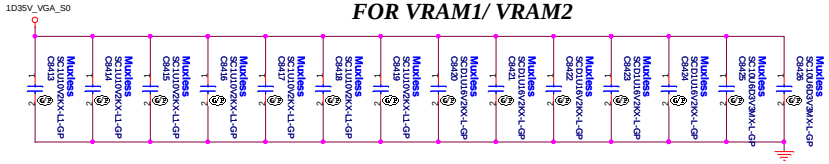
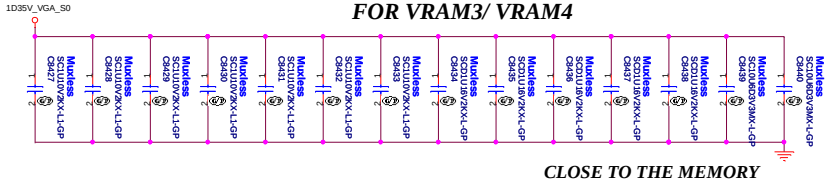


FOR VRAM1/ VRAM2



CLOSE TO THE MEMORY

FOR VRAM3/ VRAM4



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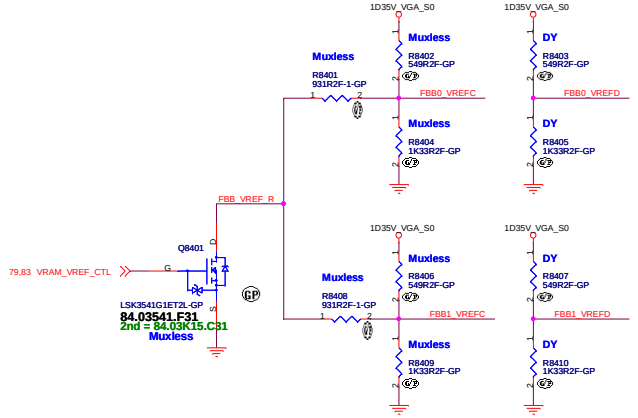

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Title: **VGA Power A**

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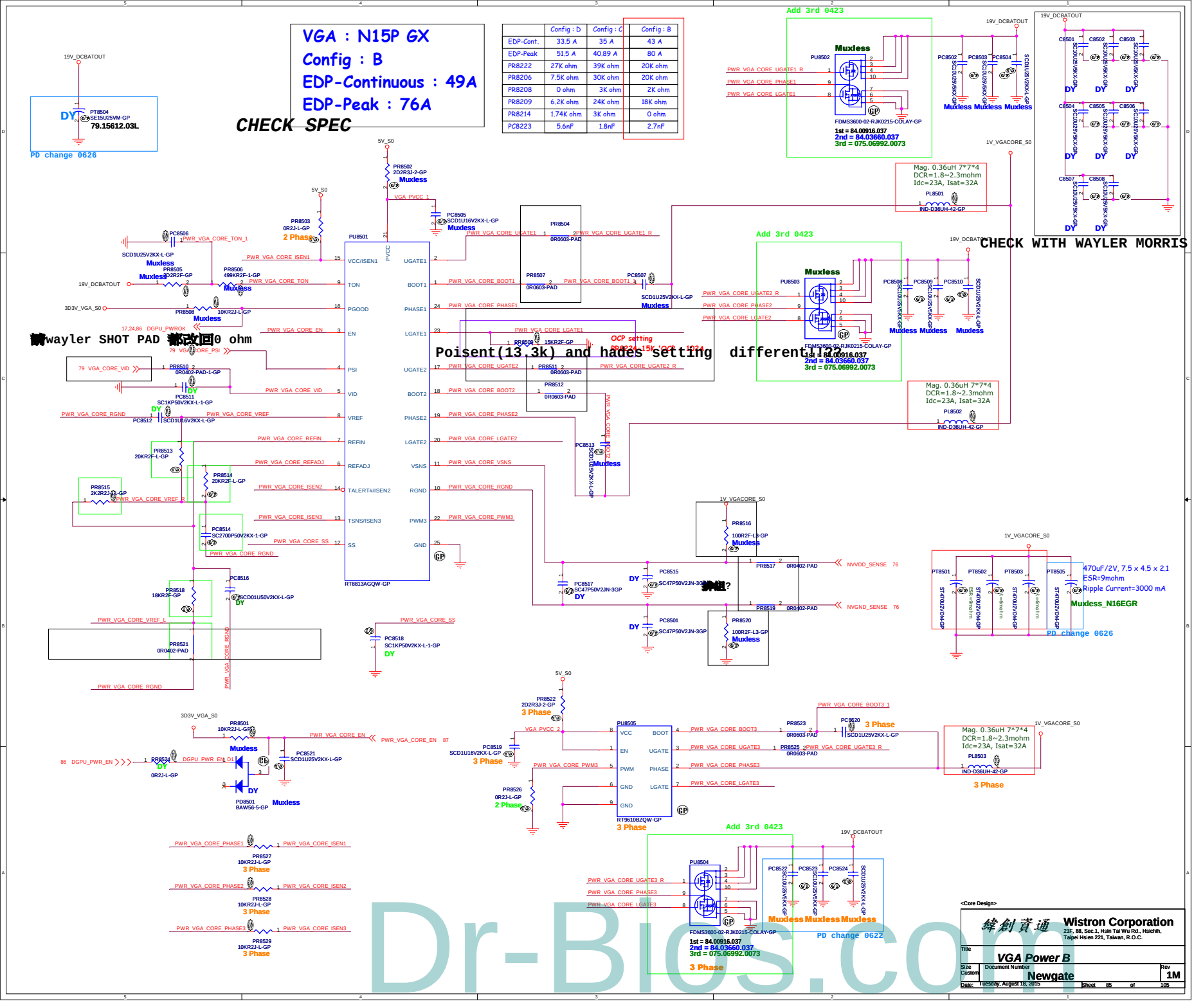
VGA : N15P GX
Config : B
EDP-Continuous : 49A
EDP-Peak : 76A
CHECK SPEC
Config : D
Config : C
Config : B
EDP-Cont. 33.5 A 35 A 43 A
EDP-Peak 51.5 A 40.89 A 80 A
PR8222 27K ohm 39K ohm 20K ohm
PR8206 7.5K ohm 30K ohm 20K ohm
PR8208 0 ohm 3K ohm 2K ohm
PR8209 6.2K ohm 24K ohm 18K ohm
PR8214 1.74K ohm 3K ohm 0 ohm
PC8223 5.6nF 1.8nF 2.7nF
Add 3rd 0423
Muxless
FDMS3600-02-RJK0215-COLAY-GP
1st = 84.00916.037
2nd = 84.03660.037
3rd = 075.06992.0073
CHECK WITH WAYLER MORRIS
Mag. 0.36uH 7*7*4
DCR=1.8~2.3mohm
Idc=23A, Isat=32A
IND-D36UH-42-GP
Wayler SHOT PAD 都改回0 ohm
Poisent(13.3k) and hades setting different!!??
OCP setting
R8524 15K OCP 1024
RT8813AGQW-GP
RT9610BZQW-GP
PD change 0626
PD change 0622
470uF/2V, 7.5 x 4.5 x 2.1
ESR=9mohm
Ripple Current=3000 mA
Muxless_N16EGR
3 Phase
2 Phase
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VGA Power B
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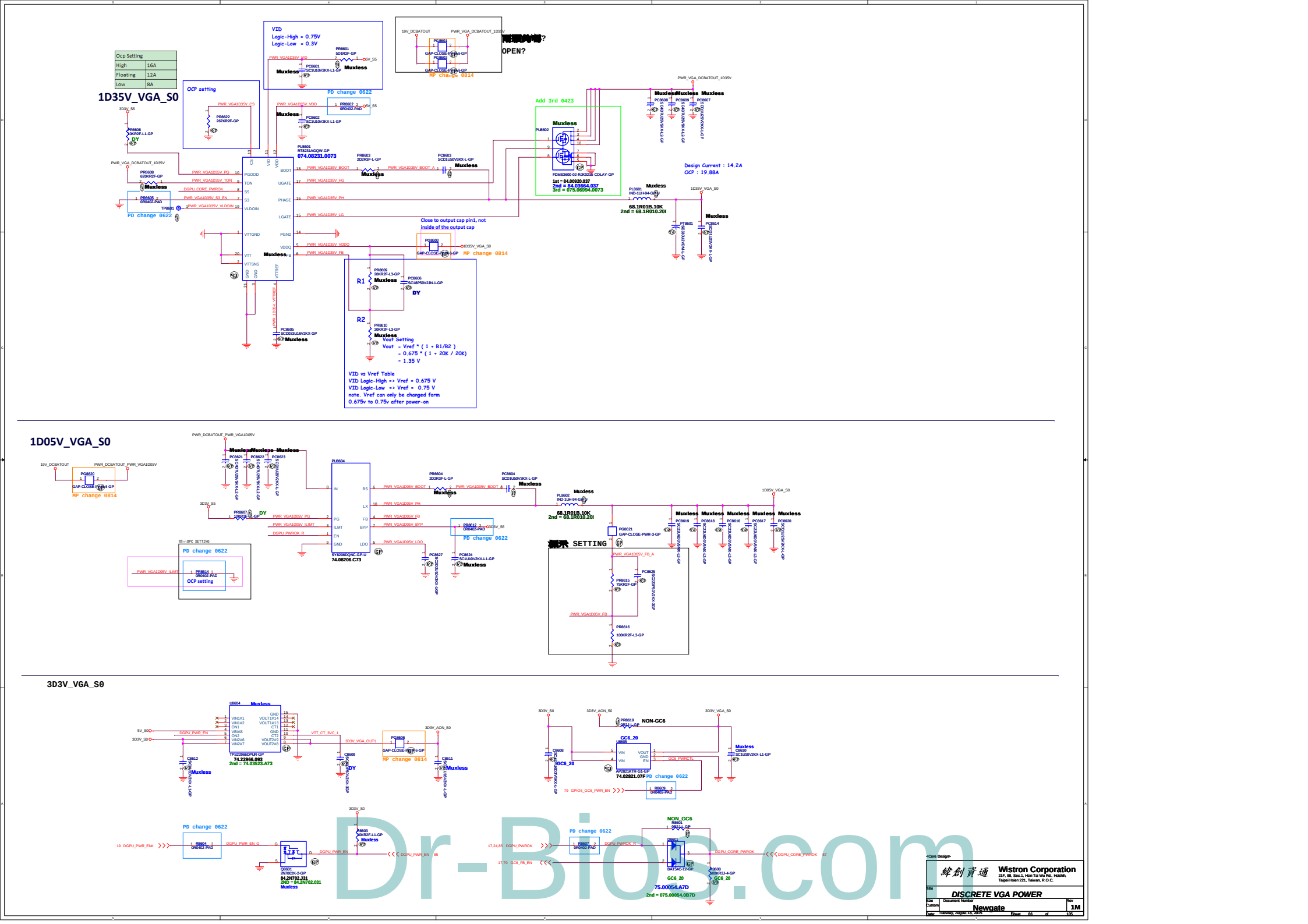
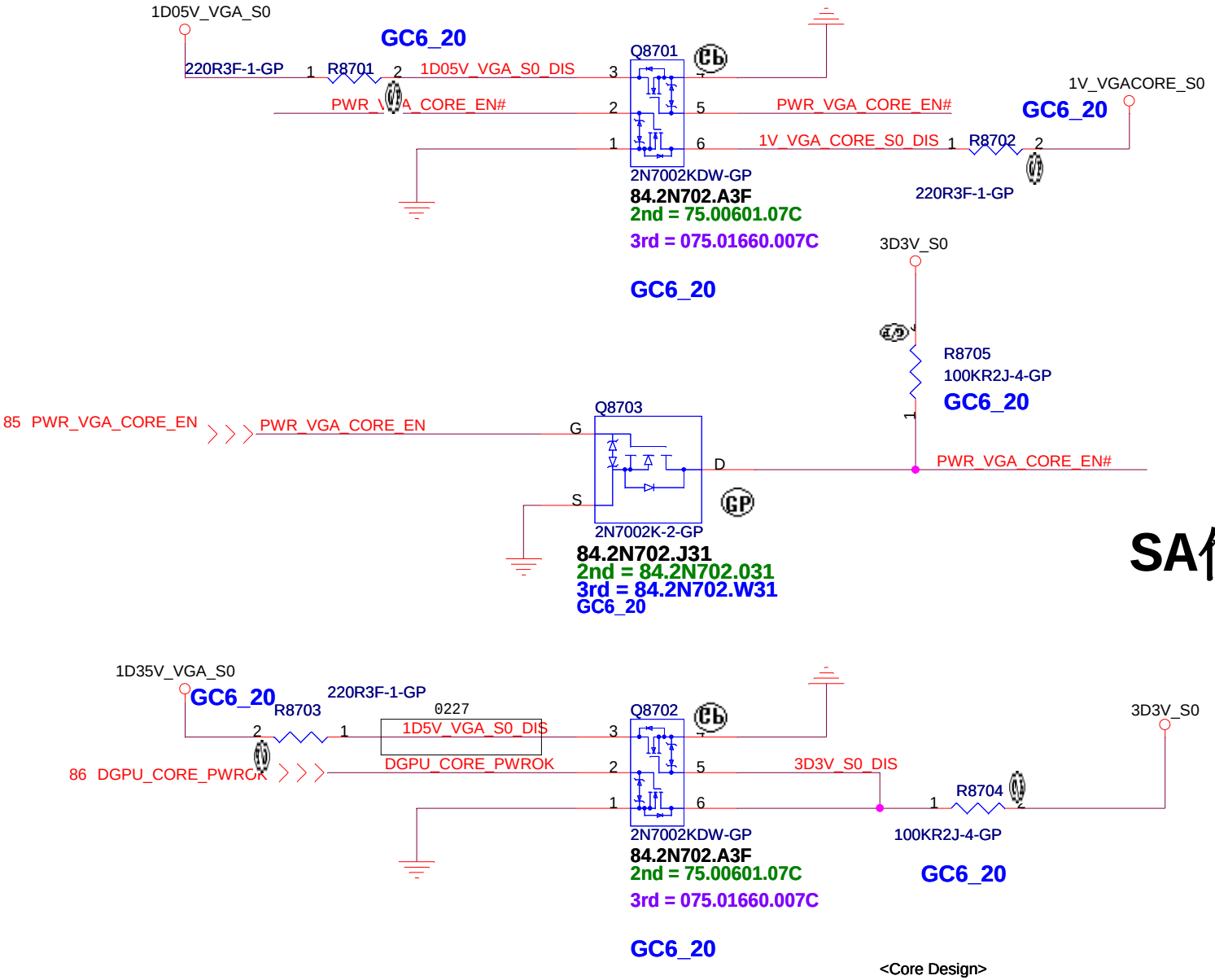

1D35V_VGA_S0
Ocp Setting
High 16A
Floating 12A
Low 8A
OCP setting
VID
Logic-High = 0.75V
Logic-Low = 0.3V
PD change 0622
MP change 0814
OPEN?
Add 3rd 0423
Design Current : 14.2A
OCP : 19.88A
Close to output cap pin1, not inside of the output cap
Vout Setting
Vout = Vref * (1 + R1/R2)
= 0.675 * (1 + 20K / 20K)
= 1.35 V
VID vs Vref Table
VID Logic-High => Vref = 0.675 V
VID Logic-Low => Vref = 0.75 V
note. Vref can only be changed form 0.675v to 0.75v after power-on
1D05V_VGA_S0
SETTING
3D3V_VGA_S0
NON-GC6
GC6_20
Dr-Bios.com
Wistron Corporation
DISCRETE VGA POWER
Newgate



SA做實驗

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Title: ***Discharge***

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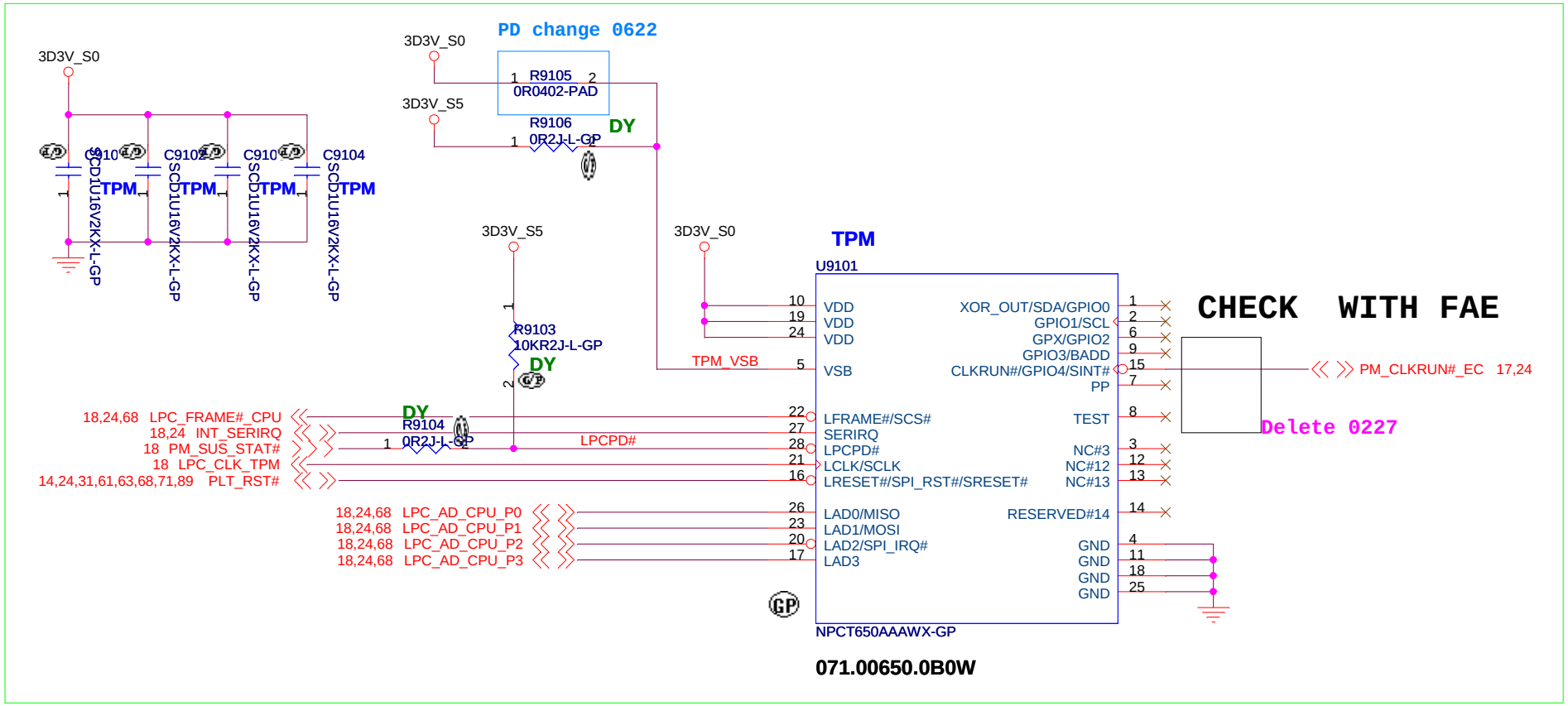

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Title: ***TPM/NPCT650***

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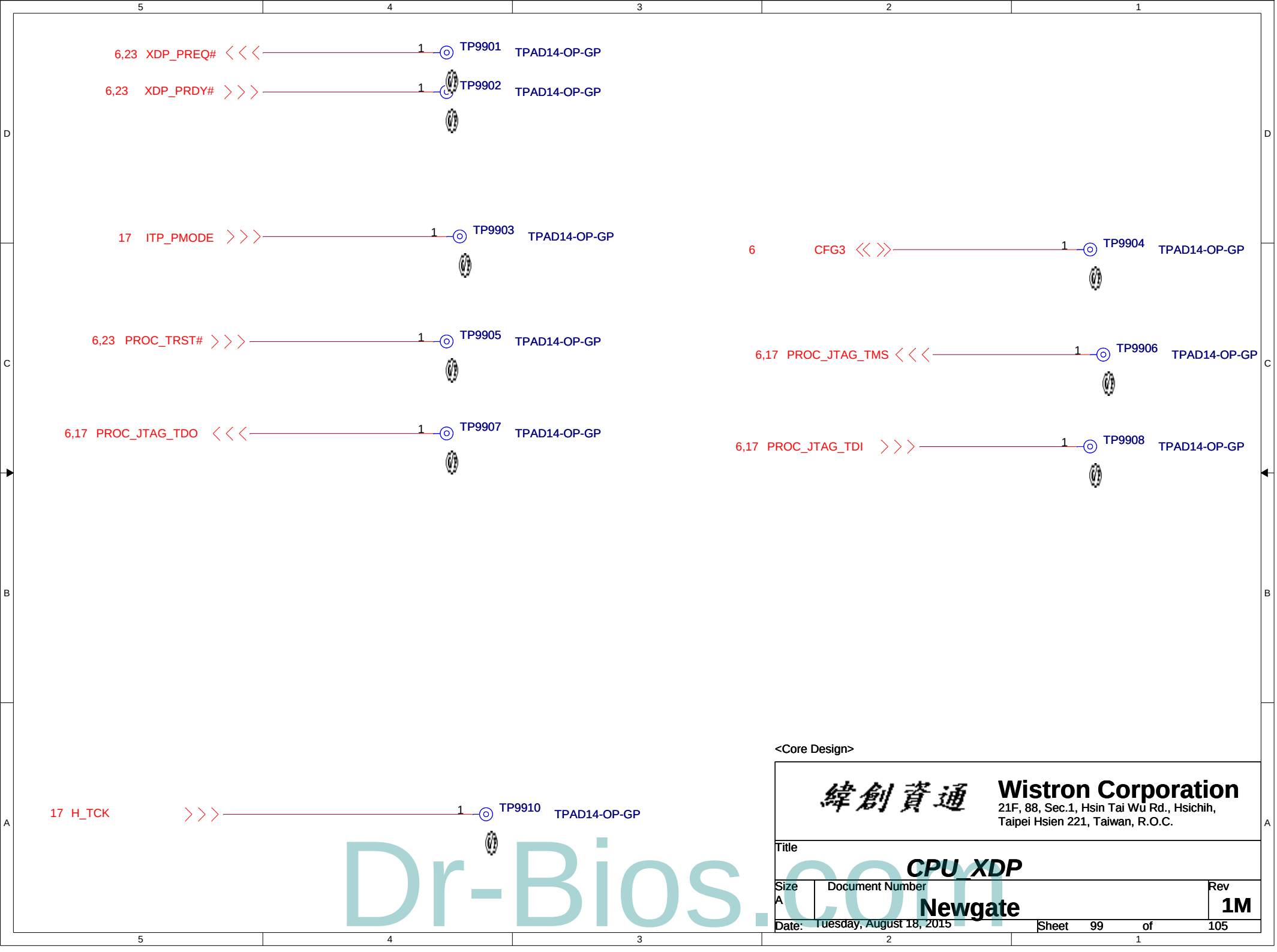

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Title: ***CPU_XDP***

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Title

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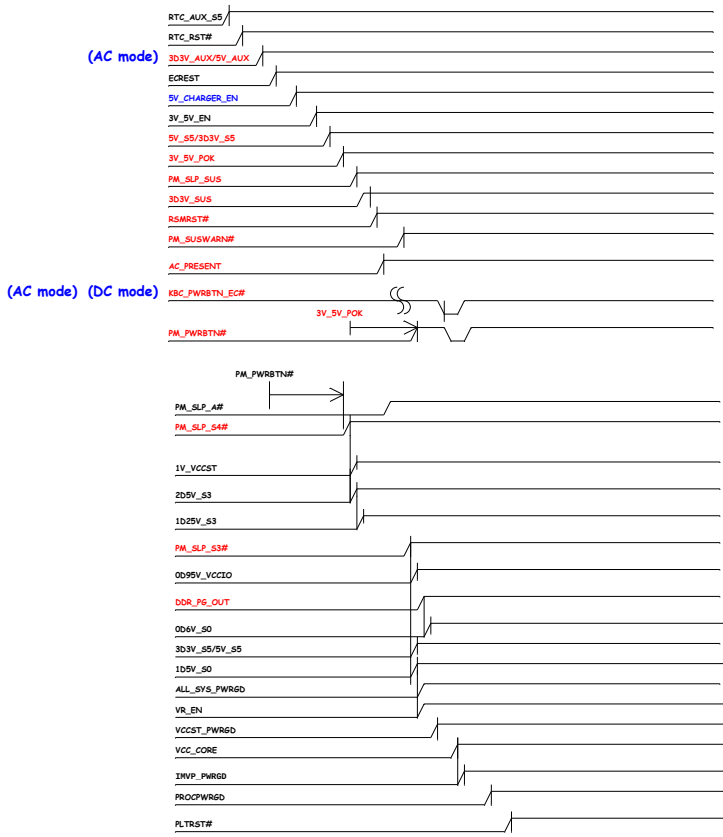
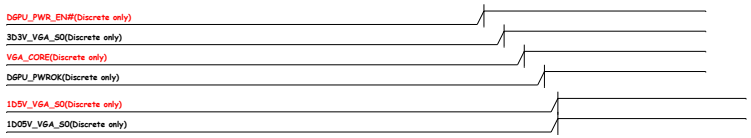
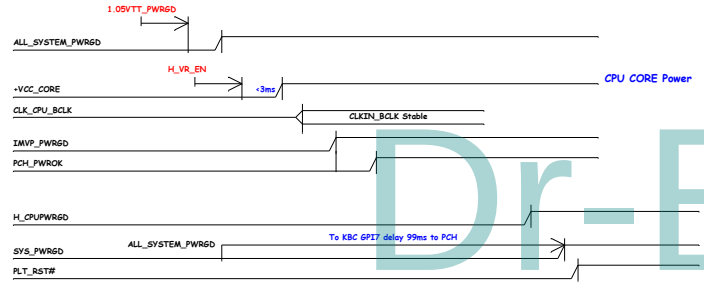
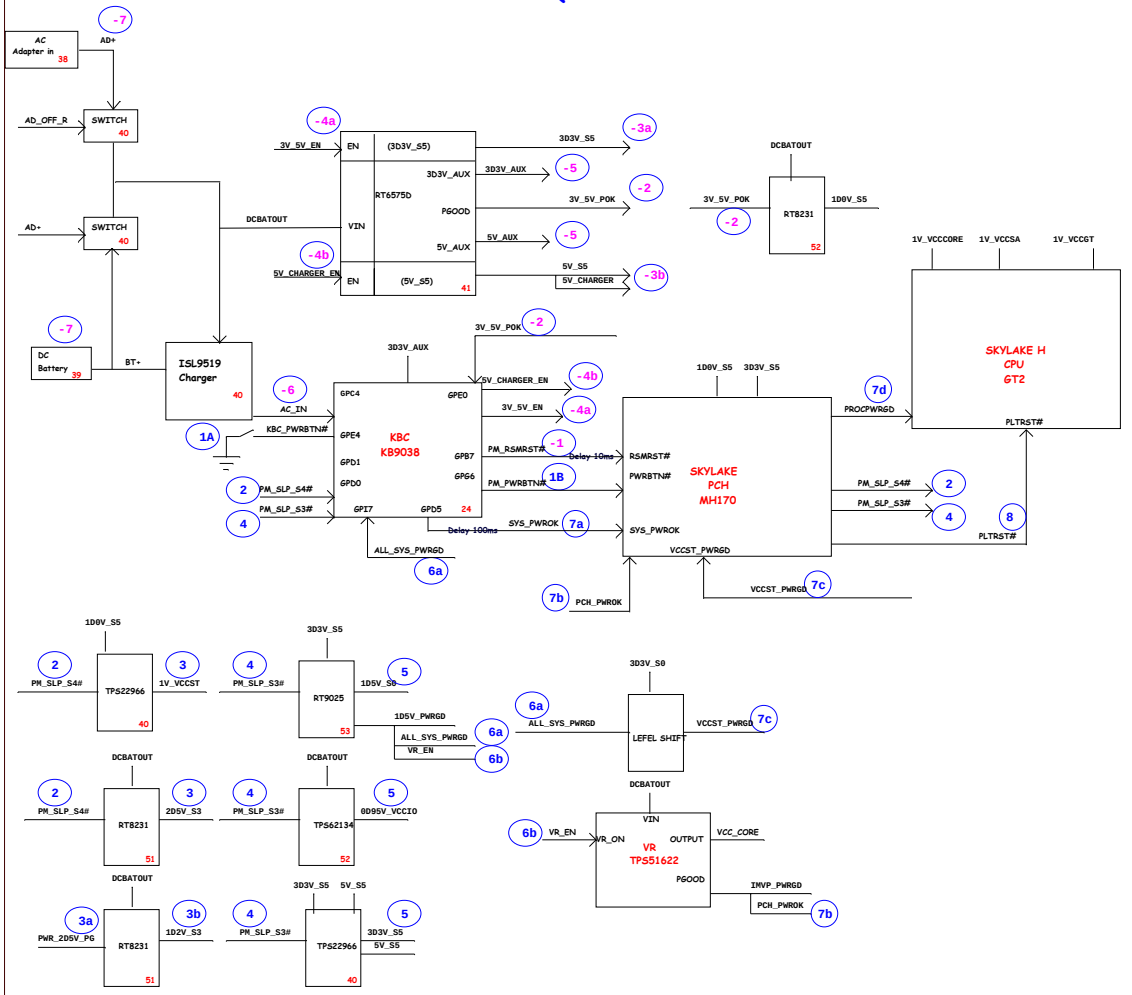
Intel-Power Up Sequence

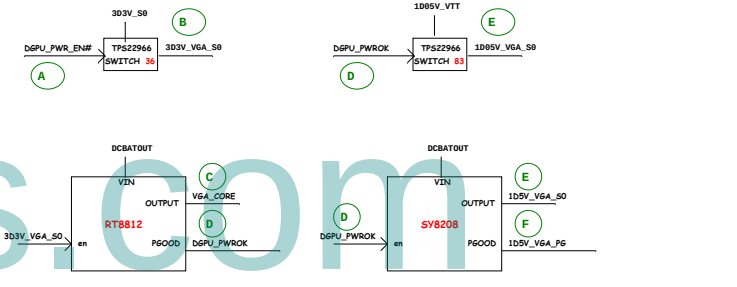






SKYLAKE H POWER UP SEQUENCE DIAGRAM





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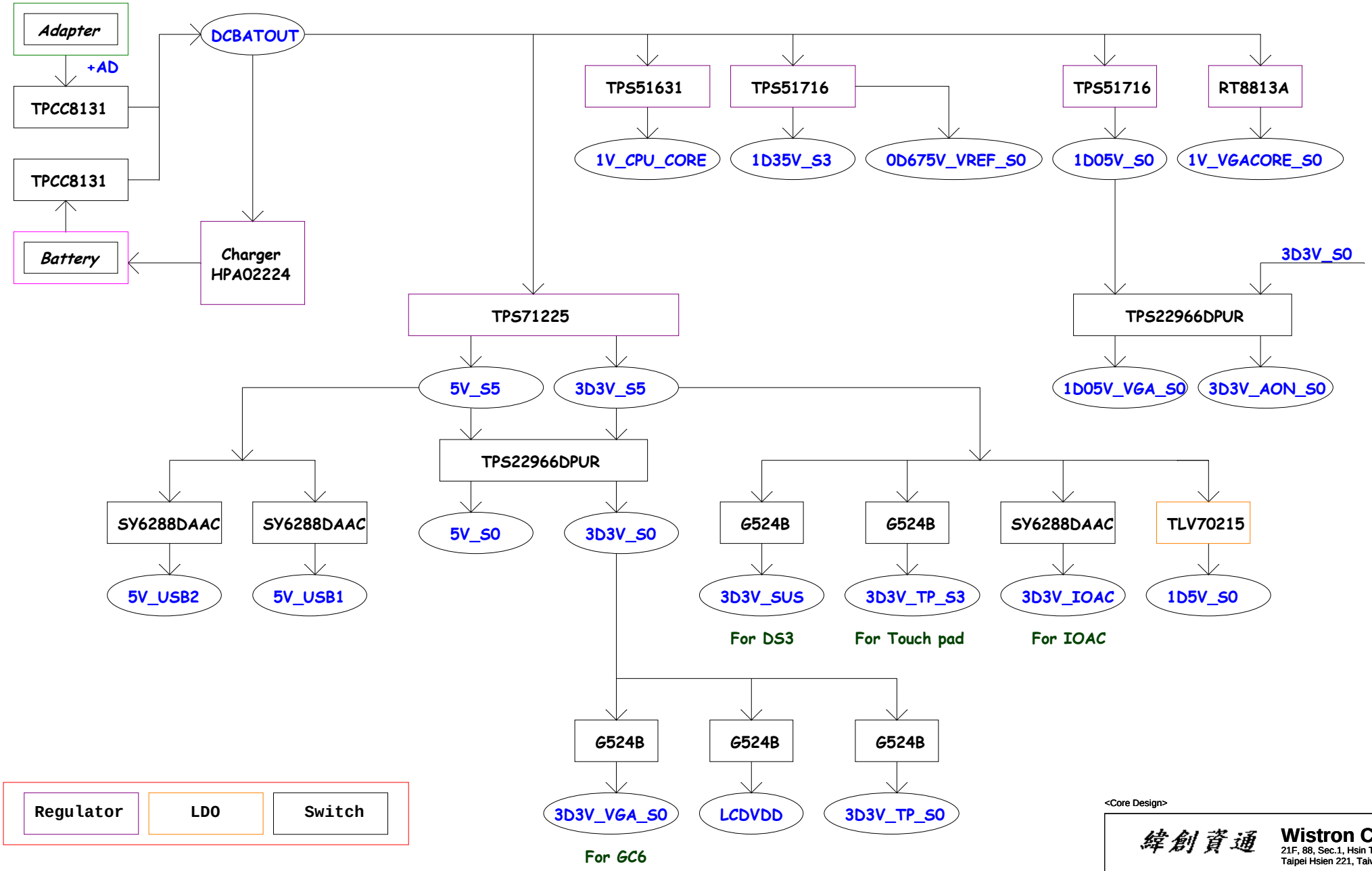
Power Sequence

Newgate

1M



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Title: Power Block Diagram

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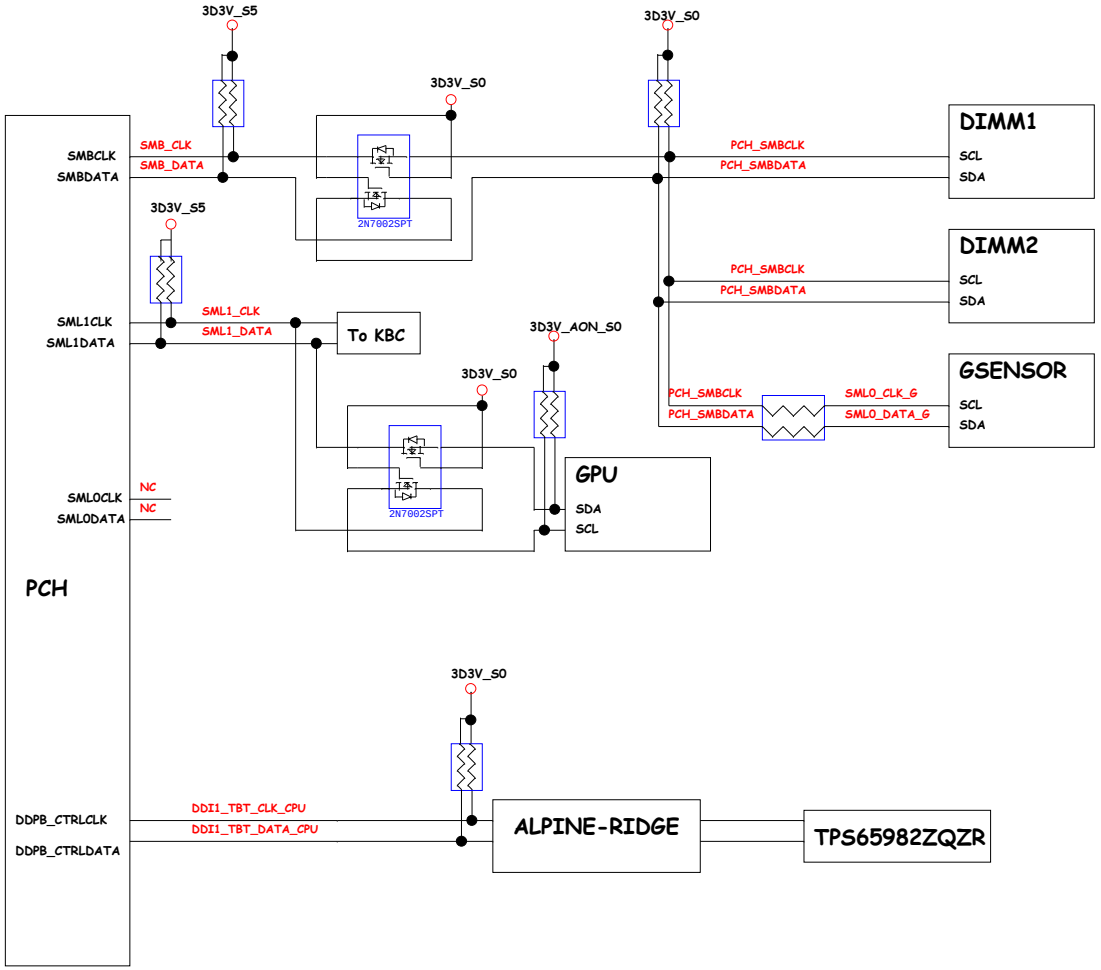
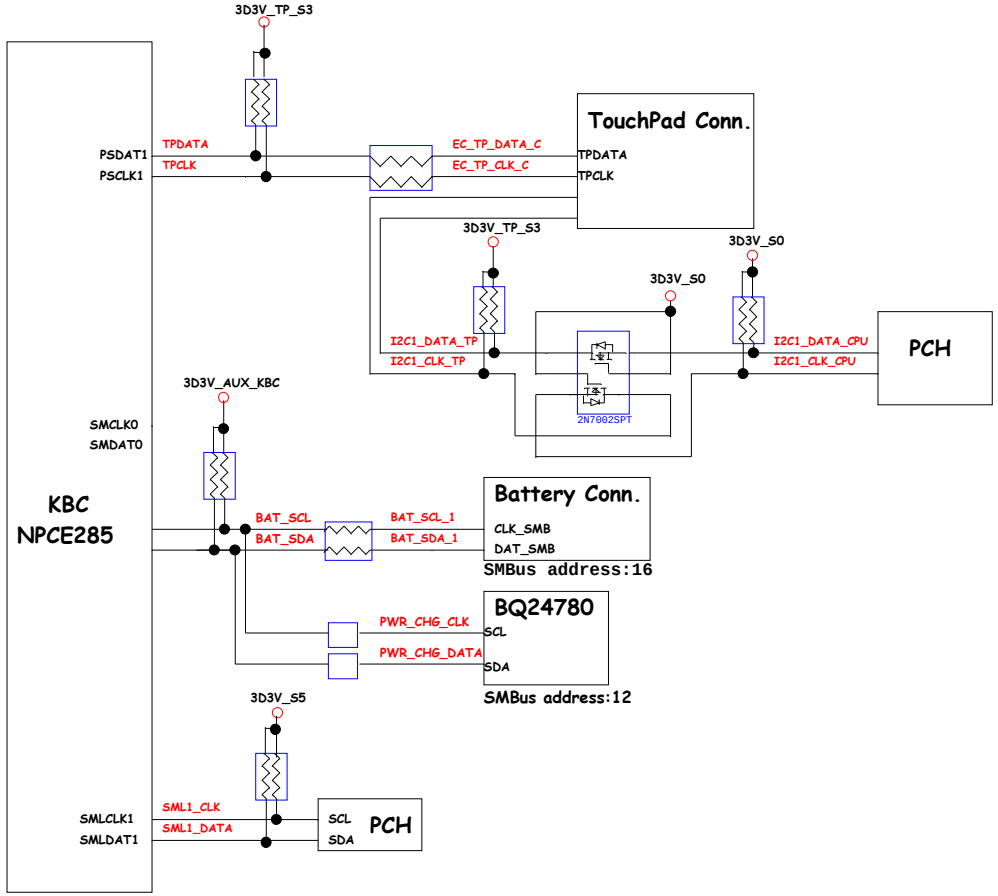
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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Title	SMBUS BLOCK DIAGRAM
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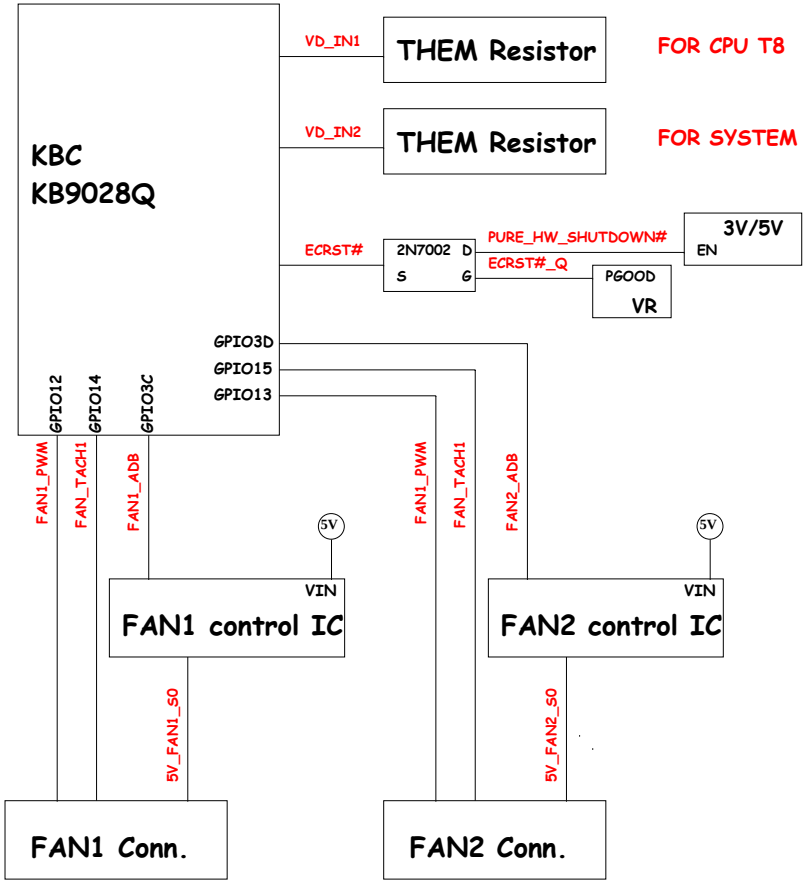
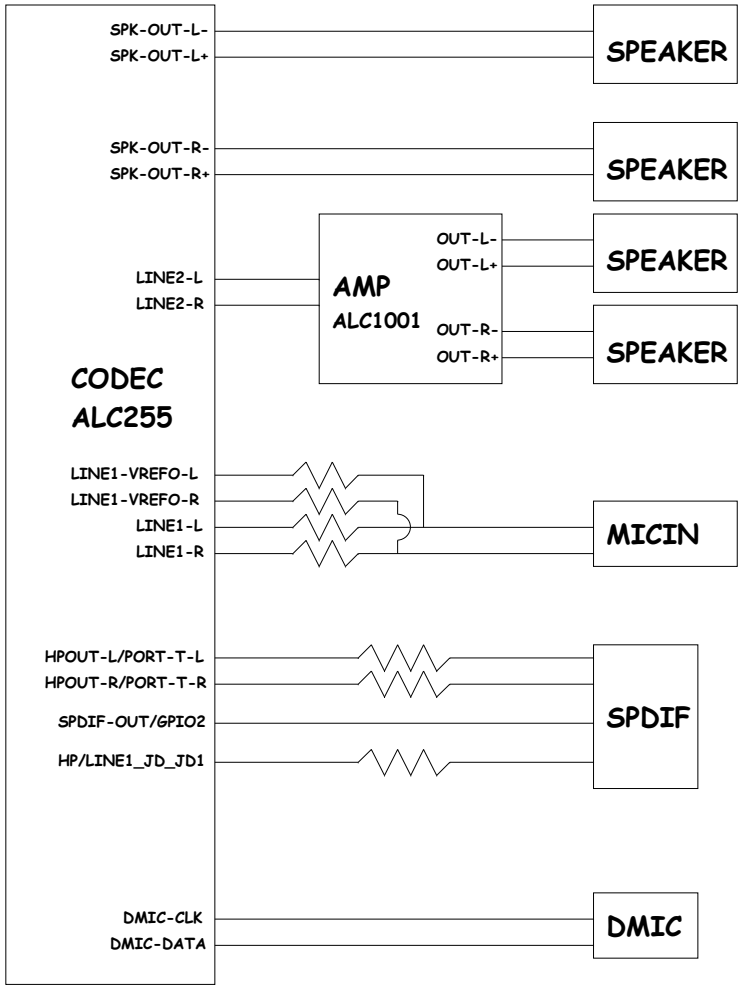
Thermal Block Diagram



Audio Block Diagram



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Title	Thermal /AUDIO Block Diagram	
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