

Newgate

Schematics Document

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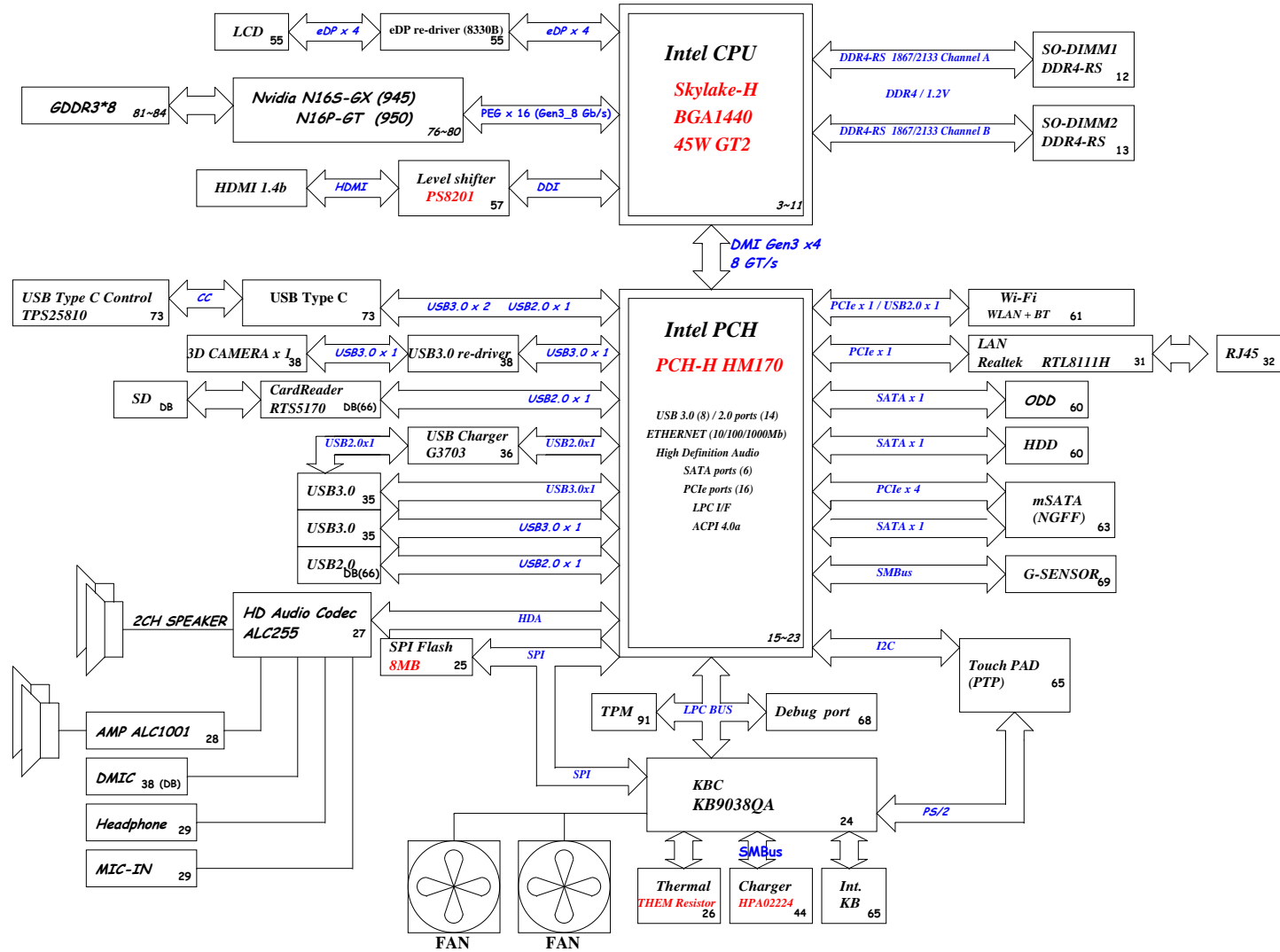
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
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Title		Cover Page	
Size	Document Number	Rev	
A	Newgate	1M	
Date:	Wednesday, August 12, 2015	Sheet	1 of 105

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Newgate Board Block Diagram

Project code : 4PD06A010001
 PCB NO : 15205
 Revision : 1M



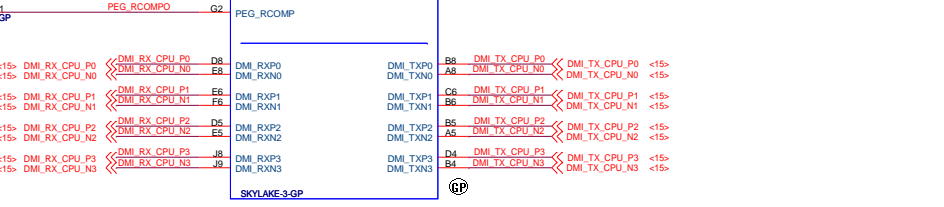
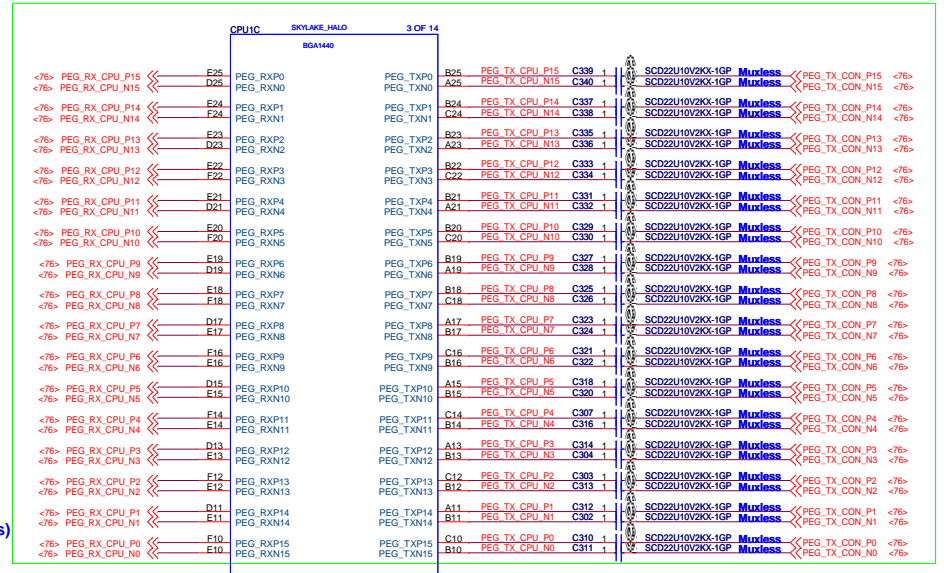
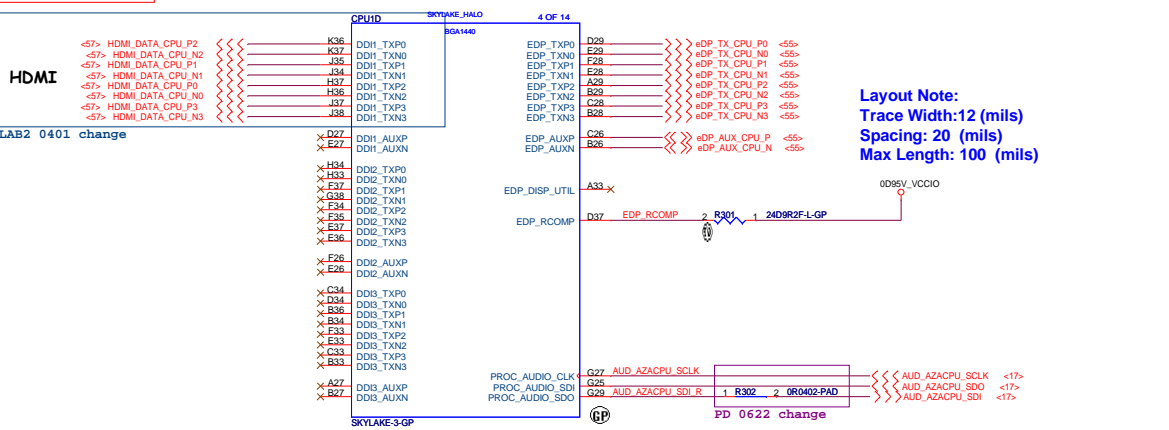
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Block Diagram	
Title Size C Date: Wednesday, August 12, 2015	Document Number Newgate Sheet 2 of 105
Rev 1M	

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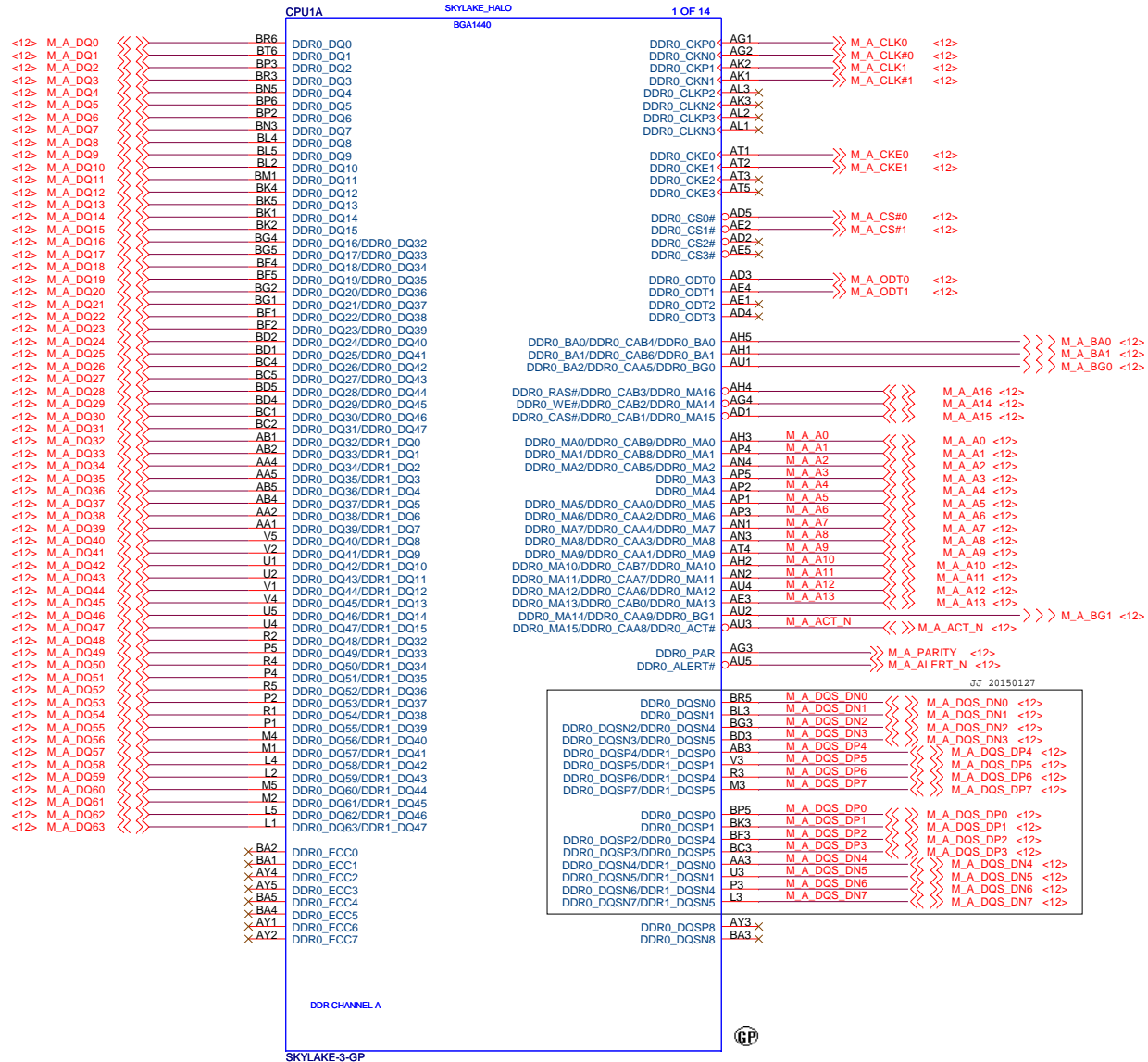
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Title: **CPU (PCIe/DMI/FDI)**

Size	Document Number	Rev
Custom	Newgate	1M

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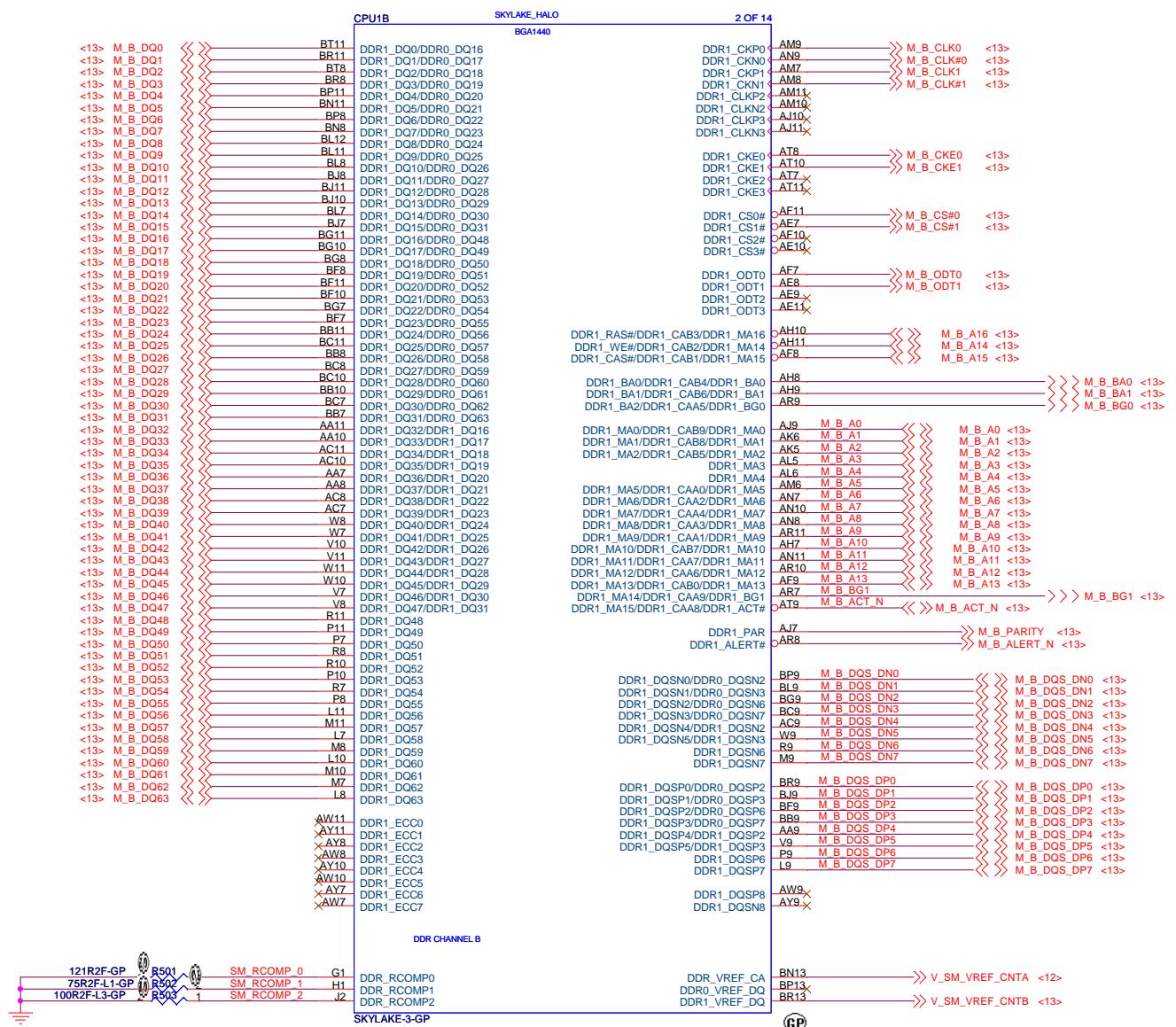


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Title		Rev
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Size	Document Number	
A3	Newgate	
Date:	Thursday, August 13, 2015	Sheet 4 of 105



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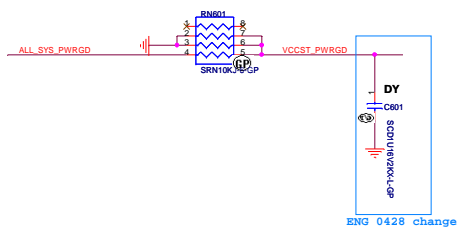
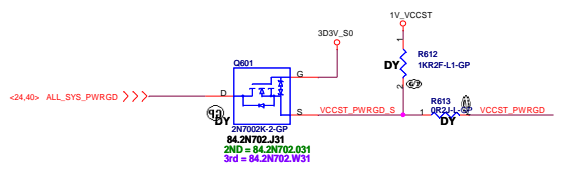
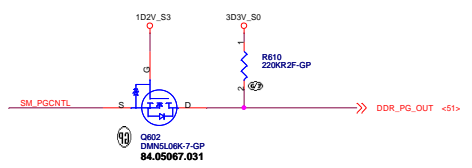
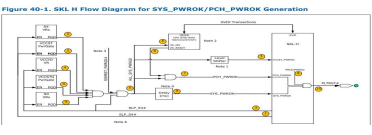
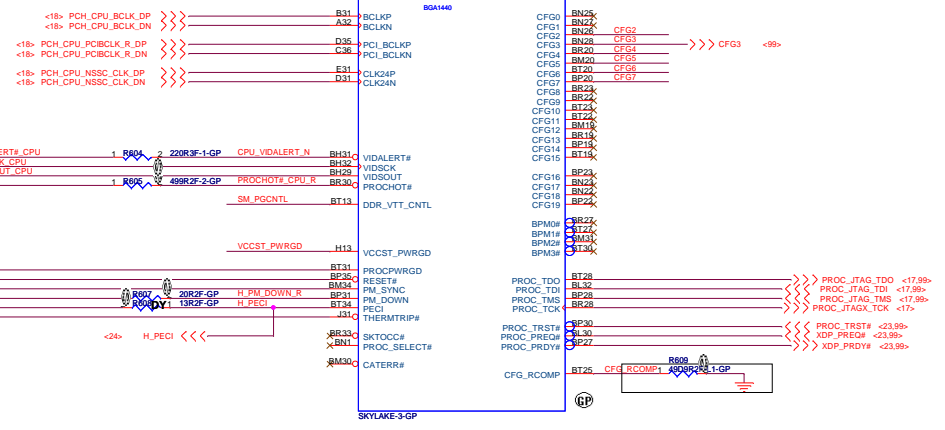
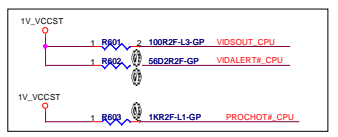
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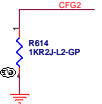
Size A3	Document Number	Rev
Date: Thursday, August 13, 2015	Newgate	1M
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AROUND_CPU

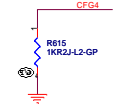
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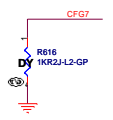
PEG Static Lane Reversal	
CFG2	1: Normal Operation: Lane # definition matches socket pin map definition 0: Lane Reversed



eDP Enable	
CFG4	1: Disable 0: Enable



PEG Training	
CFG7	1: (default) PEG Train immediately following RESET# de assertion 0 = PEG Wait for BIOS for training.



PCIe Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled / function 2 disabled 01: Reserved - (device 1 function 1 disabled / function 2 enabled) 00: x8, x4, x4 - Device 1 functions 1 and 2 enabled

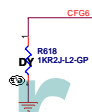
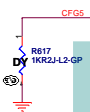


Table 6-8. Reset and Miscellaneous Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
CFG[0]	Configuration Signals: The CFG signals have a default value of "1" if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. Intel recommends placing test points on the board for CFG pins. • CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted: - 1 = (Default) Normal Operation; No stall. - 0 = Stall. • CFG[1]: Reserved configuration lane. • CFG[2]: PCI Express® Static x16 Lane Numbering Reversal. - 1 = Normal operation - 0 = Lane numbers reversed. • CFG[3]: Reserved configuration lane. • CFG[4]: eDP enable: - 1 = Disabled. - 0 = Enabled. • CFG[6:5]: PCI Express® Bifurcation - 00 = 1 x8, 2 x4 PCI Express* - 01 = reserved - 10 = 2 x8 PCI Express* - 11 = 1 x16 PCI Express* • CFG[7]: PEG Training: - 1 = (default) PEG Train immediately following RESET# de assertion. - 0 = PEG Wait for BIOS for training. • CFG[19:0]: Reserved configuration lanes.	I/O	GTL	SE	All processor lanes. CFG[2], CFG[6:5] and CFG[7] are relevant for H and S-processor line only and test point may be placed on the board for them.

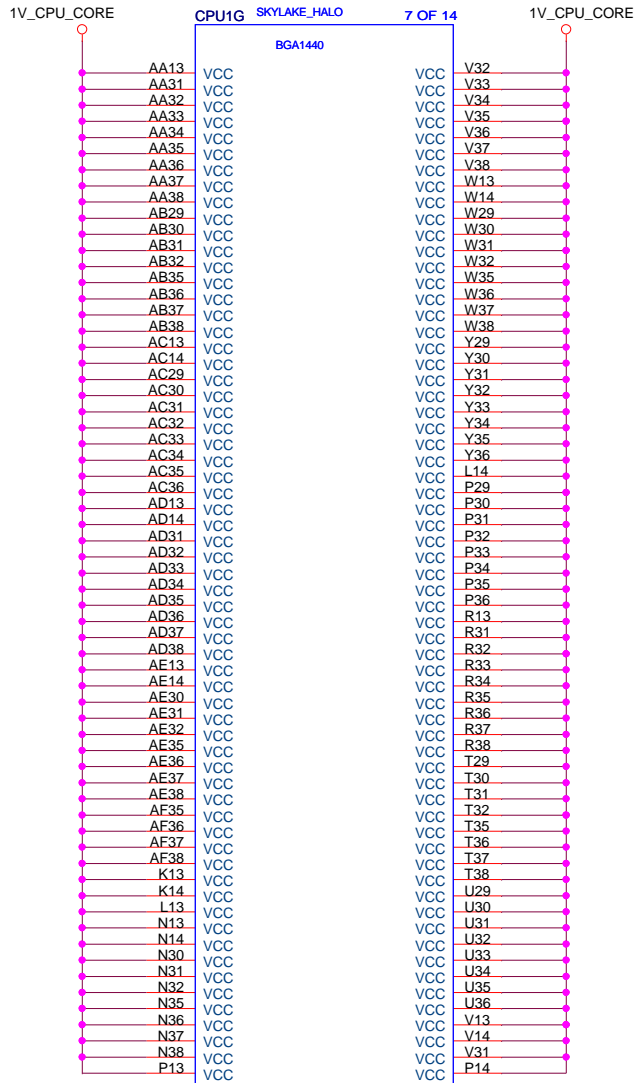
Processor Internal Pull-Up / Pull-Down Terminations

Processor Internal Pull-Up / Pull-Down Terminations

Signal Name	Pull Up/Pull Down	Rail	Value
BPM[3:0]	Pull Up	VCC _{IO}	16-60 Ω
PREQ#	Pull Up	VCC _{IO}	3 kΩ
PROC_TDI	Pull Up	VCC _{IO} ¹	3 kΩ
PROC_TMS	Pull Up	VCC _{IO} ¹	3 kΩ
CFG[19:0]	Pull Up	VCC _{IO}	3 kΩ

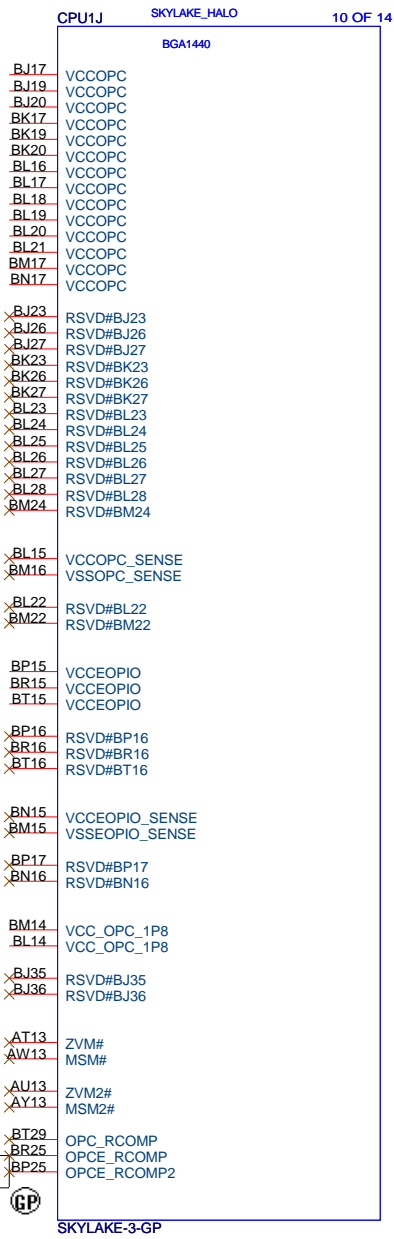
Note:
1. For SKL-S it should be VCC_{ST}

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VCC_SENSE AG37 >>> VCCCORE_SENSE <46>
 VSS_SENSE AG38 >>> VSSCORE_SENSE <46>

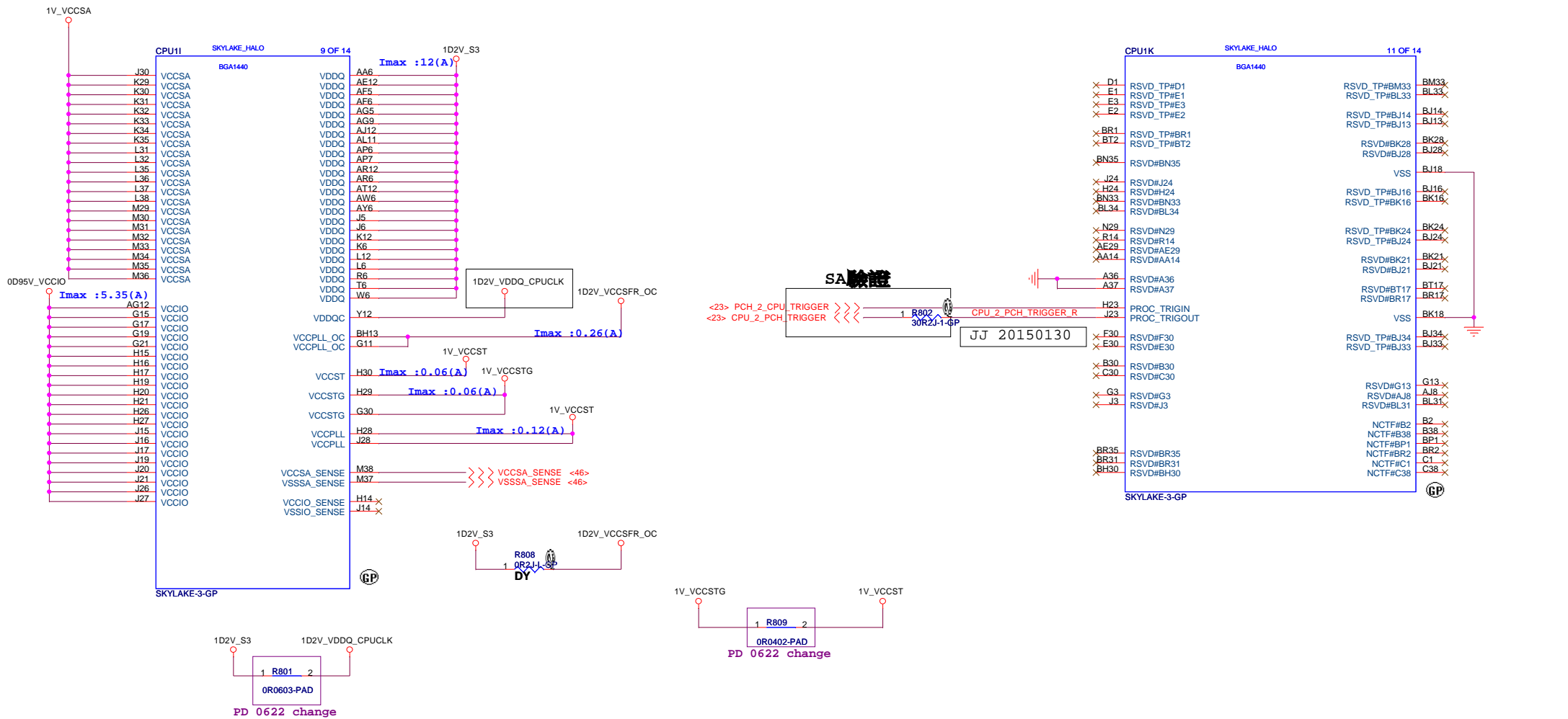
JJ 20150130



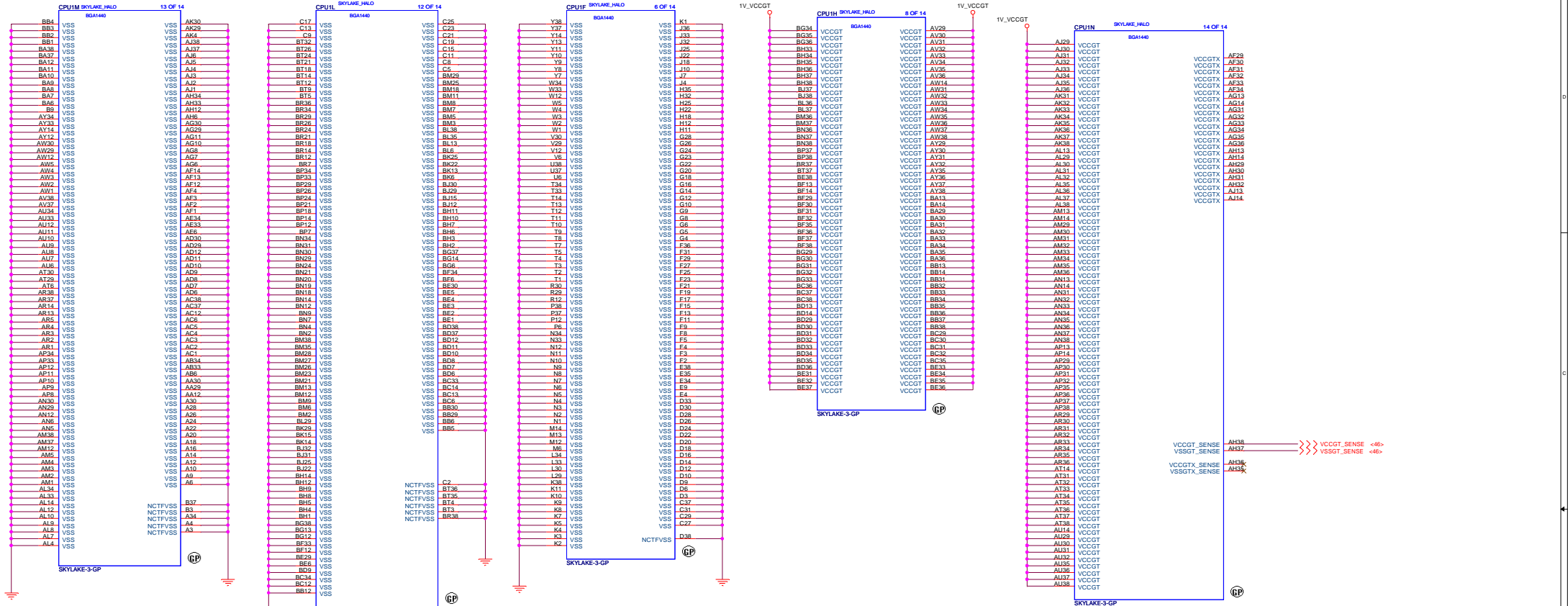
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Size Custom	Document Number	Newgate	
		Rev	1M
Date: Thursday, August 13, 2015	Sheet 7	of	105

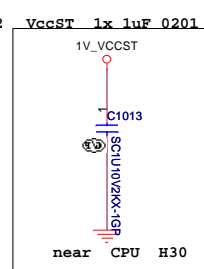
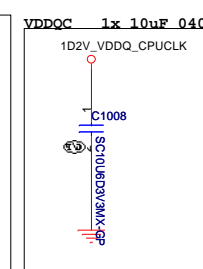
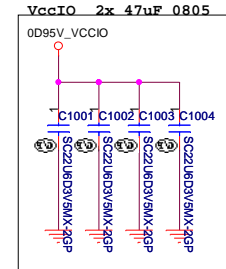
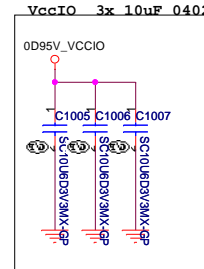
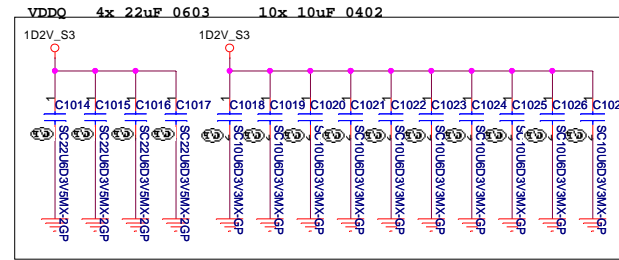
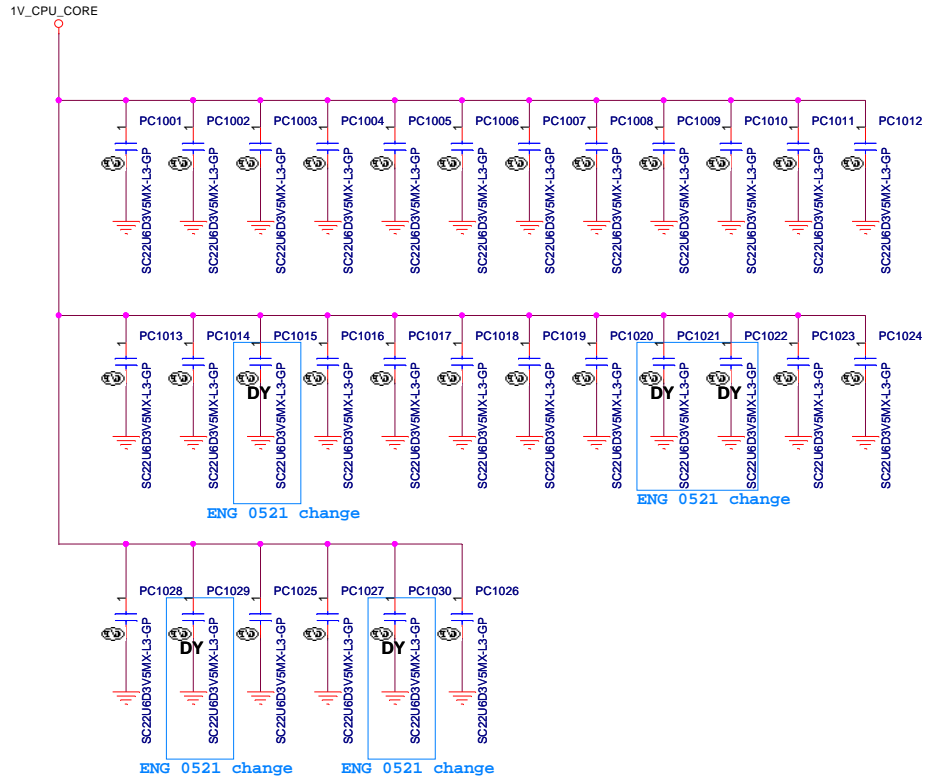
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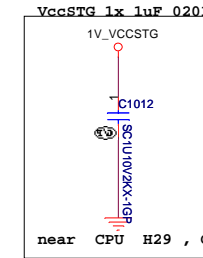
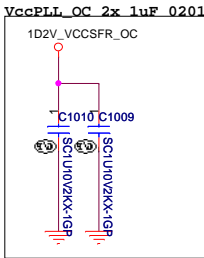
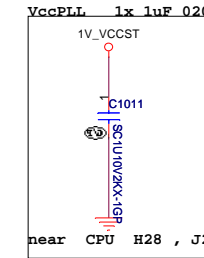
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VR: +/-5% or +/-50mV
Place close to VR output



JJ 20150130

Decoupling Requirements for SKL H Processor (Sheet 2 of 2)

Domain	Board Edge cap	Backside cap	Notes
VccGT	6x 47uF 0805	8x 22uF 0603	
		35x 10uF 0402	
		68x 1uF 0201	
VccTx	8x 22uF 0603	4x 10uF 0402	
		12x 1uF 0201	
VccSA	1x 47uF 0805	1x 47uF 0805	
		7x 10uF 0402	
		3x 1uF 0201	
VDDQ	4x 22uF 0603	10x 10uF 0402	Share supply with DRAM
VDDQC		1x 10uF 0402	
VccIO	2x 47uF 0805	3x 10uF 0402	VR: +/-5% or +/-50mV Place close to VR output
		1x 1uF 0201	
VccST		1x 1uF 0201	
VccSTG		1x 1uF 0201	Share supply with 1.0V PCH rail
VccPLL		1x 1uF 0201	
VccPLL_OC		2x 1uF 0201	Supply from 1.2V VDDQ
VccCORC		10x 10uF 0402	VR: +/-5% or +/-50mV
VccPPRO		3x 10uF 0402	VR: +/-5% or +/-50mV

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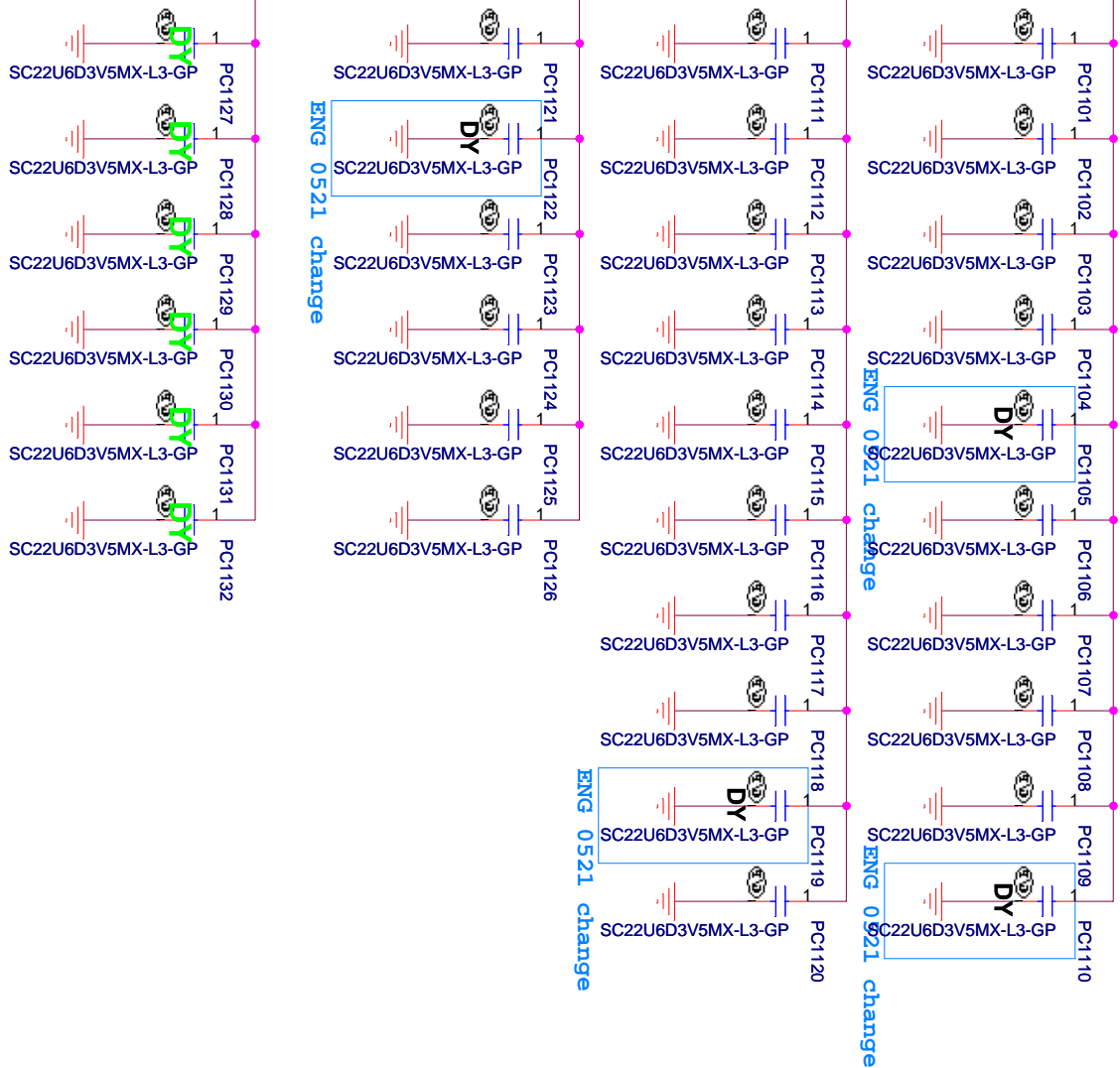
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Title: **010 CPU (Power CAP1)**

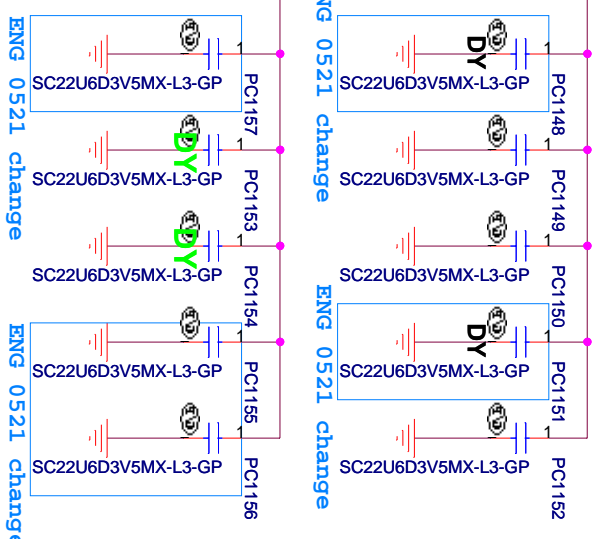
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1V_VCCGT



1V_VCCSA



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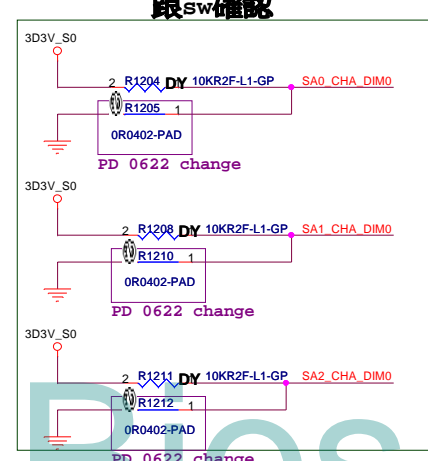
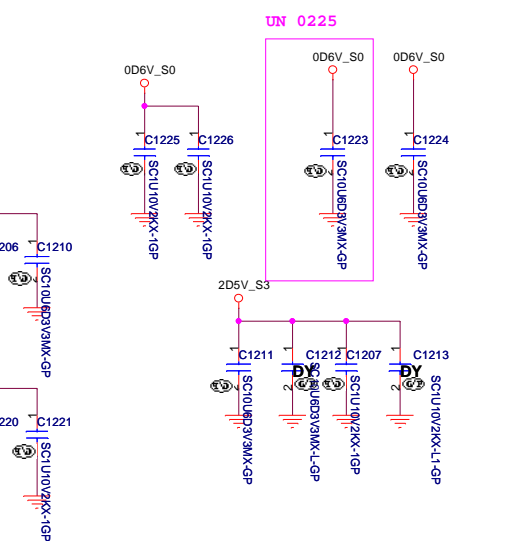
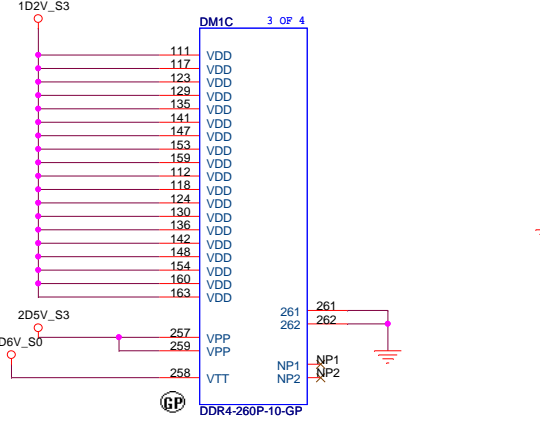
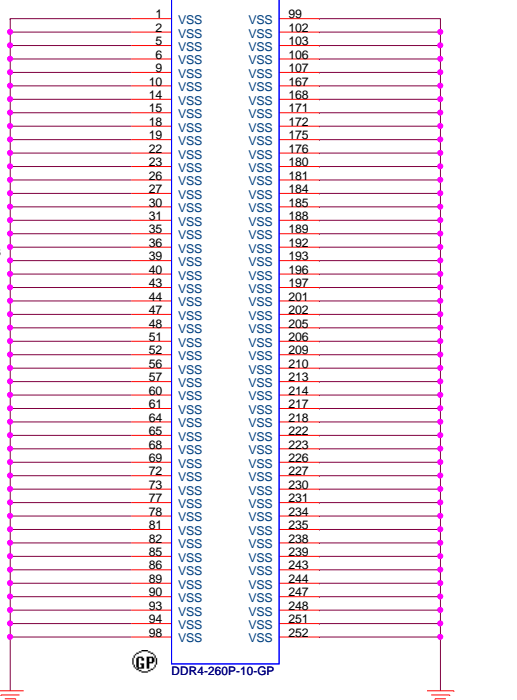
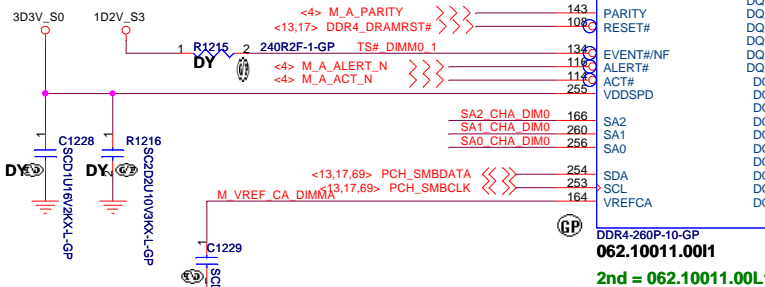
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Title **CPU (Power CAP2)**

Size A4 Document Number **Newgate** Rev **1M**

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DDR4 SWAP 0212

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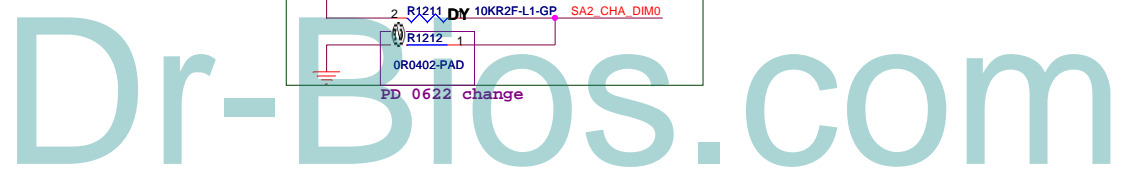
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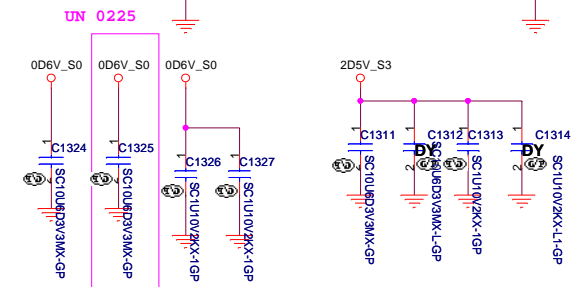
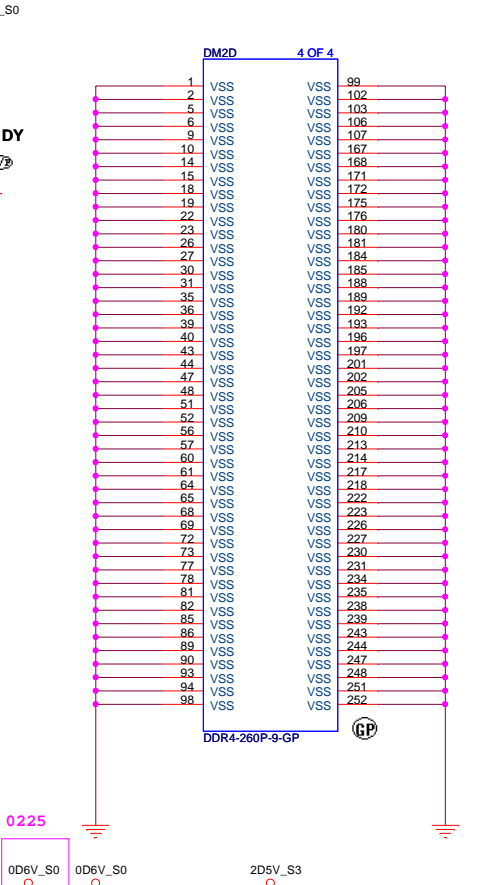
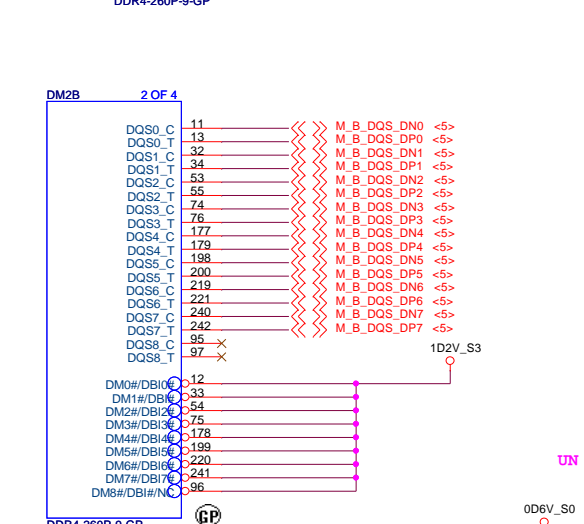
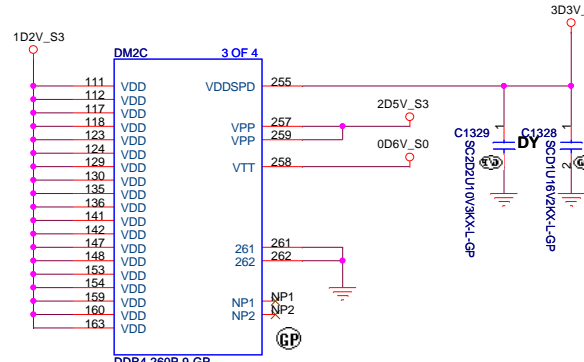
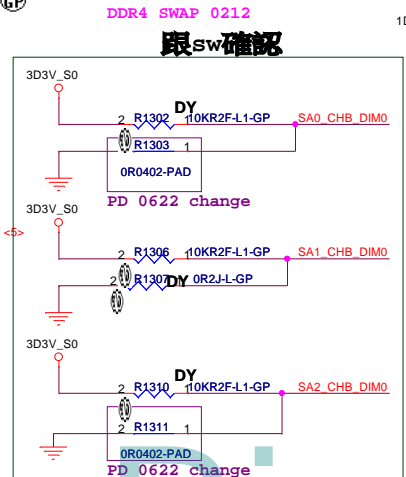
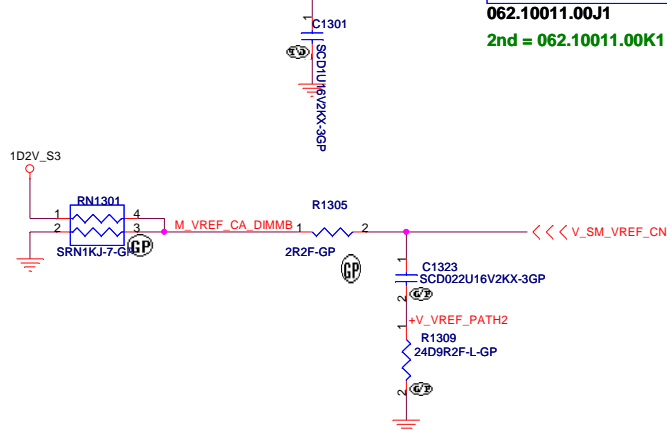
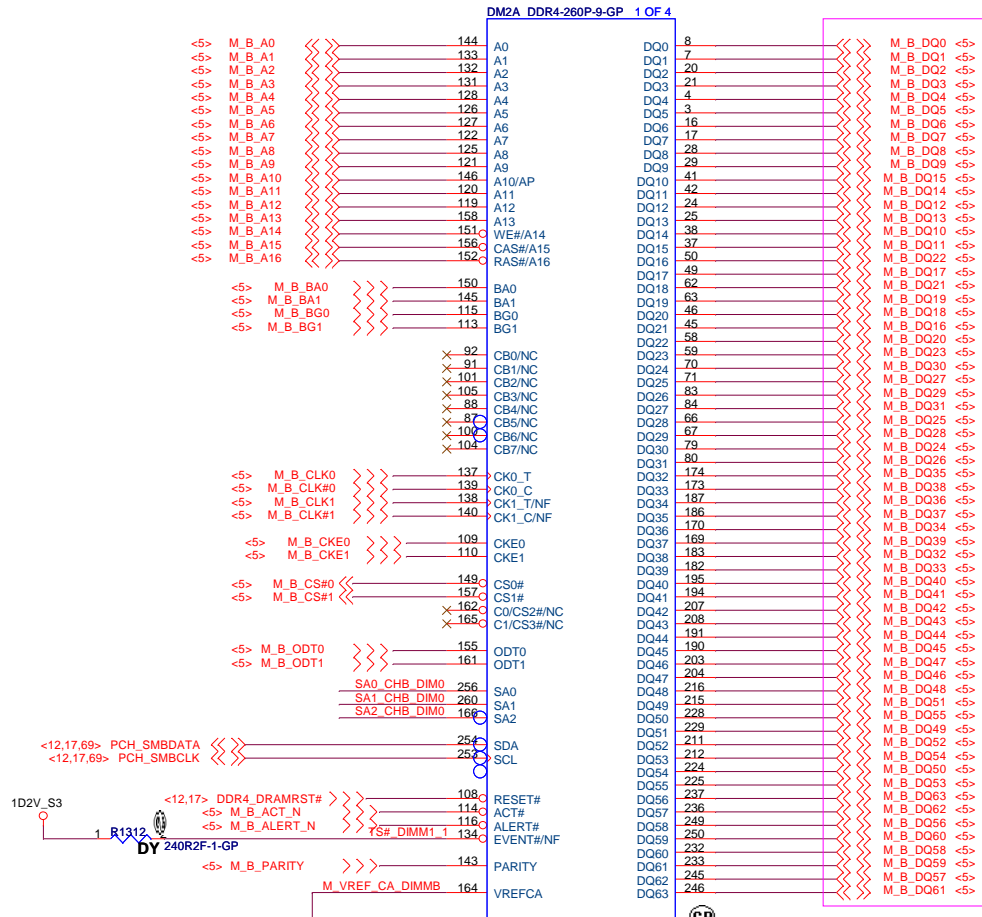
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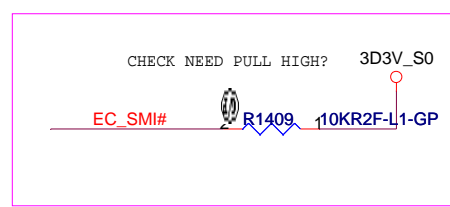
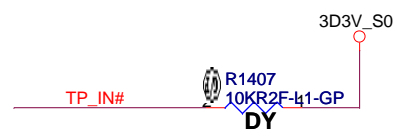
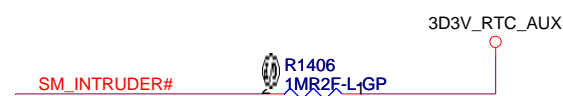
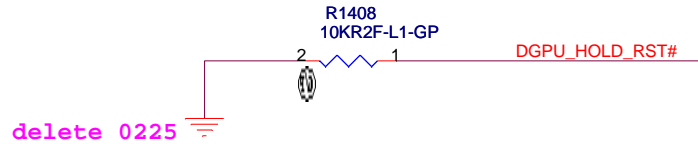
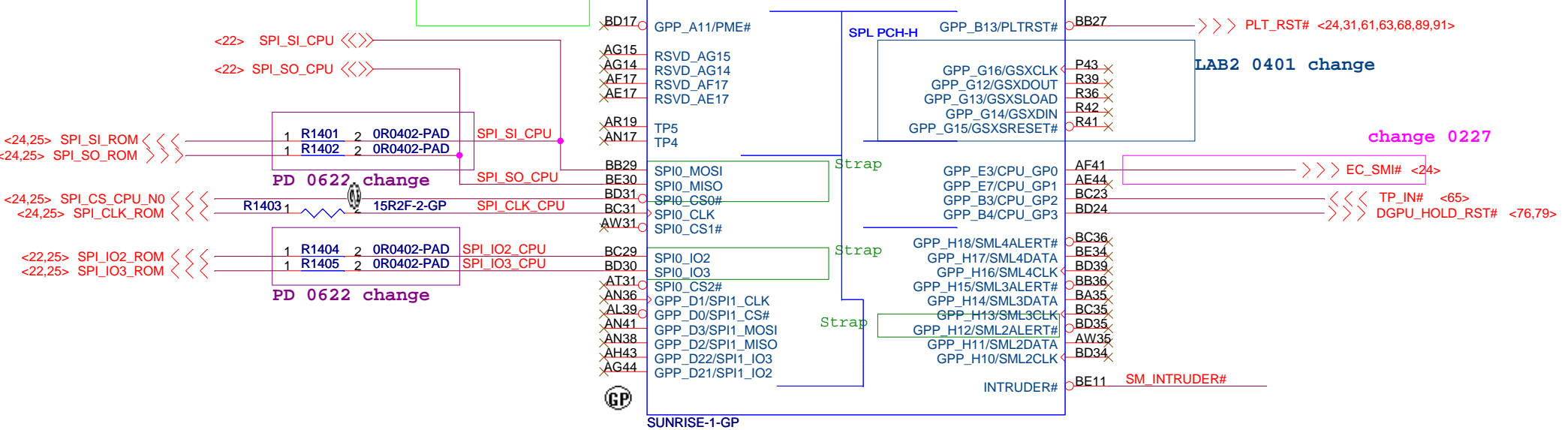
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File: **DDR3-SODIMM2**

Size A3 Document Number **Newgate** Rev **1M**

Date: Thursday, August 13, 2015 Sheet 13 of 105

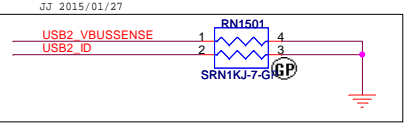
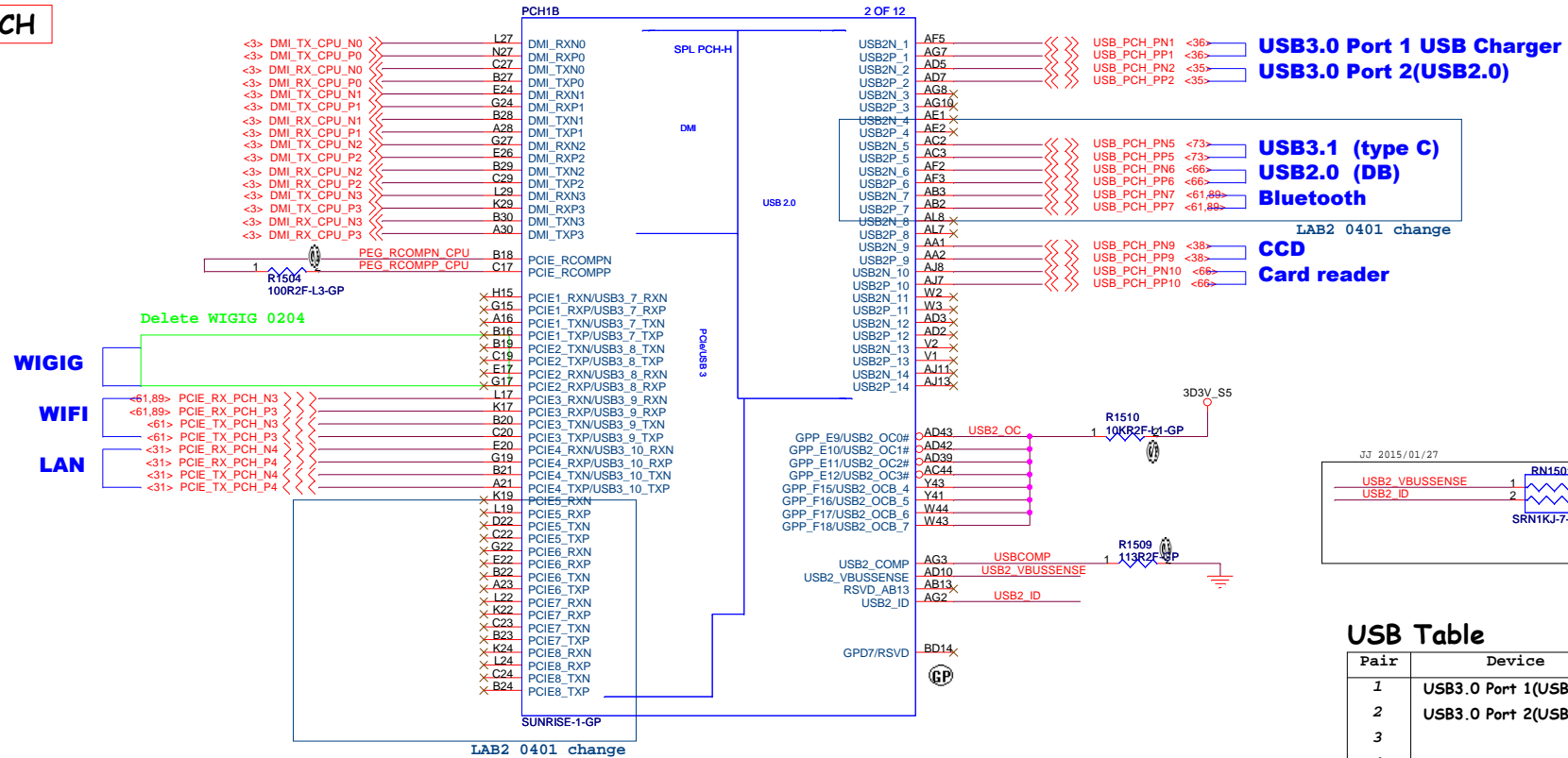


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Title PCH GPP1			
Size A4	Document Number Newgate		Rev 1M
Date: Thursday, August 13, 2015	Sheet 14	of 1	105

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SSID = PCH



USB Table

Pair	Device
1	USB3.0 Port 1(USB2.0) Charger
2	USB3.0 Port 2(USB2.0)
3	
4	
5	USB2.0
6	
7	Bluetooth
8	Touch Screen
9	CCD
10	Card reader
11	Finger Printer
12	
13	
14	

<Core Design>

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Title: **PCH PCIE DMI USB**

Size A3 Document Number: **Newgate** Rev **1M**

Date: Thursday, August 13, 2015 Sheet 15 of 105

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SSID = PCH

Delete WIGIG 0204

change 0227

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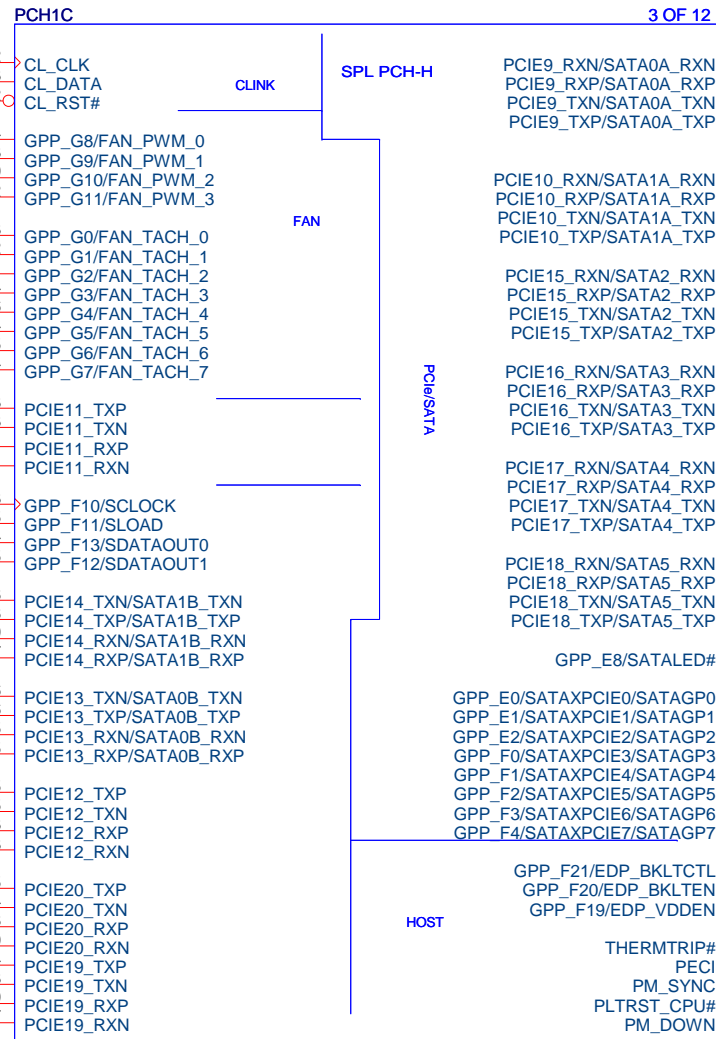
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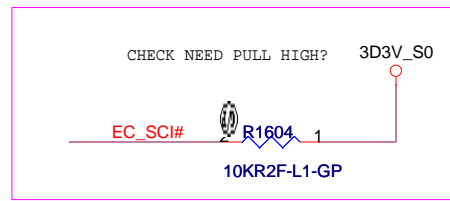
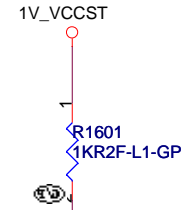
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UN 0225



SUNRISE-1-GP



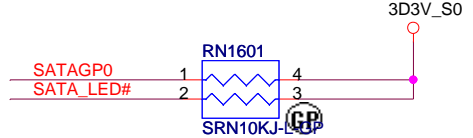
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HDD



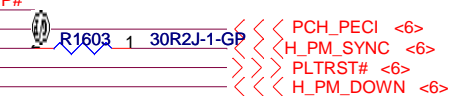
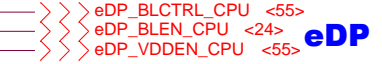
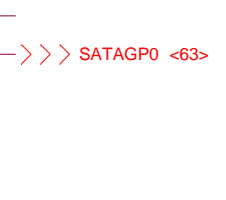
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HOST



change 0227



PCH_THERMTRIP# R1602_1 620R2F-GP

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AROUND PCH

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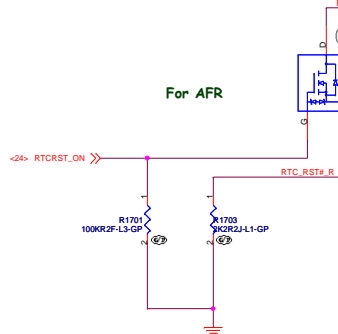
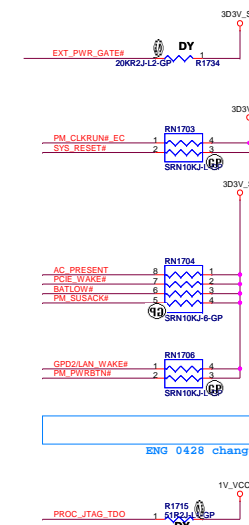
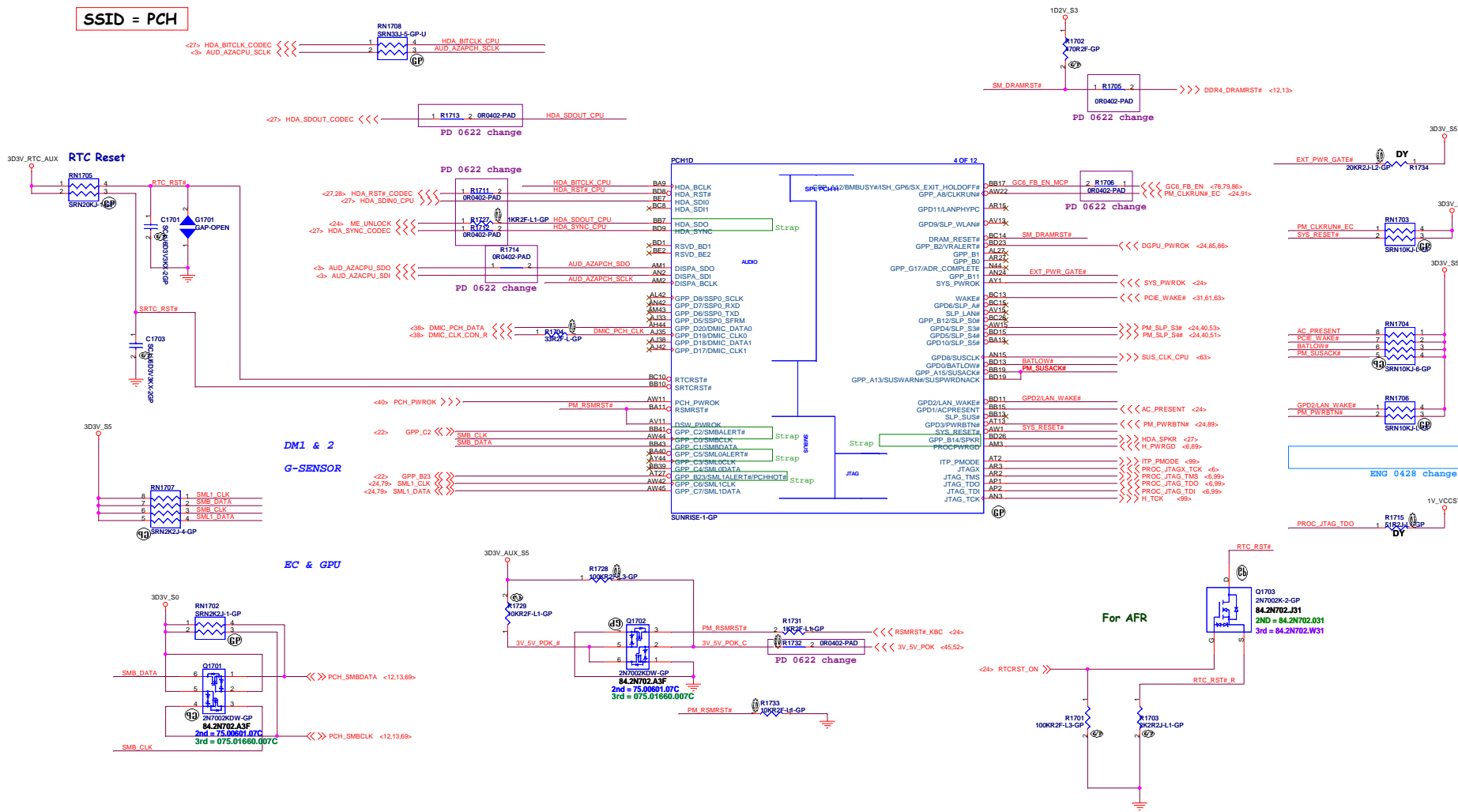
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Title PCH_PCIE_SATA

Size A4 Document Number Rev 1M

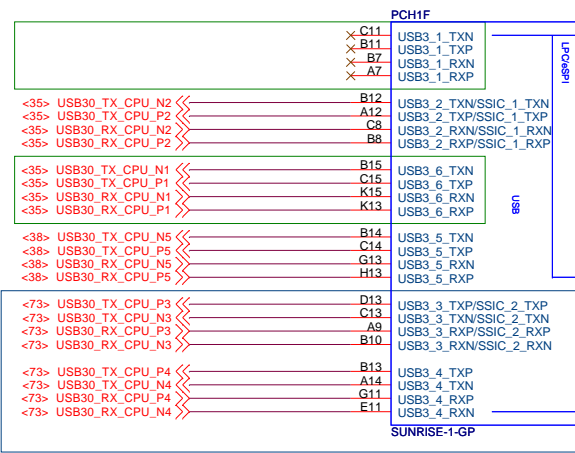
Date Thursday, August 13, 2015 Sheet 16 of 105

SSID = PCH



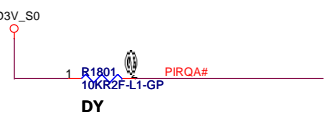
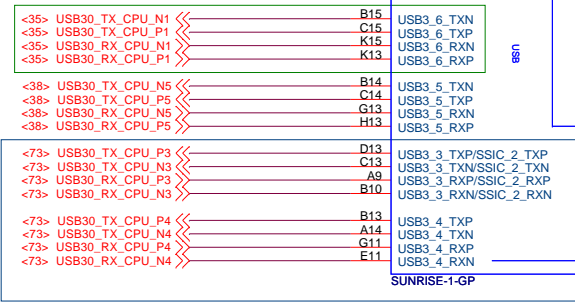
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MP 0807 change

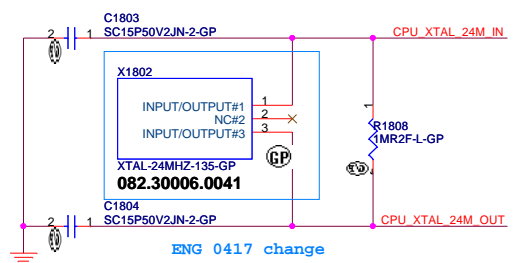
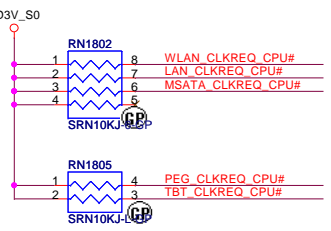


LAB2 0401 change

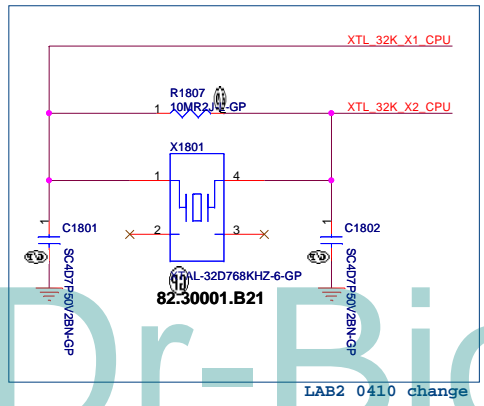
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DY

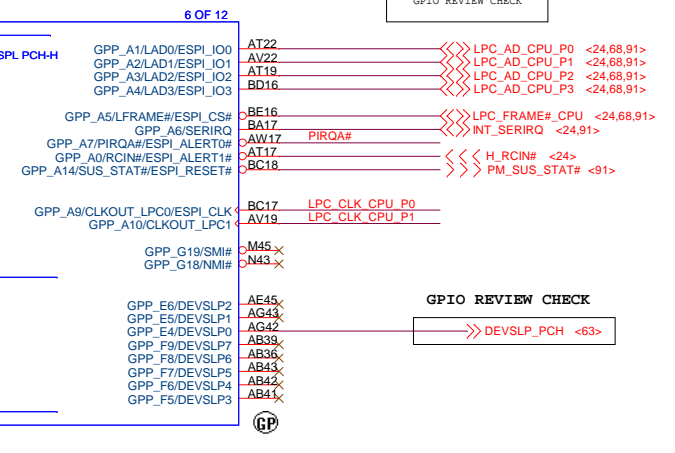


ENG 0417 change



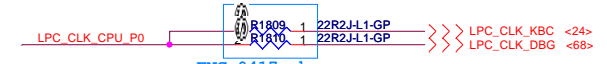
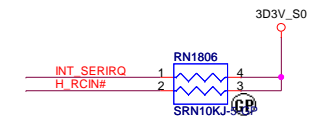
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GPIO REVIEW CHECK

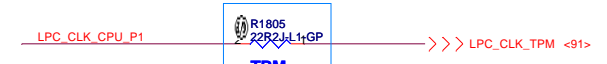


GPIO REVIEW CHECK

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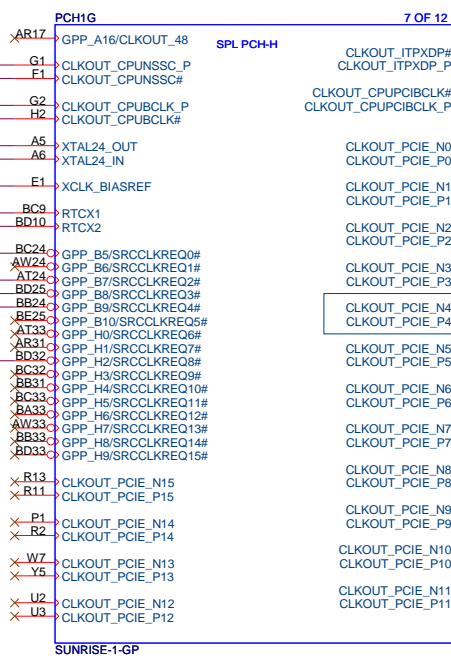
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TPM
ENG 0417 change

PEG CLOCK CHECK WITH SW

CHECK P and N



LAB2 0401 change

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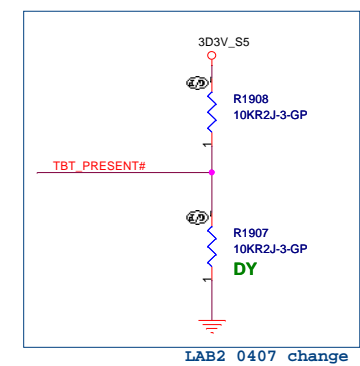
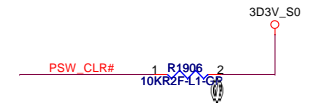
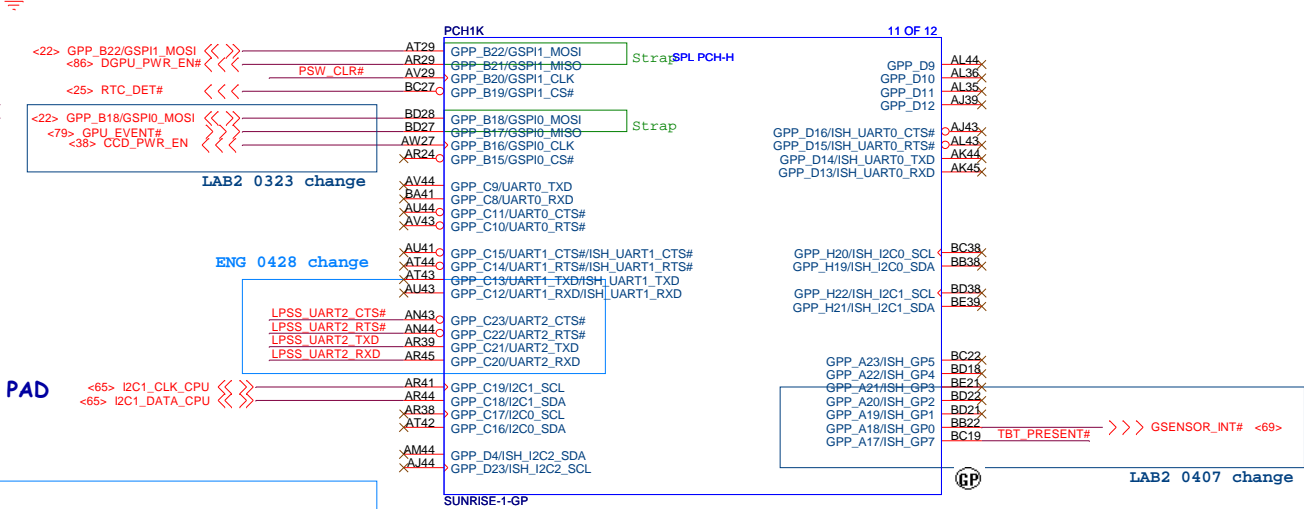
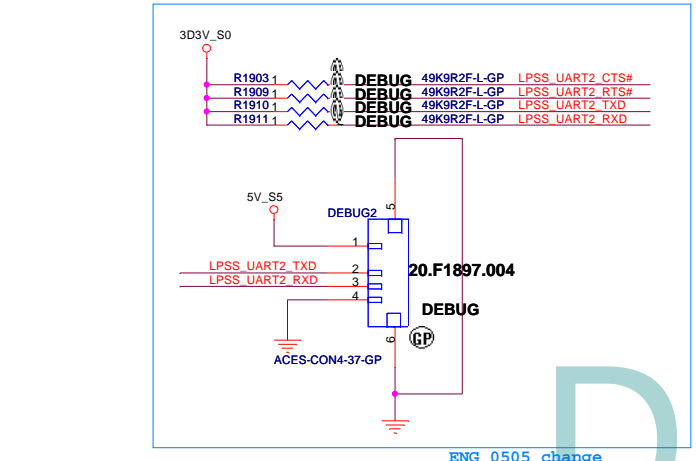
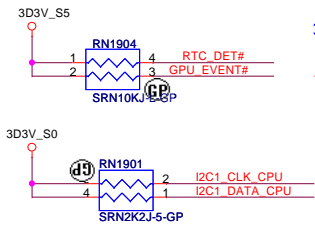
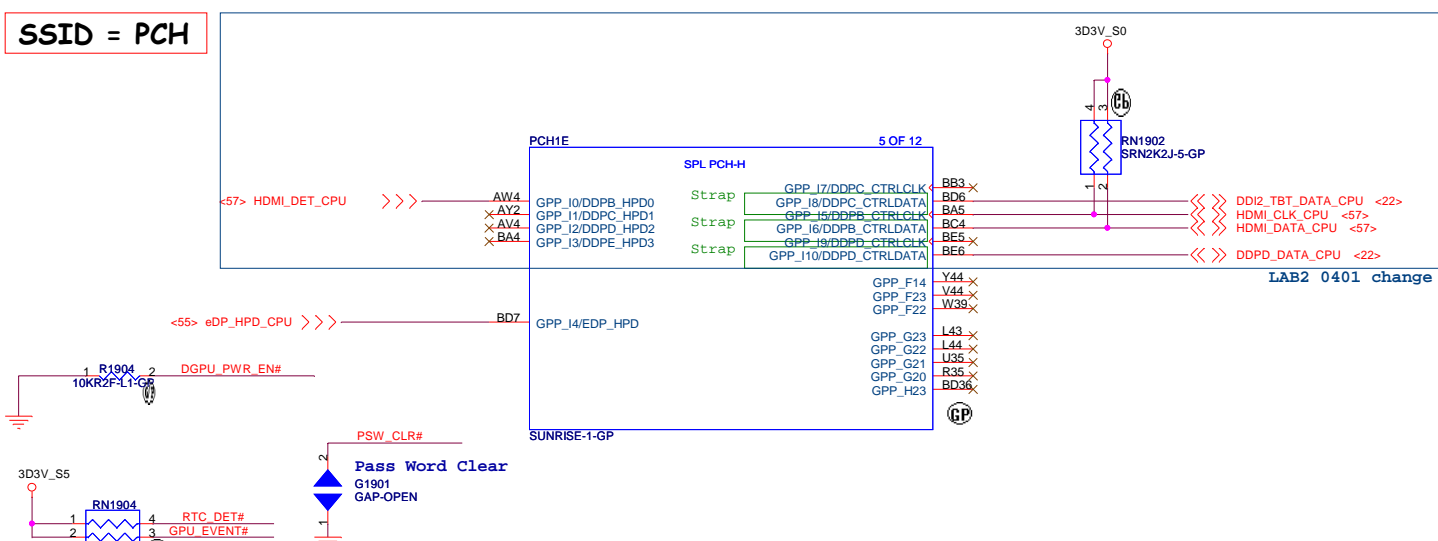
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Title			PCH USB3 CLOCK		
Size	Document Number	Newgate		Rev	1M
A3					
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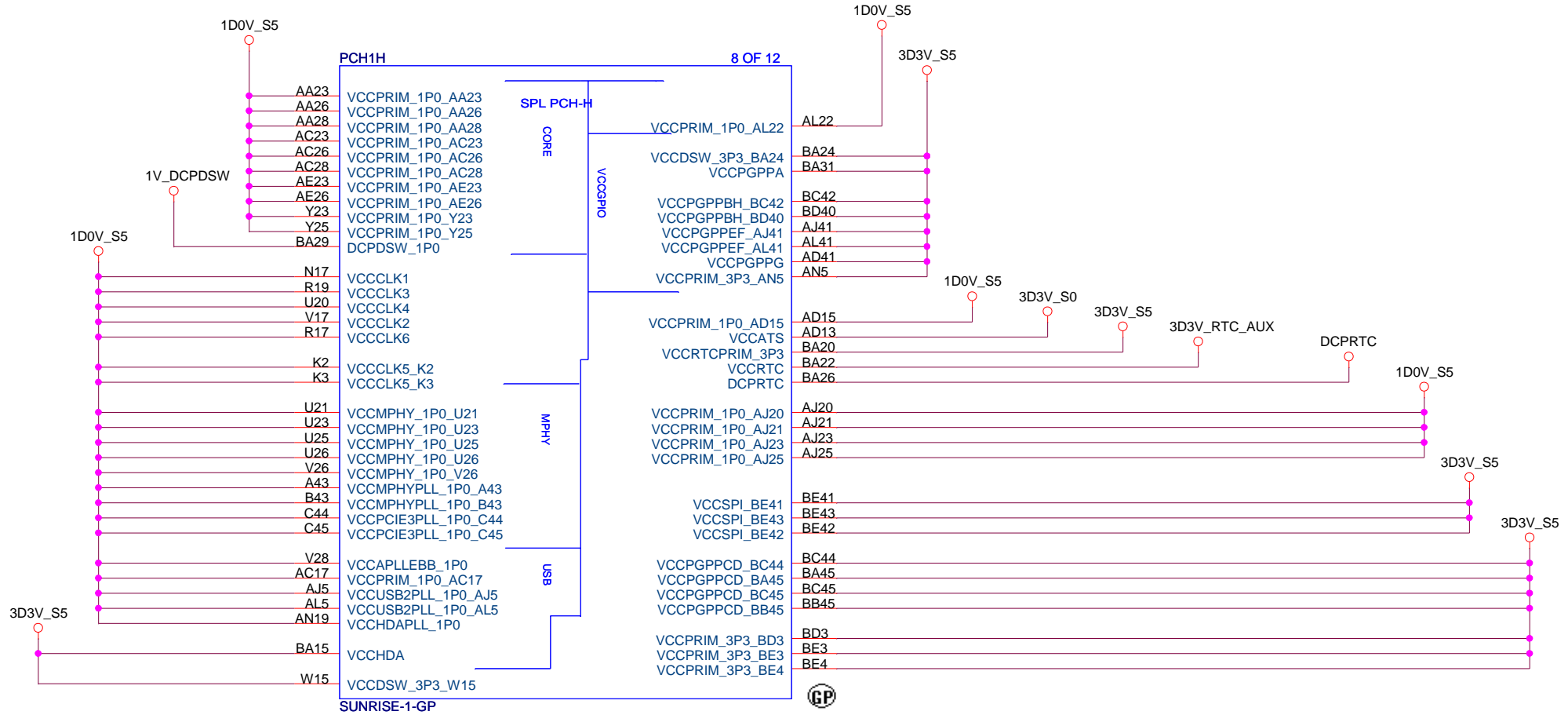
SSID = PCH



TBT_PRESENT#	HIGH	LOW
	NON TBT	WITH TBT

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SSID = PCH



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Title **PCH POWER_VCCPRIM_VCCMPHY**

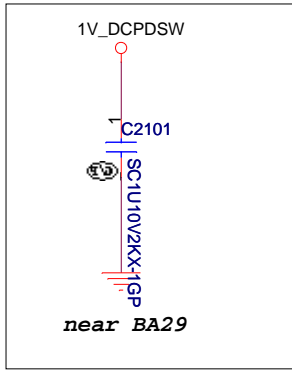
Size A4 Document Number **Newgate** Rev **1M**

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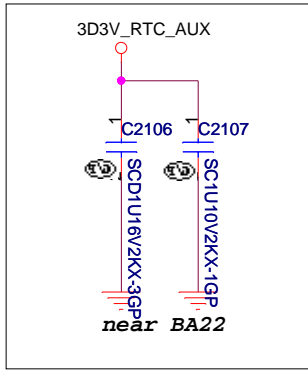
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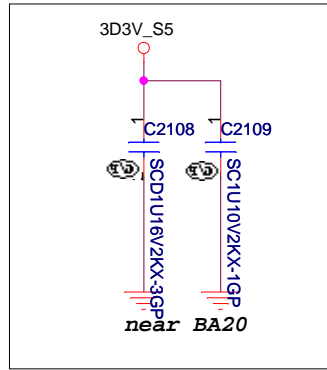
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1x 1uF



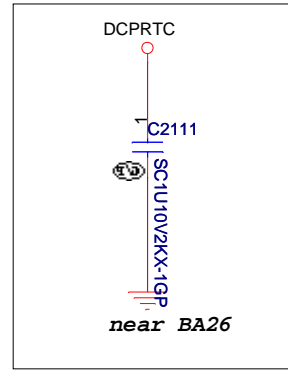
VccRTC
1x1 uF 1x0.1 uF



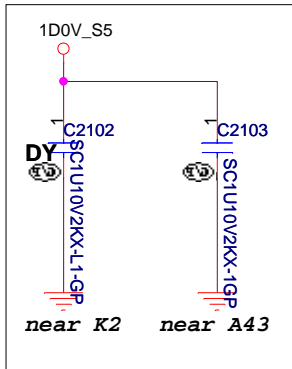
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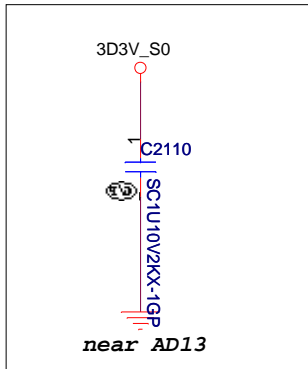
DcpRTC
1x 0.1uF



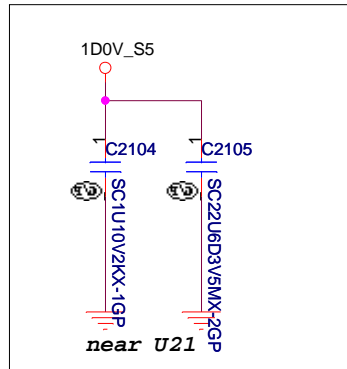
VccMPHYPLL / VccPCIE3PLL
1x1 uF



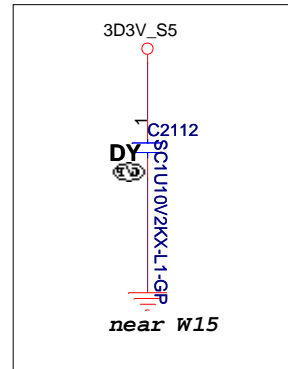
VccATS
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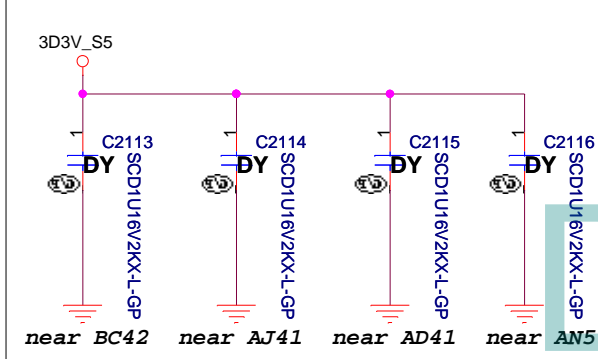
VccMPHY / VccPRIM / VccAPLLEBB
1x1 uF 1x22 uF



VccDSW
1x 1uF



VccPGPPBCH / VccPGPPEF / VccPGPPG / VccPRIM
4x 0.1 uF




Decoupling and Power Connection Requirements for SKL 5/H PCH (DT / AIO)
(Sheet 1 of 2)

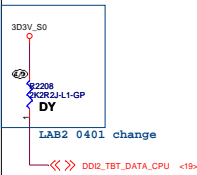
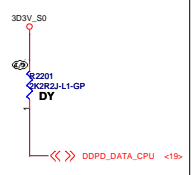
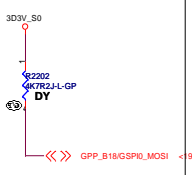
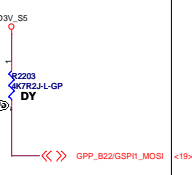
Voltage Supply	Area	PCH Pins sharing power rail	Value	Size	Quantity	Placement type (R/Jumper / E/Edge)	Place capacitor(s) near ball(s)
V1.0A	VccMPHY VccPRIM VccAPLLEBB	U21, U23, U25, U26, V26, AC17, V28	1 uF	0402	1	E (<3 mm)	U21
	VccMPHYPLL VccPCIE3PLL	A43, B43, C44, C45	22 uF	0805	1	E (<5 mm)	A43
	VccCLK5	K2, K3	1 uF	0402	1	E (<5 mm)	K2 (Note 1)
	VccCLK (1,2,3,4,6)	N17, R19, U20, V17, R17	-	-	-	-	-
	VccUSB2PLL VccHDAPLL	AJ5, AL5, AN19	-	-	-	-	-
	VccPRIM	AL22	-	-	-	-	-
	VccPRIM	AD15	-	-	-	-	-
	VccPRIM	AJ20, AJ21, AJ23, AJ25	-	-	-	-	-
	VccPRIM	AA23, AA26, AA28, AC13, AC26, AC28, AE23, AE26, Y23, Y25	-	-	-	-	-
	V1.0DS W	DcpD5W	BA29	1 uF	0402	1	E (<5 mm)
V1.8A/ V3.3A	VccPGPPBCH	BC42, BD40	0.1 uF	0402	1	E (<3 mm)	BC42 (Note 1)
	VccPGPPEF	AJ41, AL41	0.1 uF	0402	1	E (<3 mm)	AJ41 (Note 1)
	VccPGPPG	AD41	0.1 uF	0402	1	E (<3 mm)	AD41 (Note 1)
	VccPRIM	AN5	0.1 uF	0402	1	E (<3 mm)	AN5 (Note 1)
	VccPGPPA	BA31	-	-	-	-	-
V1.8A/ V1.85/ V3.3S	VccSPT	BE41, BE42, BE43	-	-	-	-	-
	VccPGPPD	BC44, BA45, BC45, BB45	-	-	-	-	-
	VccATS	AD13	1 uF	0402	1	E (<5 mm)	AD13
V1.5A/ V1.8A/ V3.3A	VccHDA	BA15	-	-	-	-	
V3.3A	VccRTCPRIM	BA20	1 uF	0402	1	E (<5 mm)	BA20
	VccPRIM	BD3, BE3, BE4	0.1 uF	0402	1	E (<3 mm)	-
V3.3RTC	VccRTC	BA22	1 uF	0402	1	E (<5 mm)	BA22
	VccDSW	W15	0.1 uF	0402	1	E (<3 mm)	-
V3.3DS W	VccDSW	W15	1 uF	0401	1	E (<3 mm)	W15 (Note 1)
	VccDSW	BA24	-	-	-	-	-
PCH Internal VRM	DcpRTC	BA26	0.1 uF	0402	1	E (<5 mm)	BA26

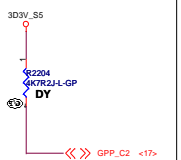
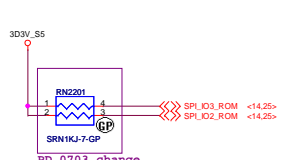
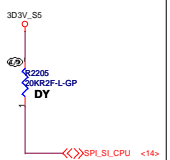
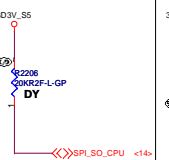
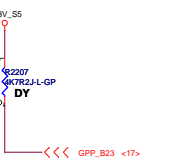
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PCH_POWER_CAP1	
Title	Document Number
Size A4	Rev 1M
Date: Wednesday, August 12, 2015	Sheet 21 of 105

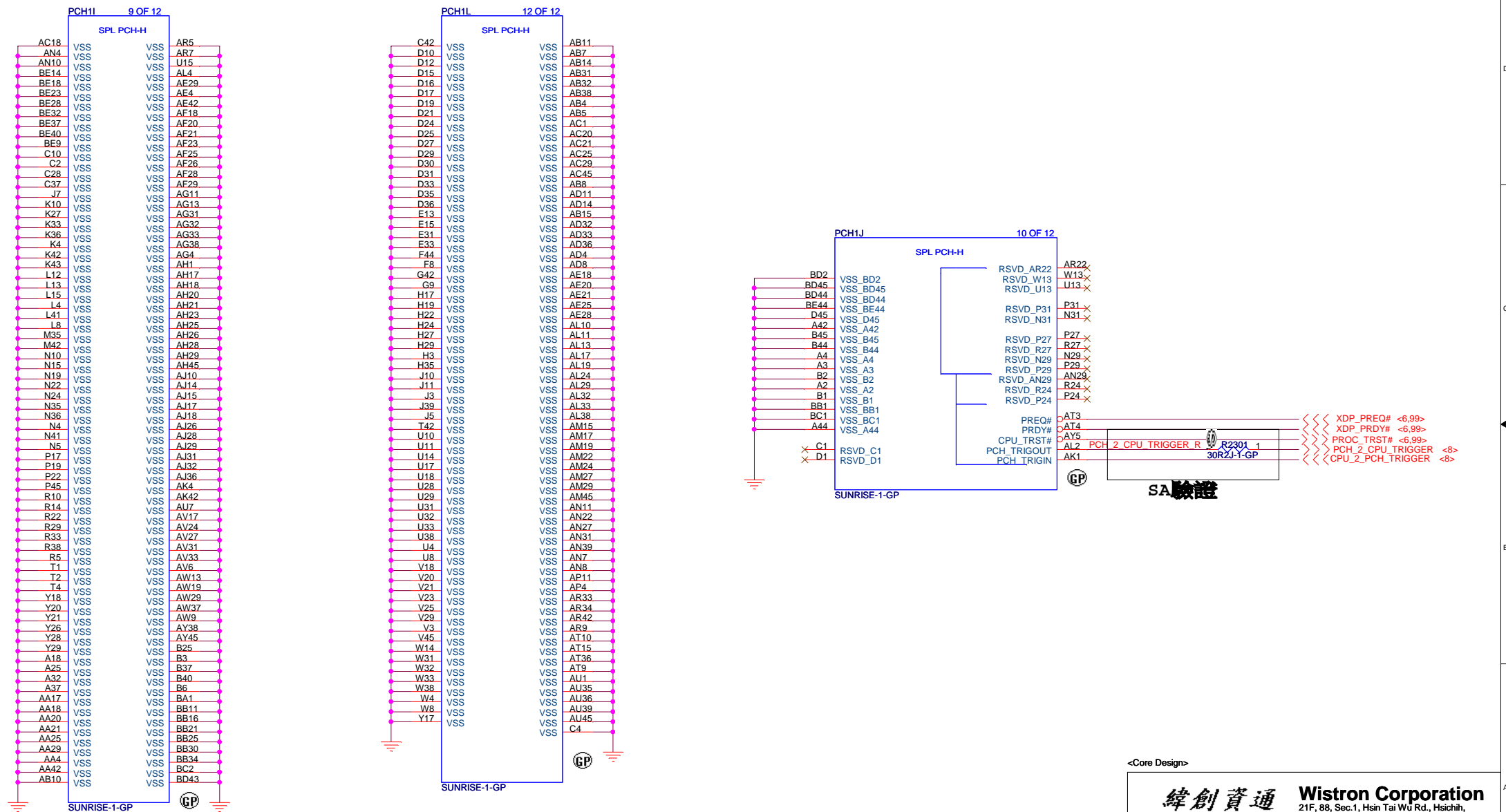
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Description	Display Port B Detected	Display Port C Detected	Display Port D Detected	No reboot	Boot BIOS strap bit BBS	Flash descriptor security override	ESPI FLASH SHARING MODE
GPIO	GPP_I6	GPP_I8	GPP_I10	GPP_B18	GPP_B22	HDA_SDO	GPP_H12
Schematic	Pull up at p.71 RV7101 						
High	Detected	Detected	Detected	Enable	LPC	Disable	1: SLAVE ATTACHED FLASH SHARING ESPI FLASH SHARING MODE
Low	Not Detected	Not Detected	Not Detected	Disable	SPI	Enable	0: MASTER ATTACHED FLASH SHARING
	internal pull-down	internal pull-down	internal pull-down	internal pull-down	internal pull-down	internal pull-down	internal pull-down

Description	Top Swap Override	eSPI or LPC	TLS Confidentiality	Reserved	Reserved	Reserved	Reserved	Reserved
GPIO	GPP_B14	GPP_C5	GPP_C2	SPIO_IO3	SPIO_IO2	SPIO_MOSI	SPIO_MISO	GPP_B23
Schematic								
High	Enable	eSPI	Enable					
Low	Disable	LPC	Disable					
	internal pull-down	internal pull-down	internal pull-down	internal pull-up	internal pull-up	internal pull-up	internal pull-up	internal pull-down

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SSID = PCH



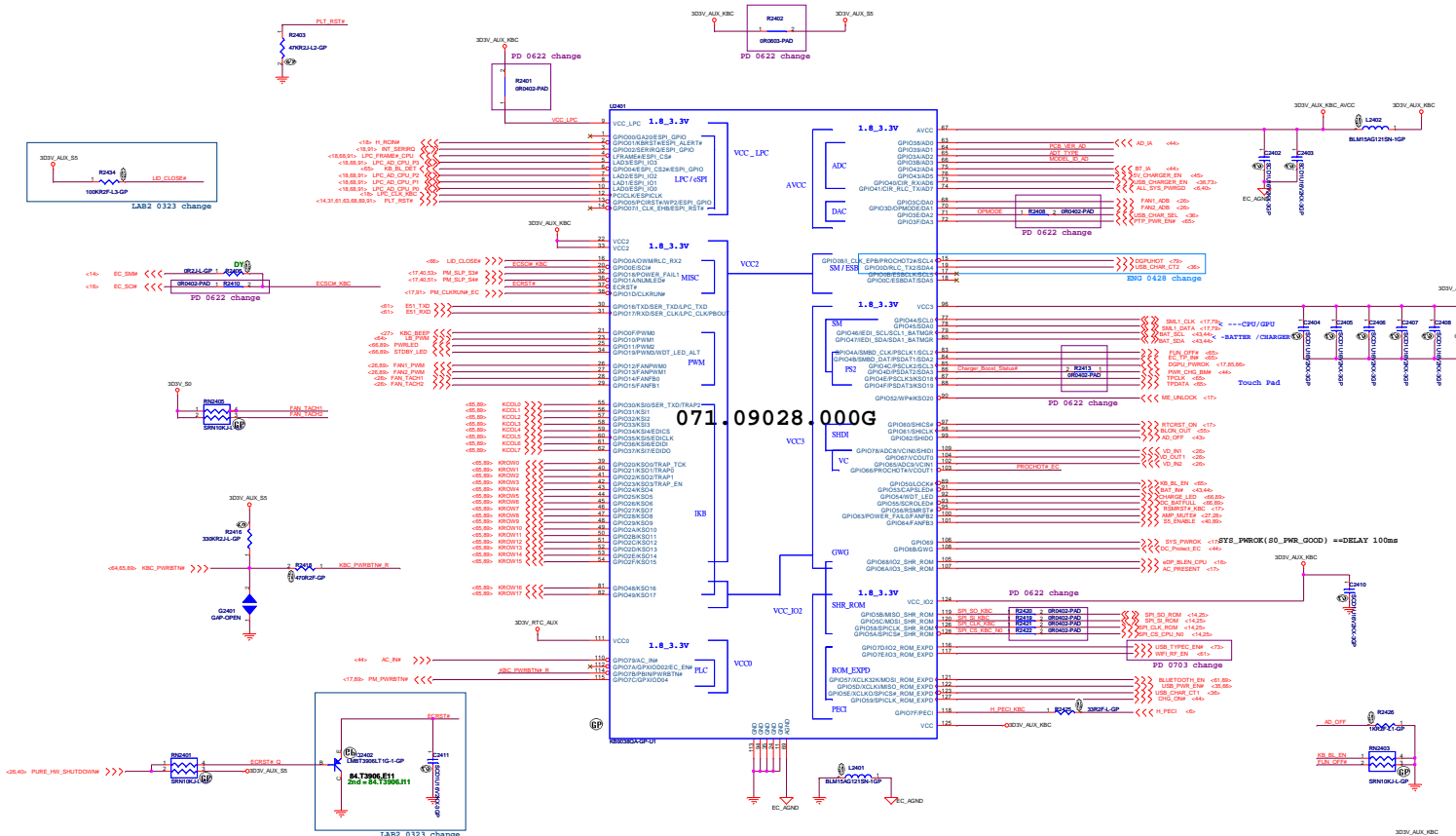
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Title: **PCH_RSVD_VSS**

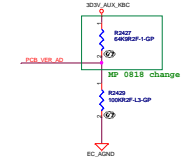
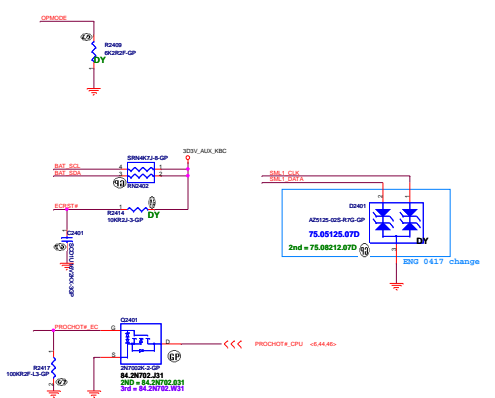
Size B Document Number: **Newgate** Rev: **1M**

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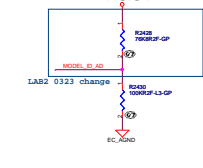


OPMODE (Pin70): PU (Default:eSPI)
OPMODE(Default/Internal PU):

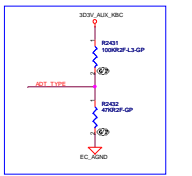
EC9028	ASB(LPC)
EC9038	DT(4091)



Pin No./Alt	Pull-Up Register	Pull-High Register	Typical Voltage	Max Voltage	IOC Firmware Setting
5A	100.0 K	10.0 K	3.000 V	3.000 V	=>2.975 V
5B	100.0 K	20.0 K	2.750 V	2.750 V	=>2.875 V
5C	100.0 K	33.0 K	2.617 V	2.617 V	=>2.918 V
5D	100.0 K	47.0 K	2.500 V	2.500 V	=>2.930 V
5E	100.0 K	68.0 K	2.371 V	2.371 V	=>1.931 V
Reserved for project use	100.0 K	76.0 K	1.807 V	1.807 V	=>1.759 V
Reserved for project use	100.0 K	100.0 K	1.650 V	1.650 V	=>1.750 V
Reserved for project use	100.0 K	140.0 K	1.589 V	1.589 V	=>1.524 V
Reserved for project use	100.0 K	174.0 K	1.281 V	1.281 V	=>1.231 V
Reserved for project use	100.0 K	215.0 K	1.048 V	1.048 V	=>0.924 V

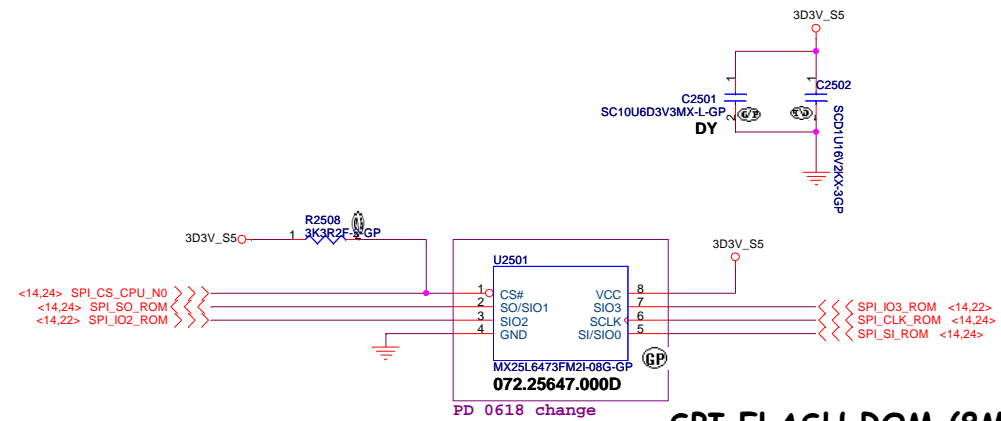


MODEL_B_05	Pull-Up Register	Pull-High Register	Typical Voltage
Rayleigh-SL_UMA	100.0 K	10.0 K	3.000 V
Rayleigh-SL_945M	100.0 K	20.0 K	2.750 V
Rayleigh-SL_950M	100.0 K	33.0 K	2.481 V
Rayleigh-SLS_950M	100.0 K	47.0 K	2.245 V
Newgate-SLS_945M	100.0 K	64.0 K	2.001 V
Newgate-SLS_950M	100.0 K	76.0 K	1.887 V
Newgate-SLS_950M	100.0 K	100.0 K	1.650 V
Reserved for project use	100.0 K	143.0 K	1.358 V
Reserved for project use	100.0 K	174.0 K	1.204 V
Reserved for project use	100.0 K	215.0 K	1.048 V



Pin No./Alt	Pull-Up Register	Pull-High Register	Typical Voltage	Max Voltage	IOC Firmware Setting
69V	NA	100.0 K	3.000 V	3.000 V	=>3.000 V
30V	100.0 K	NA	0.800 V	0.800 V	=>0.785 V
30V	10.0 K	100.0 K	0.900 V	0.900 V	=>0.900 V
45V	20.0 K	100.0 K	0.950 V	0.950 V	=>0.884 V
120V	33.0 K	100.0 K	0.918 V	0.918 V	=>0.907 V
150V	47.0 K	100.0 K	1.050 V	1.050 V	=>1.177 V
150V	68.0 K	100.0 K	1.281 V	1.281 V	=>1.177 V
Reserved	76.0 K	100.0 K	1.431 V	1.431 V	=>1.365 V
Reserved	100.0 K	100.0 K	1.552 V	1.552 V	=>1.542 V

SSID = Flash.ROM SPI FLASH ROM (8M byte) for PCH



SPI FLASH ROM (8M byte) for PCH

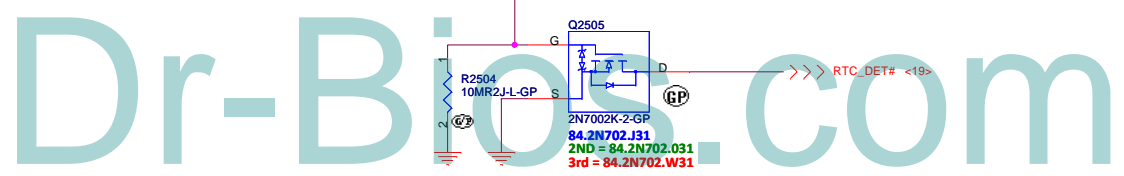
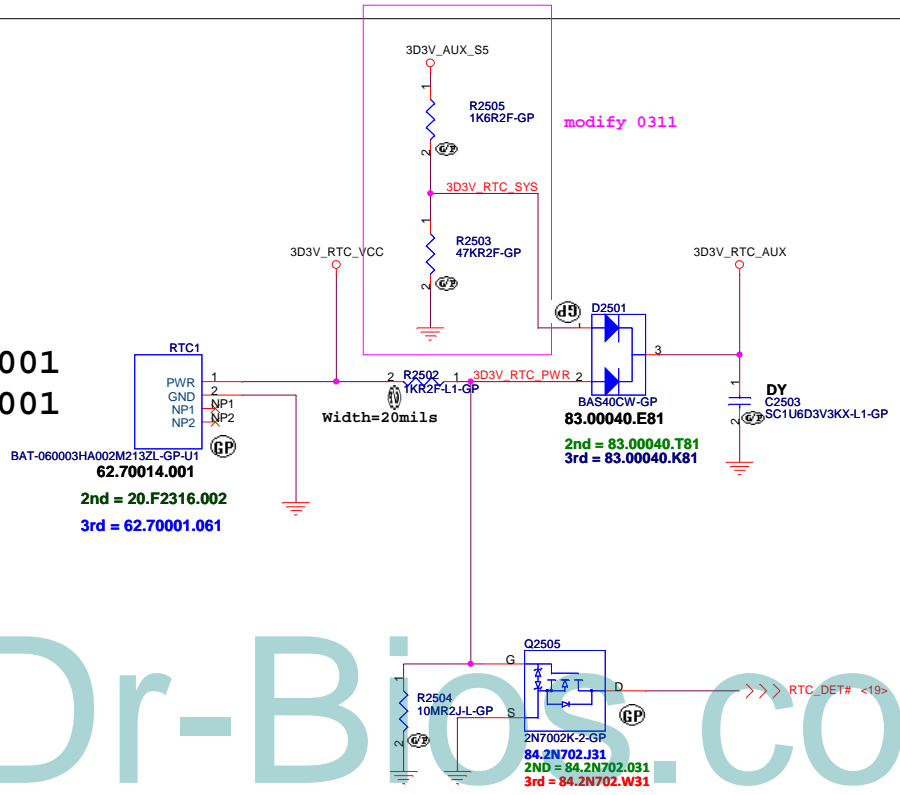
SPI ROM Equal length need to less than 500mil

SPI FLASH ROM (8M byte)

1st = 072.25647.000D (MXIC MX25L6473FM2I-08G)
2nd= 072.25Q64.0F01 (MICRON N25Q064A13ESED0F)
3rd= 72.25Q64.K01 (WINBOND W25Q64FVSSIQ)

Main Func = RTC

RTC BATTERY
1st= 23.22065.001
2nd= 23.20068.001



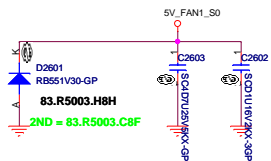
SSID = Thermal

ADB (Active Dusting Blower) function

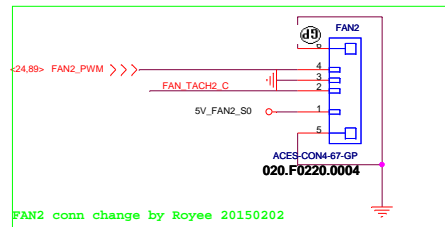
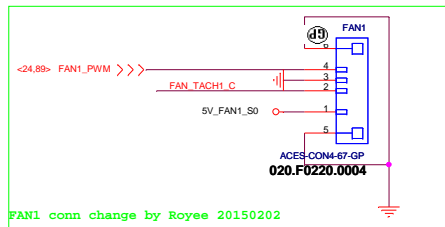
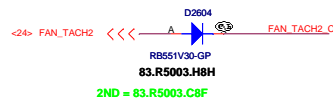
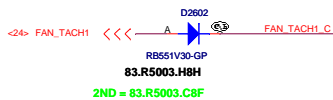
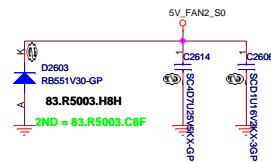
AFTP TESTPOINT



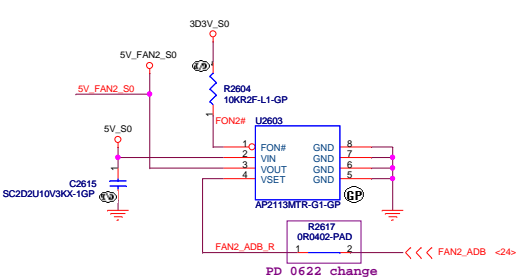
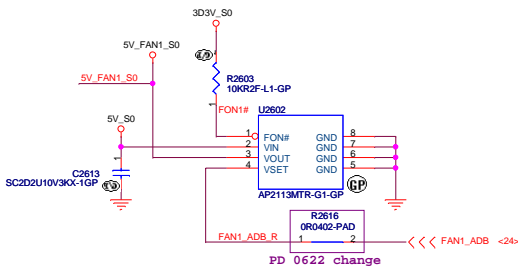
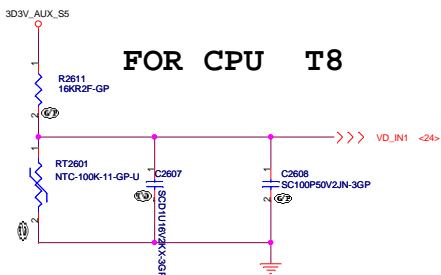
Layout 15 mil



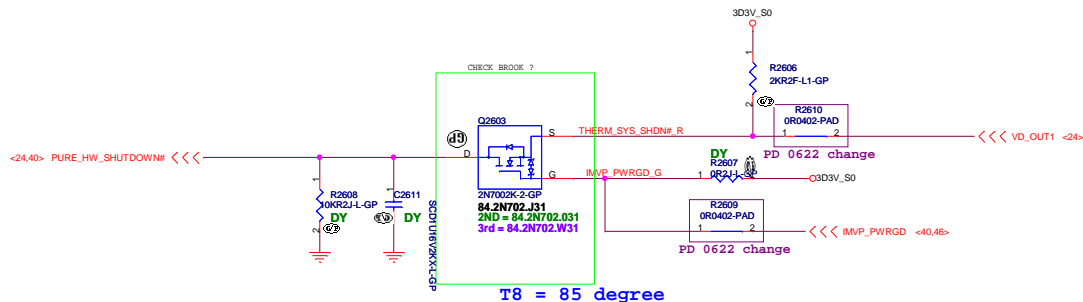
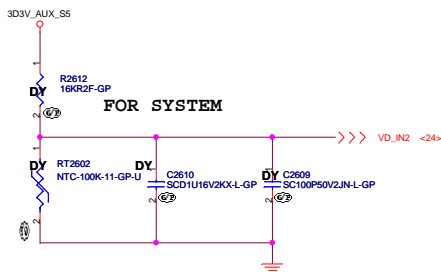
Layout 15 mil



FOR CPU T8



FOR SYSTEM

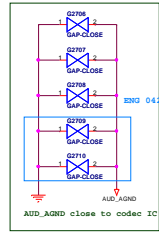
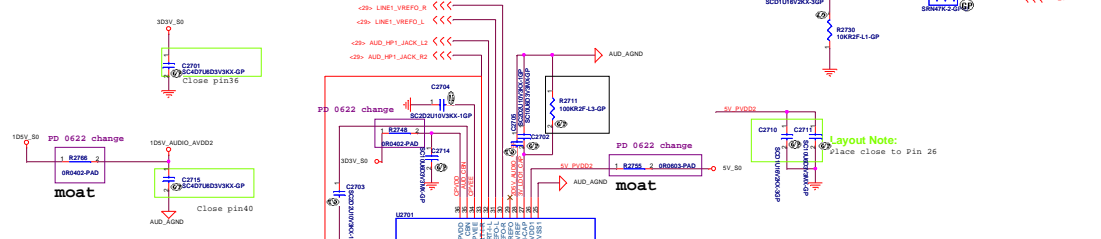
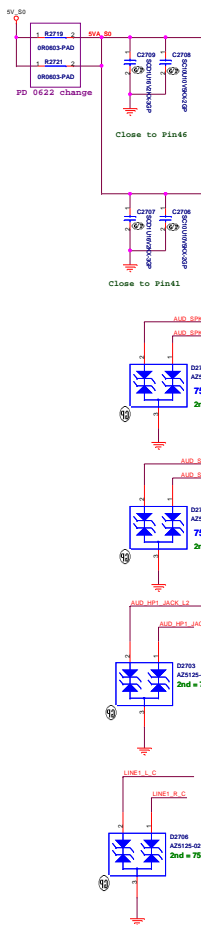


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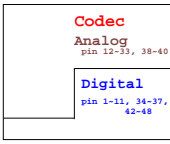
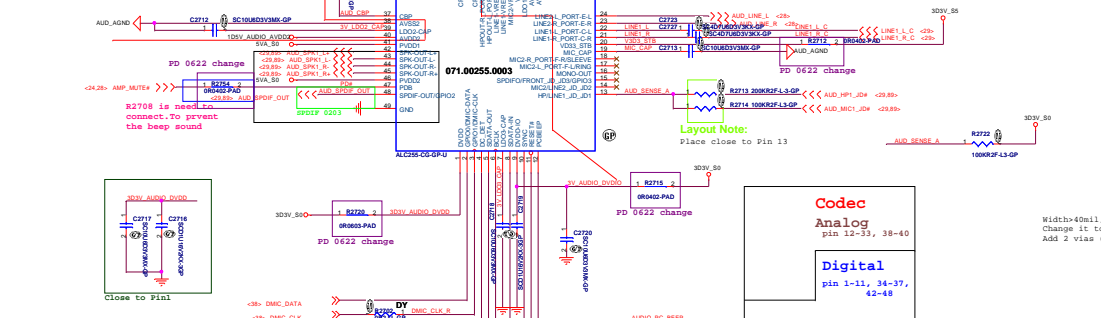
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File Thermal T8 and FAN
Size Document Number Rev 1M
Customer Newgate
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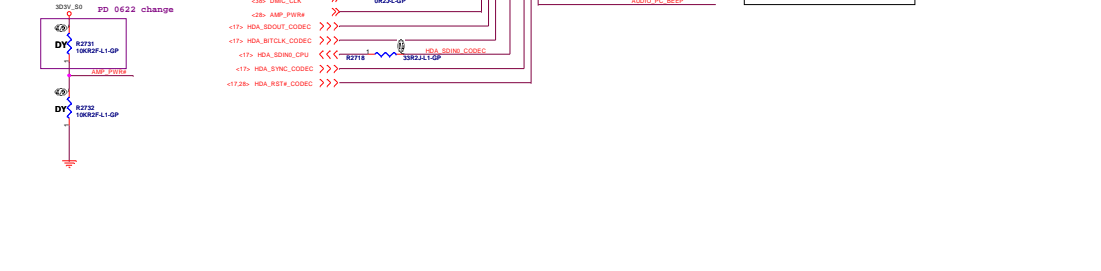


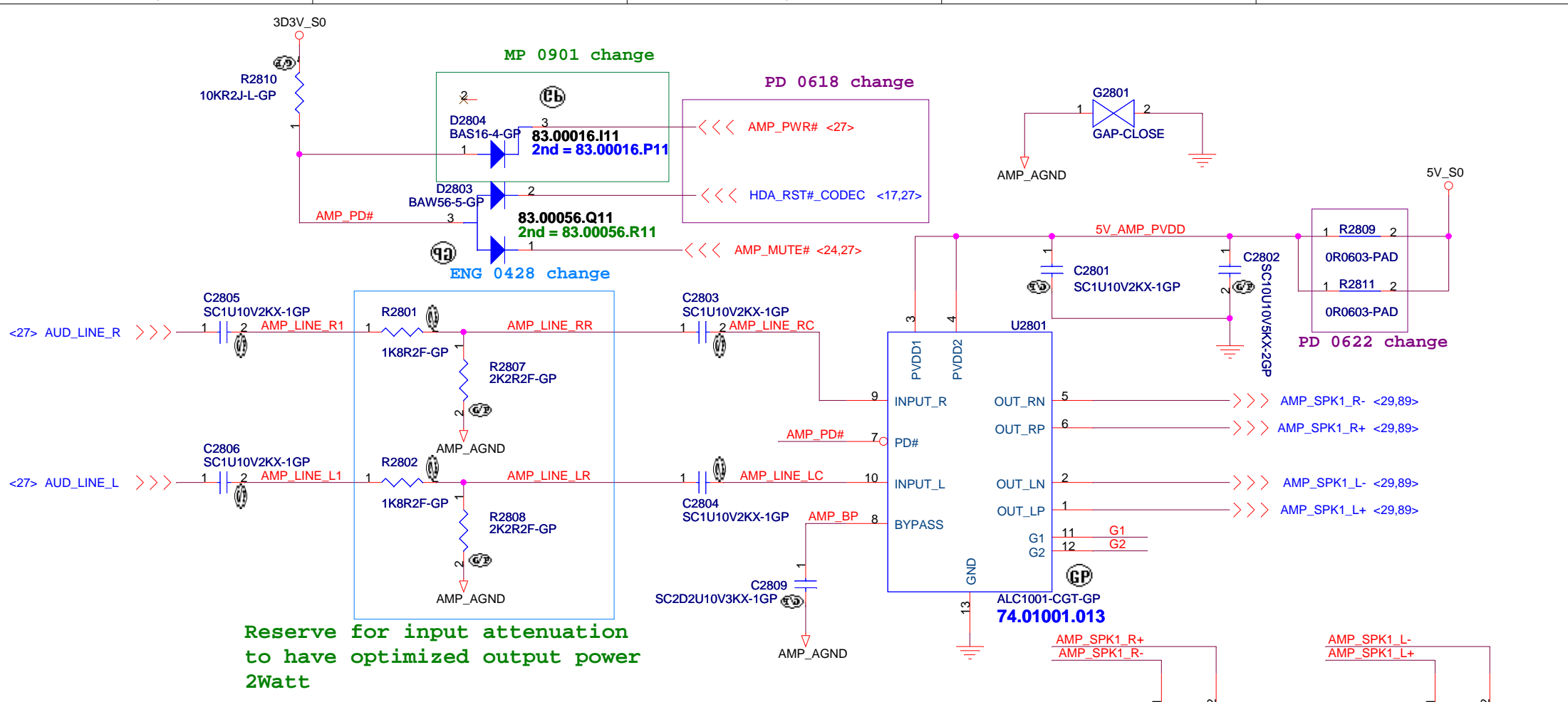
ENG 0428 change



Width=40mil, to improve Headphone Crosstalk noise change it to sharp will be better.
Add 2 vias (>0.5A) when trace layer change.

Layout Note:

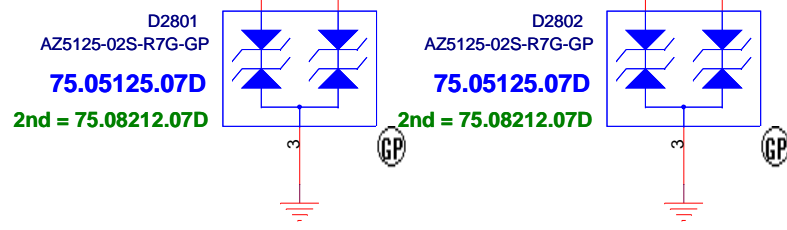
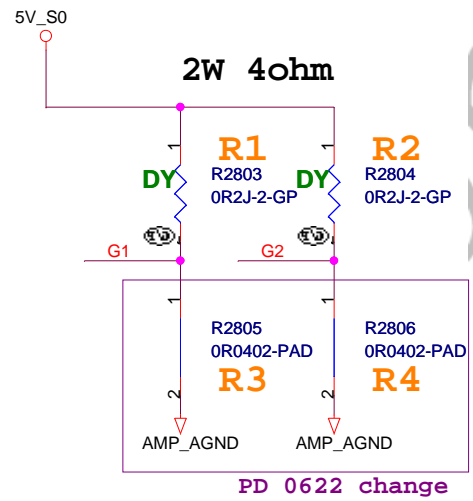




Reserve for input attenuation
to have optimized output power
2Watt

Output Gain Table

R1	R2	R3	R4	Gain (Differential)
NC	NC	0	0	11dB
0	NC	NC	0	14dB
NC	0	0	NC	19dB
0	0	NC	NC	25dB



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Title: **(Reserved)**

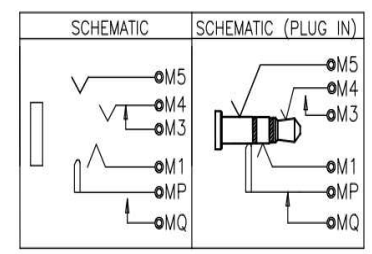
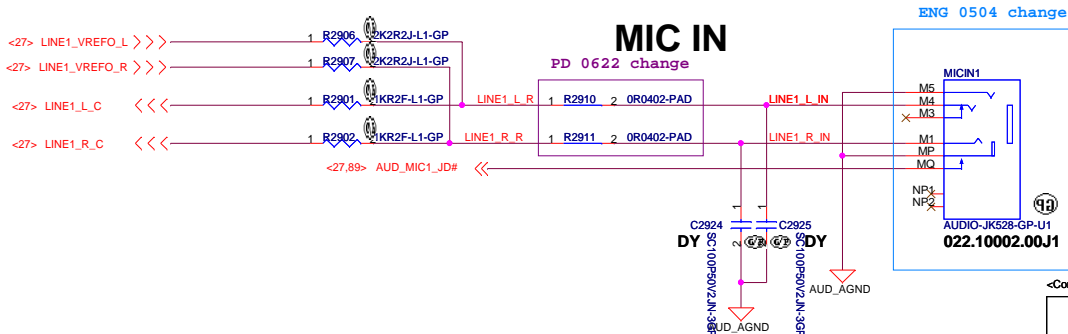
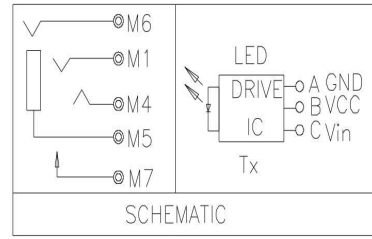
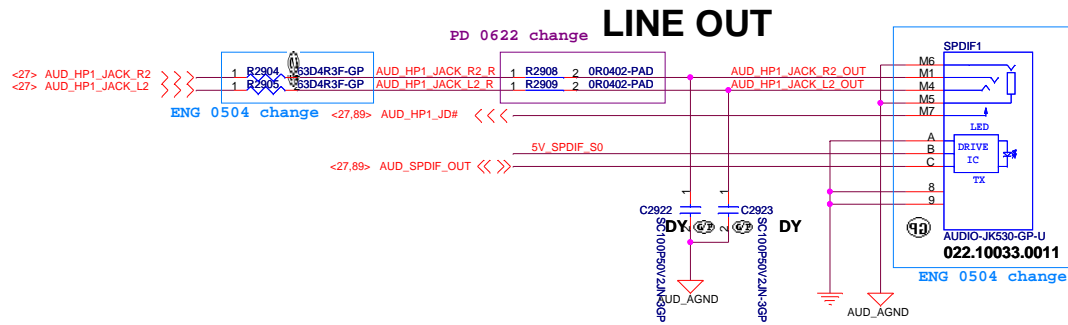
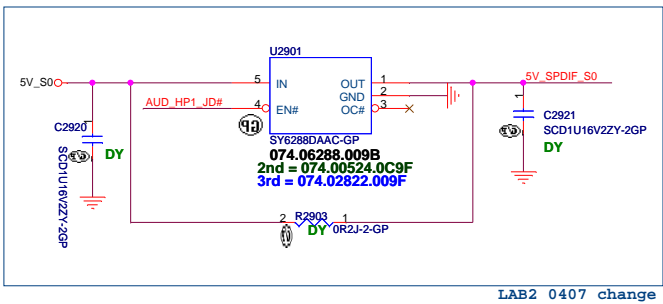
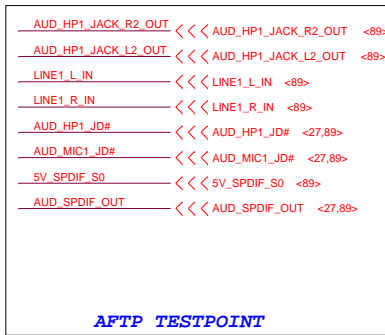
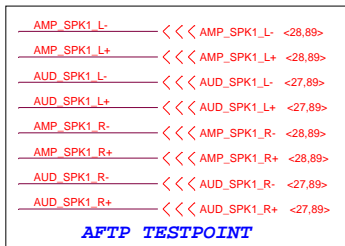
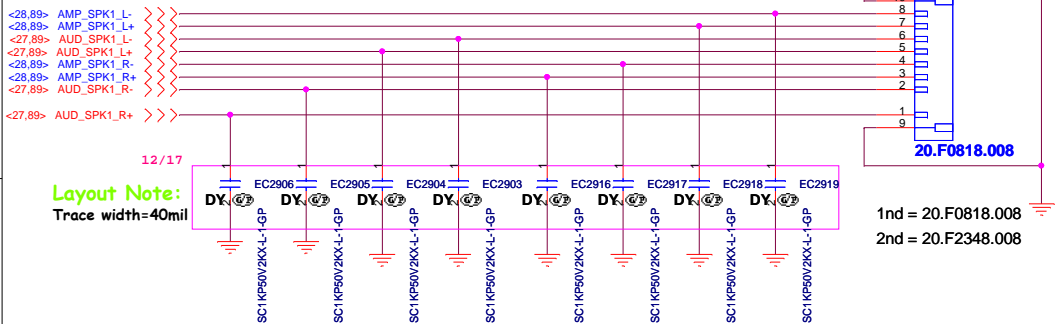
Size: A4 | Document Number: **Newgate** | Rev: **1M**

Date: Tuesday, September 01, 2015 | Sheet 28 of 105

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SSID = AUDIO

Speaker



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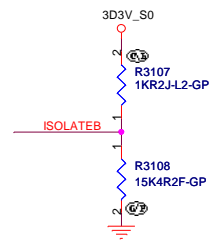
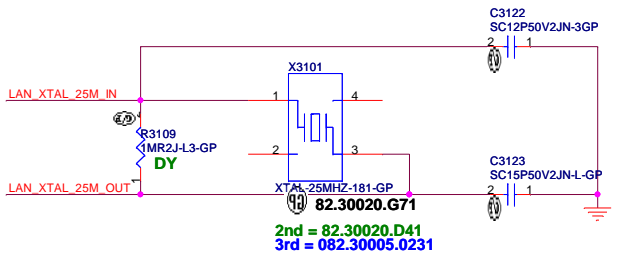
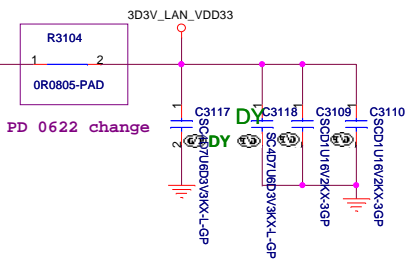
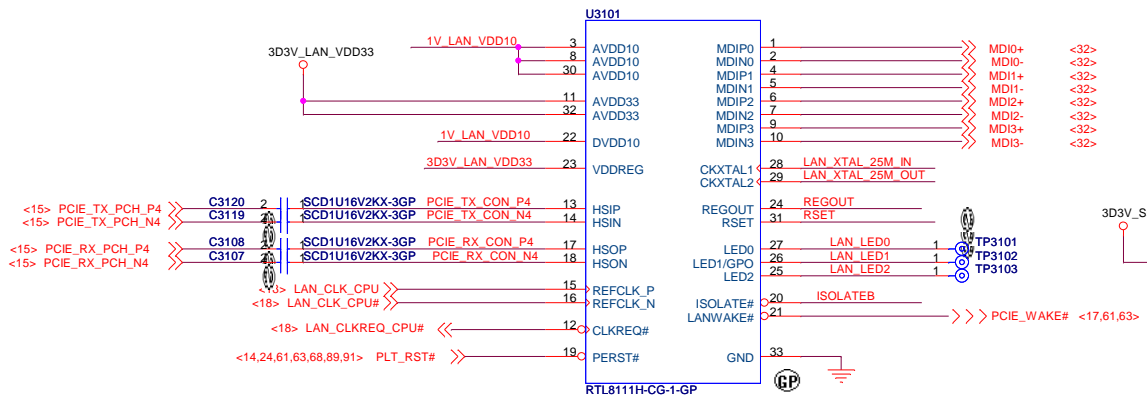
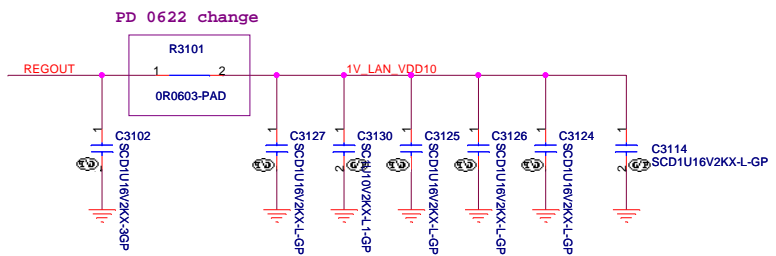
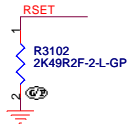
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Title: Speaker/ALC255

Size: Custom Document Number: Newgate Rev: 1M

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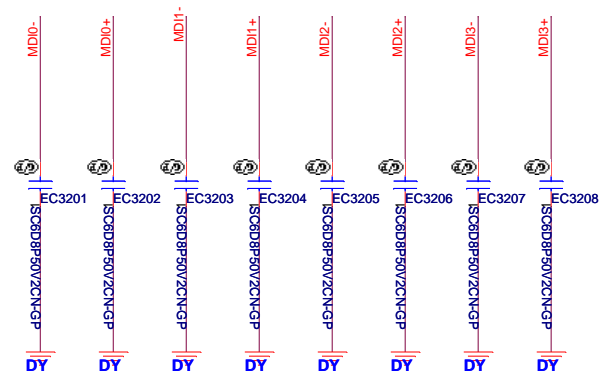
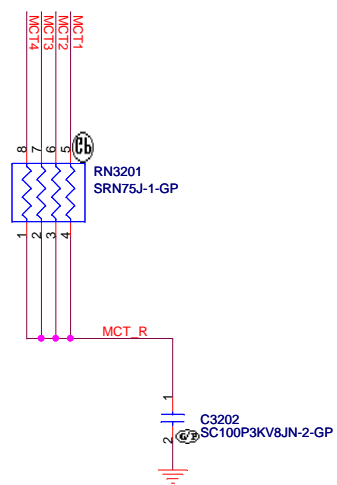
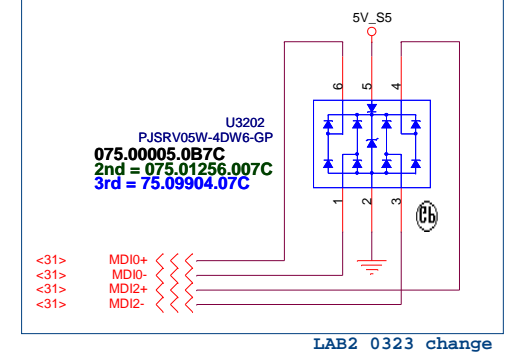
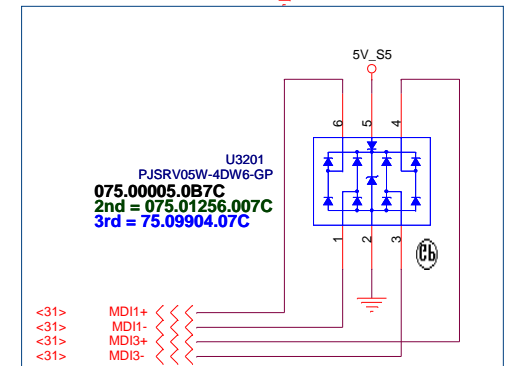
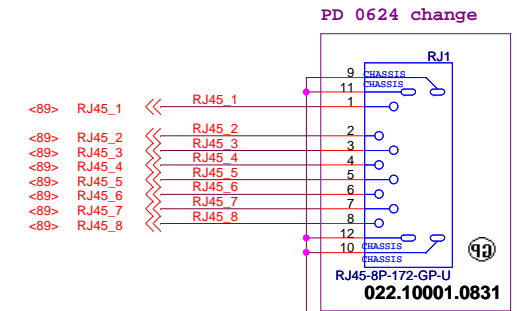
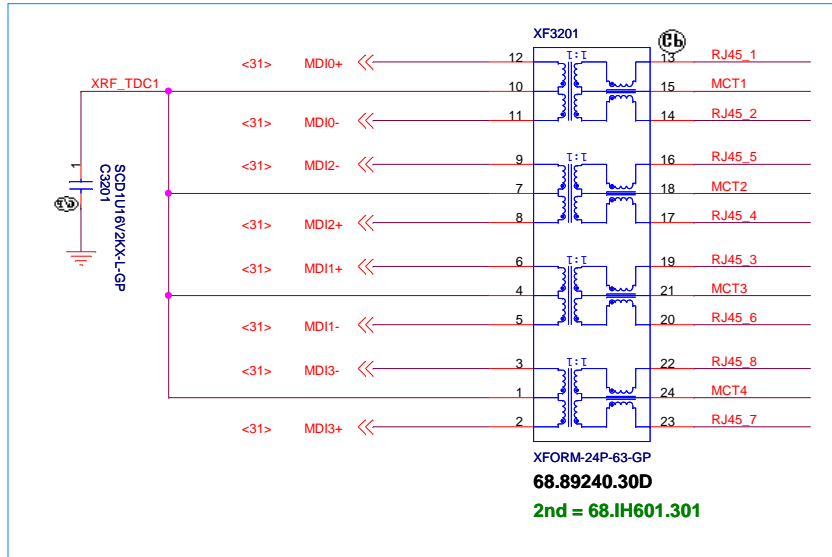


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Size	Document Number
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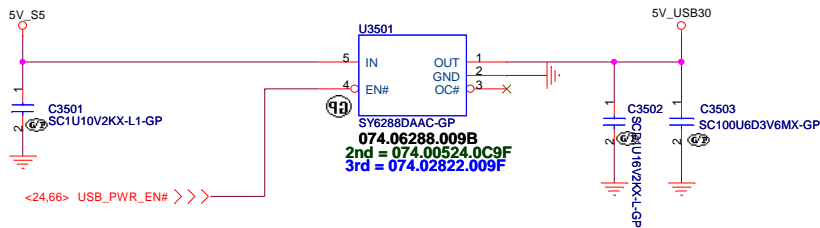
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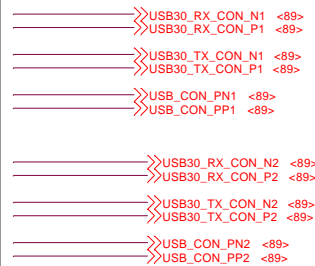
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RJ45+Transformer			
Title	Document Number		Rev
	Newgate		1M
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Low Active 2A



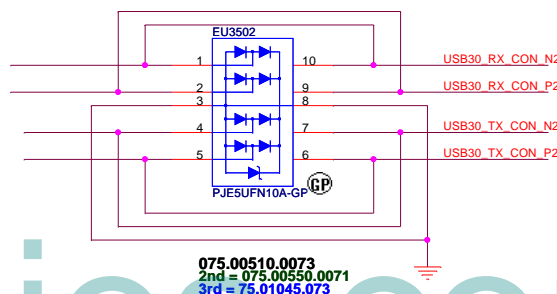
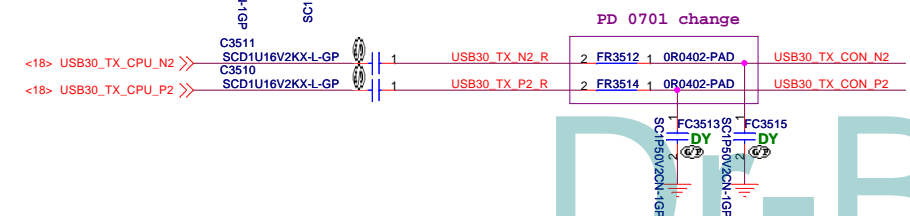
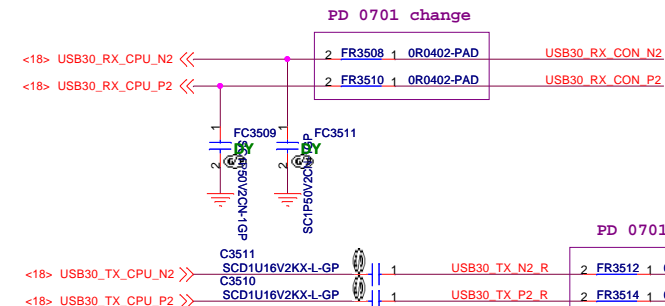
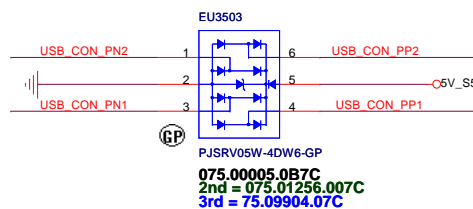
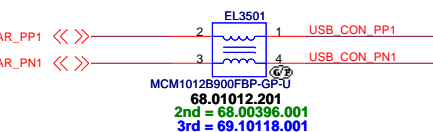
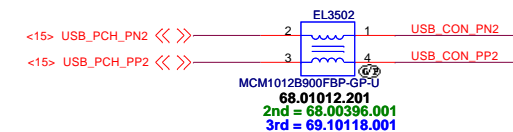
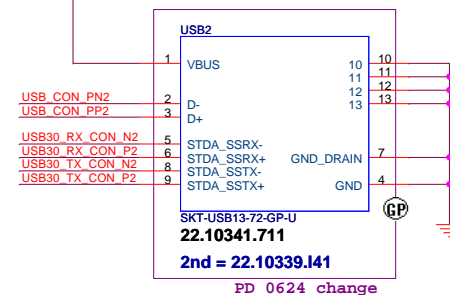
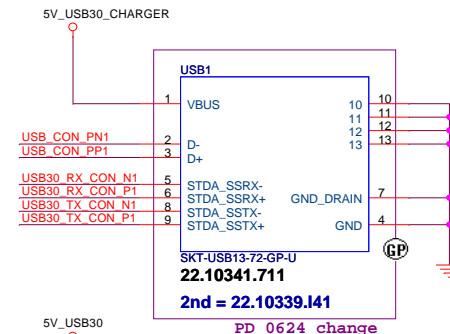
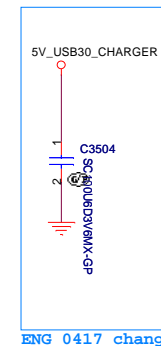
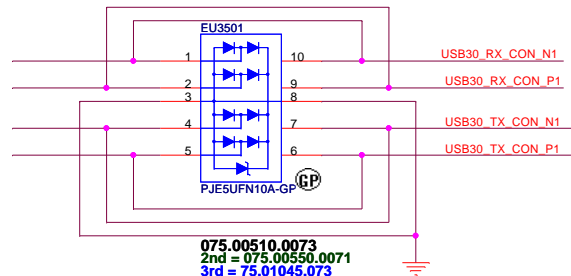
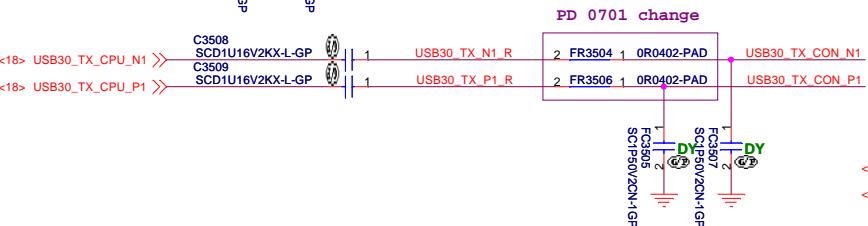
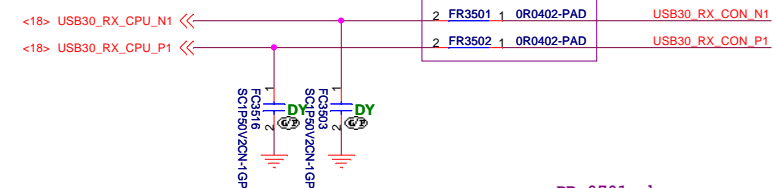
AFTP TESTPOINT



USB 3.0 Connector Pin definition

1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	

PD 0701 change

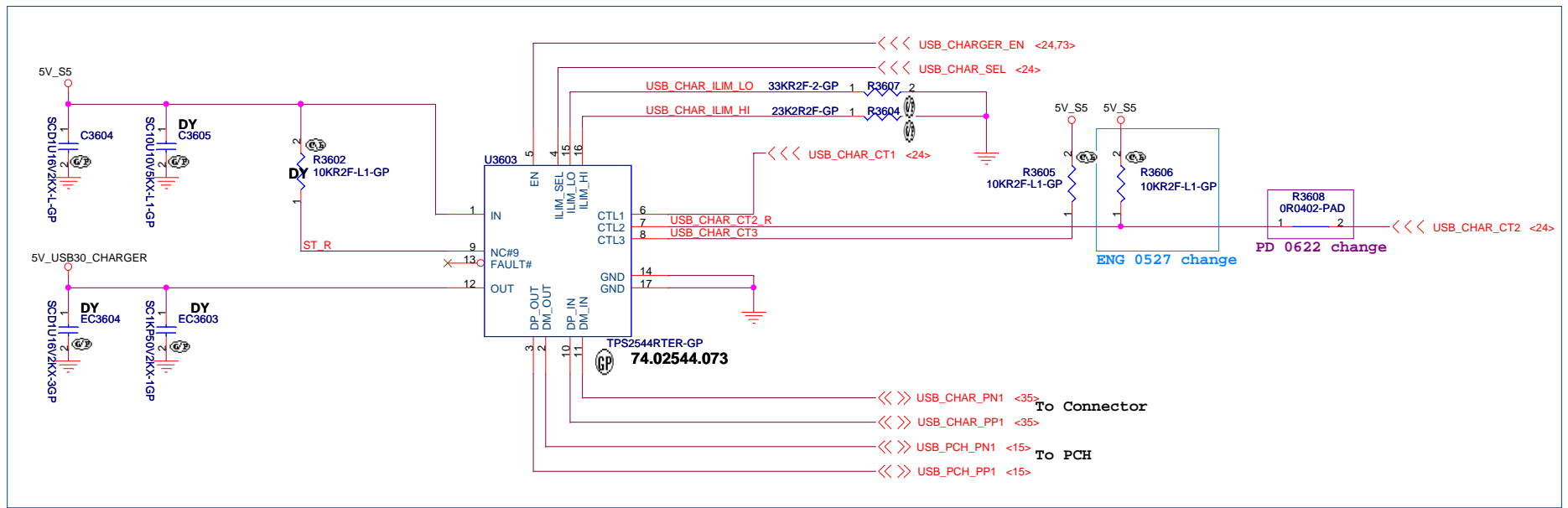


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Title USB3.0 CONN		
Size A3	Document Number Newgate	Rev 1M
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LAB2 0323 change

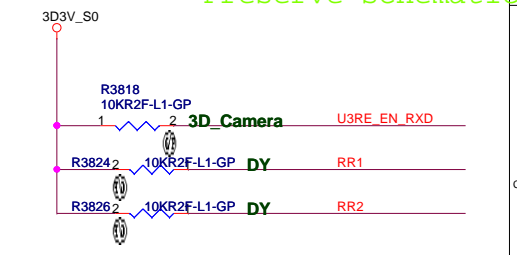
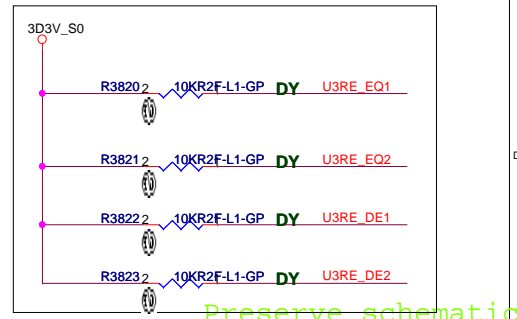
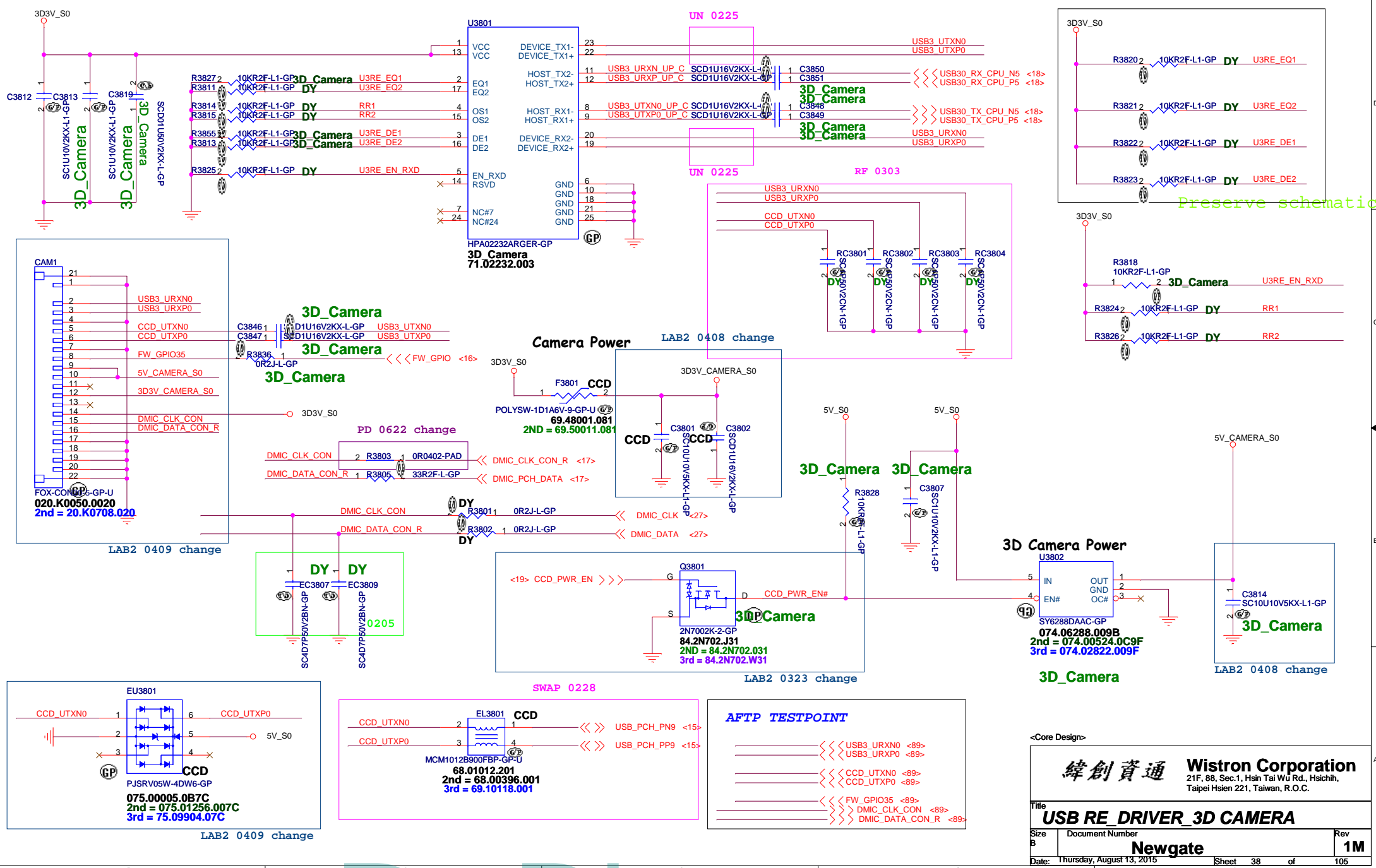
Table 2. Truth Table

CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Limit Setting	Status Output	Notice
0	0	0	0	Discharge	NA	OFF	OUT held low
0	0	0	1	Discharge	NA	OFF	
0	0	1	0	DCP_Auto	ILIM_HI	OFF	Data lines disconnected
0	0	1	1	DCP_Auto	ILIM_HI	DCP	Data lines disconnected Load Detect function active
0	1	0	0	SDP1	ILIM_LO	OFF	Data lines connected
0	1	0	1	SDP1	ILIM_HI	OFF	Data lines disconnected
0	1	1	0	DCP_Auto	ILIM_LO	OFF	Data lines disconnected
0	1	1	1	DCP_Auto	ILIM_HI	DCP	Data lines disconnected Load Detect function active
1	0	0	0	DCP_Shorted	ILIM_LO	OFF	Device forced to stay in DCP BC1.2
1	0	0	1	DCP_Shorted	ILIM_HI	OFF	Charging mode
1	0	1	0	DCP/Divider1	ILIM_LO	OFF	Device forced to stay in DCP divider1
1	0	1	1	DCP/Divider1	ILIM_HI	OFF	Charging mode
1	1	0	0	SDP1	ILIM_LO	OFF	Data lines connected
1	1	0	1	SDP1	ILIM_HI	OFF	
1	1	1	0	SDP2	ILIM_LO	OFF	Data lines disconnected
1	1	1	1	CDP	ILIM_HI	CDP	Data lines disconnected Load Detect function active

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title **USB CHARGER**
Size B Document Number **Newgate** Rev **1M**
Date: Thursday, August 13, 2015 Sheet 36 of 105



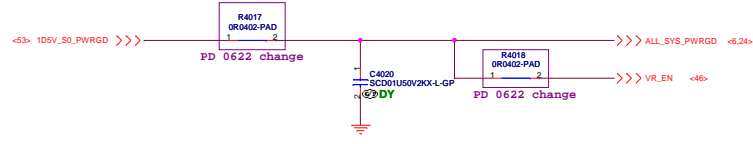
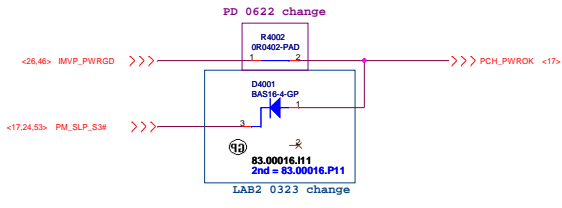
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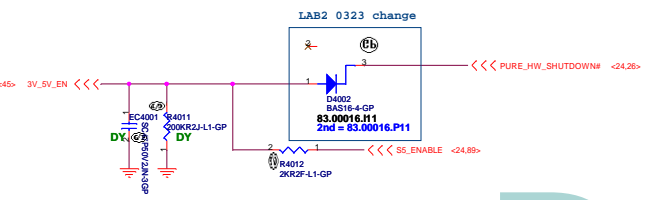
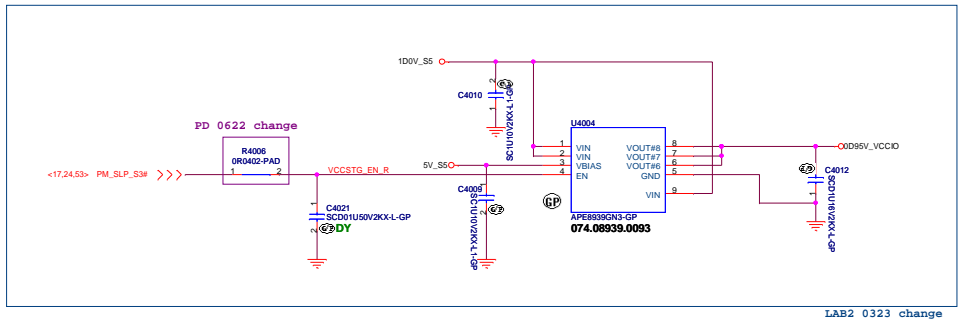
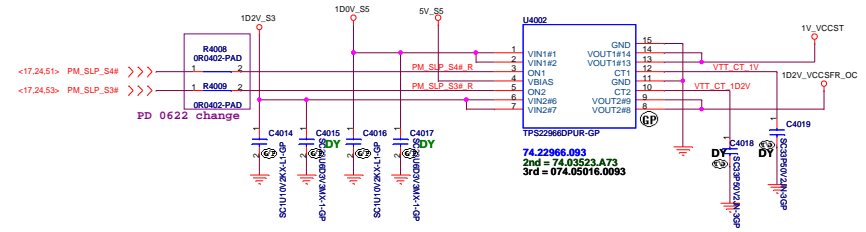
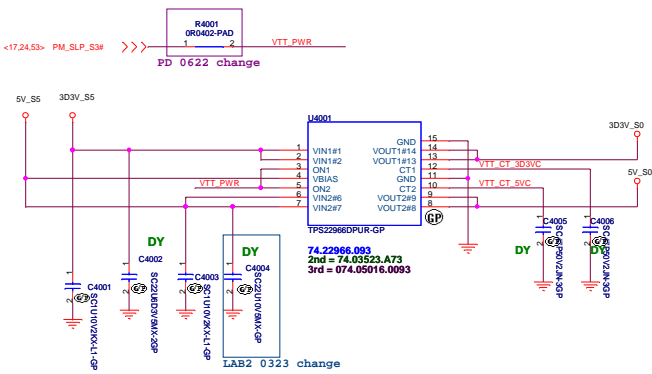
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Size P	Document Number	Rev
	Newgate	1M
Date: Thursday, August 13, 2015	Sheet 38 of	105

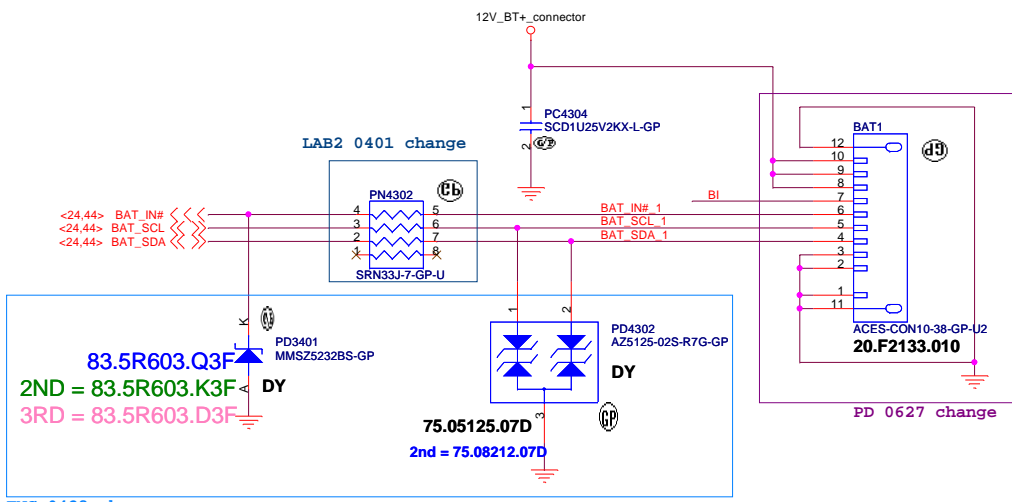
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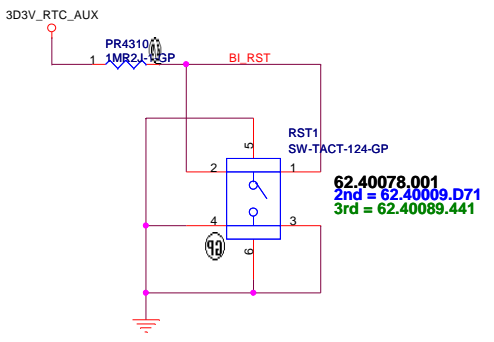
ANNIE Run Power



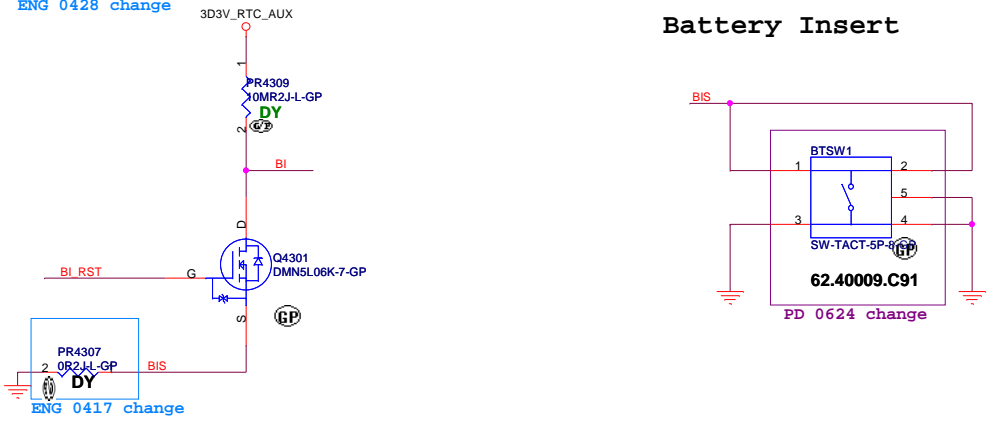
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Battery Reset



Battery Insert

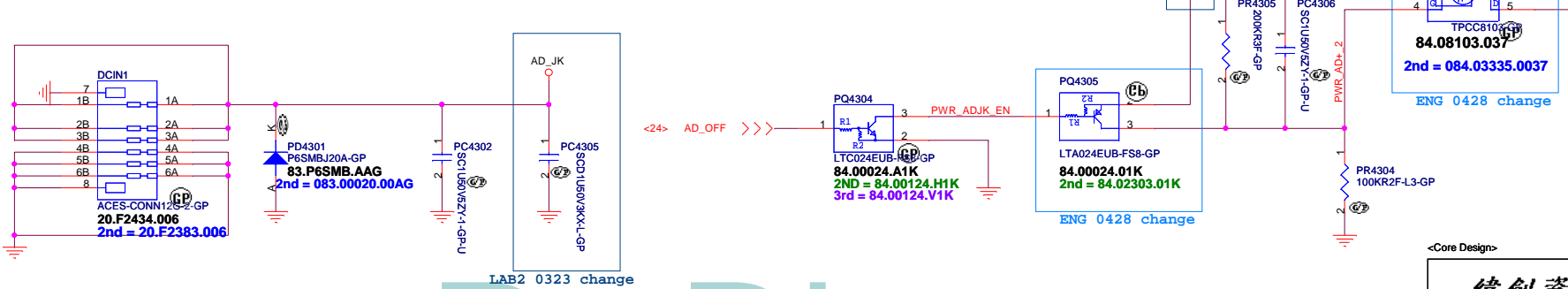


AFTP TESTPOINT

<89> BI	BI
<89> BAT_IN#_1	BAT_IN#_1
<89> BAT_SCL_1	BAT_SCL_1
<89> BAT_SDA_1	BAT_SDA_1

ANNIE solution

Adaptor in to generate DCBATOUT



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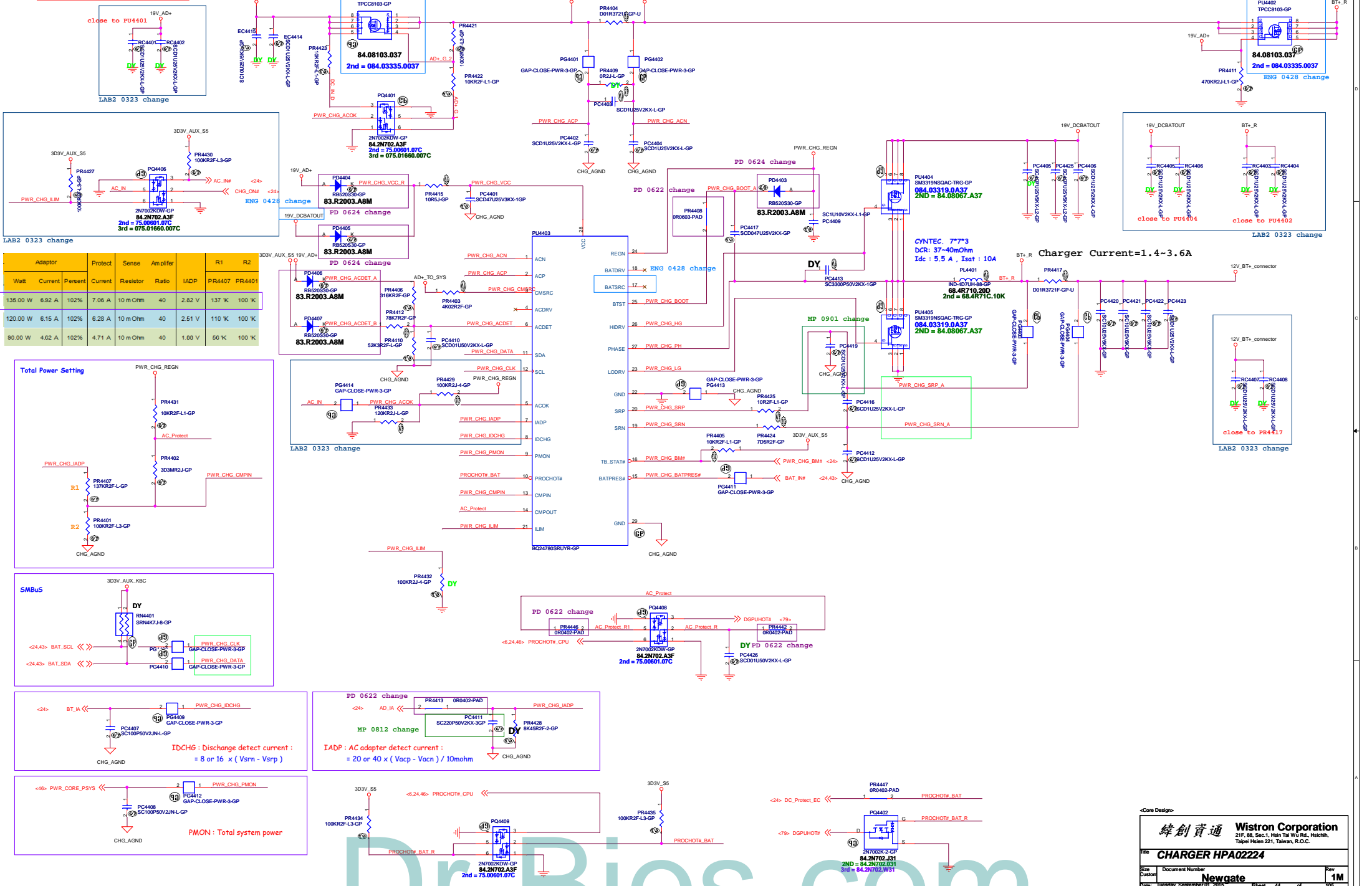
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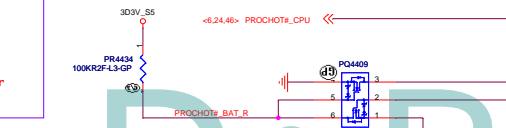
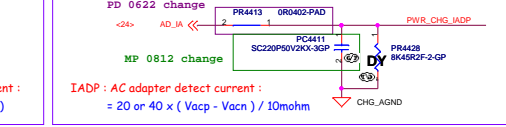
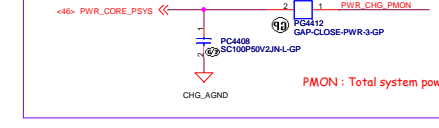
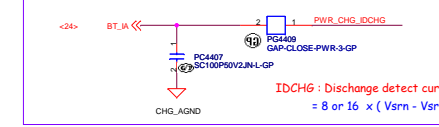
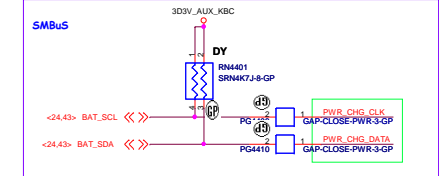
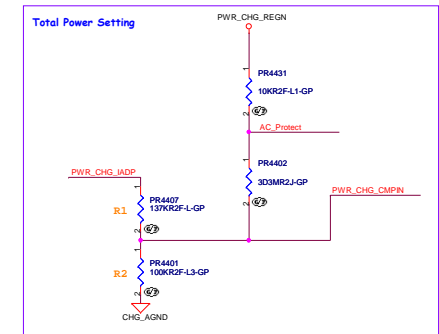
Title DC IN / BATT Conn		
Size A3	Document Number Newgate	Rev 1M
Date: Thursday, August 13, 2015	Sheet 43 of	105

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SSID = Charger



Adaptor	Protect	Sense	Amplifier	R1	R2
Watt	Current	Percent	Current	Resistor	Ratio
135.00 W	6.92 A	102%	7.06 A	10 m Ohm	40
120.00 W	6.15 A	102%	6.28 A	10 m Ohm	40
90.00 W	4.02 A	102%	4.71 A	10 m Ohm	40



Charger Current=1.4~3.6A

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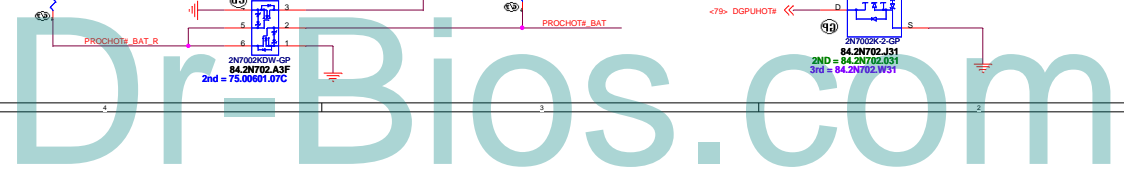
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Rev: **4**

Customer: **Newgate**

Date: Tuesday, September 01, 2015

Sheet: 44 of 105



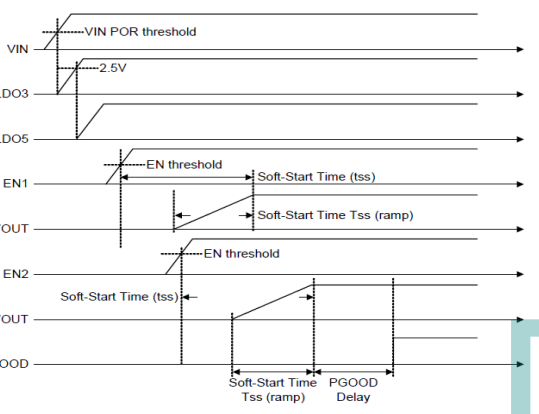
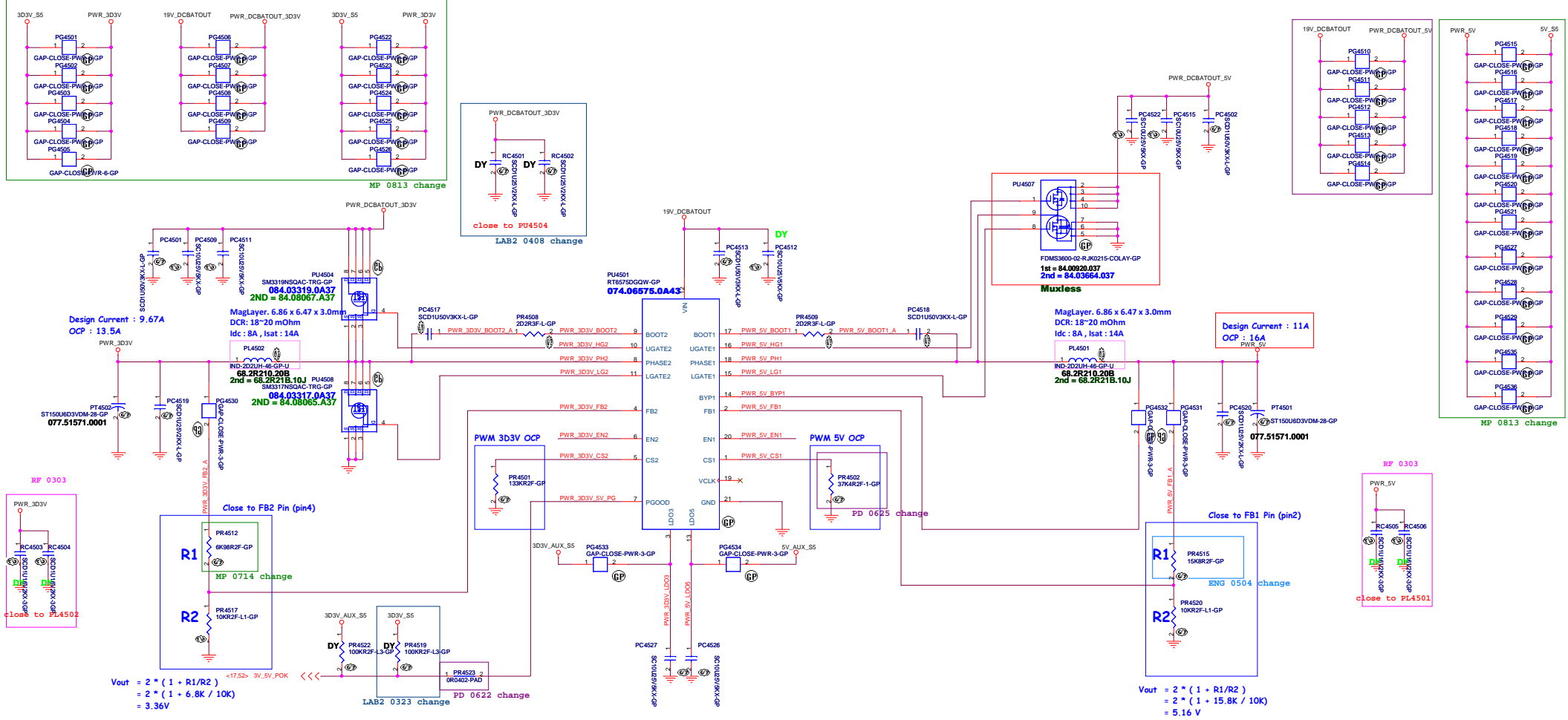
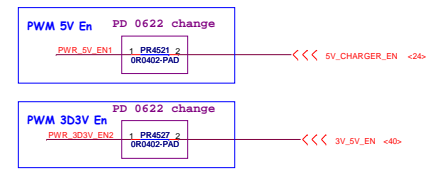
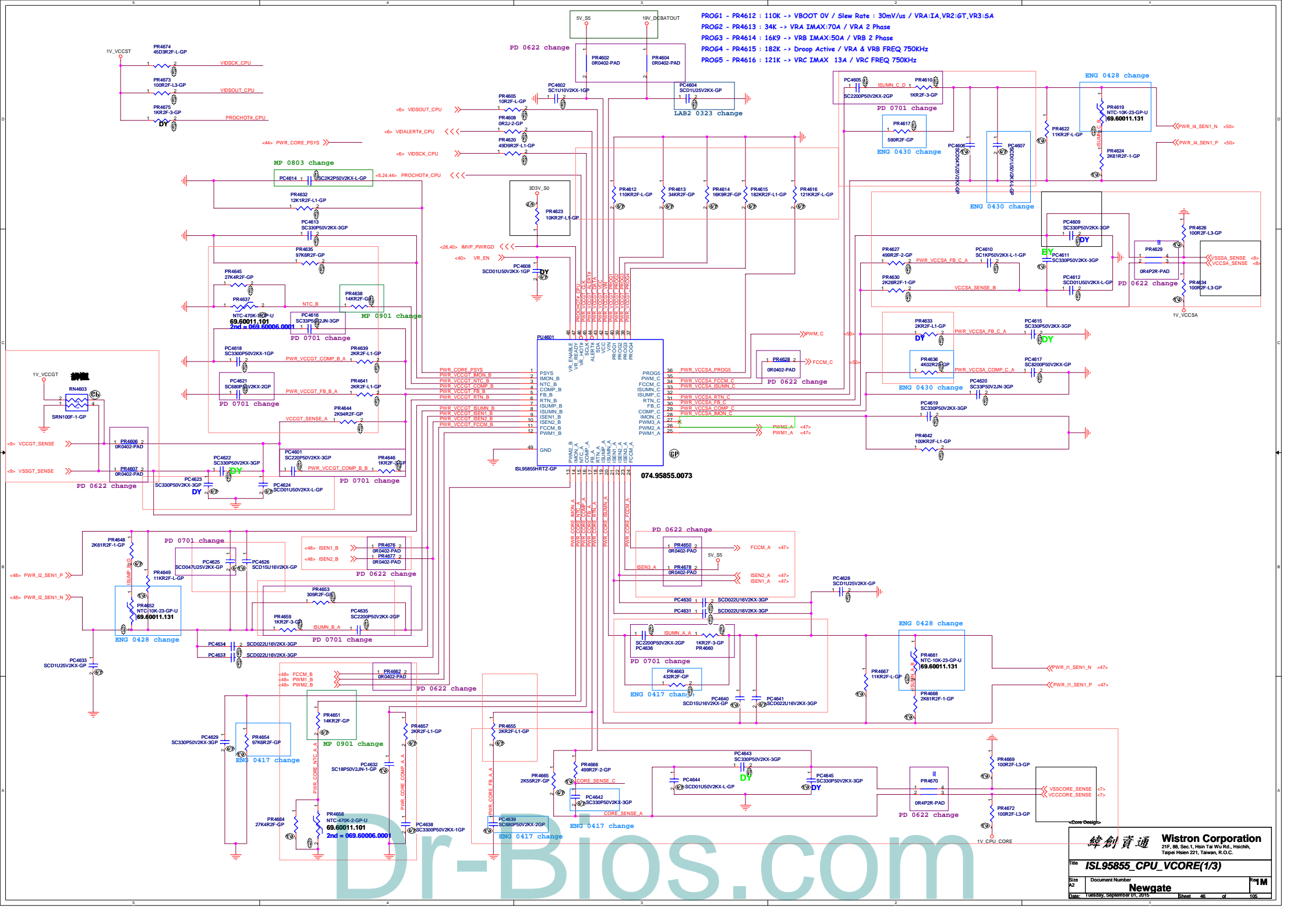


Figure 6. RT6575B Timing



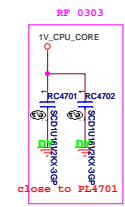
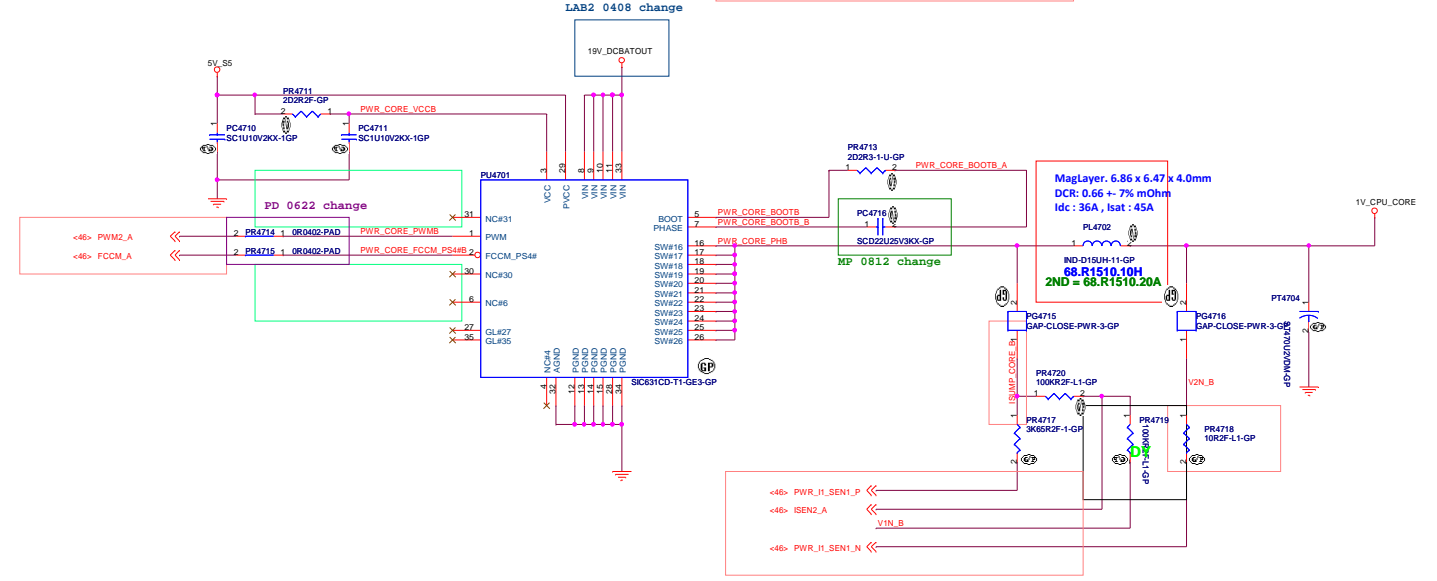
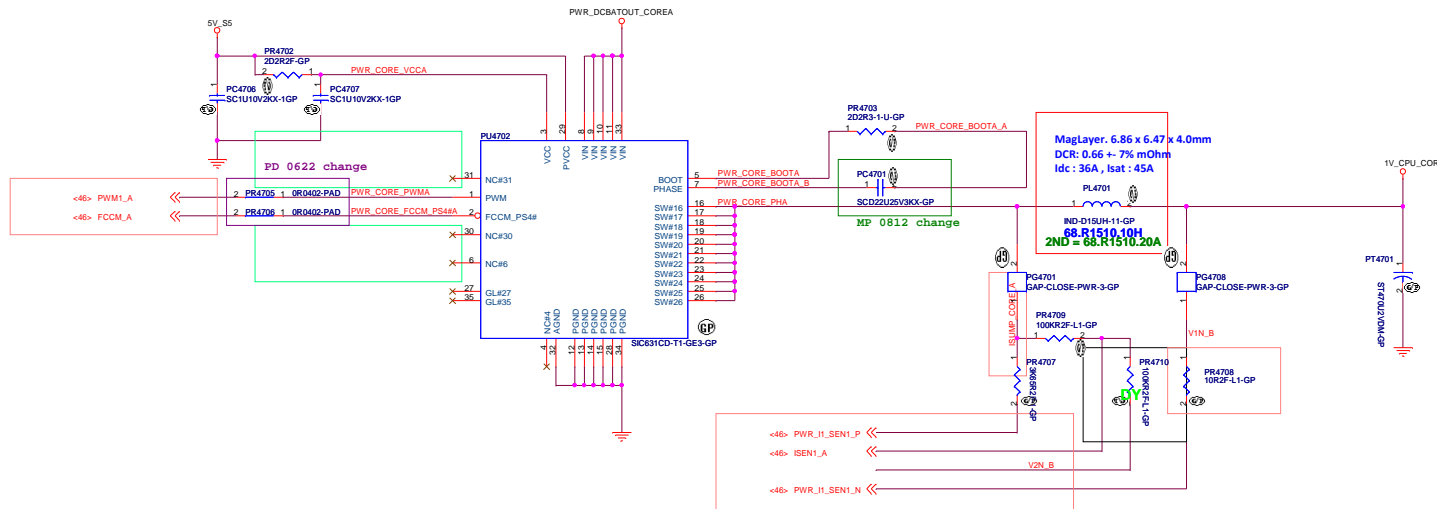
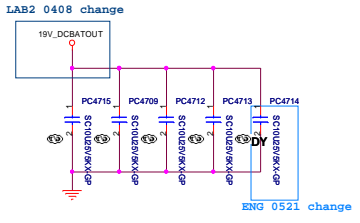
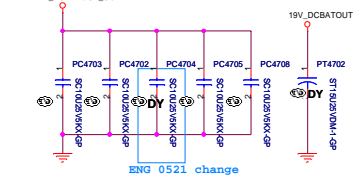
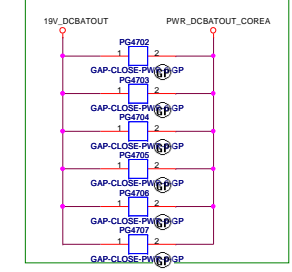
Vin POR threshold , Rising :4.6 V ; Failing : 3.7 V
 EN threshold Logic-High : 1.6 V
 EN threshold Logic-Low : 0.4 V

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PROG1 - PR4612 : 110K -> VBOOT OV / Slow Rate : 30mV/us / VRA:IA,VR2:GT,VR3:SA
PROG2 - PR4613 : 34K -> VRA IMAX:70A / VRA 2 Phase
PROG3 - PR4614 : 16K9 -> VRB IMAX:50A / VRB 2 Phase
PROG4 - PR4615 : 182K -> Droop Active / VRA & VRB FREQ 750KHz
PROG5 - PR4616 : 121K -> VRC IMAX 13A / VRC FREQ 750KHz

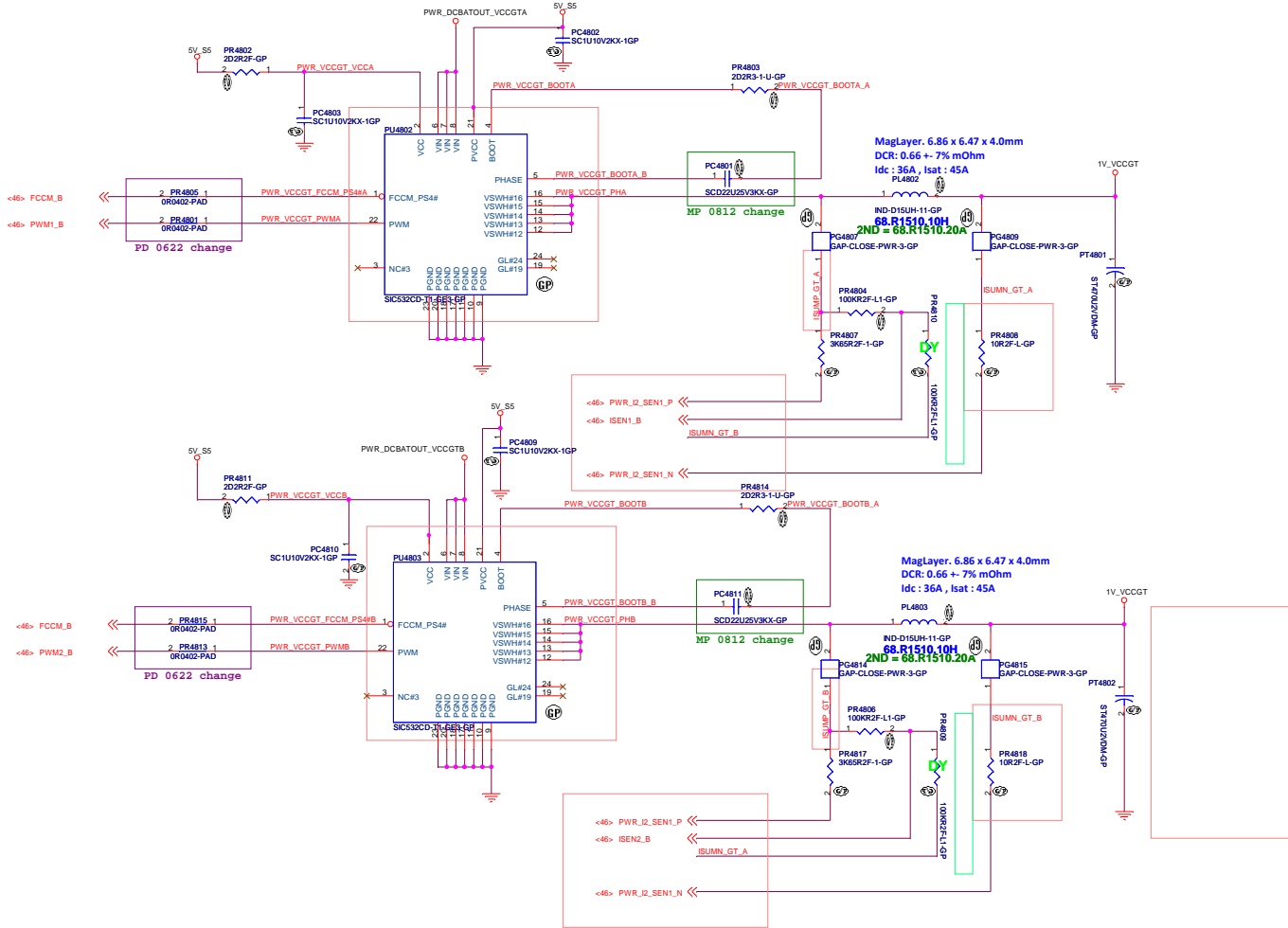
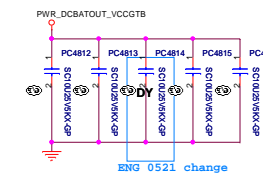
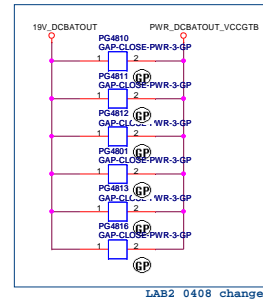
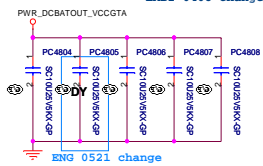
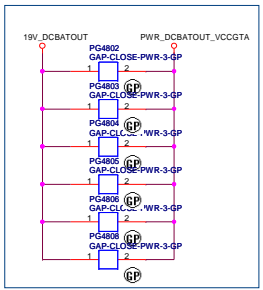
MP 0813 change



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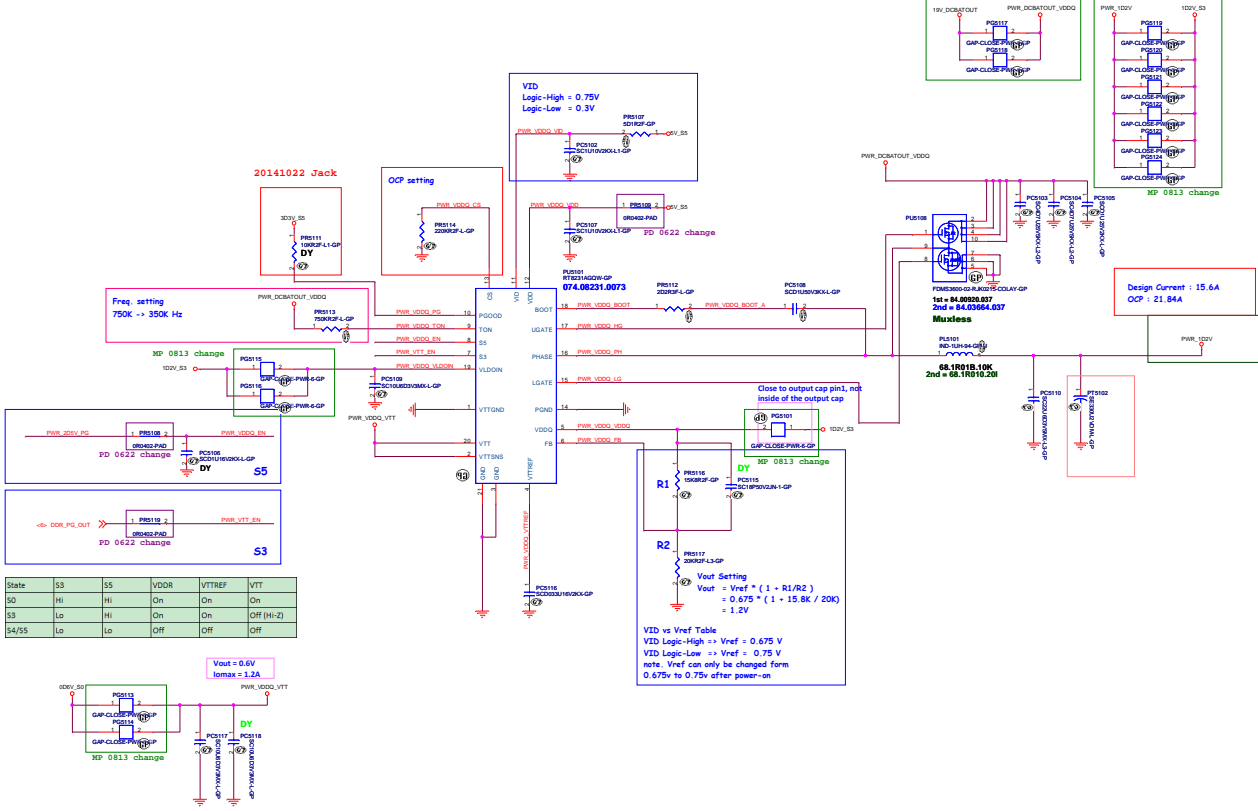
緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.	
Title	SIC631CD_CPU_VCORE(2/3)
Size	Document Number
Date	108209, August 13, 2015
Rev	1M
Sheet	47 of 100



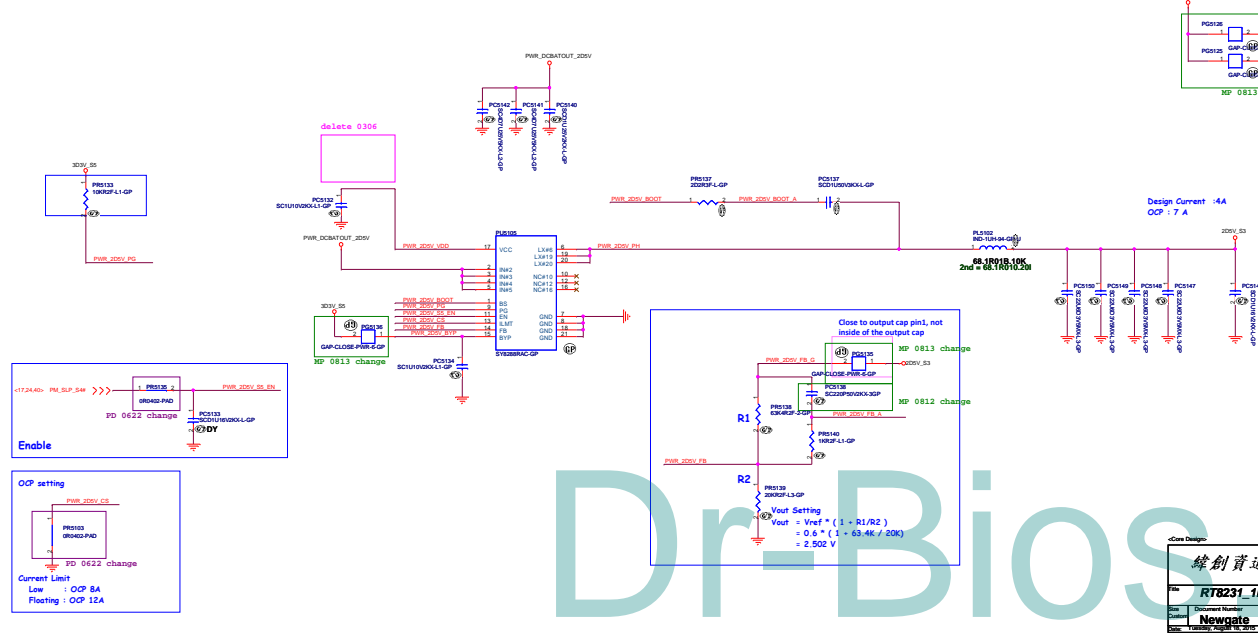
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<Core Design>

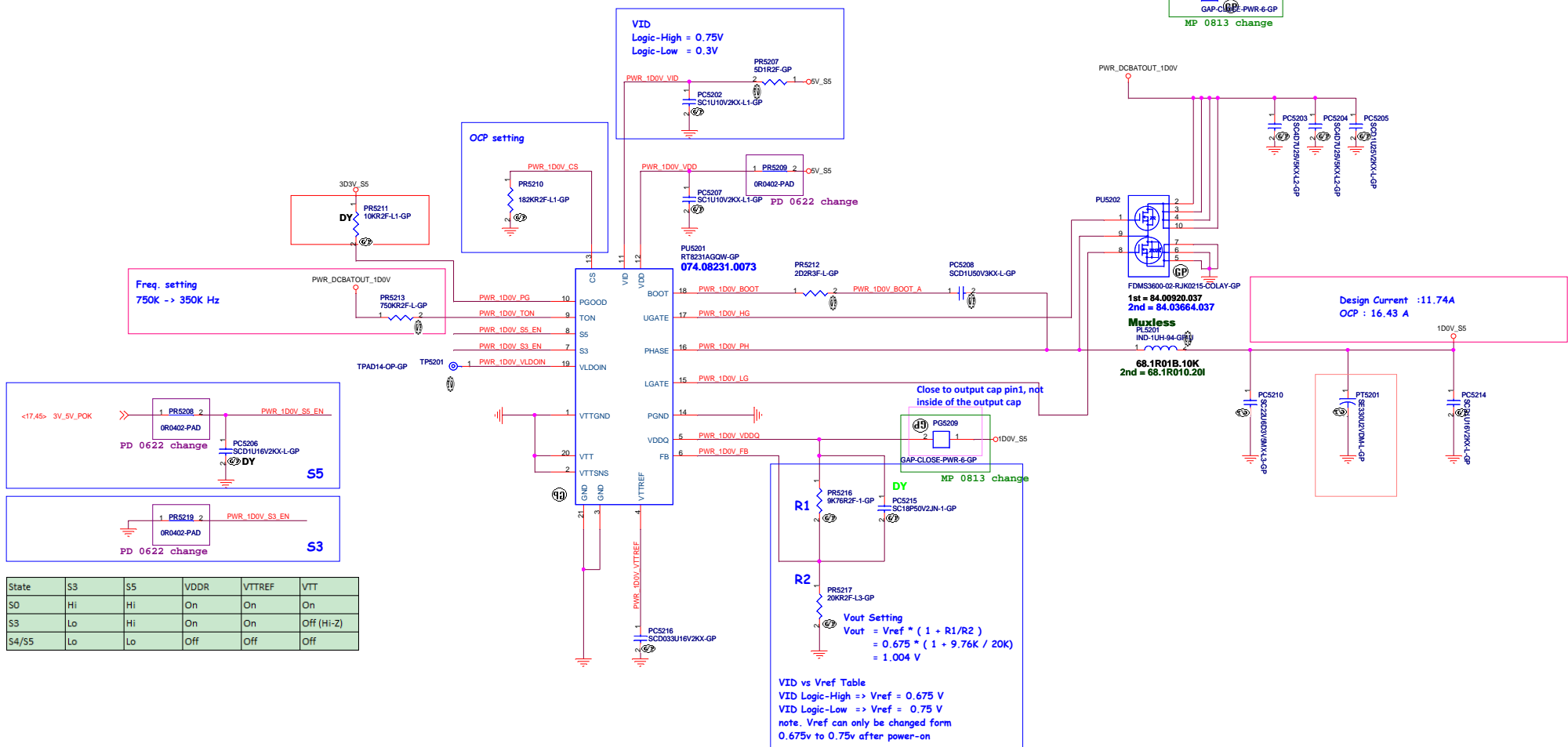
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21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsein 221, Taiwan, R.O.C.	
File	SIC631CD CPU VCORE(2/3)
Size	Document Number
PC	Newgate
Date	1/25/2015, August 18, 2015
Sheet	68 of 138
Rev	1M



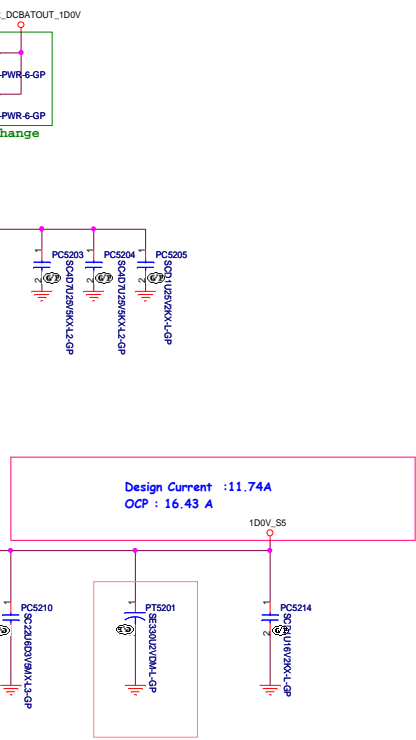
SY8288 For DDR4
Vout = 2.5V



Wistron Corporation
RT8231_1D2V
Newgate
1M

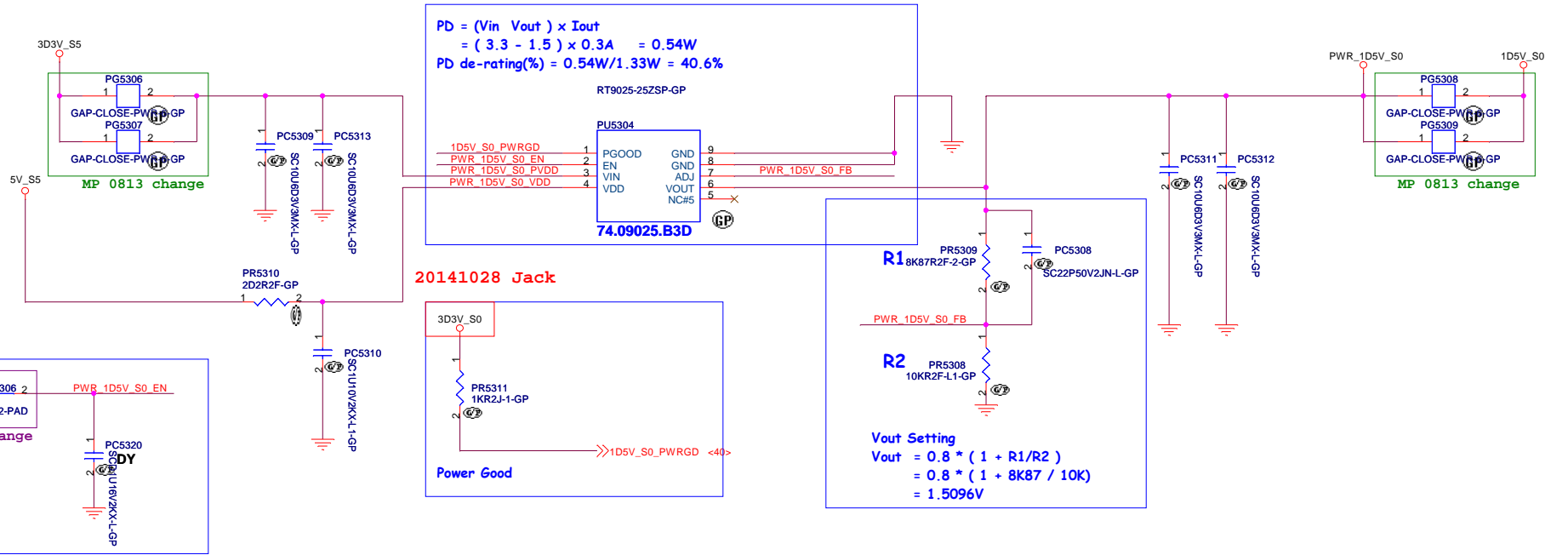


State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off



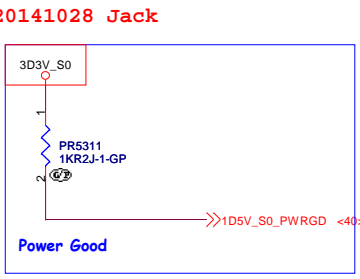
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1D5V_S0



$PD = (V_{in} - V_{out}) \times I_{out}$
 $= (3.3 - 1.5) \times 0.3A = 0.54W$
 $PD \text{ de-rating}(\%) = 0.54W / 1.33W = 40.6\%$

RT9025-25ZSP-GP

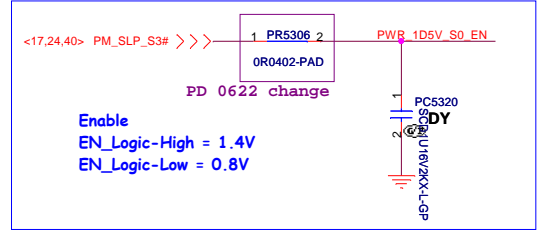


Vout Setting

$$V_{out} = 0.8 * (1 + R1/R2)$$

$$= 0.8 * (1 + 8K87 / 10K)$$

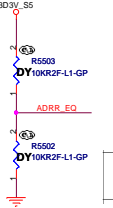
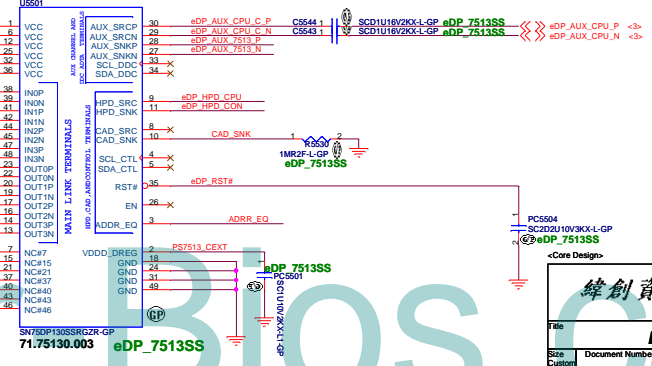
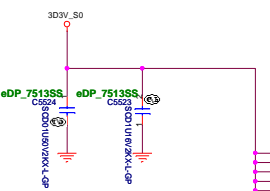
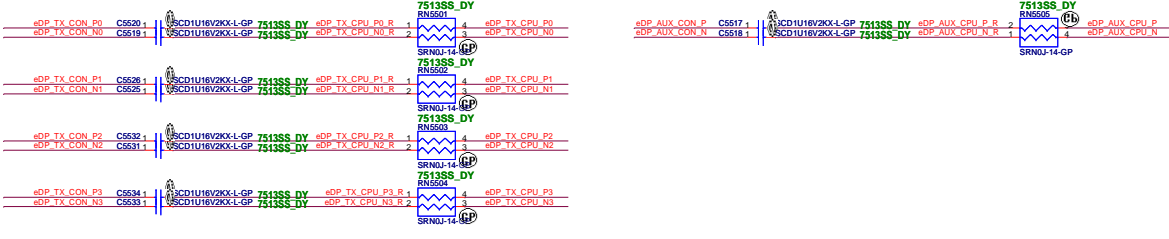
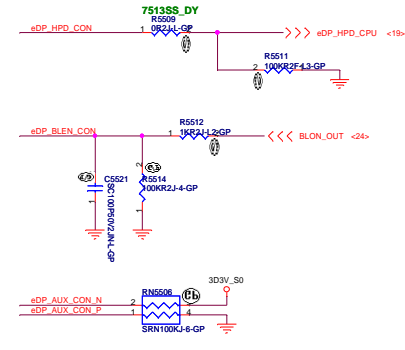
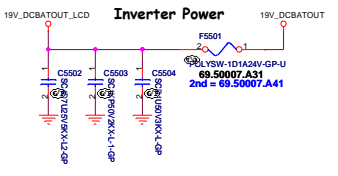
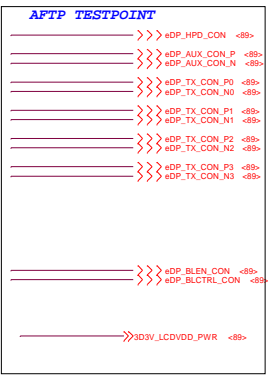
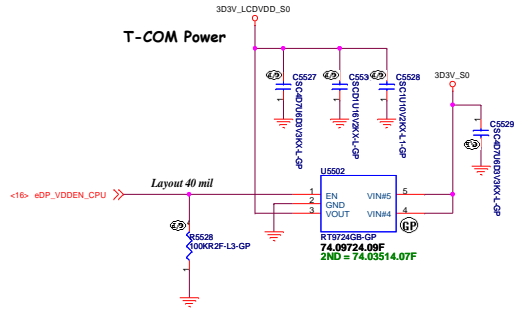
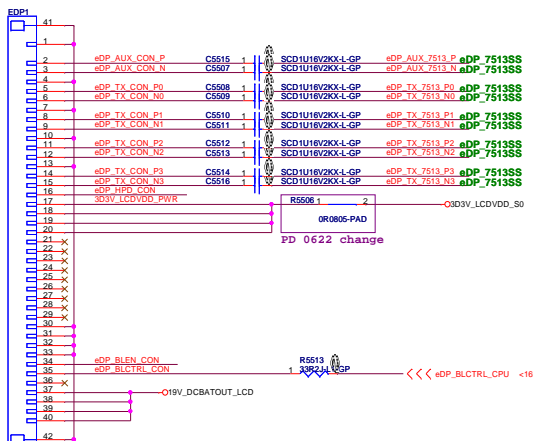
$$= 1.5096V$$



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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title RT9025_1D5V		
Size A3	Document Number Newgate	Rev 1M
Date: Tuesday, August 18, 2015	Sheet 53 of 105	



ADDR_EQ	3	3-level Input	I ² C Target Address Selected and EQ Configuration Input. If the I ² C bus is used, this input setting selects the I ² C target address, as described in Table 7. This input also configures the input EQ to the device, as described in Table 5.
---------	---	---------------	--

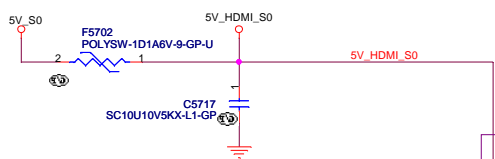
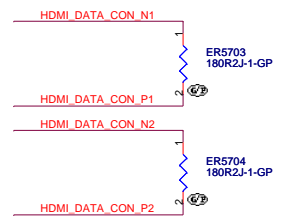
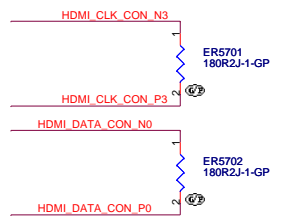
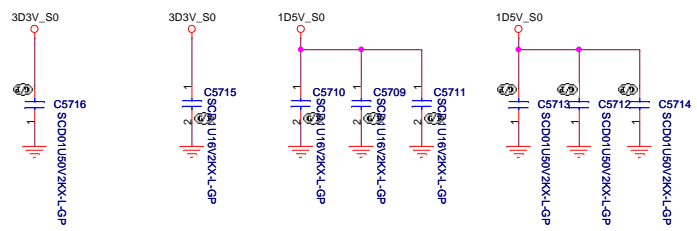
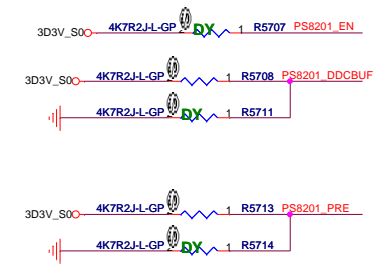
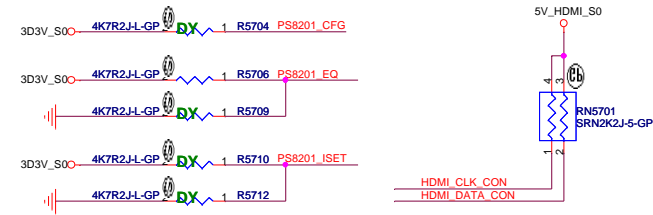
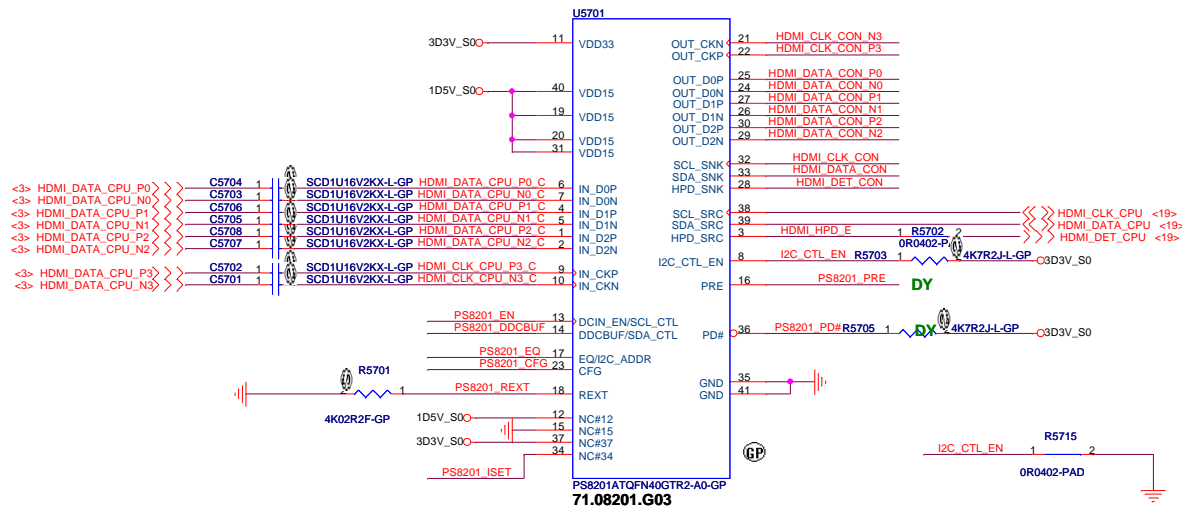
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File		EPOPIO/EDRAM Power	
Size	Document Number	Rev	
Custom	Newgate	1M	
Date:	Thursday, August 13, 2016	Sheet	55 of 105

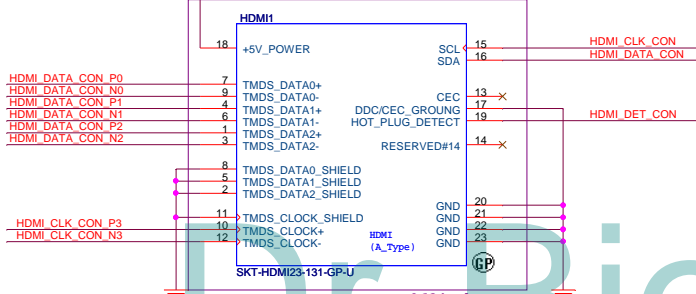


SSID = VIDEO

HDMI Level Shifter & CONNECTOR



HDMI CONN



022.10025.0091 PD 0624 change
2nd = 022.10025.0061

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Title: **HDMI Level Shifter/Conn**

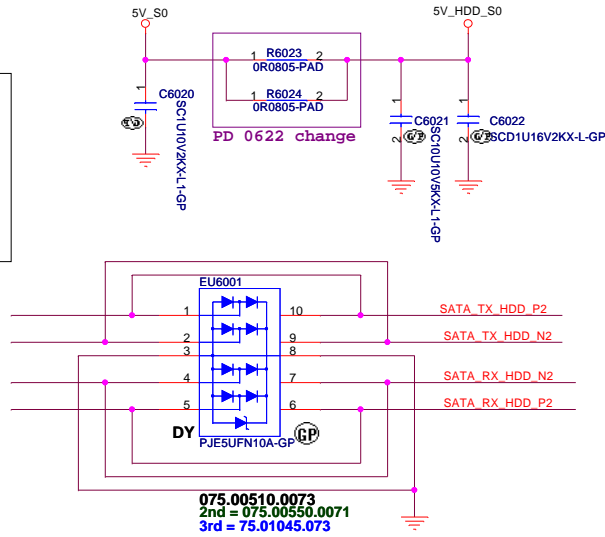
Size: Document Number
Customer: **Newgate** Rev: **1M**

Date: Thursday, August 13, 2015 Sheet 57 of 105

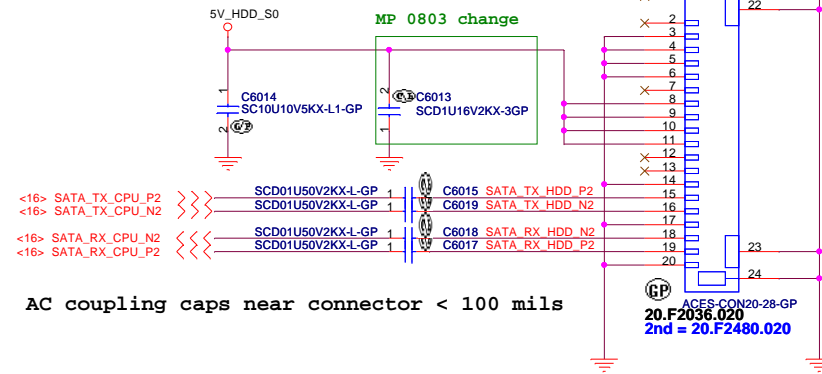
SSID = SATA

AFTP TESTPOINT

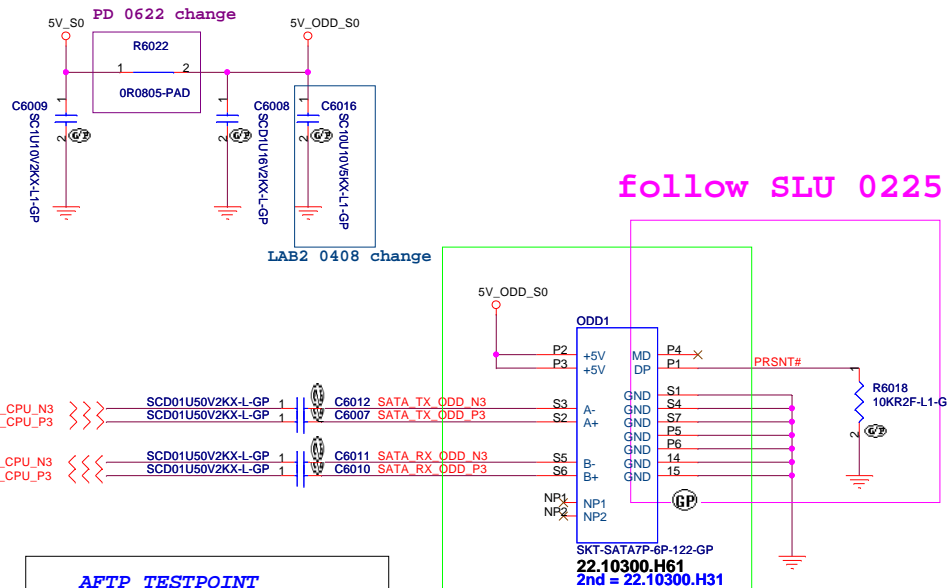
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 <89> SATA_TX_HDD_N2 >>>
 <89> SATA_RX_HDD_N2 <<<
 <89> SATA_RX_HDD_P2 <<<



SATA HDD Connector



AC coupling caps near connector < 100 mils



AFTP TESTPOINT

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 <89> SATA_TX_ODD_P3 >>>
 <89> SATA_RX_ODD_N3 <<<
 <89> SATA_RX_ODD_P3 <<<

PIN DEFINE	CONN	FFC
GND		20
GND	P5/P6	19
GND		18
ODD_DA	P4	17
NC		16
5V		15
5V		14
5V		13
5V	P2/P3	12
5V		11
5V		10
NC		9
PRSN#	P1	8
GND	S7	7
RXP	S6	6
RXN	S5	5
GND	S4	4
TXN	S3	3
TXP	S2	2
GND	S1	1

ODD1 conn change by Royee 20150202

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Title: **HDD/ODD**

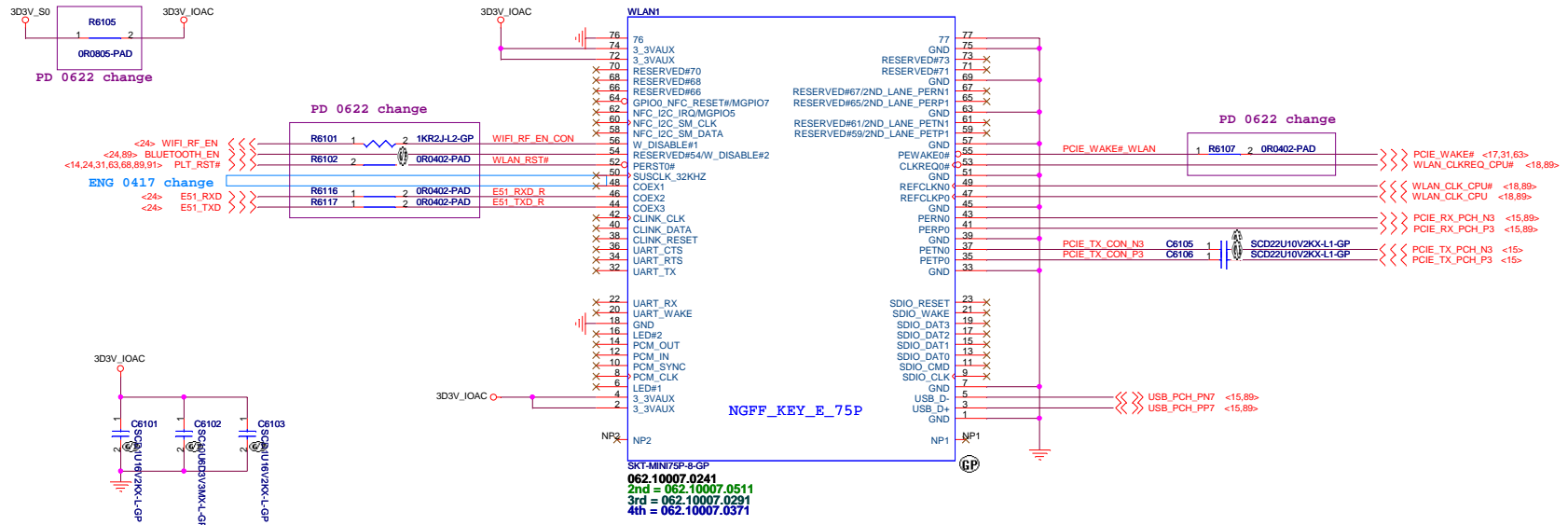
Size A3 Document Number: **Newgate** Rev **1M**

Date: Tuesday, August 18, 2015 Sheet 60 of 105

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SSID = Wireless/ Wigig

NGFF Connector (802.11a/b/g/n)



AFTP TESTPOINT

- >>> PCIE_WAKE#_WLAN <89>
- >>> WLAN_CLKREQ_CPU# <18,89>
- <<< WLAN_CLK_CPU# <18,89>
- <<< WLAN_CLK_CPU <18,89>
- >>> PCIE_RX_PCH_N3 <15,89>
- >>> PCIE_RX_PCH_P3 <15,89>
- <<< PCIE_TX_CON_N3 <89>
- <<< PCIE_TX_CON_P3 <89>
- >>> USB_PCH_PN7 <15,89>
- >>> USB_PCH_PP7 <15,89>
- >>> WIFI_RF_EN_CON <89>
- >>> BLUETOOTH_EN <24,89>
- >>> WLAN_RST# <89>
- >>> E51_RXD_R <89> **ENG 0417 change**
- >>> E51_TXD_R <89>

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Title		
Mini card-WLAN		
Size	Document Number	Rev
Custom	Newgate	1M
Date: Thursday, August 13, 2015	Sheet 61	of 105

SSID = m-SATA

Mini Card Connector (NGFF m-SATA)

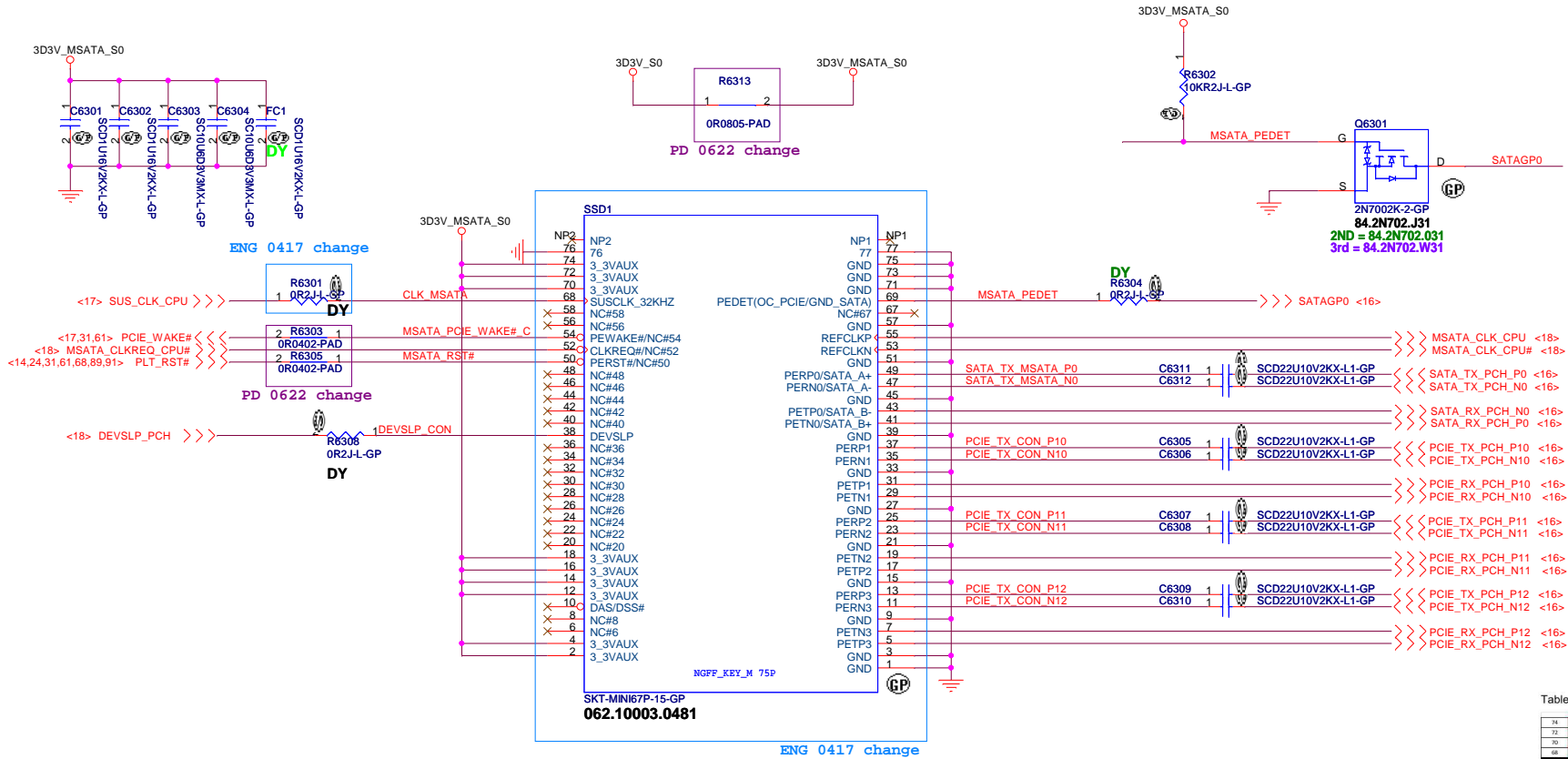


Table 34-5. SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF ²	None	None ³

Notes:

- Design Constraint: For PCIe only application, please refer to the PCIe guidelines for details.
- Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the 10 nF capacitor on Rx can be removed if DC coupled ODDs / devices are NOT used.
- Design Constraint: For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
- Design Constraint: For PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
- Design Constraints, Required: Refer to the Chapter 3, "General Differential Design Guidelines" along with the additional guidelines in this section for all design optimization guidelines.

Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

Pin	Signal	Pin	Signal
74	1.0V	75	GND
72	1.0V	73	GND
70	1.0V	71	GND
68	SUBCKL33MHZ (CPU/PA 3V)	PEDET (OC_PCIE/GND_SATA)	69
	Connector Key	Connector Key	67
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
58	N/C	GND	57
56	N/C	REFCLKP	55
54	PERP0/SATA_A+ (DEVSLP 1V) or N/C	REFCLKN	53
52	CLOCKREQ (CPU/PA 3V) or N/C	GND	51
50	PERP0/SATA_A- (DEVSLP 1V) or N/C	PETN0/SATA_A-	49
48	N/C	PETN0/SATA_A+	47
46	N/C	PETN0/SATA_B-	45
44	N/C	PETN0/SATA_B+	43
42	N/C	GND	41
40	N/C	PERP1	39
38	DEVSLP (0)	PERP1	37
36	N/C	PERP2	35
34	N/C	PERP2	33
32	N/C	PERP3	31
30	N/C	PERP3	29
28	N/C	GND	27
26	N/C	PERP0	25
24	N/C	PERP0	23
22	N/C	GND	21
20	N/C	PERP1	19
18	1.0V	PERP1	17
16	1.0V	PERP2	15
14	1.0V	PERP2	13
12	1.0V	PERP3	11
10	1.0V	PERP3	9
8	N/C	GND	7
6	N/C	PETN0	5
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<Core Design>

緯創資通

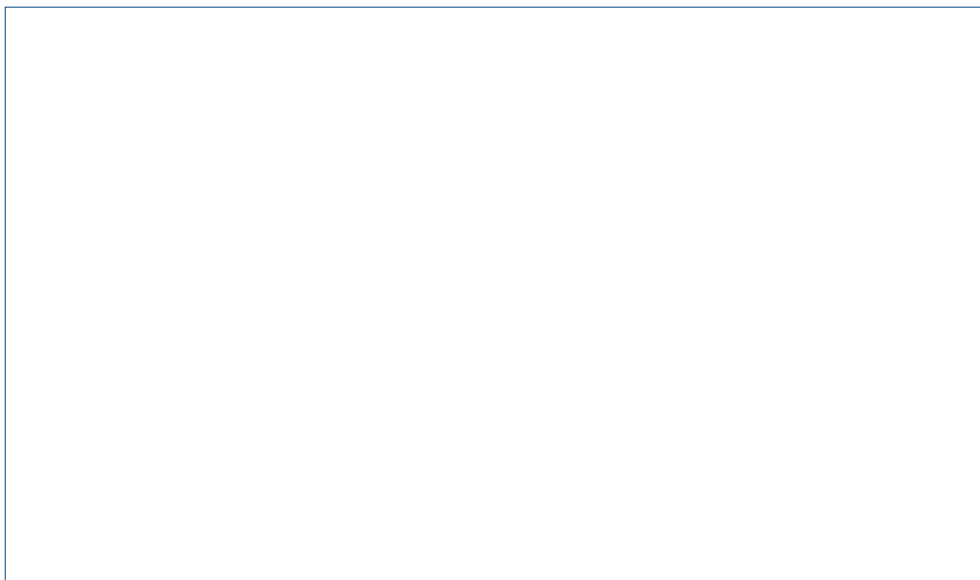
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

SSD-NGFF

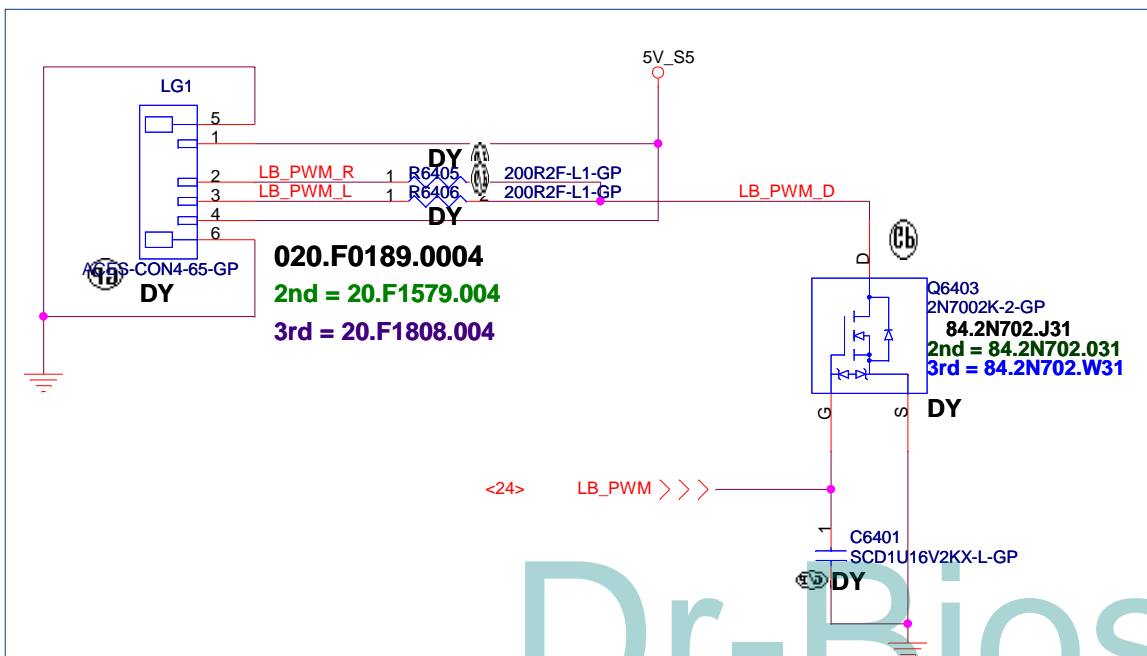
Title	SSD-NGFF		
Size A3	Document Number	Newgate	Rev 1M
Date:	Thursday, August 13, 2015	Sheet 63 of	105

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SSID = User.Interface

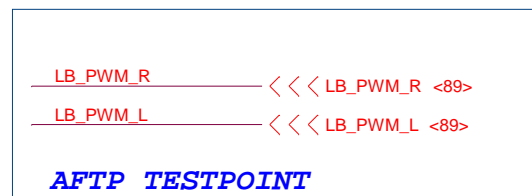
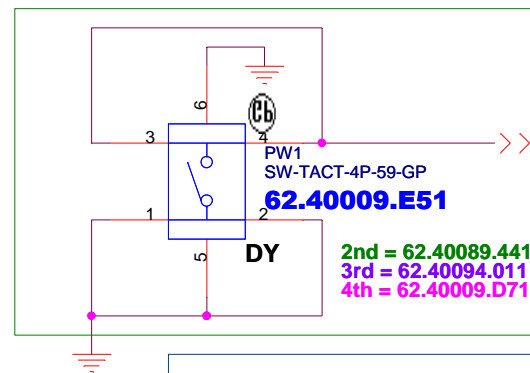


LAB2 0401 change



LAB2 0323 change

Power Button



LAB2 0323 change

<Core Design>

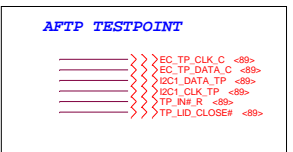
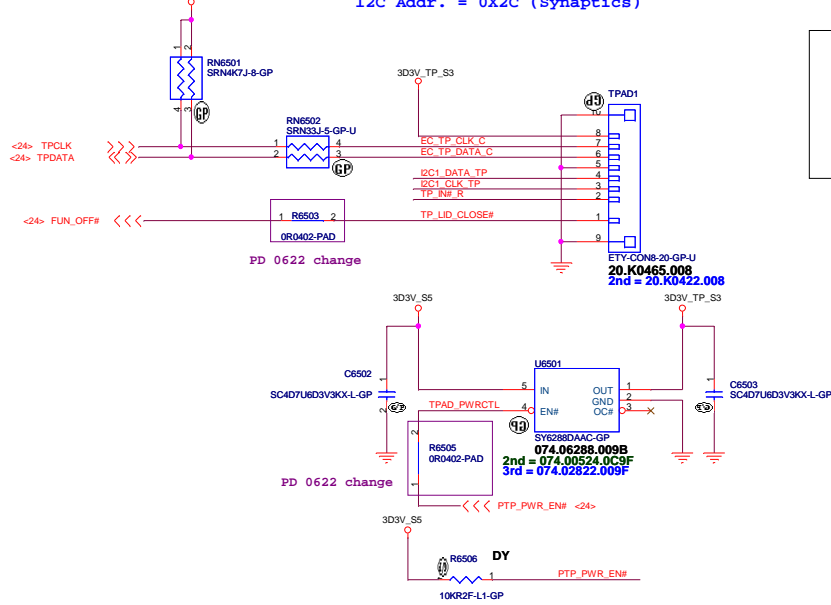
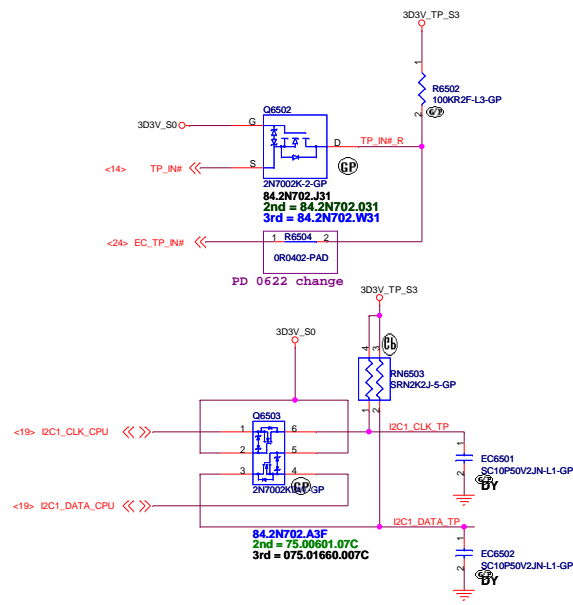
Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	

Title		
LED Bard/Power Button		
Size	Document Number	Rev
A4	Newgate	1M
Date:	Tuesday, August 18, 2015	Sheet 64 of 105

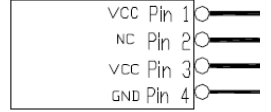
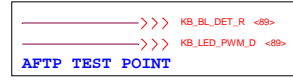
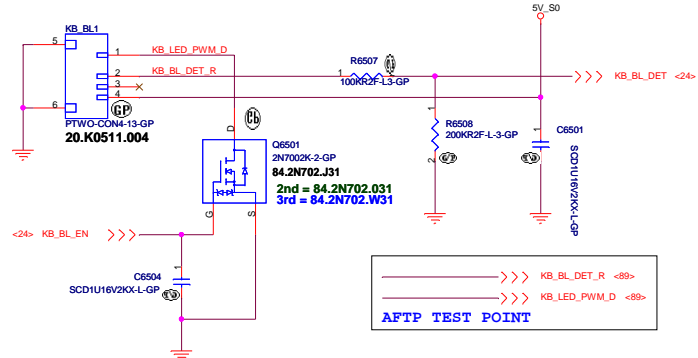
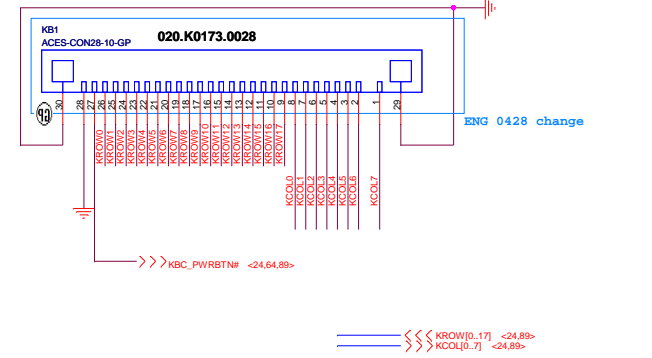
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Precision Touch Pad

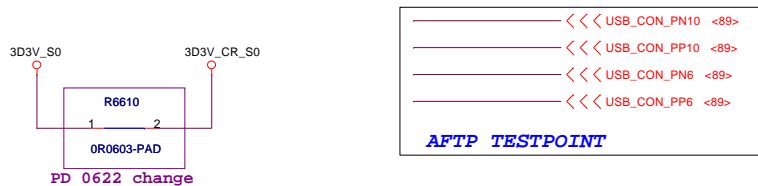
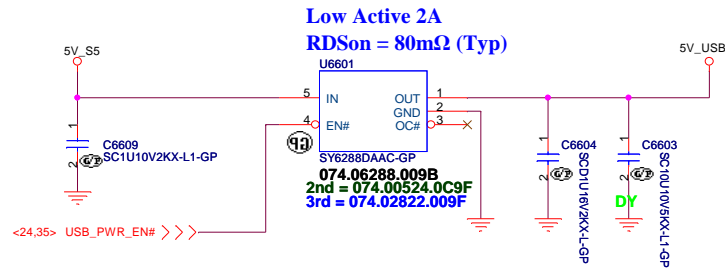
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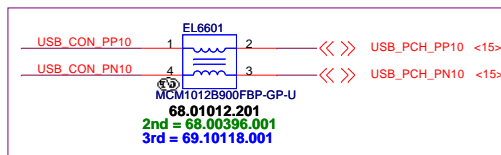
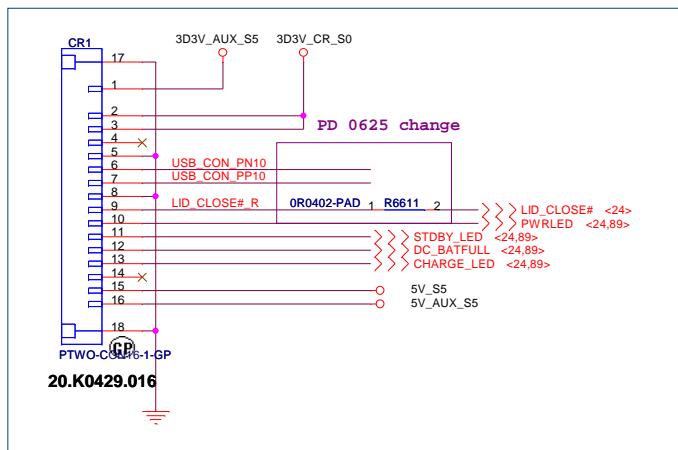
Internal Keyboard Connector



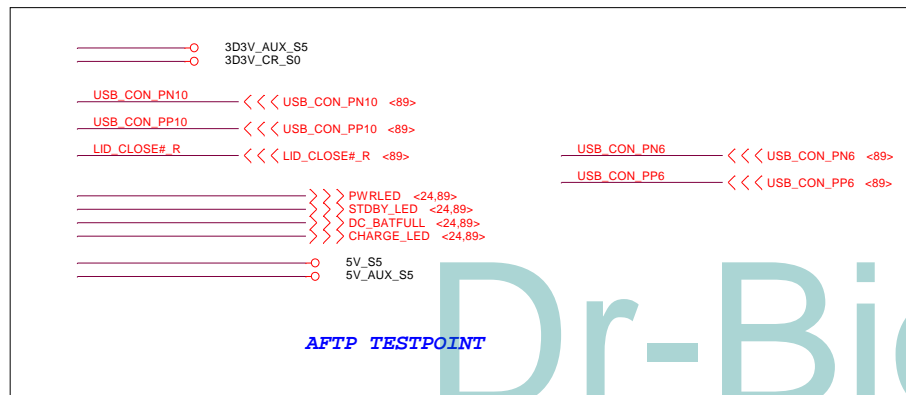
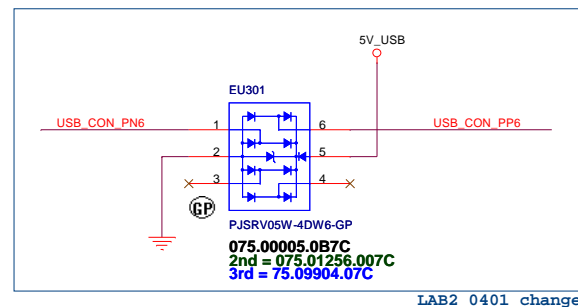
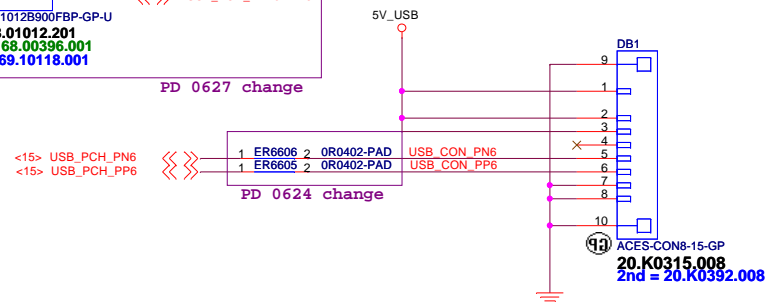
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2(C07)	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100	101	102	103	104	105	106	107	108																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																										
3(C06)	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100	101	102	103	104	105	106	107	108																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																											
4(C05)	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100	101	102	103	104	105	106	107	108																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																										
5(C04)	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100	101	102	103	104	105	106	107	108																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																												
6(C03)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100	101	102	103	104	105	106	107	108																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																													
7(C02)	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255	256	257	258	259	260	261	262	263	264	265	266	267	268	269	270	271	272	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287	288	289	290	291	292	293	294	295	296	297	298	299	300	301	302	303	304	305	306	307	308	309	310	311	312	313	314	315	316	317	318	319	320	321	322	323	324	325	326	327	328	329	330	331	332	333	334	335	336	337	338	339	340	341	342	343	344	345	346	347	348	349	350	351	352	353	354	355	356	357	358	359	360	361	362	363	364	365	366	367	368	369	370	371	372	373	374	375	376	377	378	379	380	381	382	383	384	385	386	387	388	389	390	391	392	393	394	395	396	397	398	399	400	401	402	403	404	405	406	407	408	409	410	411	412	413	414	415	416	417	418	419	420	421	422	423	424	425	426	427	428	429	430	431	432	433	434	435	436	437	438	439	440	441	442	443	444	445	446	447	448	449	450	451	452	453	454	455	456	457	458	459	460	461	462	463	464	465	466	467	468	469	470	471	472	473	474	475	476	477	478	479	480	481	482	483	484	485	486	487	488	489	490	491	492	493	494	495	496	497	498	499	500	501	502	503	504	505	506	507	508	509	510	511	512	513	514	515	516	517	518	519	520	521	522	523	524	525	526	527	528	529	530	531	532	533	534	535	536	537	538	539	540	541	542	543	544	545	546	547	548	549	550	551	552	553	554	555	556	557	558	559	560	561	562	563	564	565	566	567	568	569	570	571	572	573	574	575	576	577	578	579	580	581	582	583	584	585	586	587	588	589	590	591	592	593	594	595	596	597	598	599	600	601	602	603	604	605	606	607	608	609	610	611	612	613	614	615	616	617	618	619	620	621	622	623	624	625	626	627	628	629	630	631	632	633	634	635	636	637	638	639	640	641	642	643	644	645	646	647	648	649	650	651	652	653	654	655	656	657	658	659	660	661	662	663	664	665	666	667	668	669	670	671	672	673	674	675	676	677	678	679	680	681	682	683	684	685	686	687	688	689	690	691	692	693	694	695	696	697	698	699	700	701	702	703	704	705	706	707	708	709	710	711	712	713	714	715	716	717	718	719	720	721	722	723	724	725	726	727	728	729	730	731	732	733	734	735	736	737	738	739	740	741	742	743	744	745	746	747	748	749	750	751	752	753	754	755	756	757	758	759	760	761	762	763	764	765	766	767	768	769	770	771	772	773	774	775	776	777	778	779	780	781	782	783	784	785	786	787	788	789	790	791	792	793	794	795	796	797	798	799	800	801	802	803	804	805	806	807	808	809	810	811	812	813	814	815	816	817	818	819	820	821	822	823	824	825	826	827	828	829	830	831	832	833	834	835	836	837	838	839	840	841	842	843	844	845	846	847	848	849	850	851	852	853	854	855	856	857	858	859	860	861	862	863	864	865	866	867	868	869	870	871	872	873	874	875	876	877	878	879	880	881	882	883	884	885	886	887	888	889	890	891	892	893	894	895	896	897	898	899	900	901	902	903	904	905	906	907	908	909	910	911	912	913	914	915	916	917	918	919	920	921	922	923	924	925	926	927	928	929	930	931	932	933	934	935	936	937	938	939	940	941	942	943	944	945	946	947	948	949	950	951	952	953	954	955	956	957	958	959	960	961	962	963	964	965	966	967	968	969	970	971	972	973	974	975	976	977	978	979	980	981	982	983	984	985	986	987	988	989	990	991	992	993	994	995	996	997	998	999	1000
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Card Reader



USB2.0

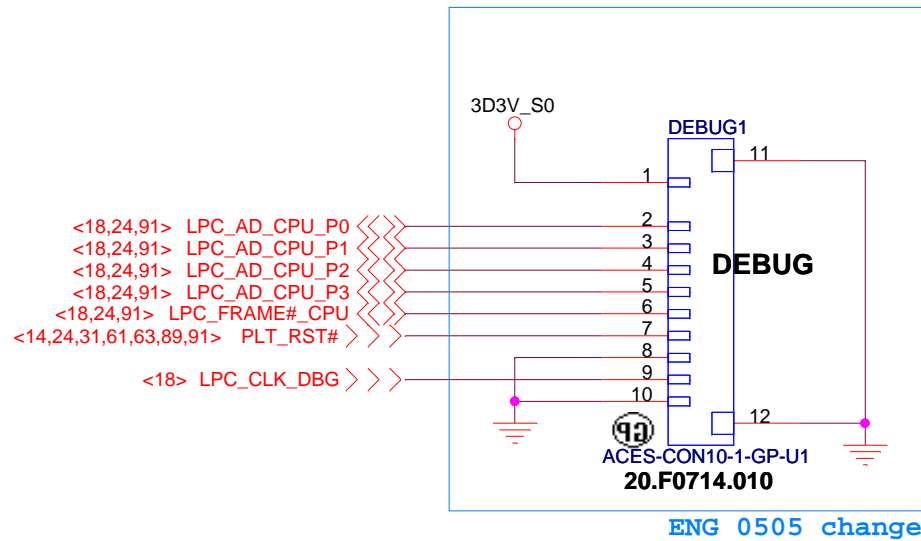


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緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title IO Board Connector		
Size A3	Document Number Newgate	Rev 1M
Date: Thursday, August 13, 2015	Sheet 66	of 105

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<Core Design>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Debug connector			
Size	Document Number		Rev
A	Newgate		1M
Date:	Thursday, August 13, 2015	Sheet 68 of	105

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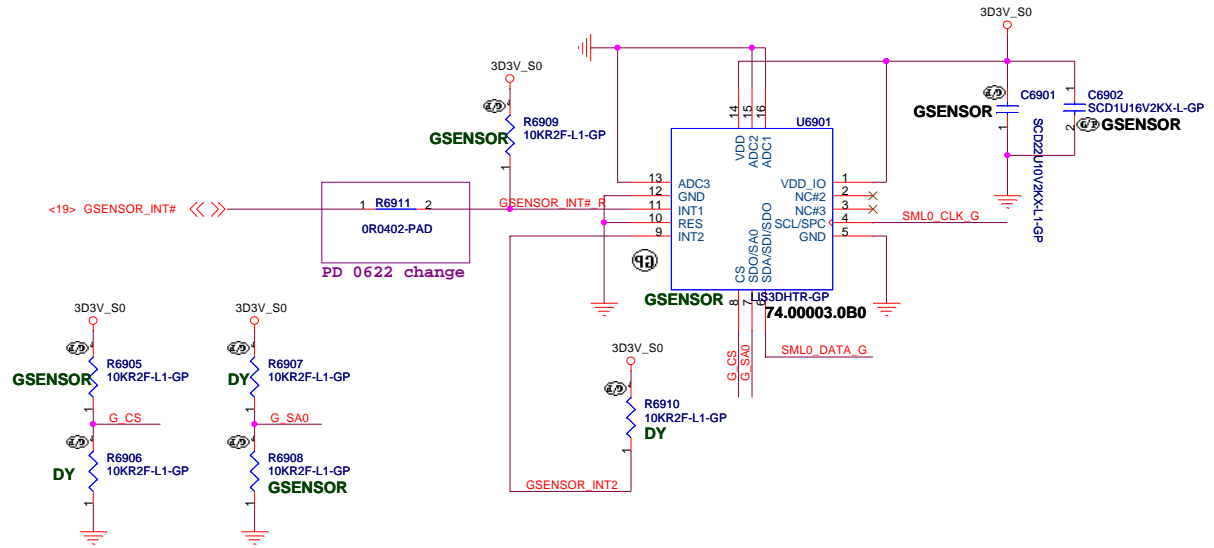
SSID = User.Interface

G Sensor

Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

CHECK WITH MICK



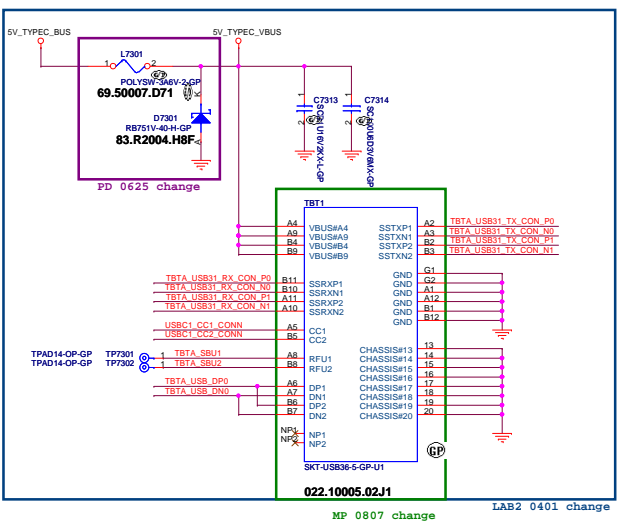
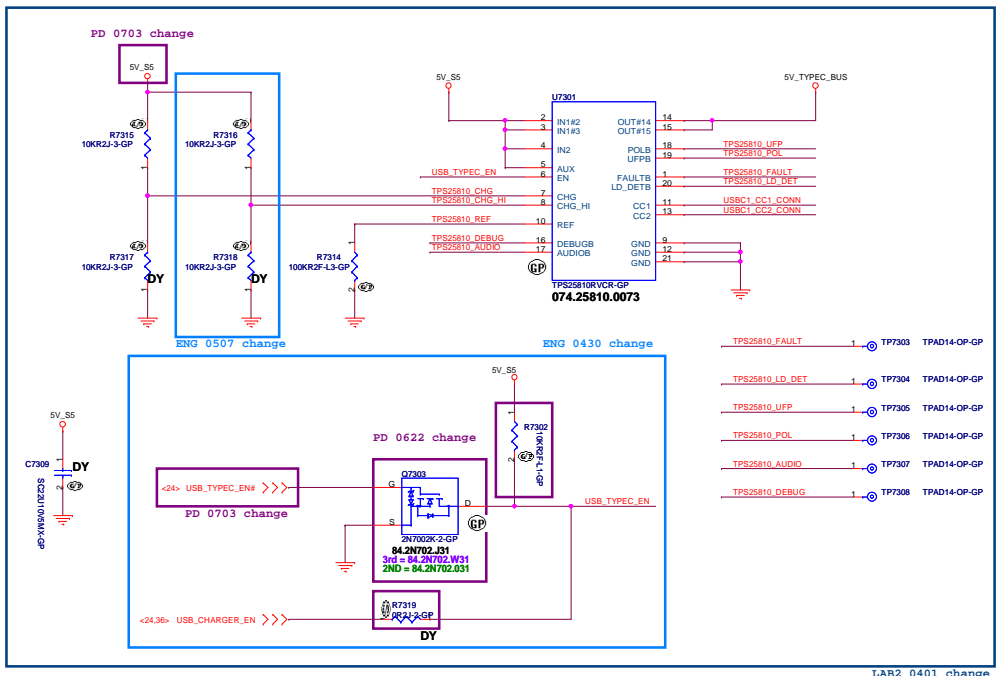
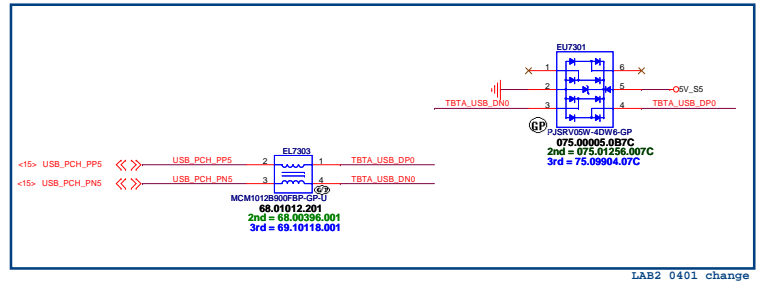
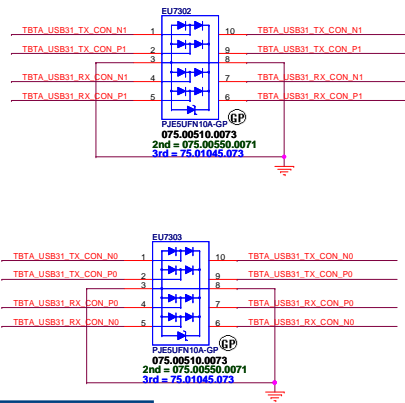
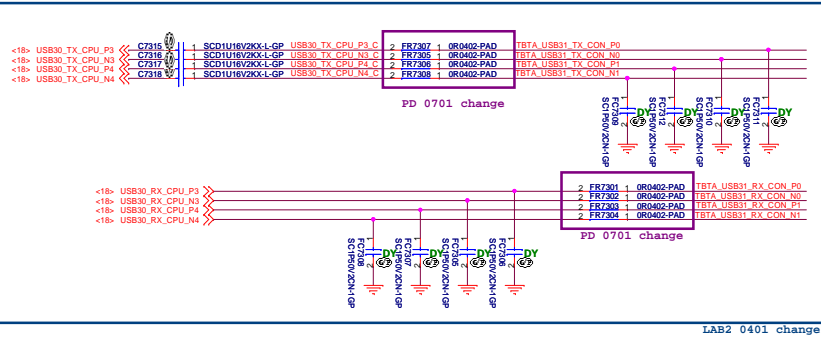
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0R0402-PAD
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0R0402-PAD
PD 0622 change

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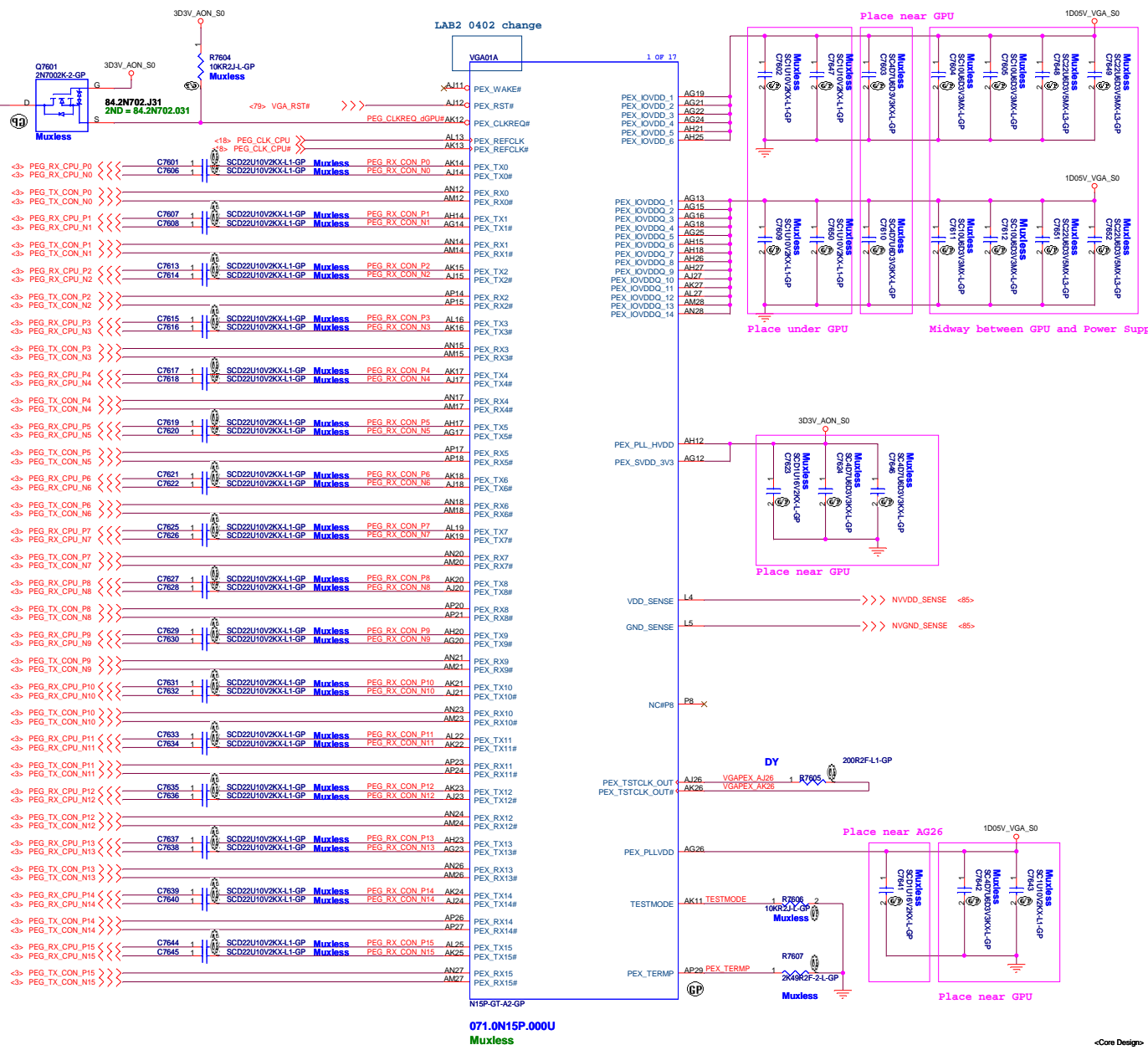
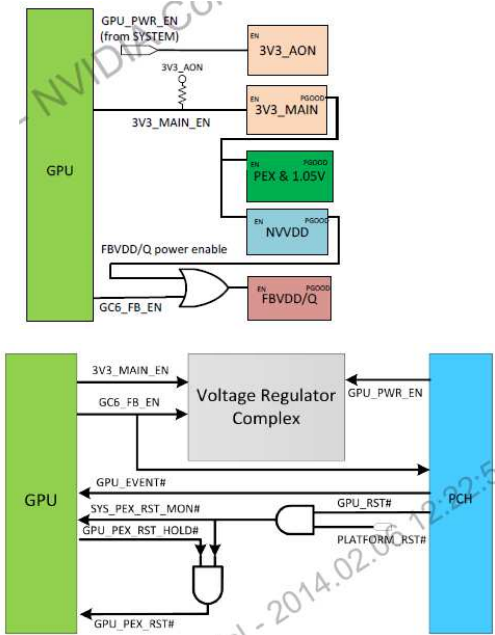
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緯創資通		Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title G-SENSOR		
Size A3	Document Number Newgate	Rev 1M
Date: Thursday, August 13, 2015		
Sheet	69	of 105



CHG	CHG_HI	CC Capability Broadcast	Current Limit	Load Detect Threshold
0	0	STD	1.67 A	NA
0	1	STD	1.67 A	NA
1	0	1.5 A	1.67 A	NA
1	1	3.0 A	3.34 A	1.77 A

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<1479> <GPU_HOLD_RST#> <> R7903 VGA_RST#
 OR2J-L-GP
 NON_GC6



071.0N15P.000U
 Muxless

<Core Design>

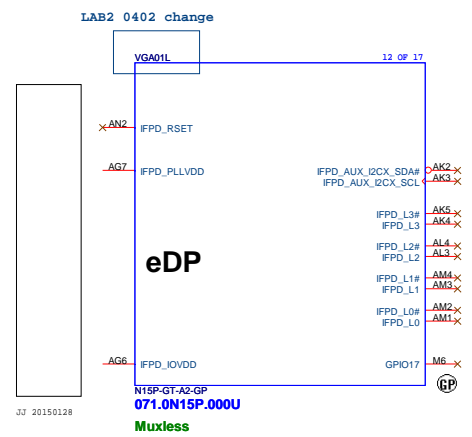
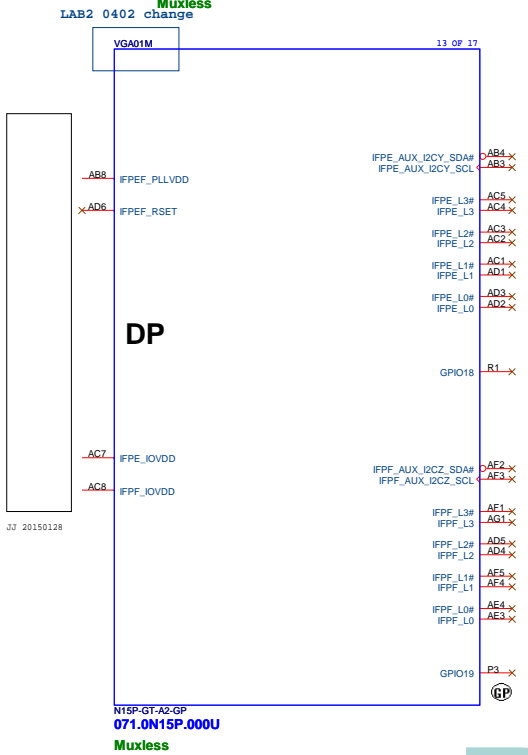
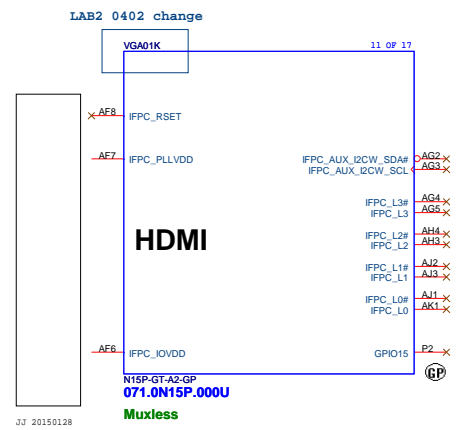
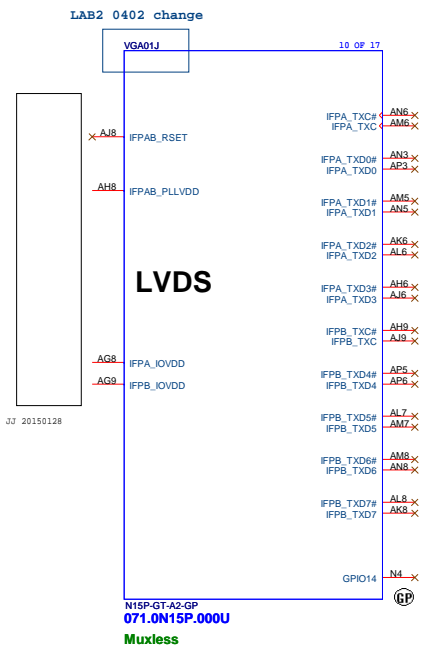
緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin-Tai Wu Rd., Hsinchu, Taipei Hsien 301, Taiwan, R.O.C.

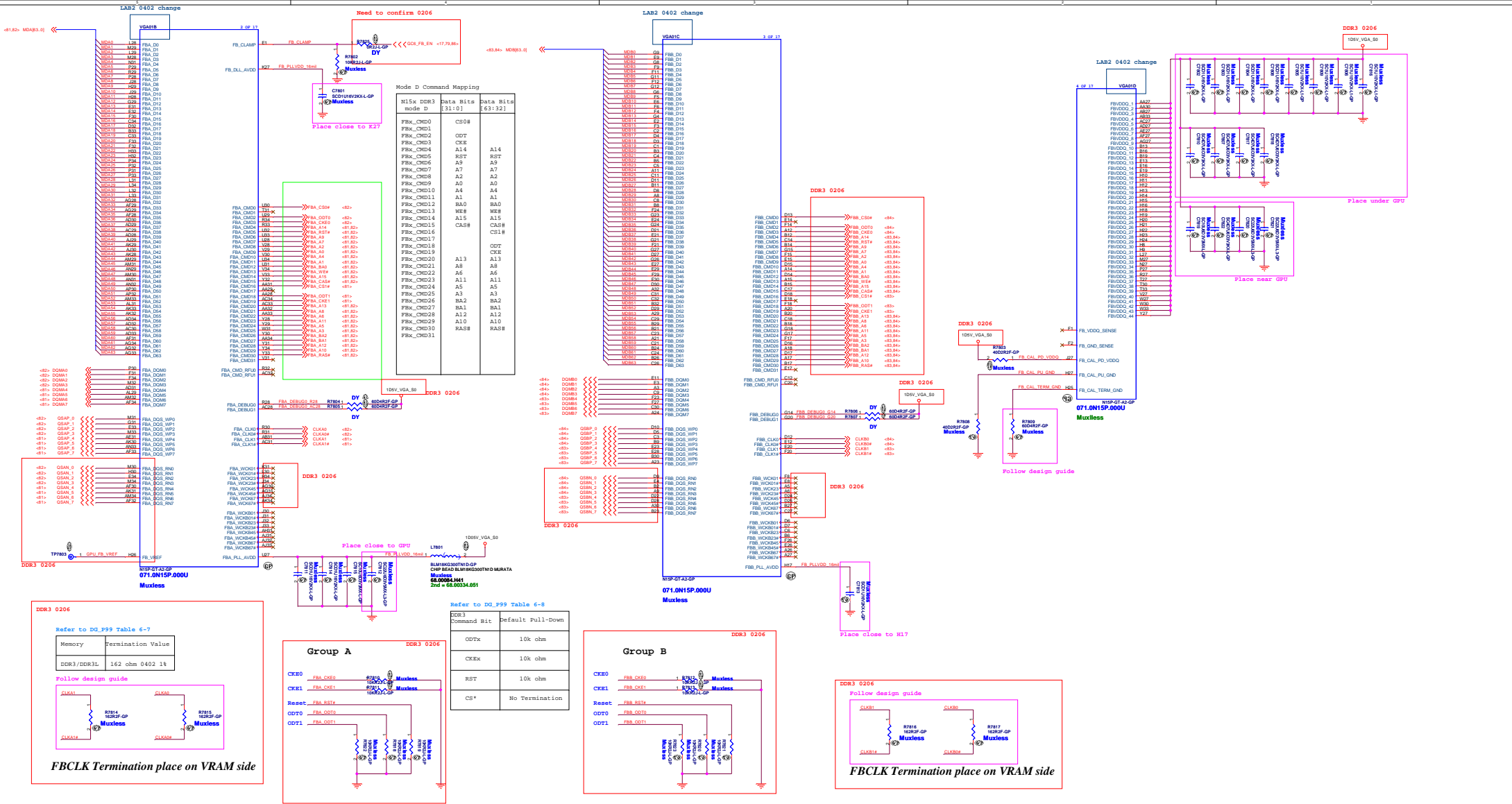
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Size: Custom Document Number: **Newgate** Rev: **1M**

Date: Thursday, August 13, 2015 Sheet: 76 of 105

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1V_VGACORE_S0

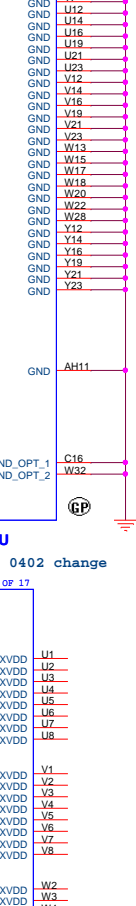
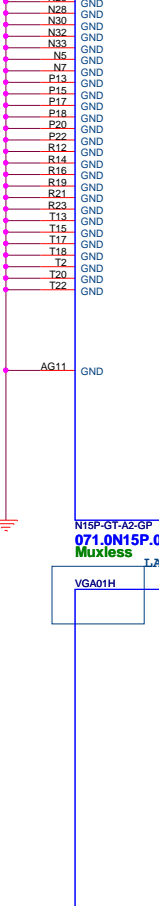
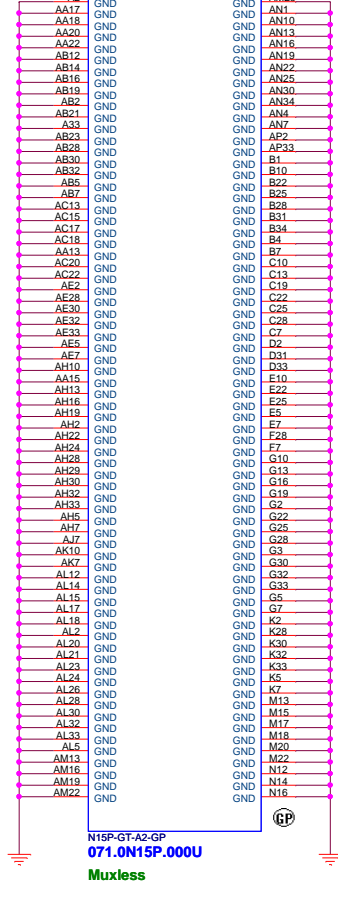
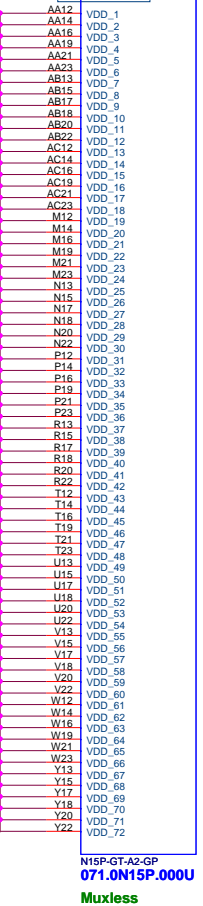
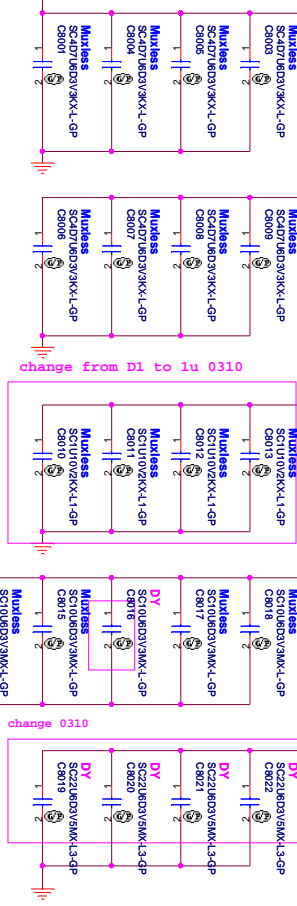
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LAB2 0402 change

LAB2 0402 change

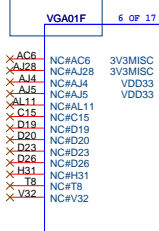
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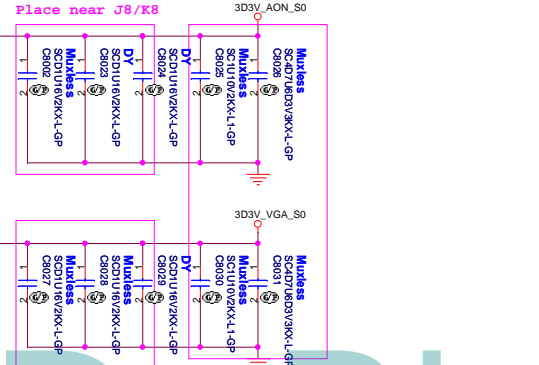


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1uF (X6S)	8
22uF (X5R)	7
4.7uF (X5R)	5
330uF (POS)	1

LAB2 0402 change



N15P-GT-A2-GP
071.0N15P.000U
Muxless



N15P-GT-A2-GP
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Muxless

VGA01H
8 OF 17



N15P-GT-A2-GP
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Muxless

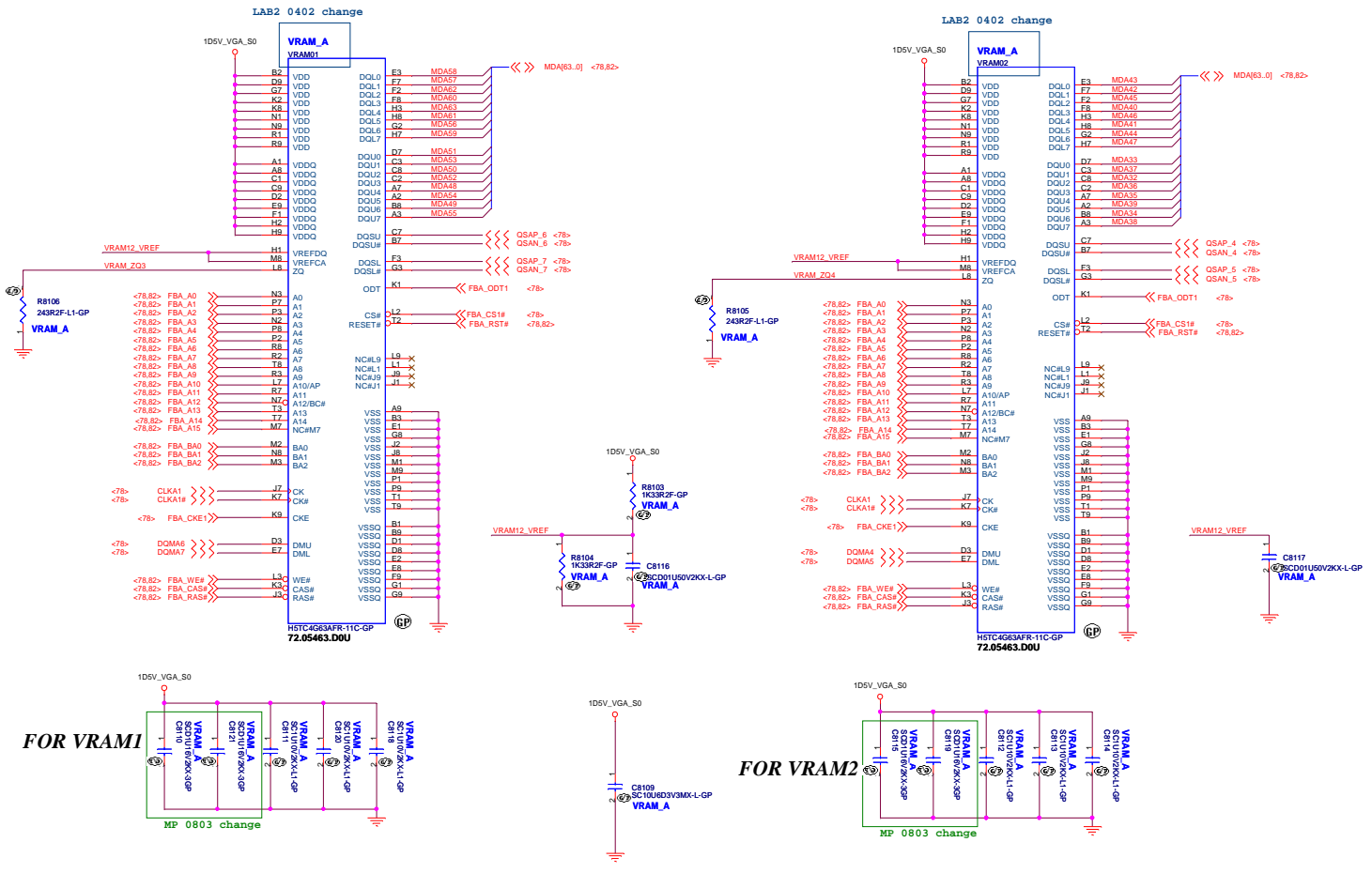
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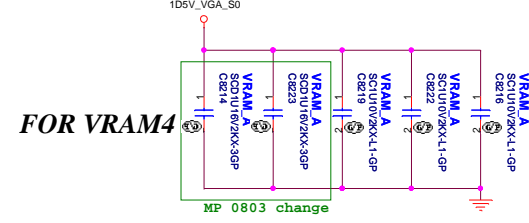
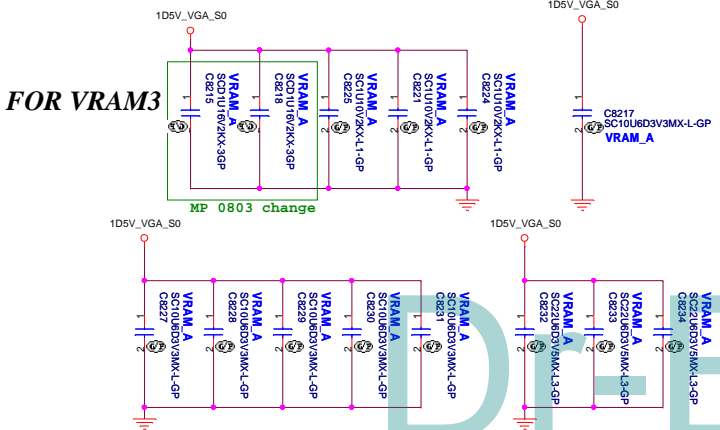
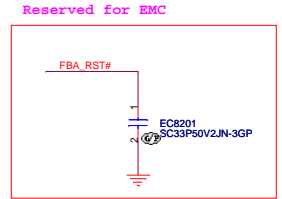
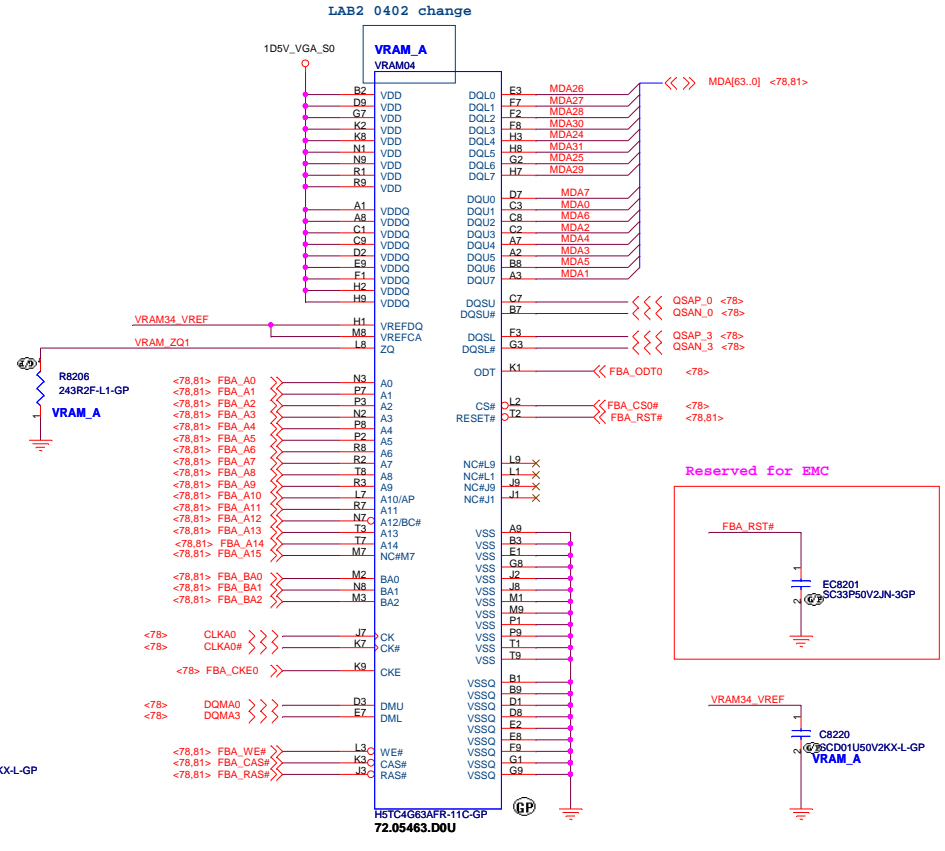
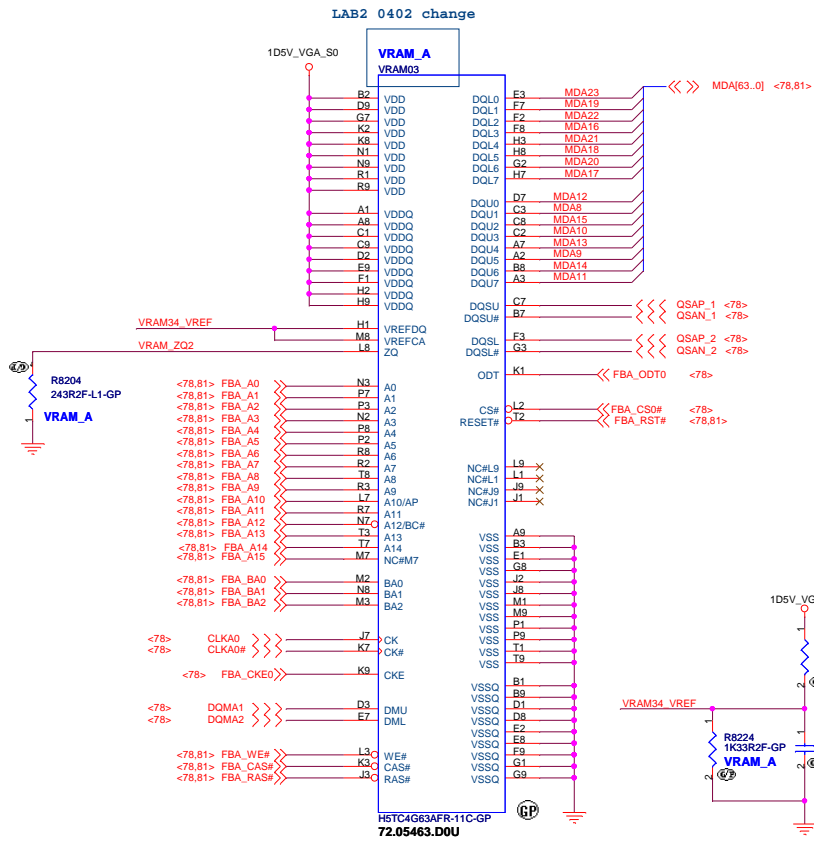
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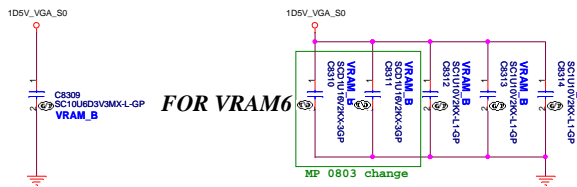
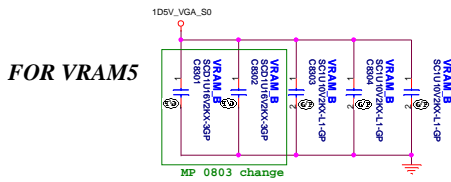
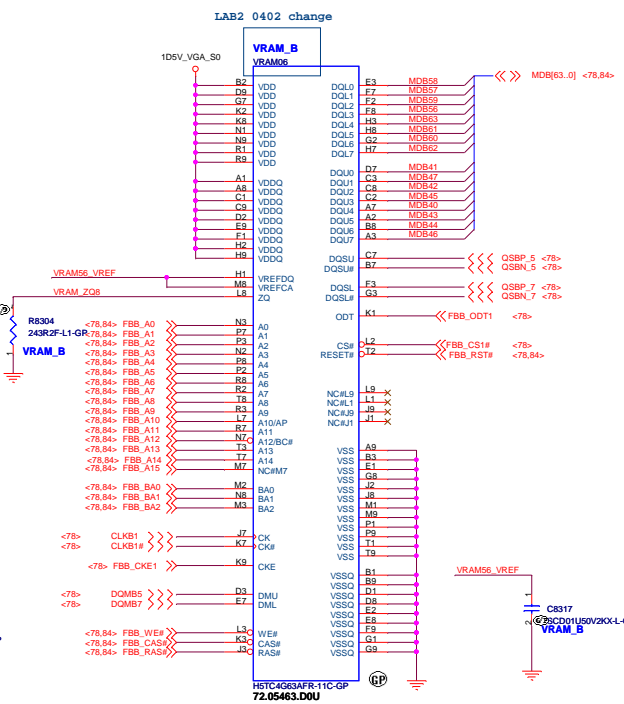
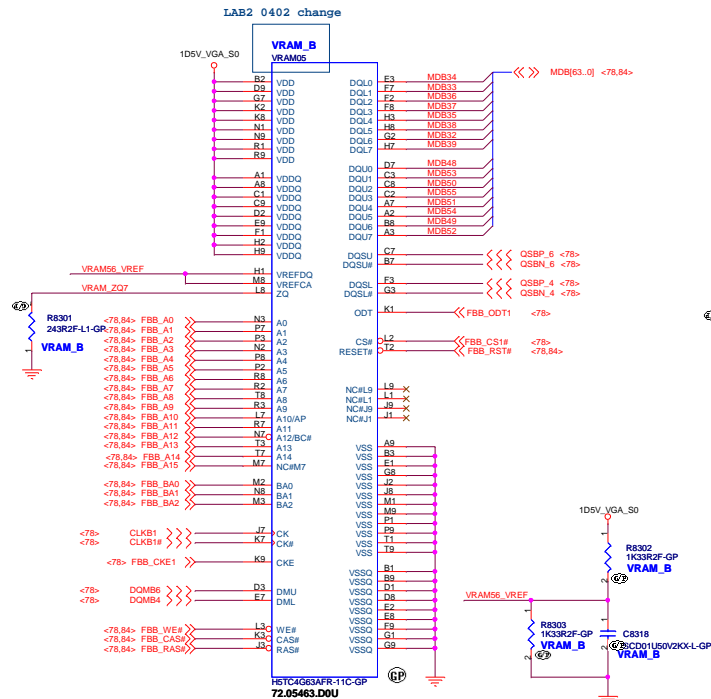
Size Custom Document Number Newgate Rev 1M

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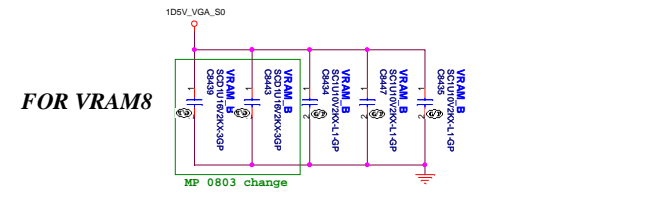
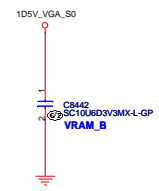
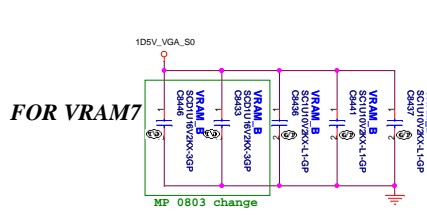
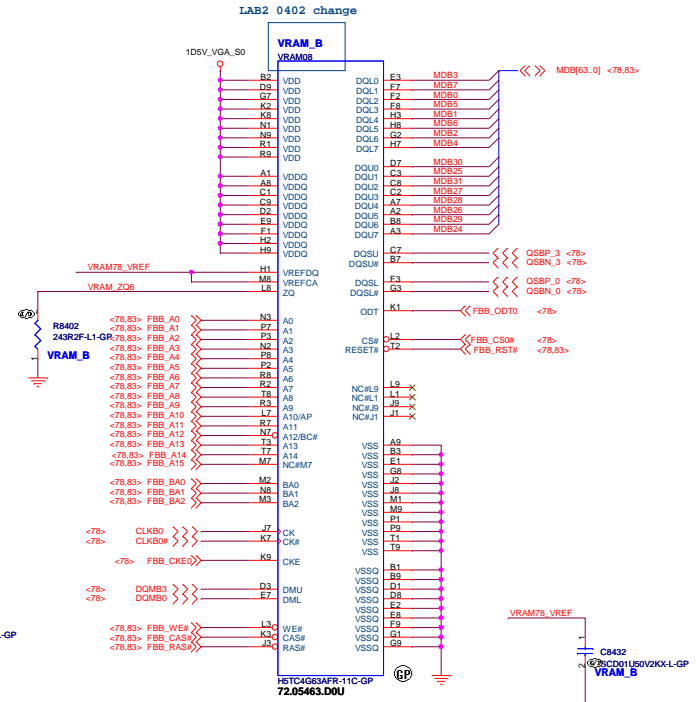
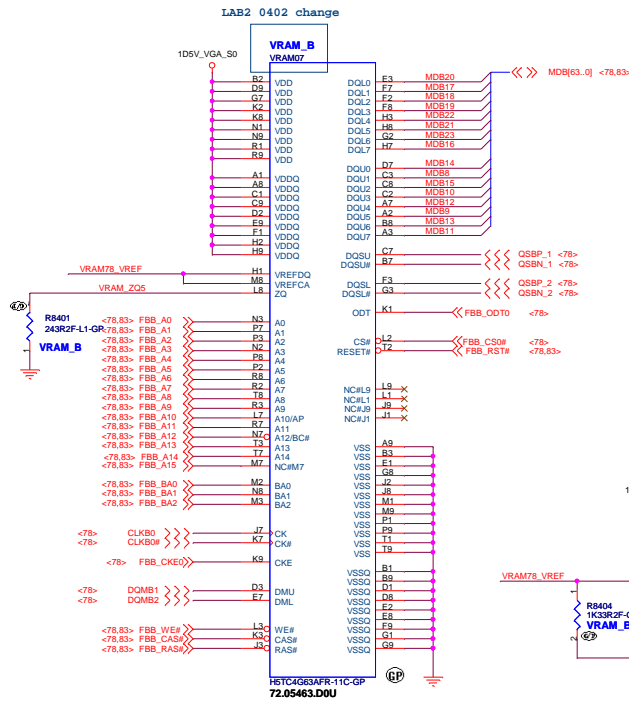




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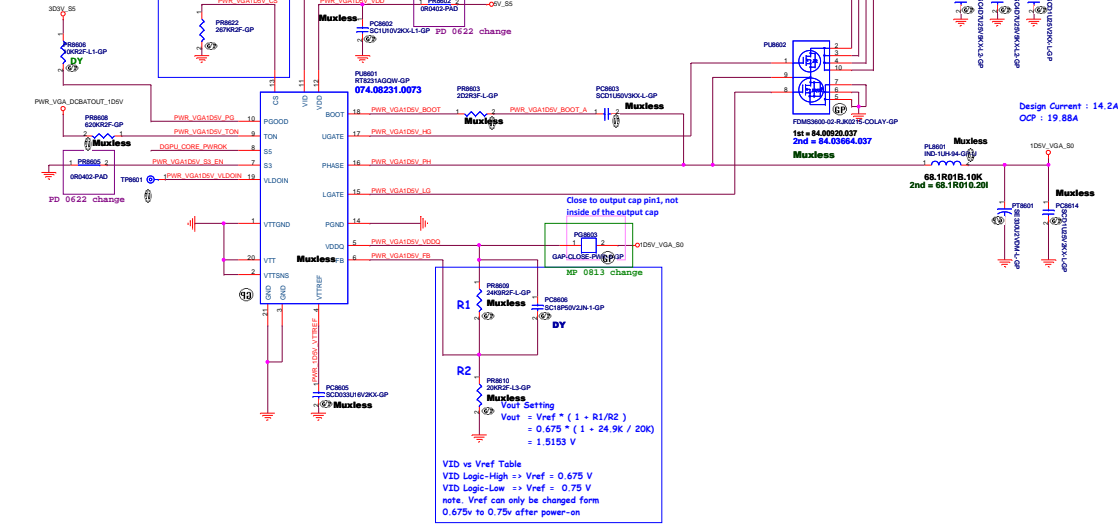
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Title		VRAM CHANNEL_B_5&6
Size	Document Number	Newgate
Custom		Rev 1M
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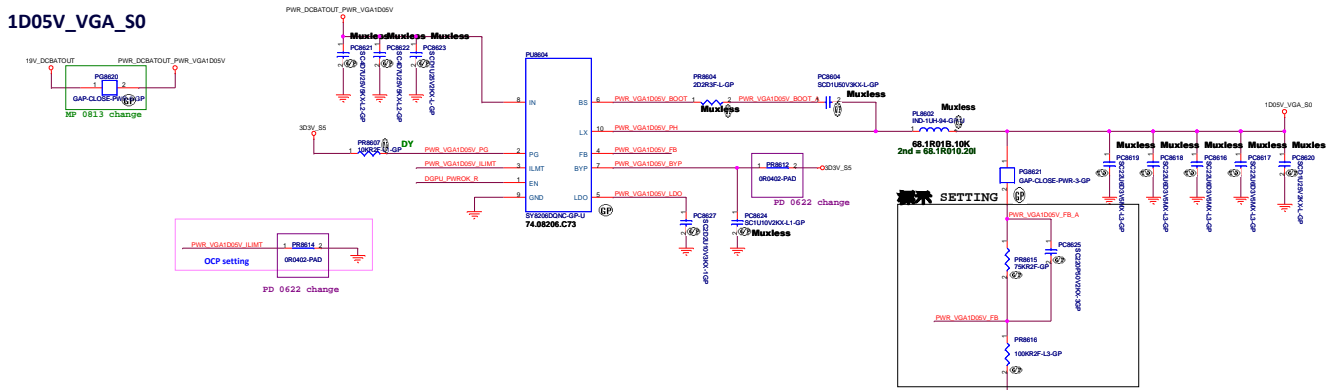


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Floating	12A
Low	8A

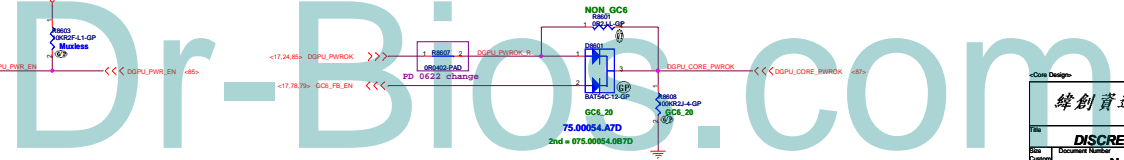
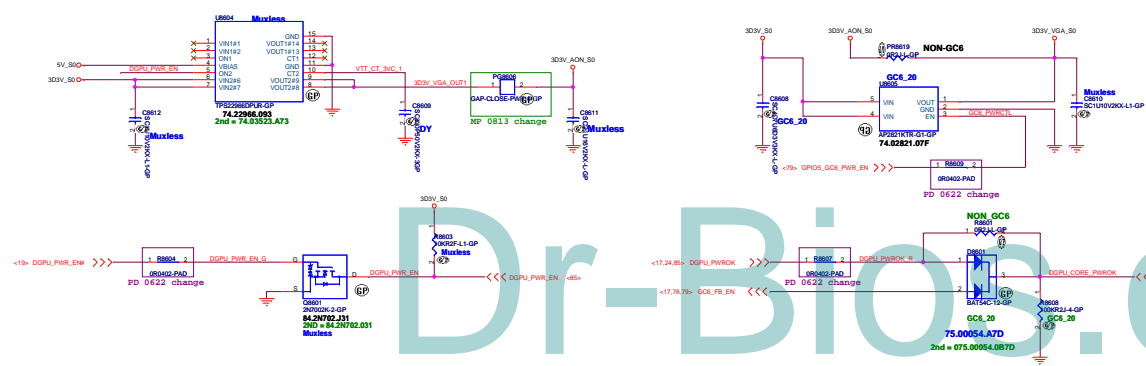
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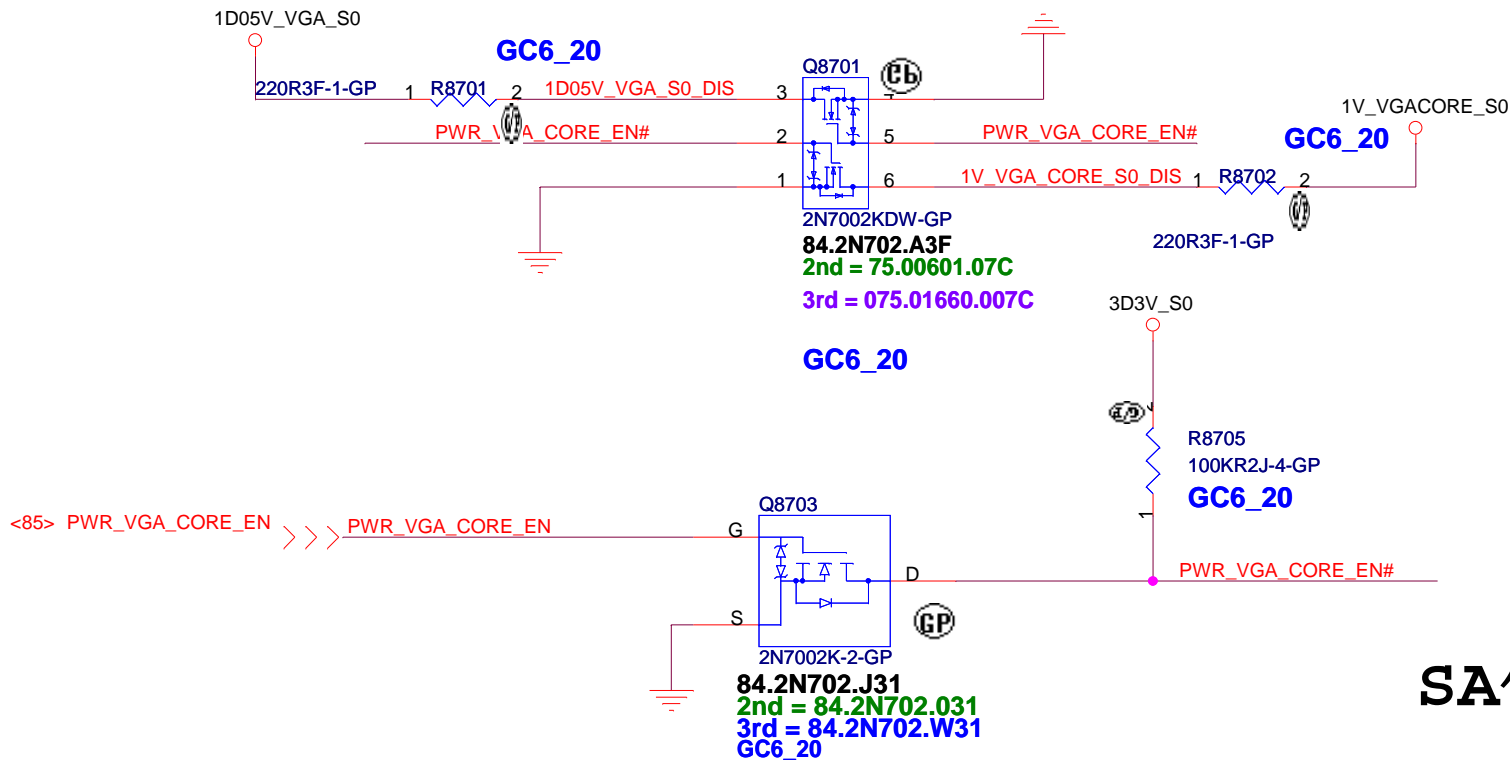


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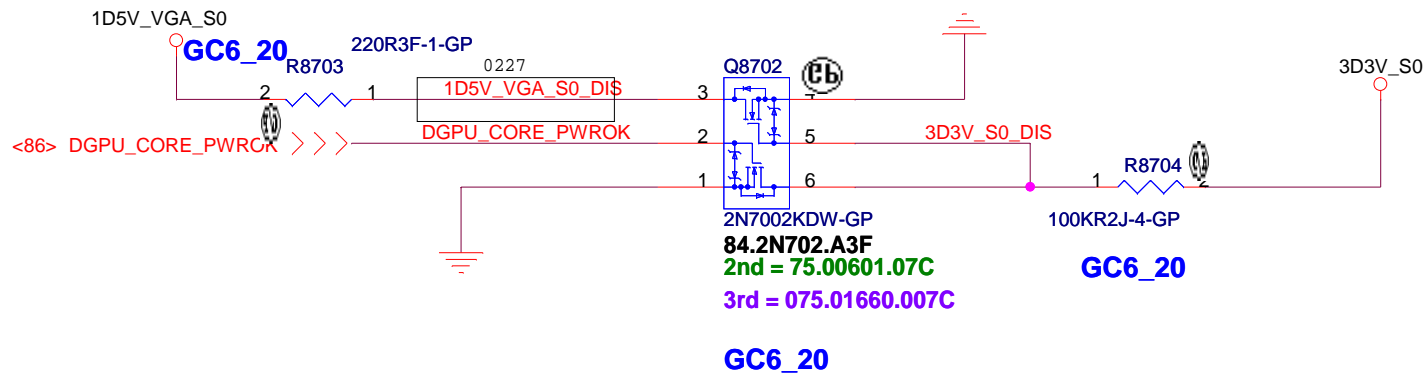


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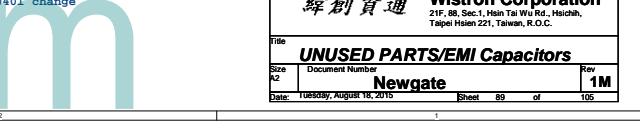
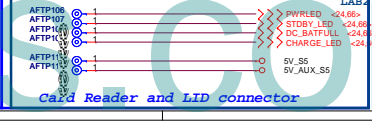
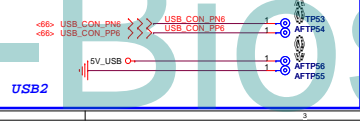
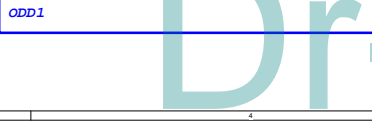
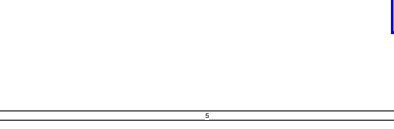
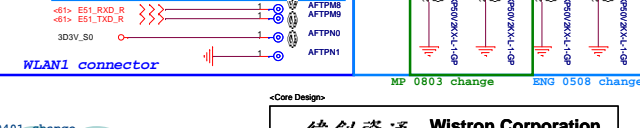
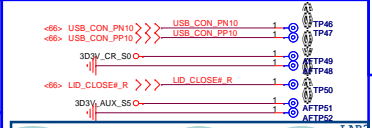
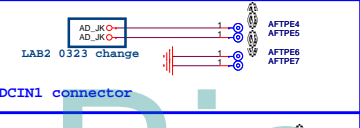
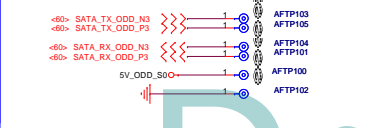
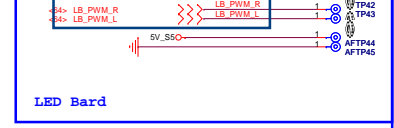
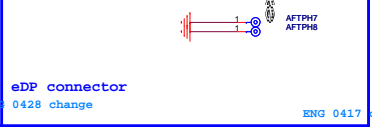
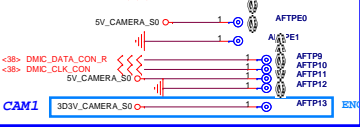
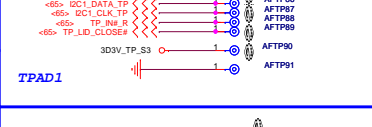
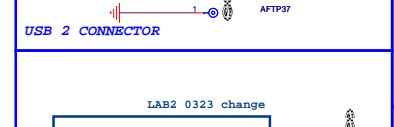
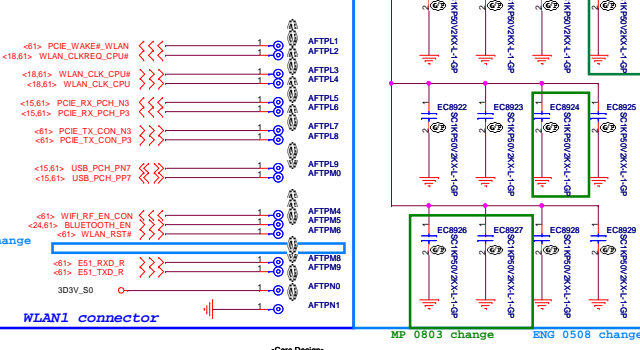
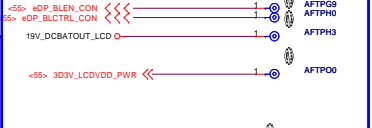
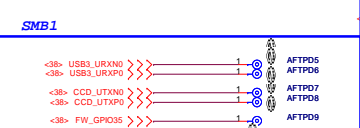
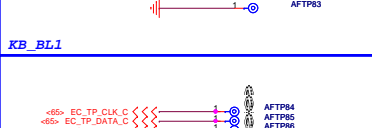
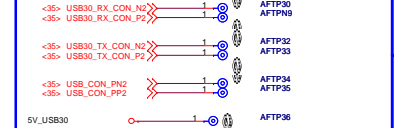
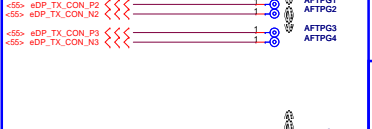
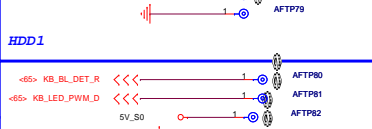
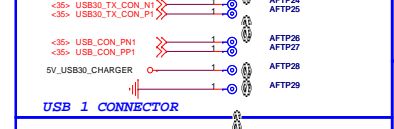
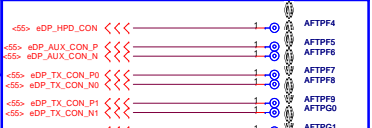
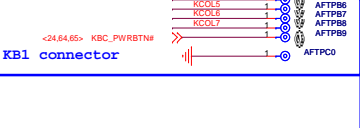
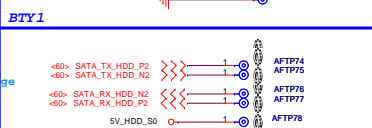
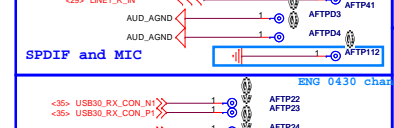
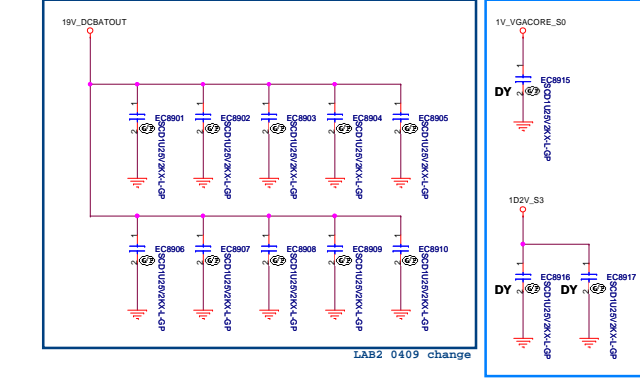
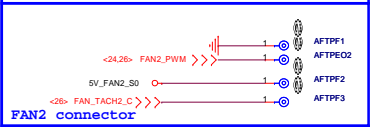
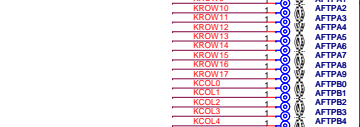
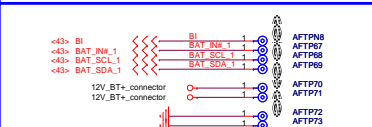
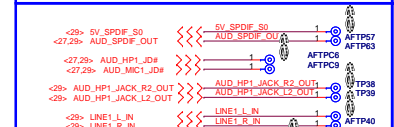
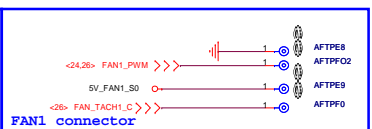
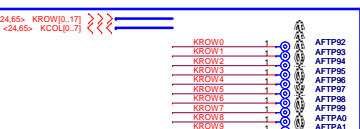
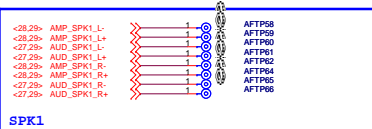
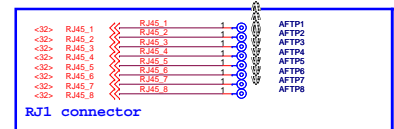
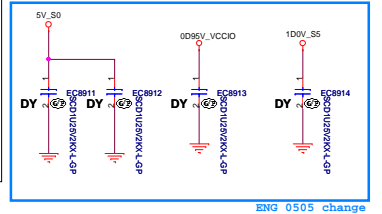
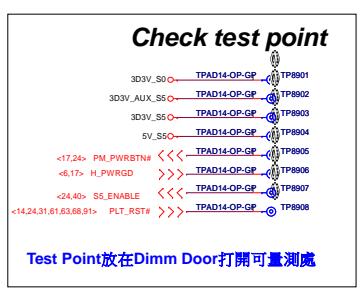
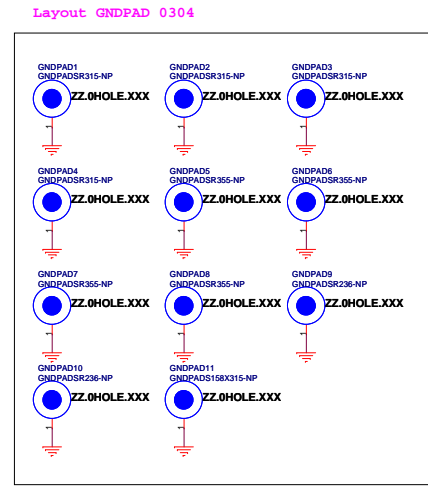
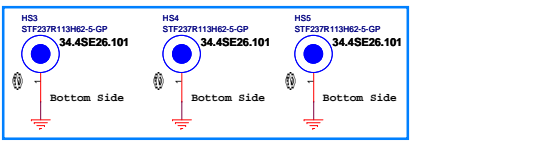
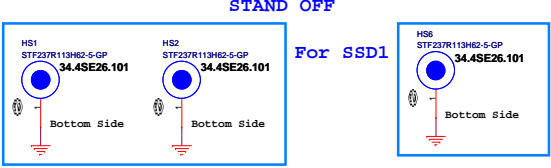
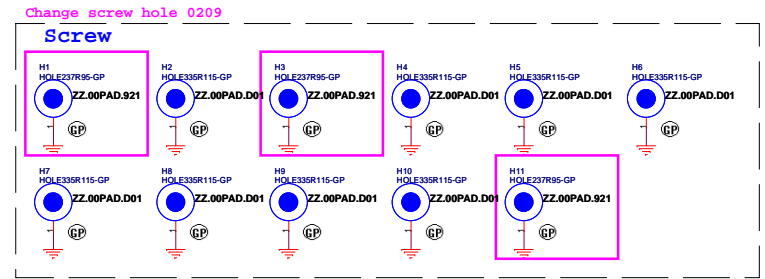
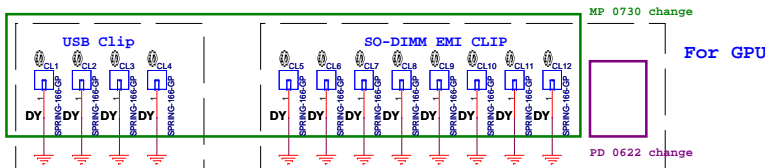
SA做實驗



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Size	Document Number		Rev
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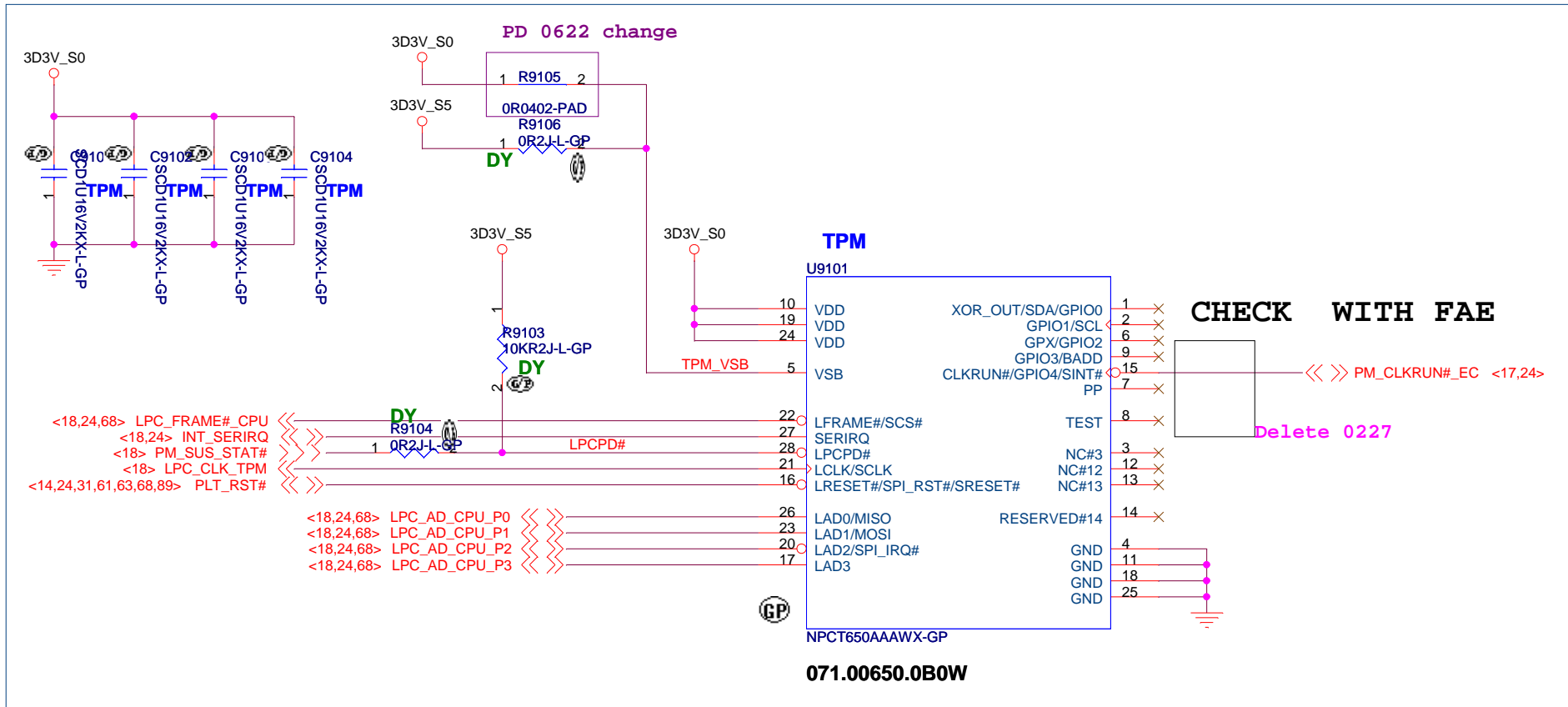
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File: **UNUSED PARTS/EMI Capacitors** Rev: **1M**


Size: Document Number

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LAB2 0401 change

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Size A4	Document Number Newgate
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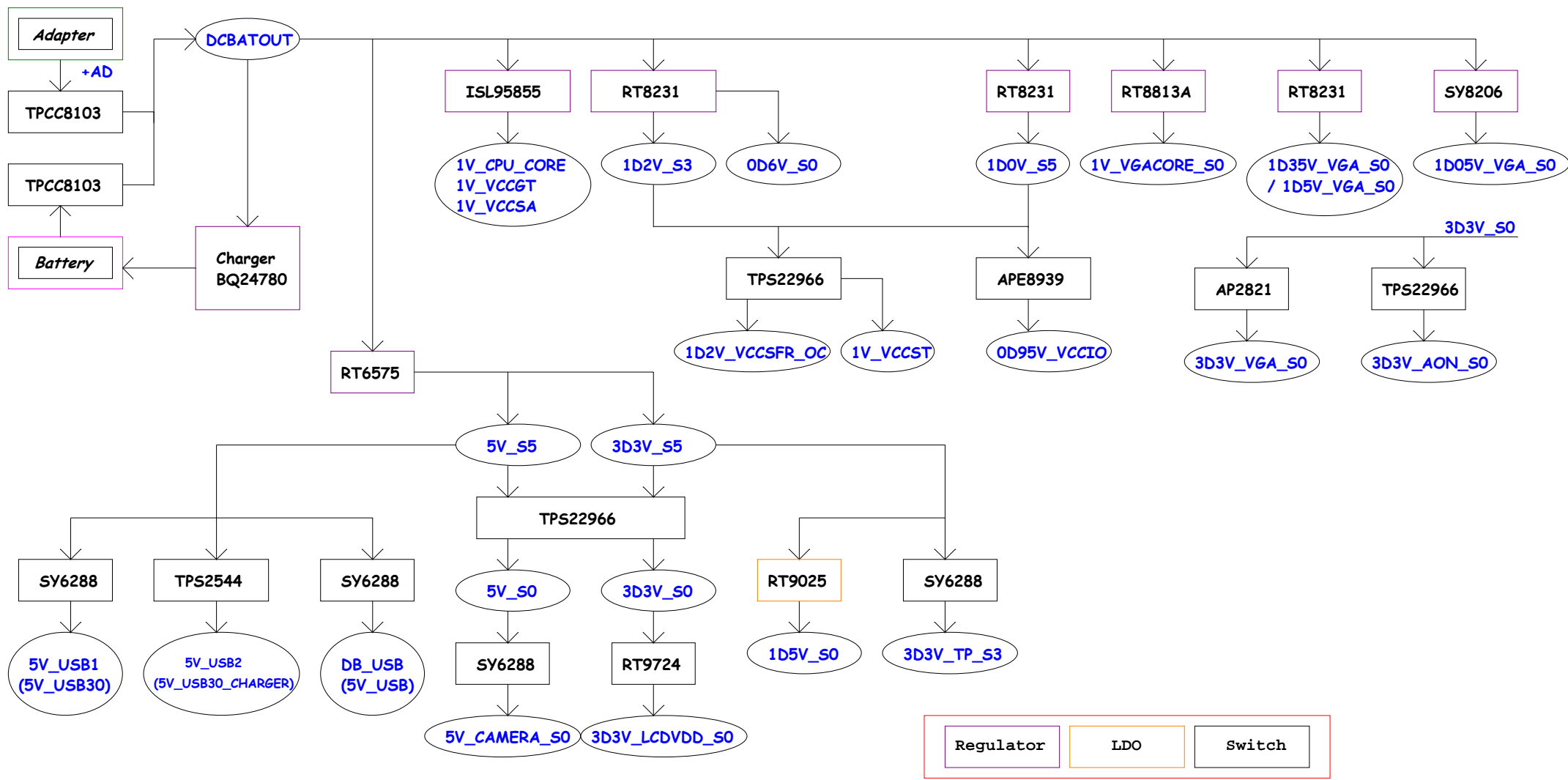
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Taipei Hsien 221, Taiwan, R.O.C.

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Size	Document Number	Rev
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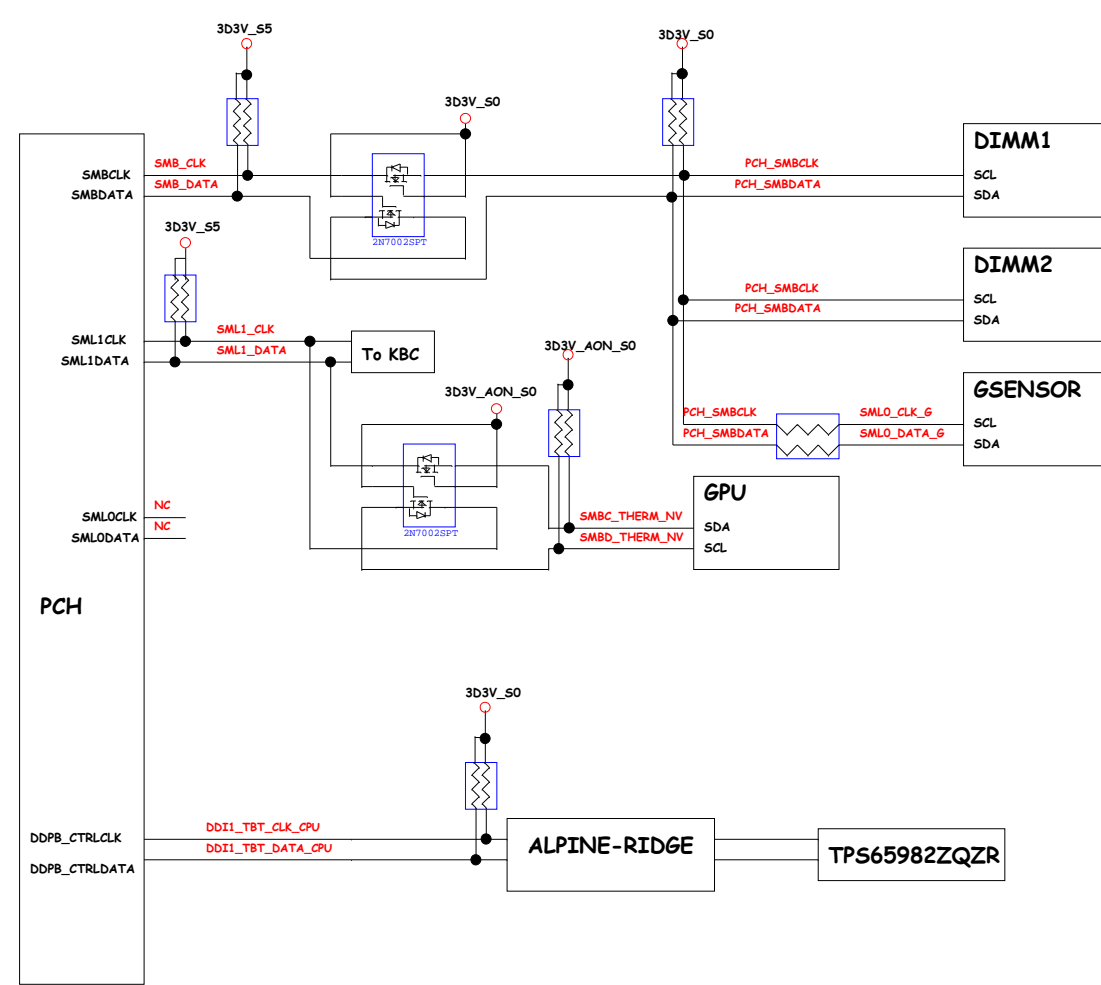
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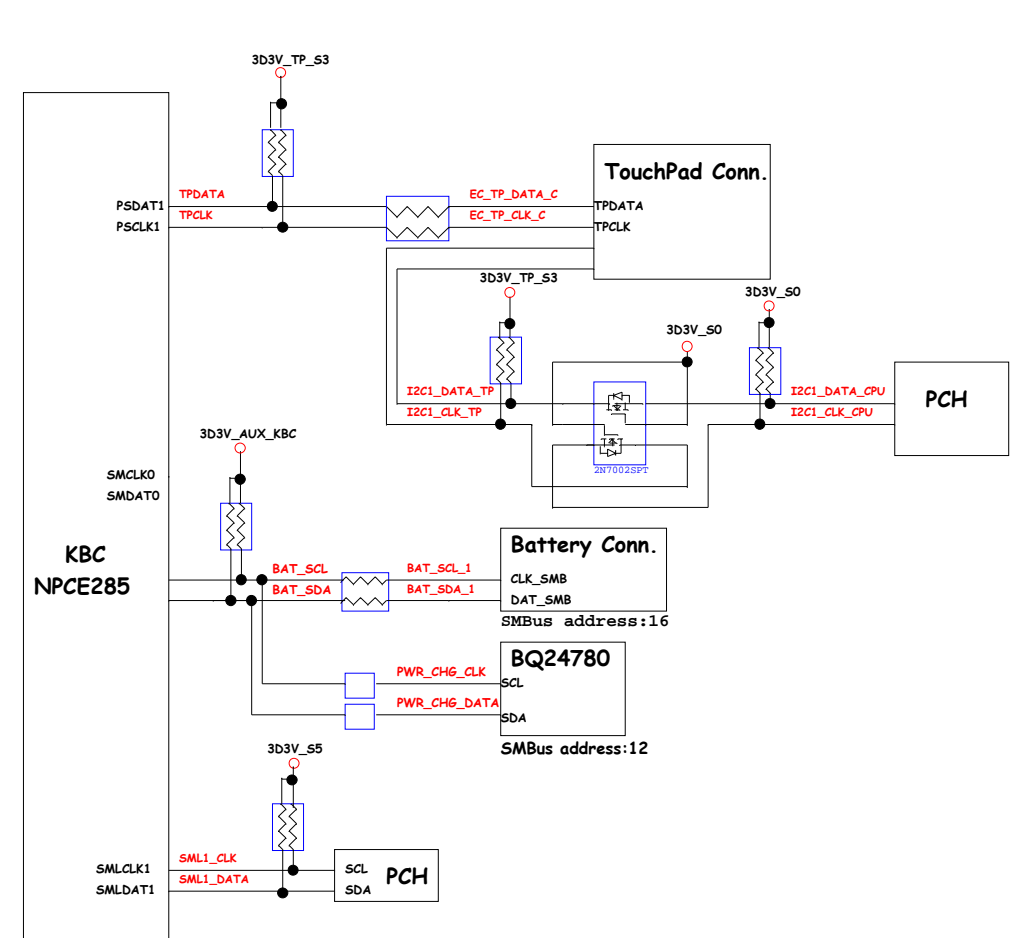
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PCH SMBus Block Diagram



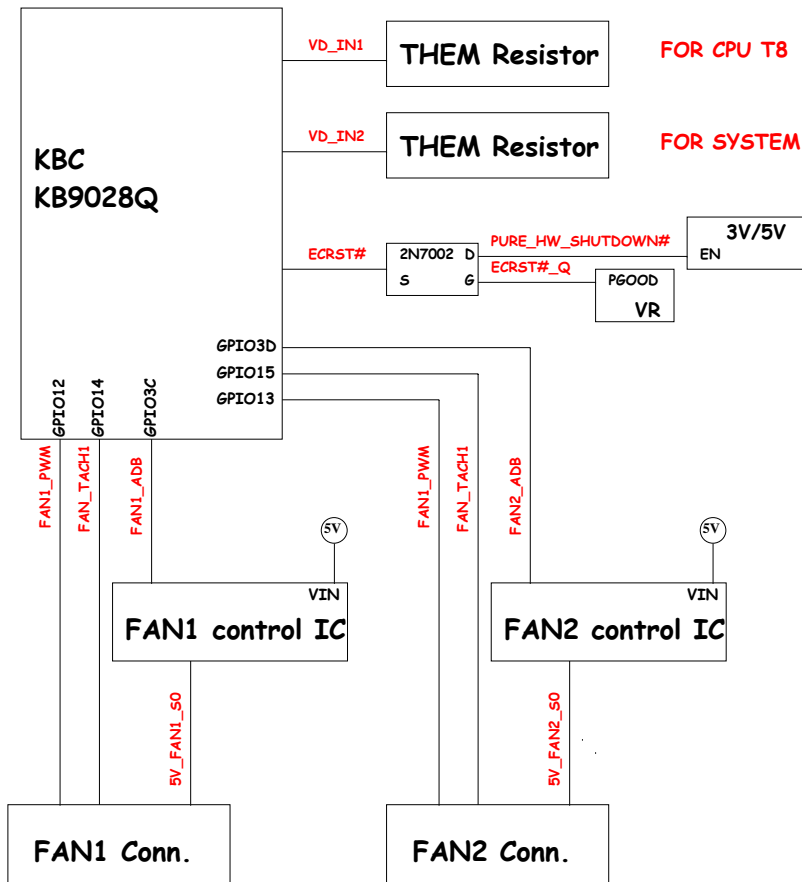
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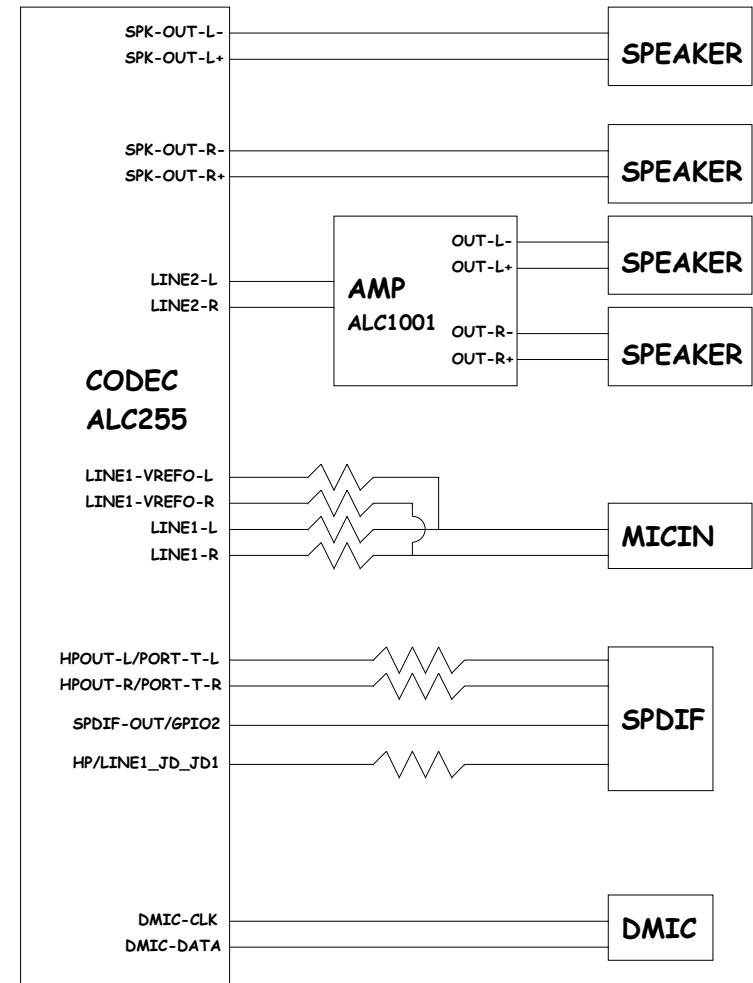
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Title: SMBUS BLOCK DIAGRAM			
Size: Custom	Document Number:	Rev:	1M
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Thermal Block Diagram



Audio Block Diagram



<Core Design>

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Title Thermal /AUDIO Block Diagram	
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