

Poseidon

Schematics Document

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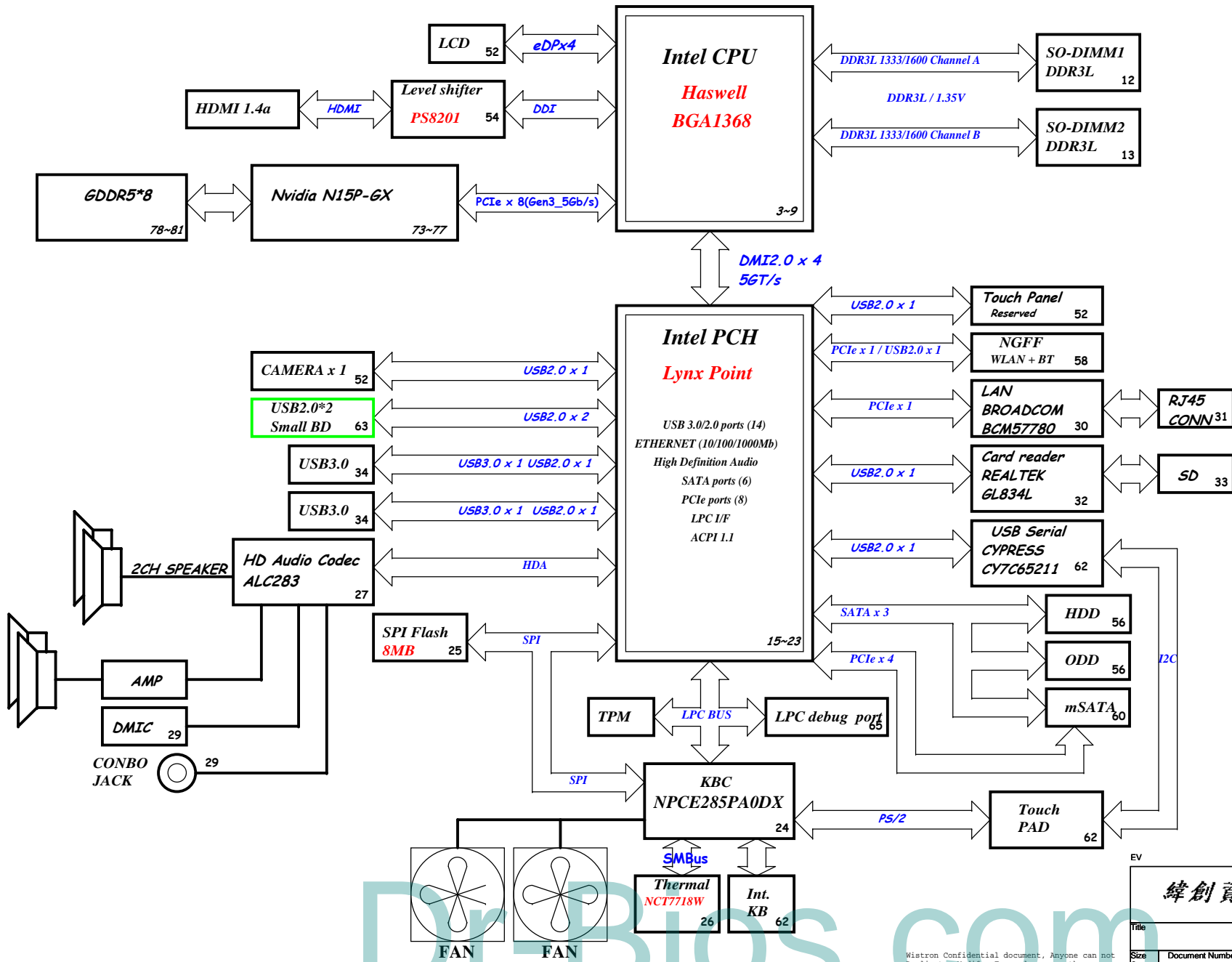
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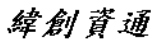
EV

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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Cover Page			
Size	Document Number	Rev	
A3			-1
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Poseidon Board Block Diagram

Project code : 4PD02G010001
 PCB NO : 14203
 Revision : -2



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Block Diagram	
Title Size Custom	Document Number Poseidon 860M
Date: Tuesday, June 17, 2014	Rev -1
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SSID = CPU

Layout Note:

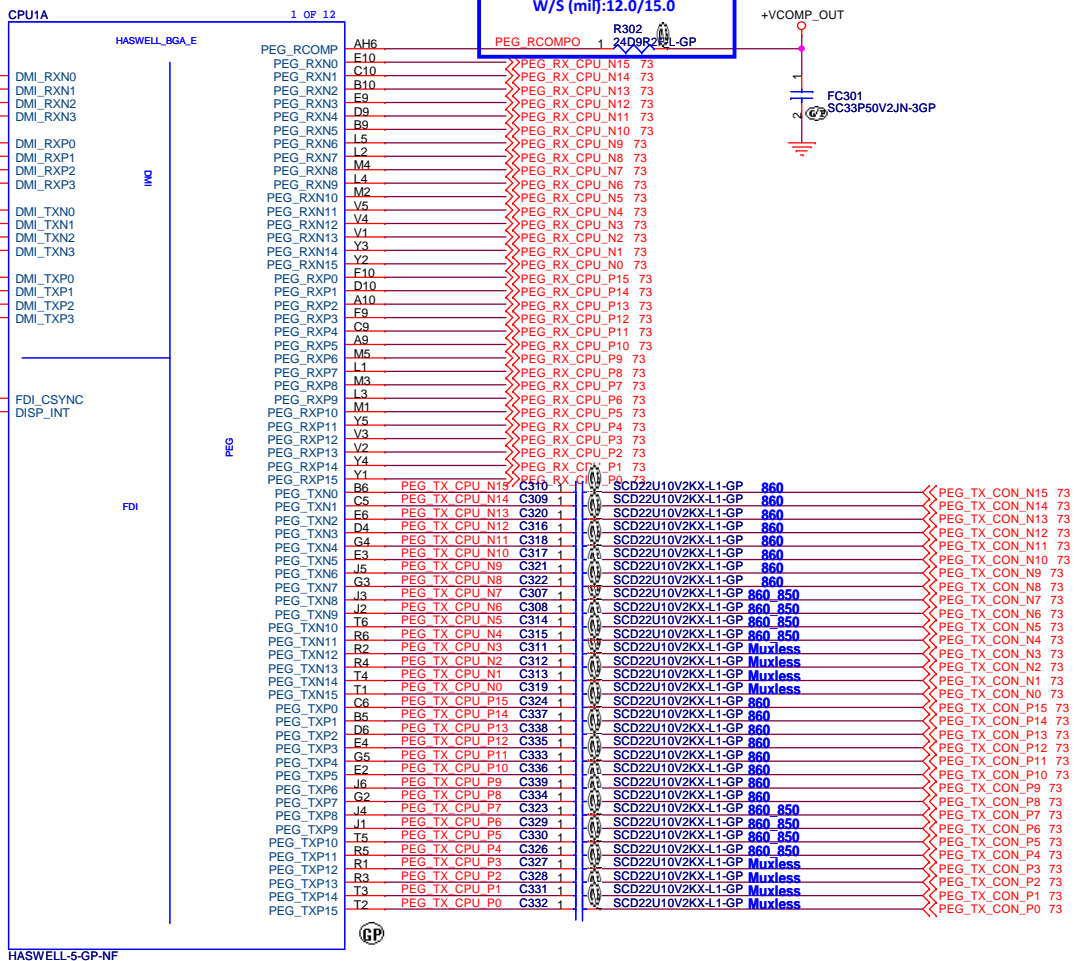
Max Length : 400 Mil
W/s (mil):12.0/15.0

Max Length : 1000~8000 Mil
Max VIA : 3

Layout Note:

- 17 DMI_TX_CPU_N0 <-> DMI TX CPU N0 AB2 DMI_RXN0
- 17 DMI_TX_CPU_N1 <-> DMI TX CPU N1 AB3 DMI_RXN1
- 17 DMI_TX_CPU_N2 <-> DMI TX CPU N2 AC3 DMI_RXN2
- 17 DMI_TX_CPU_N3 <-> DMI TX CPU N3 AC1 DMI_RXN3
- 17 DMI_TX_CPU_P0 <-> DMI TX CPU P0 AB1 DMI_RXP0
- 17 DMI_TX_CPU_P1 <-> DMI TX CPU P1 AB4 DMI_RXP1
- 17 DMI_TX_CPU_P2 <-> DMI TX CPU P2 AC4 DMI_RXP2
- 17 DMI_TX_CPU_P3 <-> DMI TX CPU P3 AC2 DMI_RXP3
- 17 DMI_RX_CPU_N0 <-> DMI RX CPU N0 AE2 DMI_TXN0
- 17 DMI_RX_CPU_N1 <-> DMI RX CPU N1 AE4 DMI_TXN1
- 17 DMI_RX_CPU_N2 <-> DMI RX CPU N2 AG4 DMI_TXN2
- 17 DMI_RX_CPU_N3 <-> DMI RX CPU N3 AG2 DMI_TXN3
- 17 DMI_RX_CPU_P0 <-> DMI RX CPU P0 AE1 DMI_TXP0
- 17 DMI_RX_CPU_P1 <-> DMI RX CPU P1 AE3 DMI_TXP1
- 17 DMI_RX_CPU_P2 <-> DMI RX CPU P2 AG3 DMI_TXP2
- 17 DMI_RX_CPU_P3 <-> DMI RX CPU P3 AG1 DMI_TXP3

- 17 FDI_CSYNC_CPU <-> F11 FDI_CSYNC
- 17 FDI_INT_CPU <-> F12 FDI_DISP_INT



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x16 Controller Negotiated Width	x8 Controller Negotiated Width	x4 Controller Negotiated Width	Processor	Physical Lanes															
				0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
x16	Off	Off	Direct	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
x8	x8	Off	Direct	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
x8	x4	x4	Direct	0	1	2	3	4	5	6	7	0	1	2	3	0	1	2	3
x16	Off	Off	Reverse	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
x8	x8	Off	Reverse	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
x8	x4	x4	Reverse	3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0

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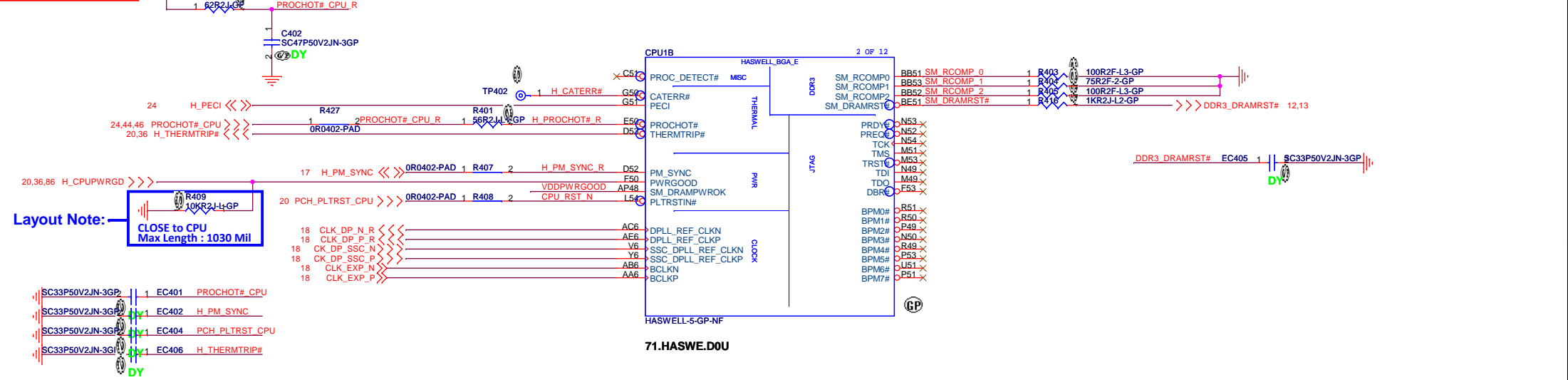
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PCIe/DMI/FDI)

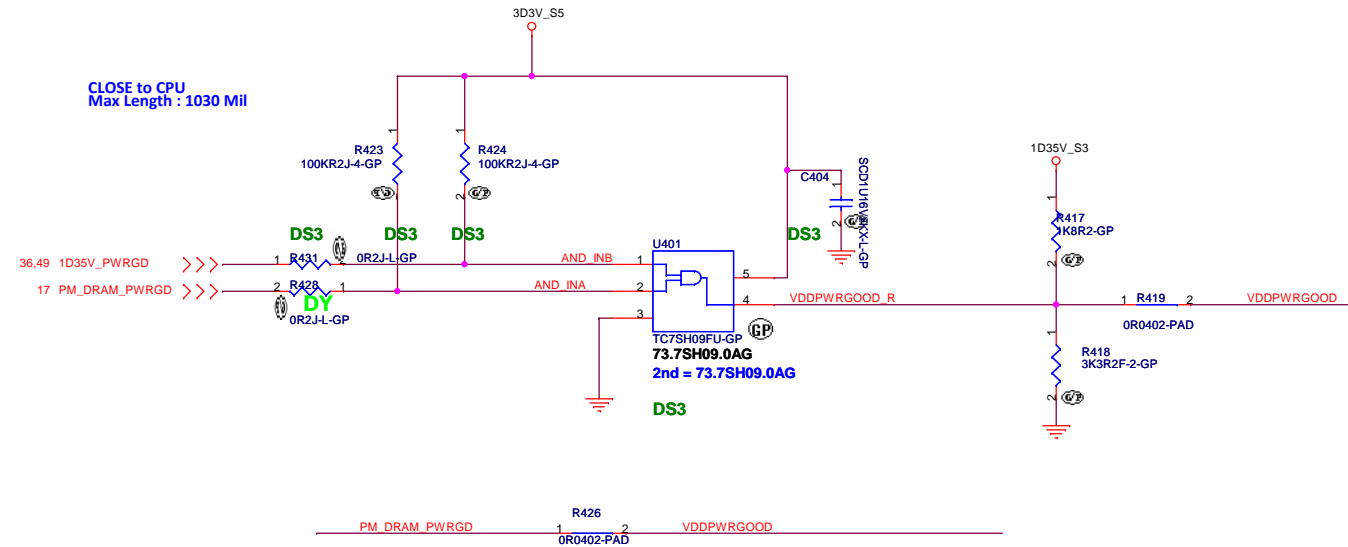
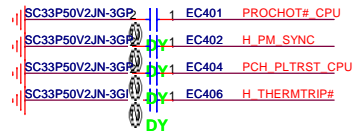
Size A3 Document Number: Poseidon 860M Rev: -1

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SSID = CPU

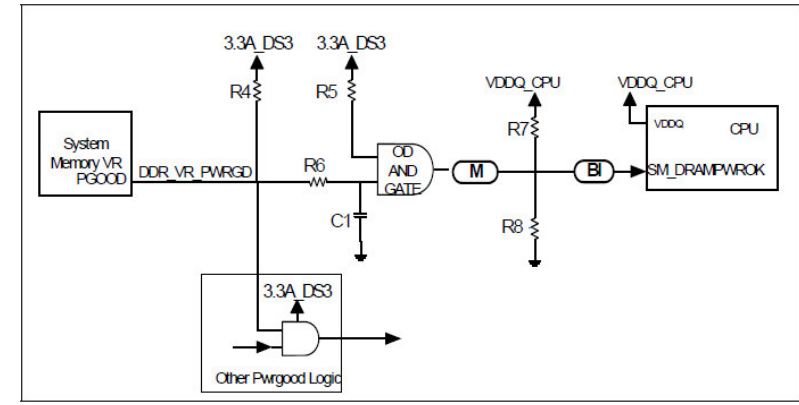


Layout Note: CLOSE to CPU Max Length : 1030 Mil



Non_DS3 S3 Power Reduction Circuit SM_DRAMPWROK

SM_DRAMPWROK Topology for platforms supporting Deep S3

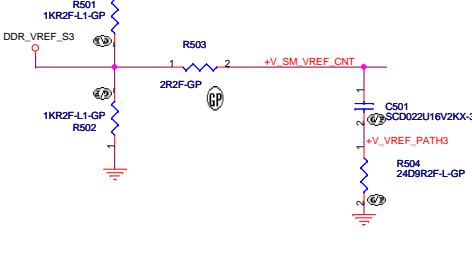
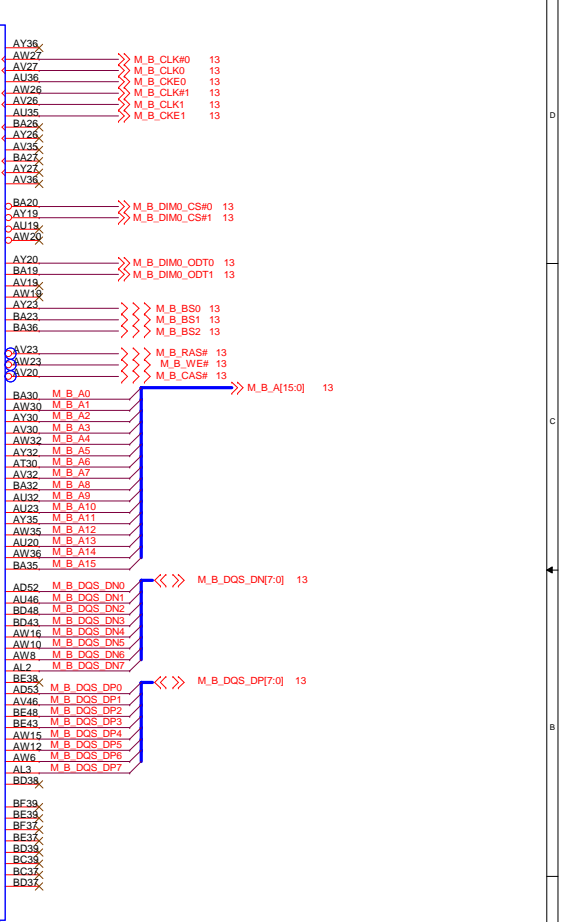
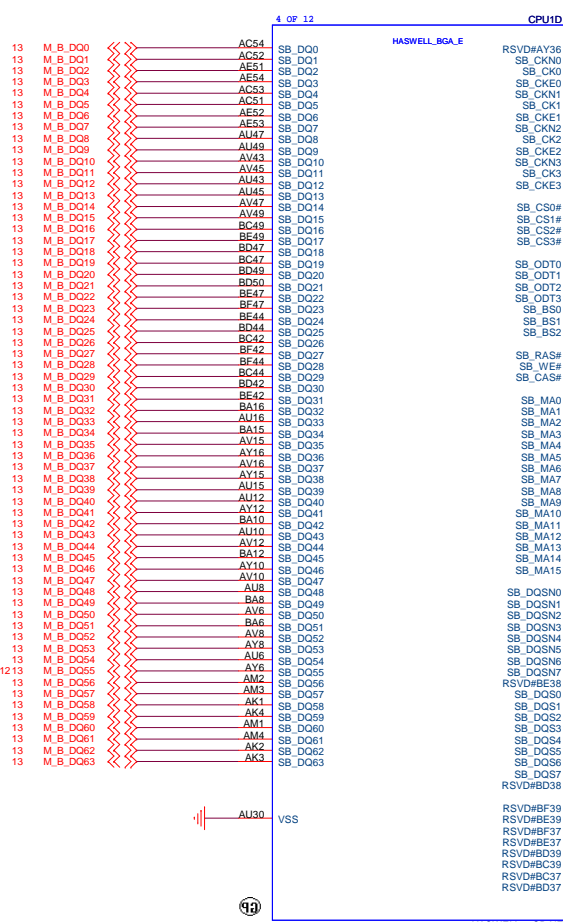
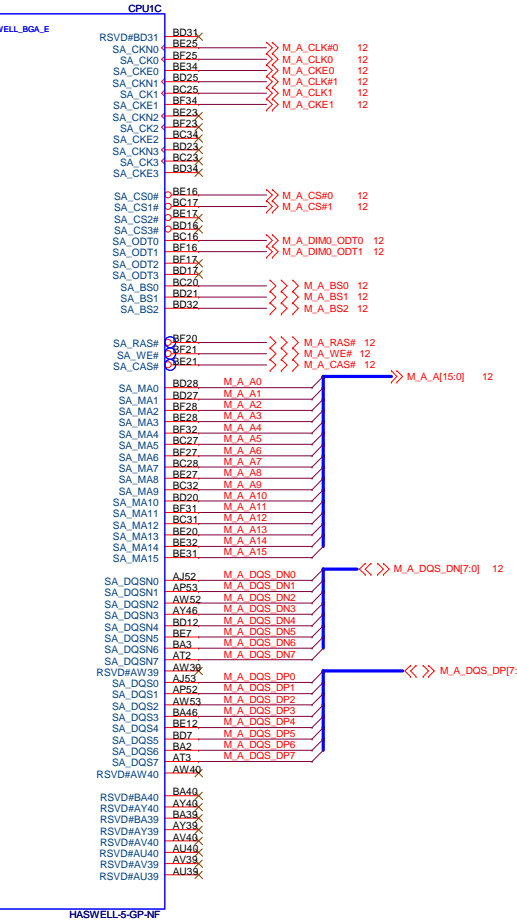
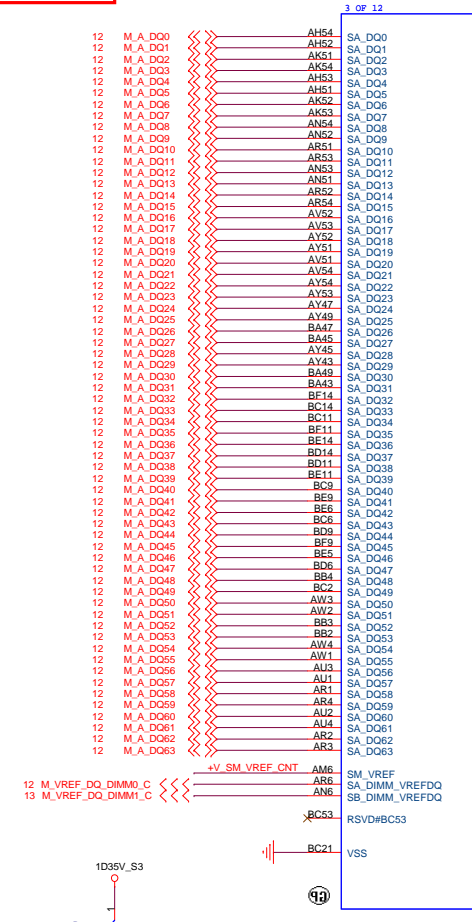


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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
CPU (THERMAL/CLOCK/PM)		
Title	Document Number	Rev
	Poseidon 860M	-1
Date: Tuesday, June 17, 2014	Sheet 4	of 102

SSID = CPU



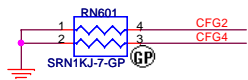
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<p style="text-align: center;">緯創資通 Wistron Corporation</p> <p style="text-align: center; font-size: small;">21F, 88, Sec.1, Hsin Ta Wu Rd., Hsichn, Taipei Hsein 221, Taiwan, R.O.C.</p>		
<p>Title</p> <p style="font-size: large; font-weight: bold;">CPU (DDR)</p>		
Size	Document Number	Rev
Custom	Poseidon 860M	-1
Date:	1/25/14, June 17, 2014	Sheet 5 of 102



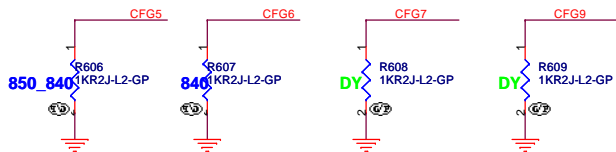
SSID = CPU

PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed

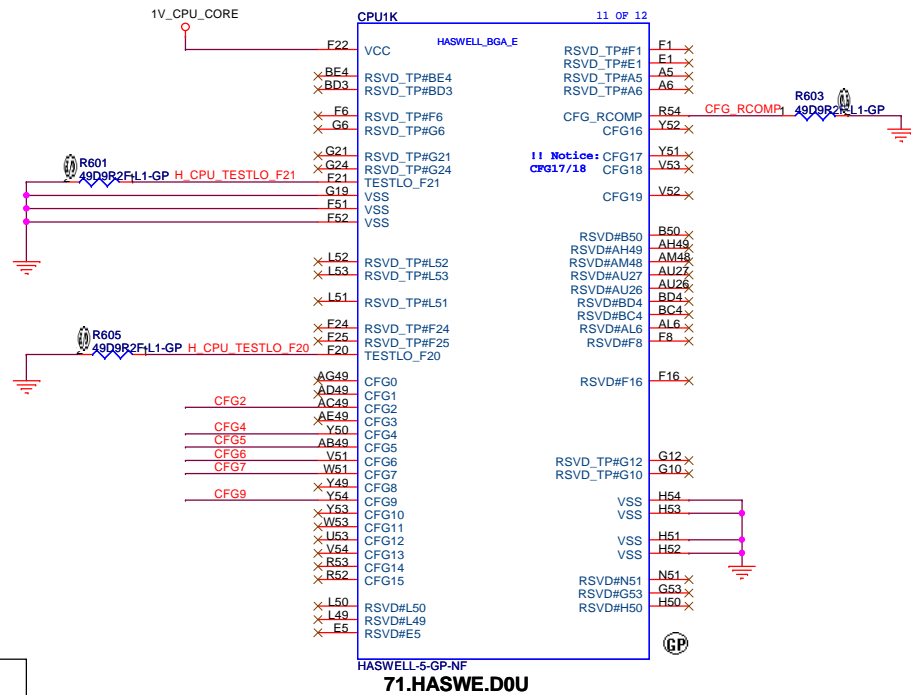


eDP Enable	
CFG4	1: Disable 0: Enable

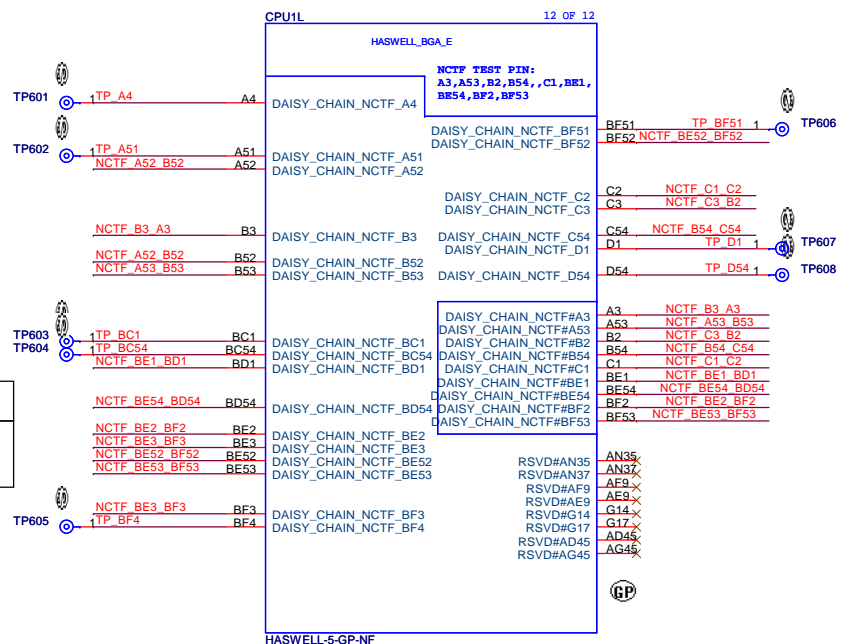
PCIe Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8, x4, x4 - Device 1 functions 1 and 2 enabled



Reserved configuration lanes. A test point may be placed on the board for these lands.	
CFG[19:7]	



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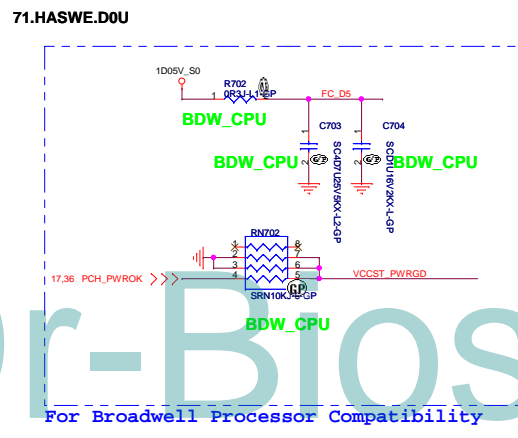
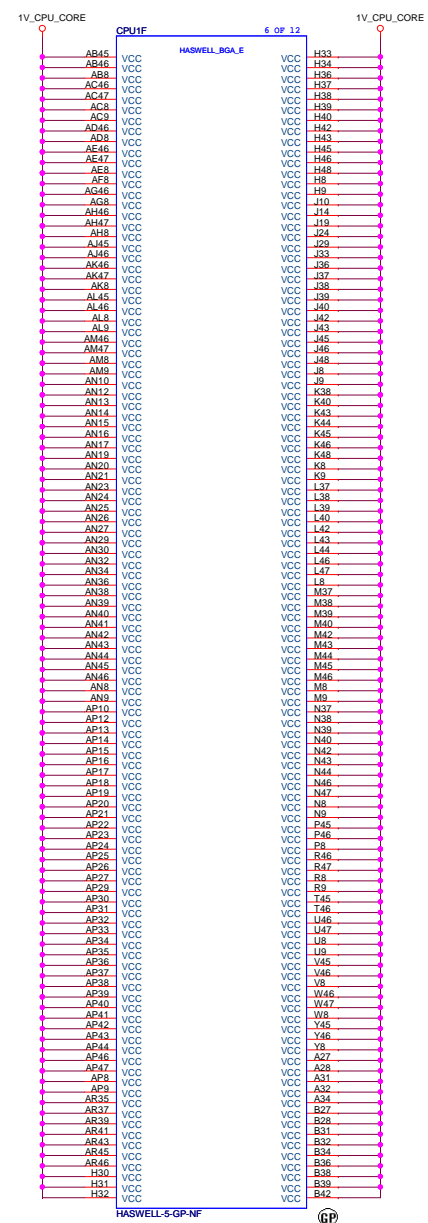
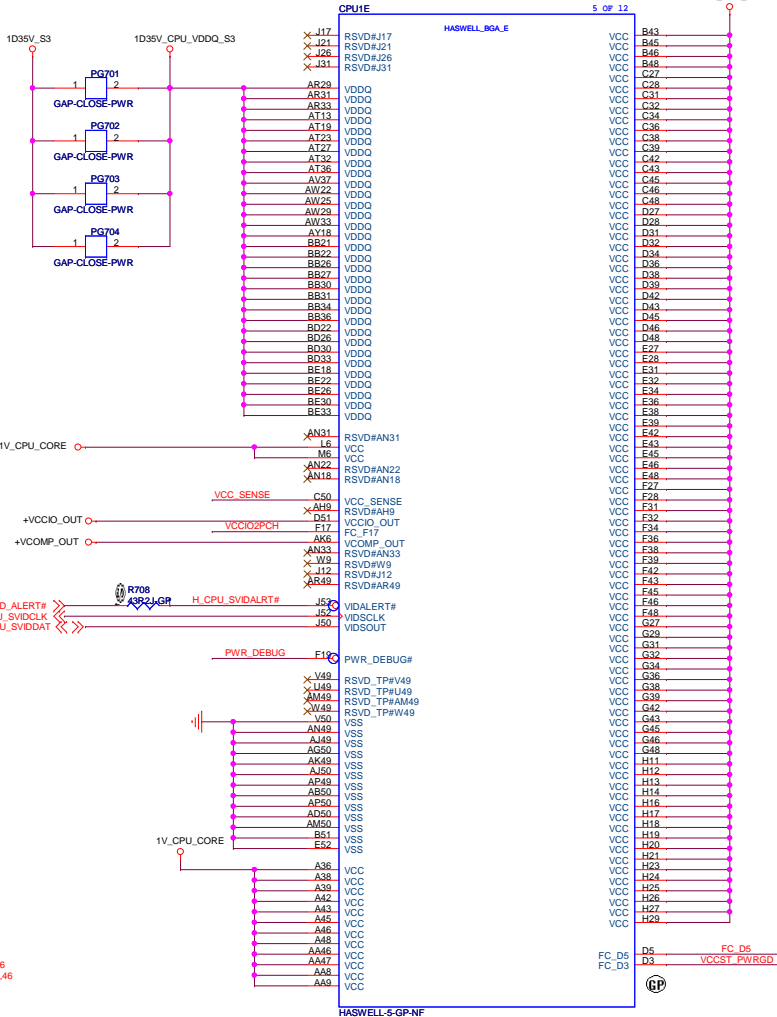
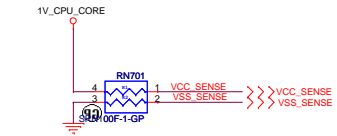
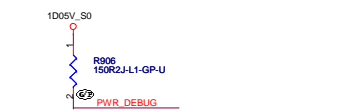
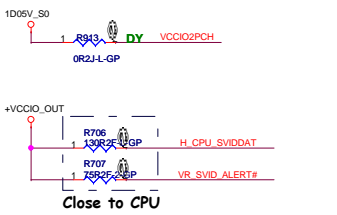
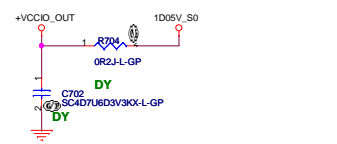
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Title: CPU (CFG)

Size Custom Document Number Poseidon 860M Rev -1

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SSID = CPU

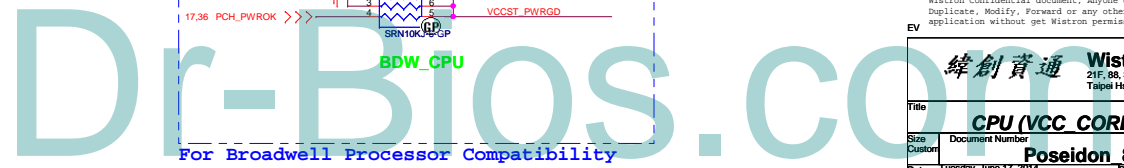


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Title CPU (VCC CORE)
Document Number Poseidon 860M
Rev -1
Date 1 Dec 2014, June 17, 2014
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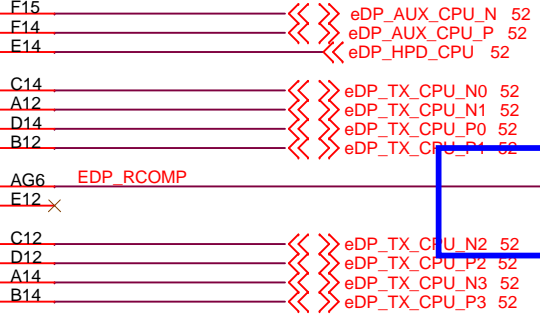
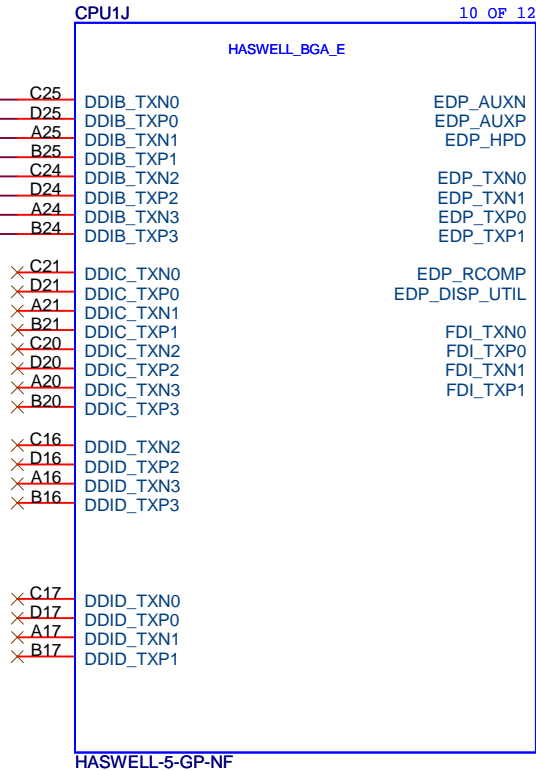


For Broadwell Processor Compatibility

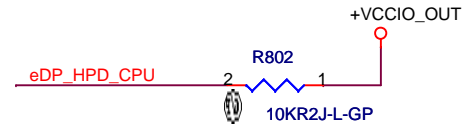
SSID = CPU

HDMI

54 HDMI_DATA_CPU_N2
 54 HDMI_DATA_CPU_P2
 54 HDMI_DATA_CPU_N1
 54 HDMI_DATA_CPU_P1
 54 HDMI_DATA_CPU_N0
 54 HDMI_DATA_CPU_P0
 54 HDMI_DATA_CPU_N3
 54 HDMI_DATA_CPU_P3



Layout Note:



HASWELL-5-GP-NF
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Title CPU (DDI/EDP)			
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CPU1G 7 OF 12

CPU1H 8 OF 12

CPU1I 9 OF 12

A11	VSS	AJ48	VSS
A15	VSS	AJ51	VSS
A19	VSS	AJ54	VSS
A22	VSS	AK48	VSS
A26	VSS	AK5	VSS
A30	VSS	AK50	VSS
A33	VSS	AK7	VSS
A37	VSS	AL1	VSS
A40	VSS	AL1	VSS
A44	VSS	AL4	VSS
AA1	VSS	AL48	VSS
AA2	VSS	AL5	VSS
AA3	VSS	AL7	VSS
AA4	VSS	AM5	VSS
AA48	VSS	AM51	VSS
AA5	VSS	AM52	VSS
AA7	VSS	AM53	VSS
AB5	VSS	AM54	VSS
AB51	VSS	AM7	VSS
AB52	VSS	AN1	VSS
AB53	VSS	AN2	VSS
AB54	VSS	AN3	VSS
AB7	VSS	AN4	VSS
AB9	VSS	AN48	VSS
AC48	VSS	AN5	VSS
AC5	VSS	AN50	VSS
AC50	VSS	AN7	VSS
AC7	VSS	AP51	VSS
AD48	VSS	AP54	VSS
AD51	VSS	AP7	VSS
AD54	VSS	AR12	VSS
AD7	VSS	AR14	VSS
AD9	VSS	AR16	VSS
AE1	VSS	AR18	VSS
AE2	VSS	AR20	VSS
AE3	VSS	AR24	VSS
AE4	VSS	AR26	VSS
AE48	VSS	AR48	VSS
AE5	VSS	AR5	VSS
AE50	VSS	AR50	VSS
AE7	VSS	AR7	VSS
AF5	VSS	AR8	VSS
AF6	VSS	AR9	VSS
AF7	VSS	AT1	VSS
AG48	VSS	AT10	VSS
AG5	VSS	AT12	VSS
AG51	VSS	AT16	VSS
AG52	VSS	AT18	VSS
AG53	VSS	AT20	VSS
AG54	VSS	AT22	VSS
AG7	VSS	AT25	VSS
AG9	VSS	AT26	VSS
AH1	VSS	AT29	VSS
AH2	VSS	AT33	VSS
AH3	VSS	AT35	VSS
AH4	VSS	AT37	VSS
AH48	VSS	AT39	VSS
AH5	VSS	AT4	VSS
AH50	VSS		
AH7	VSS		

AT40	VSS	AY50	VSS
AT42	VSS	AY9	VSS
AT43	VSS	B11	VSS
AT46	VSS	B15	VSS
AT47	VSS	B19	VSS
AT49	VSS	B22	VSS
AT5	VSS	B26	VSS
AT50	VSS	B30	VSS
AT51	VSS	B33	VSS
AT52	VSS	B37	VSS
AT53	VSS	B40	VSS
AT54	VSS	B44	VSS
AT6	VSS	B49	VSS
AT8	VSS	B67	VSS
AT9	VSS	BA13	VSS
AU13	VSS	BA18	VSS
AU18	VSS	BA22	VSS
AU22	VSS	BA25	VSS
AU25	VSS	BA29	VSS
AU29	VSS	BA33	VSS
AU33	VSS	BA37	VSS
AU37	VSS	BA4	VSS
AU42	VSS	BA42	VSS
AU5	VSS	BA5	VSS
AU9	VSS	BA50	VSS
AV1	VSS	BA51	VSS
AV13	VSS	BA52	VSS
AV18	VSS	BA53	VSS
AV2	VSS	BA9	VSS
AV22	VSS	BB10	VSS
AV25	VSS	BB11	VSS
AV29	VSS	BB12	VSS
AV3	VSS	BB14	VSS
AV33	VSS	BB15	VSS
AV37	VSS	BB16	VSS
AV4	VSS	BB17	VSS
AV42	VSS	BB18	VSS
AV5	VSS	BB20	VSS
AV50	VSS	BB23	VSS
AV9	VSS	BB25	VSS
AW13	VSS	BB28	VSS
AW18	VSS	BB32	VSS
AW37	VSS	BB33	VSS
AW43	VSS	BB37	VSS
AW48	VSS	BB38	VSS
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AW5	VSS	BB41	VSS
AW51	VSS	BB42	VSS
AW54	VSS	BB43	VSS
AW9	VSS	BB44	VSS
AY13	VSS	BB46	VSS
AY22	VSS	BB47	VSS
AY29	VSS	BB48	VSS
AY33	VSS	BB49	VSS
AY37	VSS	BB5	VSS
AY42	VSS	BB6	VSS
	VSS	BB7	VSS
	VSS	BB9	VSS

BC10	VSS	BC20	VSS
BC12	VSS	BC23	VSS
BC15	VSS	BC25	VSS
BC18	VSS	BC26	VSS
BC22	VSS	BC30	VSS
BC26	VSS	BC33	VSS
BC3	VSS	BC37	VSS
BC30	VSS	BC40	VSS
BC33	VSS	BC43	VSS
BC36	VSS	BC45	VSS
BC38	VSS	BC48	VSS
BC41	VSS	BC5	VSS
BC43	VSS	BC50	VSS
BC45	VSS	BC53	VSS
BC48	VSS	BC55	VSS
BC5	VSS	BC57	VSS
BC50	VSS	BD10	VSS
BC53	VSS	BD15	VSS
BC55	VSS	BD18	VSS
BD10	VSS	BD36	VSS
BD15	VSS	BD41	VSS
BD18	VSS	BD46	VSS
BD36	VSS	BD5	VSS
BD41	VSS	BE10	VSS
BD46	VSS	BE15	VSS
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BF38	VSS	BF46	VSS
BF41	VSS	BF48	VSS
BF44	VSS	BF7	VSS
BF46	VSS	C11	VSS
BF48	VSS	C15	VSS
BF7	VSS	C19	VSS
C11	VSS	C22	VSS
C15	VSS	C26	VSS
C19	VSS	C30	VSS
C22	VSS	C33	VSS
C26	VSS	C37	VSS
C30	VSS	C4	VSS
C33	VSS	C40	VSS
C37	VSS	C44	VSS
C4	VSS	C49	VSS
C40	VSS	C52	VSS
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C5	VSS	D19	VSS
D11	VSS	D22	VSS
D15	VSS	D26	VSS
D19	VSS	D30	VSS
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E17	VSS	E21	VSS
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E20	VSS	E24	VSS
E21	VSS	E25	VSS
E22	VSS	E26	VSS
E24	VSS	E30	VSS
E25	VSS	E33	VSS
E26	VSS	E37	VSS
E30	VSS	E40	VSS
E33	VSS	E44	VSS
E37	VSS	E49	VSS
E40	VSS	E51	VSS
E44	VSS	E53	VSS
E49	VSS	F8	VSS
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E53	VSS	F26	VSS
F8	VSS	F3	VSS
F21	VSS	F30	VSS
F26	VSS	F33	VSS
F3	VSS	F37	VSS
F30	VSS	F4	VSS
F33	VSS	F40	VSS
F37	VSS	F44	VSS
F4	VSS	F48	VSS
F40	VSS	F5	VSS
F44	VSS	G11	VSS
F48	VSS	G13	VSS
F5	VSS	G16	VSS

G20	VSS
G23	VSS
G25	VSS
G26	VSS
G30	VSS
G33	VSS
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G40	VSS
G44	VSS
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G7	VSS
G9	VSS
G9	VSS
H44	VSS
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H7	VSS
H4	VSS
H49	VSS
J51	VSS
J54	VSS
J7	VSS
K1	VSS
K2	VSS
K3	VSS
K4	VSS
K5	VSS
K6	VSS
K7	VSS
L48	VSS
L7	VSS
L9	VSS
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M50	VSS
M52	VSS
M54	VSS
M7	VSS
N48	VSS
N7	VSS
P1	VSS
P2	VSS
P3	VSS
P4	VSS
P48	VSS
P5	VSS
P50	VSS
P52	VSS
P54	VSS
P6	VSS
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R48	VSS
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Y7	VSS
Y9	VSS
AR22	VSS
AB48	VSS
P9	VSS
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BA54	VSS
BB1	VSS
BB54	VSS
BD2	VSS
BD53	VSS
BF49	VSS
BF5	VSS
BF50	VSS
BF6	VSS
C53	VSS
D2	VSS
E54	VSS
F54	VSS
G1	VSS
D50	VSS

HASWELL-5-GP-NF
71.HASWE.D0U

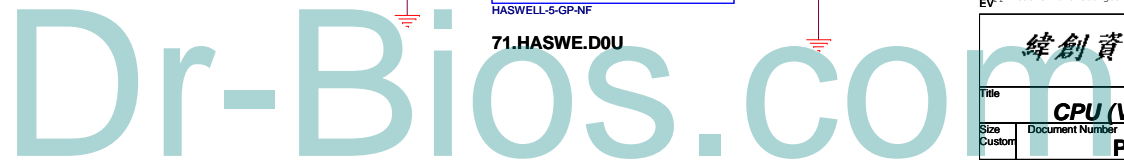
HASWELL-5-GP-NF
71.HASWE.D0U

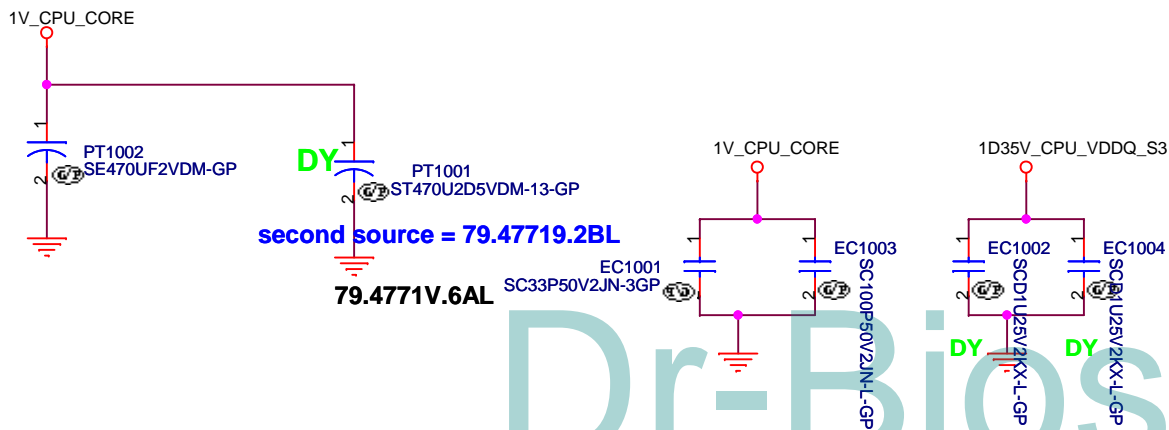
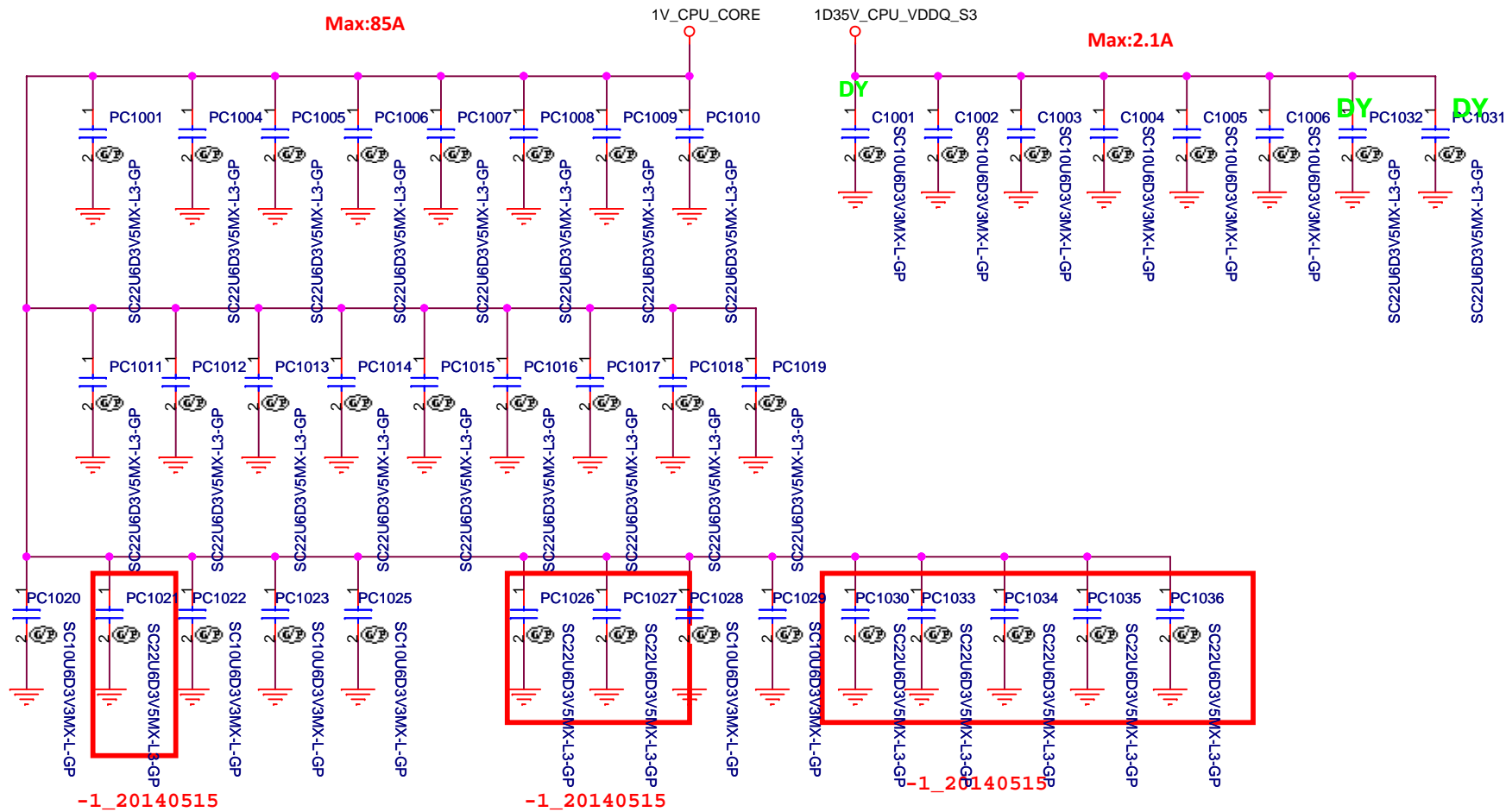
HASWELL-5-GP-NF
71.HASWE.D0U

VSS_SENSE D50 >>> VSS_SENSE 7,46

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緯創資通		
Wistron Corporation		
21F, 88, Sec.1, Hsien Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.		
Title	CPU (VSS)	
Size	Document Number	Rev
Custom	Poseidon 860M	-1
Date:	Wednesday, June 17, 2014	Sheet 9 of 102





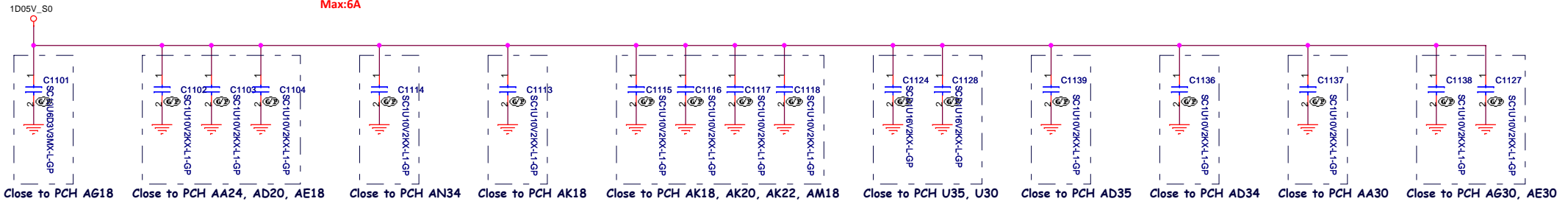
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EV

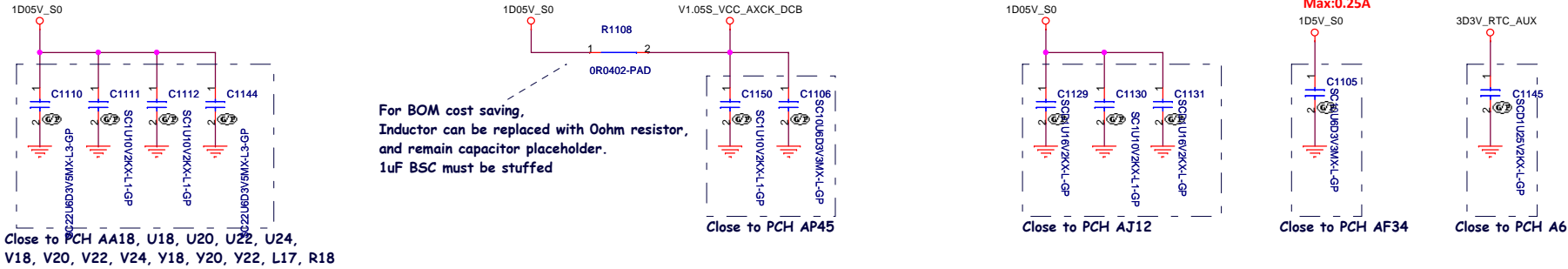
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
CPU (Power CAP1)			
Size	Document Number		Rev
A4	Poseidon 860M		-1
Date:	Tuesday, June 17, 2014	Sheet 10	of 102

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Max:6A

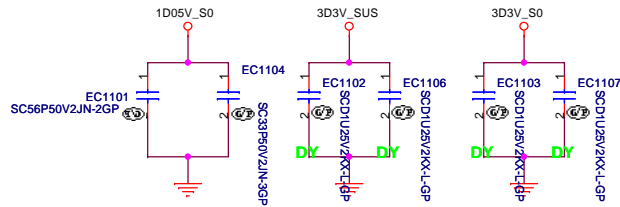
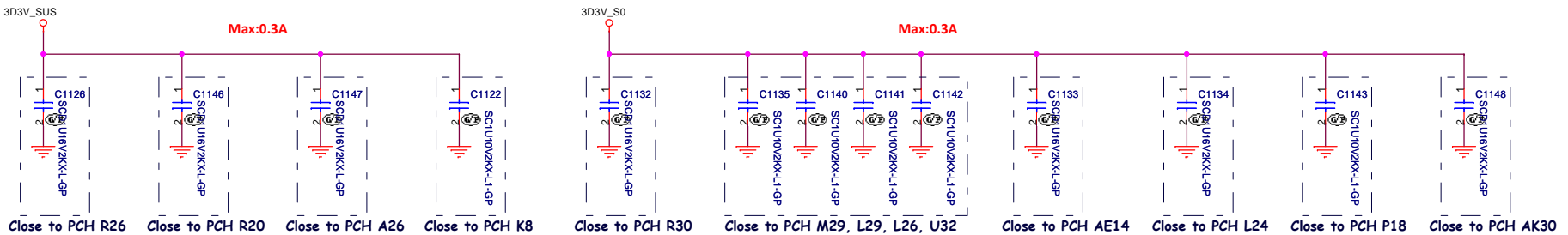


For BOM cost saving,
Inductor can be replaced with Ohm resistor,
and remain capacitor placeholder.
1uF BSC must be stuffed



Max:0.3A

Max:0.3A

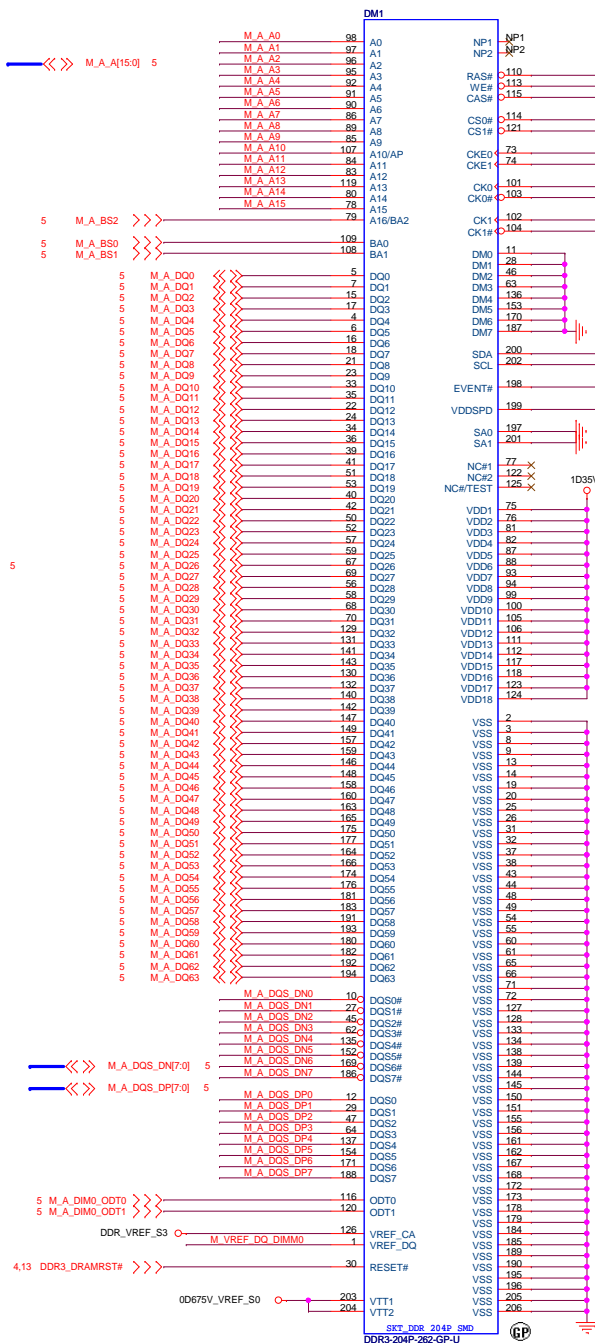
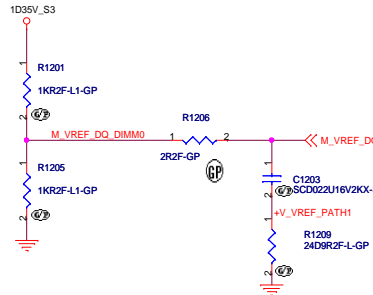
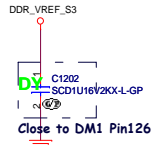


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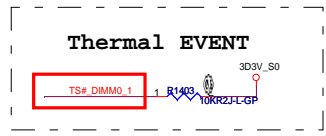
Title		Wistron Corporation	
Size		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Date		Tuesday, June 17, 2014	
Document Number		CPU (Power CAP2)	
Poseidon 860M		Rev -1	
Sheet 11		of 102	

SSID = MEMORY

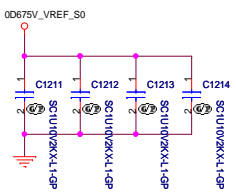
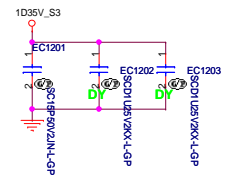


Note:
 If SA0_DIM0 = 0, SA1_DIM0 = 0
 SO-DIMMA SPD Address is 0x30
 SO-DIMMA TS Address is 0x30

 If SA0_DIM0 = 1, SA1_DIM0 = 0
 SO-DIMMA SPD Address is 0xA2
 SO-DIMMA TS Address is 0x32



Layout Note:
 Place these Caps near SO-DIMMA.
 SODIMM A DECOUPLING



Place these caps close to VTT1 and VTT2.

62.10024.S21
 2nd = 62.10024.M31
 3rd = 62.10024.Q61



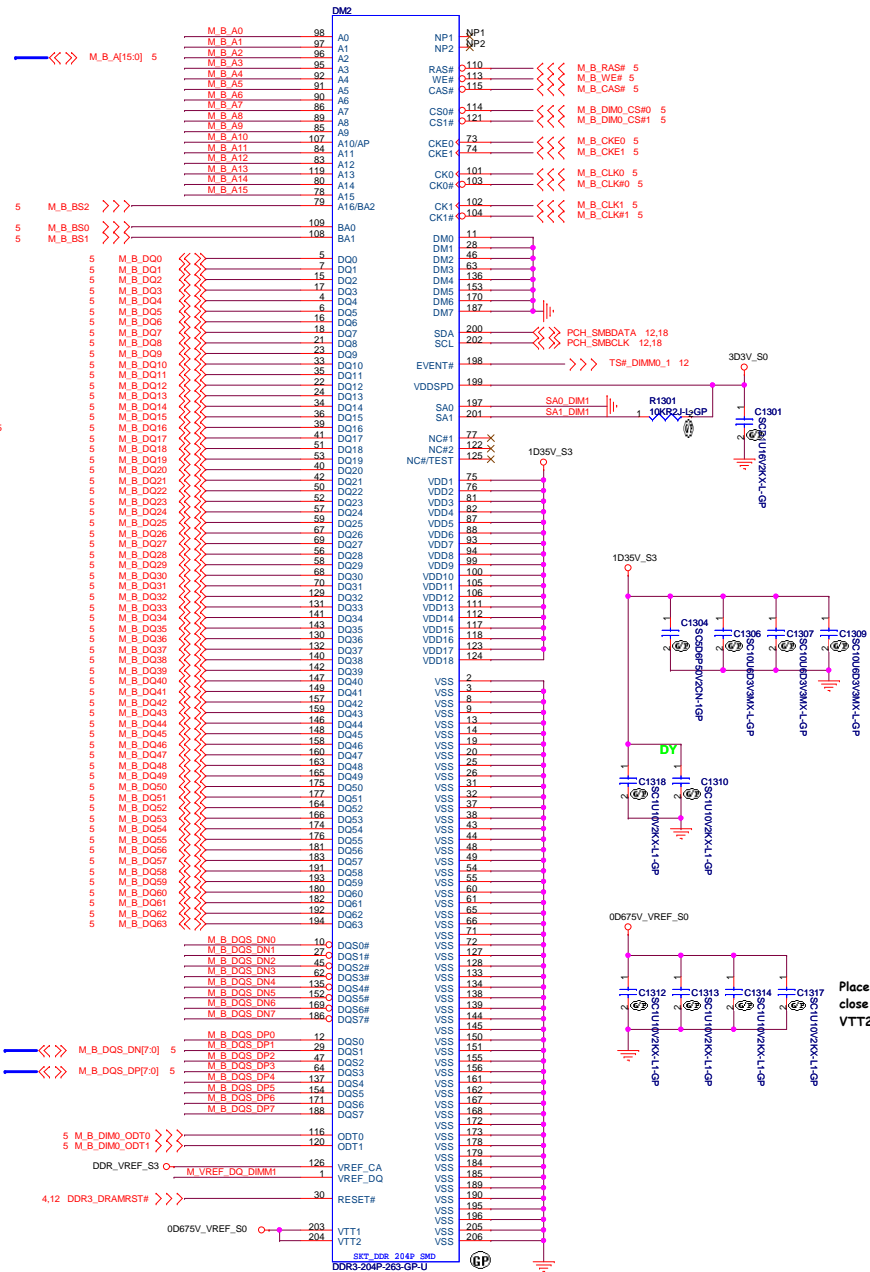
EV

緯創資通 Wistron Corporation
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Title: **DDR3-SODIMM1**

Size: Document Number
 Custom: **Poseidon 860M**

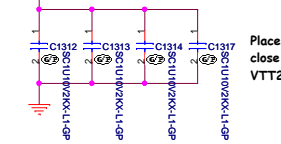
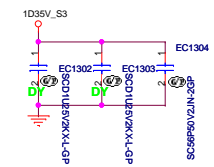
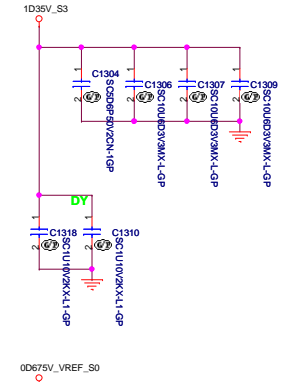
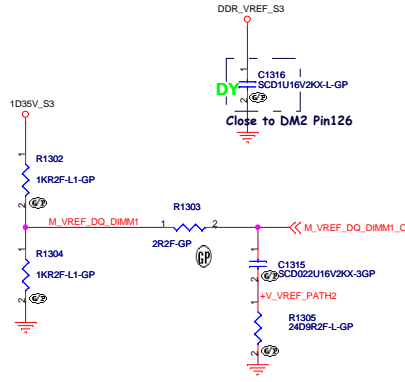
Date: Tuesday, June 17, 2014 Sheet 12 of 102 Rev -1



Note:
SO-DIMM SPD Address is 0xA4
SO-DIMM TS Address is 0x34

SO-DIMM B is placed farther from the Processor than SO-DIMM A

Layout Note:
Place these Caps near SO-DIMM B
SODIMM B DECOUPLING



Place these caps close to VTT1 and VTT2.

62.10024.S61
2nd = 62.10024.M51
3rd = 62.10024.Q71



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Title DDR3-SODIMM2		
Size Custom	Document Number Poseidon 860M	Rev -1
Date: Tuesday, June 17, 2014	Sheet 13	of 102

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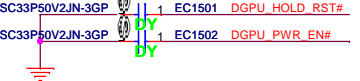
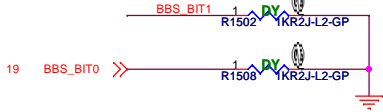
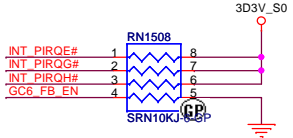
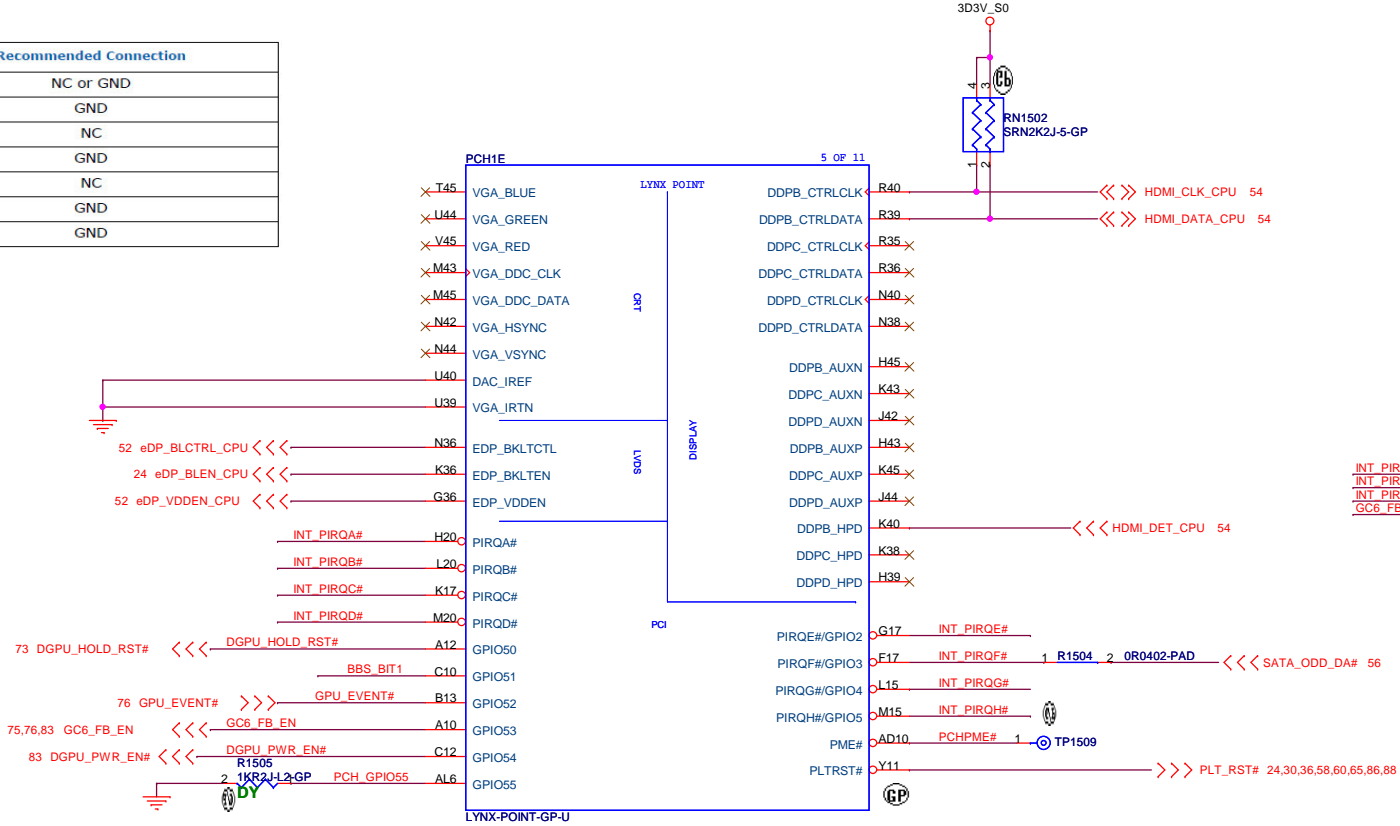
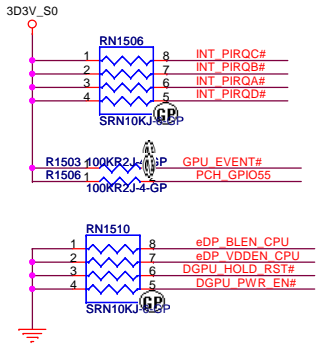
Title		
(Reserved) SODIMM_SODIMM4		
Size	Document Number	Rev
A4	Poseidon 860M	-1
Date:	Tuesday, June 17, 2014	Sheet 14 of 102

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SSID = CPU

VGA DAC Disable Recommendations

Signal Name	Recommended Connection
VGA_RED, VGA_GREEN, VGA_BLUE	NC or GND
VGA_IRTN	GND
VGA_HSYNC, VGA_VSYNC	NC
DAC_IREF	GND
DDC_CLK, DDC_DATA	NC
VCCADAC	GND
VCCADACBG	GND



BOOT BIOS Strap		
GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

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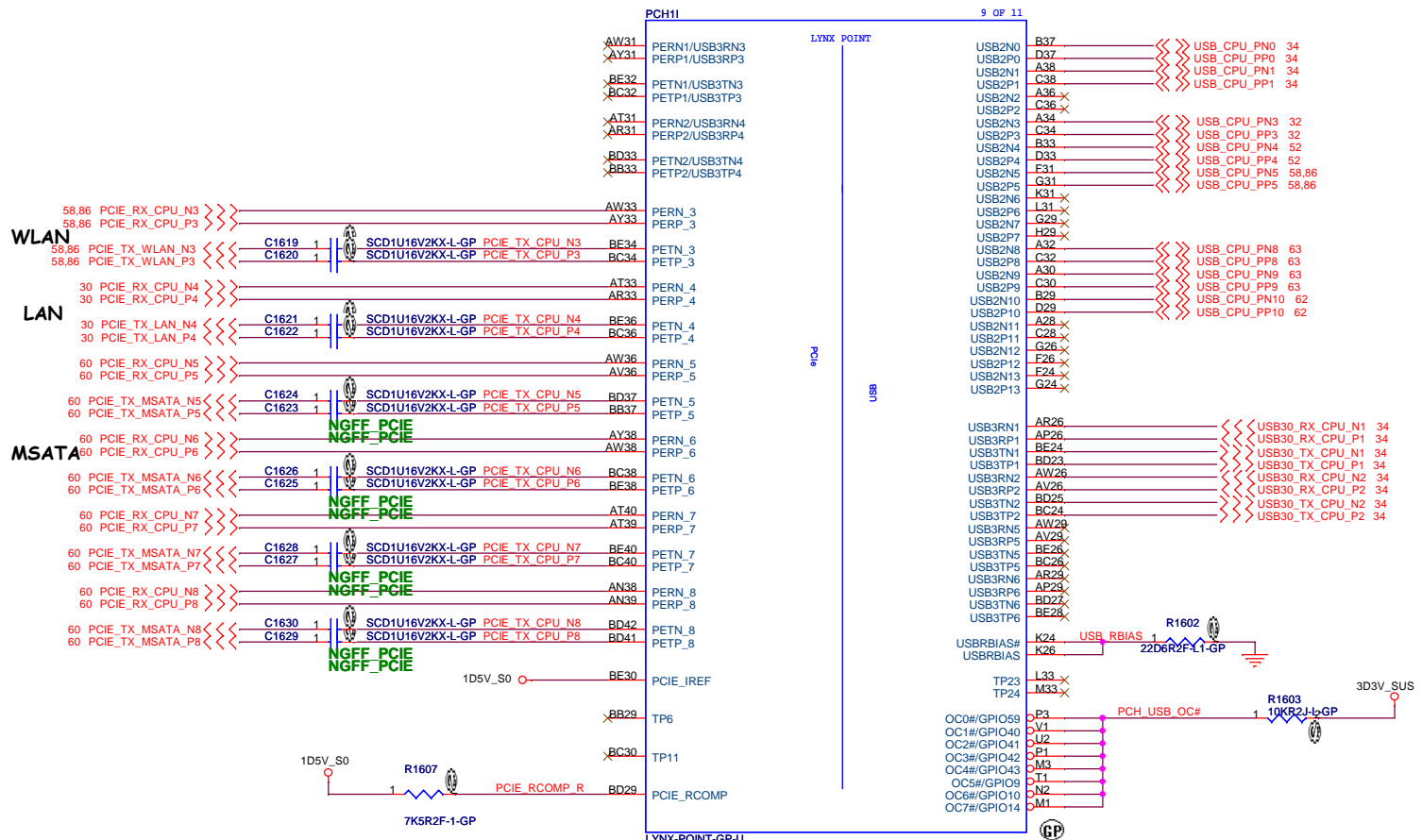
Title: **CPU(EDP SIDE BAND/GPIO/DDI)**

Size: A3 Document Number: **Poseidon 860M** Rev: **-1**

Date: Tuesday, June 17, 2014 Sheet: 15 of 102

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SSID = PCH



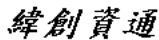
USB Table

Pair	Device
0	USB3.0(port0)
1	USB3.0(port1)
2	
3	Card Reader
4	CCD
5	Mini Card1 (WLAN)
6	TOUCH PANEL
7	
8	USB2.0
9	USB2.0
10	TOUCH PAD
11	
12	
13	

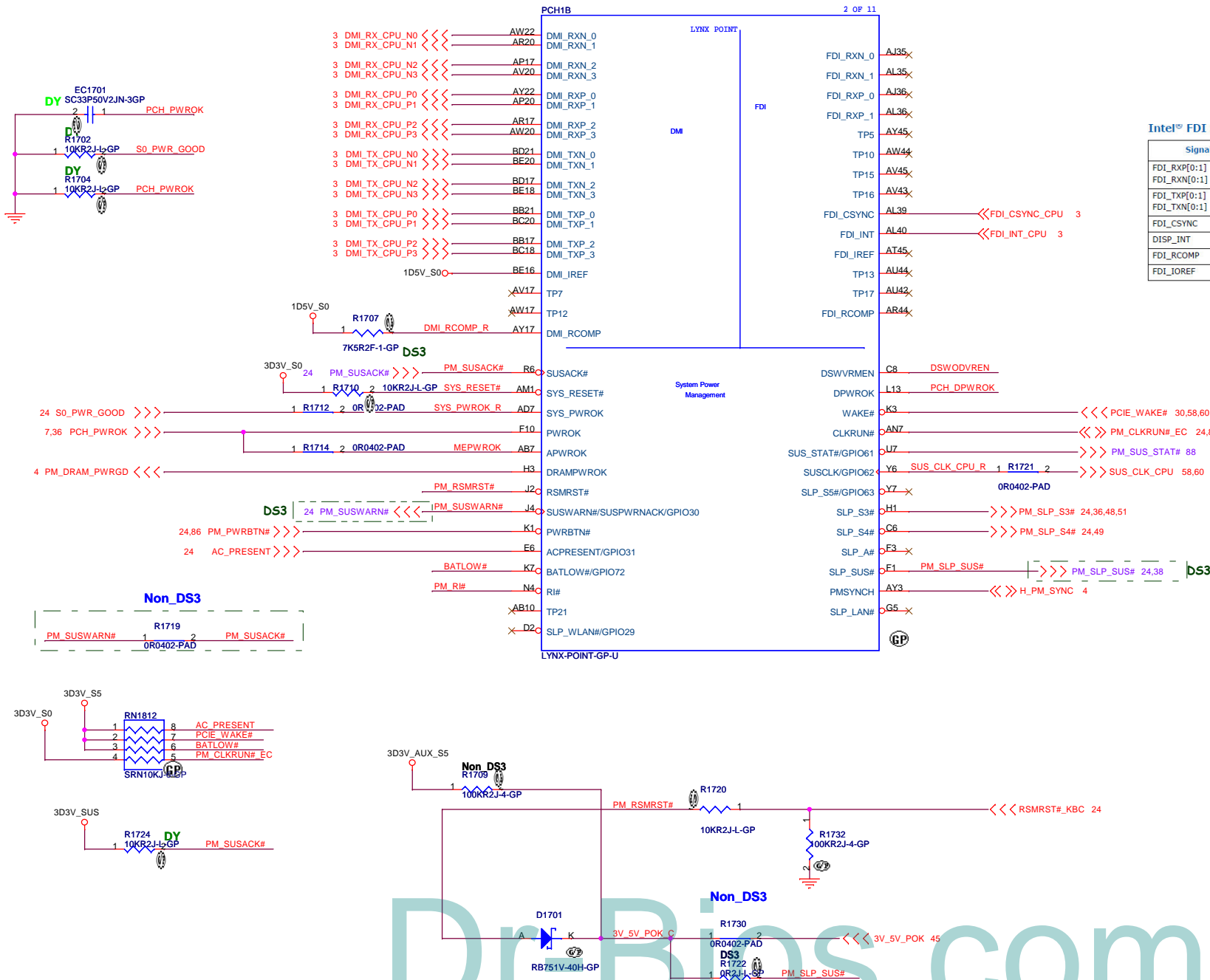
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CPU (PCI/USB)	
Poseidon 860M	
Title Size Custom Date: Tuesday, June 17, 2014	Document Number Sheet 16 of 102
	Rev -1

SSID = PCH

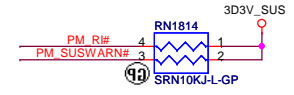
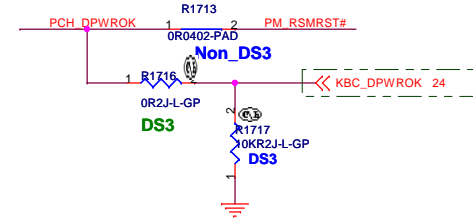


DSWODVREN - On Die DSW VR Enable

HIGH	Enabled (DEFAULT)
LOW	Disabled

Intel® FDI Signal Disabling and Termination Guidelines

Signal	Description	Disable Guidelines
FDI_RXP[0:1] FDI_RXN[0:1]	Intel FDI Receive Differential Pair on PCH	Float
FDI_TXP[0:1] FDI_TXN[0:1]	Intel FDI Transmit Differential Pair on Processor	Float
FDI_CS_SYNC	Intel FDI Composite Sync	Connect to Processor and PCH
DISP_INT	Intel FDI Hot Plug Interrupt	Connect to Processor and PCH
FDI_RCOMP	FDI Resistor Compensation	Float
FDI_IOREF	FDI Reference Voltage	Float



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EW

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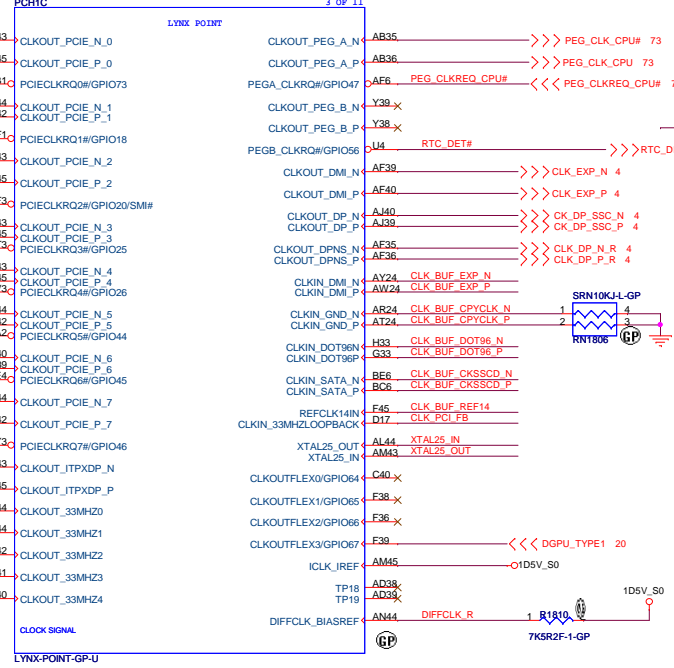
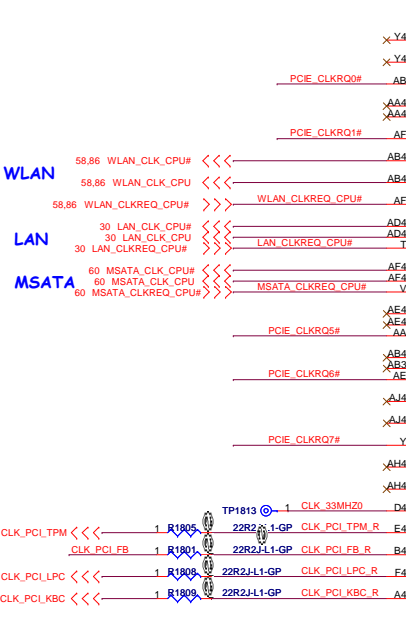
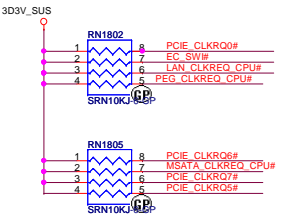
Title: CPU (DMI/FDI/PM)

Size A3 Document Number: Poseidon 860M Rev -1

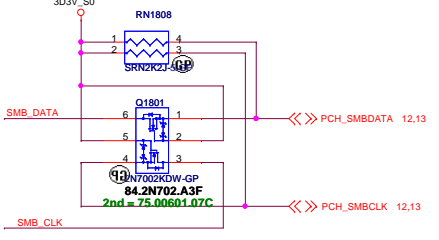
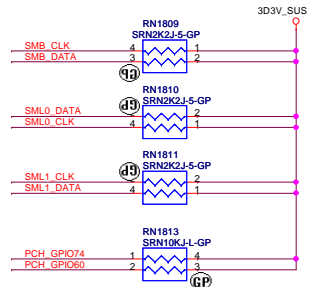
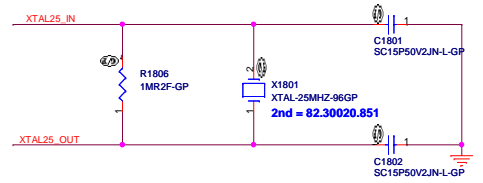
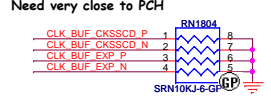
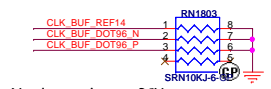
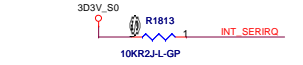
Date: Tuesday, June 17, 2014 Sheet 17 of 102

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SSID = PCH



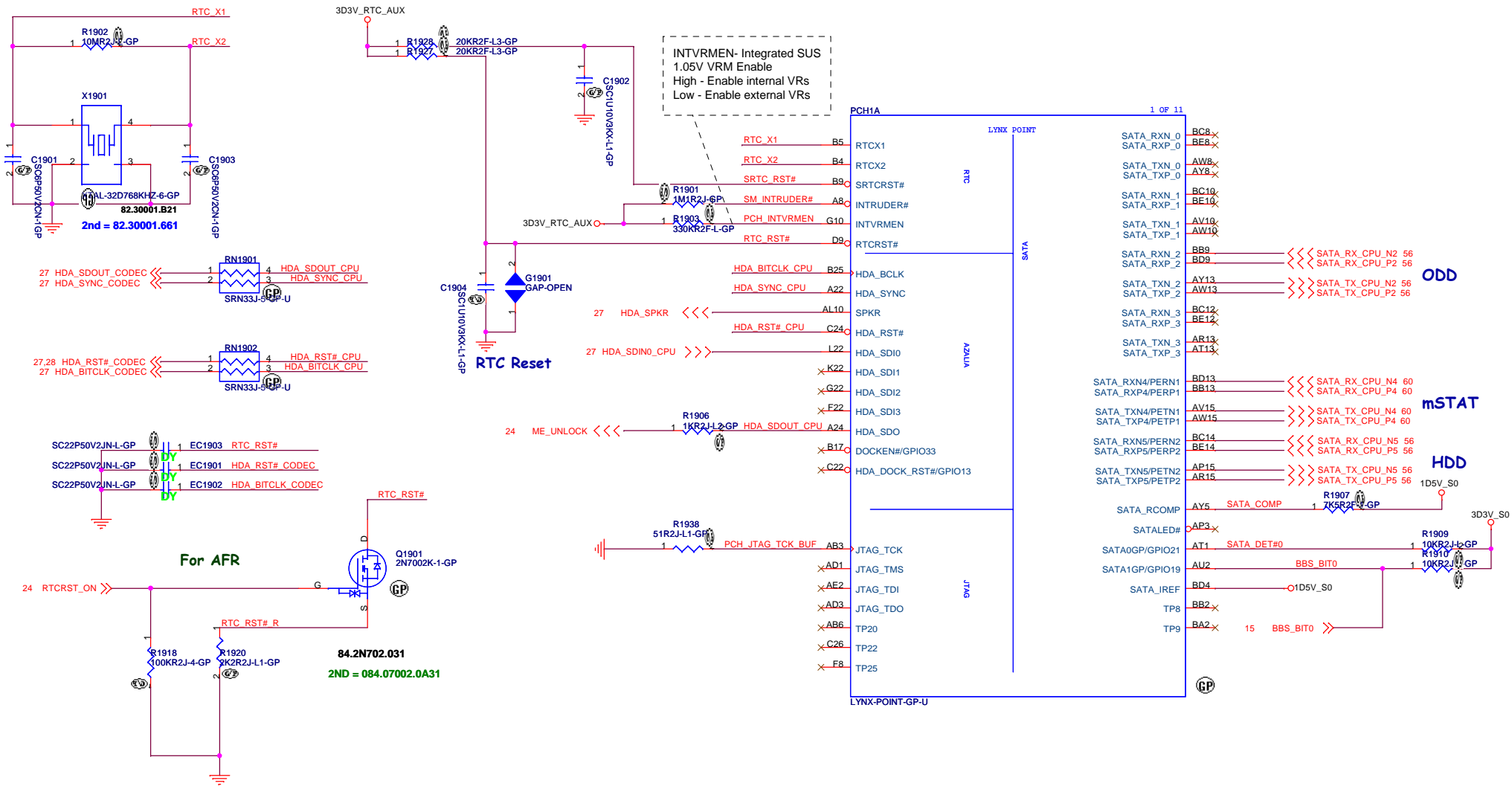
PCIECLKRQ1# and PCIECLKRQ2#
Support SO power only



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<p>緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Heichih, Taipei Hsien 221, Taiwan, R.O.C.</p>	
<p>CPU (PCI-E/SMBus/CLOCK/CL)</p>	
<p>Title</p>	<p>Document Number</p>
<p>Size</p>	<p>Rev</p>
<p>Custom</p>	<p>Poseidon 860M</p>
<p>Date: Tuesday, June 17, 2014</p>	<p>Sheet 18 of 102</p>

SSID = PCH



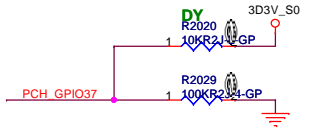
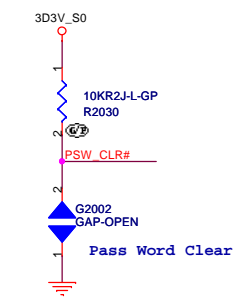
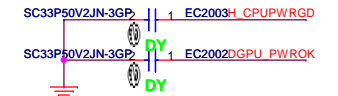
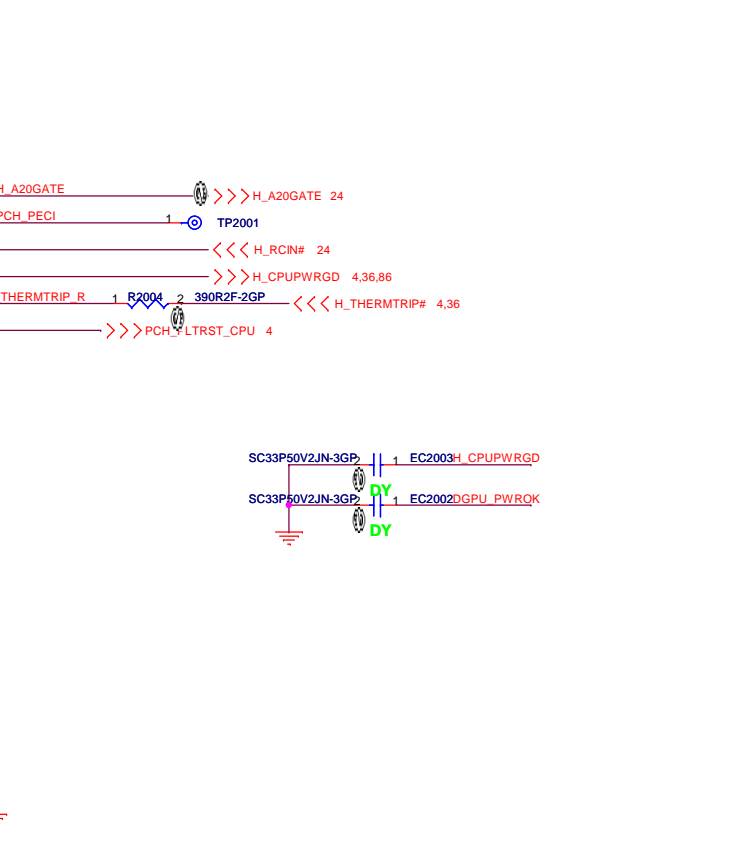
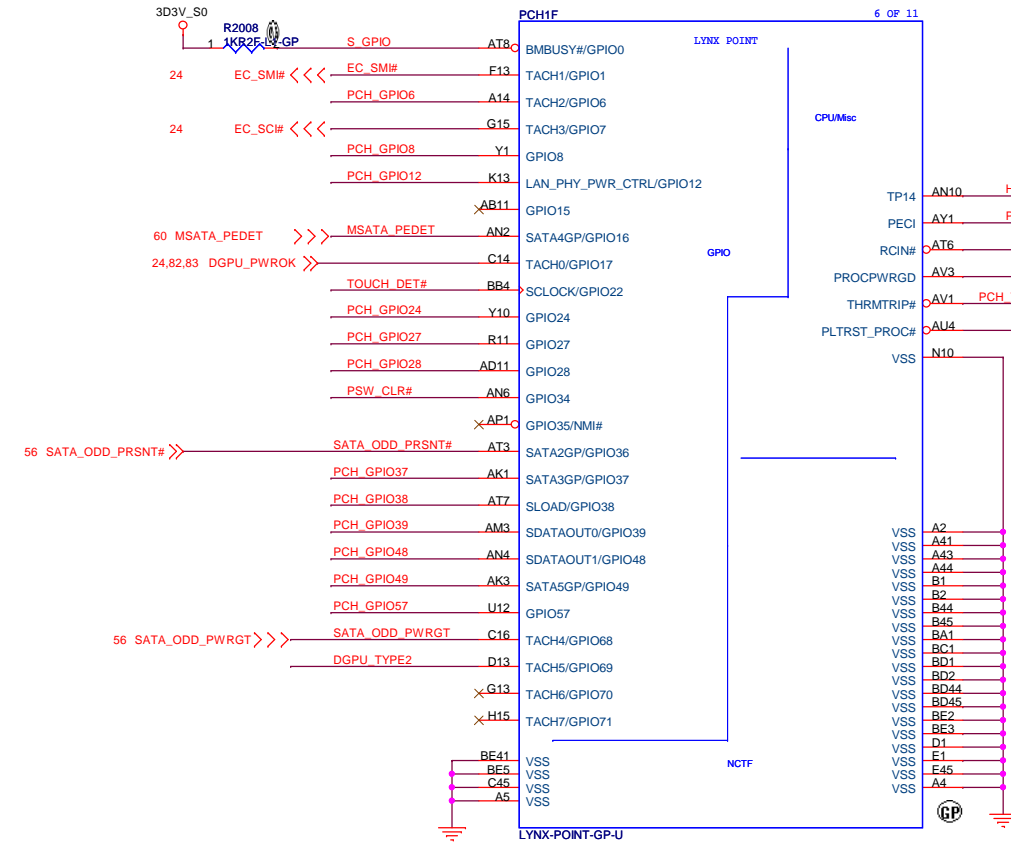
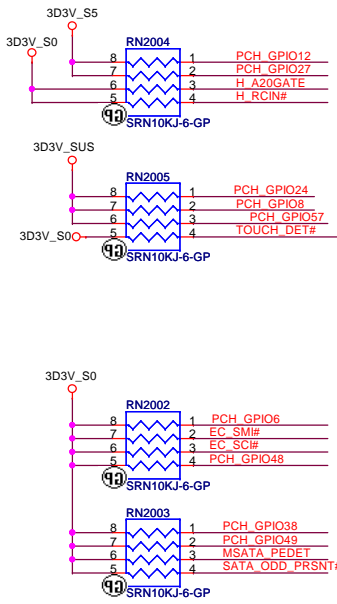
HDA_SYNC: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.

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<p>Title: CPU (RTC/LPC/SATA/HDA)</p>	
Size	Document Number
Custom	Poseidon 860M
Date: Tuesday, June 17, 2014	Sheet 19 of 102
Rev	-1

SSID = PCH



TLS Confidentiality

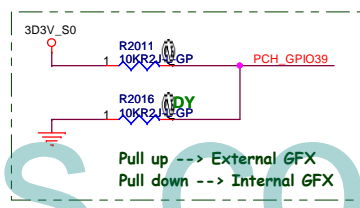
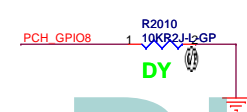
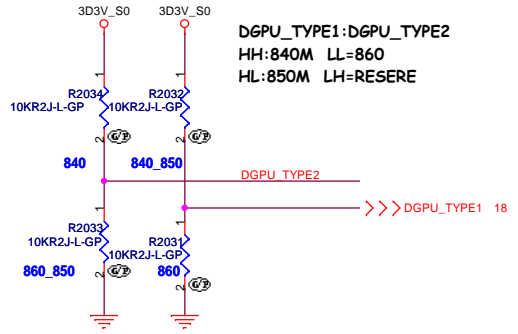
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality)

1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality)



PLL ON DIE VR ENABLE

ENABLED -- HIGH (R2013 UNSTUFFED) DEFAULT
DISABLED -- LOW (R2013 STUFFED)



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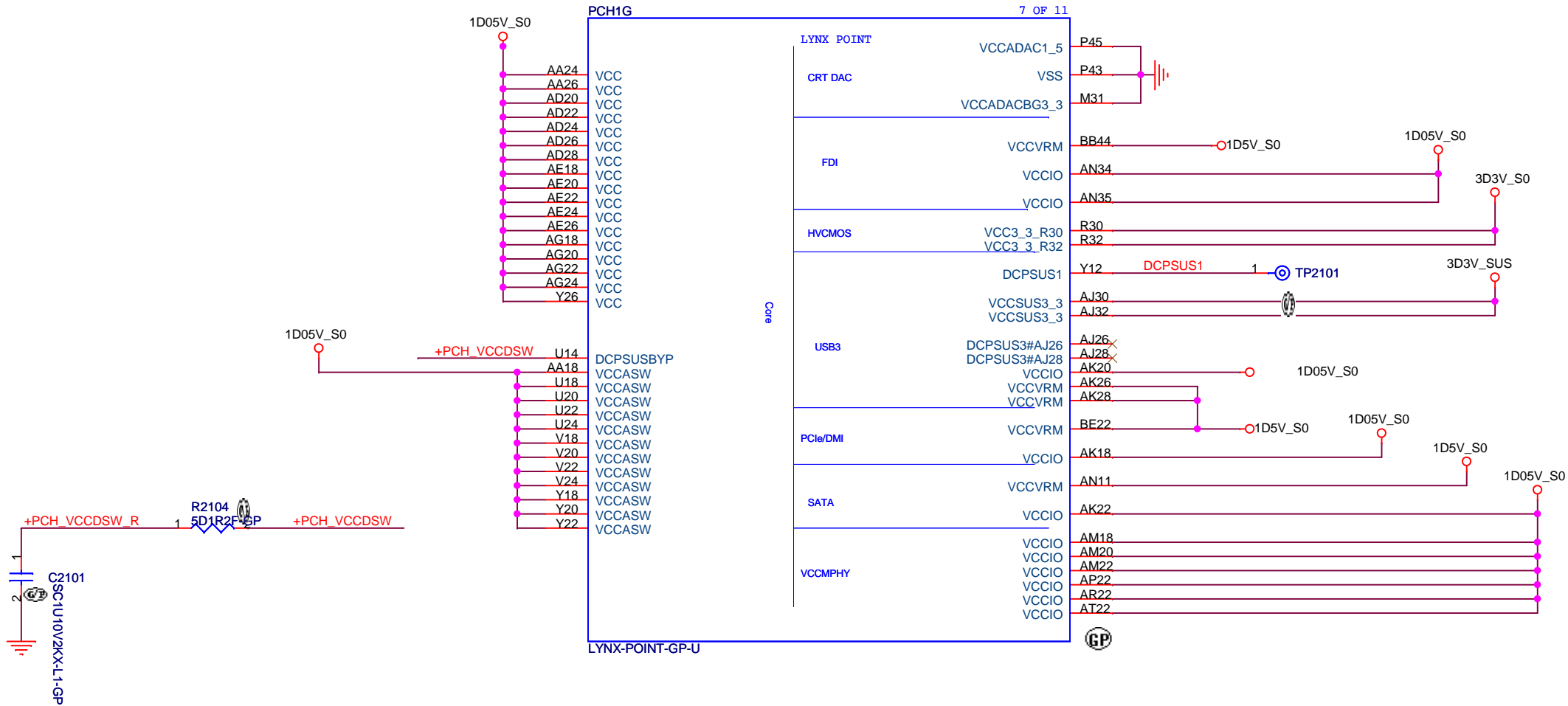
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsein 221, Taiwan, R.O.C.

Title: **CPU (GPIO/MISC)**

Size A3 Document Number: **Poseidon 860M** Rev: **-1**

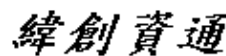
Date: Tuesday, June 17, 2014 Sheet 20 of 102

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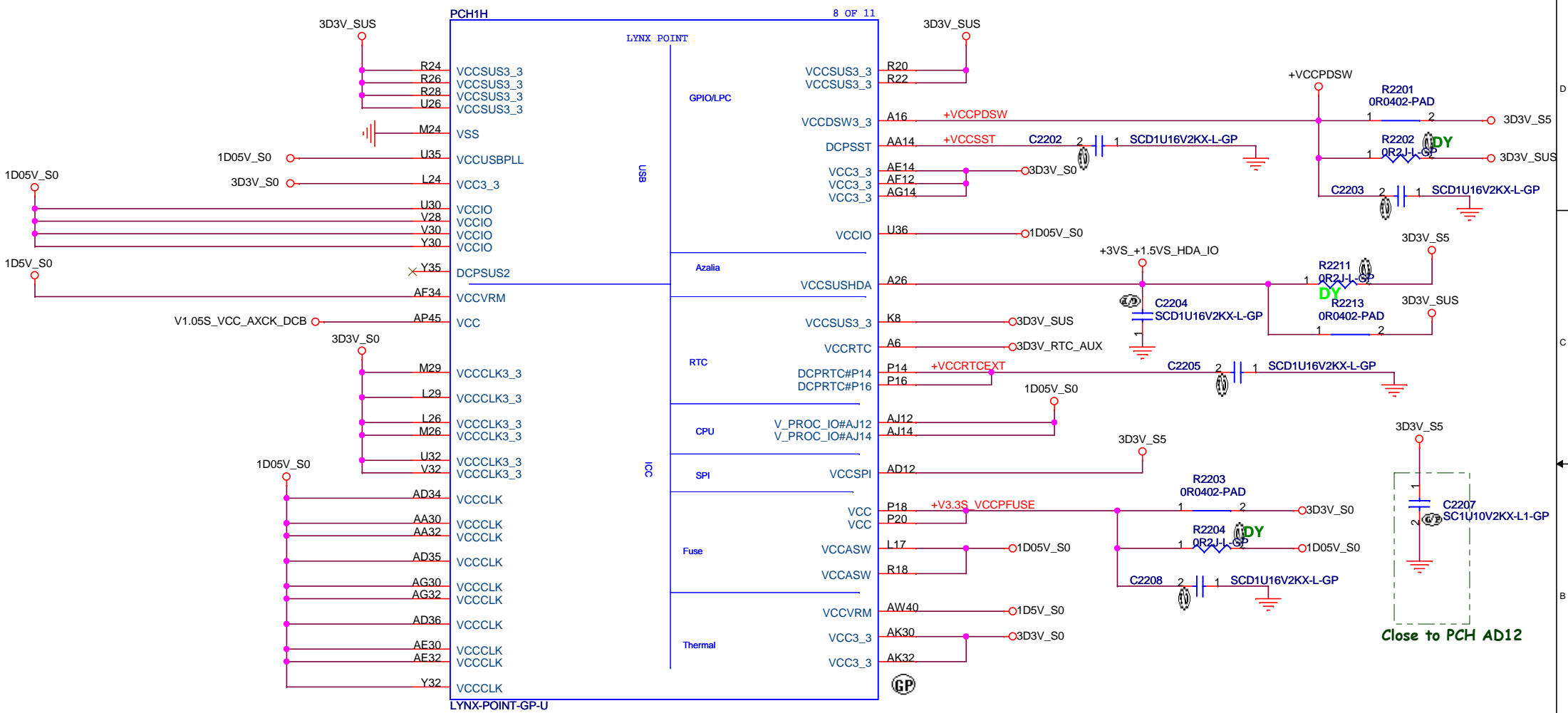


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EV

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Title	
CPU (POWER1)	
Size	Document Number
A4	Poseidon 860M
Date:	Rev
Tuesday, June 17, 2014	-1
Sheet 21 of 102	

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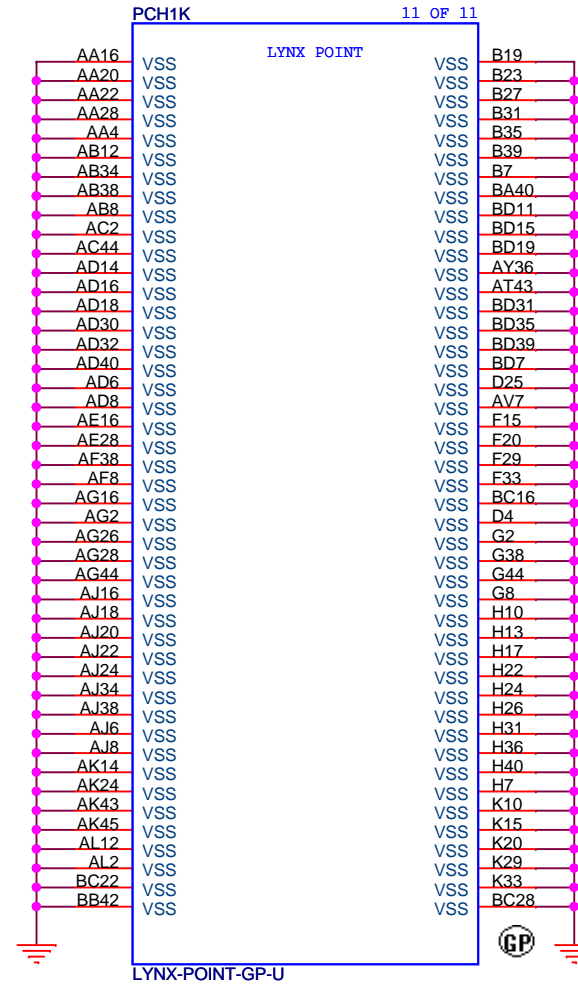
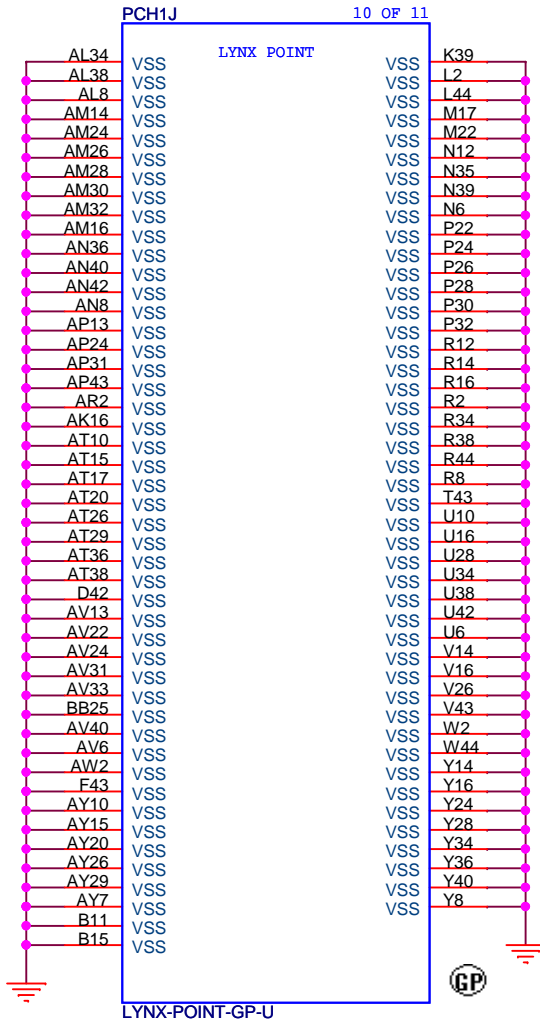
緯創資通 **Wistron Corporation**
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (RSVD)**

Size Custom	Document Number	Rev
	Poseidon 860M	-1
Date: Tuesday, June 17, 2014	Sheet 22 of 102	

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SSID = PCH



EV

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU (VSS)

Size

Document Number

Rev

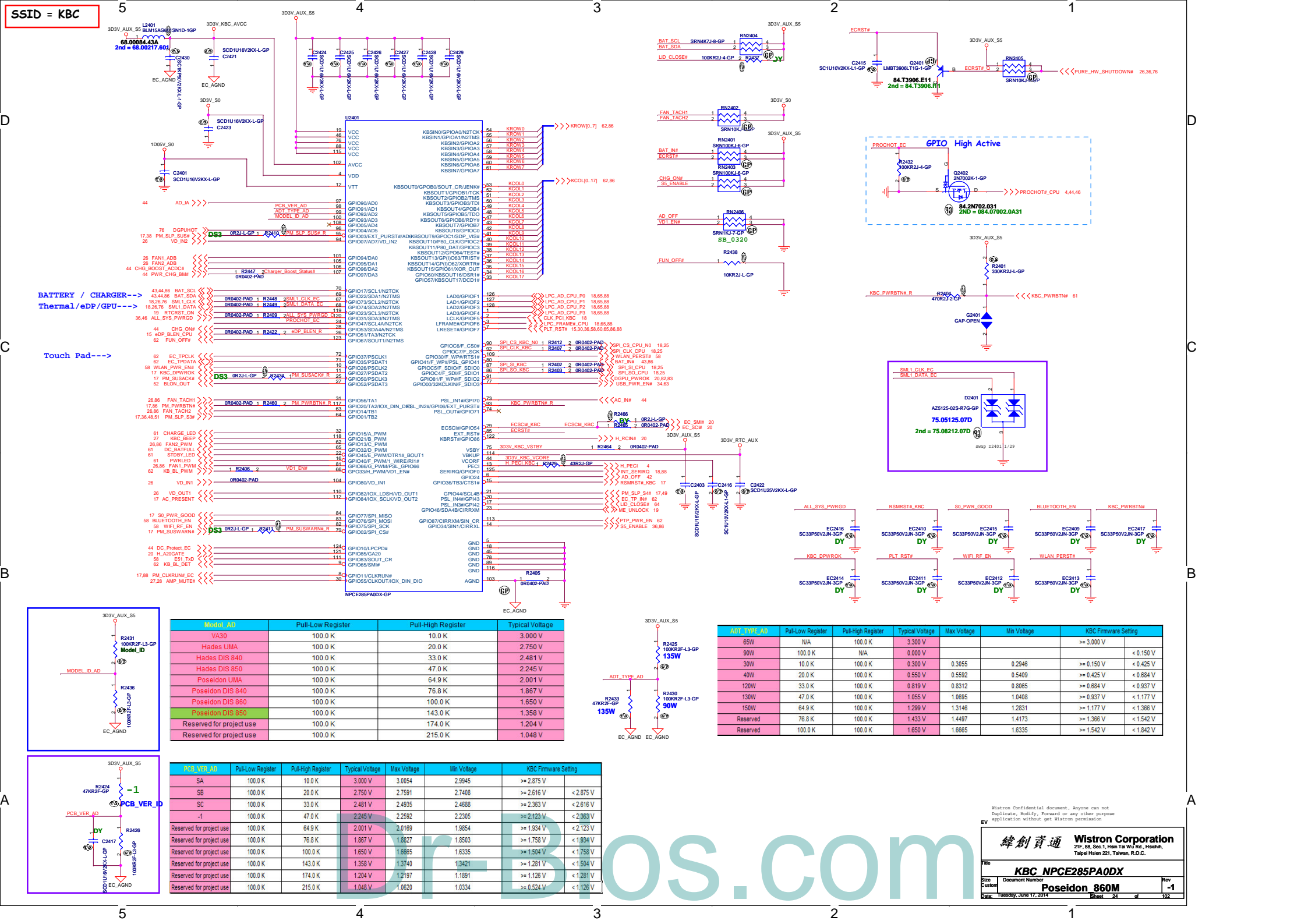
Poseidon 860M

-1

Date: Tuesday, June 17, 2014

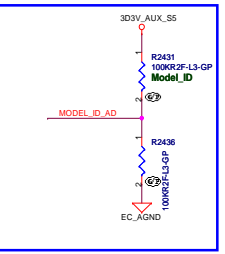
Sheet 23 of 102

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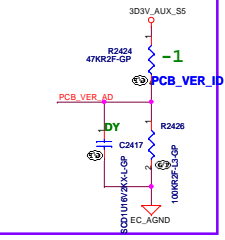


BATTERY / CHARGER-->
Thermal/eDP/GPU-->

Touch Pad-->



Model_ID	Pull-Low Register	Pull-High Register	Typical Voltage
VA30	100.0 K	10.0 K	3.000 V
Hades UMA	100.0 K	20.0 K	2.750 V
Hades DIS 840	100.0 K	33.0 K	2.481 V
Hades DIS 850	100.0 K	47.0 K	2.245 V
Poseidon UMA	100.0 K	64.9 K	2.001 V
Poseidon DIS 840	100.0 K	76.8 K	1.867 V
Poseidon DIS 860	100.0 K	100.0 K	1.650 V
Poseidon DIS 850	100.0 K	143.0 K	1.358 V
Reserved for project use	100.0 K	174.0 K	1.204 V
Reserved for project use	100.0 K	215.0 K	1.048 V



PCB_VER_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	Min Voltage	KBC Firmware Setting
SA	100.0 K	10.0 K	3.000 V	3.0054	2.9945	>= 2.875 V
SB	100.0 K	20.0 K	2.750 V	2.7591	2.7408	>= 2.616 V
SC	100.0 K	33.0 K	2.481 V	2.4935	2.4688	>= 2.363 V
-1	100.0 K	47.0 K	2.245 V	2.2592	2.2305	>= 2.123 V
Reserved for project use	100.0 K	64.9 K	2.001 V	2.0169	1.9854	>= 1.934 V
Reserved for project use	100.0 K	76.8 K	1.867 V	1.8827	1.8503	>= 1.758 V
Reserved for project use	100.0 K	100.0 K	1.650 V	1.6665	1.6335	>= 1.504 V
Reserved for project use	100.0 K	143.0 K	1.358 V	1.3740	1.3421	>= 1.281 V
Reserved for project use	100.0 K	174.0 K	1.204 V	1.2197	1.1891	>= 1.126 V
Reserved for project use	100.0 K	215.0 K	1.048 V	1.0620	1.0334	>= 0.924 V

ADT_TYP#_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	Min Voltage	KBC Firmware Setting
65W	N/A	100.0 K	3.300 V	3.3000	3.2946	>= 3.000 V
90W	100.0 K	N/A	0.000 V	0.0000	< 0.150 V	
30W	10.0 K	100.0 K	0.300 V	0.3055	0.2946	>= 0.150 V
40W	20.0 K	100.0 K	0.550 V	0.5592	0.5409	>= 0.425 V
120W	33.0 K	100.0 K	0.819 V	0.8312	0.8065	>= 0.684 V
130W	47.0 K	100.0 K	1.055 V	1.0695	1.0408	>= 0.937 V
150W	64.9 K	100.0 K	1.299 V	1.3146	1.2831	>= 1.177 V
Reserved	76.8 K	100.0 K	1.433 V	1.4497	1.4173	>= 1.366 V
Reserved	100.0 K	100.0 K	1.650 V	1.6665	1.6335	>= 1.542 V

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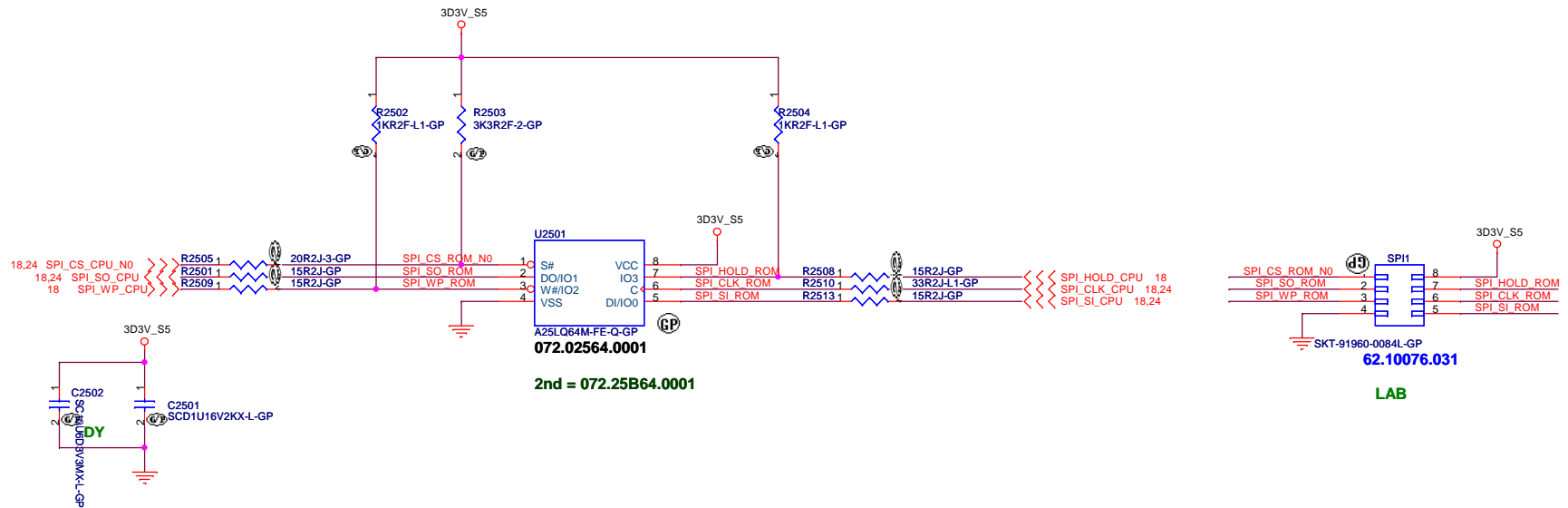
緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinshu, Taipei Hsien 221, Taiwan, R.O.C.

File: **KBC NPCE285PA0DX**
 Size: Document Number
 Custom: **Poseidon 860M**
 Date: 10/23/2014, June 17, 2014 Sheet 24 of 102 Rev 1

SSID = Flash.ROM

SPI FLASH ROM (8M byte) for PCH

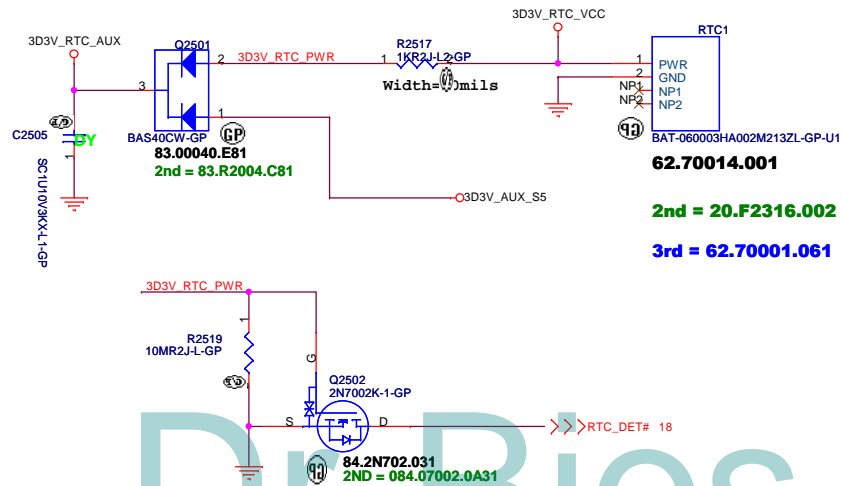
SPI ROM Equal length need to less than 500mil



2nd = 072.25B64.0001

LAB

SSID = RBAT



2nd = 20.F2316.002

3rd = 62.70001.061

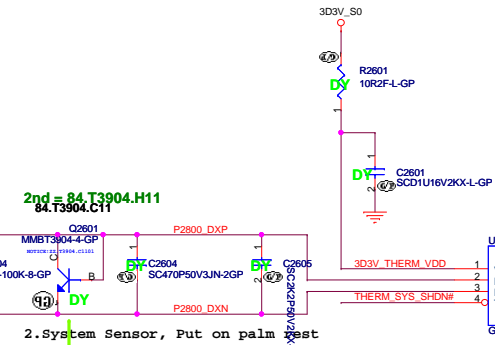
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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: Flash(KBC+PCH)/RTC			
Size: A3	Document Number:	Rev: -1	
Date: Tuesday, June 17, 2014			
Sheet 25 of 102			

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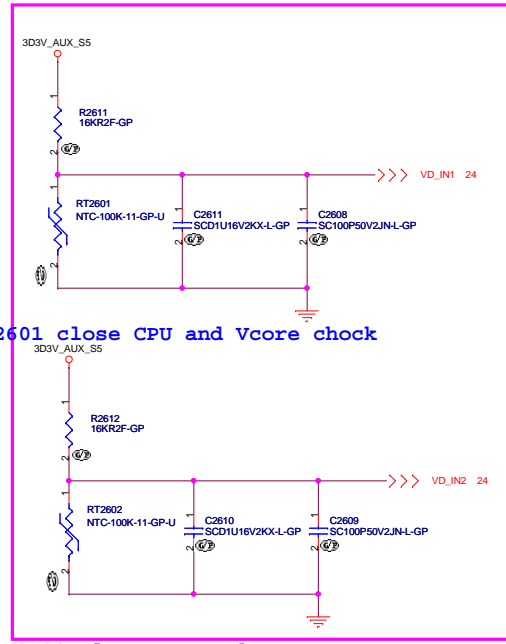
SSID = Thermal

Thermal sensor NCT 7718W



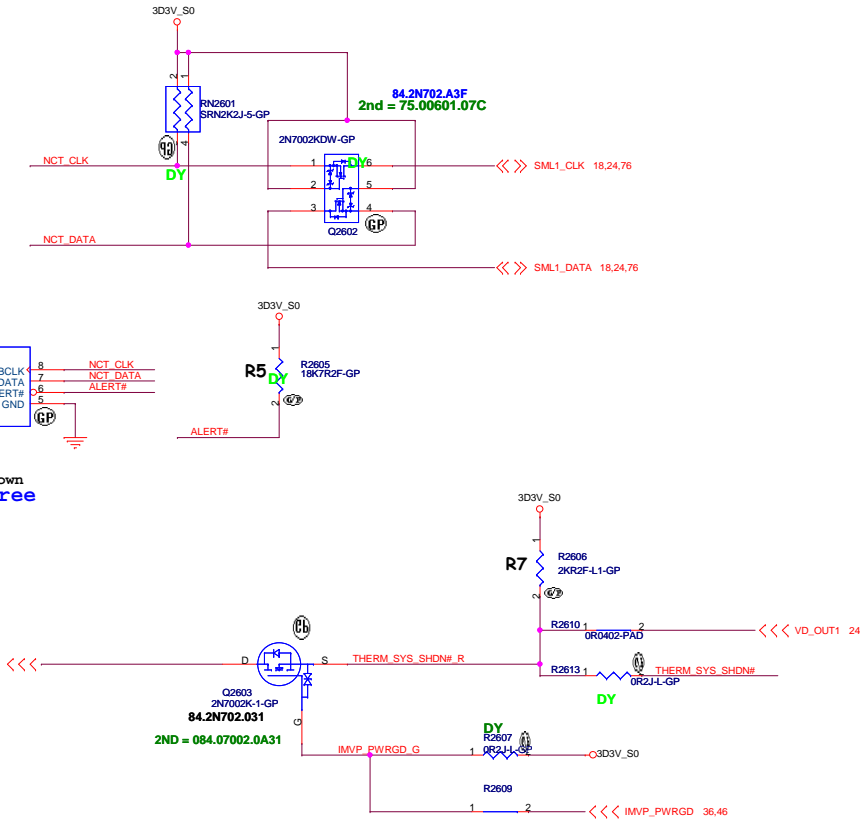
2.System Sensor, Put on palm best
Layout notice:
Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

074.00788.00B9
1.H/W T8 Shutdown
T8=85 degree

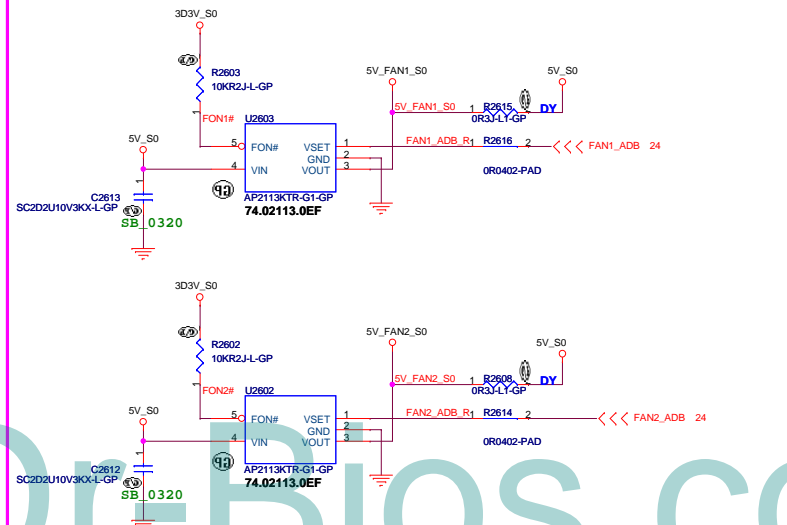


PT2601 close CPU and Vcore chock

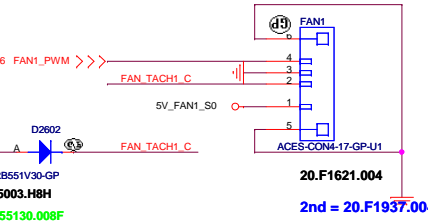
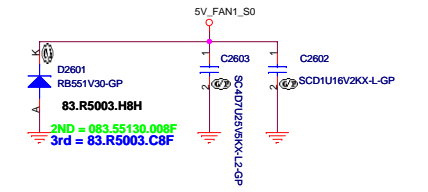
PT2602 close CPU and memory



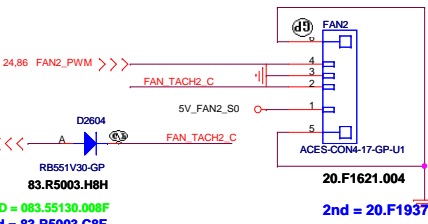
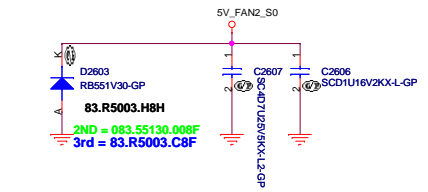
ADB (Active Dusting Blower) function



Layout 15 mil



Layout 15 mil



ALERT# / T CRIT#
Pull-up Resistor

	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
R5	77°C	87°C	97°C	107°C	117°C
7.5Kohm	79°C	89°C	99°C	109°C	119°C
10.5Kohm	81°C	91°C	101°C	111°C	121°C
14Kohm	83°C	93°C	103°C	113°C	123°C
18.7Kohm	85°C	95°C	105°C	115°C	125°C

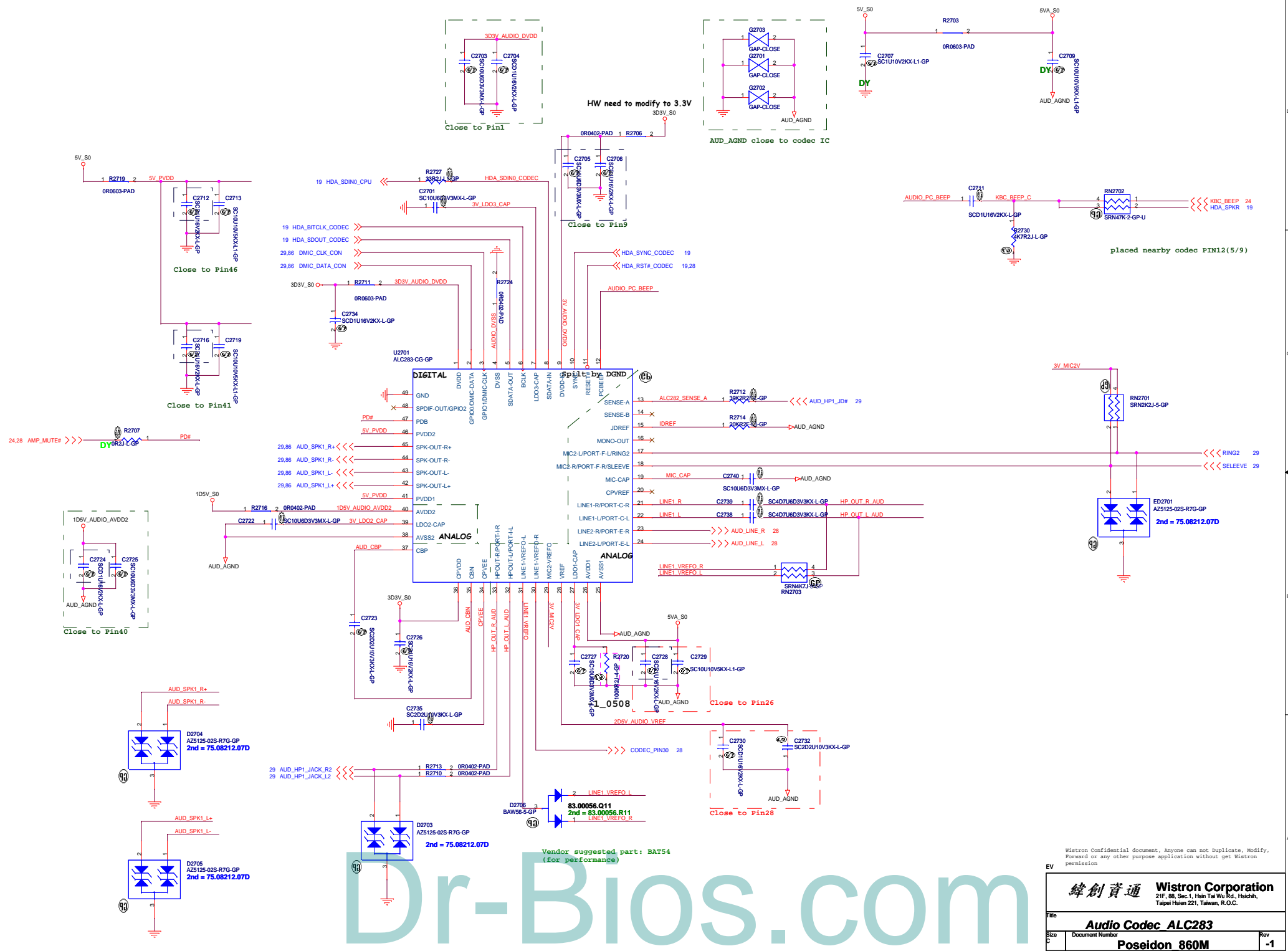
T8=85 degree - T_CRIT temperature strapping point

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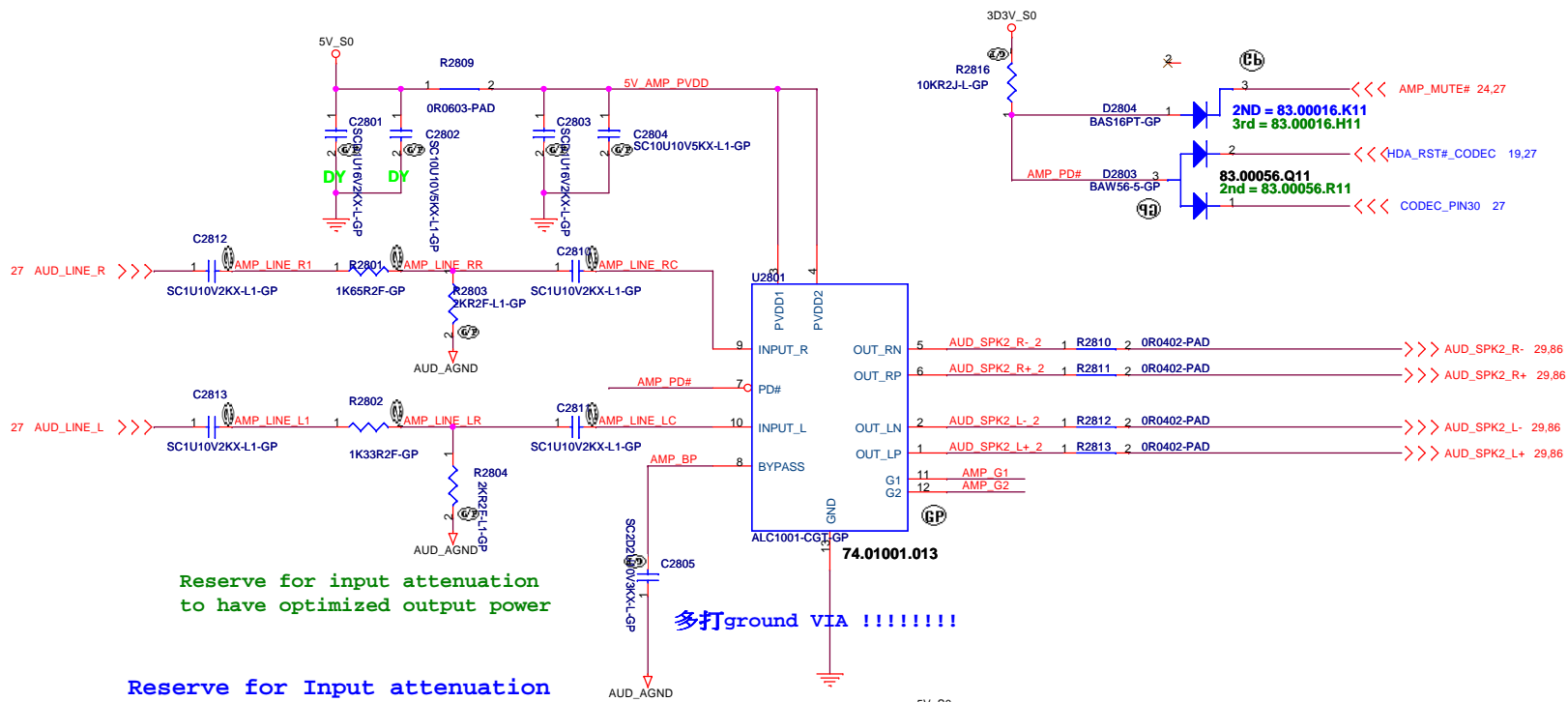
緯創資通 Wistron Corporation
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Thermal 7718/Fan Controller P2793		Rev
Size	Document Number	-1
Custom	Poseidon 860M	
Date: 1/26/2014, June 17, 2014	Sheet 26	of 102





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Reserve for input attenuation
to have optimized output power

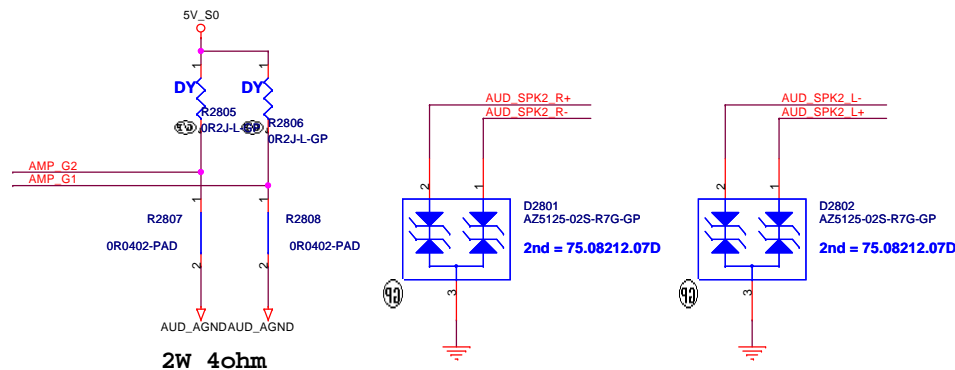
Reserve for Input attenuation
To have optimization output power

多打ground VIA !!!!!!!

Table 6. Amplifier Gain

G2	G1	Gain
0	0	11dB
0	1	14dB
1	0	19dB
1	1	25dB

*Condition is at 5V/40hm



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EV

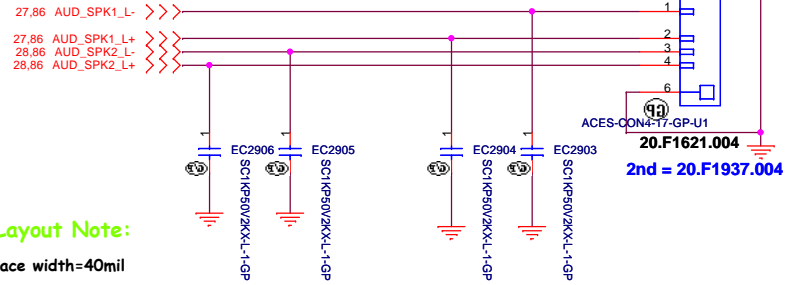
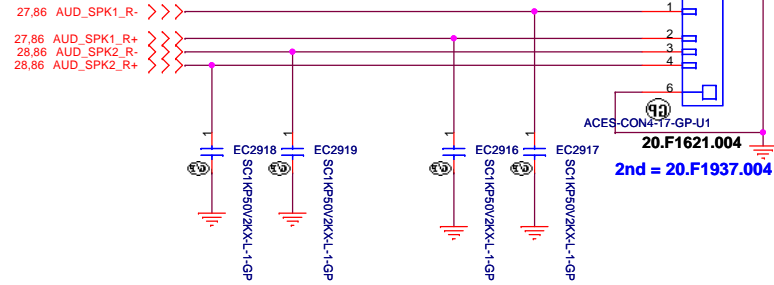
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Title		
Audio AMP 1001		
Size	Document Number	Rev
A3	Poseidon 860M	-1
Date:	Tuesday, June 17, 2014	Sheet 28 of 102

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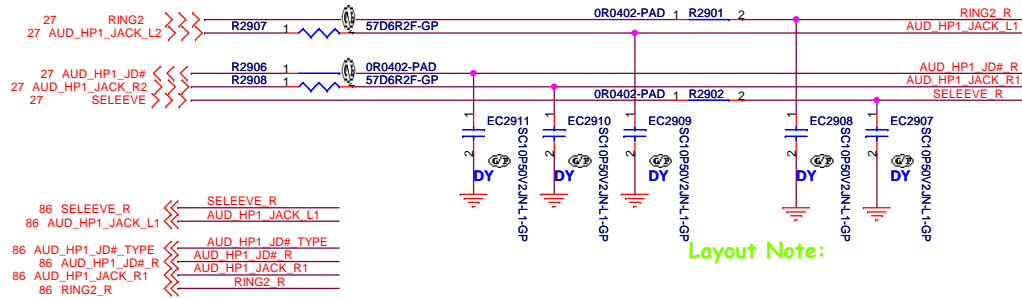
SSID = AUDIO

Speaker

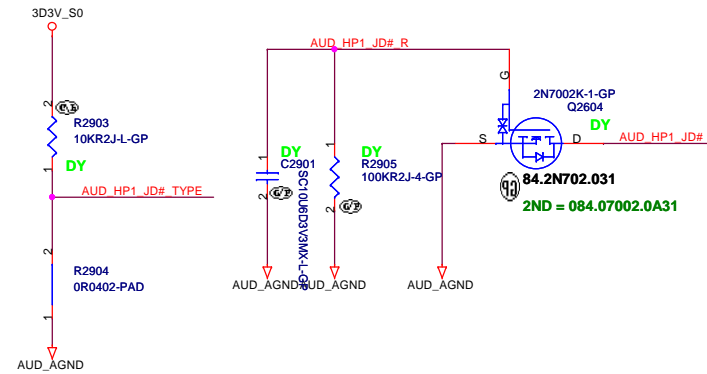
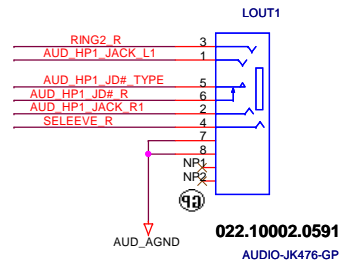


Layout Note:
Trace width=40mil

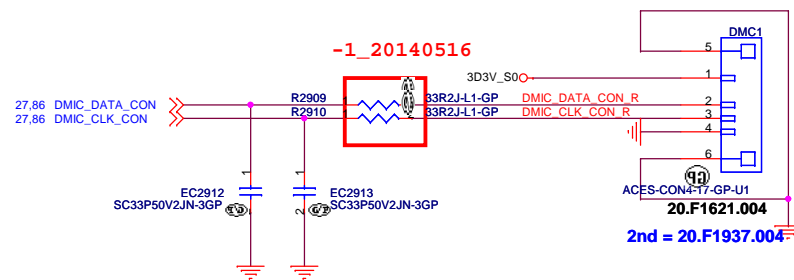
Combo Jack



Layout Note:



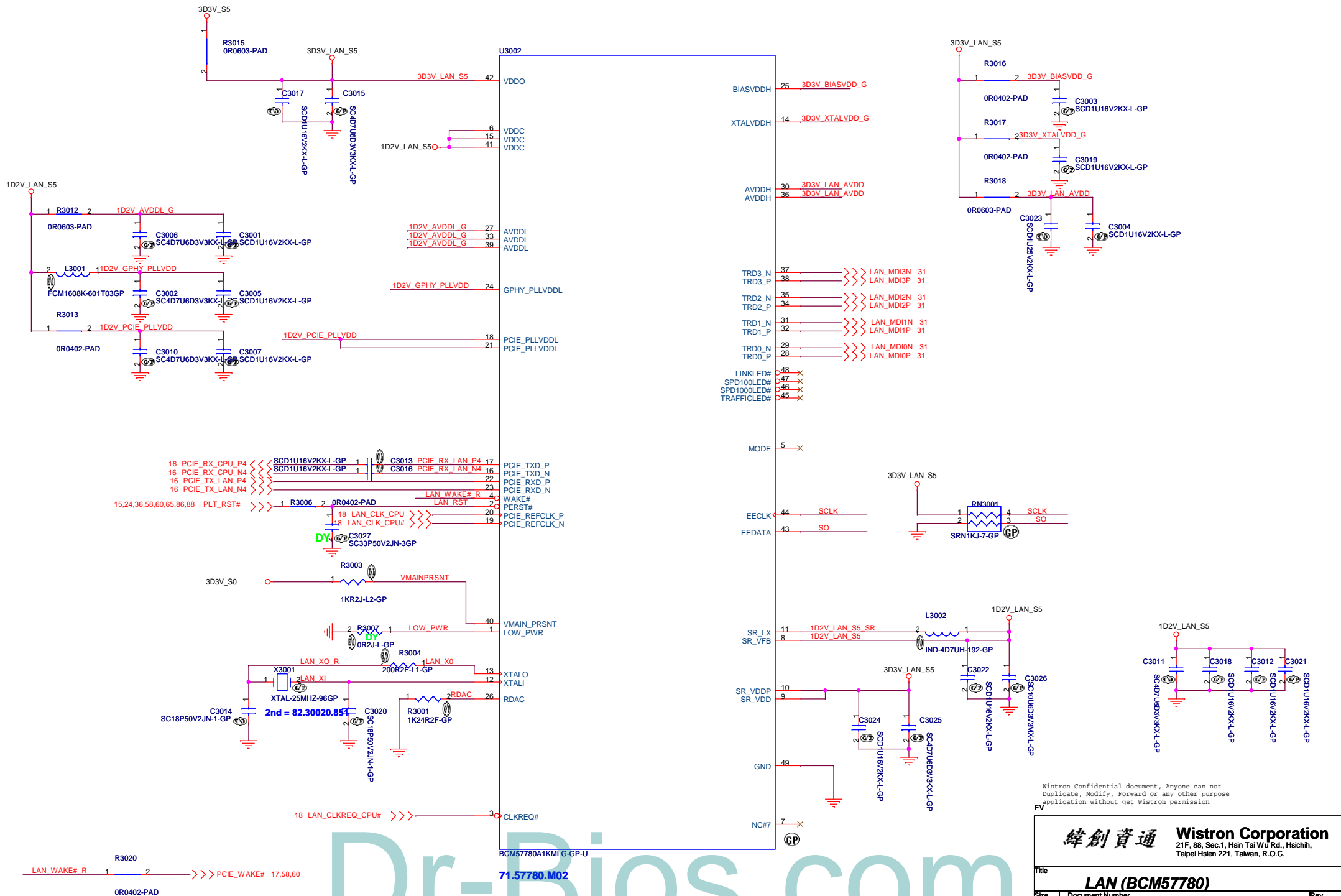
DMIC



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Audio Jack	
Title Document Number Date: Tuesday, June 17, 2014	Rev -1 Sheet 29 of 102



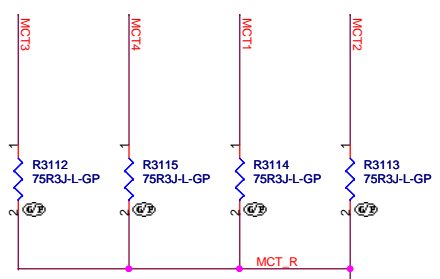
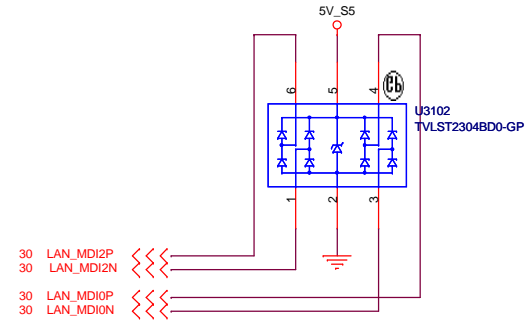
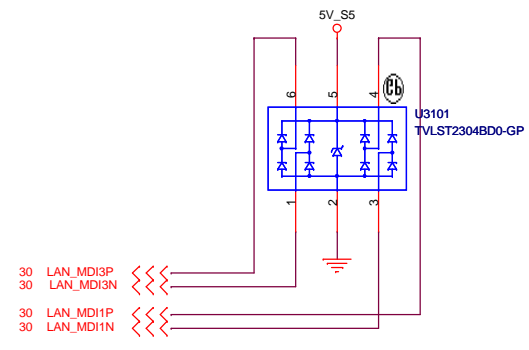
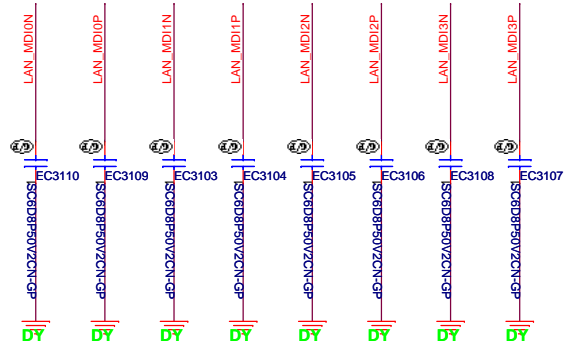
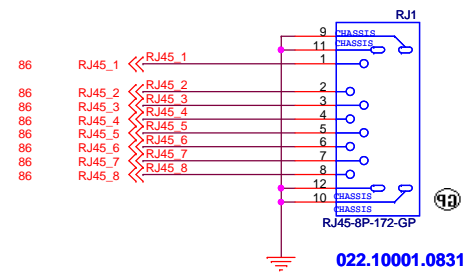
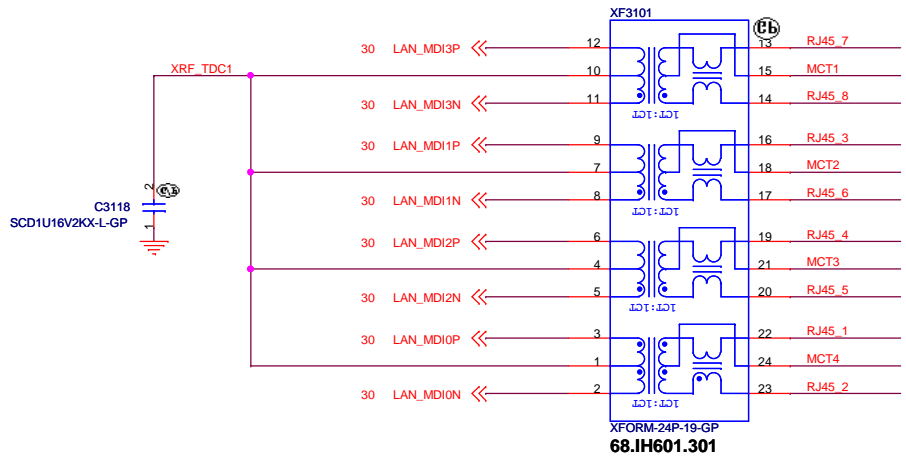
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Title		
LAN (BCM57780)		
Size	Document Number	Rev
A3	Poseidon 860M	-1
Date:	Tuesday, June 17, 2014	Sheet 30 of 102

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SSID = LAN



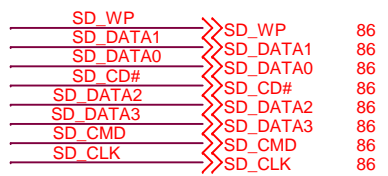
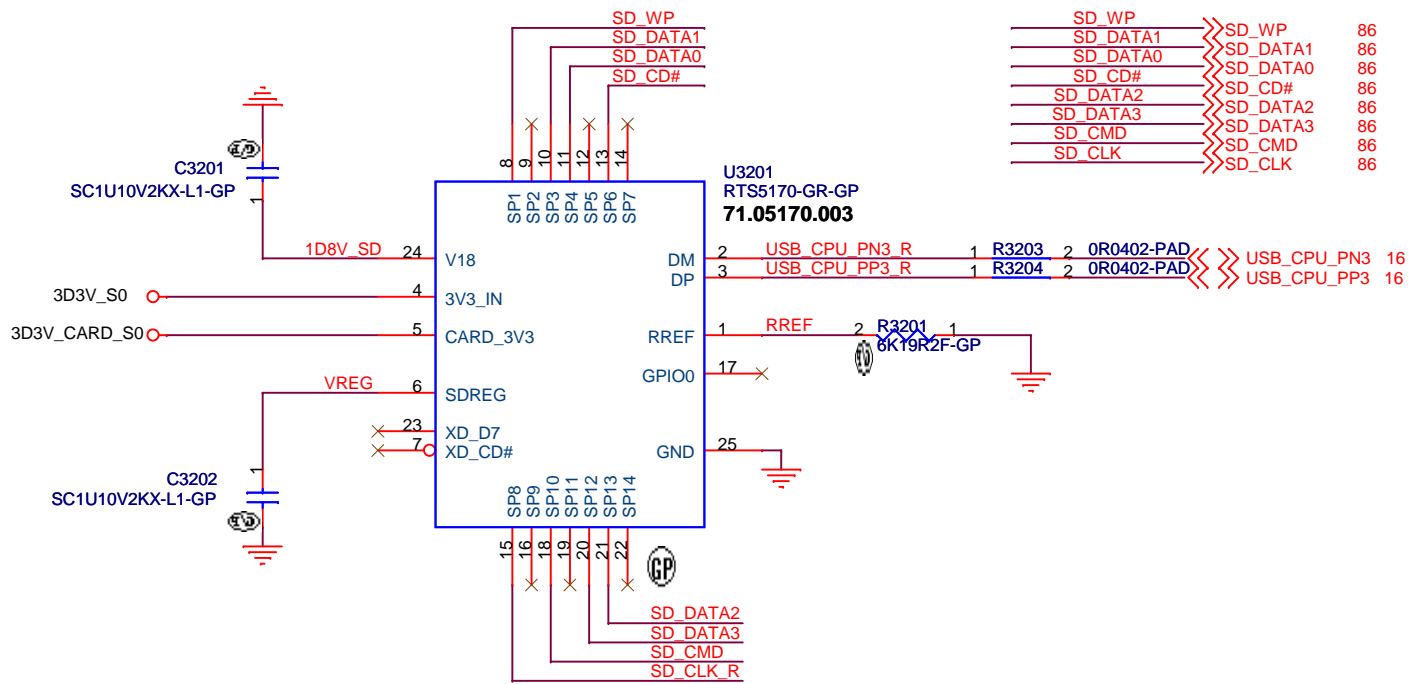
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EV

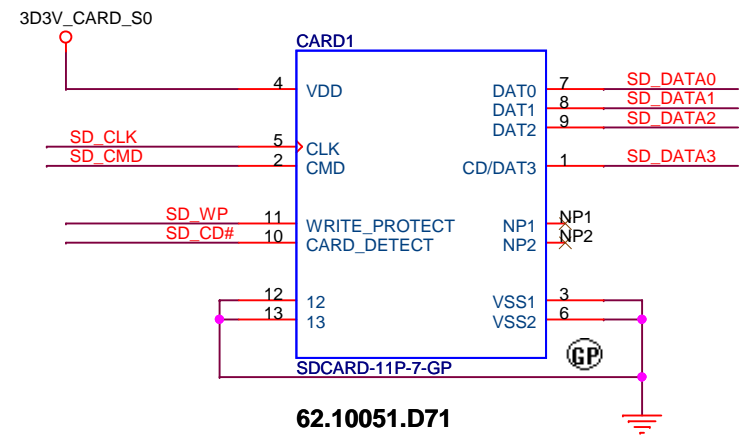
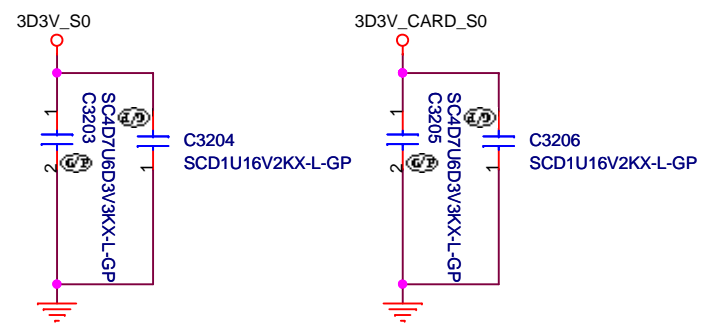
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Title: **(LAN+VGA) CONNECTOR**

Size: Custom	Document Number: Poseidon 860M	Rev: -1
Date: Tuesday, June 17, 2014	Sheet: 31	of 102

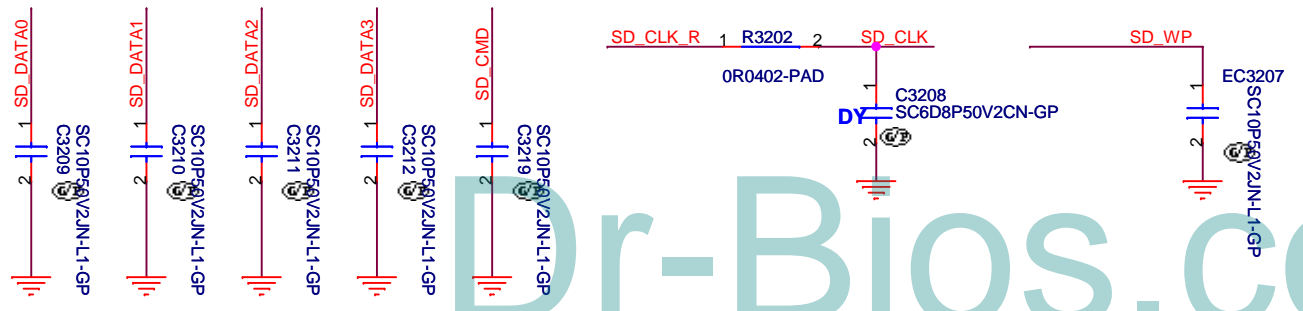


SP1	XD_CD#	SD_WP	MS_CLK
SP2	XD_RDY	SD_RE#	MS_INS#
SP3	XD_CE#	SD_D1	
SP4	XD_CLE	SD_D0	MS_D7
SP5	XD_ALE	SD_D7	MS_D3
SP6	XD_WE#	SD_CD#	
SP7	XD_WP	SD_D6	MS_D6
SP8	XD_D0	SD_CLK	MS_D2
SP9	XD_D1	SD_D5	MS_D0
SP10	XD_D2	SD_CMD	
SP11	XD_D3	SD_D4	MS_D4
SP12	XD_D4	SD_D3	MS_D1
SP13	XD_D5	SD_D2	MS_D5
SP14	XD_D6		MS_BS
	XD_D7		



2nd = 62.10051.C41

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Title **RTS5170 (CARD READER)**

Size A4	Document Number Poseidon 860M	Rev -1
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Date: Tuesday, June 17, 2014 **Sheet** 32 **of** 102

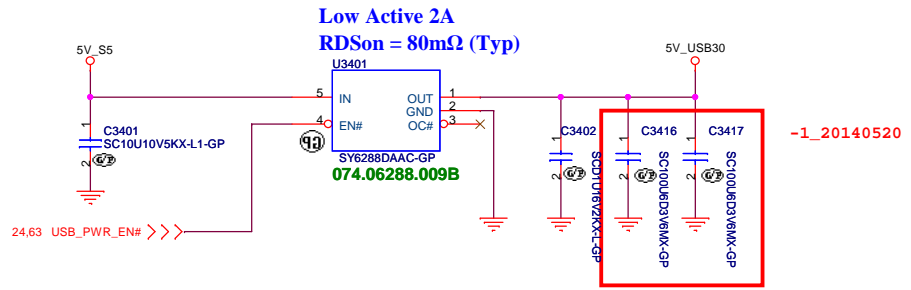
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Title			
Card Reader CONN (Reserved)			
Size	Document Number		Rev
Custom	Poseidon_860M		-1
Date:	Tuesday, June 17, 2014	Sheet 33	of 102

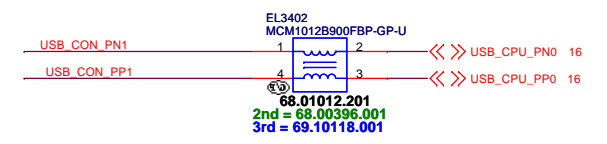
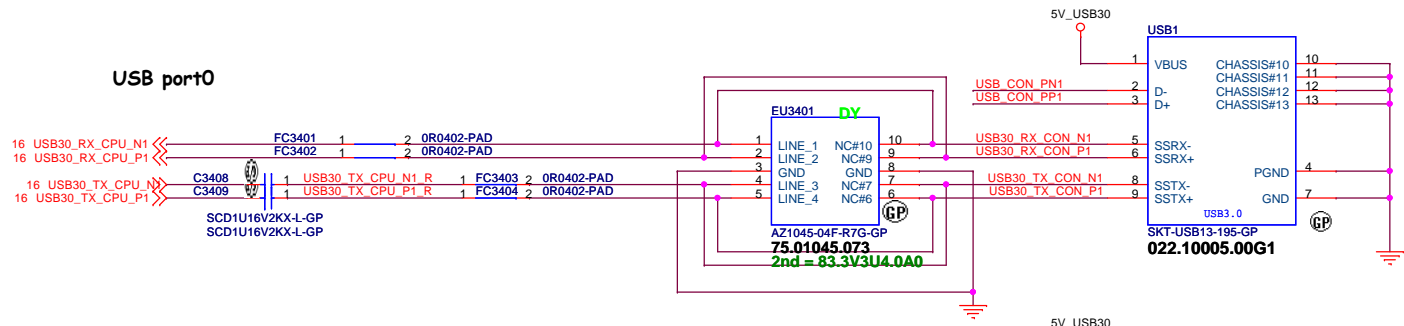
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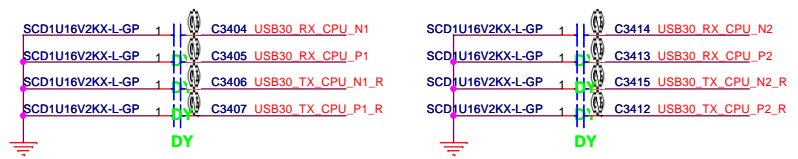
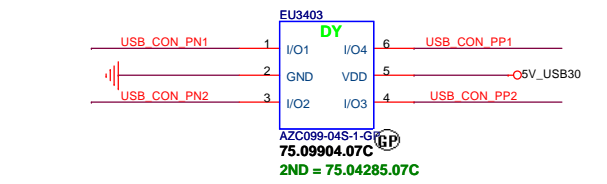
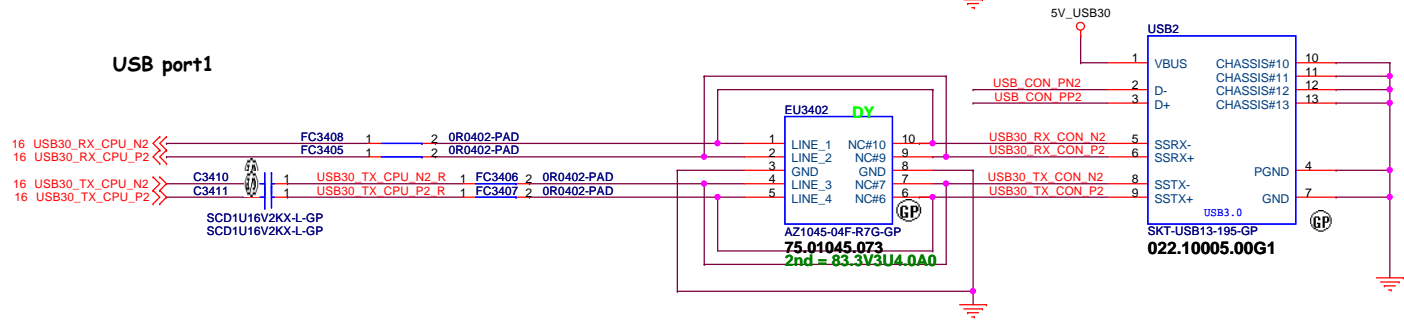
USB 3.0 Connector Pin definition

1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+

USB port0



USB port1



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Title: **USB 2.0 / 3.0 Port**

Size A3 Document Number: **Poseidon 860M** Rev: **-1**

Date: Tuesday, June 17, 2014 Sheet 34 of 102

D

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A

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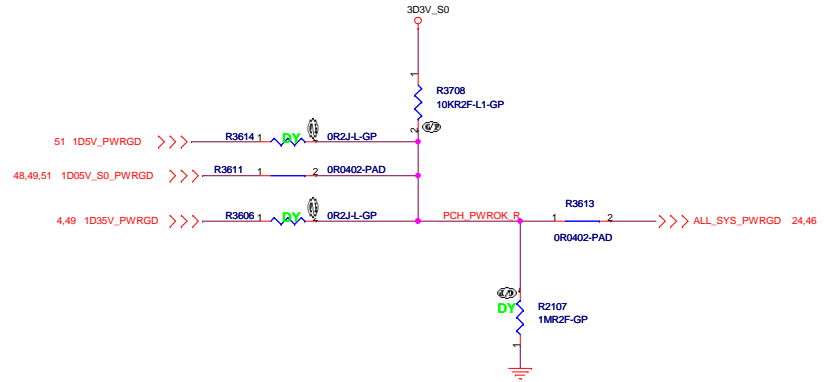
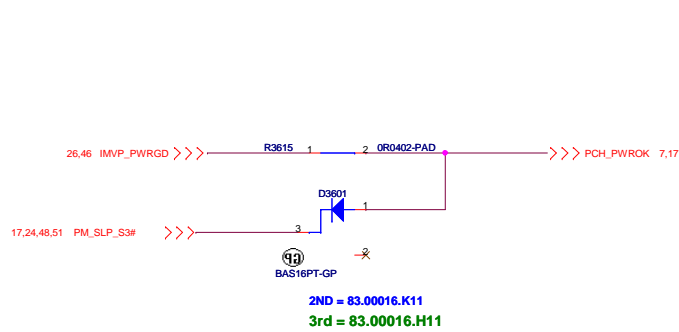
EV

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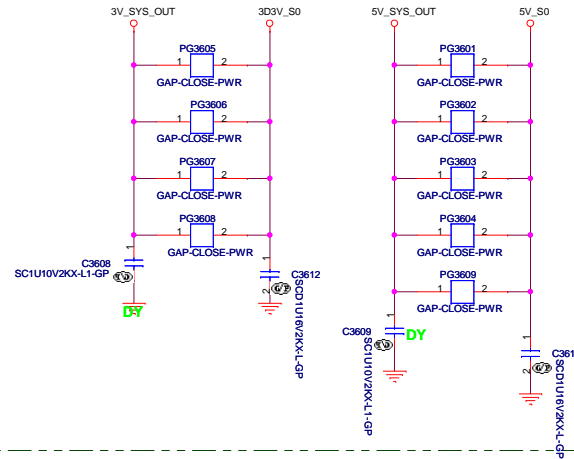
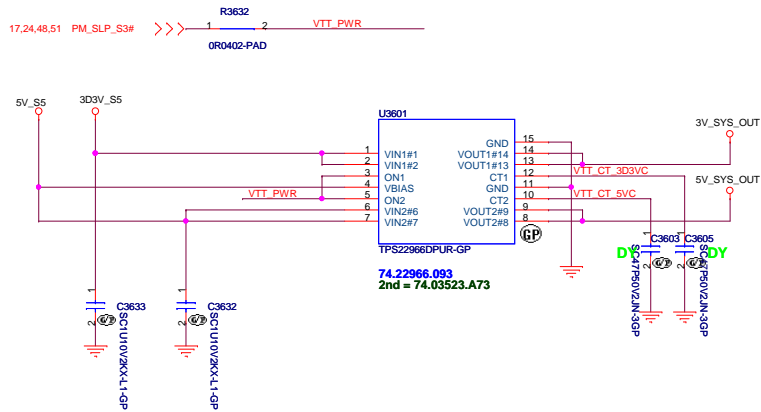
Title		
USB CHARGER		
Size	Document Number	Rev
A4	Poseidon 860M	-1
Date:	Tuesday, June 17, 2014	Sheet 35 of 102

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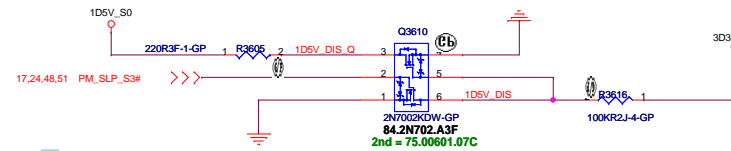
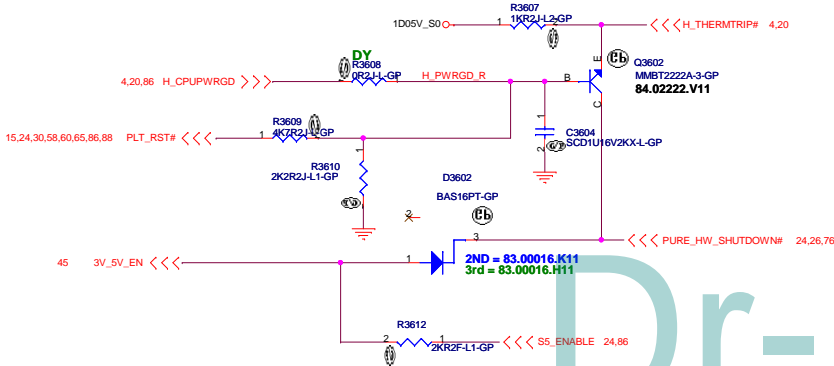
Power Sequence



ANNIE Run Power



Discharge circuit



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Title	Power Plane Enable & SEQUENCE	
Size	Document Number	Rev
Custom	Poseidon 860M	-1
Date:	1/06/09, June 17, 2014	Sheet 36 of 102

5

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C

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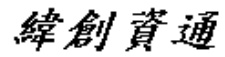
B

A

A

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Title	
ADAPTER OCP / S3 reduction	
Size	Document Number
Custom	Poseidon 860M
Date:	Rev
Tuesday, June 17, 2014	-1
Sheet 37 of 102	

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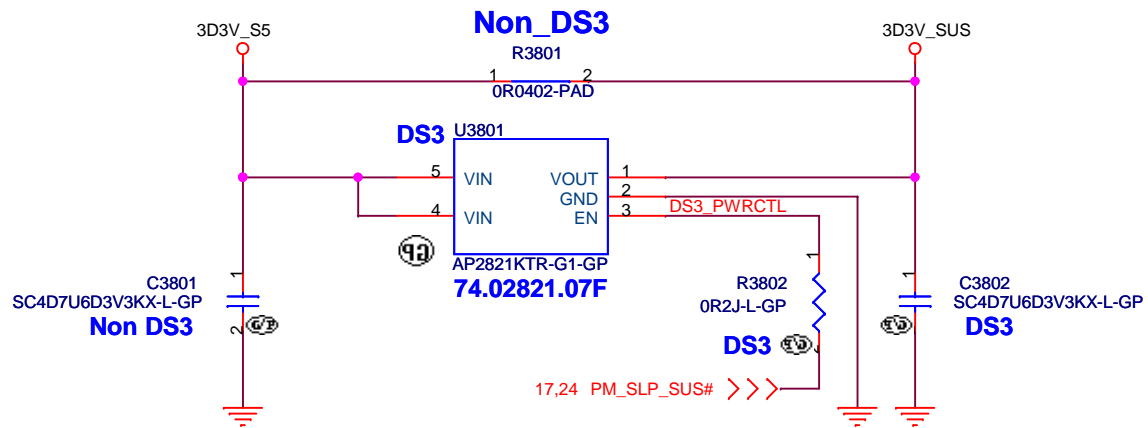
5

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Title

DS3

Size

A4

Document Number

Poseidon 860M

Rev

-1

Date: Tuesday, June 17, 2014

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D

D

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C

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A

A

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EV

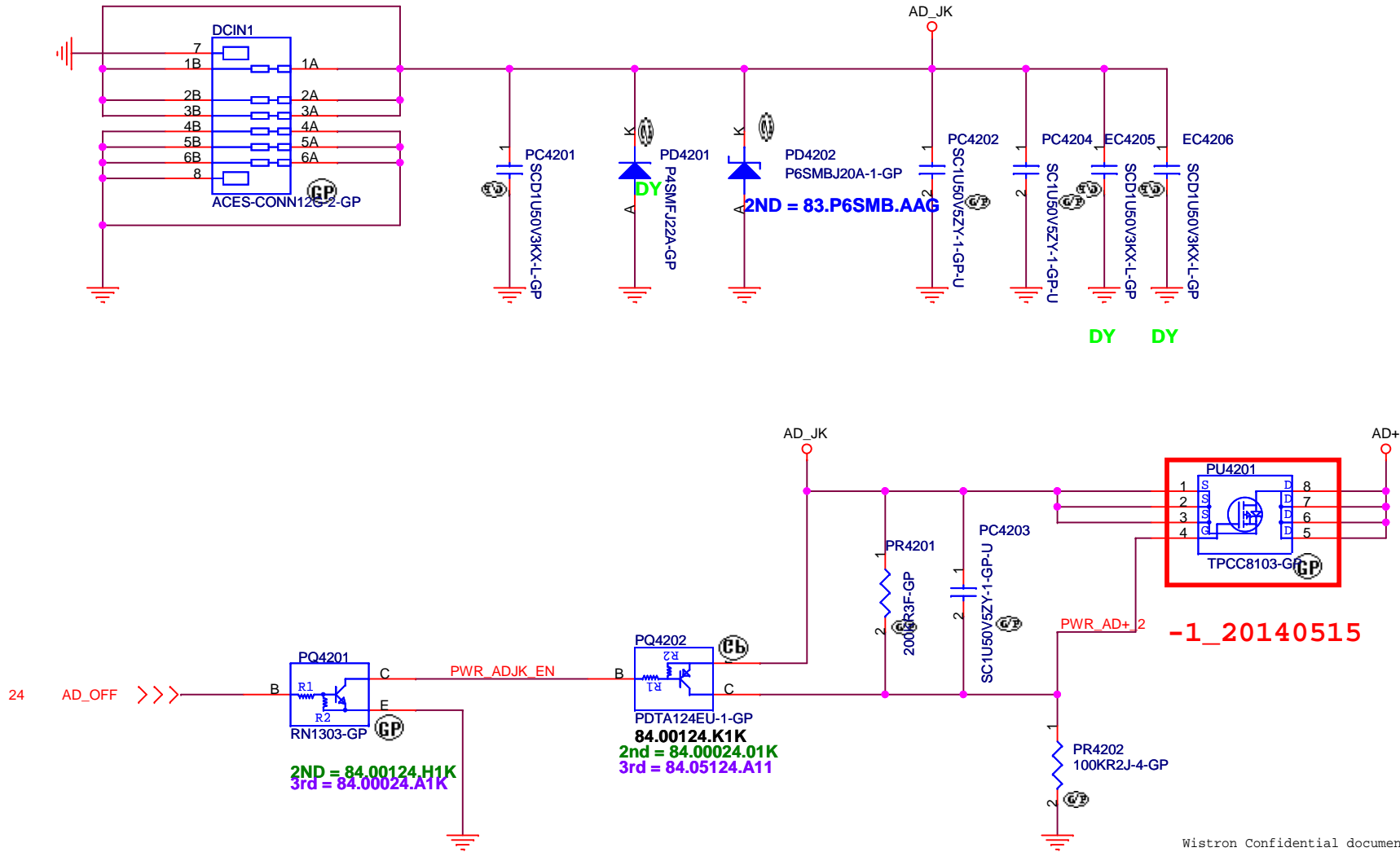
緯創資通 **Wistron Corporation**
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Title		
1D05 M		
Size	Document Number	Rev
A4	Poseidon 860M	-1
Date:	Tuesday, June 17, 2014	Sheet 39 of 102

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ANNIE solution

Adaptor in to generate DCBATOUT



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EV

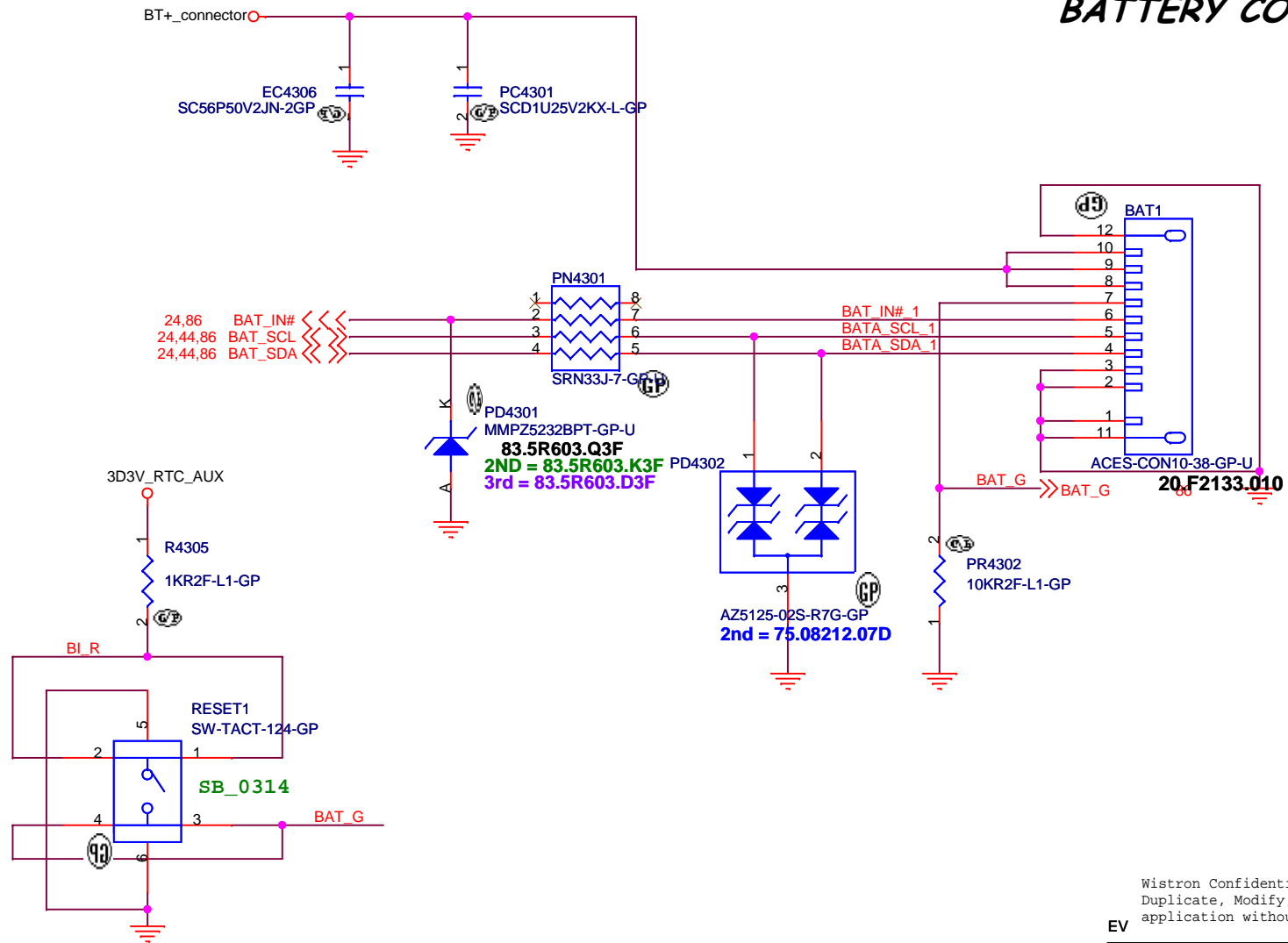
緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title			DCIN JACK
Size	Document Number	Rev	
A4	Poseidon 860M	-1	
Date	Tuesday, June 17, 2014	Sheet	42 of 102

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BATTERY CONNECTOR



62.40078.001
 2nd = 62.40009.E51
 3rd = 62.40009.D71

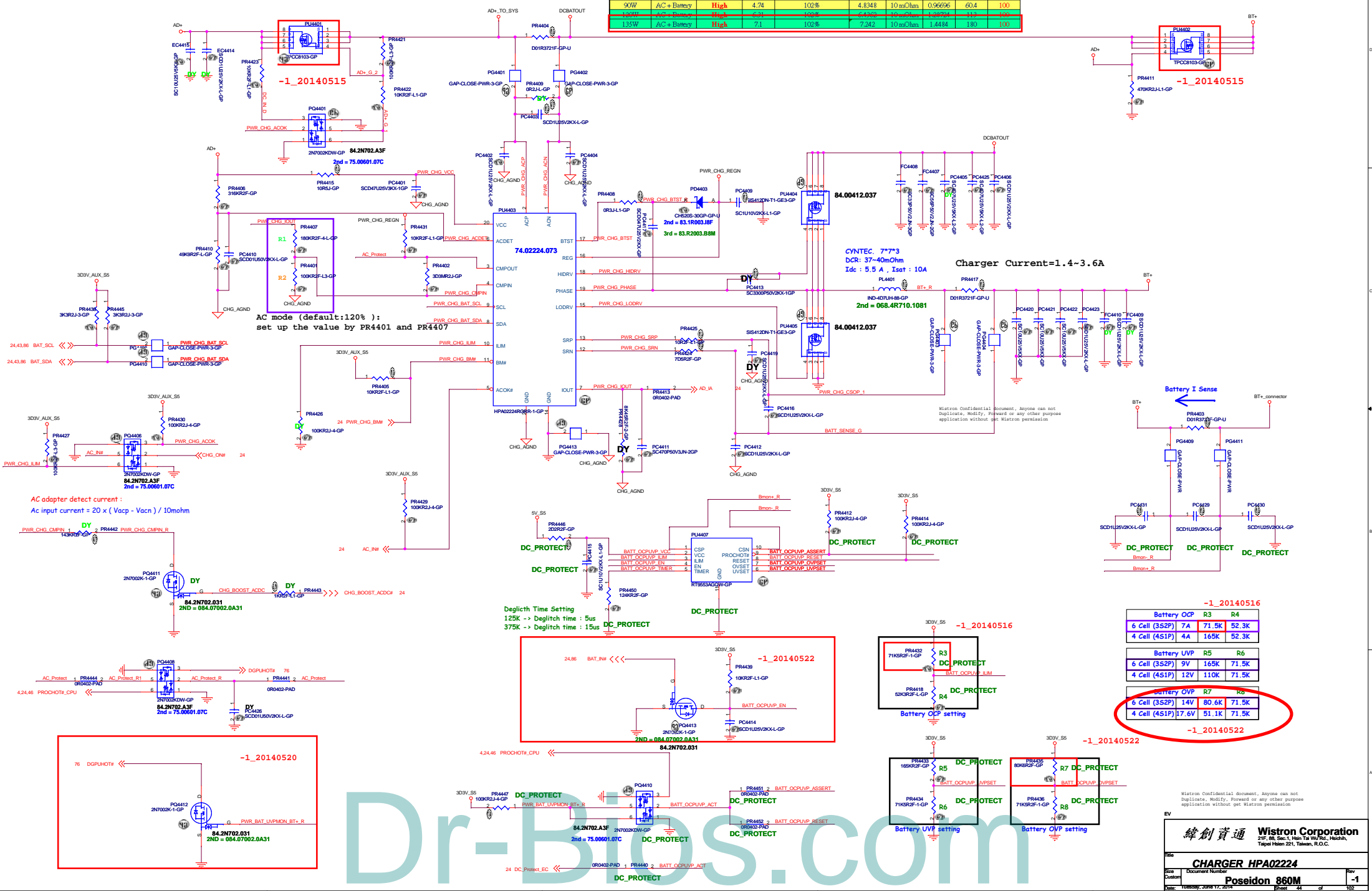
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Title			
BATT CONN			
Size A4	Document Number	Rev Poseidon 860M -1	
Date: Tuesday, June 17, 2014		Sheet 43	of 102

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	Stat	PM_SLP_A#	Adaptor Current	AC_Protect preset (85% x 120%)	AC_Protect Current	FR4404 Sense resistor	Current to Voltage	R1	FR4401
40W	AC + Battery	High	2.1	102%	2.142	20mOhm	0.8568	41.2	100
45W	AC + Battery	High	2.37	102%	2.4174	20mOhm	0.96696	60.4	100
65W	AC + Battery	High	3.42	102%	3.4884	10mOhm	0.69763	16.2	100
90W	AC + Battery	High	4.74	102%	4.8348	10mOhm	0.96696	60.4	100
120W	AC + Battery	High	6.31	102%	6.4362	10mOhm	1.28924	112	100
135W	AC + Battery	High	7.1	102%	7.242	10mOhm	1.4484	180	100



Battery OCP

	OCP	R3	R4
6 Cell (3S2P)	7A	71.5K	52.3K
4 Cell (4S1P)	4A	165K	52.3K

Battery UVP

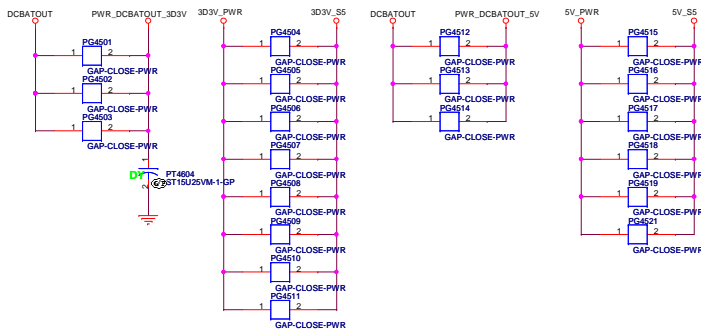
	UVP	R5	R6
6 Cell (3S2P)	9V	165K	71.5K
4 Cell (4S1P)	12V	110K	71.5K

Battery OVP

	OVP	R7	R8
6 Cell (3S2P)	14V	80.6K	71.5K
4 Cell (4S1P)	17.6V	51.1K	71.5K

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SSID = PWR.Plane.Regulator_3p3v5v



High Side
84.00412.037 SIS412
Vgs @ 4.5V,
Id = 12A,
Rds(on) = 24 ~ 30mohm

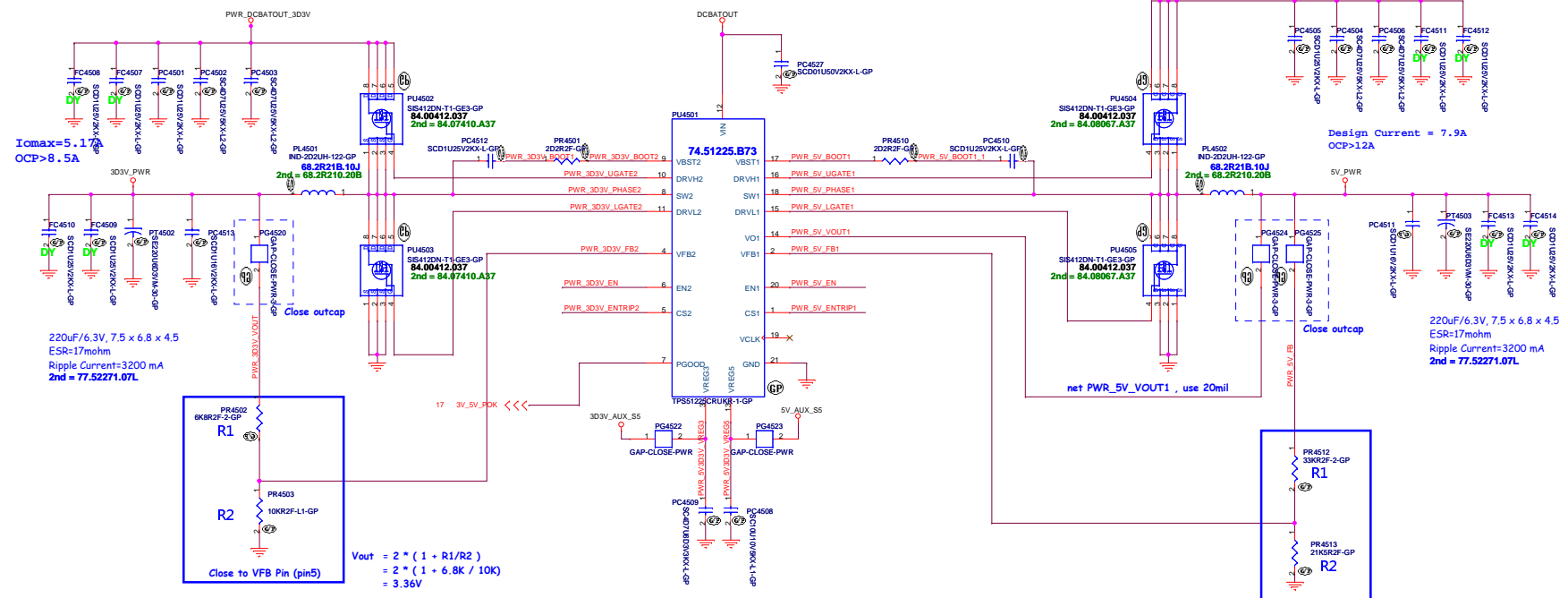
Low Side
84.00412.037 SIS412
Vgs @ 4.5V,
Id = 12A,
Rds(on) = 24 ~ 30mohm

Choke
MagLayers. 7x7x3 , 2R2
Dcr : 18 ~ 20 mOhm
Idc : 8A Isat : 14 A

High Side
84.00412.037 SIS412
Vgs @ 4.5V,
Id = 12A,
Rds(on) = 24 ~ 30mohm

Low Side
84.00412.037 SIS412
Vgs @ 4.5V,
Id = 12A,
Rds(on) = 24 ~ 30mohm

Choke
MagLayers. 7x7x3 , 2R2
Dcr : 18 ~ 20 mOhm
Idc : 8A Isat : 14 A

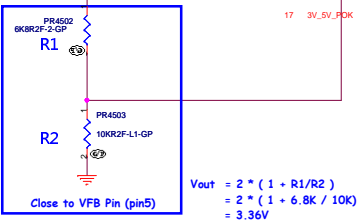


$I_{Omax} = 5.1A$
OCP > 8.5A

Design Current = 7.9A
OCP > 12A

220uF/6.3V, 7.5 x 6.8 x 4.5
ESR=17mohm
Ripple Current=3200 mA
2nd = 77.52271.07L

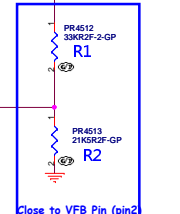
220uF/6.3V, 7.5 x 6.8 x 4.5
ESR=17mohm
Ripple Current=3200 mA
2nd = 77.52271.07L



$$V_{out} = 2 * (1 + R1/R2)$$

$$= 2 * (1 + 6.8K / 10K)$$

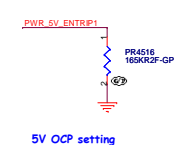
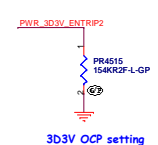
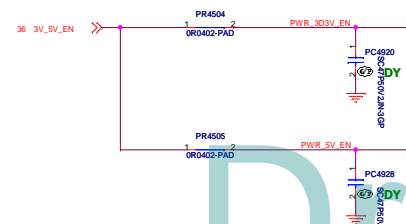
$$= 3.36V$$



$$V_{out} = 2 * (1 + R1/R2)$$

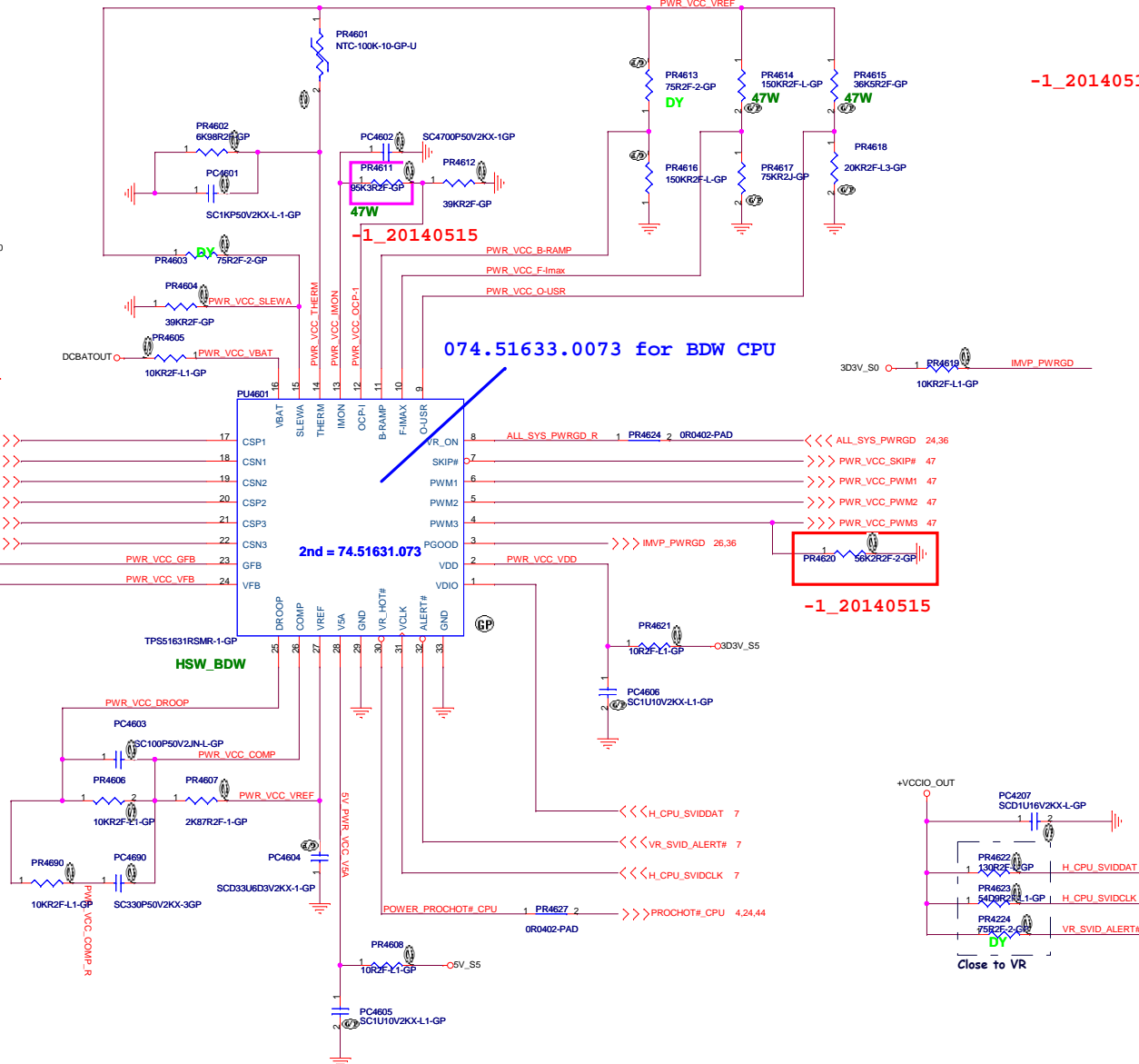
$$= 2 * (1 + 33K / 21K)$$

$$= 5.14V$$



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SSID = CPU.Regulator



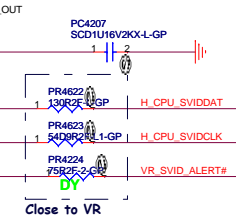
	47W
PC4602	4.7nF
	78.47224.2FL
PR4611	95.3k
	64.95325.6DL
PR4614	150k
	64.15035.6DL
PR4617	75k
	63.75334.1DL
PR4615	36.5k
	64.36525.6DL
PR4618	20k
	64.20025.6DL
PR4626	DY
PR4630	DY
PR4602	6.98k
	64.69815.6DL
PR4607	2.87k
	64.28715.6DL

-1_20140515

-1_20140515

2nd = 74.51631.073

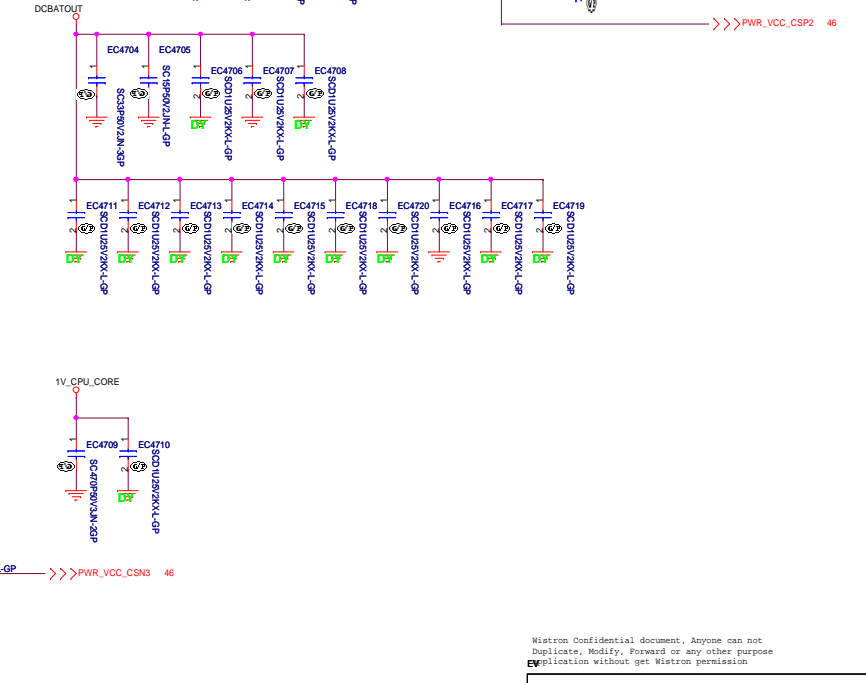
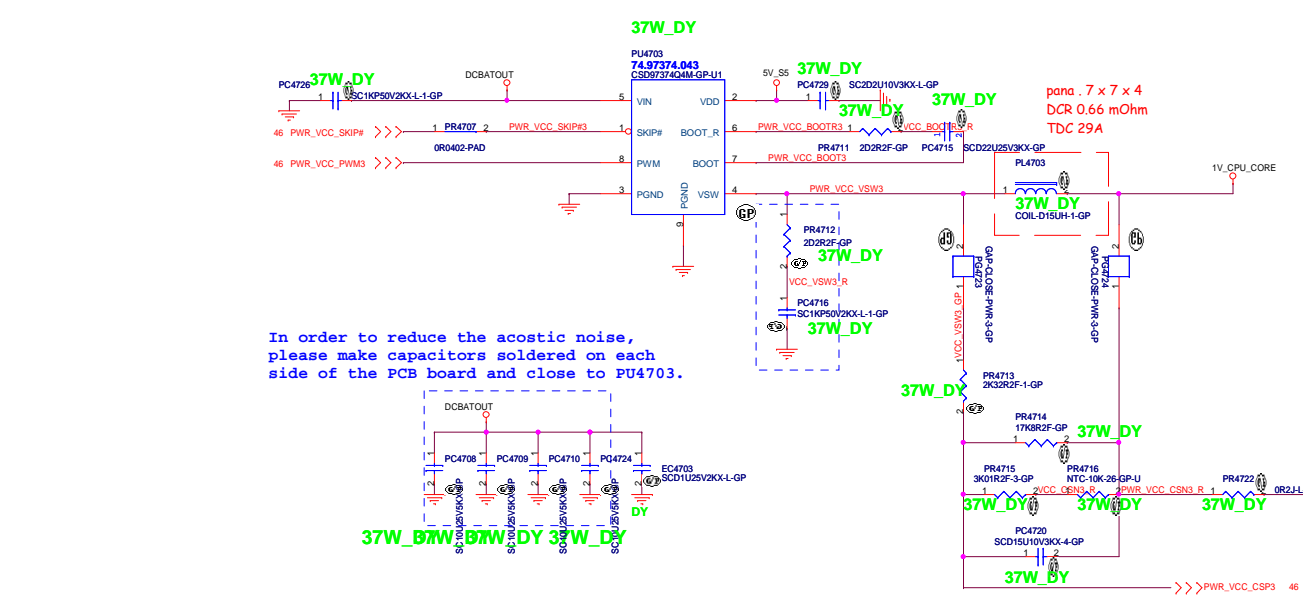
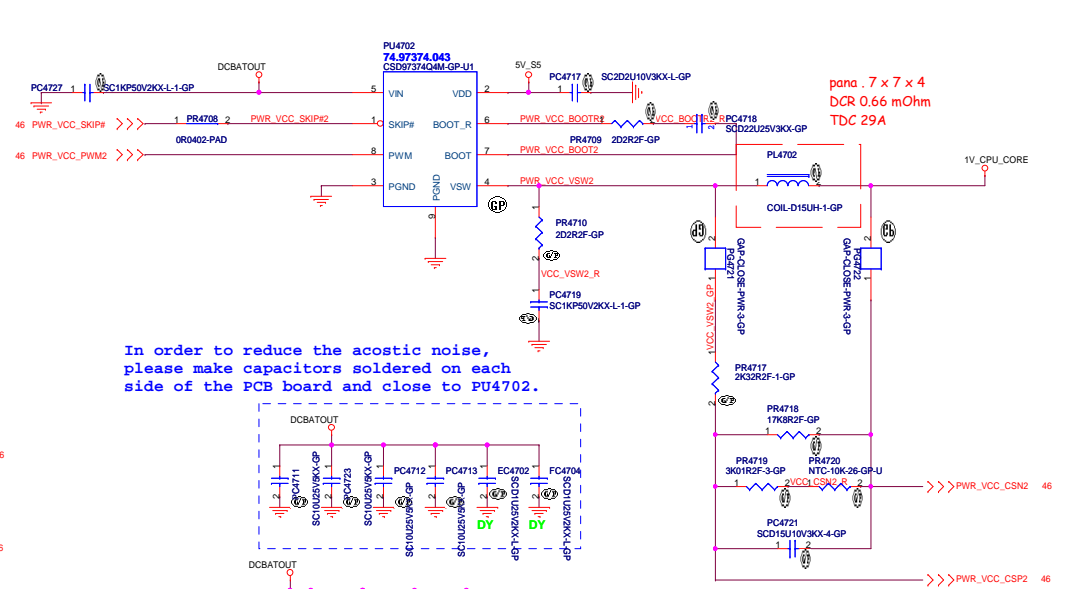
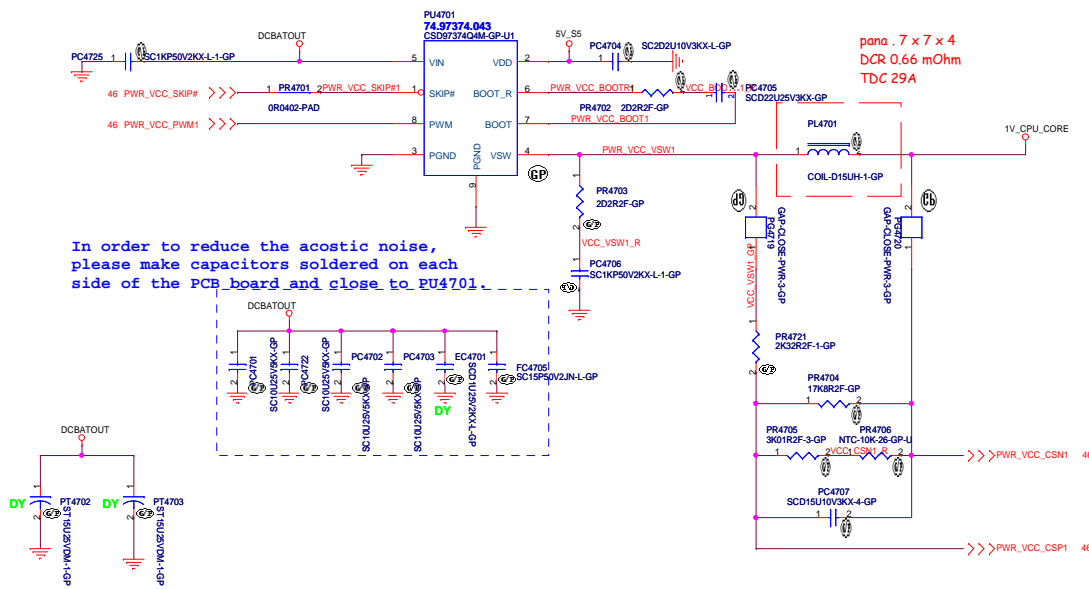
074.51633.0073 for BDW CPU



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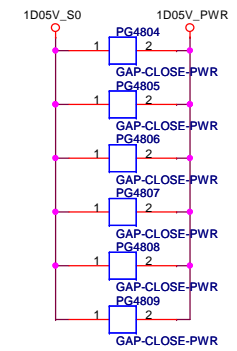
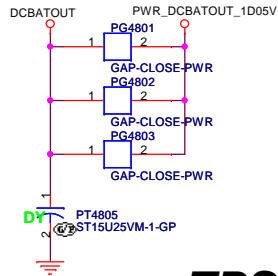
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Title	TPS51361 CPUCORE(1/2)
Size	Custom
Document Number	Poseidon 840M
Date	1 066day, June 17, 2014
Rev	-1
Sheet	46 of 102

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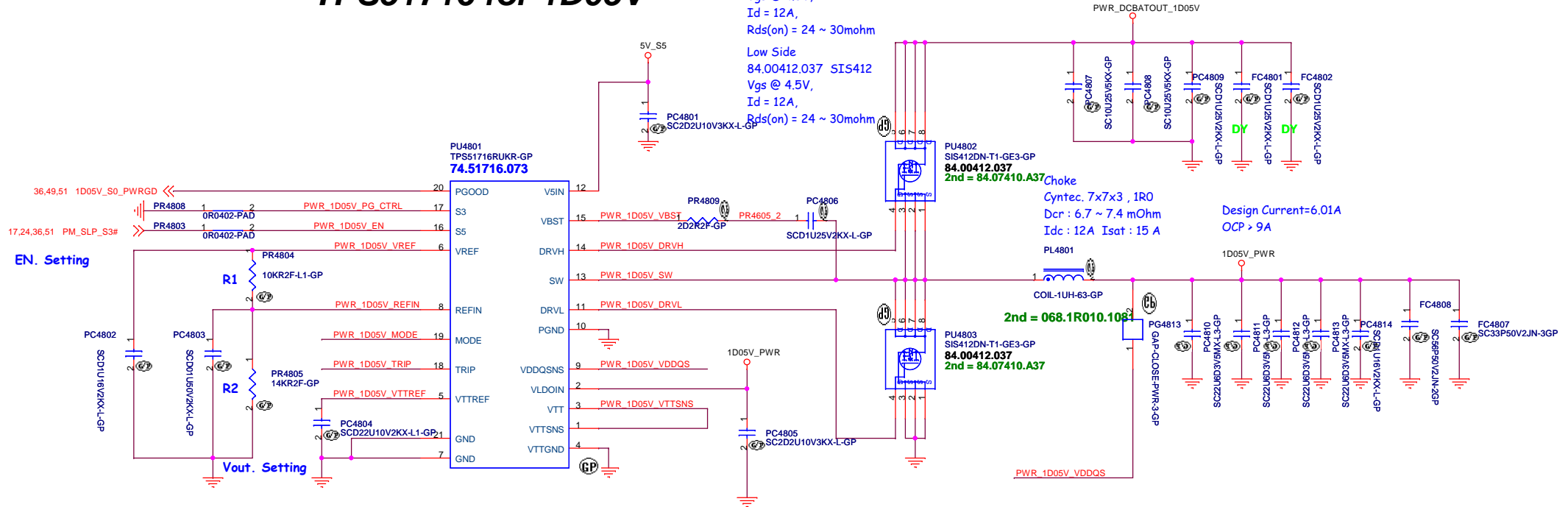
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TPS51361_CPUCORE(2/2)			
Title	Document Number	Rev	
Size	Document Number	Rev	
Poseidon 860M			-1
Date: 108day, June 17, 2014	Sheet	47	of 102



TPS51716 for 1D05V

High Side
84.00412.037 SIS412
Vgs @ 4.5V,
Id = 12A,
Rds(on) = 24 ~ 30mohm

Low Side
84.00412.037 SIS412
Vgs @ 4.5V,
Id = 12A,
Rds(on) = 24 ~ 30mohm



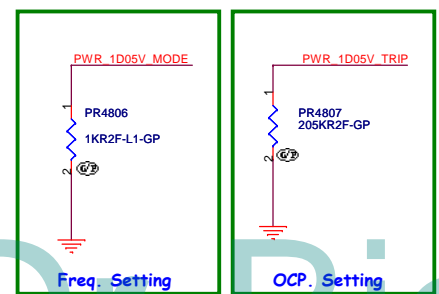
EN. Setting

Vout. Setting

Choke
Cyntec. 7x7x3, 1R0
Dcr: 6.7 ~ 7.4 mOhm
Idc: 12A Isat: 15 A

Design Current=6.01A
OCP > 9A

MODE	Frequency	Discharge Mode
PR5006	500kHz	Non-tracking Discharge
33k ohm	670kHz	
22k ohm	670kHz	Tracking Discharge
12k ohm	500kHz	
1k ohm	500kHz	



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

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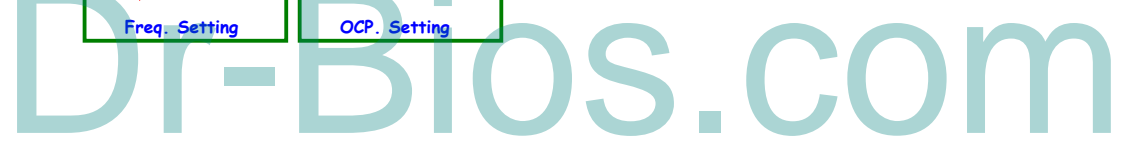
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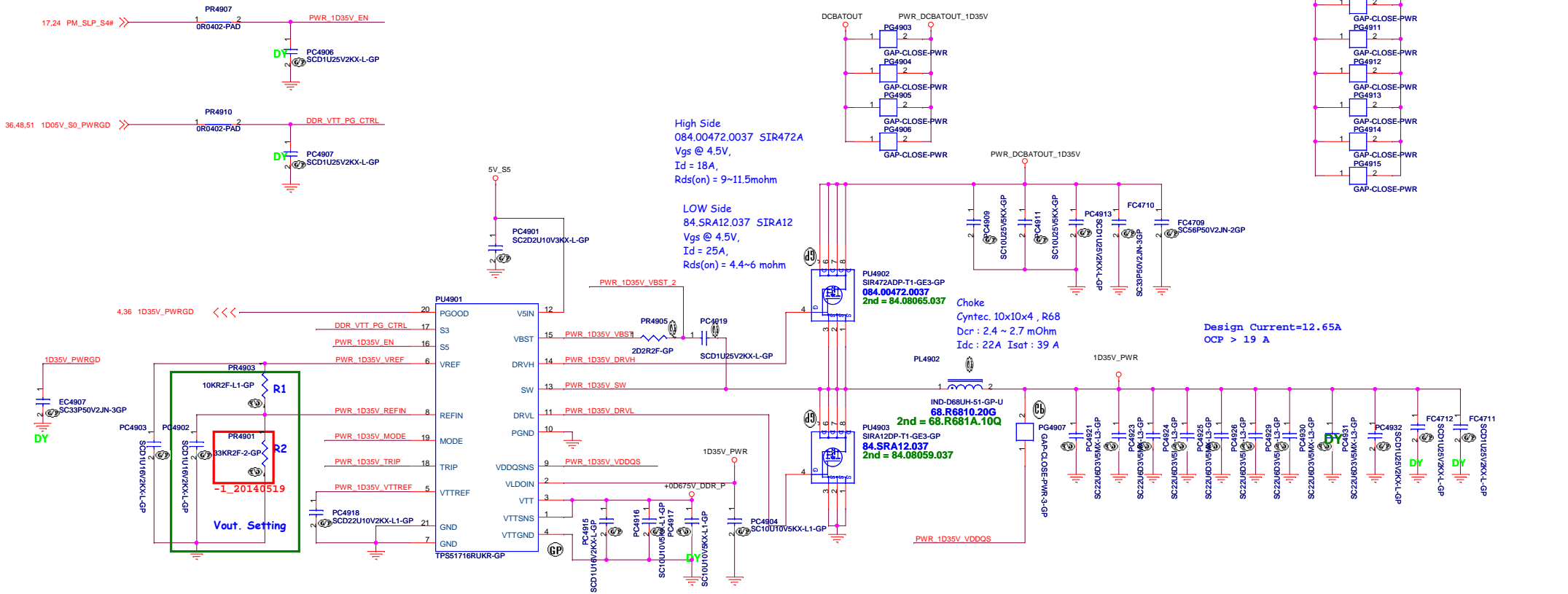
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Size A3 Document Number **Poseidon 860M** Rev **-1**

Date: Wednesday, June 18, 2014 Sheet 48 of 102

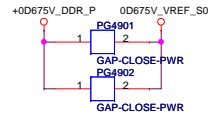
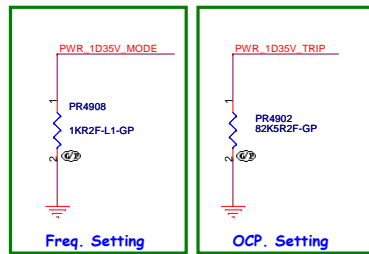


SSID = PWR.Plane.Regulator 1p35v0p675v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

PR4908	Frequency	Discharge Mode
33k ohm	500kHz	Non-tracking Discharge
22k ohm	670kHz	Non-tracking Discharge
12k ohm	670kHz	Tracking Discharge
1k ohm	500kHz	Tracking Discharge



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Title: **TPS51716 (VDDQ VTT)**

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Date: Wednesday, June 18, 2014	Sheet 49 of	102

5 4 3 2 1

D

D

C

C

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A

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EV

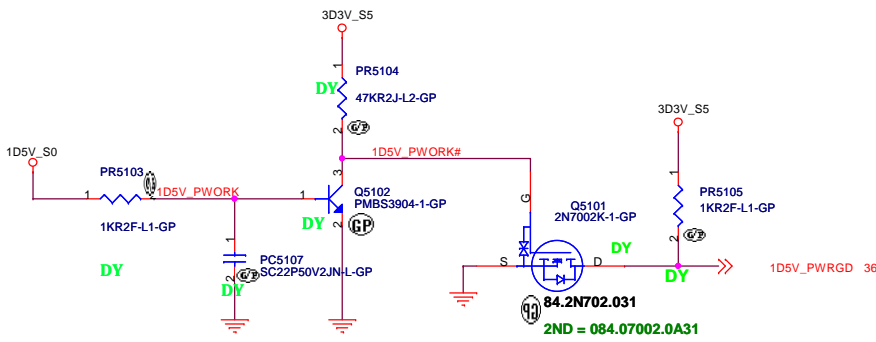
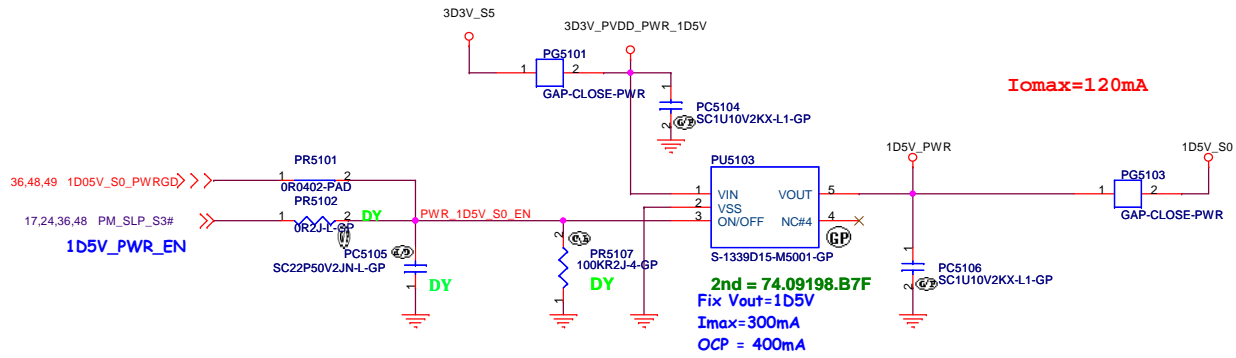
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Title		
1D8V_S0_TLV62065		
Size	Document Number	Rev
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Date:	Tuesday, June 17, 2014	Sheet 50 of 102

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5 4 3 2 1

TLV70215 for 1D5V_S0
Enable=1.5V
Disable=0.4V

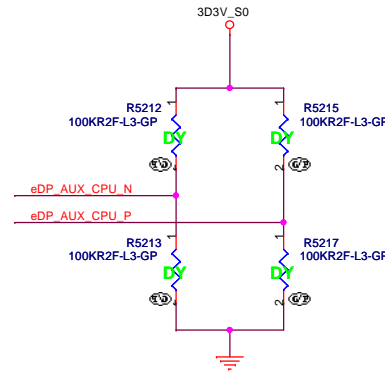
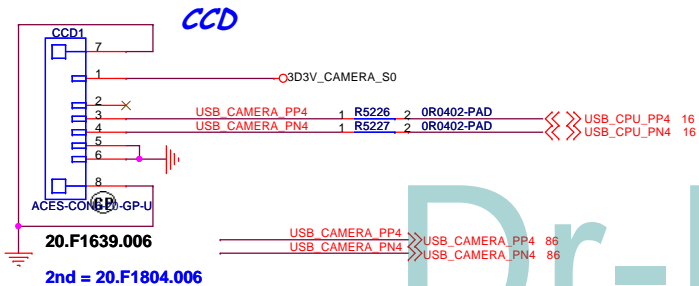
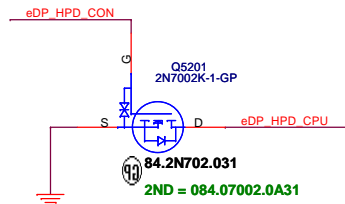
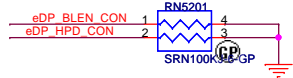
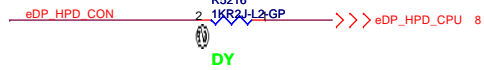
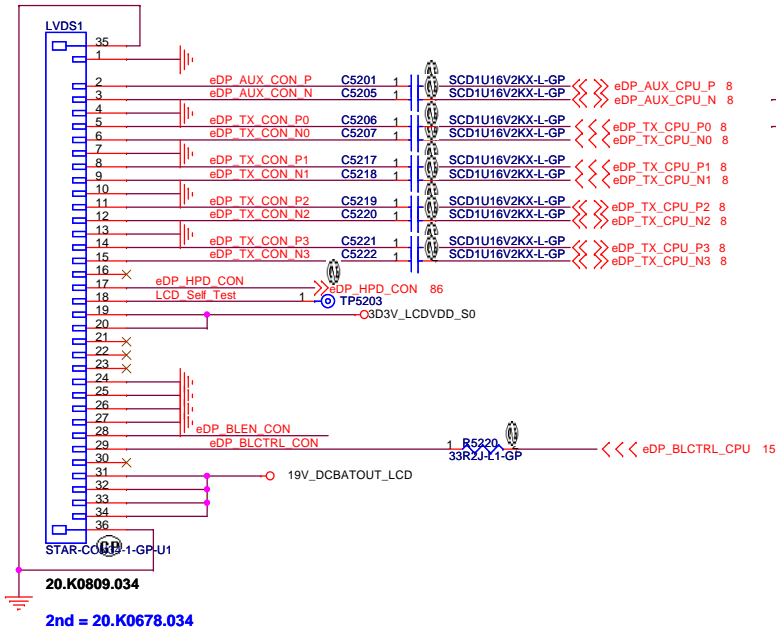


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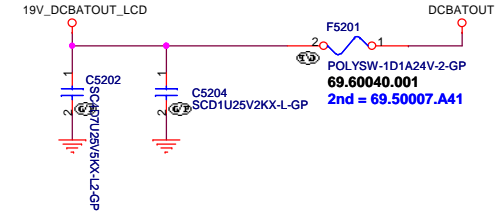
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<p>Title 1D5V_S0 TLV70215</p>		
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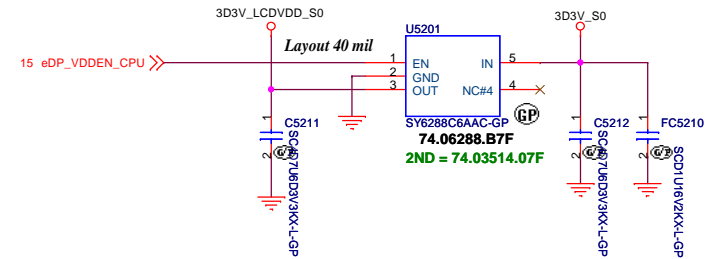
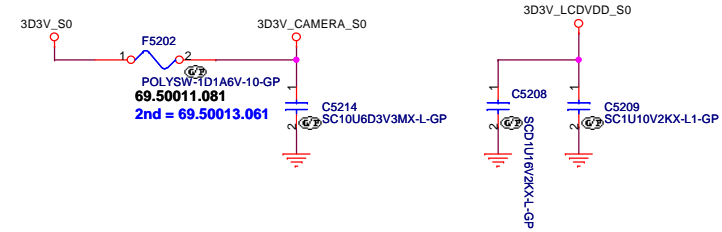
SSID = VIDEO



INVERTER POWER



Camera Power



- >>> eDP_AUX_CON_P >>> eDP_AUX_CON_P 86
- >>> eDP_AUX_CON_N >>> eDP_AUX_CON_N 86
- >>> eDP_TX_CON_P0 >>> eDP_TX_CON_P0 86
- >>> eDP_TX_CON_N0 >>> eDP_TX_CON_N0 86
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- >>> eDP_BLEN_CON 86
- >>> eDP_BLCtrl_CON 86

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Title LCD Connector	
Size A3	Document Number Poseidon 860M
Date: Tuesday, June 17, 2014	Rev -1
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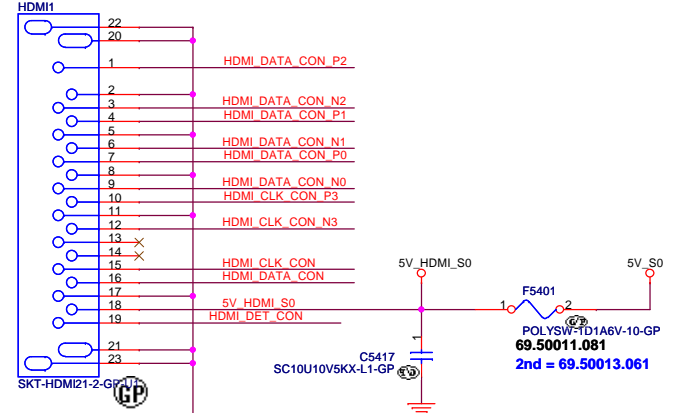
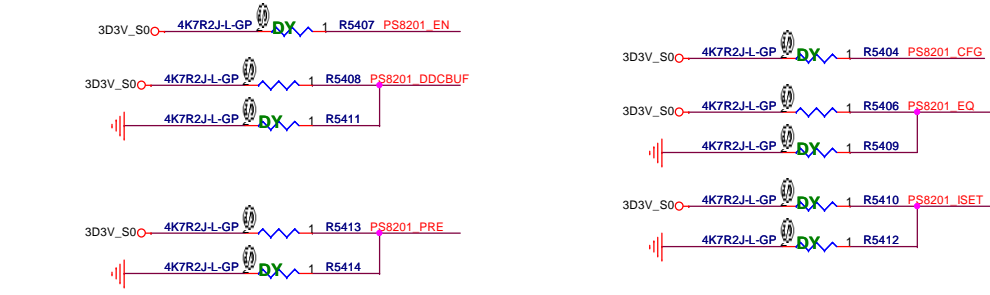
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Title			
CRT Board Connector (Reserved)			
Size	Document Number		Rev
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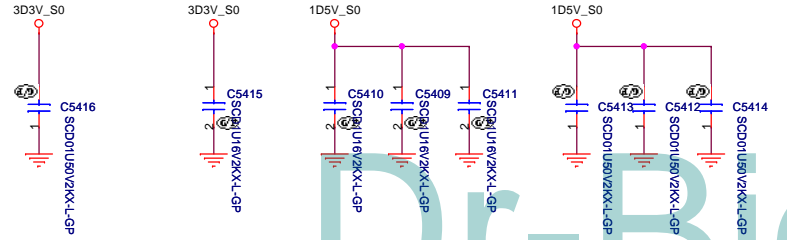
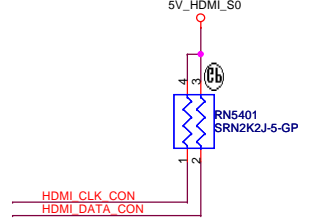
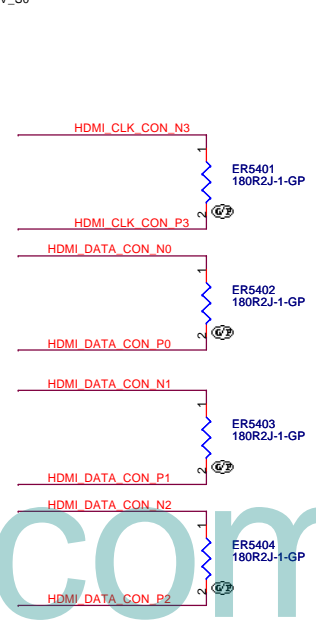
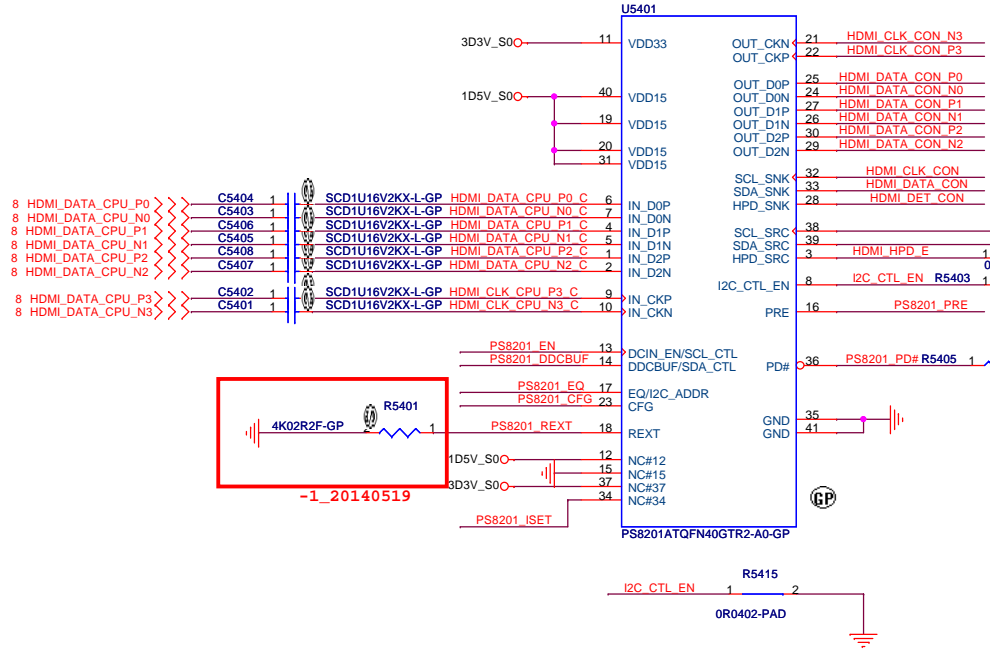
SSID = VIDEO

HDMI Level Shifter & CONNECTOR

HDMI CONN



22.10296.661
2nd = 22.10296.A71



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Title: **HDMI Level Shifter/Connector**

Size A3 Document Number: **Poseidon 860M** Rev: **-1**

Date: Tuesday, June 17, 2014 Sheet 54 of 102

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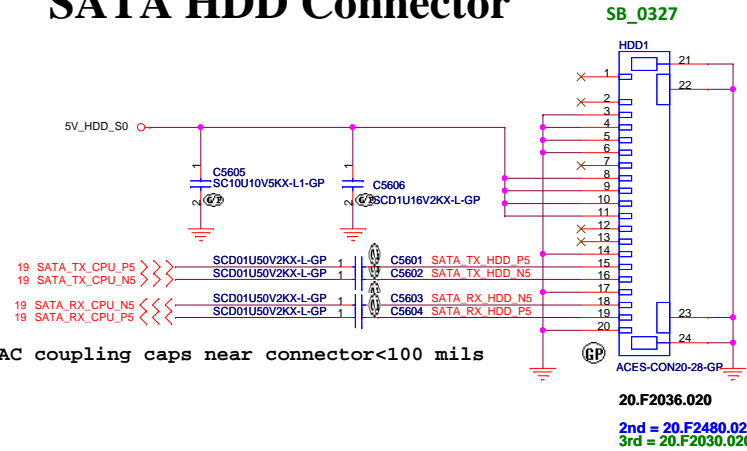
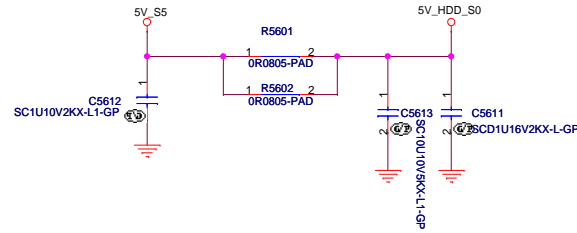
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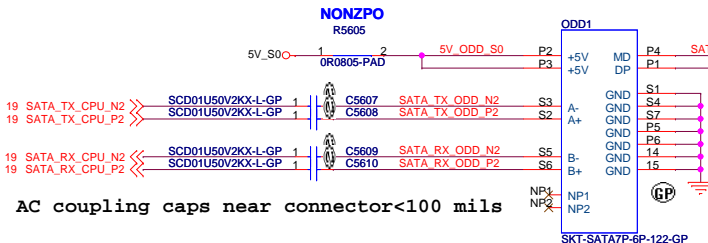
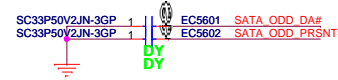
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Title			
Display Port			
Size	Document Number	Rev	
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SSID = SATA

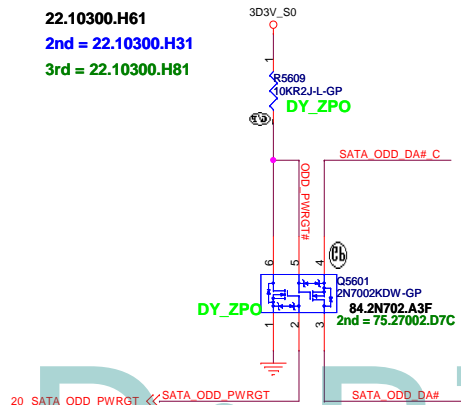
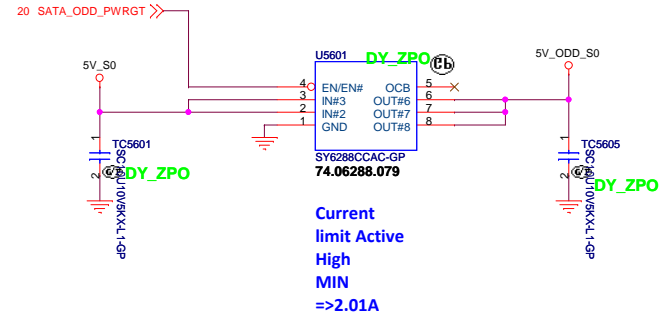
SATA HDD Connector



ODD Connector



SATA Zero Power ODD



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EV		Title	
Size		HDD / ODD / NGFF SSD	
Custom	Document Number	Poseidon 860M	
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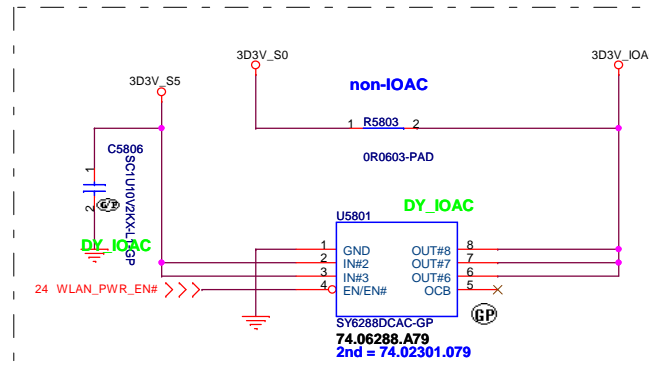
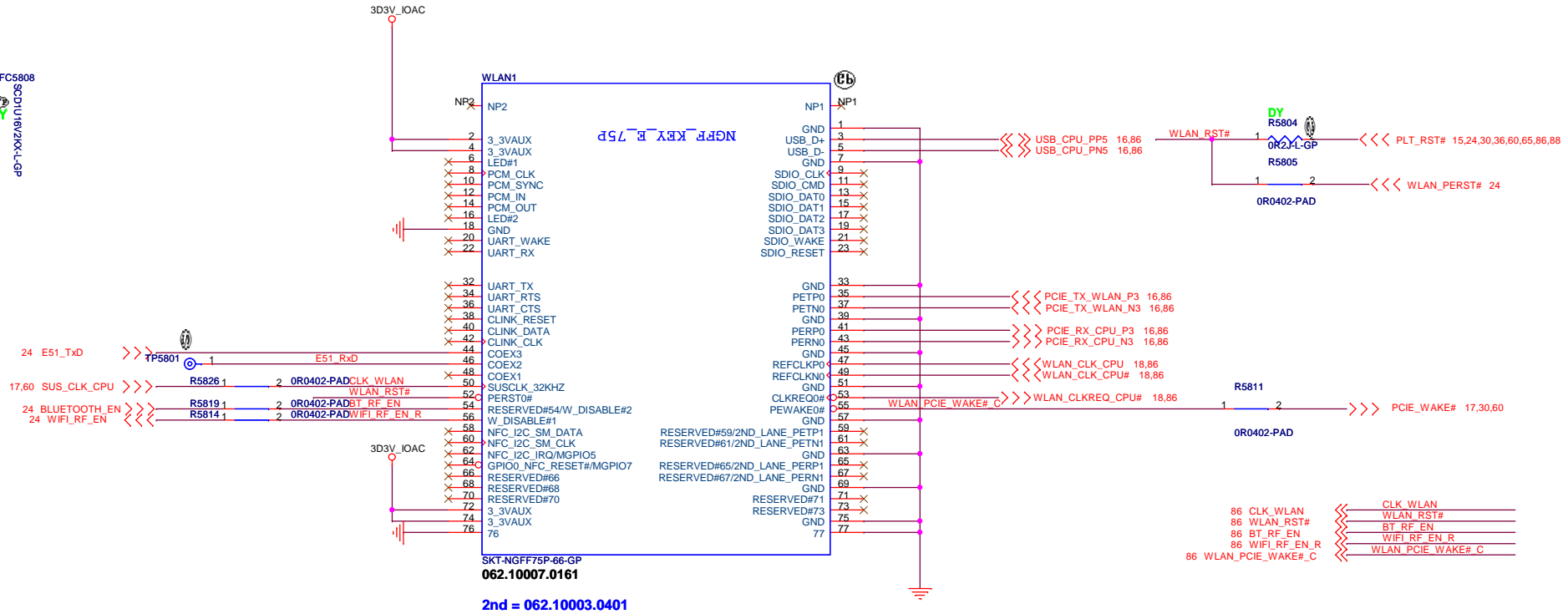
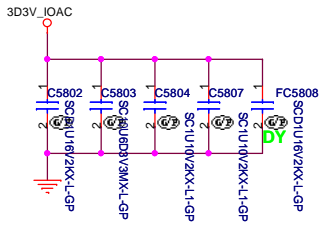
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Title			
E-SATA			
Size	Document Number		Rev
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SSID = Wireless Mini Card Connector(802.11a/b/g/n)



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MINICARD(WLAN)	
Size A3	Document Number
Poseidon 860M	
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Rev	-1

SSID = Wireless

Mini Card Connector(mSATA)

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Title

WWAN CONN

Size

A4

Document Number

Poseidon 860M

Rev

-1

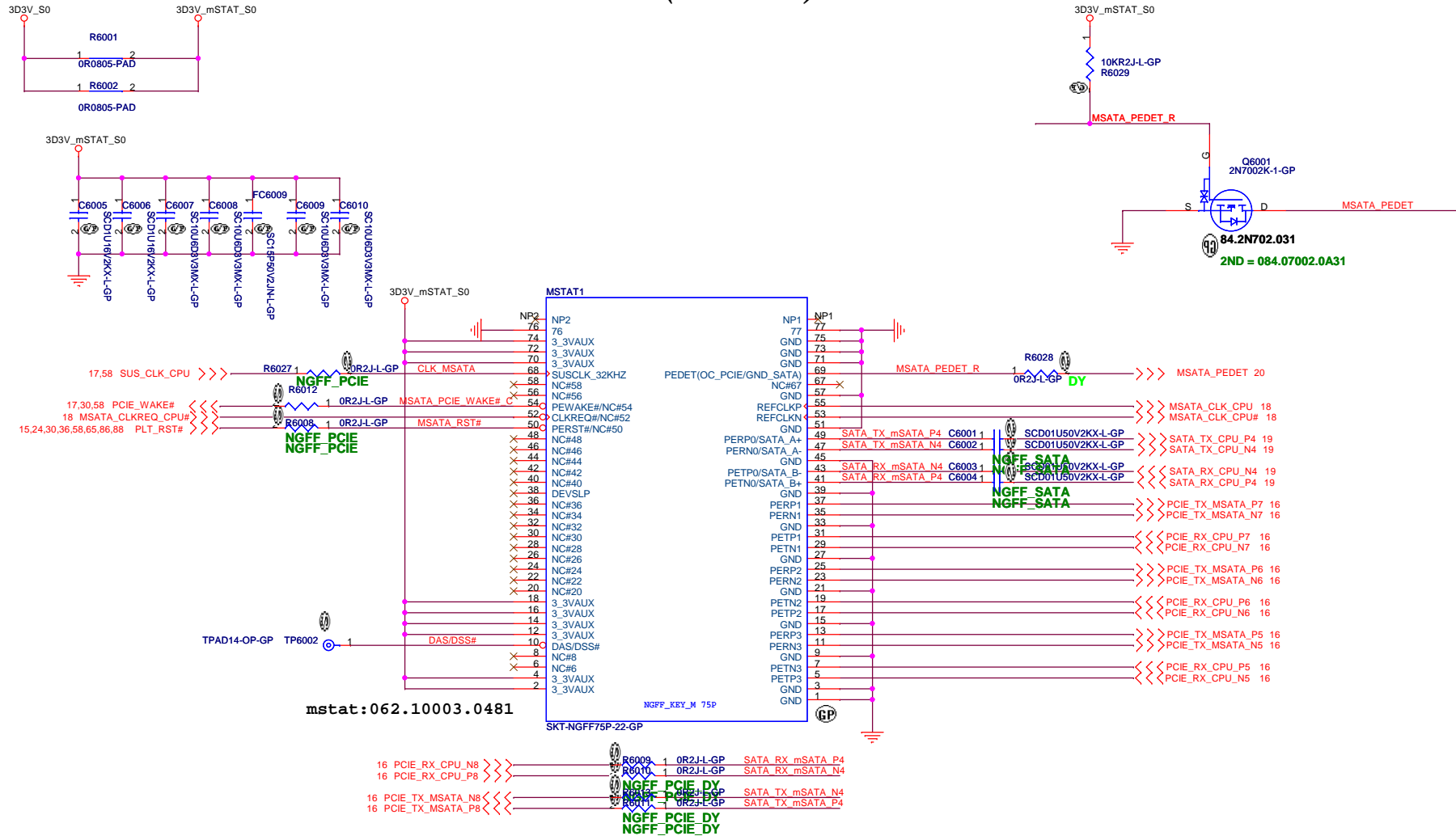
Date: Tuesday, June 17, 2014

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SSID = mSATA

Mini Card Connector(mSATA)




SATA/PCIe Gen 2 and Gen 3 Capacitor Values

Condition	PCIe Only	SATA Only	PCIe/SATA
PCH Tx	100 nF	10 nF	100 nF
PCH Rx	None	10 nF ²	None ³

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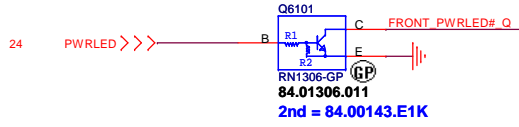
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mSATA Connector		
Size A3	Document Number	Rev
Date: Tuesday, June 17, 2014	Poseidon 860M	-1
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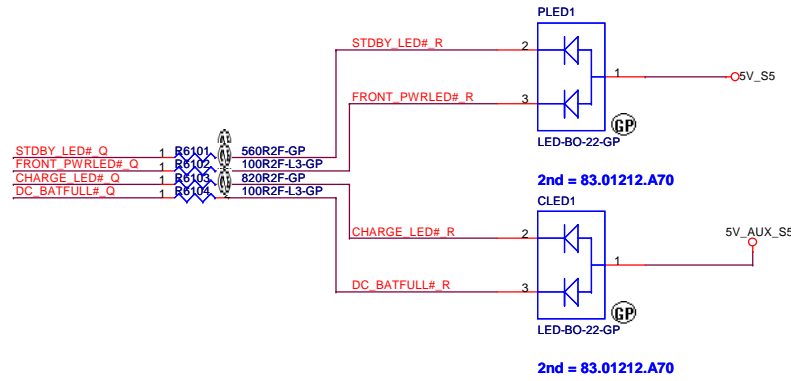
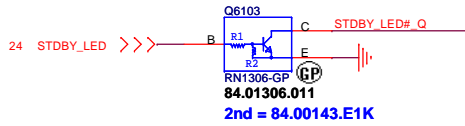
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SSID = User.Interface

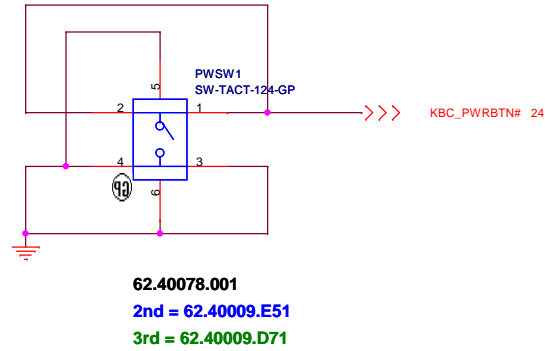
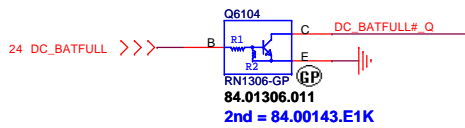
Power button LED



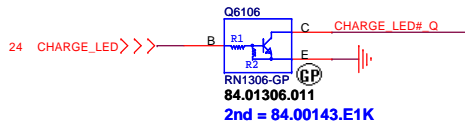
Power STDBY_LED



Battery LED2(DC_BATFULL)



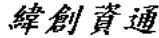
Battery LED1(CHARGE)



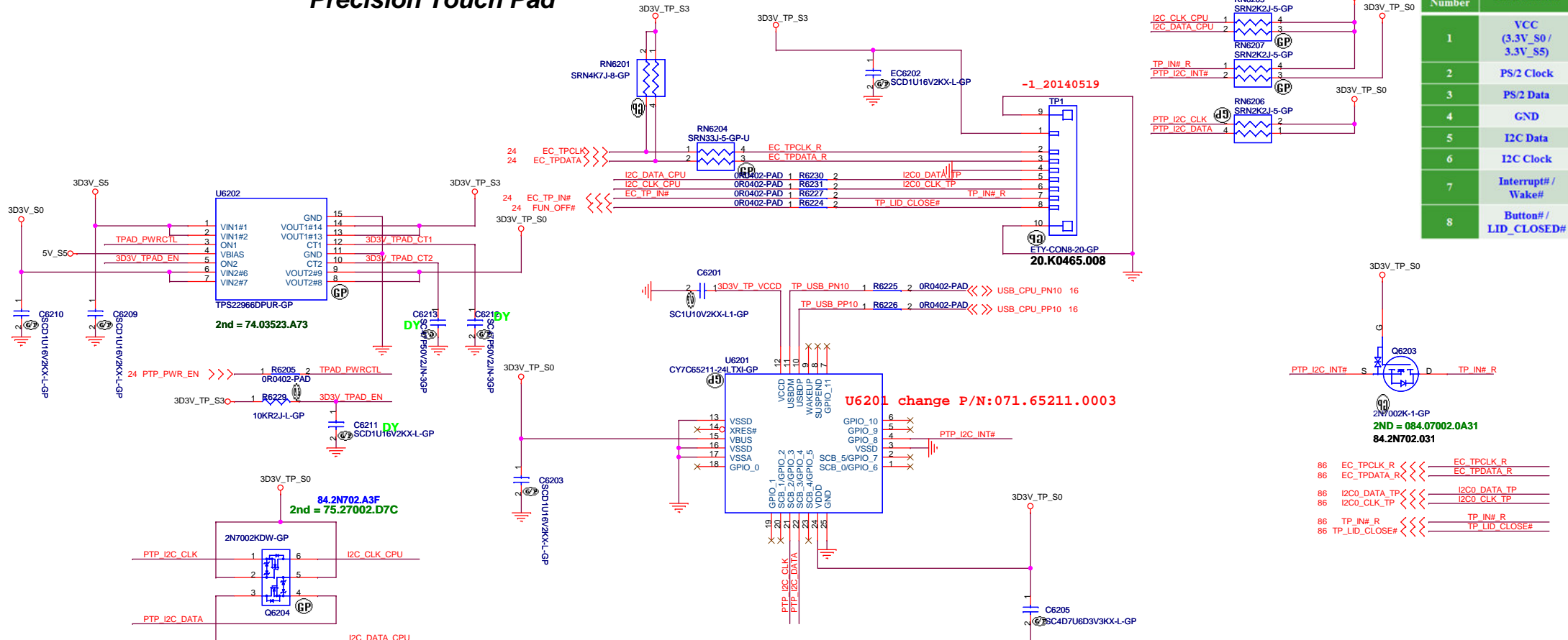
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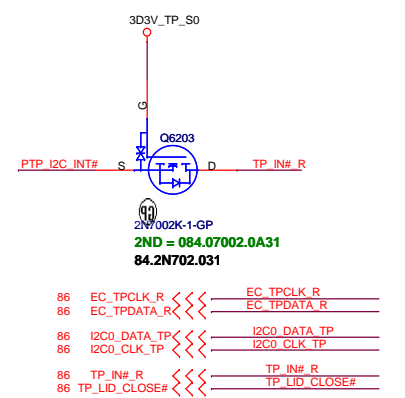
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LED Bard/Power Button		
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Precision Touch Pad

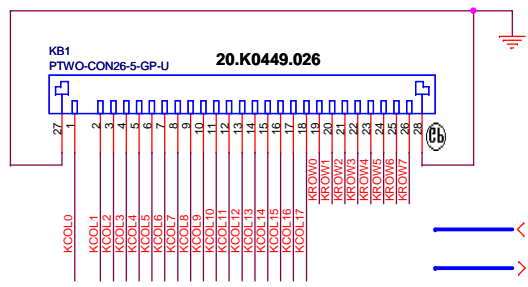


Pin Number	Pin Definition
1	VCC (3.3V_S0 / 3.3V_S5)
2	PS/2 Clock
3	PS/2 Data
4	GND
5	I2C Data
6	I2C Clock
7	Interrupt# / Wake#
8	Button# / LID_CLOSED#

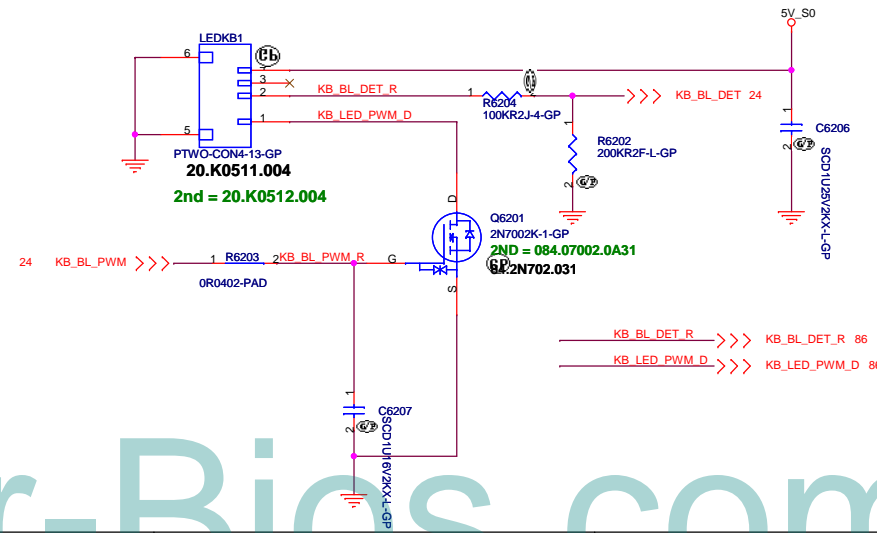


- 86 EC_TPCLK_R <<< EC_TPCLK_R
- 86 EC_TPDATA_R <<< EC_TPDATA_R
- 86 I2C0_DATA_TP <<< I2C0_DATA_TP
- 86 I2C0_CLK_TP <<< I2C0_CLK_TP
- 86 TP_IN#_R <<< TP_IN#_R
- 86 TP_LID_CLOSE# <<< TP_LID_CLOSE#

Internal Keyboard Connector



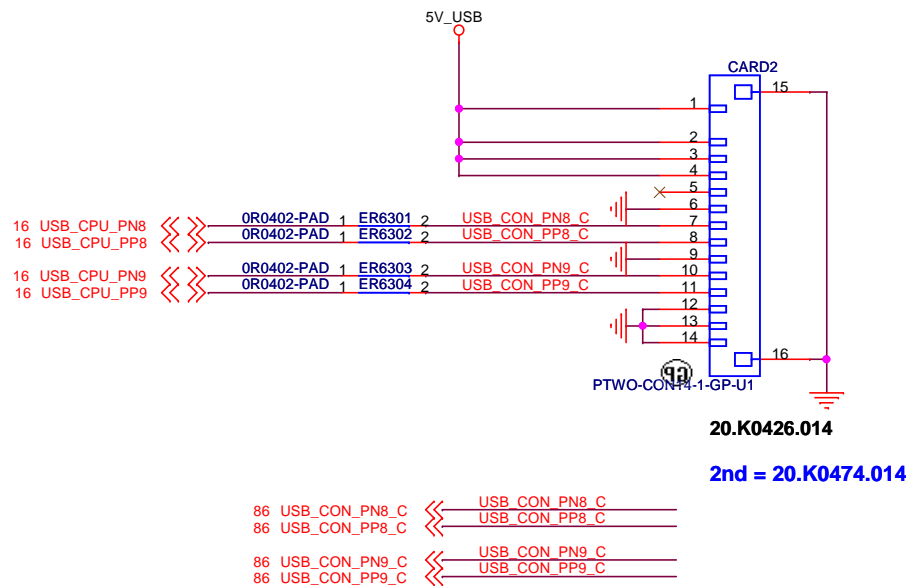
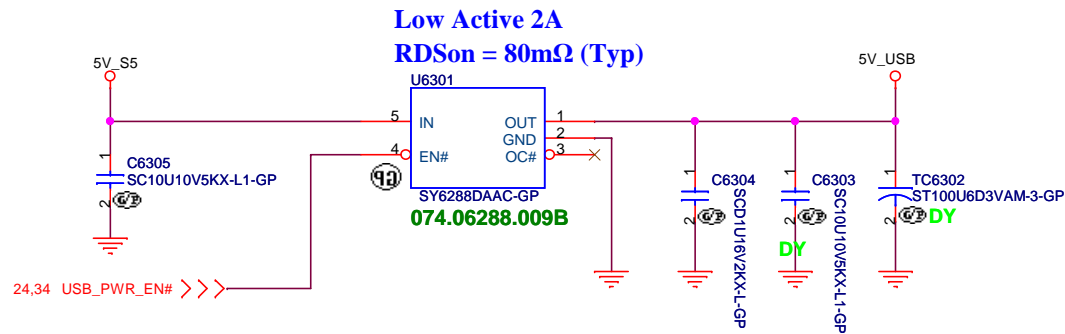
MB PIN DEFINE 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
 KB PIN DEFINE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26



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Key Board/Touch Pad			
Title	Document Number	Rev	
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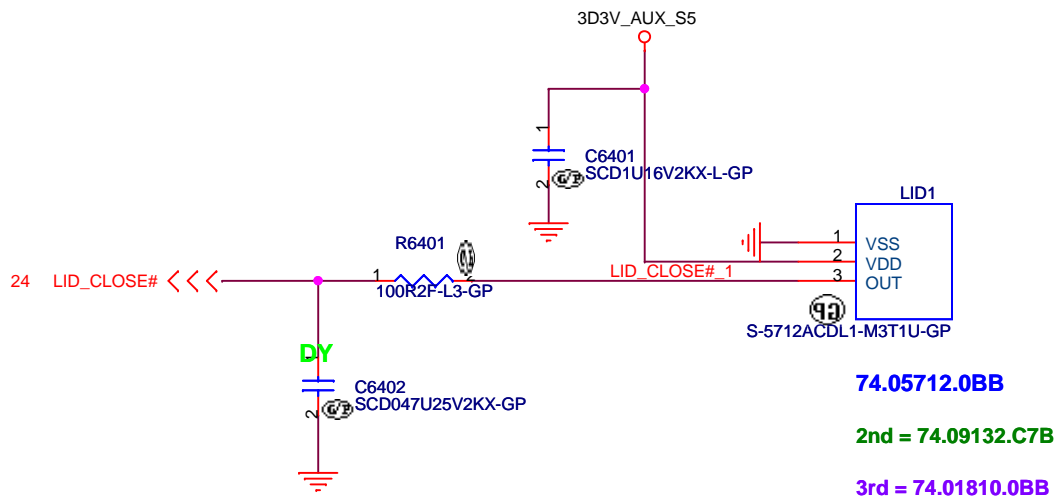


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IO Board Connector			
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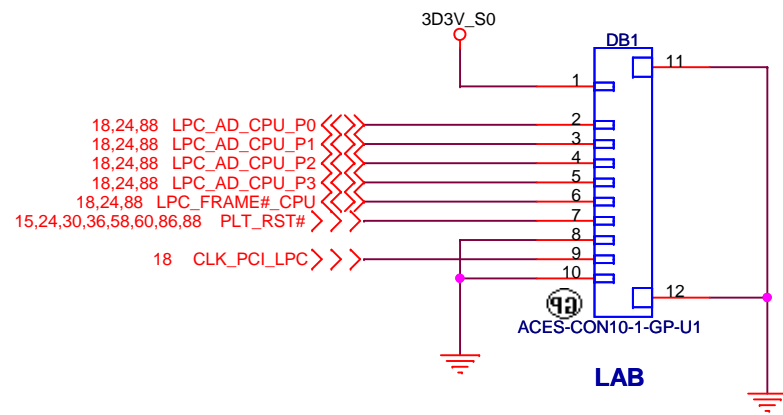
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Hall Sensor		
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Title

Dubug connector

Size

A4

Document Number

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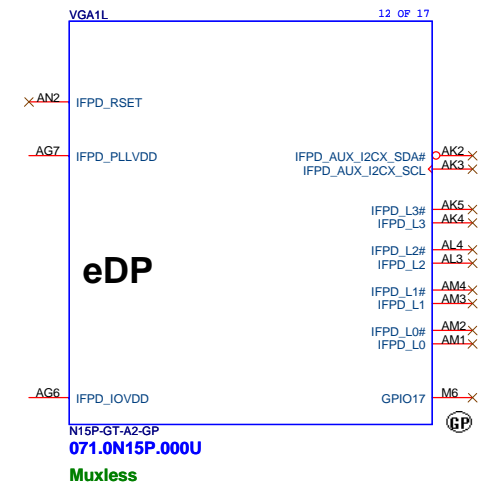
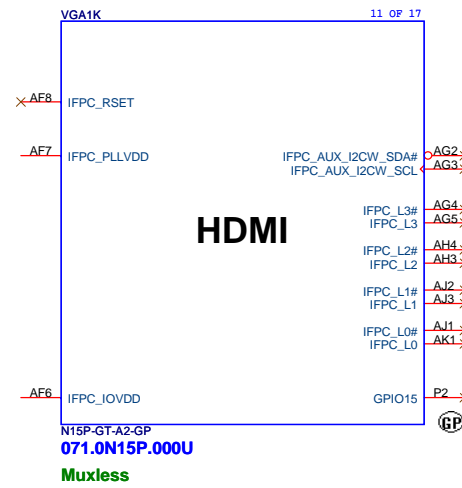
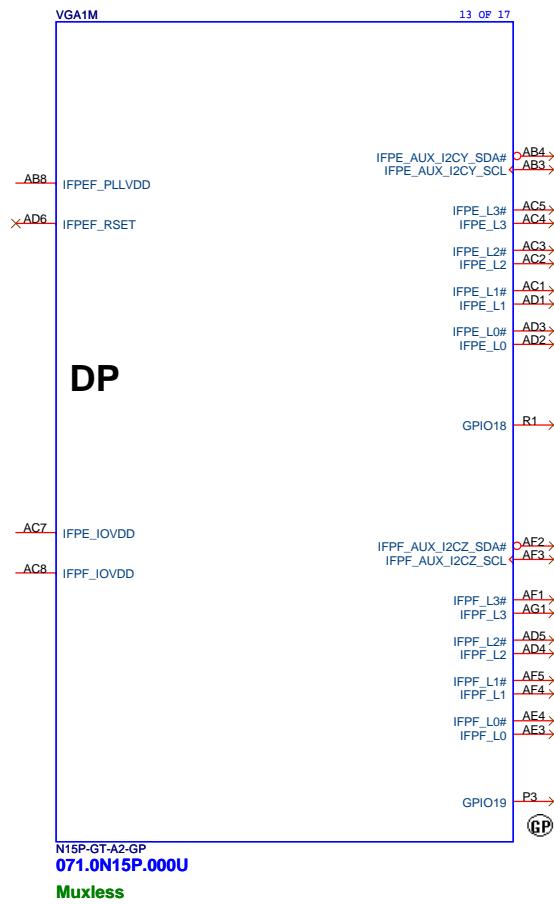
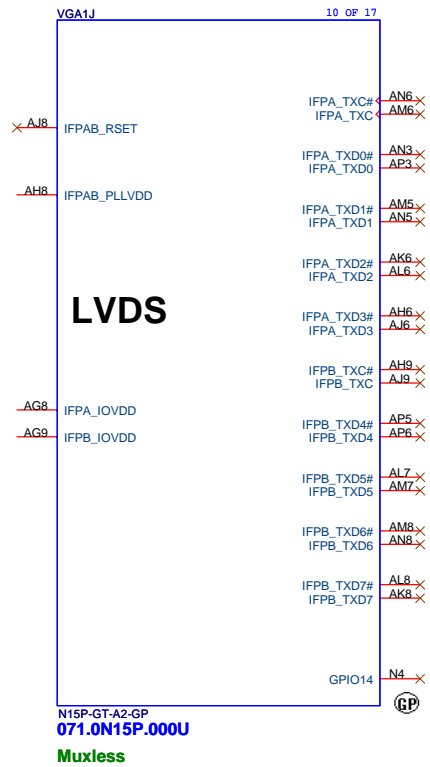
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Title		
SENSOR HUB		
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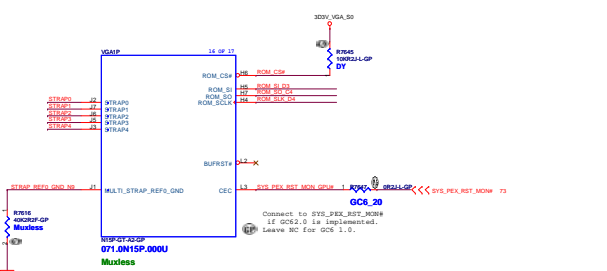
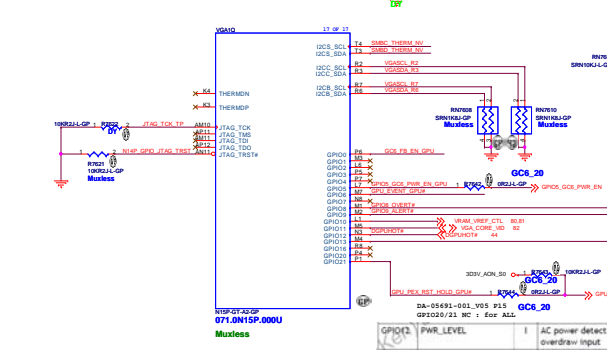
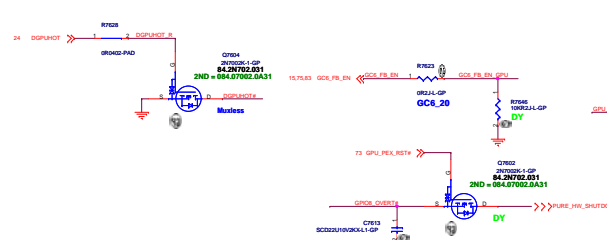
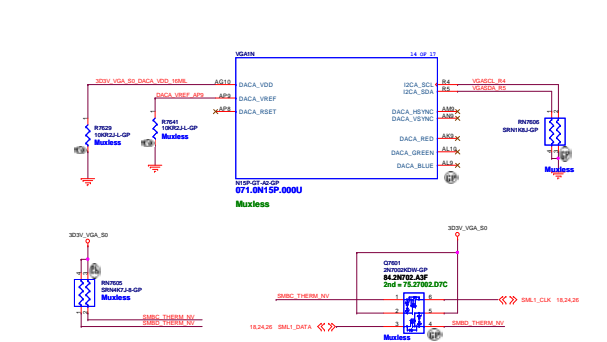


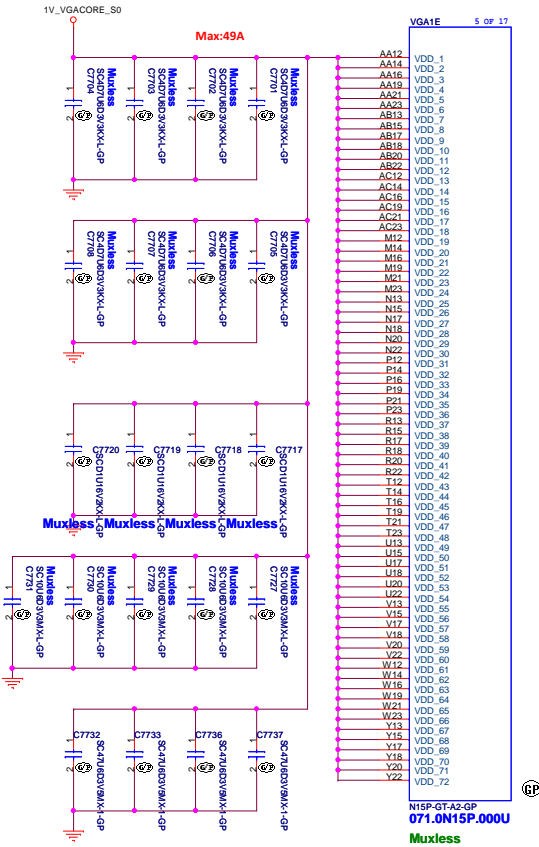
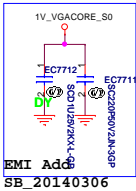
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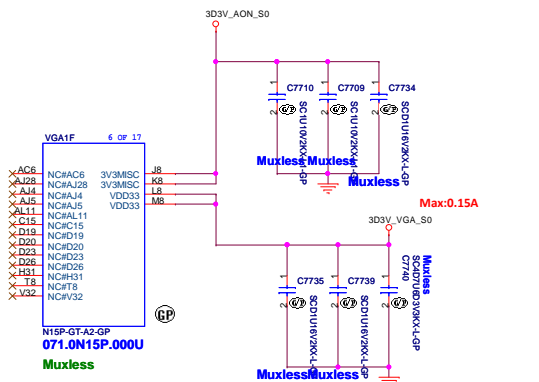
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<p>緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</p>		
<p>Title: GPU (DIGITALOUT)</p>		
Size A3	Document Number	Rev
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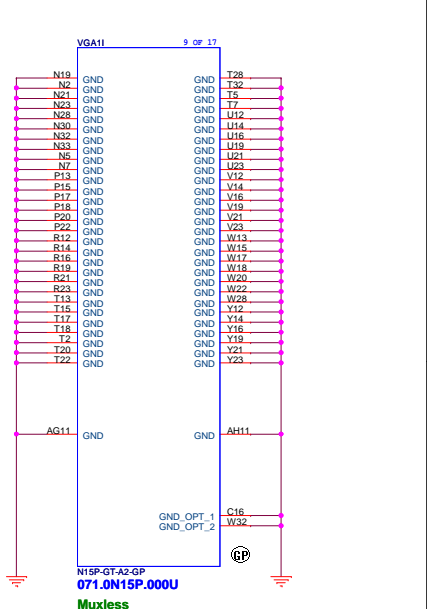
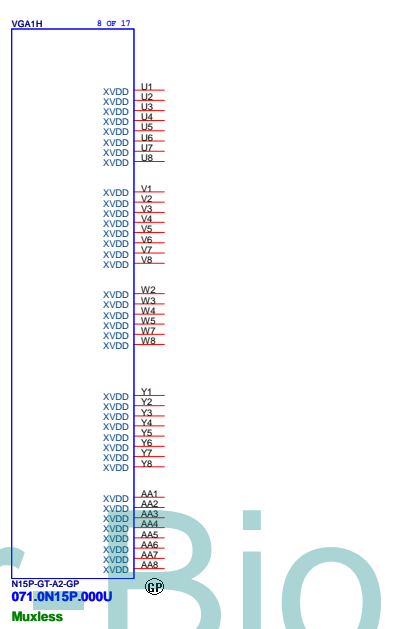
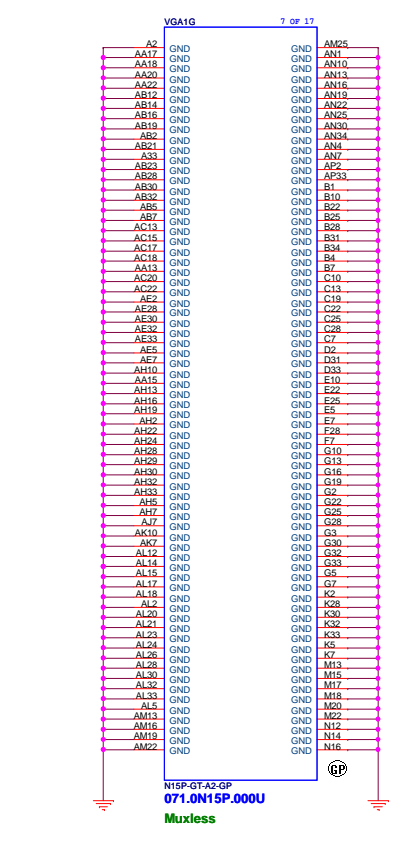




Muxless Muxless Muxless Muxless



Muxless Muxless Muxless Muxless



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Title: GPU (POWER/GND)
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TABLE
GDDR5 VIDEO MEMORY

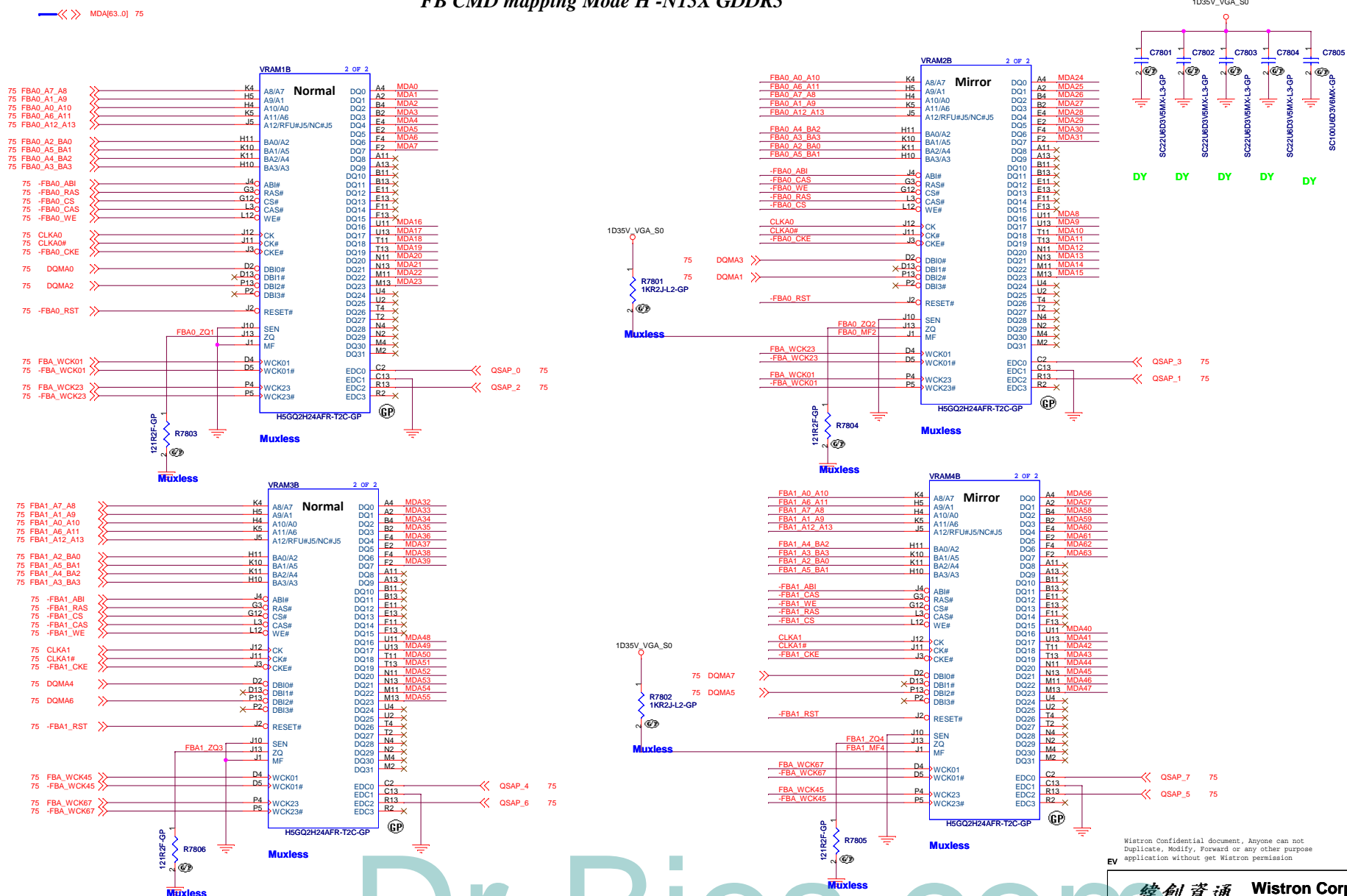
72.05224.A0U

72.20325.B0U

		HYNIX 2GBITS (64Mx32)	SAMSUNG 2GBITS (64Mx32)	HYNIX 4GBITS (128Mx32)	SAMSUNG 4GBITS (128Mx32)
U91	U92	H5GQ2H24AFR-T2C	K4G20325FD-FC04	H5GC4H24MFR (tentative)	K4G41325FC-HC03 (tentative)
U95	U96				

FB CMD mapping Mode H -N15X GDDR5

LOGIC



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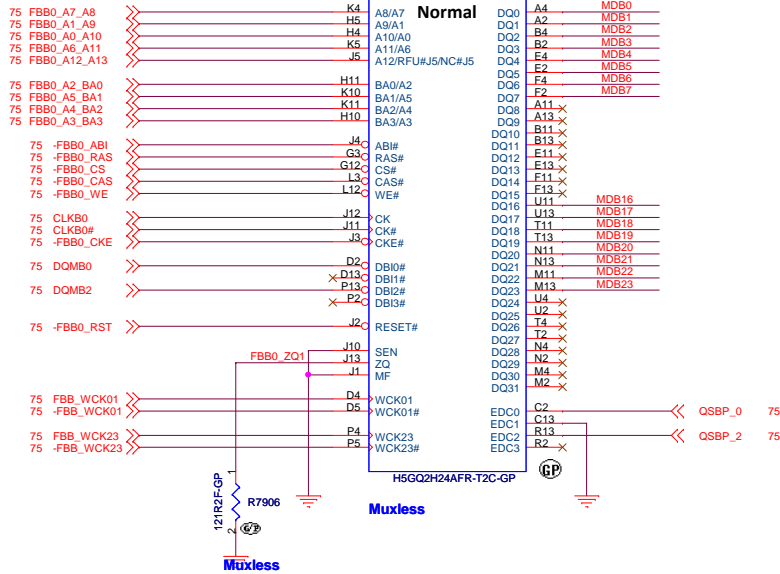
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Title		VRAM A	
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Normal



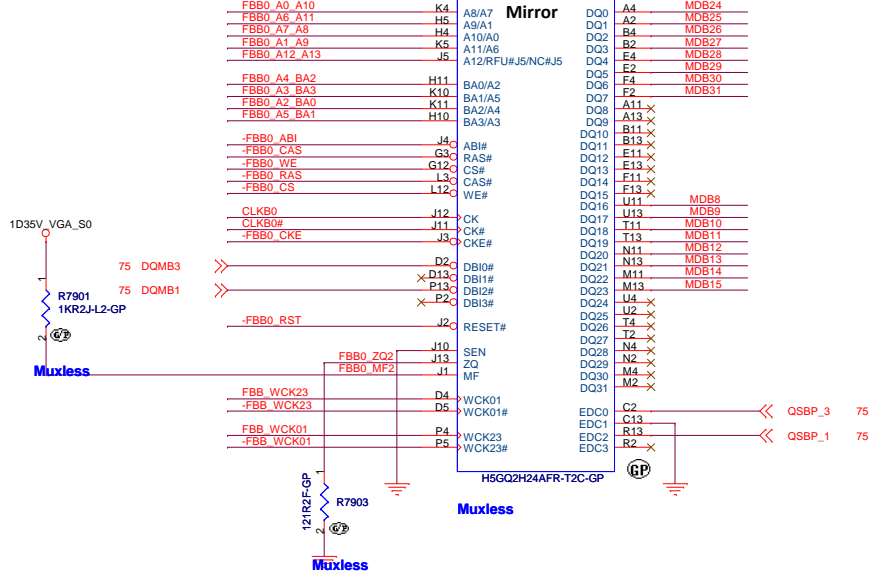
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Muxless

Muxless

VRAM6B 2 OF 2

Mirror

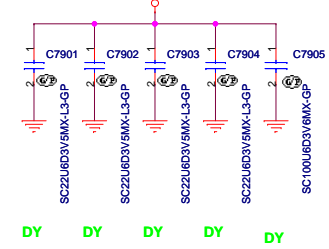


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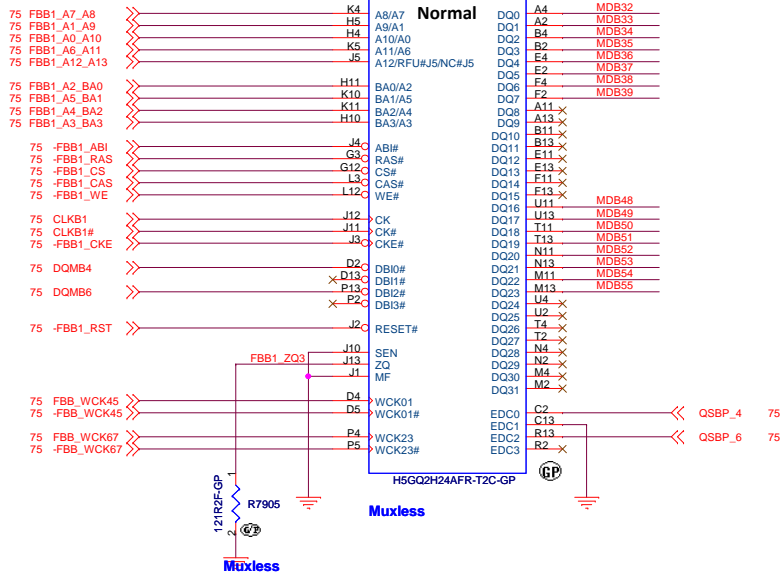
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1D35V_VGA_S0



VRAM7B 2 OF 2

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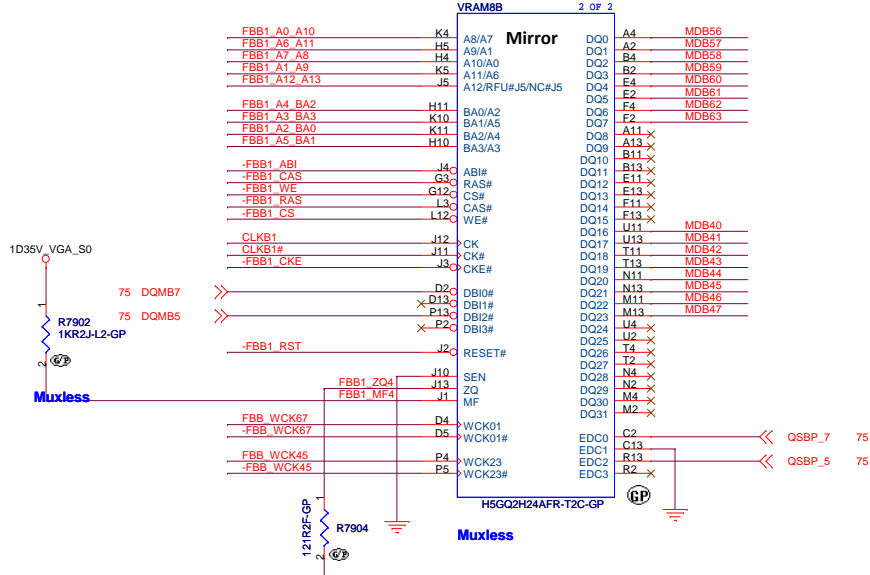
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Muxless

Muxless

VRAM8B 2 OF 2

Mirror



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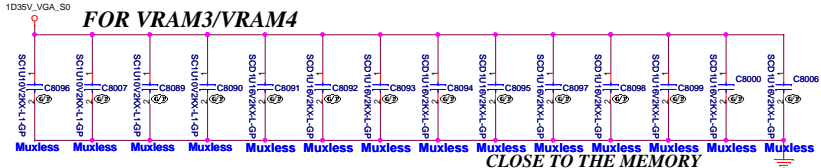
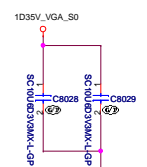
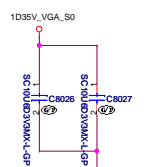
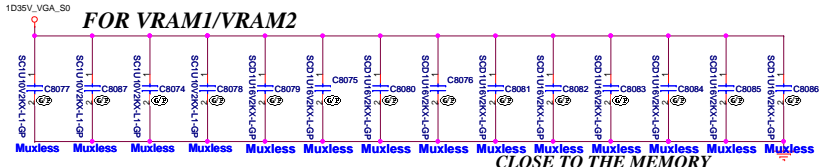
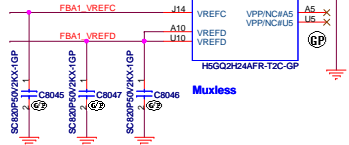
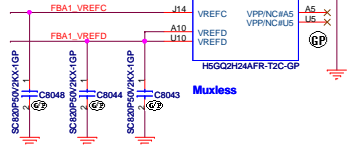
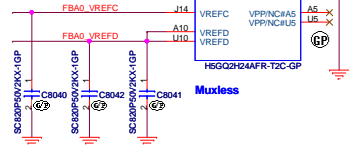
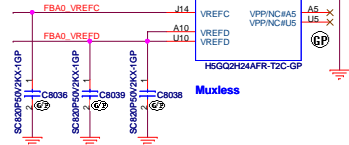
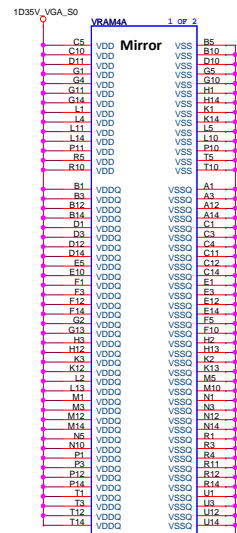
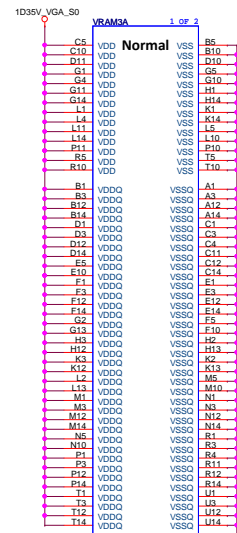
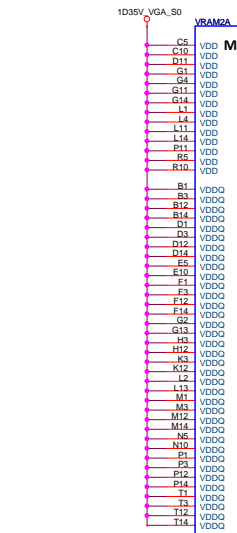
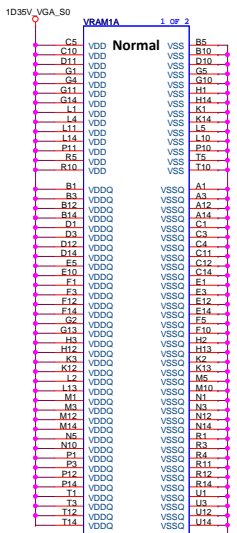
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Muxless

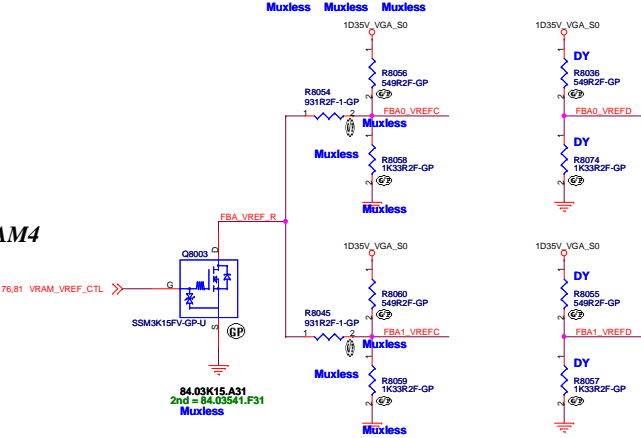
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Title		
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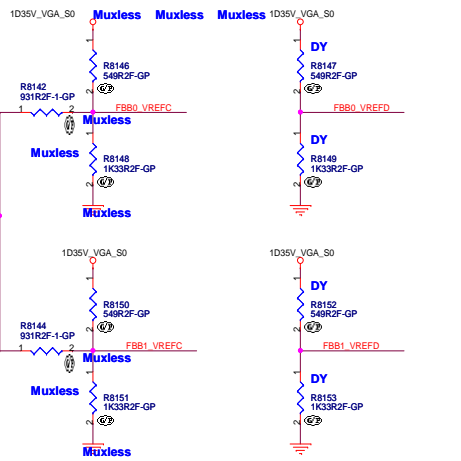
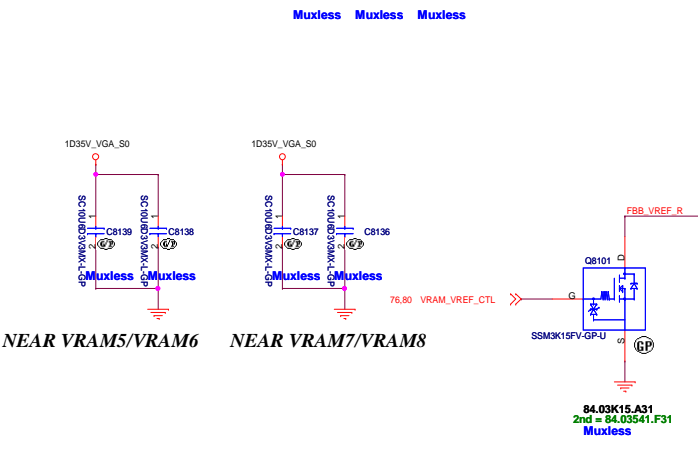
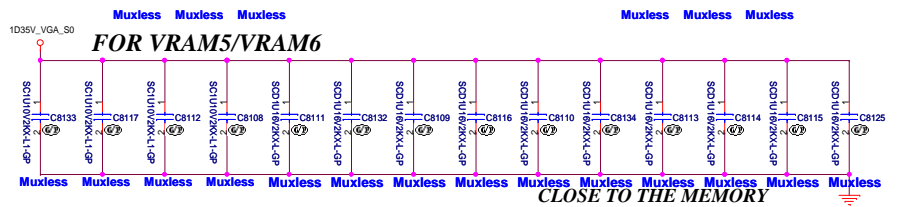
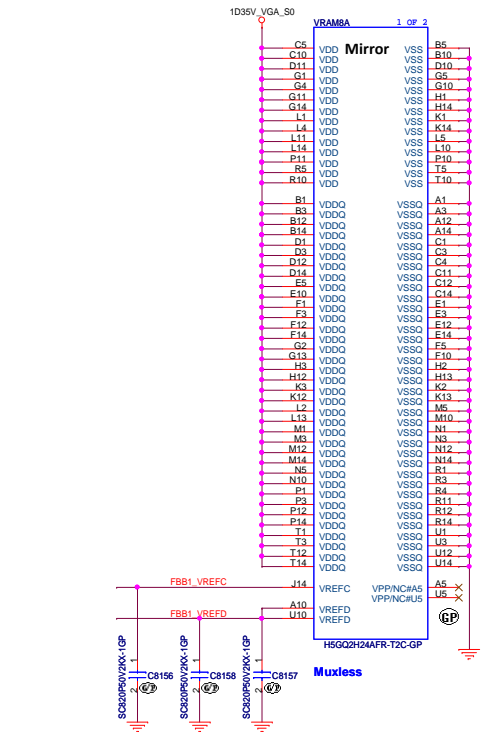
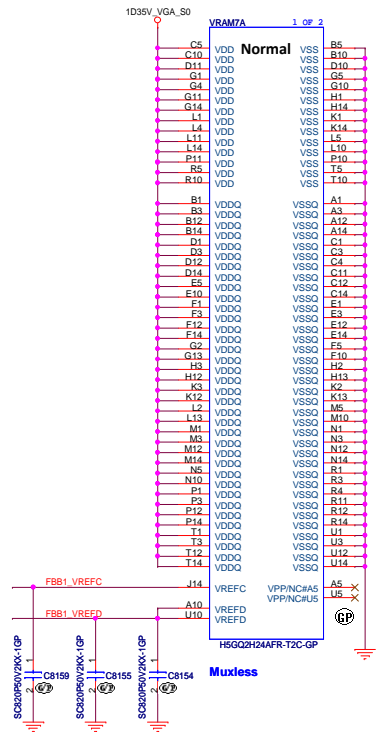
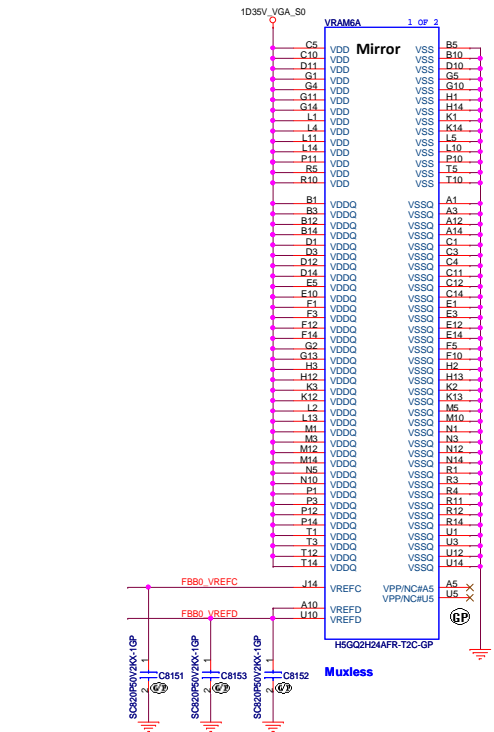
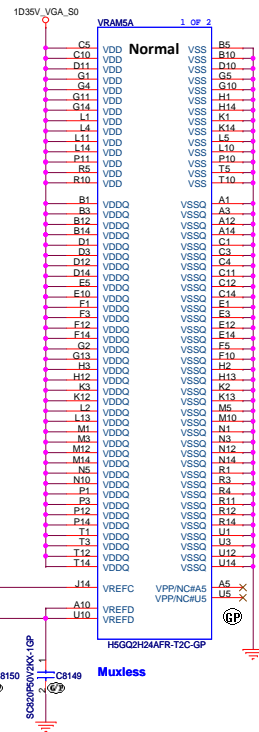


FOR VRAM1/VRAM2 FOR VRAM3/VRAM4



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VGA POWER A			
File	Document Number		Rev
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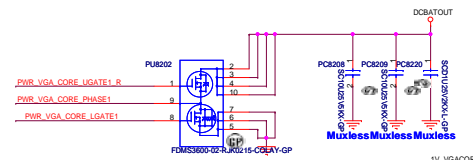
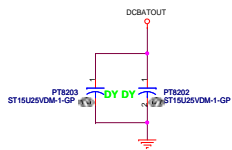
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File	VGA POWER B		Rev
Size	Document Number	Poseidon 860M	
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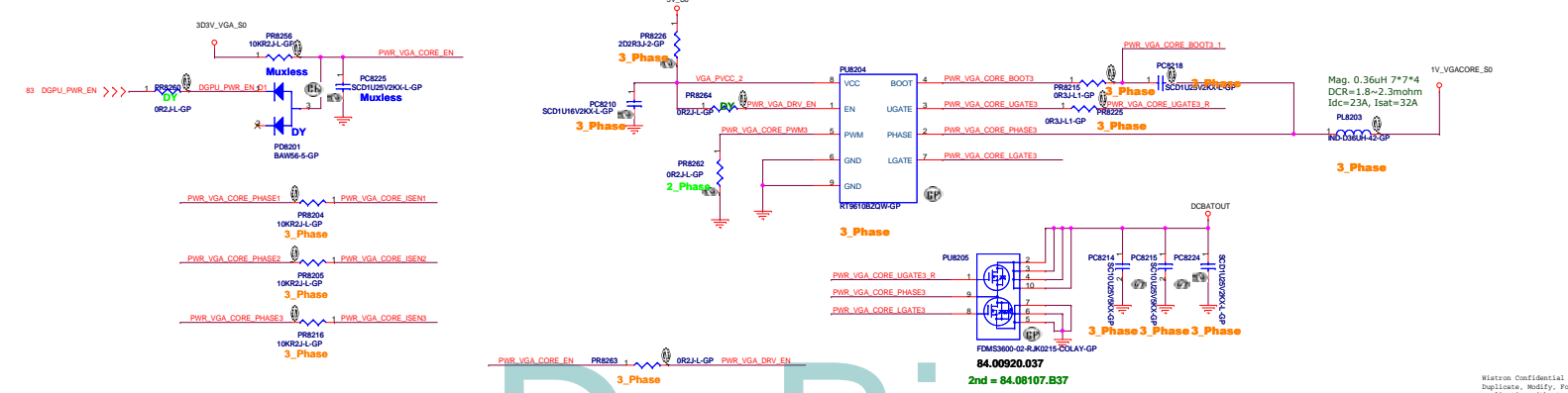
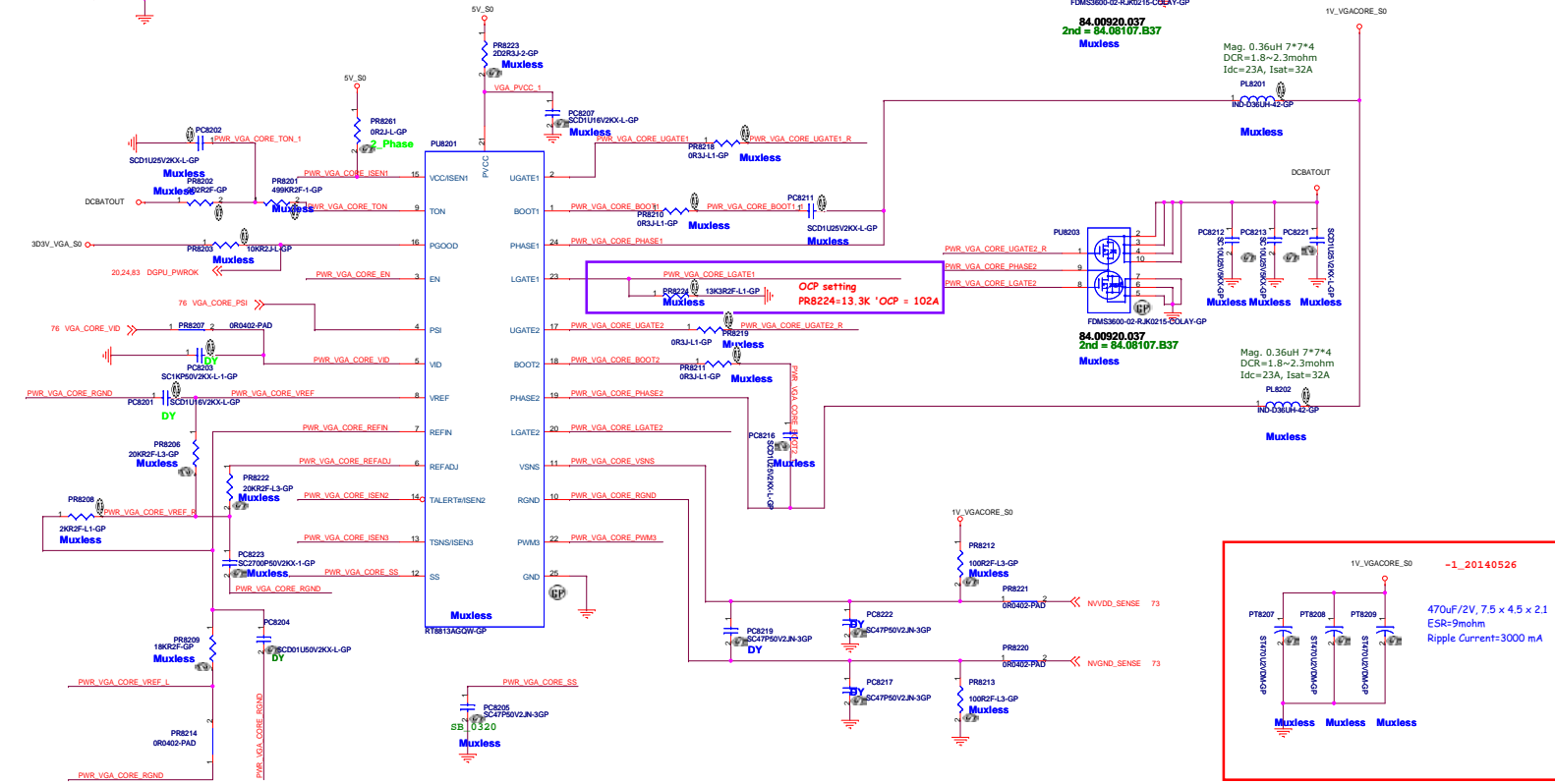
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VGA : N15P GX
 Config : B
 EDP-Continuous : 49A
 EDP-Peak : 76A

	Config : D	Config : C	Config : B
EDP-Cont.	33.5 A	35 A	43 A
EDP-Peak	51.5 A	40.89 A	80 A
PR8222	27K ohm	39K ohm	20K ohm
PR8206	7.5K ohm	30K ohm	20K ohm
PR8208	0 ohm	3K ohm	2K ohm
PR8209	6.2K ohm	24K ohm	18K ohm
PR8214	1.74K ohm	3K ohm	0 ohm
PC8223	5.6nF	1.8nF	2.7nF



Dual NMOs
 84.00920.037
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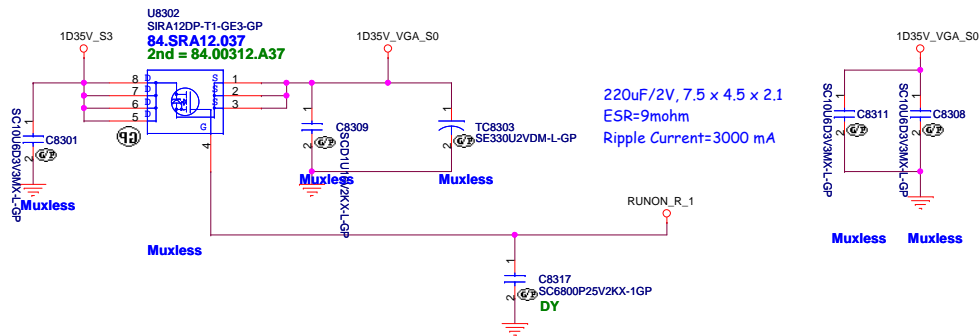
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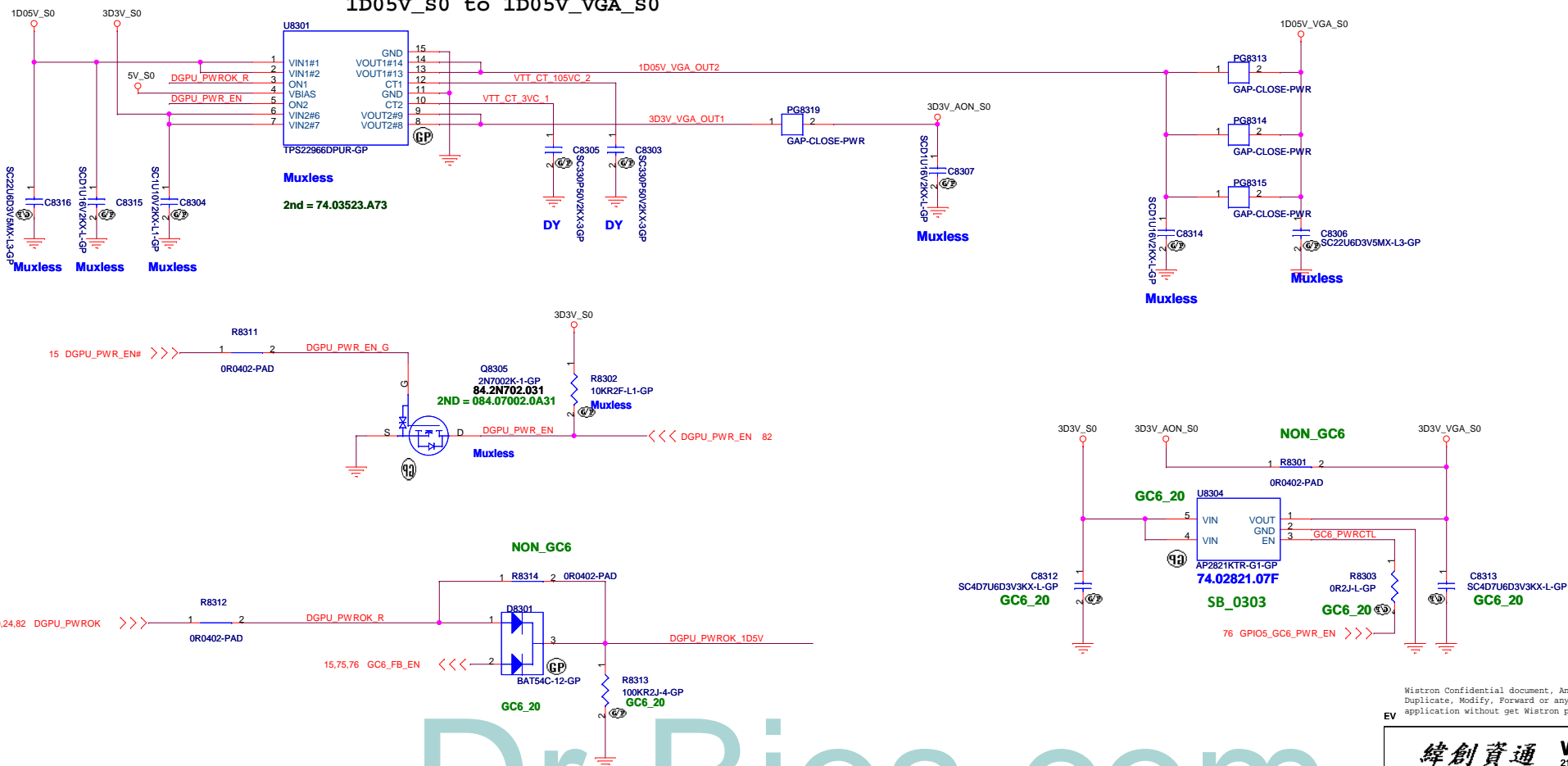
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File: RT8813A VGA CORE
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TPS22966 for VGA_1D35V(For VRAM GDDR5)



3D3V_S0 to 3D3V_VGA_S0 1D05V_S0 to 1D05V_VGA_S0



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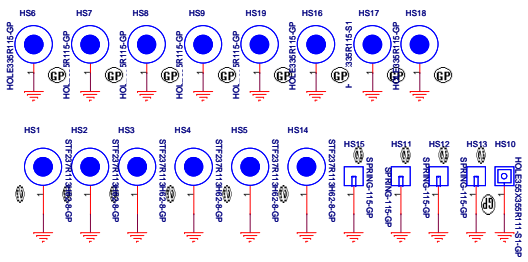
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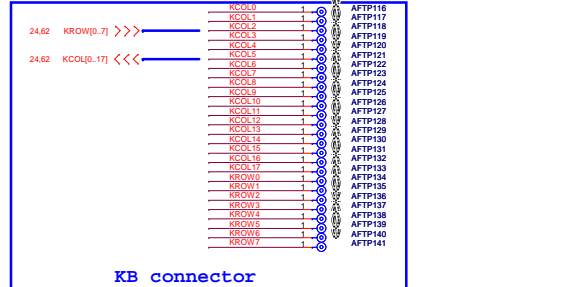
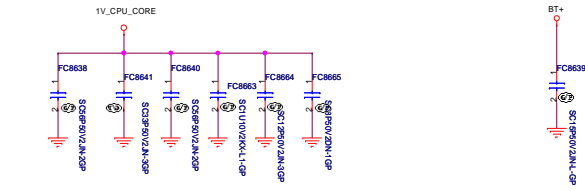
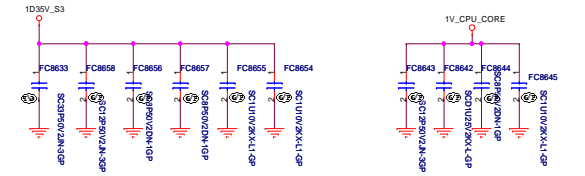
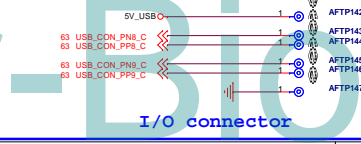
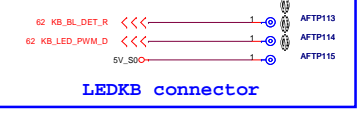
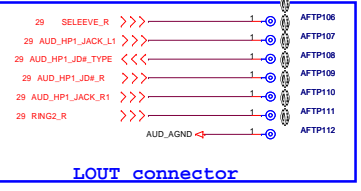
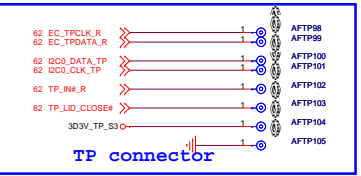
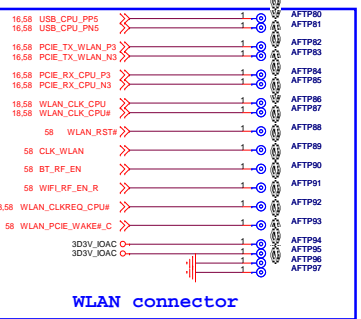
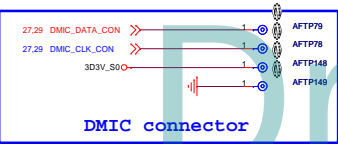
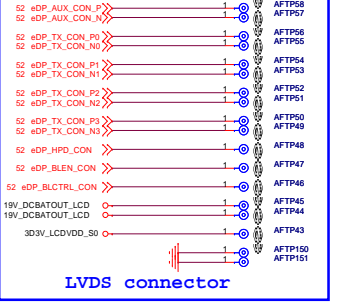
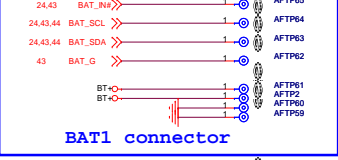
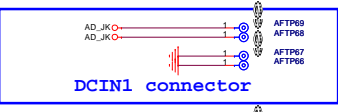
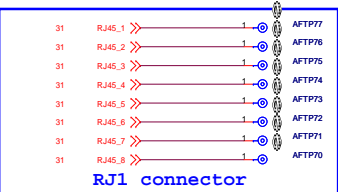
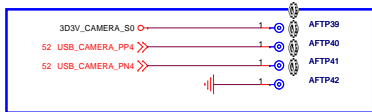
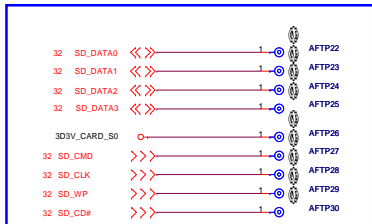
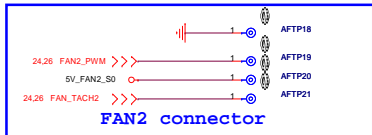
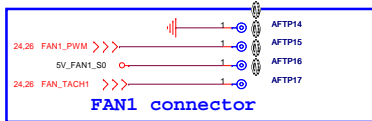
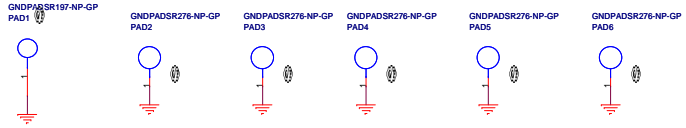
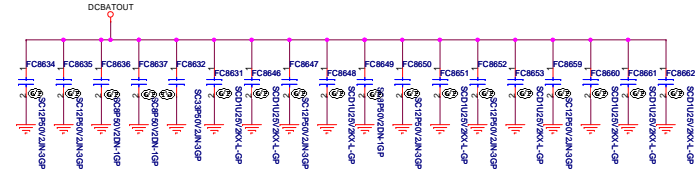
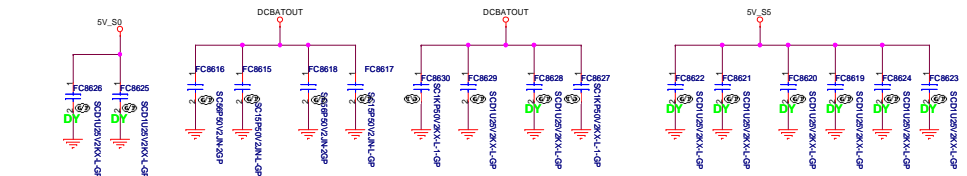
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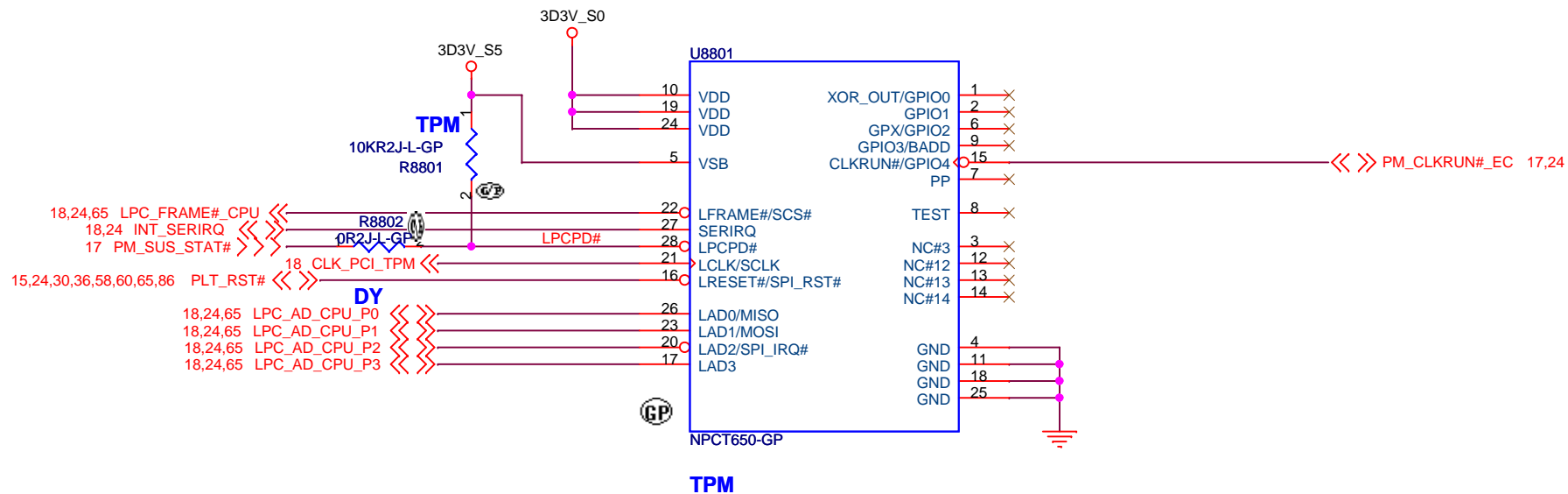


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Pin	XDP Signal Name	Target Signal	I/O	Device	Pin	XDP Signal Name	Target Signal	I/O	Device
1	OBSFN_A0	Open	I/O		2	OBSFN_A1	Open	I/O	
3	GND	GND	NA		4	OBSDATA_A[0]	Open	I/O	
5	OBSDATA_A[1]	Open	I/O		6	GND	GND	NA	
7	OBSDATA_A[2]	Open	I/O		8	OBSDATA_A[3]	Open	I/O	
9	GND	GND	NA		10	HOOK0 ¹	RSMRST#	I	System
11	HOOK1	BP_PWRGD_RST# ¹	O	System	12	HOOK2	Open	NA	
13	HOOK3	Open	NA		14	HOOK4 ¹	1.05V core	NA	
15	HOOK5	Open	NA		16	VCCOBS_AB	3.3V SUS	I	System
17	HOOK6	RSMRST# ¹	O	System	18	HOOK7	DBR# ¹	O	System
19	GND	GND	NA		20	TDO	JTAG_TDO	I	PCH
21	TRSTn	Open	NA		22	TDI	JTAG_TDI	O	PCH
23	TMS	JTAG_TMS	O	PCH	24	TCK1	Open	NA	
25	GND	GND	NA		26	TCK0	JTAG_TCK	O	PCH

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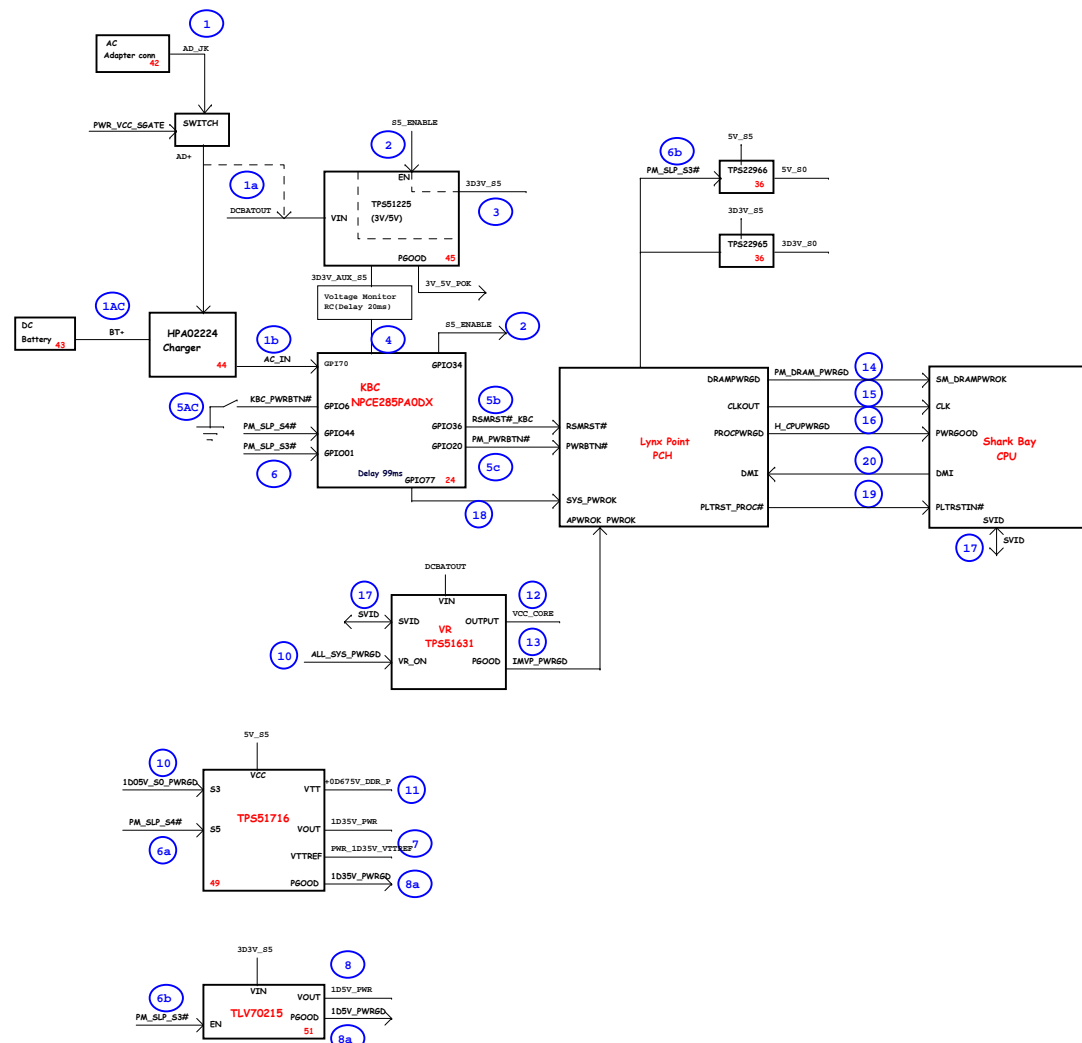
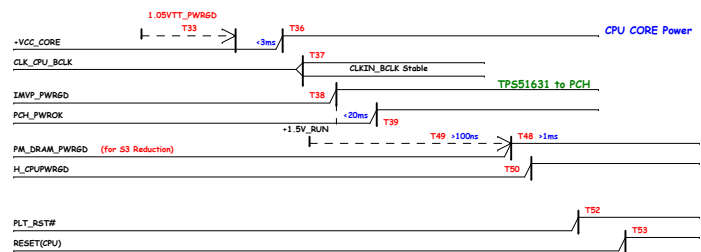
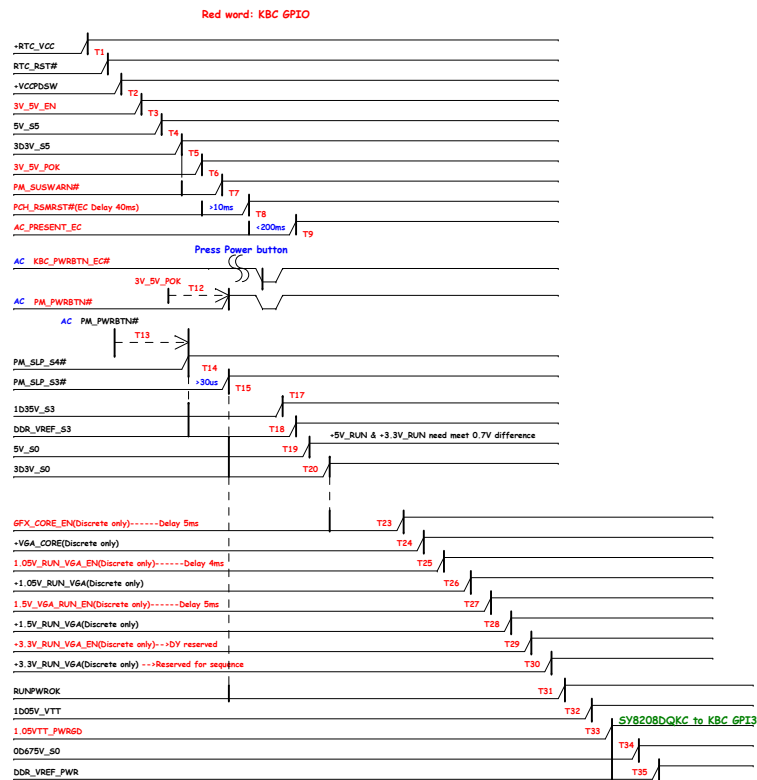
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Rev

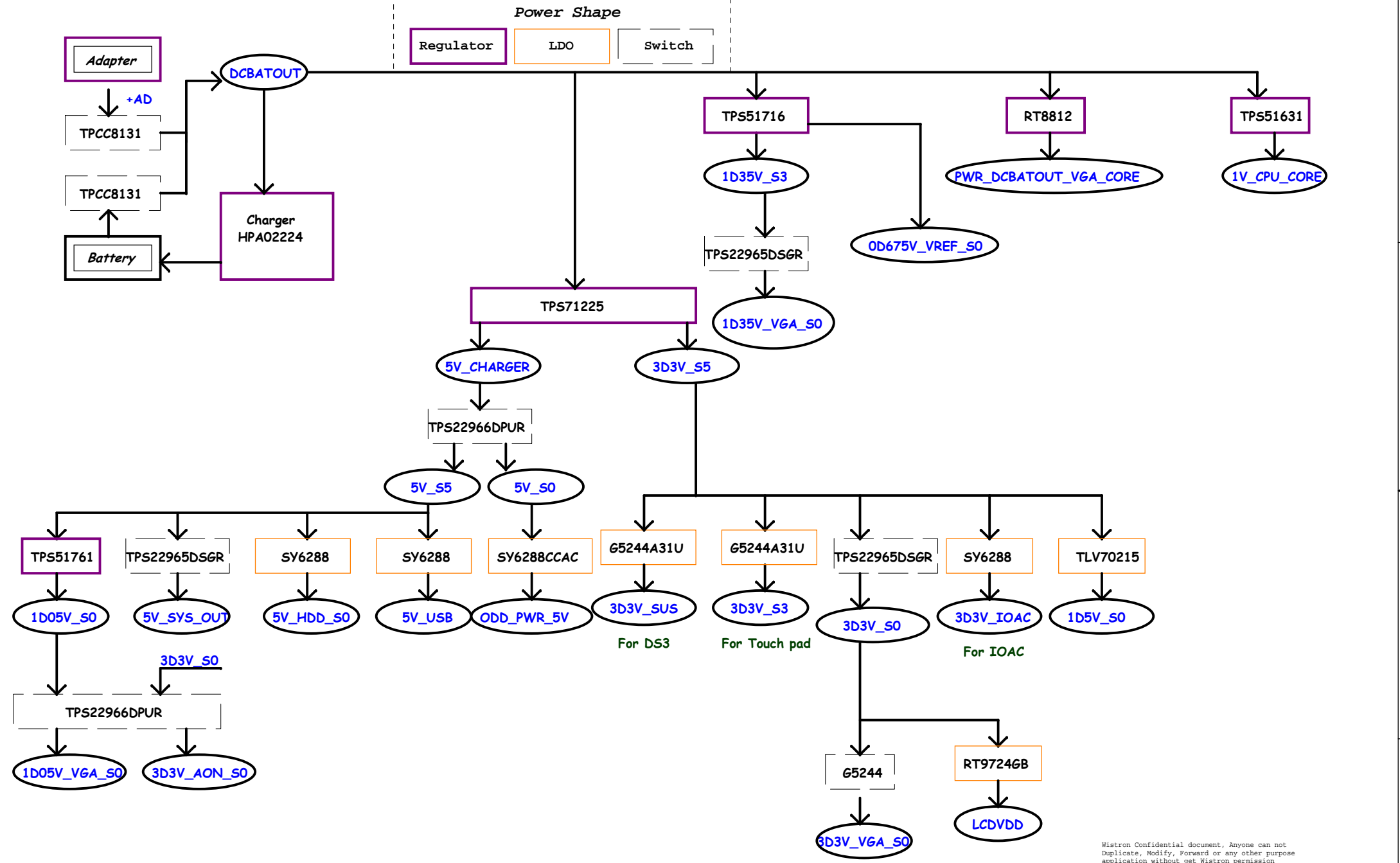
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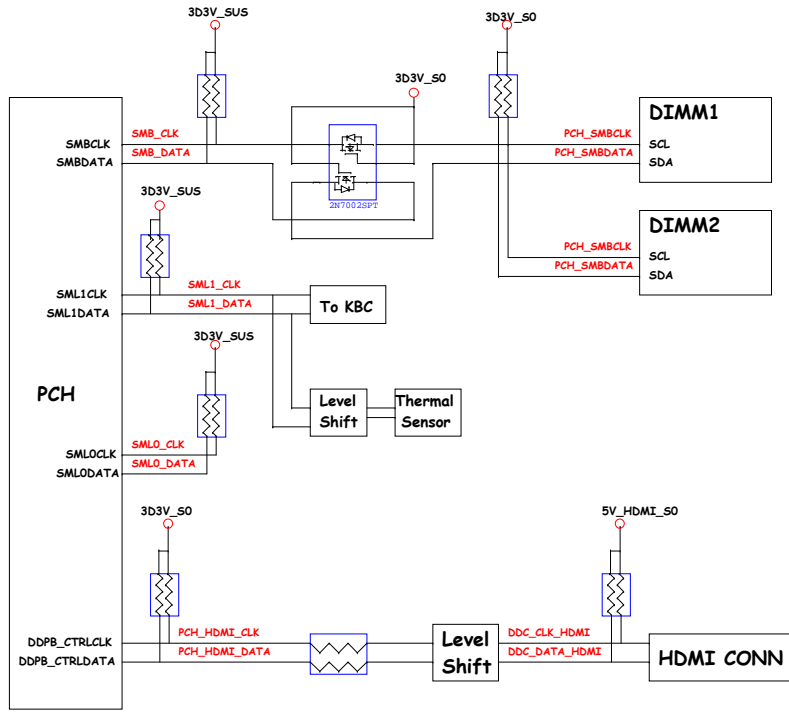


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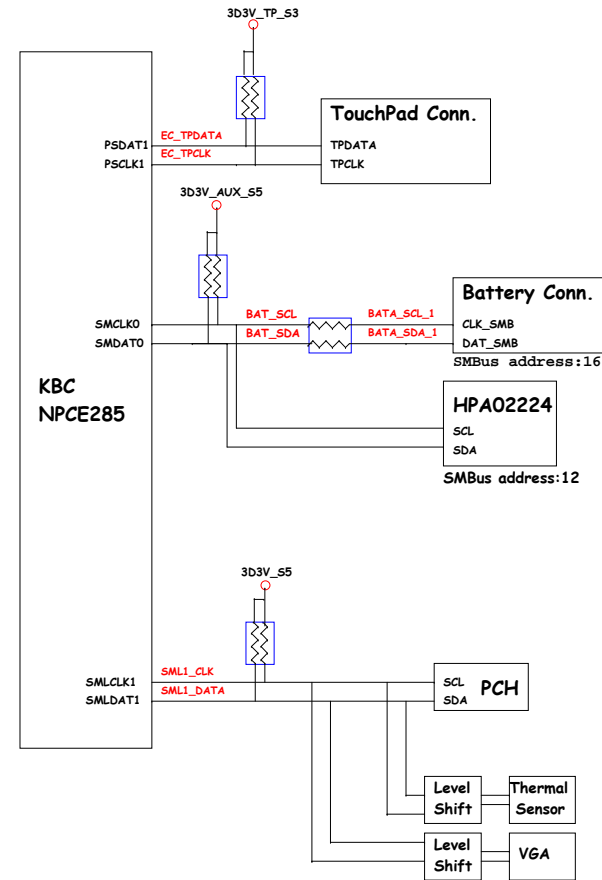
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Title: Power Block Diagram			
Size: A3	Document Number: Poseidon 860M	Rev: -1	
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PCH SMBus Block Diagram



KBC SMBus Block Diagram

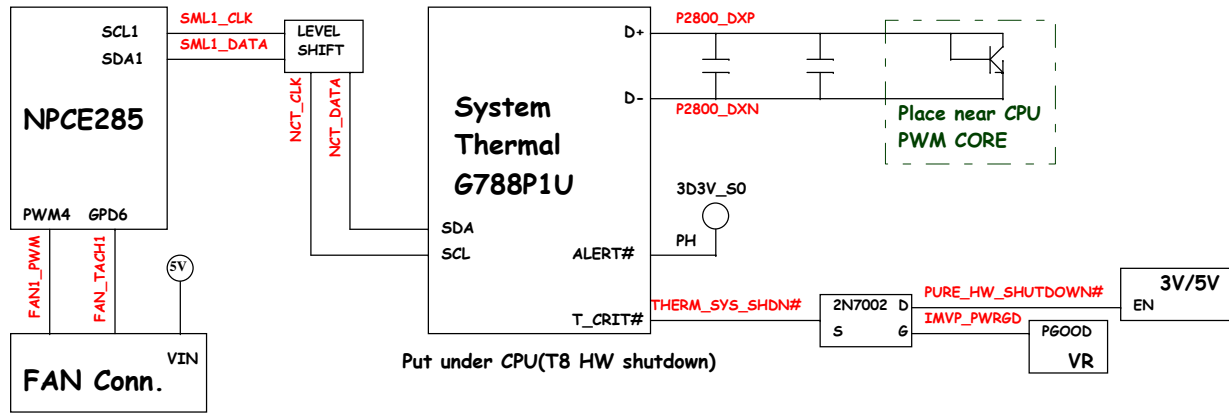


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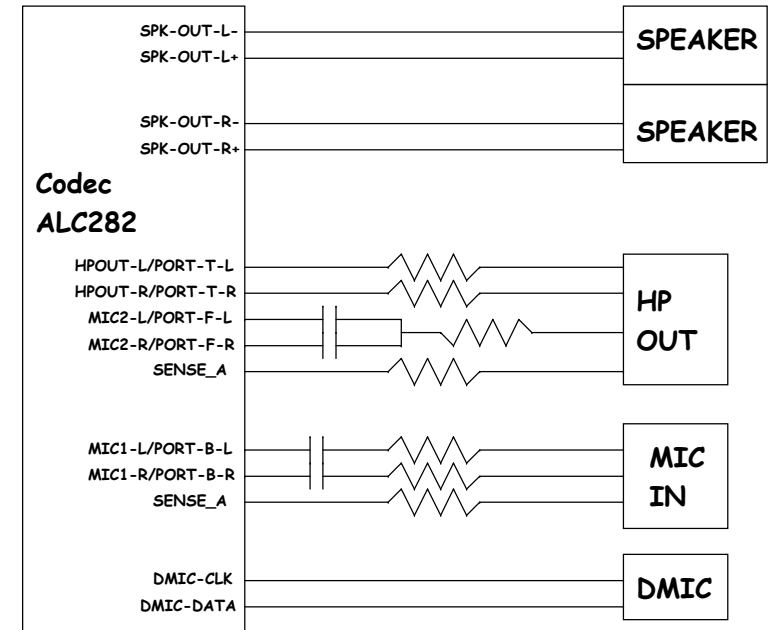
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Thermal Block Diagram



Audio Block Diagram



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