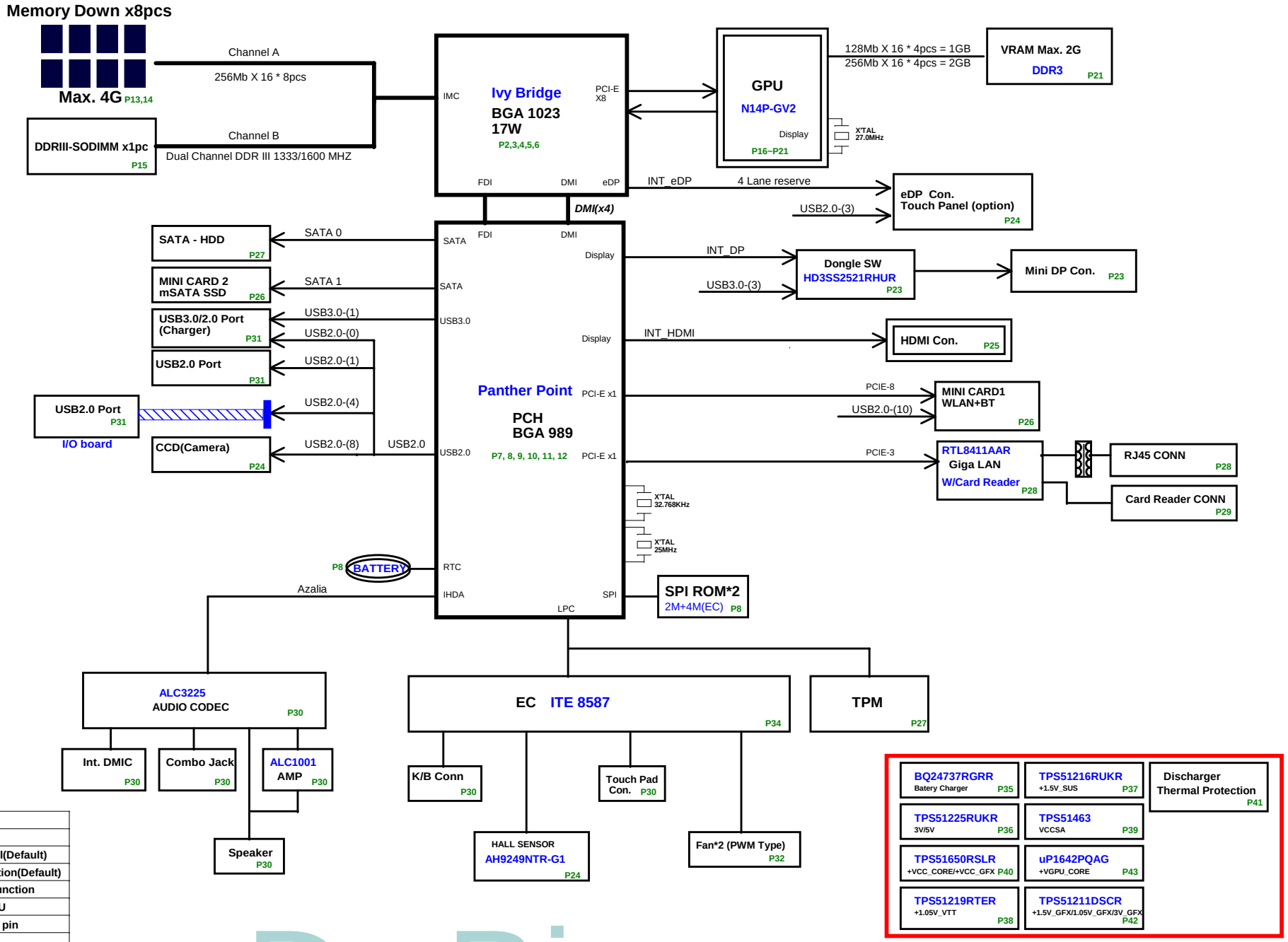
ZQK ULV SYSTEM BLOCK DIAGRAM



TPL@	Touch panel
TPM@	TPM module
NP@	Normal panel(Default)
CH@	Charge function(Default)
NCH@	No Charge function
EV@	Optimize SKU
RAMID@	RAMID strap pin
SUG@	LAN Surge
NSW@	w/o Dongle switch
SW@	w Dongle switch
KBL@	KB Backlight LED
RD@	mSATA Re-driver

Quanta Computer Inc.
PROJECT : ZQK
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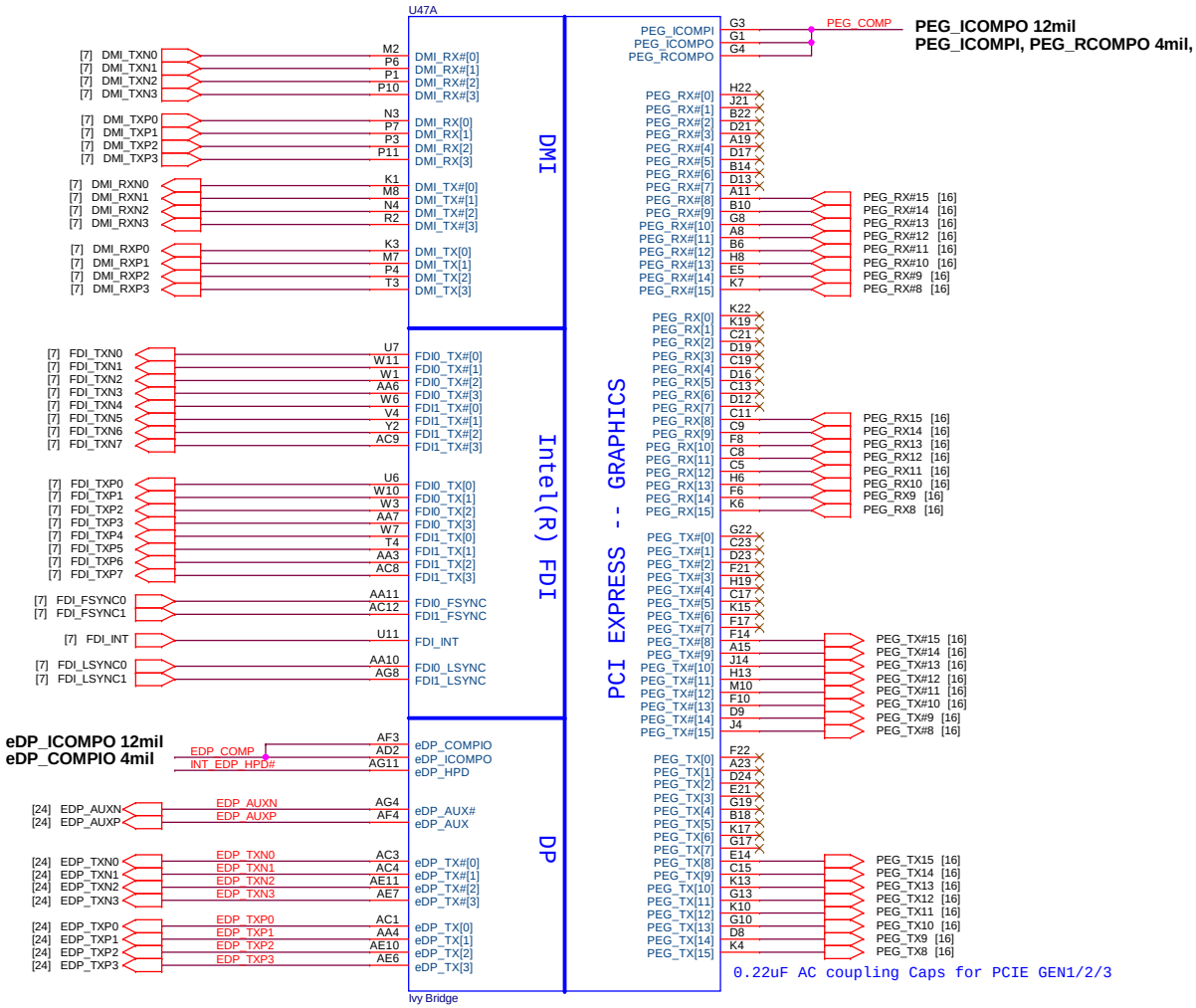
Ivy Bridge Processor (DMI,PEG,FDI) (CPU)

PEG_ICOMPI and RCOMPO signals
should be shorted and routed with
- max length = 500 mils
- typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with
- max length = 500 mils
- typical impedance = 14.5 mohms

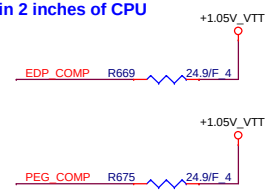


DP_COMPIO and ICOMPO signals
should be shorted near balls and routed with
- typical impedance < 25 mohms

DG 1.0 :
The recommended AC cap value is changed to 220nF for compatibility with
PCIe Gen3 on future platforms.
For Gen2 only designs, it is acceptable to continue to use the 100nF capacitor.

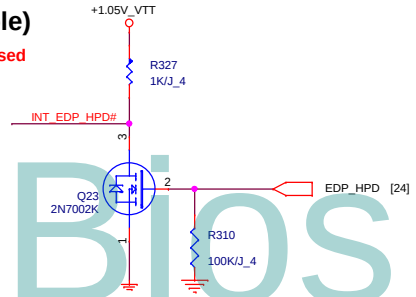
DP & PEG Compensation

CAD Note: Place PU resistor
within 2 inches of CPU



eDP Hot-plug (Disable)

HPD PU/PD resistor values based
on CRB and different to DG



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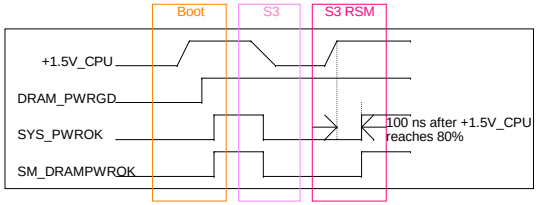
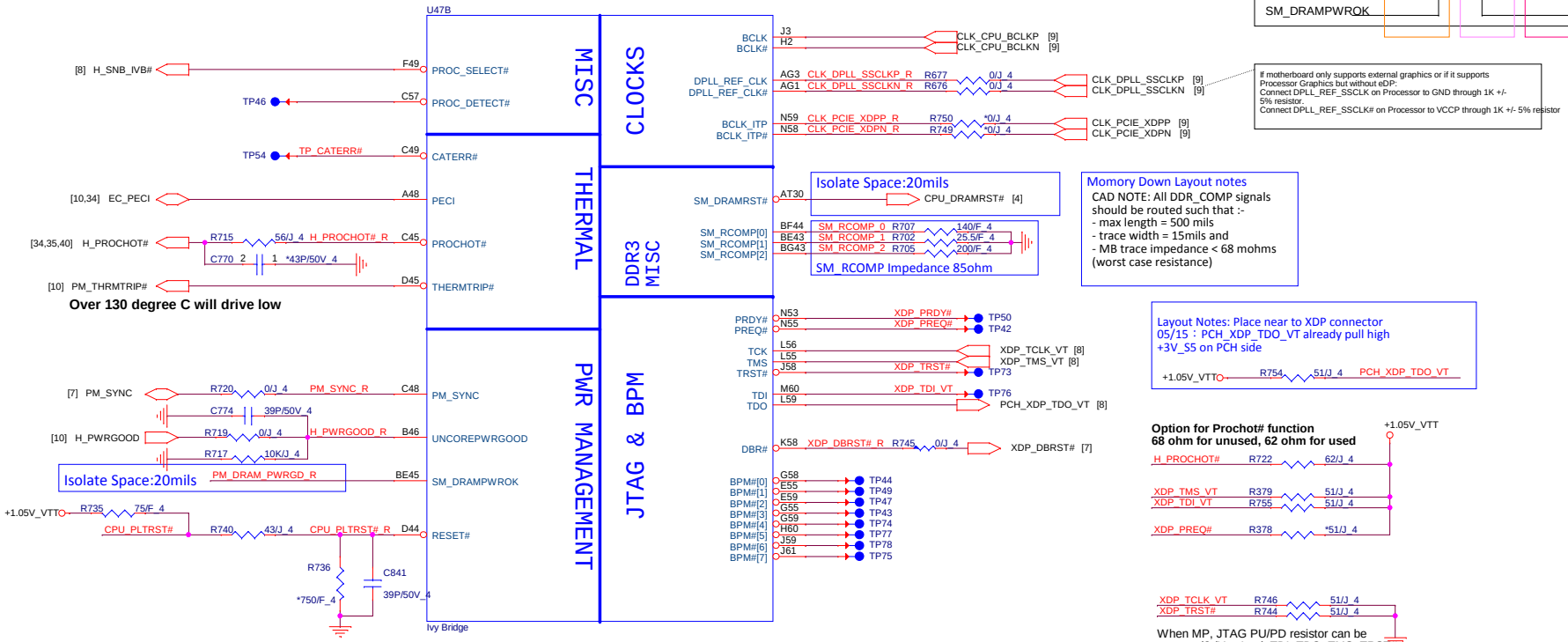
PROJECT : ZQK

Size	Document Number	Rev
	Ivy Bridge 1/5 (HOST & PCIE)	1A
Date: Monday, January 07, 2013	Sheet 2 of 46	

Ivy Bridge Processor (CLK,MISC,JTAG) (CPU)

03





If motherboard only supports external graphics or if it supports Processor Graphics but without eDP:
Connect DPLL_REF_SSCLK on Processor to GND through 1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K +/- 5% resistor

Isolate Space:20mils

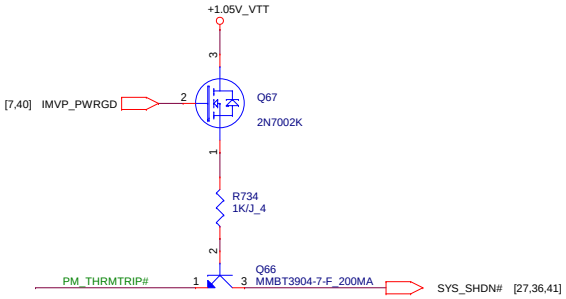
Momery Down Layout notes
CAD NOTE: All DDR_COMP signals should be routed such that :-
- max length = 500 mils
- trace width = 15mils and
- MB trace impedance < 68 mohms (worst case resistance)

Layout Notes: Place near to XDP connector
05/15：PCH_XDP_TDO_VT already pull high
+3V_S5 on PCH side

Option for Prochot# function
68 ohm for unused, 62 ohm for used

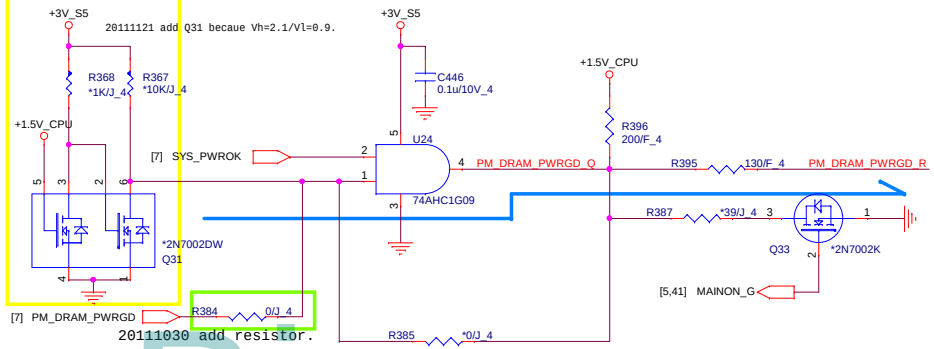
When MP, JTAG PU/PD resistor can be removed? (Yes Intel, TDI, TDO, TMS, TRST#, TCK,PREQ#, PRDY#)

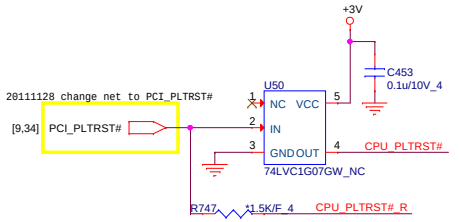
Thermal Trip (CPU)



S3 leakage circuit (CPU)

If PM_DRAM_PWEGD connector,the R5180 must stuff.





IN	OUT
L	L
H	High-Z

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PROJECT : ZQK

Size	Document Number	Rev
	Ivy Bridge 2/5 (CLK & JTAG)	1A

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Ivy Bridge Processor (CPU)

04

Channel A: On board RAM 2Rx16 8pcs

U47C

DDR SYSTEM MEMORY A

Ivy Bridge

Channel B: SO-DIMM

U47D

DDR SYSTEM MEMORY B

Ivy Bridge

+0.75V_DDR_VTT

C240 1u/6.3V_4, C239 1u/6.3V_4, C238 1u/6.3V_4, C237 1u/6.3V_4, C236 1u/6.3V_4, C241 1u/6.3V_4, C279 10u/6.3V_6

20120112 for memory down PU CAP.

S3 leakage circuit (CPU)

S3 circuit: DRAM_RST# to memory should be high during S3

20120914 Follow Z09 design to move R682 close to Q62

+1.5VSUS, +3V_S5

R680 1K/F_4, R686 1K/J_4, R684 *0/J_4, R681 1K/F_4, R682 *0/J_4, R683 0/J_4, R693 4.99K/F_4, C678 0.047u/10V_4, Q62 2N7002K

[13,14,15] DDR3_DRAMRST#

[9] DRAMRST_CNTRL_PCH

[34] EC_DRAMRST_CNTRL

[13,14,15] DEEPS3_EC

CPU_DRAMRST# [3]

20120204 Change to EC for new BIOS 0.6

Quanta Computer Inc.

PROJECT : ZQK

Size	Document Number	Rev
	Ivy Bridge 3/5 (DDR3 I/F)	1A
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IVY Bridge Processor (POWER) (CPU)

CPU VCCIO
IVY 17W:8.5A

SNB : Spec	Cose down
330uF/6mohm x 2	330uF/6mohm x 1
10uF x 10	10uF x 10
1uF x 26	1uF x 26

CPU VCCAXG
IVY 17W:TDC 18A

Spec	Cose down
3.9mΩ/LoadlineDesign	3.9mΩ/LoadlineDesign
total : 1uF x 11	total : 1uF x 11
total : 10uF x 6	total : 10uF x 12
total : 22uF x 6	tatal : 470u x 1(power side*2)
tatal : 470u x 1(power side*2)	

CPU VDDQ
IVY 45W: 5A

Spec
330uF/6mohm x 1
10uF x 8
1uF x 10

CPU Core Power
IVY 17W:TDC 33A

IVY SPEC
1.9mΩ/LoadlineDesign
total : 2.2uF x 35
total : 22uF x 12
tatal : 470u x3(Power side*1)

Cose down
IVY SPEC
1.9mΩ/LoadlineDesign
total : 2.2uF x 35
total : 10uF x 12
tatal : 470u x1(Power side*1)

IVY SPEC
22uF_8 x7 Socket TOP cavity
22uF_8 x5 Socket BOT cavity
22uF_8 x2 Socket TOP cavity (no stuff)
22uF_8 x5 Socket BOT cavity (no stuff)
330uF_7343 x2

Voltage selection for VCCIO: this pin must be pulled high on the motherboard

On CRB
H_SNB_IVB#_PWRCTRL = low, 1.0V
H_SNB_IVB#_PWRCTRL = high/NC, 1.05V

CPU VCCPL
IVY 17W:1.5A

Spec	Real
330uF/7mohm x 1	10uF x 1
1uF x 2	1uF x 2

IVY SPEC
330uF x1, 10uF_8 x1, 1uF_4 x2
Socket BOT edge.

IVY SPEC
330uF x1, 10uF_8 x1 Socket BOT edge, 10uF_8 x2 Socket BOT cavity.

CPU VCCSA
IVY 17W: 6A

Spec	Real
330uF/7mohm x 1	10uF x 3
10uF x 5	
1uF x 5	

20121203 : Add 39pF for ESD

Layout note: need routing together and ALERT need between CLK and DATA

SVID CLK

Place PU resistor close to CPU

SVID DATA

Place PU resistor close to CPU

SVID ALERT

S3	STUFF	NO_STUFF
enable	-	R5347/R6362
disable	R5347/R6362	-

S3 circuit: 1.5V input to IVB is gated & IVB Read Vref 0.75V is gated

IVY Bridge Processor (GRAPHIC POWER) (CPU)

VCCAXG_SENSE/VSSAXG_SENSE R=100, Trace impedance 15.5~34.5, <25mils.

CAD Note: +VDDR_REF_CPU should have 10 mil trace width

VID[0]	VID[1]	+VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

For SN Bridge

VID[1]	+VCCSA
0	0.9V
1	0.8V

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PROJECT : ZQK
Size: Document Number: Ivy Bridge 4/5 (POWER) Rev: 1A
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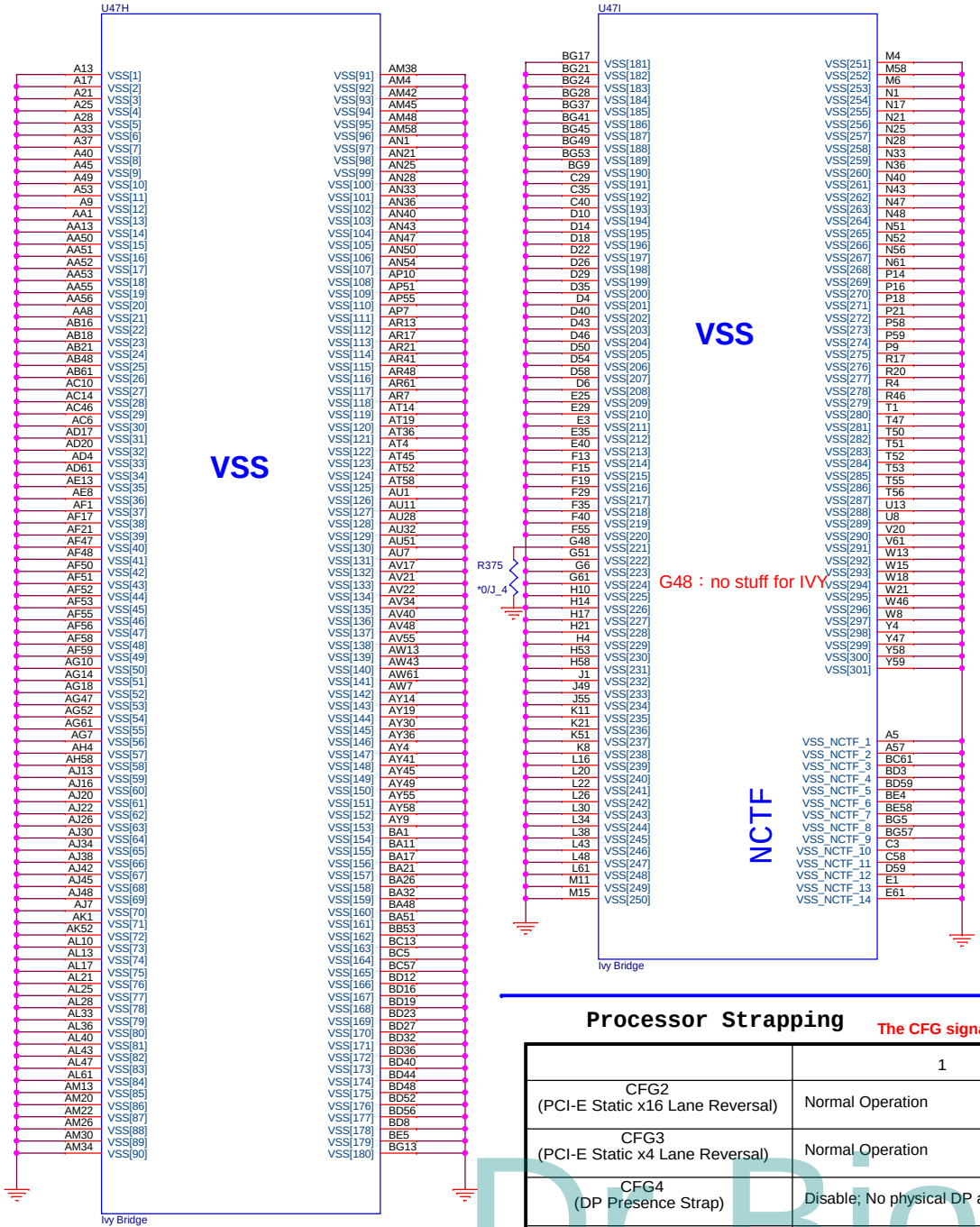
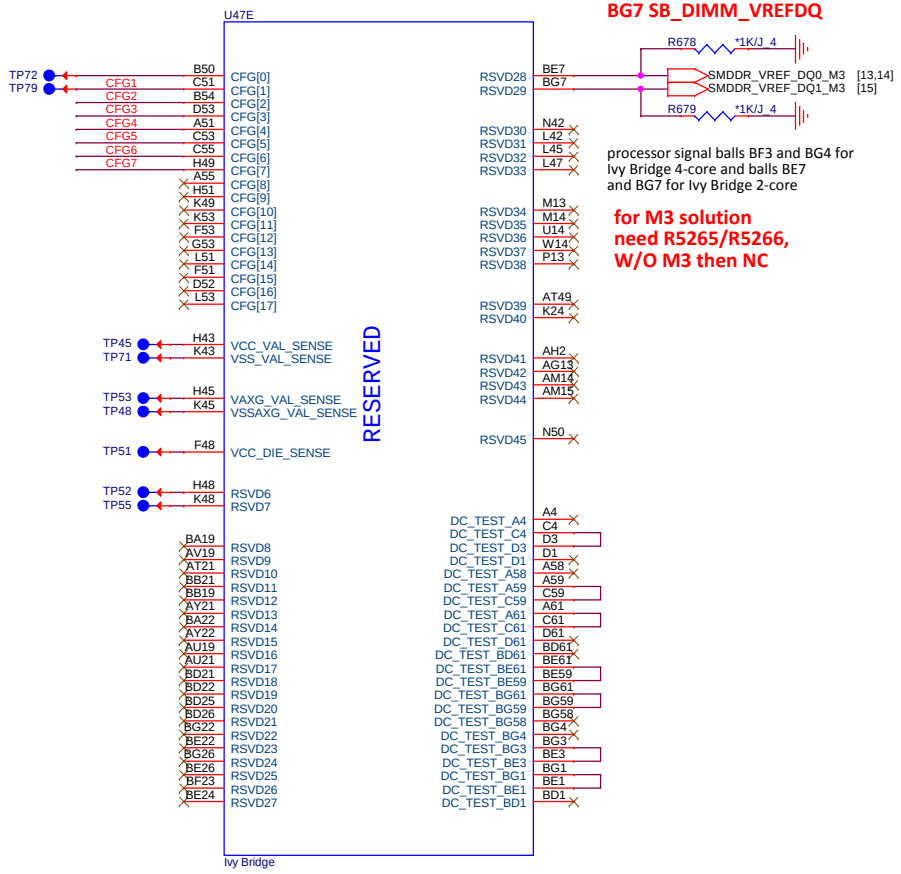
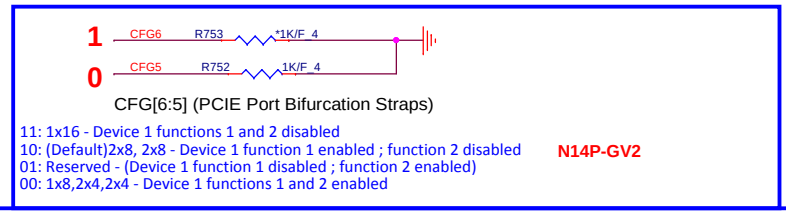
IVY Bridge Processor (GND) (CPU)



IVY Bridge Processor (RESERVED, CFG) (CPU)

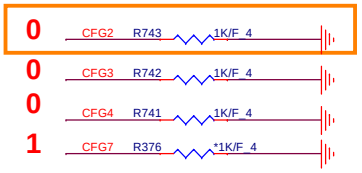




Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PCI-E Static x16 Lane Reversal)	Normal Operation	**Lane Reversed**
CFG3 (PCI-E Static x4 Lane Reversal)	Normal Operation	**Lane Reversed**
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	**Enable; An ext DP device is connected to eDP**
CFG7 (PEG Defer Training)	**PEG train immediately following xxRESETB de assertion**	PEG wait for BIOS training



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PROJECT : ZQK

Size	Document Number	Rev
	Ivy Bridge 5/5 (GND)	1A
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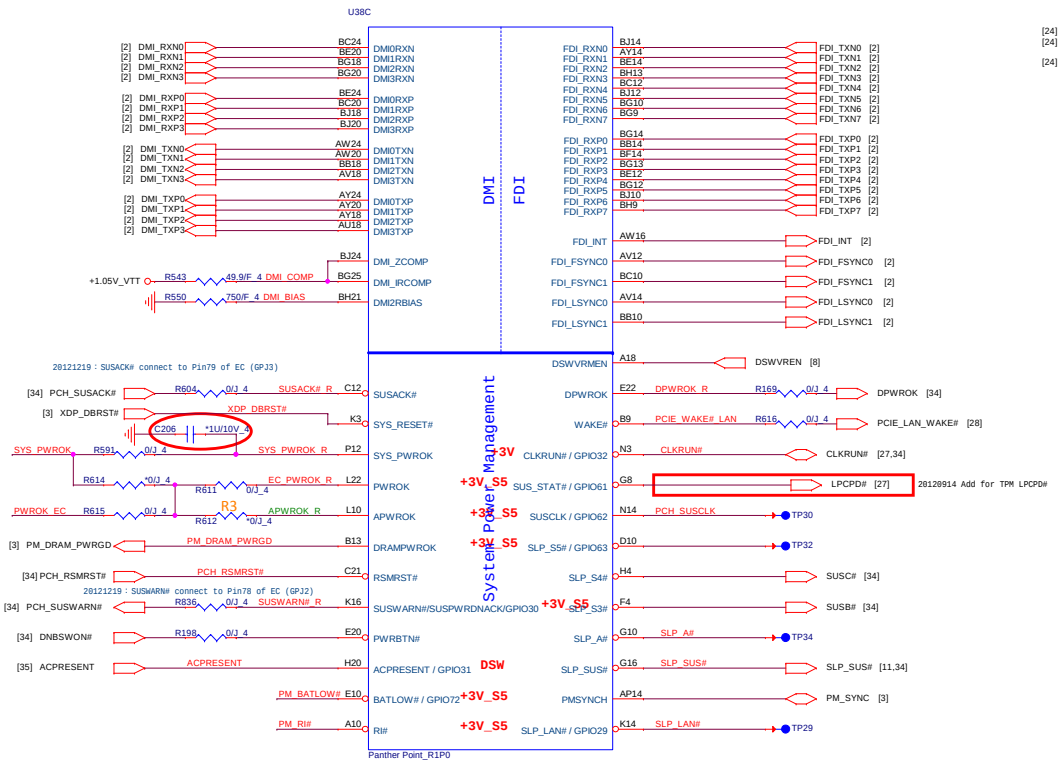
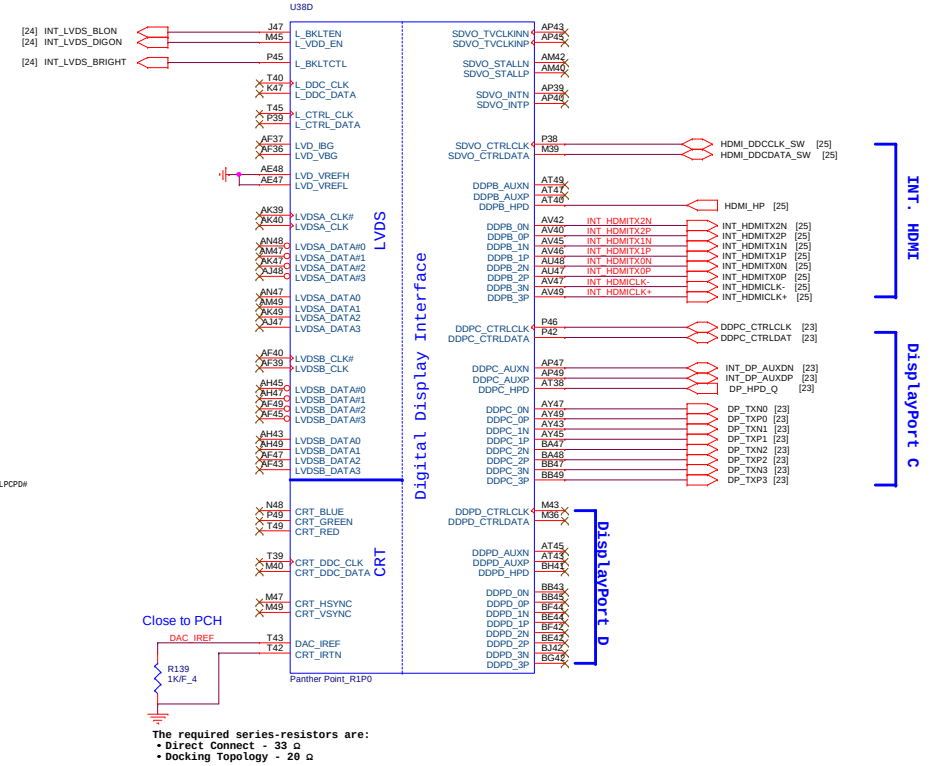
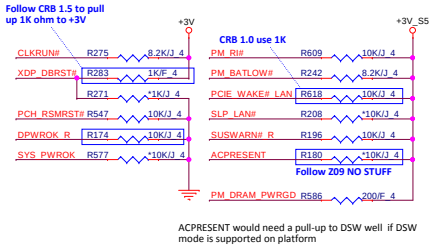
CPT/PPT (DMI,FDI,PM) (CLG)



CPT/PPT (LVDS,DDI)



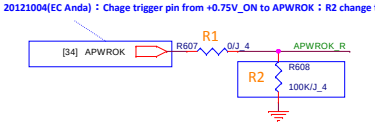
PCH Pull-high/low (CLG)



ACPRESENT would need a pull-up to DSW well if DSW mode is supported on platform

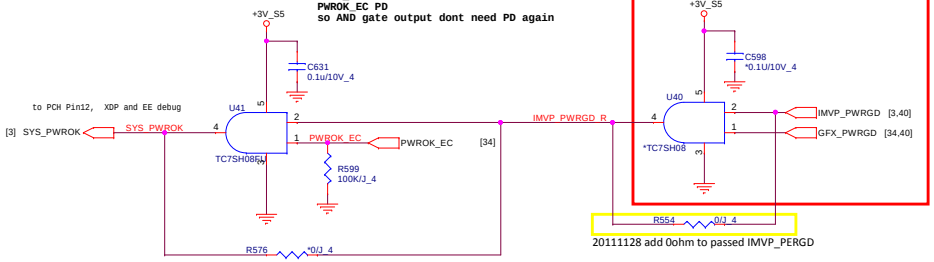
20120706:Speed up 250ms to boot up
R1,R2,R3 for EC power on 250 ms

20121004(EC Anda)：Chage trigger pin from +0.75V_ON to APWROK：R2 change to 100K



System PWR_OK (CLG)

IMVP_PWRGD PU +3V
PWROK_EC PD
so AND gate output dont need PD again



20111128 add 0ohm to passed IMVP_PERGD

include GFX_PWRGD to SYS_PWROK for PCH check

Quanta Computer Inc.
PROJECT : ZQK

Size	Document Number	Rev
	PCH 1/6 (DMI/FDI/VIDEO)	1A
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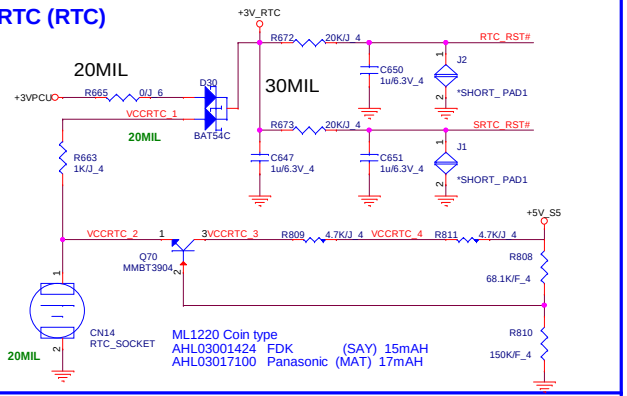
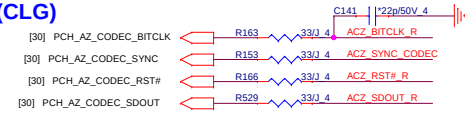
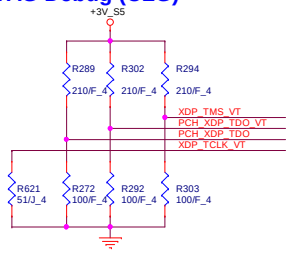
RTC (RTC)



HDA Bus (CLG)

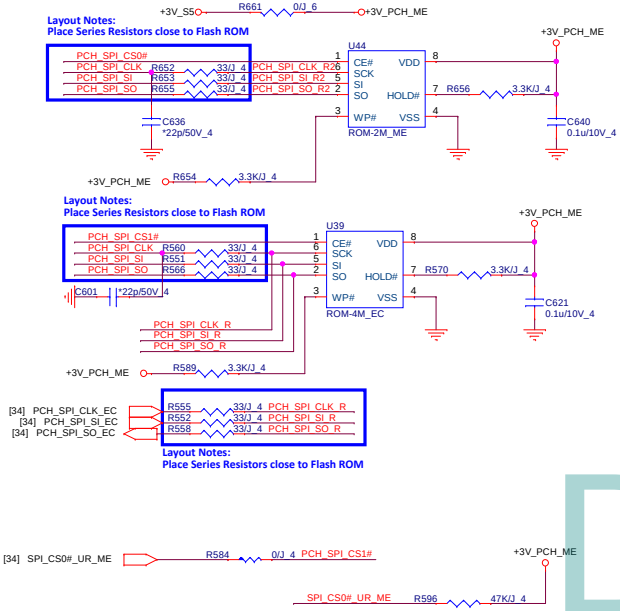


PCH JTAG Debug (CLG)



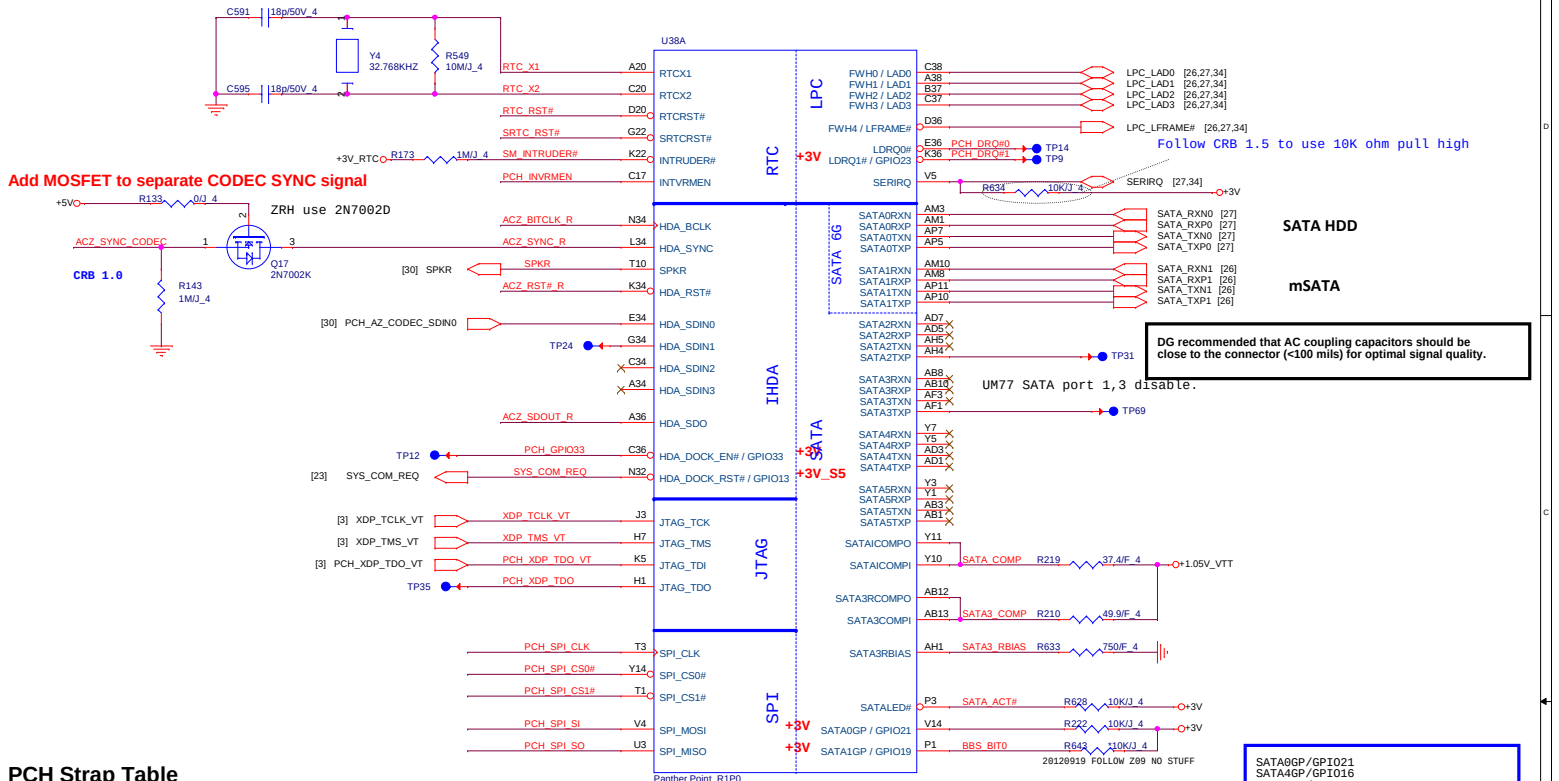
PCH Dual SPI (CLG) (Default for WIN8)

W25Q32BVSSIG / AKE391P0N00------>4MB
W25Q16BVSSIG / AKE38FP0N01----->2MB



PCH2 (CLG)

CPT/PPT (HDA,JTAG,SATA) (CLG)

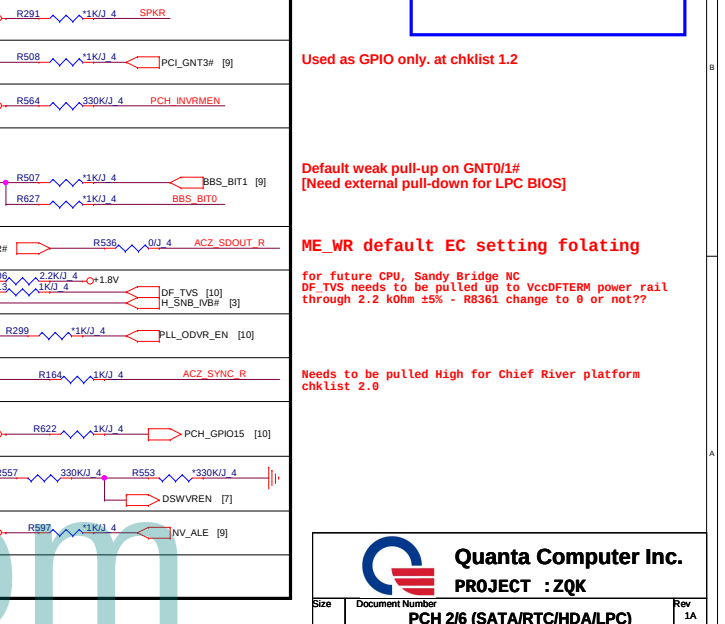


PCH Strap Table

Pin Name	Strap description	Sampled	Configuration
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK	

GNT1#	GPIO19	Boot Location
1	1	SPI *
0	0	LPC

HDA_SDO	Flash Descriptor Security	RSMRST	0 = effect (default)(weak pull-down 20K) 1 = overridden
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss (weak pull-down 20K) 1 = Set to Vcc
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (weak pull-up 10K)
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V
GPIO15	Intel ME Crypto Transport Layer Security (TLS) cipher suite internal PD	RSMRST	0 = Disable (Default) 1 = Enable
DSWVREN	DEEP S4/S5 well On Die DSW VR Enable	DSW	High = Enable (Default) Low = Disable
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)



Quanta Computer Inc.
PROJECT : ZQK

Size	Document Number	Rev
	PCH 2/6 (SATA/RTC/HDA/LPC)	1A

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CPT/PPT (PCI,USB,NVRAM) (CLG)

CPT/PPT (PCI-E,SMBUS,CLK)

20111122 add for Touch pad interrupt pin from GPIO13 to GPIO11.

Layout Notes:
USB3 TX AC cap place at connector side, AC cap to connector < 400mils

USB30 Port1: EXT USB3.0 Port
USB30 Port3: Mini DP port

USB3.0

MB USB WITH 3.0 PORT
MB USB 2.0 Port
Mini DP WITH 3.0 PORT
Touch Panel
DB USB 2.0 Port

USB Port1 can be used on debug mode
XHCI for USBP0-3

EHCI1

USB port6/7 may not be available on all PCH sku (HM55 support 12port only)

USB Port9 can be used on debug mode
1001：(BIOS) Use port1 is enough
EHCI2

Camera
BT+WL

UM77 USB port 6,7,12,13 disable.

PCIE port 1 for commeral model S3 can't weak up.

Wireless
LAN

UM77/HM70 will disable 5~8 PCIE ports

20110908 WLAN support S3 wake up function.

Wireless
LAN

For LAN
For EC

20120201 Change CAP from 27P to 10P.

PLTRST#(CLG)

20120522：follow CRB to modify power plan to +3V
check list 2.0：When connected to the processor the PLTRST# signal should be level shifted to 1.05V.

PCI/USBOC# Pull-up(CLG)

MPC Switch Control

MPC_PWR_CTRL#	Low = MPC ON High = MPC OFF (Default)

CLK_REQ/Strap Pin(CLG)

CLOCK TERMINATION for FCIM
(Full Clock Integration Mode)

SMBus(EC) (CLG)

SMBus(PCH) (CLG)

S5
S0

20120712：Add 0ohm reserved for two sides of SMBUS since they are the same power plane (CRB no level shift)

DDRIII Memory down strap (CLG)

Vender	RAM_IDn	Q PN	Mfr. PN	Freq.
Hynix	0000			
Elpida	0001	AKD5JGST400	EDJ4216EBBG-DJ-F	1333MHz
	0010	AKD5JGST407	EDJ4216EFBG-GNL-F	1600MHz

EV@: For Optimize SKU
IV@: For UMA SKU

	dGPU_PW_CTRL# (GPIO68) CTL : dGPU_VRON	SKU_ID1 (GPIO64)	SKU_ID0 (GPIO16)	VGA H/W Signal	Setup Menu	
UMA Only	1	0	0	UMA	Hidden	UMA boot
dGPU Only	0 or 1	0	1	GPU	Hidden	GPU boot
Switchable (Mux)	0	1	0	UMA+GPU	dGPU/SG	UMA boot
Optimize (Muxless)	0	1	1	UMA	UMA/SG	UMA boot

dGPU_PW_CTRL#
1 = GPU power is control by H/W (pure Discrete SKU)
0 = GPU power is control by PCH GPIO (Discrete, SG or Optimize)

Quanta Computer Inc.
PROJECT : ZQK
PCH 3/6 (PCIE/USB/CLK/SMB)
Rev 1A
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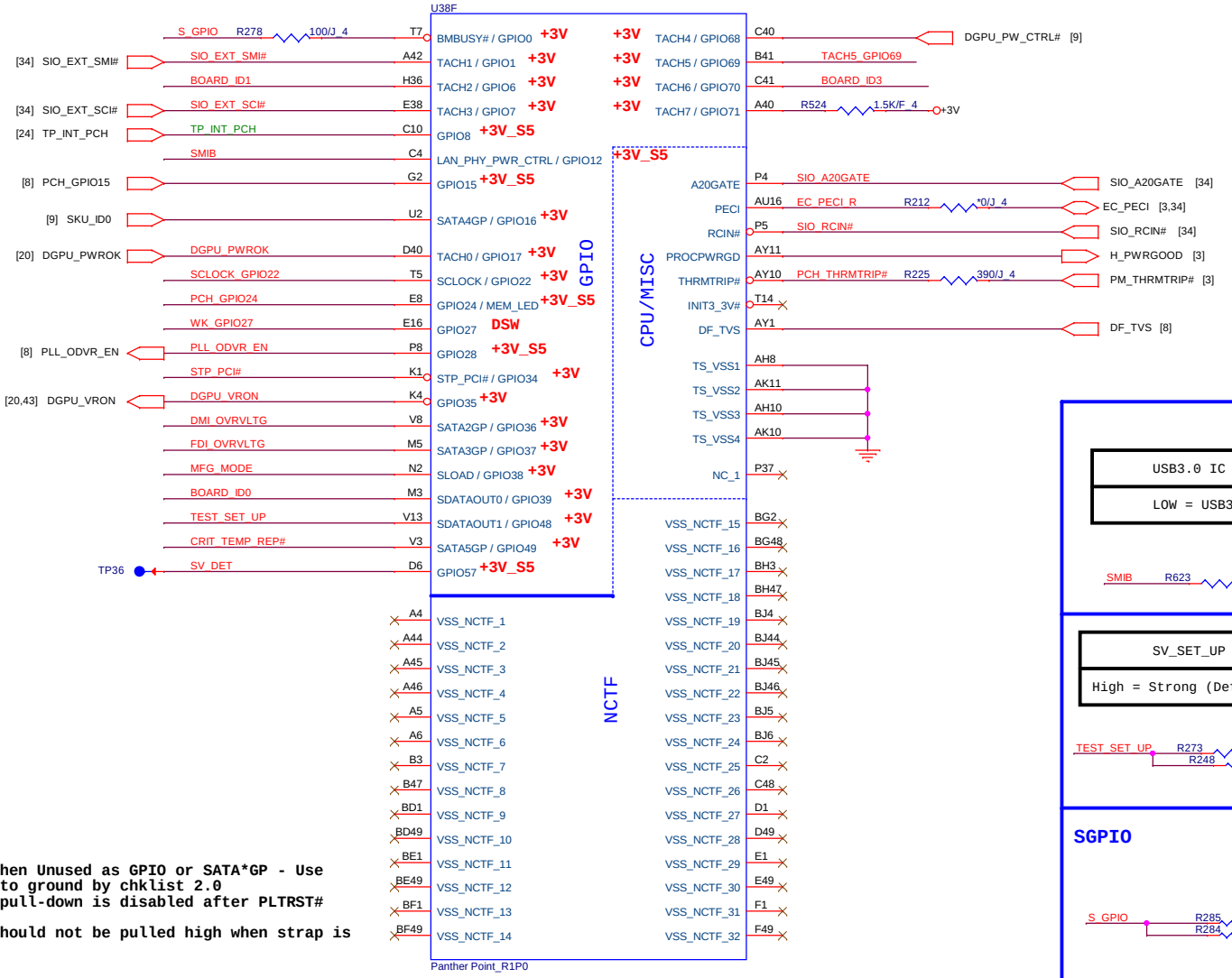
CPT/PPT (GPIO,VSS_NCTF,RSVD) (CLG)

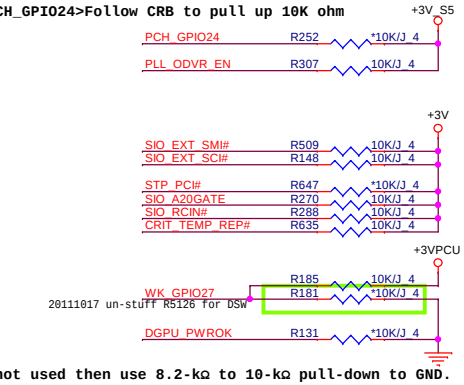


SATA2GP/SATA3GP : When Unused as GPIO or SATA*GP - Use 8.2K-10K pull-down to ground by chklist 2.0
NOTE: The internal pull-down is disabled after PLTRST# deasserts.
NOTE: This signal should not be pulled high when strap is sampled.

GPIO Pull-up/Pull-down (CLG)

10

20120625 : <PCH_GPIO24>Follow CRB to pull up 10K ohm



GPIO27 : If not used then use 8.2-kΩ to 10-kΩ pull-down to GND.

USB3.0 IC CTL
LOW = USB3.0 IC

+3V_S5 SMIB R623 10K/J_4

DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

+3V R229 *10K/J_4 DMI_OVRVLTG R279 *200K/F_4

SV_SET_UP
High = Strong (Default)

+3V TEST_SET_UP R273 10K/J_4 R248 *1K/J_4

+3V_S5 R280 *10K/J_4 SV_DET R274 100K/J_4
high VDDR=+1.35V_SUS for DDR3L
Low VDDR =+1.5V_SUS(default)
assign to VID for VDDR control

SGPIO

+3V S_GPIO R285 1K/J_4 R284 *1K/J_4

+3V
R631 10K/J_4 BOARD_ID0 R646 *10K/J_4
R162 10K/J_4 BOARD_ID1 R151 *10K/J_4
R99 *10K/J_4 BOARD_ID2 R105 10K/J_4
R520 10K/J_4 BOARD_ID3 R522 *10K/J_4
R506 *10K/J_4 BOARD_ID4 R505 10K/J_4
[9,32] BOARD_ID2
[9,24] BOARD_ID4

	High	Low
BOARD_ID0	GDDR5	DDR3
BOARD_ID1	Disable on board memory	Enable on board memory
BOARD_ID2	Pin8 of SYNAPTICS and ELAN are NC pin Default is pull high BIOS maybe will use EEPROM detection	
BOARD_ID3		
BOARD_ID4	No touch panel	Touch panel

2011/09/01 add select resistor

TACH5_GPIO69 R510 1K/J_4

LVDS = Pull HIGH eDP = Pull LOW

20120607 : follow CRB pull down

+3V R298 100K/J_4 FDI_OVRVLTG R290 *1K/J_4

FDI TERMINATION VOLTAGE OVERRIDE	LOW - Tx, Rx terminated to same voltage

+3V SCLOCK_GPIO22 R268 10K/J_4 R250 *1K/J_4

G_SENSOR_ID	High = Disable (Default) Low = Enable

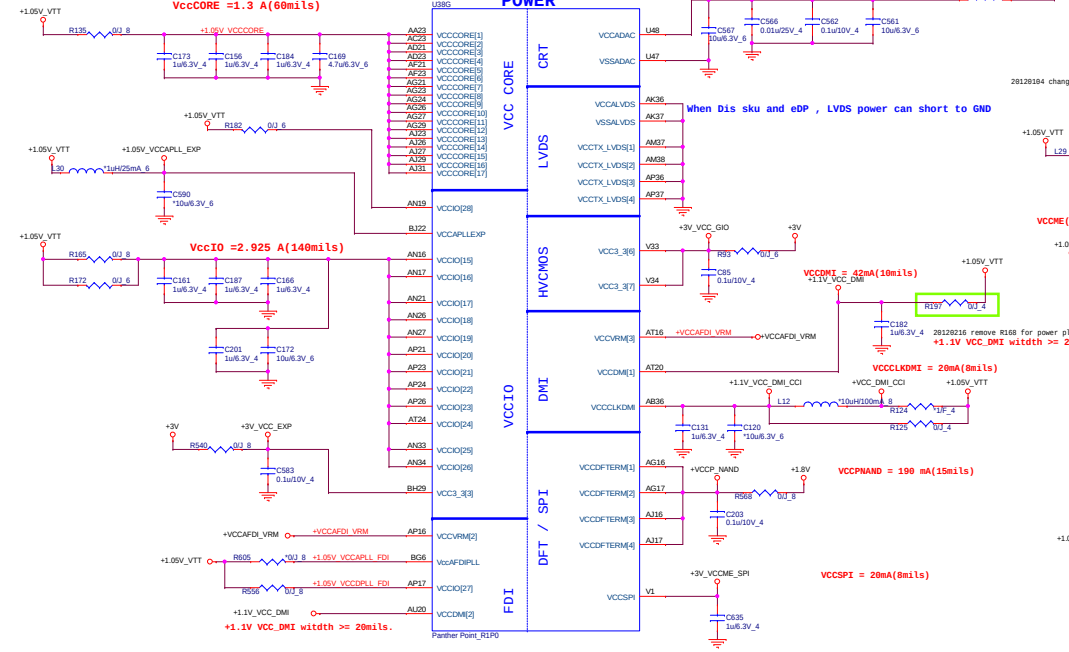
MFG-TEST

+3V MFG_MODE R644 10K/J_4 R629 *1K/J_4

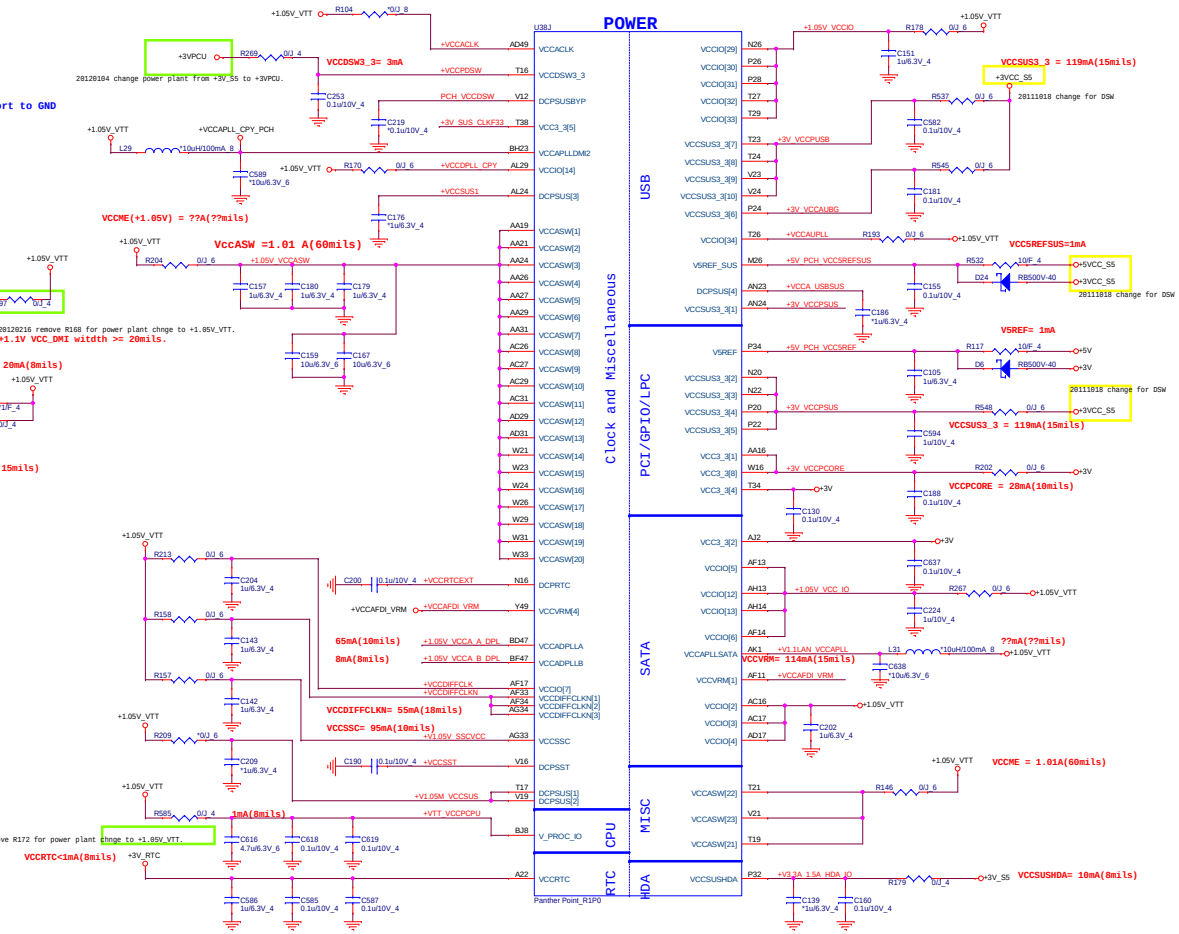
Quanta Computer Inc.
PROJECT : ZQK

Size	Document Number	Rev
	PCH 4/6 (GPIO/MISC)	1A
Date: Monday, January 07, 2013	Sheet 10 of 46	

CPT/PPT (POWER) (CLG)



CPT/PPT (POWER) (CLG)



20111018 ADD DSW Cricuit
20111030 modify cuirucit.

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PROJECT :ZQK

Size	Document Number	Rev
	PCH 5/6 (POWER)	1A
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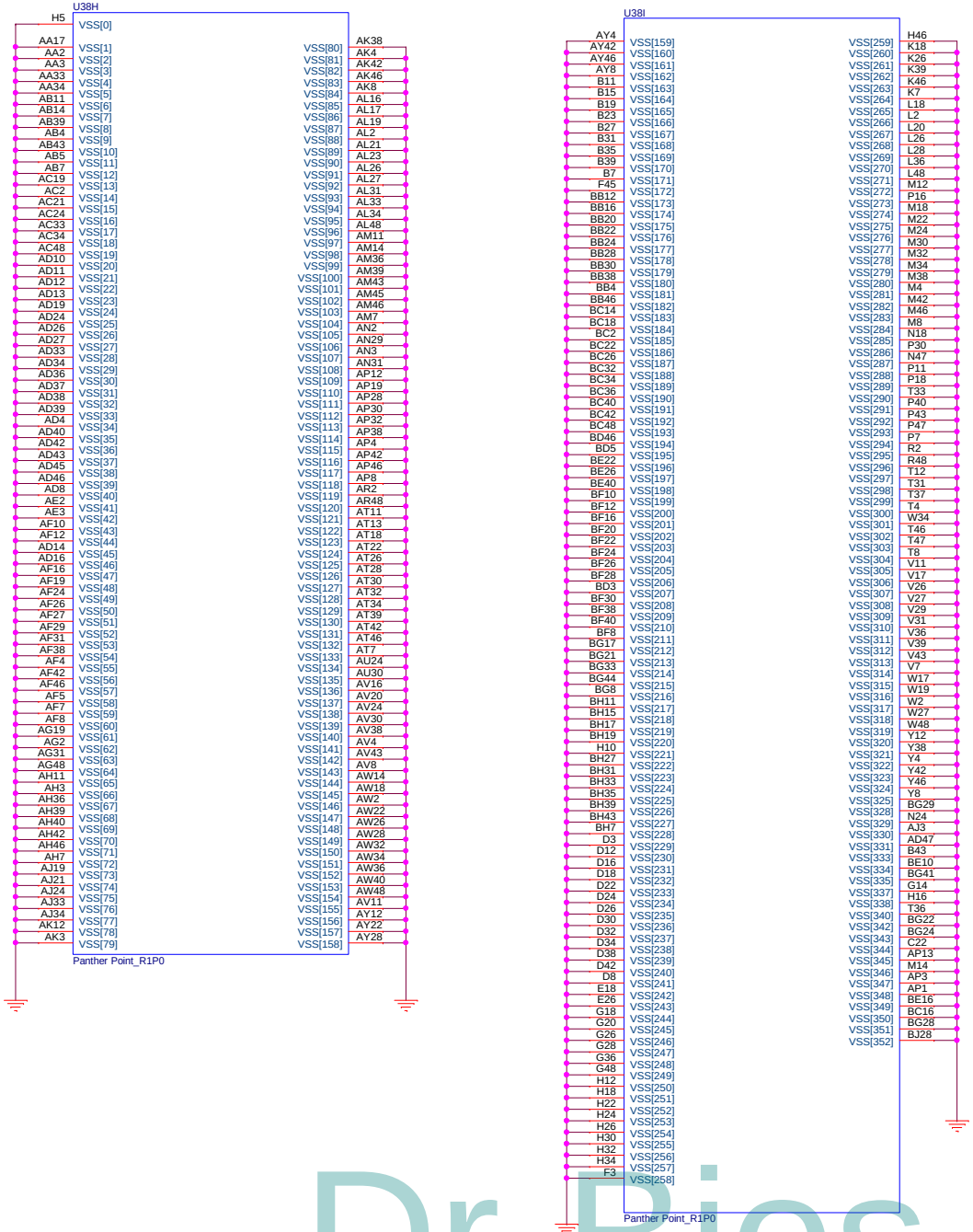
IBEX PEAK-M (GND) (CLG)



Quanta Computer Inc.
PROJECT : ZQK

Size	Document Number	Rev
	PCH 6/6 (GND)	1A
Date: Monday, January 07, 2013	Sheet 12 of 46	

DDR ON BOARD RAM (DDR)

Checklist 2.0:
M3 has to be no stuff on Chief River

BYTE0_0-7
BYTE1_8-15
BYTE2_16-23
BYTE3_24-31
BYTE4_32-39
BYTE5_40-47
BYTE6_48-55
BYTE7_56-63

SO-DIMMB SPD Address is 0XA4
SO-DIMMB TS Address is 0X34

Should be 240 Ohms +-1%

Place these Caps near Memory Down

SPD address= A0 hex (for MD devices)

	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1

WP =1 : WRITE DISABLE

CRB Add

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PROJECT : ZQK
DDR3 MEMORY DOWN X 16
Rev 1A
Date: Monday, January 07, 2013 Sheet 13 of 46

DDR ON BOARD RAM (DDR)

Checklist 2.0:
M3 has to be no stuff on Chief River

SO-DIMMB SPD Address is 0XA4
SO-DIMMB TS Address is 0X34

BYTE0_0-7
BYTE1_8-15
BYTE2_16-23
BYTE3_24-31
BYTE4_32-39
BYTE5_40-47
BYTE6_48-55
BYTE7_56-63

U43 U46 U48 U49

RAM_DDR3

100-BALL SDRAM DDR3

Should be 240 Ohms +-1%

R671 240/F_4
R688 240/F_4
R718 240/F_4
R765 240/F_4

C484 1.6P/50V_4
R254 30/F_4
R253 30/F_4
C243 0.1u/10V_4

C716 C693 C721 C726 C507 C680 C702 0.1u/10V_4

C249 C506 C733 C724 C254 C719 C492 0.1u/10V_4

R572 1K/F_4
R573 1K/F_4
C603 0.1u/10V_4
R571 *0/J_6

CRB Add
Q56 *AP2302GN
change to 1K/F_4
R562 1K/F_4
R563 1K/F_4
C600 0.1u/10V_4
R565 *0/J_6

Quanta Computer Inc.
PROJECT : ZQK
Size: Document Number: DDR3 MEMORY DOWN X 16 Rev: 1A
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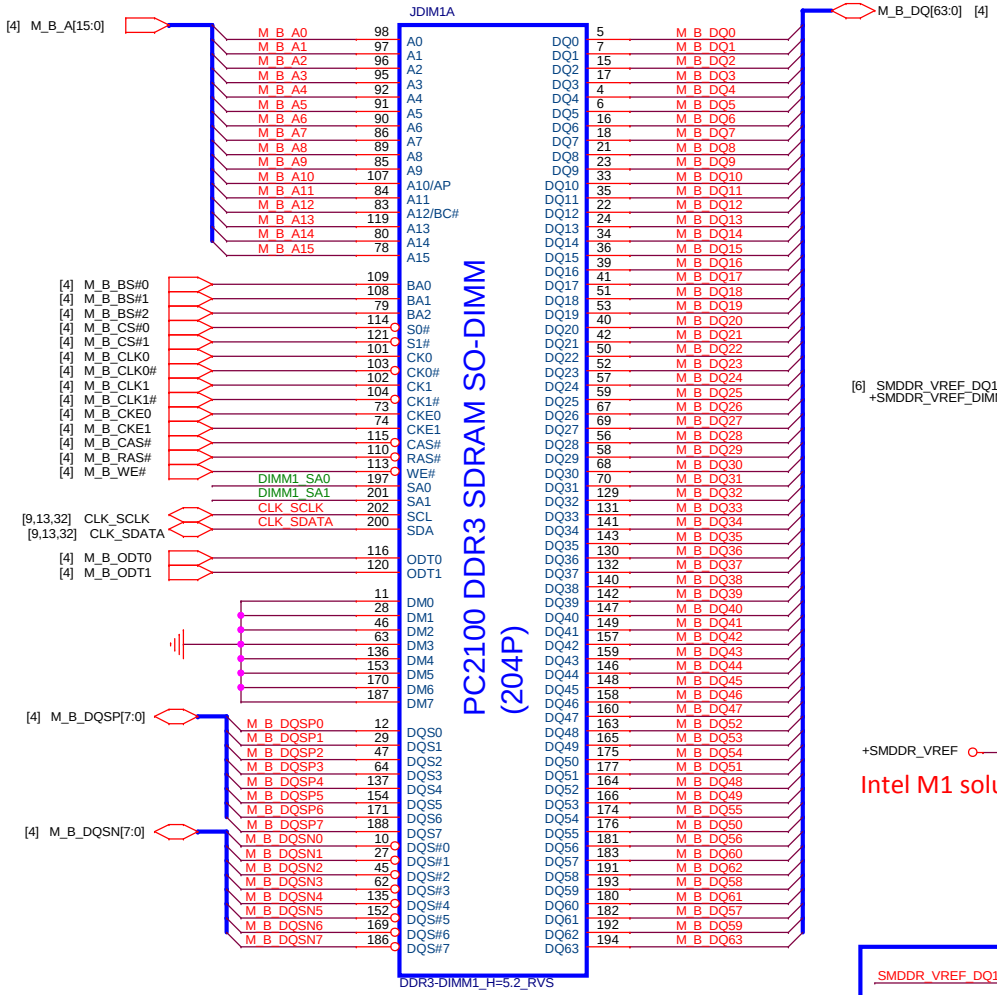
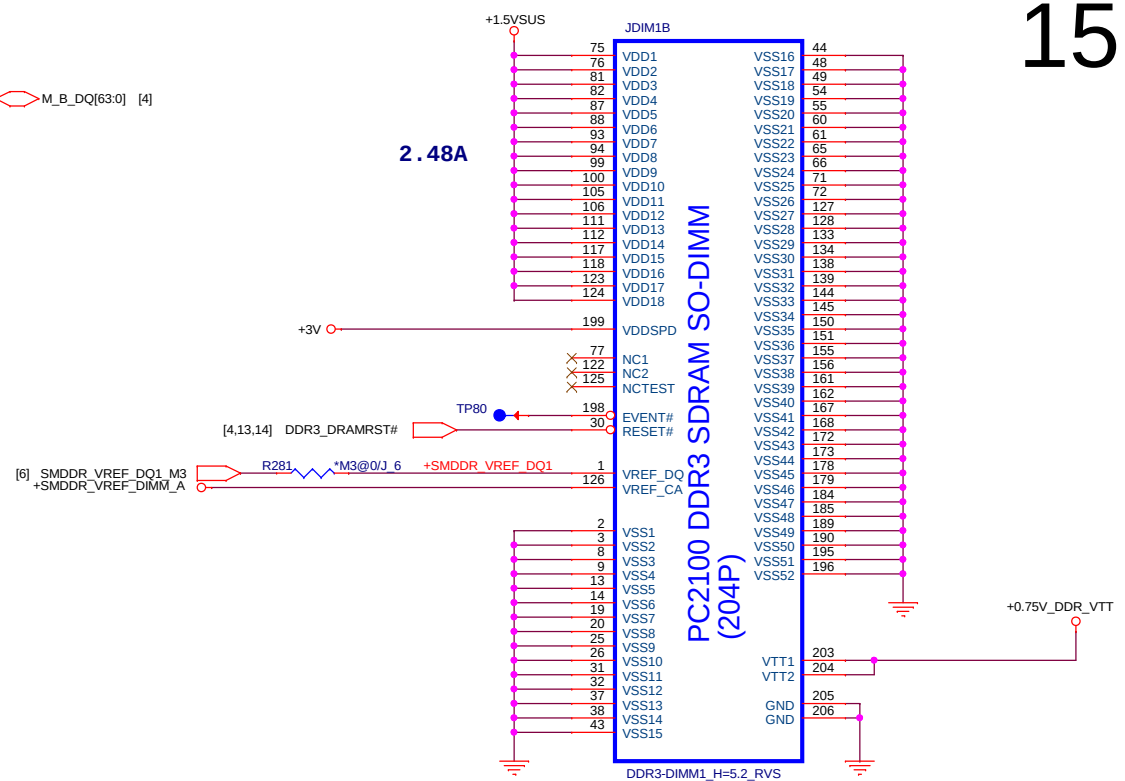
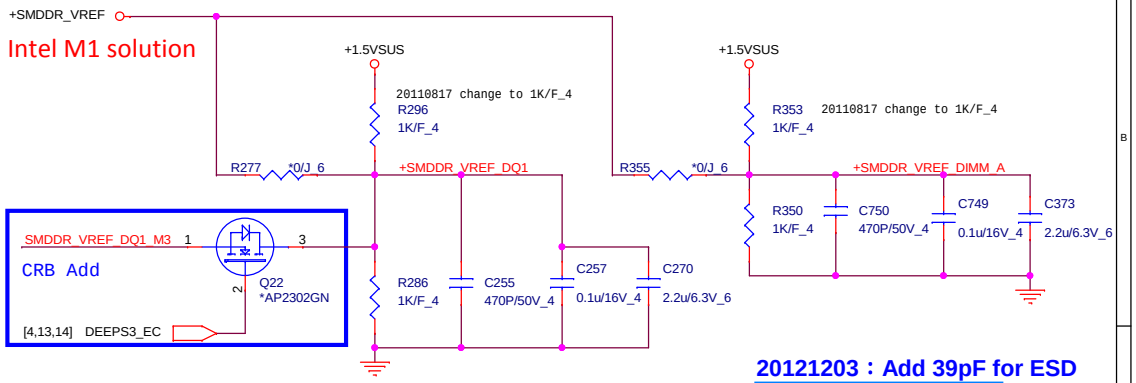
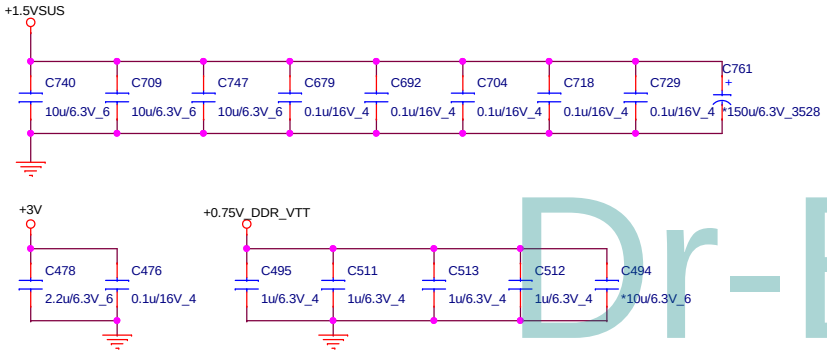
DDR3 DIMM-A (DDR)

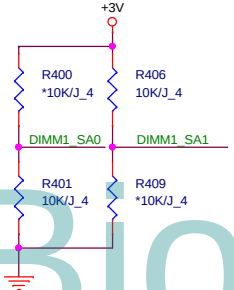






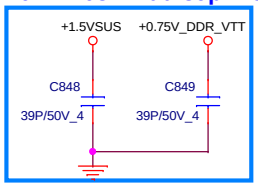
Place these Caps near SO_DIMM-A





	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1

20121203 : Add 39pF for ESD



Quanta Computer Inc.
PROJECT : ZQK

Size	Document Number	Rev
	DDR3 DIMMA-RSV H=5.2	1A
Date: Monday, January 07, 2013	Sheet 15 of 46	

Layout Notes:
+1.05_GFX trace width = 250mils

1000mA

+1.05V_GFX

To be placed no further from the GPU than bewteen BGA and Power supply
C207 EV@22u/6.3V_8
C208 EV@22u/6.3V_8
C171 EV@10u/6.3V_6
C183 EV@10u/6.3V_6
place near balls
C158 EV@4.7u/6.3V_6
C147 EV@1u/6.3V_4
place under BGA
C154 EV@1u/6.3V_4

+1.05V_GFX
To be placed no further from the GPU than bewteen BGA and Power supply
C226 EV@22u/6.3V_8
C225 EV@22u/6.3V_8
C246 EV@10u/6.3V_6
C247 EV@10u/6.3V_6
place near balls
C178 EV@4.7u/6.3V_6
C149 EV@1u/6.3V_4
place under BGA
C148 EV@1u/6.3V_4

2500mA

U35A

[PEG Interface]

AG19 PEX_IOVDD_1
AG21 PEX_IOVDD_2
AG22 PEX_IOVDD_3
AG24 PEX_IOVDD_4
AH21 PEX_IOVDD_5
AH25 PEX_IOVDD_6

AG13
AG15 PEX_IOVDDQ_1
AG16 PEX_IOVDDQ_2
AG18 PEX_IOVDDQ_3
AG25 PEX_IOVDDQ_4
AH15 PEX_IOVDDQ_5
AH18 PEX_IOVDDQ_6
AH26 PEX_IOVDDQ_7
AH27 PEX_IOVDDQ_8
AJ27 PEX_IOVDDQ_9
AK27 PEX_IOVDDQ_10
AL27 PEX_IOVDDQ_11
AM28 PEX_IOVDDQ_12
AM28 PEX_IOVDDQ_13
AN28 PEX_IOVDDQ_14

PEX_RX0	AN12	PEG_TX8_C	C629	EV@0.22u/10V_4
PEX_RX0_N	AM12	PEG_TX#8_C	C628	EV@0.22u/10V_4
PEX_RX1	AN14	PEG_TX9_C	C611	EV@0.22u/10V_4
PEX_RX1_N	AM14	PEG_TX#9_C	C612	EV@0.22u/10V_4
PEX_RX2	AP14	PEG_TX10_C	C627	EV@0.22u/10V_4
PEX_RX2_N	AP15	PEG_TX#10_C	C626	EV@0.22u/10V_4
PEX_RX3	AN15	PEG_TX11_C	C610	EV@0.22u/10V_4
PEX_RX3_N	AM15	PEG_TX#11_C	C609	EV@0.22u/10V_4
PEX_RX4	AN17	PEG_TX12_C	C624	EV@0.22u/10V_4
PEX_RX4_N	AM17	PEG_TX#12_C	C625	EV@0.22u/10V_4
PEX_RX5	AP17	PEG_TX13_C	C608	EV@0.22u/10V_4
PEX_RX5_N	AP18	PEG_TX#13_C	C607	EV@0.22u/10V_4
PEX_RX6	AN18	PEG_TX14_C	C623	EV@0.22u/10V_4
PEX_RX6_N	AM18	PEG_TX#14_C	C622	EV@0.22u/10V_4
PEX_RX7	AN20	PEG_TX15_C	C605	EV@0.22u/10V_4
PEX_RX7_N	AM20	PEG_TX#15_C	C606	EV@0.22u/10V_4
PEX_RX8	AP20			
PEX_RX8_N	AP21			
PEX_RX9	AN21			
PEX_RX9_N	AM21			
PEX_RX10	AN23			
PEX_RX10_N	AM23			
PEX_RX11	AP23			
PEX_RX11_N	AP24			
PEX_RX12	AN24			
PEX_RX12_N	AM24			
PEX_RX13	AN26			
PEX_RX13_N	AM26			
PEX_RX14	AP26			
PEX_RX14_N	AP27			
PEX_RX15	AN27			
PEX_RX15_N	AM27			

PEG_TX8 [2]
PEG_TX#8 [2]
PEG_TX9 [2]
PEG_TX#9 [2]
PEG_TX10 [2]
PEG_TX#10 [2]
PEG_TX11 [2]
PEG_TX#11 [2]
PEG_TX12 [2]
PEG_TX#12 [2]
PEG_TX13 [2]
PEG_TX#13 [2]
PEG_TX14 [2]
PEG_TX#14 [2]
PEG_TX15 [2]
PEG_TX#15 [2]

LAYOUT NOTES:
UNDAER: WITHIN 150MILS
NEAR: WITHIN 1378MILS

PEX_TX0	AK14	PEG_RX8_C	C197	EV@0.22u/10V_4
PEX_TX0_N	AJ14	PEG_RX#8_C	C198	EV@0.22u/10V_4
PEX_TX1	AH14	PEG_RX9_C	C216	EV@0.22u/10V_4
PEX_TX1_N	AG14	PEG_RX#9_C	C217	EV@0.22u/10V_4
PEX_TX2	AK15	PEG_RX10_C	C214	EV@0.22u/10V_4
PEX_TX2_N	AJ15	PEG_RX#10_C	C215	EV@0.22u/10V_4
PEX_TX3	AL16	PEG_RX11_C	C195	EV@0.22u/10V_4
PEX_TX3_N	AK16	PEG_RX#11_C	C196	EV@0.22u/10V_4
PEX_TX4	AK17	PEG_RX12_C	C213	EV@0.22u/10V_4
PEX_TX4_N	AJ17	PEG_RX#12_C	C212	EV@0.22u/10V_4
PEX_TX5	AH17	PEG_RX13_C	C194	EV@0.22u/10V_4
PEX_TX5_N	AG17	PEG_RX#13_C	C193	EV@0.22u/10V_4
PEX_TX6	AK18	PEG_RX14_C	C192	EV@0.22u/10V_4
PEX_TX6_N	AJ18	PEG_RX#14_C	C191	EV@0.22u/10V_4
PEX_TX7	AL19	PEG_RX15_C	C211	EV@0.22u/10V_4
PEX_TX7_N	AK19	PEG_RX#15_C	C210	EV@0.22u/10V_4
PEX_TX8	AK20			
PEX_TX8_N	AJ20			
PEX_TX9	AH20			
PEX_TX9_N	AG20			
PEX_TX10	AK21			
PEX_TX10_N	AJ21			
PEX_TX11	AL22			
PEX_TX11_N	AK22			
PEX_TX12	AK23			
PEX_TX12_N	AJ23			
PEX_TX13	AH23			
PEX_TX13_N	AG23			
PEX_TX14	AK24			
PEX_TX14_N	AJ24			
PEX_TX15	AL25			
PEX_TX15_N	AK25			

PEG_RX8 [2]
PEG_RX#8 [2]
PEG_RX9 [2]
PEG_RX#9 [2]
PEG_RX10 [2]
PEG_RX#10 [2]
PEG_RX11 [2]
PEG_RX#11 [2]
PEG_RX12 [2]
PEG_RX#12 [2]
PEG_RX13 [2]
PEG_RX#13 [2]
PEG_RX14 [2]
PEG_RX#14 [2]
PEG_RX15 [2]
PEG_RX#15 [2]

PEX_REFCLK AL13 — CLK_PCIE_VGAP [9]
PEX_REFCLK_N AK13 — CLK_PCIE_VGAN [9]

PEX_TSTCLK_OUT AJ26 PEX_TSTCLK R186 *EV@200/F_4
PEX_TSTCLK_OUT_N AK26 PEX_TSTCLK#

0815 change R53 to 1% tolerance

PEX_WAKE AJ11 PEGX_WAKE — TP26
PEX_RST_N AJ12 PEGX_RST#

PEX_CLKREQ_N AK12 PEX_CLKREQ#

PEX_TERMP AP29 PEX_TERMP R590 EV@2.49K/F_4
TESTMODE R195 EV@10K/F_4
TESTMODE AK11

PEX_PLLVDD AG26
PEX_PLL_HVDD AH12
PEX_SVDD_3V3 AG12
3.3V_AUX_NC P8
VDD_SENSE L4
GND_SENSE L5

EV@N14P_GV2

0817 RSVD R46 and C49 for GV2 co-layout sDDR3

PEX_PLLVDD : 0.3MM = 12mils (150mA)

PEX_PLLVDD R207 EV@0_6 — +1.05V_GFX

Place near BGA
C185 EV@4.7u/6.3V_6
C145 EV@1u/6.3V_4
C163 EV@0.1u/10V_4
PLACE UNDAER BALLS
C199 *EV@1u/6.3V_4

C72 EV@0.1u/10V_4
C89 EV@4.7u/6.3V_6
C99 EV@4.7u/6.3V_6
+3V_GFX
PLACE NEAR BALLS

AH12/AG12 need 210mA of +3V_GFX

GPU_VCCP_SENSE [43]
GPU_VSSP_SENSE [43]

8mils width (0.2MM)

1001：Remove 3V3MISC by FAE Nelson suggestion
FAE：Please use +3V_GFX to instead 3V3MISC power rail

1001：Remove 3V3MISC's Cap by FAE Nelson suggestion

PLACE NEAR TO GPU BALLS

PLACE UNDER GPU BALLS

1001：Remove 3V3MISC by FAE Nelson suggestion
FAE：Please use +3V_GFX to instead 3V3MISC power rail

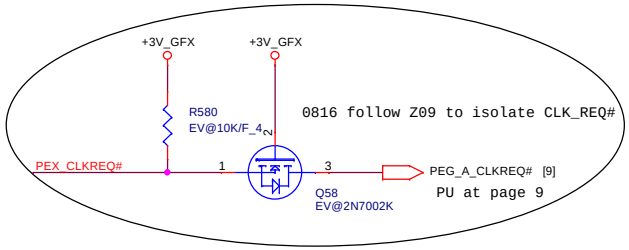
+3V_GFX
L8/M8/K8/J8 0.4MM = 16mils

J8 VDD33_1
K8 VDD33_2
L8 VDD33_3
M8 VDD33_4

PLACE NEAR TO GPU L8/M8
+3V_GFX
C144 EV@4.7u/6.3V_6
C152 *EV@1u/6.3V_4
C153 EV@0.1u/10V_4
C59 EV@0.1u/10V_4
C65 *EV@0.1u/10V_4
PLACE UNDAER GPU BALLS L8/M8

AC6 NC_1
AJ28 NC_2
AJ4 NC_3
AJ5 NC_4
AL11 NC_5
C15 NC_6
D19 NC_7
D20 NC_8
D23 NC_9
D26 NC_10
H31 NC_11
T8 NC_12
V32 NC_13

Layout Notes:
Place decoupling CAPs close to GPU



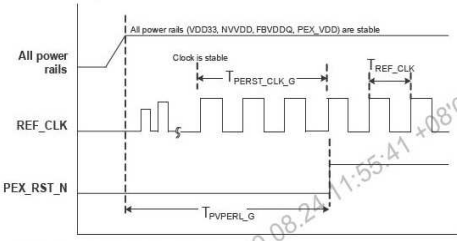
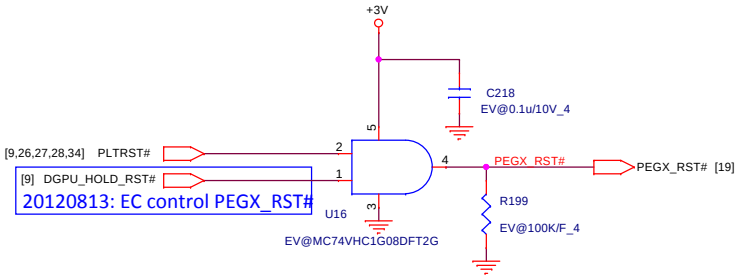


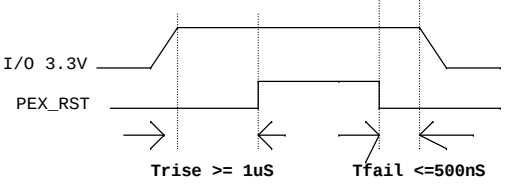
Figure 3-18. PEX_RST_N Timing for GPU

Table 3-8. N11x Reset Requirements for PCI Express 2.0

Constraint Parameter	Requirement	Notes
T_{PVPERL_G}	$T_{PVPERL\_G} \geq 1us$	
$T_{PERST\_CLK\_G}$	$T_{PERST\_CLK\_G} \geq 1T_{REF\_CLK}$	



PEX_RST timing



Quanta Computer Inc.
PROJECT : ZQK

Size	Document Number	Rev
	DGPU 1/5 (PEG)	1A

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U35B [MEMORY I/F A]

U35C MEMORY I/F C

DBI

EDC

0816 follow DG to place caps

LAYOUT NOTES:
UNDAER: WITHIN 150MILS
NEAR: WITHIN 1378MILS

PLACE UNDER GPU BALLS

0.1u x 6 stuff x4

1u x 6 stuff x4

4.7u x 6 stuff x4

PLACE NEAR TO GPU BALLS

10u x 4 stuff x2

22u x 4 stuff x2

15mils width

0815 no stuff follow CRB

GC6 connect to EC

C6218 close ball K27 35mA

PLACE NEAR TO GPU BALLS
PLACE UNDER GPU BALLS
+FB_PLLAVDD = 0.3mm 12mils
U27+H17 62mA

1012(FAE)：Reserve +FB_PLLAVDD evan without CH-B

C107 close to ball H17

0815 confirm with ZQS (sDDR3)

0813
sDDR3
R1=42.2/F
R2=51.1/F

Layout Notes: PLACE CLOSE TO GPU BALLS

RSVD 330u, ZQS have one

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PROJECT : ZQK

Size	Document Number	Rev
	DGPU 2/5 (Memory)	1A

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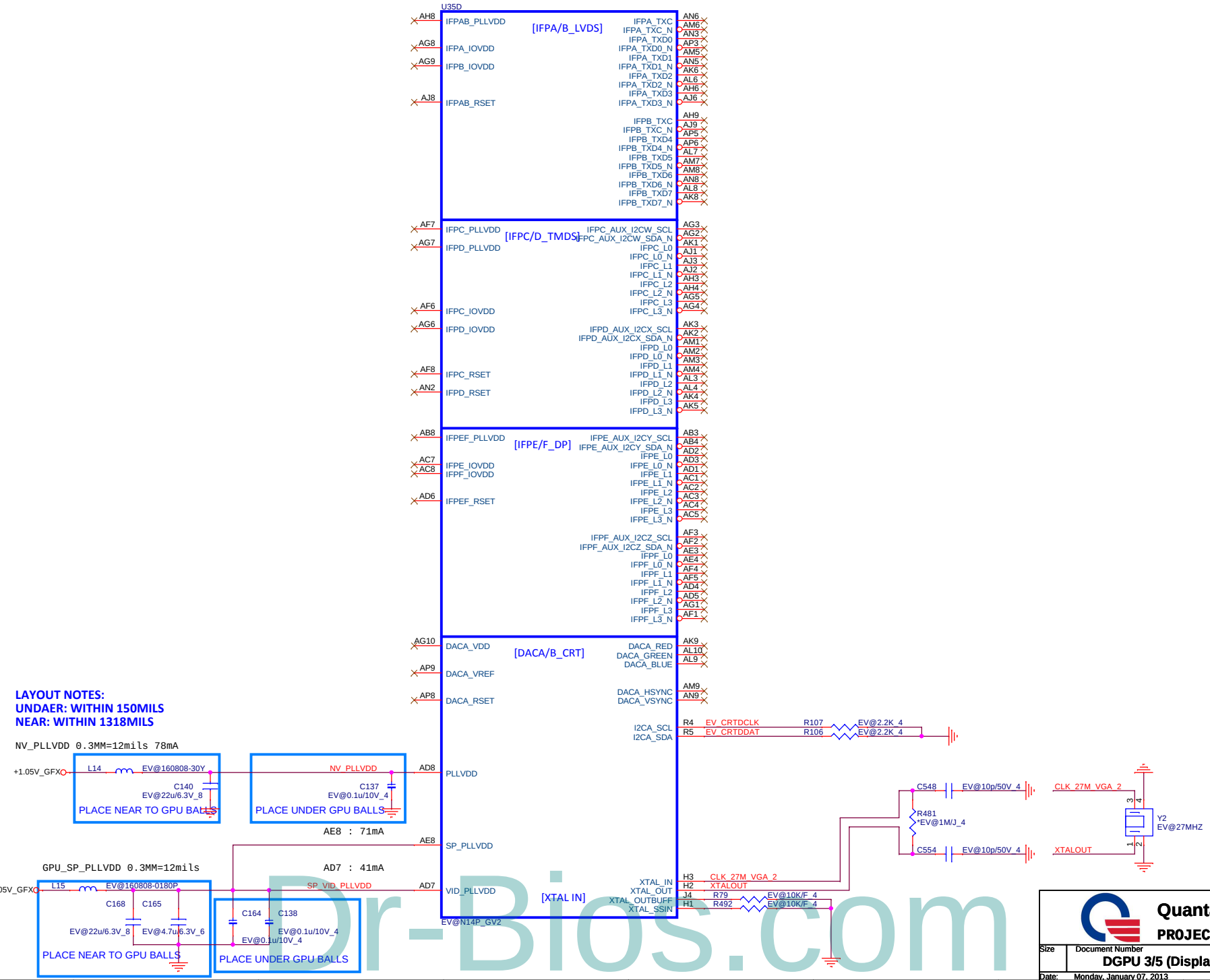

Quanta Computer Inc.
PROJECT : ZQK

Size	Document Number	Rev
	DGPU 3/5 (Display)	1A

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Logical Strap Bit Mapping

	PU-VDD	PD
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	FB_1	FB_0	SMB_ALT_ADDR	VGA_DEVICE	1000
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM	1292
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	0010
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	0000
STRAP4	RESERVED	PCIE SPEED CHANGE GEN3	PCIE_MAX SPEED	DP_PLL_VDD33	0111

STRAP3
Optimus ---> 4.99k PD
Discrete only ---> 15K PD

Resistor P/N
4.99K---> CS24992FB26
10K ---> CS31002FB26
15K ---> CS31502FB24
20K ---> CS32002FB29
24.9K---> CS32492FB16
30.1K---> CS33012FB18
34.8K---> CS33482FB22
45.3K---> CS34532FB18

Table 123 Binary Strap Mode Mapping

Strap Pin Name	Strap Mapping	Resistance	Polarity
ROM_SCLK	SMB_ALT_ADDR	10k Ω	Pull-down to GND
ROM_SI	SUB_VENDOR	10k Ω	Pull-up to 3V3 if VBIOS ROM exists Pull-down to GND if no VBIOS ROM
ROM_SO	VGA_DEVICE	10k Ω	Pull-down to GND (no display)
STRAP0	RAM_CFG[0]	10k Ω	See Note below
STRAP1	RAM_CFG[1]	10k Ω	See Note below
STRAP2	RAM_CFG[2]	10k Ω	See Note below
STRAP3	RAM_CFG[3]	10k Ω	See Note below
STRAP4	PCIE_MAX_SPEED	10k Ω	Pull-down to GND

N14M-GE device ID is 0x1140
N14M-GE is use binary strap setting
A.ROM_SI - 10K pull down
B.ROM_SO - 10K pull down
F.STRAP 3 - 10k pull down

Micron : MT41K256M16HA-107G:E (QPN = AKD5PGSTL05)
strap= 0xD =(0x1101)
STRAP 3&2&0 =10K Pull high
STRAP 1= 10K Pull down

1001 : Remove 3V3MISC by FAE Nelson suggestion
FAE : Please use +3V_GFX to instead 3V3MISC power rail

A.ROM_SI - Memeory strap
B.ROM_SO - 5K pull high
D.STRAP 0 - 45k pull high
E.STRAP 1 : GV2- 45K pull down
GT - 5K pull down
F.STRAP 3 - 5k pull down

C2.For N14P-GV2+SDDR3 sku
N14P-GV2 QS device ID=0x1292 'This is QS device ID
1.ROM_SCLK =5K pull high
2.STRAP2= 15k pull down
3.STRAP4=45 pull down 'For N14P-GV2 QS

N14P-GT device ID=0x0FE4
1.ROM_SCLK =15K pull down
2.STRAP2= 25k pull down
3.STRAP4=45K pull down

0817 : FB_CLAMP have PD, EC programing to avoid leakage
0928 FAE Nelson : Add a MOS to avoid power leakage issue pin 2 connect to +3V_GFX power rail

0928 FAE Nelson : Please add 10k pull up to +3V on FB_CLAMP_REQ# signal also

0816 EC programing GPI

PSI stuff 10k at GPU side ready, remove power page of pu 10k
GPIO20/21 available on N14P-GV2

R3	
N14x others	40.2K
N14M-GE/GL	NC

GPIO8 VGA thrmtrip# => inform EC over temperature protect

0816 dGPU_OTP# = EC control

0816 dGPU_ALT# = EC control

GPIO9 for ADPS circuit to infrom EC NV dGPU VPS Alert

0817 CEC is NC for GK107

GPIO12 HW throttle over power protect

0816 dGPU_OPP# = EC control

GPIO12 AC detect
AC high
DC low

0815 RSVD VGPU_TALERT# to throttle GPU power

SMBus (VGA)

1001 : Remove 3V3MISC by FAE Nelson suggestion
FAE : Please use +3V_GFX to instead 3V3MISC power rail

EC/S5

VGA/+3V_GFX

Table 3. N14M-GS/LP and N14P-GV2 DDR3 Recommended Memories 128Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CK (MHz)	Memory Date Code Minimum	Status
128Mx16 DDR3	Samsung	0x7	1.5 V/ 1.5 V	K4W2G1646E-BC1A	1000	1204	Production Candidate
				K4W2G1646E-BC11	900	1204	Production Candidate
	Micron	0x5	1.5 V/ 1.5 V	MT41J128M16JT-093G:K	1000	1150	Production Candidate
				MT41J128M16JT-107G:K	900	1150	Production Candidate
256Mx16 DDR3	Samsung	0x3	1.5 V/ 1.5 V	K4W4G1646B-HC11	900	H/A	Production Candidate
	Micron	0x1	1.5 V/ 1.5 V	MT41K256M16HA-107G:E	900	H/A	Production Candidate

Table 8. N14P-GS/LP/GE/GT DDR3 Recommended Memories 128Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CK (MHz)	Memory Date Code Minimum	Status
128M~16 DDR3	Samsung	0x7	1.5 V/ 1.5 V	K4W2G1646E-BC1A	1000	1204	Production ready
				K4W2G1646E-BC11	900	1204	Production ready
	Micron	0x5	1.5 V/ 1.5 V	MT41J128M16JT-093G:K	1000	1234	Production ready
				MT41J128M16JT-107G:K	900	1150	Production ready
	Hynix	0x6	1.5V/ 1.5V	H5TQ2G63DFR-H0C	1000	H/A	Production Candidate
				H5TQ2G63DFR-11C	900	H/A	Production Candidate

Table 2. N14M-GE/GL DDR3 Recommended Memories 256Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CK (MHz)	Memory Date Code Minimum	Status
256M~16 DDR3	Samsung	0x8	1.5 V/ 1.5 V	K4W4G1646B-HC11	900	H/A	Production ready
	Micron	0xD	1.5 V/ 1.5 V	MT41K256M16HA-107G:E	900	H/A	Production ready
	Hynix	0x3	1.5V/ 1.5V	H5TQ4G63MFR-11C	900	H/A	Production ready
		0x4		H5TQ4G63AFR-11C		H/A	Post Production Candidate

Table 1. N14M-GE/GL DDR3 Recommended Memories 128Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CK (MHz)	Memory Date Code Minimum	Status
128M~16 DDR3	Micron	0x1	1.5 V/ 1.5 V	MT41J128M16JT-093G:K	1000	1234	Production ready
				MT41J128M16JT-107G:K	900	1150	Production ready
	Samsung	0x5	1.5 V/ 1.5 V	K4W2G1646E-BC1A	1000	1204	Production ready
				K4W2G1646E-BC11	900	1204	Production ready
	Hynix	0x6	1.5V/ 1.5V	H5TQ2G63DFR-H0C	1000	H/A	Production ready
				H5TQ2G63DFR-11C	900	H/A	Production ready

Vender	Strap	Q PN	Mfr. PN	Freq.	GPU
Micron	0001	AKD5PGSTL05	MT41K256M16HA-107G:E	900MHz	N14P-GT1 & GV2
Hynix	0110	AKD5MGWTW17	H5TQ2G63DFR-11C	900MHz	N14P-GT

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+VGPU_CORE

U35F [GPU VDD] EV@N14P_GV2

AA12	VDD_001	XVDD_001	U1
AA14	VDD_002	XVDD_002	U2
AA16	VDD_003	XVDD_003	U3
AA19	VDD_004	XVDD_004	U4
AA21	VDD_005	XVDD_005	U5
AA23	VDD_006	XVDD_006	U6
AB13	VDD_007	XVDD_007	U7
AB15	VDD_008	XVDD_008	U8
AB17	VDD_009	XVDD_009	V1
AB18	VDD_010	XVDD_010	V2
AB20	VDD_011	XVDD_011	V3
AB22	VDD_012	XVDD_012	V4
AC12	VDD_013	XVDD_013	V5
AC14	VDD_014	XVDD_014	V6
AC16	VDD_015	XVDD_015	V7
AC19	VDD_016	XVDD_016	V8
AC21	VDD_017	XVDD_017	W2
AC23	VDD_018	XVDD_018	W3
M12	VDD_019	XVDD_019	W4
M14	VDD_020	XVDD_020	W5
M16	VDD_021	XVDD_021	W7
M19	VDD_022	XVDD_022	W8
M21	VDD_023	XVDD_023	Y1
M23	VDD_024	XVDD_024	Y2
N13	VDD_025	XVDD_025	Y3
N15	VDD_026	XVDD_026	Y4
N17	VDD_027	XVDD_027	Y5
N18	VDD_028	XVDD_028	Y6
N20	VDD_029	XVDD_029	Y7
N22	VDD_030	XVDD_030	Y8
P12	VDD_031	XVDD_031	AA1
P14	VDD_032	XVDD_032	AA2
P16	VDD_033	XVDD_033	AA3
P19	VDD_034	XVDD_034	AA4
P21	VDD_035	XVDD_035	AA5
P23	VDD_036	XVDD_036	AA6
R13	VDD_037	XVDD_037	AA7
R15	VDD_038	XVDD_038	AA8
R17	VDD_039		
R18	VDD_040		
R20	VDD_041		
R22	VDD_042		
T12	VDD_043		
T14	VDD_044		
T16	VDD_045		
T19	VDD_046		
T21	VDD_047		
T23	VDD_048		
U13	VDD_049		
U15	VDD_050		
U17	VDD_051		
U18	VDD_052		
U20	VDD_053		
U22	VDD_054		
V13	VDD_055		
V15	VDD_056		
V17	VDD_057		
V18	VDD_058		
V20	VDD_059		
V22	VDD_060		
W12	VDD_061		
W14	VDD_062		
W16	VDD_063		
W19	VDD_064		
W21	VDD_065		
W23	VDD_066		
Y13	VDD_067		
Y15	VDD_068		
Y18	VDD_069		
Y17	VDD_070		
Y20	VDD_071		
Y22	VDD_072		

U35G [GPU GND] EV@N14P_GV2

A2	GND_1	GND_101	D2
AA17	GND_2	GND_102	D31
AA18	GND_3	GND_103	D33
AA20	GND_4	GND_104	E10
AA22	GND_5	GND_105	E22
AB12	GND_6	GND_106	E25
AB14	GND_7	GND_107	E5
AB16	GND_8	GND_108	E7
AB19	GND_9	GND_109	F28
AB2	GND_10	GND_110	F7
AB21	GND_11	GND_111	G10
A33	GND_12	GND_112	G13
AB23	GND_13	GND_113	G16
AB28	GND_14	GND_114	G19
AB30	GND_15	GND_115	G2
AB32	GND_16	GND_116	G22
AB5	GND_17	GND_117	G25
AB7	GND_18	GND_118	G28
AC13	GND_19	GND_119	G3
AC15	GND_20	GND_120	G30
AC17	GND_21	GND_121	G32
AC18	GND_22	GND_122	G33
AA13	GND_23	GND_123	G5
AC20	GND_24	GND_124	G7
AC22	GND_25	GND_125	K2
AE2	GND_26	GND_126	K28
AE28	GND_27	GND_127	K30
AE30	GND_28	GND_128	K32
AE32	GND_29	GND_129	K33
AE33	GND_30	GND_130	K5
AE5	GND_31	GND_131	K7
AE7	GND_32	GND_132	M13
AH10	GND_33	GND_133	M15
AA15	GND_34	GND_134	M17
AH13	GND_35	GND_135	M18
AH16	GND_36	GND_136	M20
AH19	GND_37	GND_137	M22
AH2	GND_38	GND_138	N12
AH22	GND_39	GND_139	N14
AH24	GND_40	GND_140	N16
AH28	GND_41	GND_141	N19
AH29	GND_42	GND_142	N2
AH30	GND_43	GND_143	N21
AH32	GND_44	GND_144	N23
AH33	GND_45	GND_145	N28
AH5	GND_46	GND_146	N30
AH7	GND_47	GND_147	N32
AJ7	GND_48	GND_148	N33
AK10	GND_49	GND_149	N5
AK7	GND_50	GND_150	N7
AL12	GND_51	GND_151	P13
AL14	GND_52	GND_152	P15
AL15	GND_53	GND_153	P17
AL17	GND_54	GND_154	P18
AL18	GND_55	GND_155	P20
AL2	GND_56	GND_156	P22
AL20	GND_57	GND_157	R12
AL21	GND_58	GND_158	R14
AL23	GND_59	GND_159	R16
AL24	GND_60	GND_160	R19
AL26	GND_61	GND_161	R21
AL28	GND_62	GND_162	R23
AL30	GND_63	GND_163	T13
AL32	GND_64	GND_164	T15
AL33	GND_65	GND_165	T17
AL5	GND_66	GND_166	T18
AM13	GND_67	GND_167	T2
AM16	GND_68	GND_168	T20
AM19	GND_69	GND_169	T22
AM22	GND_70	GND_170	AG11
AM25	GND_71	GND_171	T28
AN1	GND_72	GND_172	T32
AN10	GND_73	GND_173	T5
AN13	GND_74	GND_174	T7
AN16	GND_75	GND_175	U12
AN19	GND_76	GND_176	U14
AN22	GND_77	GND_177	U16
AN25	GND_78	GND_178	U19
AN30	GND_79	GND_179	U21
AN34	GND_80	GND_180	U23
AN4	GND_81	GND_181	V12
AN7	GND_82	GND_182	V14
AP2	GND_83	GND_183	V16
AP33	GND_84	GND_184	V19
B1	GND_85	GND_185	V21
B19	GND_86	GND_186	V23
B22	GND_87	GND_187	W13
B25	GND_88	GND_188	W15
B28	GND_89	GND_189	W17
B31	GND_90	GND_190	W19
B34	GND_91	GND_191	W20
B4	GND_92	GND_192	W22
B7	GND_93	GND_193	W28
C10	GND_94	GND_194	Y12
C13	GND_95	GND_195	Y14
C19	GND_96	GND_196	Y16
C22	GND_97	GND_197	Y19
C25	GND_98	GND_198	Y21
C28	GND_99	GND_199	Y23
C7	GND_100	GND_200	AH11
			C16
		GND_OPT_1	
		GND_OPT_2	W32

+VGPU_CORE

C596 EV@330u/2V_7343

Power request ESR

PLACE UNDER GPU BALLS

+VGPU_CORE 0.1uF x 8 population x 4

C90	EV@0.1u/10V_4
C98	EV@0.1u/10V_4
C91	EV@0.1u/10V_4
C108	EV@0.1u/10V_4
C97	*EV@0.1u/10V_4
C116	*EV@0.1u/10V_4
C107	*EV@0.1u/10V_4
C115	*EV@0.1u/10V_4

LAYOUT NOTES:
UNDAER: WITHIN 150MILS
NEAR: WITHIN 1378MILS

PLACE UNDER GPU BALLS

+VGPU_CORE 4.7uF x 15 population x10

C102	C100	C117	C129	C103	C88	C69	C82
EV@4.7u/6.3V_6	EV@4.7u/6.3V_6	EV@4.7u/6.3V_6	EV@4.7u/6.3V_6	EV@4.7u/6.3V_6	EV@4.7u/6.3V_6	EV@4.7u/6.3V_6	EV@4.7u/6.3V_6

+VGPU_CORE

C83	C104	C113	C121	C101	C122	C133
EV@4.7u/6.3V_6	EV@4.7u/6.3V_6	*EV@4.7u/6.3V_6	*EV@4.7u/6.3V_6	*EV@4.7u/6.3V_6	*EV@4.7u/6.3V_6	*EV@4.7u/6.3V_6

PLACE NEAR TO GPU BALLS

+VGPU_CORE 47u x1 22u x7 4.7u x6 330u x1 stuff x 1 stuff x 5 RSVD by DG

C617	C128	C599	C597	C132	C111	C112	C588
EV@330u/2.5V_3528	EV@47u/6.3V_8	EV@22u/6.3V_8	EV@4.7u/25V_8	EV@4.7u/25V_8	EV@4.7u/25V_8	EV@4.7u/25V_8	EV@4.7u/25V_8

+VGPU_CORE 0817 RSVD more NVVDD caps by NV DG

C92	C93	C74	C73	C592	C124	C127
*EV@22u/6.3V_8	*EV@22u/6.3V_8	*EV@22u/6.3V_8	*EV@22u/6.3V_8	*EV@22u/6.3V_8	*EV@22u/6.3V_8	*EV@4.7u/25V_8

+1.05V_GFX R187 EV@4.7K/J_4 DGPU_POK2 C175 *EV@1000P/50V_4 Q20 EV@MMBT3904-7-F DGPU_PGOK-1

+1.5V_GFX R167 EV@4.7K/J_4 DGPU_POK4 C146 *EV@1000P/50V_4 R176 *EV@0_4 Q19 EV@MMBT3904-7-F DGPU_POK_O

+3V_GFX R140 EV@4.7K/J_4 DGPU_PWROK [10]

+3V R161 EV@4.7K/J_4 C123 EV@1000P/50V_4 Q15 EV@DTC144EUA R147 EV@100K/F_4

0814 POWER GD connect to EC

for meet Power down sequence
for +3V_GFX

+VGPU_CORE D3 EV@RB500V-40 +3V_GFX

+1.5V_GFX D2 *EV@RB500V-40

20120911: D6002 no stuff when GC6 support.

+3V C87 *EV@0.1u/10V_4 HWPG_1.5VGFX VGPU_PWRGD U12 EV@MC74VHC1G08DFT2G 1.05V_GFX_EN [42] R103 *EV@0_4

PU at page 43

0816 GC6 need system 3V to control FBVDDQ

+3V C71 EV@0.1u/10V_4 [42] FBVDDQ_EN R83 EV@100K/F_4 U11 EV@74AHC1G32GW EC_FB_CLAMP [17,19,34] VGPU_PWRGD_R R82 EV@0/J_4 R87 *EV@0_4 C70 *EV@0.1u/10V_4 VGPU_PWRGD [43] DGPU_VRON [10,43]

20120914: H/W Add for HWPG_1.5VGFX
20121018: Circuit combination

+3V R59 EV@4.7K/J_4 DGPU_POK_O C49 EV@1000p/50V_4

+3V_GFX R43 EV@4.7K/J_4 Q5 EV@DTC144EUA R49 EV@100K/F_4 HWPG_1.5VGFX

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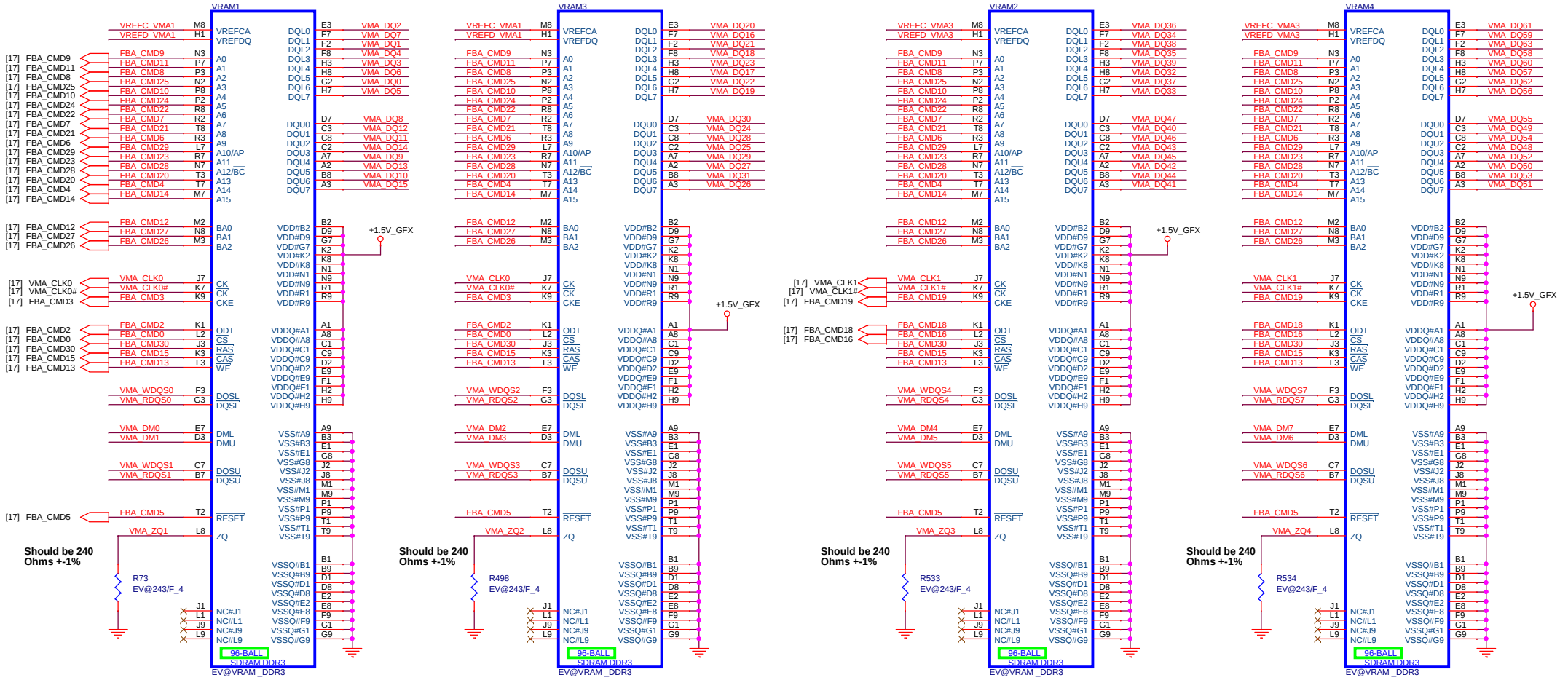
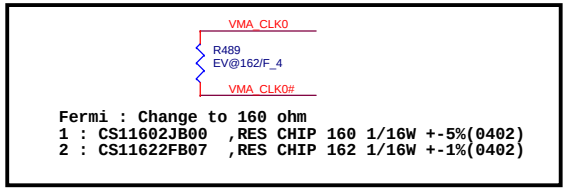
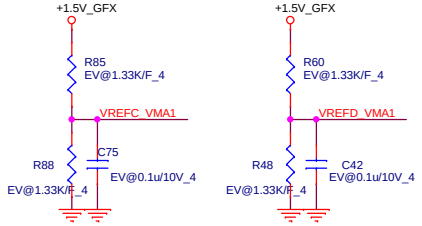
CHANNEL A: 1024MB DDR3

[17] VMA_DQ[63..0]
[17] VMA_DM[7..0]
[17] VMA_WDQS[7..0]
[17] VMA_RDQS[7..0]



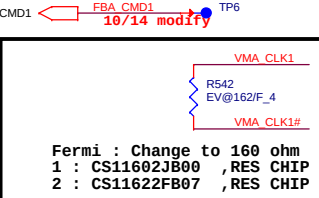
Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

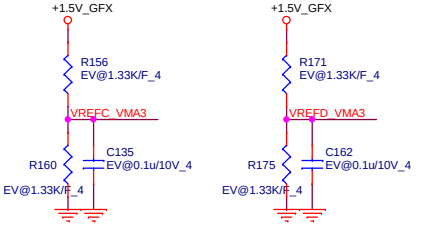


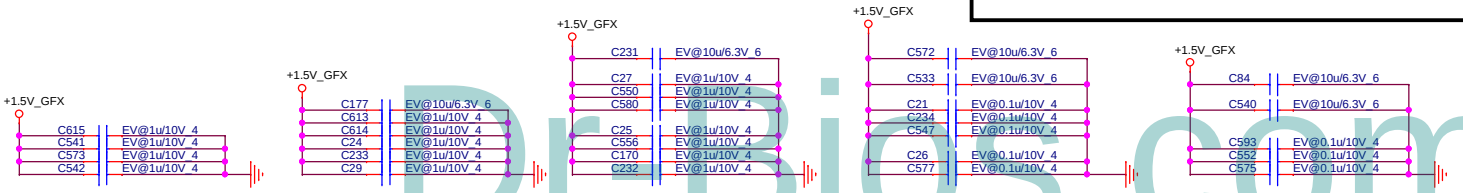


[17] FBA_CMD17 → FBA_CMD17 → TP11
[17] FBA_CMD1 → FBA_CMD1 → TP6
10/14 modify

Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)







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PROJECT : ZQK

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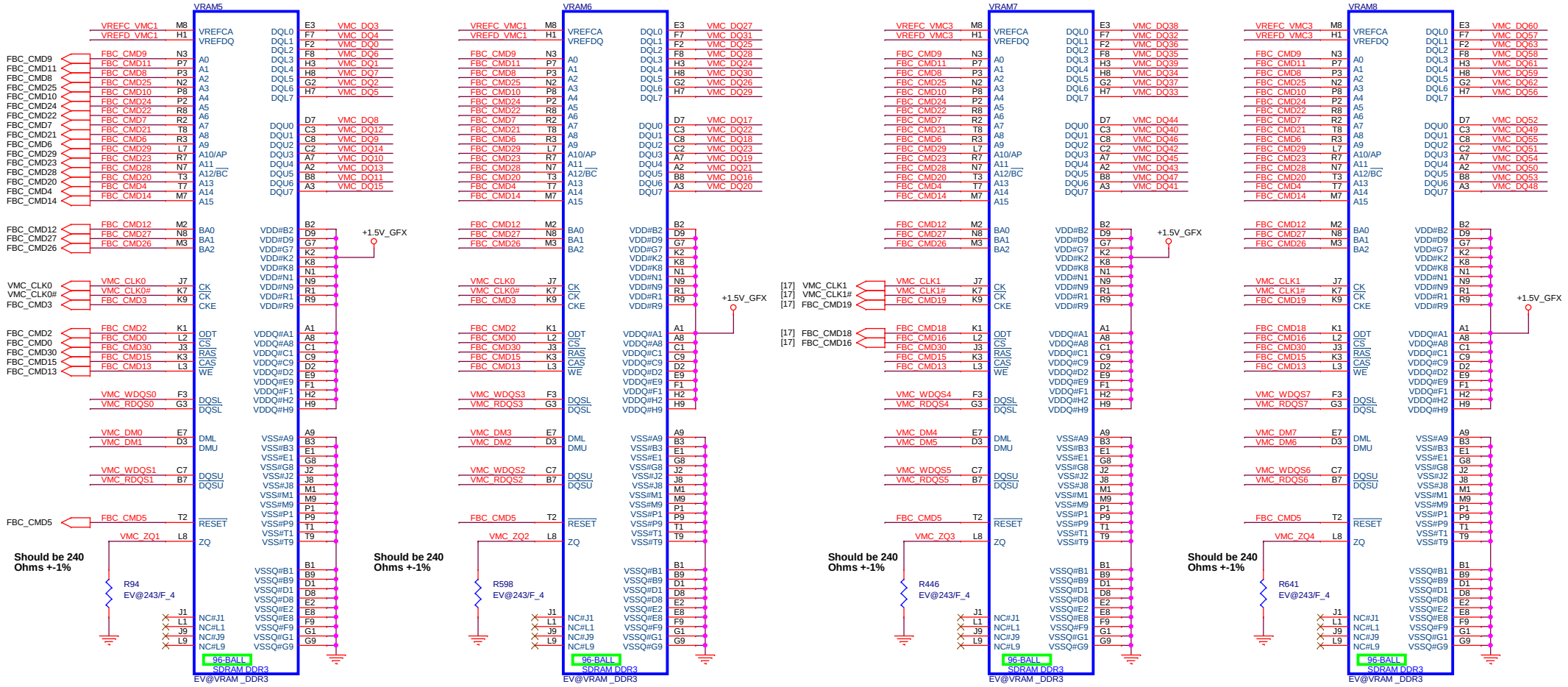
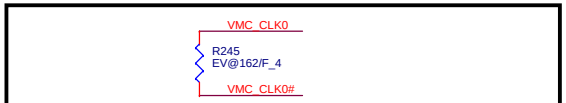
HYNIX 900MHz 1G AKD5LZWTW02
HYNIX 900MHz 2G AKD5MGWTW16

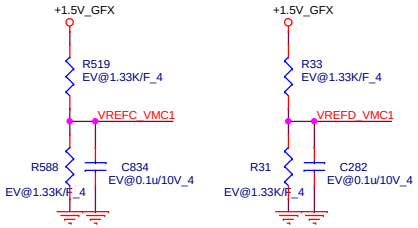
CHANNEL B: 1024MB DDR3

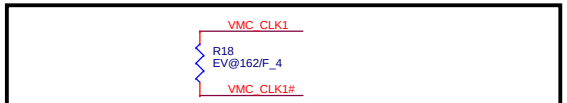
[17] VMC_DQ[63..0]
[17] VMC_DM[7..0]
[17] VMC_WDQS[7..0]
[17] VMC_RDQS[7..0]



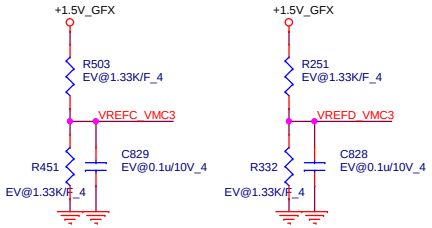
Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

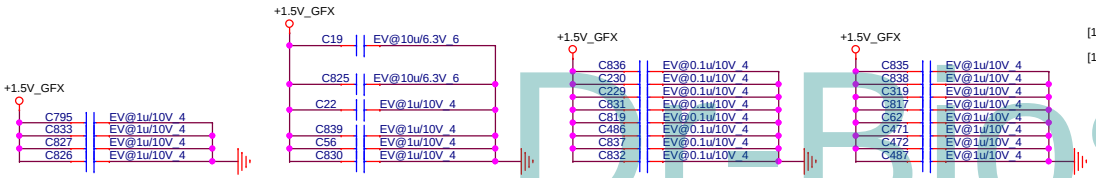


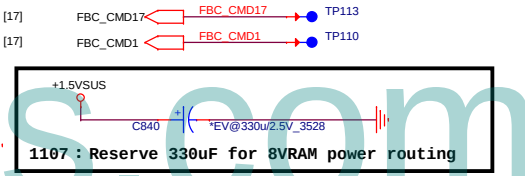




Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)







1107 : Reserve 330uF for 8VRAM power routing

Quanta Computer Inc.
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Size	Document Number	Rev
	N13P-LP DDR3 VRAM 2/2	1A
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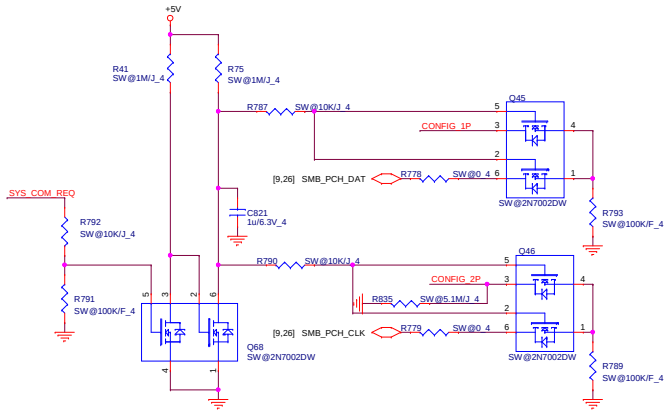
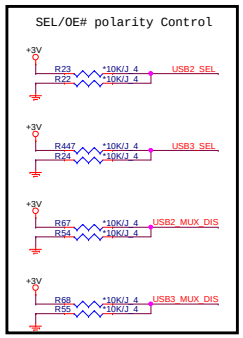
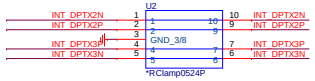
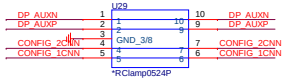
mini DP ML (DPP)

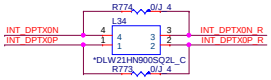


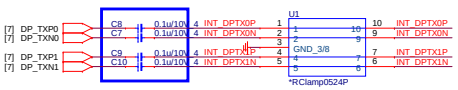


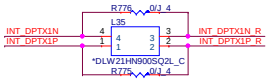
ESD Protect (EMC)





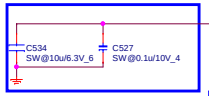


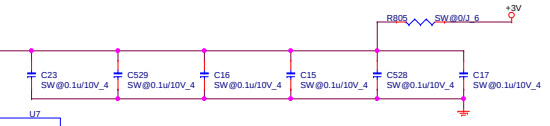




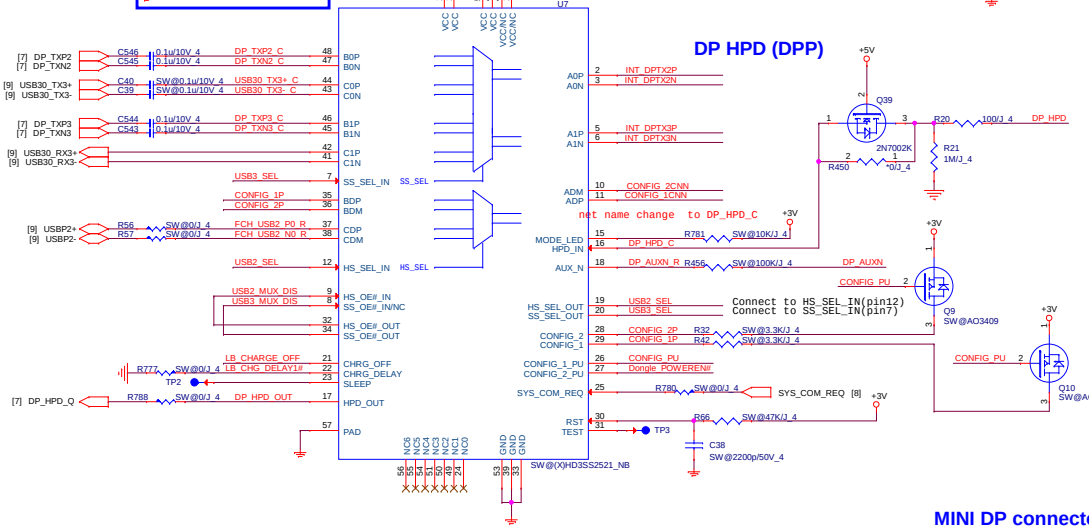
Layout Notes:
Place decoupling CAPs close to Connector Close to DP connector

Layout Notes:
Place near Pin13 and Pin14

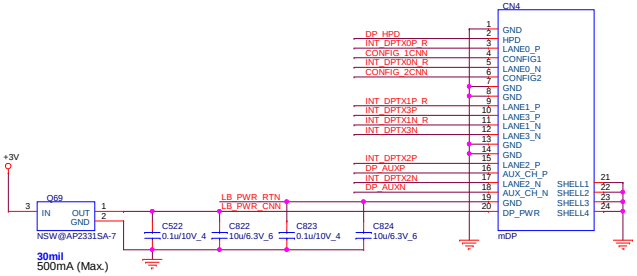




DP HPD (DPP)

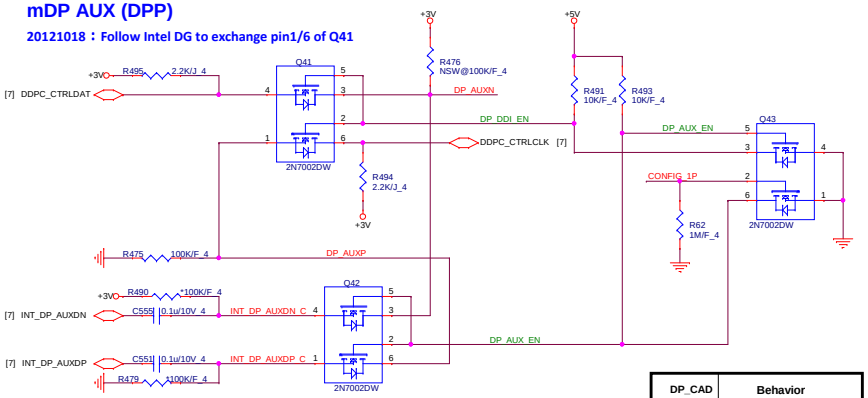


MINI DP connector (DPP)

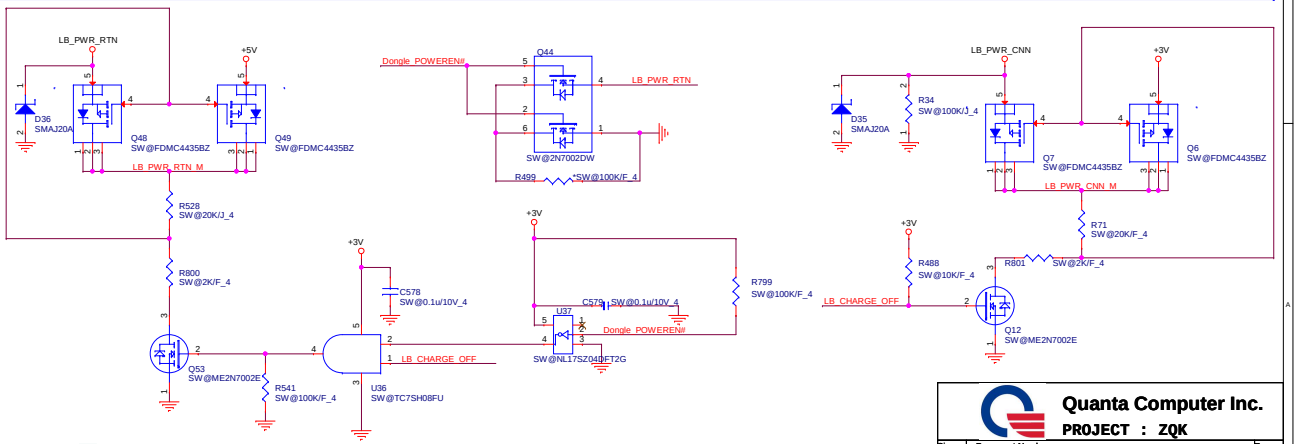


mDP AUX (DPP)

20121018：Follow Intel DG to exchange pin1/6 of Q41



DP_CAD	Behavior
Low	DP signal (AC couple)
High	TMDS signal (DC couple)



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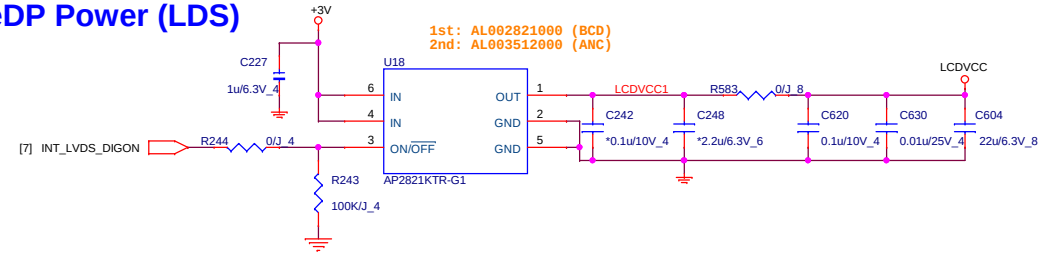
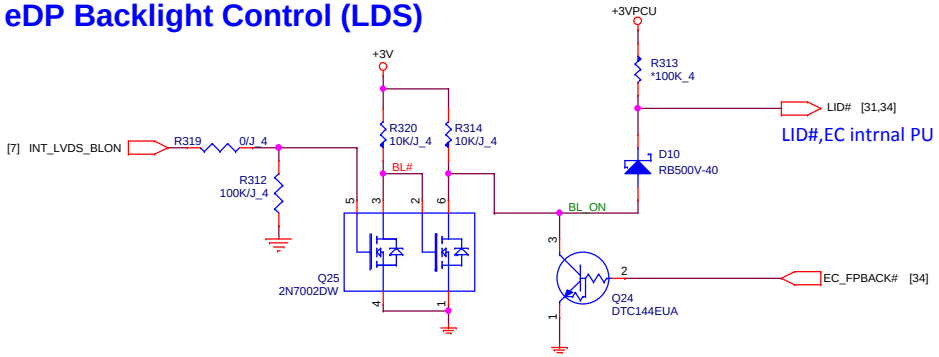
eDP Power (LDS)

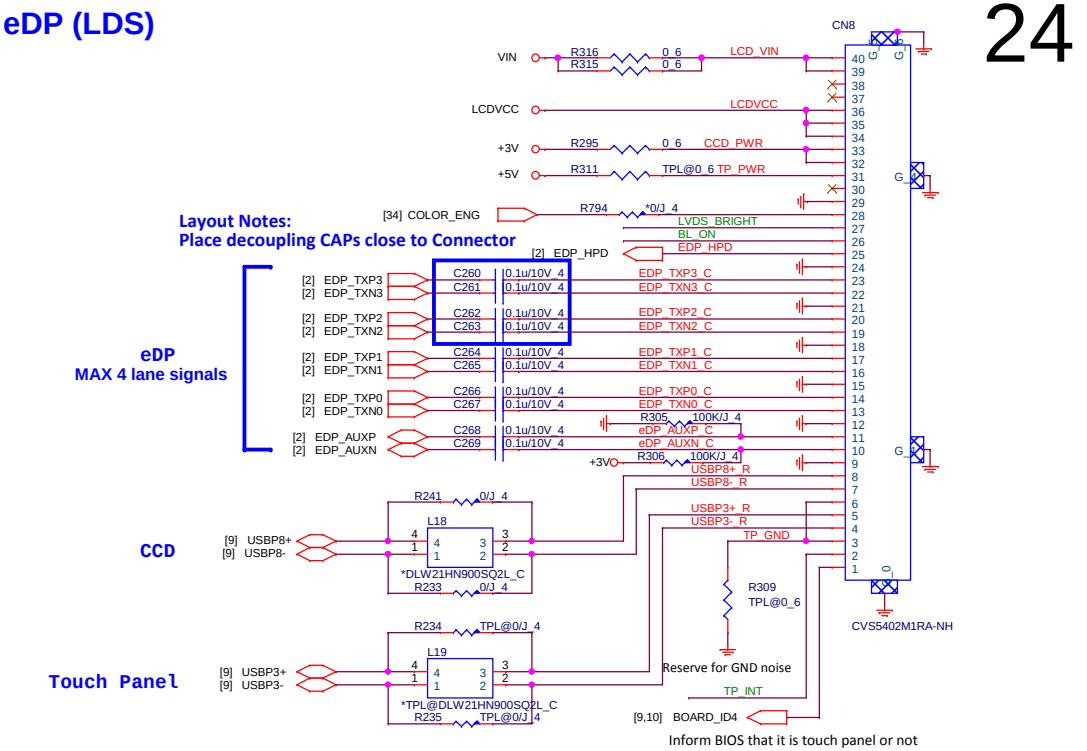


eDP Backlight Control (LDS)

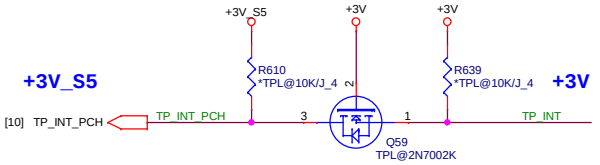


eDP Brightness Control (LDS)

eDP (LDS)



Touch Panel interrupt signal：
1016：Exchange Q59 pin 1 & 3 direction to prevent leakage



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Size	Document Number	Rev
	eDP/CAMERA/LID	1A
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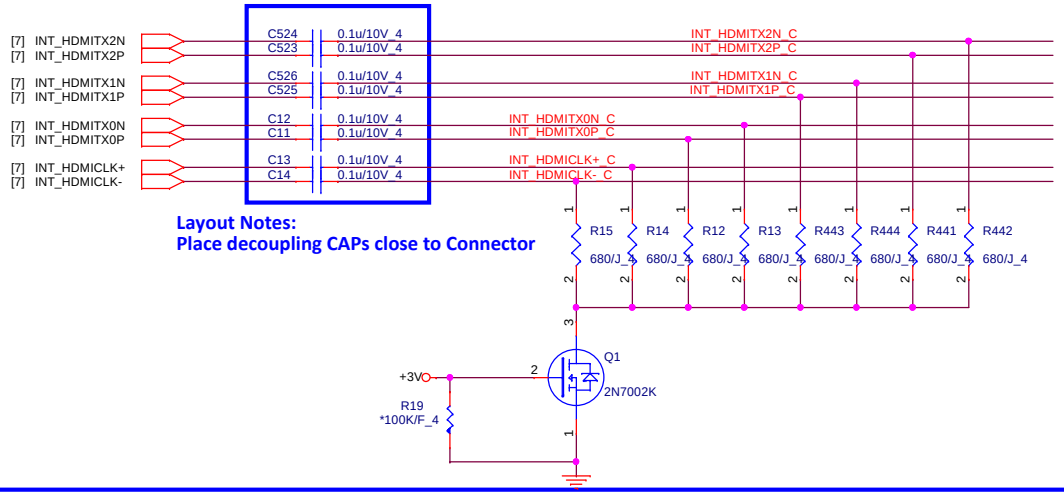
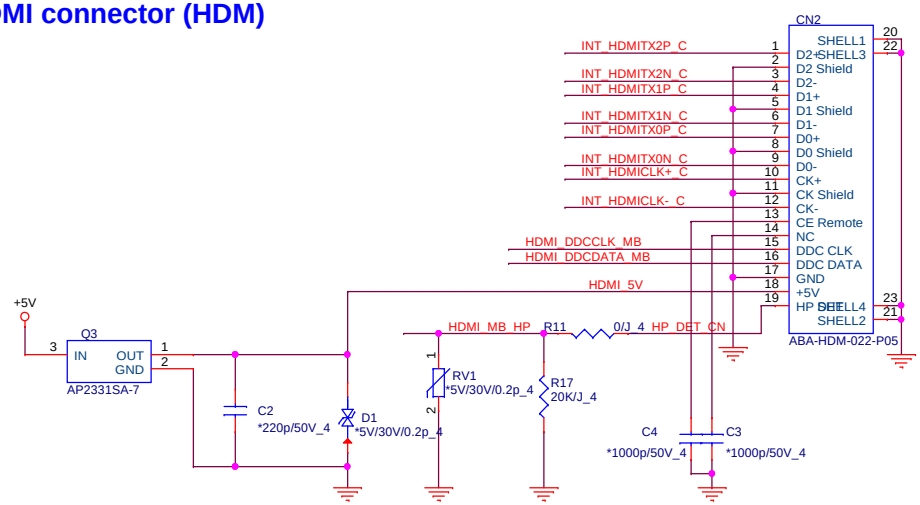
HDMI Cost Reduced level shift (HDM)

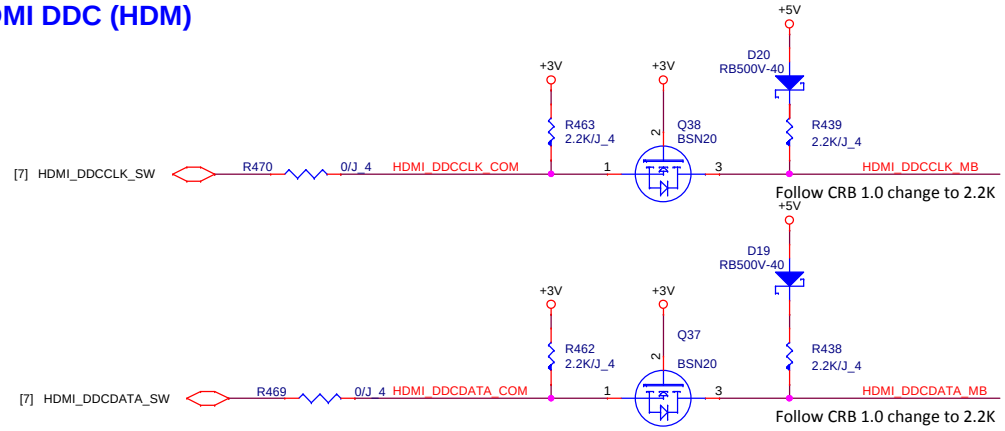


Layout Notes:
Place decoupling CAPs close to Connector

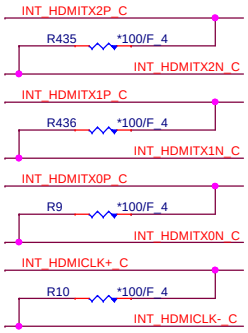
HDMI connector (HDM)



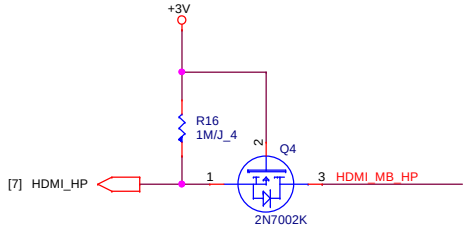
HDMI DDC (HDM)



EMI (EMC)



HDMI-detect (HDM)



Quanta Computer Inc.
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	HDMI	1A
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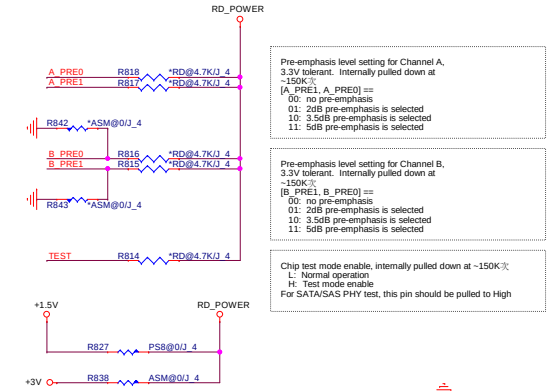
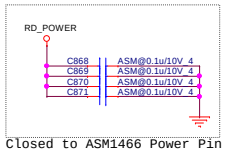
mSATA Redriver (HDD)





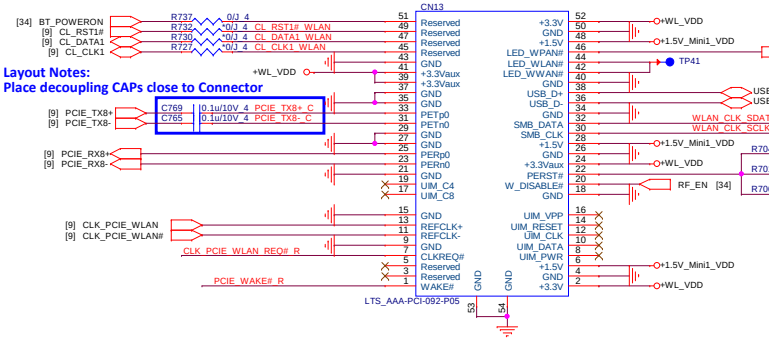
Closed to ASM1466 Power Pin

MINI-CARD WLAN(MPC)

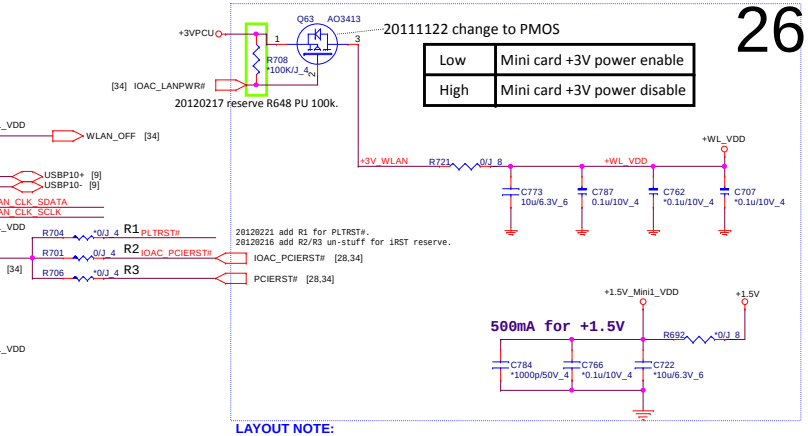
+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

Check LED signal. (active high or low)

H=5.2mm

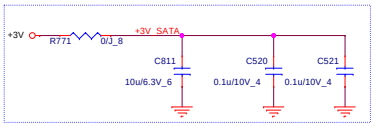


Layout Notes:
Place decoupling CAPs close to Connector



LAYOUT NOTE:
CLOSE TO CONNECTOR

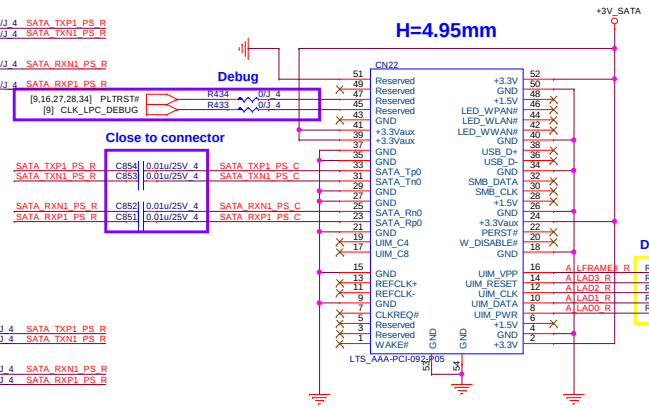
mSATA (HDD)



LAYOUT NOTE:
CLOSE TO CONNECTOR

rating = 1000mA @ 128G

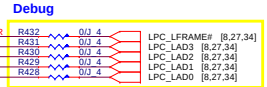
H=4.95mm



Debug

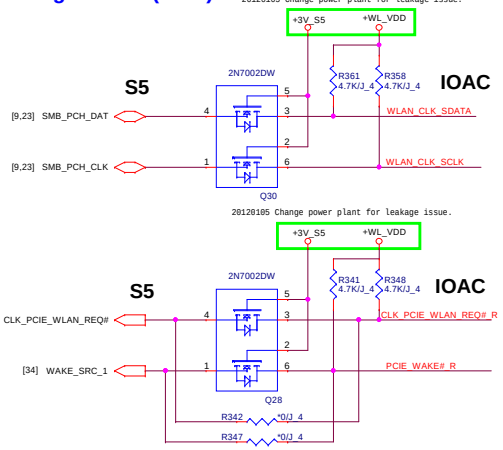
Close to connector

Debug



Leakage circuit (MPC)

20120105 Change power plant for leakage issue.



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	Mini Card/mSATA	1A

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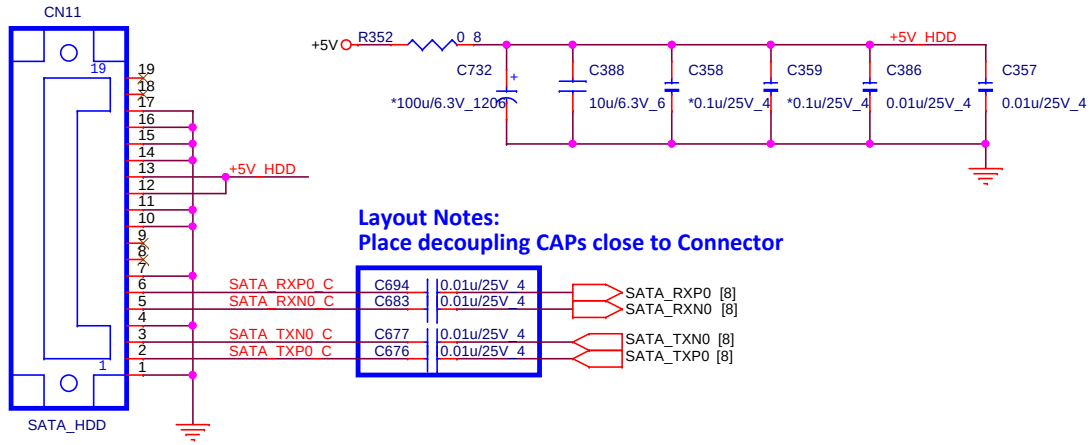
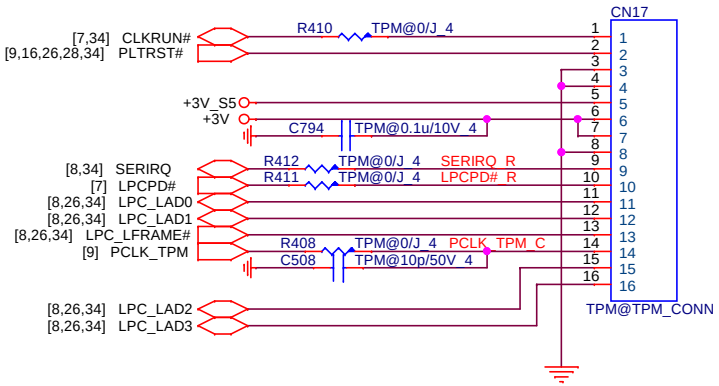
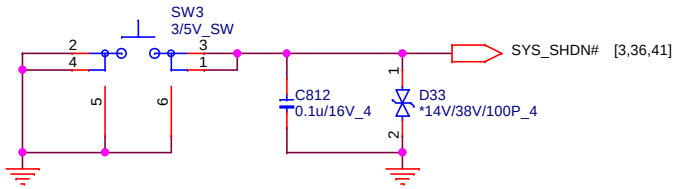
MAIN SATA HDD (HDD)



TPM (TPM)



3/5VPCU reset switch (CLG)



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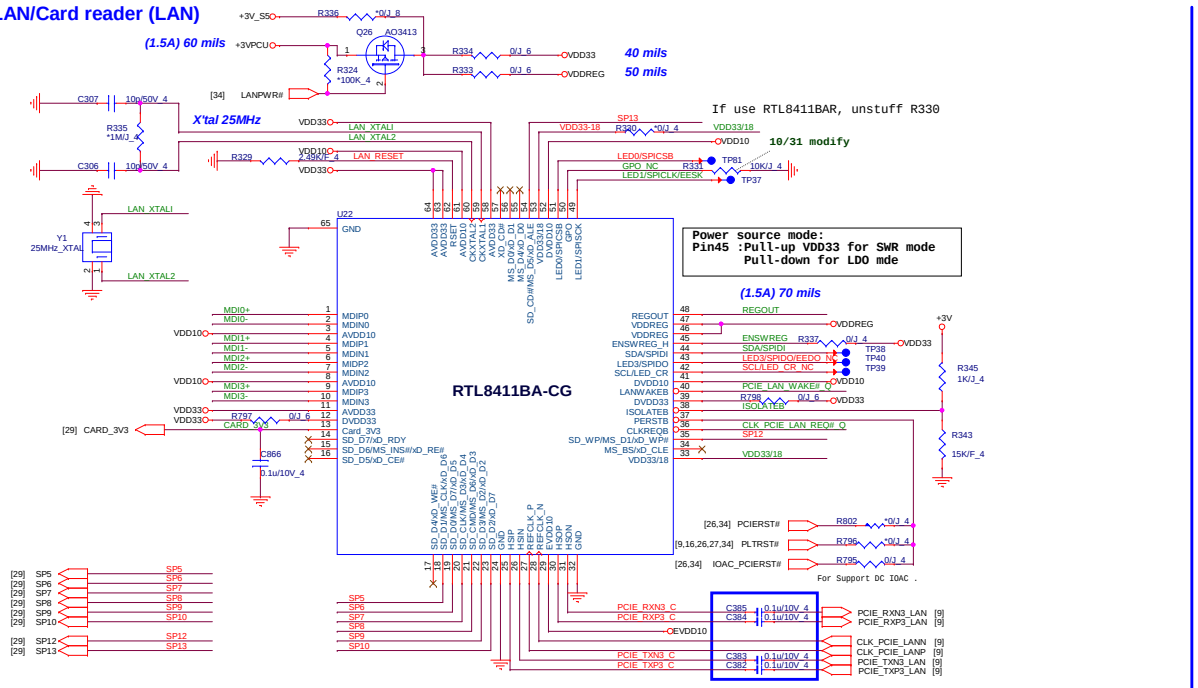
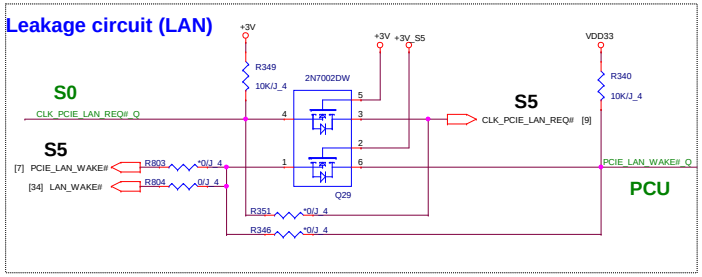
LAN/Card reader (LAN)

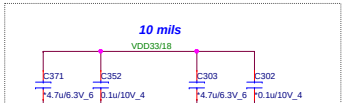


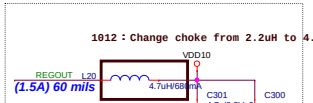
Leakage circuit (LAN)

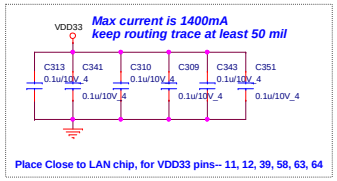


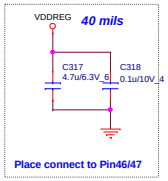
1012 : LAN request pin power domain need to sync with ISOLATEB pin

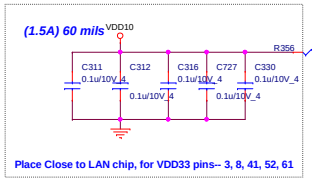
1016 : Exchange Q29 pin 3 & 4 to prevent leakage issue

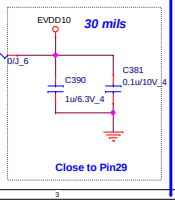




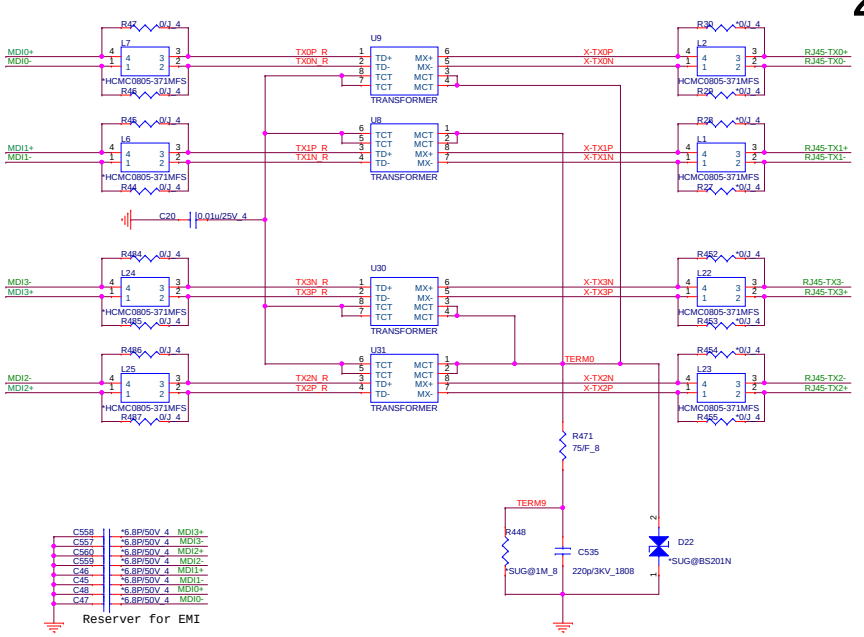




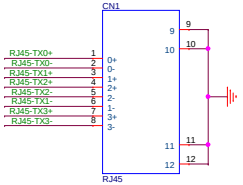




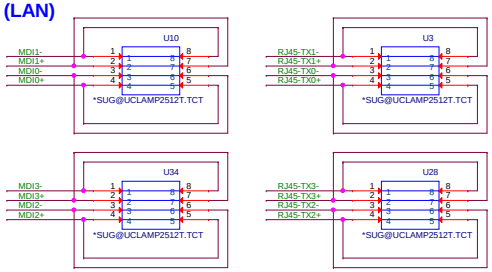
Transformer (LAN)



RJ45 CONNECTOR (LAN)



SURGE (LAN)



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	LAN-RTL8411/CARD READER	1A

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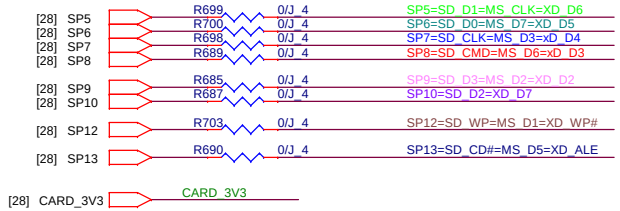
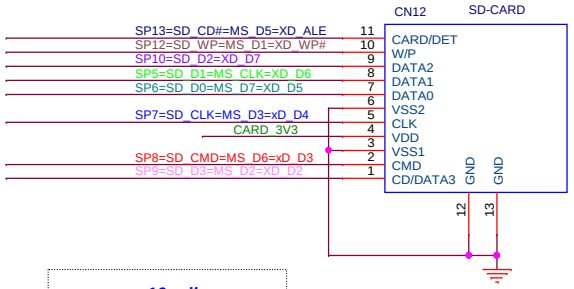
CARD READER CONNECTOR (MMC)

SD/MMC CARD READER (MMC)

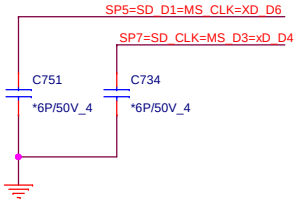
Share Pin

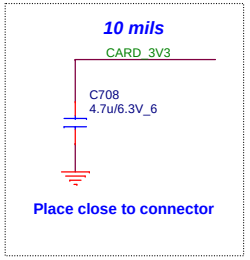
SP1	SD_D7		xD_RDY
SP2	SD_D6	MS_INS#	xD_RE#
SP3	SD_D5		xD_CE#
SP4	SD_D4		xD_WE#
SP5	SD_D1	MS_CLK	xD_D6
SP6	SD_D0	MS_D7	xD_D5
SP7	SD_CLK	MS_D3	xD_D4
SP8	SD_CMD	MS_D6	xD_D3
SP9	SD_D3	MS_D2	xD_D2
SP10	SD_D2		xD_D7
SP11		MS_BS	xD_CLE
SP12	SD_WP	MS_D1	xD_WP#
SP13	SD_CD#	MS_D5	xD_ALE
SP14		MS_D4	xD_D0
SP15		MS_D0	xD_D1
SP16			xD_CD#





EMI





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	CARD READER CONNECTOR	1A
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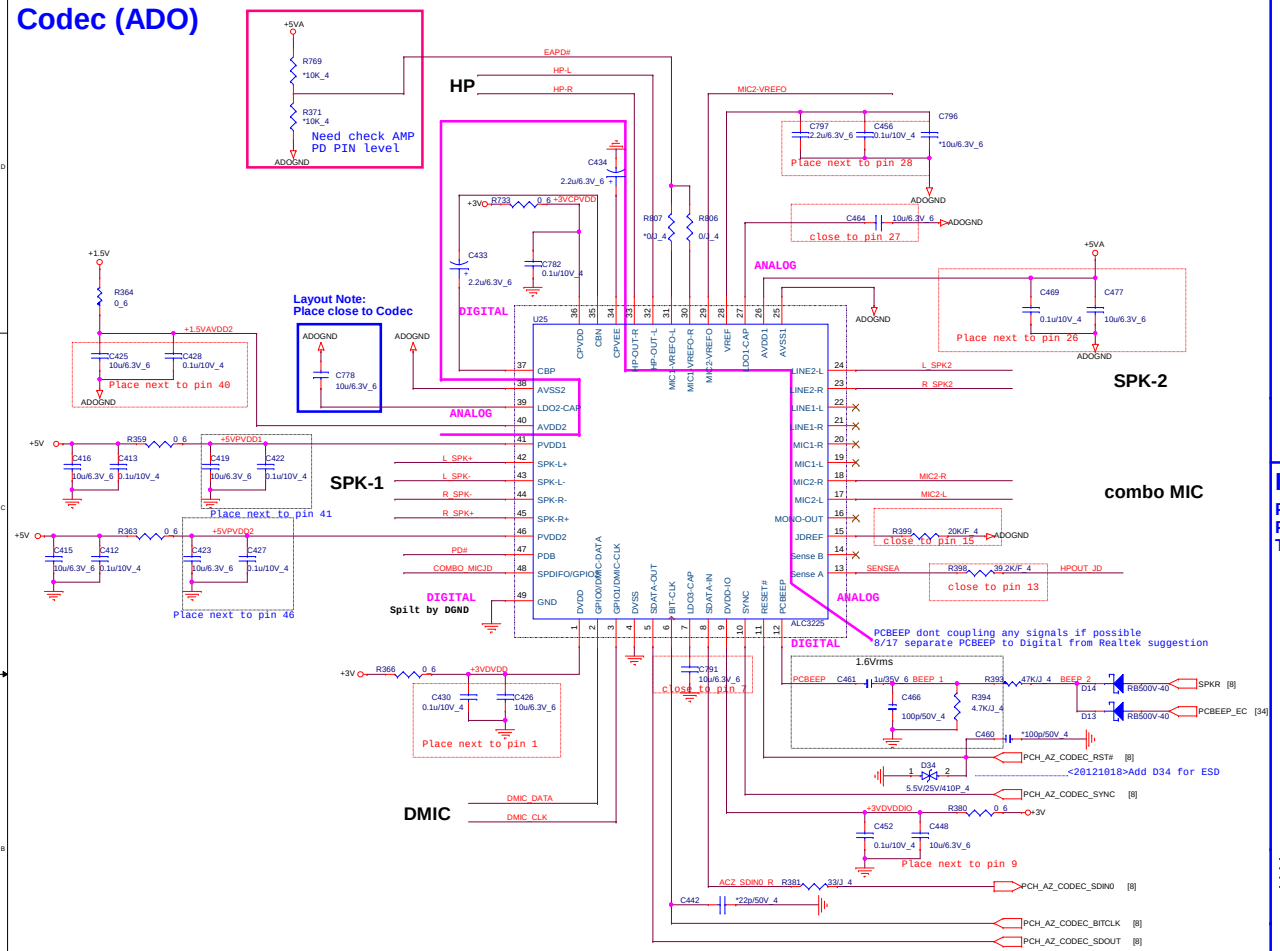
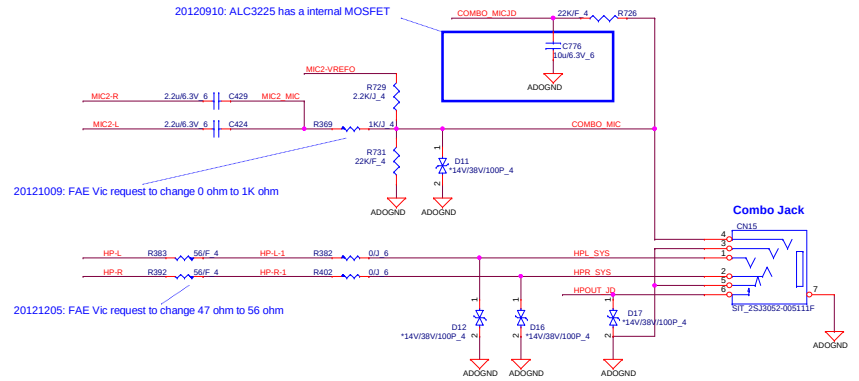
Codec (ADO)



HEADPHONE/Mic combo (AMP)

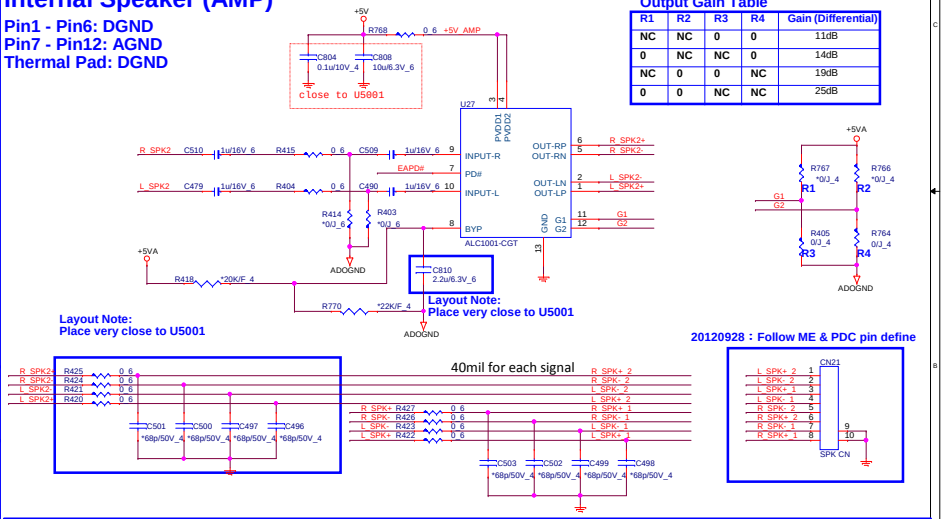


Internal Speaker (AMP)

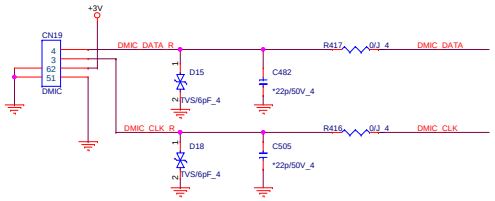
Pin1 - Pin6: DGND
Pin7 - Pin12: AGND
Thermal Pad: DGND

Output Gain Table

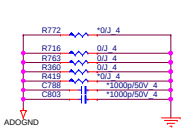
R1	R2	R3	R4	Gain (Differential)
NC	NC	0	0	11dB
0	NC	NC	0	14dB
NC	0	0	NC	19dB
0	0	NC	NC	25dB



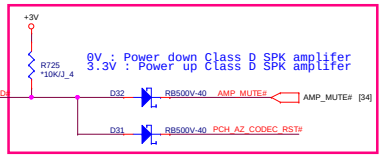
INT DMIC (AMP)



Power(ADO)



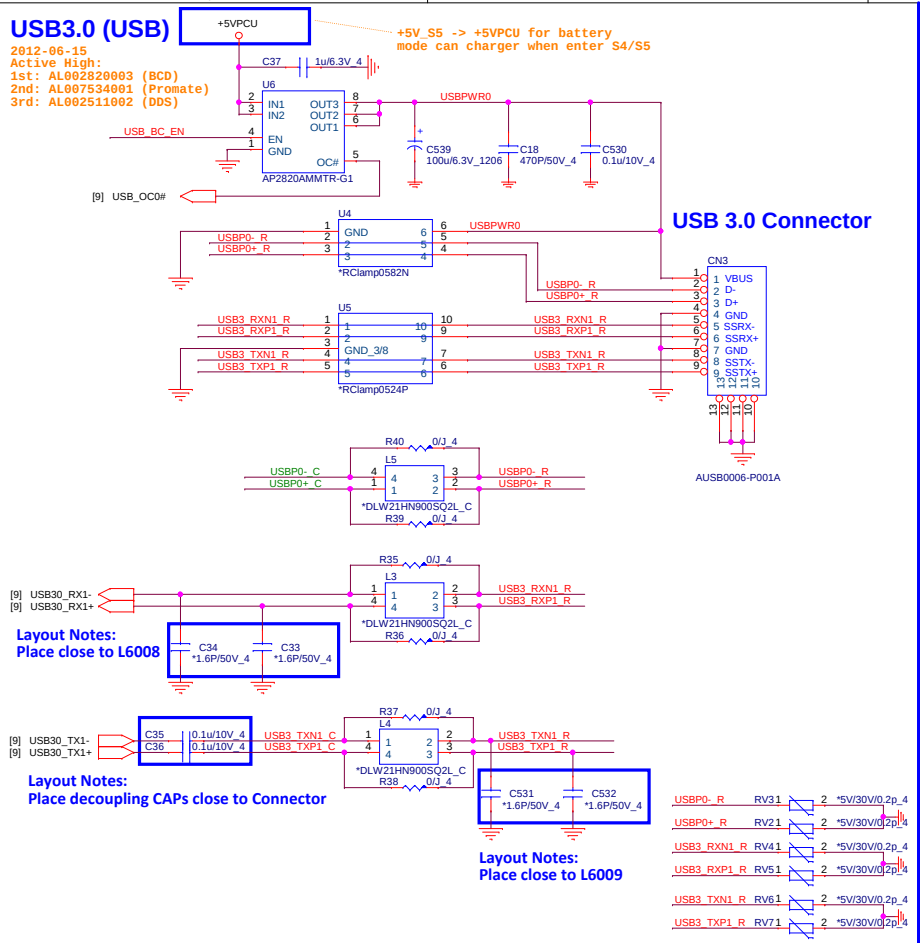
Mute(ADO)



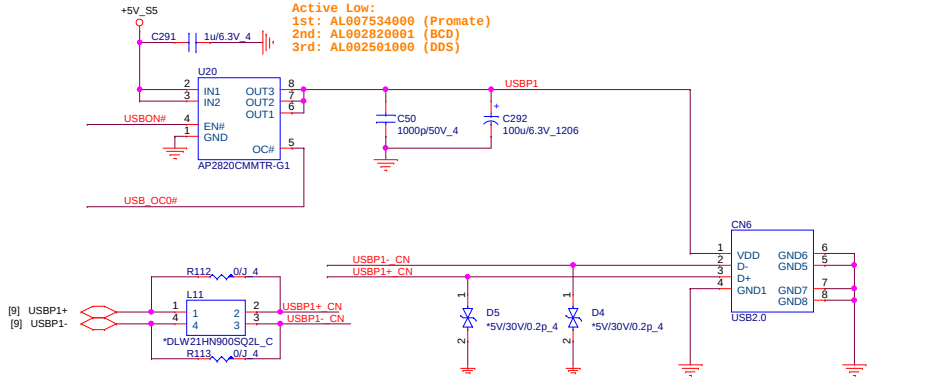
Quanta Computer Inc.			
PROJECT : ZQK			
Size	Document Number		Rev
	REALTEK ALC3225		1A
Date: Monday, January 07, 2013		Sheet 30 of 46	

USB3.0 (USB)

2012-06-15
Active High:
1st: AL002820003 (BCD)
2nd: AL007534001 (Promate)
3rd: AL002511002 (DDS)



USB2.0 (USB)

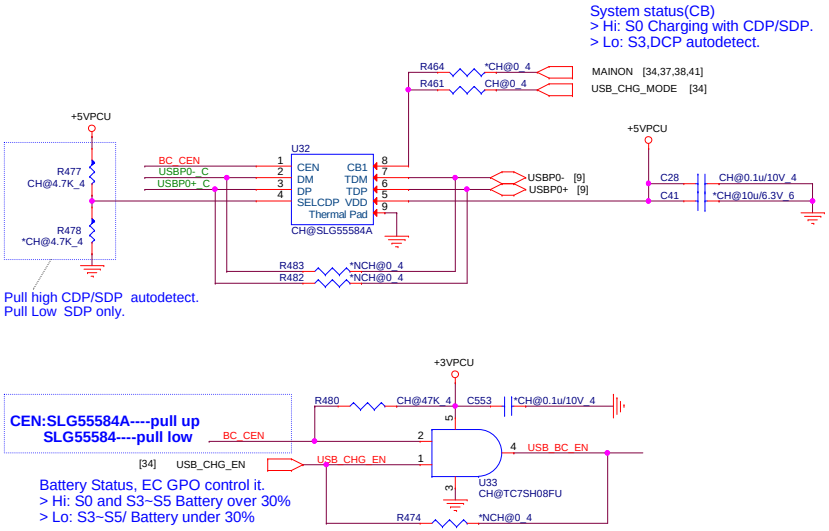


USB Charger to 3.0 (USB)

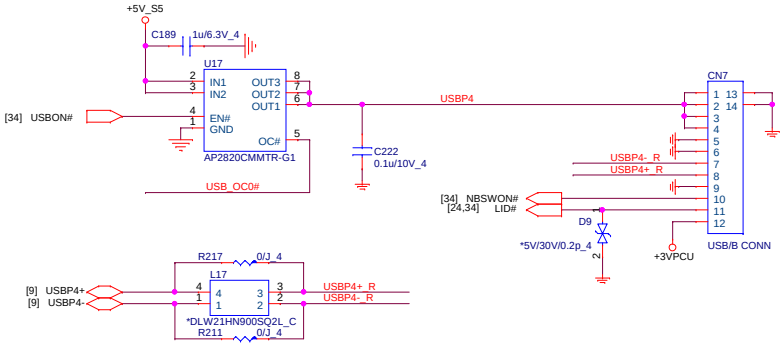
Name	USB data	State	Max Current	Apple Device
SDP	YES	S0~S3	500mA	500mA
CDP	YES	S0~S3	1500mA	500mA
DCP,Auto	NO	S4~S5	1800mA	1800mA

CB	SELCDP	FuncionFuncion
0	X	DCP autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP only
1	1	S0 charging with CDP or SDP only (depending on external device)

CH@: Default stuff



I/O board (USB)



Quanta Computer Inc.
PROJECT : ZQK

Size	Document Number	Rev
	INT&EXT USB	1A

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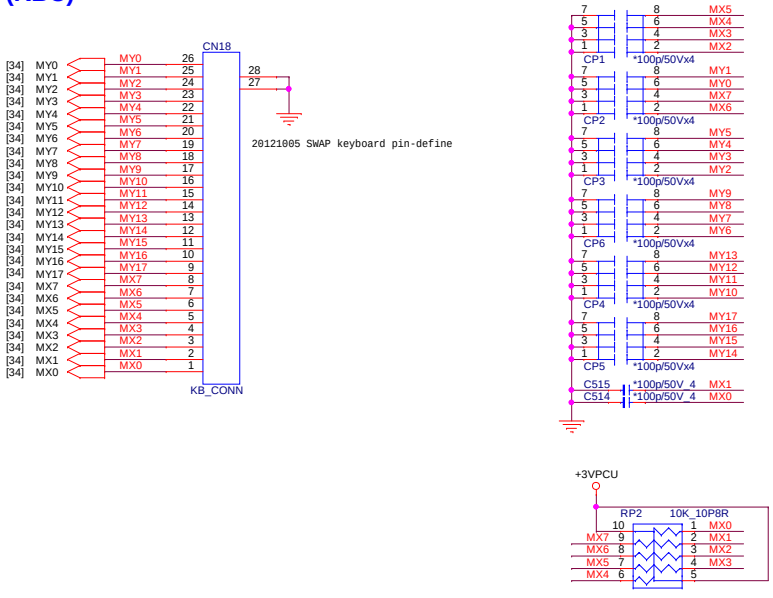
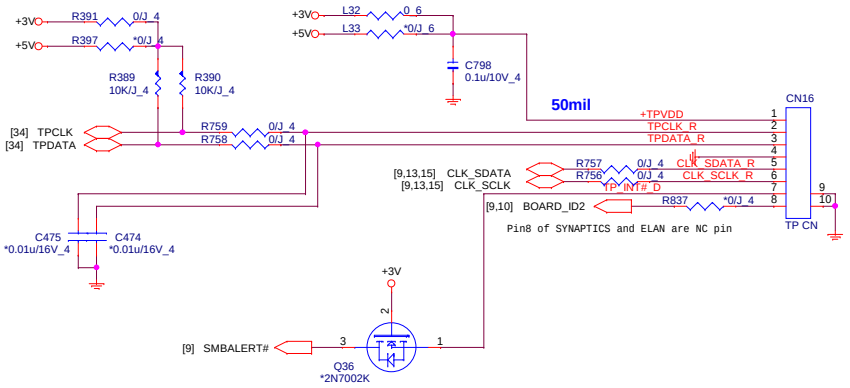
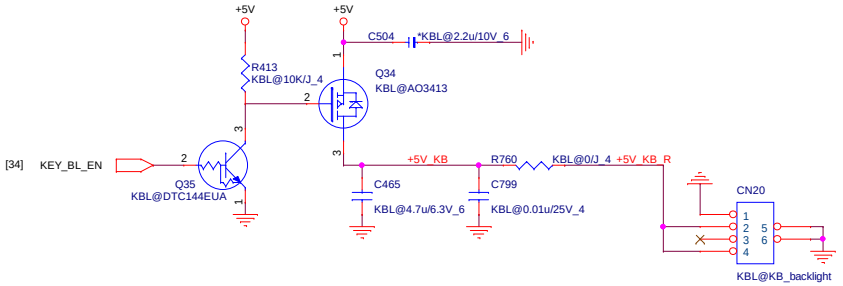
K/B (KBC)



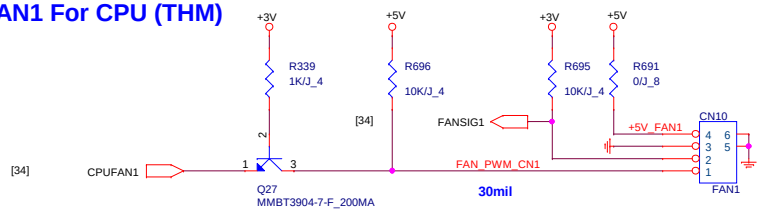
TOUCHPAD BOARD CONN (TPD)



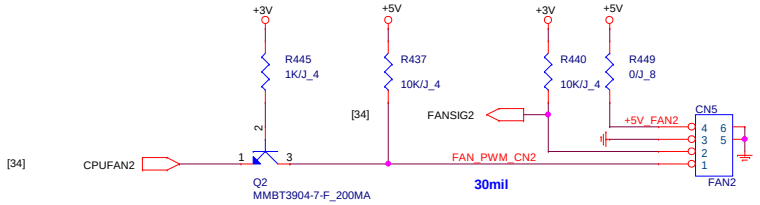
KB_BL LED (KBC)



FAN1 For CPU (THM)



FAN2 For GPU (THM)

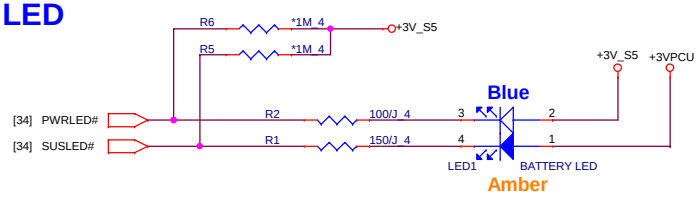


Quanta Computer Inc.
PROJECT : ZQK

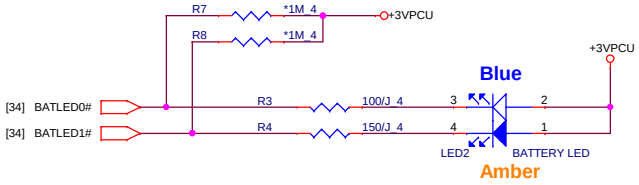
Size	Document Number	Rev
	KB/TP/FAN	1A
Date: Monday, January 07, 2013	Sheet 32 of 46	

LED(UIF)

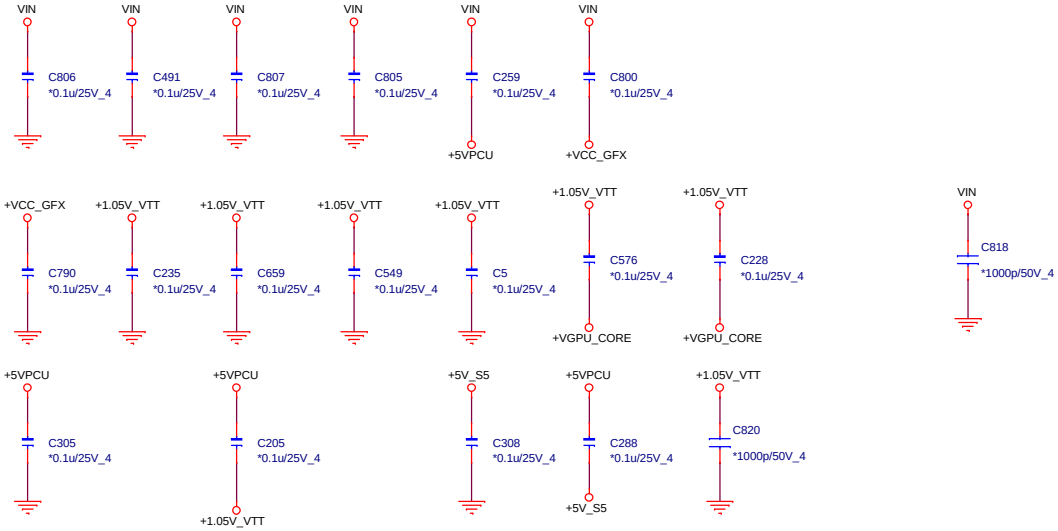
Power LED



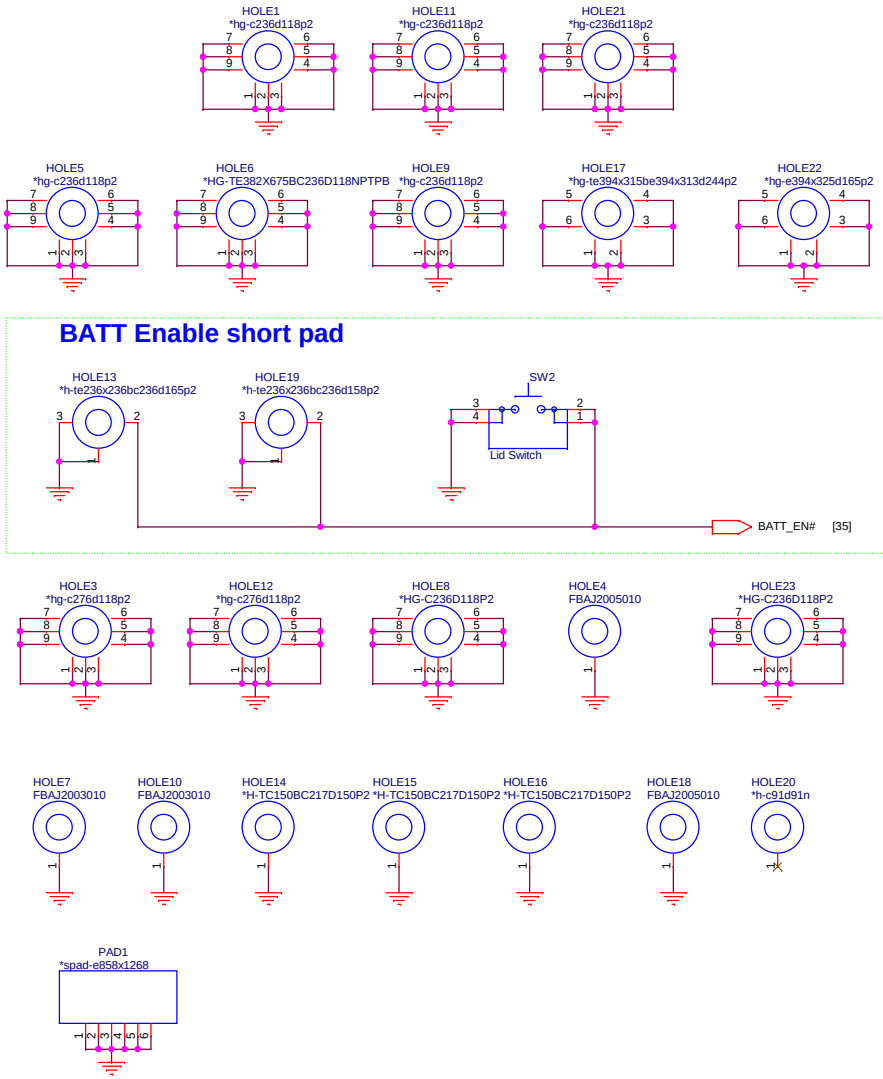
Battery



Stitching cap (EMC)



HOLE(OTH)



Quanta Computer Inc.
PROJECT : ZQK

Size	Document Number	Rev
	LED/ Hole	1A
Date: Monday, January 07, 2013	Sheet 33 of 46	

EC(KBC)

+3VPCU_EC and +3V_RTC minimum trace width 12mils.

1008 : Change Power rail from +3VPCU to +3VPCU_EC (For PLL Power)

12 mils

12 mils

IT8587

LPC

GPIO

PS/2

SM BUS

CIR

UART port

WAKE UP

EXTERNAL SERIAL FLASH

PWM

A/D D/A

Input only

SPI ENABLE

KBMX

CLOCK

Please do not place any pull-up resistor on GPG0, GPG2, and GPG6 (Reserved hardware strapping).

Layout Notes:
Place Series Resistors close to ITE8587

IT8587E/EX

SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH/VGA

SM BUS PU(KBC)

HWPG(KBC)

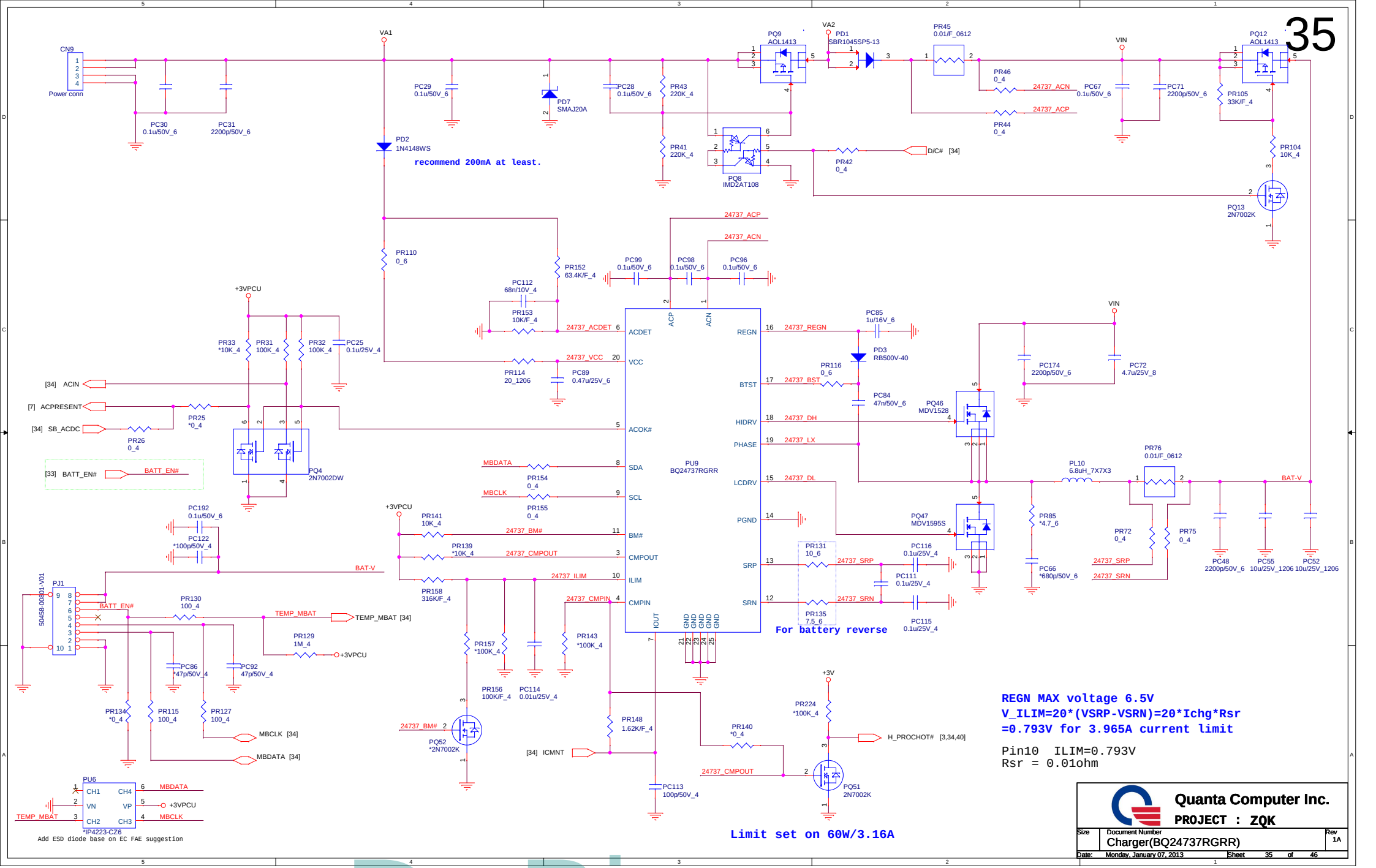
For test only

Power Switch

iRST

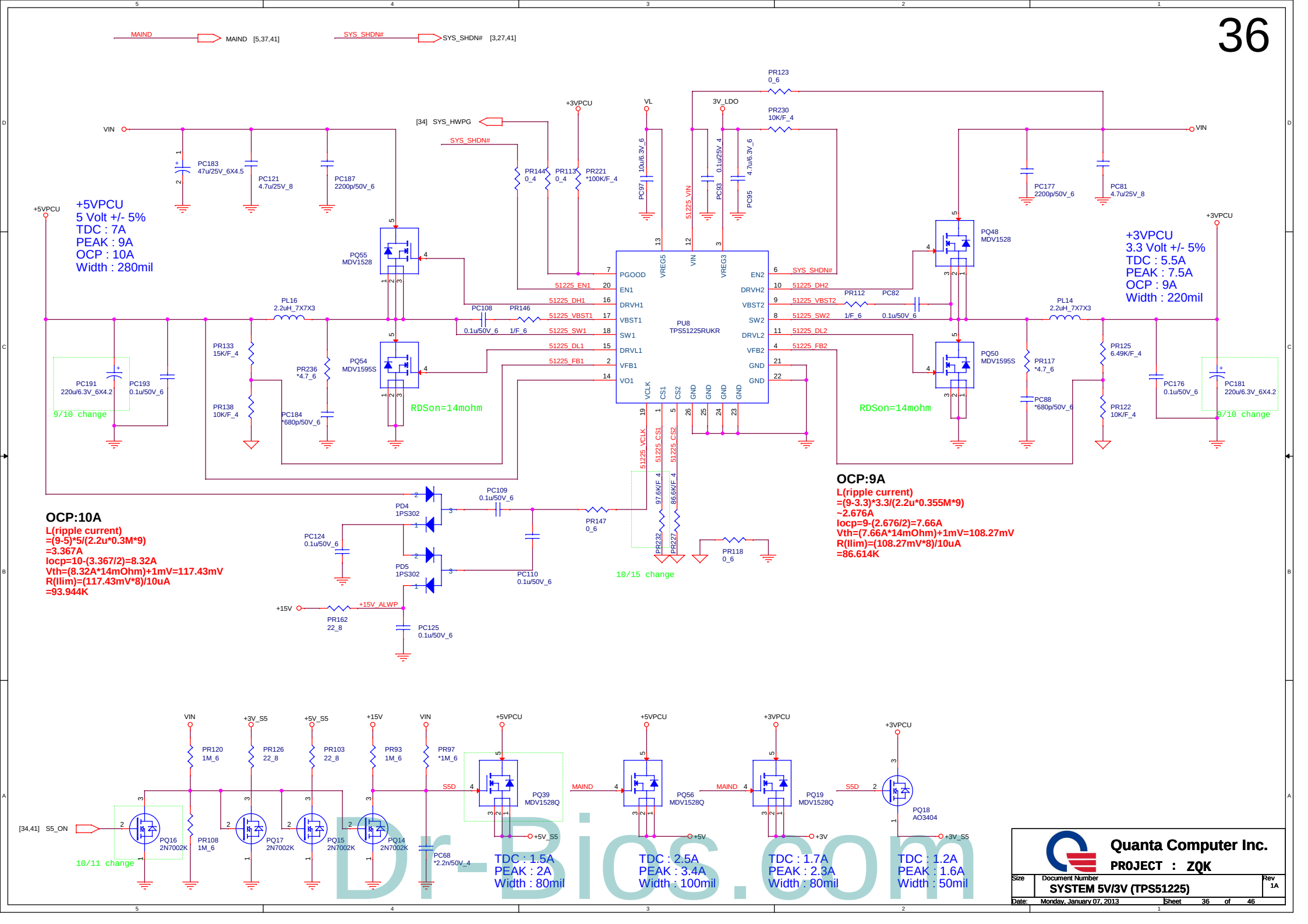
20120217 reserve iRST function.

Quanta Computer Inc.
PROJECT : ZQK
KBC IT8587
Size | Document Number | Rev 1A
Date: Monday, January 07, 2013 | Sheet 34 of 46



Quanta Computer Inc.
PROJECT : ZQK

Size	Document Number	Rev
	Charger(BQ24737RGRR)	1A
Date: Monday, January 07, 2013	Sheet 35 of 46	


MAIND
MAIND [5,37,41]
SYS_SHDN#
SYS_SHDN# [3,27,41]
+5VPCU
5 Volt +/- 5%
TDC : 7A
PEAK : 9A
OCP : 10A
Width : 280mil
+3VPCU
3.3 Volt +/- 5%
TDC : 5.5A
PEAK : 7.5A
OCP : 9A
Width : 220mil
VIN
VL
3V_LDO
[34] SYS_HWPG
SYS_SHDN#
PU8
TPS51225RUKR
PGOOD
EN1
DRVH1
VBST1
SW1
DRVL1
VFB1
VO1
VCLK
CS1
CS2
VREG5
VREG3
EN2
DRVH2
VBST2
SW2
DRVL2
VFB2
GND
PQ55 MDV1528
PQ54 MDV1595S
PQ48 MDV1528
PQ50 MDV1595S
PL16 2.2uH_7X7X3
PL14 2.2uH_7X7X3
RDSon=14mohm
RDSon=14mohm
9/10 change
9/10 change
10/15 change
OCP:10A
L(ripple current)
=(9-5)*5/(2.2u*0.3M*9)
=3.367A
Iocp=10-(3.367/2)=8.32A
Vth=(8.32A*14mOhm)+1mV=117.43mV
R(Ilim)=(117.43mV*8)/10uA
=93.944K
OCP:9A
L(ripple current)
=(9-3.3)*3.3/(2.2u*0.355M*9)
~2.676A
Iocp=9-(2.676/2)=7.66A
Vth=(7.66A*14mOhm)+1mV=108.27mV
R(Ilim)=(108.27mV*8)/10uA
=86.614K
PD4 1PS302
PD5 1PS302
+15V
+15V_ALWP
PR162 22_8
PC125 0.1u/50V_6
PR147 0_6
PR118 0_6
PR123 0_6
PR230 10K/F_4
PC177 2200p/50V_6
PC81 4.7u/25V_8
PC88 *680p/50V_6
PR125 6.49K/F_4
PR122 10K/F_4
PC176 0.1u/50V_6
PC181 220u/6.3V_6X4.2
PC191 220u/6.3V_6X4.2
PC193 0.1u/50V_6
PR133 15K/F_4
PR138 10K/F_4
PR236 *4.7_6
PC184 *680p/50V_6
PR117 *4.7_6
PC108 0.1u/50V_6
PR146 1/F_6
PR112 1/F_6
PC82 0.1u/50V_6
PC109 0.1u/50V_6
PC110 0.1u/50V_6
PC124 0.1u/50V_6
PR232 97.6K/F_4
PR227 86.6K/F_4
PC97 10u/6.3V_6
PC93 0.1u/25V_4
PC95 4.7u/6.3V_6
PR144 0_4
PR113 0_4
PR221 *100K/F_4
51225_EN1
51225_DH1
51225_VBST1
51225_SW1
51225_DL1
51225_FB1
51225_DH2
51225_VBST2
51225_SW2
51225_DL2
51225_FB2
51225_VCLK
51225_CS1
51225_CS2
51225_VIN
[34,41] S5_ON
10/11 change
VIN
+3V_S5
+5V_S5
+15V
VIN
PR120 1M_6
PR126 22_8
PR103 22_8
PR93 1M_6
PR97 *1M_6
PR108 1M_6
S5D
PQ16 2N7002K
PQ17 2N7002K
PQ15 2N7002K
PQ14 2N7002K
PC68 *2.2n/50V_4
PQ39 MDV1528Q
PQ56 MDV1528Q
PQ19 MDV1528Q
PQ18 AO3404
MAIND
MAIND
S5D
+5VPCU
+5VPCU
+3VPCU
+3VPCU
+5V_S5
+5V
+3V
+3V_S5
TDC : 1.5A
PEAK : 2A
Width : 80mil
TDC : 2.5A
PEAK : 3.4A
Width : 100mil
TDC : 1.7A
PEAK : 2.3A
Width : 80mil
TDC : 1.2A
PEAK : 1.6A
Width : 50mil
Dr-Bios.com
Quanta Computer Inc.
PROJECT : ZQK
Size
Document Number
SYSTEM 5V/3V (TPS51225)
Rev
1A
Date: Monday, January 07, 2013
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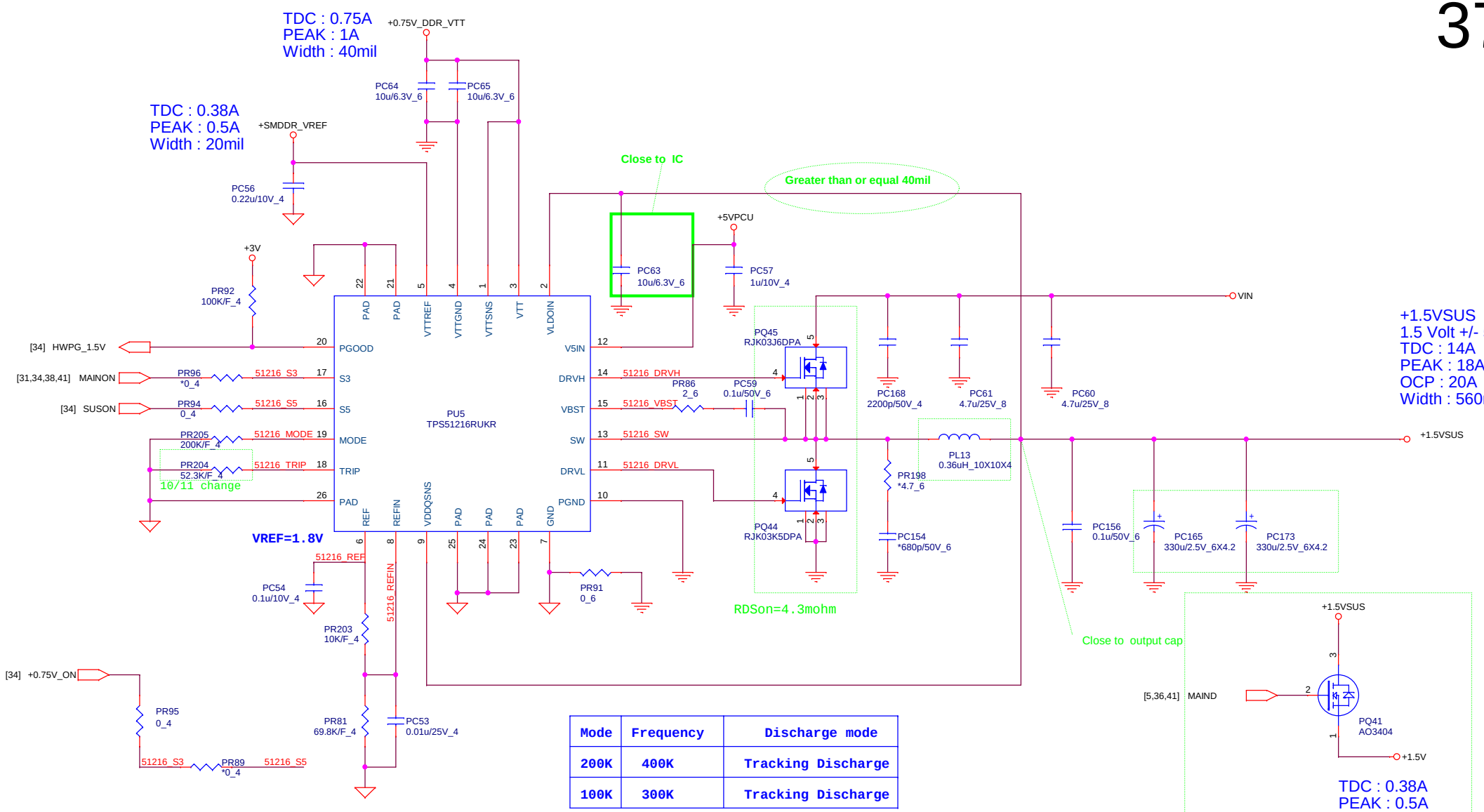


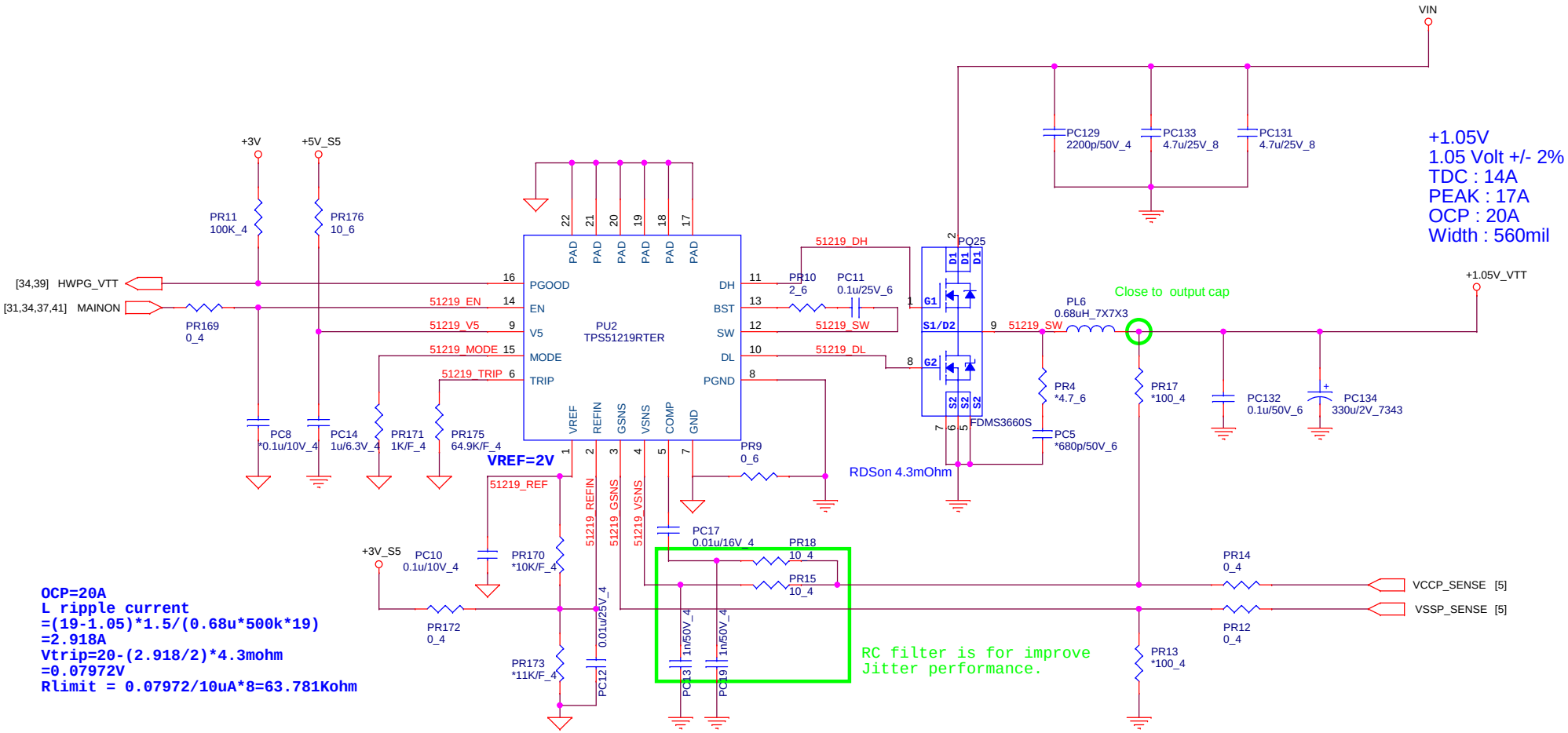
Mode	Frequency	Discharge mode
200K	400K	Tracking Discharge
100K	300K	Tracking Discharge

	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

OCP=20A
L ripple current
=(19-1.5)*1.5/(0.36u*400k*19)
=9.594A
Vtrip=20-(9.594/2)*4.3mohm
=0.065372V
Rlimit=0.065372/10uA*8=52.297Kohm

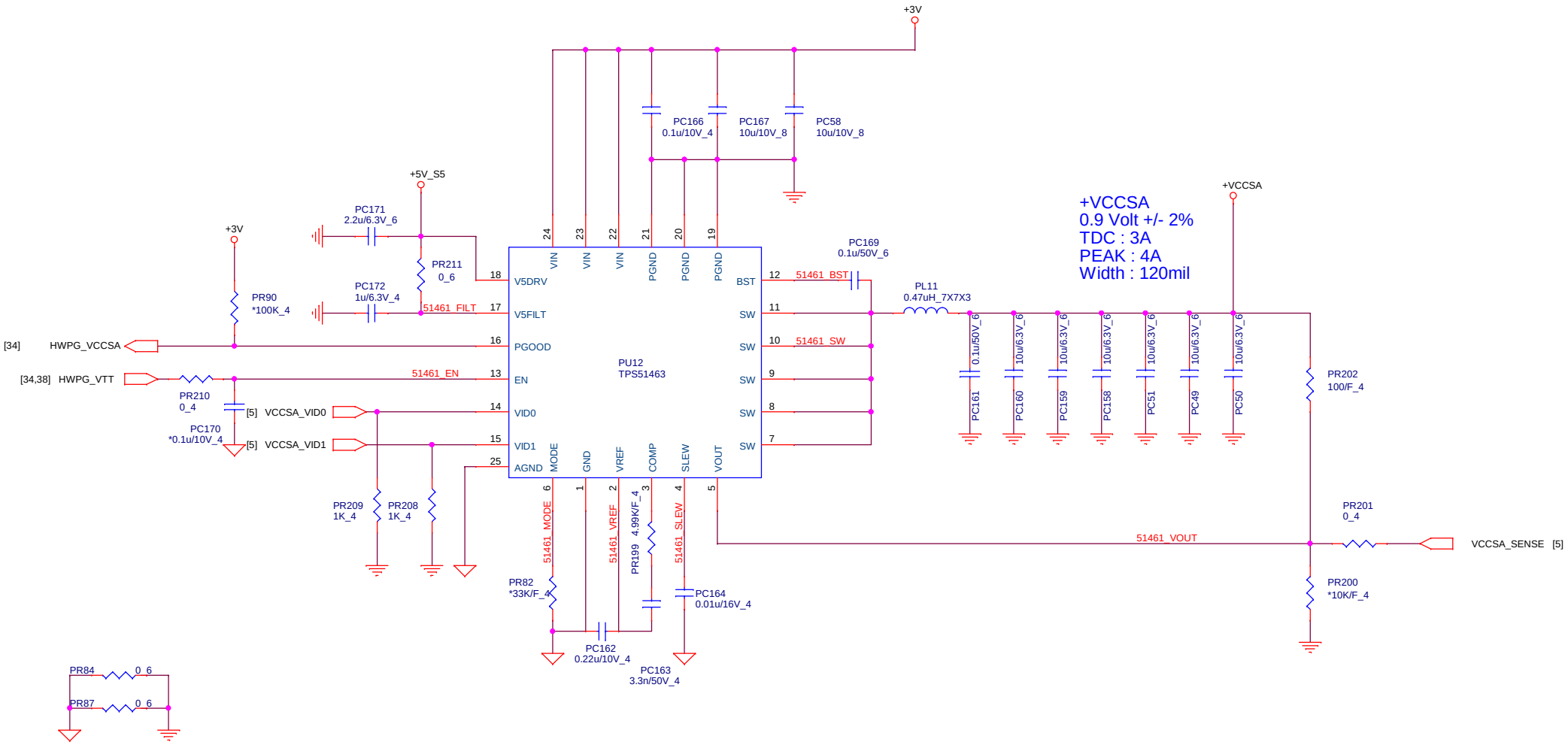
Quanta Computer Inc.
PROJECT : ZQK

Size	Document Number	Rev
	DDR 1.5V(TPS51216)	1A
Date: Monday, January 07, 2013	Sheet 37 of 46	



Quanta Computer Inc.
PROJECT : ZQK

Size	Document Number	Rev
	+1.05V (TPS51219)	1A
Date: Monday, January 07, 2013	Sheet 38 of 46	



VID0	VID1	+VCCSA
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

default 0.9V

Quanta Computer Inc.
PROJECT : ZQK

Size	Document Number	Rev
	VCCSA(TPS51463)	1A

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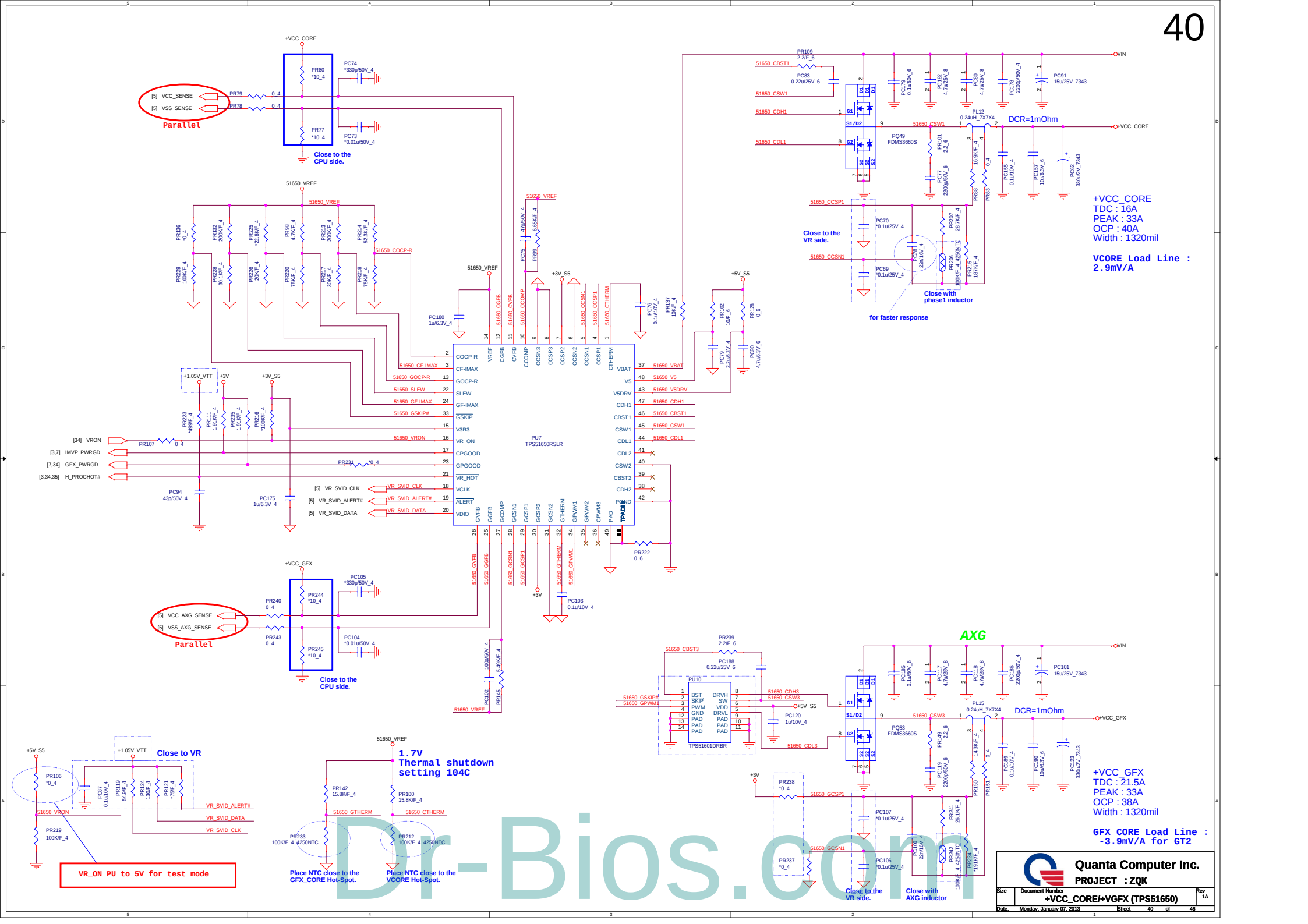

Quanta Computer Inc.
PROJECT : ZQK

Size	Document Number	Rev
	+VCC_CORE/+VGFX (TPS51650)	1A
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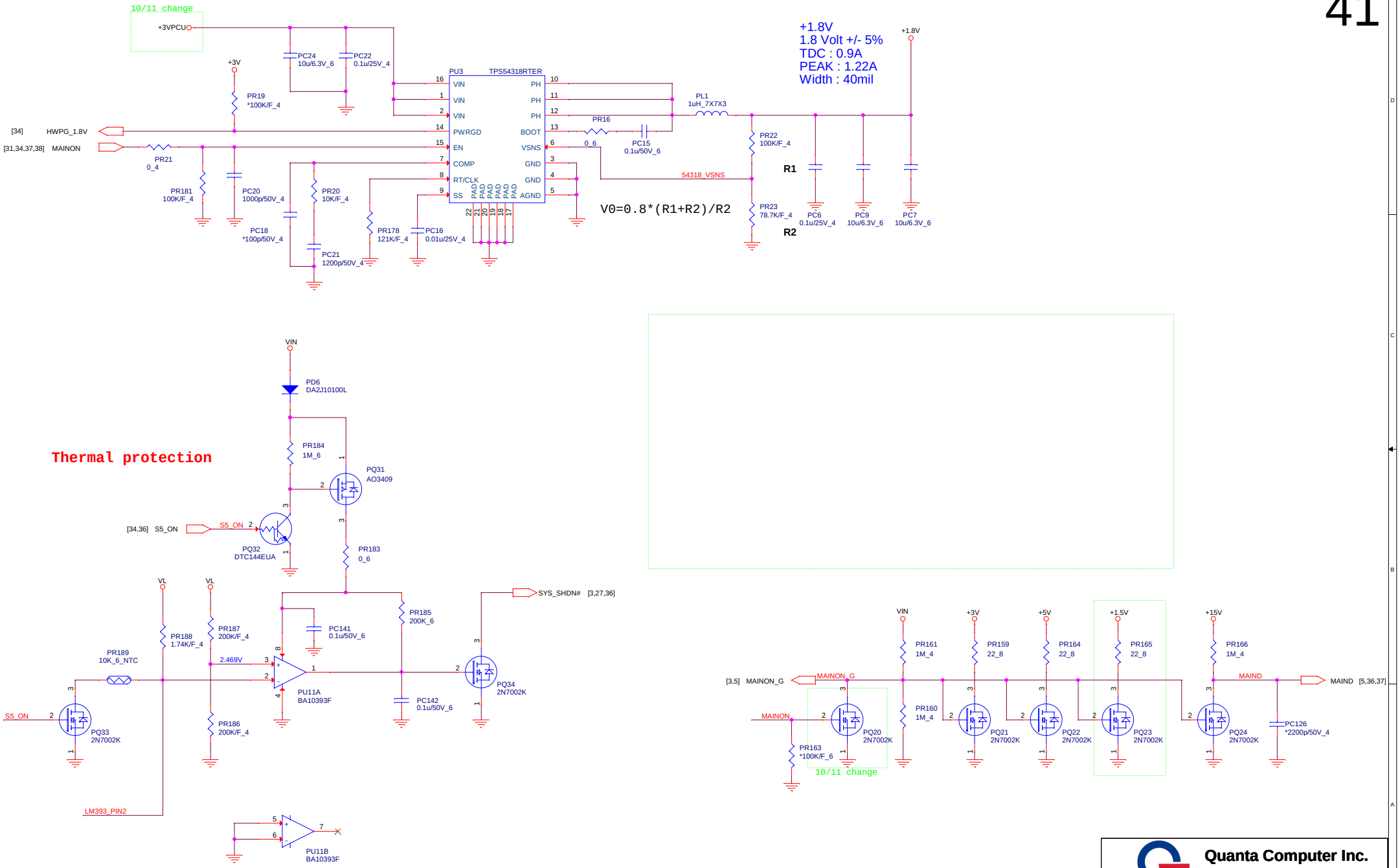
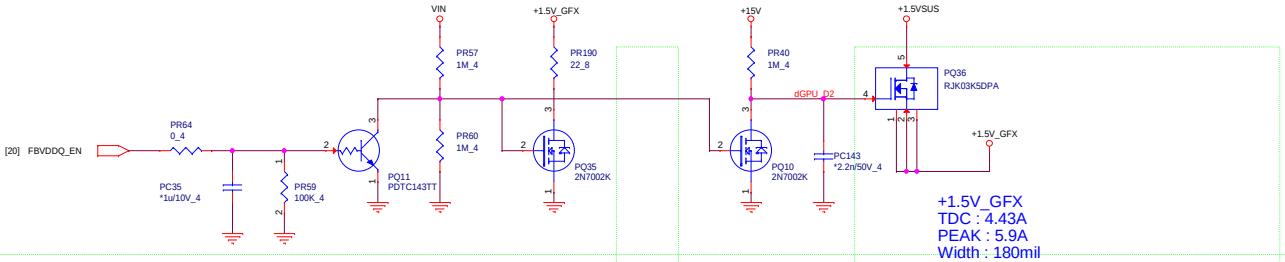


Quanta Computer Inc.
PROJECT : ZQK

Size	Document Number	Rev
	+1.8V/Discharge/Thermal	1A
Date: Monday, January 07, 2013	Sheet 41 of 46	

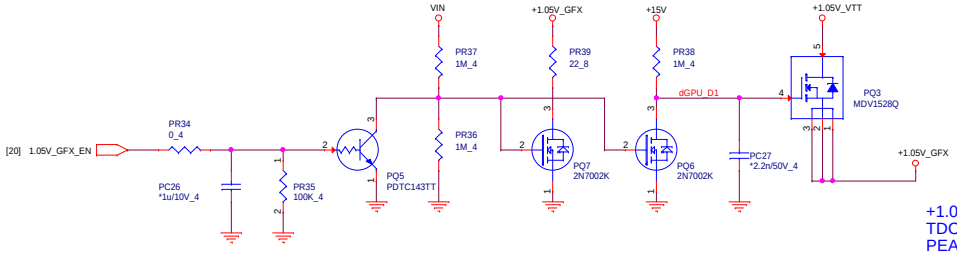
10/1 Change



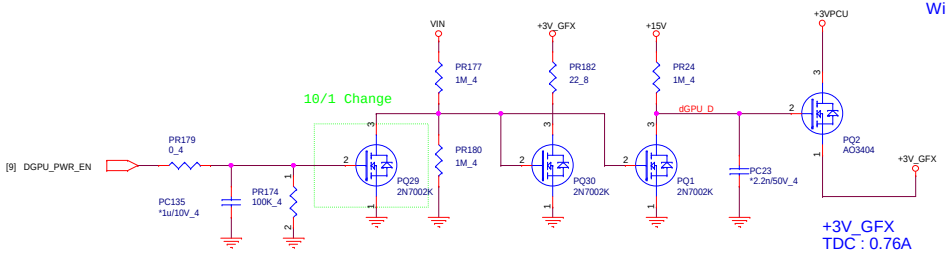
+1.5V_GFX
TDC : 4.43A
PEAK : 5.9A
Width : 180mil

10/5 Reserve switching power for +1.5V_GFX

OCP=7.5A
L ripple current
=(19-1.5)*1.5/(2.2u*290k*19)
=2.165A
Vtrip=7.5-(2.165/2)*14mohm
=0.0898V
Rlimit=0.0898/10uA*8=71.873Kohm



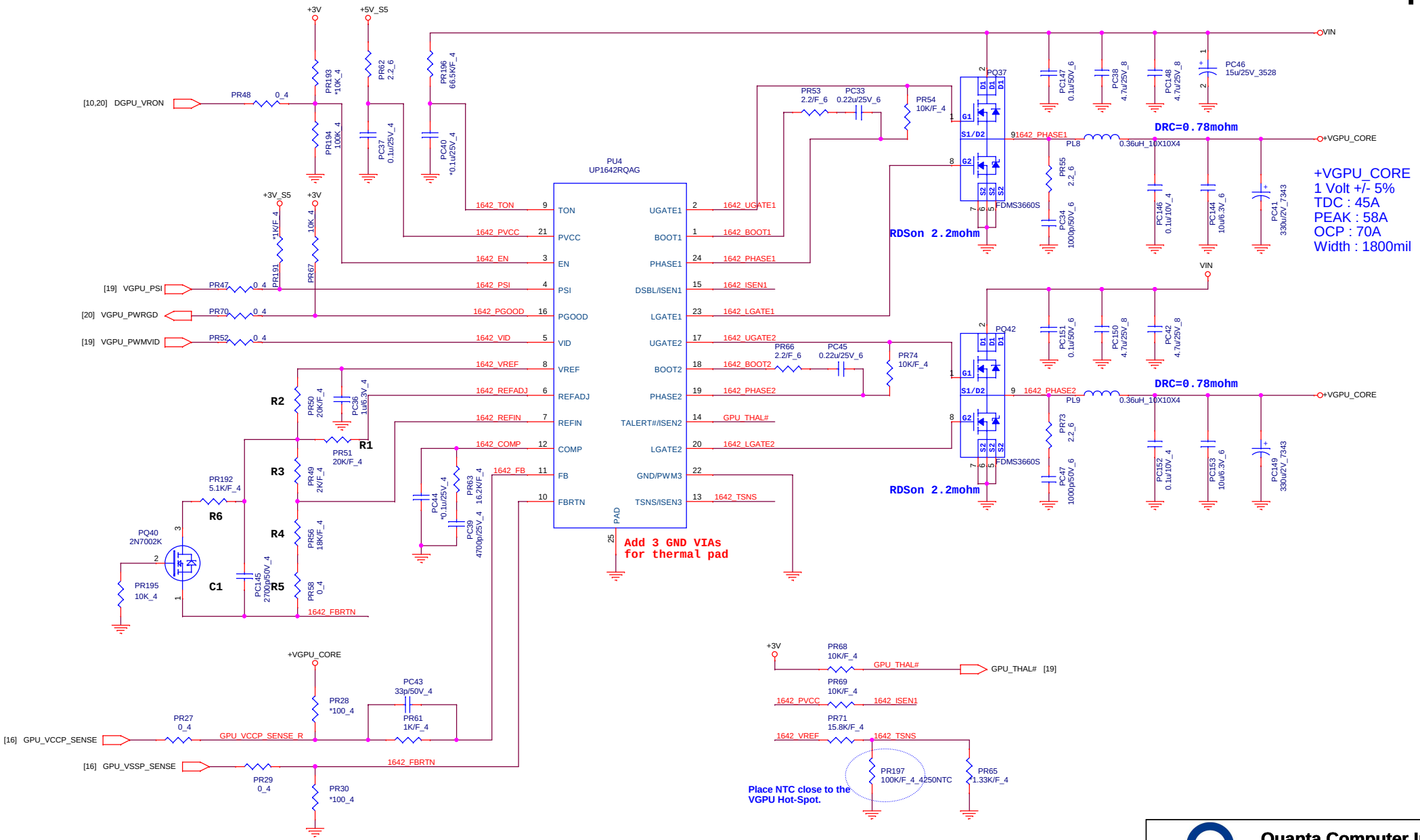
+1.05V_GFX
TDC : 2.3A
PEAK : 3A
Width : 100mil



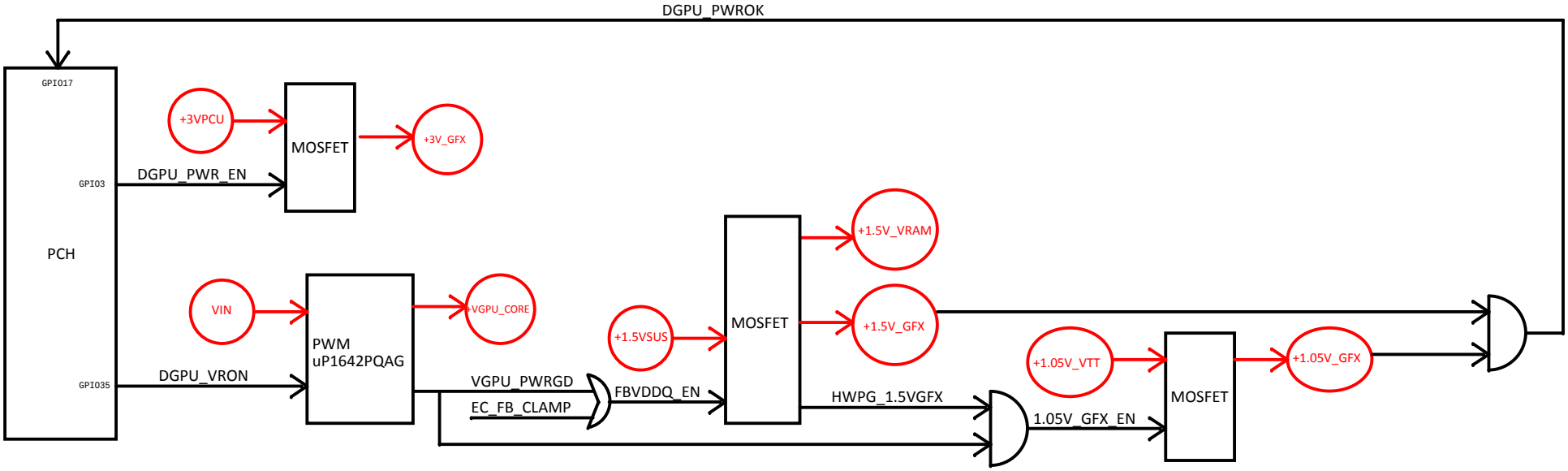
+3V_GFX
TDC : 0.76A
PEAK : 1A
Width : 40mil

Quanta Computer Inc.
PROJECT : ZQK

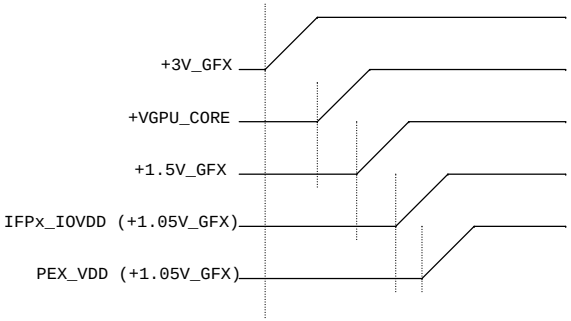
Size	Document Number	Rev
	+VGPU_CORE(UP1642PQAG)	1A
Date: Monday, January 07, 2013	Sheet 42 of 46	



Quanta Computer Inc.	
PROJECT : ZQK	
Size	Document Number: +VGPU_CORE(UP1642PQAG) — Rev: 1A
Date: Monday, January 07, 2013	Sheet 43 of 46



Power Sequence

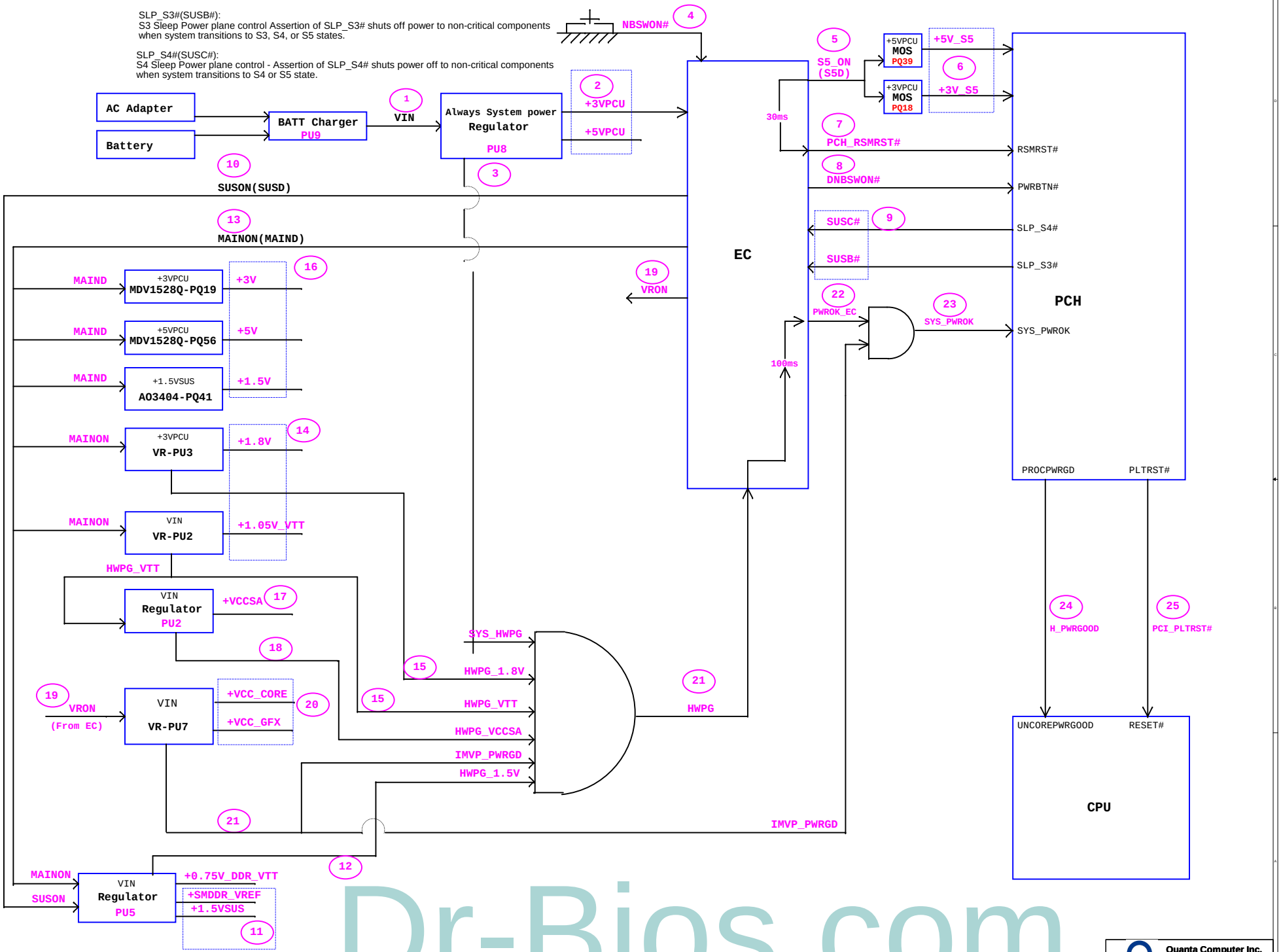


All rails must be powered off within 10 ms from the first rail powering off.

Quanta Computer Inc. PROJECT : ZQK		
Size	Document Number: Power Sequence	Rev 1A
Date: Monday, January 07, 2013	Sheet 44 of 46	

SLP_S3#(SUSB#):
S3 Sleep Power plane control Assertion of SLP_S3# shuts off power to non-critical components when system transitions to S3, S4, or S5 states.

SLP_S4#(SUSC#):
S4 Sleep Power plane control - Assertion of SLP_S4# shuts power off to non-critical components when system transitions to S4 or S5 state.



Quanta Computer Inc.
PROJECT : ZQK
power sequence block diagram

Model	Date	CHANGE LIST
ZQK	1203	1.Change C774 from 0.1uF to 39pF for ESD 2.Add C841~C850 39pF for ESD 3.Change U19,U21,U23,U26,U43,U46,U48,U49 PN from AKD5JGST404 to AKD5JGST407
	1205	1.Change LED1/LED2 PN：BEB00028ZA0；FP：led19-123-y2st1d-c30-2t-4p 2.Change R383/R392 from 47 ohm to 56 ohm
	1206	1.Change SW2 PN： DHPATE2CK03；FP：sw-ate-2ck-v-tr-4p
	1210	1.Delete PL2/PL3/PL4/PL5 2.Add RTC charge circiut and modify CN14 PN and FP (DFHS02FS032/ml1220-smt) 3.Update CN4 FP to "dp-adis0022-p001a-20p-smt"
	1211	1.Add mSATA re-driver circuit 2.Change CN22 PN & FP as same as CN13
	1212	1.Modify Hole4 FP to H-TC197BC142D142P2 2.Change mSATA redriver power rail to +1.5V
	1213	1.Add R828~R831 for co-layout 2.Add N14M-GE binary strap setting information
	1214	1.Change USB DB power to 4 pins 2.Change CN4 PN to DFTD20FR001
	1217	1.Update Hole6/Hole17/Hole22 FP 2.Add C866 by FAE suggestion 3.Change C706 from 10uF to 4.7uF 4.Add pull down 100K by EC-Anda command (R832/R833/R834) 5.Change TEMP_MBAT fromPJ1 pin 5 to pin 6 (BATT_EN#) , then pin 6 is NC pin 6.Un stuff PR96 7.Add R835 and change R785 to 5.1M ohm 8.Mark R746 to NSW@ due to pin18 of U7 has internal +3V
	1219	1.SUSLED# power from +3V_S5 to +3V_PCU (for Deep S3) 2.Change eDP connector CN8 PN and FP (DFHS40FS095 / gs12401-1011-40p-r-nh-smt)
	1220	1.Add net PCH_SUSWARN# connect to Pin78 of EC (GPJ2) 2.Add net PCH_SUSACK# connect to Pin79 of EC (GPJ3)
	1221	1.Change PR191 PU voltage from +3V to +3V_S5
	1224	1.Unstuff PR28/PR30 2.Reserve R837
	1225	1.Change PU4 PN from AL001642000 to AL001642001
	1226	1.Change U15 PN from AJ085870F03 to AJ085870F04
	1228	1.Co-layout mSATA re-driver IC-U51 (PS8521A & ASM1466)
	0102	1.Unstuff PR191 (Already PU on HW side) 2.Reserve R842/R843
	0103	1.SWAP EC pin：BATLED1# change to pin32 ; ME_WR# change to pin25
	0104	1.Change U38 PN from AJ0QPRG0T03 to AJSLJ8C0T05
	0107	1.Update Hole6/Hole17 FP 2.Update Pad1 PN to FBZRK011010 3.Update Hole4 PN to FBAJ2005010