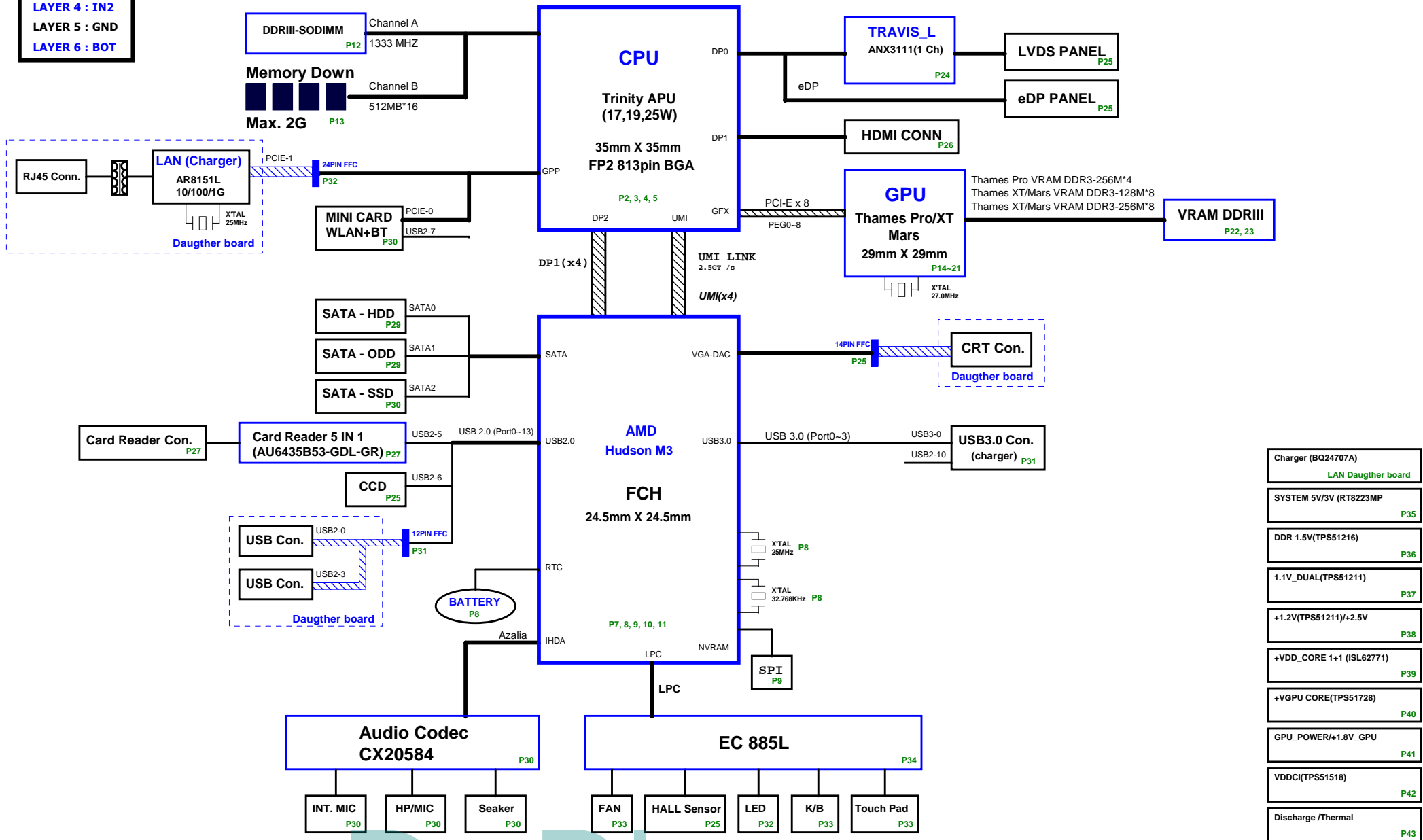


15.6" ZRP Block Diagram



PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : SVCC
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : GND
- LAYER 6 : BOT

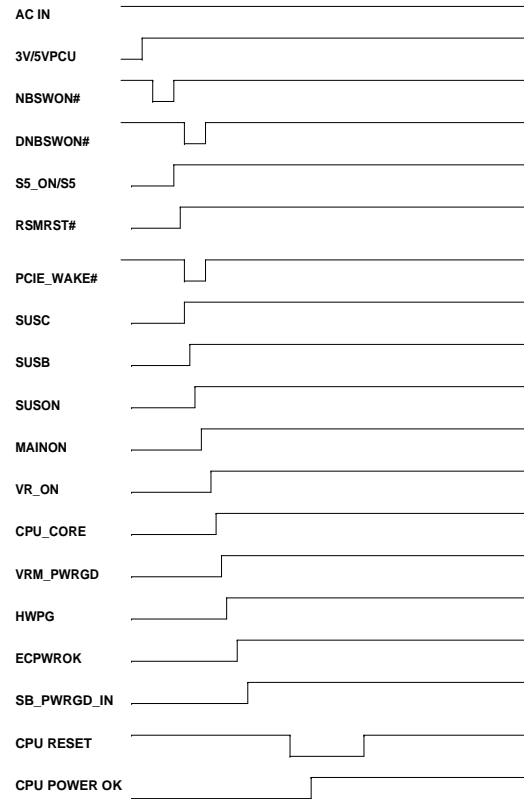


Charger (BQ24707A)
LAN Daughter board
SYSTEM 5V/3V (RT8223MP)
DDR 1.5V(TPS51216)
1.1V_DUAL(TPS51211)
+1.2V(TPS51211)/+2.5V
+VDD_CORE 1+1 (ISL62771)
+VGPU CORE(TPS51728)
GPU_POWER/+1.8V_GPU
VDDCI(TPS51518)
Discharge /Thermal

Dr-Bios.com

ITEM	DESCRIPTION	MARK
1	LVDS Panel Sku	LVDS@
2	eDP Panel Sku	eDP@
3	VGA Sku	EV@
4	VGA Thames Sku	EV_T@
5	VGA Mars Sku	EV_M@
6	VGA Sku for Thames and Mars stuff different value parts	EV_SP@
7	GPU 128bit Sku	EV_128@
8	GPU 128bit Sku of Special part value change	EV_128SP@
9	USB Charge Functions Sku	CH@
10	No USB Charge Functions Sku	NCH@
11	USB3.0 Re-Driver Sku	RD@
12	No USB3.0 Re-Driver Sku	NRD@
13	Always connect functions Sku	AC@
14	No Always connect functions Sku	NAC@
15	Special part value change or modify for different BOM sku	SP@

Power Sequence



Hudson M3 SM BUS

FCH SMBUS	Pin NO.	SMBUS Function Define
PCLK_SMB PDAT_SMB (+3V)	AD26 AD25	DDR / RFID
SCLK1 SDATA1 (+3V_S5)	T7 R7	not used
SCLK2 SDATA2 (+3V_S5)	H19 G19	EC
SCLK3 SDATA3 (+3VPCU)	G22 G21	BATTERY
SCL4 SDATA4 (+3V_S5)	J19 K19	not used

KBC(EC) SM BUS

KBC SMBUS	Pin NO.	SMBUS Function Define
MBCLK MBDATA (+3VPCU)	110 111	Battery
MBCLK_THRM MBDATA_THRM (+3VPCU)	115 116	Thermal

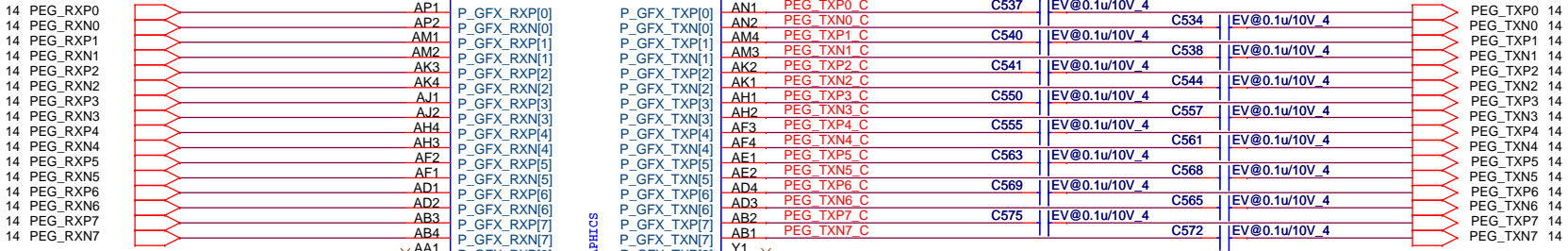
EC	FCH	Device	I2C_Device(S)
I2Ce_1(M)	I2Cf_2(M)	Charger	Battery
I2Ce_2(M)		APU	
I2Ce_3(M)			
	I2Cf_3(M)	APU	
	I2Cf_1(M)		
	I2Cf_0(M)	DDR	WLAN/3G Image Sensor

EC will Conflict with FCH.
Do not mount

PEG X 8

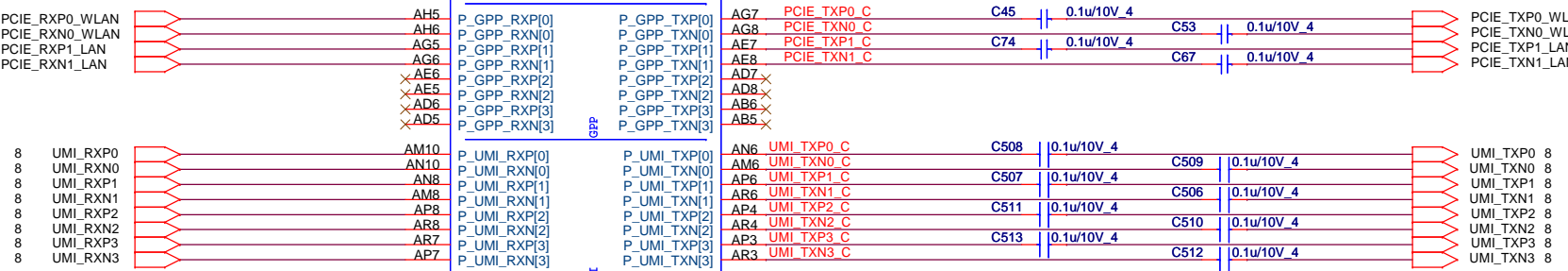
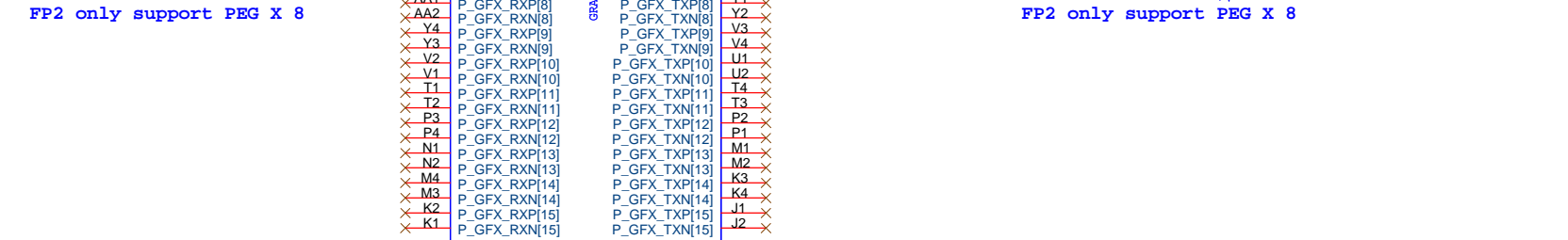
PEG X 8

U25A



TO WLAN
TO LAN

TO WLAN
TO LAN



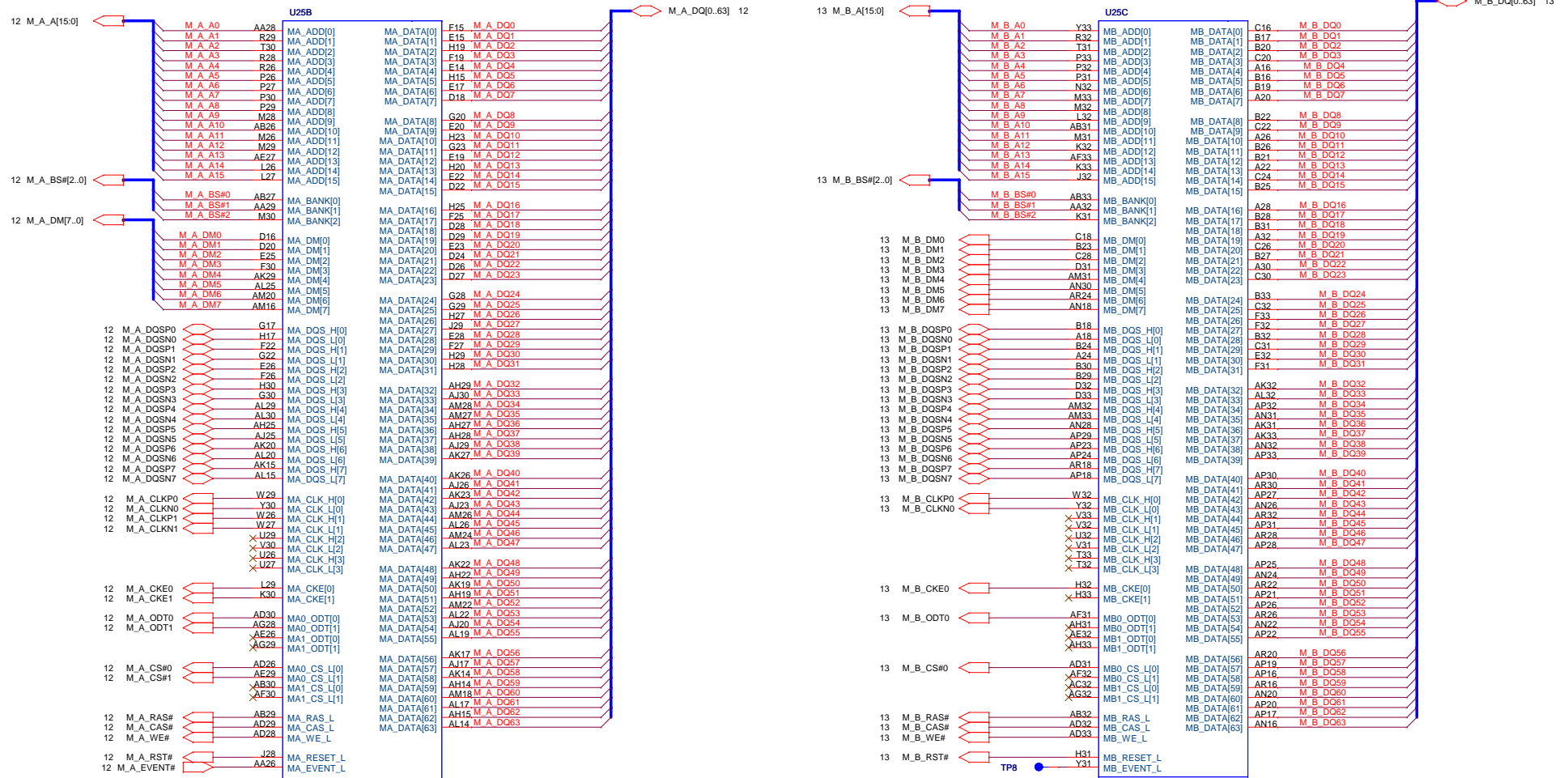
SP@TRINITY APU_BGA813

- SP : A10(AJ04655UT01)
- A8(AJ04555VT01)
- A6(AJ04455UT01)
- A4(AJ04355UT00)

Quanta Computer Inc.
PROJECT : ZRP

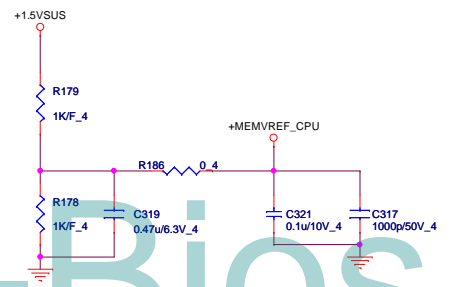
Size	Document Number	Rev
	APU 1/4(PCIE/UMI/GPP/HDT)	A1A
Date:	Friday, June 01, 2012	Sheet 3 of 44

Soldermask openings for all bottom side vias/TPs under FS1



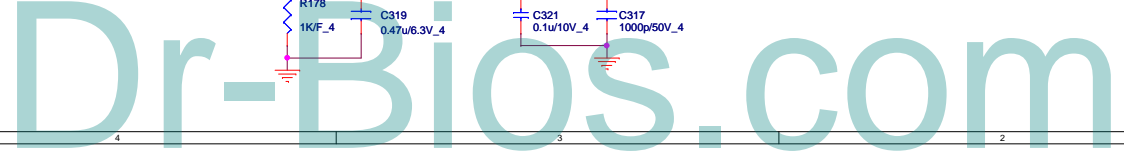
+MEMVREF_CPU R410 39.2/F 4 +M_ZVDDIO AJ32
 +1.5VSUS R179 1K/F_4
 Place close to APU within 1" SP@TRINITY APU_BGA813

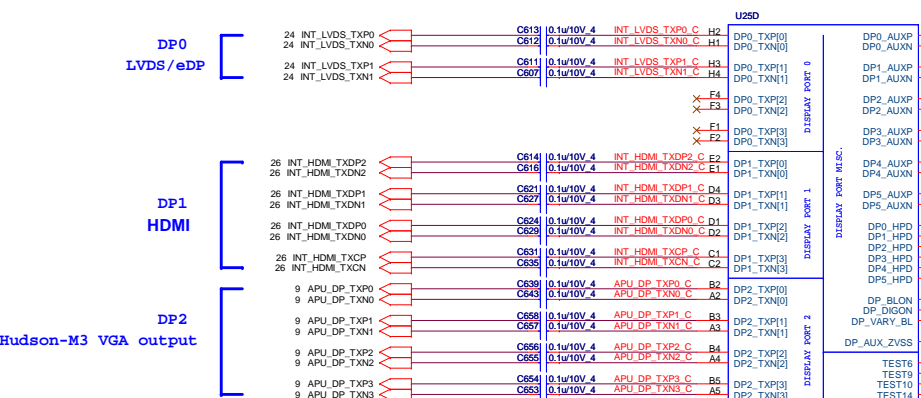
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 A8(AJ04555VT01)
 A6(AJ04455UT01)
 A4(AJ04355UT00)



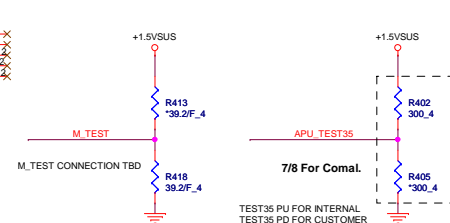
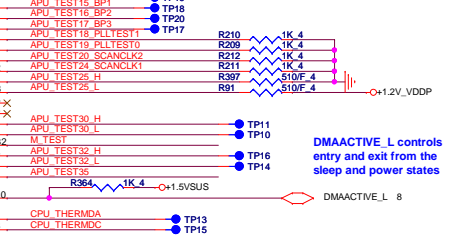
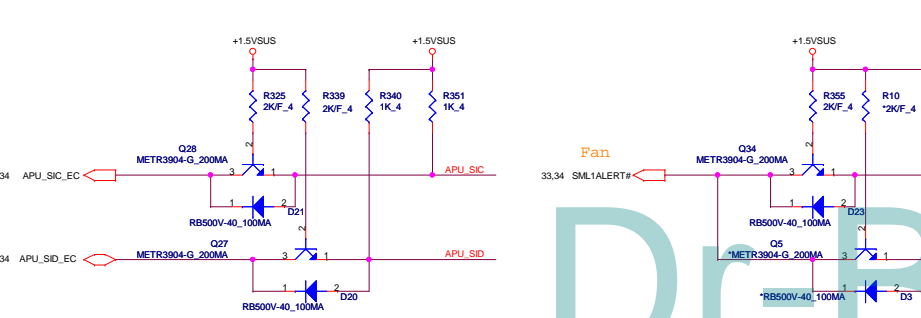
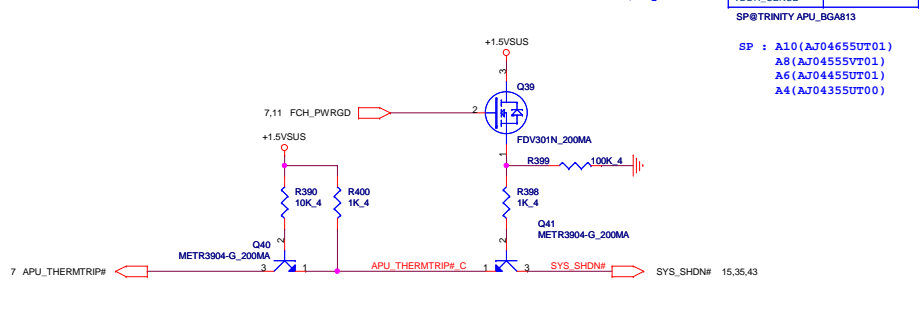
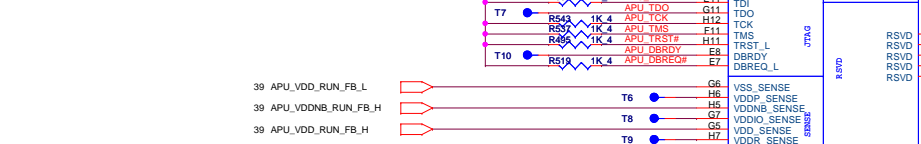
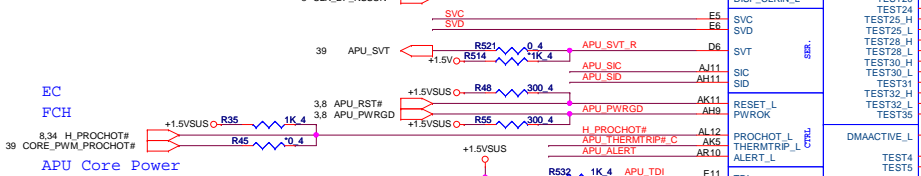
SP@TRINITY APU_BGA813

SP : A10(AJ04655UT01)
 A8(AJ04555VT01)
 A6(AJ04455UT01)
 A4(AJ04355UT00)

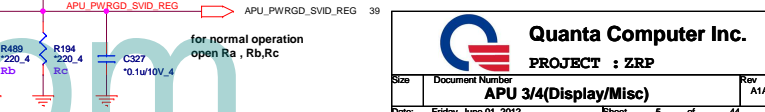
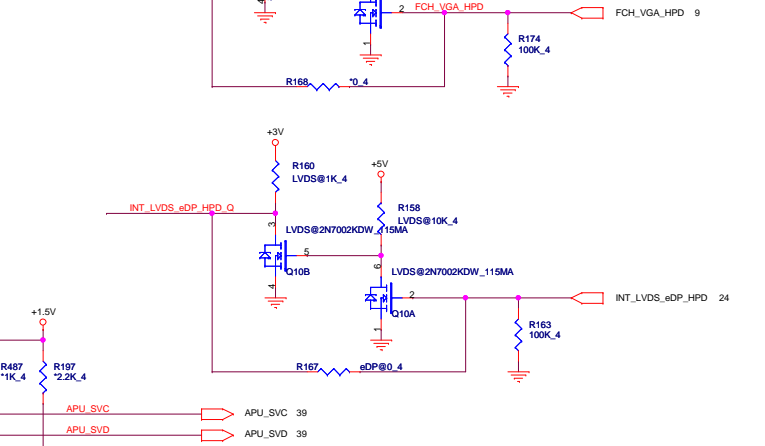
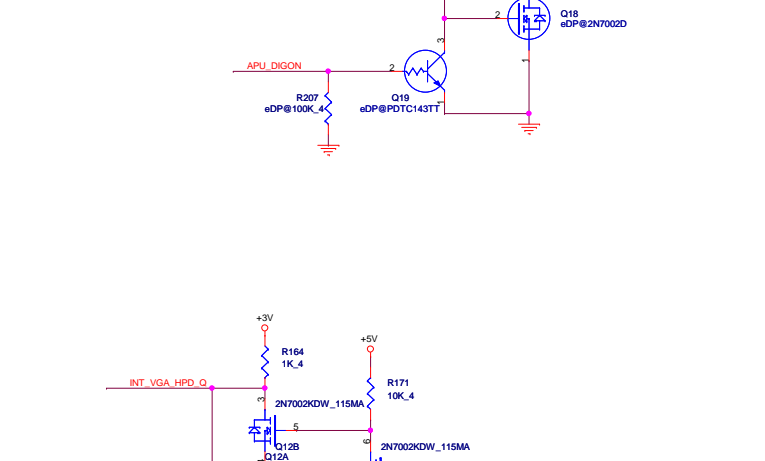
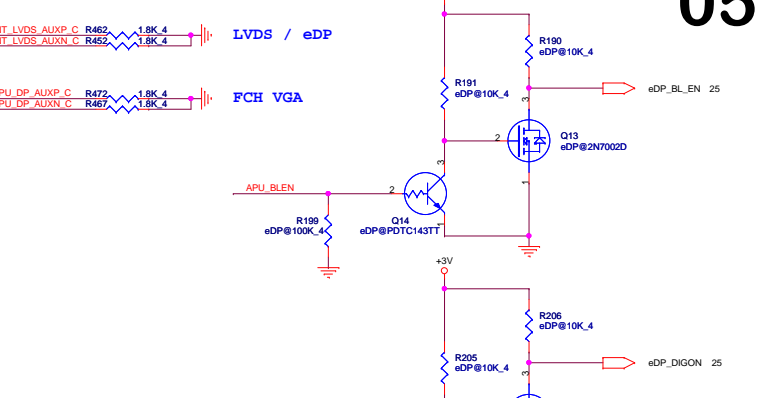




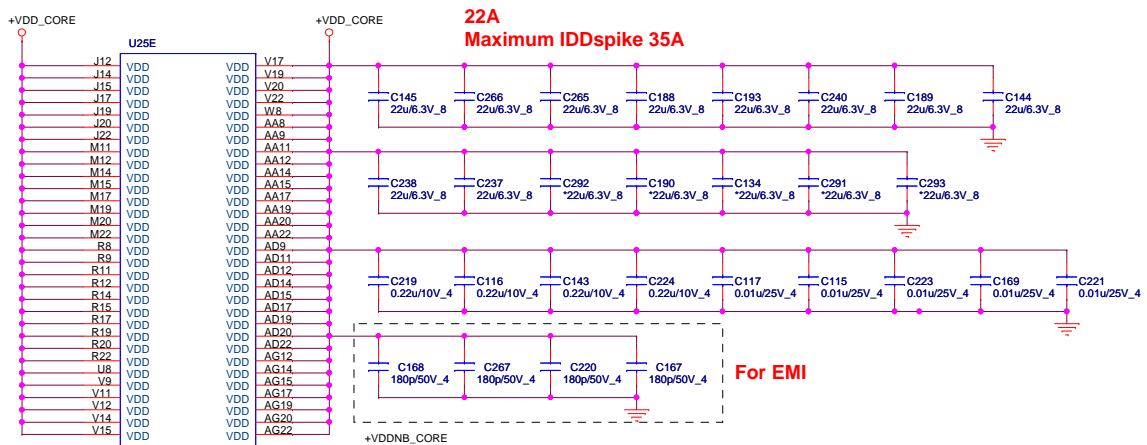
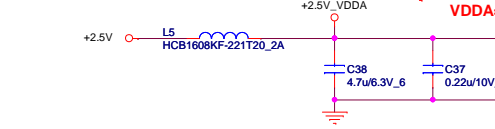
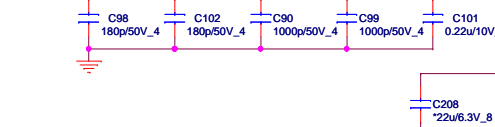
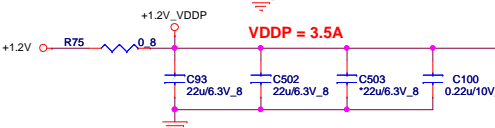
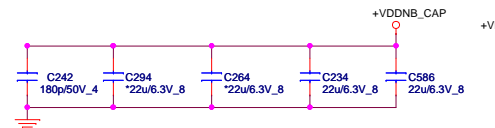
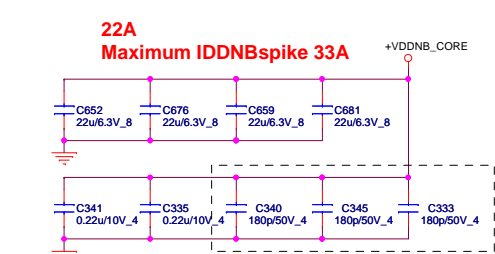
Note: CLK_APU_HCLKP/N is 100MHZ SSC
 Note: CLK_DP_NSSCP/N is 100MHZ non-SSC



BOOT VOLTAGE				
SVC	SVD	VFIX_+VDD =VCC/GND	VFIX_+VDD =OPEN	
0	0	1.1	1.1	
0	1	1.0	1.2	
1	0	0.9	1.0	
1	1	0.8	0.8	

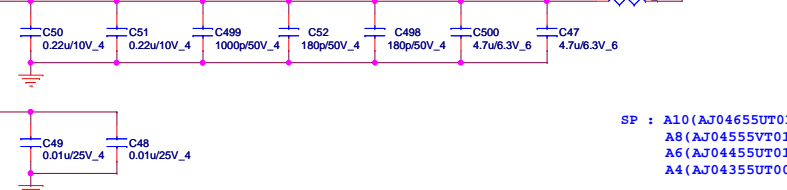
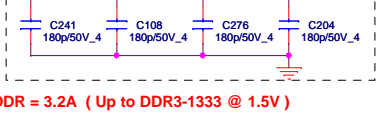


Quanta Computer Inc.
 PROJECT : ZRP
 Document Number: APU 3/4(Display/Misc)
 Date: Friday, June 01, 2012
 Sheet: 5 of 44

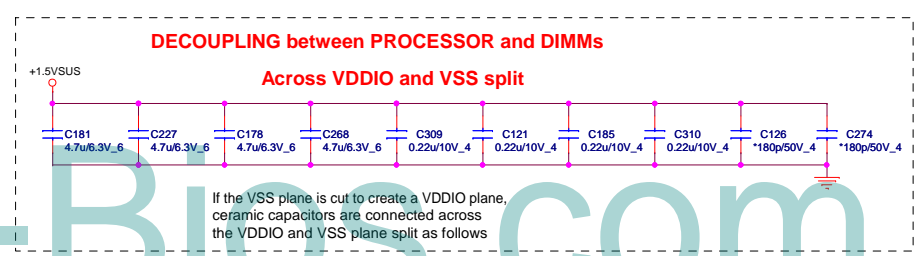


APU POWER TABLE

PIN NAME	NET NAME	VOLTAGE
VDD	+VDD_CORE	1.0V - 1.3V
VDDNB	+VDDNB_CORE	1.06V - 1.325V
VDDIO	+1.5VSUS	1.5V
VDDP	+1.2V_VDDP	+1.2V
VDDA	+2.5V_VDDA	+2.5V



SP : A10(AJ04655UT01)
 A8(AJ04555VT01)
 A6(AJ04455VT01)
 A4(AJ04355UT00)

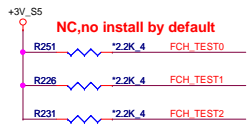


U25F

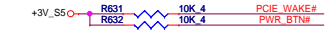
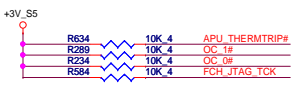
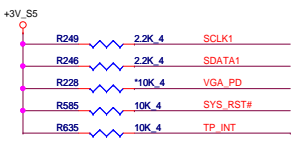
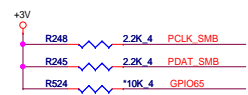
A17	VSS	V11
A19	VSS	Y12
A21	VSS	Y14
A23	VSS	Y15
A25	VSS	Y17
A27	VSS	Y19
A29	VSS	Y20
A31	VSS	Y22
B1	VSS	AA4
C4	VSS	AA5
C33	VSS	AB7
D5	VSS	AB8
D9	VSS	AC1
D11	VSS	AC2
D13	VSS	AC4
D15	VSS	AC9
D17	VSS	AC11
D19	VSS	AC12
D21	VSS	AC14
D23	VSS	AC15
D25	VSS	AC17
D30	VSS	AC19
E4	VSS	AC20
E8	VSS	AC22
E27	VSS	AC23
E29	VSS	AC25
E30	VSS	AE4
E33	VSS	AE9
F5	VSS	AE11
F6	VSS	AE12
F7	VSS	AE14
F8	VSS	AE15
F17	VSS	AE17
F20	VSS	AF19
F23	VSS	AF20
F28	VSS	AF22
F29	VSS	AF23
G1	VSS	AF25
G2	VSS	AG1
G4	VSS	AG2
G15	VSS	AG4
G19	VSS	AG9
G25	VSS	AG11
G26	VSS	AG26
G27	VSS	AH7
G33	VSS	AH17
H8	VSS	AH20
H9	VSS	AH23
H22	VSS	AH26
H26	VSS	AH30
J4	VSS	AJ4
J8	VSS	AJ5
J9	VSS	AJ6
J11	VSS	AJ7
J23	VSS	AJ9
J25	VSS	AJ14
J26	VSS	AJ15
J27	VSS	AJ19
J30	VSS	AJ22
K9	VSS	AJ27
K11	VSS	AJ28
K12	VSS	AJ33
K14	VSS	AK6
K15	VSS	AK8
K17	VSS	AK25
K19	VSS	AK28
K20	VSS	AK30
K22	VSS	AL1
L1	VSS	AL2
L2	VSS	AL4
L4	VSS	AL8
M8	VSS	AL11
M23	VSS	AL27
M25	VSS	AL28
N4	VSS	AL33
N11	VSS	AM5
N12	VSS	AM7
N14	VSS	AM8
N15	VSS	AM9
N17	VSS	AM11
N19	VSS	AM15
N20	VSS	AM17
N22	VSS	AM19
N23	VSS	AM21
R1	VSS	AM23
R2	VSS	AM25
R4	VSS	AM29
T9	VSS	AM30
T11	VSS	AN3
T12	VSS	AN4
T14	VSS	AN33
T15	VSS	AP5
T17	VSS	AP9
T19	VSS	AR2
T20	VSS	AR5
T22	VSS	AR9
U4	VSS	AR17
W1	VSS	AR19
W2	VSS	AR21
W4	VSS	AR23
W5	VSS	AR25
W6	VSS	AR27
W7	VSS	AR29
Y9	VSS	AR31

Quanta Computer Inc.
PROJECT : ZRP

Size	Document Number	Rev
	APU 4/4(Power/GND)	A1A
Date:	Friday, June 01, 2012	Sheet 6 of 44

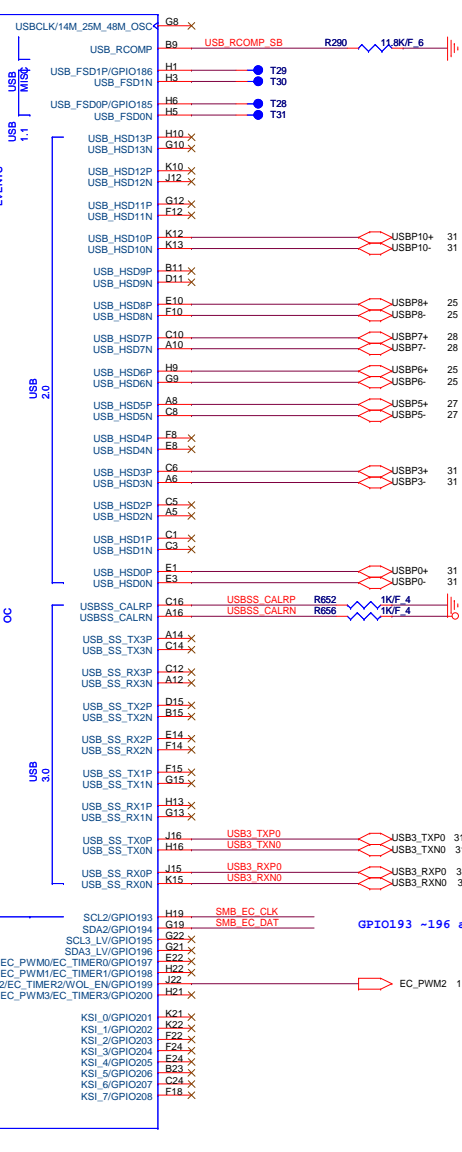
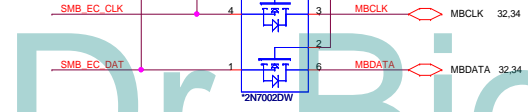
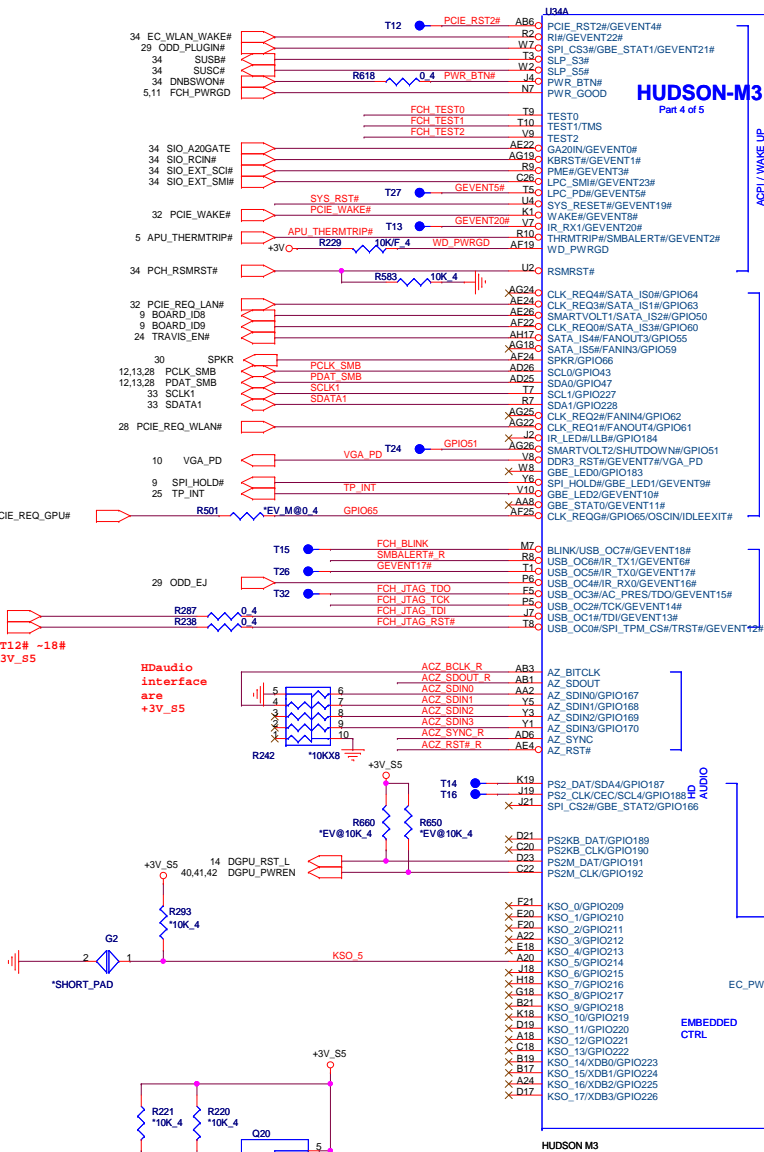
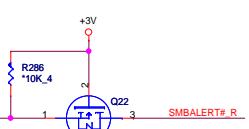
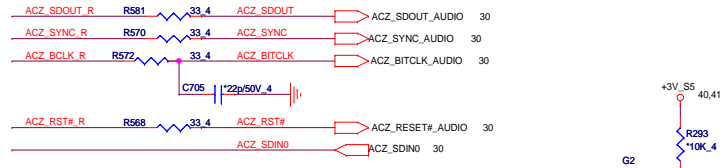


remove pull hi (chip internal have pull hi)



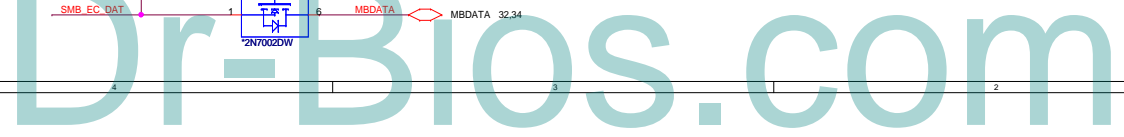
Note:LLB#, WAKE# and PWR_BTN need pull up to +3VPCU only if S5+ mode is supported

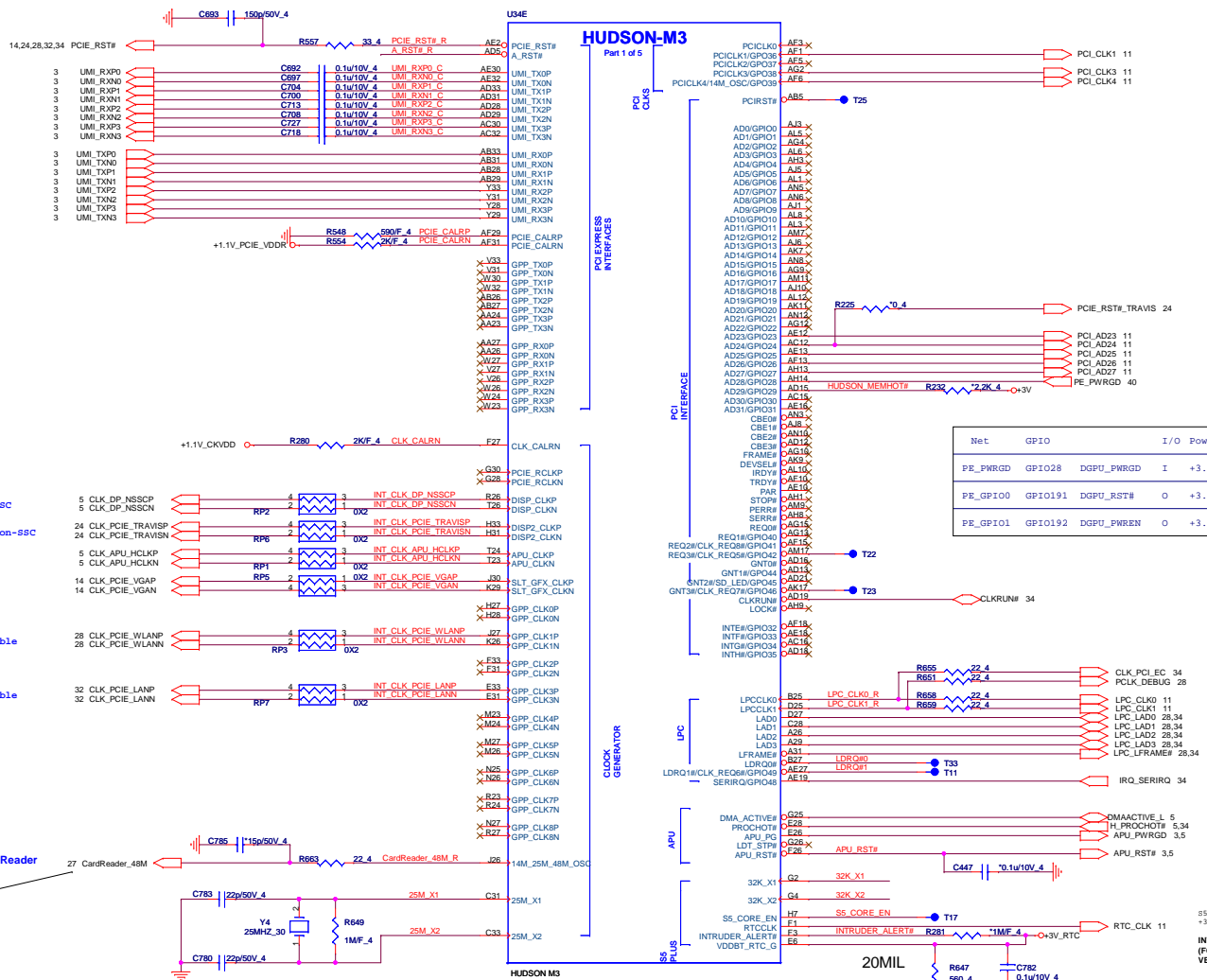
To Azalia



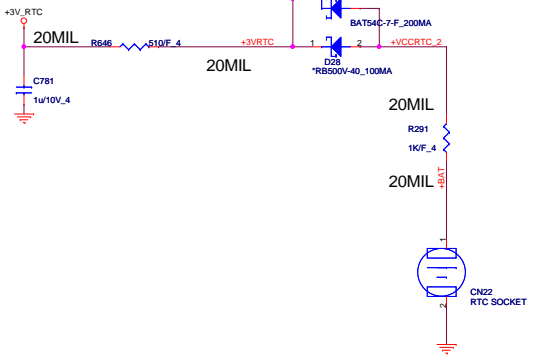
Quanta Computer Inc.
 PROJECT : ZRP

Size Document Number FCH 115/(GPIO/USB/AZ) Rev A1A
 Date: Friday, June 01, 2012 Sheet 7 of 44



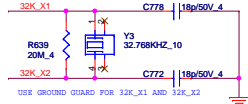


RTC Circuitry(RTC)



Net	GPIO	I/O	Power Well	DOS
PE_PWRGD	GPIO28	DGPU_PWRGD	I +3.3V	"0->1"
PE_GPIO0	GPIO191	DGPU_RST#	O +3.3V	"0->1"
PE_GPIO1	GPIO192	DGPU_PWRN	O +3.3V	"0->1"

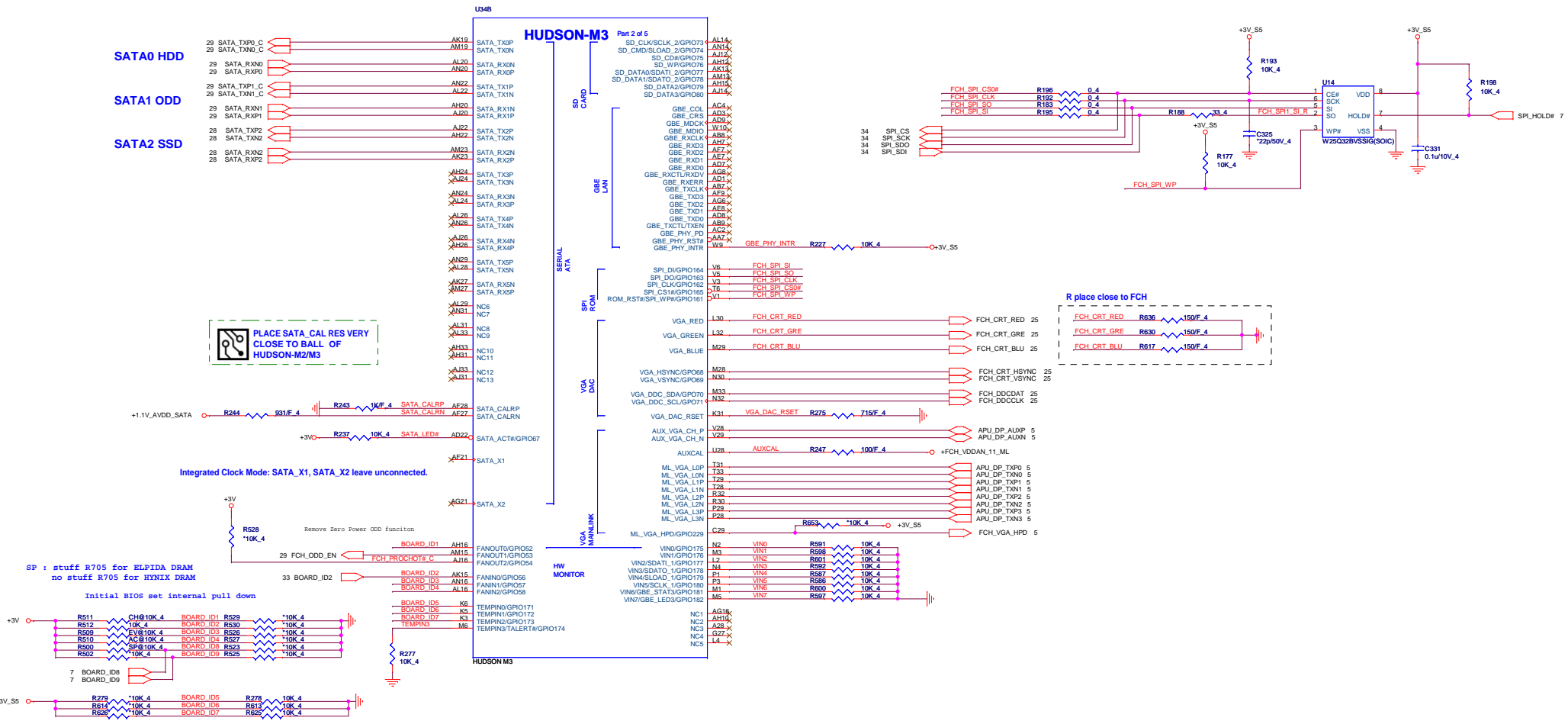
For EMI



S5_CORE_EN is necessary to connect enable pin of +3VPCU/+5VPCU regulator for S5+ mode implementation
 INTRUDER_ALERT# Left not connected (FCH has 50-kohm Internal pull-up to VBAT).

For CardReader 48M layout issues

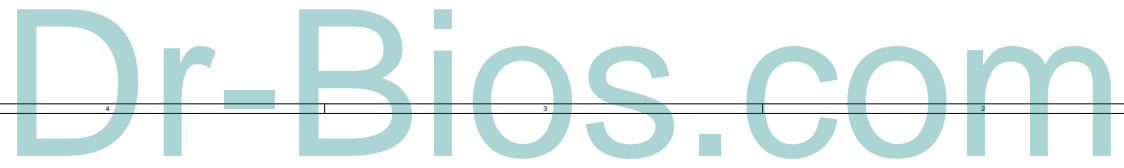
Quanta Computer Inc.
PROJECT :ZRP
 Size: _____ Document Number: **FCH 2/5(ACP/PCI/CLK)** Rev: **A1A**
 Date: **Frid, June 01, 2012** Sheet: **8** of **44**



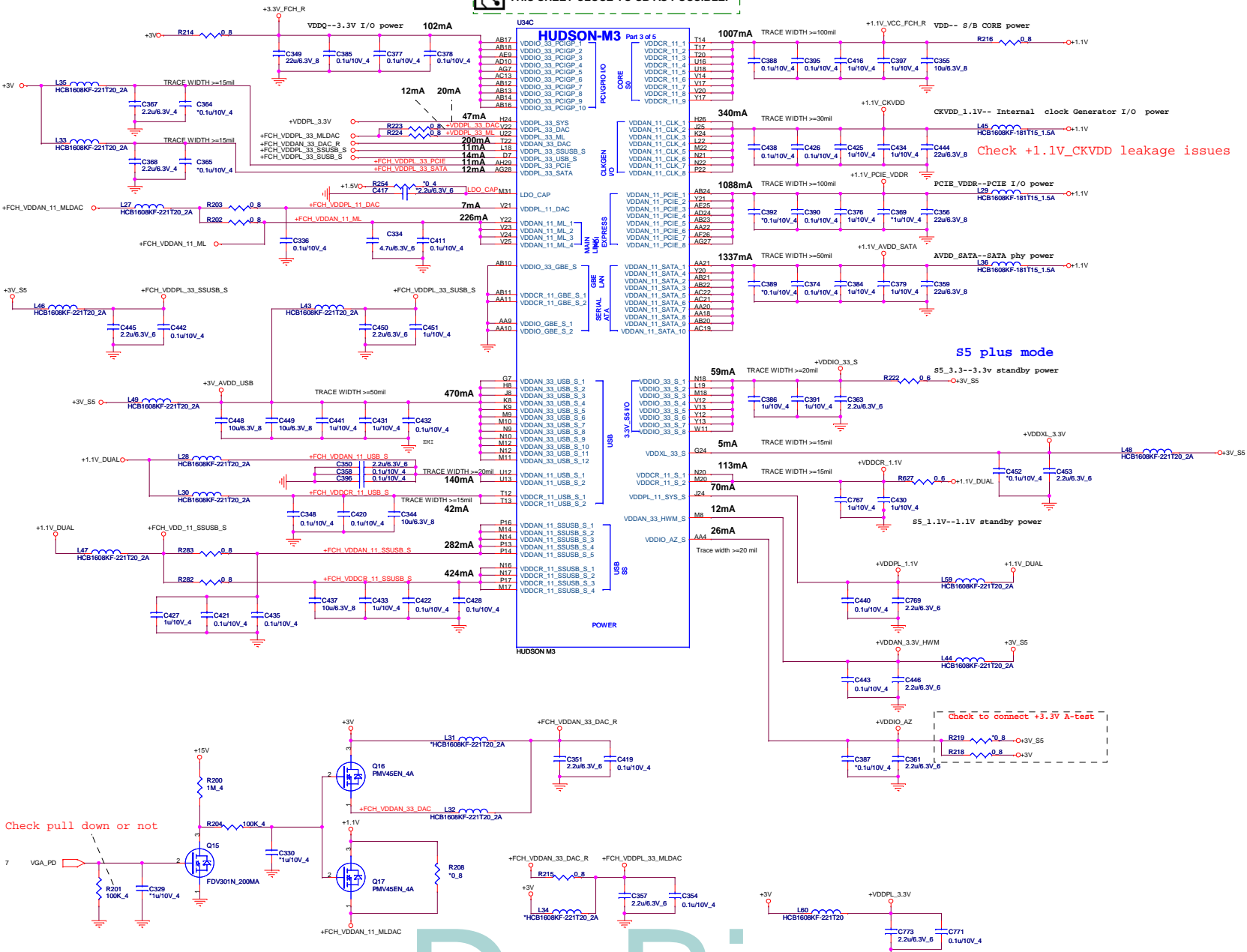
BOARD ID SETTING ID5, ID6, ID7, S5 Power State

Board ID	ID1	ID2	ID3	ID4	ID5	ID6	ID7	ID8	ID9
USB Charge	H								
No USB Charge	L								
Synaptics ELAN		H							
VGA SKU UMA SKU			H						
AC No AC				H					
Reserve					H				
Reserve						H			
Reserve							H		
ELPIDA DRAM HYNIX DRAM								H	L
Reserve									H

Quanta Computer Inc.
PROJECT : ZRP
 Size Document Number **FCH 3/5(SATA/VGA/GND/SPI)** Rev A1A
 Date: Friday, June 01, 2012 Sheet 9 of 44



PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.




HUDSON-M3 Part 5 of 5		
A3	VSS_1	T25
A3	VSS_2	T27
B1	VSS_3	T28
B1	VSS_4	T29
D13	VSS_5	T30
D13	VSS_6	T31
E16	VSS_7	T32
E16	VSS_8	T33
F7	VSS_9	T34
F7	VSS_10	T35
F14	VSS_11	T36
F14	VSS_12	T37
F14	VSS_13	T38
F14	VSS_14	T39
F14	VSS_15	T40
F14	VSS_16	T41
F14	VSS_17	T42
F14	VSS_18	T43
F14	VSS_19	T44
F14	VSS_20	T45
F14	VSS_21	T46
F14	VSS_22	T47
F14	VSS_23	T48
F14	VSS_24	T49
F14	VSS_25	T50
F14	VSS_26	T51
F14	VSS_27	T52
F14	VSS_28	T53
F14	VSS_29	T54
F14	VSS_30	T55
F14	VSS_31	T56
F14	VSS_32	T57
F14	VSS_33	T58
F14	VSS_34	T59
F14	VSS_35	T60
F14	VSS_36	T61
F14	VSS_37	T62
F14	VSS_38	T63
F14	VSS_39	T64
F14	VSS_40	T65
F14	VSS_41	T66
F14	VSS_42	T67
F14	VSS_43	T68
F14	VSS_44	T69
F14	VSS_45	T70
F14	VSS_46	T71
F14	VSS_47	T72
F14	VSS_48	T73
F14	VSS_49	T74
F14	VSS_50	T75
F14	VSS_51	T76
F14	VSS_52	T77
F14	VSS_53	T78
F14	VSS_54	T79
F14	VSS_55	T80
F14	VSS_56	T81
F14	VSS_57	T82
F14	VSS_58	T83
F14	VSS_59	T84
F14	VSS_60	T85
F14	VSS_61	T86
F14	VSS_62	T87
F14	VSS_63	T88
F14	VSS_64	T89
F14	VSS_65	T90
F14	VSS_66	T91
F14	VSS_67	T92
F14	VSS_68	T93
F14	VSS_69	T94
F14	VSS_70	T95
F14	VSS_71	T96
F14	VSS_72	T97
F14	VSS_73	T98
F14	VSS_74	T99
F14	VSS_75	T100
F14	VSS_76	T101
F14	VSS_77	T102
F14	VSS_78	T103
F14	VSS_79	T104
F14	VSS_80	T105
F14	VSS_81	T106
F14	VSS_82	T107
F14	VSS_83	T108
F14	VSS_84	T109
F14	VSS_85	T110
F14	VSS_86	T111
F14	VSS_87	T112
F14	VSS_88	T113
F14	VSS_89	T114
F14	VSS_90	T115
F14	VSS_91	T116
F14	VSS_92	T117
F14	VSS_93	T118
F14	VSS_94	T119
F14	VSS_95	T120
F14	VSS_96	T121
F14	VSS_97	T122
F14	VSS_98	T123
F14	VSS_99	T124
F14	VSS_100	T125

Check pull down or not

Check to connect +3.3V A-test

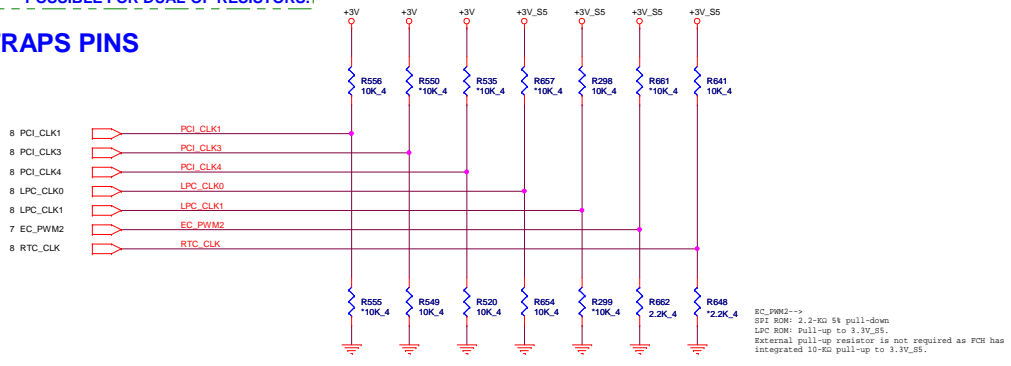
Check +1.1V_CKVDV leakage issues


Quanta Computer Inc.
 PROJECT : ZRP
 Size : Document Number
FCH 4/5(POWER)
 Date : Friday, June 01, 2012
 Sheet 10 of 44



OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

STRAPS PINS

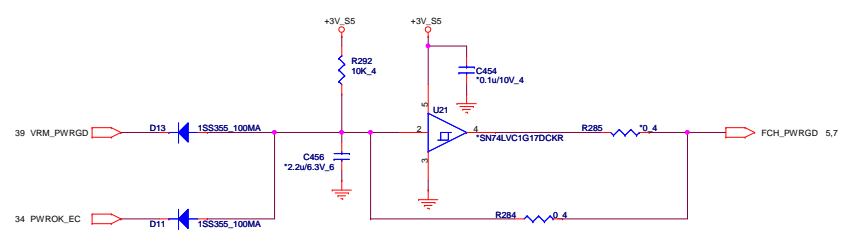


Remove PCI_CLK2 function

REQUIRED STRAPS

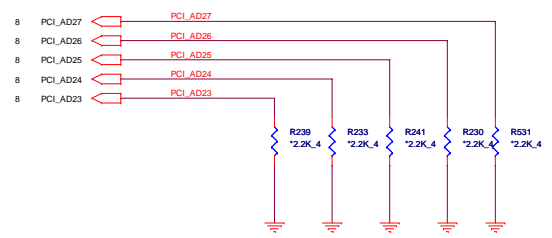
	-----	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	-----	ALLOW PCIE Gen2 DEFAULT	-----	USE DEBUG STRAP	non_Fusion CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	SS PLUS MODE DISABLED DEFAULT
PULL LOW	-----	FORCE PCIE Gen1	-----	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM DEFAULT	SS PLUS MODE ENABLED

FCH PWRGD CKT



DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

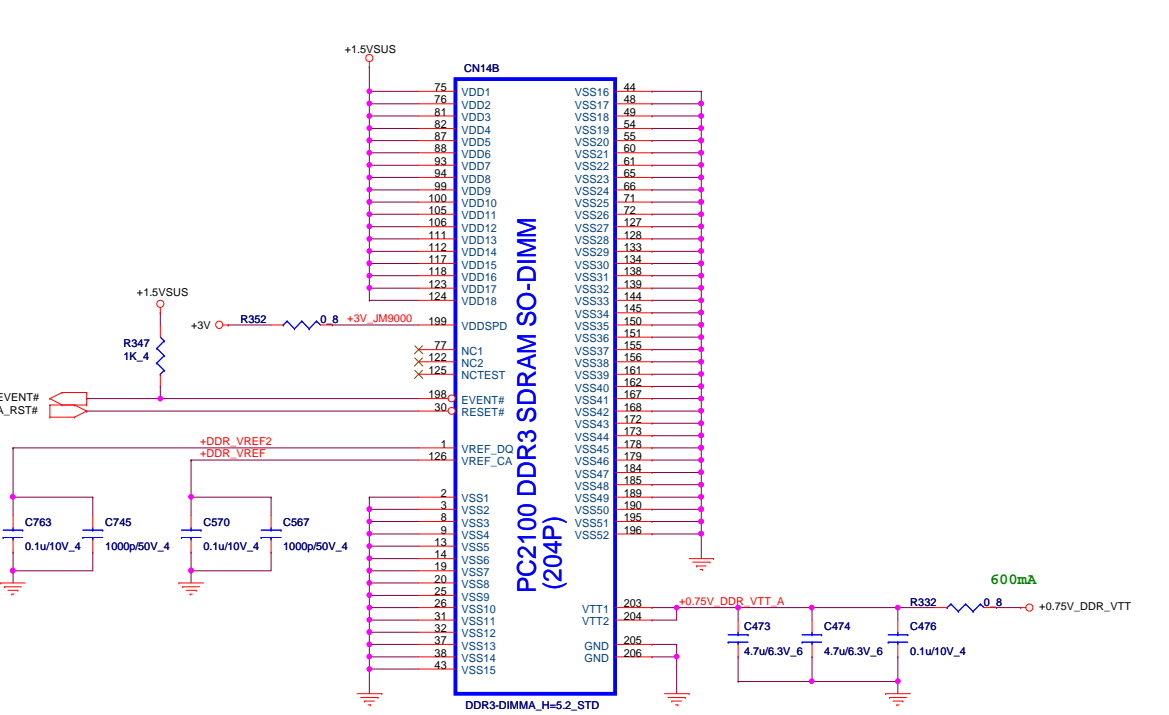
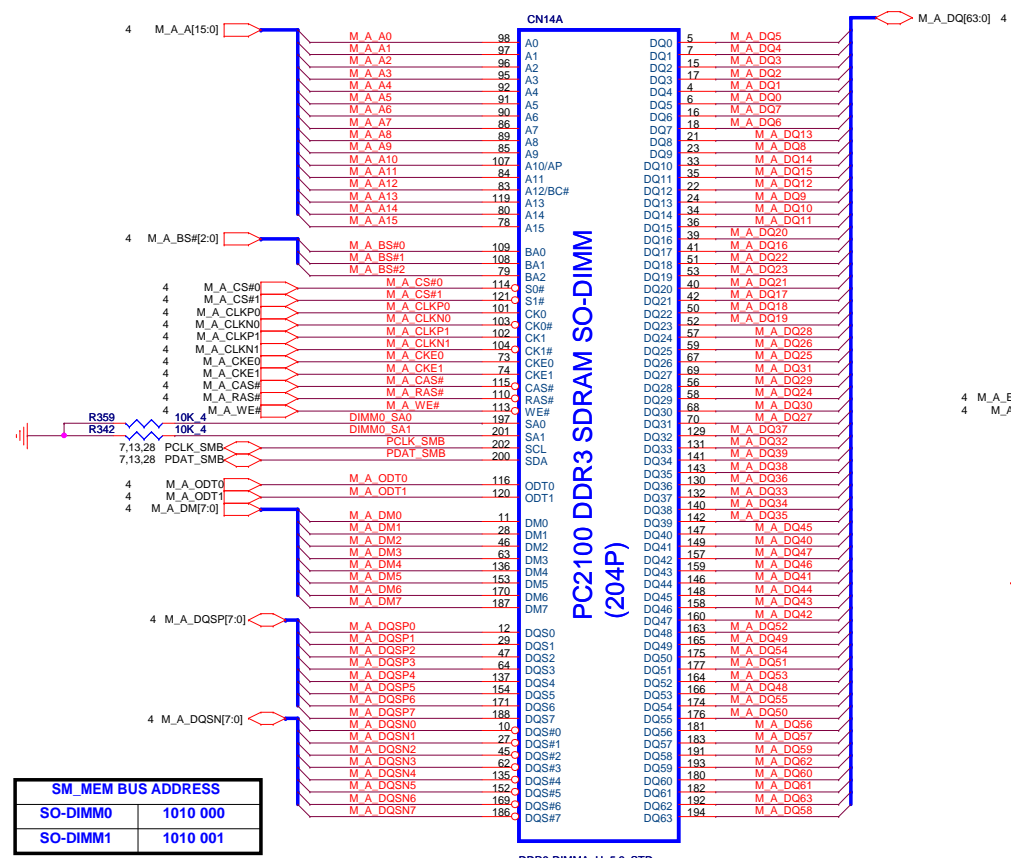
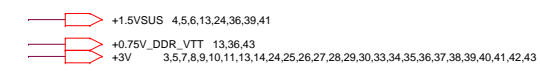


	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

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PROJECT : ZRP

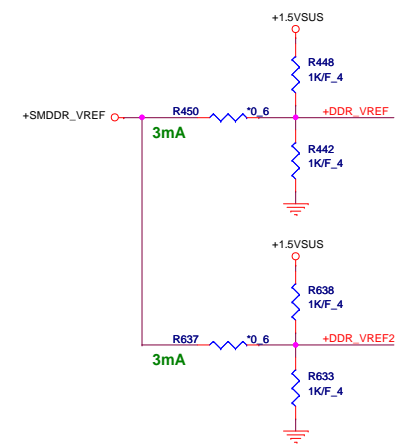
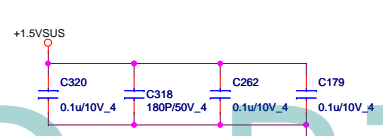
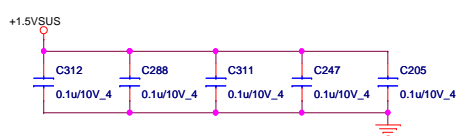
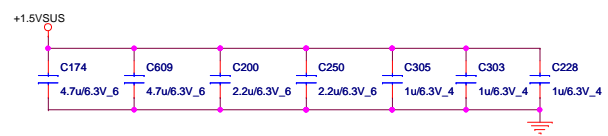
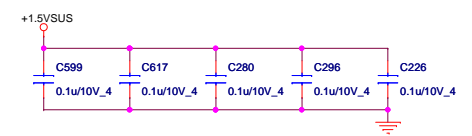
Size	Document Number	Rev
	FCH 5/5(STRAP & PWRGD)	A1/A
Date: Friday, June 01, 2012	Sheet	11 of 44

DDR3 DIMM-A



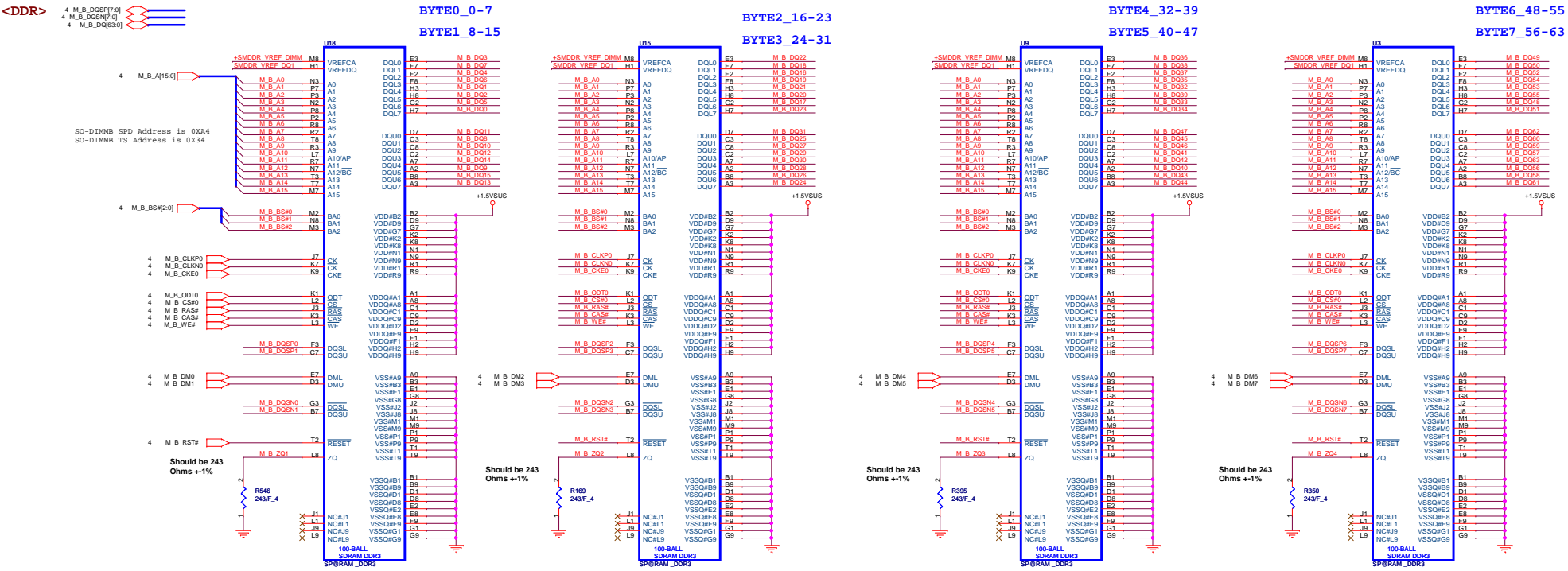
SM_MEM BUS ADDRESS	
SO-DIMM0	1010 000
SO-DIMM1	1010 001

Place these Caps near So-Dimm A

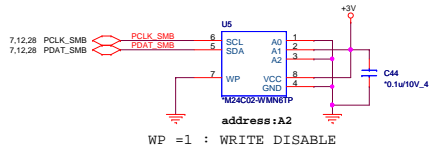


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PROJECT : ZRP

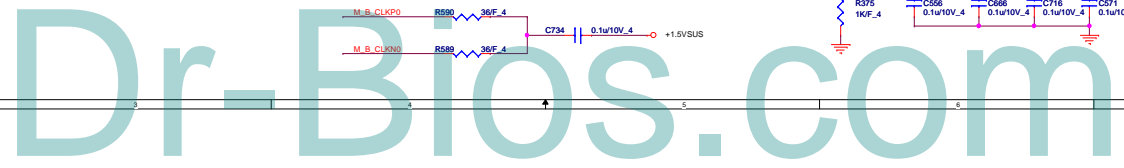
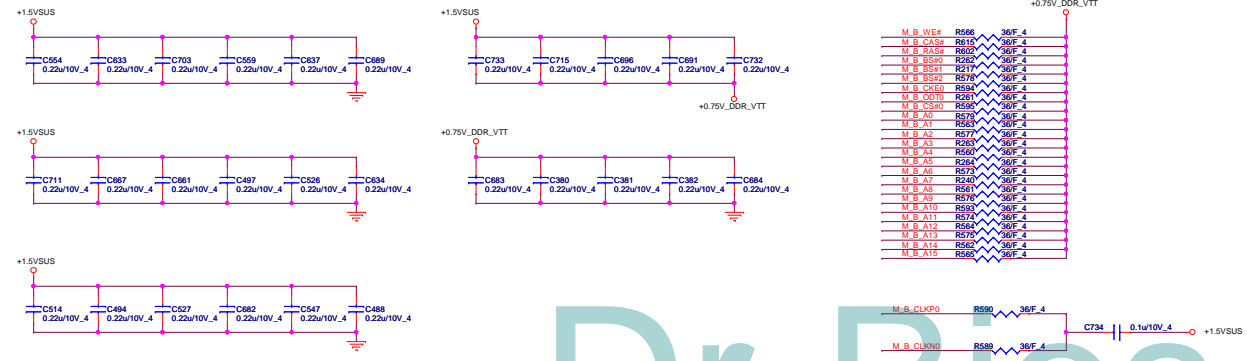
Size	Document Number	Rev
	DDR3 SO-DIMM A	A1A
Date:	Friday, June 01, 2012	Sheet 12 of 44

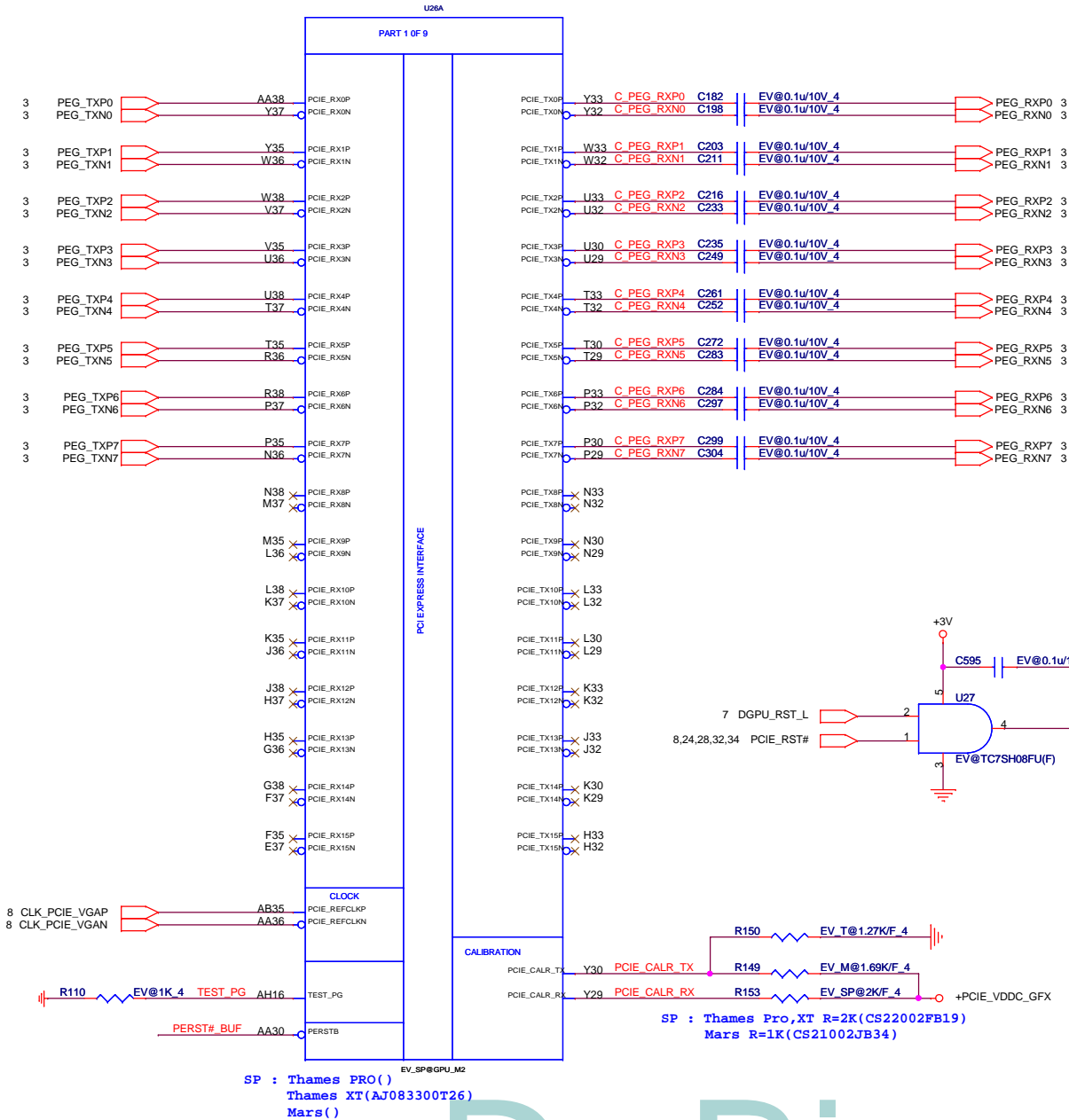


SP : ELPIDA DRAM P/N : AKD5JGST400
 HYNIX DRAM P/N : AKD5JGQW101

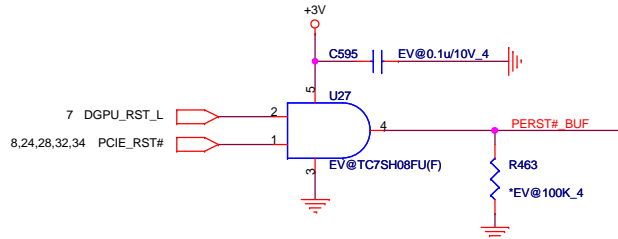
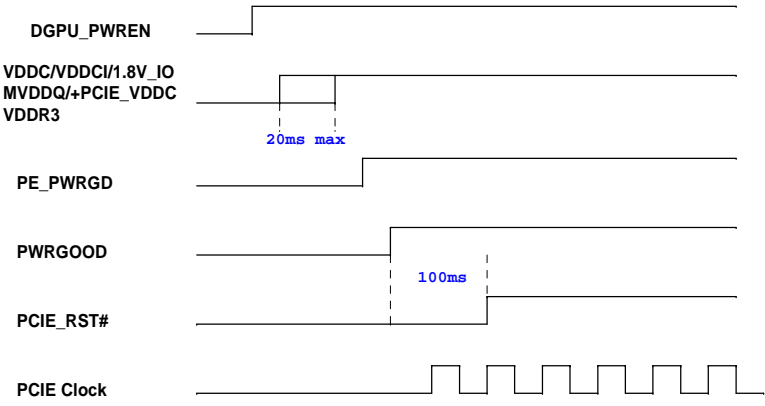


Place these Caps near Memory Down





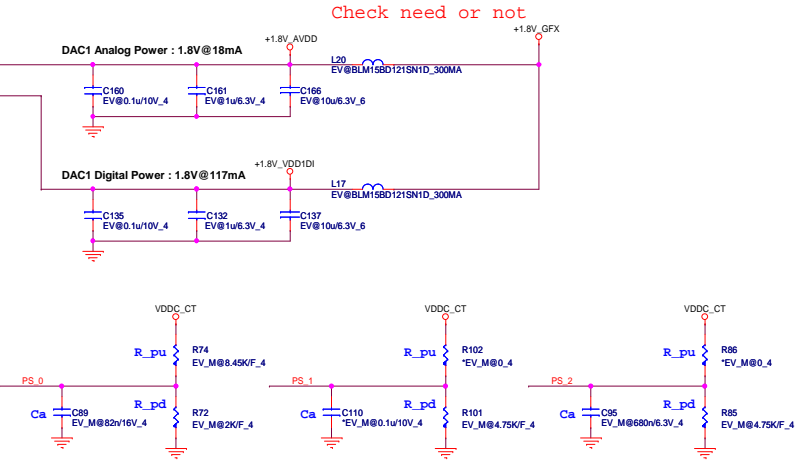
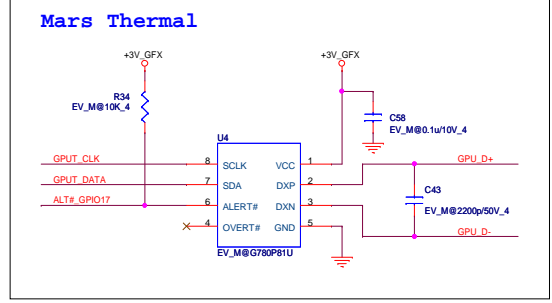
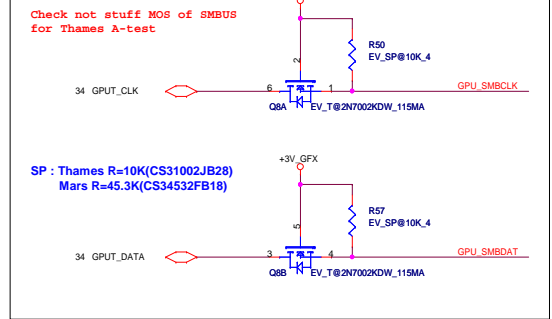
**Thames(Pro,XT) and Mars Power-on sequence
PX5.0(no BACO)**



Quanta Computer Inc.
PROJECT : ZRP

Size	Document Number	Rev
	Thames_M2/ PEG*16	A1A
Date:	Friday, June 01, 2012	Sheet 14 of 44

Thames Pro, XT Thermal



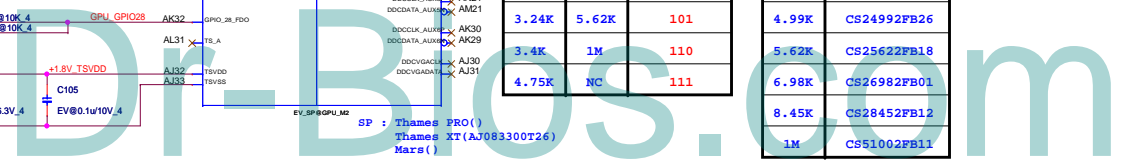
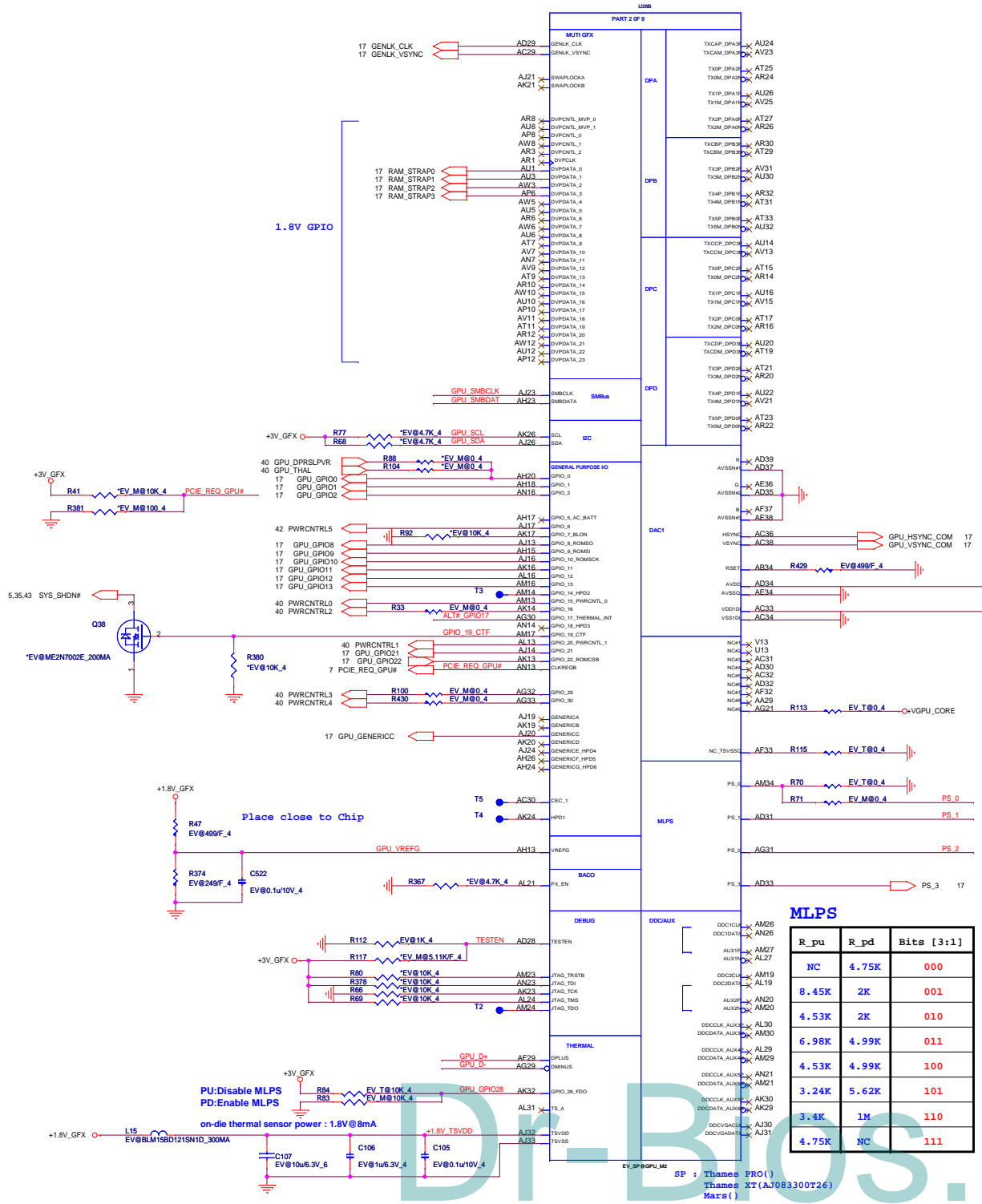
MLPS

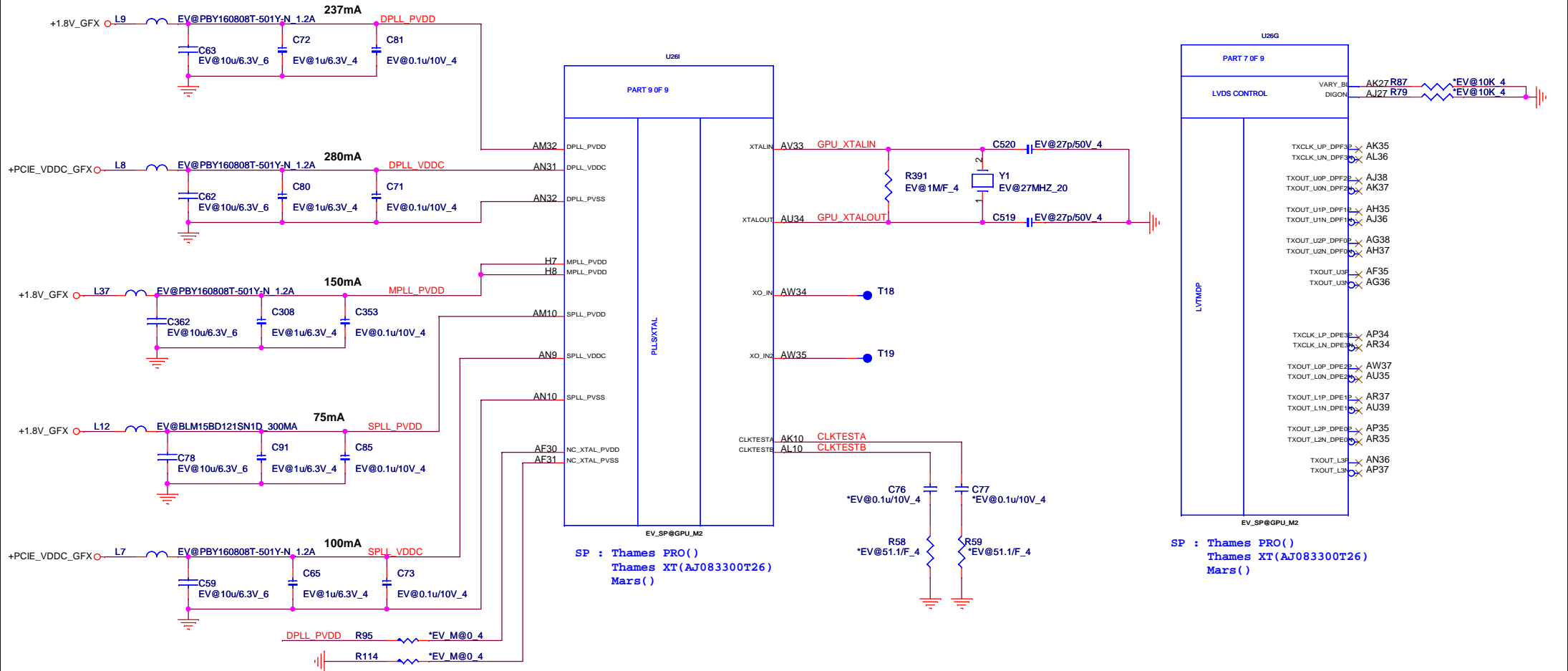
R_pu	R_pd	Bits [3:1]
NC	4.75K	000
8.45K	2K	001
4.53K	2K	010
6.98K	4.99K	011
4.53K	4.99K	100
3.24K	5.62K	101
3.4K	1M	110
4.75K	NC	111

Ra	P/N
2K	CS22002FB19
3.24K	CS23242FB09
3.4K	CS23402FB08
4.53K	CS24532FB08
4.75K	CS24752FB12
4.99K	CS24992FB26
5.62K	CS25622FB18
6.98K	CS26982FB01
8.45K	CS28452FB12
1M	CS51002FB11


MLPS Bit	Bits [5:1]
PS_0	01001
PS_1	11000
PS_2	00000
PS_3	00XXX

Ca	Bits [5:4]	P/N
680nF	00	CH4681K9B00
82nF	01	CH3823K1B00
10nF	10	CH31003KB11
NC	11	





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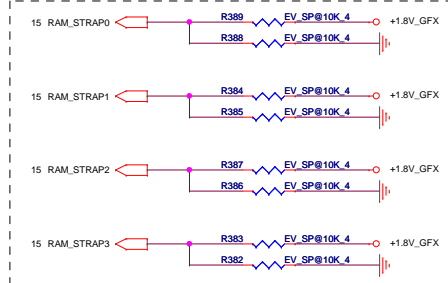
 Quanta Computer Inc. PROJECT : ZRP		Rev A1A
Date:	Friday, June 01, 2012	Sheet 16 of 44

Thames Pro,XT USE Mars USE

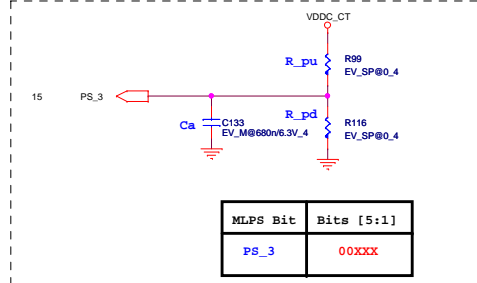
Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP3 DVPDATA_3	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0	MLPS
Hynix	H5TQ1G63DFR-11C (64M*16)	AKD5LZWTW05 * 8	1GB	0	0	0	0	000
	H5TQ2G63DFR-11C (128M*16)	AKD5MGWTW17 * 4	1GB	0	0	0	1	
		AKD5MGWTW17 * 8	2GB	0	0	1	0	001
Samsung	K4W1G1646G-BC11 (64M*16)	AKD5EGGT500 * 8	1GB	0	1	0	0	010
	K4W2G1646C-HC11 (128M*16)	AKD5MGWT500 * 4	1GB	0	1	0	1	
		AKD5MGWT500 * 8	2GB	0	1	1	0	011
AMD	23EY2387MC11 (64M*16)	AKD5EZWT700 * 8	1GB	1	0	0	0	100
	23EY4187MC11 (128M*16)	AKD5DZWT700 * 4	1GB	1	0	0	1	
		AKD5DZWT700 * 8	2GB	1	0	1	0	101

CONFIGURATION STRAPS -- SEE EACH DATABOOK FOR STRAP DETAILS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET				Default Setting
STRAPS	MLPS	GPIO PIN	DESCRIPTION OF DEFAULT SETTINGS	
MLPS_DISABLE	NA	GPIO_28_FDO	Enable MLPS, NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP	X
TX_PWRS_ENB	PS_1[4]	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X
TX_DEEMPH_EN	PS_1[5]	GPIO1	PCIe Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	X
BIF_GEN3_EN_A	PS_1[1]	GPIO2	PCIe Gen3 Enable (NOTE: RESERVED for Thames/Whistler/Seymour) 0: GEN3 not supported at power-on 1: GEN3 supported at power-on	1
BIF_VGA_DIS	PS_2[4]	GPIO9	VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	PS_0[3:1]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type 100 - 512Kbit M25P05A (ST) 101 - 1Mbit M25P10A (ST) 101 - 2Mbit M25P20 (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 100 - 512Kbit Pm25LV12 (Chingis) 101 - 1Mbit Pm25LV10 (Chingis)	XXX
BIOS_ROM_EN	PS_2[3]	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled	X
AUD[1] AUD[0]	NA NA	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
CEC_DIS	PS_0[4]	GENLK_VSYNC	Enable CEC function. Reserved for Thames/Whistler/Seymour 0: Disabled 1: Enabled	X
RESERVED RESERVED RESERVED	PS_1[3] PS_1[2] NA	GENLK_CLK GPIO8 GPIO21 GENERICC	NOTE: ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR IF THESE GPIOs ARE USED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET Reserved Reserved Reserved Reserved (for Thames/Whistler/Seymour only)	0 0 0 0
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	NA NA NA	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX

SP : Thames DDR3 Memory TYPE Set



SP : Mars DDR3 Memory TYPE Set



MLPS

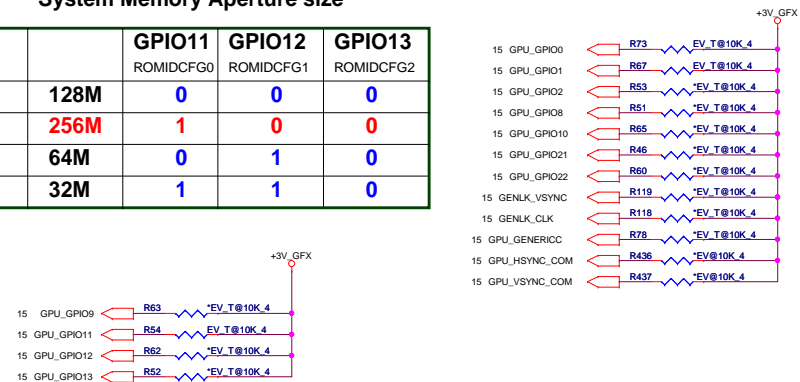
R_pu	R_pd	Bits [3:1]
NC	4.75K	000
8.45K	2K	001
4.53K	2K	010
6.98K	4.99K	011
4.53K	4.99K	100
3.24K	5.62K	101
3.4K	1M	110
4.75K	NC	111

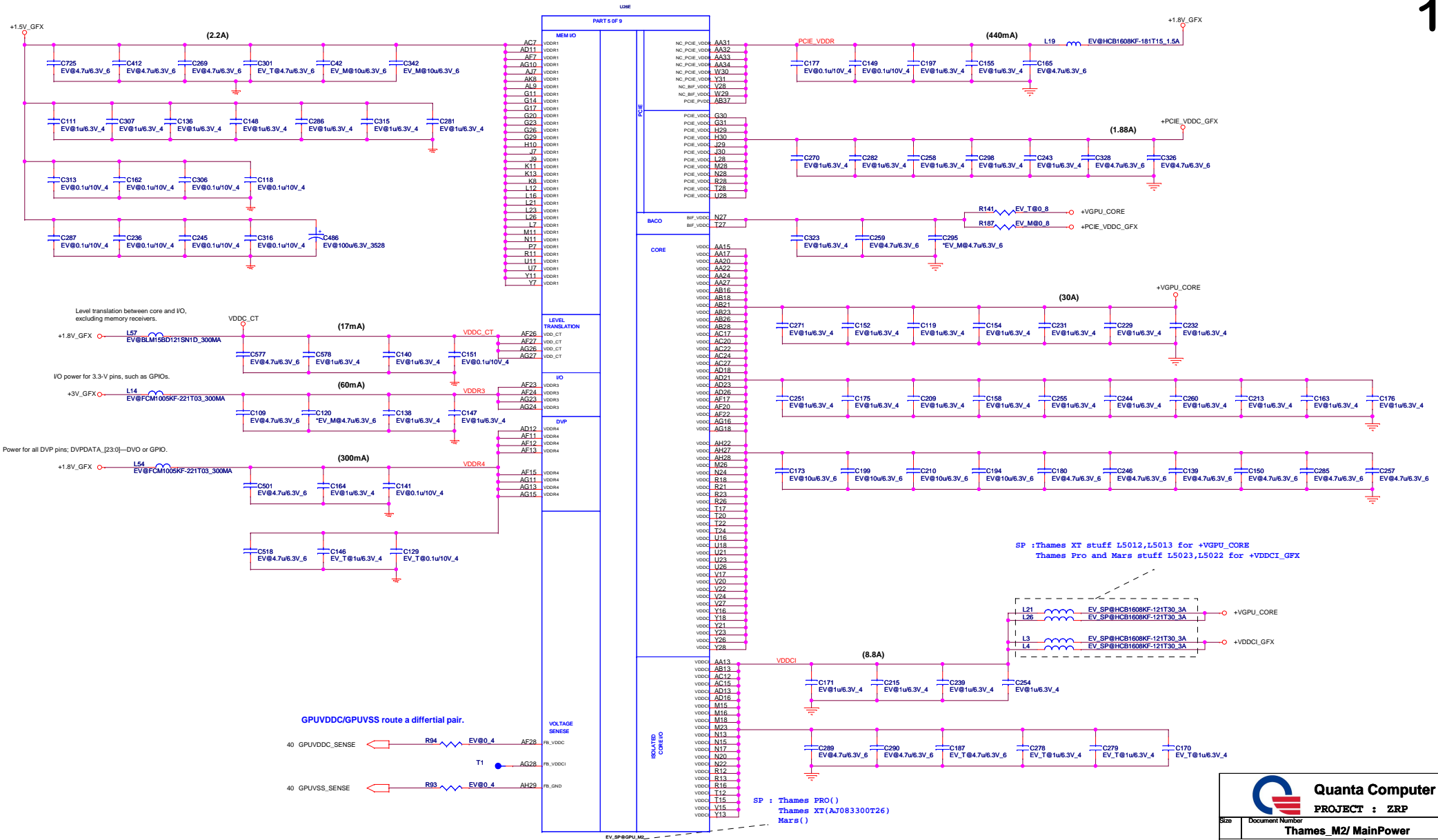
Ra	P/N
2K	CS22002FB19
3.24K	CS23242FB09
3.4K	CS23402FB08
4.53K	CS24532FB08
4.75K	CS24752FB12
4.99K	CS24992FB26
5.62K	CS25622FB18
6.98K	CS26982FB01
8.45K	CS28452FB12
1M	CS51002FB11

Ca	Bits [5:4]	P/N
680nF	00	CH4681K9B00
82nF	01	CH3823K1B00
10nF	10	CH31003KB11
NC	11	

System Memory Aperture size

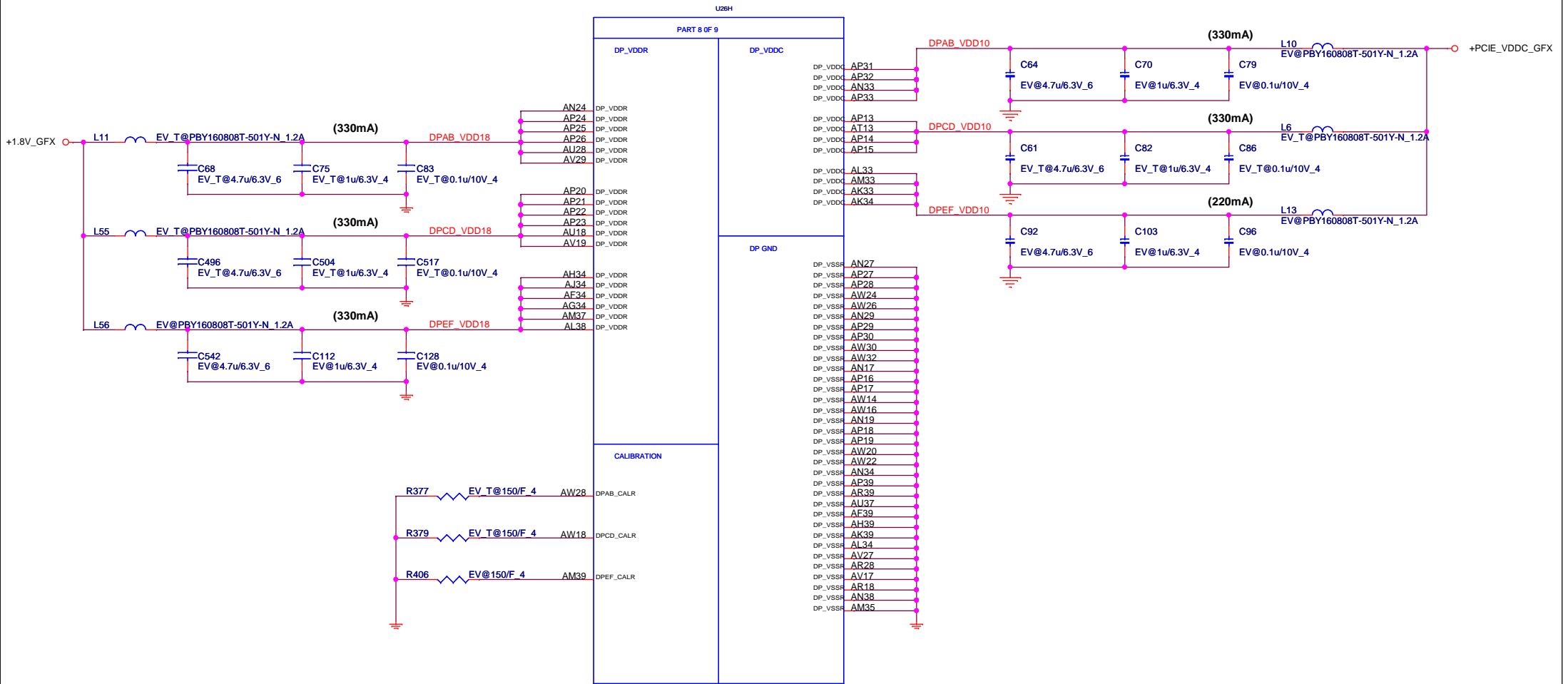
GPIO9 BIOSROM		GPIO11 ROMIDCFG0	GPIO12 ROMIDCFG1	GPIO13 ROMIDCFG2
0	128M	0	0	0
0	256M	1	0	0
0	64M	0	1	0
0	32M	1	1	0






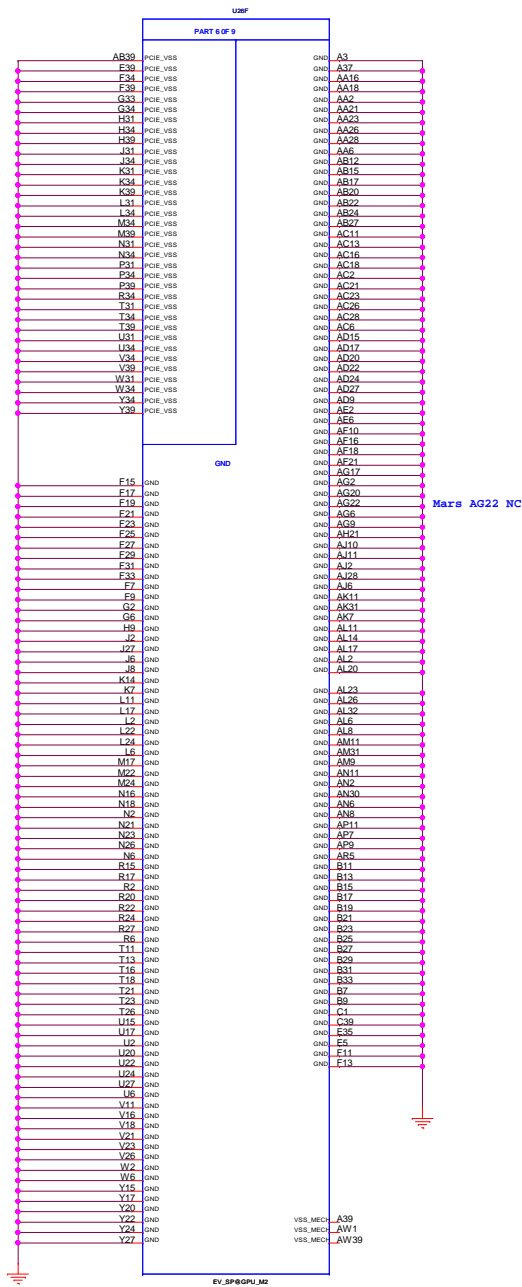
Quanta Computer Inc.
PROJECT : ZRP

Size	Document Number	Rev
	Thames_M2/ MainPower	A1A
Date:	Friday, June 01, 2012	Sheet 18 of 44



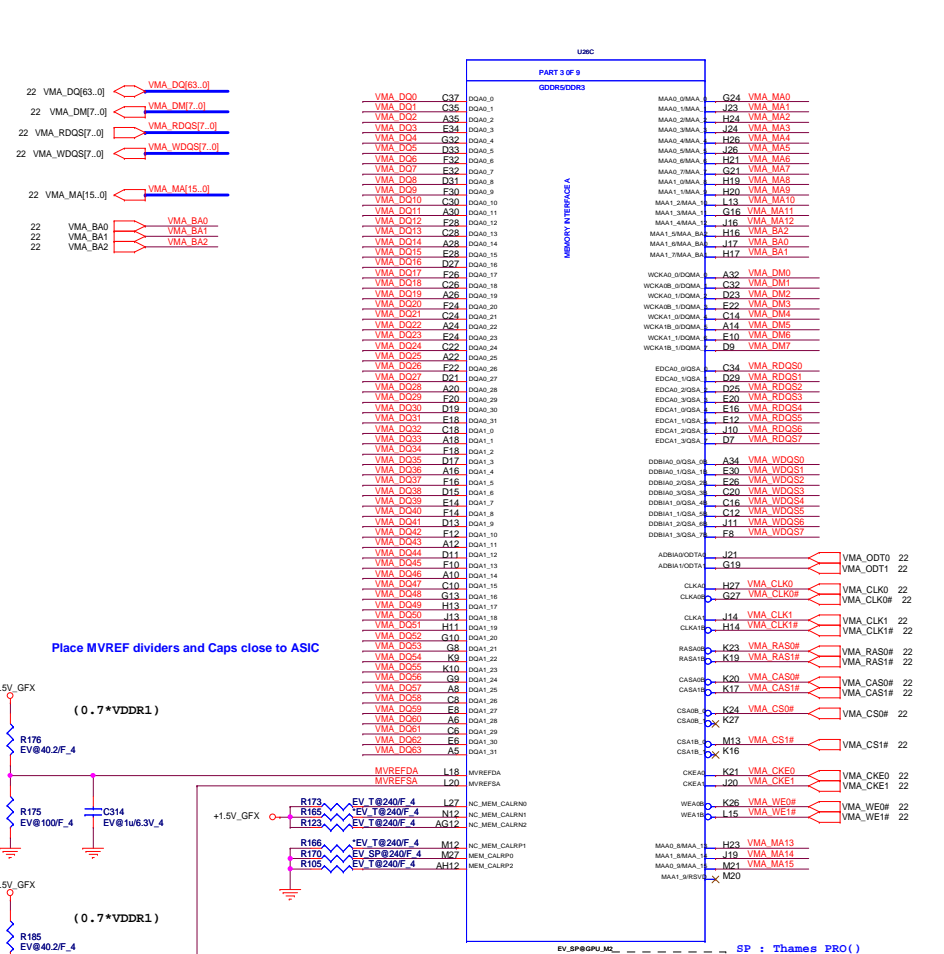
EV_SP@GPU_M2
 SP : Thames PRO()
 Thames XT(AJ083300T26)
 Mars()

 Quanta Computer Inc. PROJECT : ZRP		Rev A1A
Date:	Friday, June 01, 2012	Sheet 19 of 44

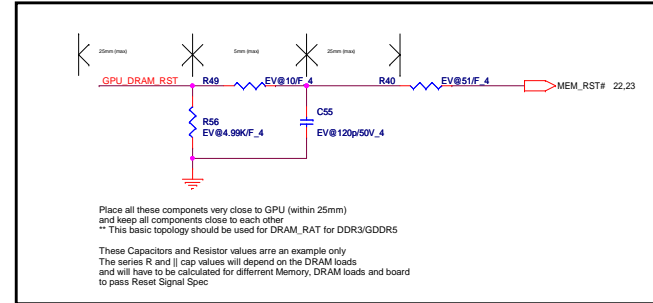
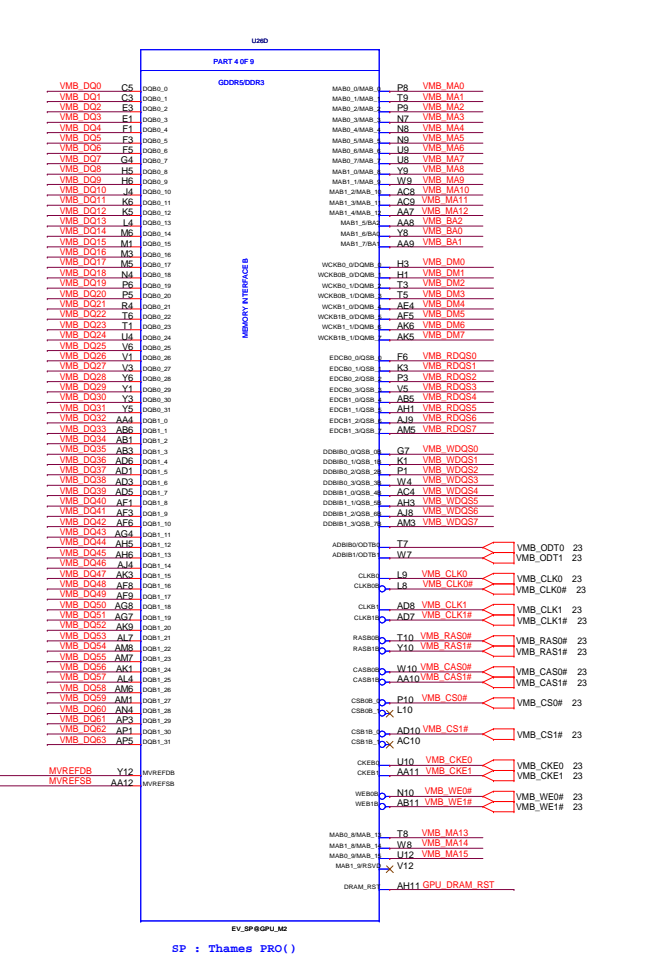
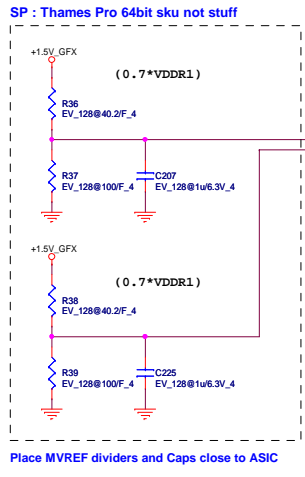


SP : Thames PRO()
Thames XT(AJ083300T26)
Mars ()

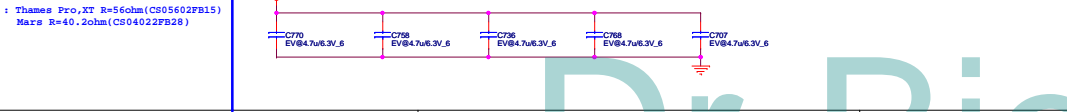
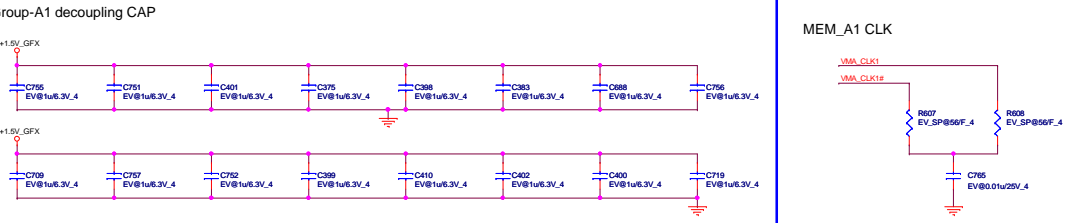
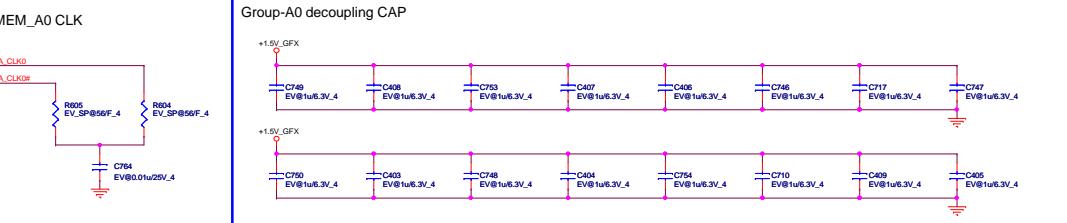
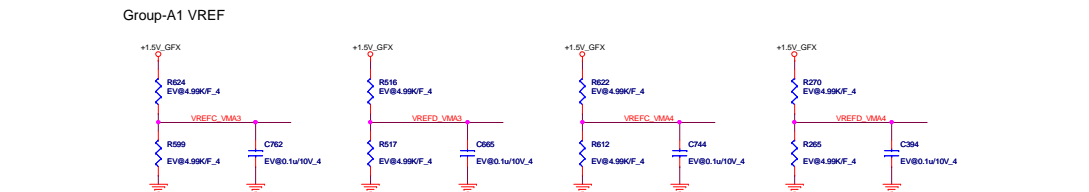
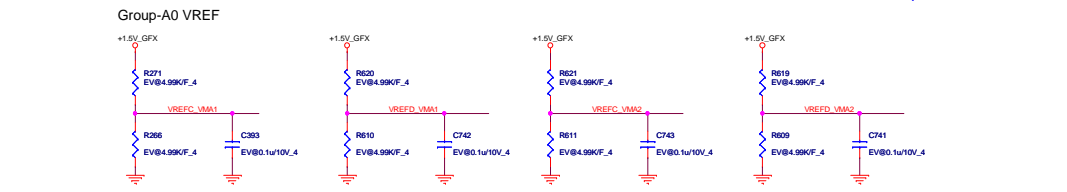
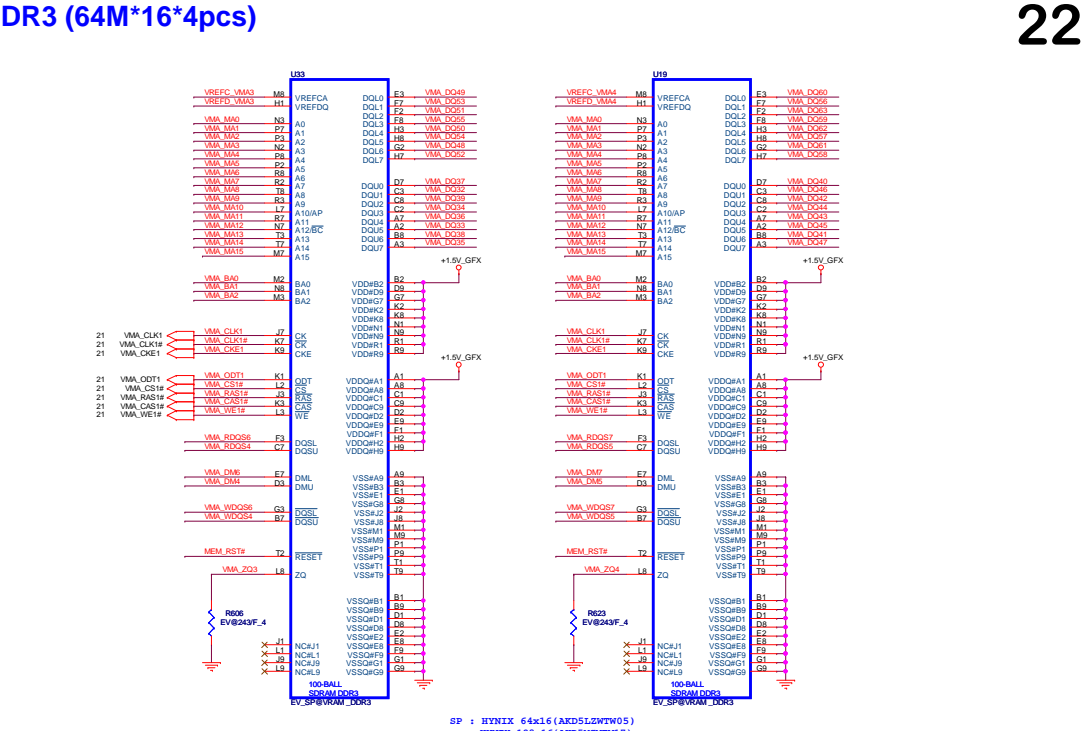
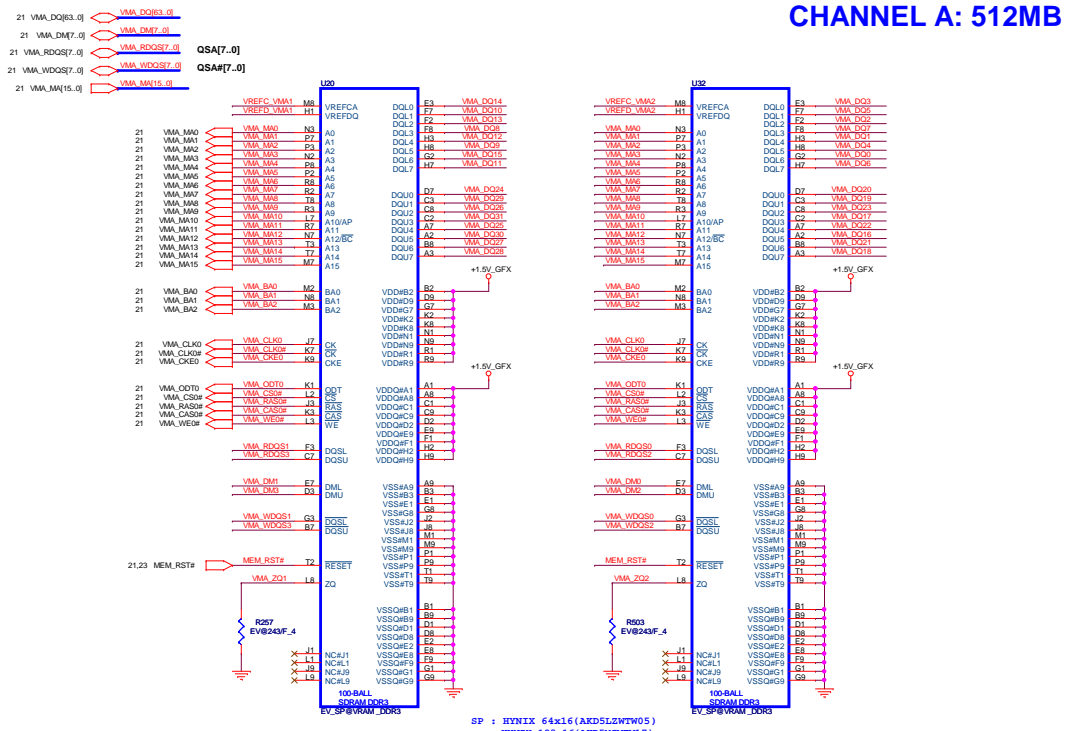
<VGA>



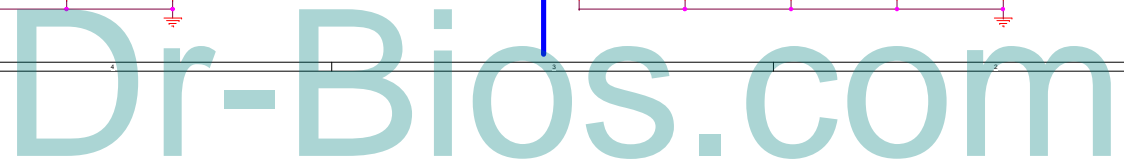
Ball Name	Thames	Mars
MEM_CALRN0	240ohm	X
MEM_CALRN1	X	X
MEM_CALRN2	240ohm	X
MEM_CALRP0	240ohm	120ohm
MEM_CALRP1	X	X
MEM_CALRP2	240ohm	X



CHANNEL A: 512MB DDR3 (64M*16*4pcs)

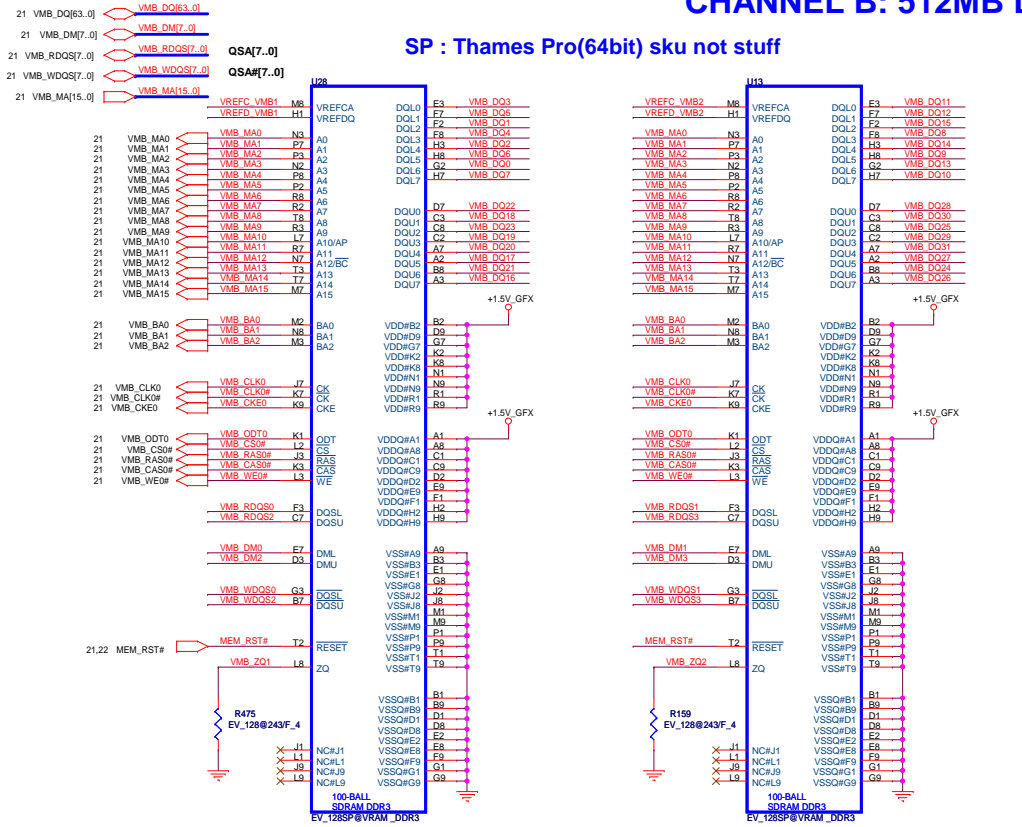


Quanta Computer Inc.
PROJECT : ZRP
Thames_M2/VRAM_A
Date: Friday, June 01, 2012
Sheet: 22 of 44

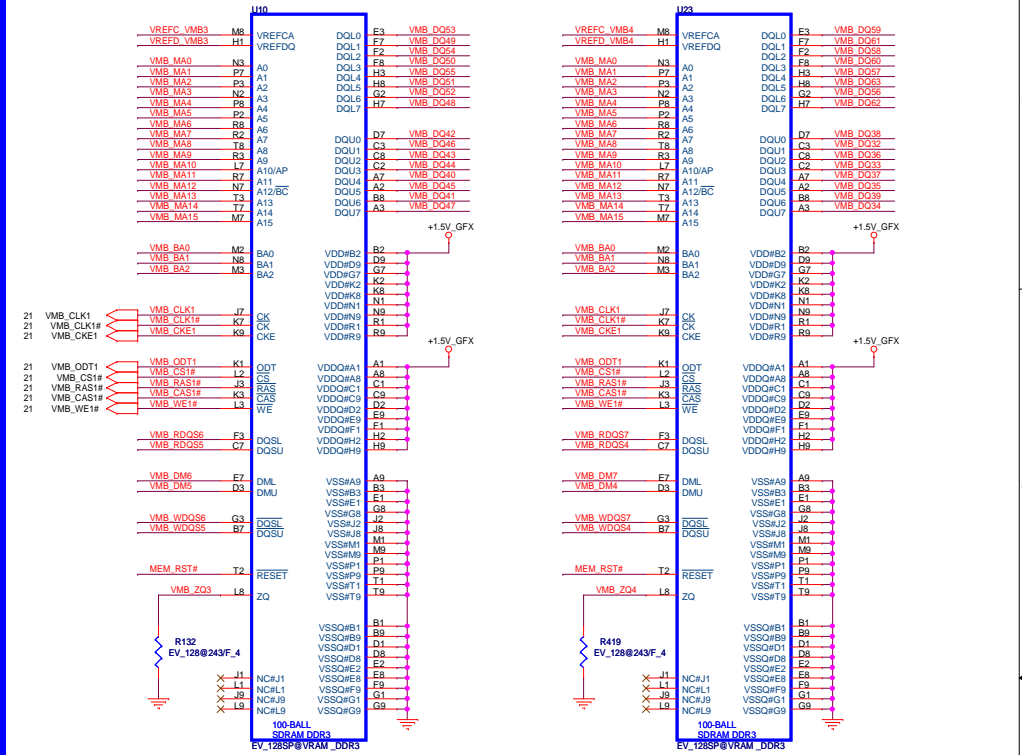


CHANNEL B: 512MB DDR3 (64M*16*4pcs)

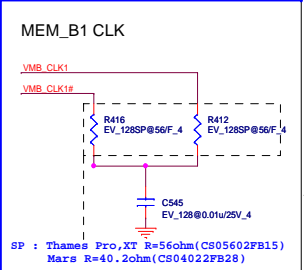
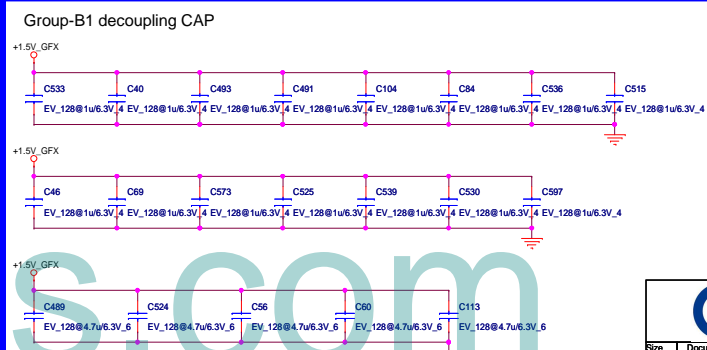
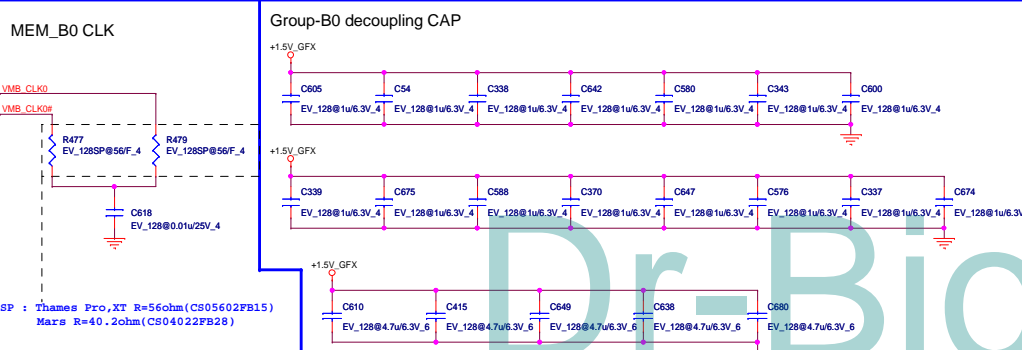
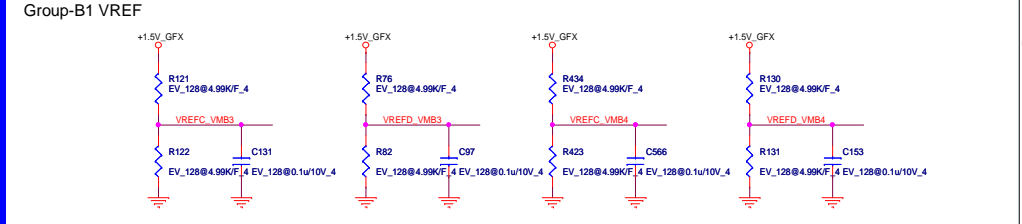
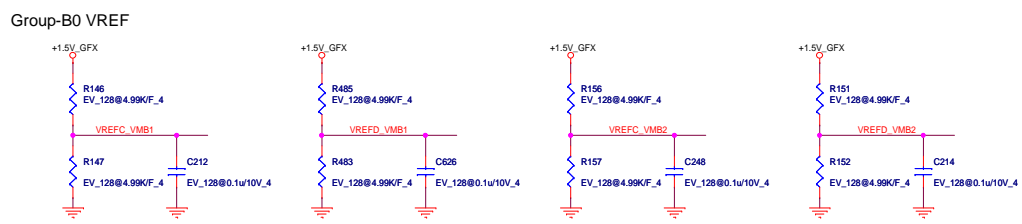
SP : Thames Pro(64bit) sku not stuff



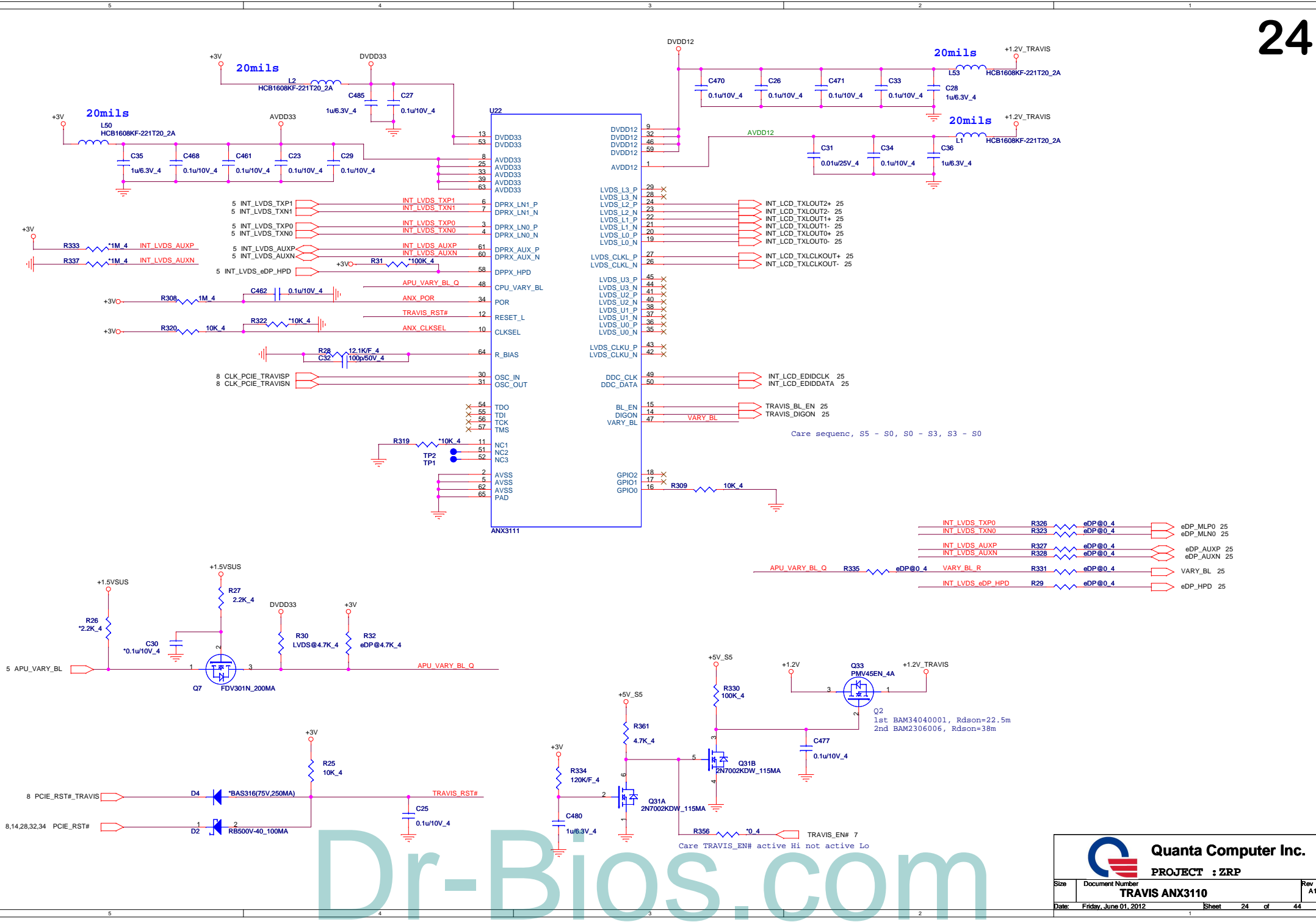
SP : HYNIX 64x16 (AKD5LZWTW05)
HYNIX 128x16 (AKD5MGWTW17)



SP : HYNIX 64x16 (AKD5LZWTW05)
HYNIX 128x16 (AKD5MGWTW17)



SP : Thames Pro,XT R=56ohm(CS05602FB15)
Mars R=40.2ohm(CS04022FB28)

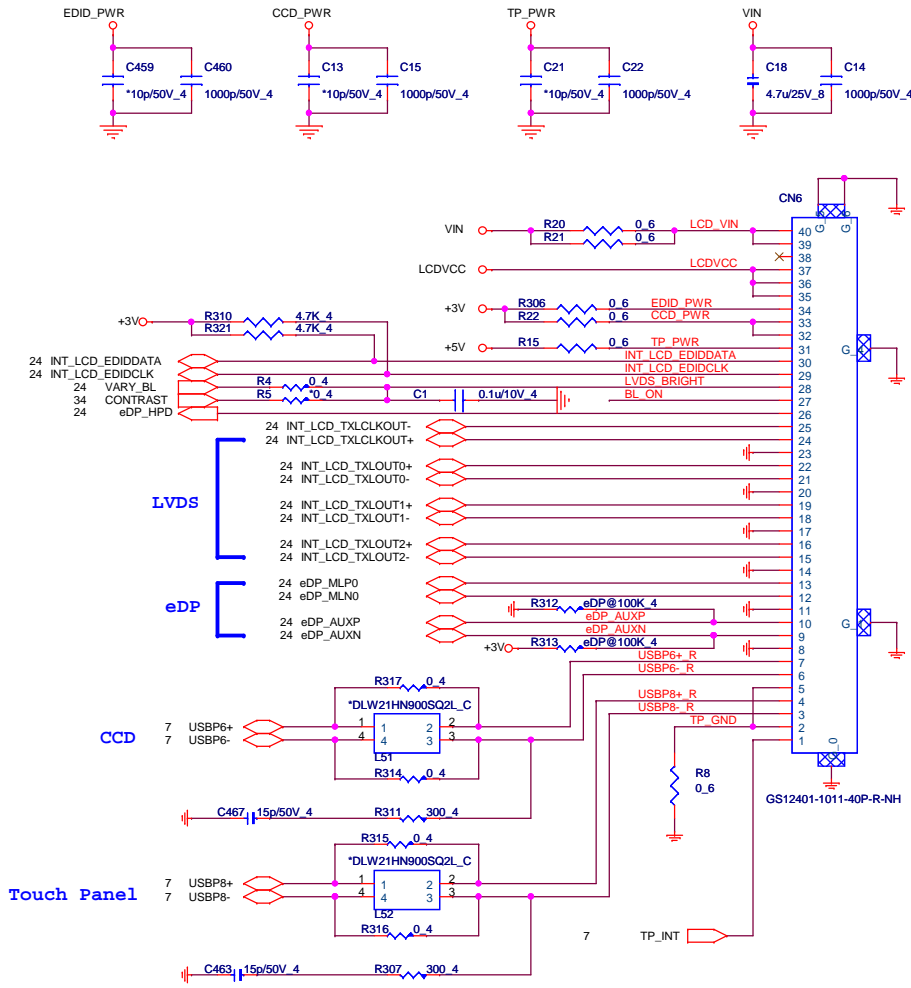


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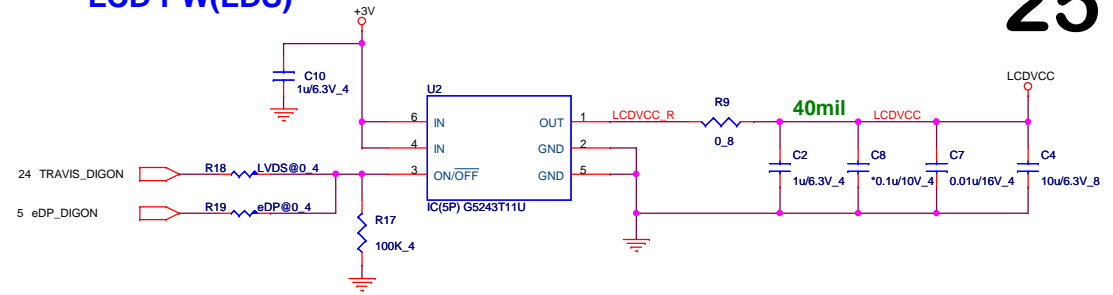
Quanta Computer Inc.
PROJECT : ZRP

Size	Document Number	Rev
	TRAVIS ANX3110	A1A
Date:	Friday, June 01, 2012	Sheet 24 of 44

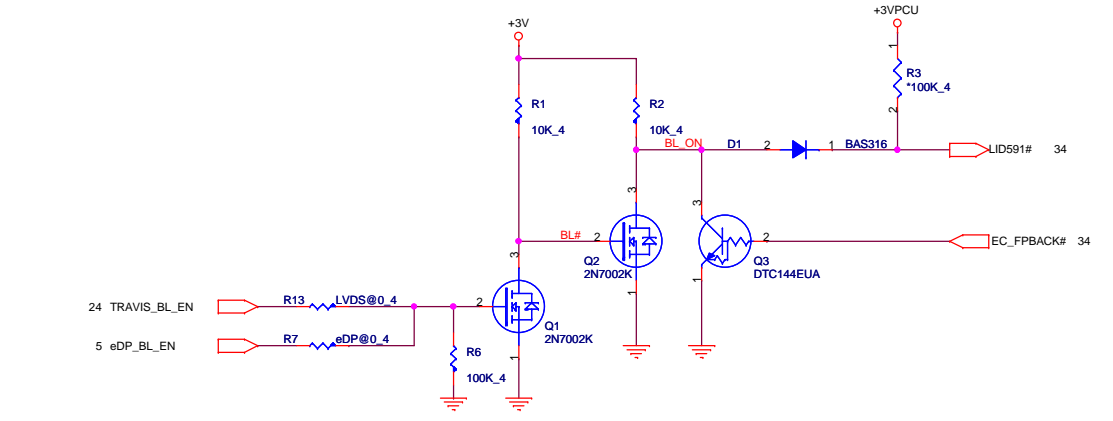
LVDS(LDS)



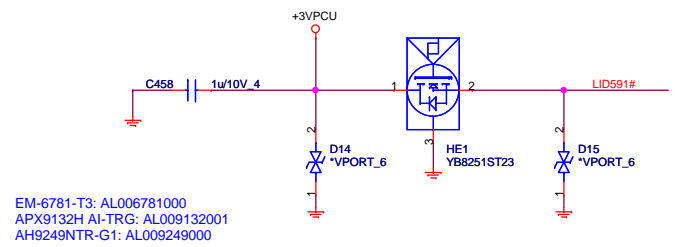
LCD PW(LDS)



Backlight Control(LDS)

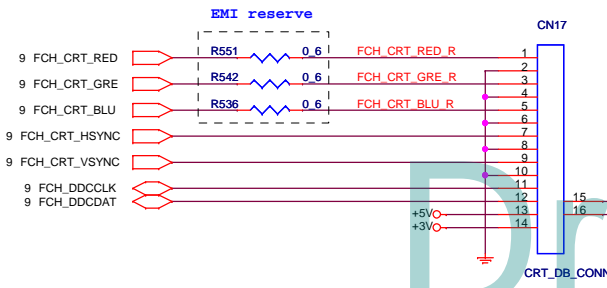


Lid Switch (HSR)

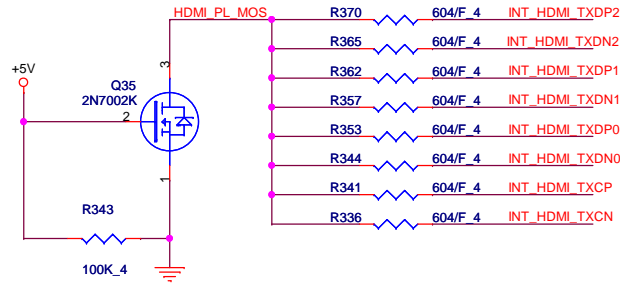
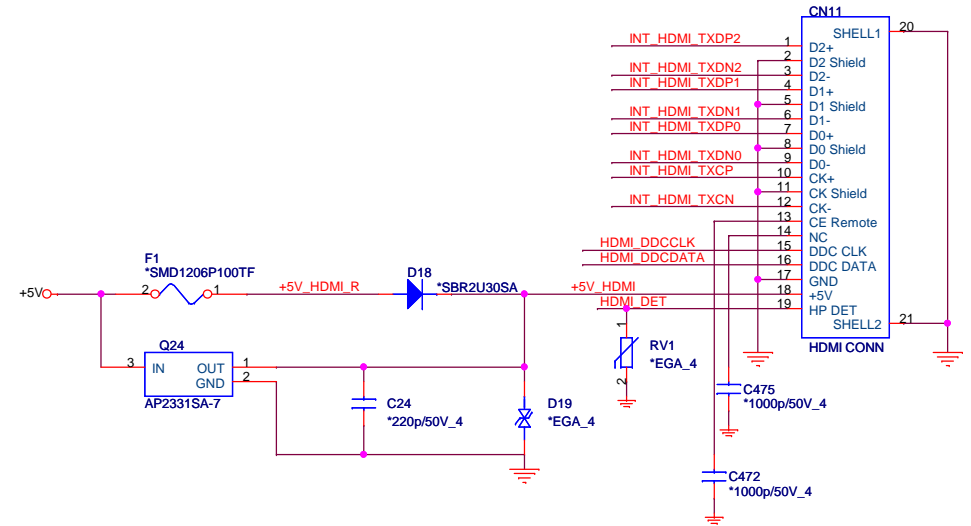
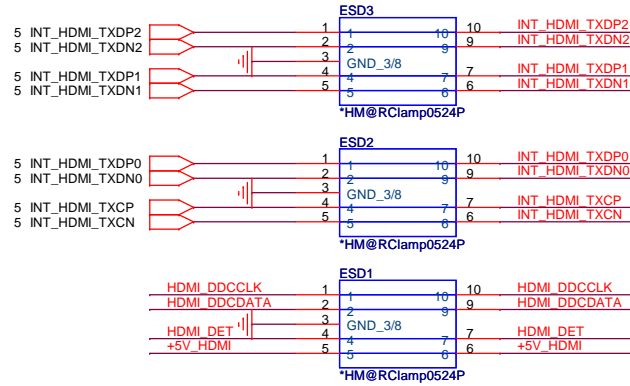


EM-6781-T3: AL006781000
 APX3132H AI-TRG: AL009132001
 AH9249NTR-G1: AL009249000

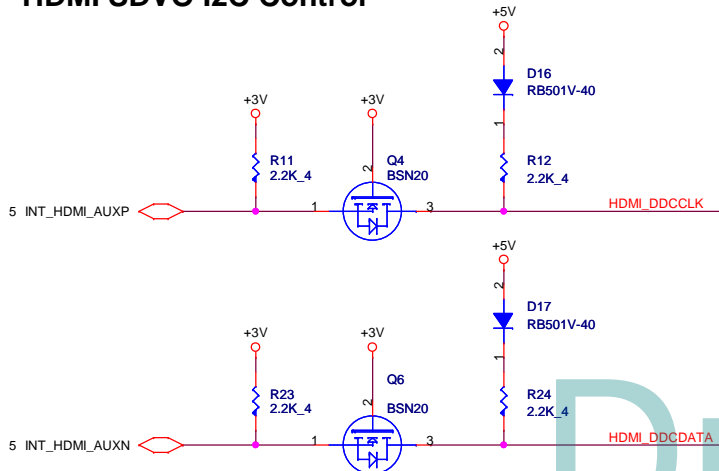
CRT DB



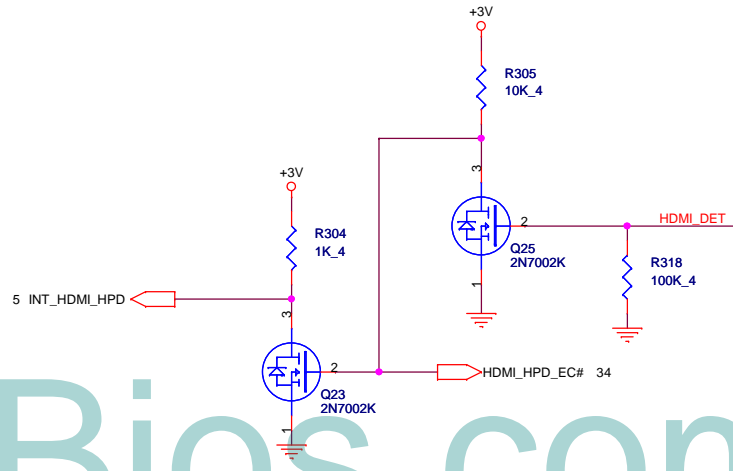
ESD



HDMI SDVO I2C Control

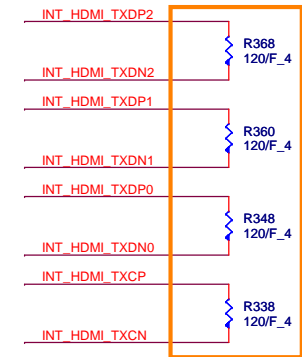


HDMI HPD SENSE

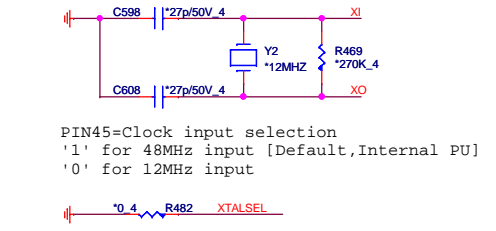
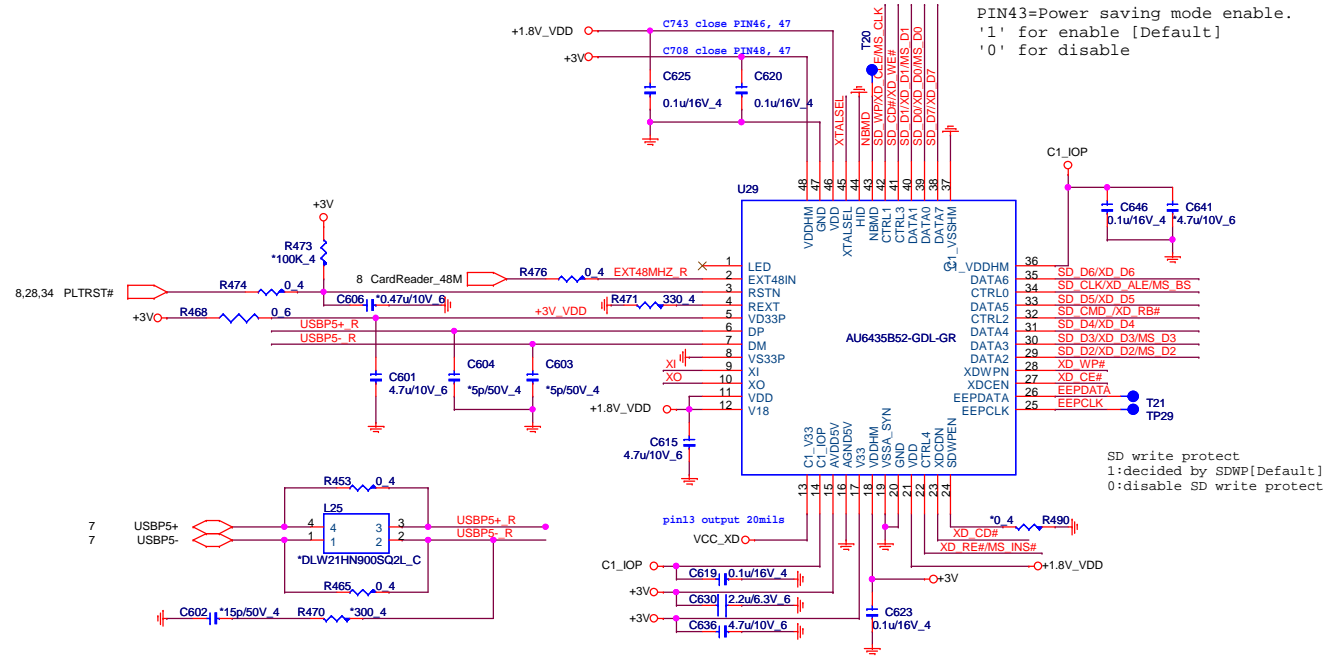


EMI reserve for HDMI(EMC)

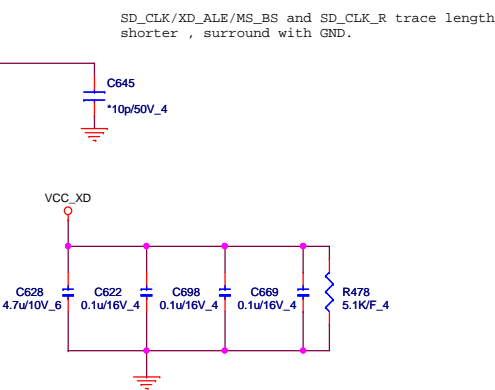
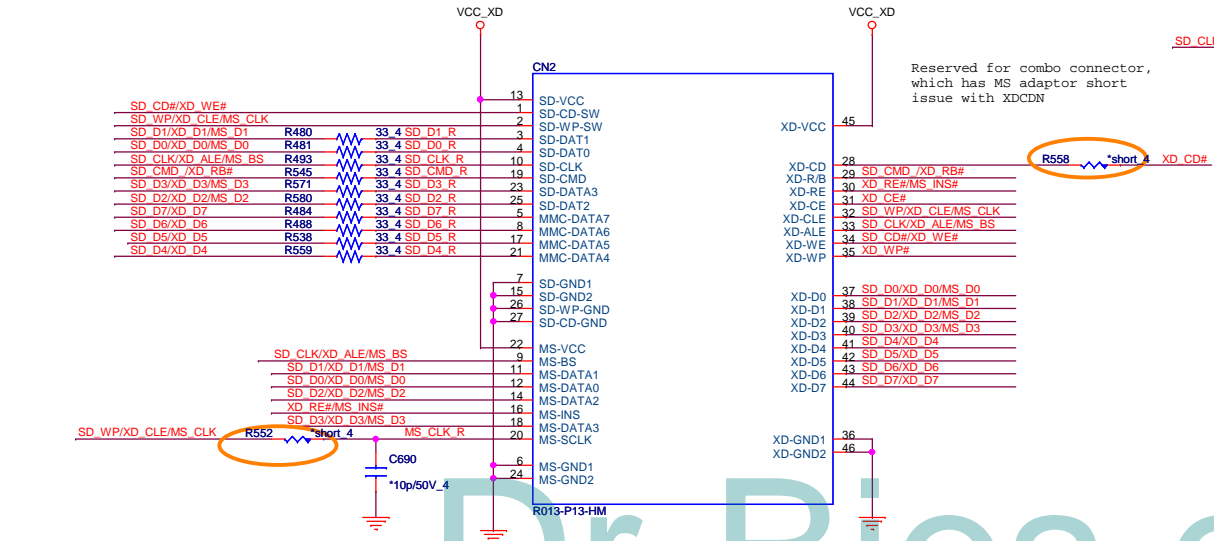
Close connector



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5 IN 1 CARD READER CONN (SD/MMC)



SD_WP/XD_CLE/MS_CLK and MS_CLK_R trace length shorter , surround with GND.

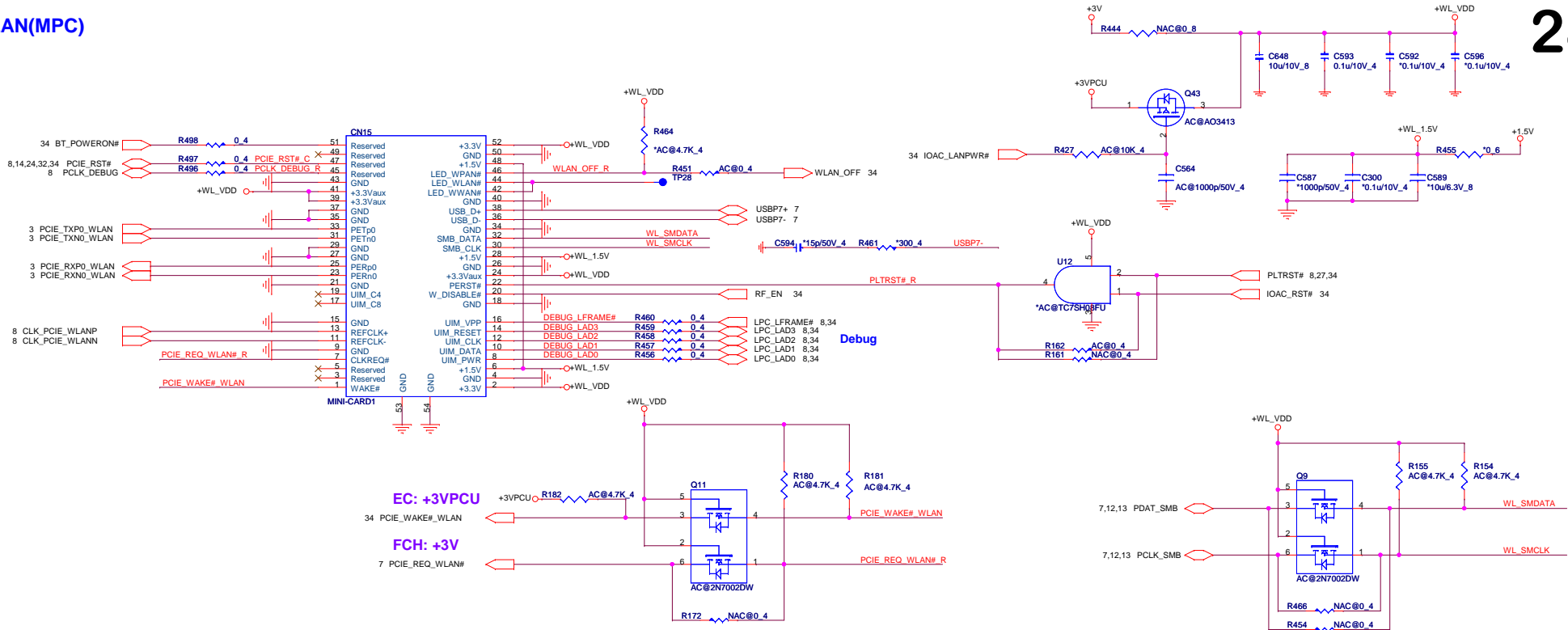


Quanta Computer Inc.
PROJECT : ZRP

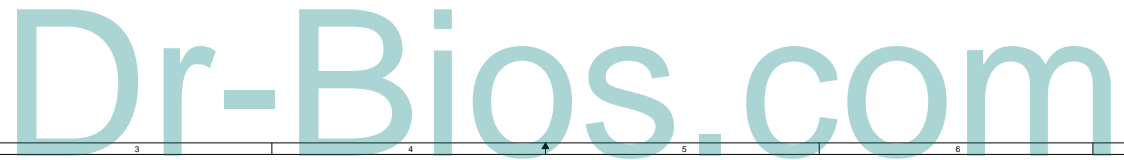
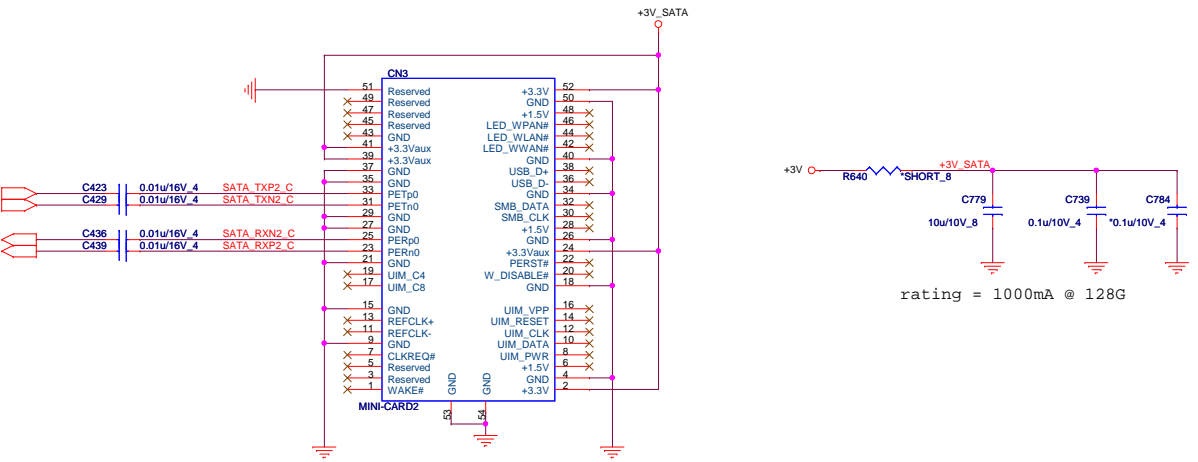
Size	Document Number	Rev
	CardReader (5 IN 1)	A1A
Date:	Friday, June 01 2012	Sheet 27 of 44

MINI-CARD WLAN(MPC)

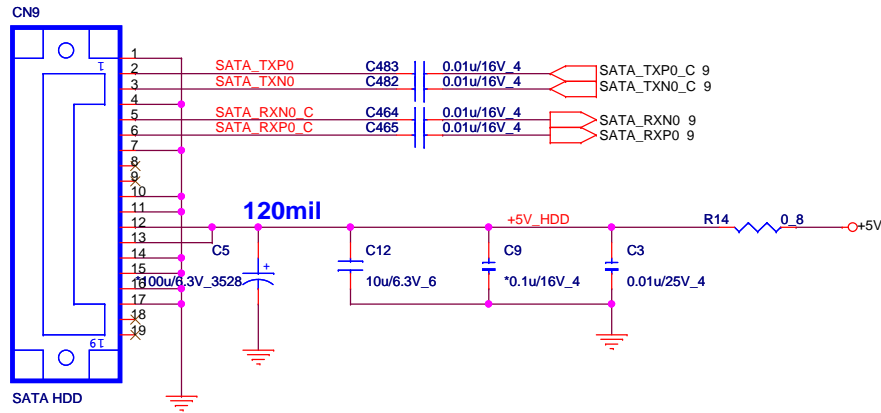
+3.3V: 1000mA
+3.3Vaux: 330mA
+1.5V: 500mA



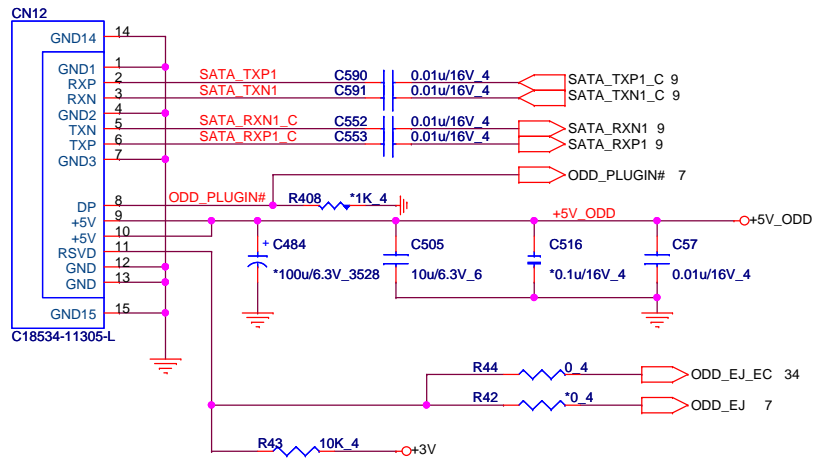
MINI-CARD SSD



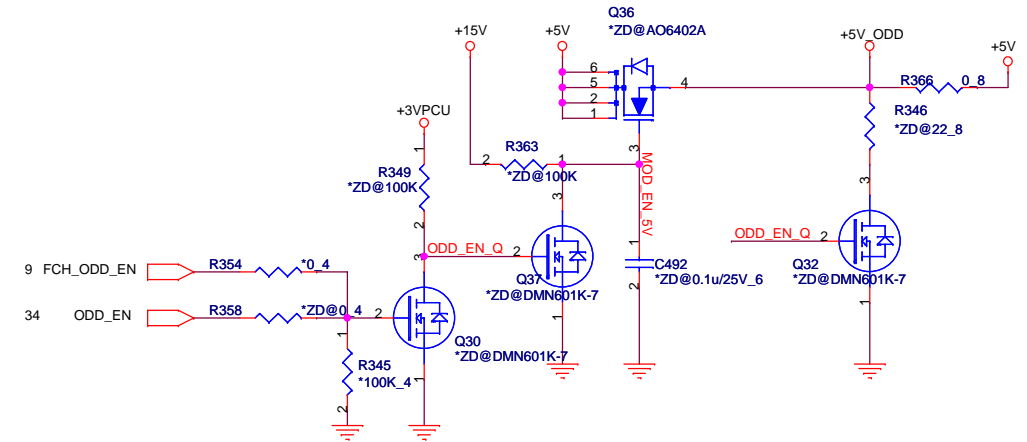
SATA HDD



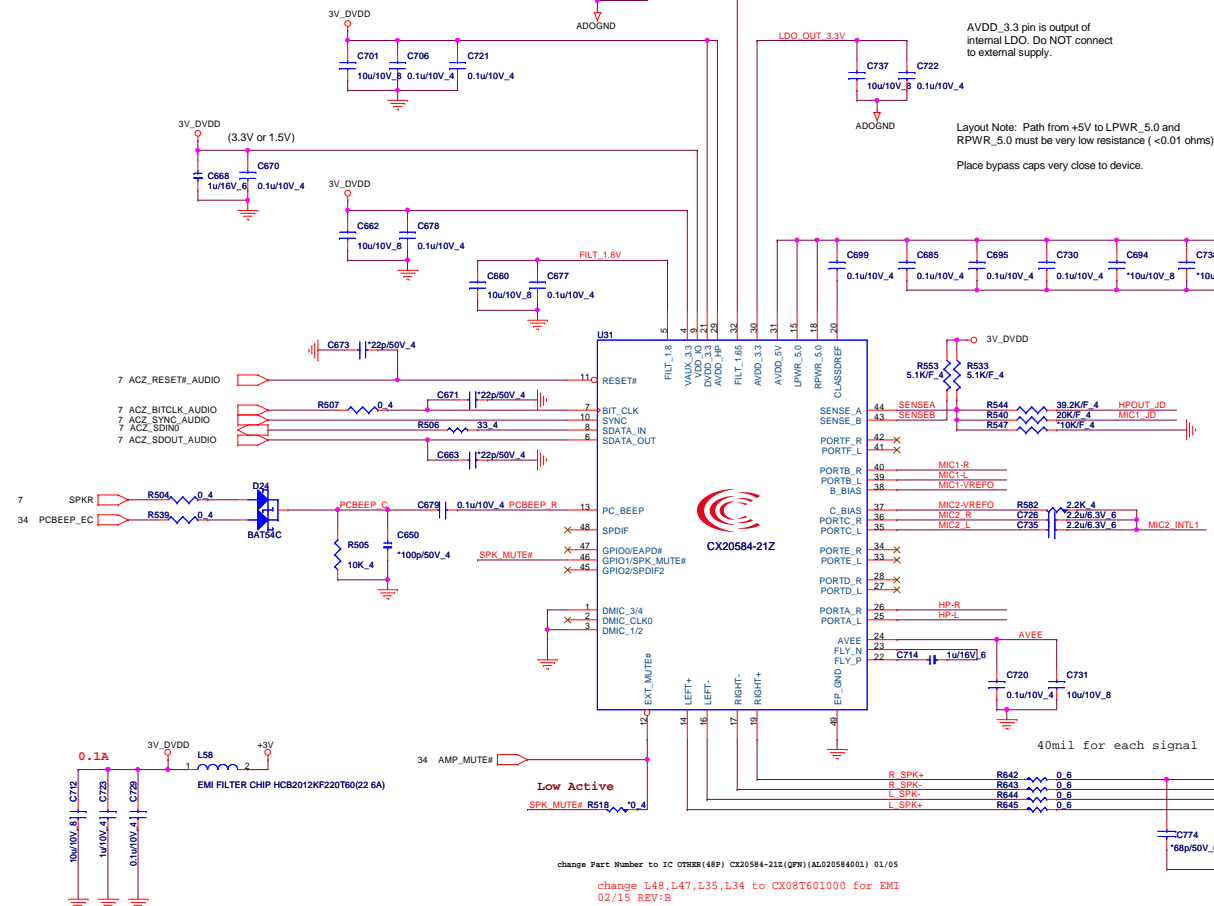
SATA ODD



Zero Power (ODD)



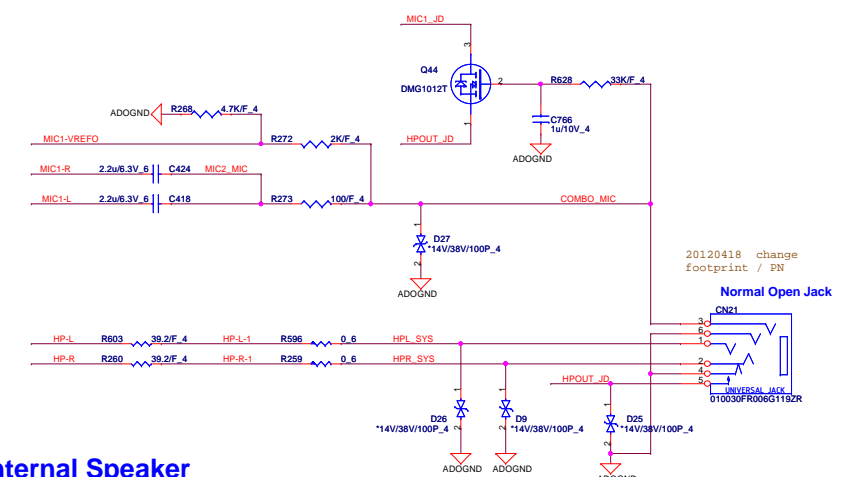
AUDIO CODEC



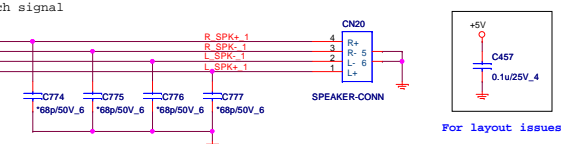
Port Configuration

- Notes:
- Port A: Headphone jack (jack shared with S/PDIF)
 - Port B: Internal MIC (mono or stereo)
 - Port C: Microphone/LI/LO jack
 - Port D: Line Out jack (Optional)
 - Port E: Line In jack (Optional)
 - Port F: Not used.
 - Port G: Internal stereo speakers
 - Port J: Internal stereo digital mic (Optional)
 - Port H: S/PDIF (jack shared with headphone)

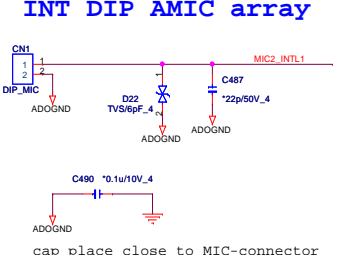
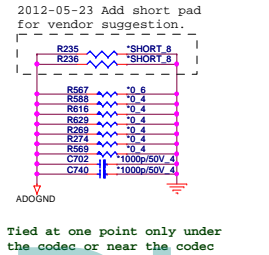
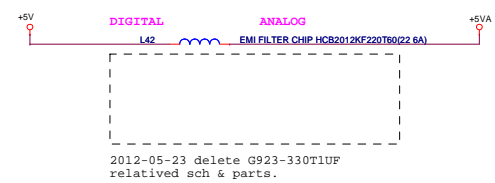
HEADPHONE/Mic combo



Internal Speaker



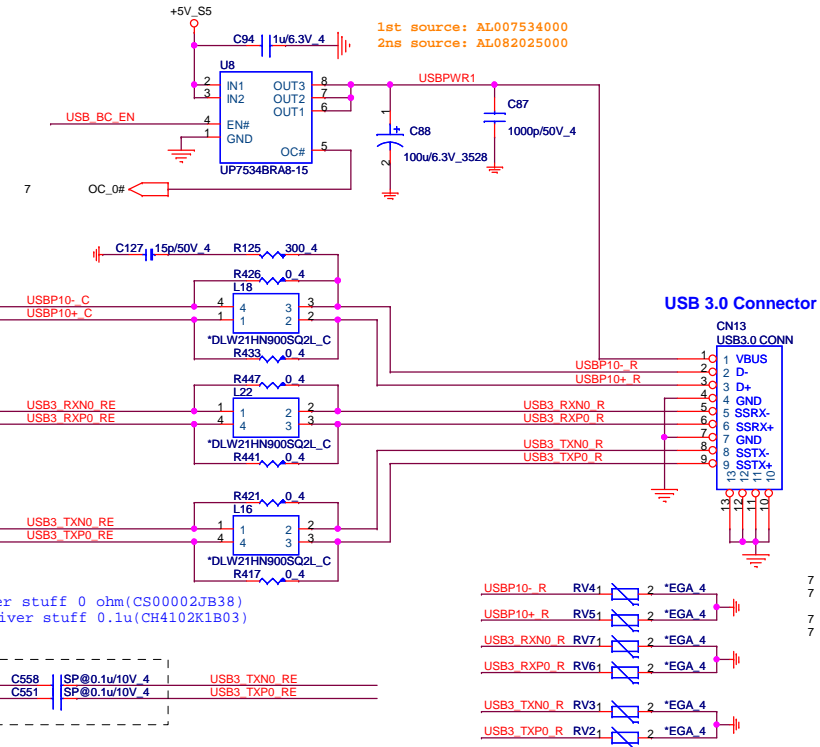
Power (ADO)



- The VDD_IO and VAUX_3.3 pins should be connected to same power supply domain as HDA bus controller so that the HDA controller and codec bus interface will power-up at the same time. This will avoid bus leakage issues if using HDA controller with bus pull-up strap options. See other FET option on this page if these supplies are not on same domain as HDA controller.
- To support Wake-on-Jack, the codec VAUX_3.3 pin must be powered from a Standby supply.
- C309, C310, C311 are optional. Do not install unless needed for EMI/SI.

Quanta Computer Inc.
 PROJECT : ZRP
 Size Document Number
CONEXANT 20584
 Date: Friday, June 01, 2012 Sheet 30 of 44 Rev 1A

USB3.0/2.0

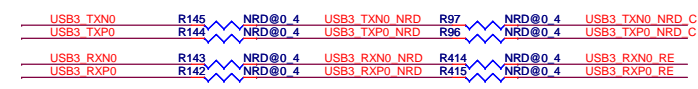
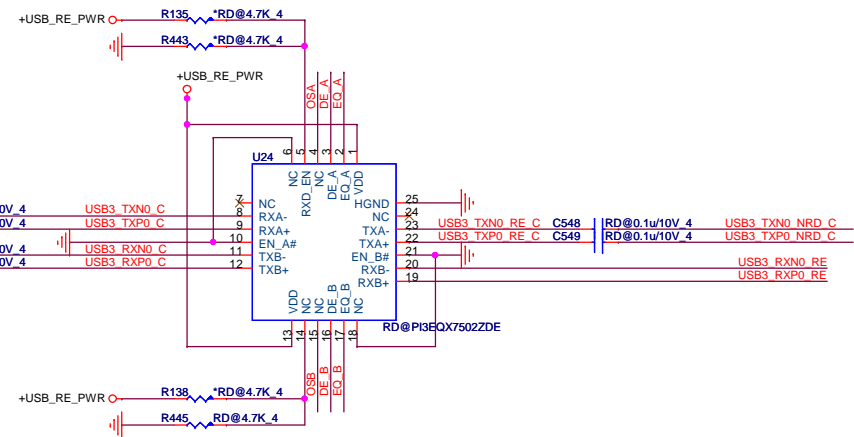
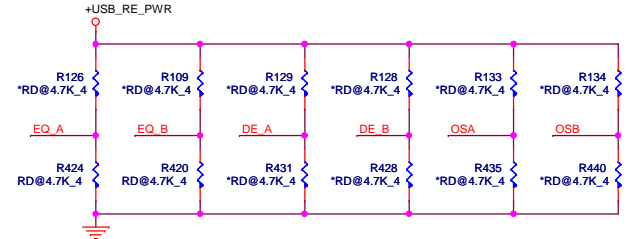
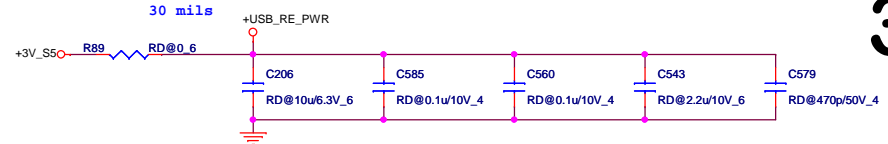
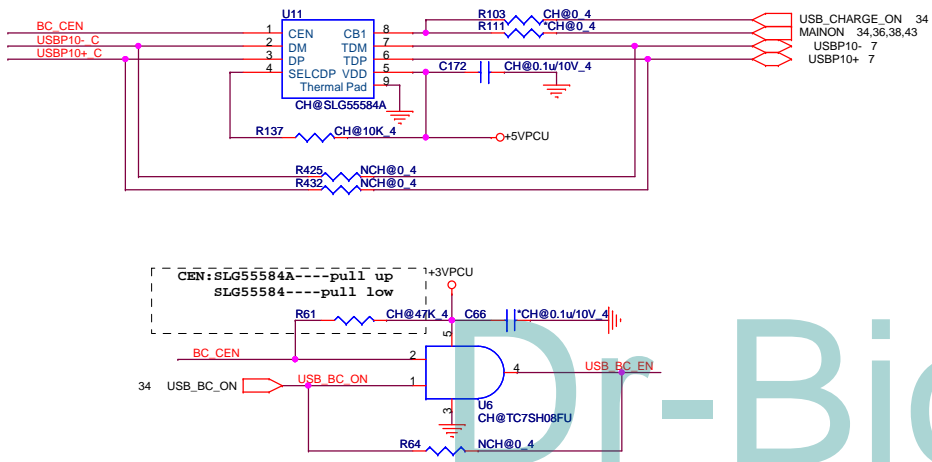


SP : 1. Re-Driver stuff 0 ohm(CS00002JB38)
 2. No Re-Driver stuff 0.1u(CH4102K1B03)

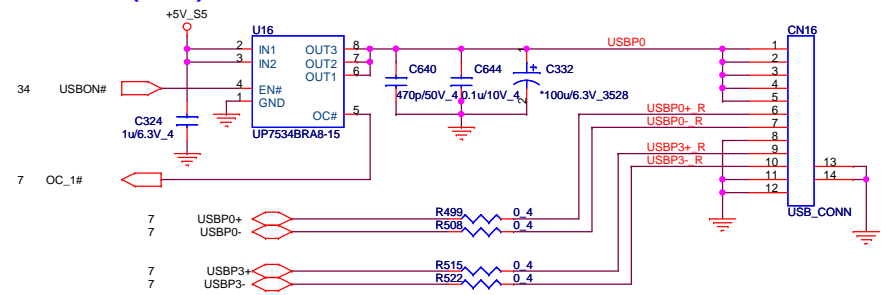


USB Charger to 3.0

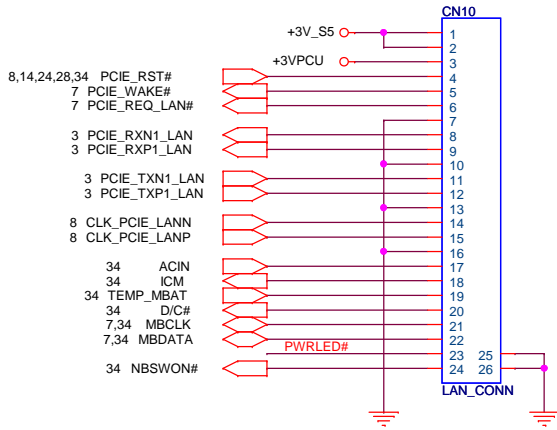
CB	SELCDP	Function
0	X	DCP autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP only
1	1	S0 charging with CDP or SDP only (depending on external device)



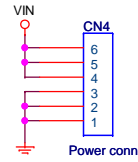
EXT. USB(USB)



LAN& Charger DB

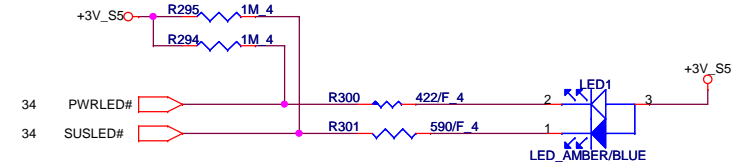


POWER M/B (DCD)

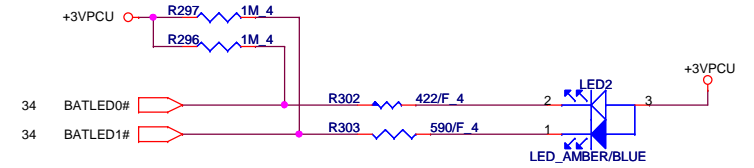


LED(UIF)

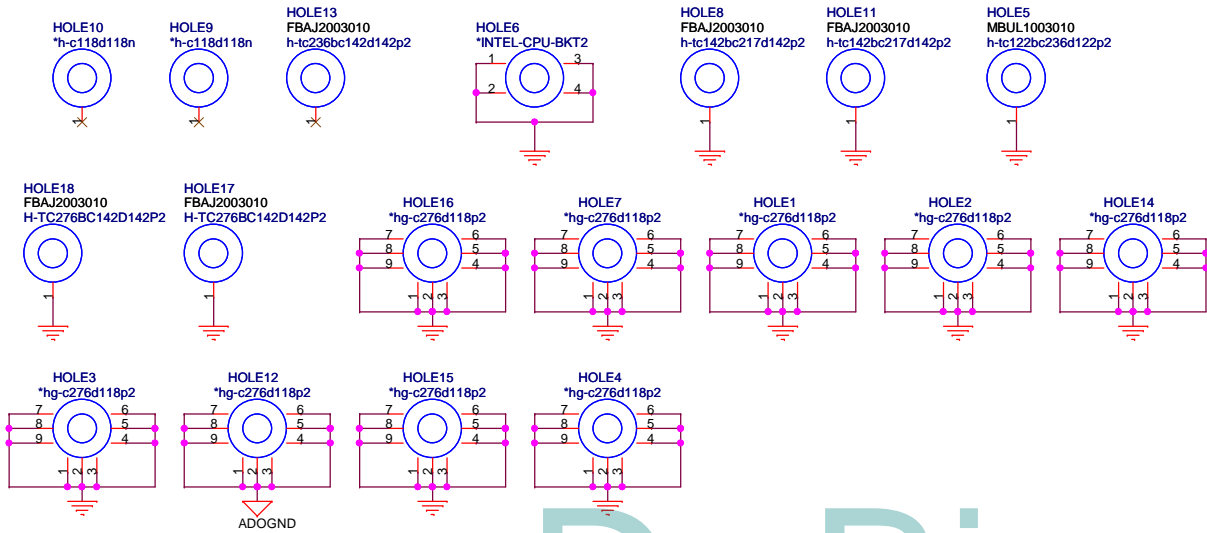
Power



Battery



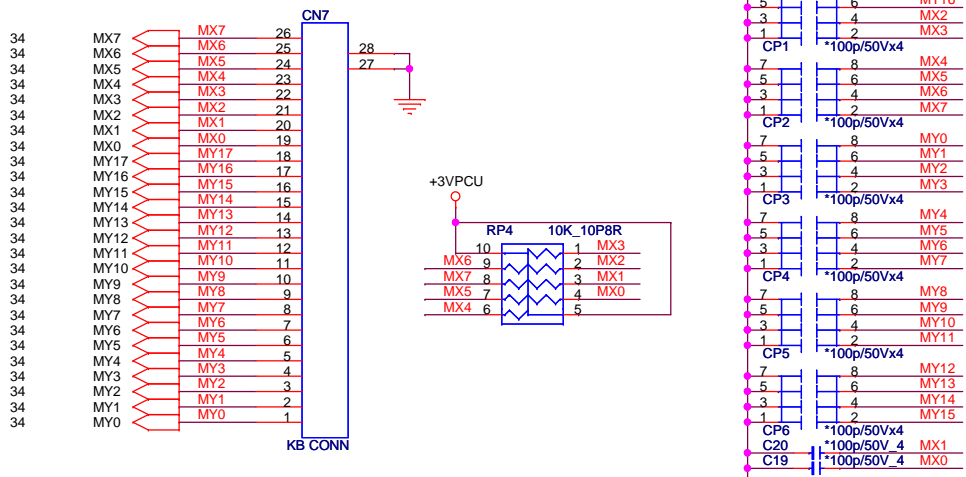
HOLE(OTH)



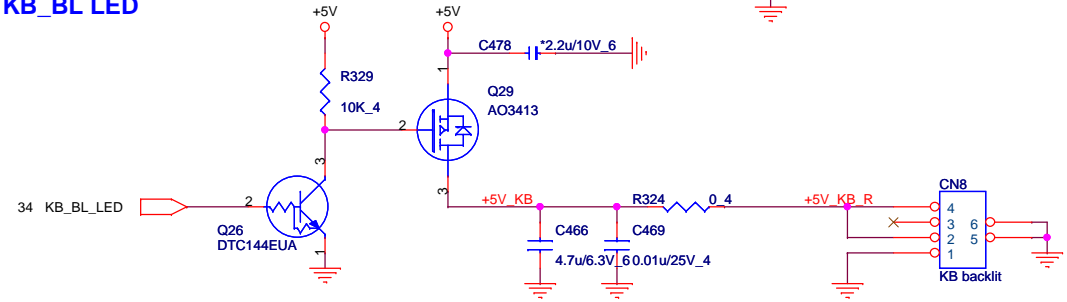
EE RETURN-PATH CAPACITORS(EMC)

		Quanta Computer Inc. PROJECT : ZRP	
		Size Document Number LAN DB/ LED/ EMI/ Hole	Rev A1A
Date: Friday, June 01, 2012		Sheet 32 of 44	

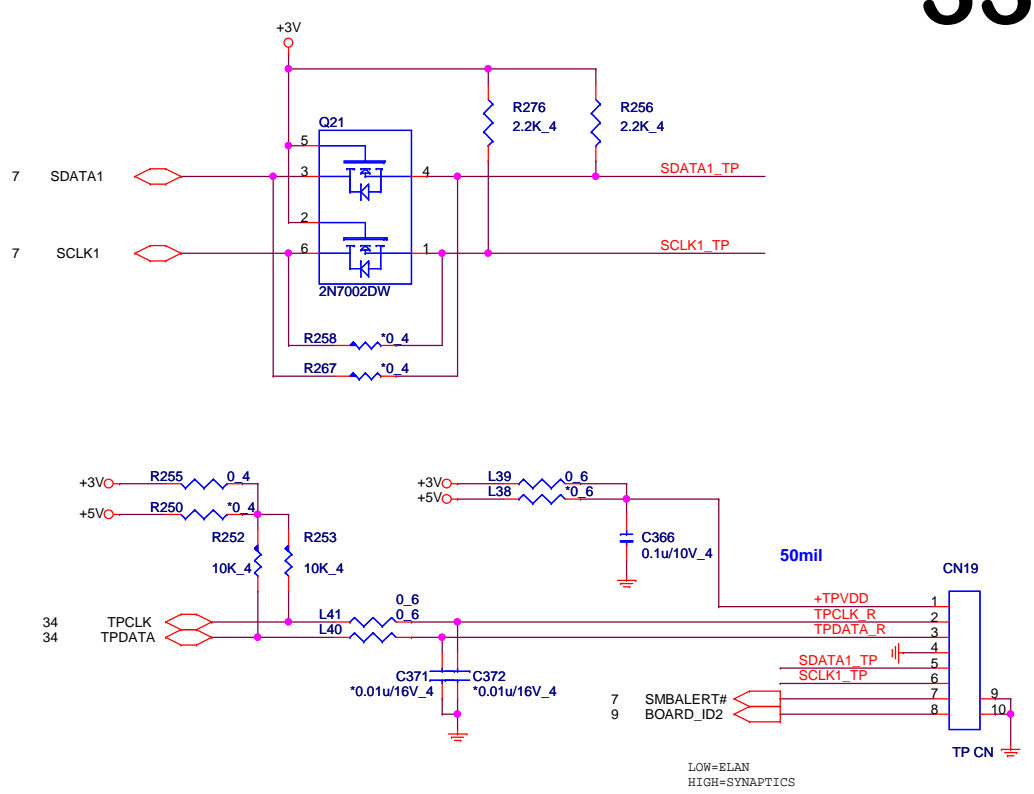
K/B(KBC)



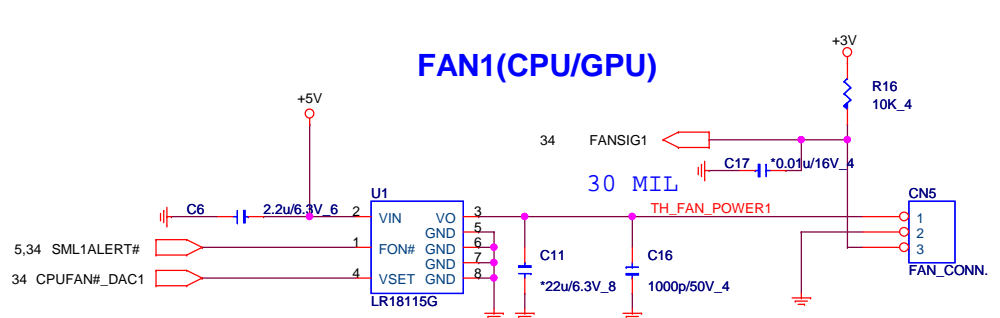
KB_BL LED



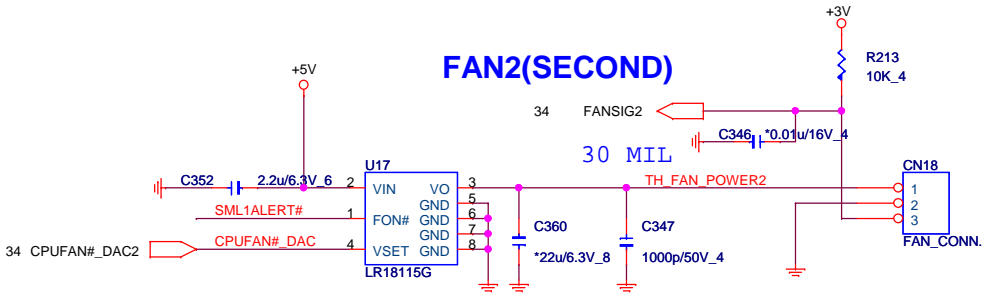
TOUCHPAD BOARD CONN(TPD)



CPU FAN(THM)



FAN2(SECOND)

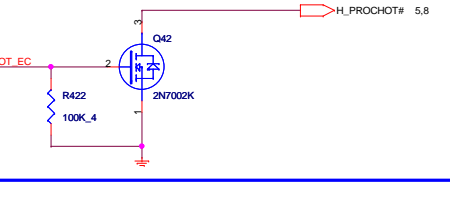
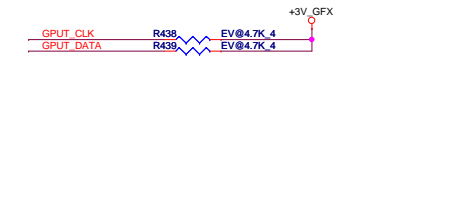
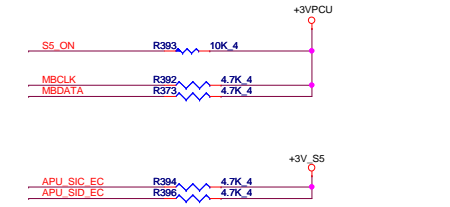


Quanta Computer Inc.
PROJECT : ZRP

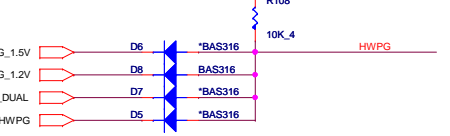
Size	Document Number	Rev
	KB/TP/FAN	A1A
Date:	Friday, June 01, 2012	Sheet 33 of 44

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SM BUS PU(KBC)



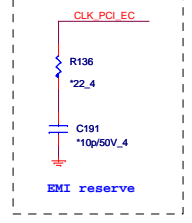
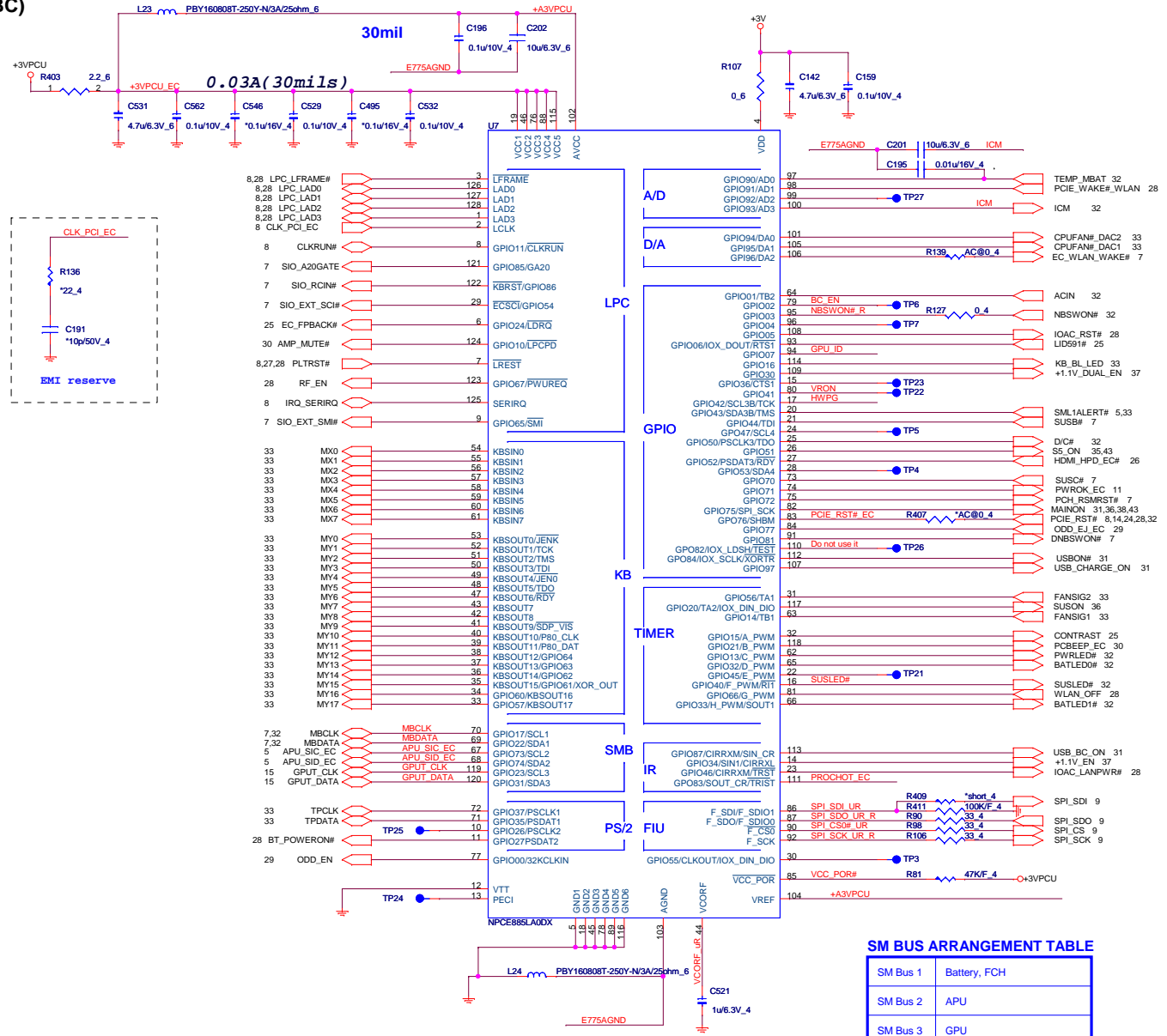
HWPG(KBC)



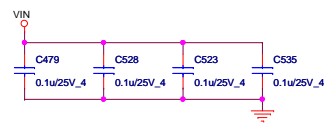
SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery, FCH
SM Bus 2	APU
SM Bus 3	GPU

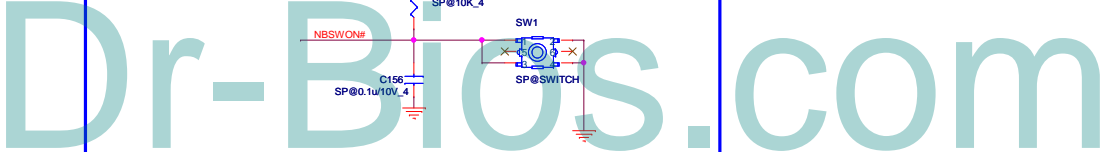
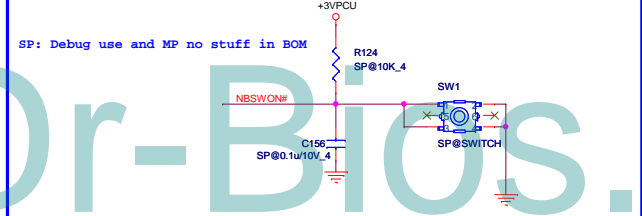
EC(KBC)



Placement for EC of VIN power plan



POWER-ON SWITCH (KBC)

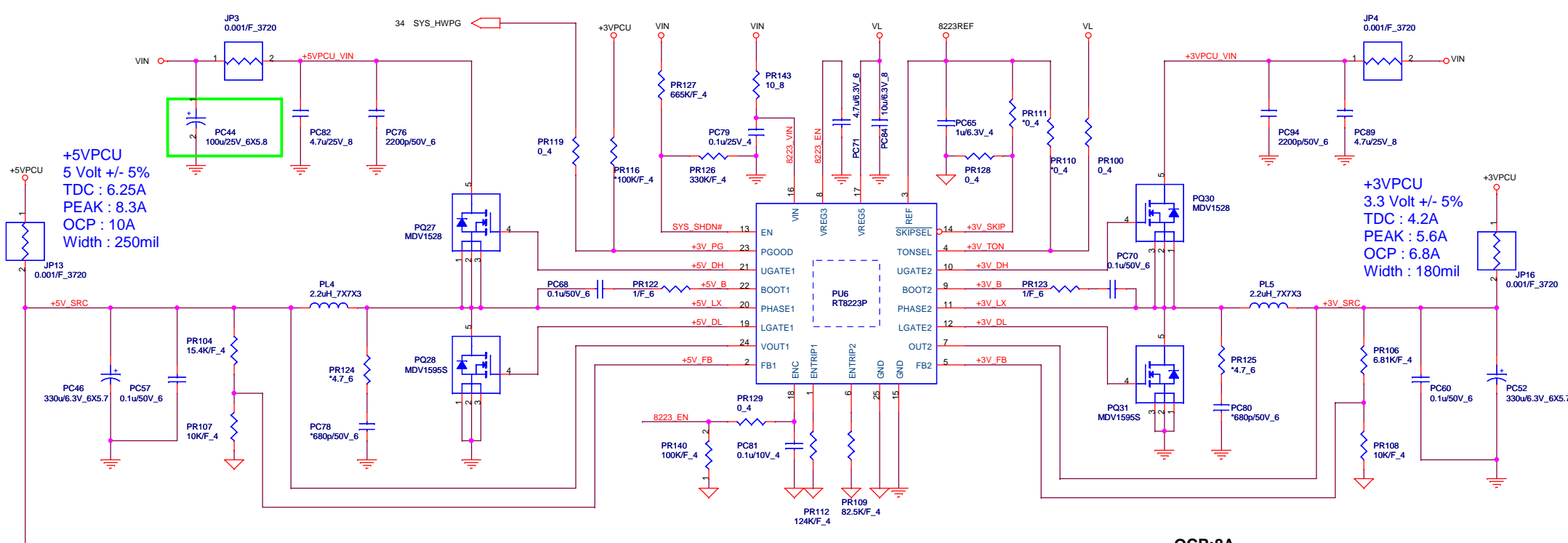


Quanta Computer Inc.
PROJECT : ZRP
NPCE885/FLASH

Size	Document Number	Rev
		ATA

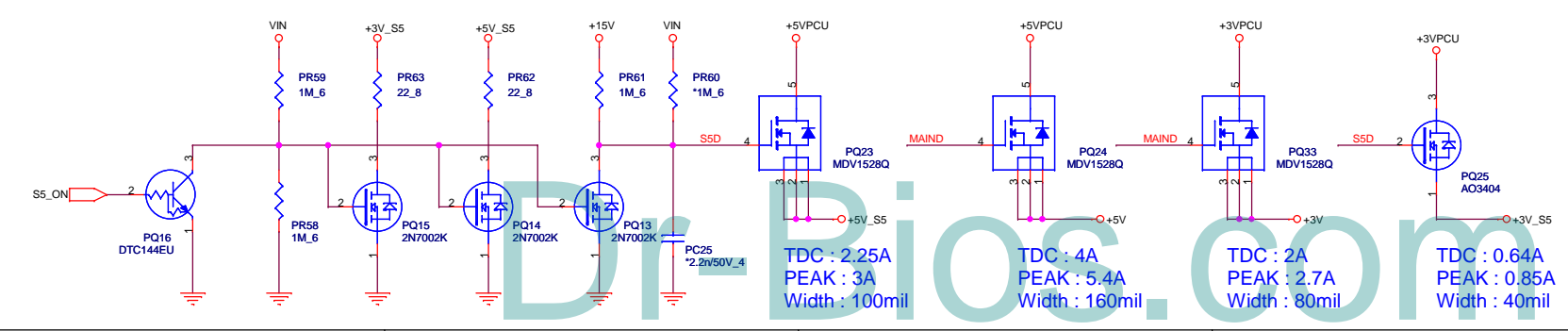
Date: Friday, June 01, 2012 Sheet 34 of 44

Ven=7.23V



OCP:10A
 $L(\text{ripple current}) = (9-5) \cdot 5 / (2.2 \mu\text{H} \cdot 0.4\text{M}^2 \cdot 9) = 2.525\text{A}$
 $I_{\text{ocp}} = 10 - (2.525/2) = 8.74\text{A}$
 $V_{\text{th}} = 8.74\text{A} \cdot 14\text{m}\Omega = 122.32\text{mV}$
 $R(\text{Ilim}) = (122.3\text{mV} \cdot 10) / 10\mu\text{A} \sim 122.3\text{K}$

OCP:8A
 $L(\text{ripple current}) = (9-3.3) \cdot 3.3 / (2.2 \mu\text{H} \cdot 0.5\text{M}^2 \cdot 9) \sim 1.9\text{A}$
 $I_{\text{ocp}} = 6.8 - (1.9/2) = 5.85\text{A}$
 $V_{\text{th}} = 5.85\text{A} \cdot 14\text{m}\Omega = 81.9\text{mV}$
 $R(\text{Ilim}) = (81.9\text{mV} \cdot 10) / 10\mu\text{A} \sim 81.9\text{K}$



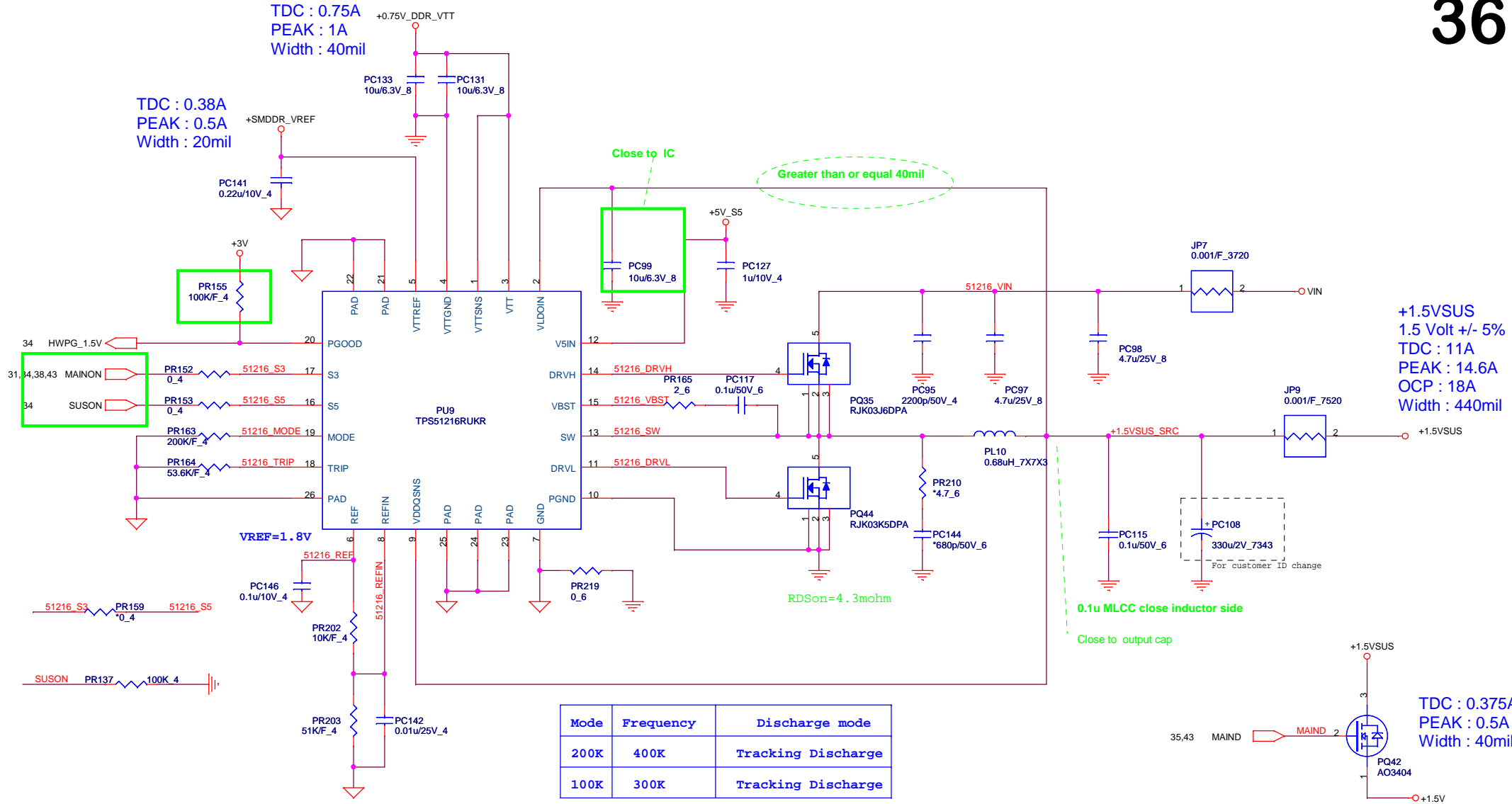
TDC : 2.25A
 PEAK : 3A
 Width : 100mil

TDC : 4A
 PEAK : 5.4A
 Width : 160mil

TDC : 2A
 PEAK : 2.7A
 Width : 80mil

TDC : 0.64A
 PEAK : 0.85A
 Width : 40mil

Quanta Computer Inc.
 PROJECT : ZRP
 SYSTEM 5V/3V (RT8223P)
 Date: Friday, June 01, 2012 Sheet 35 of 44
 Rev A1A



TDC : 0.75A
PEAK : 1A
Width : 40mil

TDC : 0.38A
PEAK : 0.5A
Width : 20mil

+1.5VSUS
1.5 Volt +/- 5%
TDC : 11A
PEAK : 14.6A
OCP : 18A
Width : 440mil

VREF=1.8V

Greater than or equal 40mil

0.1u MLCC close inductor side
Close to output cap

RDSon=4.3mohm

Mode	Frequency	Discharge mode
200K	400K	Tracking Discharge
100K	300K	Tracking Discharge

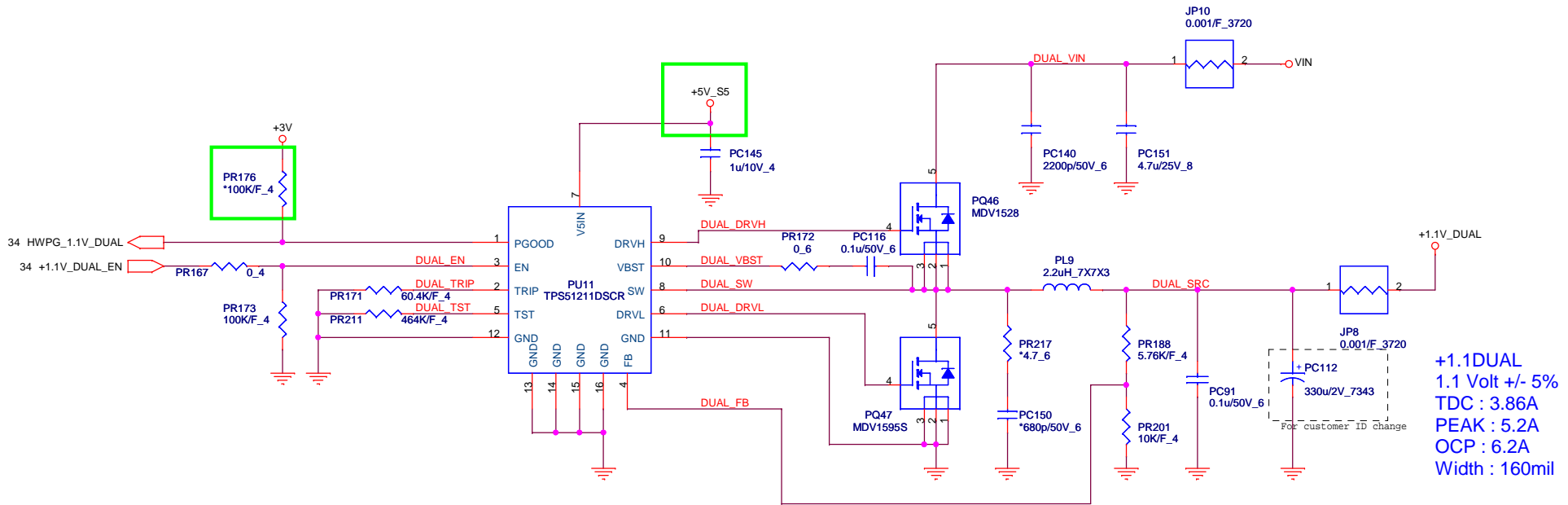
OCP=18A
L ripple current
=(19-1.5)*1.5/(0.68u*400k*19)
=5.079A
Vtrip=18-(5.079/2)*4.3mohm
=0.06647V
Rlimit=0.06647/10uA*8~53.183Kohm

	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

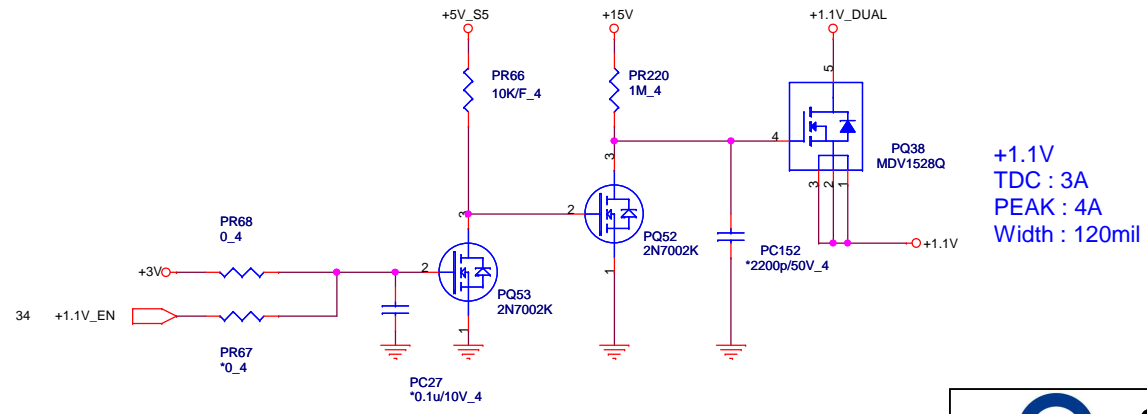
Quanta Computer Inc.
PROJECT : ZRP

Size Document Number Rev A1A
DDR 1.5V(TPS51216)

Date: Friday, June 01, 2012 Sheet 36 of 44

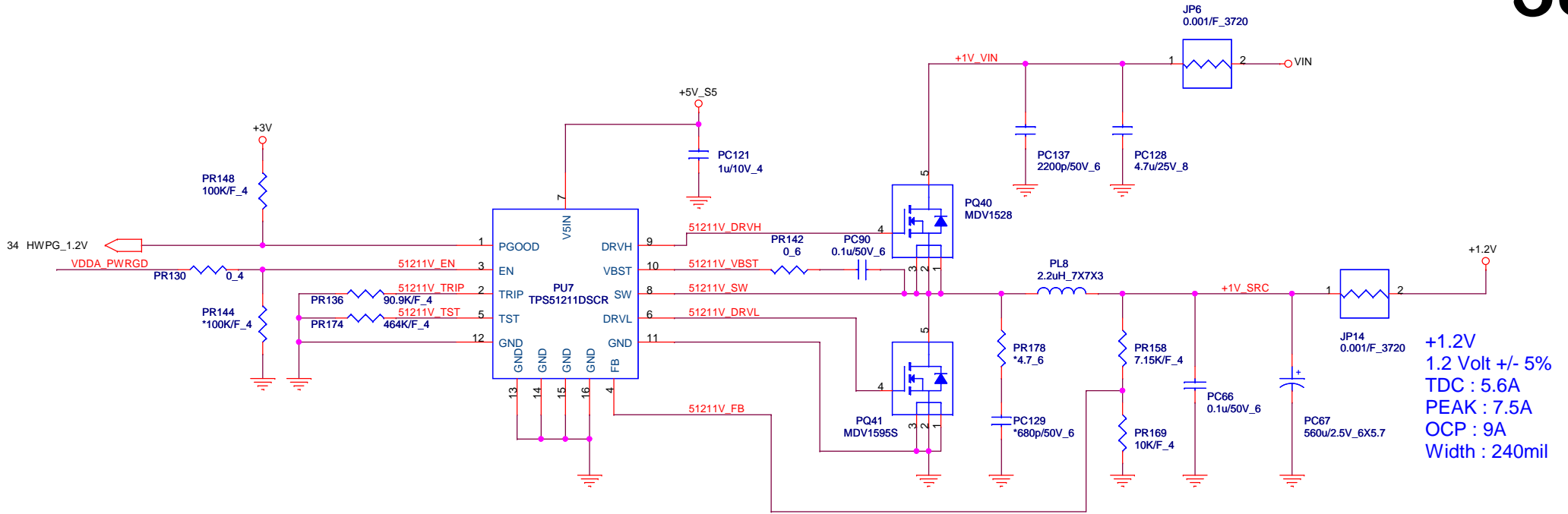


OCP=5A
 L ripple current
 $= (19-1.1) * 1.1 / (2.2u * 290k * 19)$
 $= 1.624A$
 $V_{trip} = 6.2 - (1.624/2) * 14mohm$
 $= 0.07542V$
 $R_{limit} = 0.07542 / 10uA * 8 - 60.34Kohm$

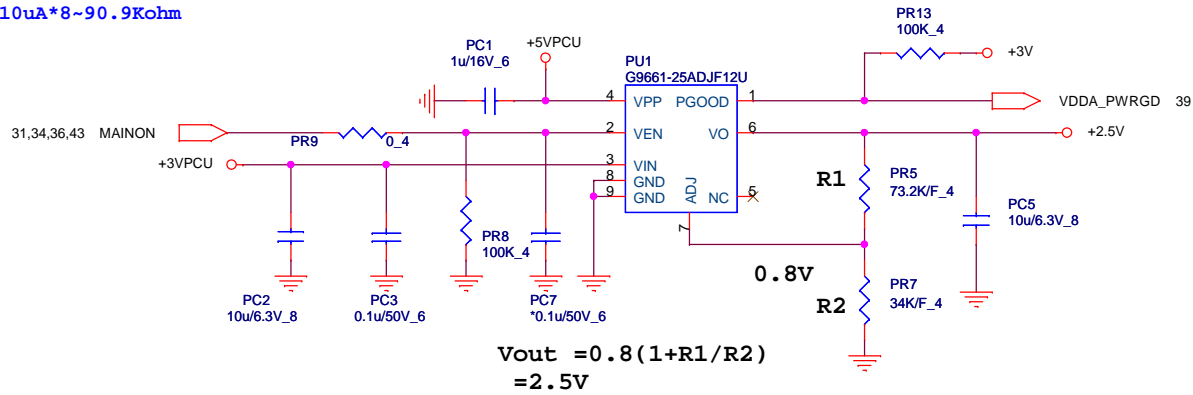


Quanta Computer Inc.
 PROJECT : ZRP

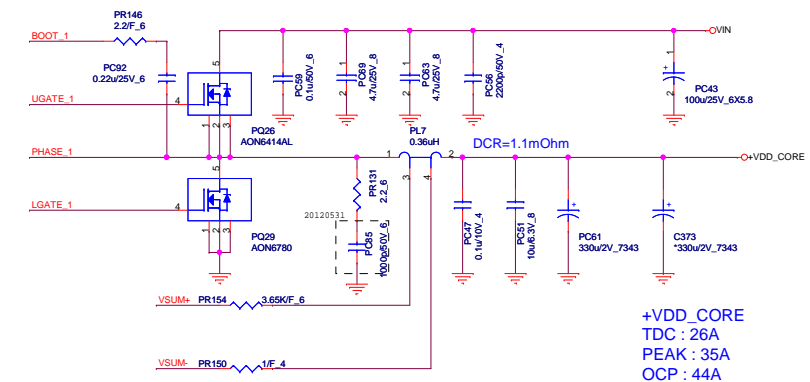
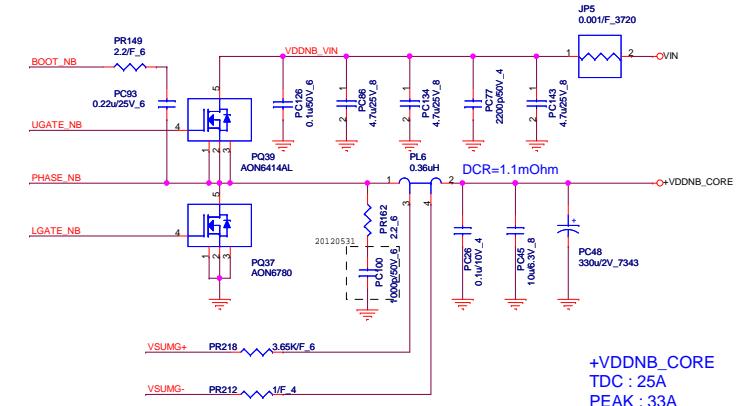
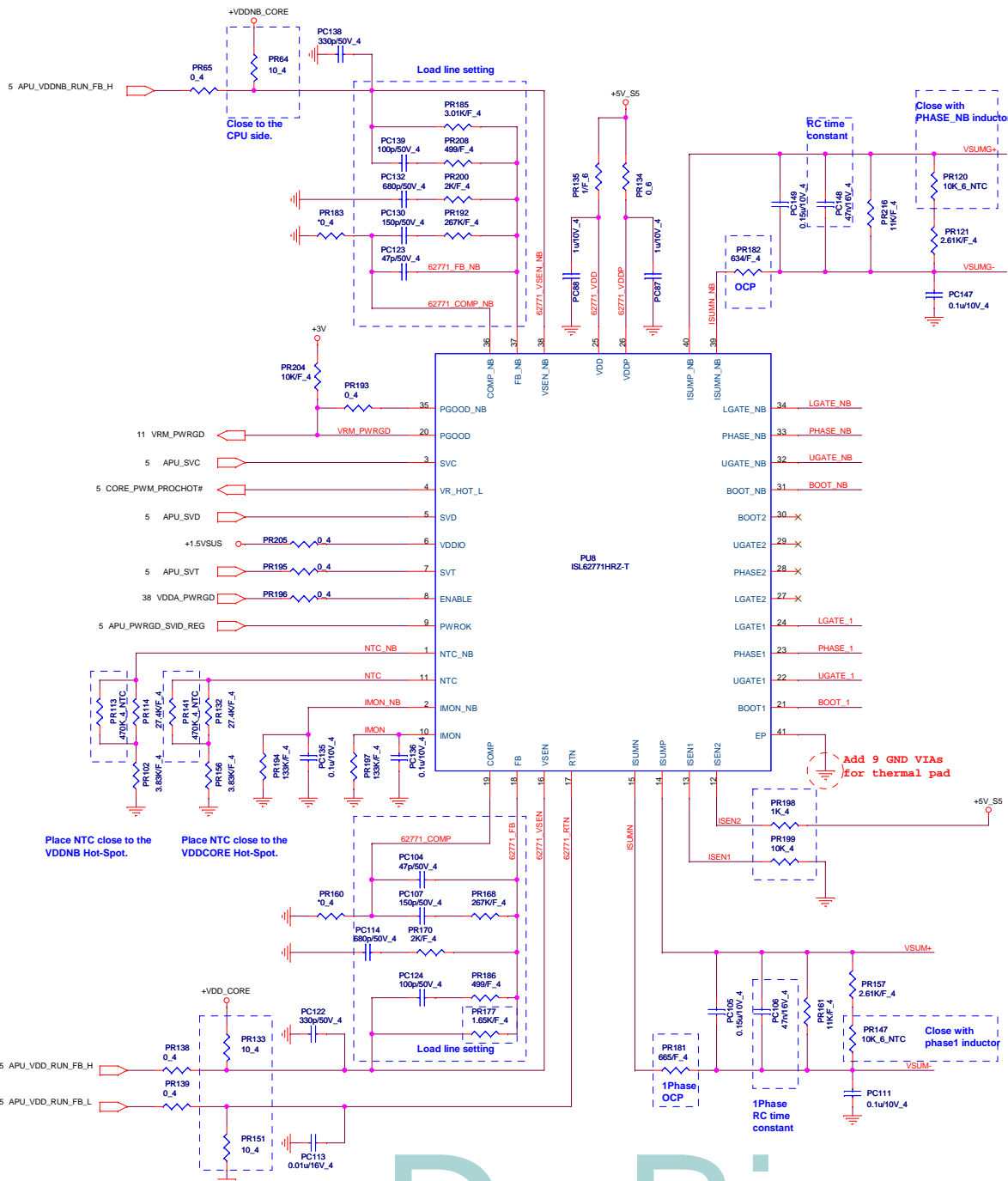
Size	Document Number	Rev
	+1.1V_DUAL(TPS51211)	A1A
Date:	Friday, June 01, 2012	Sheet 37 of 44



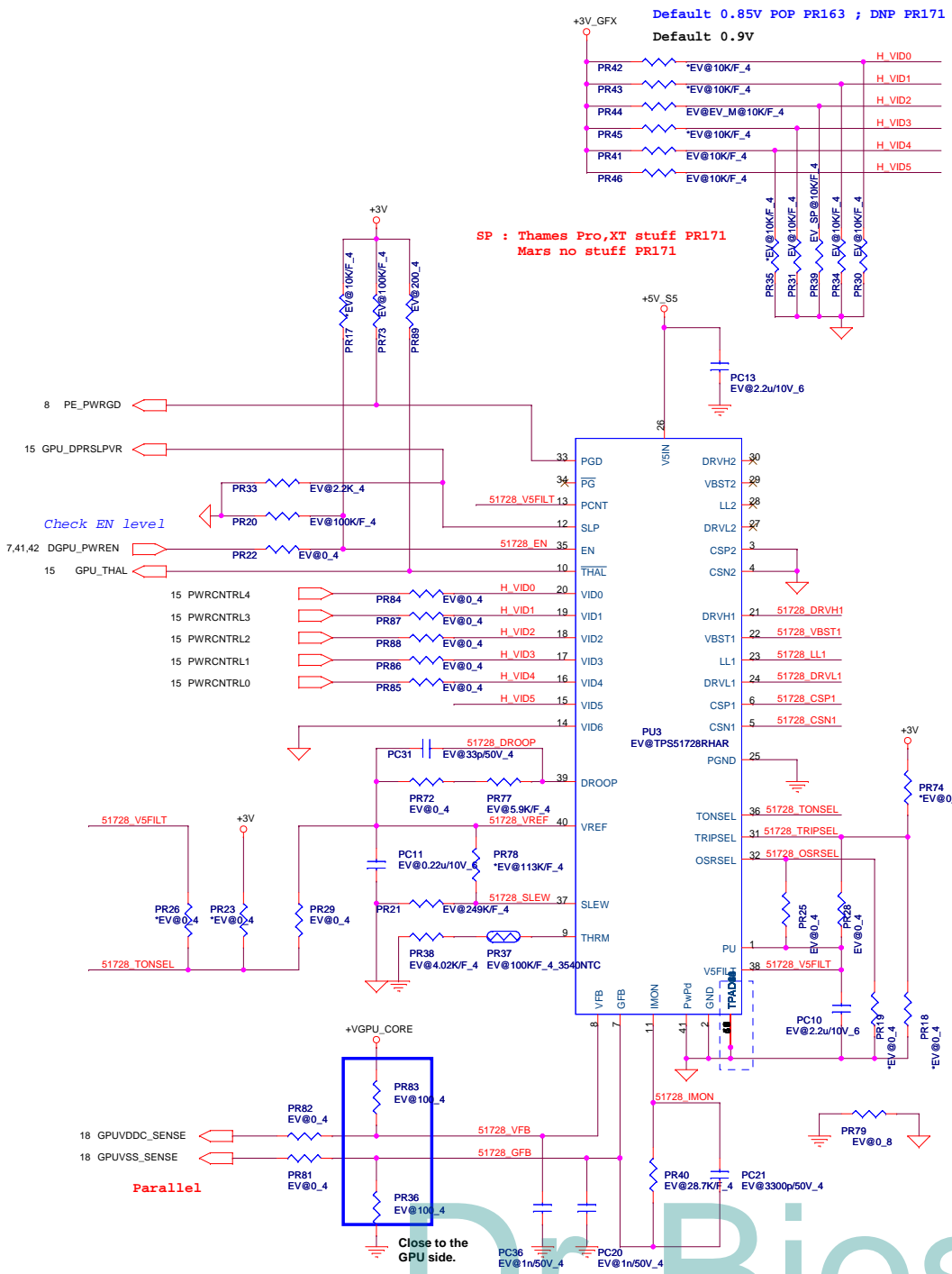
OCP=9A
 L ripple current
 $= (19 - 1.2) * 1.05 / (2.2 * 290k * 19)$
 $= 1.762A$
 $V_{trip} = 9 - (1.762 / 2) * 14mohm$
 $= 0.1136V$
 $R_{limit} = 0.1136 / 10uA * 8 \sim 90.9Kohm$



		Quanta Computer Inc.	
		PROJECT : ZRP	
Size	Document Number	+1.2V(TPS51211)+2.5V	
Date:	Friday, June 01, 2012	Sheet	38 of 44
		Rev	A1A



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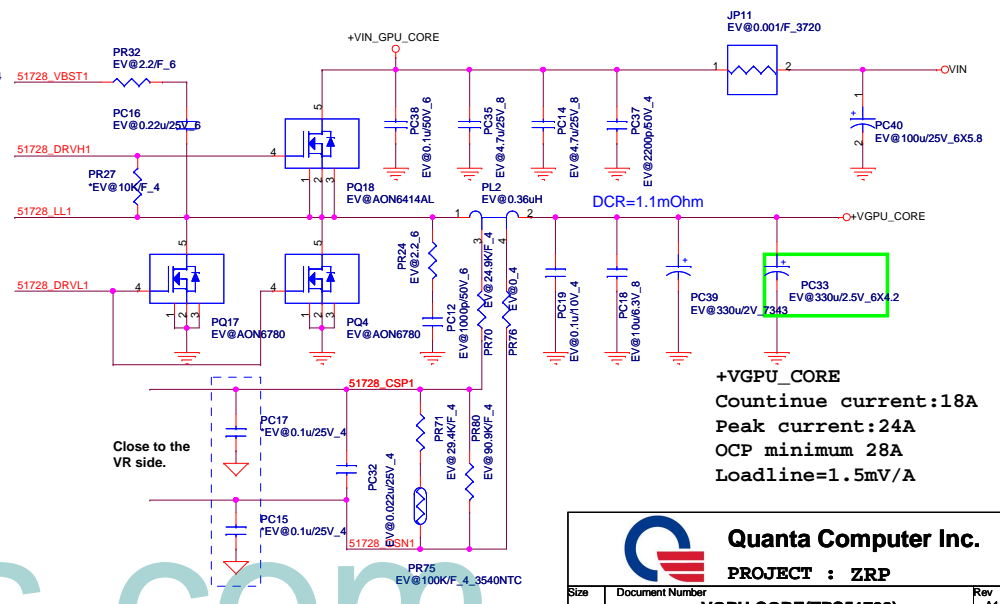


Thames(Pro,XT) VDDC VID TABLE

VDDC(V)	PWRCNTRL0 (VID4) (GPIO_15)	PWRCNTRL1 (VID3) (GPIO_20)
0.900	1	0
1.000	0	1

Mars VDDC VID TABLE

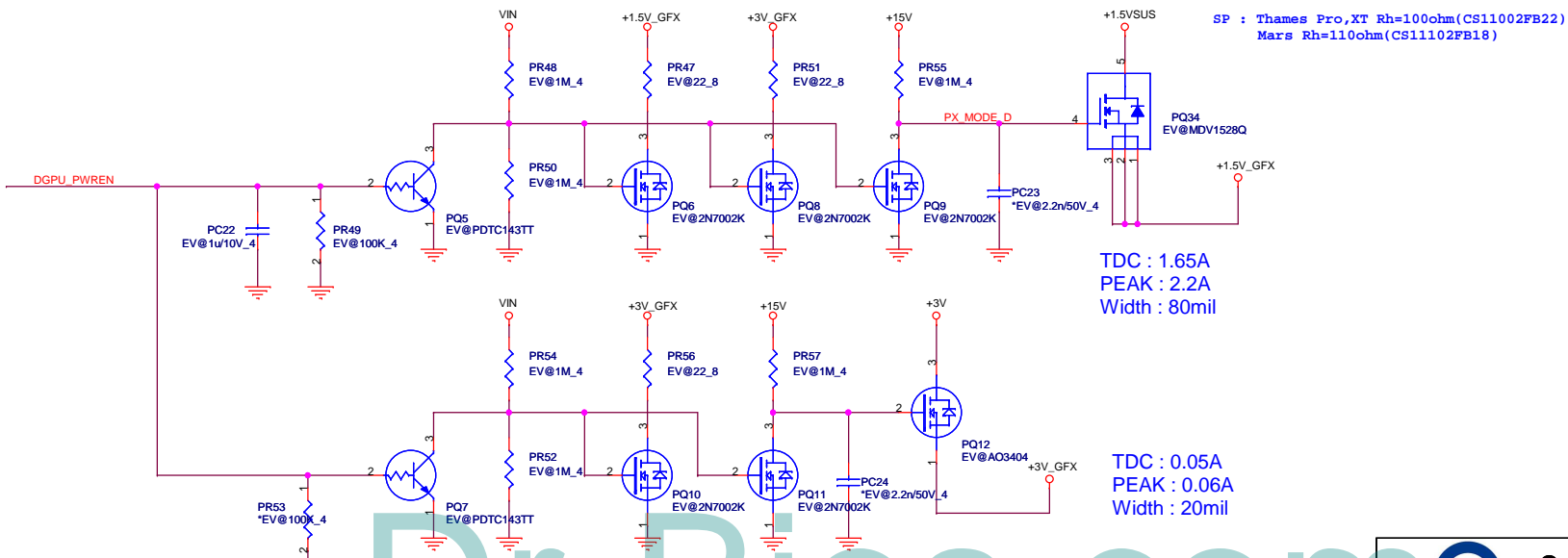
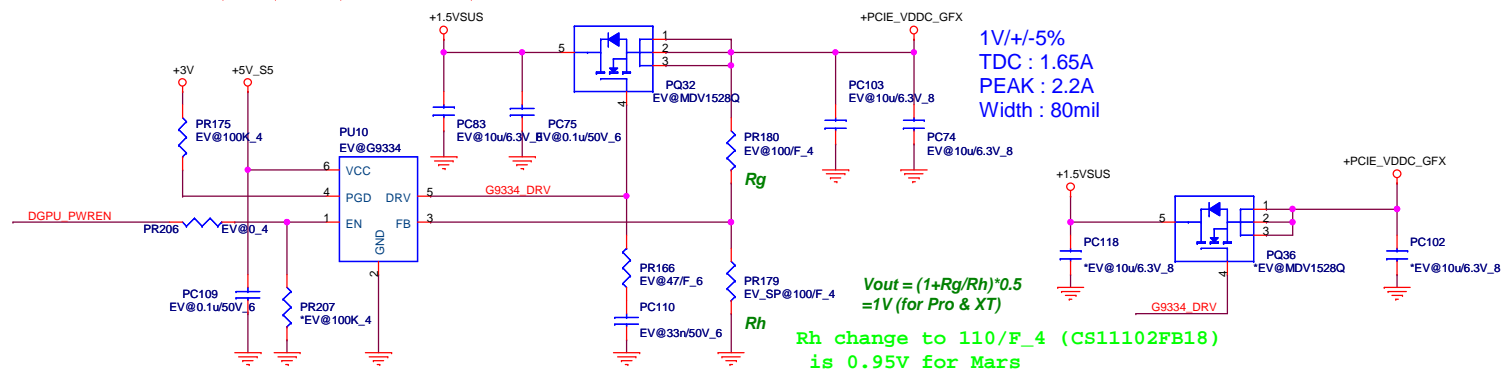
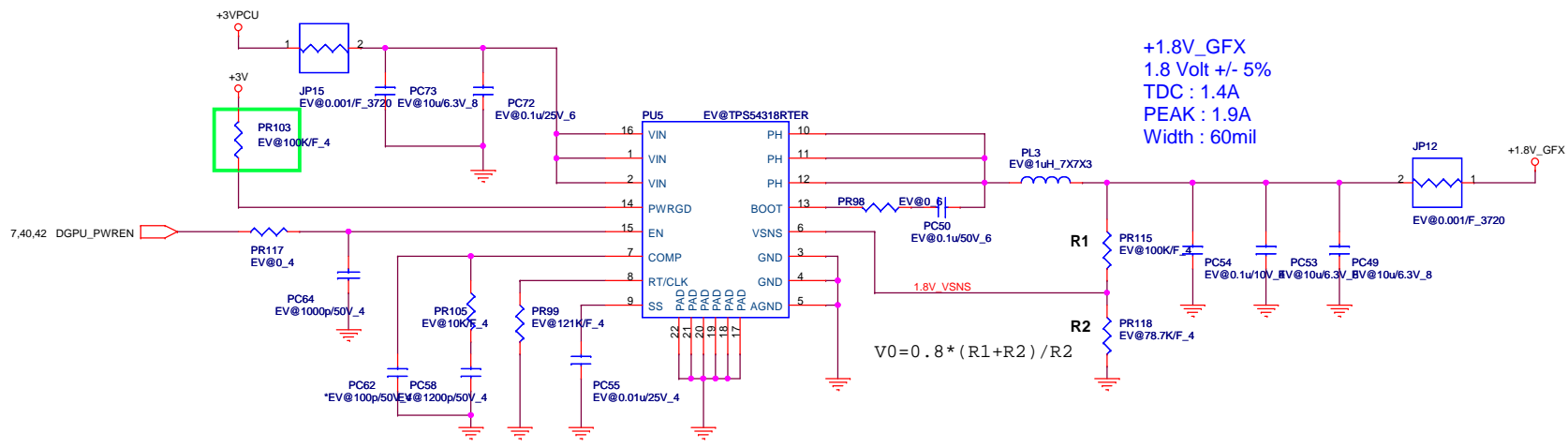
VDDC(V)	PWRCNTRL0 (VID4) (GPIO_15)	PWRCNTRL1 (VID3) (GPIO_20)	PWRCNTRL2 (VID2) (GPIO_16)	PWRCNTRL3 (VID1) (GPIO_29)	PWRCNTRL4 (VID0) (GPIO_30)
1.100	0	0	0	0	0
1.075	0	0	0	1	0
1.050	0	0	1	0	0
1.025	0	0	1	1	0
1.000	0	1	0	0	0
0.975	0	1	0	1	0
0.950	0	1	1	0	0
0.925	0	1	1	1	0
0.900	1	0	0	0	0
0.875	1	0	0	1	0
0.850	1	0	1	0	0
0.825	1	0	1	1	0
0.800	1	1	0	0	0



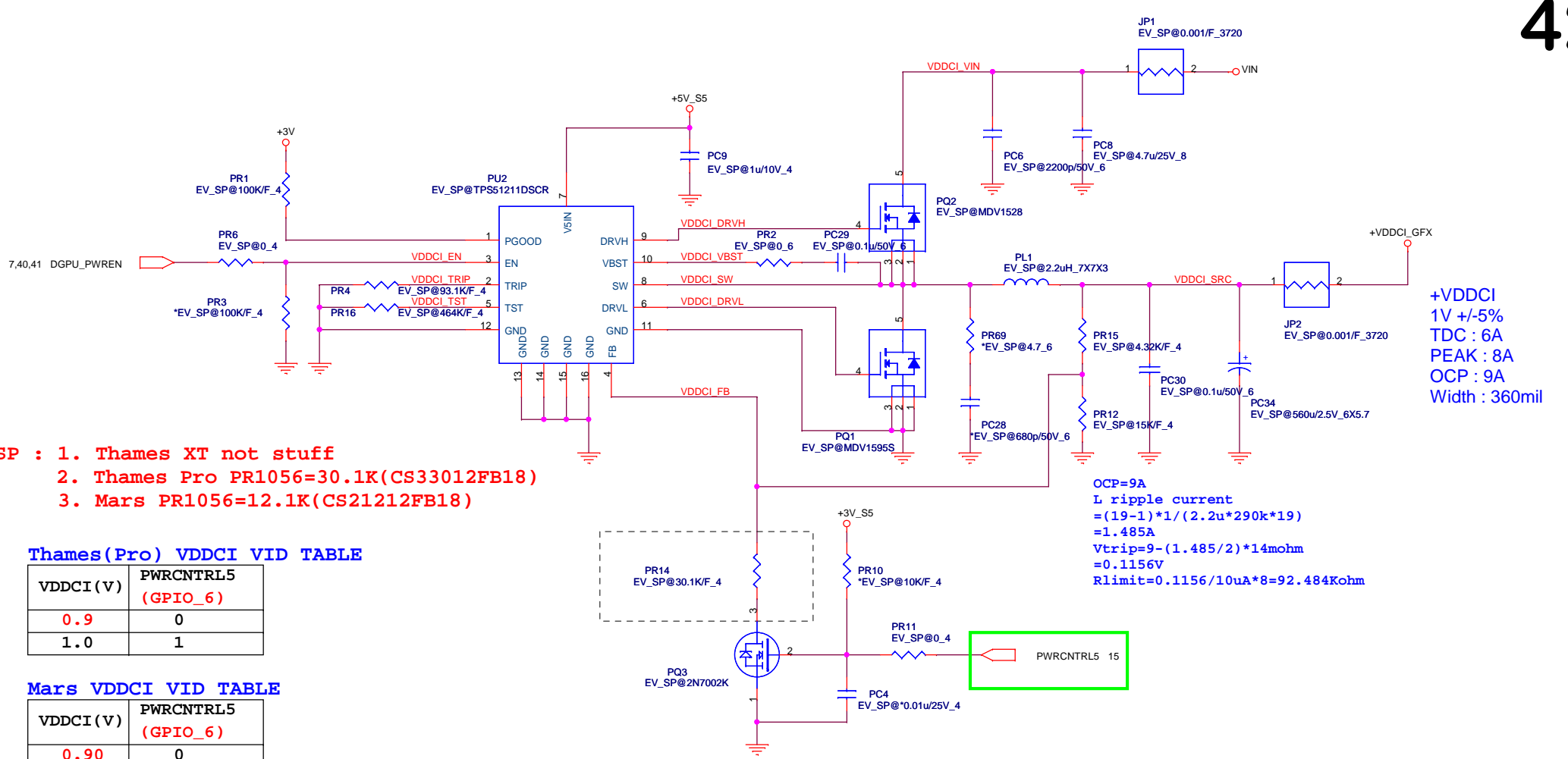
Quanta Computer Inc.
PROJECT : ZRP

Size	Document Number	Rev
	+VGPU CORE(TPS51728)	A1A

Date: Friday, June 01, 2012 Sheet 40 of 44



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+VDDCI
1V +/-5%
TDC : 6A
PEAK : 8A
OCP : 9A
Width : 360mil

OCP=9A
L ripple current
= (19-1) * 1 / (2.2u * 290k * 19)
= 1.485A
Vtrip = 9 - (1.485 / 2) * 14mohm
= 0.1156V
Rlimit = 0.1156 / 10uA * 8 = 92.484Kohm

- SP : 1. Thames XT not stuff
- 2. Thames Pro PR1056=30.1K(CS33012FB18)
- 3. Mars PR1056=12.1K(CS21212FB18)

Thames(Pro) VDDCI VID TABLE

VDDCI (V)	PWRCTRL5 (GPIO_6)
0.9	0
1.0	1

Mars VDDCI VID TABLE

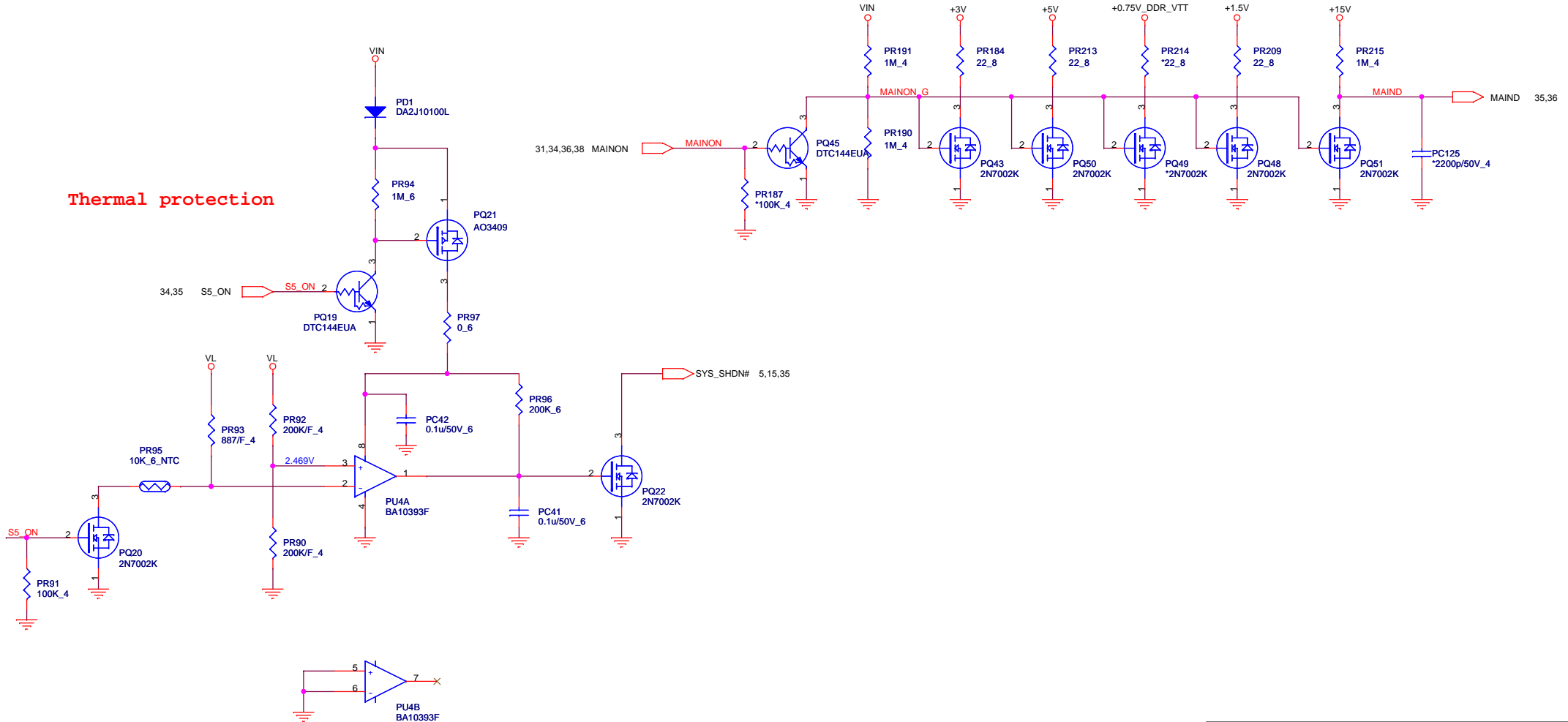
VDDCI (V)	PWRCTRL5 (GPIO_6)
0.90	0
0.95	1

PR1056 change to 12.1K/F_4 (CS21212FB18) for Mars 0.95V


Quanta Computer Inc.
PROJECT : ZRP

Size	Document Number	Rev
	VDDCI(TPS51518)	A1A
Date:	Friday, June 01, 2012	Sheet 42 of 44

Thermal protection




For EC control thermal protection (output 3.3V)

 Quanta Computer Inc. PROJECT : ZRP		Rev
		A1A
Size	Document Number	Discharge/Thermal Sheet 43 of 44
Date: Friday, June 01, 2012		

MODEL	REV	CHANGE LIST	Model	ZRP MB BOARD	
			Page	From	To
ZRP M/B	A	First Release	1		
			2		
			3		
			4		
			5		
			6		
			7		
			8		
			9		
			10		
			11		
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			39		
			40		
			41		

ZRP
 APPROVED BY :
 PCBA NO :
 CHECK BY :
 REV: A
 DRAWING BY :
 DOC. NO :
 DATE :



Size	Document Number	 Quanta Computer Inc. PROJECT : ZRP	Rev A1A