Husk/Petra
UMA/Muxless Schematics Document
Ivy Bridge
Intel PCH

DY :None Installed
DIS:DIS installed
DIS_Muxless :BOTH DIS or Muxless installed
DIS_PX:BOTH DIS or PX installed
DIS_PX_Muxless:DIS or PX or Muxless installed.
Muxless: Muxless installed.(PX4.0)
PX:MUX installed.(PX3.0)
PX_Muxless:BOTH PX or Muxless installed.
UMA:UMA installed
UMA_Muxless:BOTH UMA or Muxless installed
UMA_PX_Muxless:UMA or PX or Muxless installed

ANNIE: ONLY FOR ANNIE solution.
PSL: KBC795 PSL circuit for 10mW solution installed.
10mW: External circuit for 10mW solution installed.
65W: for 65W adaptor installed.
90W: for 90W adaptor installed.

<Core Design>

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Title: Cover Page
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Date: Monday, March 05, 2012 | Sheet 1 of 103

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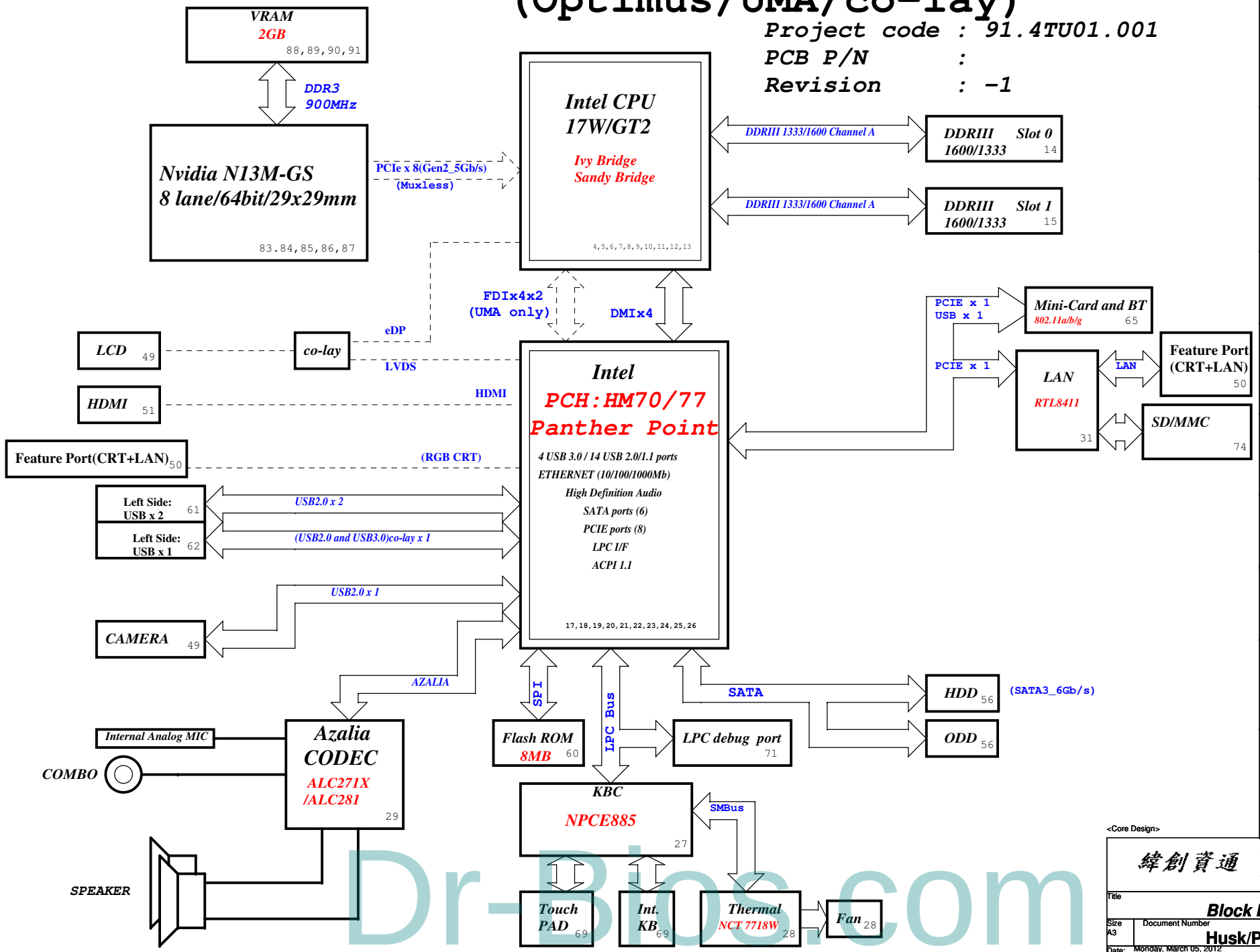
Husk and Petra Block Diagram (Optimus/UMA/co-lay)

Project code : 91.4TU01.001
PCB P/N :
Revision : -1



CHARGER BQ24727 40	
INPUTS	OUTPUTS
DCBATOUT	BT+

SYSTEM DC/DC RT8223MGQW 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

CPU DC/DC ISL95836HRTZ 42~43	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC ISL95836HRTZ 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE

SYSTEM DC/DC TPS51218DSCR 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC RT8207LGQW 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

LDO RT9025-25ZSP 47	
INPUTS	OUTPUTS
3D3V_S0	1D8V_S0

LDO G978 48	
INPUTS	OUTPUTS
1D05_VTT	0D85V_S0

VGA ISL62882CHRTZ 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

Switches 93	
INPUTS	OUTPUTS
3D3V_S0	3D3V_VGA_S0
1D05V_VTT	1D05V_VGA_S0
1D5V_S3	1D5V_VGA_S0

PCB LAYER

L1:Top L4:Signal
L2:VCC L5:GND
L3:Signal L6:Bottom

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PCH Strapping

Huron River Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Huron River Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	0
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	1

POWER PLANE	VOLTAGE	Voltage Rails ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

PCIE Routing

LANE1	Mini Card2(WWAN)
LANE2	Mini Card1(WLAN)
LANE3	Card Reader
LANE4	Onboard LAN
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	New Card

SATA Table

SATA	
Pair	Device
0	HDD1
1	HDD2
2	N/A
3	N/A
4	ODD
5	ESATA

USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGER
9	USB Ext. port 2
10	EDP CAMERA
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

SMBus ADDRESSES

I² C / SMBus Addresses Device	Ref Des	HURON RIVER ORB Address	Hex	Bus
EC SMBus 1 Battery CHARGER				BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP				SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI				PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

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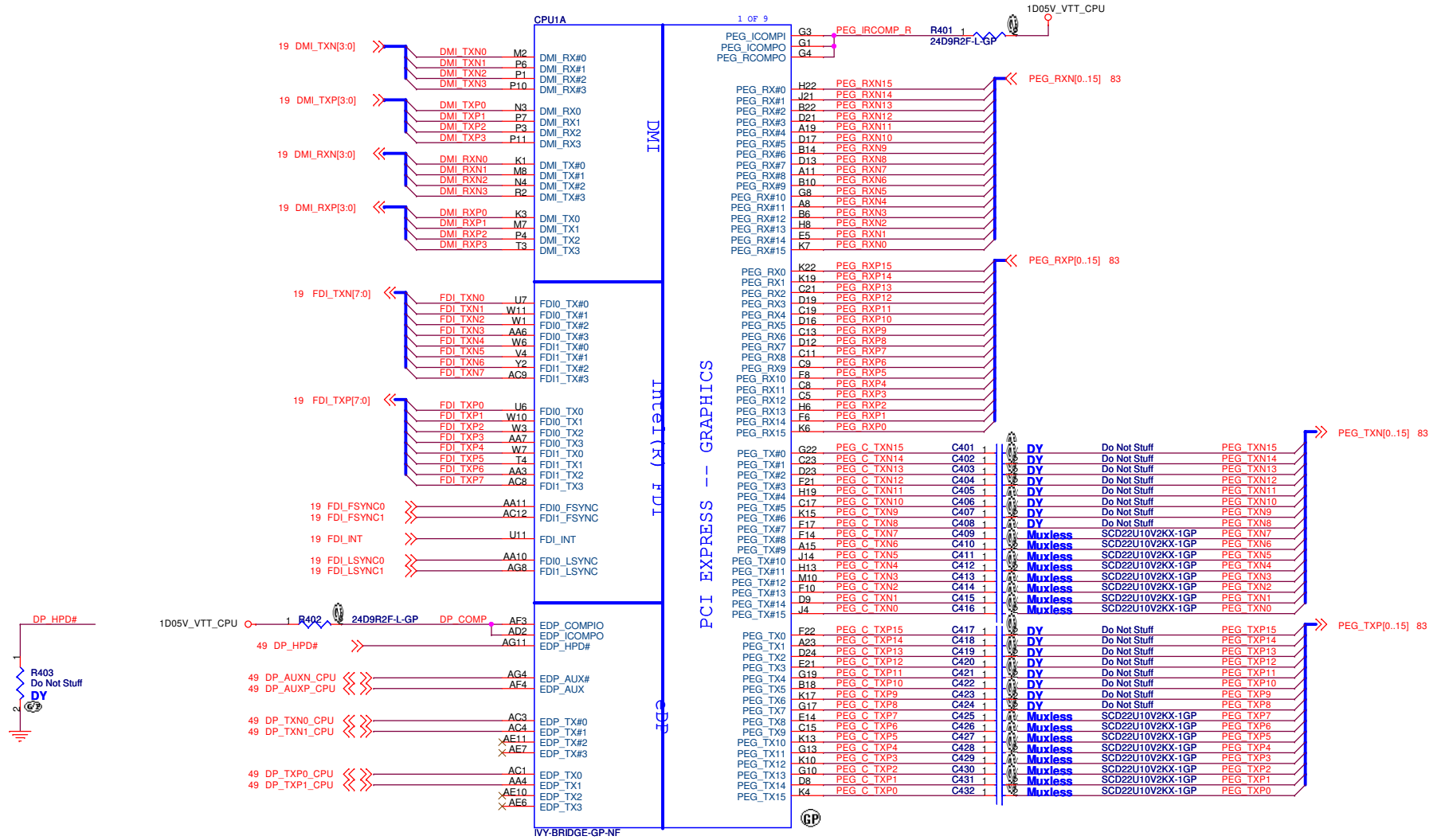
SSID = CPU



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Title: CPU (PCIE/DMI/FDI)

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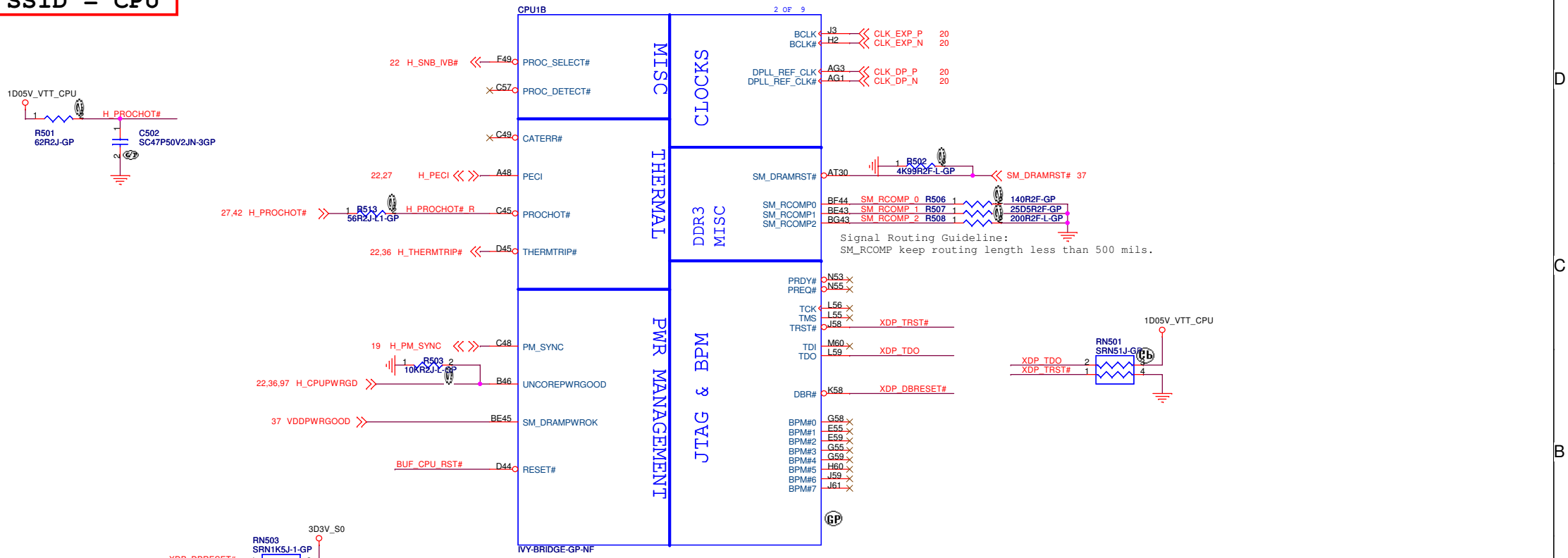
SSID = CPU



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Title: CPU (THERMAL/CLOCK/PM)

Size: Custom | Document Number: Husk/Petra | Rev: -1

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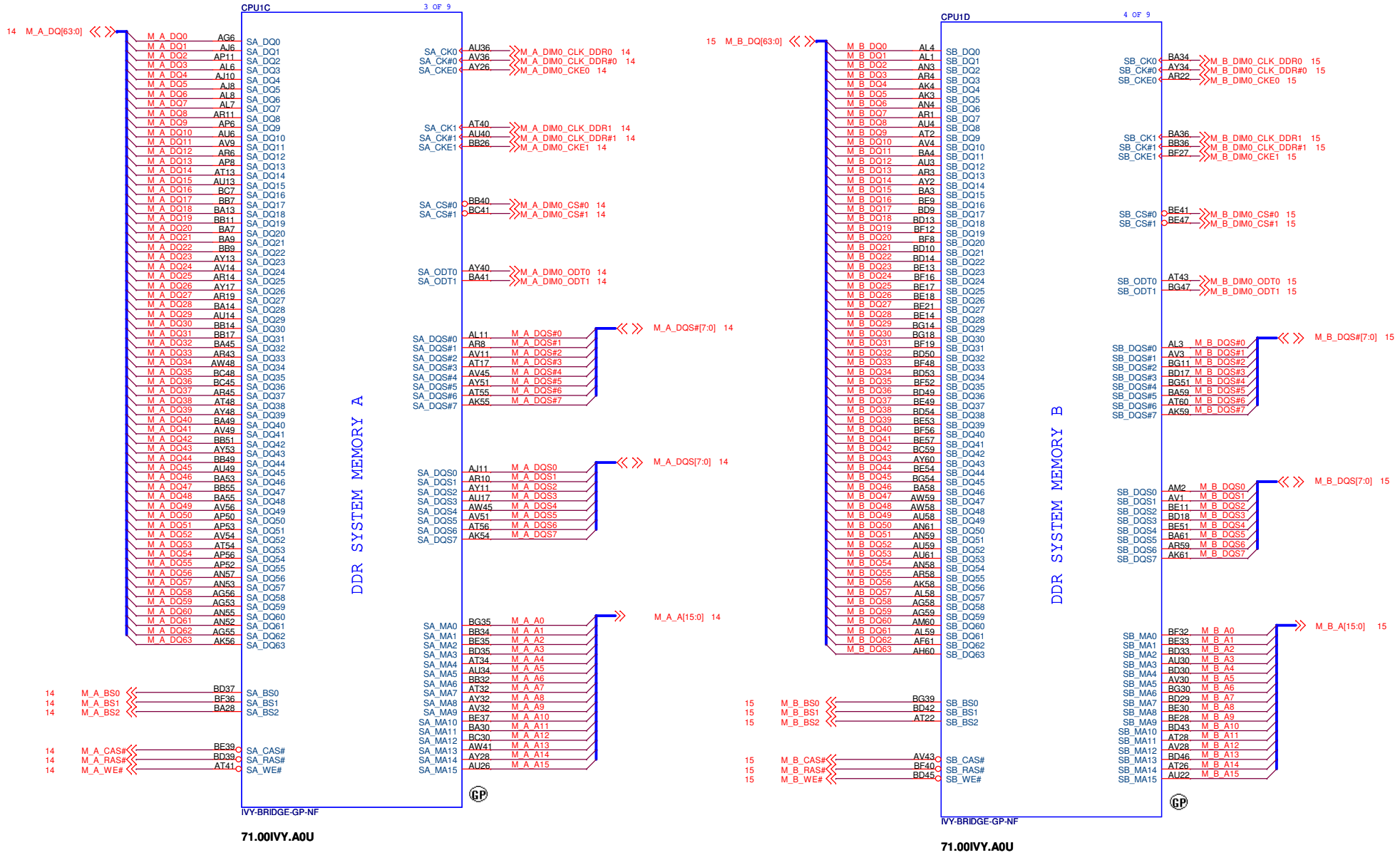
SSID = CPU



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Title: CPU (DDR)

Size: A3 | Document Number: Husk/Petra | Rev: -1

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SSID = CPU

PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed

CFG2
R702
1KR2J-L2-GP
Muxless

Enabl EDP function	
CFG4	1:Disable 0:Enable

CFG4
R703
1KR2J-L2-GP
EDP

PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

CFG5
R704
Do Not Stuff
DY

CFG6
R705
Do Not Stuff
DY

PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

CFG7
R706
Do Not Stuff
DY

Do Not Stuff TP701 1 CFG0_TP
Do Not Stuff TP702 1 CFG1_TP
CFG2
Do Not Stuff TP703 1 CFG3_TP
CFG4
CFG5
CFG6
CFG7

CPU1E 5 OF 9

RESERVED

B50	CFG0	BCLK_ITP	N59
C51	CFG1	BCLK_ITP#	N58
B54	CFG2		
D53	CFG3		
A51	CFG4	RSVD30	N42
C53	CFG5	RSVD31	L42
C55	CFG6	RSVD32	L45
H49	CFG7	RSVD33	L47
A55	CFG8		
H51	CFG9		
K49	CFG10	RSVD34	M13
K53	CFG11	RSVD35	M14
F53	CFG12	RSVD36	U14
G53	CFG13	RSVD37	W14
L51	CFG14	RSVD38	P13
F51	CFG15		
D52	CFG16		
L53	CFG17	RSVD39	AT49
		RSVD40	K24
H43	VCC_VAL_SENSE		
K43	VSS_VAL_SENSE	RSVD41	AH2
		RSVD42	AG13
H45	VAXG_VAL_SENSE	RSVD43	AM14
K45	VSSAXG_VAL_SENSE	RSVD44	AM15
		RSVD45	N50
F48	VCC_DIE_SENSE		
G48	RSVD47		
H48	RSVD6		
K48	RSVD7		
		DC_TEST_A4	A4
		DC_TEST_C4	C4
BA19	RSVD8	DC_TEST_D3	D3
AV19	RSVD9	DC_TEST_D1	D1
AT21	RSVD10	DC_TEST_A58	A58
BB21	RSVD11	DC_TEST_A59	A59
BB19	RSVD12	DC_TEST_C59	C59
AY21	RSVD13	DC_TEST_A61	A61
BA22	RSVD14	DC_TEST_C61	C61
AY22	RSVD15	DC_TEST_D61	D61
AU19	RSVD16	DC_TEST_BD61	BD61
AU21	RSVD17	DC_TEST_BE61	BE61
BD21	RSVD18	DC_TEST_BE59	BE59
BD22	RSVD19	DC_TEST_BG61	BG61
BD25	RSVD20	DC_TEST_BG59	BG59
BD26	RSVD21	DC_TEST_BG58	BG58
BG22	RSVD22	DC_TEST_BG4	BG4
BE22	RSVD23	DC_TEST_BG3	BG3
BG26	RSVD24	DC_TEST_BE3	BE3
BE26	RSVD25	DC_TEST_BG1	BG1
BF23	RSVD26	DC_TEST_BE1	BE1
BE24	RSVD27	DC_TEST_BD1	BD1

GP

IVY-BRIDGE-GP-NF

71.00IVY.A0U

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SSID = CPU

POWER

ULV:17W
Iccmax:33A
ICC_TDC:25A

Iccmax:8.5A
ICC_TDC:8.5A

CPU1F

6 OF 9

CORE SUPPLY

PEG IO AND DDR IO

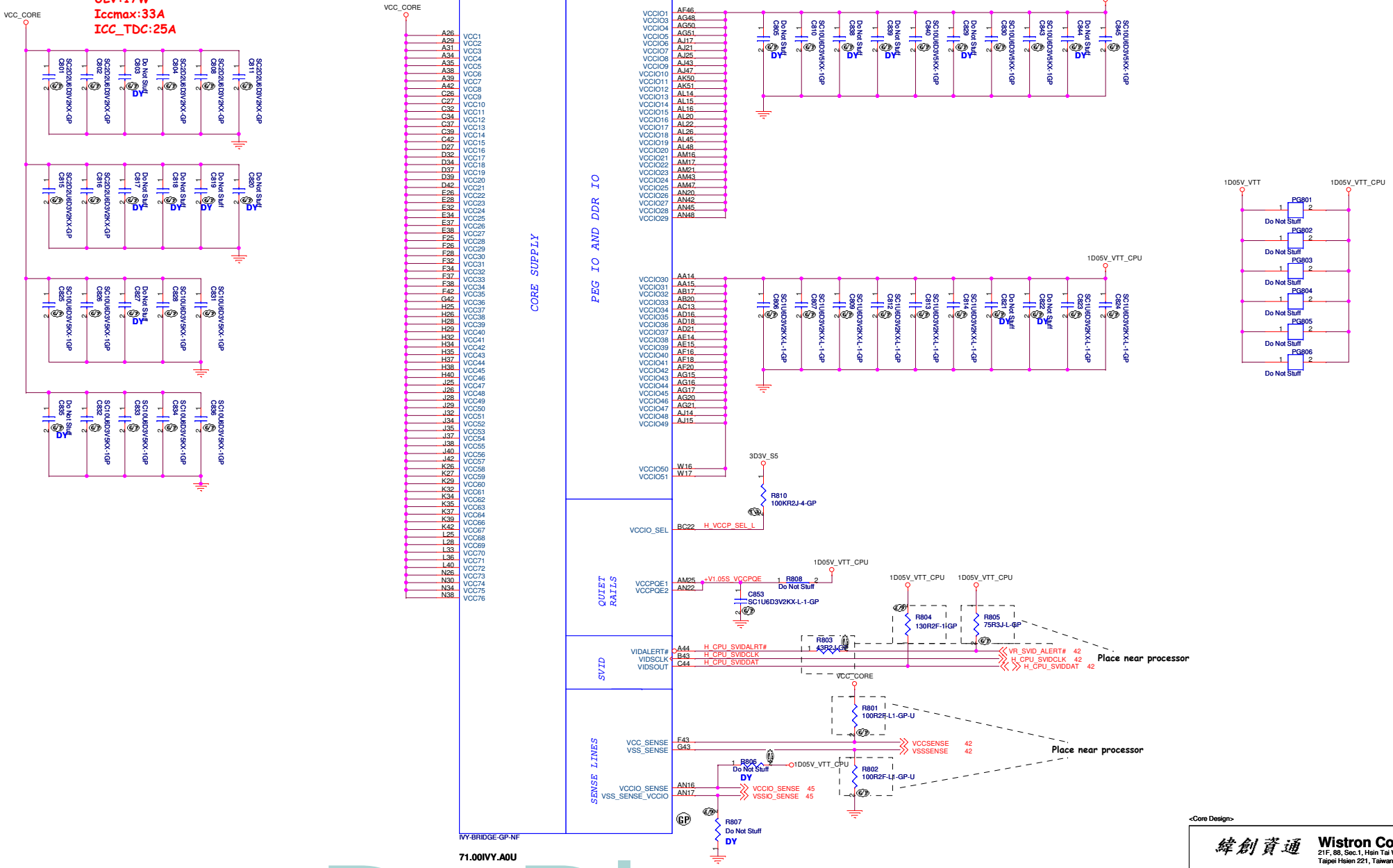
QUIET RAILS

SVID

SENSE LINES

IVY-BRIDGE-GP-NF

71.00IVY.A0U



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Title: CPU (VCC_CORE)

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SSID = CPU

POWER

Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT
should have 10 mils trace width.

Iccmax:18A(GT1)
ICC_TDC:12A(GT1)

CPU1G

7 OF 9

VCC_GFXCORE

SC1U6D3V5KX-1GP C902, C903, C904 DY, C905, C906, C919, C920, C921 DY

SC1U6D3V2KX-L-1GP C907, C909, C914, C916

VAXG1 VAXG2 VAXG3 VAXG4 VAXG5 VAXG6 VAXG7 VAXG8 VAXG9 VAXG10 VAXG11 VAXG12 VAXG13 VAXG14 VAXG15 VAXG16 VAXG17 VAXG18 VAXG19 VAXG20 VAXG21 VAXG22 VAXG23 VAXG24 VAXG25 VAXG26 VAXG27 VAXG28 VAXG29 VAXG30 VAXG31 VAXG32 VAXG33 VAXG34 VAXG35 VAXG36 VAXG37 VAXG38 VAXG39 VAXG40 VAXG41 VAXG42 VAXG43 VAXG44 VAXG45 VAXG46 VAXG47 VAXG48 VAXG49 VAXG50 VAXG51 VAXG52 VAXG53 VAXG54 VAXG55 VAXG56

GRAPHICS

VREF

SM_VREF AY43 → +V_SM_VREF_CNT 37

SA_DIMM_VREFDQ BE7 ← M_VREF_DQ_DIMM0_C
SB_DIMM_VREFDQ BG7 ← M_VREF_DQ_DIMM1_C

M_VREF_DQ_DIMM0_C 37
M_VREF_DQ_DIMM1_C 37

BE7 and BG7 is NC ball in HR

RN902 Do Not Stuff DY

DDR3 - 1.5V RAILS

Iccmax:5A

1D5V_S0

VDDQ1 AJ28, VDDQ2 AJ33, VDDQ3 AJ36, VDDQ4 AJ40, VDDQ5 AL30, VDDQ6 AL34, VDDQ7 AL38, VDDQ8 AL42, VDDQ9 AM33, VDDQ10 AM36, VDDQ11 AM40, VDDQ12 AN30, VDDQ13 AN34, VDDQ14 AN38, VDDQ15 AR26, VDDQ16 AR29, VDDQ17 AR30, VDDQ18 AR32, VDDQ19 AR34, VDDQ20 AR36, VDDQ21 AR40, VDDQ22 AV41, VDDQ23 AW26, VDDQ24 BA40, VDDQ25 BB28, VDDQ26 BG33

SC1U6D3V5KX-1GP C910, C911, C912 DY, C913, C924 DY, C925

SC1U6D3V2KX-L-1GP C916, C917, C926 DY

QUIET RAILS

PROCESSOR DDR 1.5V QUIET RAIL (BGA only)
+V1.5S_VCCD_Q should be short to +V1.5S_VCCDDQ on board

VCCDQ1 AM28, VCCDQ2 AN26 ← +1.5S_VCCD_Q

1D5V_S0

R909 Do Not Stuff

C923 SC1U6D3V2KX-L-1GP

SENSE LINES

VAXG_SENSE F45, VSSAXG_SENSE G45

42 VCC_AXG_SENSE
42 VSS_AXG_SENSE

VCC_GFXCORE

R906 100R2F-L1-GP-U

R907 100R2F-L1-GP-U

R906,R907 close to CPU

VCC_AXG_SENSE
VSS_AXG_SENSE

1.8V RAIL

1D8V_S0

ICC_MAX:1.2A

C922 SC1U10V2KX-1GP

VCCPLL1 BB3, VCCPLL2 BC1, VCCPLL3 BC4

SENSE LINES

VDDQ_SENSE BC43 TP_VDDQ_SENSE
VSS_SENSE_VDDQ BA43 TP_VDDQ_VSS

TP901 Do Not Stuff
TP902 Do Not Stuff

0D85V_S0

R902 100R2F-L1-GP-U

R902 need be close to pin U10.

VCCSA_SENSE U10 ← VCCSA_SENSE

SA RAIL

0D85V_S0

ICC_MAX:6A

C915 SC10U6D3V5KX-1GP

VCCSA1 L17, VCCSA2 L21, VCCSA3 N16, VCCSA4 N20, VCCSA5 N22, VCCSA6 P17, VCCSA7 P20, VCCSA8 R16, VCCSA9 R18, VCCSA10 R21, VCCSA11 U15, VCCSA12 V16, VCCSA13 V17, VCCSA14 V18, VCCSA15 V21, VCCSA16 W20

VCCSA VID lines

VCCSA_VID0 D48, VCCSA_VID1 D49 ← VCCSA_VID0, VCCSA_VID1

VCCSA_VID[0]	VCCSA_VID[1]	Selected VCCSA (XE & SV segments)	Selected VCCSA (ULV segment)
0	0	0.9 V	0.9 V
0	1	0.8 V	0.85 V
1	0	0.725 V	0.775 V
1	1	0.675 V	0.75 V

1D05V_VTT_CPU 1D05V_VTT_CPU

R908 Do Not Stuff DY
R912 Do Not Stuff DY

VCCSA_VID0 → VCCSA_VID0 48
VCCSA_VID1 → VCCSA_VID1 48

R913 10KR2J-L-GP
R914 10KR2J-L-GP

IVY-BRIDGE-GP-NF

71.00IVY.A0U

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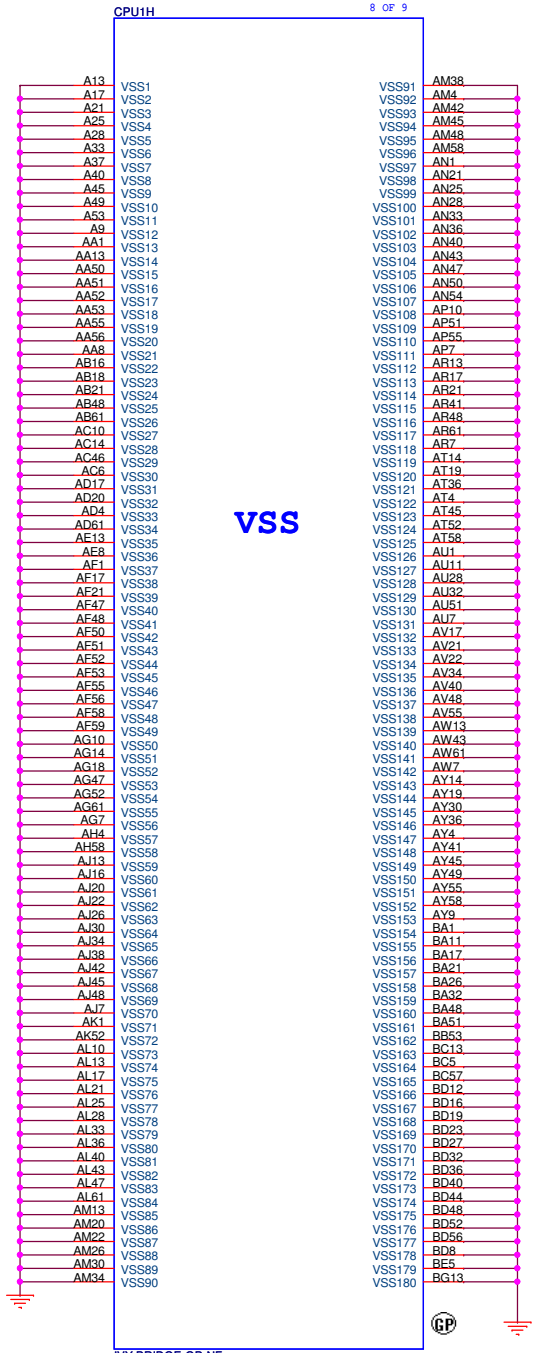

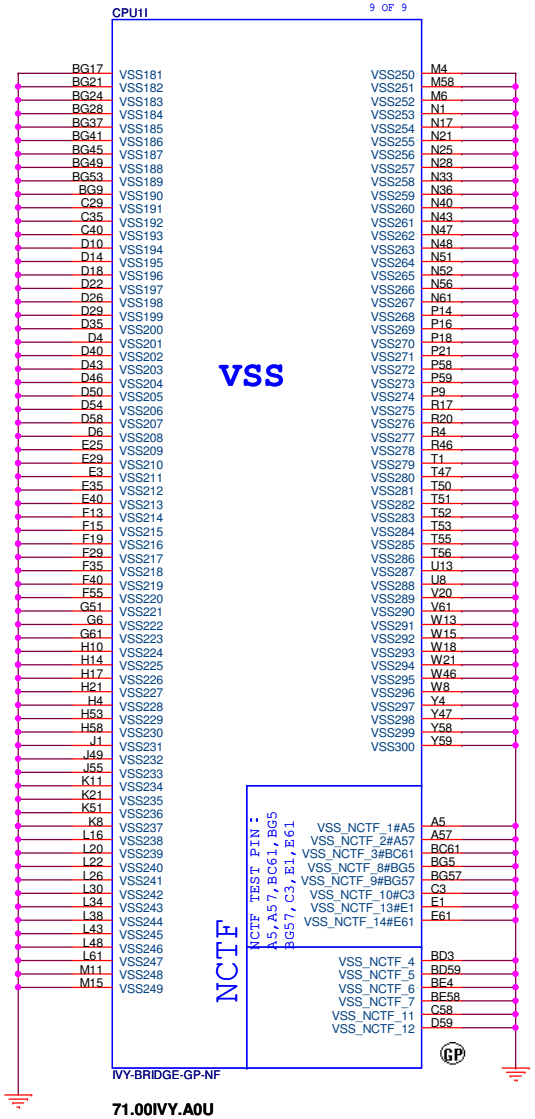

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Title: CPU (VSS)

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Title: ***Reserved***

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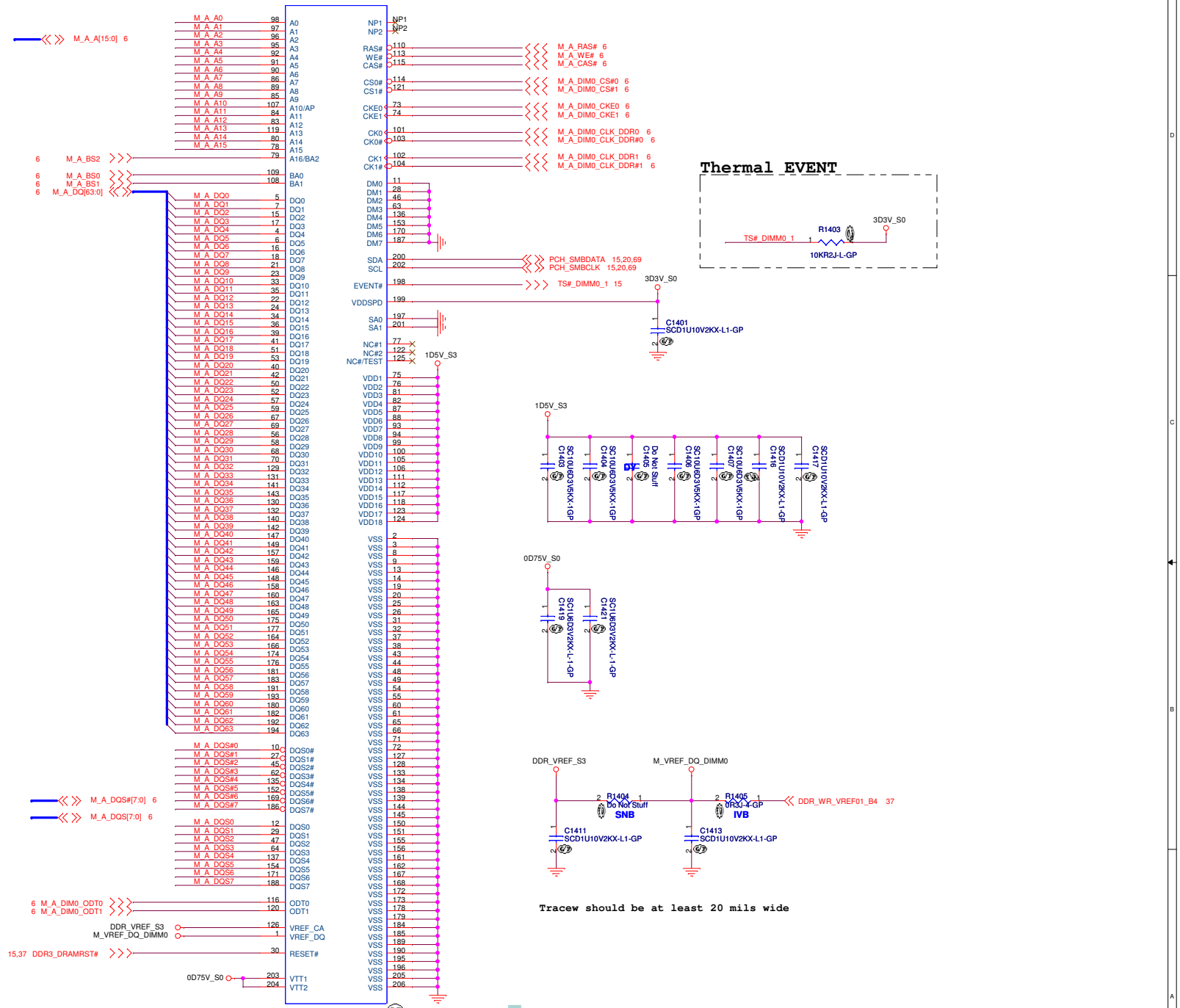
SSID = MEMORY



Thermal EVENT

Tracew should be at least 20 mils wide

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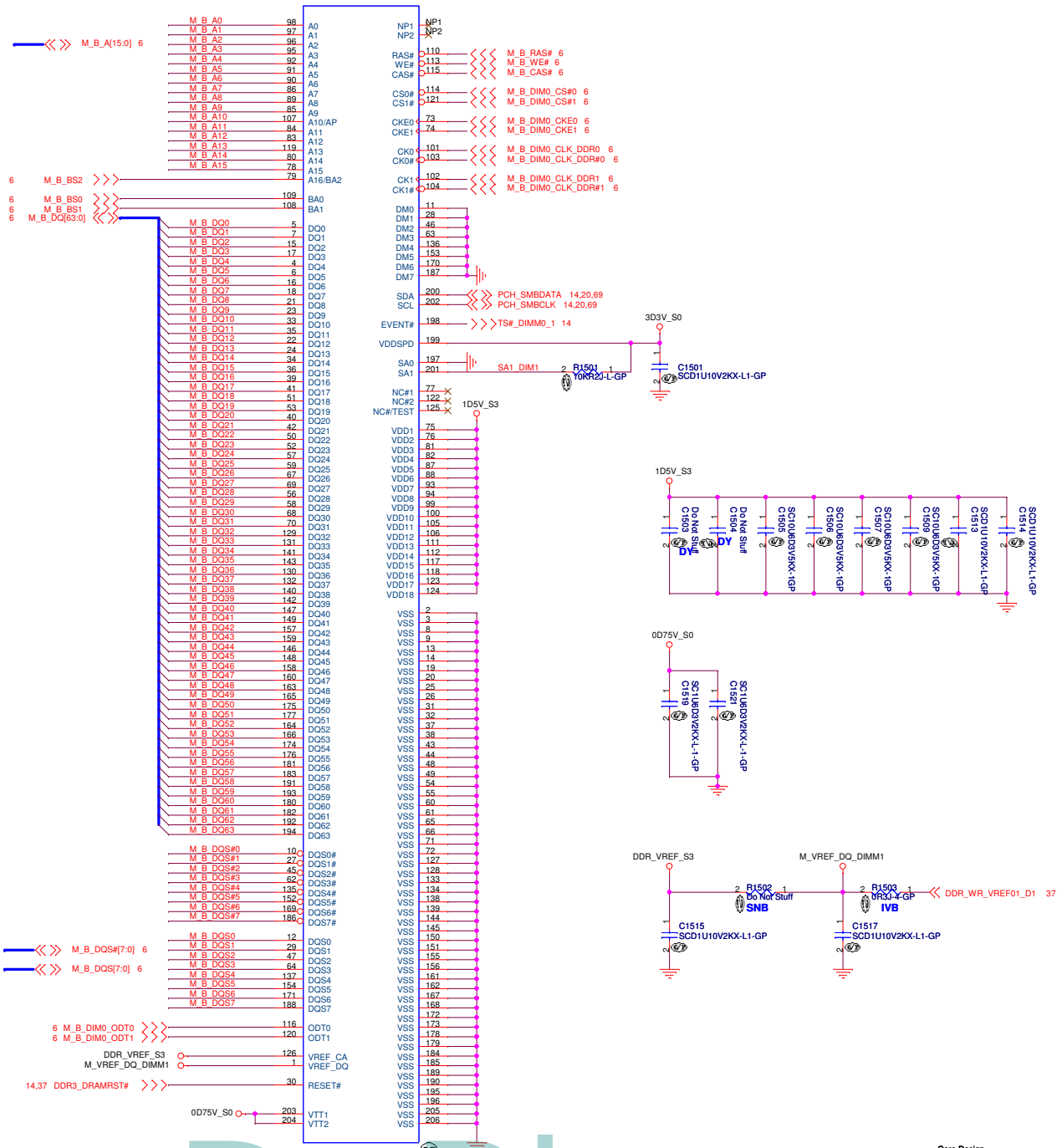
Title: ***DDR3-SODIMM1***

Size: Custom | Document Number: **Husk/Petra** | Rev: **-1**

Date: Monday, March 05, 2012 | Sheet 14 of 103

SSID = MEMORY



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Title: DDR3-SODIMM2

Size: Custom | Document Number: Husk/Petra | Rev: -1

Date: Monday, March 05, 2012 | Sheet 15 of 102

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Title: ***DDR3-SODIMM2***

Size	Document Number	Rev
A4	**Husk/Petra**	-1

Date: Monday, March 05, 2012 Sheet 16 of 103

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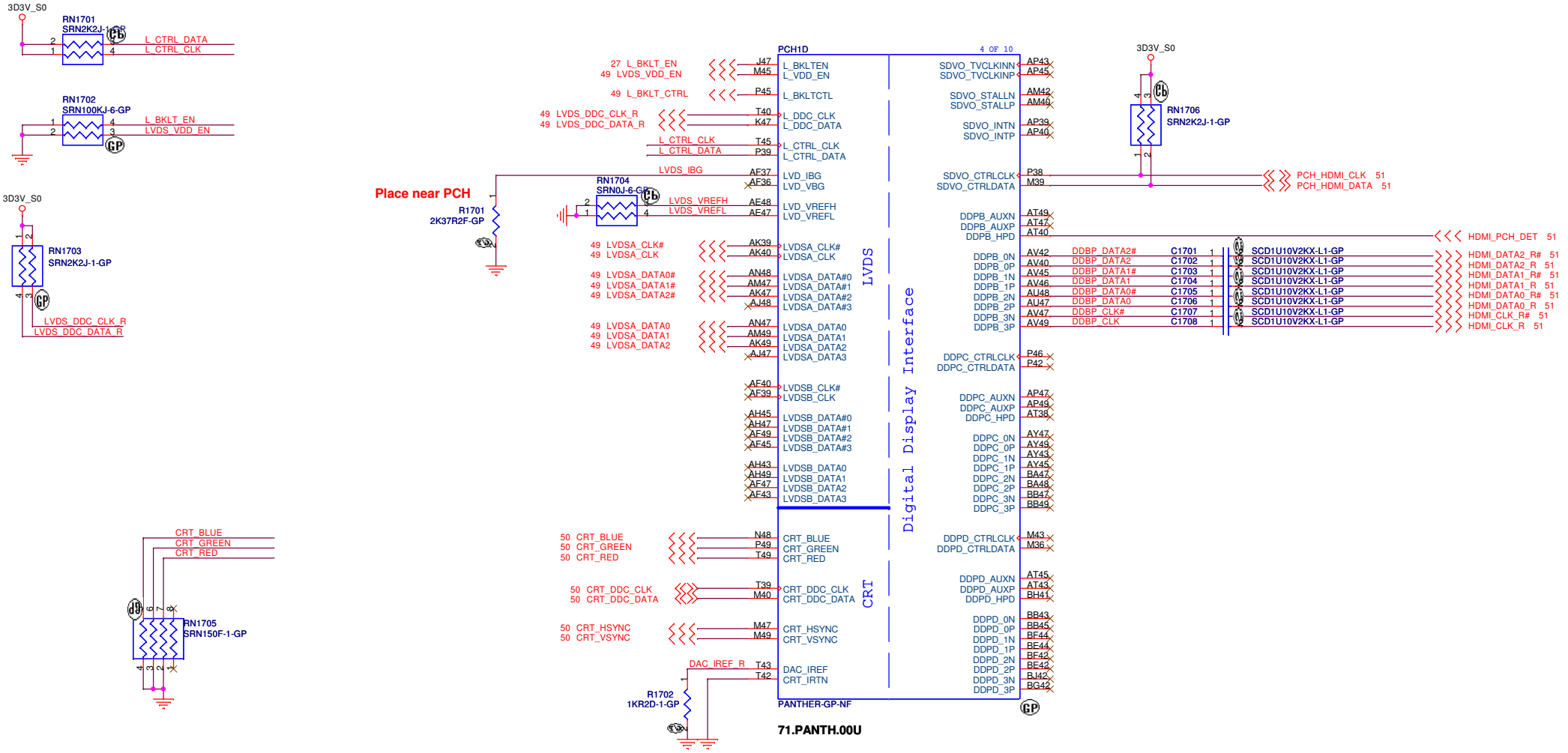

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緯創資通 Wistron Corporation
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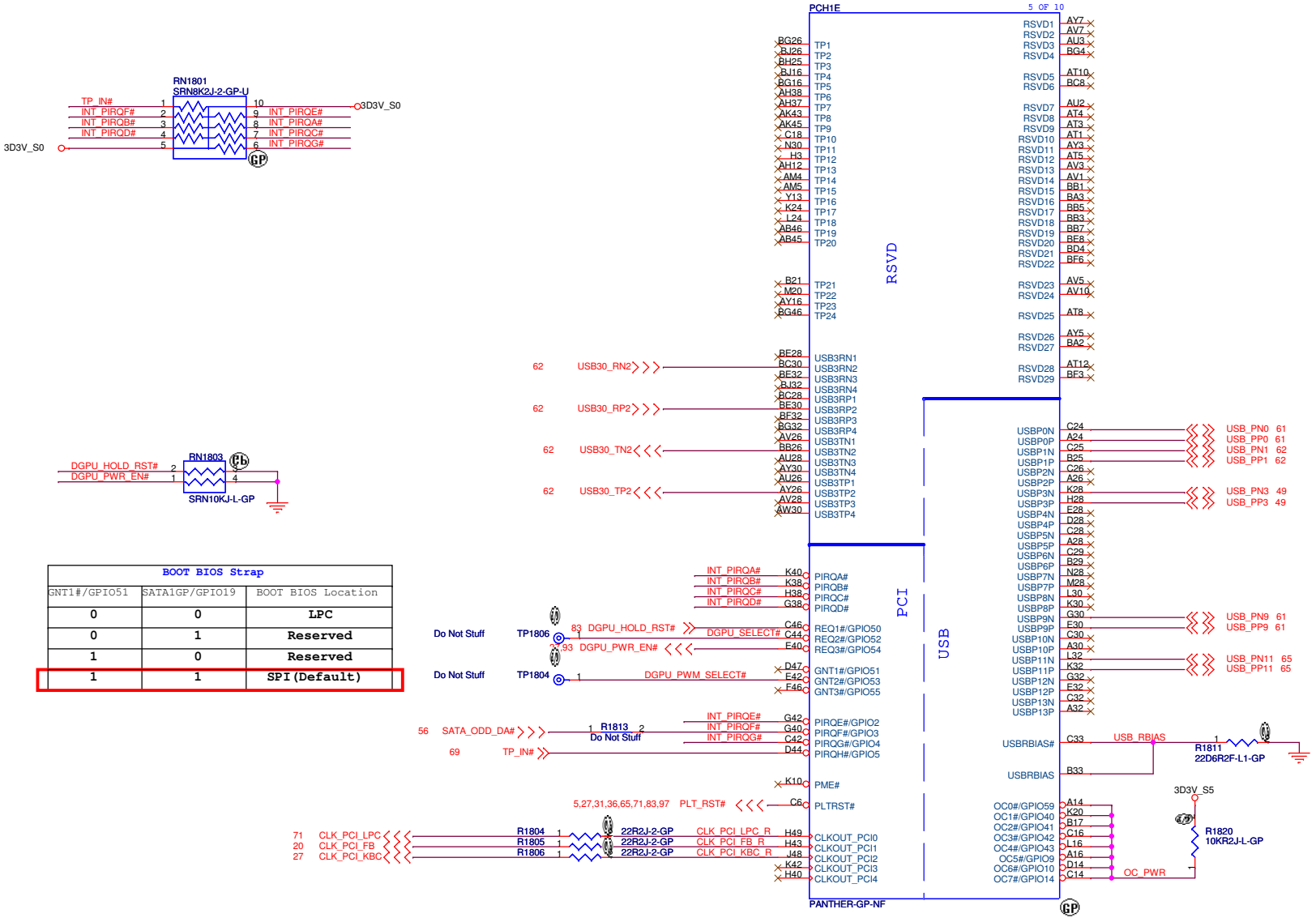
Title: PCH (LVDS/CRT/DDI)

Size	Document Number	Rev
A3	Husk/Petra	-1

Date: Monday, March 05, 2012 Sheet 17 of 103

SSID = PCH



BOOT BIOS Strap

GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI (Default)

USB Table

Pair	Device
0	USB2.0 Ext. port 1
1	USB3.0/USB2.0 Ext. port 2
2	
3	CCD
4	
5	
6	may not be available
7	may not be available
8	
9	USB2.0 Ext. port 3
10	
11	Mini Card1 (WLAN+BT)
12	
13	

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Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI/USB/NVRAM)

Size: Custom | Document Number: Husk/Petra | Rev: -1

Date: Monday, March 05, 2012 | Sheet 18 of 103

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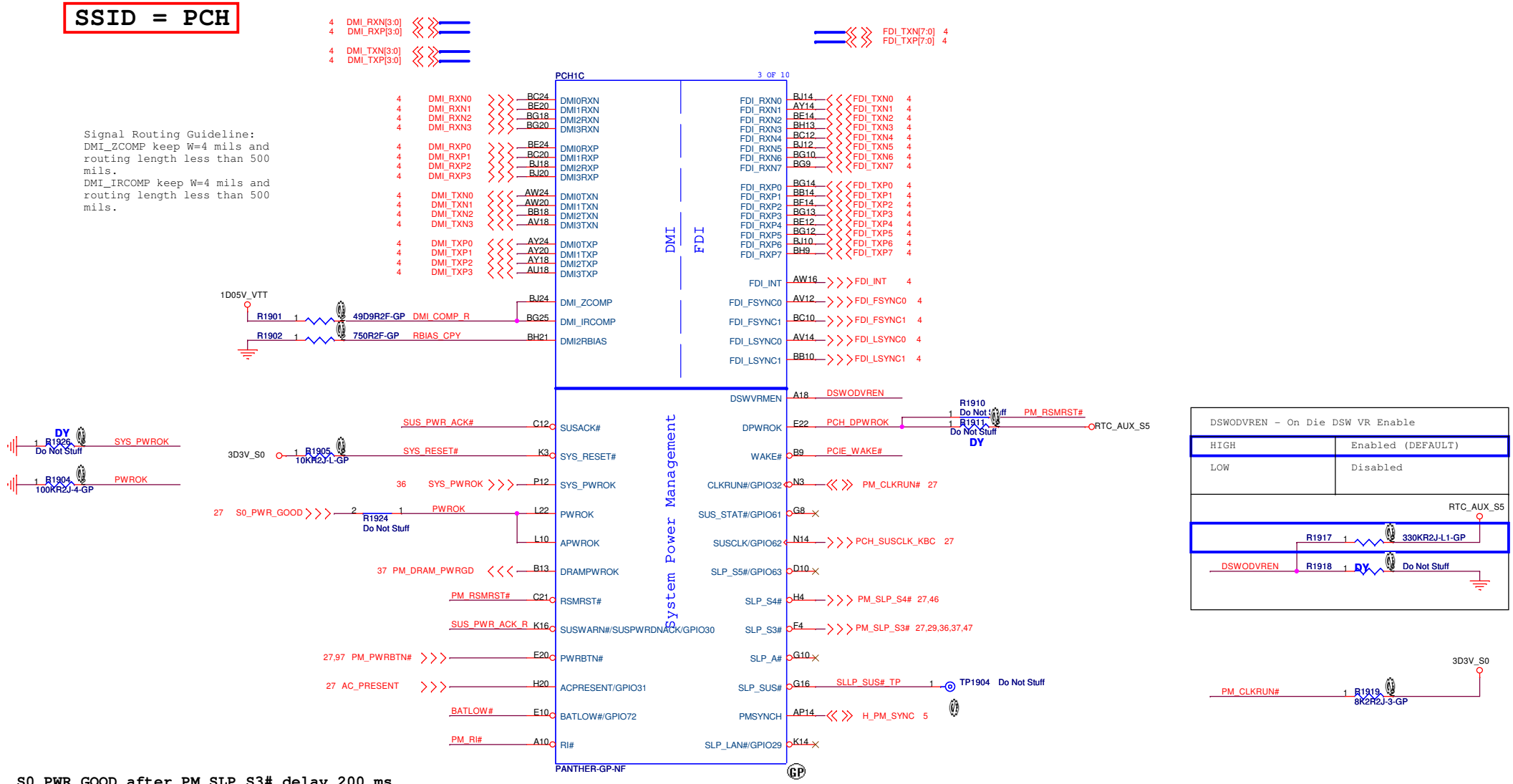
SSID = PCH

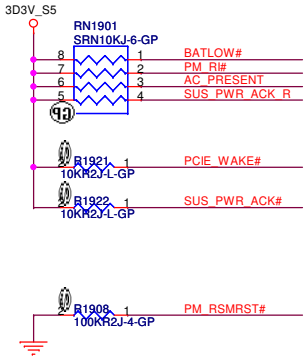
Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.

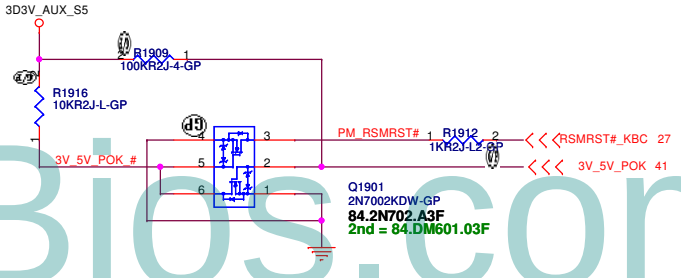


DSWODVREN - On Die DSW VR Enable

HIGH	Enabled (DEFAULT)
LOW	Disabled

S0_PWR_GOOD after PM_SLP_S3# delay 200 ms





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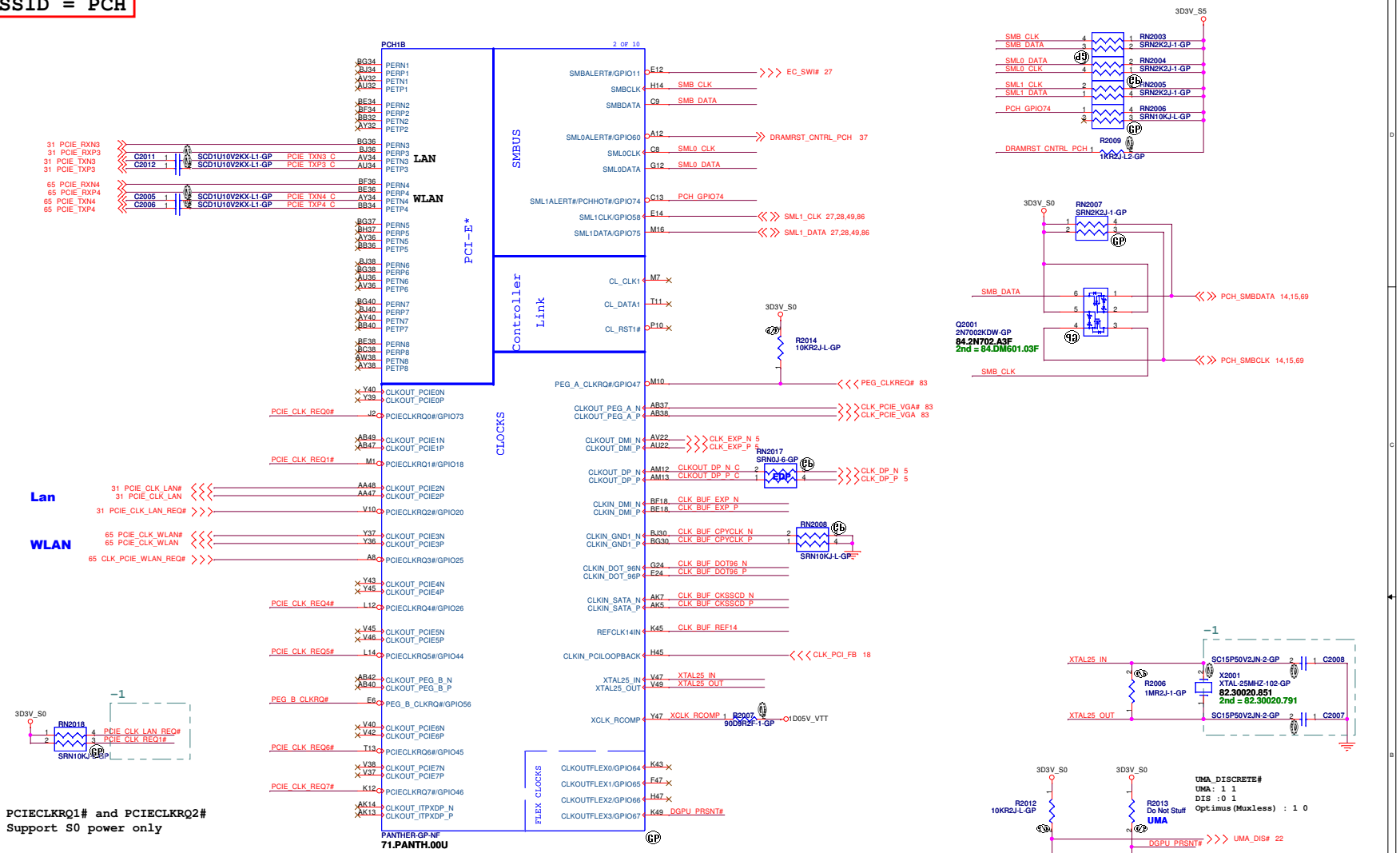
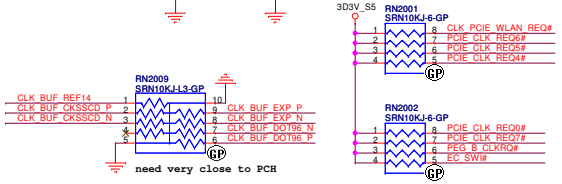
Title: PCH (DM I/FDI/PM)

Size: A3 | Document Number: Husk/Petra | Rev: -1

Date: Monday, March 05, 2012 | Sheet 19 of 103

SSID = PCH





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Title: PCH (PCI-E/SMBUS/CLOCK/CL)

Size: Custom | Document Number: Husk/Petra | Rev: -1

Date: Monday, March 05, 2012 | Sheet 20 of 103

SSID = PCH

RTC_AUX_S5 -1

R2115 20KR2F-L-GP
R2116 20KR2F-L-GP
C2103 SC1U16V3KX-5GP

INTVRMEN- Integrated SUS 1.05V VRM Enable
High - Enable internal VRs
Low - Enable external VRs

RTC_X1 — R2101 10MR2J-L-GP — RTC_X2
X2101 X-32D768KHZ-34GPU
82.30001.661
2nd = 82.30001.B21
C2101 SC6P50V2CN-1GP
C2102 SC6P50V2CN-1GP
-1

C2104 SC1U16V3KX-5GP
G2101 Do Not Stuff

RTC Reset

R2104 1MR2J-L-GP
R2105 330KR2F-L-GP
RTC_AUX_S5

27 RTCRST_ON — Q2102 2N7002K-2-GP — RTC_RST#
R2106 100KR2F-L1-GP
R2111 2KR2F-3-GP
84.2N702.J31
2ND = 84.2N702.031

PCH1A — 1 OF 10

RTC_X1	A20	RTCX1	RTC
RTC_X2	C20	RTCX2	
RTC_RST#	D20	RTCRST#	
SRTC_RST#	G22	SRTCRST#	
SM_INTRUDER#	K22	INTRUDER#	
PCH_INTVRMEN	C17	INTVRMEN	
HDA_BITCLK	N34	HDA_BCLK	IHDA
HDA_SYNC	L34	HDA_SYNC	
29 HDA_SPKR	T10	SPKR	
HDA_RST#	K34	HDA_RST#	
29 HDA_SDIN0	E34	HDA_SDIN0	
	G34	HDA_SDIN1	
	C34	HDA_SDIN2	
	A34	HDA_SDIN3	
27 ME_UNLOCK — R2107 1KR2J-L2-GP	A36	HDA_SDOUT	
	C36	HDA_DOCK_EN#/GPIO33	
	N32	HDA_DOCK_RST#/GPIO13	
R2121 4K7R2J-L-GP — PCH_JTAG_TCK_BUF	J3	JTAG_TCK	JTAG
	H7	JTAG_TMS	
	K5	JTAG_TDI	
	H1	JTAG_TDO	
27,60 SPI_CLK_R — R2108 33R2J-L1-GP — PCH_SPI_CLK	T3	SPI_CLK	SPI
27,60 SPI_CS0#_R — R2109 33R2J-L1-GP — PCH_SPI_CS0#	Y14	SPI_CS0#	
	T1	SPI_CS1#	
27,60 SPI_SI_R — R2110 33R2J-L1-GP — PCH_SPI_SI	V4	SPI_MOSI	
27,60 SPI_SO_R	U3	SPI_MISO	

	C38	FWH0/LAD0	LPC
	A38	FWH1/LAD1	
	B37	FWH2/LAD2	
	C37	FWH3/LAD3	
	D36	FWH4/LFRAME#	
	E36	LDRQ0#	
	K36	LDRQ1#/GPIO23	
	V5	SERIRQ	
	AM3	SATA0RXN	SATA 6G
	AM1	SATA0RXP	
	AP7	SATA0TXN	
	AP5	SATA0TXP	
	AM10	SATA1RXN	
	AM8	SATA1RXP	
	AP11	SATA1TXN	
	AP10	SATA1TXP	
	AD7	SATA2RXN	SATA
	AD5	SATA2RXP	
	AH5	SATA2TXN	
	AH4	SATA2TXP	
	AB8	SATA3RXN	
	AB10	SATA3RXP	
	AF3	SATA3TXN	
	AF1	SATA3TXP	
	Y7	SATA4RXN	
	Y5	SATA4RXP	
	AD3	SATA4TXN	
	AD1	SATA4TXP	
	Y3	SATA5RXN	
	Y1	SATA5RXP	
	AB3	SATA5TXN	
	AB1	SATA5TXP	
	Y11	SATAICOMPO	
	Y10	SATAICOMPI	
	AB12	SATA3RCOMPO	
	AB13	SATA3COMPI	
	AH1	SATA3RBIAS	
	P3	SATALED#	
	V14	SATA0GP/GPIO21	
	P1	SATA1GP/GPIO19	

PANTHER-GP-NF

71.PANTH.00U

LPC_AD[0..3] 27,71
LPC_AD0 LPC_AD1 LPC_AD2 LPC_AD3
LPC_FRAME# 27,71
INT_SERIRQ 27

HDD1
SATA_RXN0 56
SATA_RXP0 56
SATA_TXN0 56
SATA_TXP0 56

ODD
SATA_RXN4 56
SATA_RXP4 56
SATA_TXN4 56
SATA_TXP4 56

1D05V_VTT
SATA_COMP — R2112 37D4R2F-GP
1D05V_VTT
SATA3_COMP — R2113 49D9R2F-GP
RBIAS_SATA3 — R2114 750R2F-GP
SATA_LED#
SATA_DET#0

3D3V_S0
22 PSW_CLR#
RN2103 SRN10KJ-6-GP
SATA_LED#
INT_SERIRQ
SATA_DET#0

29 HDA_CODEC_SYNC — R2122 DY 1 Do Not Stuff — HDA_SYNC
29 HDA_CODEC_SDOUT — R2123 33R2J-L1-GP — HDA_SDOUT
29 HDA_CODEC_RST# — RN2102 SRN33J-5-GP-U — HDA_RST#
29 HDA_CODEC_BITCLK — HDA_BITCLK

Flash Descriptor Security Overide	
HDA_SDOUT	Low = Default High = Enable

+3VS_+1.5VS_HDA_IO — R2102 Do Not Stuff DY — HDA_SDOUT

PLL ODVR VOLTAGE	
HDA_SYNC	Low = 1.8V (Default) High = 1.5V

+3VS_+1.5VS_HDA_IO — R2103 1KR2J-L2-GP — HDA_SYNC

5V_S0 — Q2101 2N7002K-2-GP — HDA_SYNC_R — R2124 33R2J-L1-GP — HDA_SYNC
HDA_CODEC_SYNC
84.2N702.J31
2ND = 84.2N702.031

HDA_CODEC_BITCLK — EC2102 Do Not Stuff DY
HDA_CODEC_SDOUT — EC2103 Do Not Stuff DY
SPI_CS0#_R — EC2101 Do Not Stuff DY

HDA_SYNC: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.

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Title: PCH (SPI/RTC/LPC/SATA/IHDA)
Size: Custom | Document Number: Husk/Petra | Rev: -1
Date: Monday, March 05, 2012 | Sheet 21 of 103

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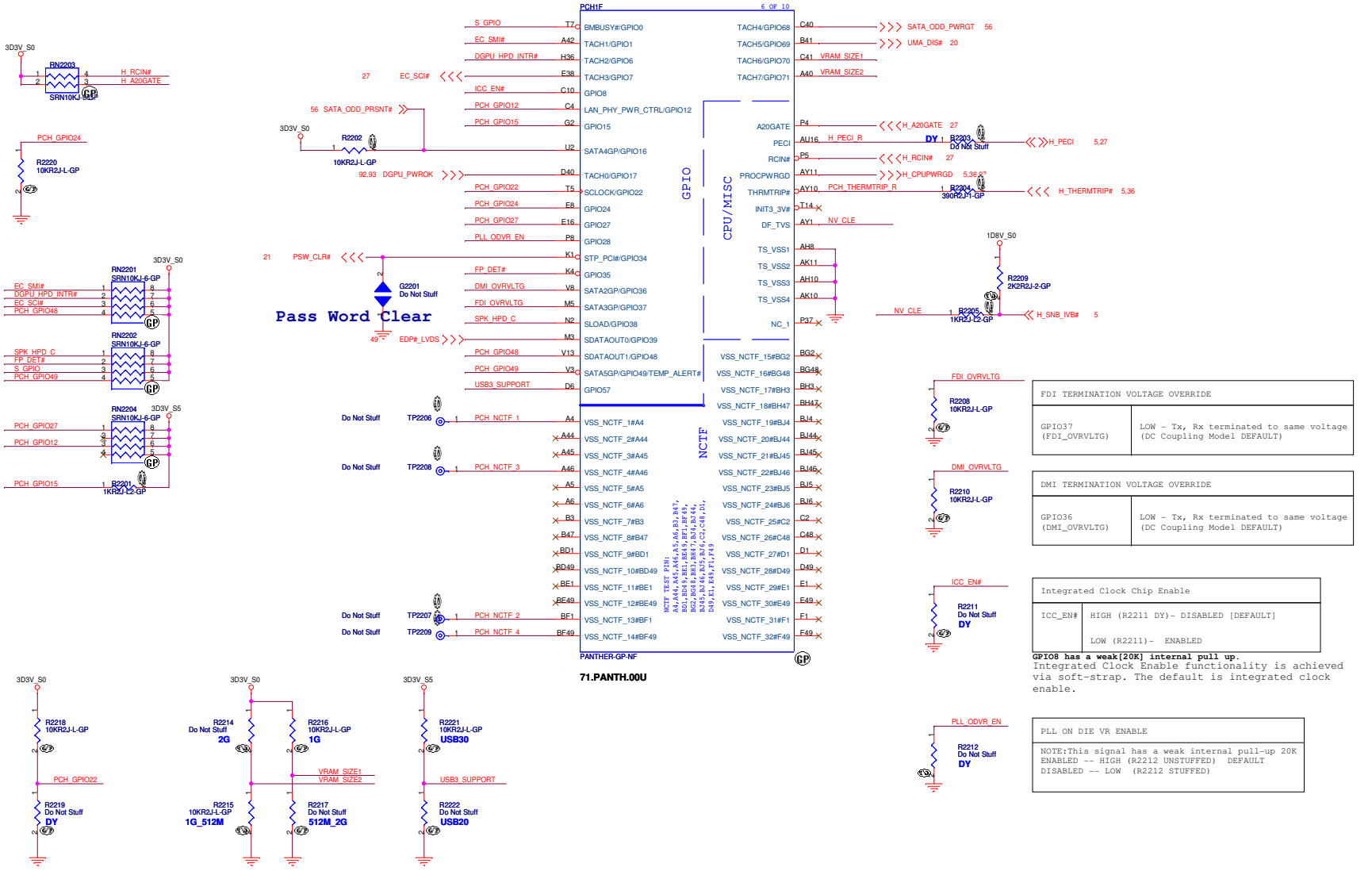
SSID = PCH



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Title: PCH (GPIO/CPU)

Size: Custom | Document Number: Husk/Petra | Rev: -1

Date: Monday, March 05, 2012 | Sheet 22 of 103

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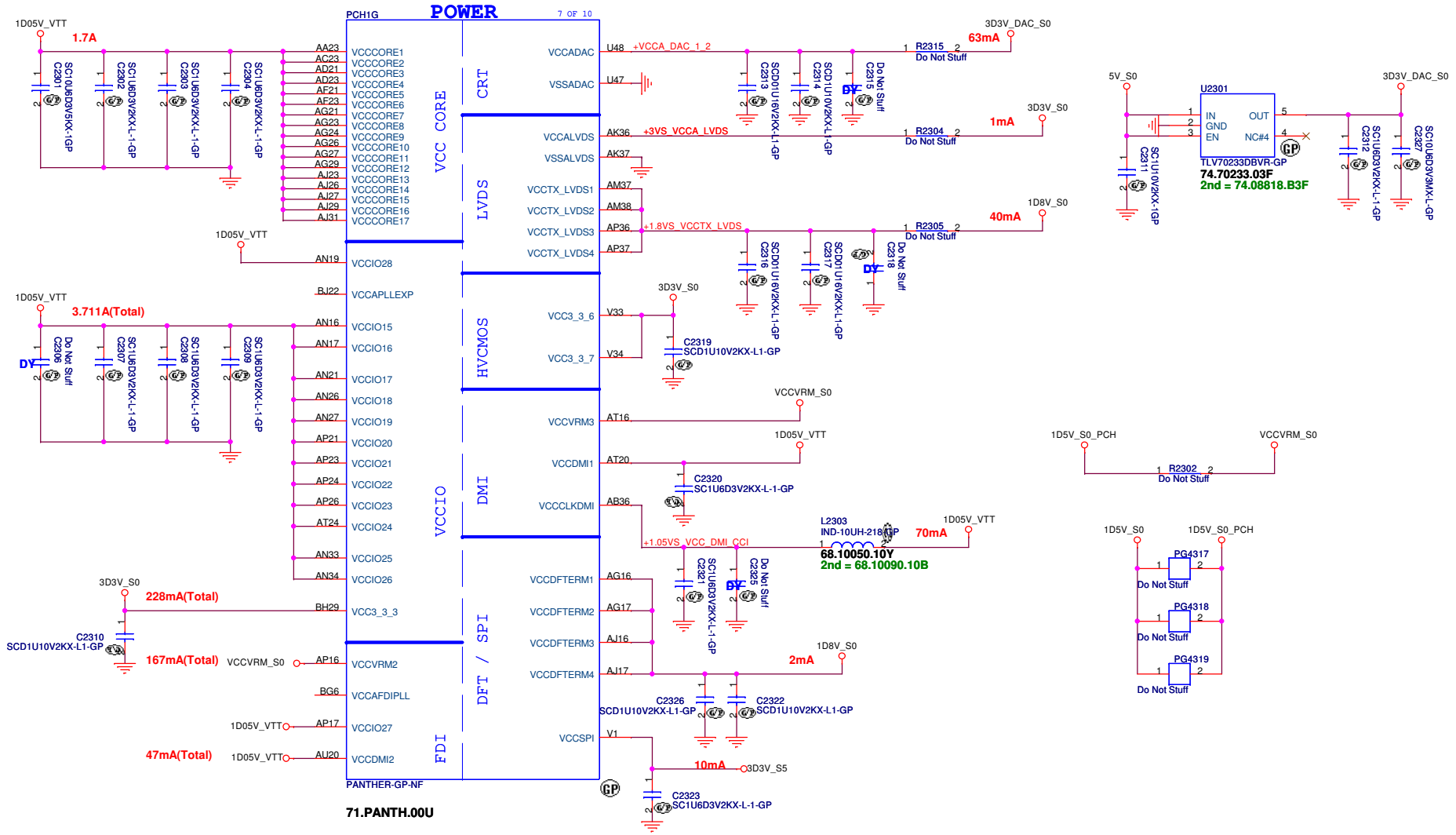
SSID = PCH



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Title: PCH (POWER1)

Size: A3 | Document Number: Husk/Petra | Rev: -1

Date: Monday, March 05, 2012 | Sheet 23 of 103

SSID = PCH

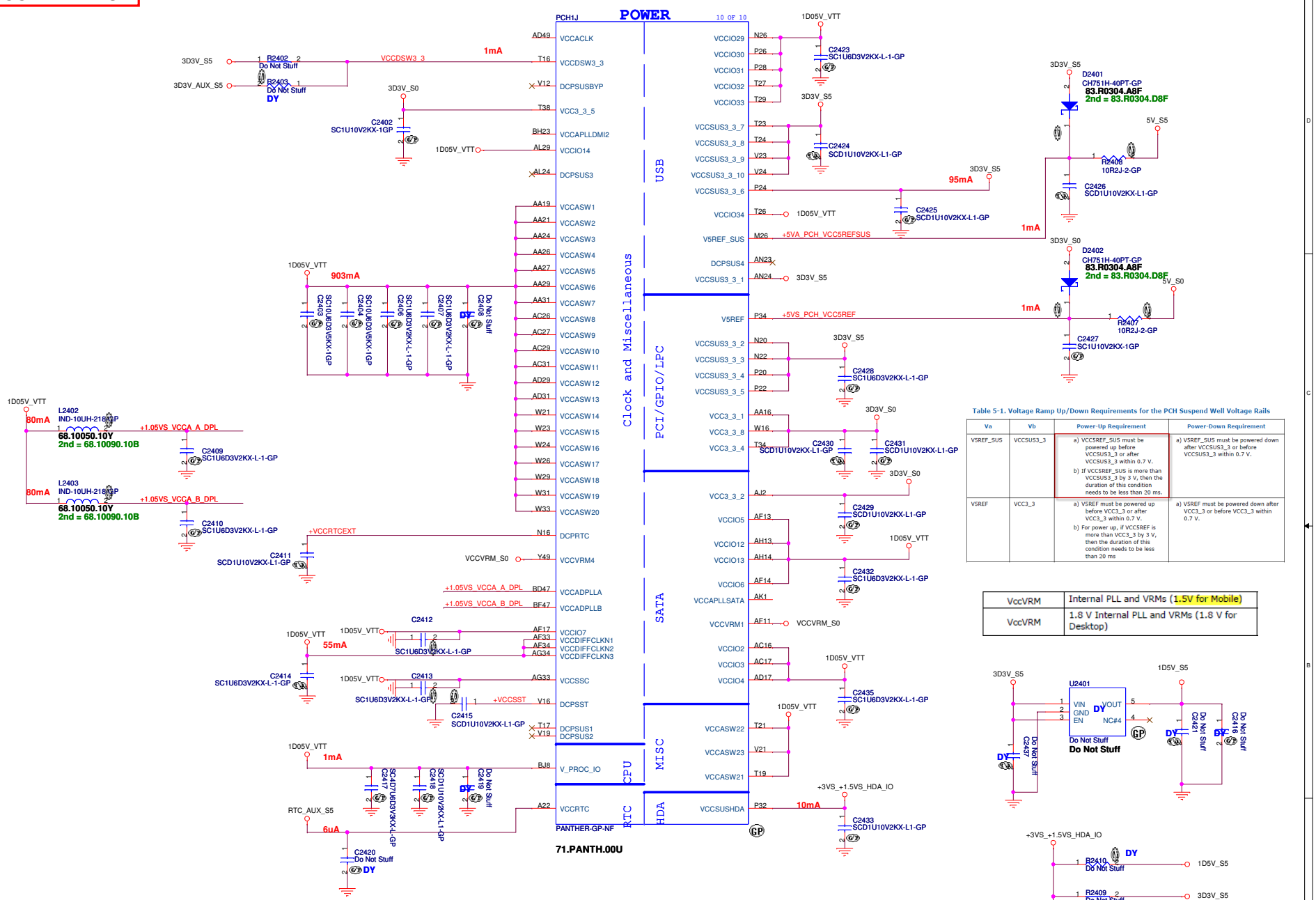

Table 5-1. Voltage Ramp Up/Down Requirements for the PCH Suspend Well Voltage Rails

Va	Vb	Power-Up Requirement	Power-Down Requirement
VSREF_SUS	VCCSUS3_3	a) VCC5REF_SUS must be powered up before VCCSUS3_3 or after VCCSUS3_3 within 0.7 V. b) If VCC5REF_SUS is more than VCCSUS3_3 by 3 V, then the duration of this condition needs to be less than 20 ms.	a) VSREF_SUS must be powered down after VCCSUS3_3 or before VCCSUS3_3 within 0.7 V.
VSREF	VCC3_3	a) VSREF must be powered up before VCC3_3 or after VCC3_3 within 0.7 V. b) For power up, if VCC5REF is more than VCC3_3 by 3 V, then the duration of this condition needs to be less than 20 ms	a) VSREF must be powered down after VCC3_3 or before VCC3_3 within 0.7 V.

VccVRM	Internal PLL and VRMs (1.5V for Mobile)
VccVRM	1.8 V Internal PLL and VRMs (1.8 V for Desktop)

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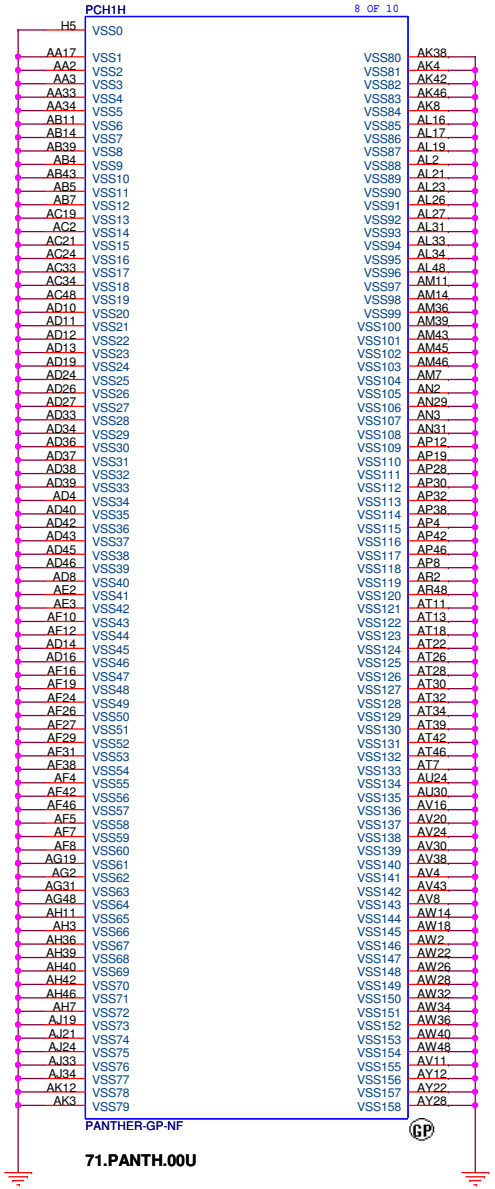
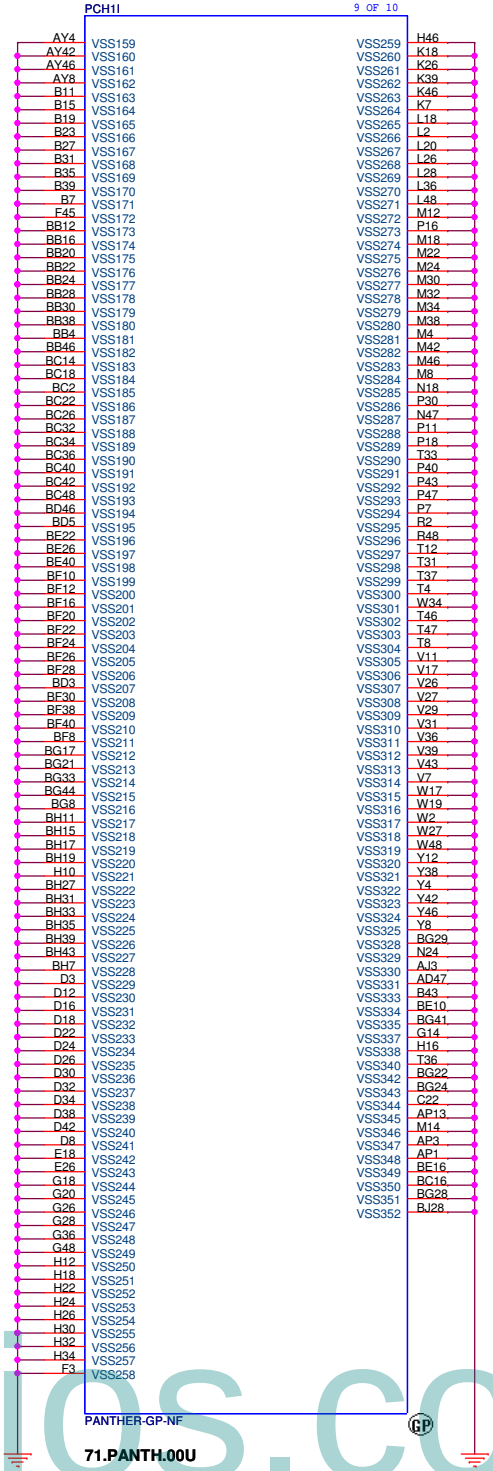
Title: PCH (POWER2)

Size: Custom | Document Number: Husk/Petra | Rev: -1

Date: Monday, March 05, 2012 | Sheet 24 of 103

SSID = PCH





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Title: ***PCH (VSS)***

Size	Document Number	Rev
A3	**Husk/Petra**	-1

Date: Monday, March 05, 2012 Sheet 25 of 103

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Title: ***Clock(colay)***

Size	Document Number	Rev
A4	**Husk/Petra**	-1

Date: Monday, March 05, 2012 Sheet 26 of 103

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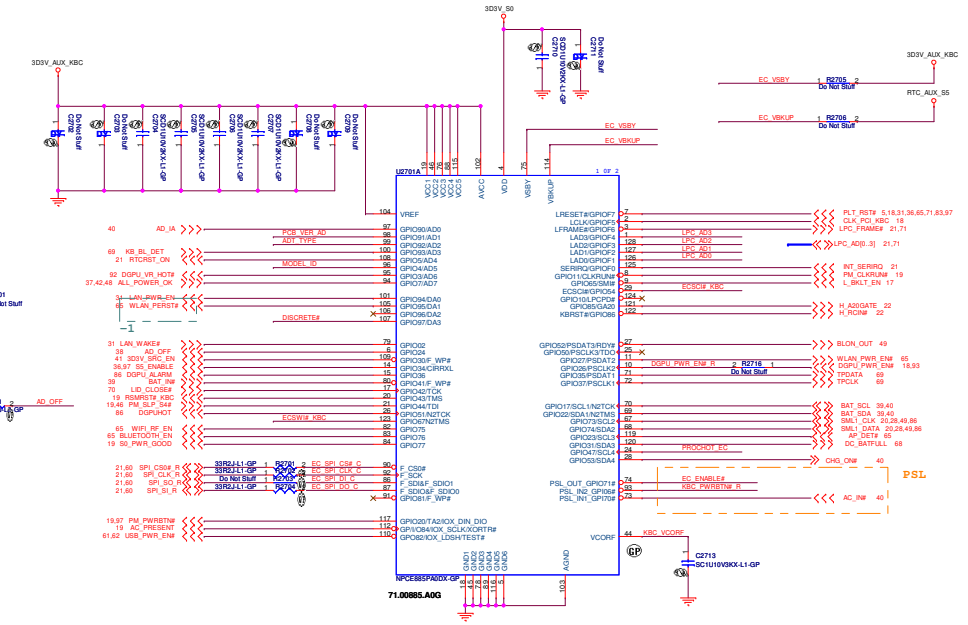
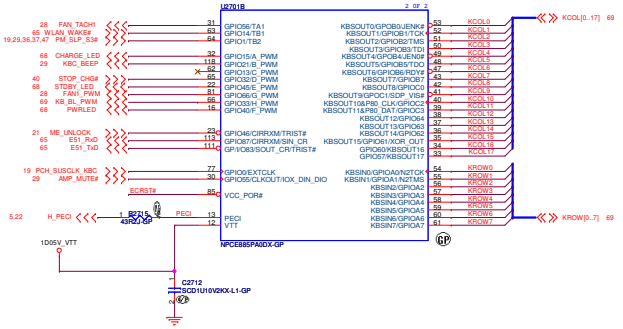
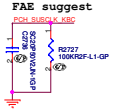
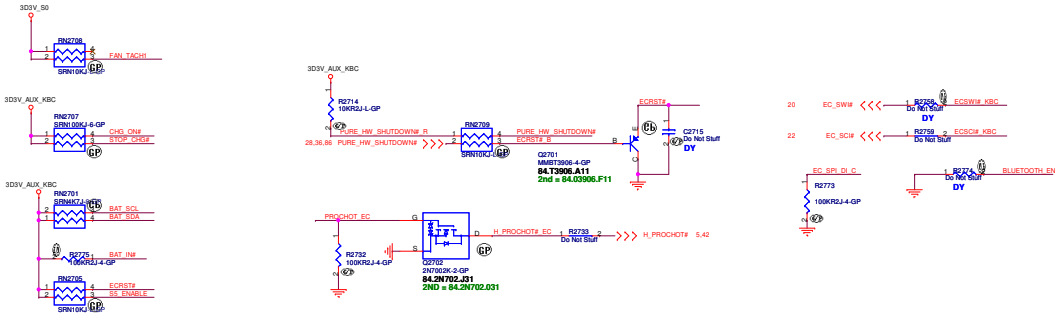
SSID = KBC



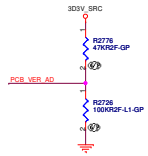


FAE suggest



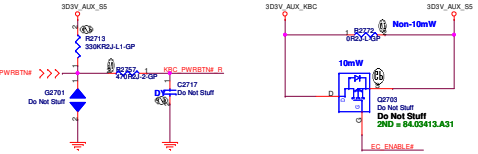


PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.48V
-1	100.0K	47.0K	2.24V
-1M	100.0K	64.9K	2.0V
-2	100.0K	76.8	1.87V
-3	100.0K	100K	1.65V
-3M	100.0K	143.0K	1.358V
-1M For PCH B3	100.0K	174.0K	1.204V
		64.17435.6DL	
-4	100.0K	215.0K	1.047V

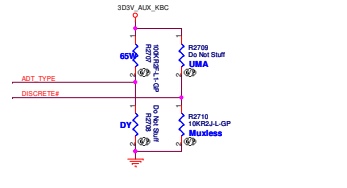


ADT_TYPE A/D(PIN99)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
65W	N/A	100.0K	3.3V
90W	100.0K	N/A	0V
30W	10.0K	100.0K	0.3V
40W	20.0K	100.0K	0.55V
120W	33.0K	100.0K	0.82V
Reserved	47.0K	100.0K	1.06V
Reserved	64.9K	100.0K	1.3V

PSL Function

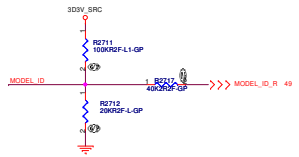


Inputs			Output
PSL_IN1_GPI70	PSL_IN2_GPI06	Bit 1 of P7DOUT Register	PSL_OUT_GPIO71
Low	X	X	Low
High	High-to-Low	X	Low
High	X	0-to-1	High



PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	SERIES RESISTOR	VOLTAGE
14"(AMD)	30K	100K	40.2K	0.7615
15"(AMD)	30K	100K	40.2K	0.4838
14"(NV)	20K	100K	40.2K	0.55
15"(NV)	20K	100K	40.2K	0.3888

pin 5 is NC, the model is 14"
pin 5 is GND, the model is 15"



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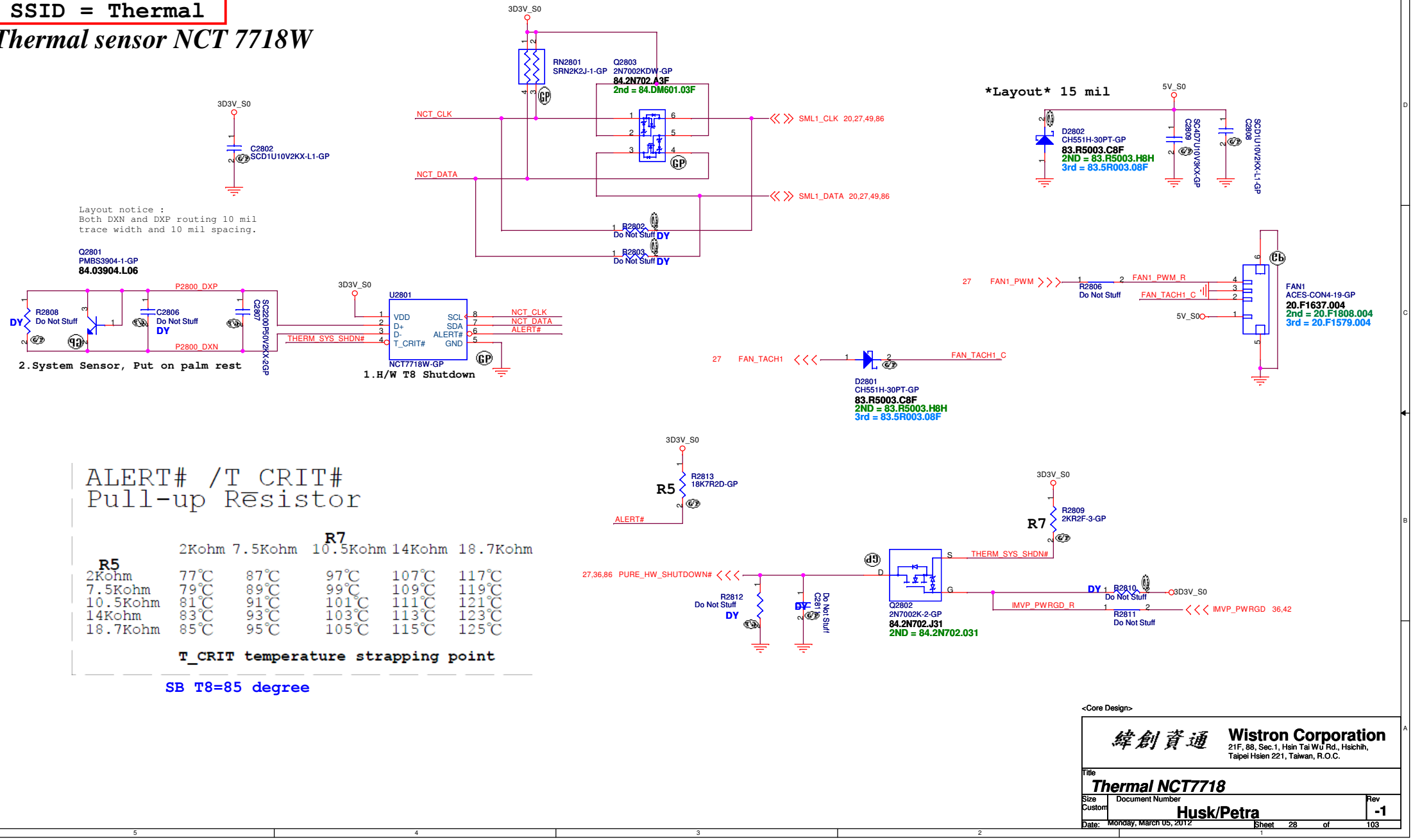
Title: KBC NPCE885
Size: Custom | Document Number: Husk/Petra | Rev: -1
Date: Monday, March 05, 2012 | Sheet 27 of 103

SSID = Thermal

Thermal sensor NCT 7718W



ALERT# /T_CRIT# Pull-up Resistor

R5 \ R7	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
2Kohm	77℃	87℃	97℃	107℃	117℃
7.5Kohm	79℃	89℃	99℃	109℃	119℃
10.5Kohm	81℃	91℃	101℃	111℃	121℃
14Kohm	83℃	93℃	103℃	113℃	123℃
18.7Kohm	85℃	95℃	105℃	115℃	125℃

T_CRIT temperature strapping point

SB T8=85 degree

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: *Thermal NCT7718*

Size: Custom | Document Number: Husk/Petra | Rev: -1

Date: Monday, March 05, 2012 | Sheet 28 of 103

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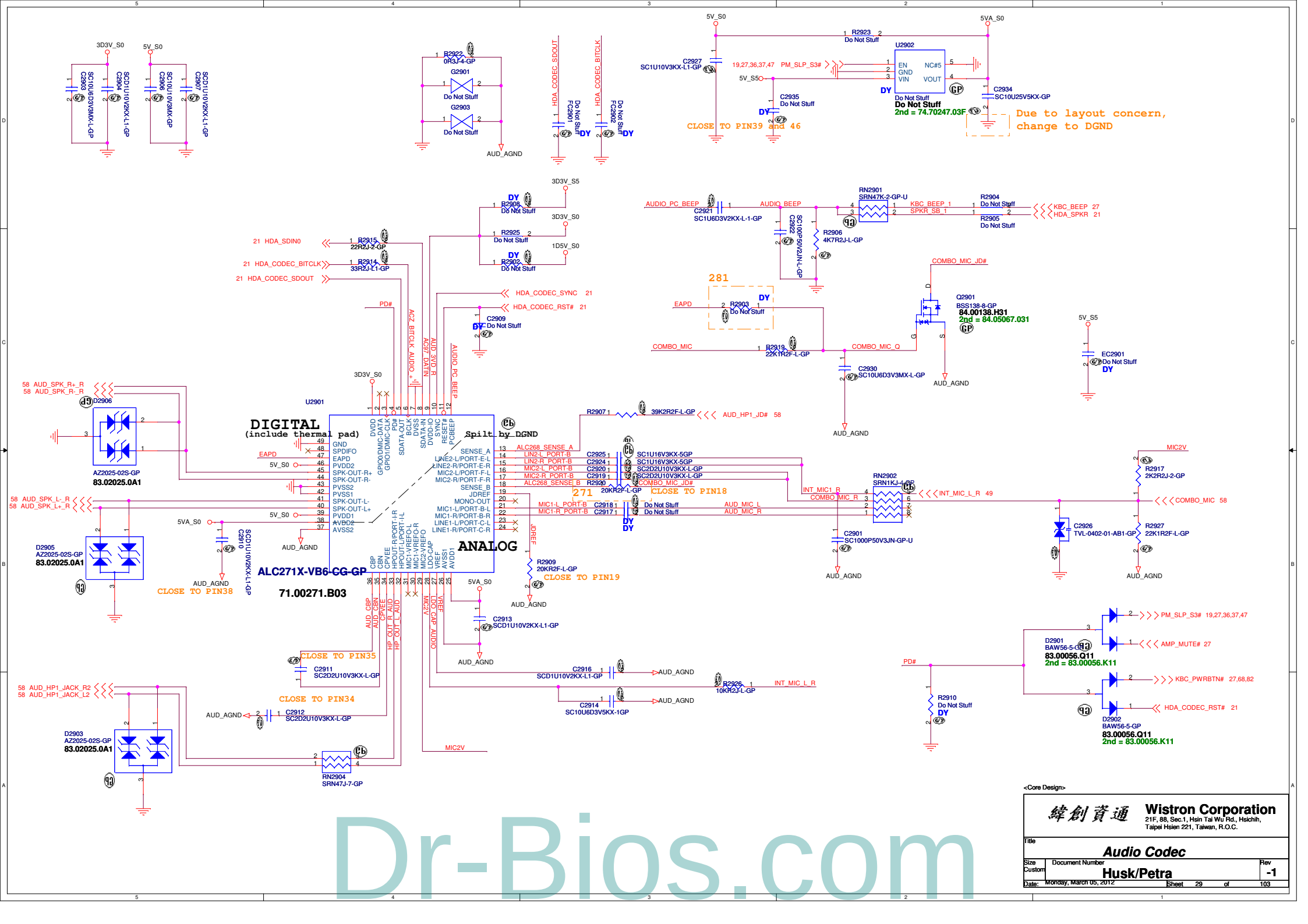
DIGITAL
(include thermal pad)
Spilt by DGND
ANALOG
ALC271X-VB6-CG-GP
71.00271.B03
U2901
U2902
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Audio Codec
Husk/Petra
-1
Monday, March 05, 2012
Sheet 29 of 103
Due to layout concern, change to DGND
CLOSE TO PIN39 and 46
CLOSE TO PIN38
CLOSE TO PIN35
CLOSE TO PIN34
CLOSE TO PIN18
CLOSE TO PIN19
Dr-Bios.com

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<Core Design>

緯創資通 **Wistron Corporation**

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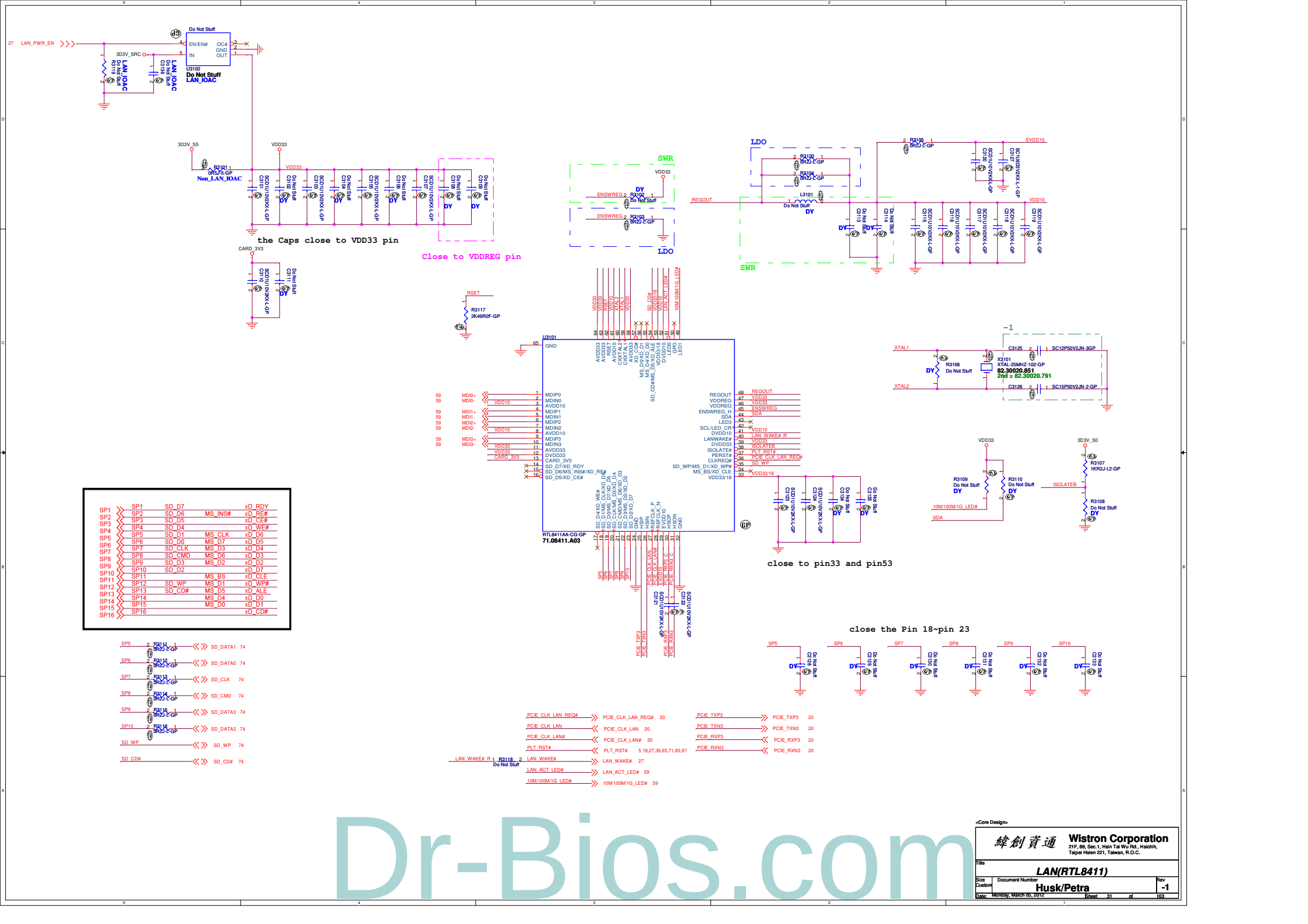
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Audio AMP***

Size	Document Number	Rev
A3	Husk/Petra	-1

Date: Monday, March 05, 2012 Sheet 30 of 103



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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN(RTL8411)

Size: Custom | Document Number: Husk/Petra | Rev: -1

Date: Monday, March 05, 2012 | Sheet 31 of 103

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***RTS5159 (CARD READER)***

Size	Document Number	Rev
Custom	**Husk/Petra**	**-1**

Date: Monday, March 05, 2012 Sheet 32 of 103

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(Blanking)

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	Husk/Petra	-1

Date: Monday, March 05, 2012 Sheet 33 of 103

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(Blanking)

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	Husk/Petra	-1

Date: Monday, March 05, 2012 Sheet 34 of 103

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
USB 3.0 Controller

Size	Document Number	Rev
Custom	**Husk/Petra**	-1

Date: Monday, March 05, 2012 Sheet 35 of 103

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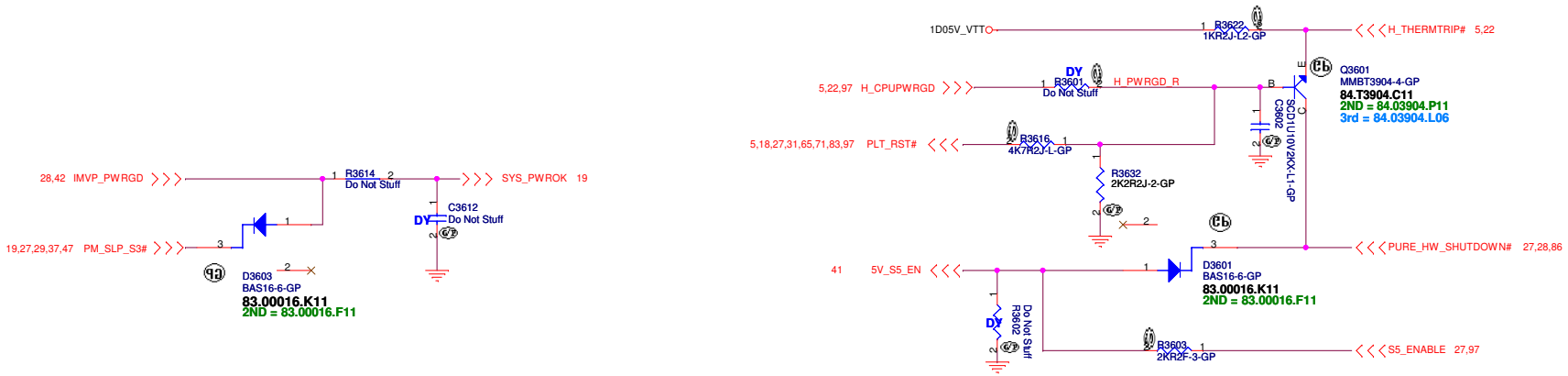
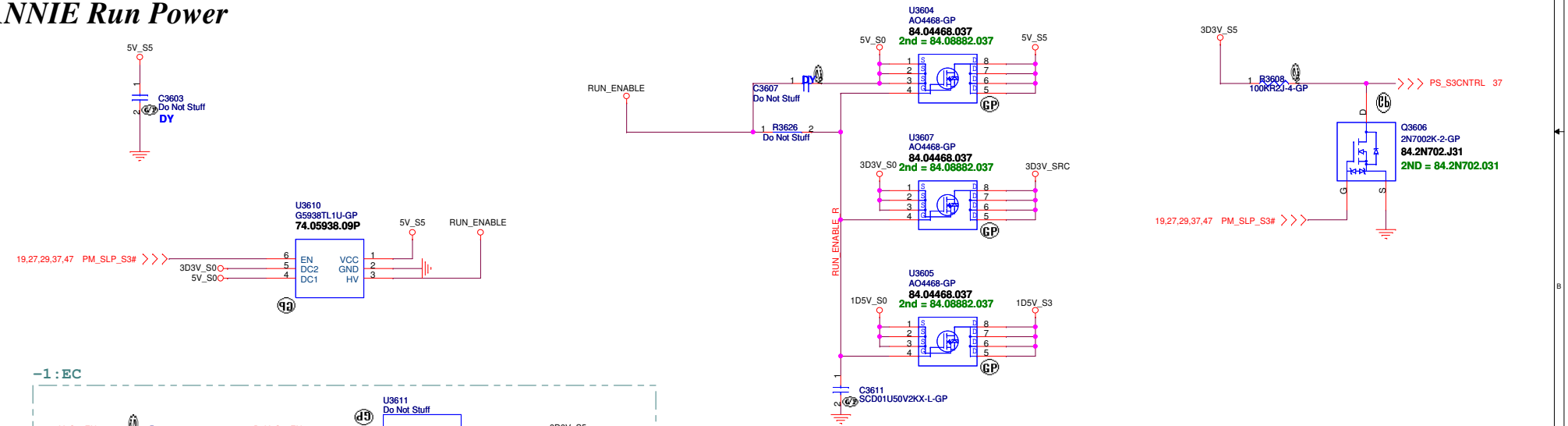
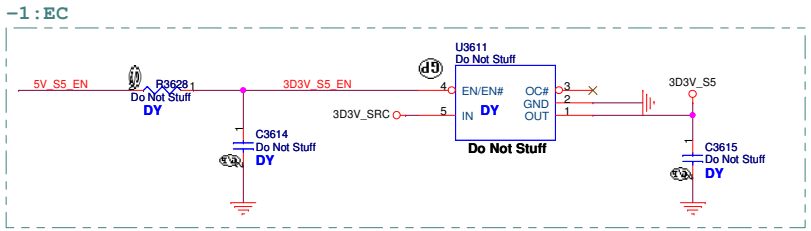
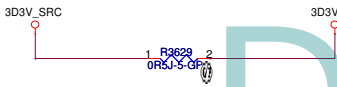
Power Sequence



ANNIE Run Power







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<Core Design>

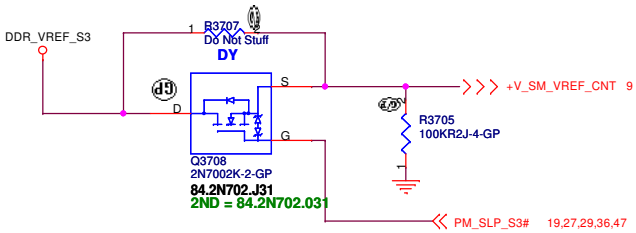
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

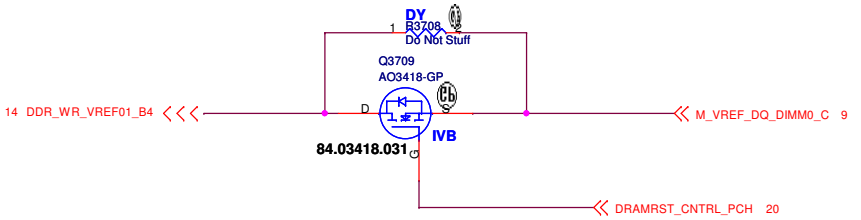
Title: Power Plane Enable

Size: Custom | Document Number: Husk/Petra | Rev: -1

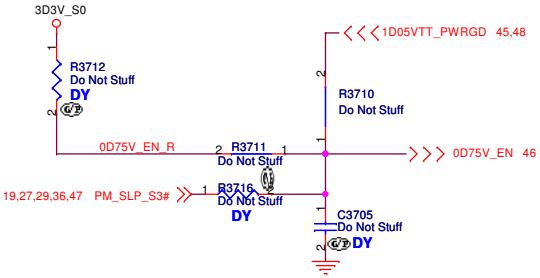
Date: Wednesday, March 07, 2012 | Sheet 36 of 103

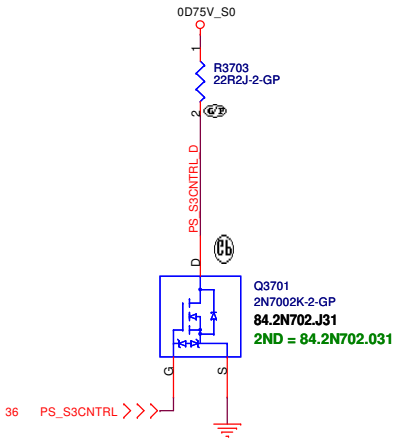
Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation

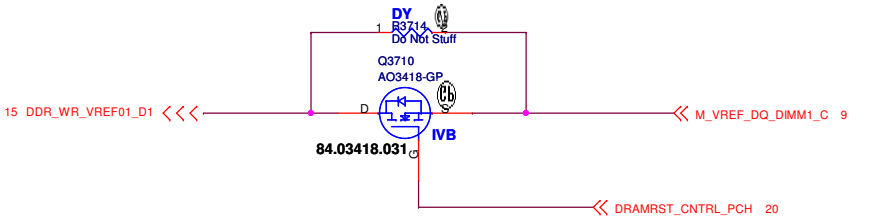




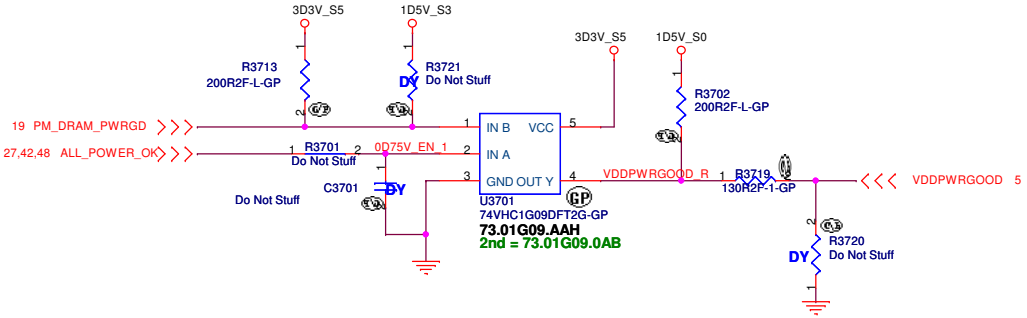
Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK



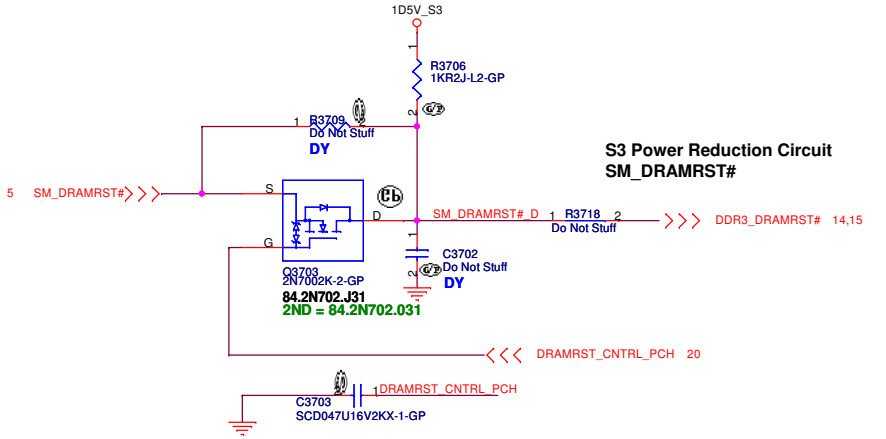




Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



S3 Power Reduction Circuit
SM_DRAMRST#

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ADAPTER

Size: A3 | Document Number: Husk/Petra | Rev: -1

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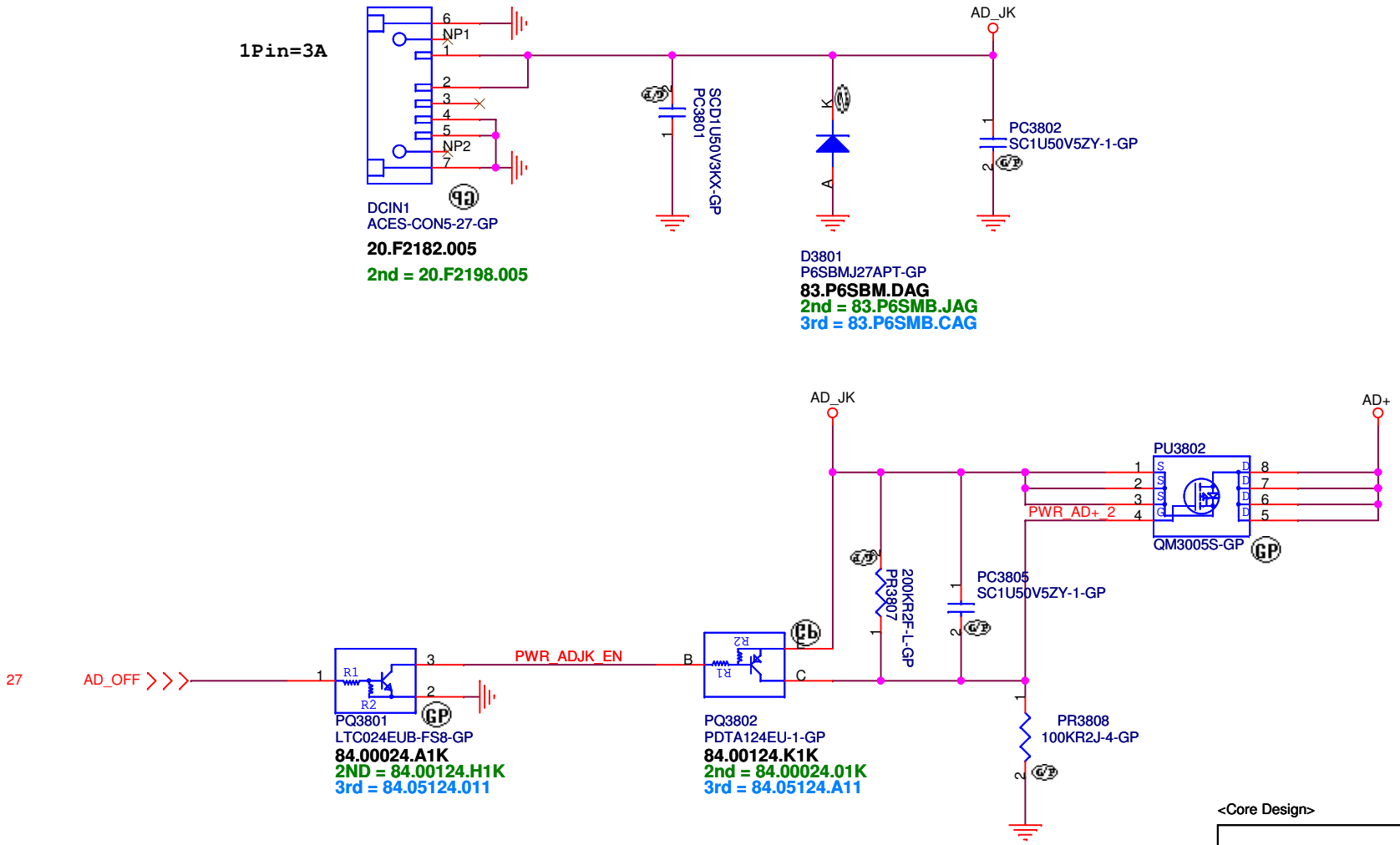

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DCIN JACK**

Size: A4 | Document Number: **Husk/Petra** | Rev: **-1**

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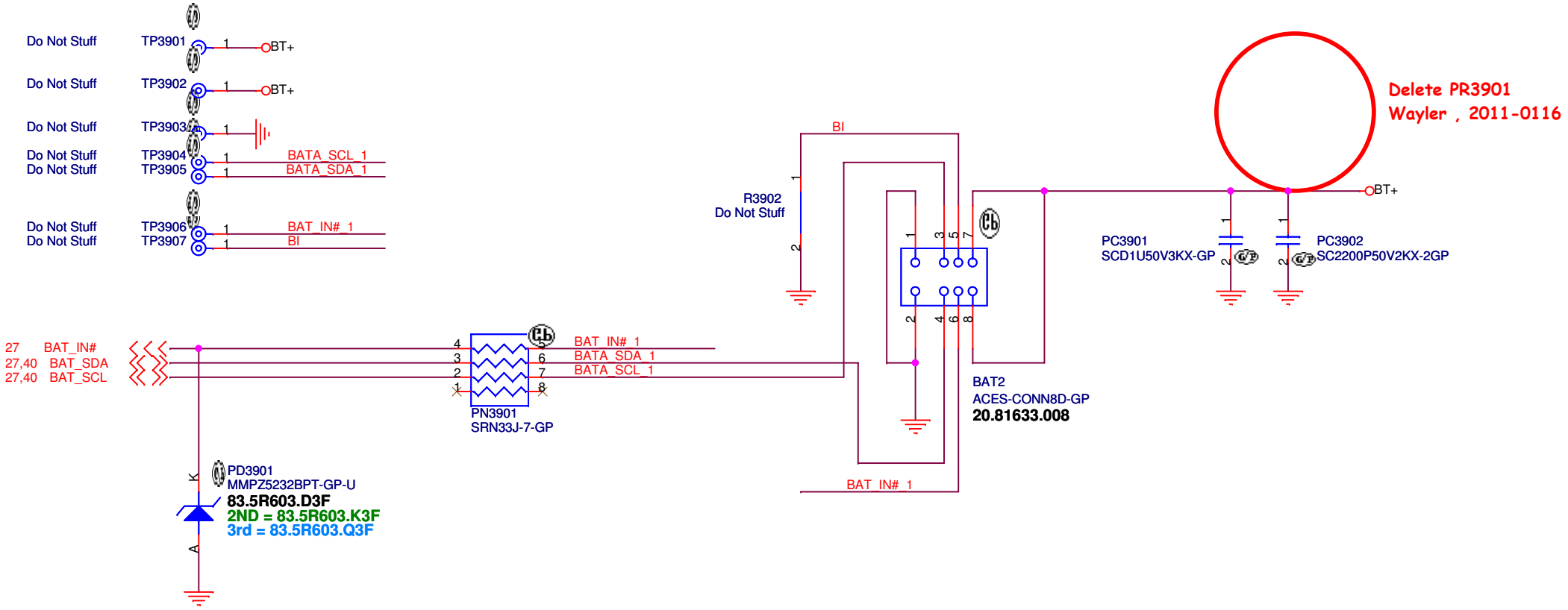
BATTERY CONNECTOR



<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***BATT CONN***	
Size A4	Document Number **Husk/Petra**	Rev **-1**
Date: Monday, March 05, 2012	Sheet 39 of 103	

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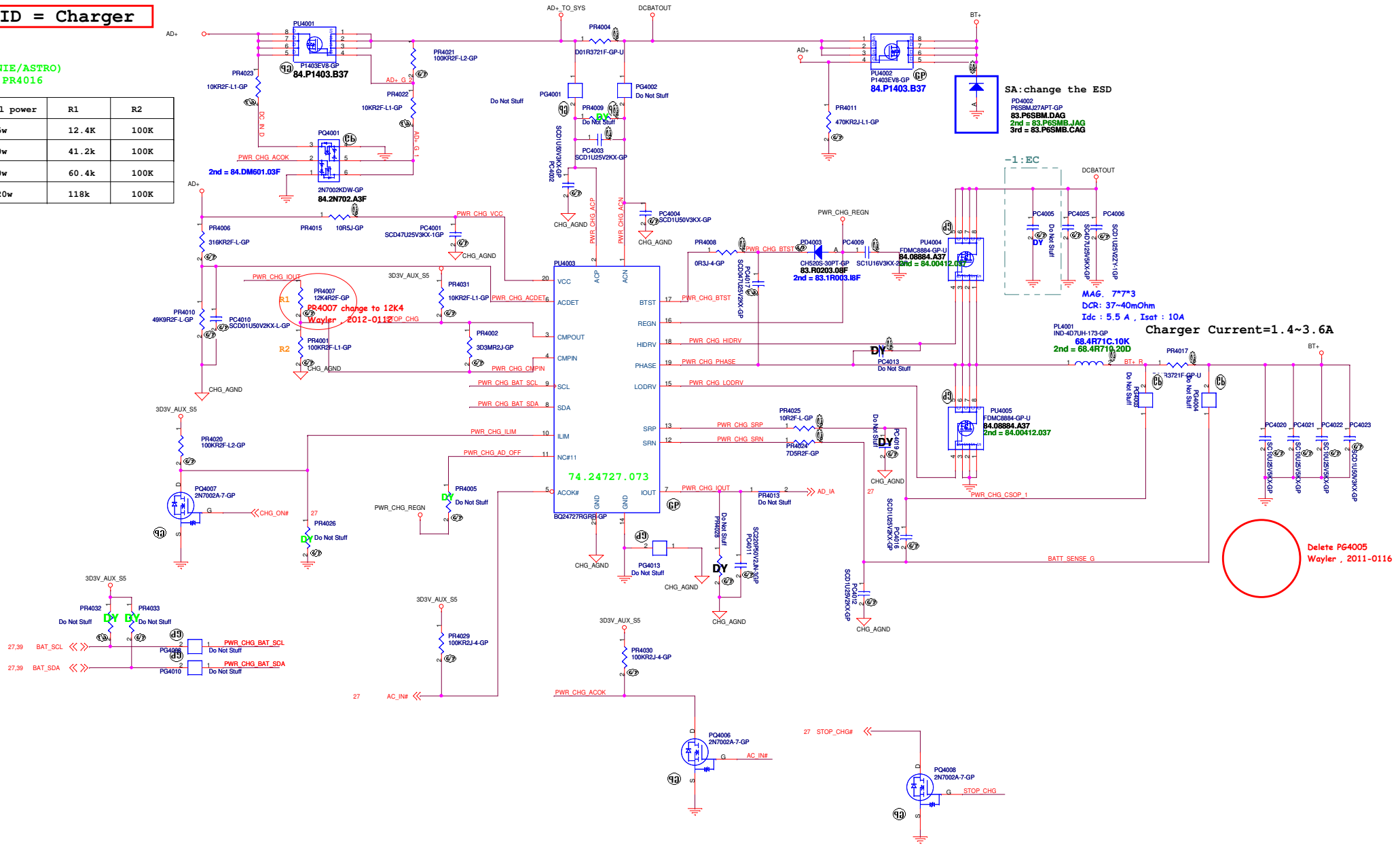
SSID = Charger

A8 (ANNIE/ASTRO)
PR4014,PR4016

AD+ total power	R1	R2
65w	12.4K	100K
80w	41.2k	100K
90w	60.4k	100K
120w	118k	100K



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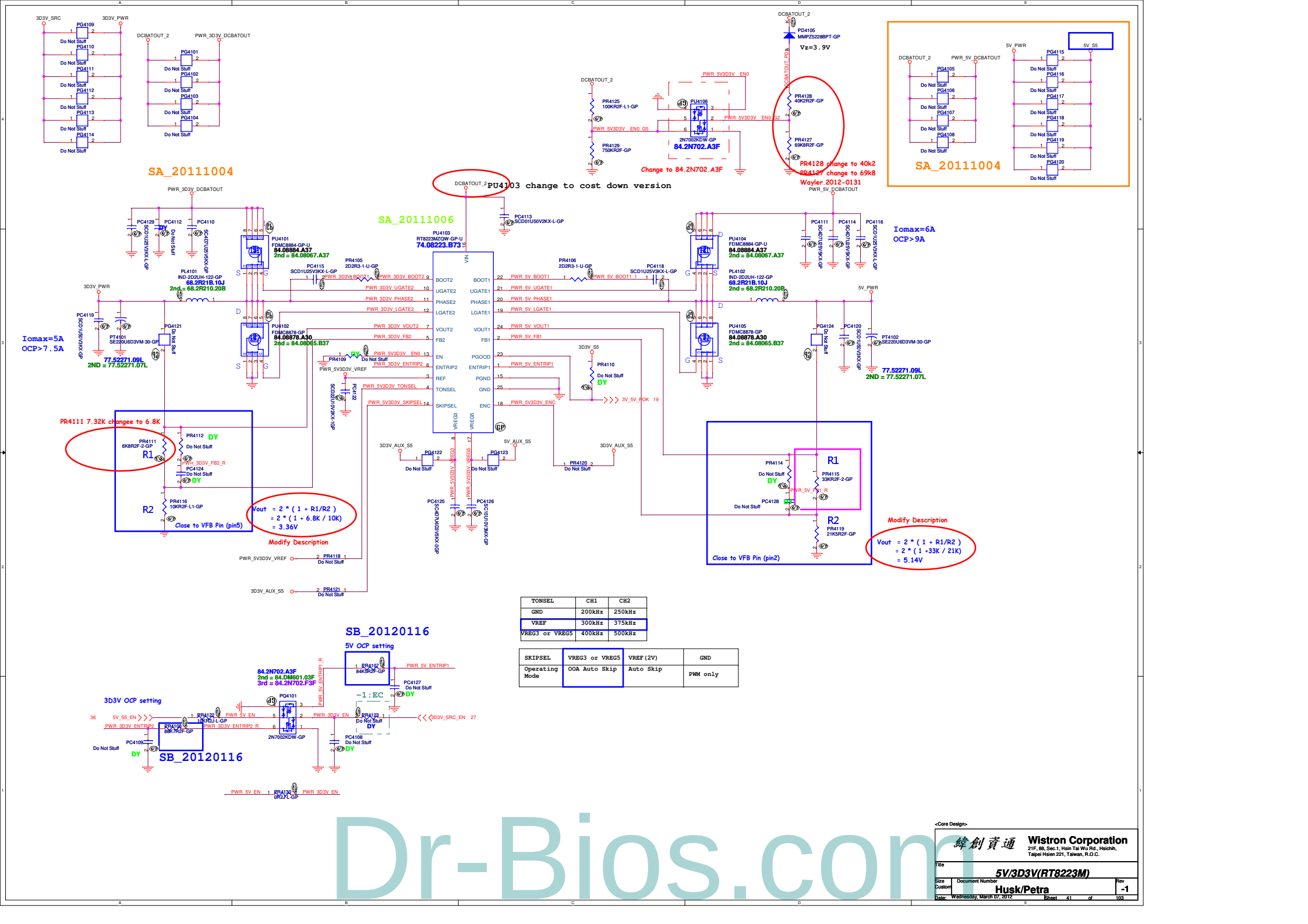
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER BQ24707A

Size: Custom | Document Number: Husk/Petra | Rev: -1

Date: Tuesday, March 06, 2012 | Sheet 40 of 108



TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3 or VREG5	400kHz	500kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

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<Core Design>

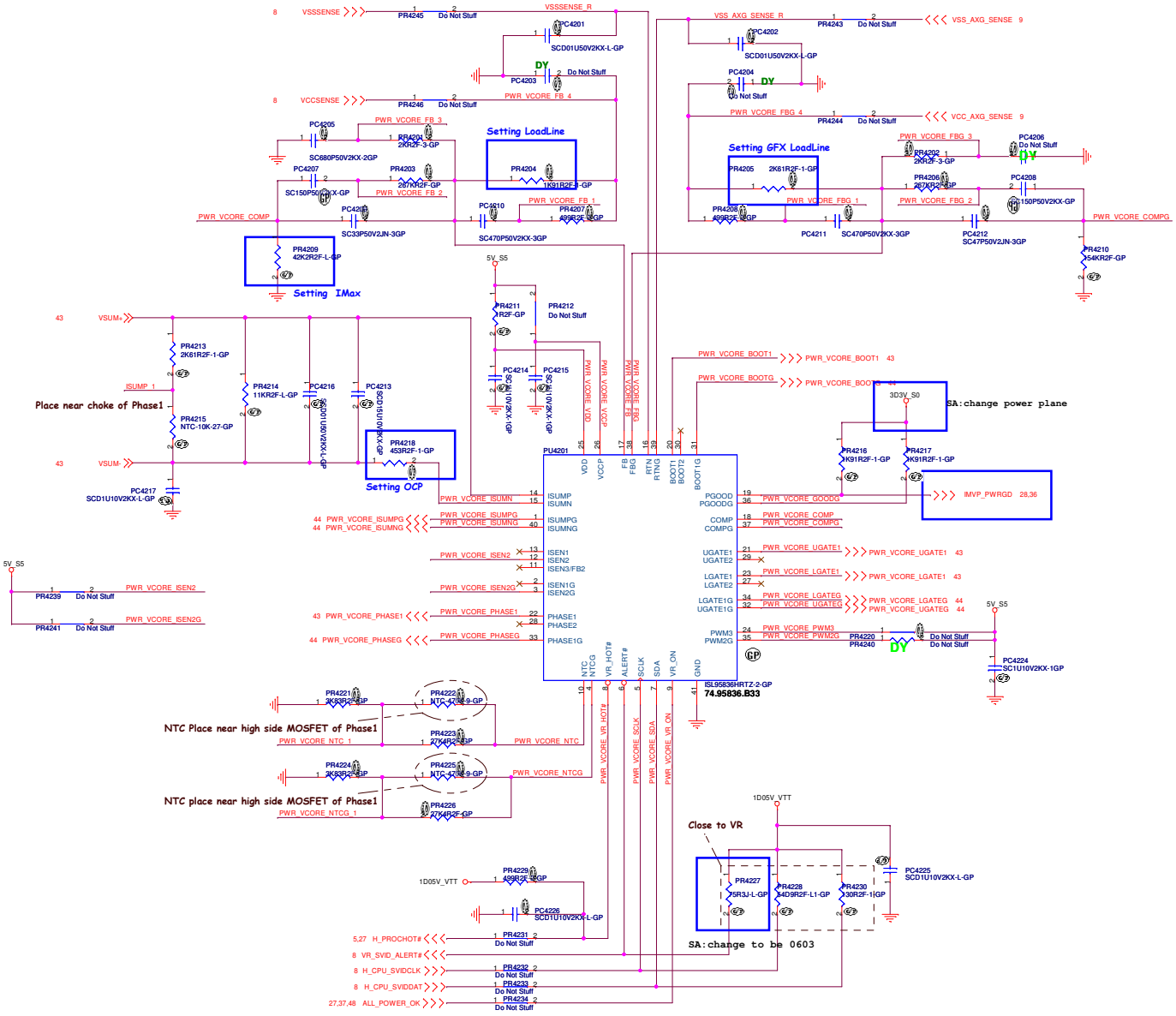
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 5V/3D3V(RT8223M)

Size: Custom | Document Number: Husk/Petra | Rev: -1

Date: Wednesday, March 07, 2012 | Sheet 41 of 103

SSID = CPU.Regulator



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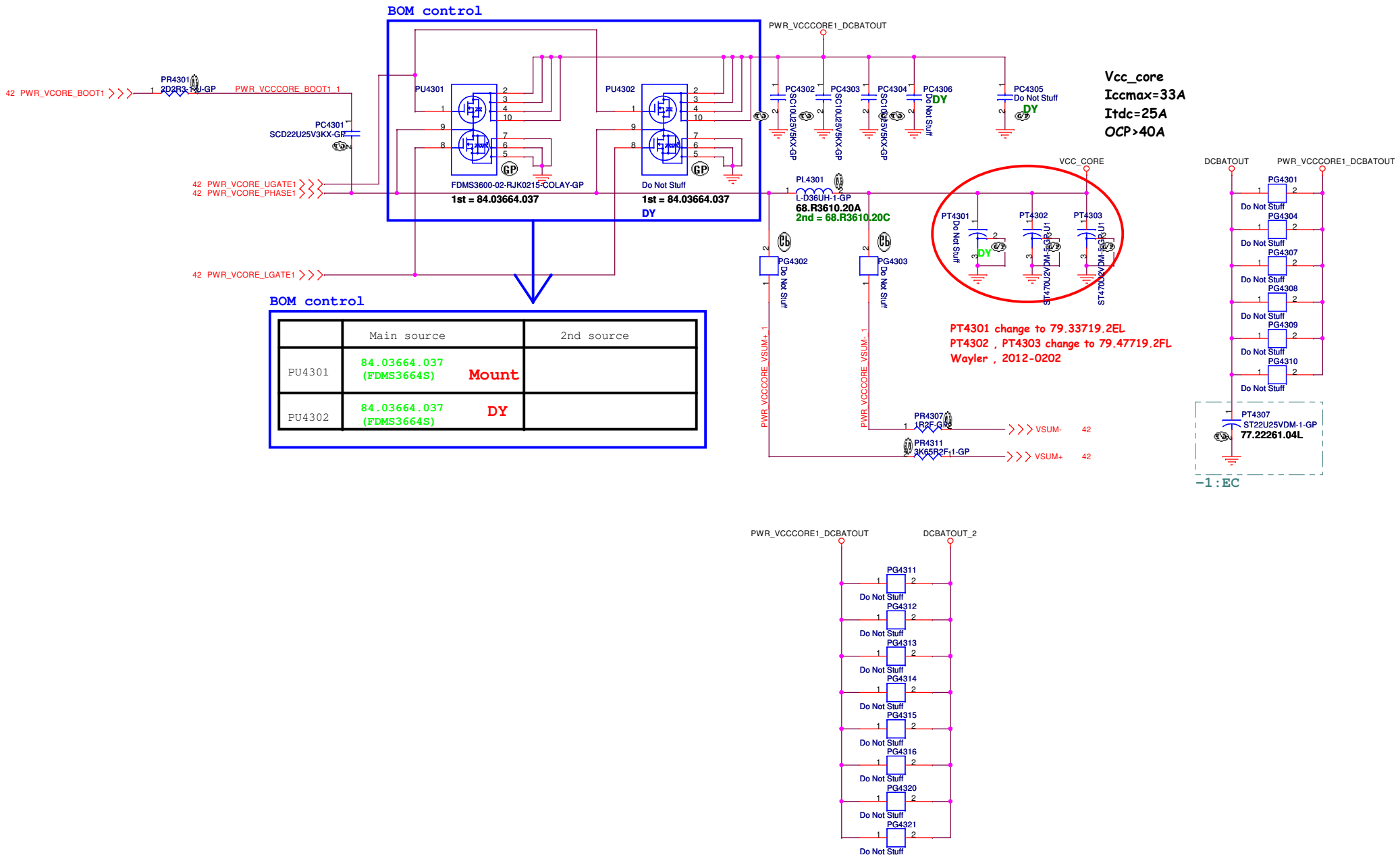
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL95836_CPU_CORE(1/3)

Size: Custom | Document Number: Husk/Petra | Rev: -1

Date: Monday, March 05, 2012 | Sheet 42 of 102



BOM control

	Main source	2nd source
PU4301	84.03664.037 (FDMS3664S) Mount	
PU4302	84.03664.037 (FDMS3664S) DY	

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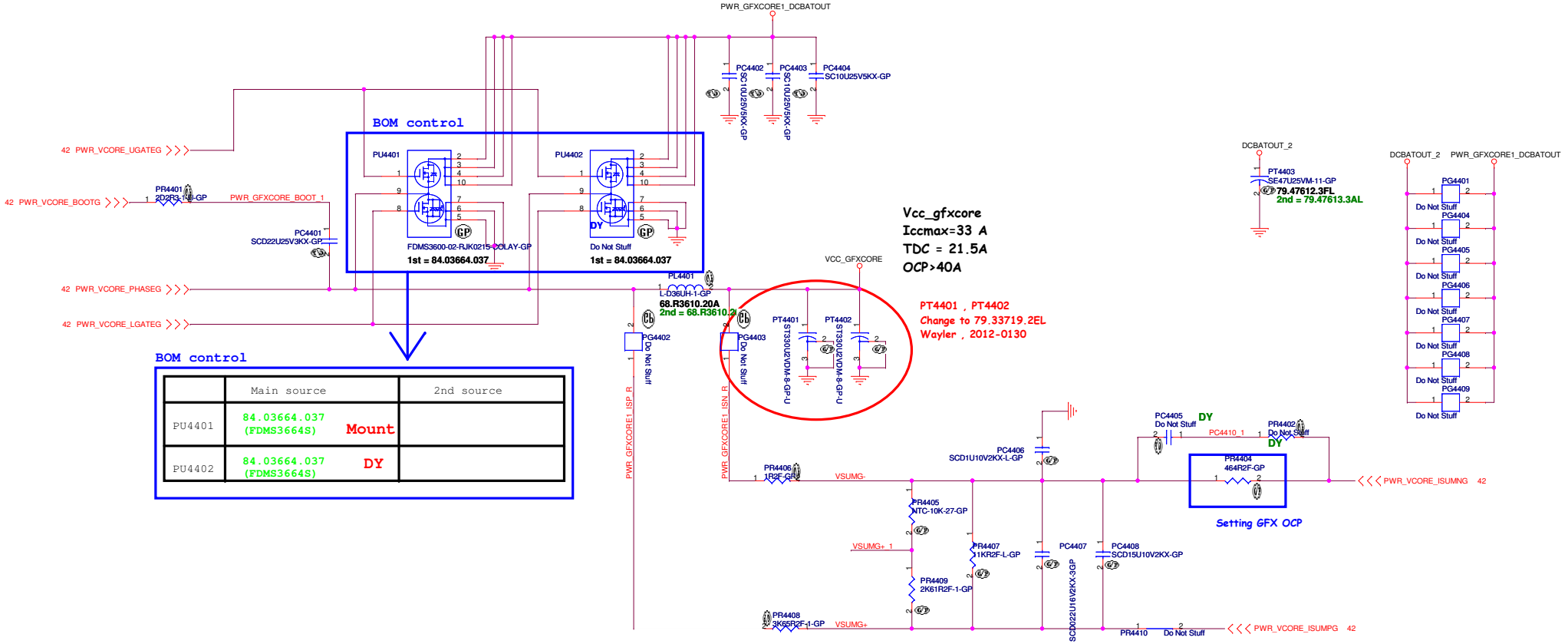
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL95836_CPU_CORE(2/3)

Size: A3 | Document Number: Husk/Petra | Rev: -1

Date: Tuesday, March 06, 2012 | Sheet 43 of 102



BOM control

	Main source	2nd source
PU4401	84.03664.037 (FDMS3664S) Mount	
PU4402	84.03664.037 (FDMS3664S) DY	

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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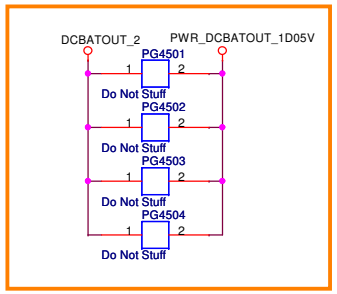
Title: ISL95836_CPU_CORE(3/3)

Size: Custom | Document Number: Husk/Petra | Rev: -1

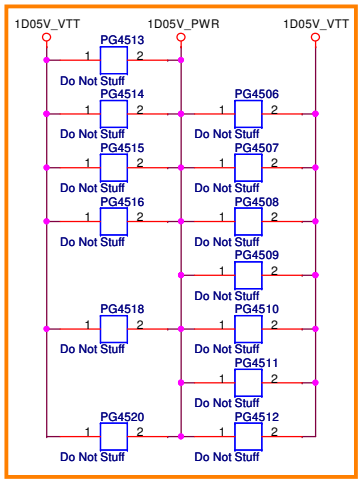
Date: Tuesday, March 06, 2012 | Sheet 44 of 102

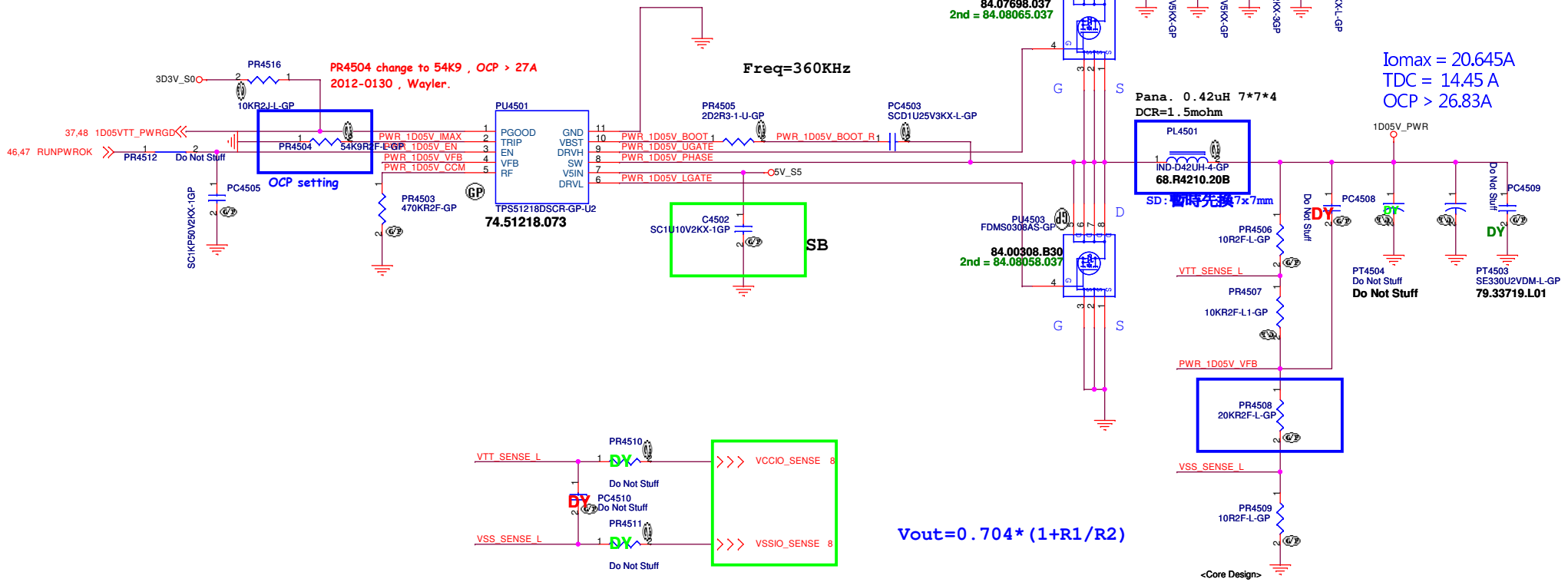
TPS51218D for 1D05V

SA_20111004



SA_20111013





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Title: DC to DC_1D05V(TPS51218D)

Size: A3 | Document Number: Husk/Petra | Rev: -1

Date: Monday, March 05, 2012 | Sheet 45 of 103

SSID = PWR.Plane.Regulator_1p5v0p75v

Change power source

SA_20111004

SC:delete PT4601

RT8207L for 1D5V

OCP setting

PR4603 change to 8K87 , OCP>24A
2012 - 0111 - Wayler

20100728

Close to pin23

Close to pin23

Iomax=1A
OCP>1.5A

Close to output cap pin1, not inside of the output cap

PU4601 change to 74.08207.D73
2012 - 0111 - Wayler

PR4608 change to 30.9K
2012 - 0111 - Wayler

Close to PIN9

+0.75VS
Iomax: 1.2A

CYNTEC. 0.68uH 7*7*3
DCR= 5 ~ 5.5 mohm
Idc=15.5A, Isat=25A

IccMAX = 18.38A
IccTDC = 12.86A
OCP > 23.89A

Vout=0.75*(1+R1/R2)

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

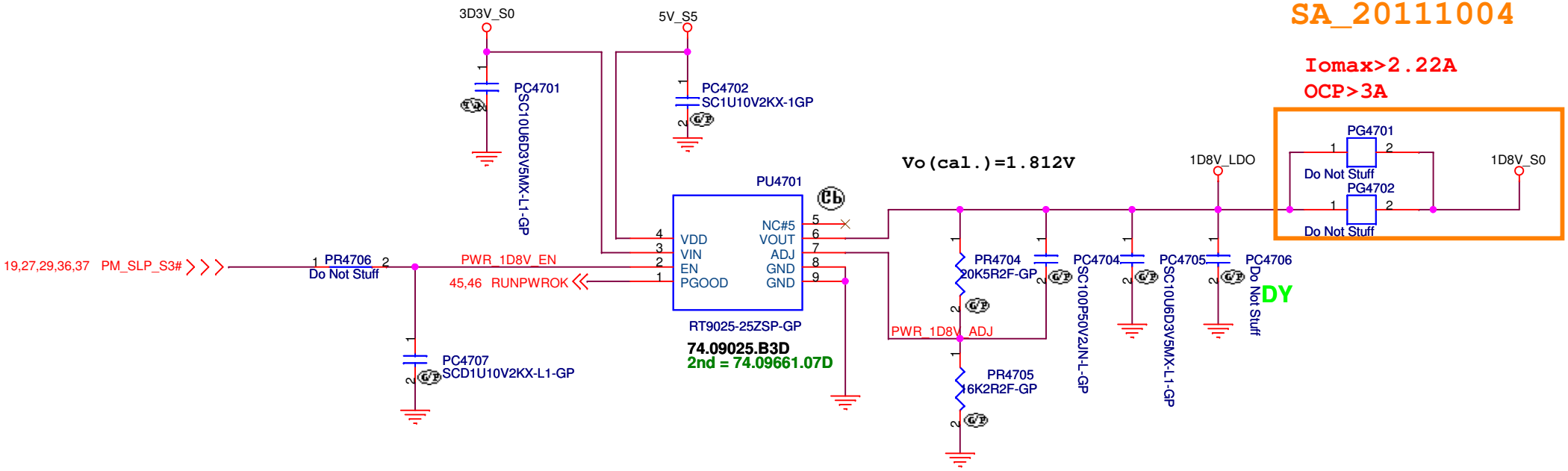
Title: RT8207

Size: Custom | Document Number: Husk/Petra | Rev: -1

Date: Wednesday, March 07, 2012 | Sheet 46 of 103

SSID = PWR.Plane.Regulator_1p8v

RT9025 for 1D8V_S0



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *LDO_1D8V(RT9025)*

Size	Document Number	Rev
A4	Husk/Petra	-1

Date: Monday, March 05, 2012 Sheet 47 of 103

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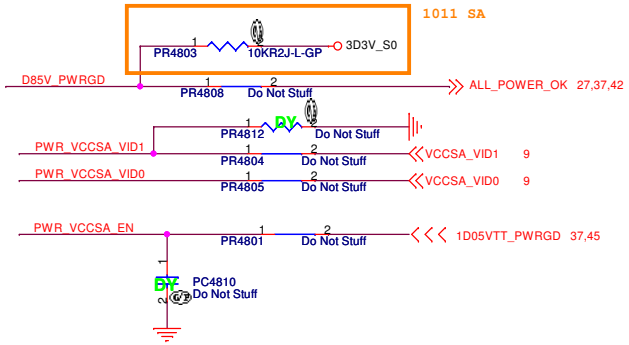
LDO G978 for VCCSA



D0, D1 V_0 Selection Table

D0	D1	V_0 MODE=0	V_0 MODE=1
0	0	0.9V	0.9V
0	1	0.8V	0.85V
1	0	0.725V	0.775V
1	1	0.675V	0.75V

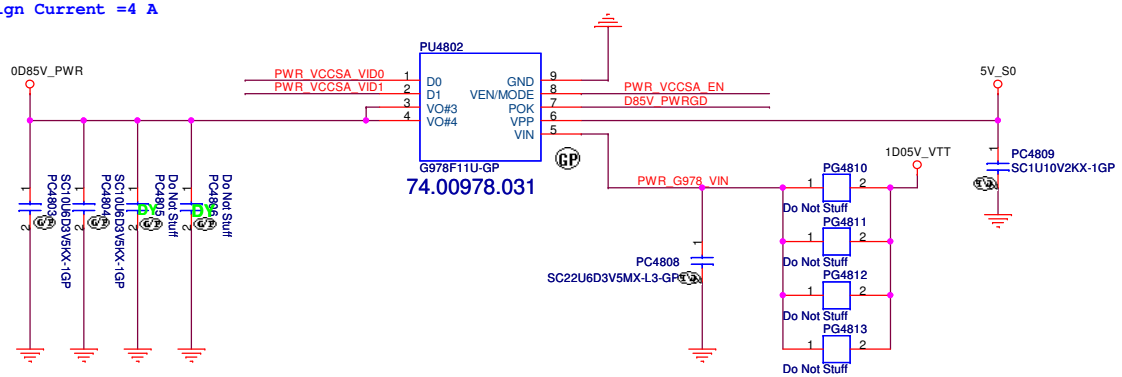
"x" means "don't care".

VEN/MODE Logic

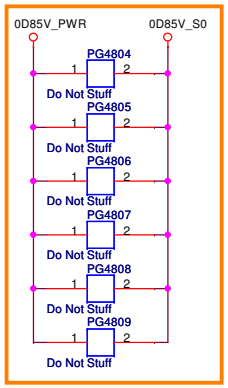
VEN/MODE (VPP=5V)	EN logic
<0.6V	0
>1.0V	1

VEN/MODE (VPP=5V)	MODE logic
<2.0V	0
>2.6V	1

Design Current =4 A



1011 SA



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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

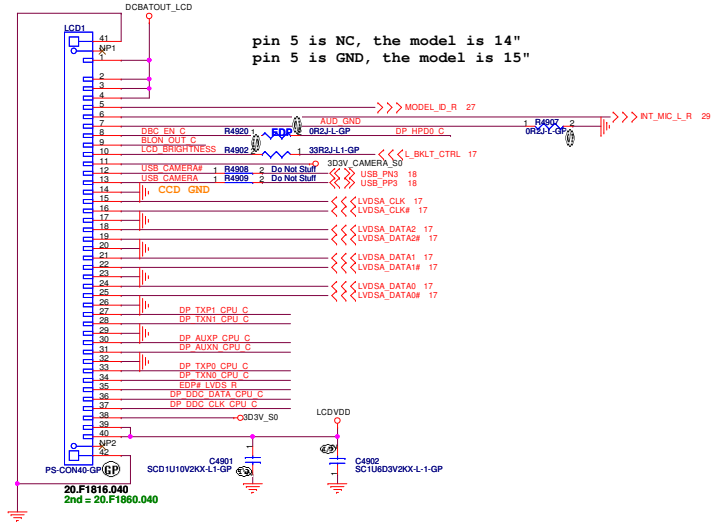
Title: ***VCCSA LDO G978***

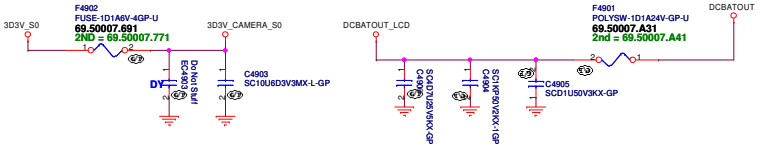
Size: A3 | Document Number: **Husk/Petra** | Rev: -1

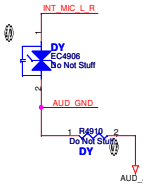
Date: Monday, March 05, 2012 | Sheet 48 of 103

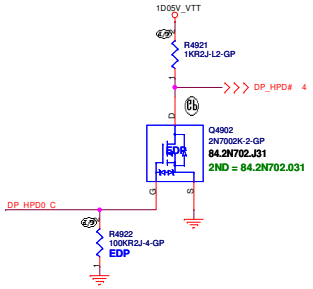
SSID = VIDEO

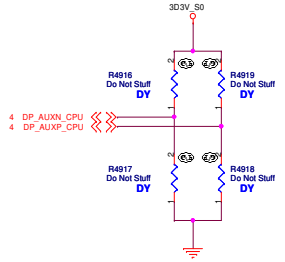
pin 5 is NC, the model is 14"
pin 5 is GND, the model is 15"

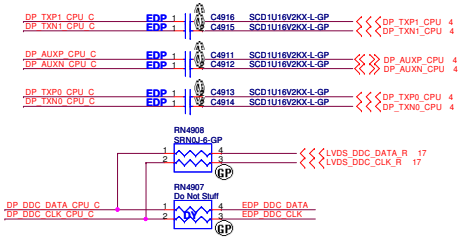


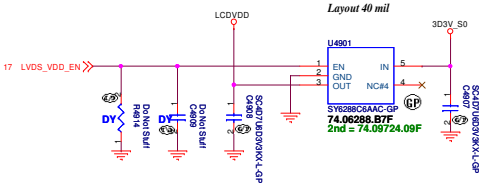


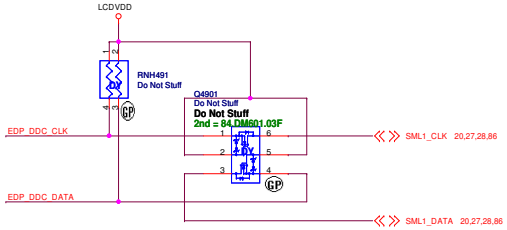


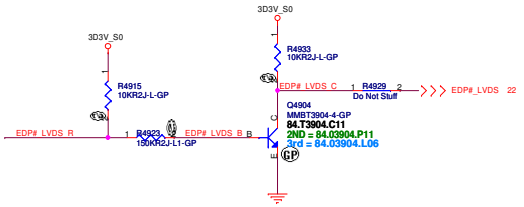




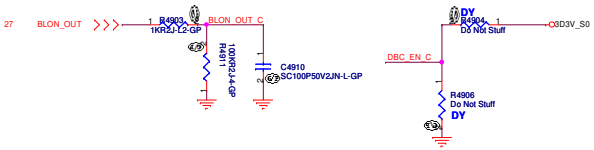


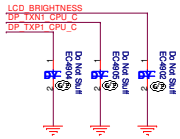






EDP: pin35 NC
LVDS: pin35 GND





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<Core Design>

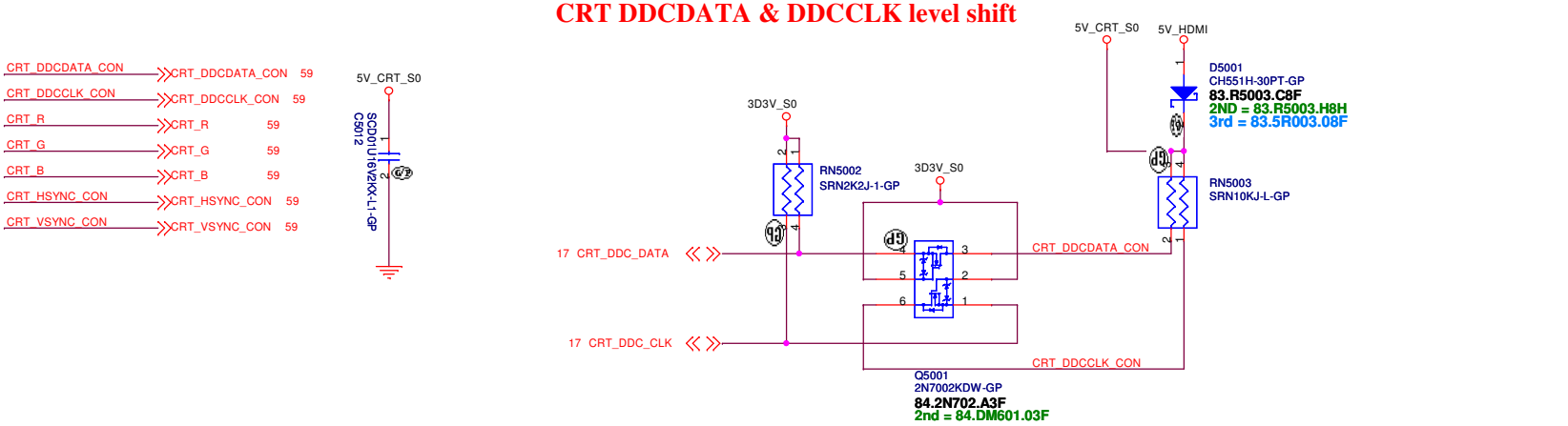
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

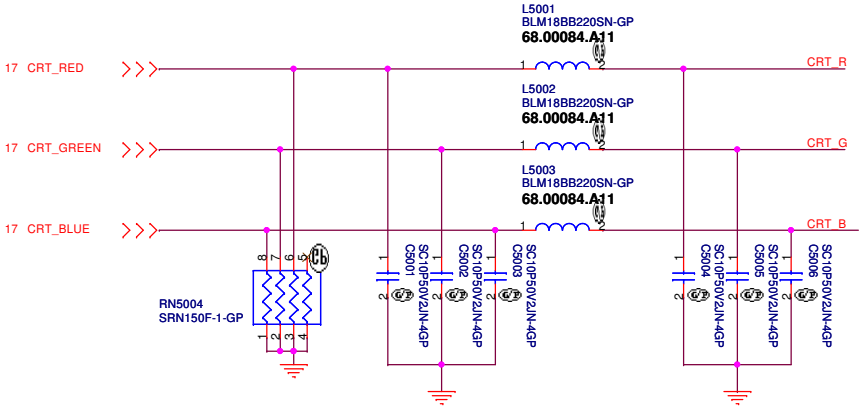
Title: LCD Connector

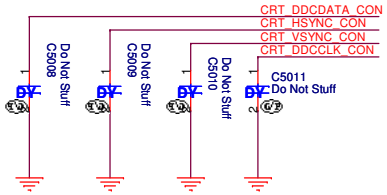
Size: A2 | Document Number: Husk/Petra | Rev: -1

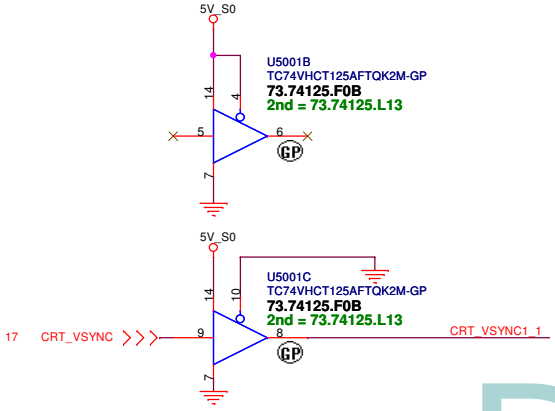
Date: Tuesday, March 06, 2012 | Sheet 49 of 103

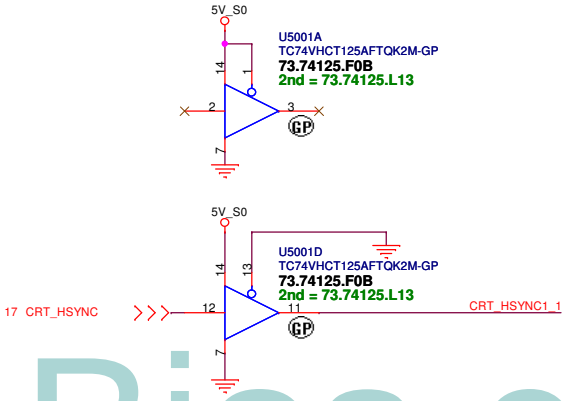
CRT DDCDATA & DDCCLK level shift

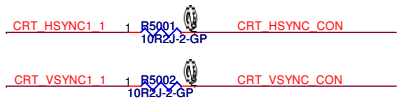












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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

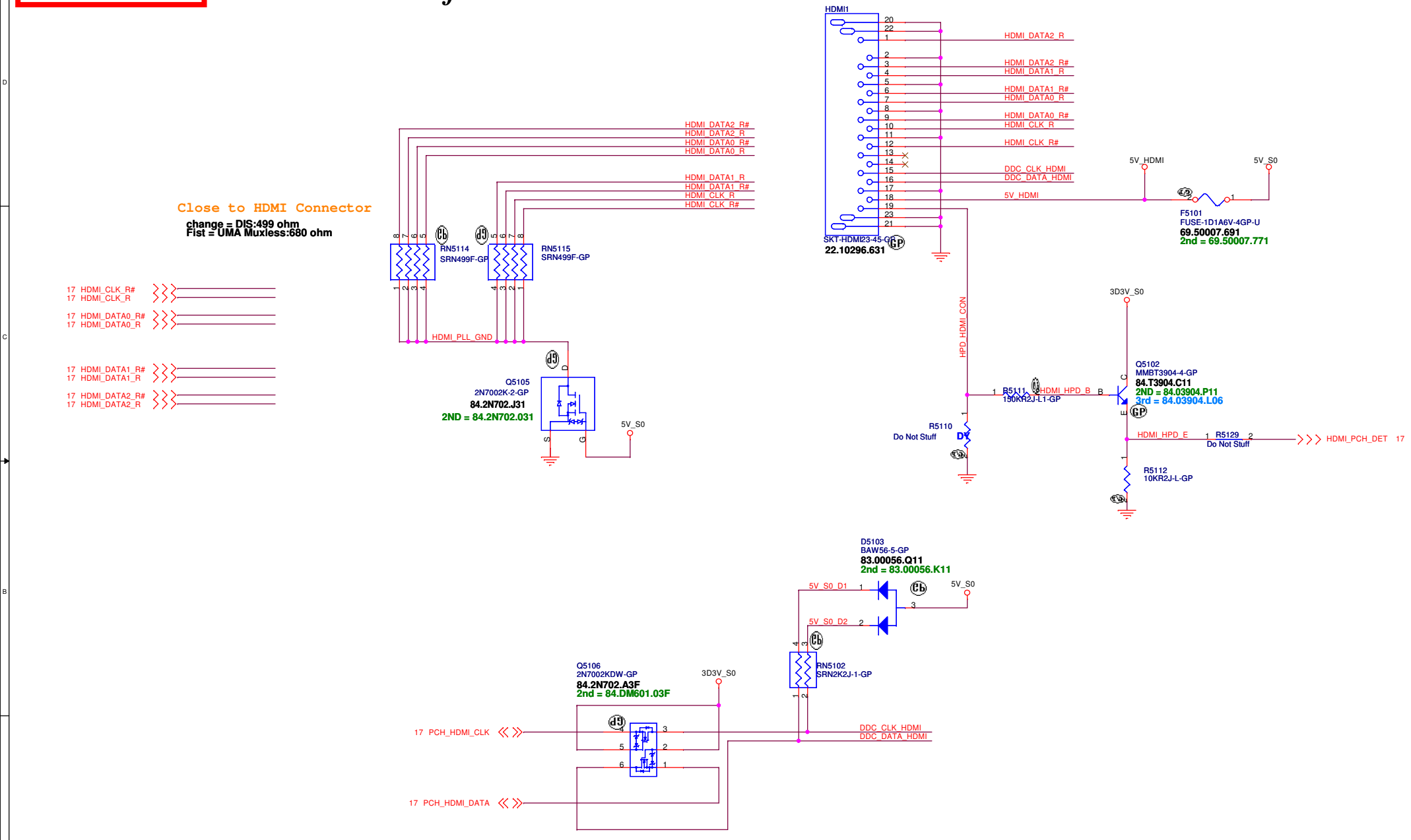
Title: **CRT Connector**

Size: A3 | Document Number: **Husk/Petra** | Rev: -1

Date: Monday, March 05, 2012 | Sheet 50 of 103

SSID = VIDEO

HDMI Level Shifter & CONNECTOR



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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter/Connector

Size	Document Number	Rev
A3	Husk/Petra	-1

Date: Monday, March 05, 2012 Sheet 51 of 103

LED BACKLIGHT CONVERTER POWER

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: eDP

Size: A3 | Document Number: Husk/Petra | Rev: -1

Date: Monday, March 05, 2012 | Sheet 52 of 103

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***S-VIDEO***

Size	Document Number	Rev
A4	**Husk/Petra**	**-1**

Date: Monday, March 05, 2012 Sheet 53 of 103

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	Husk/Petra	-1

Date: Monday, March 05, 2012 Sheet 54 of 103

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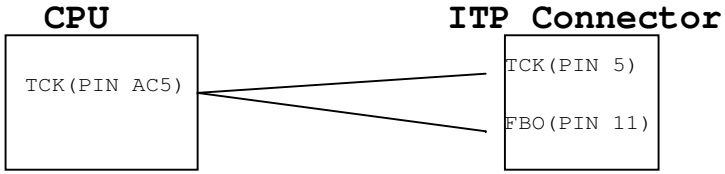
SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ITP

Size: A4 | Document Number: Husk/Petra | Rev: -1

Date: Monday, March 05, 2012 | Sheet 55 of 103

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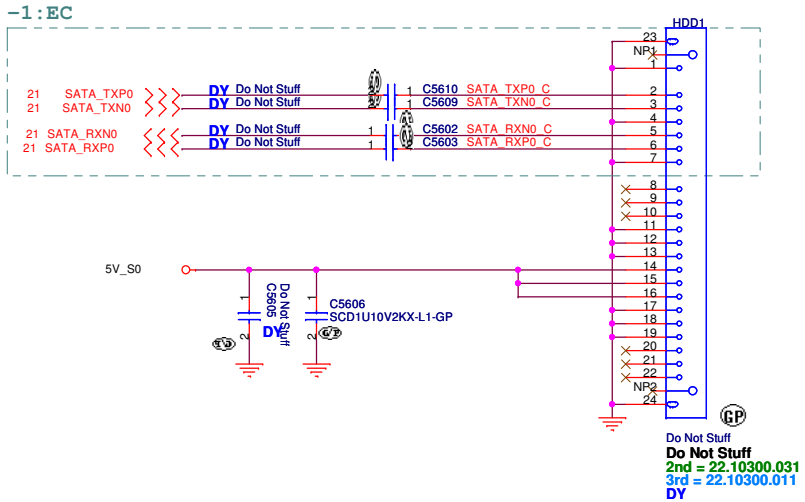
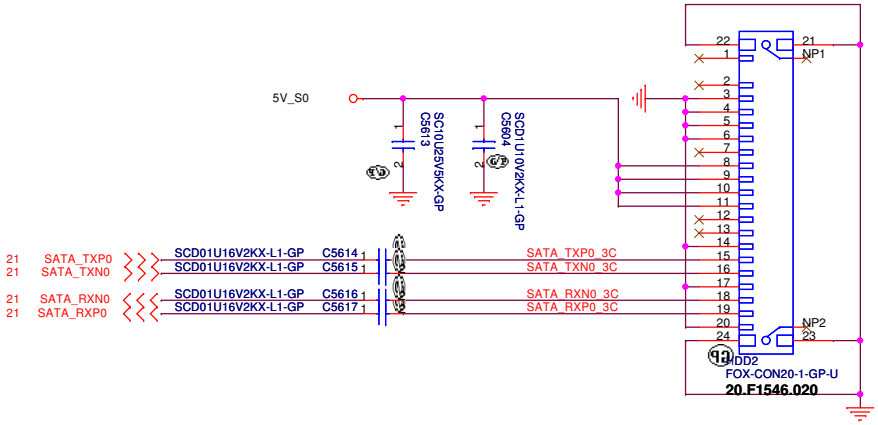
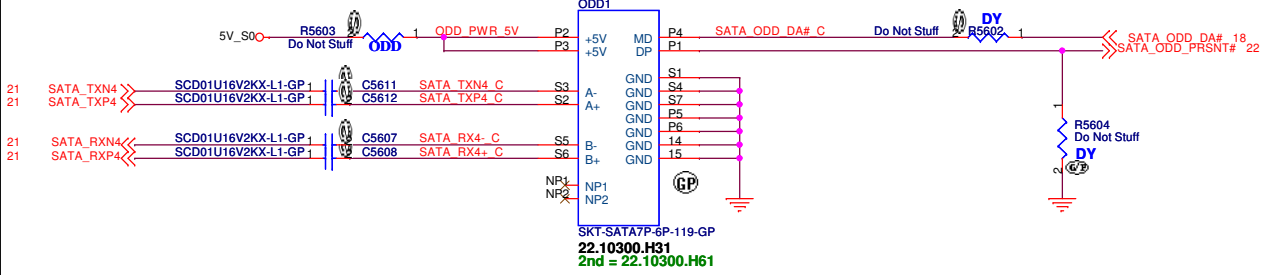
SSID = SATA

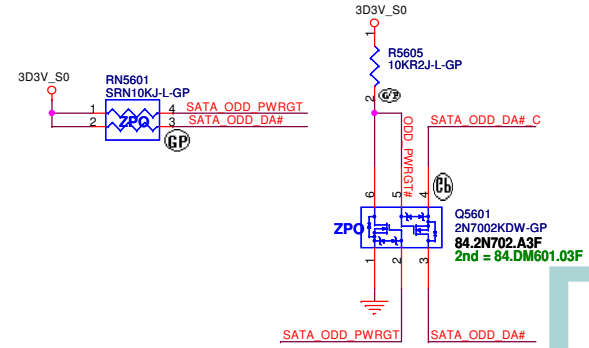
SATA HDD Connector



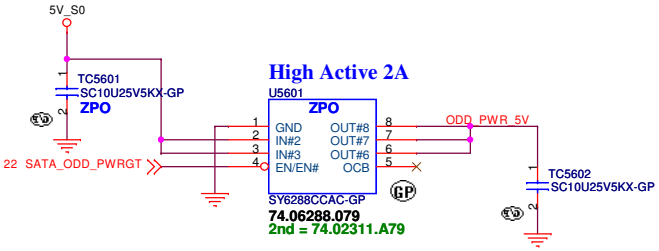


ODD Connector





SATA Zero Power ODD



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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/ODD

Size: A3 | Document Number: Husk/Petra | Rev: -1

Date: Friday, March 09, 2012 | Sheet 56 of 103

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***E-SATA/USB CHARGER***

Size	Document Number	Rev
A3	**Husk/Petra**	**-1**

Date: Monday, March 05, 2012 Sheet 57 of 103

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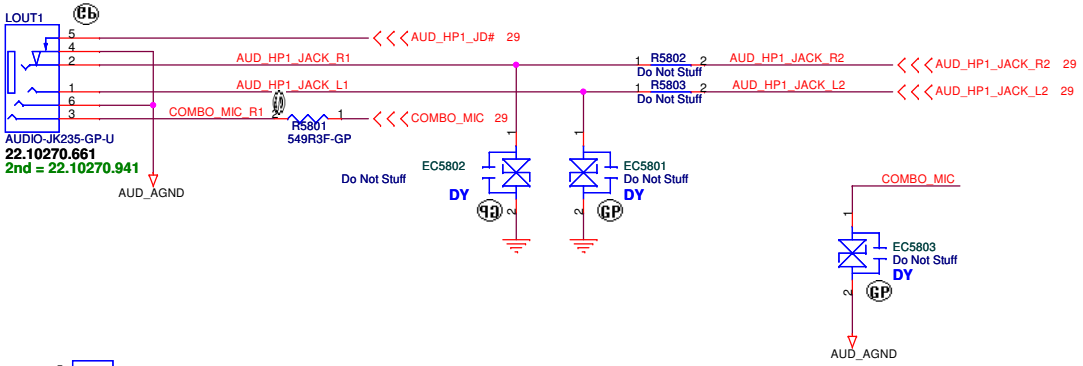
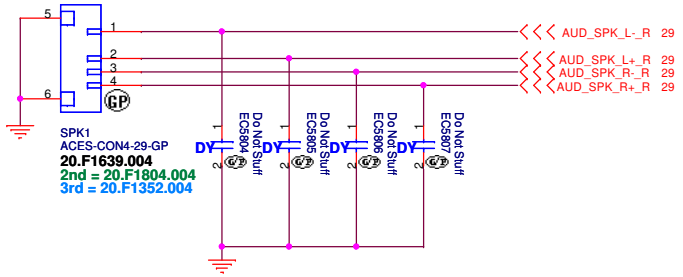
SSID = AUDIO





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<Core Design>

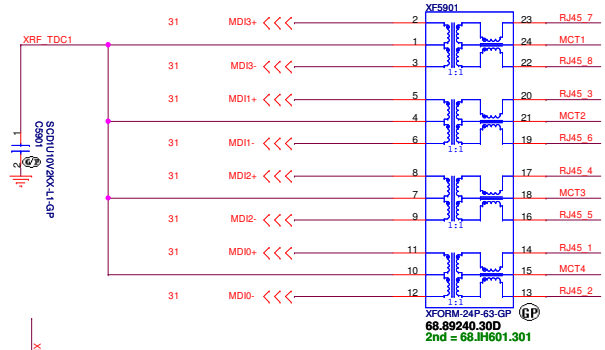
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

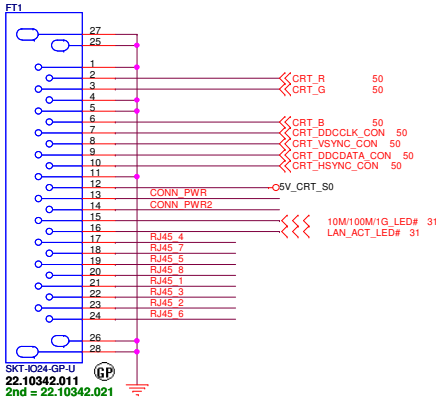
Title: ***Audio Jack***

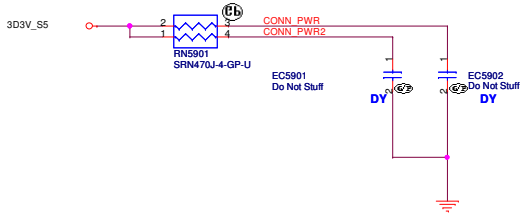
Size: A3 | Document Number: **Husk/Petra** | Rev: **-1**

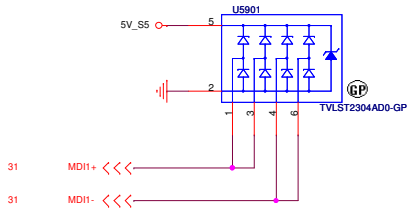
Date: Monday, March 05, 2012 | Sheet 58 of 103

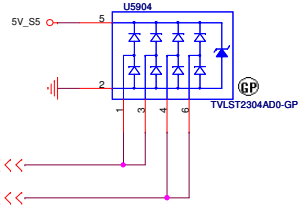
SSID = LAN

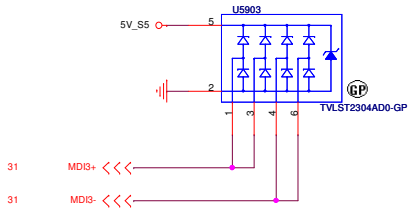


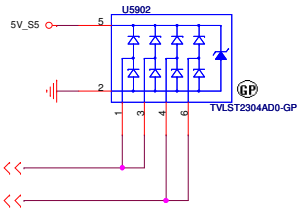


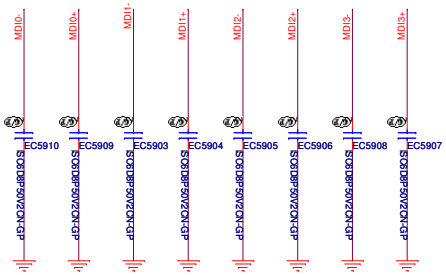


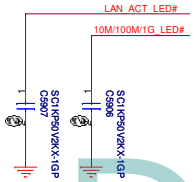


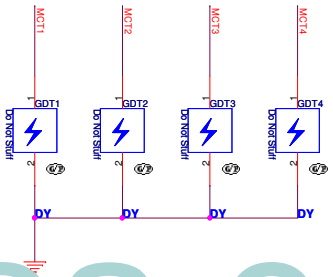


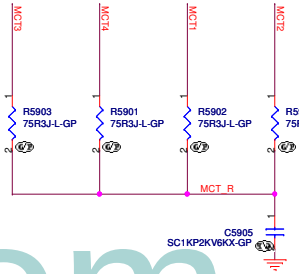












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<Core Design>

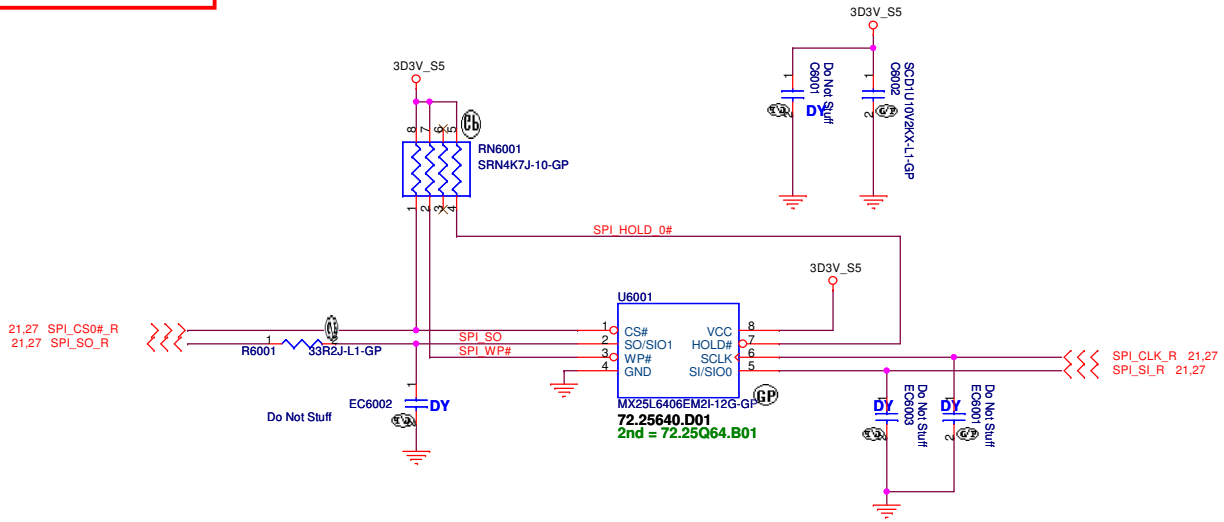
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN CONNECTOR**

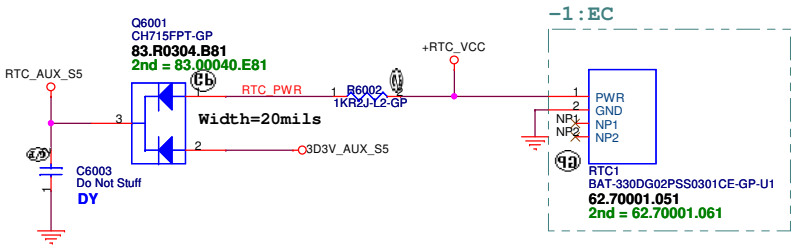
Size: Custom | Document Number: **Husk/Petra** | Rev: **-1**

Date: Tuesday, March 06, 2012 | Sheet 59 of 103

SSID = Flash.ROM



SSID = RTC



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Flash/RTC***

Size	Document Number	Rev
Custom	**Husk/Petra**	-1

Date: Tuesday, March 06, 2012 Sheet 60 of 103

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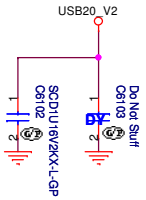
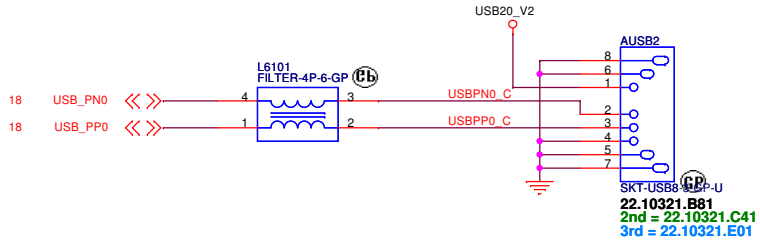
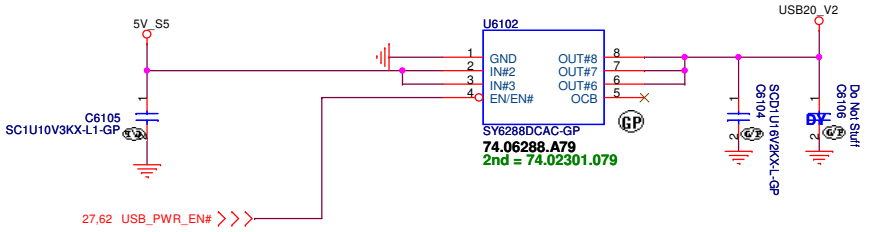
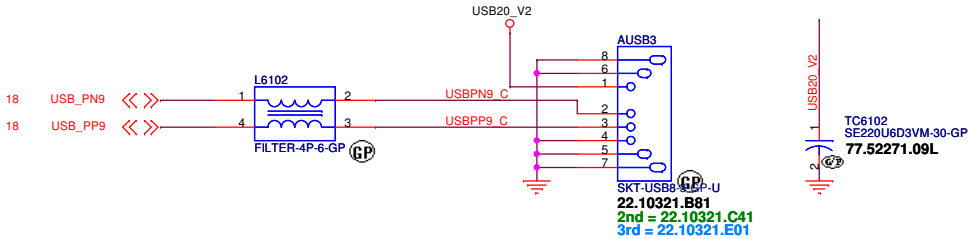
SSID = USB





Low Active 2A





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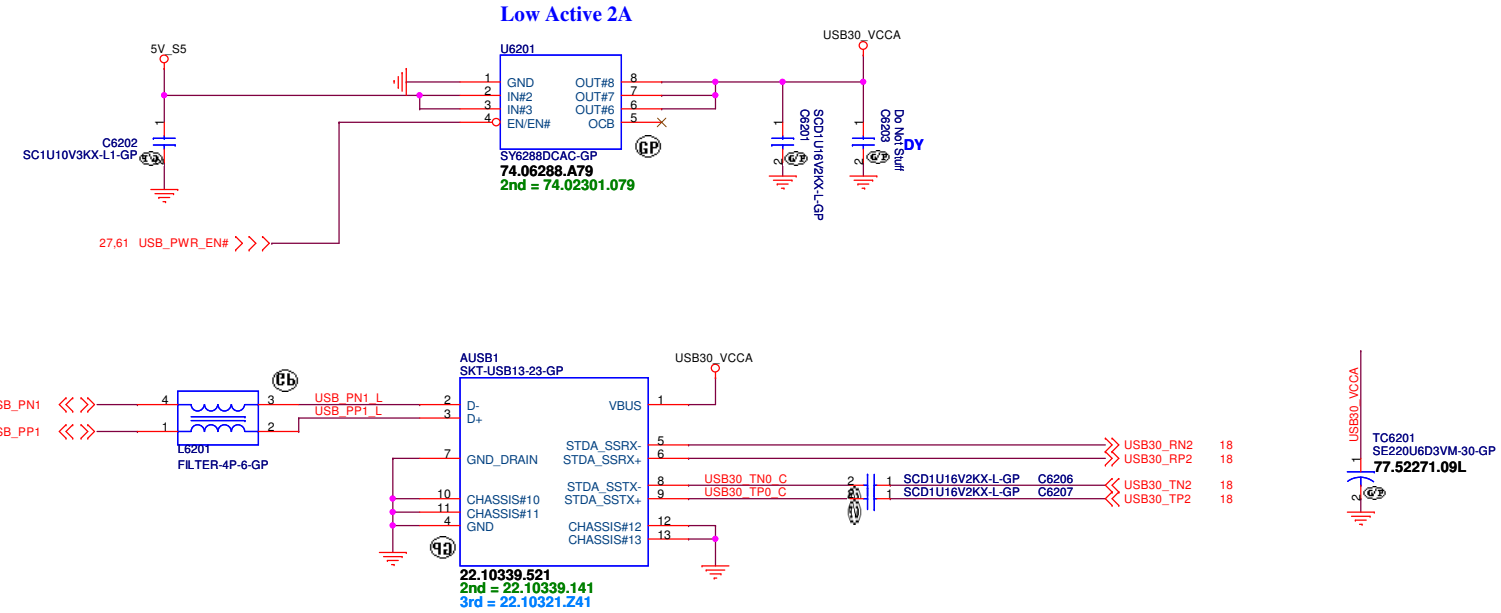
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB Power SW***

Size	Document Number	Rev
A3	Husk/Petra	-1

Date: Monday, March 05, 2012 Sheet 61 of 103



USB 3.0 Connector Pin definition		
1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB 3.0 Port

Size: A3 | Document Number: Husk/Petra | Rev: -1

Date: Monday, March 05, 2012 | Sheet 62 of 103

SSID = User.Interface

Bluetooth Module conn.

ANNIE Bluetooth Module

<Core Design>

緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Bluetooth***		
Size: A4	Document Number: **Husk/Petra**	Rev: **-1**
Date: Monday, March 05, 2012	Sheet 63 of 103	

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***RESERVED***

Size	Document Number	Rev
A4	**Husk/Petra**	-1

Date: Monday, March 05, 2012 Sheet 64 of 103

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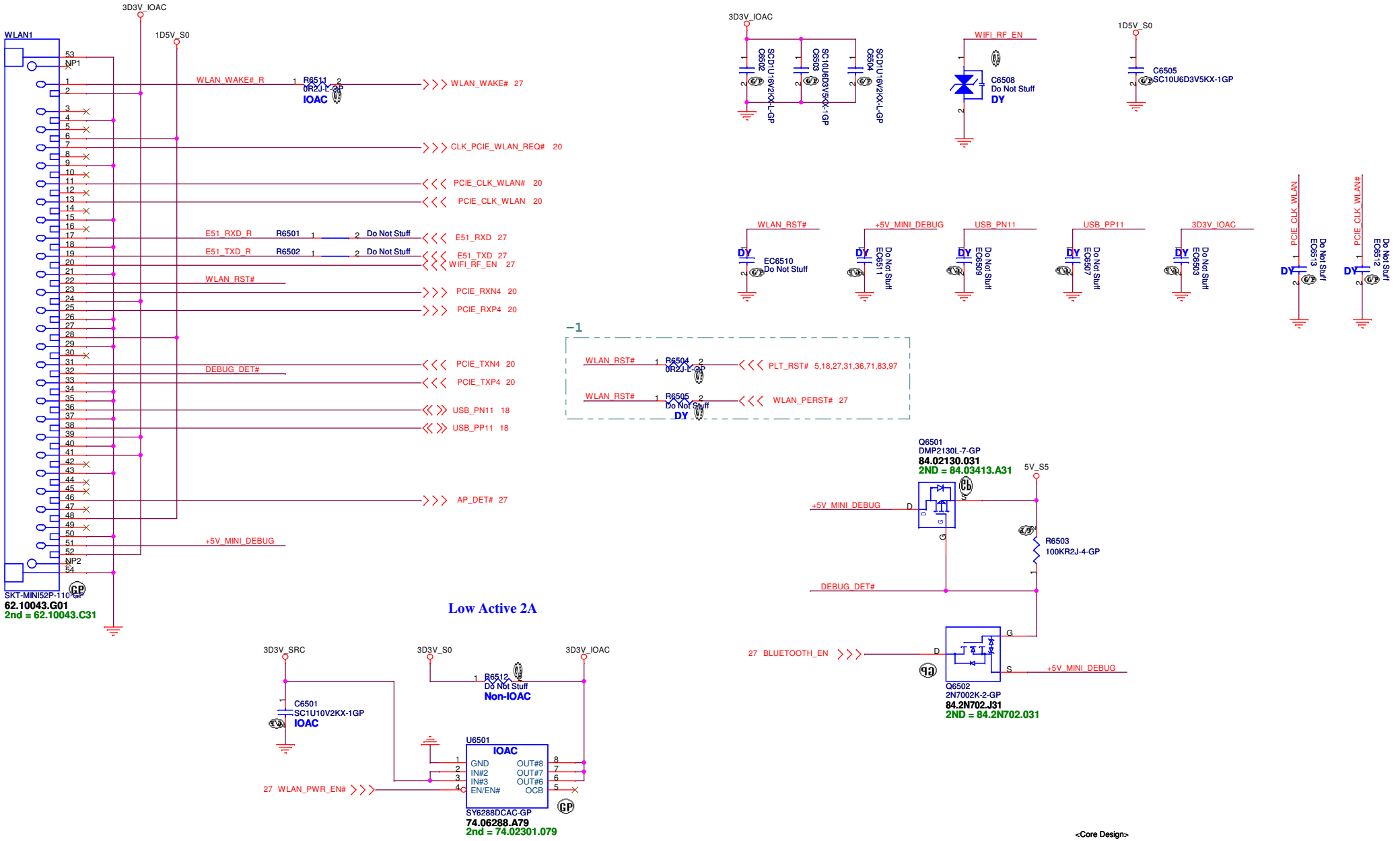
SSID = Wireless

Mini Card Connector(802.11a/b/g/n)



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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINICARD(WLAN)/ITP CONN

Size: A3 | Document Number: Husk/Petra | Rev: -1

Date: Monday, March 05, 2012 | Sheet 65 of 103

SSID = Wireless

Mini Card Connector(WWAN)

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **WWAN Connector**

Size	Document Number	Rev
A4	Husk/Petra	-1

Date: Monday, March 05, 2012 Sheet 66 of 103

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	Husk/Petra	-1

Date: Monday, March 05, 2012 Sheet 67 of 103

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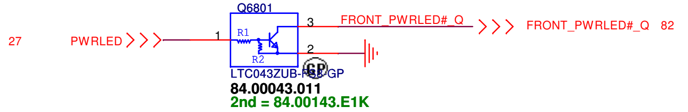
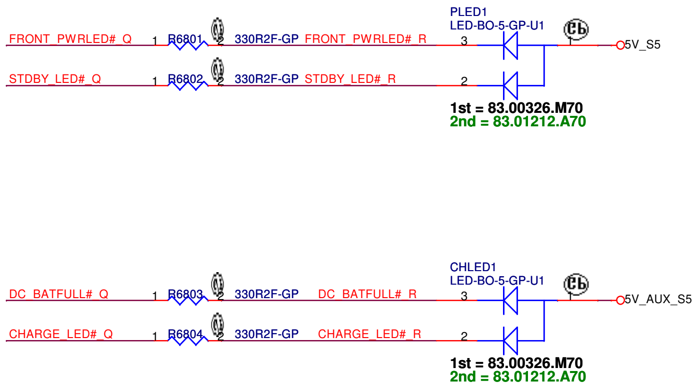
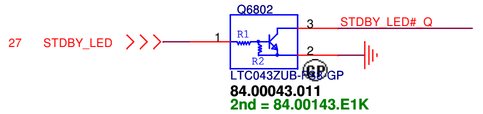
Power button LED

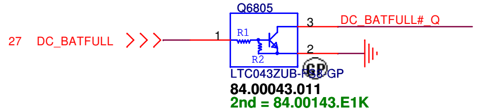


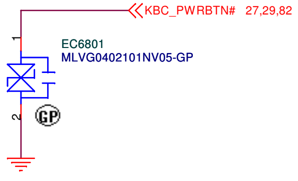


Power STDBY_LED

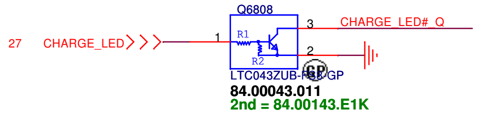


Battery LED2(DC_BATFULL)





Battery LED1(CHARGE)



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *LED Bard/Power Button*		
Size: Custom	Document Number: **Husk/Petra**	Rev: -1
Date: Monday, March 05, 2012	Sheet 68 of 103	

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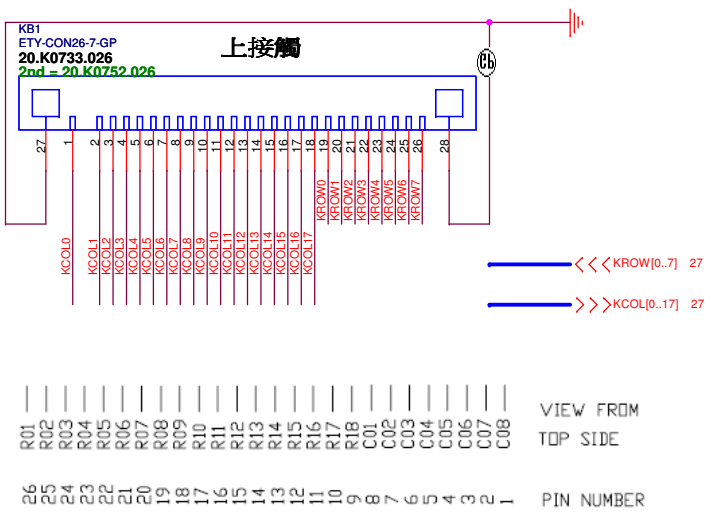
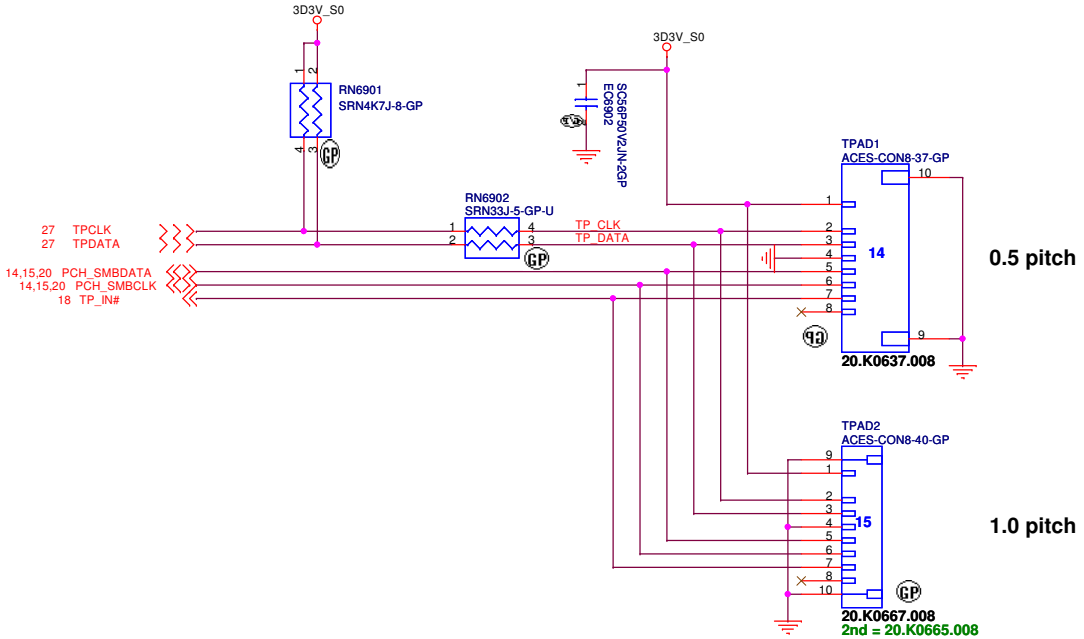
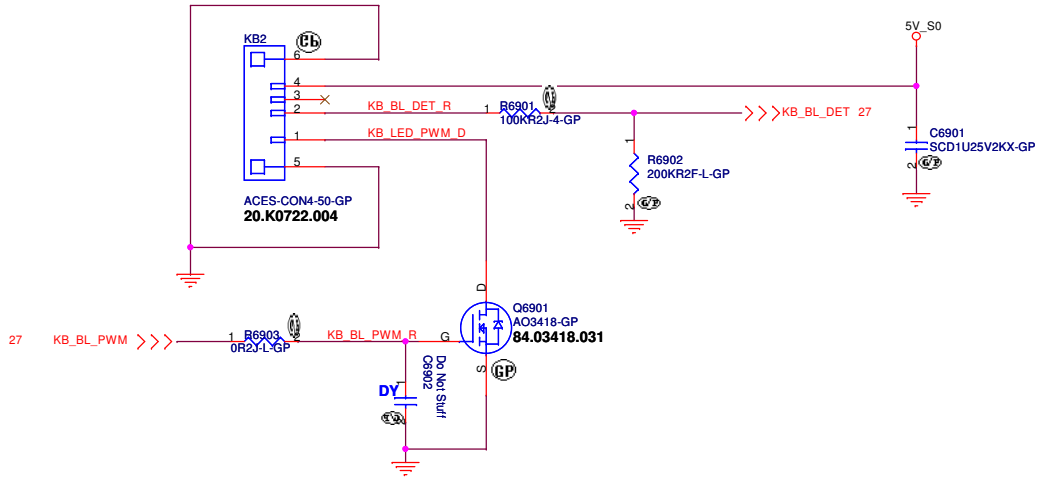
SSID = KBC

Internal KeyBoard Connector



TOUCH PAD





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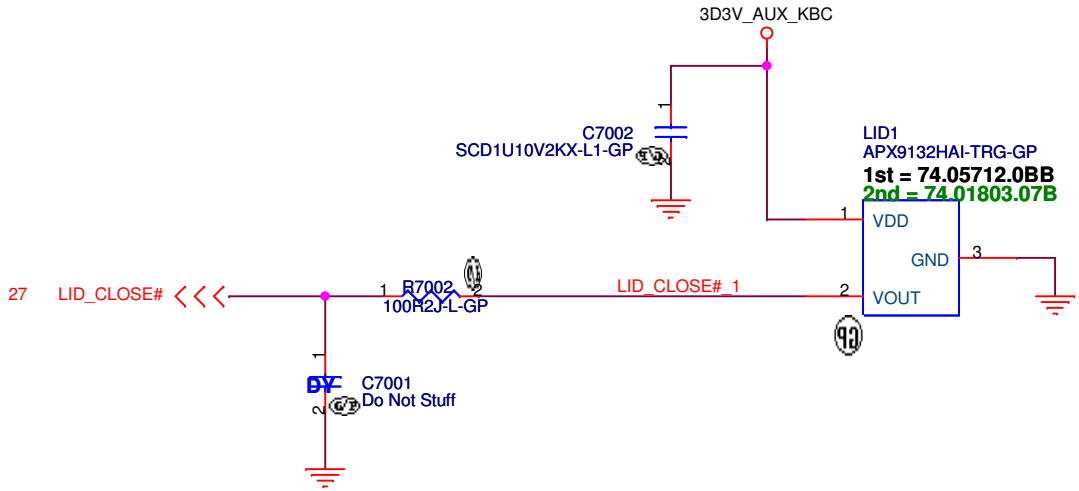
Title: Key Board/Touch Pad

Size	Document Number	Rev
A3	Husk/Petra	-1

Date: Monday, March 05, 2012 Sheet 69 of 103



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緯創資通 **Wistron Corporation**
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Title: ***Hall Sensor***

Size	Document Number	Rev
A4	**Husk/Petra**	-1

Date: Monday, March 05, 2012 Sheet 70 of 103

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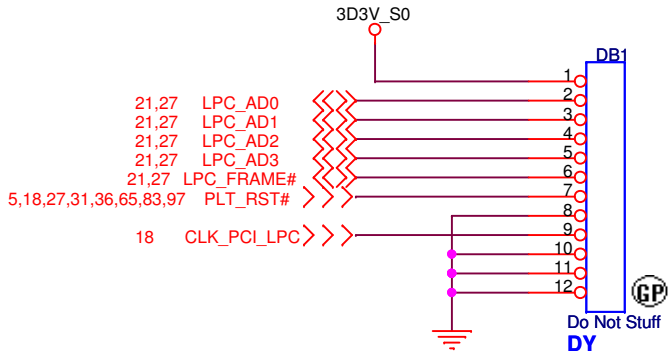

<Core Design>

緯創資通 **Wistron Corporation**
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Title: ***Dubug connector***

Size	Document Number	Rev
A4	**Husk/Petra**	-1

Date: Monday, March 05, 2012 Sheet 71 of 103

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Title: ***Reserved***

Size: A3 | Document Number: Husk/Petra | Rev: -1

Date: Monday, March 05, 2012 | Sheet 72 of 103

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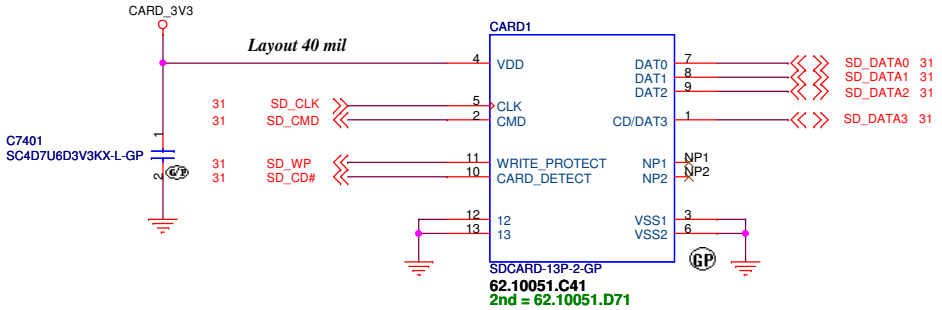
Title: ***Reserved***

Size: A3 | Document Number: Husk/Petra | Rev: -1

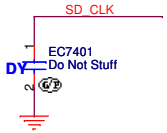
Date: Monday, March 05, 2012 | Sheet 73 of 103

SSID = SDIO

SD/MMC Card Reader



SP1	SP1	SD_D7		xD_RDY
SP2	SP2	SD_D6	MS_INS#	xD_RE#
SP3	SP3	SD_D5		xD_CE#
SP4	SP4	SD_D4		xD_WE#
SP5	SP5	SD_D1	MS_CLK	xD_D6
SP6	SP6	SD_D0	MS_D7	xD_D5
SP7	SP7	SD_CLK	MS_D3	xD_D4
SP8	SP8	SD_CMD	MS_D6	xD_D3
SP9	SP9	SD_D3	MS_D2	xD_D2
SP10	SP10	SD_D2		xD_D7
SP11	SP11		MS_BS	xD_CLE
SP12	SP12	SD_WP	MS_D1	xD_WP#
SP13	SP13	SD_CD#	MS_D5	xD_ALE
SP14	SP14		MS_D4	xD_D0
SP15	SP15		MS_D0	xD_D1
SP16	SP16			xD_CD#



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: CARD Reader CONN

Size: Custom | Document Number: Husk/Petra | Rev: -1

Date: Monday, March 05, 2012 | Sheet 74 of 103

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SSID = ExpressCard

+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA

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Title: New Card

Size: A3 | Document Number: Husk/Petra | Rev: -1

Date: Monday, March 05, 2012 | Sheet 75 of 103

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<Core Design>

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Title: ***Reserved***

Size	Document Number	Rev
A4	Husk/Petra	-1

Date: Monday, March 05, 2012 Sheet 76 of 103

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Title: ***Reserved***

Size	Document Number	Rev
A4	**Husk/Petra**	**-1**

Date: Monday, March 05, 2012 Sheet 77 of 103

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Title: ***Reserved***

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A4	**Husk/Petra**	-1

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SSID = User.Interface

Free Fall Sensor

Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

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Taipei Hsien 221, Taiwan, R.O.C.

Title: G- Sensor

Size: A4 | Document Number: Husk/Petra | Rev: -1

Date: Monday, March 05, 2012 | Sheet 79 of 103

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Title: ***Reserved***

Size	Document Number	Rev
A4	**Husk/Petra**	-1

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Title: ***Reserved***

Size	Document Number	Rev
A4	Husk/Petra	-1

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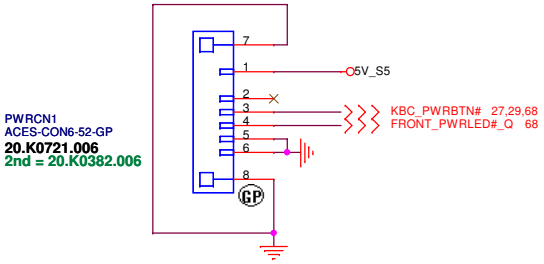

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緯創資通 **Wistron Corporation**
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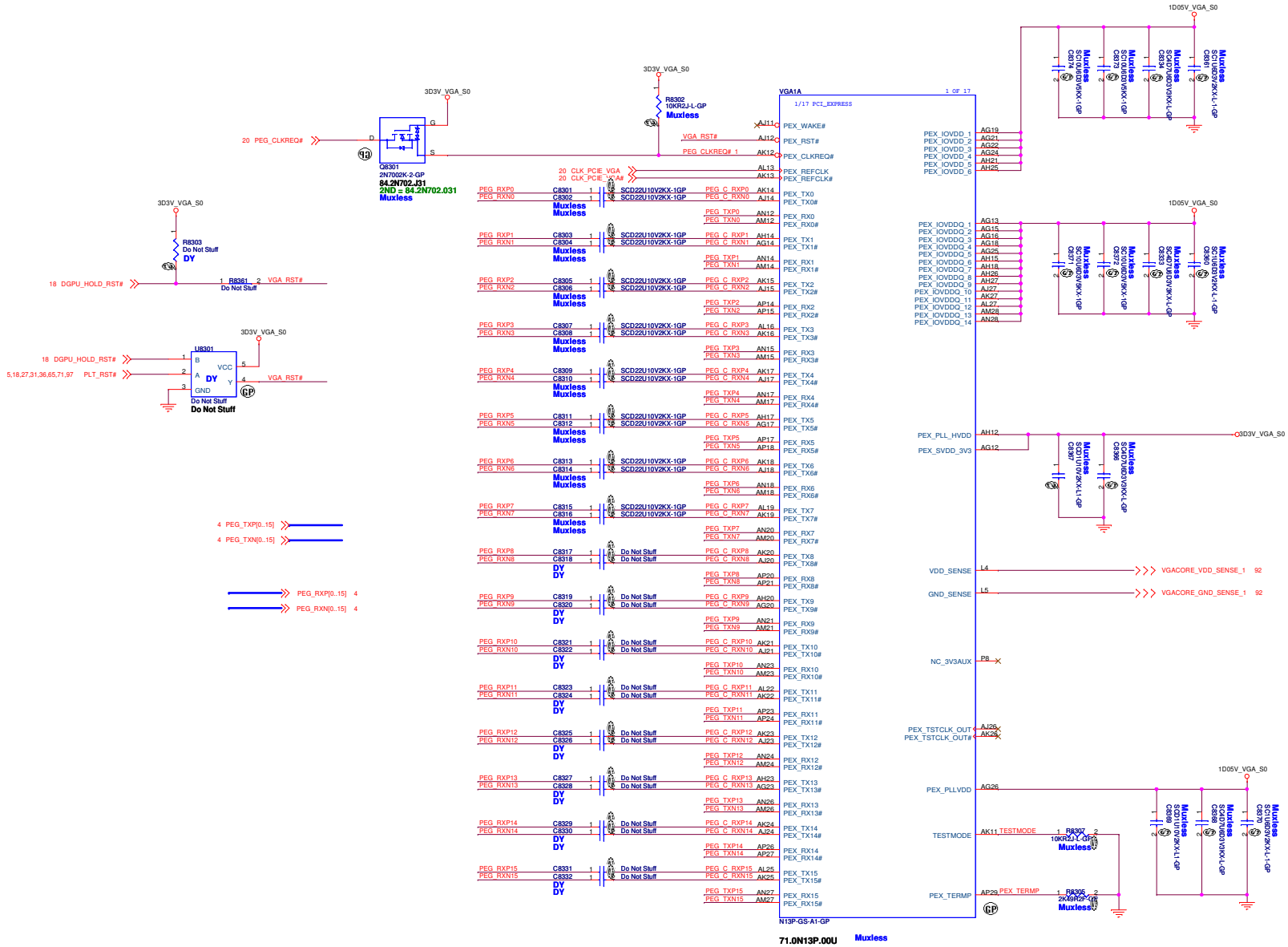
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***IO Board Connector***

Size	Document Number	Rev
A3	**Husk/Petra**	**-1**

Date: Monday, March 05, 2012 Sheet 82 of 103



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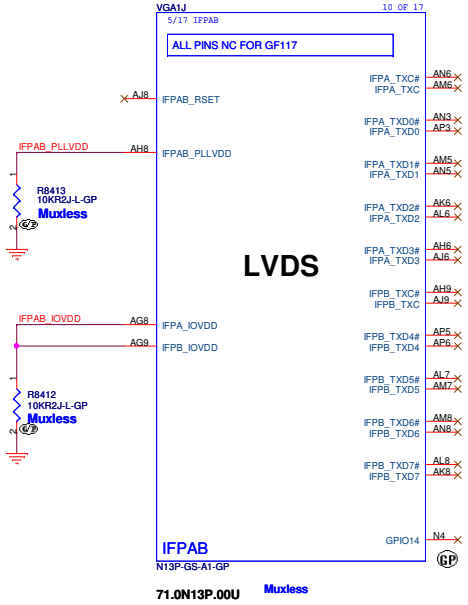
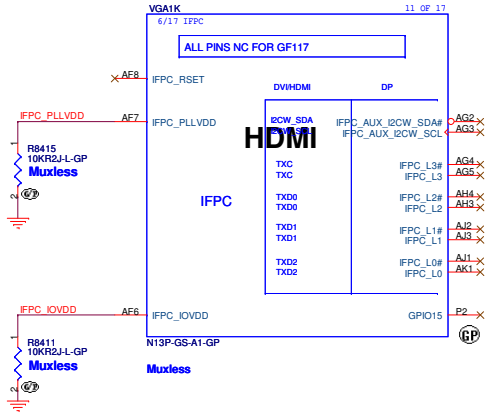
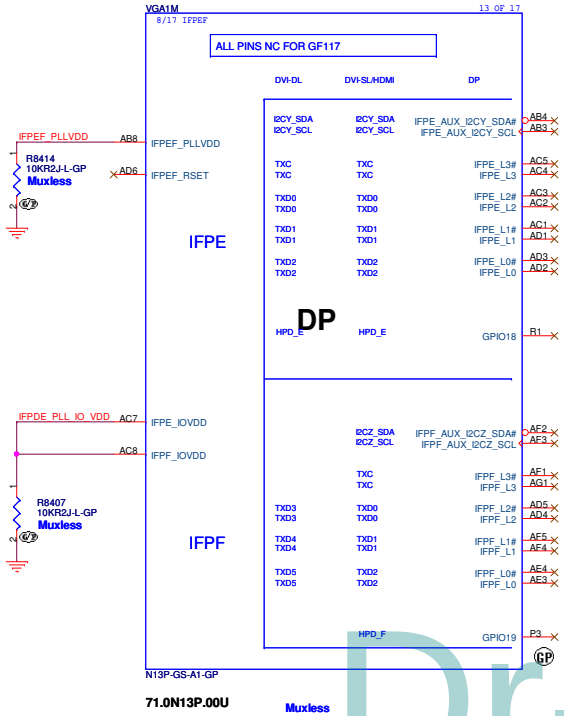
Title: GPU_PCIE/STRAPPING(1/5)

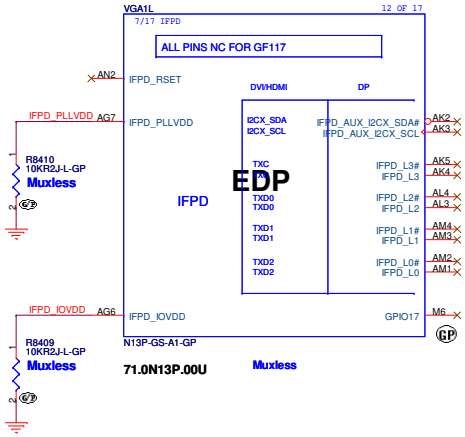
Size: A2 | Document Number: Husk/Petra | Rev: -1

Date: Monday, March 05, 2012 | Sheet 83 of 103









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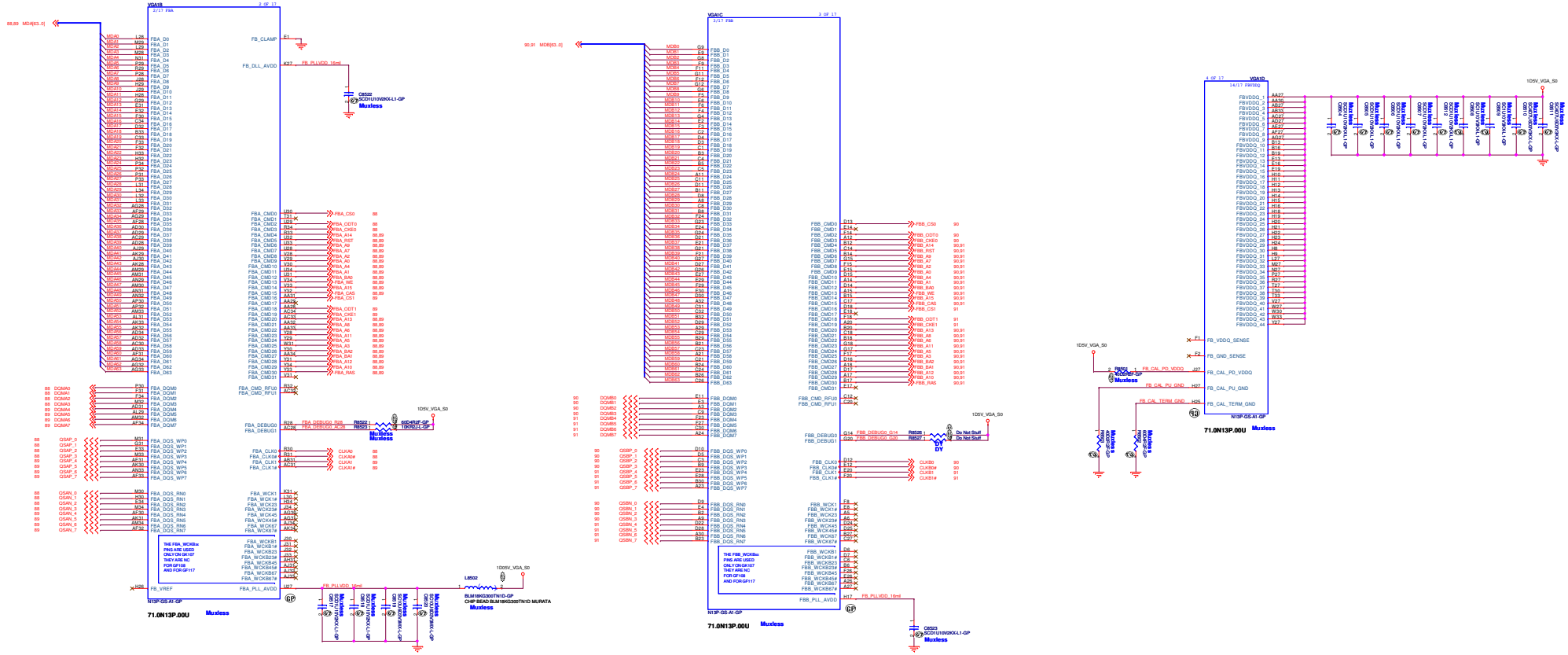
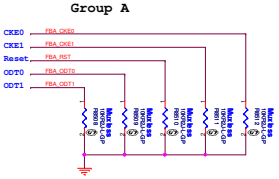
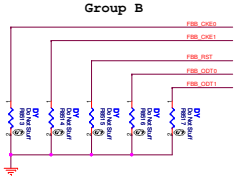
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU Memory(2/5)
Size: Custom | Document Number: Husk/Petra | Rev: -1
Date: Monday, March 05, 2012 | Sheet 84 of 103



FBCLK Termination place on VRAM side





FBCLK Termination place on VRAM side

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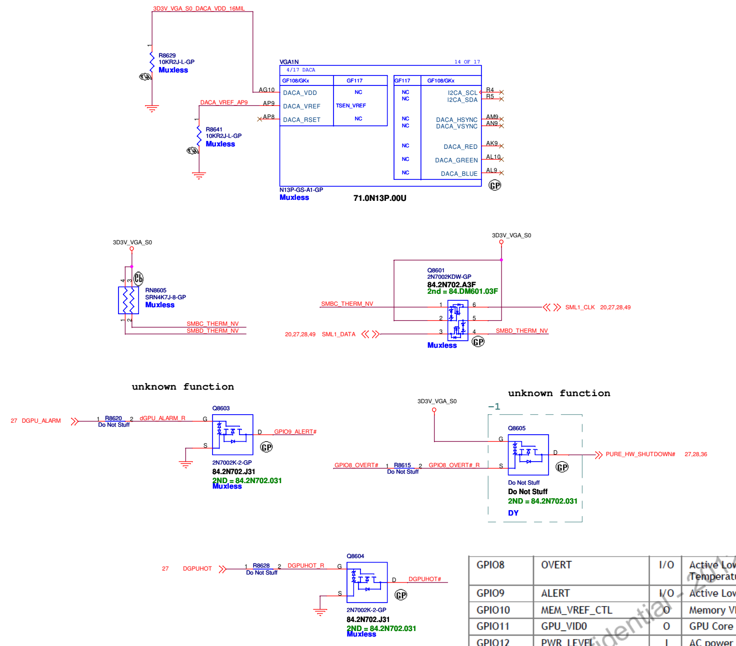
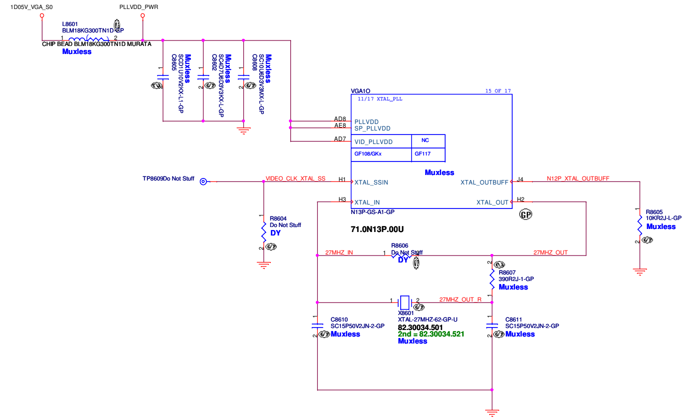
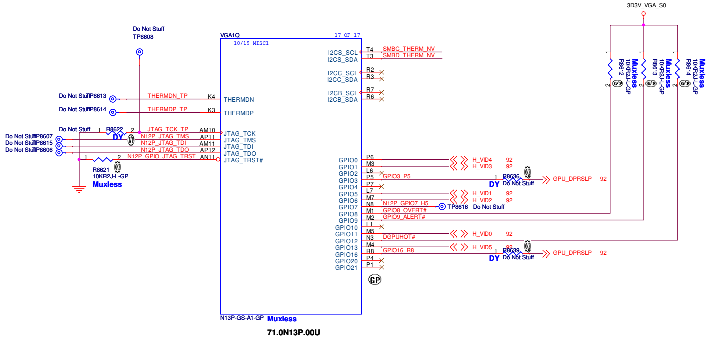


GPIO8	OVERT	I/O	Active Low Thermal Catastrophic Over Temperature
GPIO9	ALERT	I/O	Active Low Thermal Alert
GPIO10	MEM_VREF_CTL	O	Memory VREF Control
GPIO11	GPU_VID0	O	GPU Core VDD VID0
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input





VRAM Table(N13P-GS/GT/LP/GL/GLP/NS/GE)

	Hynix 2G_B-Die 0110(0x6) 128*16	Hynix 1G 0010(0x2) 64*16	Samsung 2G_C-Die 0111(0x7) 128*16	Samsung 1G 0011(0x3) 64*16
ROM_SI R8627	34.8Kohm 64.34825.6DL	15Kohm 64.15025.6DL	45Kohm 64.45325.6DL	20Kohm 64.20025.6DL

5Kohm
64.49915.6DL

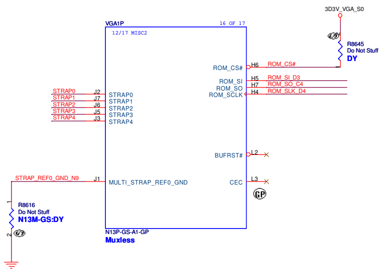
10Kohm
64.10025.L0L

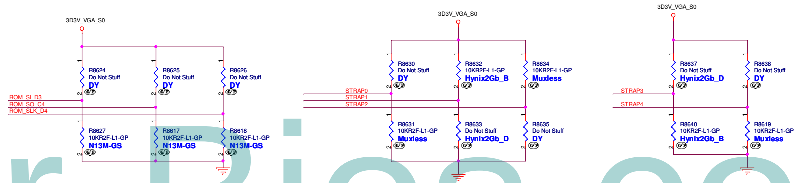
VRAM Table(N13M-GS/NS)

Hynix 2G_D-die 1100(0xC) 128*16	Hynix 2G_B-die 0110(0x6) 128*16

```
Logical Strap Bit Mapping
Resistor  Pull-up Pull-down
 5Kohms    1000    0000
 10Kohms   1001    0001
 15Kohms   1010    0010
 20Kohms   1011    0011
 25Kohms   1100    0100
 30Kohms   1101    0101
 35Kohms   1110    0110
 45Kohms   1111    0111
```

Mode	Product	NVCLK (MHz)	MCLK (MHz)	NVVDD (V)
MAX Point (MP)	N13M-GS/-NS	712.5	900	–
TDP Point (TP)	N13M-GS/-NS	625	900	–
HW Boot Voltage	N13M-GS/-NS	–	–	0.875





Strap Pin Name	Strap Mapping	Resistance	Polarity
ROM_SCLK	SMB_ALT_ADDR	10k Ω	Pull-down to GND
ROM_SI	SUB_VENDOR	10k Ω	Pull-up to 3V3 if VBIOS ROM exists Pull-down to GND if no VBIOS ROM
ROM_SO	VGA_DEVICE	10k Ω	Pull-down to GND (no display)
STRAP0	RAM_CFG[0]	10k Ω	See Note
STRAP1	RAM_CFG[1]	10k Ω	See Note
STRAP2	RAM_CFG[2]	10k Ω	See Note
STRAP3	RAM_CFG[3]	10k Ω	See Note
STRAP4	PCIE_MAX_SPEED	10k Ω	Pull-down to GND

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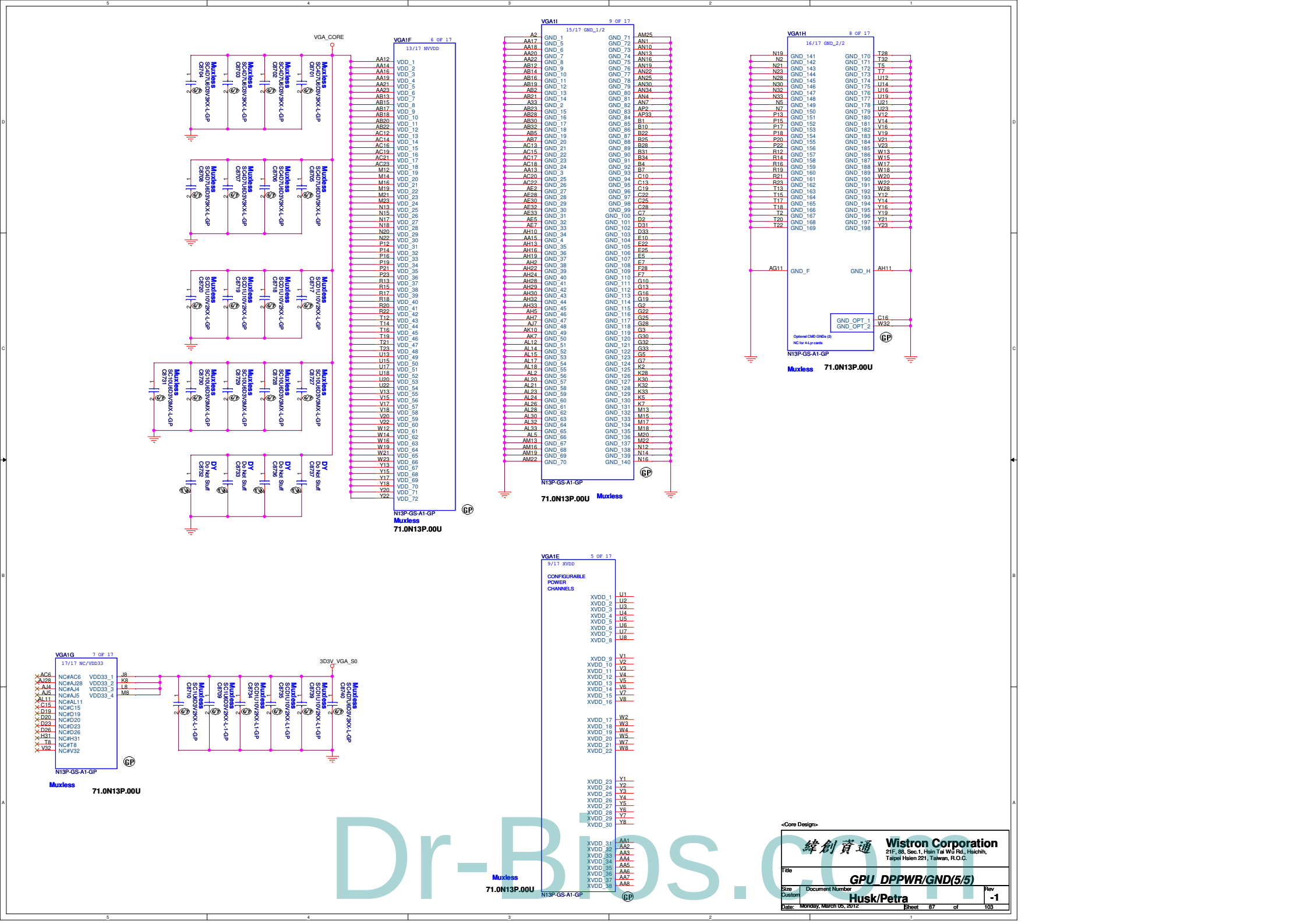

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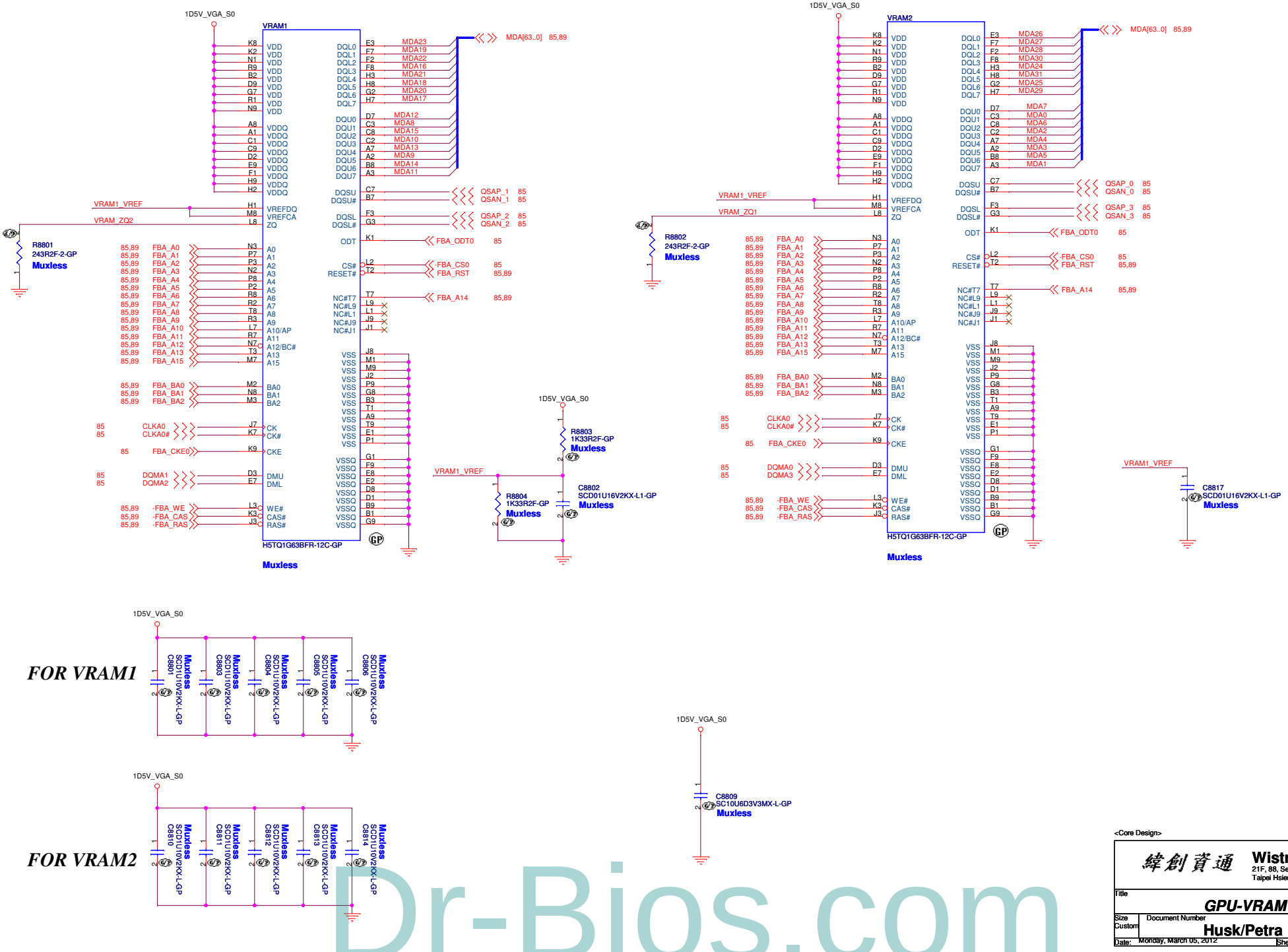
Title: GPU_DPPWR/GND(5/5)

Size: Custom | Document Number: Husk/Petra | Rev: -1

Date: Monday, March 05, 2012 | Sheet 87 of 103



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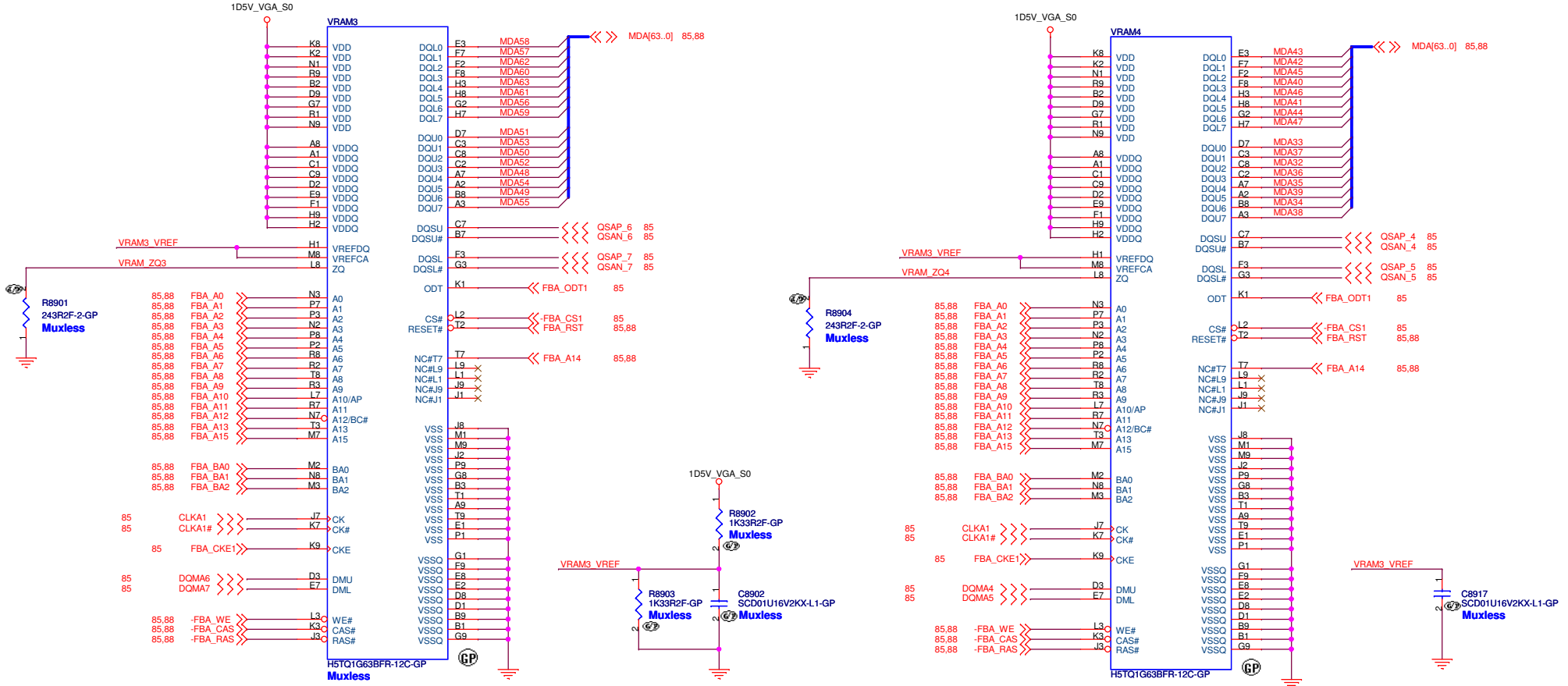
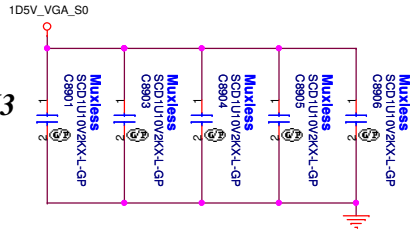
Title: GPU-VRAM1,2 (1/4)

Size: Custom | Document Number: Husk/Petra | Rev: -1

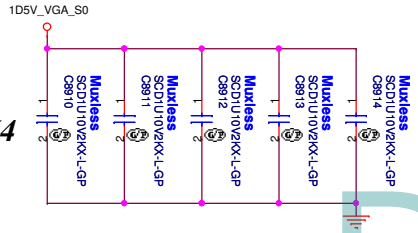
Date: Monday, March 05, 2012 | Sheet 88 of 103

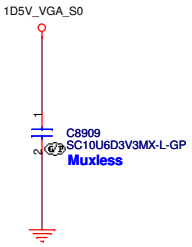


FOR VRAM3



FOR VRAM4





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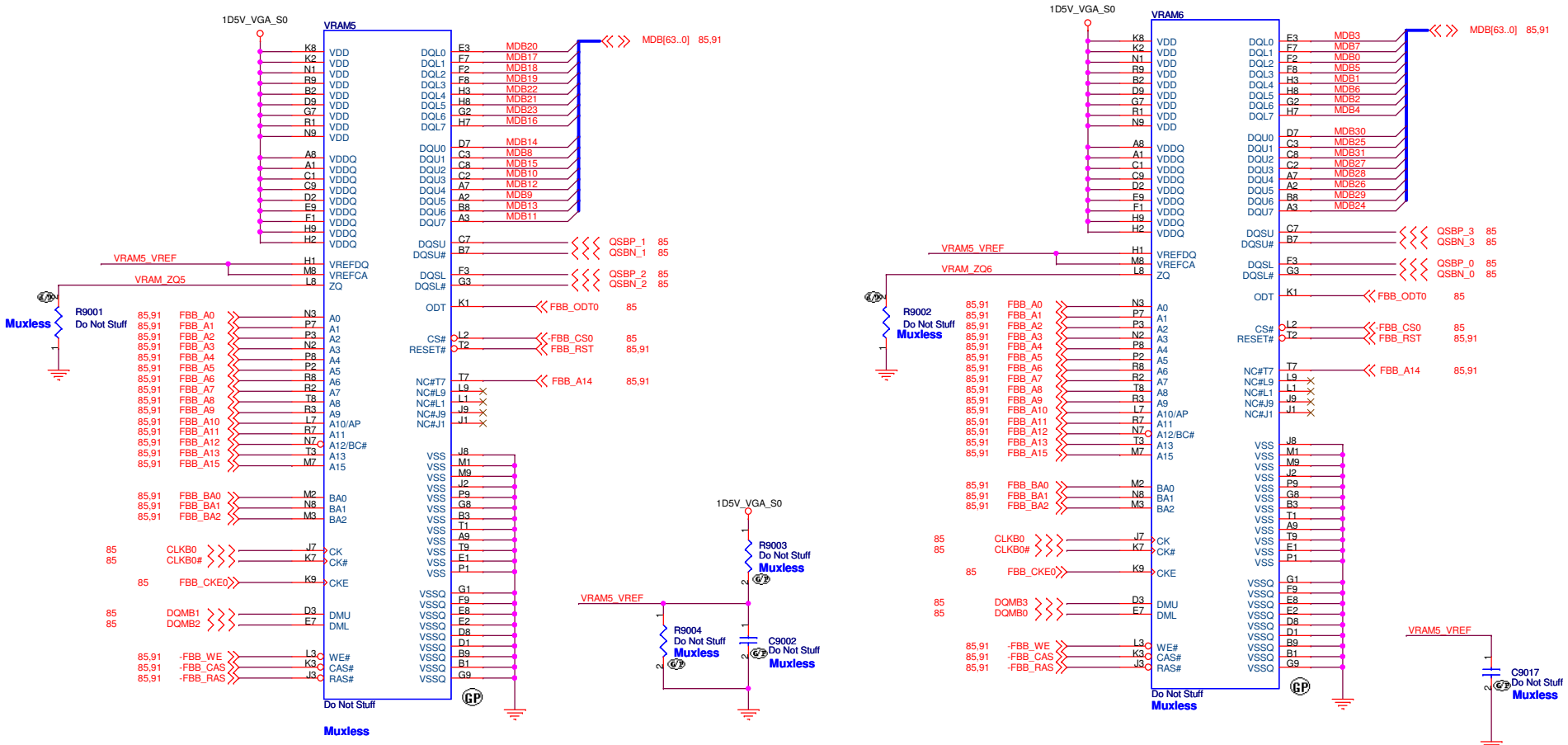
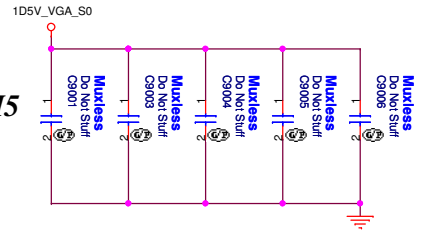
Title: **GPU-VRAM3,4 (2/4)**

Size: Custom | Document Number: Husk/Petra | Rev: -1

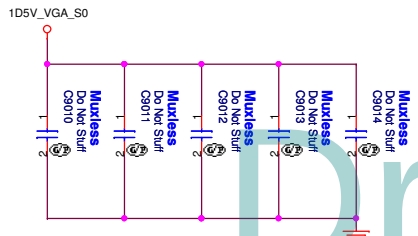
Date: Monday, March 05, 2012 | Sheet 89 of 103



FOR VRAM5



FOR VRAM6



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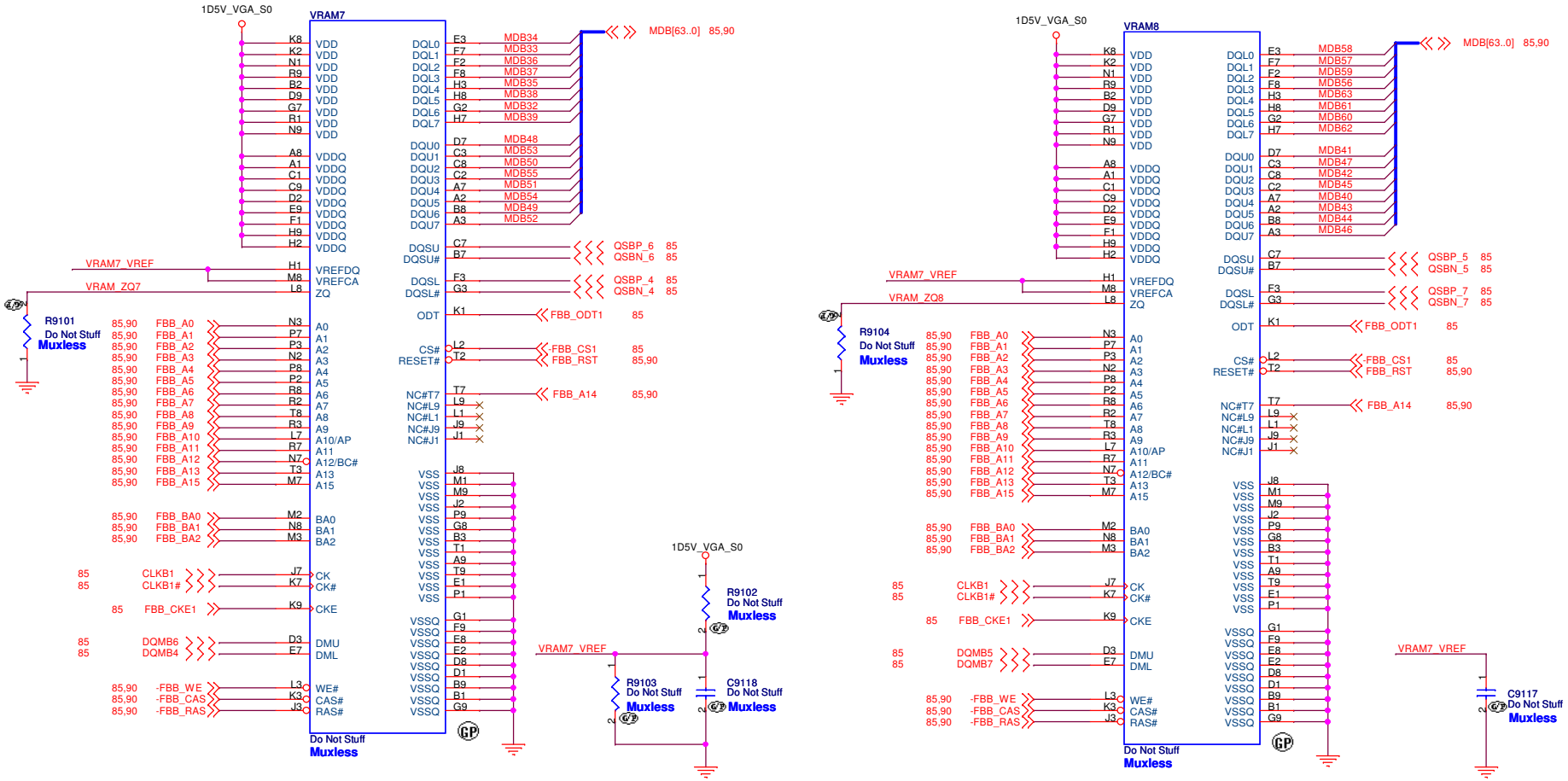
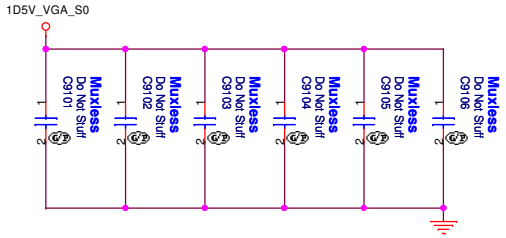
Title: **GPU-VRAM5,6 (3/4)**

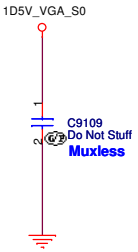
Size: Custom | Document Number: Husk/Petra | Rev: -1

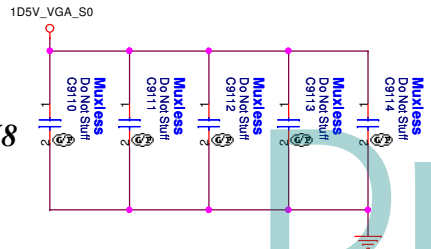
Date: Monday, March 05, 2012 | Sheet 90 of 103





FOR VRAM7





FOR VRAM8

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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **GPU-VRAM7,8 (4/4)**

Size	Document Number	Rev
Custom	Husk/Petra	-1

Date: Monday, March 05, 2012 Sheet 91 of 103

SSID = PWR.Plane.Regulator_GFX

Change power source Net
Wayler 12/07

		N13P-GS-LP 71.0N13P.00U	N13P-GL 71.0N13P.B0U	N13M-GS 71.0N13M.E0U
NVVDD Boot Voltage		0.9V VID[6:0]=0110000	0.975V VID[6:0]=0101010	0.875V VID[6:0]0110010
NV_VID1	PR9215	DY	63.10334.L0L	63.10334.L0L
	PR9230	63.10334.L0L	DY	DY
NV_VID3	PR9217	DY	63.10334.L0L	DY
	PR9232	63.10334.L0L	DY	63.10334.L0L
NV_VID4	PR9218	63.10334.L0L	DY	63.10334.L0L
	PR9233	DY	63.10334.L0L	DY

PR9218 Mount , PR9233 DY For N13M-GS Vboot = 0.875V

1 phase change 0ohm

Panasonic. 0.36uH 10*11.5*4
DCR=1.1mohm
Idc=17A, Isat=24A

Vga_core
Iccmax=24A
OCP>40A

Panasonic. 0.36uH 10*11.5*4
DCR=1.1mohm
Idc=17A, Isat=24A

1phase PR9261 mount
2phase PR9261 DY

1phase PR9259 , PR9260 mount
2phase PR9259 , PR9260 DY

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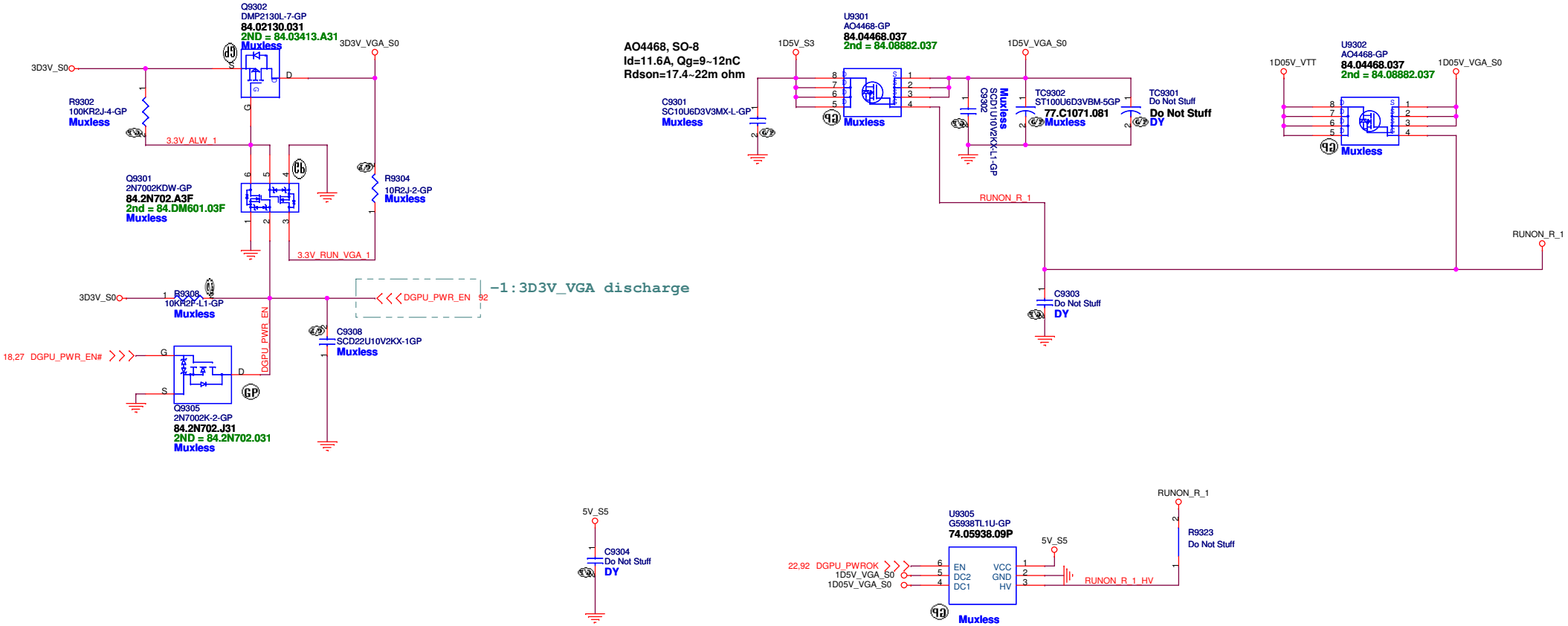
Title: TPS51728_VGA_CORE
Size: Document Number: Husk/Petra
Rev: -1
Date: Thursday, March 08, 2012 Sheet 92 of 103



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **DISCRETE VGA POWER**

Size	Document Number	Rev
Custom	Husk/Petra	-1
Date: Monday, March 05, 2012	Sheet 93 of 103	

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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: ***LVDS_Switch***

Size	Document Number	Rev
A4	**Husk/Petra**	**-1**

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Title: ***CRT_Switch***

Size: A3 | Document Number: **Husk/Petra** | Rev: **-1**

Date: Monday, March 05, 2012 | Sheet 95 of 103

SSID = SDIO

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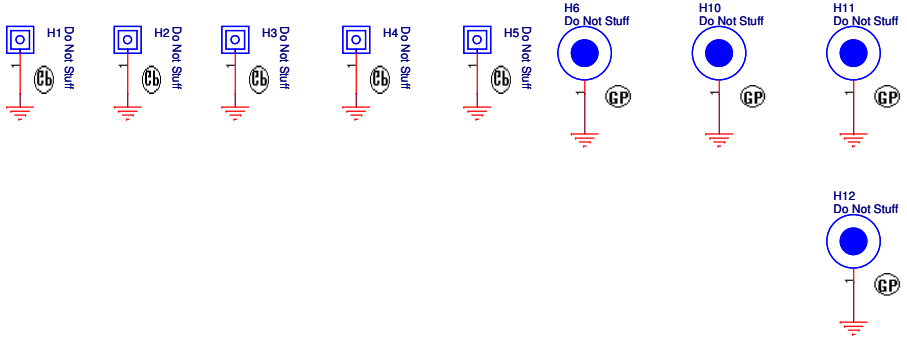
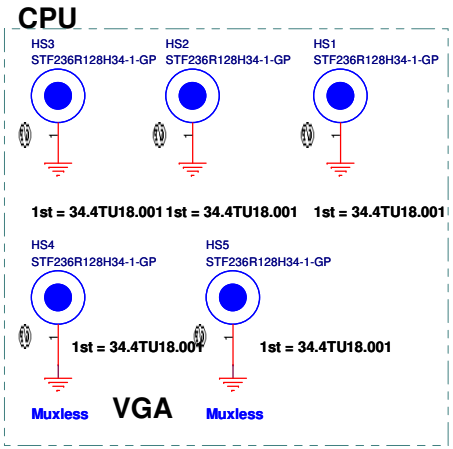
Title: TOUCH PANEL

Size	Document Number	Rev
A2	Husk/Petra	-1

Date: Monday, March 05, 2012 Sheet 96 of 103





-1:EC(34.4TU18.001)
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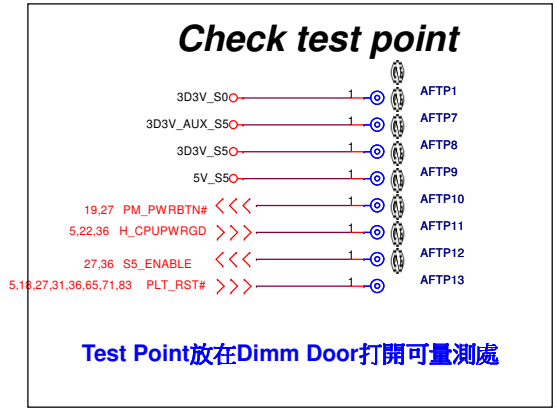
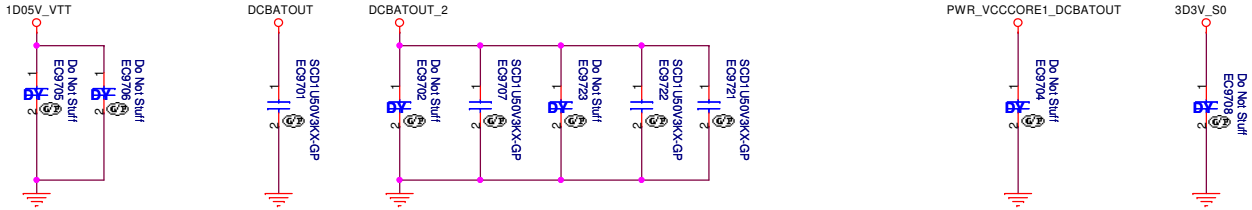
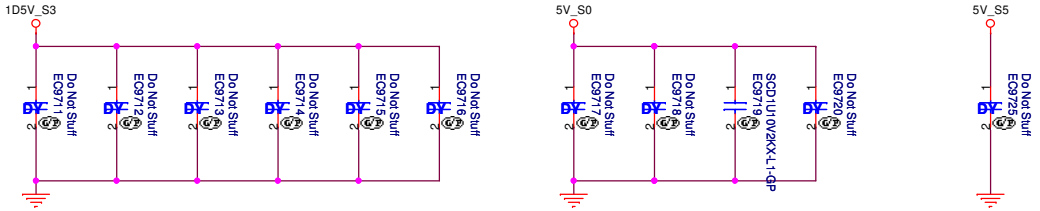
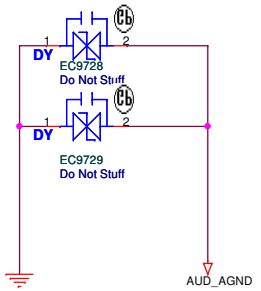
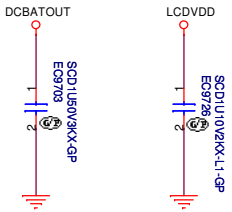


Test Point放在Dimm Door打開可量測處









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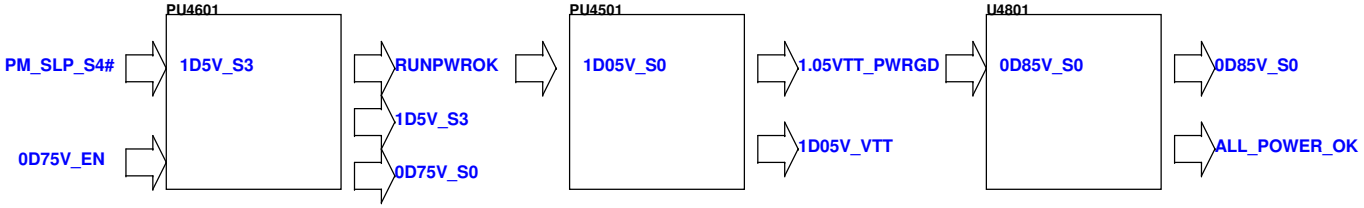
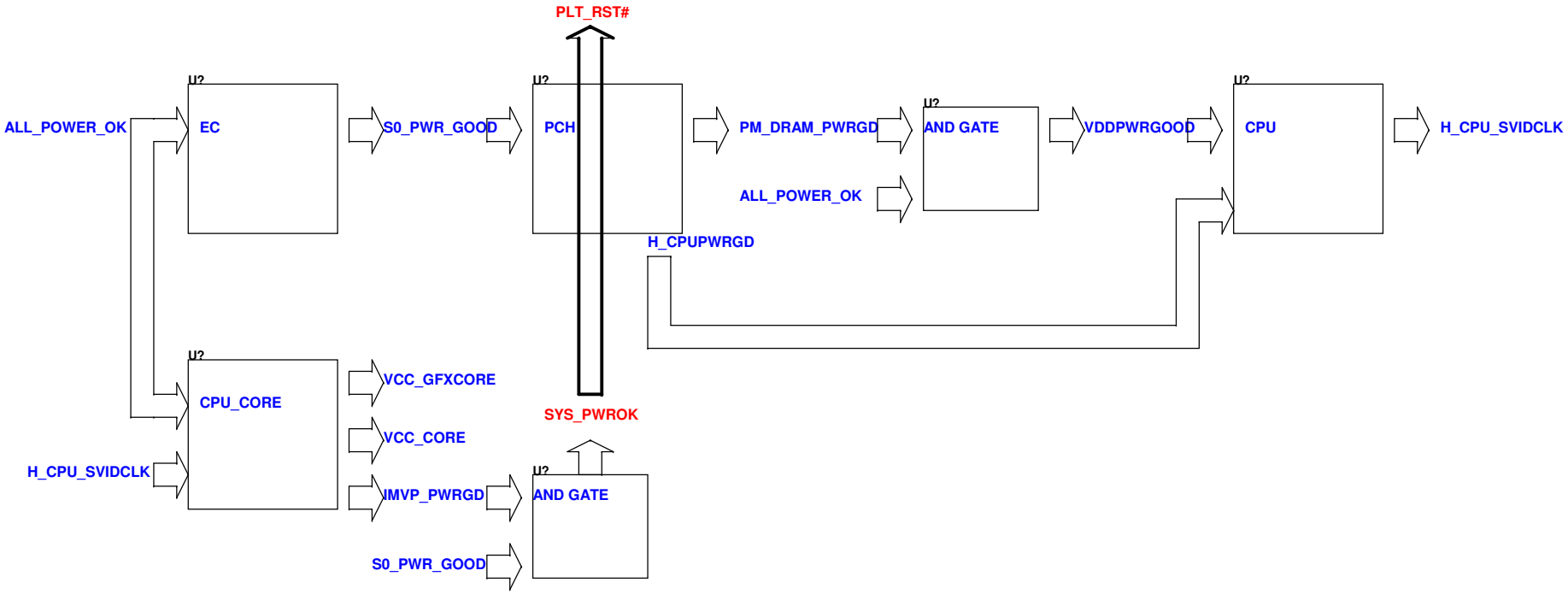
Title: UNUSED PARTS/EMI Capacitors

Size: A3 | Document Number: Husk/Petra | Rev: -1

Date: Thursday, March 08, 2012 | Sheet 97 of 103

Power Sequence





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Title: Change History

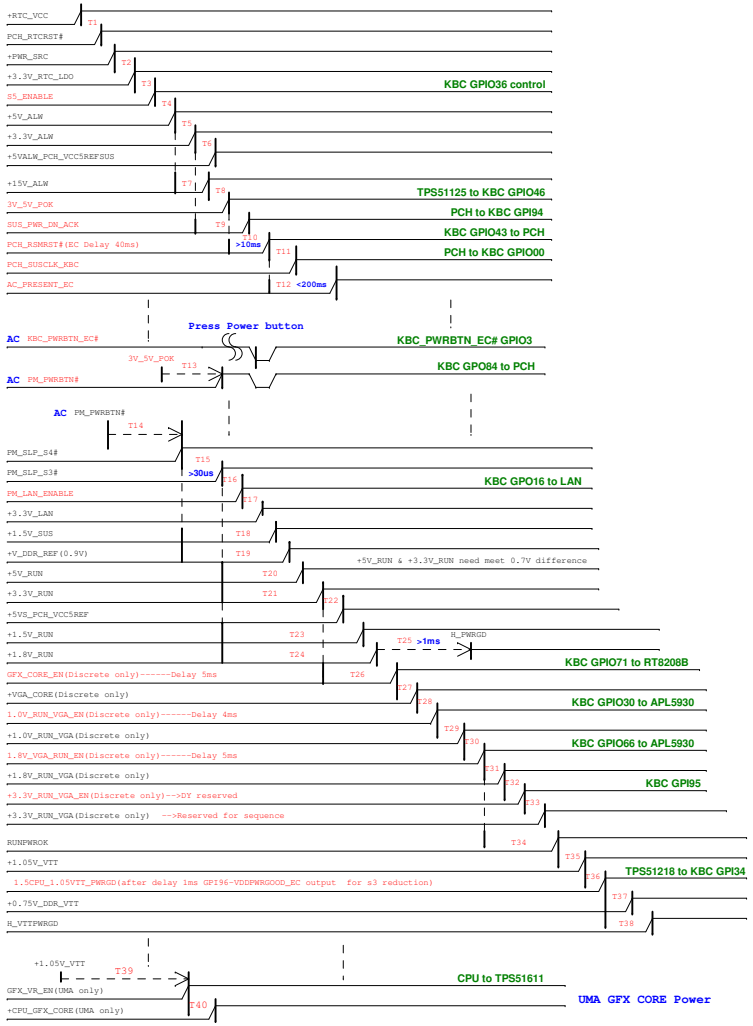
Size	Document Number	Rev
A3	Husk/Petra	-1

Date: Monday, March 05, 2012 Sheet 98 of 103

Intel-Power Up Sequence

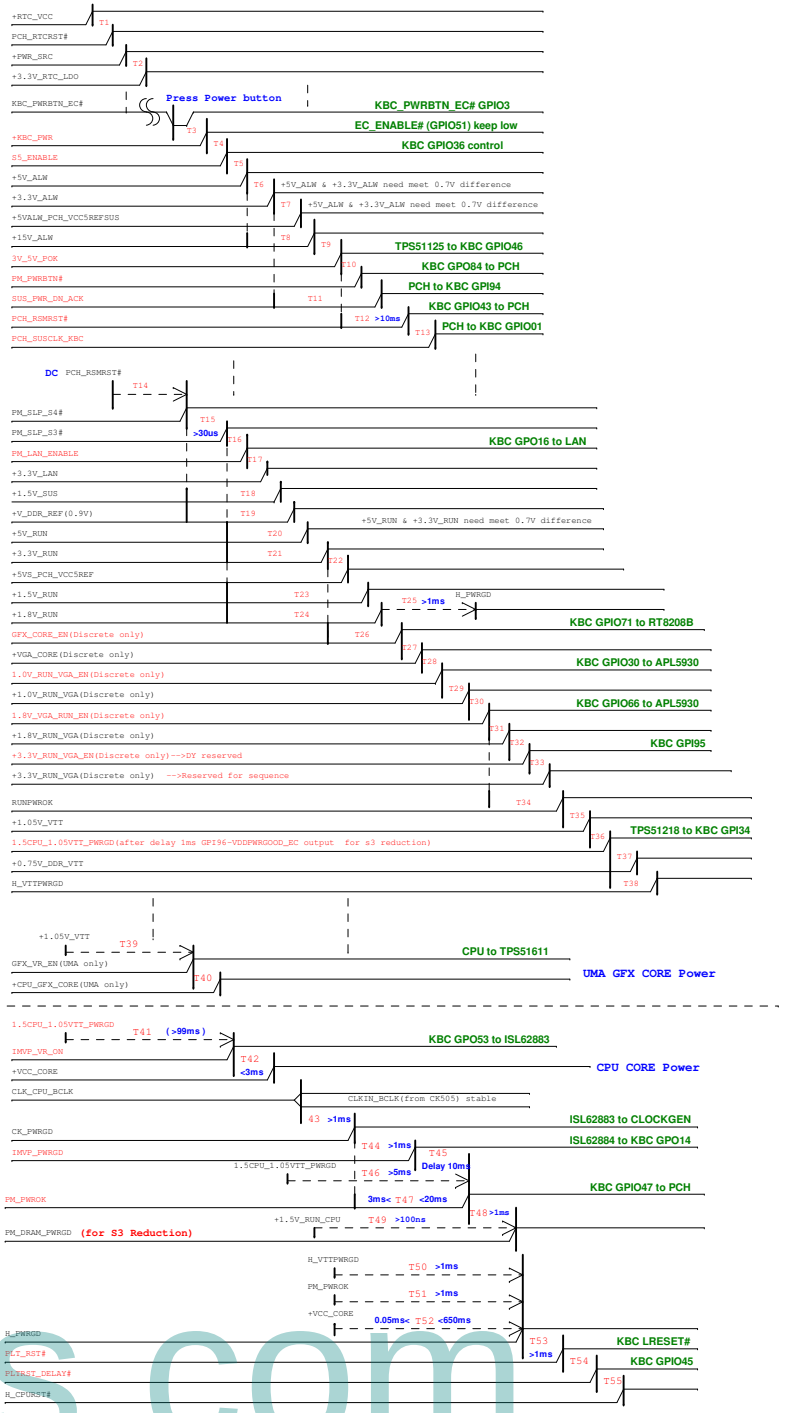
(AC mode)

red word: KBC GPIO



(DC mode)

red word: KBC GPIO



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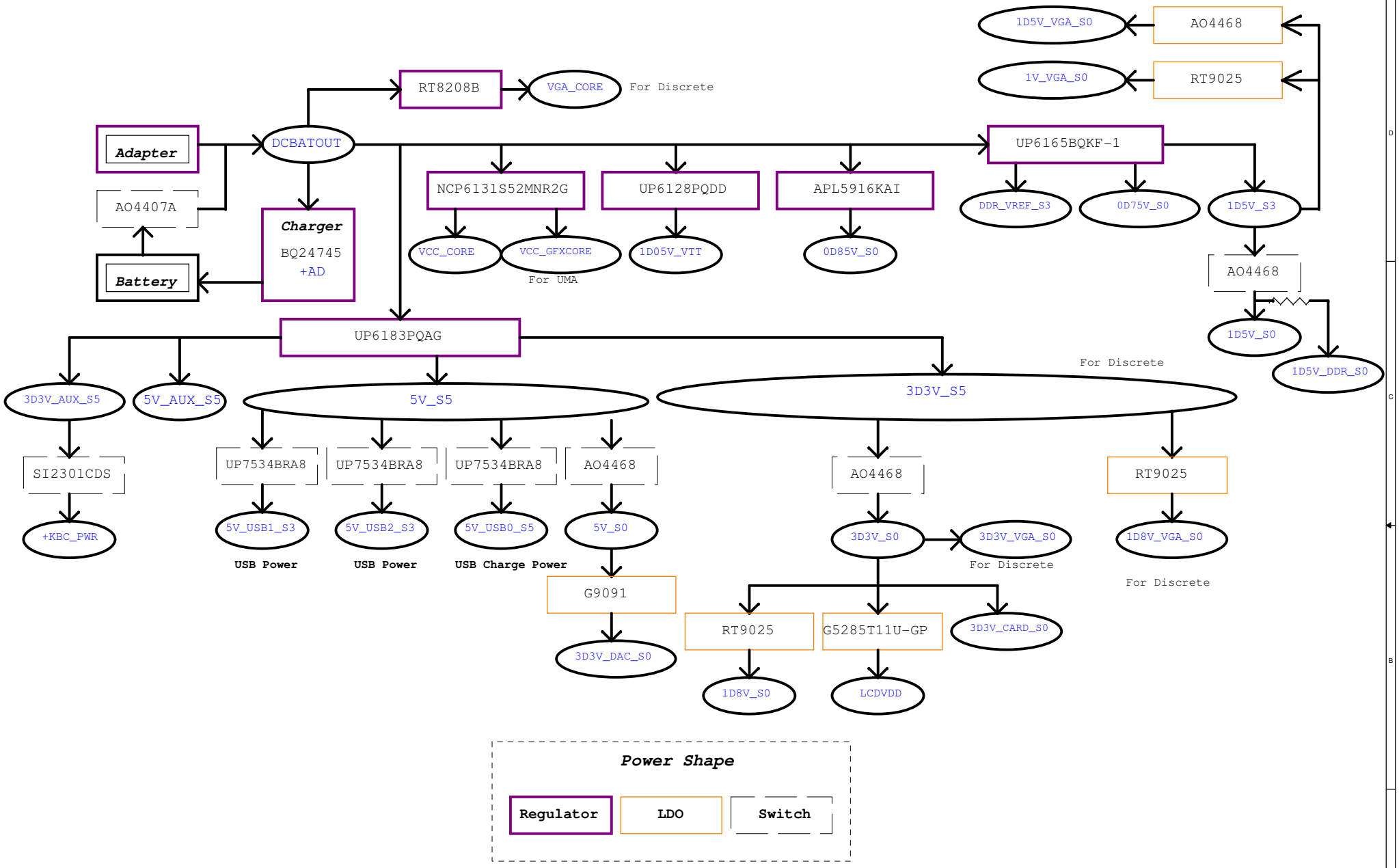
Title: Power Sequence
Size: M | Document Number: Husk/Petra | Rev: -1
Date: Monday, March 05, 2012 | Sheet 59 of 103



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Title: **Power Block Diagram**

Size	Document Number	Rev
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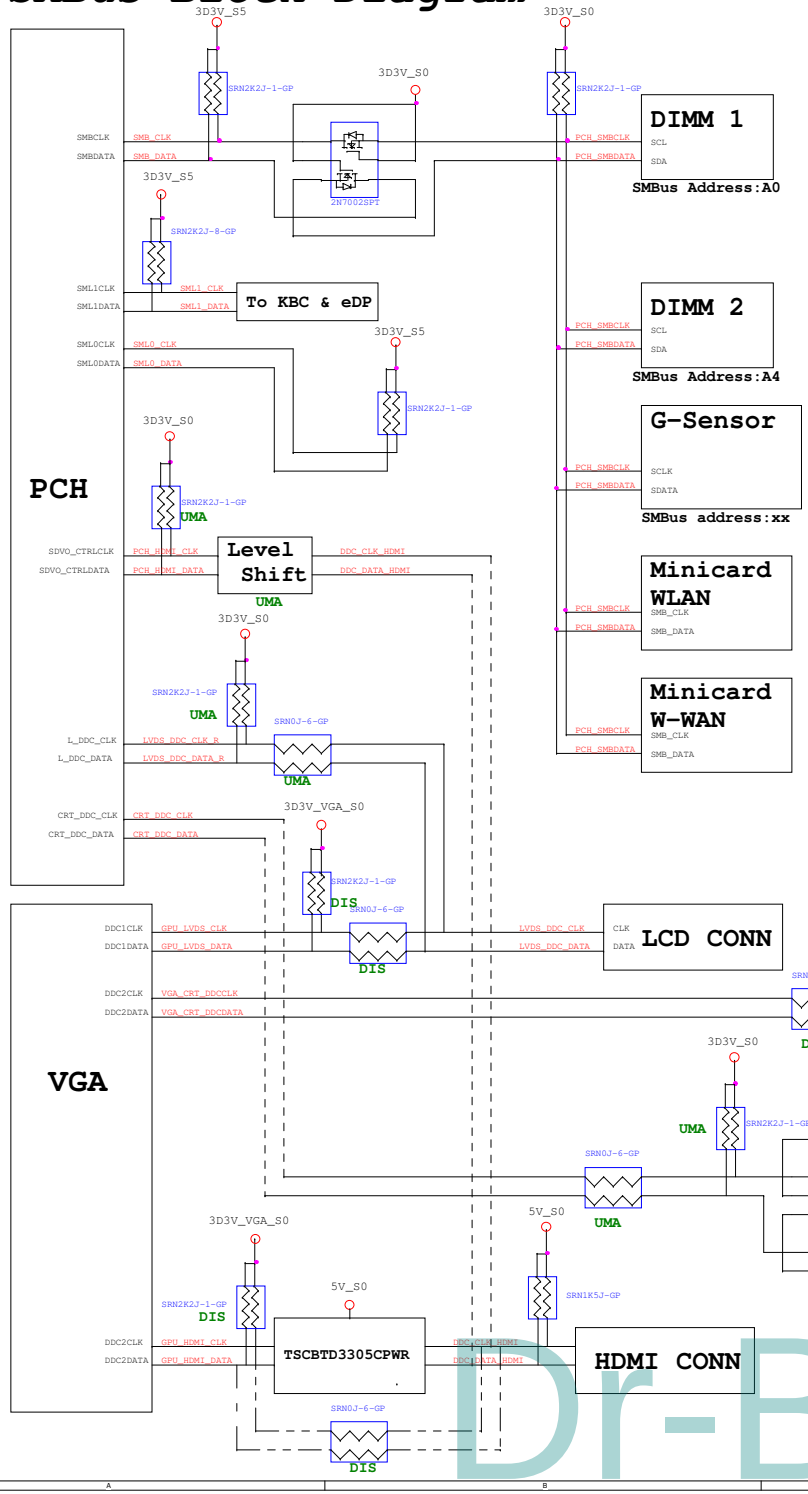
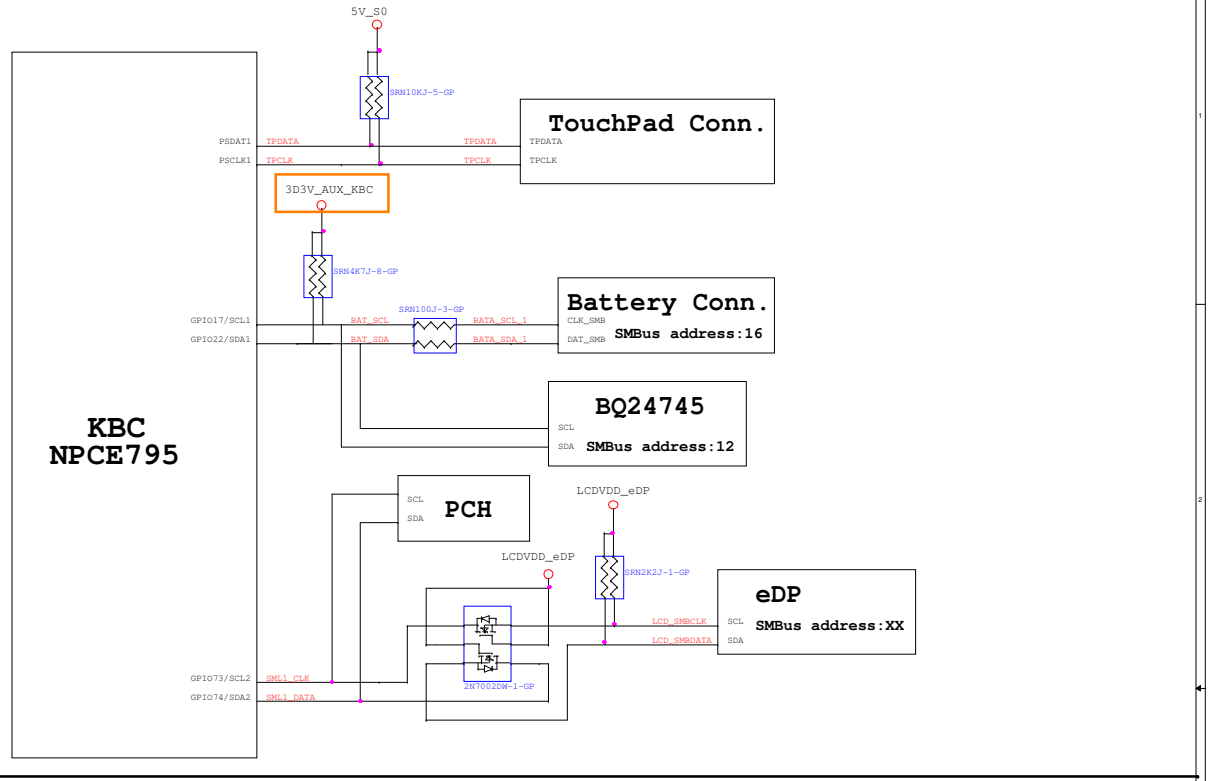
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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Title: SMBUS Block Diagram

Size: A2 | Document Number: Husk/Petra | Rev: -1

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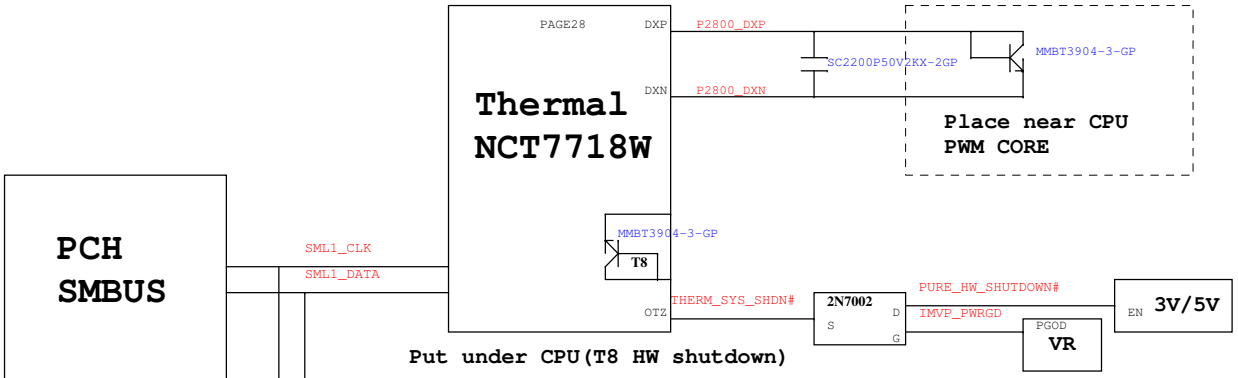
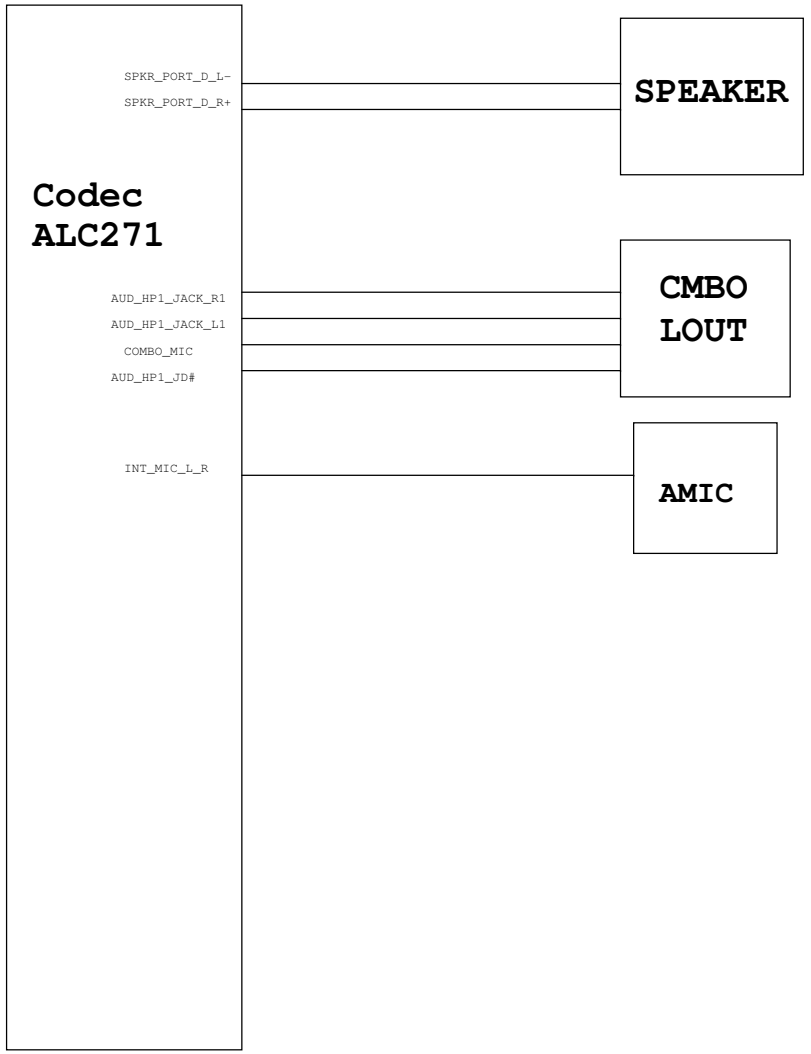
Thermal Block Diagram



Audio Block Diagram



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Title: Thermal/Audio Block Diagram

Size	Document Number	Rev
Custom	Husk/Petra	-1

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