

# Husk/Petra UMA/Muxless Schematics Document Ivy Bridge Intel PCH

*DY :None Installed*  
*DIS:DIS installed*  
*DIS\_Muxless :BOTH DIS or Muxless installed*  
*DIS\_PX:BOTH DIS or PX installed*  
*DIS\_PX\_Muxless:DIS or PX or Muxless installed.*  
*Muxless: Muxless installed.(PX4.0)*  
*PX:MUX installed.(PX3.0)*  
*PX\_Muxless:BOTH PX or Muxless installed.*  
*UMA:UMA installed*  
*UMA\_Muxless:BOTH UMA or Muxless installed*  
*UMA\_PX\_Muxless:UMA or PX or Muxless installed*

*ANNIE: ONLY FOR ANNIE solution.*  
*PSL: KBC795 PSL circuit for 10mW solution installed.*  
*10mW: External circuit for 10mW solution installed.*  
*65W: for 65W adaptor installed.*  
*90W: for 90W adaptor installed.*

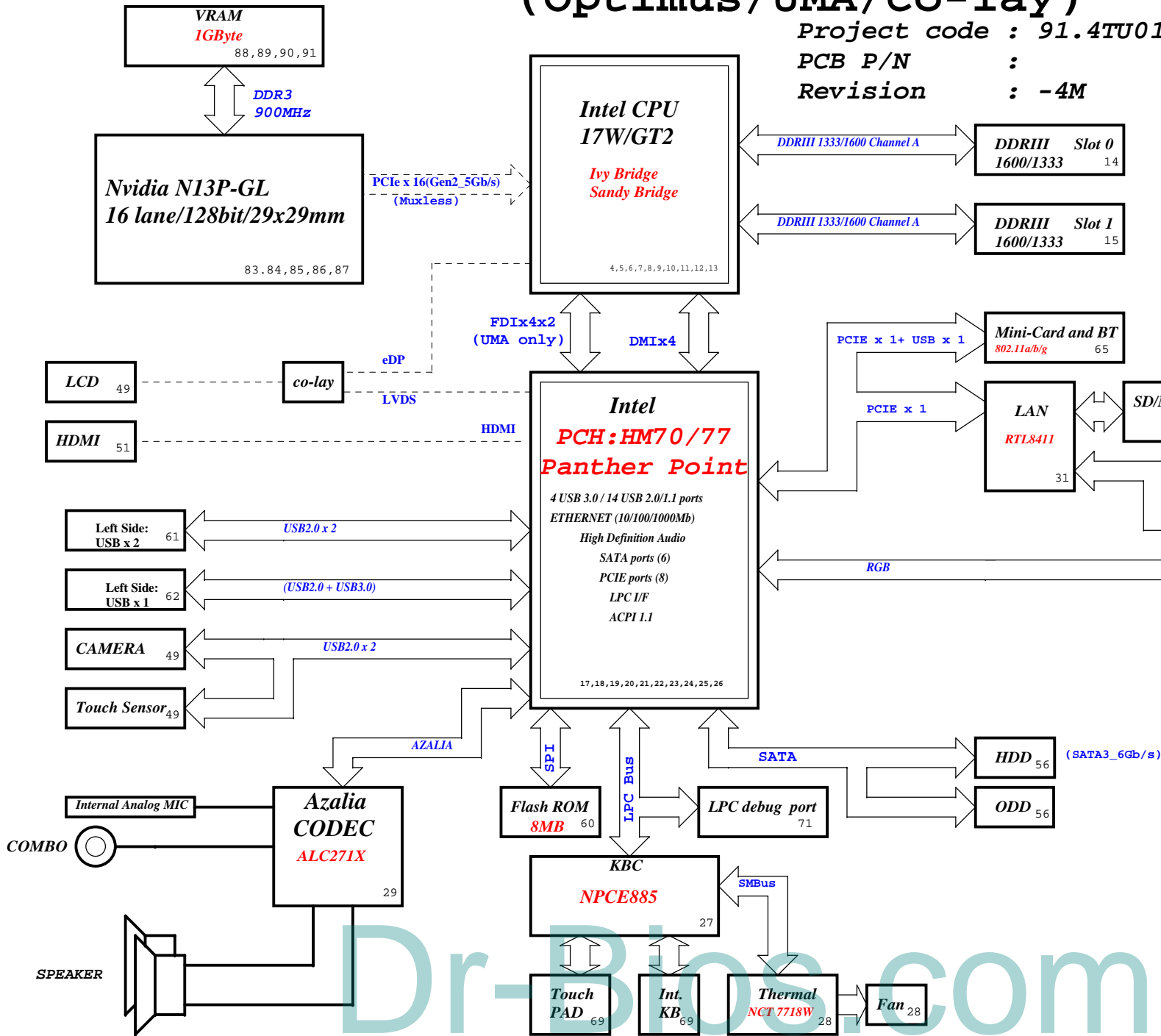
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DIS IVB Touch

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Title			
<b>Cover Page</b>			
Size A3	Document Number	Rev	
	<b>Husk/Petra</b>	<b>-4M</b>	
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# Husk and Petra Block Diagram (Optimus/UMA/co-lay)

Project code : 91.4TU01.001  
PCB P/N :  
Revision : -4M



<b>CHARGER</b> BQ24727 40	
INPUTS	OUTPUTS
DCBATOUT	BT+
<b>SYSTEM DC/DC</b> RT8223MGQW 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5
<b>CPU DC/DC</b> ISL95836HRTZ 42~43	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
<b>SYSTEM DC/DC</b> ISL95836HRTZ 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE
<b>SYSTEM DC/DC</b> TPS51218DSCR 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT
<b>SYSTEM DC/DC</b> RT8207LGQW 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3
<b>LDO</b> RT9025-25ZSP 47	
INPUTS	OUTPUTS
3D3V_S0	1D8V_S0
<b>LDO</b> G978 48	
INPUTS	OUTPUTS
1D05_VTT	0D85V_S0
<b>VGA</b> ISL62882CHRTZ 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE
<b>Switches</b> 93	
INPUTS	OUTPUTS
3D3V_S0	3D3V_VGA_S0
1D05V_VTT	1D05V_VGA_S0
1D5V_S3	1D5V_VGA_S0
<b>PCB LAYER</b>	
L1:Top	L4:Signal
L2:VCC	L5:GND
L3:Signal	L6:Bottom

DIS I/VB Touch

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Title: **Block Diagram**

Size A3 Document Number **Husk/Petra** Rev **-4M**

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Name	Schematics Notes
SPKR	<b>Reboot option at power-up</b> Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	<b>Enable Danbury:</b> Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. <b>Disable Danbury:</b> left floating, no pull-down required.
NV_ALE	<b>Enable Danbury:</b> Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] <b>Disable Danbury:</b> leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	<b>Default = Do not connect (floating)</b> High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

**USB Table**

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA / USB CHARGER
9	USB Ext. port 2
10	EDP CAMERA
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

**SATA Table**

SATA	
Pair	Device
0	HDD1
1	HDD2
2	N/A
3	N/A
4	ODD
5	ESATA

**PCIE Routing**

LANE1	Mini Card2(WWAN)
LANE2	Mini Card1(WLAN)
LANE3	Card Reader
LANE4	Onboard LAN
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	New Card

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	<b>PCI-Express Static Lane Reversal</b>	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		Disabled - No Physical Display Port attached to 1: Embedded DisplayPort. Enabled - An external Display Port device is connect to the EMBEDDED display Port 0:	0
CFG[6:5]	<b>PCI-Express Port Bifurcation Straps</b>	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	<b>PEG DEFER TRAINING</b>	1: PEG Train immediately following XXRESETB de assertion 0: PEG Wait for BIOS for training	1

POWER PLANE	VOLTAGE	Voltage Rails	
		ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_SFPCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW_Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

**SMBus ADDRESSES**

I <sup>2</sup> C / SMBus Addresses	Ref Des	HURON RIVER ORB	
		Address	Hex Bus
EC SMBus 1 Battery CHARGER		BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA	
EC SMBus 2 PCH eDP		SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA	
PCH SMBus SO-DIMM (SPD) SO-DIMM (SPD) Digital Pot G-Sensor MINI		PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK	

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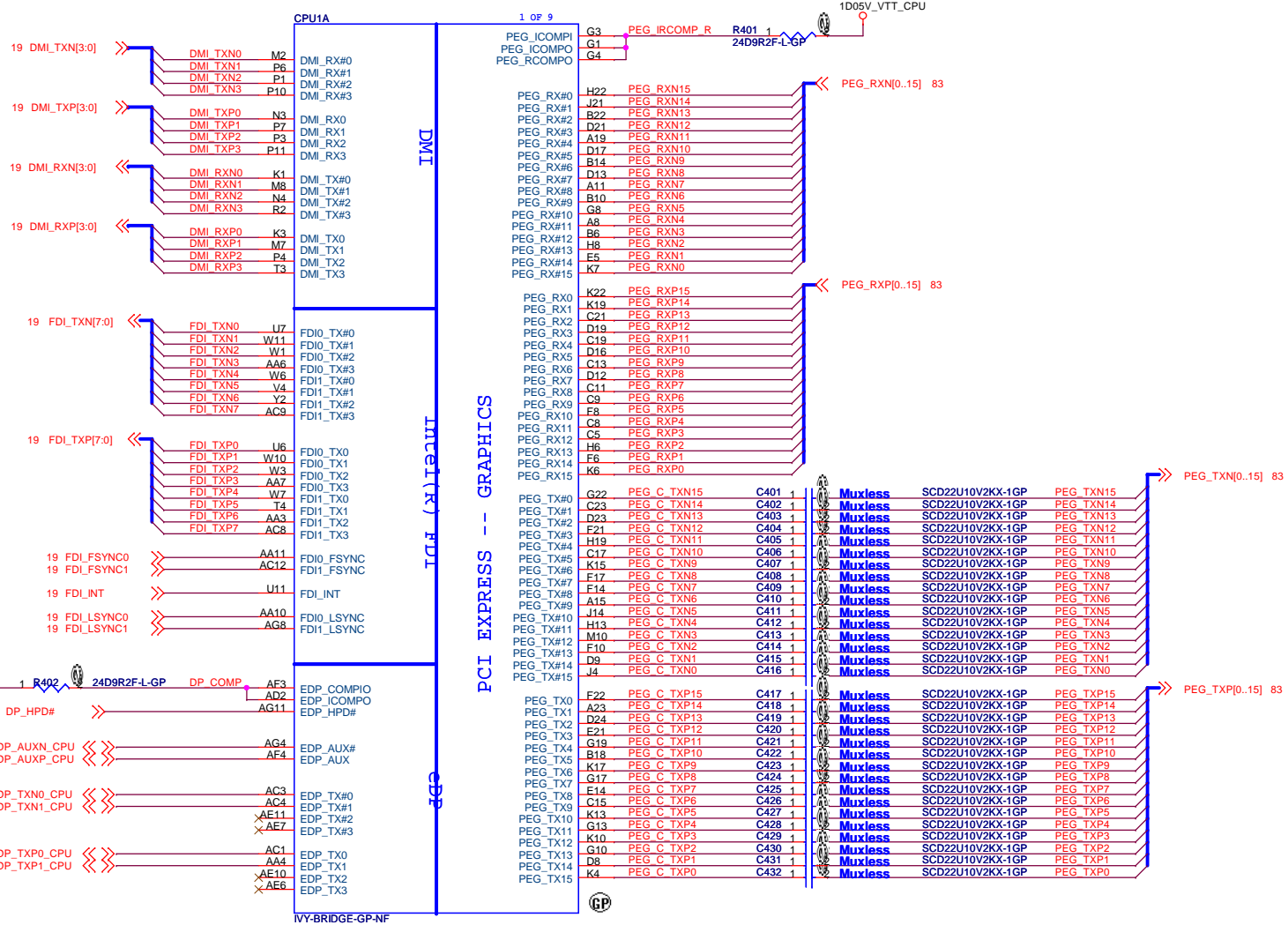
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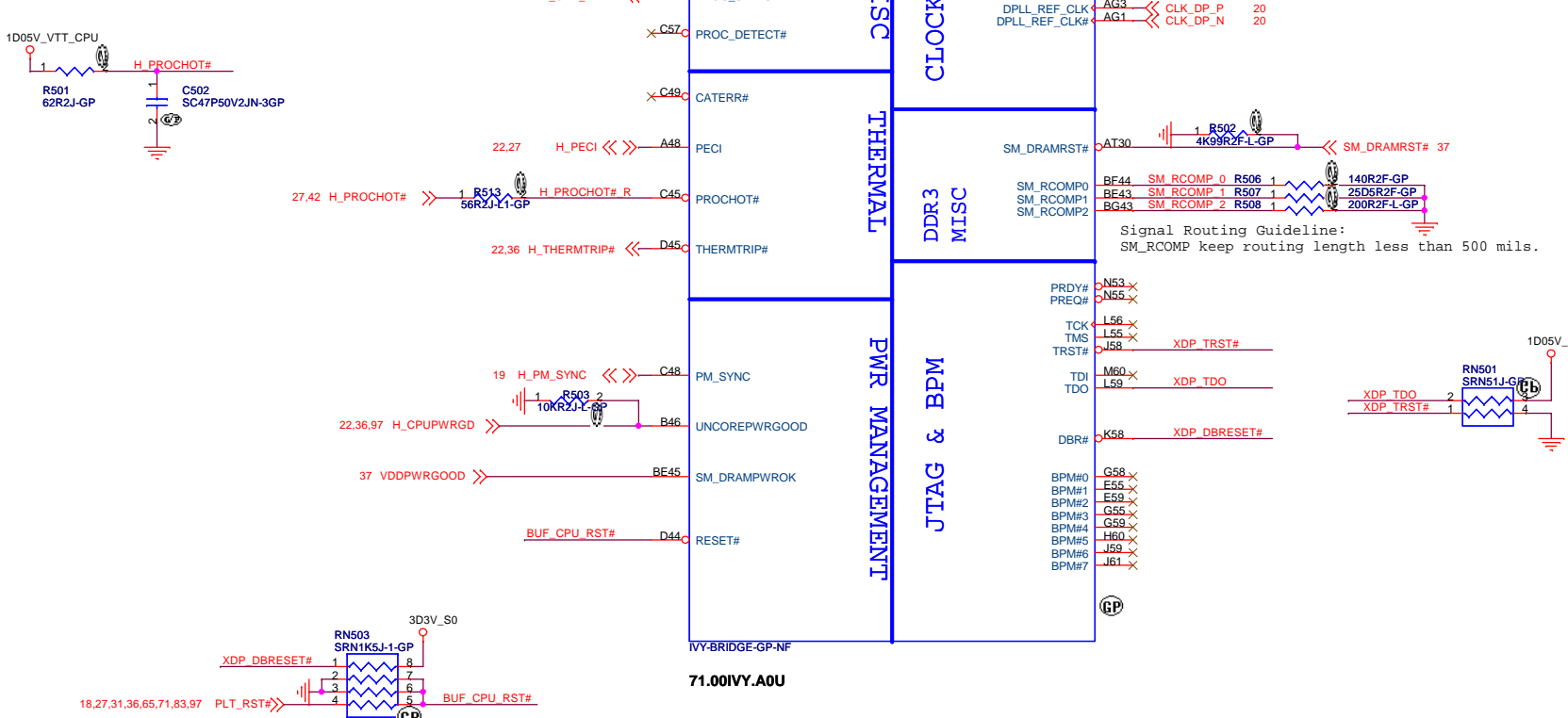
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SSID = CPU



SSID = CPU



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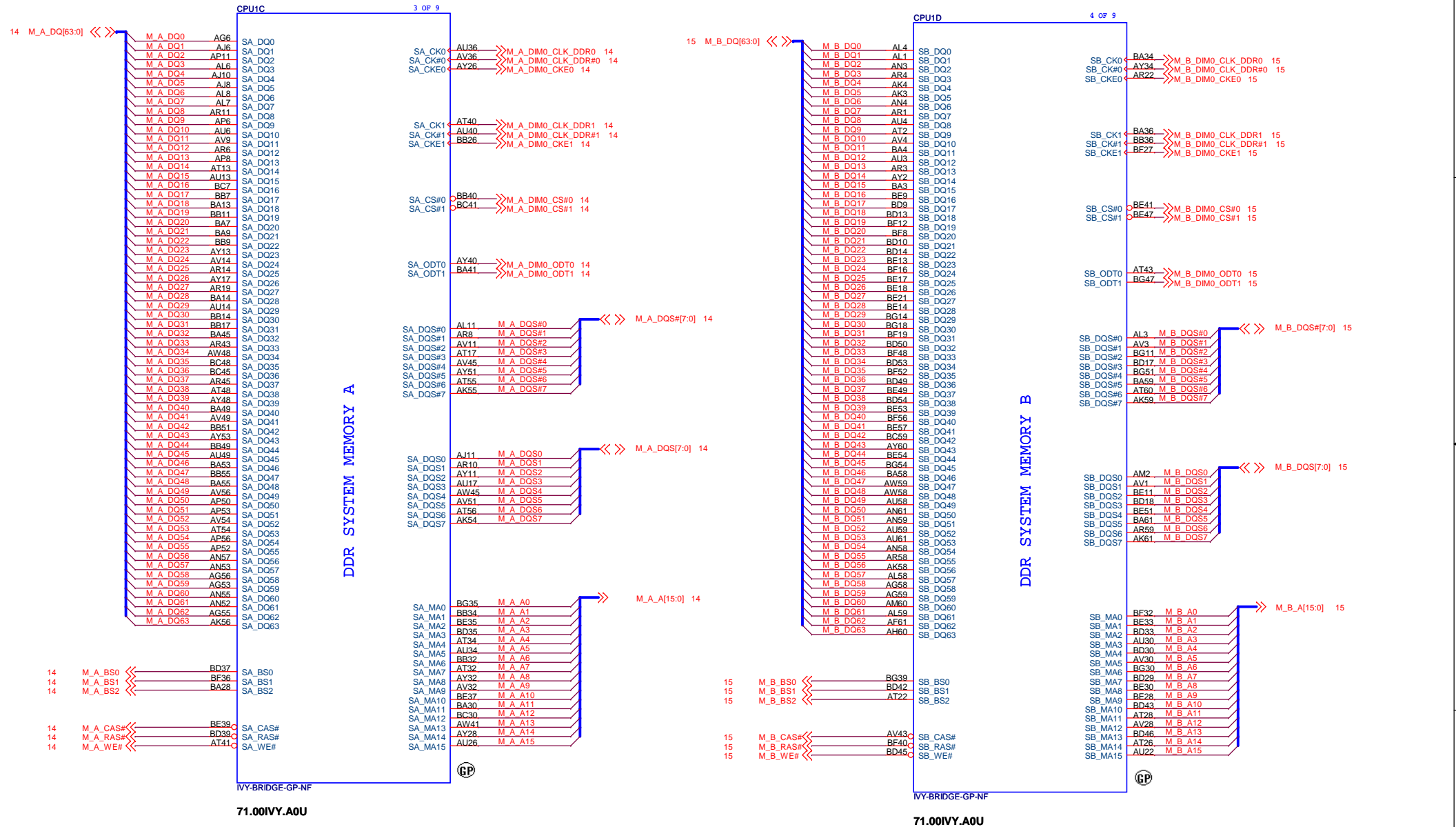
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Title **CPU (THERMAL/CLOCK/PM)**

Size Custom	Document Number <b>Husk/Petra</b>	Rev <b>-4M</b>
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SSID = CPU



71.00IVY.A0U

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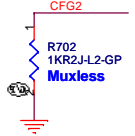
Title CPU (DDR)

Size A3 Document Number Husk/Petra Rev -4M

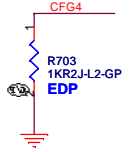
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# SSID = CPU

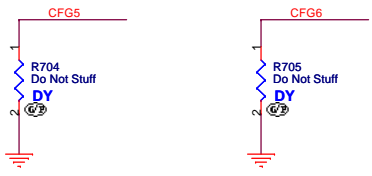
PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed



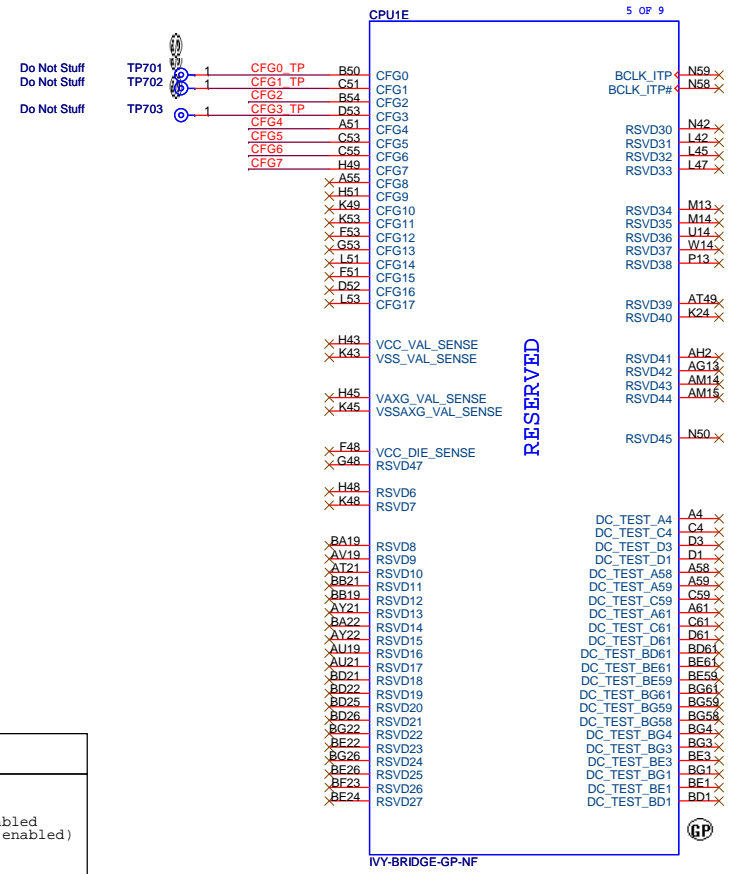
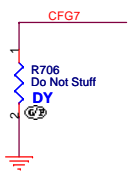
Enabl EDP function	
CFG4	1: Disable 0: Enable



PCIe Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



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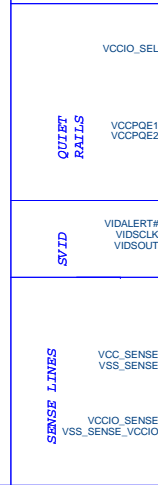
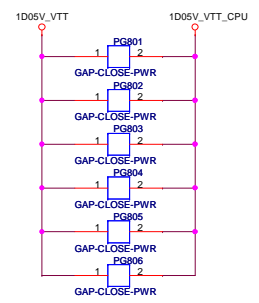
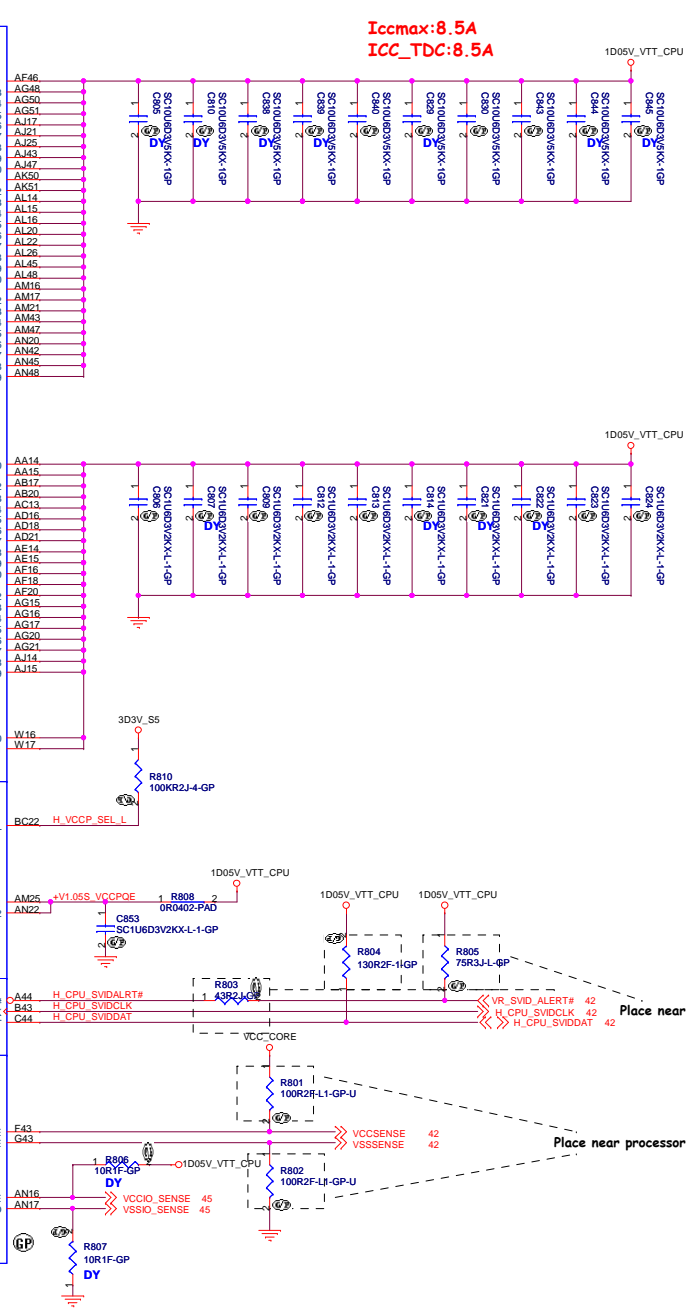
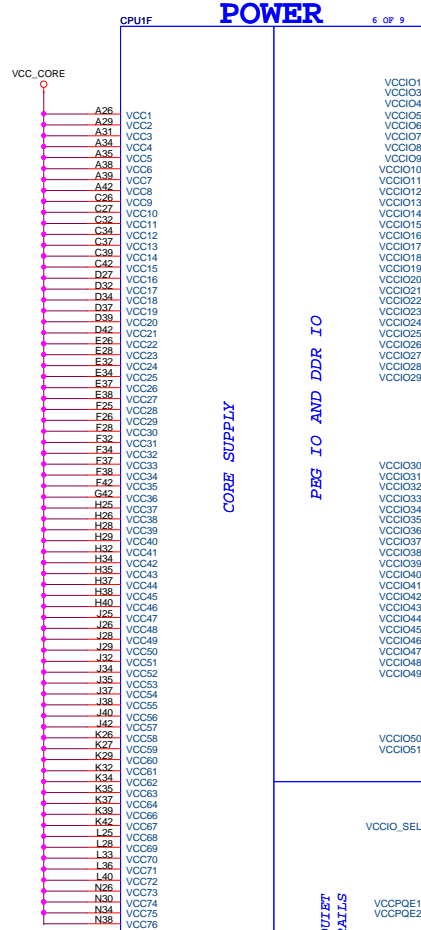
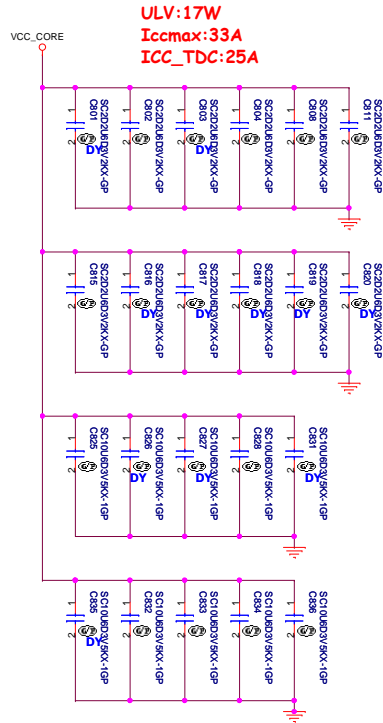
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Title: **CPU (RESERVED)**

Size A3 Document Number: **Husk/Petra** Rev: **-4M**

Date: Thursday, September 06, 2012 Sheet 7 of 103

SSID = CPU



Place near processor

Place near processor

HY-BRIDGE-GP-NF  
71.00IVY.A0U

DS-IB Touch

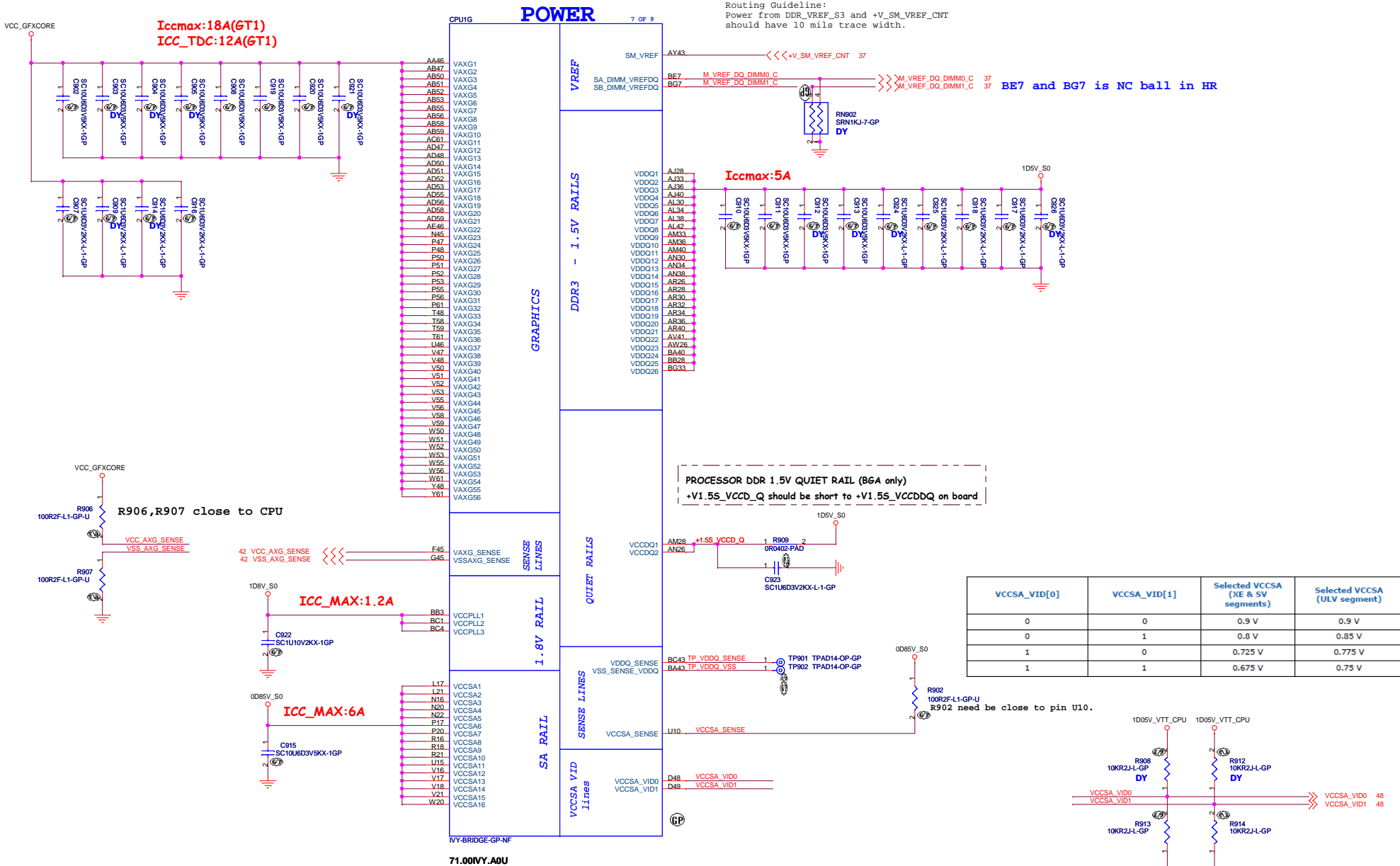
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Title			<b>CPU (VCC CORE)</b>
Size	Document Number	Rev	
Custom	<b>Husk/Petra</b>	<b>-4M</b>	
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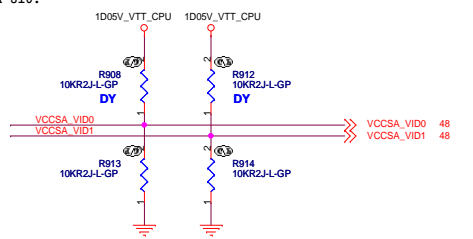


Routing Guideline:  
Power from DDR\_VREF\_S3 and +V\_SM\_VREF\_CNT should have 10 mils trace width.



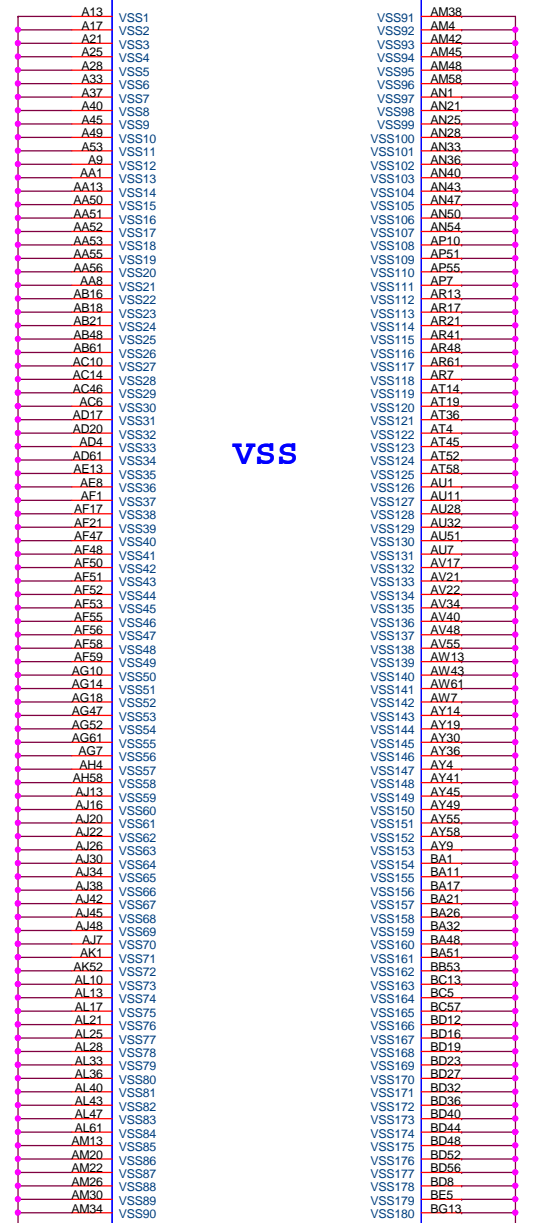
PROCESSOR DDR 1.5V QUIET RAIL (B6A only)  
+V1.5S\_VCCD\_Q should be short to +V1.5S\_VCCDDQ on board

VCCSA_VID[0]	VCCSA_VID[1]	Selected VCCSA (XE & SV segments)	Selected VCCSA (ULV segment)
0	0	0.9 V	0.9 V
0	1	0.8 V	0.85 V
1	0	0.725 V	0.775 V
1	1	0.675 V	0.75 V



SSID = CPU

CPU1H 8 OF 9

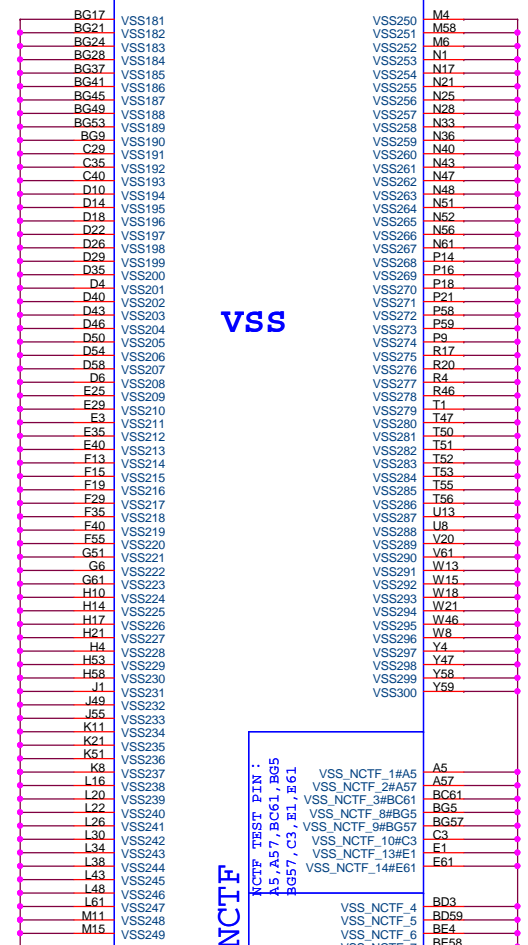


IVY-BRIDGE-GP-NF

71.00IVY.A0U



CPU1I 9 OF 9



IVY-BRIDGE-GP-NF

71.00IVY.A0U

VSS

NCTF

NCTF TEST PIN :

A5, A57, EC61, BG5	VSS_NCTF_1#A5	A5
BG57, C3, E1, E61	VSS_NCTF_2#A57	A57
	VSS_NCTF_3#BC61	BC61
	VSS_NCTF_8#BG5	BG5
	VSS_NCTF_9#BG57	BG57
	VSS_NCTF_10#C3	C3
	VSS_NCTF_13#E1	E1
	VSS_NCTF_14#E61	E61
	VSS_NCTF_4	BD3
	VSS_NCTF_5	BD59
	VSS_NCTF_6	BE4
	VSS_NCTF_7	BE58
	VSS_NCTF_11	C58
	VSS_NCTF_12	D59



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<b>XDP</b>			
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A4	<b>Husk/Petra</b>	<b>-4M</b>
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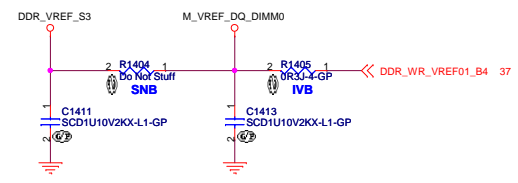
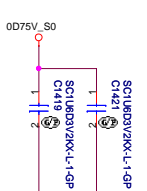
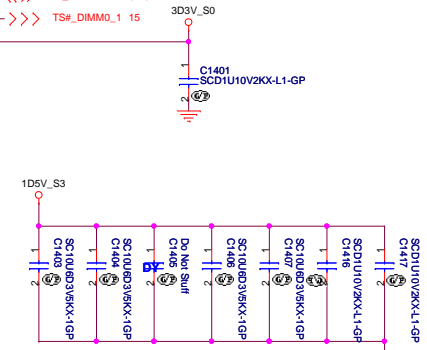
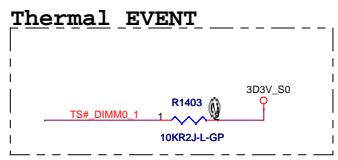
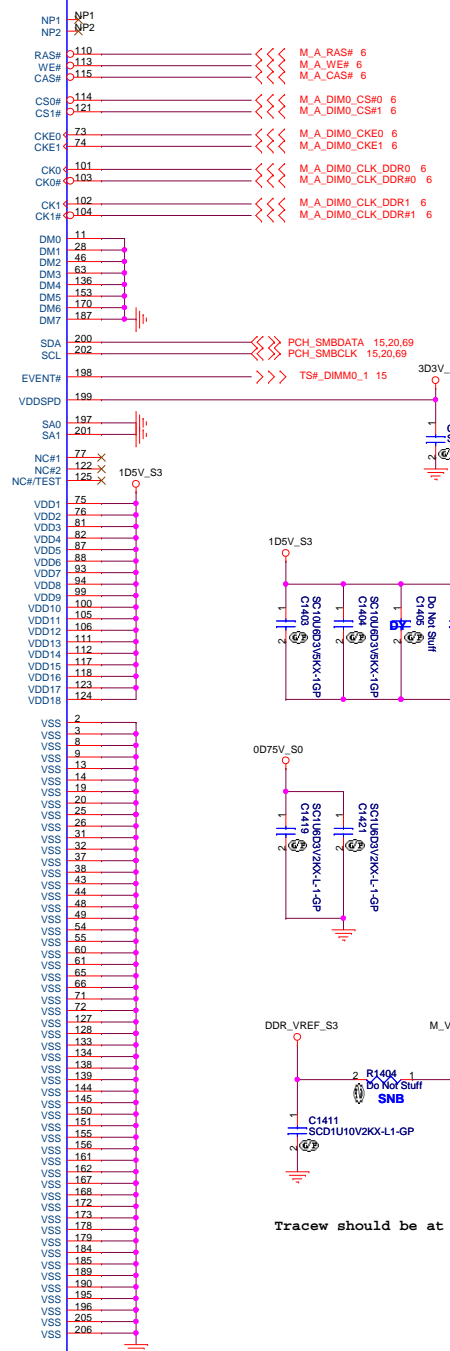
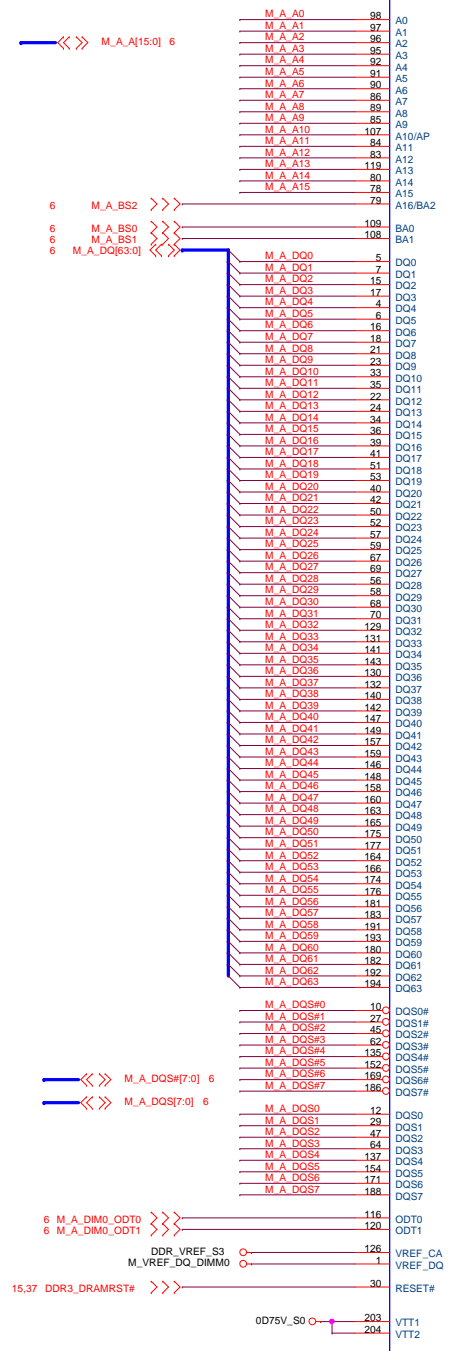
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**SSID = MEMORY**



Trace width should be at least 20 mils wide

DM1  
DDR3-204P-122-GP  
62.10017.Z51  
2nd = 62.10017.M51  
3rd = 62.10024.G21

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Title: **DDR3-SODIMM1**

Size: Custom Document Number: Husk/Petra Rev: -4M

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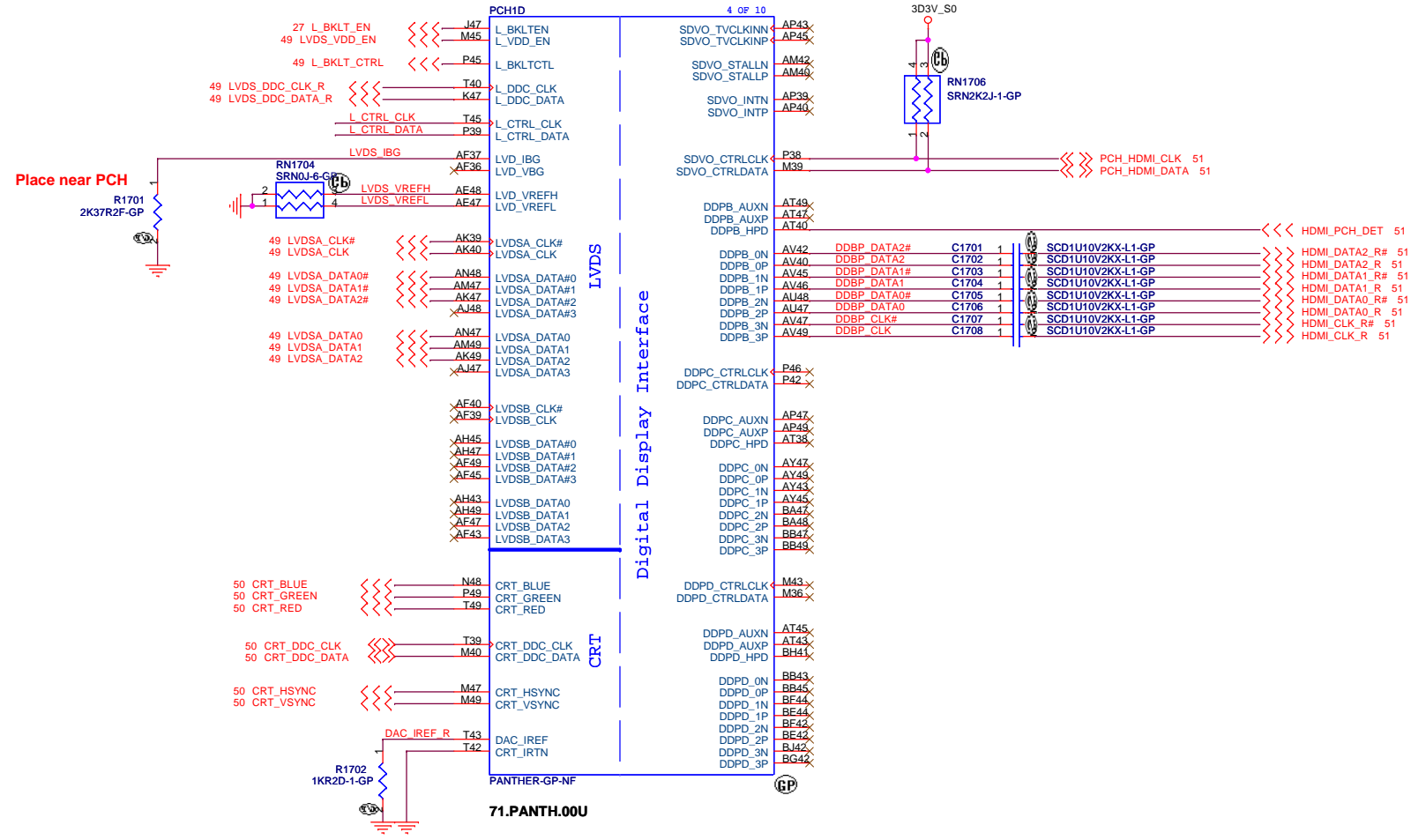
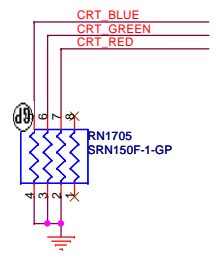
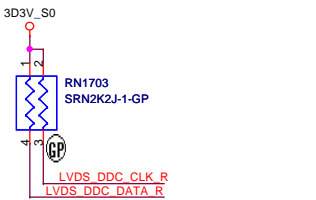
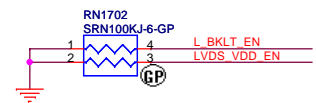
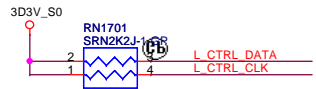
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Title **DDR3-SODIMM2**

Size A4 Document Number **Husk/Petra** Rev **-4M**

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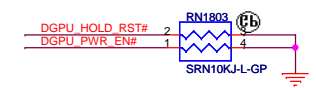
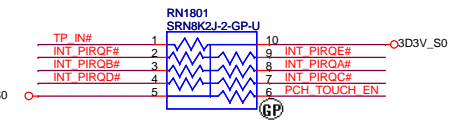
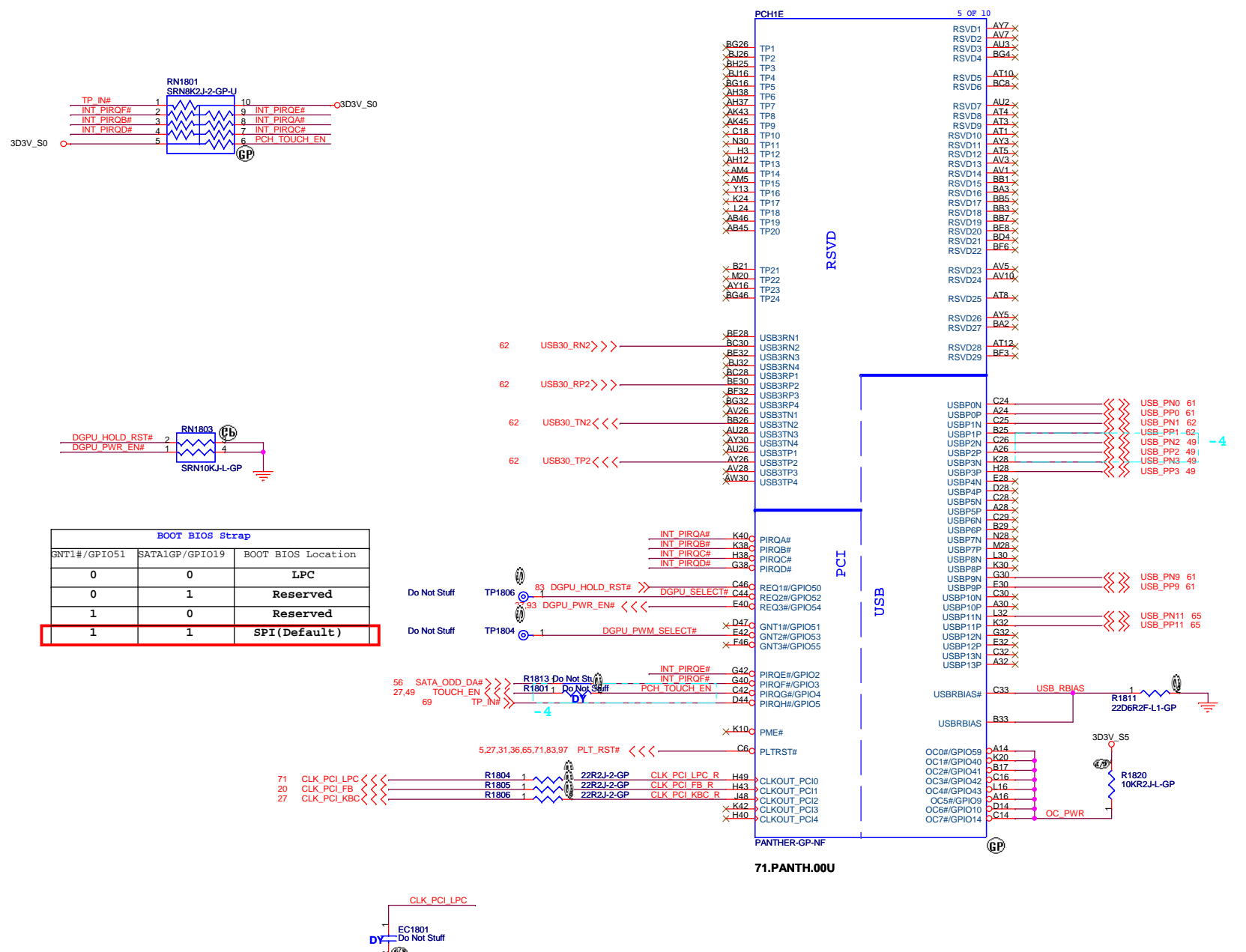
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Title: **PCH (LVDS/CRT/DDI)**

Size A3 Document Number: **Husk/Petra** Rev: **-4M**

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BOOT BIOS Strap		
SNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

USB Table

Pair	Device
0	USB2.0 Ext. port 1
1	USB3.0/USB2.0 Ext. port 2
2	Touch panel
3	CCD
4	
5	
6	may not be available
7	may not be available
8	
9	USB2.0 Ext. port 3
10	
11	Mini Card1 (WLAN+BT)
12	
13	

DIS I/B Touch

**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (PCI/USB/NVRAM)**

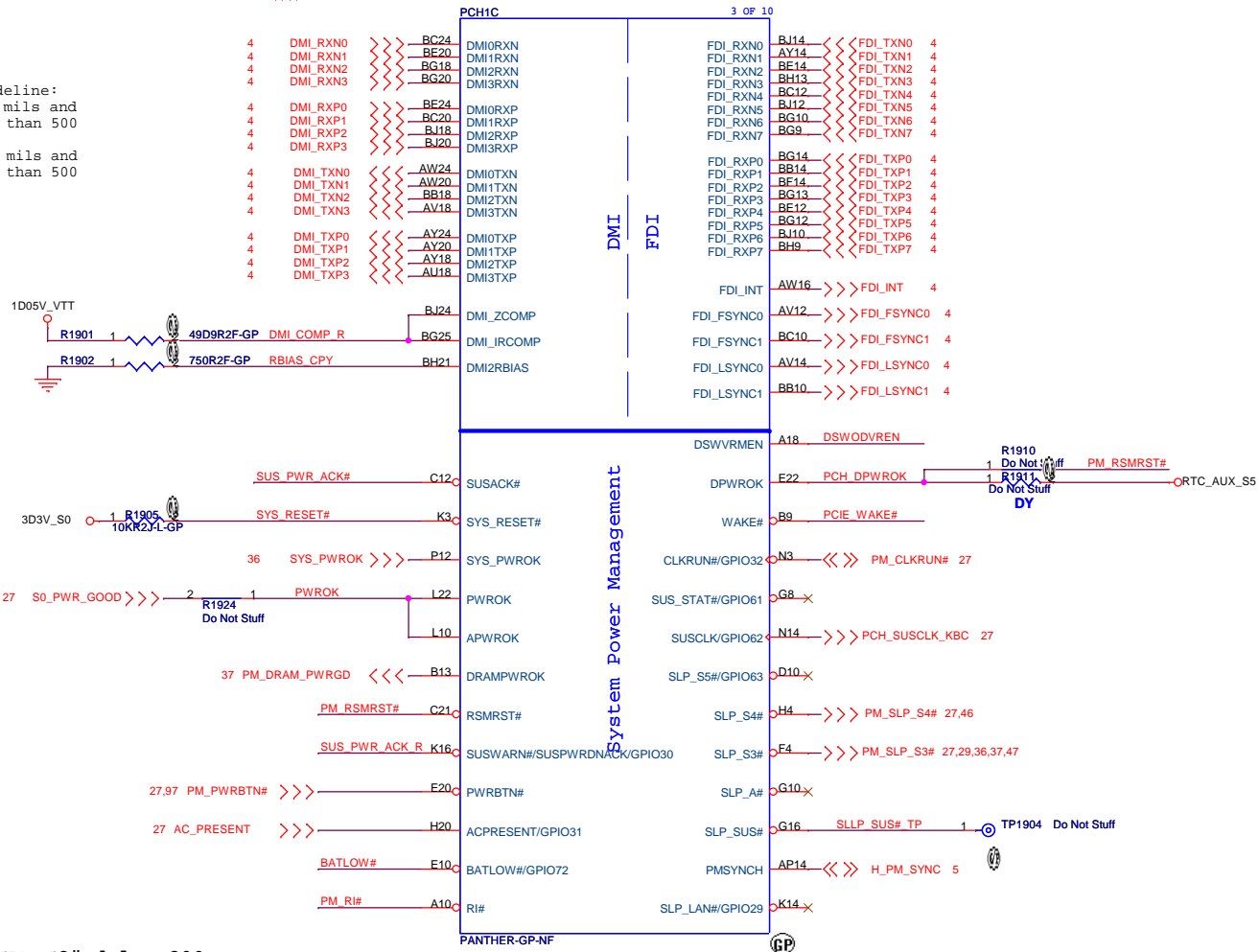
Size: Custom Document Number: **Husk/Petra** Rev: **-4M**

Date: Thursday, September 06, 2012 Sheet 18 of 103

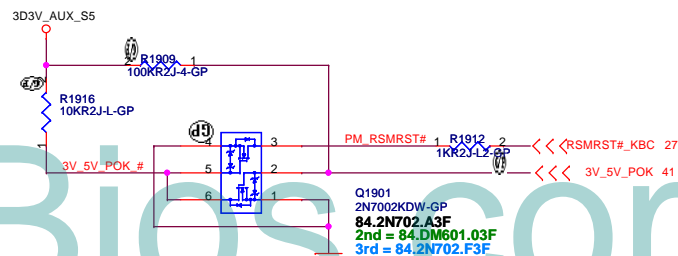
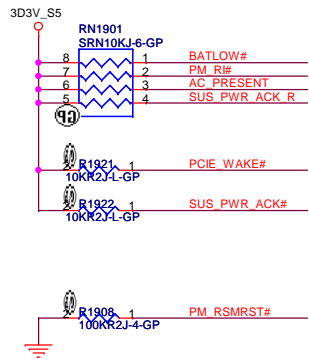
**SSID = PCH**



Signal Routing Guideline:  
DMI\_ZCOMP keep W=4 mils and routing length less than 500 mils.  
DMI\_IRCOMP keep W=4 mils and routing length less than 500 mils.

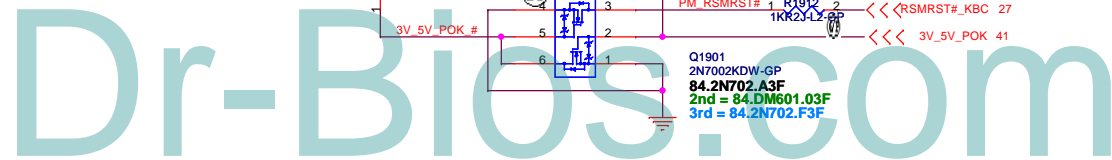


S0\_PWR\_GOOD after PM\_SLP\_S3# delay 200 ms



DSWODVREN - On Die DSW VR Enable

HIGH	Enabled (DEFAULT)
LOW	Disabled



DIS IVB Touch

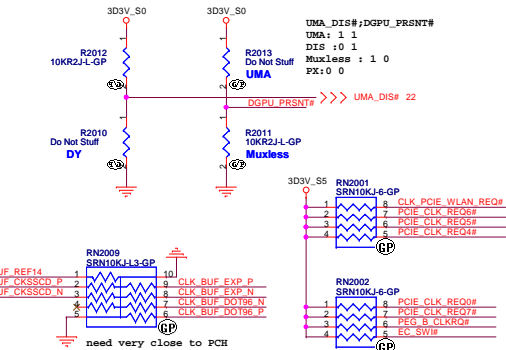
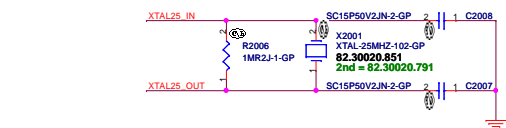
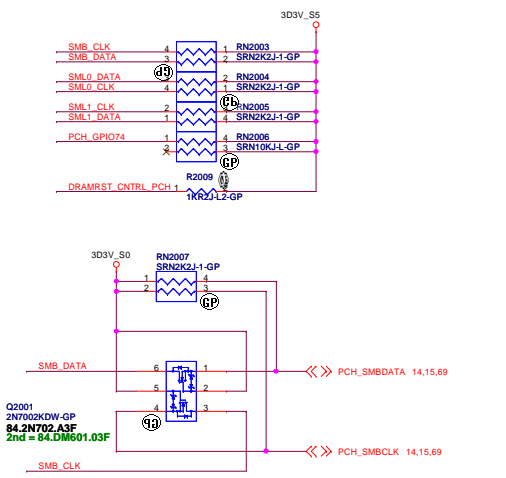
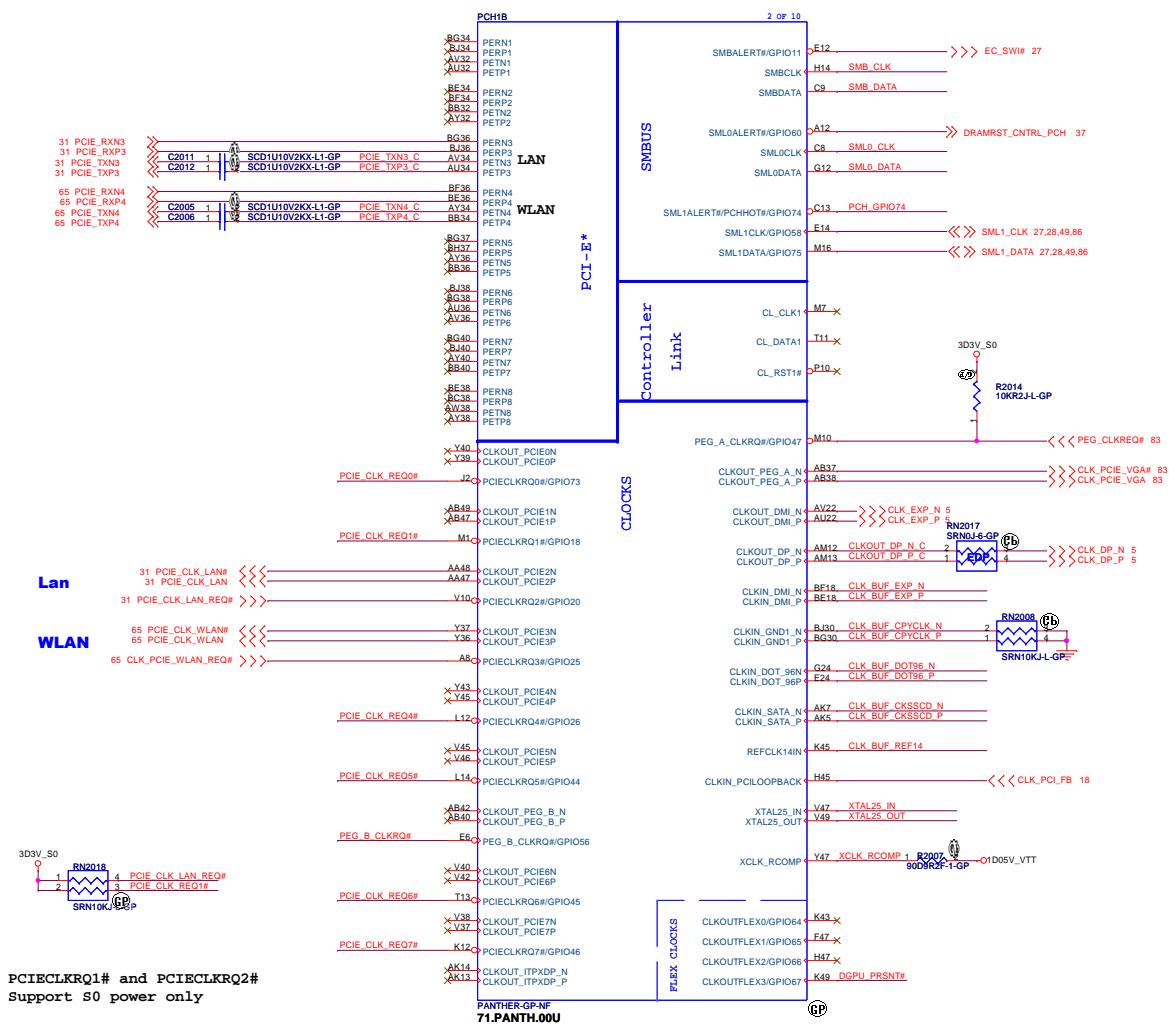
**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (DM I/FDI/PM)**

Size A3 Document Number: **Husk/Petra** Rev: **-4M**

Date: Thursday, September 06, 2012 Sheet 19 of 103

SSID = PCH



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21F, 86, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI-E/SMBUS/CLOCK/CL)

Size: Document Number

Customer: Husk/Petra

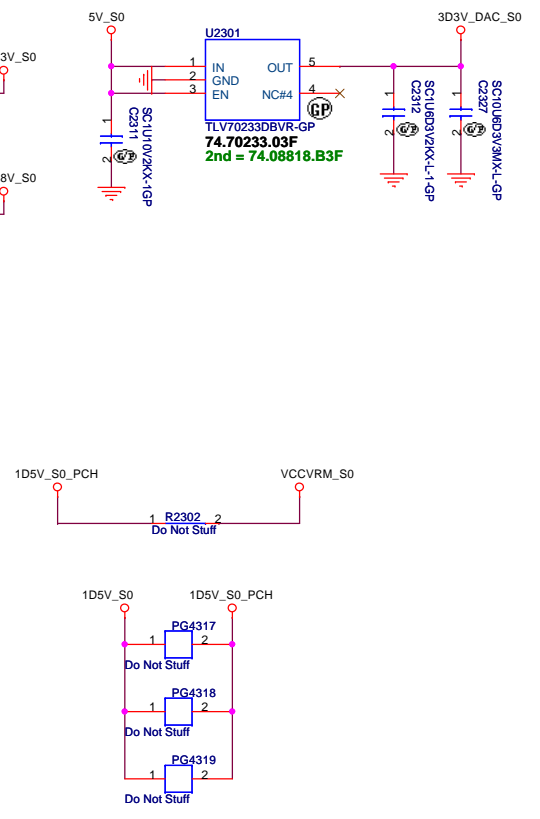
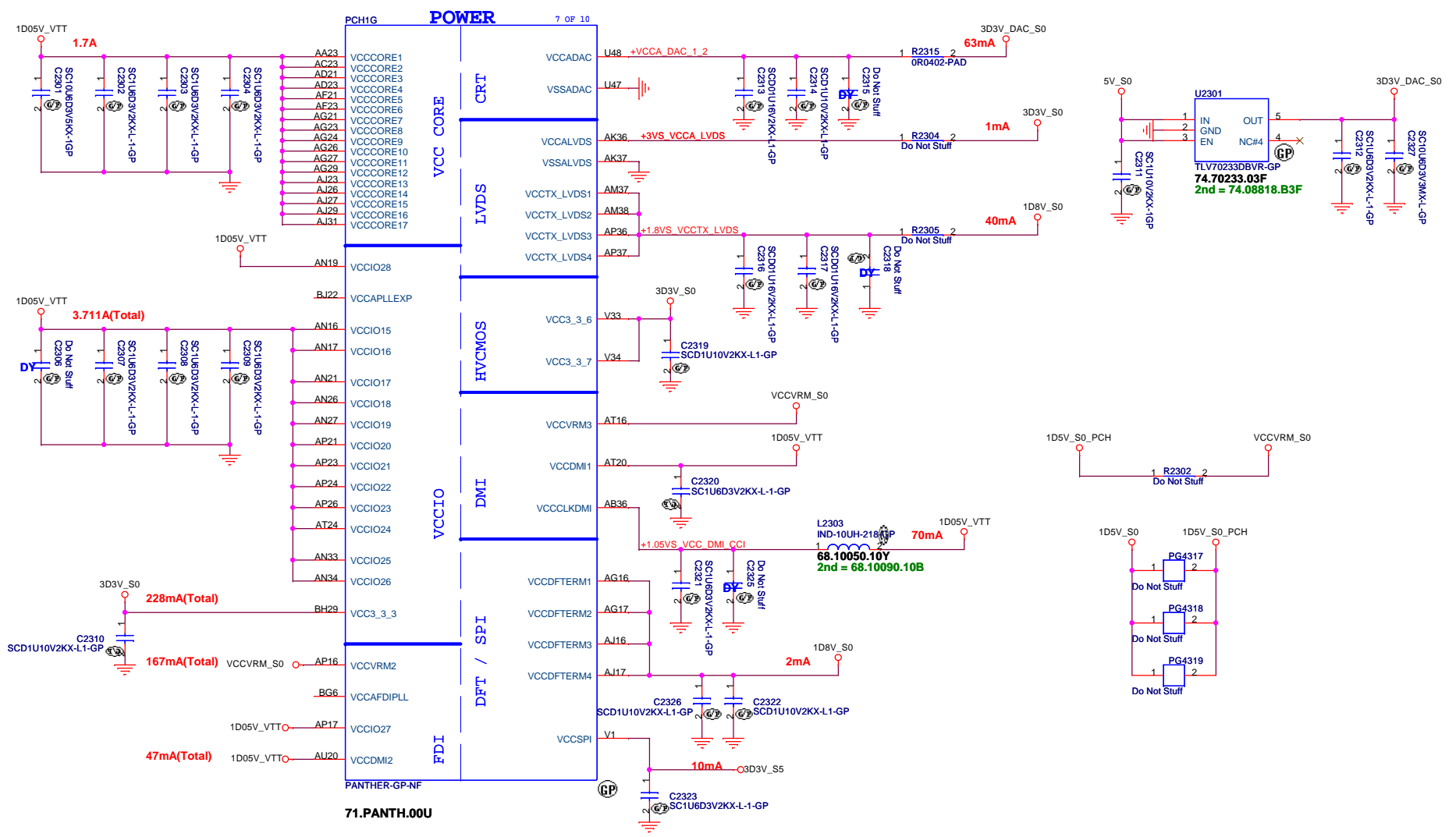
Date: Thursday, September 06, 2012

Sheet: 20 of 103

Rev: -4M







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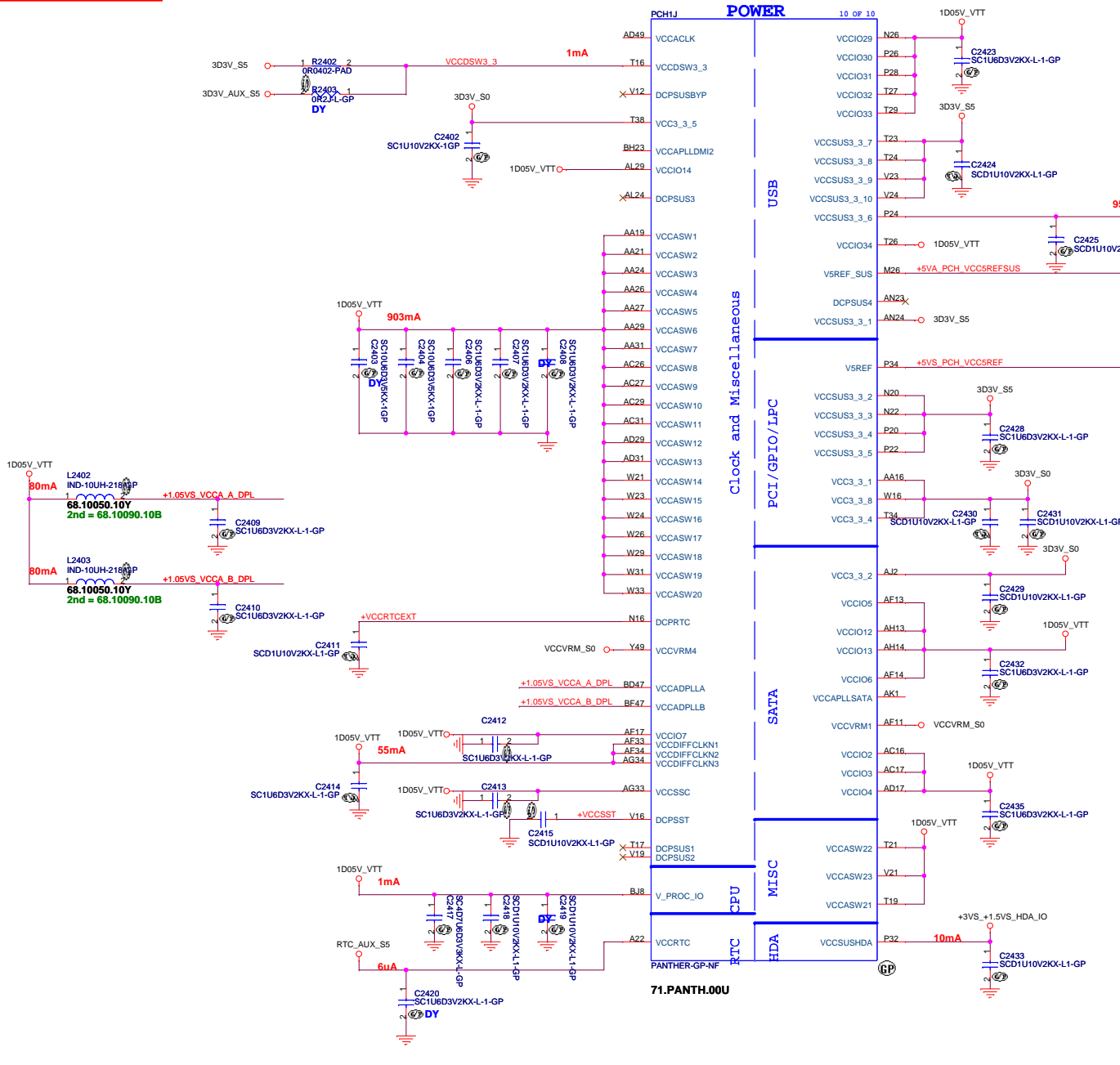
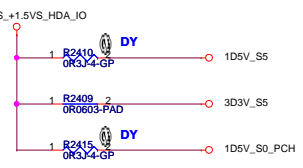
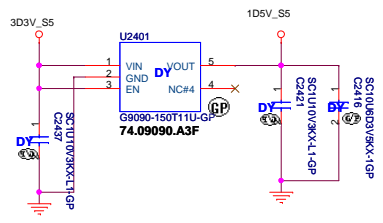


Table 5-1. Voltage Ramp Up/Down Requirements for the PCH Suspend Well Voltage Rails

Va	Vb	Power-Up Requirement	Power-Down Requirement
V\$REF_SUS	VCC\$US3_3	a) VCC\$REF_SUS must be powered up before VCC\$US3_3 or after VCC\$US3_3 within 0.7 V. b) If VCC\$REF_SUS is more than VCC\$US3_3 by 3 V, then the duration of this condition needs to be less than 20 ms.	a) V\$REF_SUS must be powered down after VCC\$US3_3 or before VCC\$US3_3 within 0.7 V.
V\$REF	VCC3_3	a) V\$REF must be powered up before VCC3_3 or after VCC3_3 within 0.7 V. b) For power up, if VCC\$REF is more than VCC3_3 by 3 V, then the duration of this condition needs to be less than 20 ms.	a) V\$REF must be powered down after VCC3_3 or before VCC3_3 within 0.7 V.

VccVRM	Internal PLL and VRMs (1.5V for Mobile)
VccVRM	1.8 V Internal PLL and VRMs (1.8 V for Desktop)





SSID = PCH

PCH1H 8 OF 10

H5	VSS0	
AA17	VSS1	VSS80 AK38
AA2	VSS2	VSS81 AK4
AA3	VSS3	VSS82 AK42
AA33	VSS4	VSS83 AK46
AA34	VSS5	VSS84 AK6
AB11	VSS6	AL16
AB14	VSS7	VSS85 AL17
AB39	VSS8	VSS86 AL19
AB4	VSS9	VSS87 AL2
AB43	VSS10	VSS88 AL21
AB5	VSS11	VSS89 AL23
AB7	VSS12	VSS90 AL26
AC19	VSS13	VSS91 AL27
AC2	VSS14	VSS92 AL31
AC21	VSS15	VSS93 AL33
AC24	VSS16	VSS94 AL34
AC33	VSS17	VSS95 AL48
AC34	VSS18	VSS96 AL48
AC48	VSS19	VSS97 AM11
AD10	VSS20	VSS98 AM14
AD11	VSS21	VSS99 AM36
AD12	VSS22	VSS100 AM39
AD13	VSS23	VSS101 AM43
AD19	VSS24	VSS102 AM45
AD24	VSS25	VSS103 AM46
AD26	VSS26	AM7
AD27	VSS27	VSS104 AN2
AD33	VSS28	VSS105 AN29
AD34	VSS29	VSS106 AN3
AD36	VSS30	VSS107 AN31
AD37	VSS31	VSS108 AP12
AD38	VSS32	VSS109 AP19
AD39	VSS33	VSS110 AP28
AD4	VSS34	VSS111 AP30
AD40	VSS35	VSS112 AP32
AD42	VSS36	VSS113 AP38
AD43	VSS37	VSS114 AP4
AD45	VSS38	VSS115 AP42
AD46	VSS39	VSS116 AP46
AD8	VSS40	VSS117 AP8
AE2	VSS41	VSS118 AR2
AE3	VSS42	VSS119 AR48
AE10	VSS43	VSS120 AT11
AE12	VSS44	VSS121 AT13
AD14	VSS45	VSS122 AT18
AD16	VSS46	VSS123 AT22
AE16	VSS47	VSS124 AT26
AF19	VSS48	VSS125 AT28
AF24	VSS49	VSS126 AT28
AF26	VSS50	VSS127 AT30
AF27	VSS51	VSS128 AT32
AF29	VSS52	VSS129 AT34
AF31	VSS53	VSS130 AT39
AF38	VSS54	VSS131 AT42
AF4	VSS55	VSS132 AT46
AF42	VSS56	VSS133 AT7
AF46	VSS57	VSS134 AU24
AF5	VSS58	VSS135 AU30
AF7	VSS59	VSS136 AV16
AF8	VSS60	VSS137 AV20
AG19	VSS61	VSS138 AV24
AG2	VSS62	VSS139 AV30
AG31	VSS63	VSS140 AV38
AG48	VSS64	VSS141 AV4
AH11	VSS65	VSS142 AV43
AH3	VSS66	VSS143 AV8
AH36	VSS67	VSS144 AW14
AH39	VSS68	VSS145 AW18
AH40	VSS69	VSS146 AW2
AH42	VSS70	VSS147 AW22
AH46	VSS71	VSS148 AW26
AH7	VSS72	VSS149 AW28
AJ19	VSS73	VSS150 AW34
AJ21	VSS74	VSS151 AW36
AJ24	VSS75	VSS152 AW40
AJ33	VSS76	VSS153 AW48
AJ34	VSS77	VSS154 AW48
AK12	VSS78	VSS155 AV11
AK3	VSS79	VSS156 AY12
		VSS157 AY22
		VSS158 AY28

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71.PANTH.00U

PCH1I 9 OF 10

AY4	VSS159	VSS259 H46
AY42	VSS160	VSS260 K18
AY46	VSS161	VSS261 K26
AY8	VSS162	VSS262 K33
B11	VSS163	VSS263 K46
B15	VSS164	VSS264 K7
B19	VSS165	VSS265 L18
B23	VSS166	VSS266 L2
B27	VSS167	VSS267 L20
B31	VSS168	VSS268 L28
B35	VSS169	VSS269 L36
B39	VSS170	VSS270 L48
B7	VSS171	VSS271 M12
F45	VSS172	VSS272 M12
BB12	VSS173	VSS273 P16
BB16	VSS174	VSS274 M18
BB20	VSS175	VSS275 M22
BB22	VSS176	VSS276 M30
BB24	VSS177	VSS277 M32
BB28	VSS178	VSS278 M34
BB30	VSS179	VSS279 M38
BB38	VSS180	VSS280 M4
BB4	VSS181	VSS281 M42
BB46	VSS182	VSS282 M46
BC14	VSS183	VSS283 M8
BC18	VSS184	VSS284 N18
BC2	VSS185	VSS285 P30
BC22	VSS186	VSS286 N47
BC26	VSS187	VSS287 P11
BC32	VSS188	VSS288 P18
BC34	VSS189	VSS289 T33
BC36	VSS190	VSS290 P40
BC40	VSS191	VSS291 P43
BC42	VSS192	VSS292 P47
BC48	VSS193	VSS293 P7
BD46	VSS194	VSS294 R2
BD5	VSS195	VSS295 R48
BE22	VSS196	VSS296 T12
BE26	VSS197	VSS297 T31
BE40	VSS198	VSS298 T37
BE10	VSS199	VSS299 T4
BE12	VSS200	VSS300 W34
BE16	VSS201	VSS301 T46
BE20	VSS202	VSS302 T47
BE22	VSS203	VSS303 T8
BE24	VSS204	VSS304 V11
BE26	VSS205	VSS305 V17
BE28	VSS206	VSS306 V27
BD3	VSS207	VSS307 V29
BE30	VSS208	VSS308 V31
BE38	VSS209	VSS309 V36
BF40	VSS210	VSS310 V39
BF8	VSS211	VSS311 V43
BG17	VSS212	V7
BG21	VSS213	VSS312 W19
BG33	VSS214	VSS313 W2
BG44	VSS215	VSS314 W27
BG8	VSS216	VSS315 W48
BH11	VSS217	VSS316 Y12
BH15	VSS218	VSS317 Y38
BH17	VSS219	VSS318 Y4
BH19	VSS220	VSS319 Y42
H10	VSS221	VSS320 Y46
BH27	VSS222	VSS321 Y8
BH31	VSS223	VSS322 RG29
BH33	VSS224	VSS323 N24
BH35	VSS225	VSS324 AD47
BH39	VSS226	VSS325 B43
BH43	VSS227	VSS326 BE10
BH7	VSS228	VSS327 BG41
D3	VSS229	VSS328 G14
D12	VSS230	VSS329 H16
D16	VSS231	VSS330 T36
D18	VSS232	VSS331 BG22
D22	VSS233	VSS332 BG24
D24	VSS234	VSS333 C22
D26	VSS235	VSS334 AP13
D30	VSS236	VSS335 M14
D32	VSS237	VSS336 AP3
D34	VSS238	VSS337 AP1
D38	VSS239	VSS338 BE16
D42	VSS240	VSS339 BC16
D8	VSS241	VSS340 RG28
E18	VSS242	VSS341 BJ28
E26	VSS243	
G18	VSS244	
G20	VSS245	
G26	VSS246	
G28	VSS247	
G36	VSS248	
G48	VSS249	
H12	VSS250	
H18	VSS251	
H22	VSS252	
H24	VSS253	
H26	VSS254	
H30	VSS255	
H32	VSS256	
H34	VSS257	
F3	VSS258	

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71.PANTH.00U

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21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (VSS)**

Size A3 Document Number: **Husk/Petra** Rev: **-4M**

Date: Thursday, September 06, 2012 Sheet 25 of 103

5

4

3

2

1

D

D

C

C

B

B

A

A

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<b>緯創資通</b> <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
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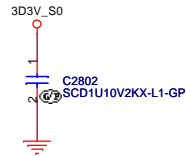
Title		<b><i>Clock(colay)</i></b>
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Size	Document Number	Rev
A4	<b>Husk/Petra</b>	<b>-4M</b>

Date: Thursday, September 06, 2012	Sheet 26 of 103
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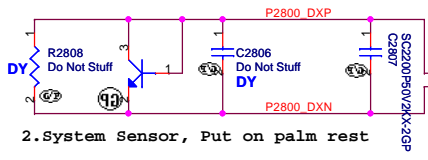


# Thermal sensor NCT 7718W

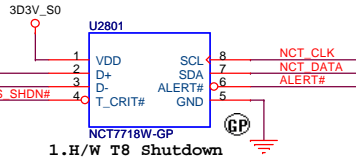


Layout notice :  
Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

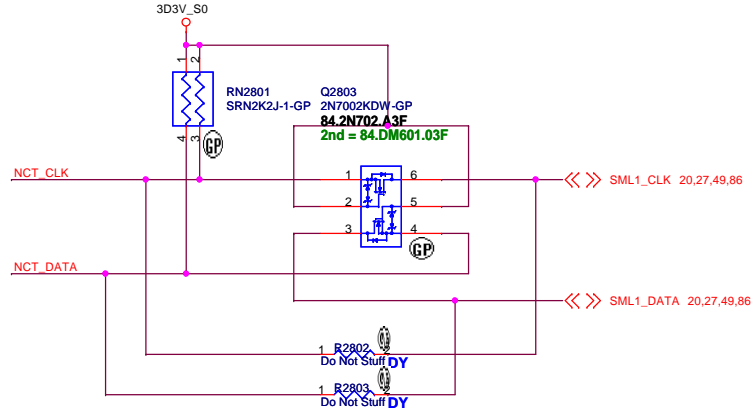
Q2801  
PMBS3904-1-GP  
84.03904.L06



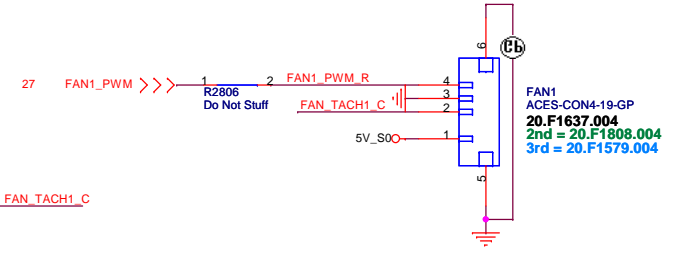
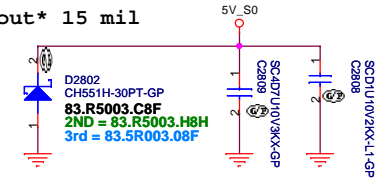
2. System Sensor, Put on palm rest



1.H/W T8 Shutdown



\*Layout\* 15 mil

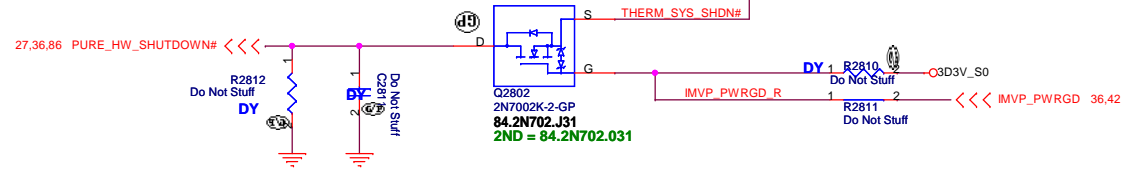
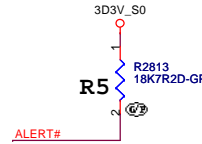


ALERT# /T CRIT#  
Pull-up Resistor

R5	2Kohm	7.5Kohm	R7 10.5Kohm	14Kohm	18.7Kohm
2Kohm	77°C	87°C	97°C	107°C	117°C
7.5Kohm	79°C	89°C	99°C	109°C	119°C
10.5Kohm	81°C	91°C	101°C	111°C	121°C
14Kohm	83°C	93°C	103°C	113°C	123°C
18.7Kohm	85°C	95°C	105°C	115°C	125°C

T\_CRIT temperature strapping point

SB T8=85 degree



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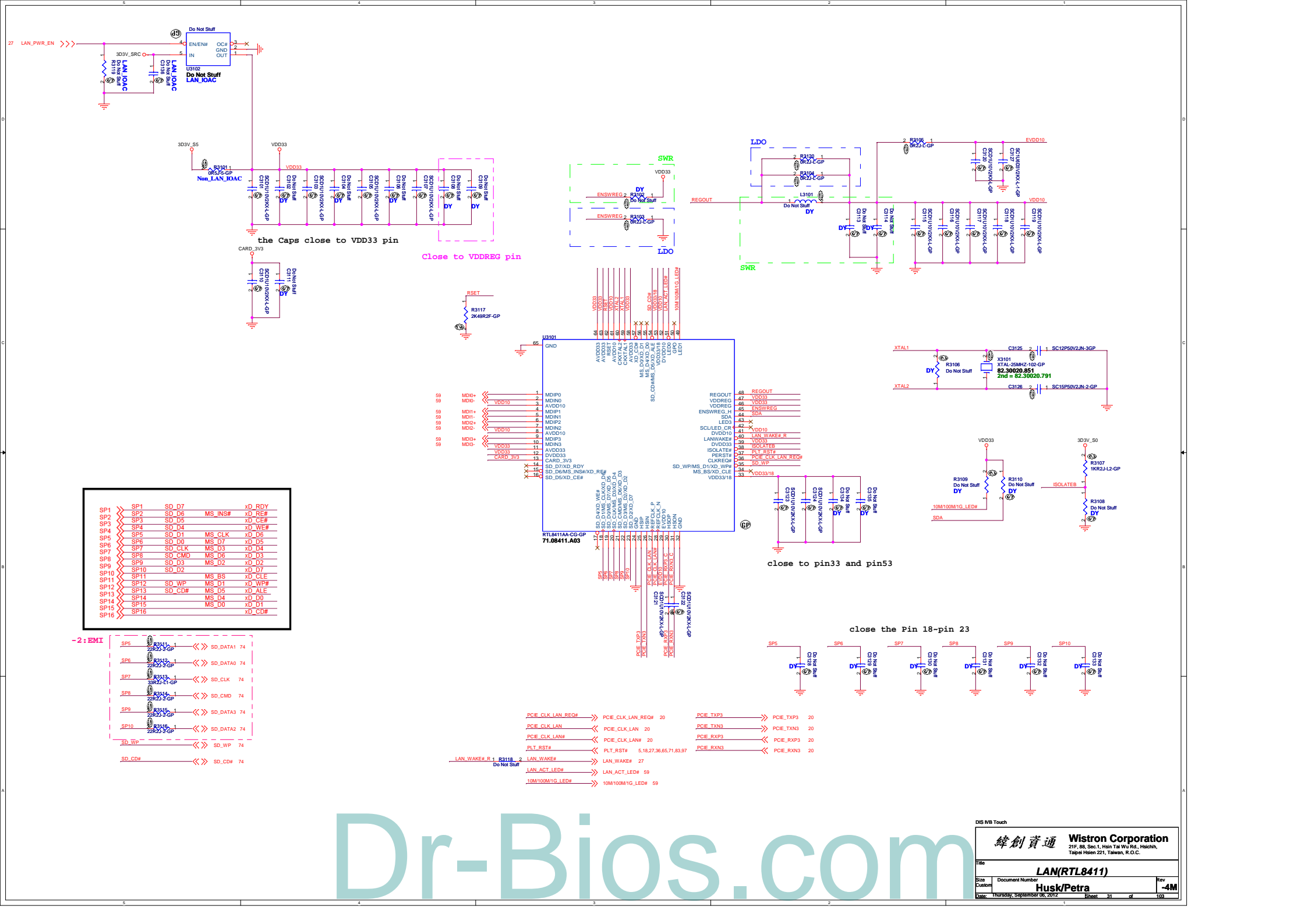
<b>緯創資通</b>		<b>Wistron Corporation</b>	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
<b>Thermal NCT7718</b>			
Title	Document Number		Rev
Custom	<b>Husk/Petra</b>		<b>-4M</b>
Date:	Thursday, September 06, 2012	Sheet	28 of 103



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Title <b>Audio AMP</b>	
Size A3	Document Number <b>Husk/Petra</b>
Date: Thursday, September 06, 2012	Rev <b>-4M</b>
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SP1	SP1	SD D7	MS_INS#	xD_RDY
SP2	SP2	SD D6	MS_RE#	xD_RE#
SP3	SP3	SD D5	MS_CE#	xD_CE#
SP4	SP4	SD D4	MS_WIE#	xD_WIE#
SP5	SP5	SD D1	MS_CLK	xD_D6
SP6	SP6	SD D0	MS_D7	xD_D5
SP7	SP7	SD CLK	MS_D3	xD_D4
SP8	SP8	SD CMD	MS_D6	xD_D3
SP9	SP9	SD D3	MS_D2	xD_D2
SP10	SP10	SD D2	MS_D7	xD_D7
SP11	SP11	MS_BS	MS_D1	xD_CLE
SP12	SP12	SD_WP	MS_D1	xD_WP#
SP13	SP13	SD_CD#	MS_D5	xD_ALE
SP14	SP14	MS_D4	MS_D4	xD_D0
SP15	SP15	MS_D0	MS_D0	xD_D1
SP16	SP16	MS_CD#	MS_CD#	xD_CD#

- 2 : EMI

SP5	R3111	1	SD_DATA1	74
SP8	R3112	1	SD_DATA0	74
SP7	R3113	1	SD_CLK	74
SP8	R3114	1	SD_CMD	74
SP9	R3115	1	SD_DATA3	74
SP10	R3116	1	SD_DATA2	74
SD_WP			SD_WP	74
SD_CD#			SD_CD#	74

PCIE_CLK_LAN_REQ#	PCIE_CLK_LAN_REQ#	20	PCIE_TXP3	PCIE_TXP3	20
PCIE_CLK_LAN	PCIE_CLK_LAN	20	PCIE_TXN3	PCIE_TXN3	20
PCIE_CLK_LAN#	PCIE_CLK_LAN#	20	PCIE_RXP3	PCIE_RXP3	20
PLT_RST#	PLT_RST#	518,27,36,65,71,83,97	PCIE_RXN3	PCIE_RXN3	20
LAN_WAKE#	LAN_WAKE#	27			
LAN_ACT_LED#	LAN_ACT_LED#	59			
10M/100M1G_LED#	10M/100M1G_LED#	59			

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緯創資通 Wistron Corporation  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsin 221, Taiwan, R.O.C.

Title: LAN(RTL8411)

Size: Document Number: Rev: 4M

Date: 19/05/2012, September 19, 2012 Sheet: 31 of 100



DIS IWB Touch		
<b>緯創資通</b>		<b>Wistron Corporation</b>
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
<b>RTS5159 (CARD READER)</b>		
Size	Document Number	Rev
Custom	<b>Husk/Petra</b>	<b>-4M</b>
Date:	Thursday, September 06, 2012	Sheet 32 of 103

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			21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
<b>Reserved</b>					
Size	Document Number				Rev
A4	<b>Husk/Petra</b>				<b>-4M</b>
Date: Thursday, September 06, 2012			Sheet	33	of 103

(Blanking)

DIS IVB Touch

**緯創資通** **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title		
<b>Reserved</b>		
Size	Document Number	Rev
A4	<b>Husk/Petra</b>	<b>-4M</b>
Date:	Thursday, September 06, 2012	Sheet 34 of 103

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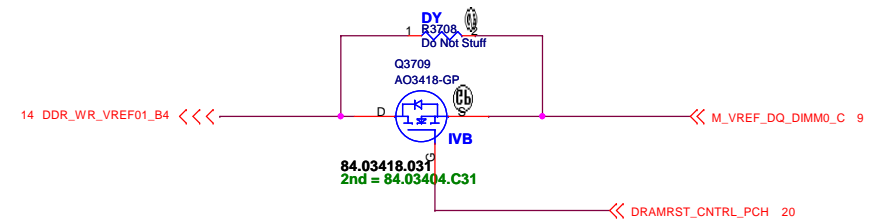
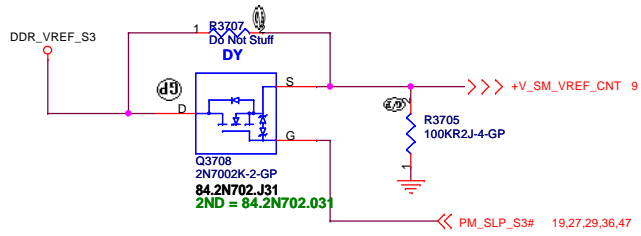
DIS IVB Touch

<b>緯創資通</b>		<b>Wistron Corporation</b>	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
<b>USB 3.0 Controller</b>			
Size	Document Number	Rev	
Custom	<b>Husk/Petra</b>	<b>-4M</b>	
Date:	Thursday, September 06, 2012	Sheet 35	of 103

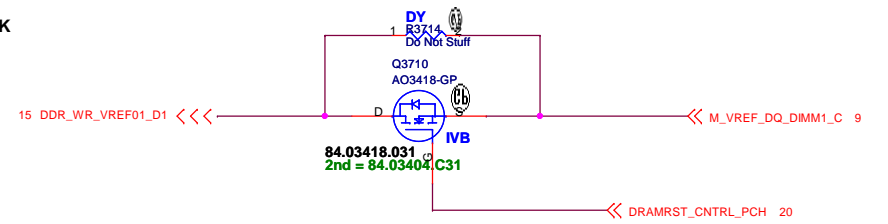
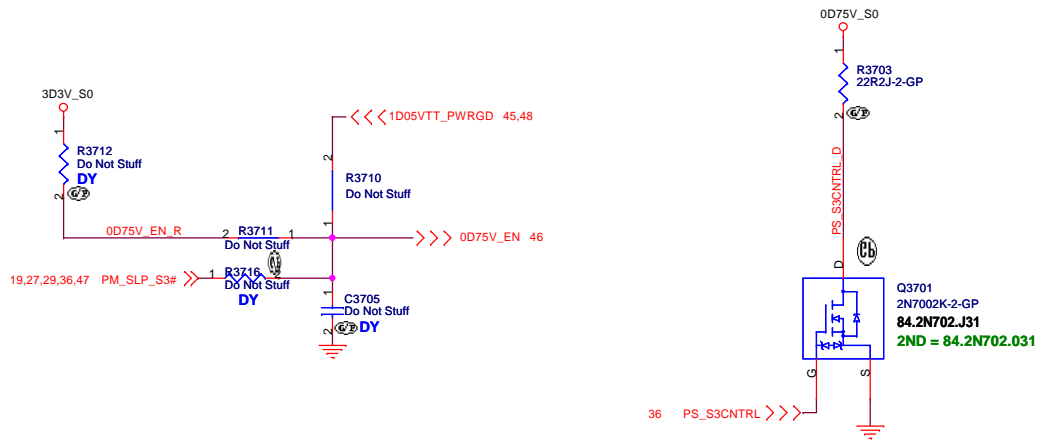
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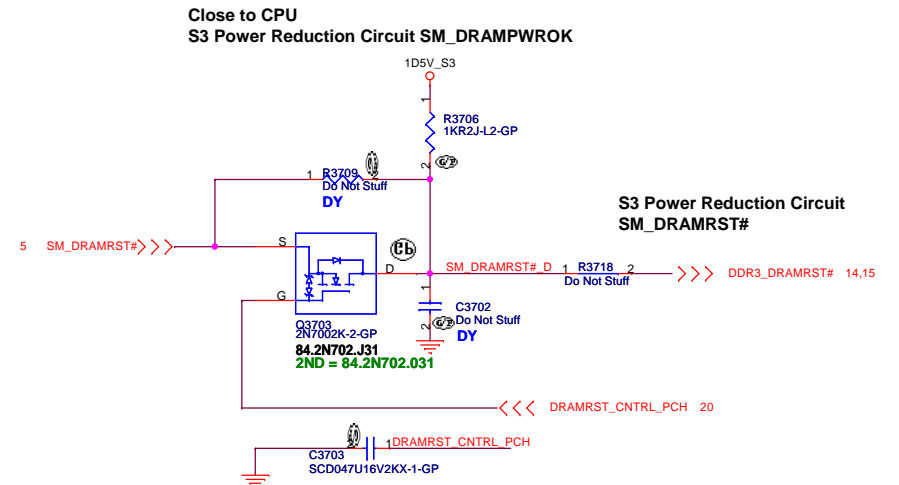
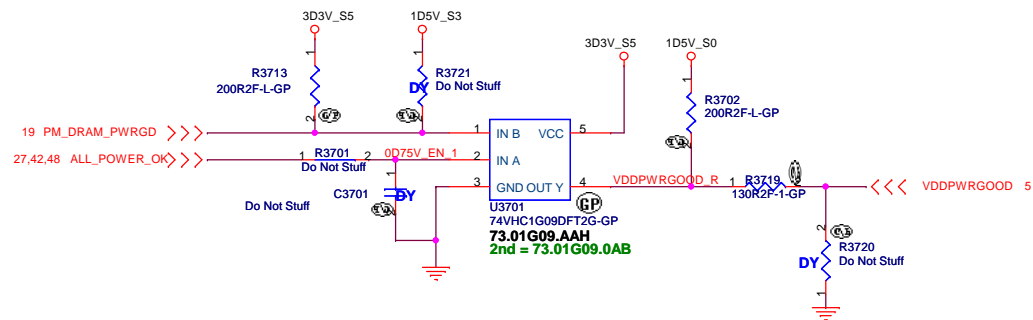
Close to CPU  
S3 Power Reduction Circuit Processor VREF\_DQ Implementation



Close to DIMM  
S3 Power Reduction Circuit SM\_DRAMPWROK



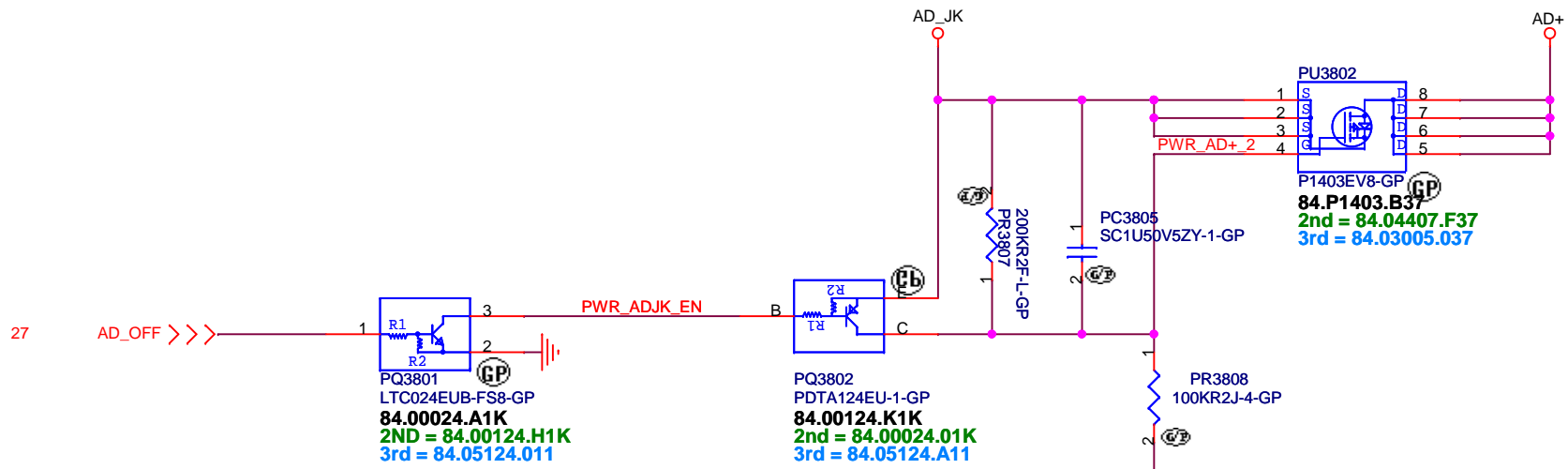
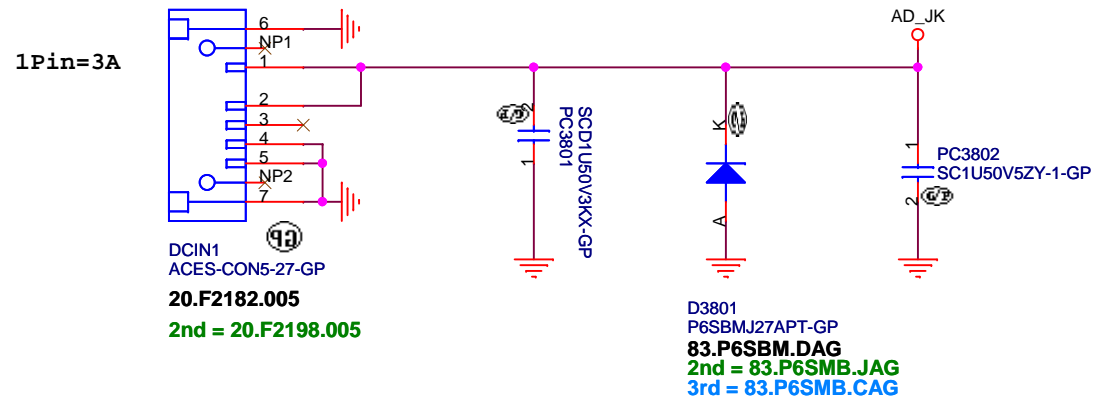
Close to CPU  
S3 Power Reduction Circuit SM\_DRAMPWROK



DIS IVB Touch

		<b>Wistron Corporation</b> 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: <b>ADAPTER</b>		
Size: A3	Document Number: <b>Husk/Petra</b>	Rev: <b>-4M</b>
Date: Thursday, September 06, 2012 Sheet 37 of 103		

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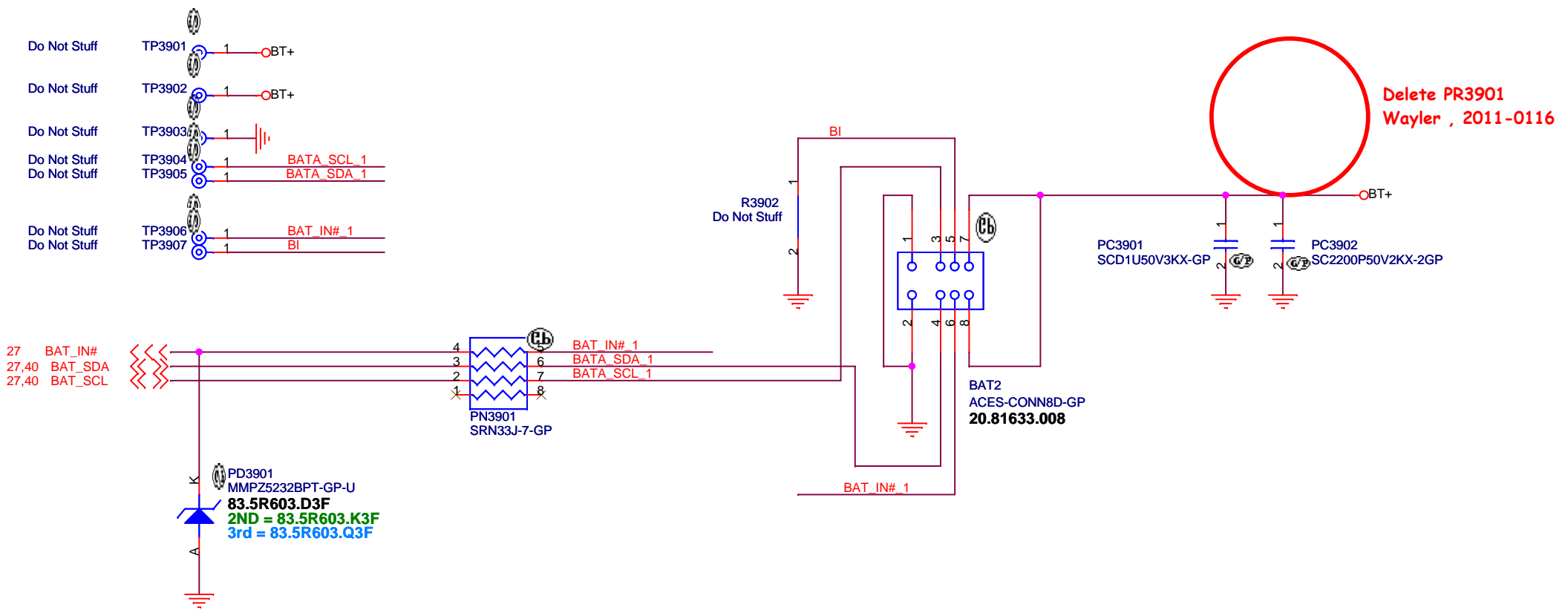
DIS IVB Touch

**緯創資通** **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title		
<b>DCIN JACK</b>		
Size	Document Number	Rev
A4	<b>Husk/Petra</b>	<b>-4M</b>
Date:	Thursday, September 06, 2012	Sheet 38 of 103

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# BATTERY CONNECTOR



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	<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
--	---

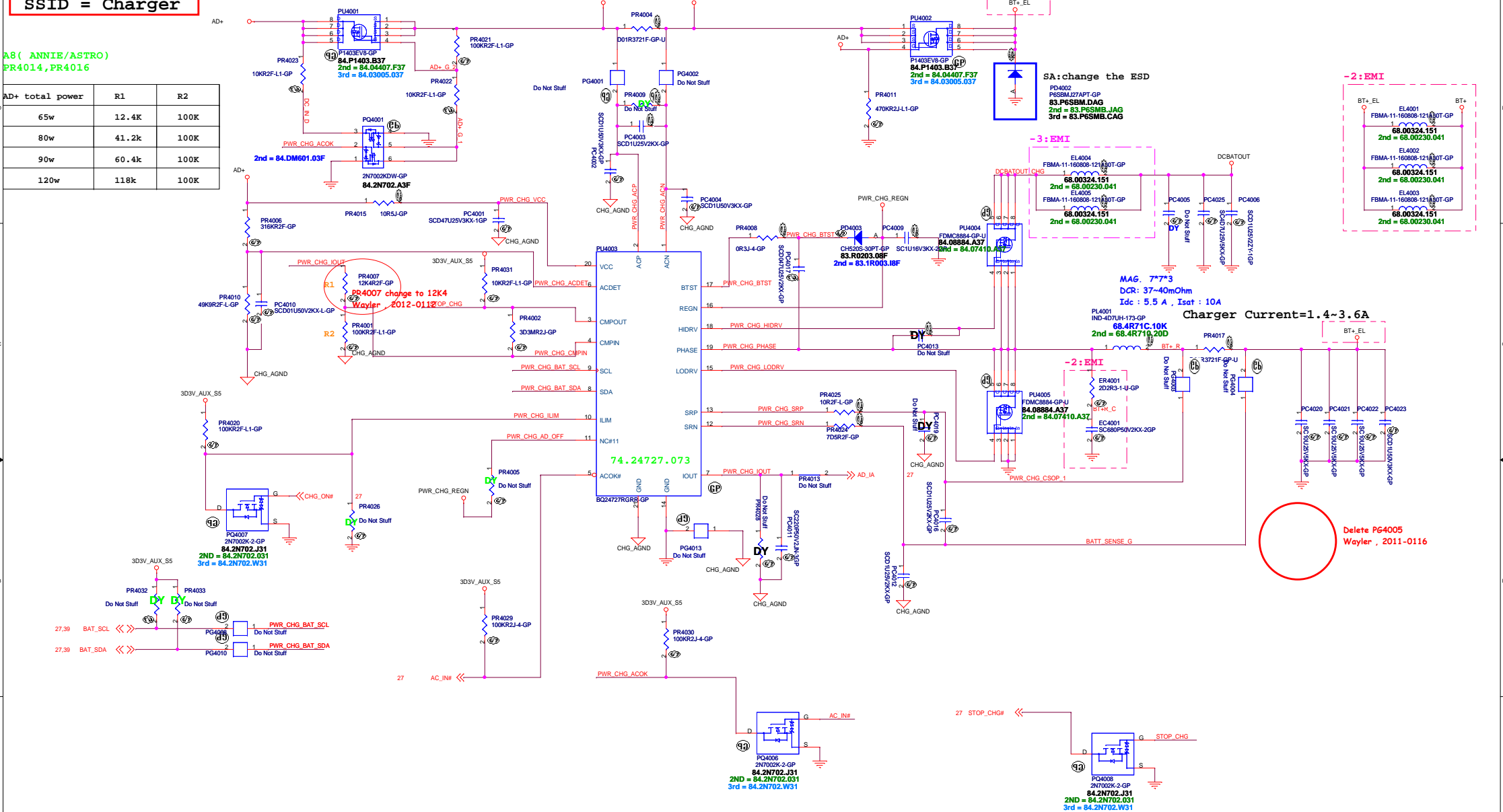
Title		<b>BATT CONN</b>	
Size	Document Number	Rev	
A4	Husk/Petra	<b>-4M</b>	
Date:	Thursday, September 06, 2012	Sheet	39 of 103

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**SSID = Charger**

A8 (ANNIE/ASTRO)  
PR4014, PR4016

AD+ total power	R1	R2
65w	1.2.4K	100K
80w	41.2k	100K
90w	60.4k	100K
120w	118k	100K



PR4007 change to 12K4  
Waylor 2012-0112 OP CHG

SA: change the ESD

- 3 : EMI

- 2 : EMI

Charger Current = 1.4 ~ 3.6A

Delete P64005  
Waylor, 2011-0116

DIS I/VB Touch

緯創資通 Wistron Corporation  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

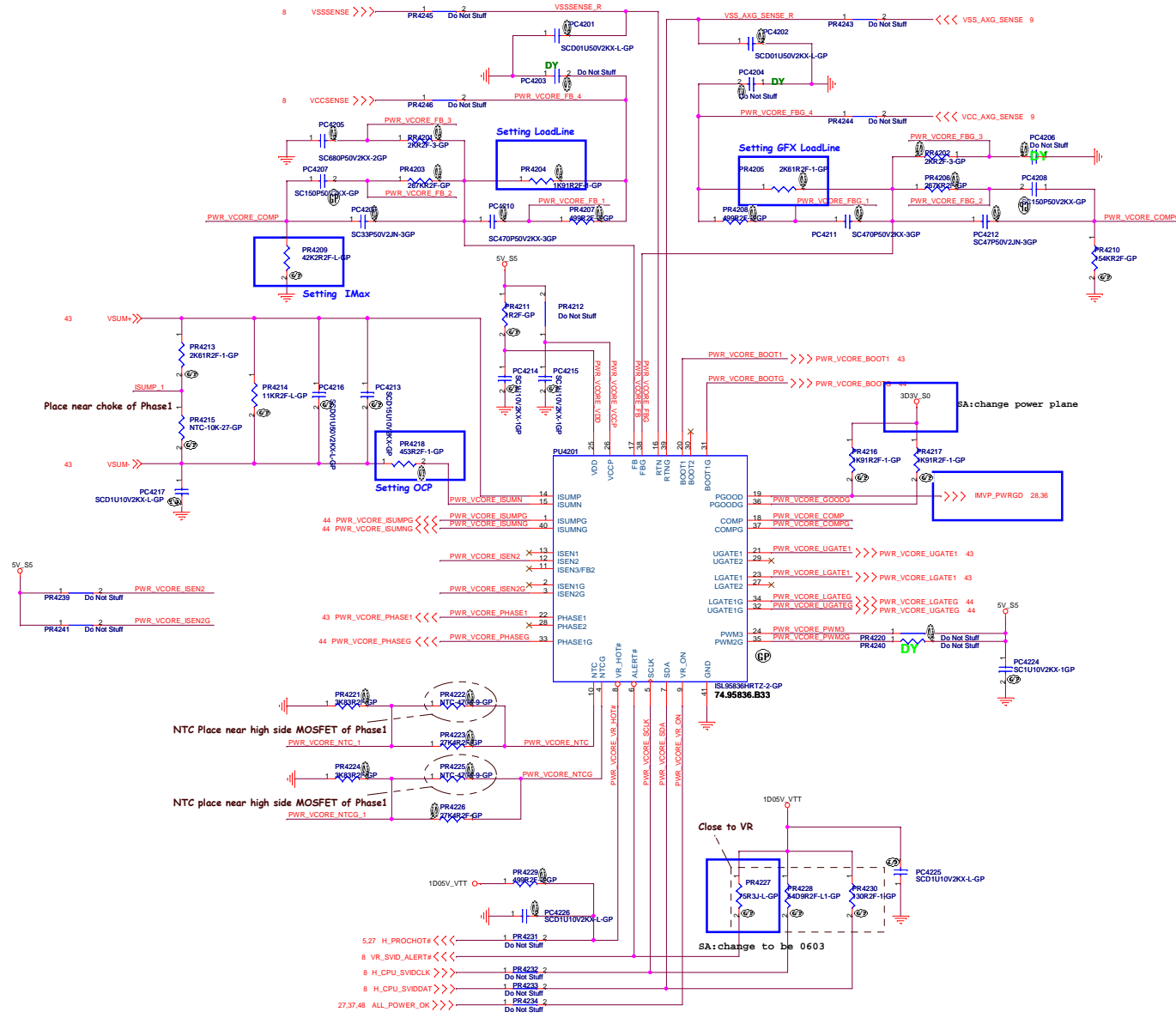
File: **CHARGER BQ24707A**

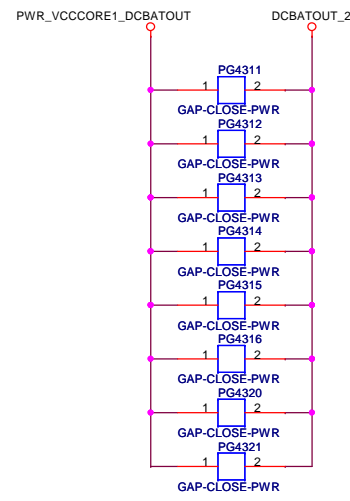
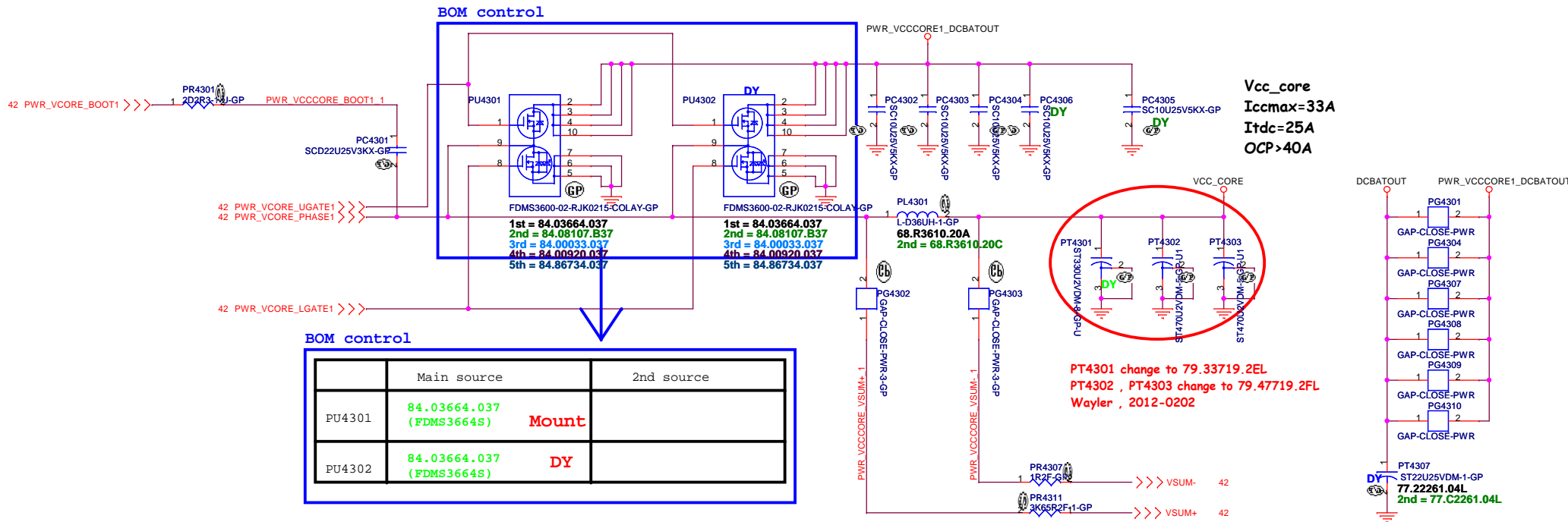
Size: Custom Document Number Husk/Petra Rev: -4M

Date: Thursday, September 06, 2012 Sheet: 40 of 108



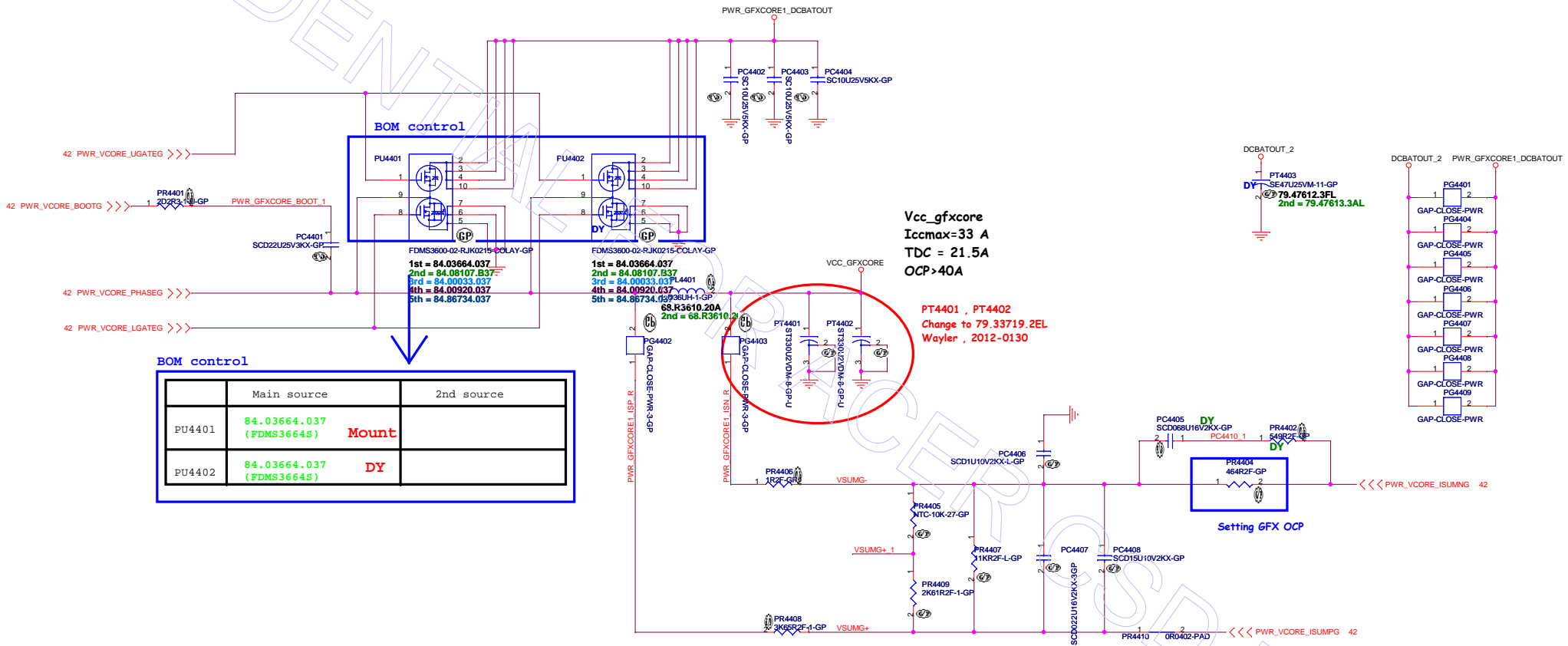






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CONFIDENTIAL



**BOM control**

	Main source	2nd source
PU4401	84.03664.037 (FDMS3664S)	Mount
PU4402	84.03664.037 (FDMS3664S)	DY

Vcc\_gfxcore  
Iccmax=33 A  
TDC = 21.5A  
OCP > 40A

PT4401 , PT4402  
Change to 79.33719.2EL  
Wayler , 2012-0130

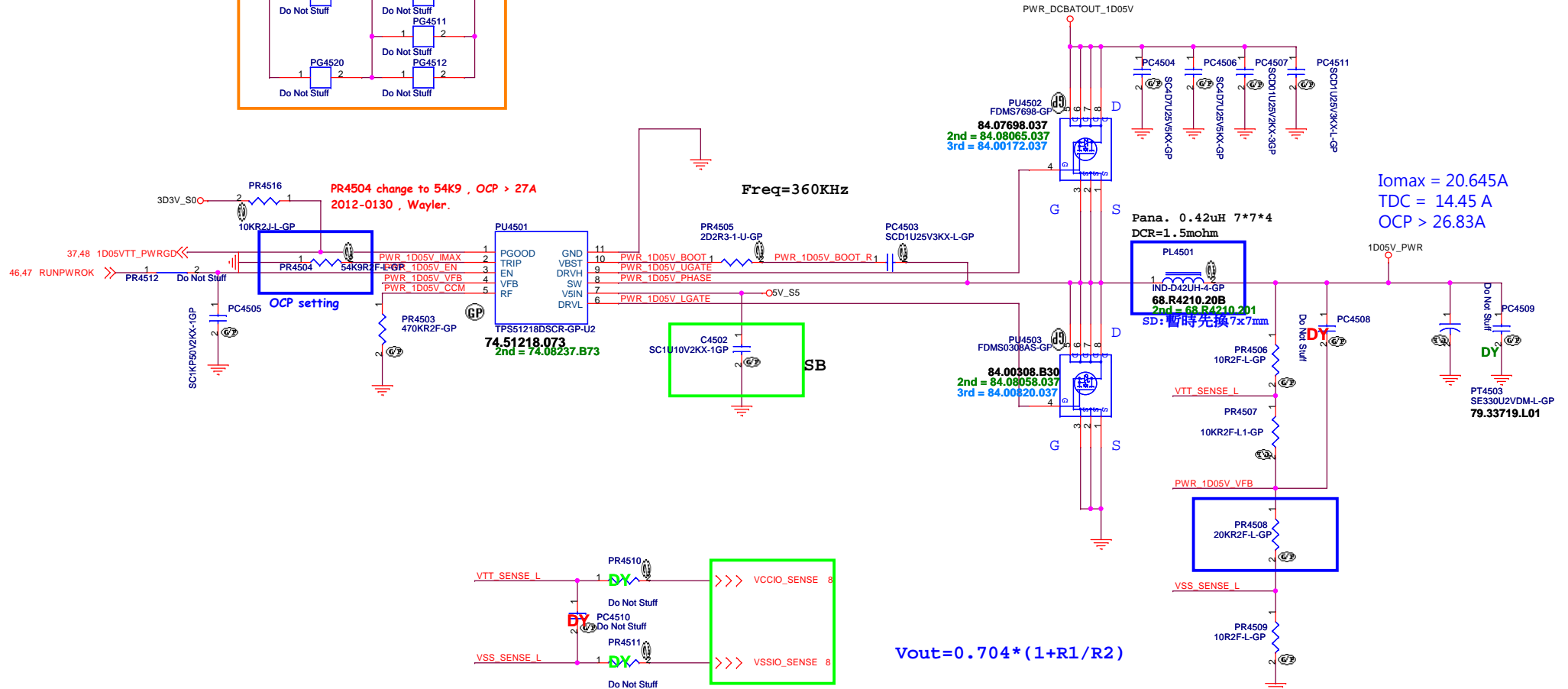
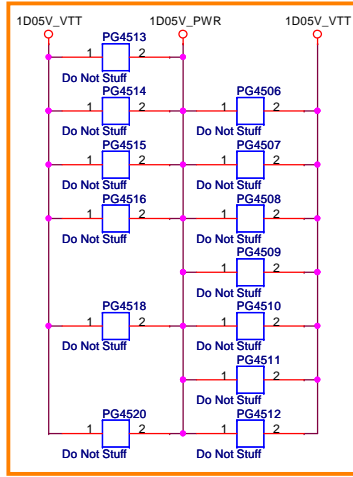
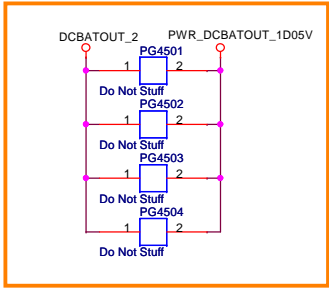
Setting GFX OCP

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SA\_20111004

SA\_20111013

# TPS51218D for 1D05V



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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **DC to DC 1D05V(TPS51218D)**

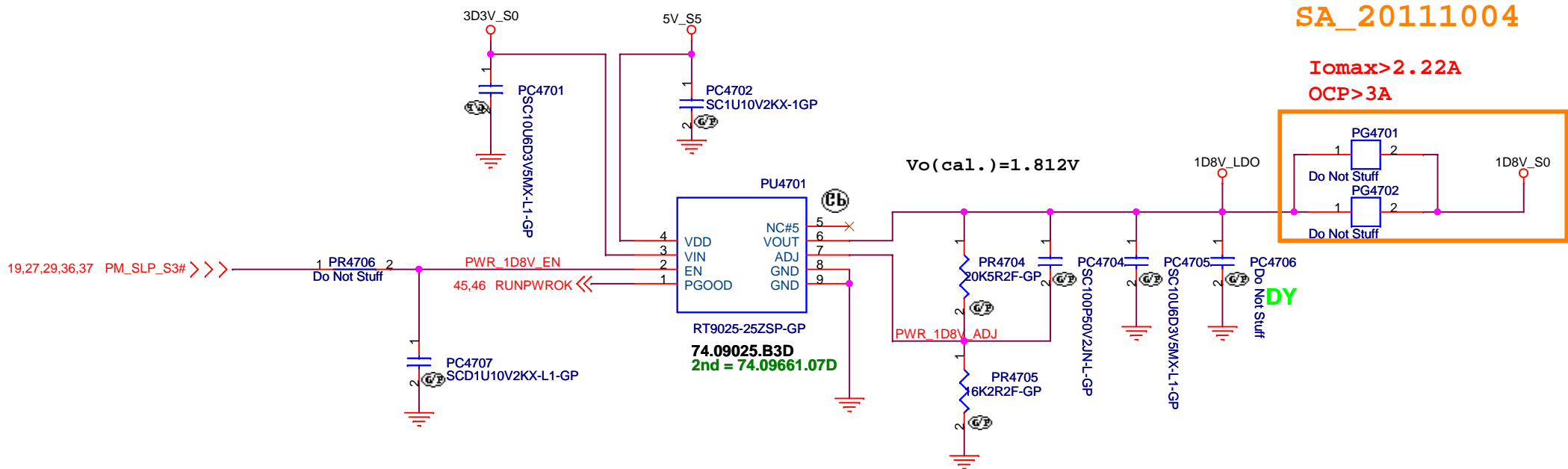
Size: A3 Document Number: **Husk/Petra** Rev: **-4M**

Date: Thursday, September 06, 2012 Sheet 45 of 103



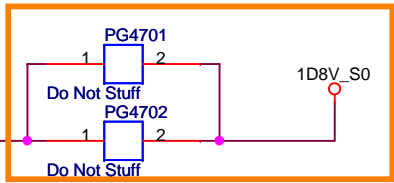
**SSID = PWR.Plane.Regulator\_1p8v**

### RT9025 for 1D8V\_S0



SA\_20111004

Iomax > 2.22A  
OCP > 3A



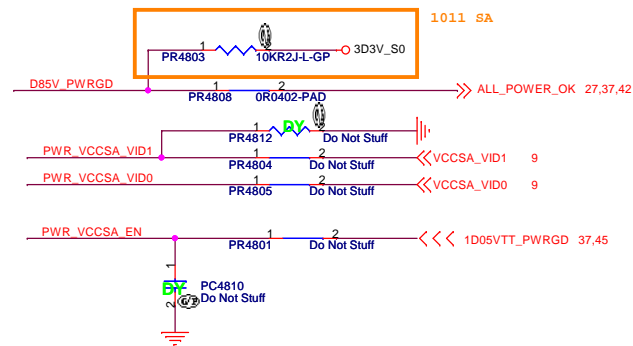
DIS IVB Touch

**緯創資通** **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title		<b>LDO 1D8V(RT9025)</b>	
Size	Document Number	Rev	
A4	<b>Husk/Petra</b>	<b>-4M</b>	
Date	Thursday, September 06, 2012	Sheet	47 of 103

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# LDO G978 for VCCSA



D0, D1 V<sub>O</sub> Selection Table

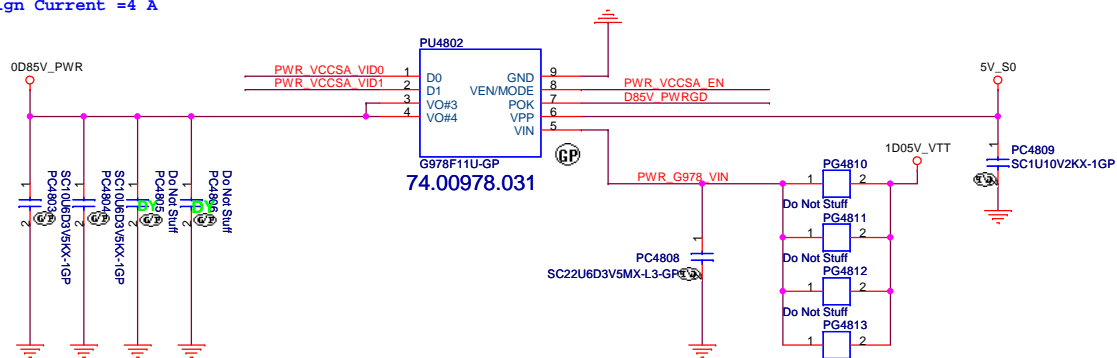
D0	D1	V <sub>O</sub> MODE=0	V <sub>O</sub> MODE=1
0	0	0.9V	0.9V
0	1	0.8V	0.85V
1	0	0.725V	0.775V
1	1	0.675V	0.75V

"x" means "don't care".

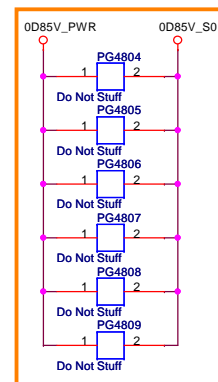
VEN/MODE Logic

VEN/MODE (VPP=5V)	EN logic	VEN/MODE (VPP=5V)	MODE logic
<0.6V	0	<2.0V	0
>1.0V	1	>2.6V	1

Design Current = 4 A



1011 SA

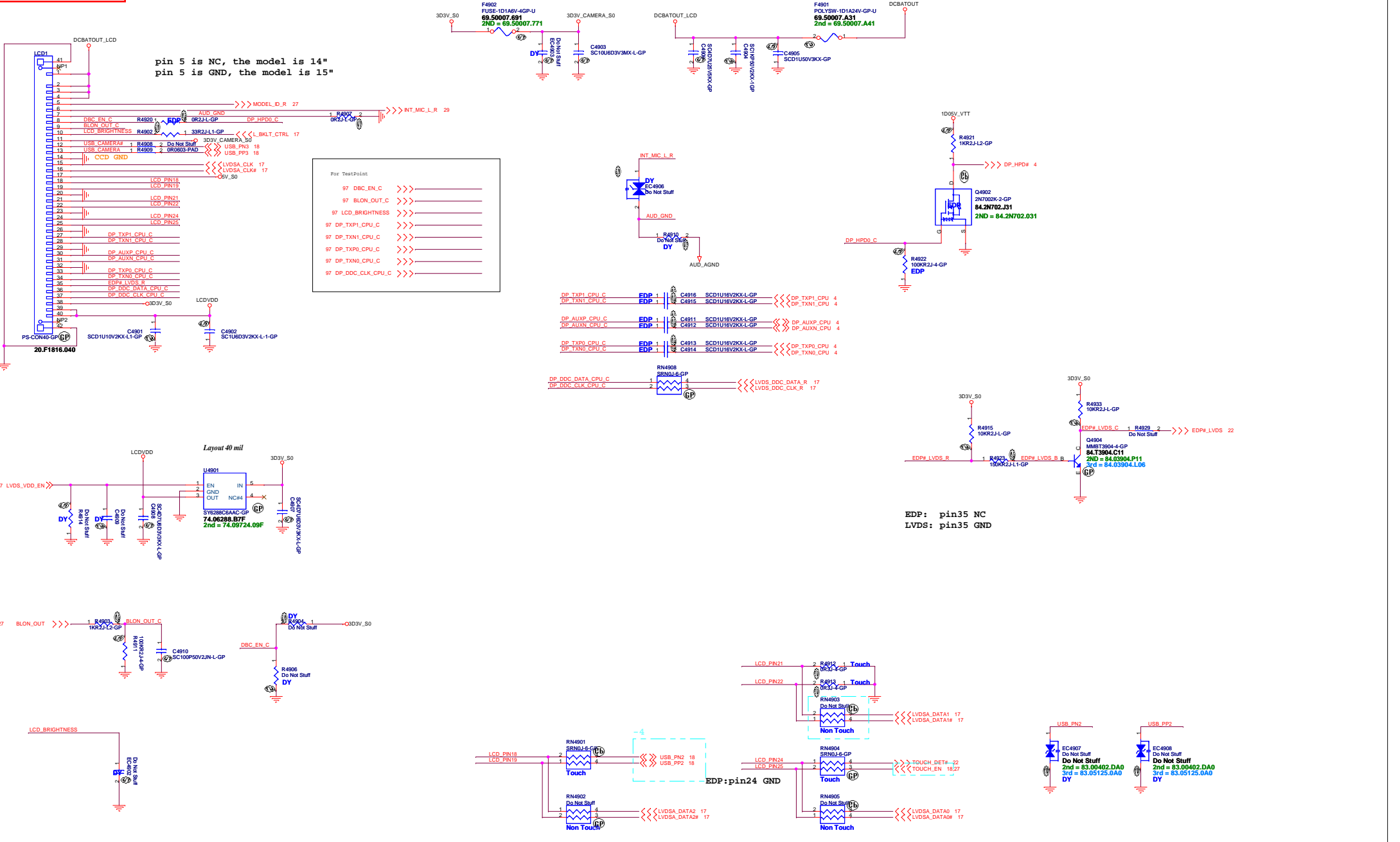


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DIS I/8 Touch

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>VCCSA LDO G978</b>			
Title			
Size	Document Number	Rev	
A3	Husk/Petra	-4M	
Date:	Thursday, September 06, 2012	Sheet	48 of 103

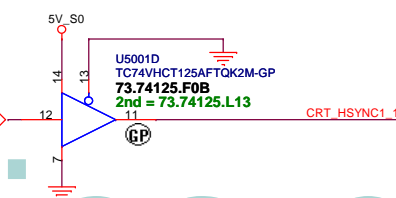
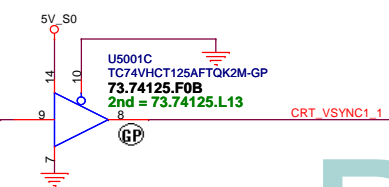
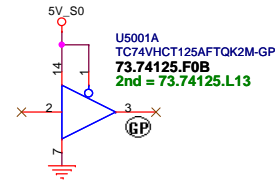
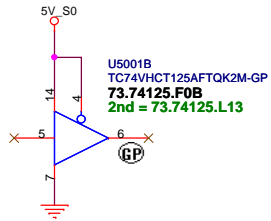
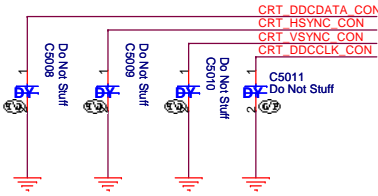
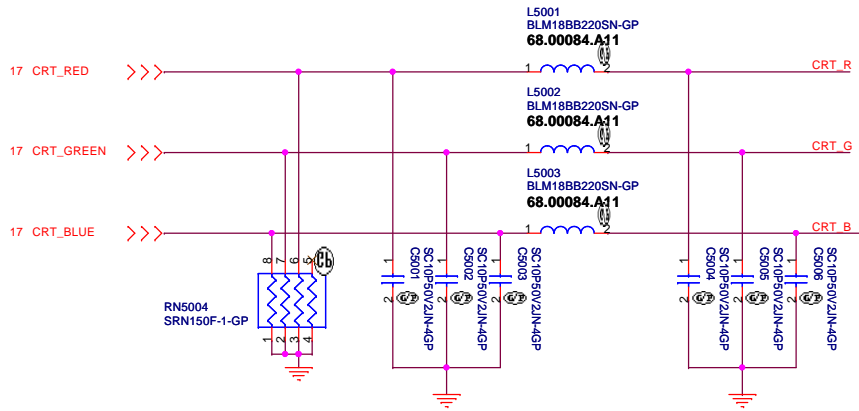
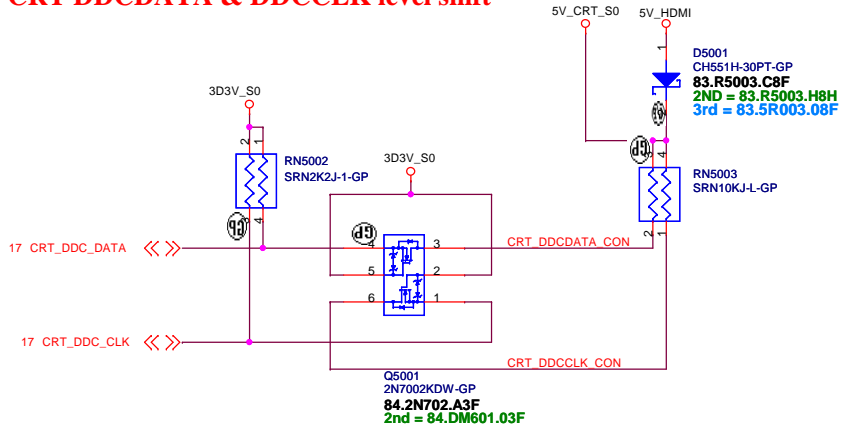
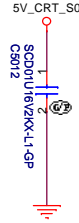




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# CRT DDCDATA & DDCCLK level shift

- CRT\_DDCDATA\_CON >>> CRT\_DDCDATA\_CON 59
- CRT\_DDCCLK\_CON >>> CRT\_DDCCLK\_CON 59
- CRT\_R >>> CRT\_R 59
- CRT\_G >>> CRT\_G 59
- CRT\_B >>> CRT\_B 59
- CRT\_HSYNC\_CON >>> CRT\_HSYNC\_CON 59
- CRT\_VSYNC\_CON >>> CRT\_VSYNC\_CON 59



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DIS IVB Touch

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Taipei Hsien 221, Taiwan, R.O.C.

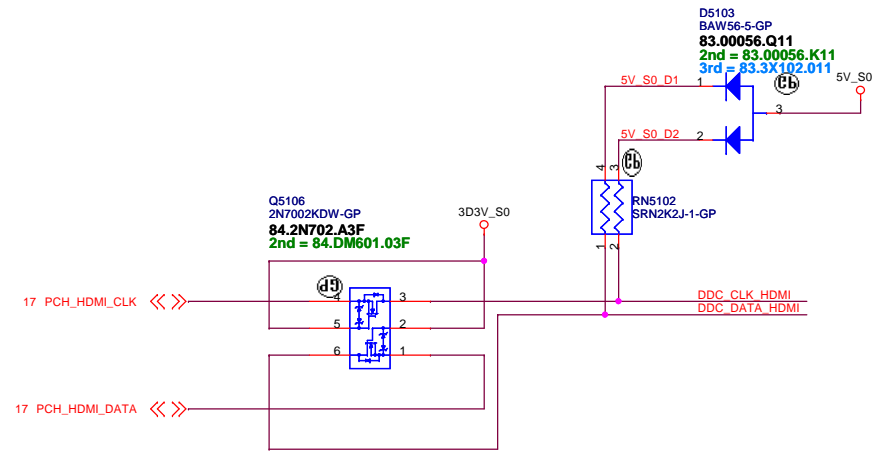
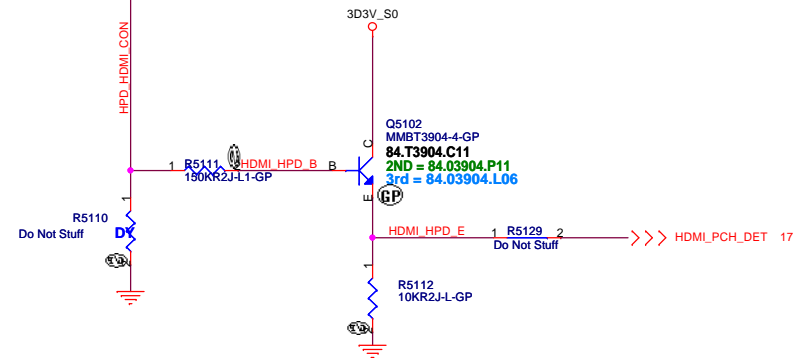
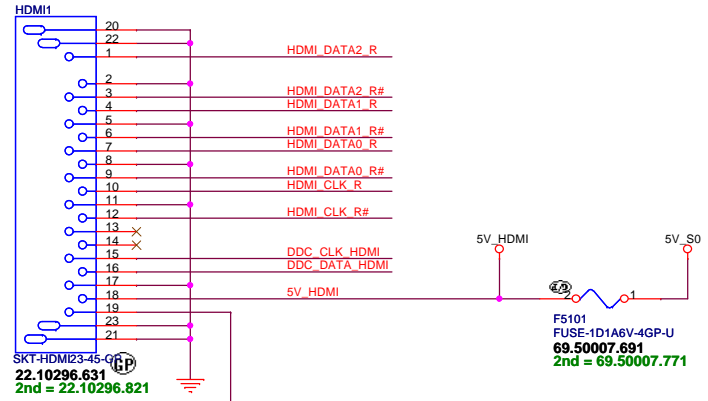
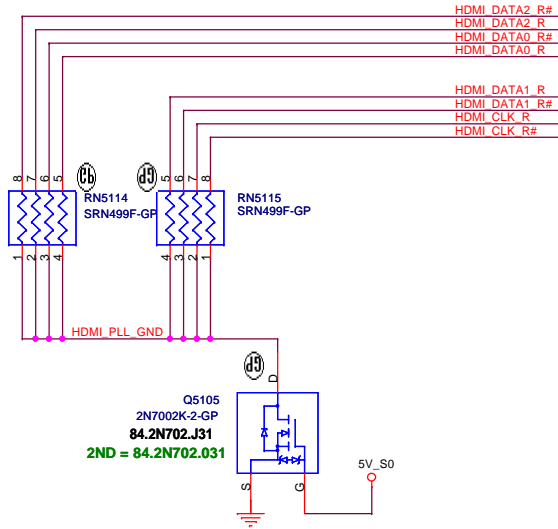
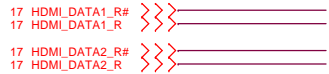
Title			<b>CRT Connector</b>
Size	Document Number	Rev	
A3	<b>Husk/Petra</b>	<b>-4M</b>	
Date:	Thursday, September 06, 2012	Sheet	50 of 103

SSID = VIDEO

# HDMI Level Shifter & CONNECTOR

Close to HDMI Connector

change = DIS:499 ohm  
Fist = UMA Muxless:680 ohm



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DIS IVB Touch

緯創資通 Wistron Corporation  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **HDMI Level Shifter/Connector**

Size A3 Document Number: **Husk/Petra** Rev: **-4M**

Date: Thursday, September 06, 2012 Sheet 51 of 103

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DIS IVB Touch

緯創資通 <b>Wistron Corporation</b> <small>21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</small>	
<b>Title</b> <b>eDP</b>	
<b>Size</b> A3	<b>Document Number</b> <b>Husk/Petra</b>
<b>Date:</b> Thursday, September 06, 2012	<b>Rev</b> <b>-4M</b>
Sheet 52 of 103	

(Blanking)

DIS IVB Touch

**緯創資通** **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title		
<b>S-VIDEO</b>		
Size	Document Number	Rev
A4	<b>Husk/Petra</b>	<b>-4M</b>
Date:	Thursday, September 06, 2012	Sheet 53 of 103

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(Blanking)

DIS IVB Touch

**緯創資通** **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

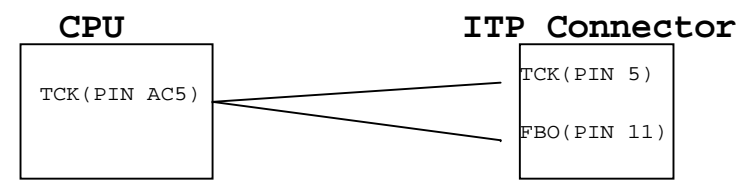
Title		
<b>Reserved</b>		
Size	Document Number	Rev
A4	<b>Husk/Petra</b>	<b>-4M</b>
Date:	Thursday, September 06, 2012	Sheet 54 of 103

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**SSID = User.Interface**

# *ITP Connector*

H\_CPURST# use pull-up Resistor close  
ITP connector 500 mil ( max ),  
others place near CPU side.



DIS IVB Touch

緯創資通

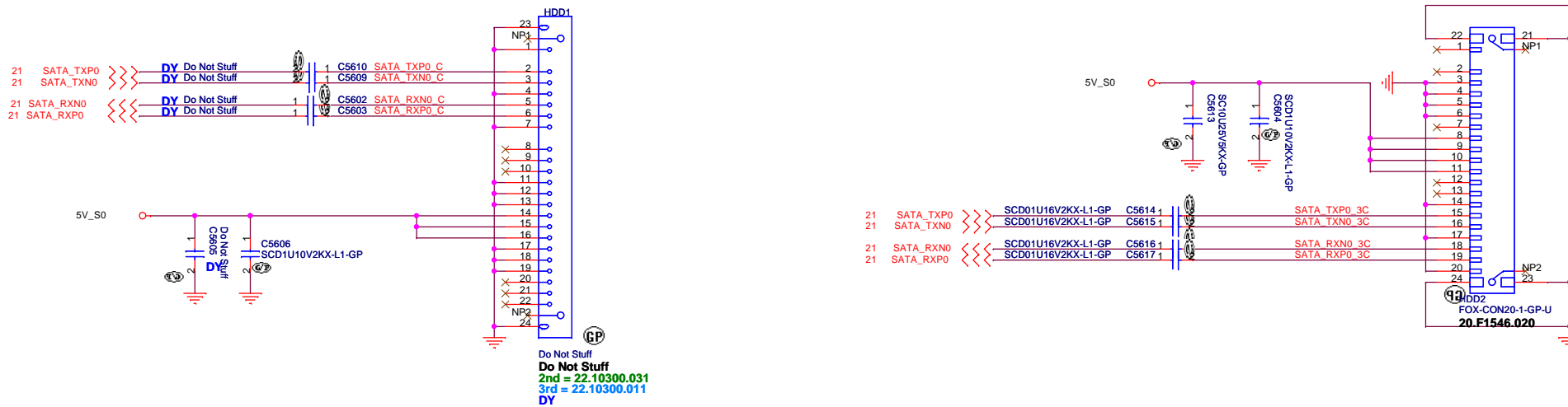
**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

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Title			<b>ITP</b>		
Size	Document Number		Rev		
A4	<b>Husk/Petra</b>		<b>-4M</b>		
Date:	Thursday, September 06, 2012		Sheet	55	of 103

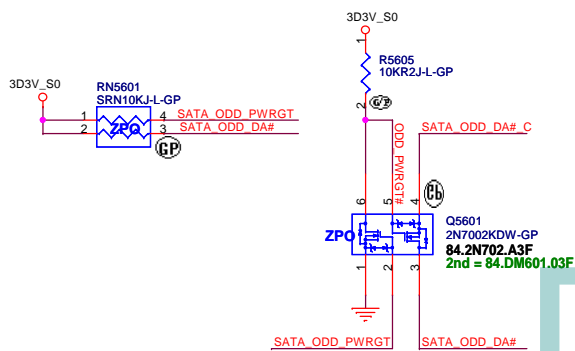
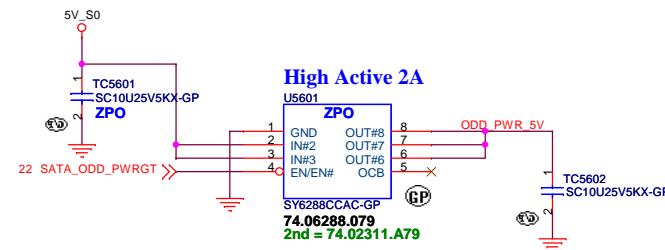
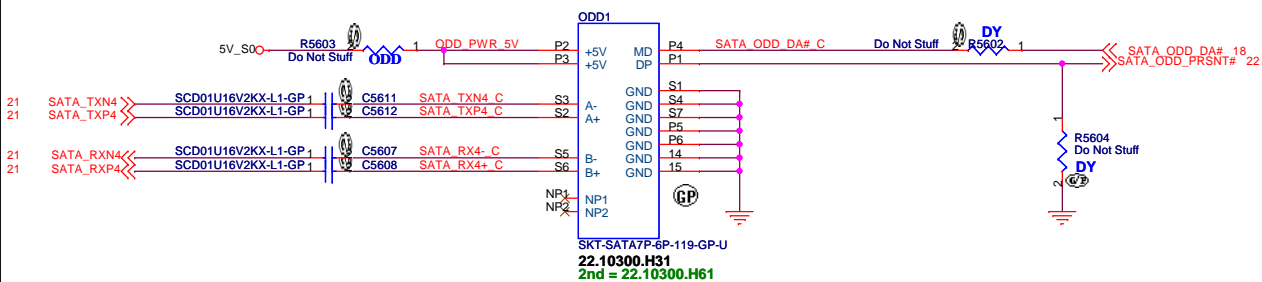
SSID = SATA

# SATA HDD Connector



# ODD Connector

## SATA Zero Power ODD



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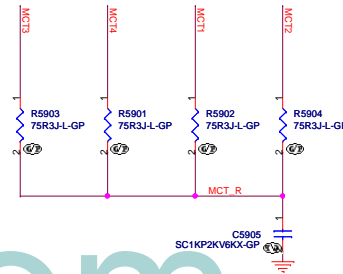
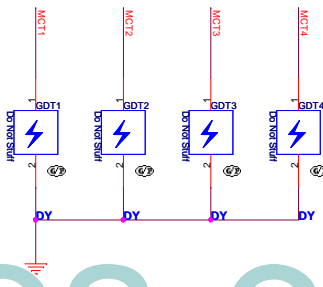
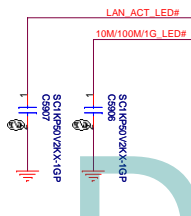
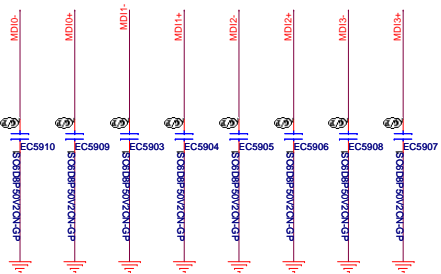
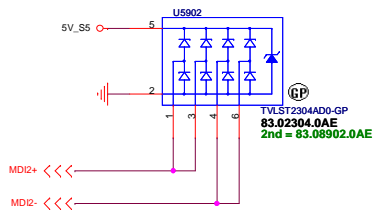
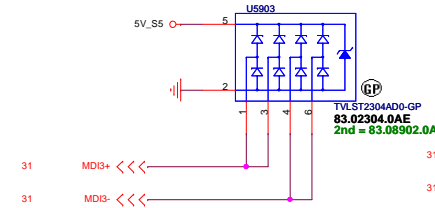
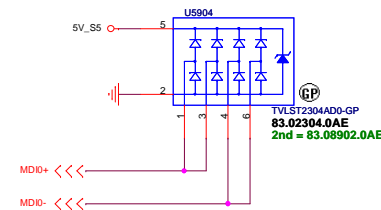
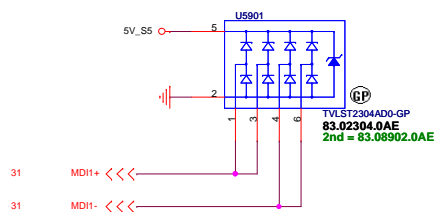
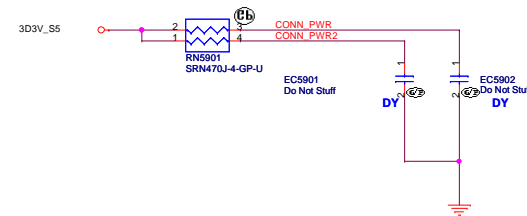
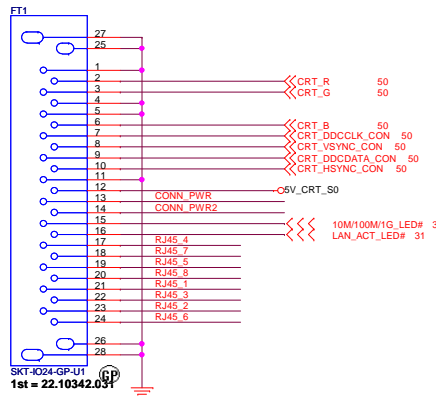
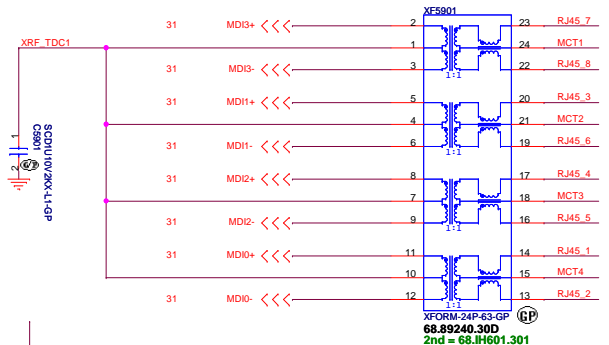
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DIS IVB Touch

緯創資通		<b>Wistron Corporation</b> 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		<b>E-SATA/USB CHARGER</b>	
Size A3	Document Number <b>Husk/Petra</b>	Rev <b>-4M</b>	
Date: Thursday, September 06, 2012	Sheet 57	of	103



**SSID = LAN**



DIS I/B Touch

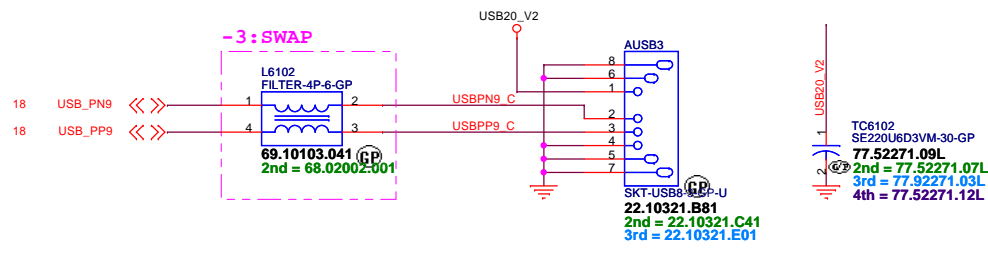
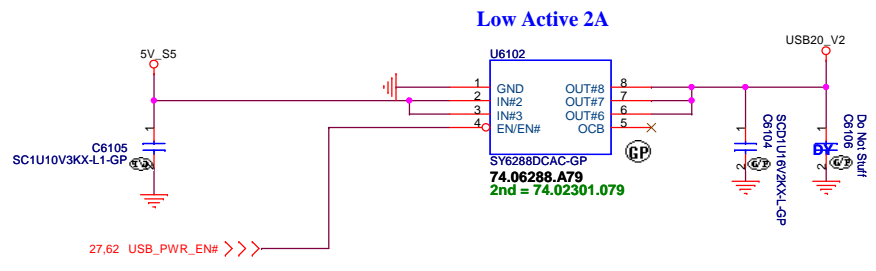
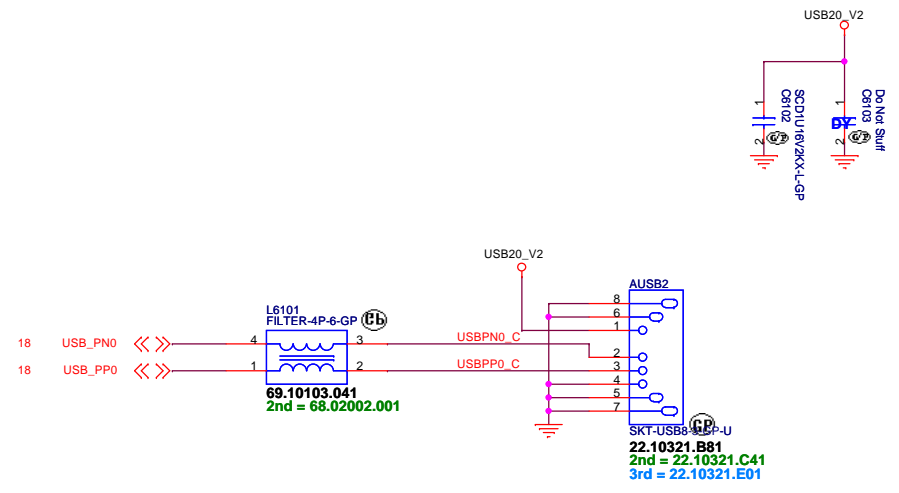
緯創資通 Wistron Corporation  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN CONNECTOR  
Size: Document Number: Husk/Petra  
Date: Monday, November 12, 2012 Sheet 59 of 103

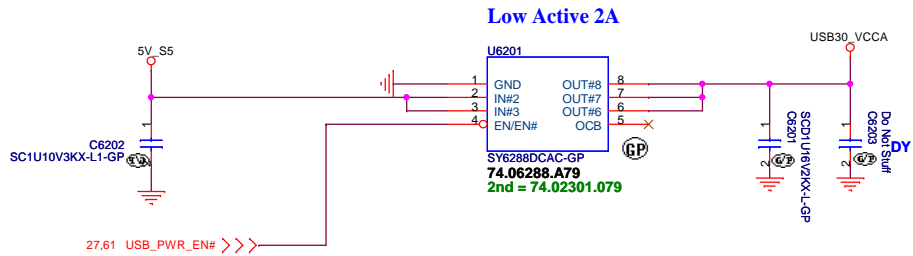
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SSID = USB



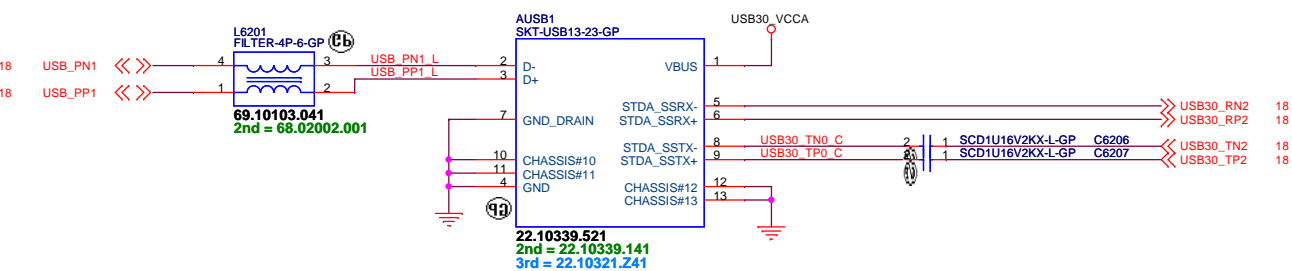
Dr-Bios.com



**Low Active 2A**

U6201  
SY6288DCAC-GP  
74.06288.A79  
2nd = 74.02301.079

27.61 USB\_PWR\_EN# >>>



L6201  
FILTER-4P-6-GP  
69.10103.041  
2nd = 68.02002.001

AUSB1  
SKT-USB13-23-GP  
22.10339.521  
2nd = 22.10339.141  
3rd = 22.10321.241

TC6201  
SE220U6D3VM-30-GP  
77.52271.09L  
2nd = 77.52271.07L  
3rd = 77.92271.03L  
4th = 77.52271.12L

USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+

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DIS IVB Touch

**緯創資通 Wistron Corporation**  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB 3.0 Port**

Size A3 Document Number: **Husk/Petra** Rev: **-4M**

Date: Thursday, September 13, 2012 Sheet 62 of 103

**SSID = User.Interface**  
Bluetooth Module conn.

## *ANNIE Bluetooth Module*

DIS IVB Touch

**緯創資通** **Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

Title

**Bluetooth**

Size

Document Number

Rev

A4

**Husk/Petra**

**-4M**

Date: Thursday, September 06, 2012

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5

4

3

2

1

D

D

C

C

B

B

A

A

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DIS IVB Touch

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--

Title		<b>RESERVED</b>
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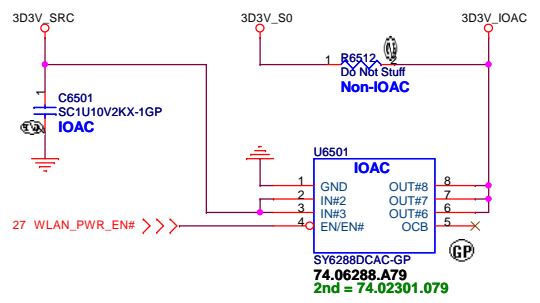
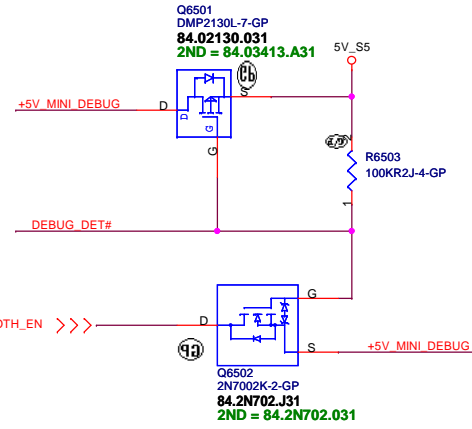
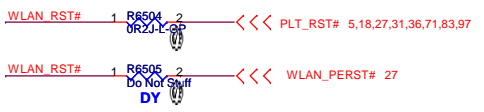
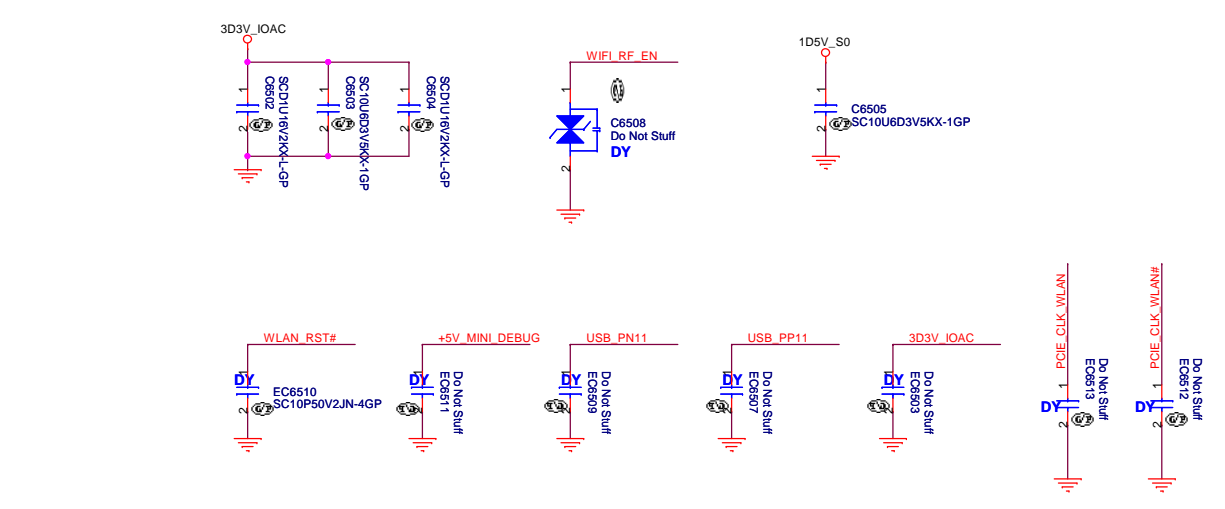
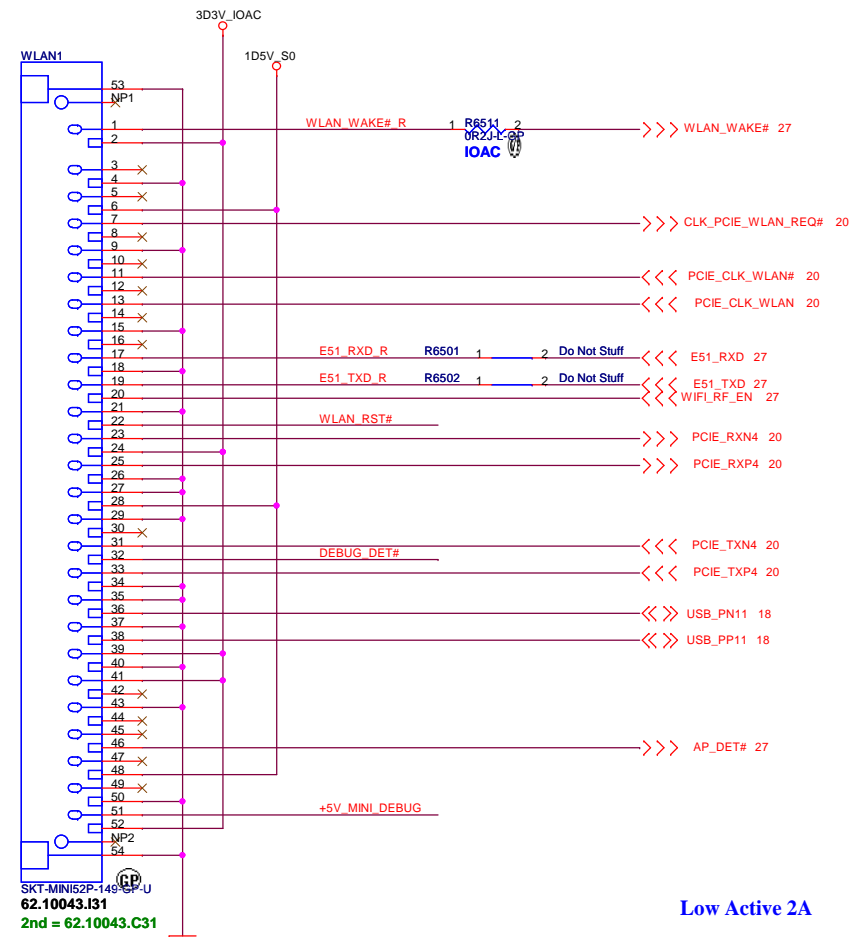
Size	Document Number	Rev
A4	<b>Husk/Petra</b>	<b>-4M</b>

Date: Thursday, September 06, 2012	Sheet 64 of 103
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**SSID = Wireless**

# Mini Card Connector(802.11a/b/g/n)



Low Active 2A

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DIS IVB Touch

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Title: **MINICARD(WLAN)/TP CONN**

Size: A3 Document Number: Husk/Petra Rev: -4M

Date: Friday, December 21, 2012 Sheet 65 of 103

SSID = Wireless

# Mini Card Connector(WWAN)

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緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title

**WWAN Connector**

Size  
A4

Document Number

**Husk/Petra**

Rev

**-4M**

Date: Thursday, September 06, 2012

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Taipei Hsien 221, Taiwan, R.O.C.

Title

**Reserved**

Size

A4

Document Number

**Husk/Petra**

Rev

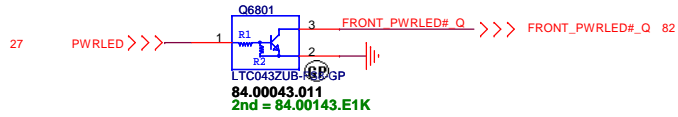
**-4M**

Date: Thursday, September 06, 2012

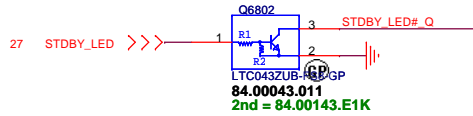
Sheet 67 of 103

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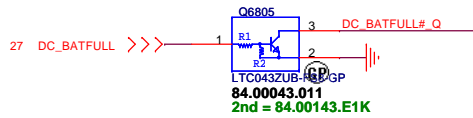
## Power button LED



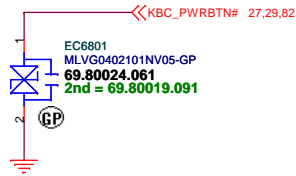
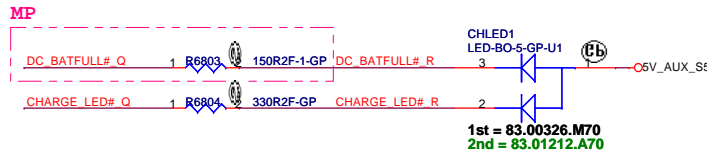
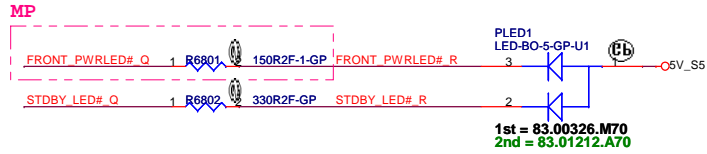
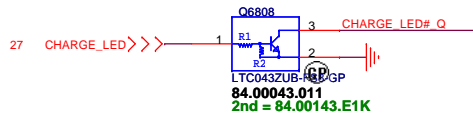
## Power STDBY\_LED



## Battery LED2 (DC\_BATFULL)



## Battery LED1 (CHARGE)



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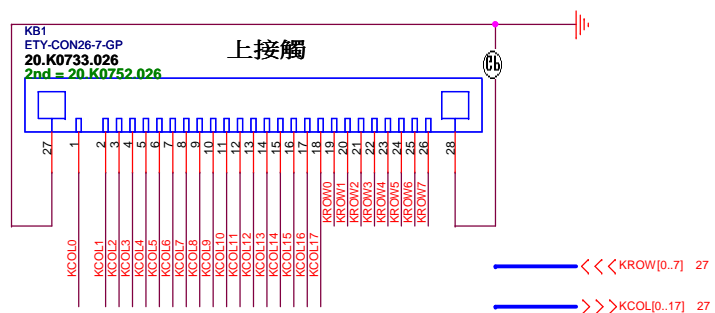
緯創資通 Wistron Corporation  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title <b>LED Bard/Power Button</b>		
Size Custom	Document Number <b>Husk/Petra</b>	Rev <b>-4M</b>
Date: Thursday, September 06, 2012	Sheet 68 of 103	

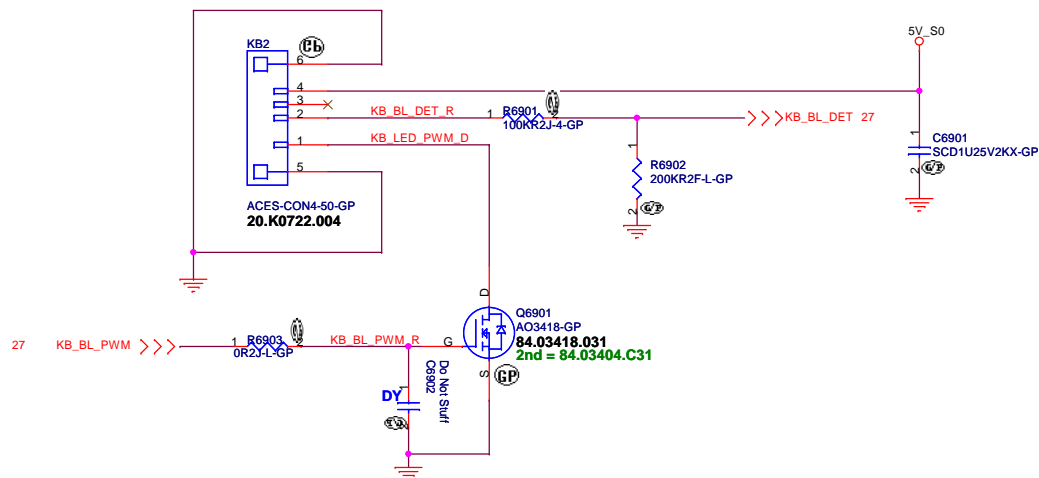
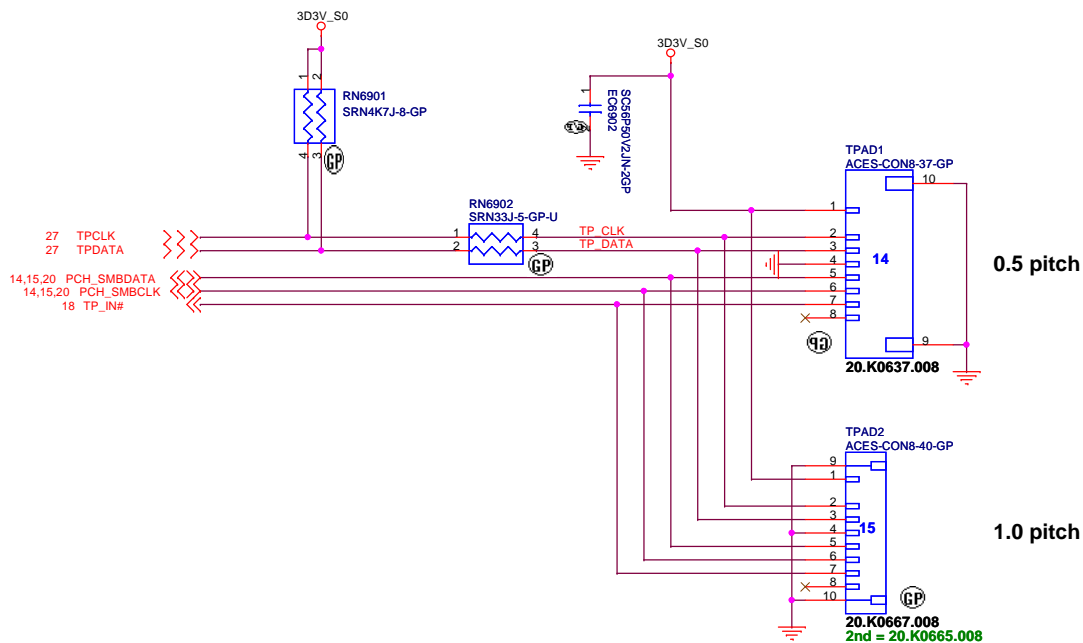
SSID = KBC

# Internal KeyBoard Connector

# TOUCH PAD



R01	R02	R03	R04	R05	R06	R07	R08	R09	R10	R11	R12	R13	R14	R15	R16	R17	R18	C01	C02	C03	C04	C05	C06	C07	C08	VIEW FROM TOP SIDE
26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	PIN NUMBER

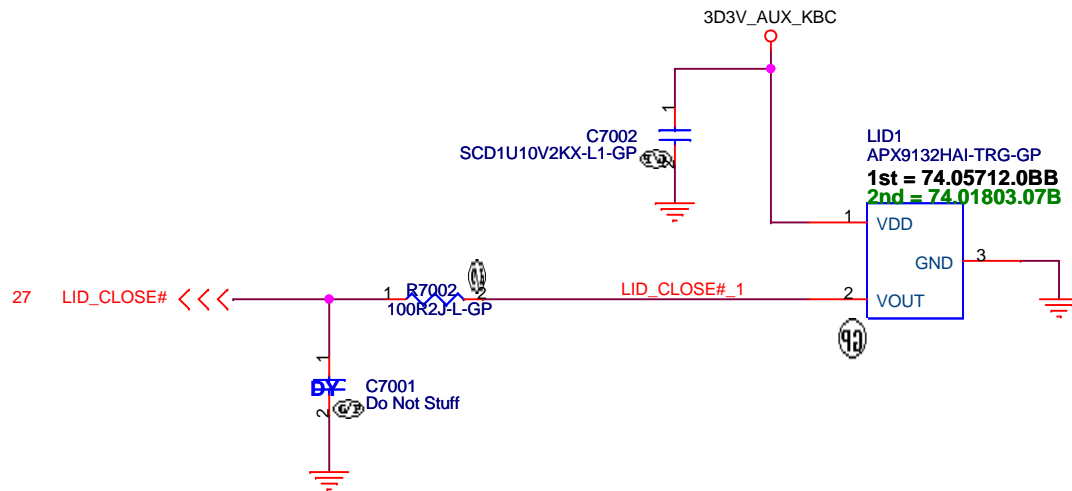


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Title			<b>Key Board/Touch Pad</b>		
Size	Document Number				Rev
A3	<b>Husk/Petra</b>				<b>-4M</b>
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Taipei Hsien 221, Taiwan, R.O.C.

Title

**Hall Sensor**

Size  
A4

Document Number

**Husk/Petra**

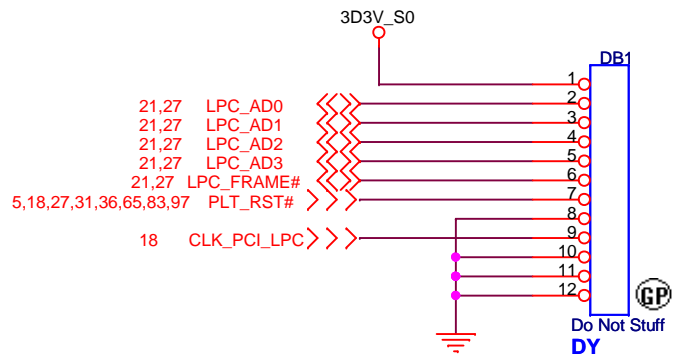
Rev

**-4M**

Date: Thursday, September 06, 2012

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Title

**Dubug connector**

Size  
A4

Document Number

**Husk/Petra**

Rev

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Date: Thursday, September 06, 2012

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緯創資通 <b>Wistron Corporation</b> 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>Reserved</b>	
Size A3	Document Number <b>Husk/Petra</b>
Date: Thursday, September 06, 2012	Sheet 72 of 103
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(Blanking)

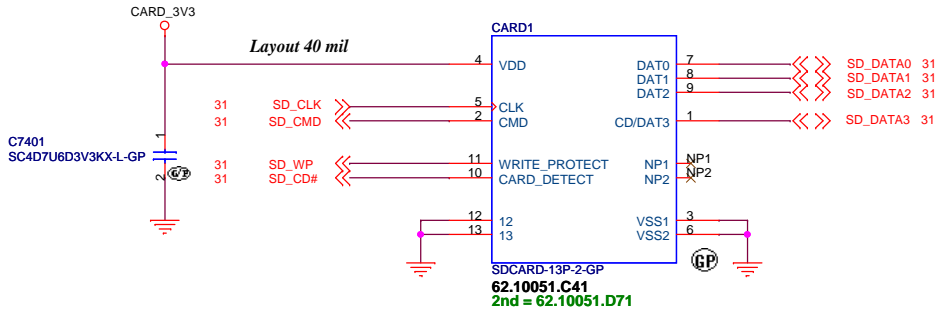
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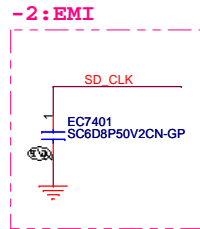
緯創資通		<b>Wistron Corporation</b>	
		21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>Reserved</b>			
Size	Document Number	Rev	
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**SSID = SDIO**

# SD/MMC Card Reader



SP1	SP1	SD_D7	MS_INS#	xD_RDY
SP2	SP2	SD_D6	MS_INS#	xD_RE#
SP3	SP3	SD_D5	MS_INS#	xD_CE#
SP4	SP4	SD_D4	MS_INS#	xD_WE#
SP5	SP5	SD_D1	MS_CLK	xD_D6
SP6	SP6	SD_D0	MS_D7	xD_D5
SP7	SP7	SD_CLK	MS_D3	xD_D4
SP8	SP8	SD_CMD	MS_D6	xD_D3
SP9	SP9	SD_D3	MS_D2	xD_D2
SP10	SP10	SD_D2	MS_D2	xD_D7
SP11	SP11	SD_D2	MS_BS	xD_CLE
SP12	SP12	SD_WP	MS_D1	xD_WP#
SP13	SP13	SD_CD#	MS_D5	xD_ALE
SP14	SP14	MS_D4	MS_D4	xD_D0
SP15	SP15	MS_D0	MS_D0	xD_D1
SP16	SP16	MS_D0	MS_D0	xD_CD#



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Title		
CARD Reader CONN		
Size	Document Number	Rev
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SSID = ExpressCard

+1.5V\_CARD Max. 650mA, Average 500mA.  
+3.3V\_CARD Max. 1300mA, Average 1000mA  
+3.3V\_CARDAUX Max. 275mA

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		21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>New Card</b>			
Size	Document Number		Rev
A3	<b>Husk/Petra</b>		<b>-4M</b>
Date:	Thursday, September 06, 2012	Sheet	75 of 103

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Taipei Hsien 221, Taiwan, R.O.C.

Title **Reserved**

Size A4 Document Number **Husk/Petra** Rev **-4M**

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<b>緯創資通</b>		<b>Wistron Corporation</b>
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title **Reserved**

Size A4	Document Number <b>Husk/Petra</b>	Rev <b>-4M</b>
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Title

**Reserved**

Size  
A4

Document Number

**Husk/Petra**

Rev

**-4M**

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**SSID = User.Interface**

## Free Fall Sensor

Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

DIS IVB Touch

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Title

**G- Sensor**

Size  
A4

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5

4

3

2

1

D

D

C

C

B

B

A

A

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DIS IVB Touch

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Title	
<b>Reserved</b>	

Size	Document Number	Rev
A4	<b>Husk/Petra</b>	<b>-4M</b>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

**Reserved**

Size  
A4

Document Number

**Husk/Petra**

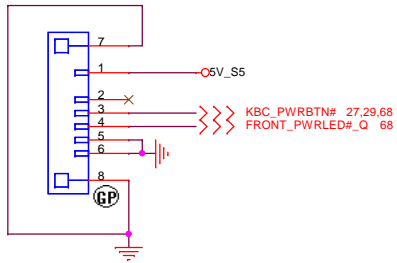
Rev  
**-4M**

Date: Thursday, September 06, 2012

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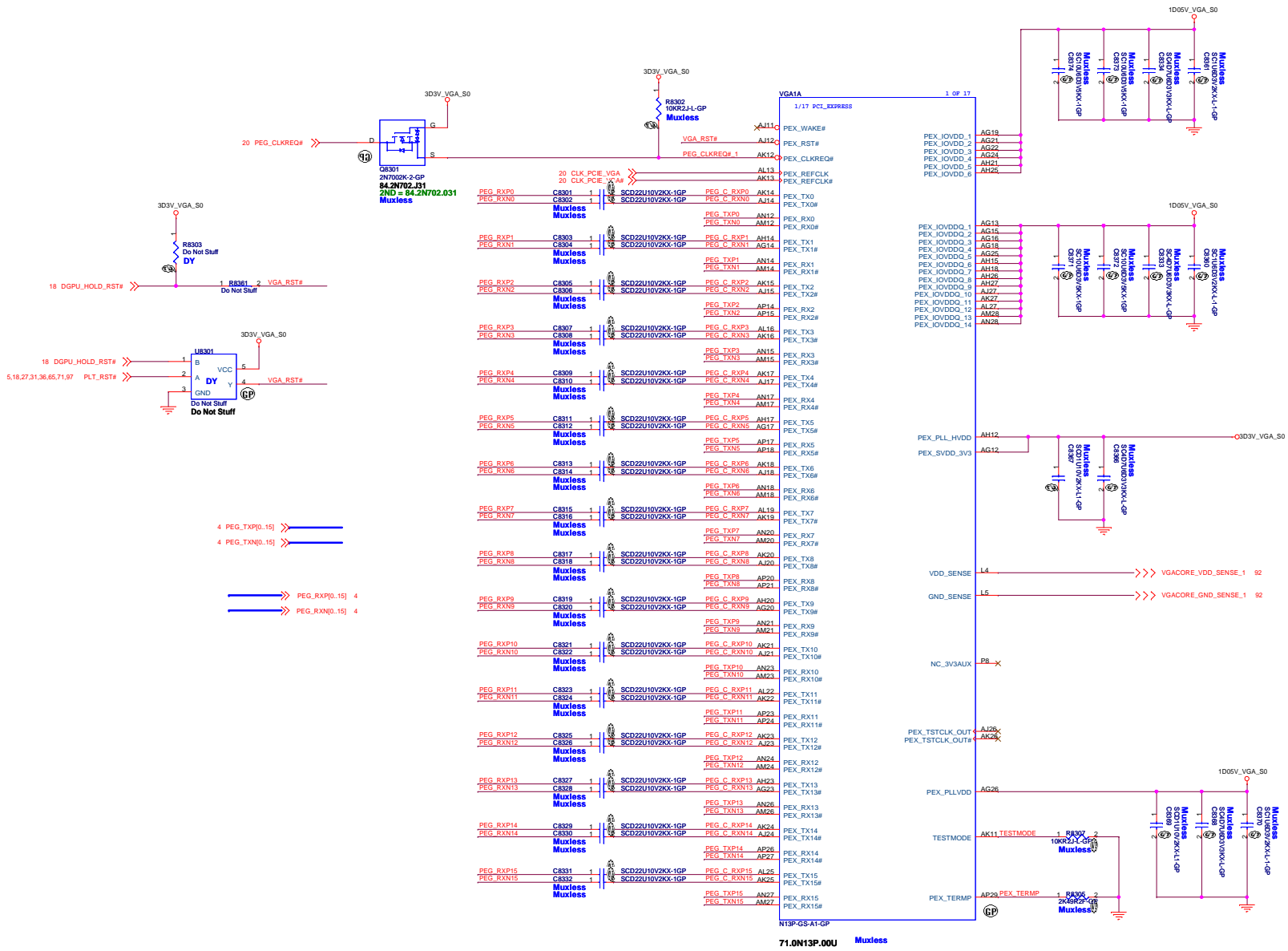
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ACES-CON6-52-GP  
20.K0721.006  
2nd = 20.K0382.006



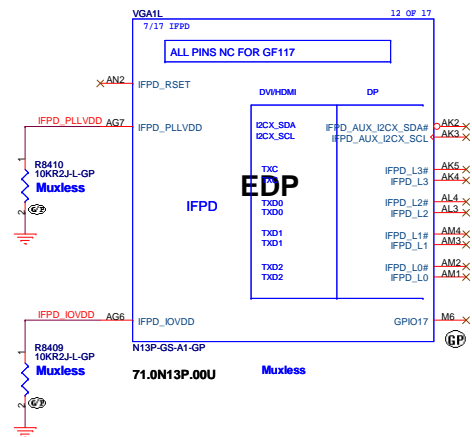
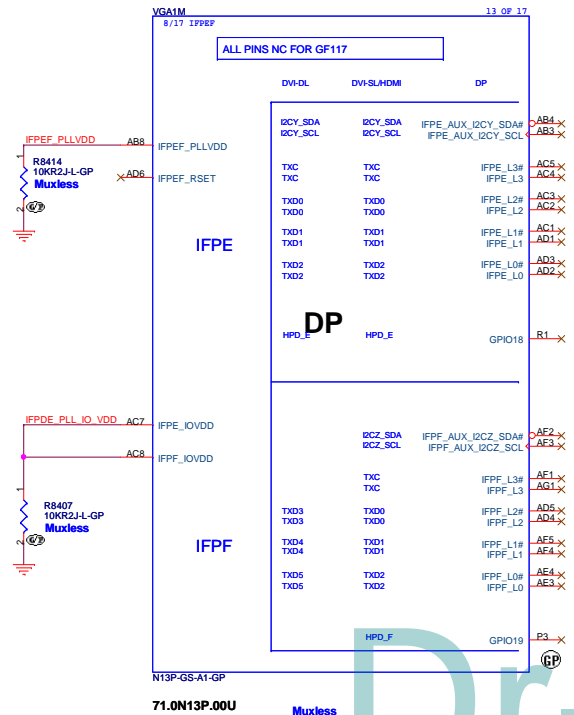
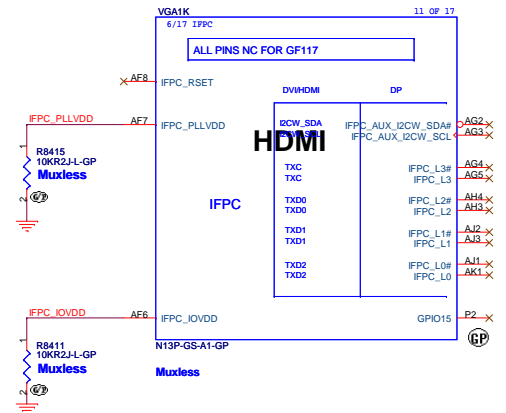
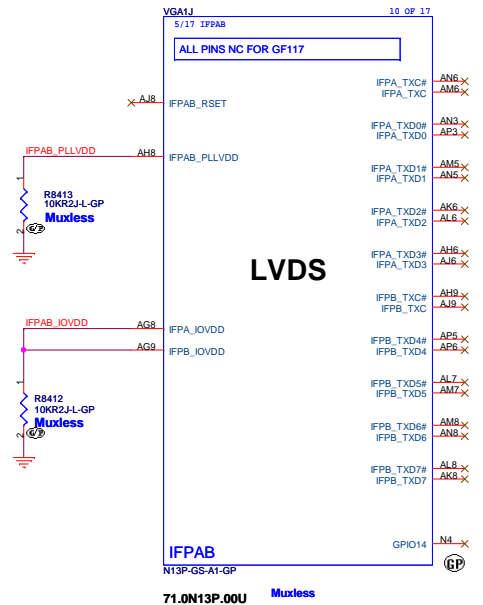
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		21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
IO Board Connector			
Size	Document Number	Rev	
A3	Husk/Petra	-4M	
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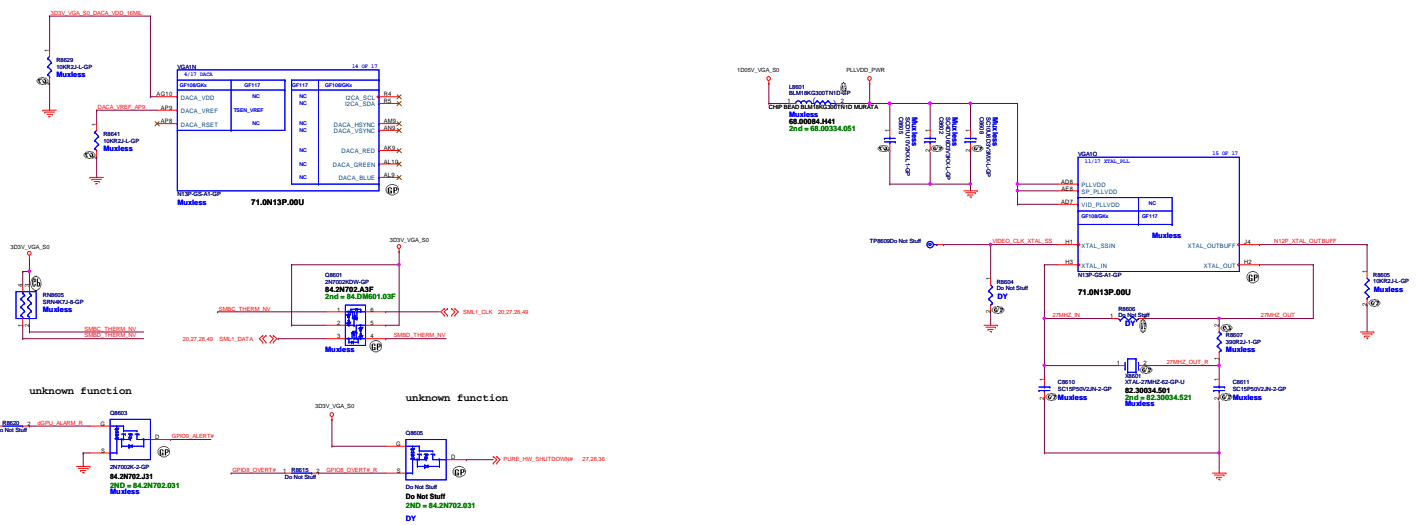


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GPIO#	OVERT	I/O	Action
GPIO8	OVERT	I/O	Active Low Thermal Catastrophic Over Temperature
GPIO9	ALERT	I/O	Active Low Thermal Alert
GPIO10	MEM_VREF_CTL	I/O	Memory VREF Control
GPIO11	GPU_VID0	O	GPU Core VDD VID0
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw Input

VRAM Table(N13P-GS/GT/LP/GL/GLP/NS/GE)

	Hynix 2G_B-Die 0110(0x6) 128*16	Hynix 1G_D-die 0010(0x2) 64*16	Samsung 2G_C-Die 0111(0x7) 128*16	Samsung 1G_G-die 0011(0x3) 64*16
5Kohm				
64.49915.6DL				
10Kohm				
64.10025.L0L				
ROM_SI R8627	34.8Kohm 64.34825.6DL	15Kohm 64.15025.6DL	45Kohm 64.45325.6DL	20Kohm 64.20025.6DL

VRAM Table(N13M-GS/NS)

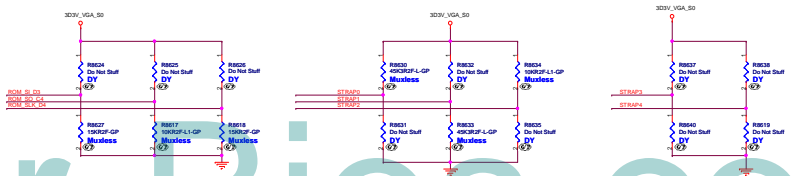
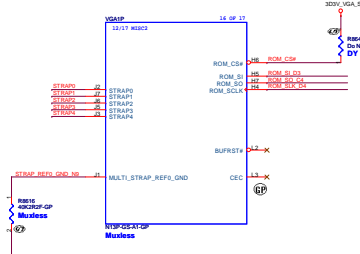
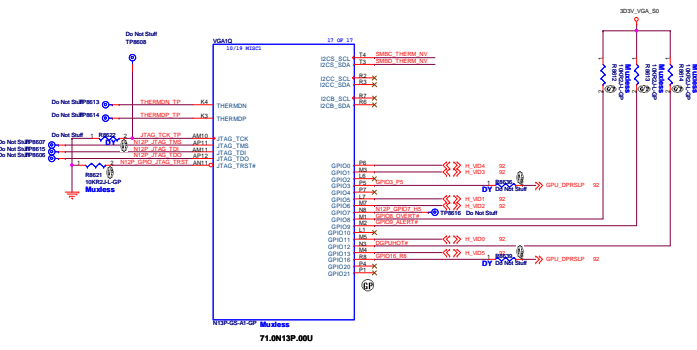
Hynix 2G_D-die 1100(0x6C) 128*16	Hynix 2G_B-die 0110(0x6) 128*16
--	---------------------------------------

Mode	Product	NVCLK (MHz)	MCLK (MHz)	NVVD0 (V)
MAX Point (MP)	H13P-GL/-HS1	800	900	--
	H13P-GLP	660	900	--
TDP Point (TP)	H13P-GL/-HS1	660	900	--
	H13P-GLP	475	900	--
HW Boot Voltage	H13P-GL/-HS1	--	--	0.95
	H13P-GLP	--	--	0.90

Logical Strap Bit Mapping

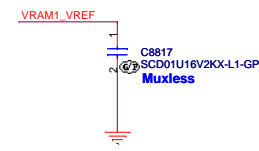
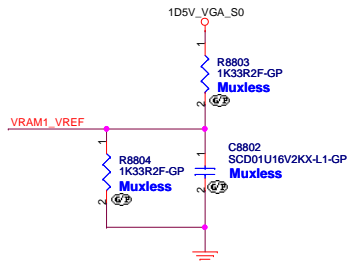
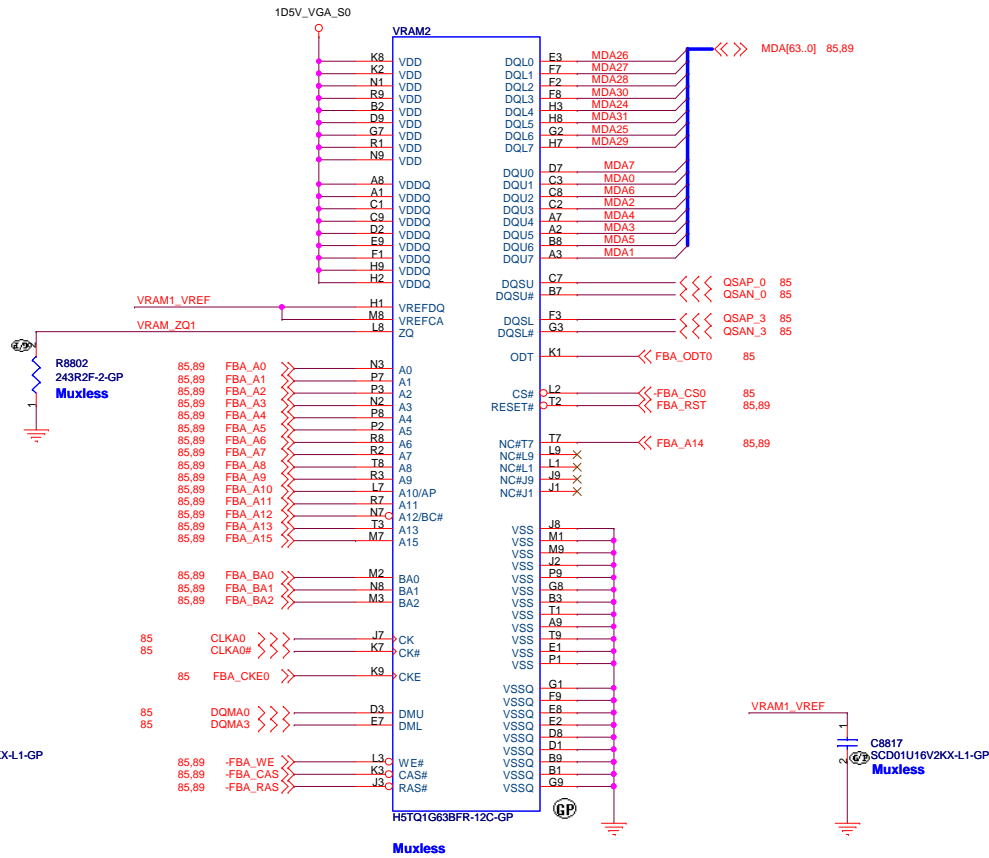
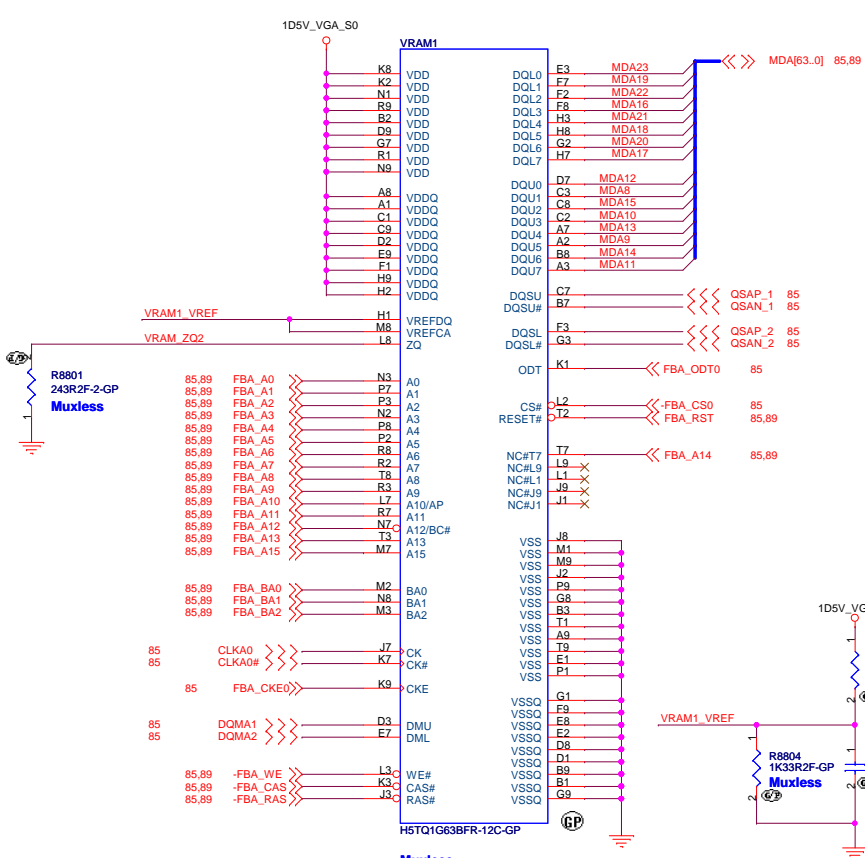
Resistor	Pull-up	Pull-down
50kohms	1001	0000
100kohms	1001	0001
150kohms	1010	0010
200kohms	1011	0011
250kohms	1100	0100
300kohms	1101	0101
350kohms	1110	0110
400kohms	1111	0111

Strap Pin Nmae	Logical strapping name bit#3	Logical strapping name bit#2	Logical strapping name bit#1	Logical strapping name bit#0
ROM_SCLK	PCL.DEVID[4]	SUB.VENDOR	SLOT_CLK_CFG/	PEX_PLL_EN_TERM
	0	0	1	0
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[2]	RAMCFG[0]
	0	0	0	0
ROM_S0	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
	0	0	0	1
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
	1	1	1	1
STRAP1	3GIO_PADCFG[5]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
	0	1	1	1
STRAP2	PCL.DEVID[3]	PCL.DEVID[2]	PCL.DEVID[1]	PCL.DEVID[0]
	1	0	0	1
STRAP3	N/A	N/A	N/A	N/A
STRAP4	N/A	N/A	N/A	N/A

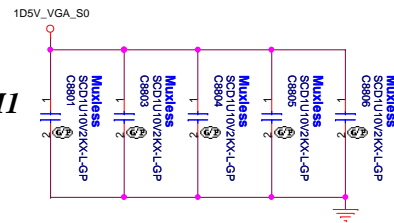


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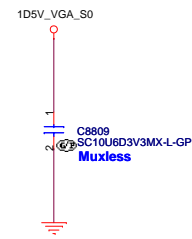
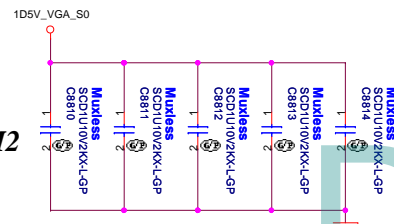




FOR VRAM1

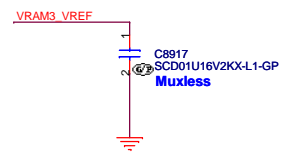
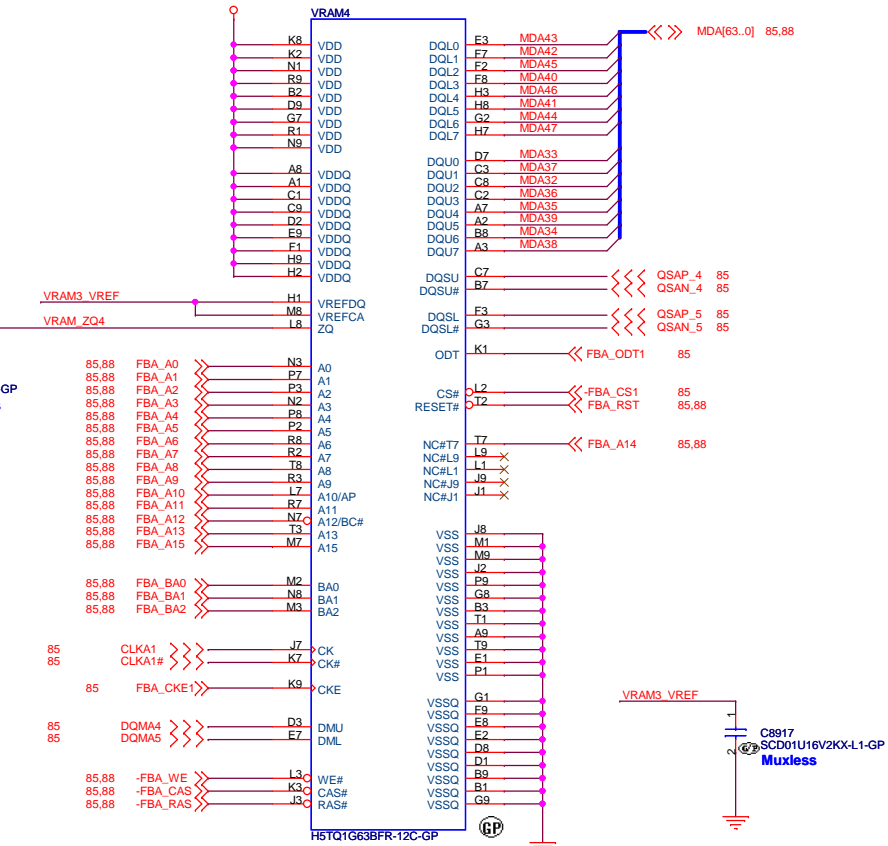
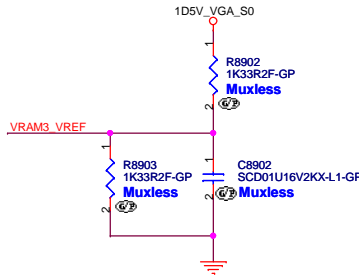
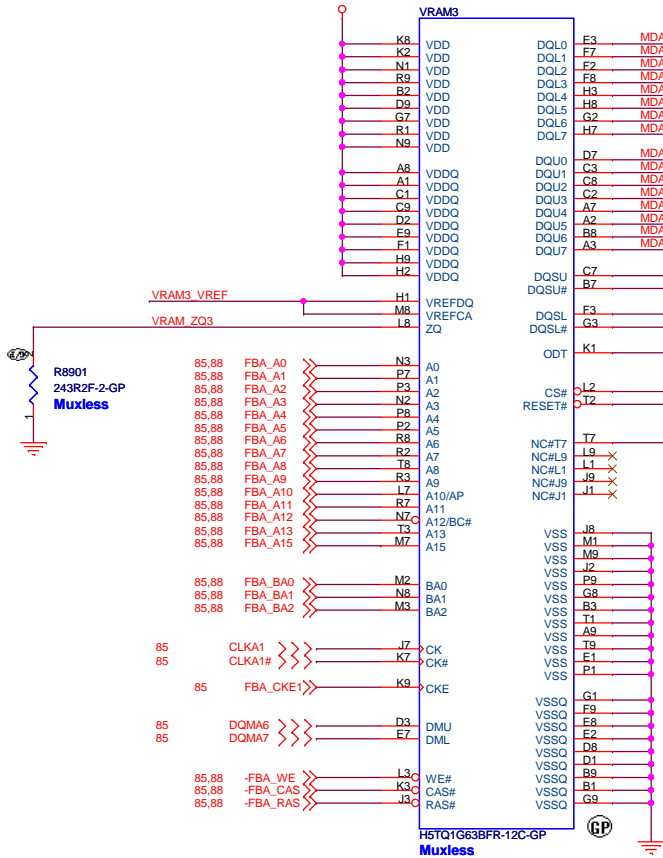


FOR VRAM2

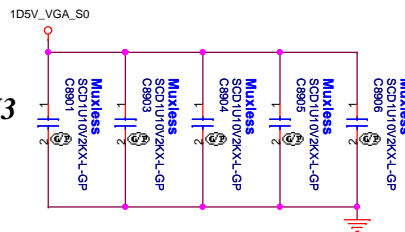


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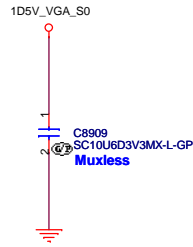
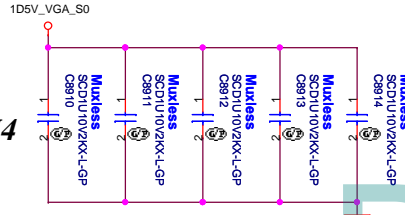




FOR VRAM3



FOR VRAM4



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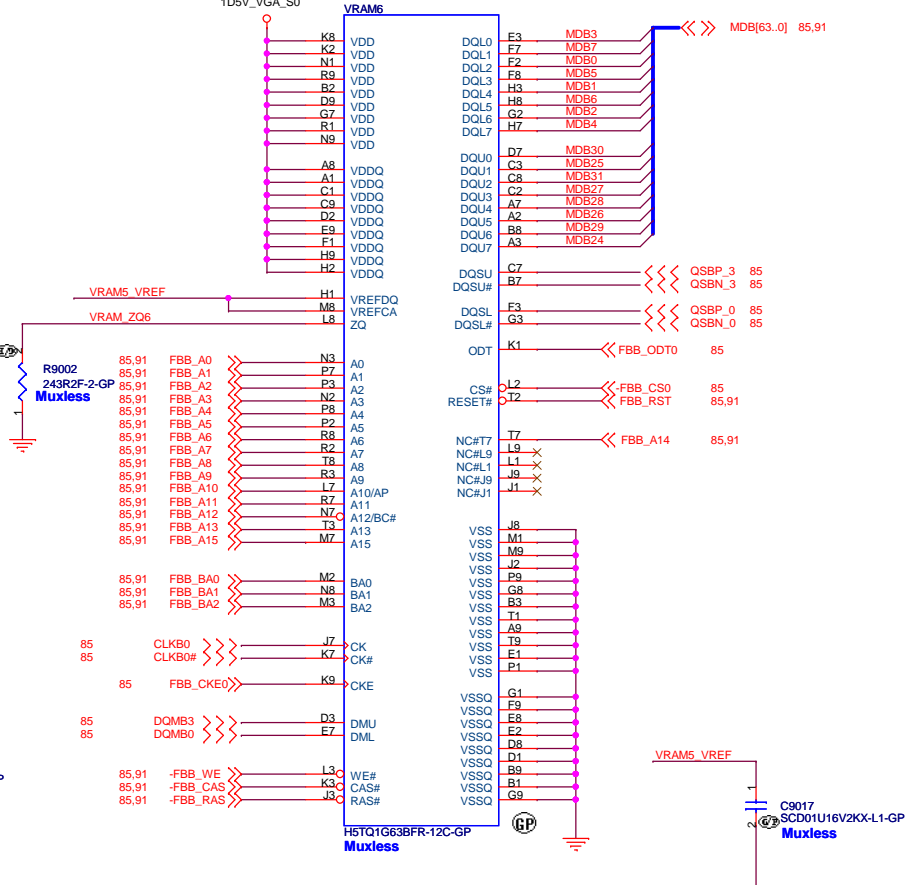
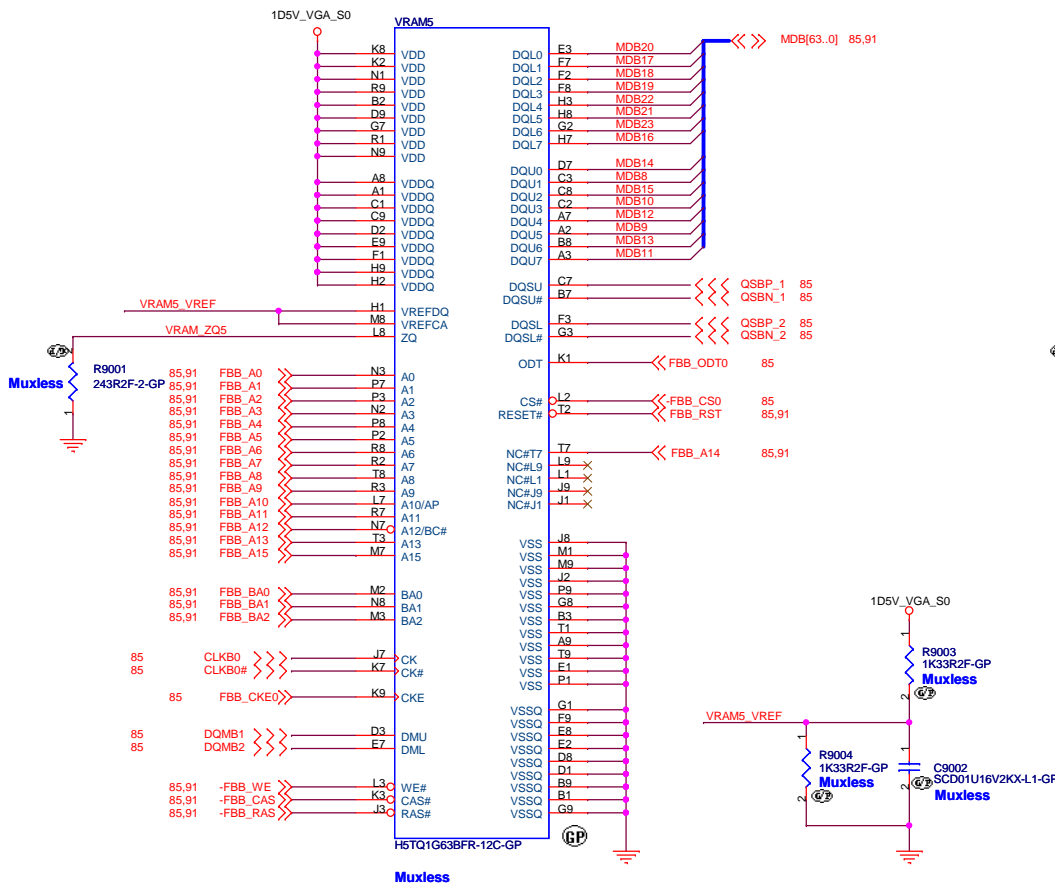
DIS IVB Touch

**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

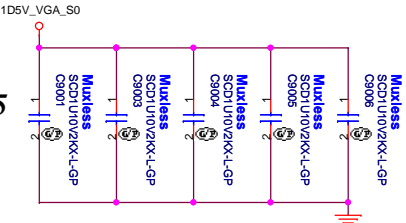
Title: **GPU-VRAM3,4 (2/4)**

Size: Custom Document Number: **Husk/Petra** Rev: **-4M**

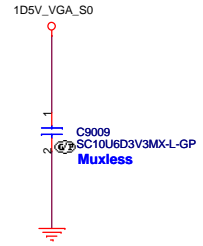
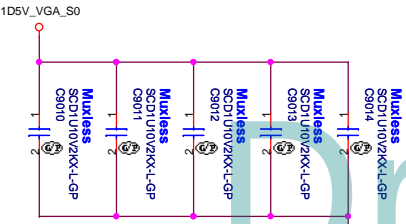
Date: Thursday, September 06, 2012 Sheet 89 of 103



**FOR VRAM5**



**FOR VRAM6**

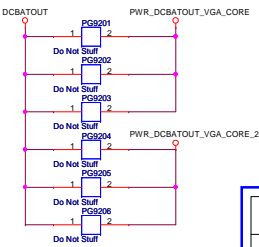


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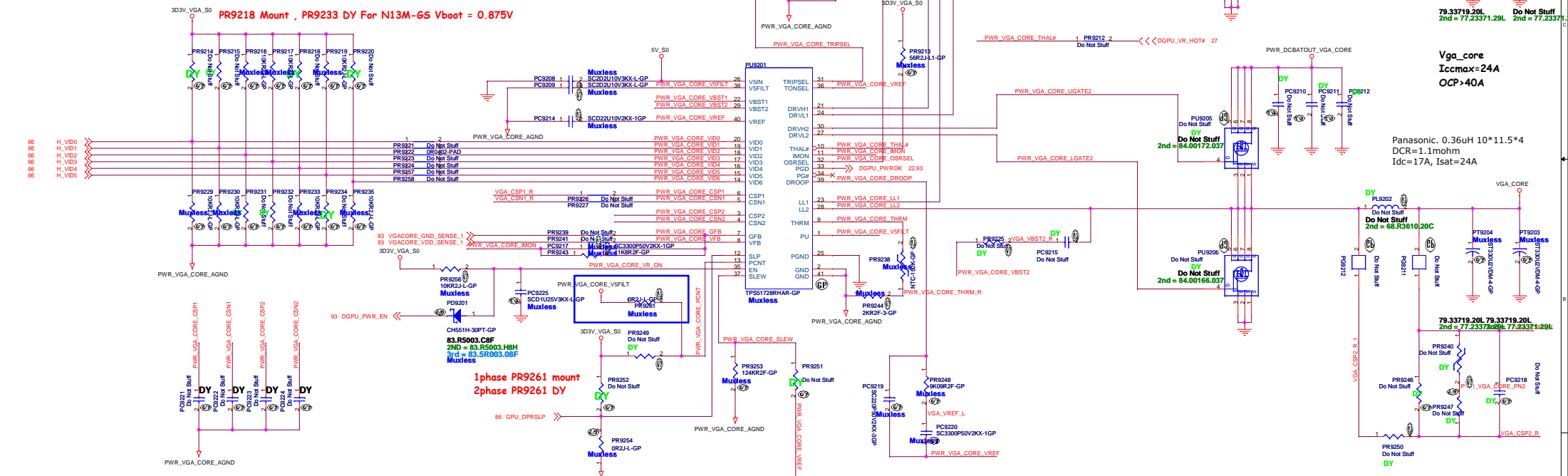
**SSID = PWR.Plane.Regulator\_GFX**

Change power source Net  
Wayler 12/07



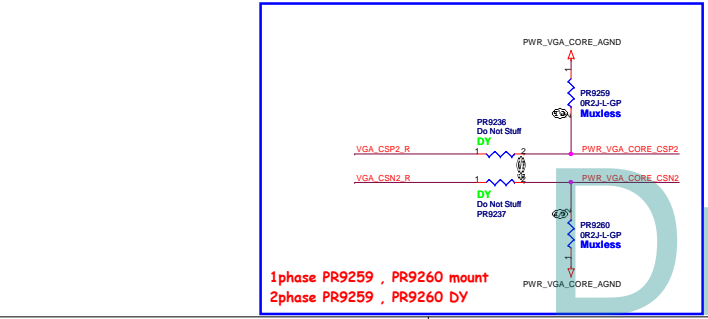
	N13P-GS-LP 71.0N13P.00U	N13P-GL 71.0N13P.B0U	N13M-GS 71.0N13M.E0U
NV_VDD Boot Voltage	0.9V VID[6:0]=0110000	0.95V VID[6:0]=0101100	0.875V VID[6:0]0110010
NV_VID1	PR9215 DY	DY	63.10334.L0L
	PR9230 63.10334.L0L	63.10334.L0L	DY
NV_VID3	PR9217 DY	63.10334.L0L	DY
	PR9232 63.10334.L0L	DY	63.10334.L0L
NV_VID4	PR9218 63.10334.L0L	DY	63.10334.L0L
	PR9233 DY	63.10334.L0L	DY

PR9218 Mount , PR9233 DY For N13M-GS Vboot = 0.875V

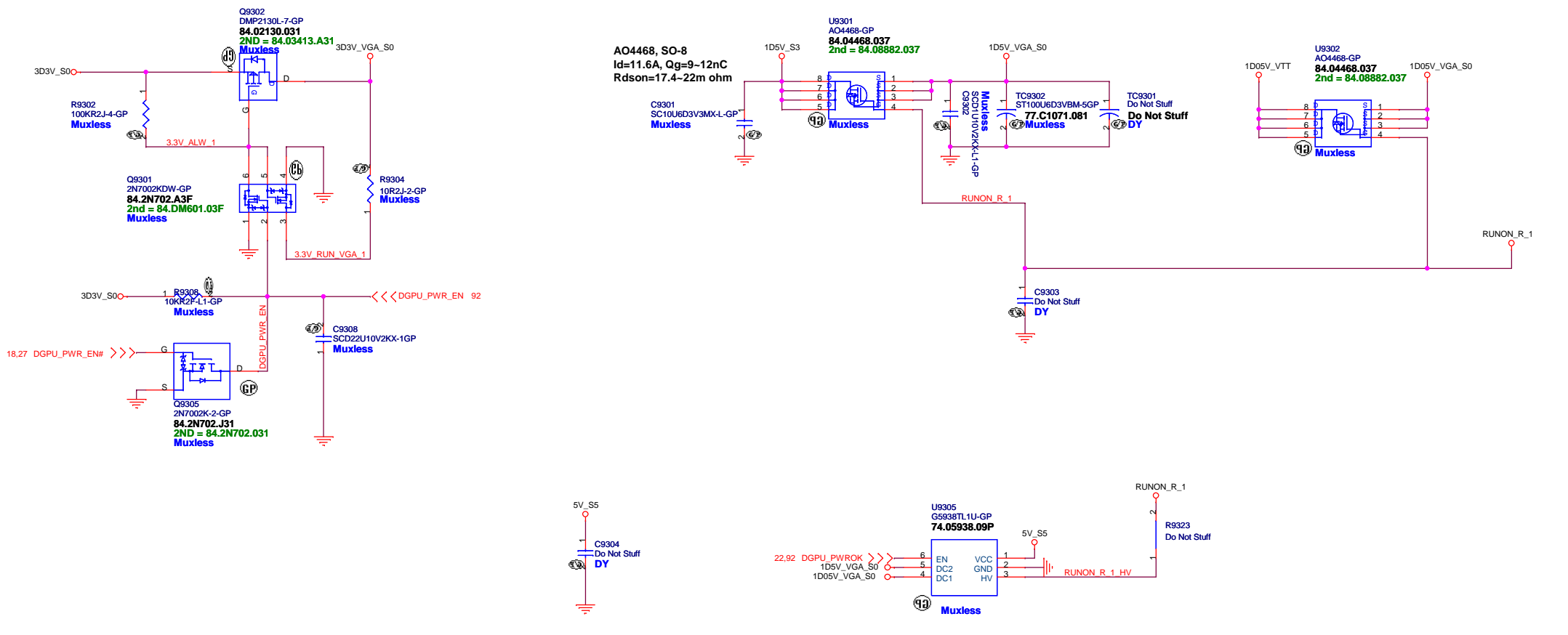


86 H\_VID0  
86 H\_VID1  
86 H\_VID2  
86 H\_VID3  
86 H\_VID4  
86 H\_VID5

83 VGACORE\_GND\_SENSE\_1  
83 VGACORE\_VDD\_SENSE\_1  
83 VGASO



1phase PR9259 , PR9260 mount  
2phase PR9259 , PR9260 DY



DIS IVB Touch

緯創資通		<b>Wistron Corporation</b>	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title		<b>DISCRETE VGA POWER</b>	
Size	Document Number	Rev	
Custom	<b>Husk/Petra</b>	<b>-4M</b>	
Date:	Thursday, September 06, 2012	Sheet	93 of 103

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DIS IVB Touch

<b>緯創資通</b> <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
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Title	<b>LVDS Switch</b>	
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Size	Document Number	Rev
A4	<b>Husk/Petra</b>	<b>-4M</b>

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		21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>CRT Switch</b>			
Size	Document Number	Rev	
A3	<b>Husk/Petra</b>	<b>-4M</b>	
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SSID = SDIO

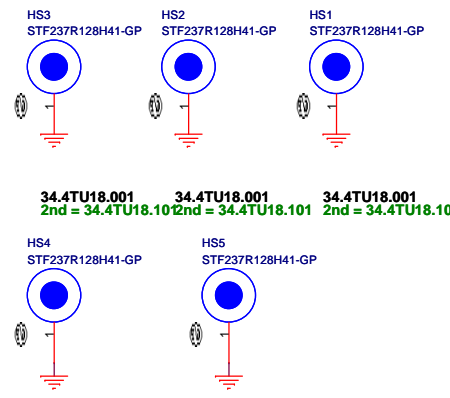
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DIS IWB Touch

緯創資通		Wistron Corporation	
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichia, Taipei Hsien 221, Taiwan, R.O.C.		21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichia, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
TOUCH PANEL			
Size	Document Number	Rev	
A2	Husk/Petra	-4M	
Date:	Thursday, September 06, 2012	Sheet	98 of 100

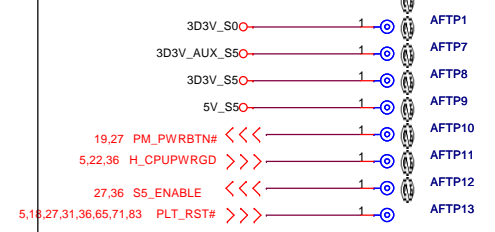


### CPU

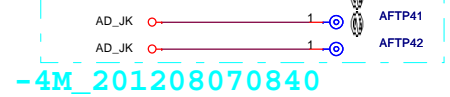
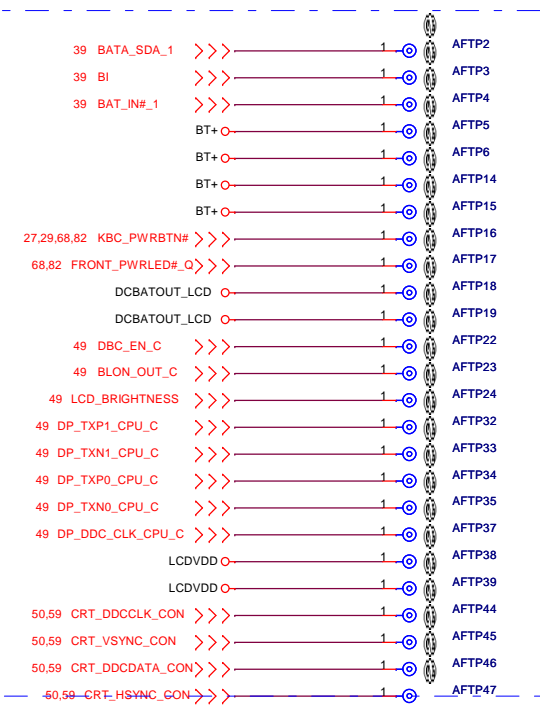
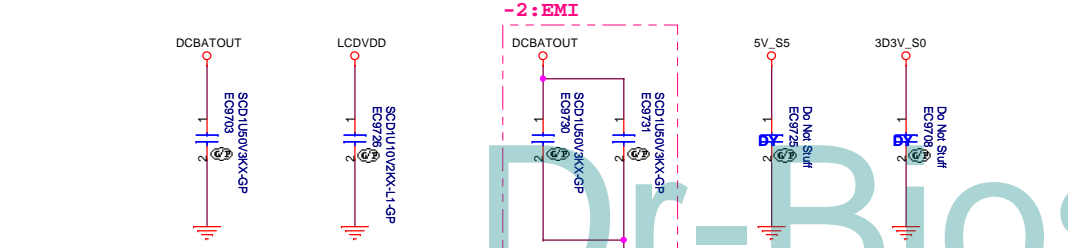
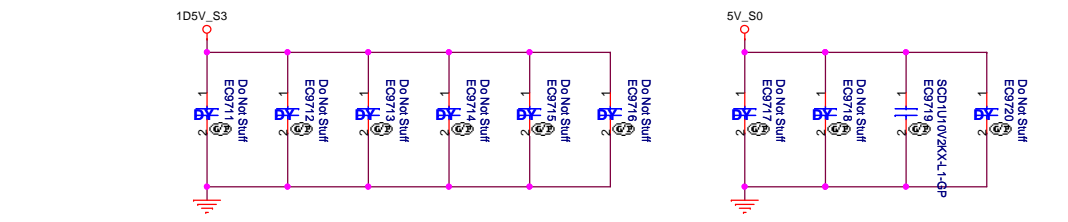
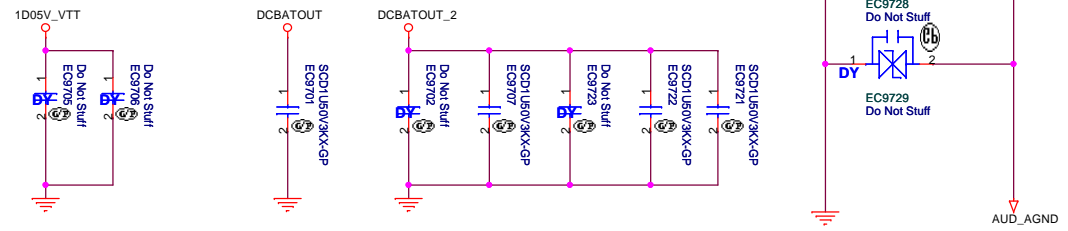
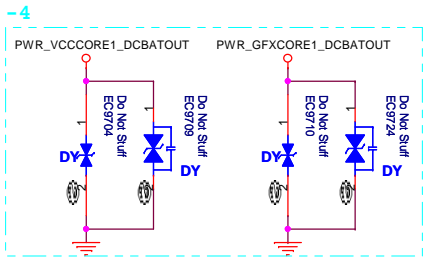


**VGA**  
 34.4TU18.001  
 2nd = 34.4TU18.101  
 Muxless

### Check test point



Test Point放在Dimm Door打開可量測處



-4M-201208070840

-4M-201208031615

DIS I/B Touch

**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsein 221, Taiwan, R.O.C.

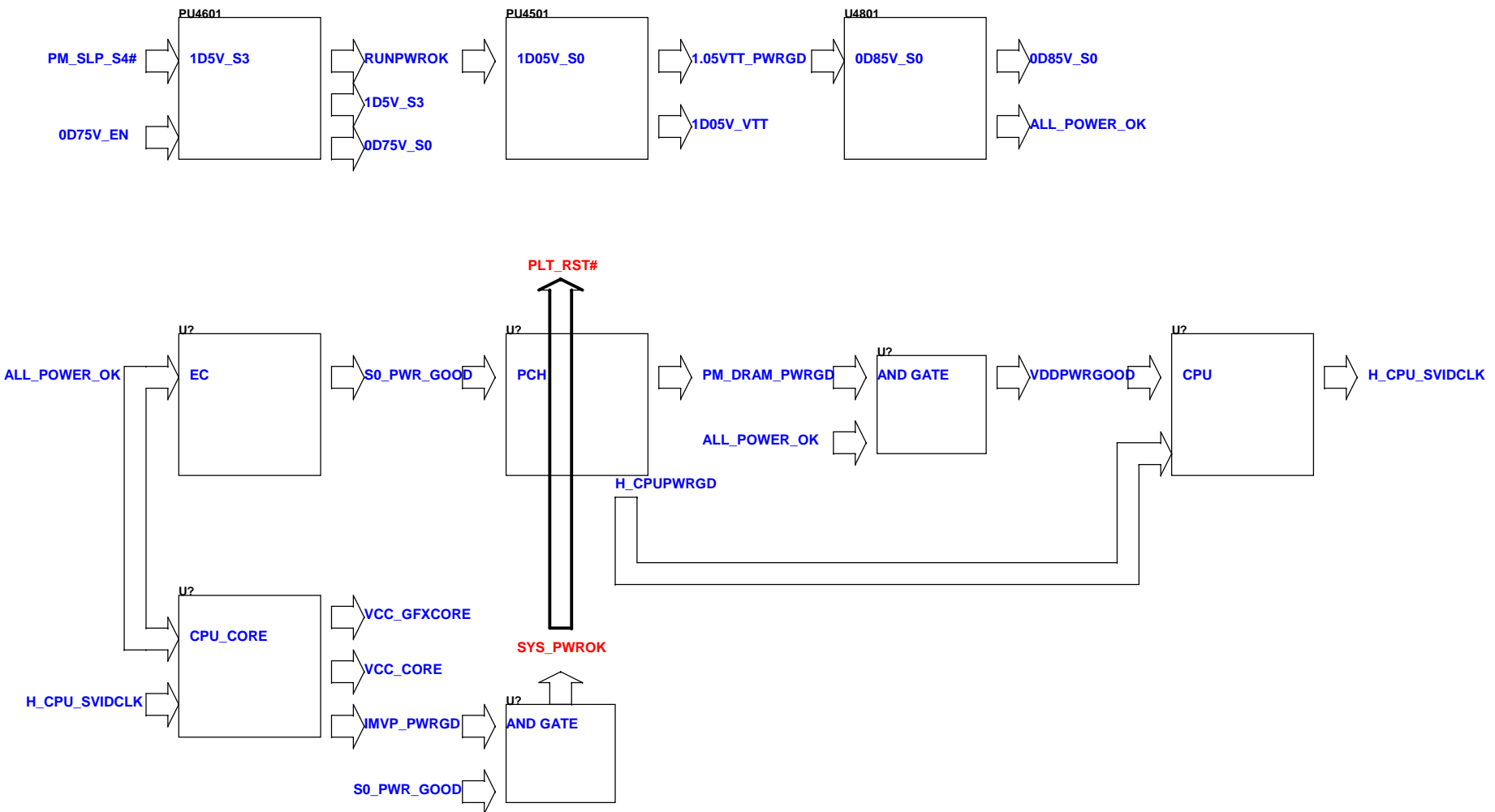
Title: **UNUSED PARTS/EMI Capacitors**

Size: A3 Document Number: **Husk/Petra** Rev: **-4M**

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# Power Sequence



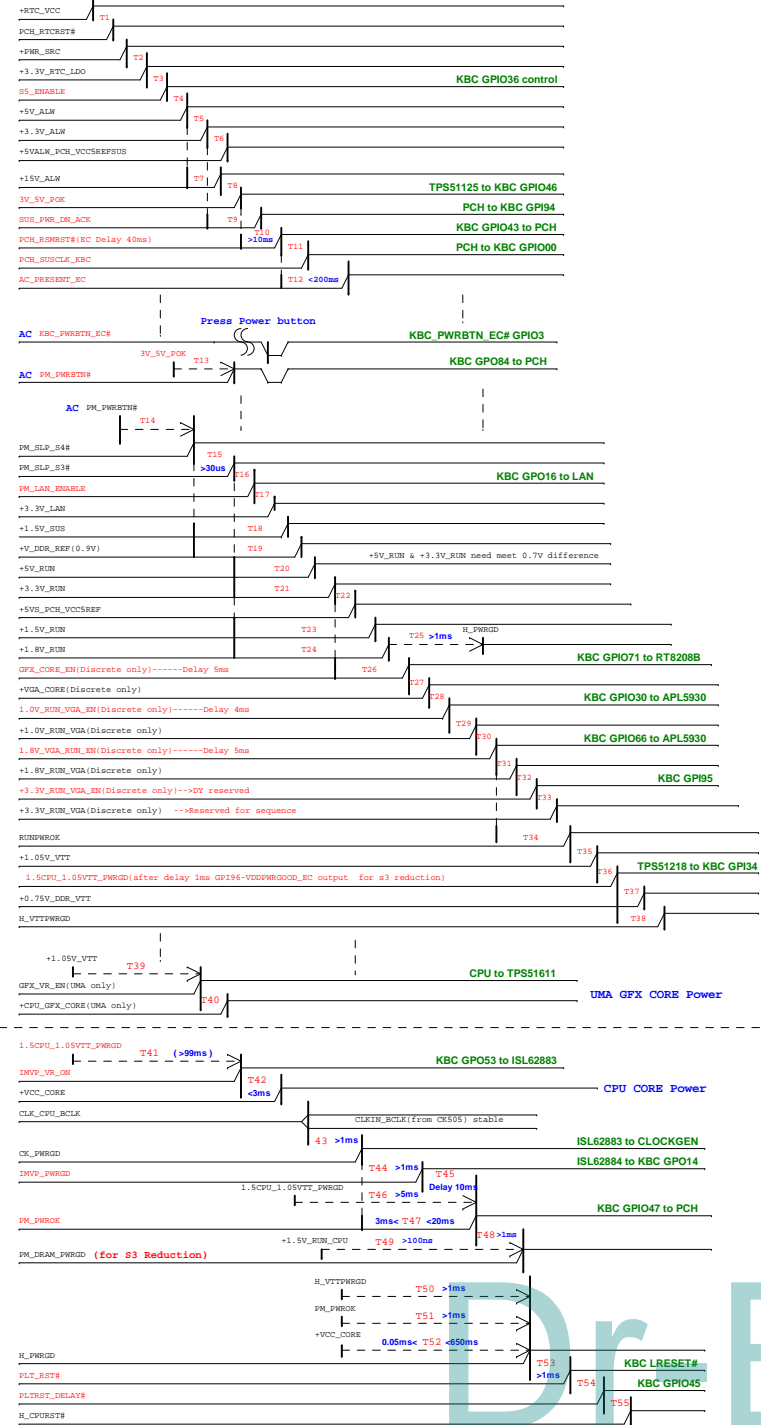
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DIS IVB Touch		
緯創資通		Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
Change History		
Size	Document Number	Rev
A3	Husk/Petra	-4M
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# Intel-Power Up Sequence

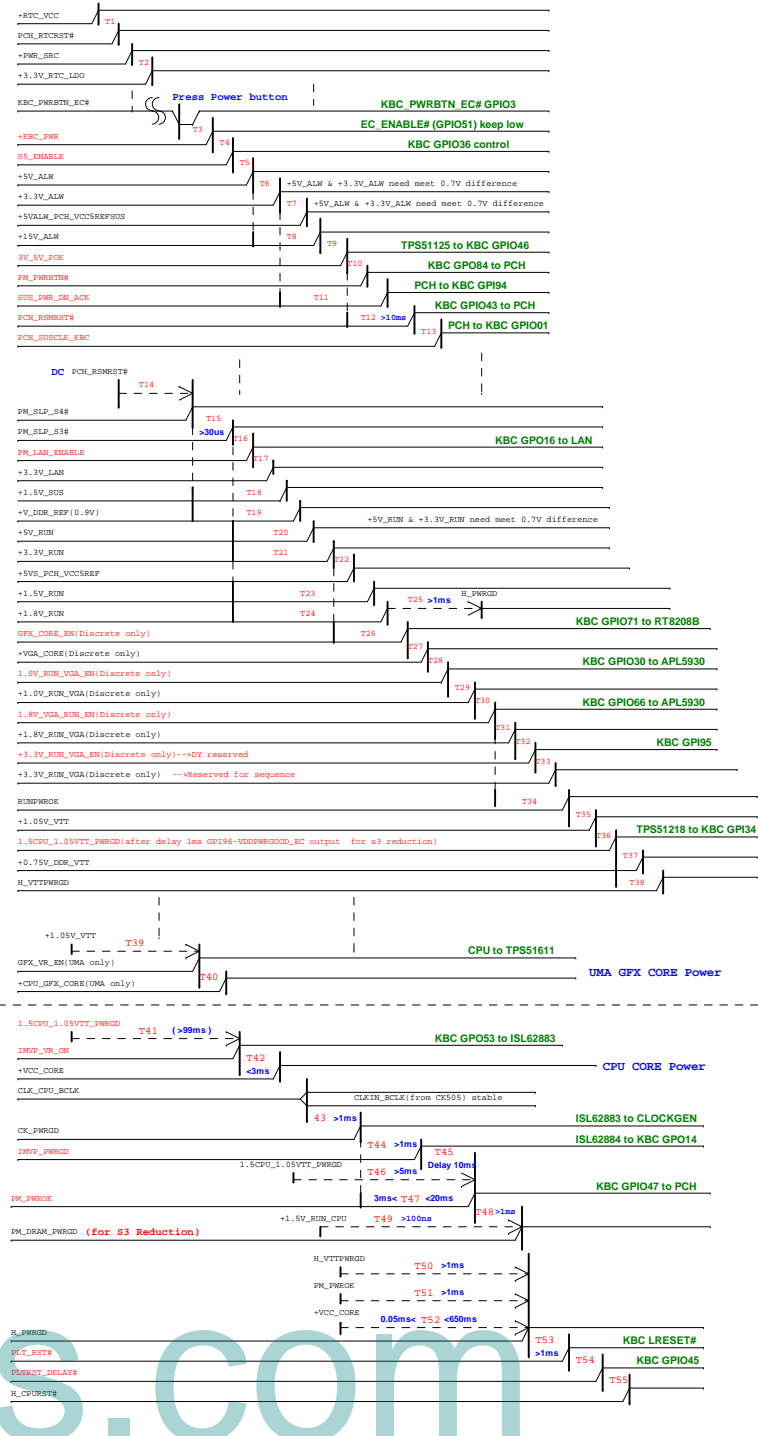
(AC mode)

red word: KBC GPIO

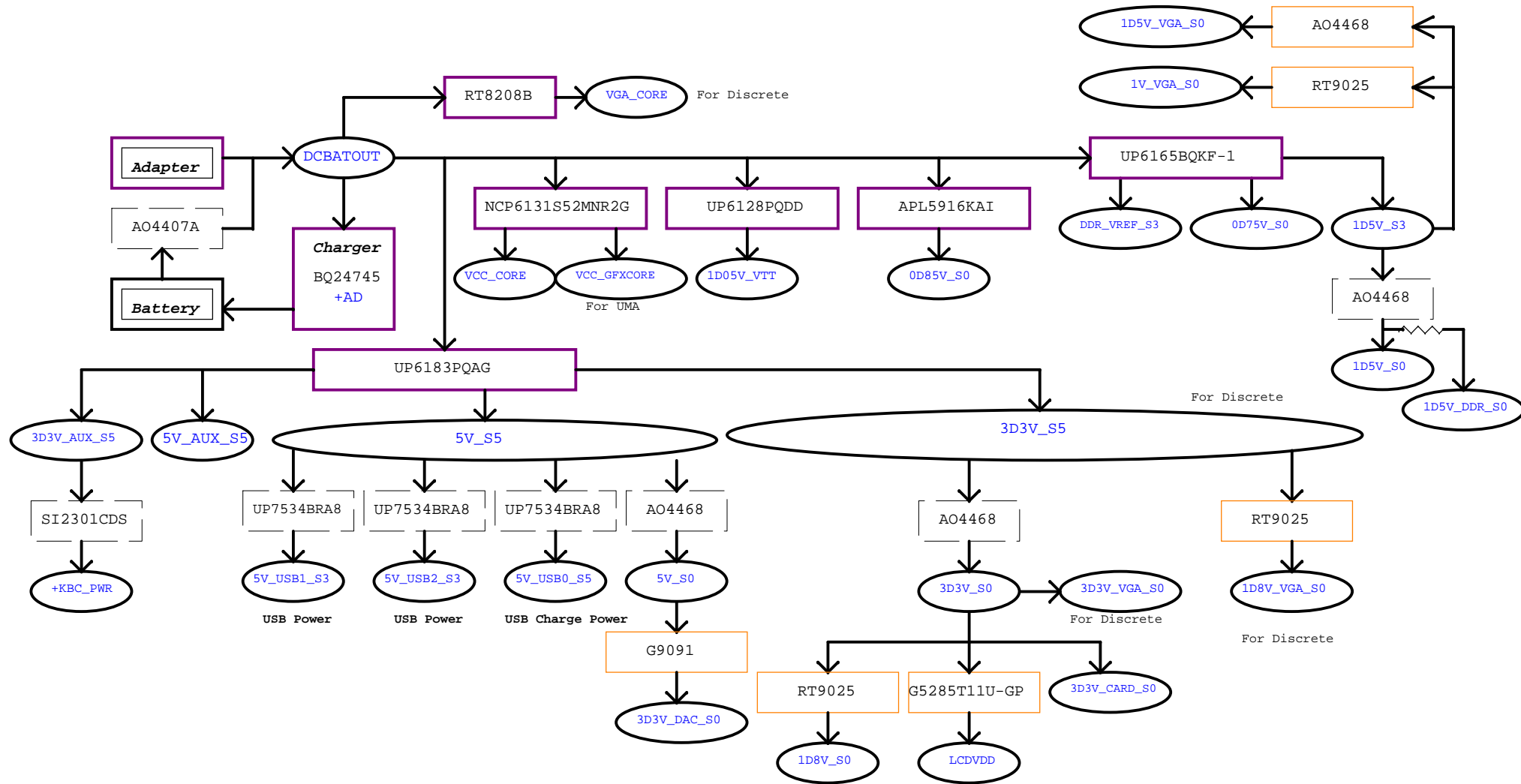


(DC mode)

red word: KBC GPIO

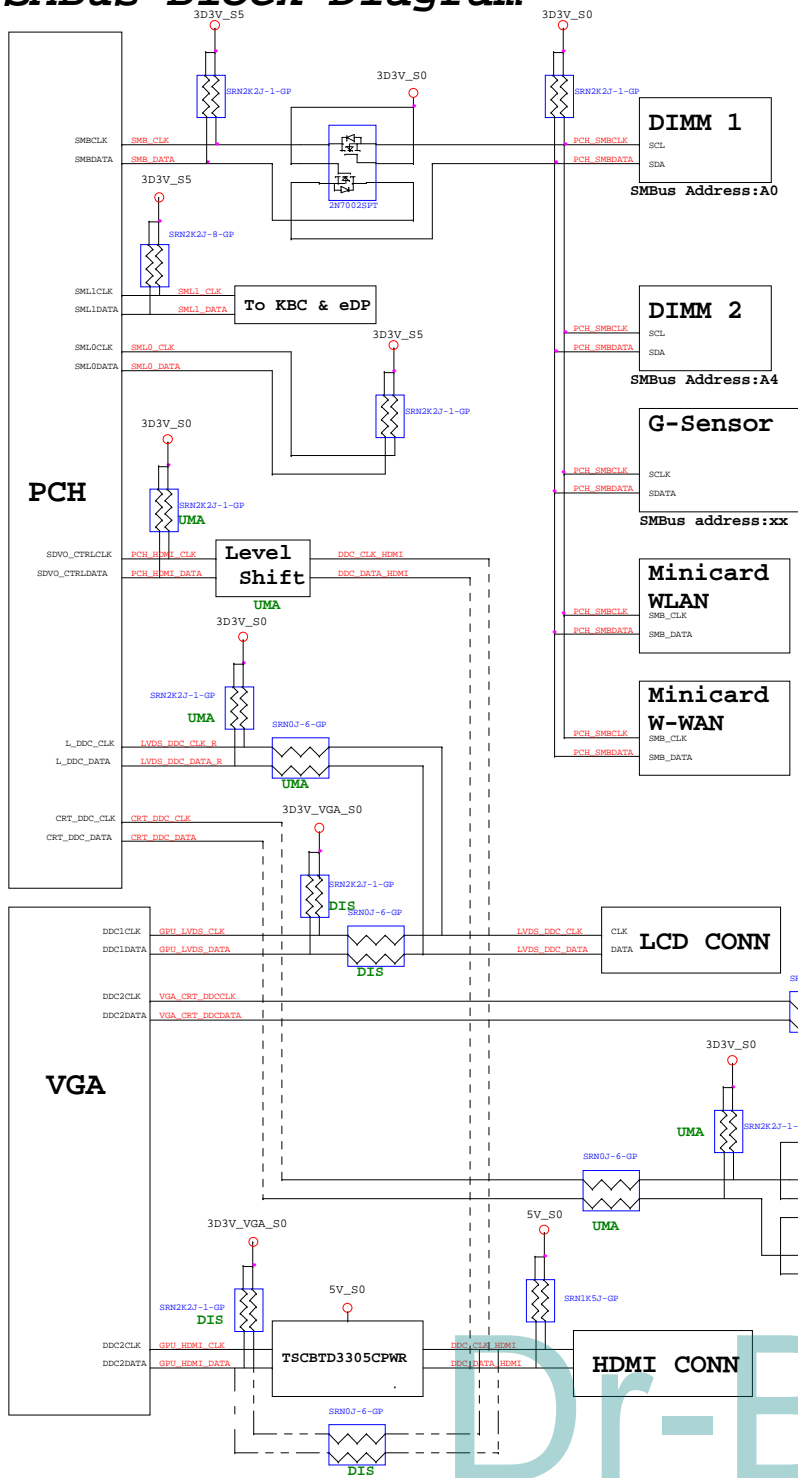


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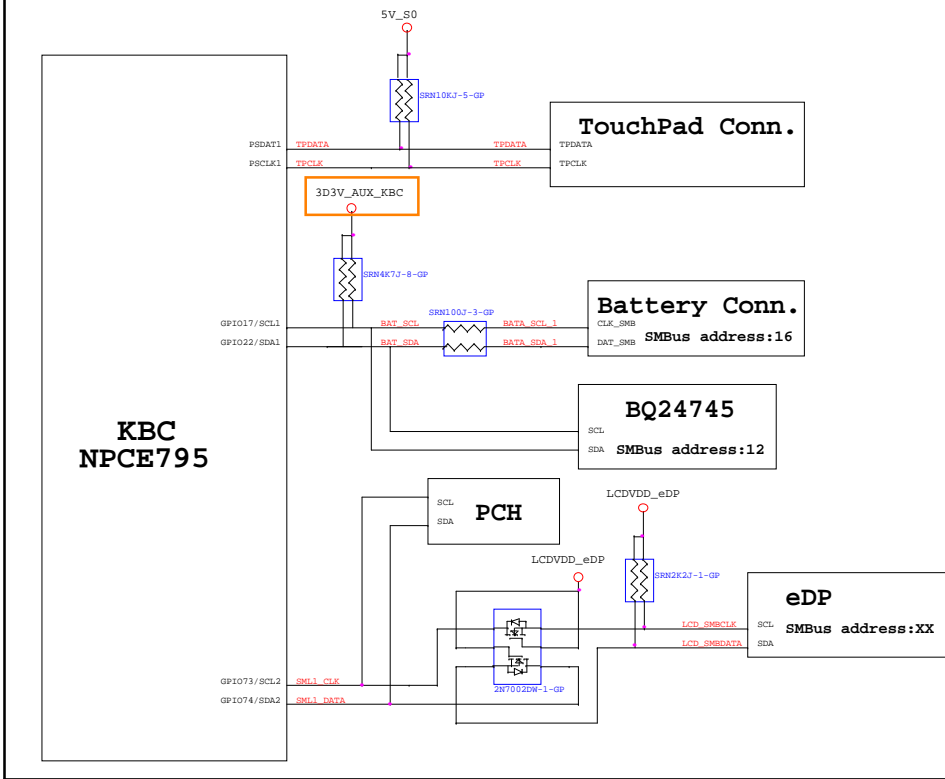


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# PCH SMBus Block Diagram

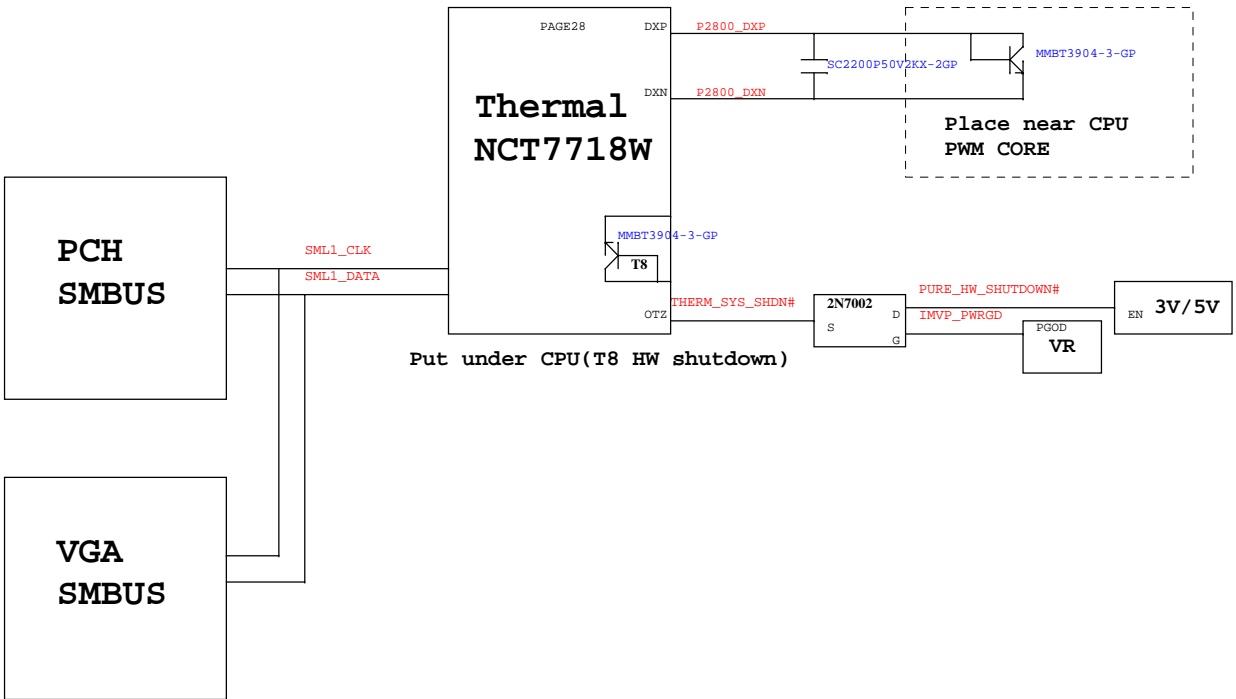


# KBC SMBus Block Diagram

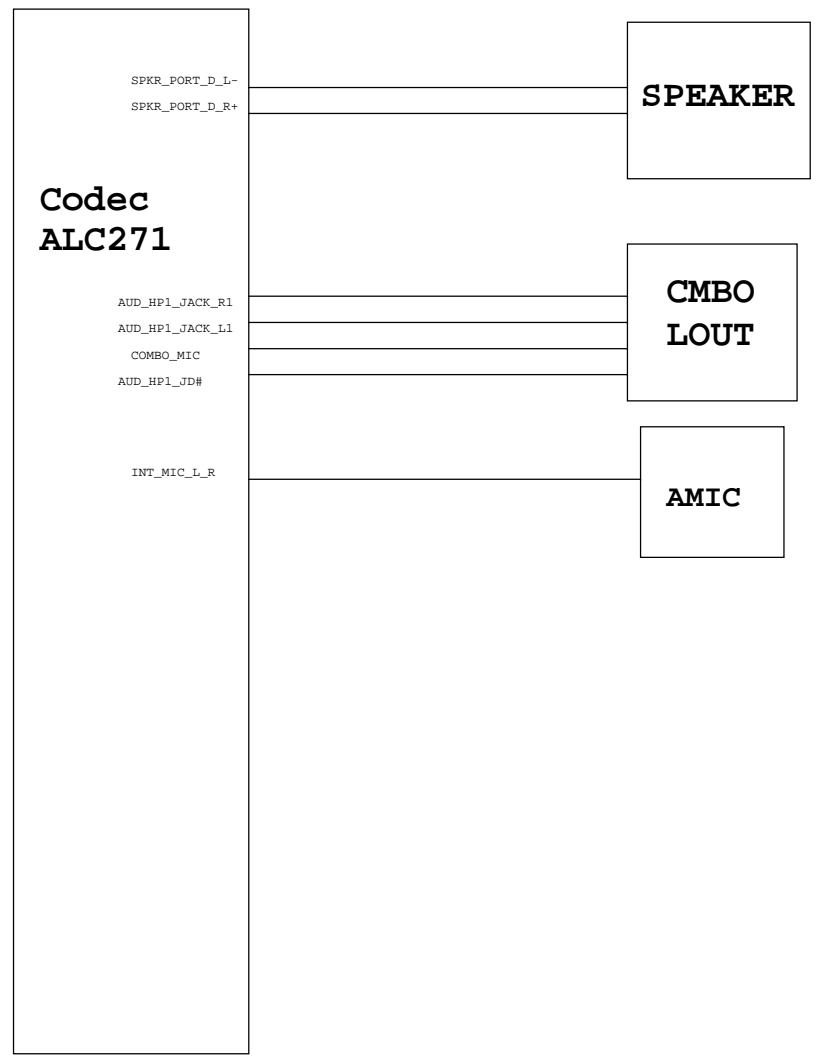


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# Thermal Block Diagram



# Audio Block Diagram



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