Husk/Petra
UMA/Muxless Schematics Document
Ivy Bridge
Intel PCH

DY :None Installed
DIS:DIS installed
DIS_Muxless :BOTH DIS or Muxless installed
DIS_PX:BOTH DIS or PX installed
DIS_PX_Muxless:DIS or PX or Muxless installed.
Muxless: Muxless installed.(PX4.0)
PX:MUX installed.(PX3.0)
PX_Muxless:BOTH PX or Muxless installed.
UMA:UMA installed
UMA_Muxless:BOTH UMA or Muxless installed
UMA_PX_Muxless:UMA or PX or Muxless installed

ANNIE: ONLY FOR ANNIE solution.
PSL: KBC795 PSL circuit for 10mW solution installed.
10mW: External circuit for 10mW solution installed.
65W: for 65W adaptor installed.
90W: for 90W adaptor installed.

IVB

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

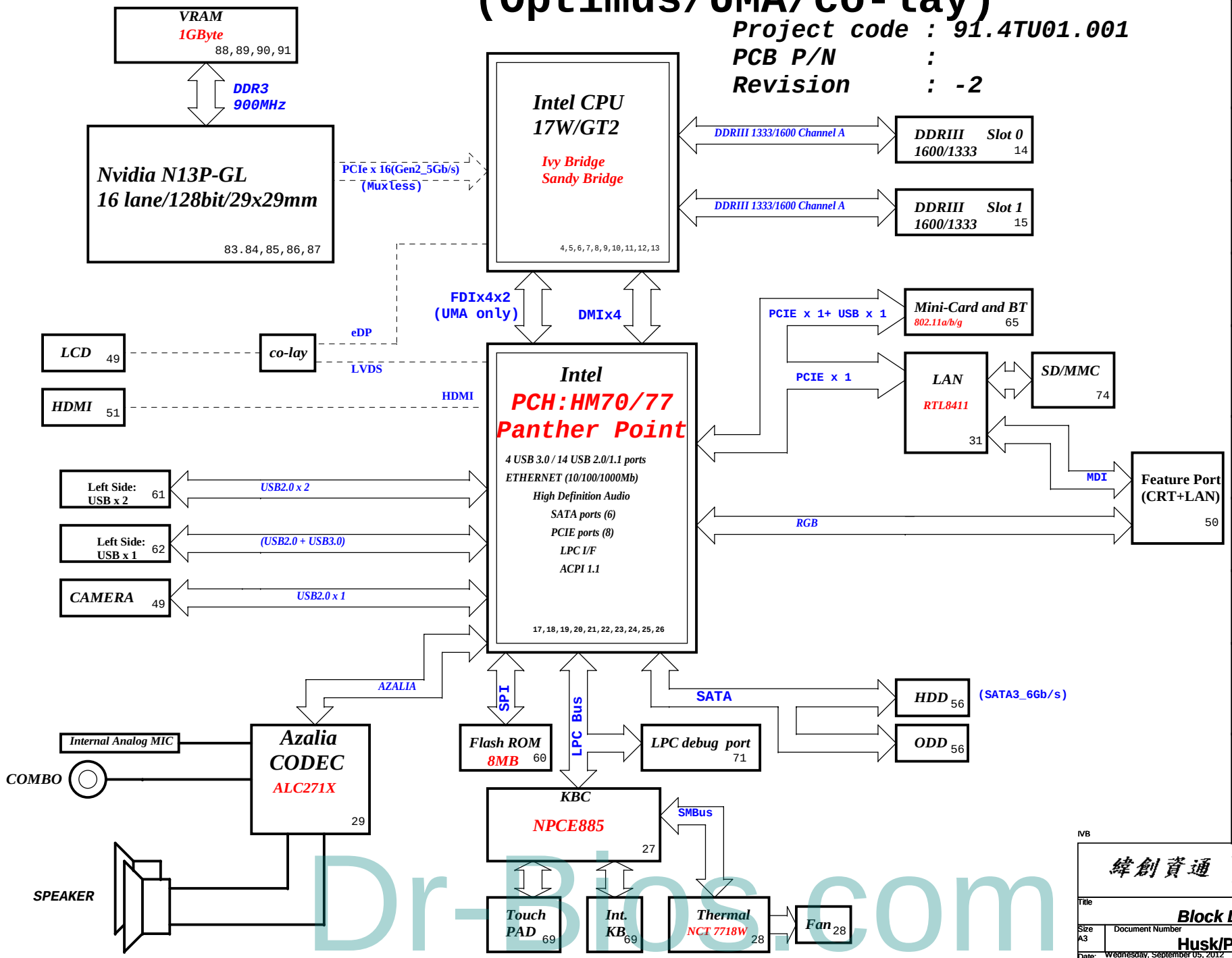
Title: Cover Page

Size: A3 | Document Number: Husk/Petra | Rev: -2

Date: Thursday, April 19, 2012 | Sheet 1 of 103

Husk and Petra Block Diagram (Optimus/UMA/co-lay)

Project code : 91.4TU01.001
PCB P/N :
Revision : -2



CHARGER BQ24727 40	
INPUTS	OUTPUTS
DCBATOUT	BT+

SYSTEM DC/DC RT8223MGQW 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

CPU DC/DC ISL95836HRTZ 42~43	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC ISL95836HRTZ 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE

SYSTEM DC/DC TPS51218DSCR 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC RT8207LGQW 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

LDO RT9025-25ZSP 47	
INPUTS	OUTPUTS
3D3V_S0	1D8V_S0

LDO G978 48	
INPUTS	OUTPUTS
1D05_VTT	0D85V_S0

VGA ISL62882CHRTZ 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

Switches 93	
INPUTS	OUTPUTS
3D3V_S0	3D3V_VGA_S0
1D05V_VTT	1D05V_VGA_S0
1D5V_S3	1D5V_VGA_S0

PCB LAYER

L1:Top L4:Signal
L2:VCC L5:GND
L3:Signal L6:Bottom

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Title: Block Diagram

Size	Document Number	Rev
A3	Husk/Petra	-2

Date: Wednesday, September 05, 2012 Sheet 2 of 103

PCH Strapping

Huron River Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Huron River Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	**1**
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	**0**
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	**11**
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	**1**

Voltage Rails

POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

PCIE Routing

LANE1	Mini Card2(WWAN)
LANE2	Mini Card1(WLAN)
LANE3	Card Reader
LANE4	Onboard LAN
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	New Card

SATA Table

SATA	
Pair	Device
0	HDD1
1	HDD2
2	N/A
3	N/A
4	ODD
5	ESATA

USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGER
9	USB Ext. port 2
10	EDP CAMERA
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

SMBus ADDRESSES

I² C / SMBus Addresses Device	Ref Des	HURON RIVER ORB Address	Hex	Bus
EC SMBus 1 Battery CHARGER				BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP				SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI				PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

VB

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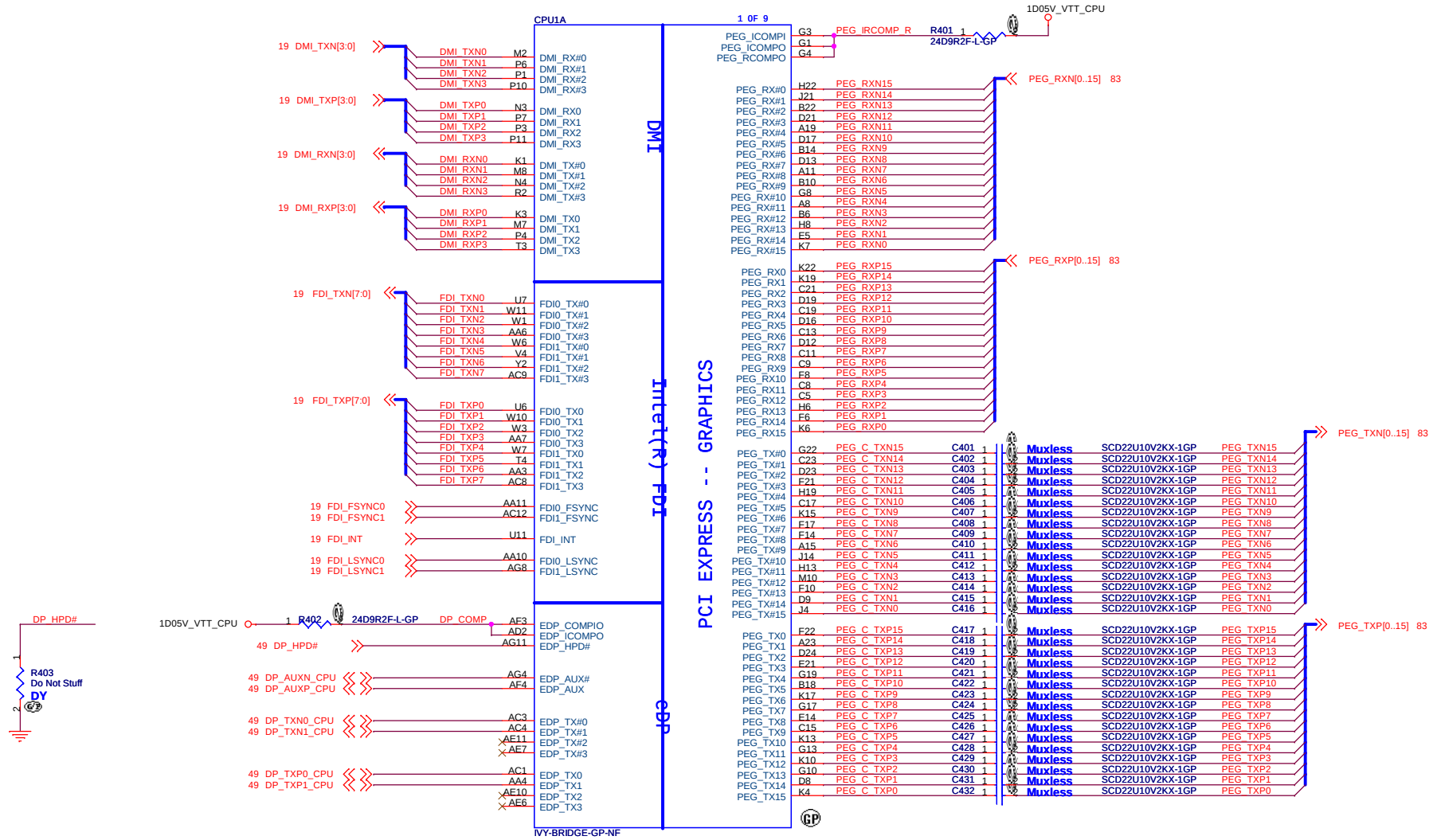
Title: Table of Content

Size: A3 | Document Number: Husk/Petra | Rev: -2

Date: Thursday, April 19, 2012 | Sheet 3 of 103

SSID = CPU



IVB

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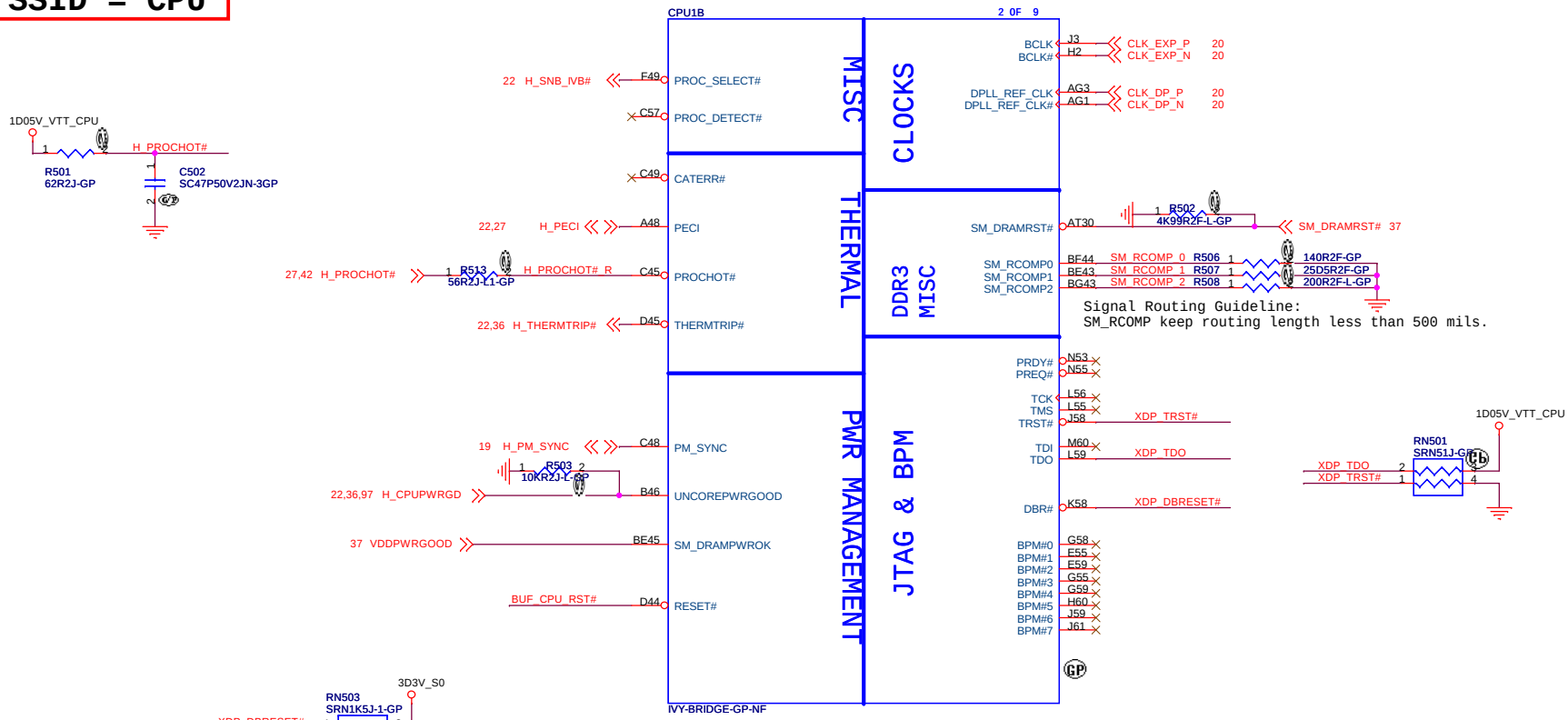
Title: CPU (PCIE/DMI/FDI)

Size: A3 | Document Number: Husk/Petra | Rev: -2

Date: Thursday, April 19, 2012 | Sheet 4 of 103

SSID = CPU



IVB

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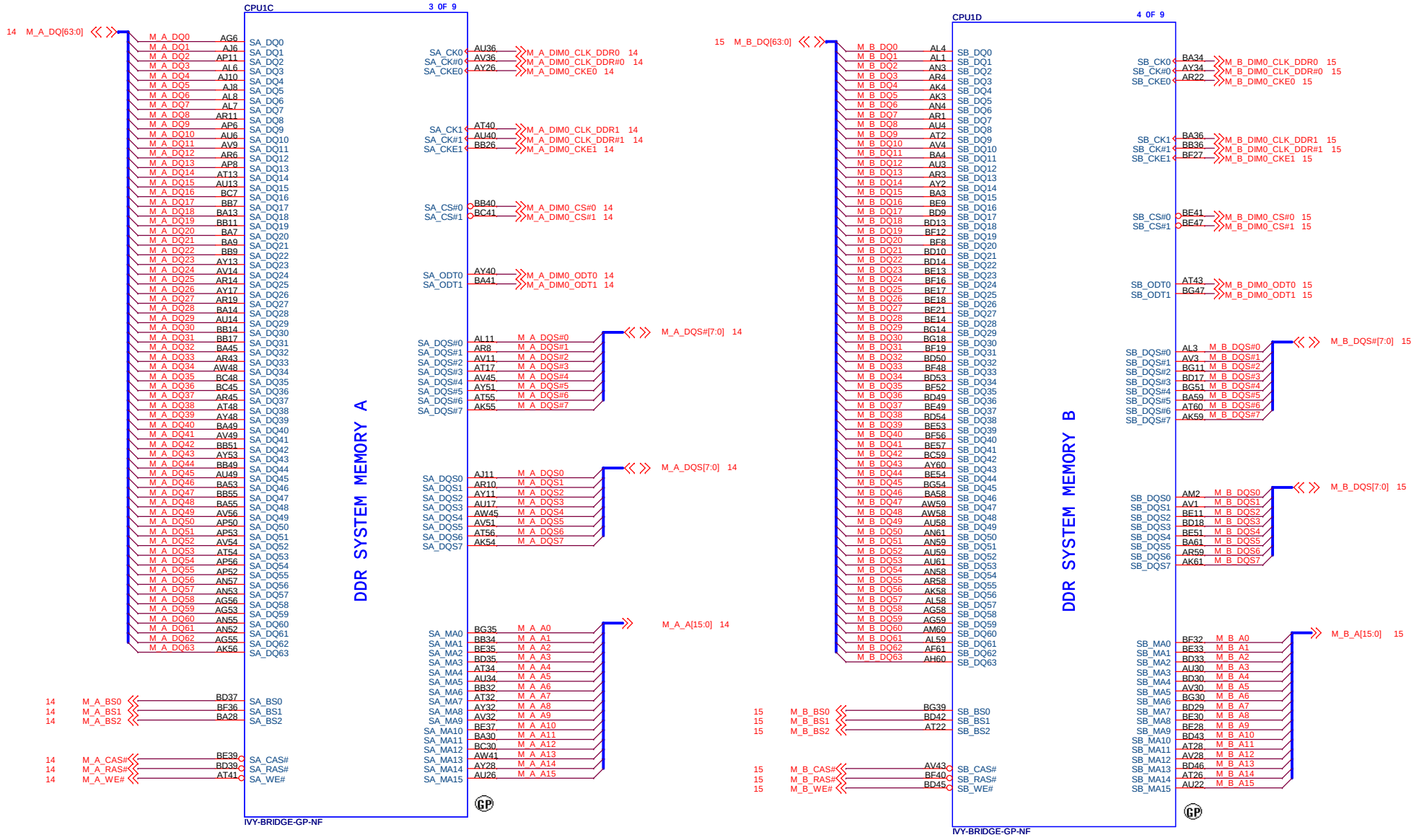
Title	***CPU (THERMAL/CLOCK/PM)***
Size: Custom	Document Number: **Husk/Petra** — Rev: **-2**
Date: Thursday, April 19, 2012	Sheet 5 of 103

SSID = CPU



IVB

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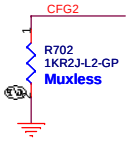
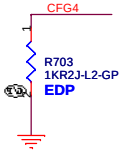
Title: CPU (DDR)		
Size: A3	Document Number: Husk/Petra	Rev: -2
Date: Thursday, April 19, 2012	Sheet 6 of 103	

SSID = CPU

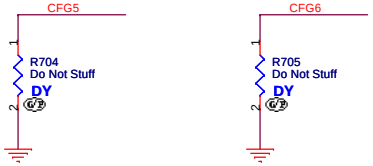
PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



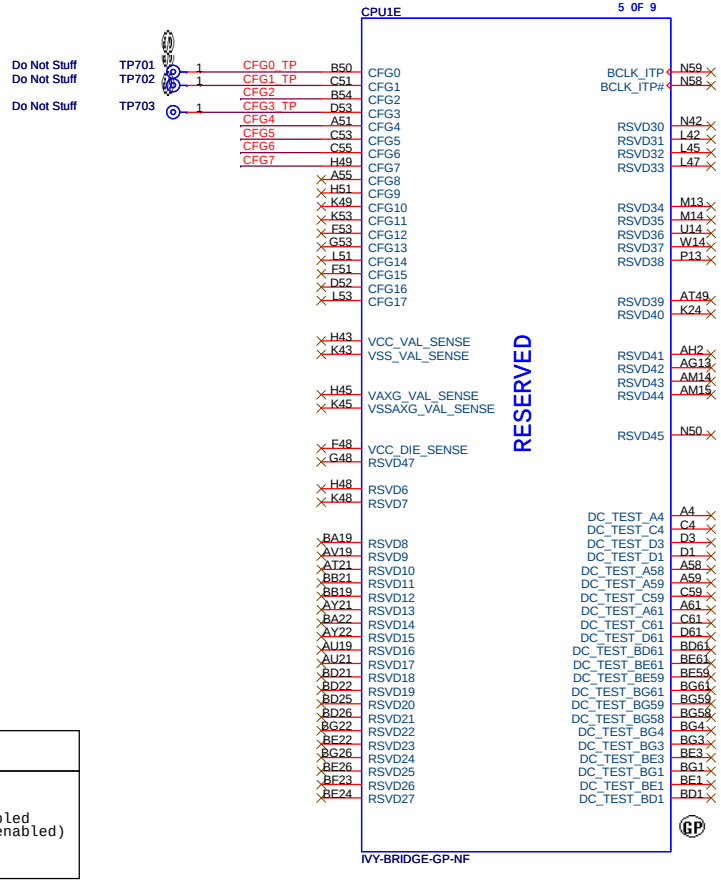
Enabl EDP function	
CFG4	1:Disable 0:Enable



PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



71.00IVY.A0U

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Title: ***CPU (RESERVED)***

Size	Document Number	Rev
A3	Husk/Petra	-2

Date: Thursday, April 19, 2012 Sheet 7 of 103

SSID = CPU

POWER

ULV:17W
Iccmax:33A
ICC_TDC:25A

Iccmax:8.5A
ICC_TDC:8.5A

CPU1F

6 OF 9

CORE SUPPLY

PEG IO AND DDR IO

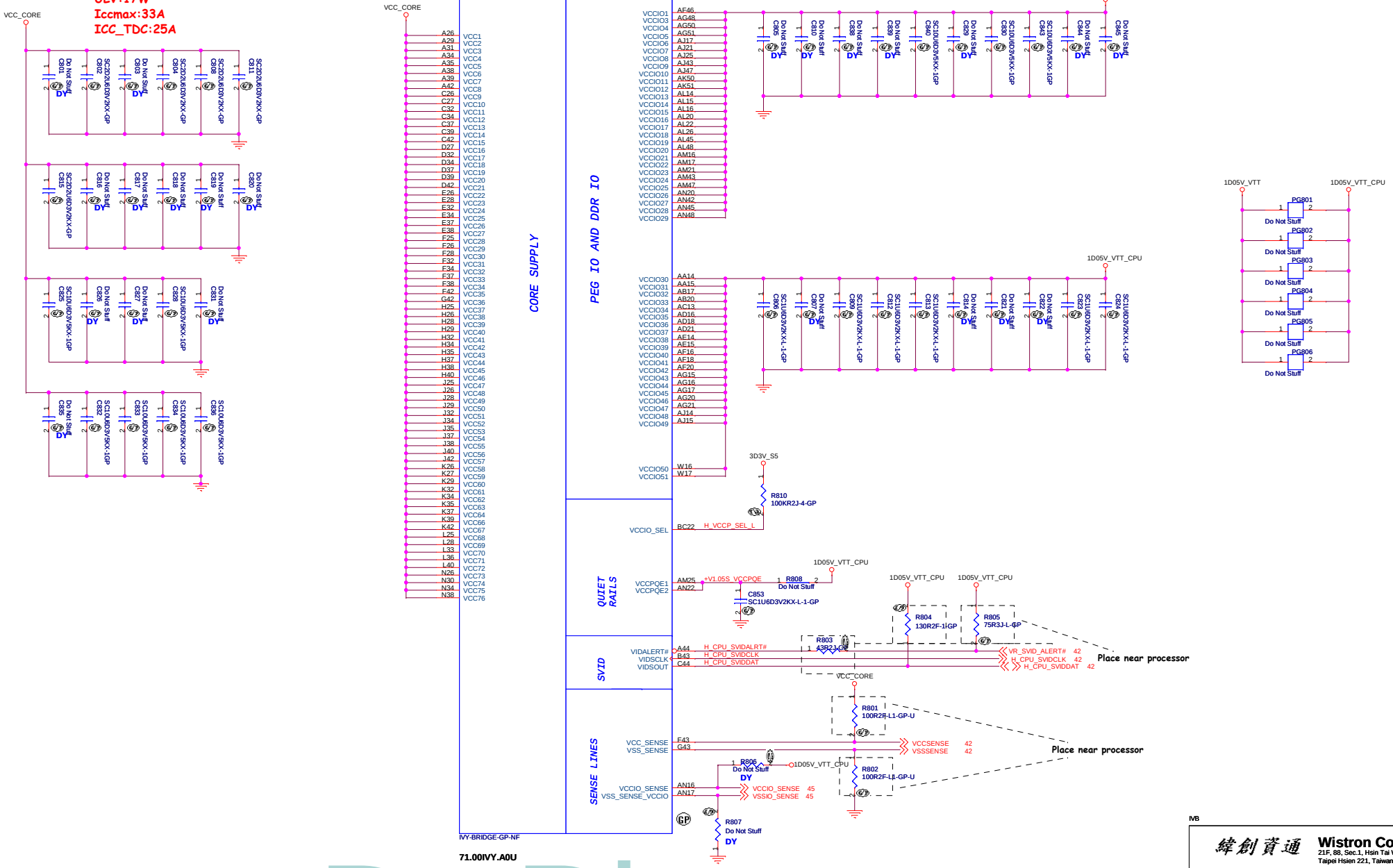
QUIET RAILS

SVID

SENSE LINES

IVY-BRIDGE-GP-NF

71.00IVY.A0U



IVB

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Title: **CPU (VCC_CORE)**

Size: Custom | Document Number: **Husk/Petra** | Rev: **-4M**

Date: Tuesday, October 09, 2012 | Sheet 8 of 103

SSID = CPU

POWER

Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT
should have 10 mils trace width.

Iccmax:18A(GT1)
ICC_TDC:12A(GT1)

VCC_GFXCORE

CPU1G — 7 OF 9

GRAPHICS: VAXG1, VAXG2, VAXG3, VAXG4, VAXG5, VAXG6, VAXG7, VAXG8, VAXG9, VAXG10, VAXG11, VAXG12, VAXG13, VAXG14, VAXG15, VAXG16, VAXG17, VAXG18, VAXG19, VAXG20, VAXG21, VAXG22, VAXG23, VAXG24, VAXG25, VAXG26, VAXG27, VAXG28, VAXG29, VAXG30, VAXG31, VAXG32, VAXG33, VAXG34, VAXG35, VAXG36, VAXG37, VAXG38, VAXG39, VAXG40, VAXG41, VAXG42, VAXG43, VAXG44, VAXG45, VAXG46, VAXG47, VAXG48, VAXG49, VAXG50, VAXG51, VAXG52, VAXG53, VAXG54, VAXG55, VAXG56

SENSE LINES: VAXG_SENSE, VSSAXG_SENSE

1.8V RAIL: VCCPLL1, VCCPLL2, VCCPLL3

SA RAIL: VCCSA1, VCCSA2, VCCSA3, VCCSA4, VCCSA5, VCCSA6, VCCSA7, VCCSA8, VCCSA9, VCCSA10, VCCSA11, VCCSA12, VCCSA13, VCCSA14, VCCSA15, VCCSA16

IVY-BRIDGE-GP-NF

71.00IVY.A0U

VREF: SM_VREF, SA_DIMM_VREFDQ, SB_DIMM_VREFDQ

DDR3 - 1.5V RAILS: VDDQ1–VDDQ26

QUIET RAILS: VCCDQ1, VCCDQ2

SENSE LINES: VDDQ_SENSE, VSS_SENSE_VDDQ, VCCSA_SENSE

VCCSA VID lines: VCCSA_VID0, VCCSA_VID1

SM_VREF — AY43 — +V_SM_VREF_CNT 37

SA_DIMM_VREFDQ — BE7 — M_VREF_DQ_DIMM0_C — M_VREF_DQ_DIMM0_C 37
SB_DIMM_VREFDQ — BG7 — M_VREF_DQ_DIMM1_C — M_VREF_DQ_DIMM1_C 37

BE7 and BG7 is NC ball in HR

RN902 Do Not Stuff DY

Iccmax:5A

1D5V_S0

PROCESSOR DDR 1.5V QUIET RAIL (BGA only)
+V1.5S_VCCD_Q should be short to +V1.5S_VCCDDQ on board

1D5V_S0 — +1.5S_VCCD_Q — R909 Do Not Stuff — C923 SC1U6D3V2KX-L-1-GP

R906 100R2F-L1-GP-U
R907 100R2F-L1-GP-U
R906,R907 close to CPU

VCC_AXG_SENSE
VSS_AXG_SENSE

42 VCC_AXG_SENSE — F45 VAXG_SENSE
42 VSS_AXG_SENSE — G45 VSSAXG_SENSE

1D8V_S0 — ICC_MAX:1.2A — C922 SC1U10V2KX-1GP

0D85V_S0 — ICC_MAX:6A — C915 SC10U6D3V5KX-1GP

BC43 TP_VDDQ_SENSE — TP901 Do Not Stuff
BA43 TP_VDDQ_VSS — TP902 Do Not Stuff

0D85V_S0 — R902 100R2F-L1-GP-U
R902 need be close to pin U10.

U10 VCCSA_SENSE

D48 VCCSA_VID0
D49 VCCSA_VID1

VCCSA_VID[0]	VCCSA_VID[1]	Selected VCCSA (XE & SV segments)	Selected VCCSA (ULV segment)
0	0	0.9 V	0.9 V
0	1	0.8 V	0.85 V
1	0	0.725 V	0.775 V
1	1	0.675 V	0.75 V

1D05V_VTT_CPU — R908 Do Not Stuff DY — R912 Do Not Stuff DY
VCCSA_VID0 — VCCSA_VID0 48
VCCSA_VID1 — VCCSA_VID1 48
R913 10KR2J-L-GP — R914 10KR2J-L-GP

IVB

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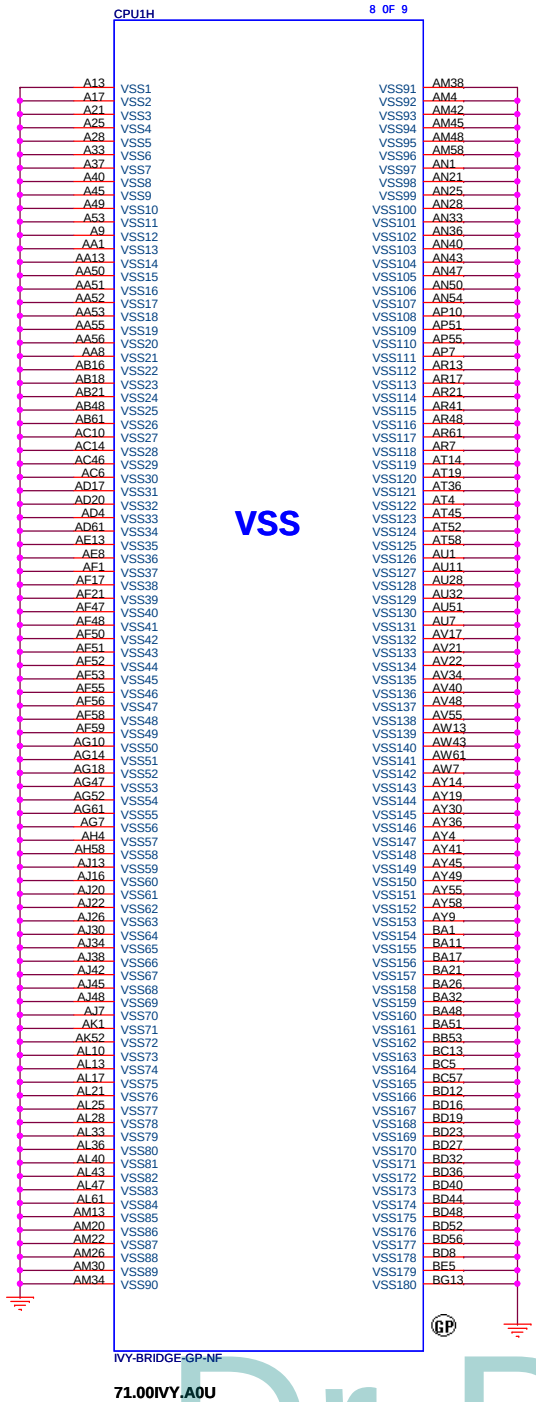
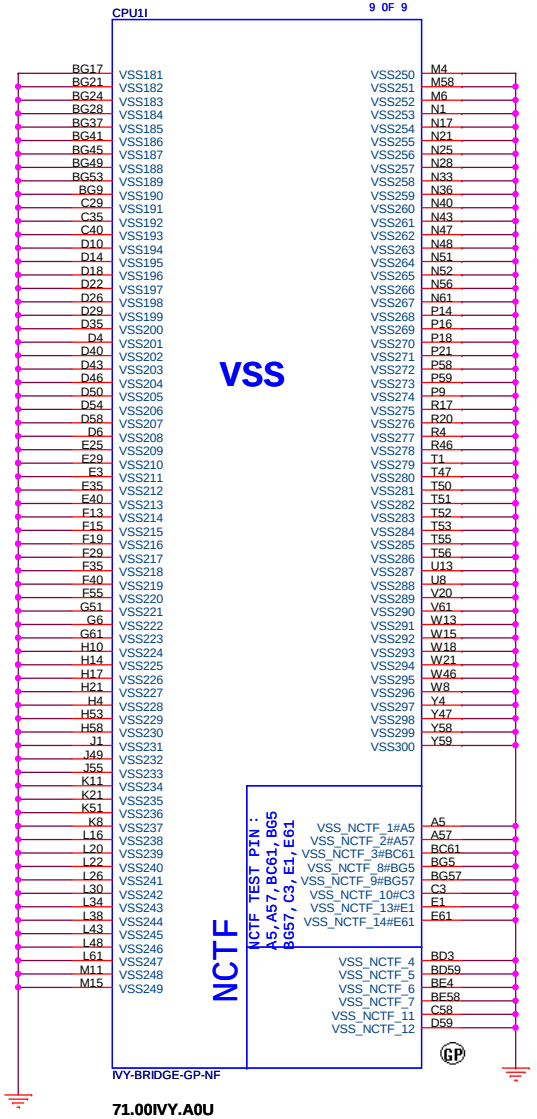
Title: CPU (VCC_GFXCORE)
Size: Custom | Document Number: Husk/Petra | Rev: -4M
Date: Tuesday, October 09, 2012 | Sheet 9 of 103

SSID = CPU



71.00IVY.A0U



71.00IVY.A0U

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Title: ***CPU (VSS)***

Size	Document Number	Rev
A3	Husk/Petra	-2

Date: Thursday, April 19, 2012 Sheet 10 of 103

IVB

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Title: ***XDP***

Size: A3 | Document Number: **Husk/Petra** | Rev: **-2**

Date: Thursday, April 19, 2012 | Sheet 11 of 103

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IVB

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Title: ***Reserved***

Size	Document Number	Rev
A4	Husk/Petra	-2

Date: Thursday, April 19, 2012 Sheet 12 of 103

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IVB

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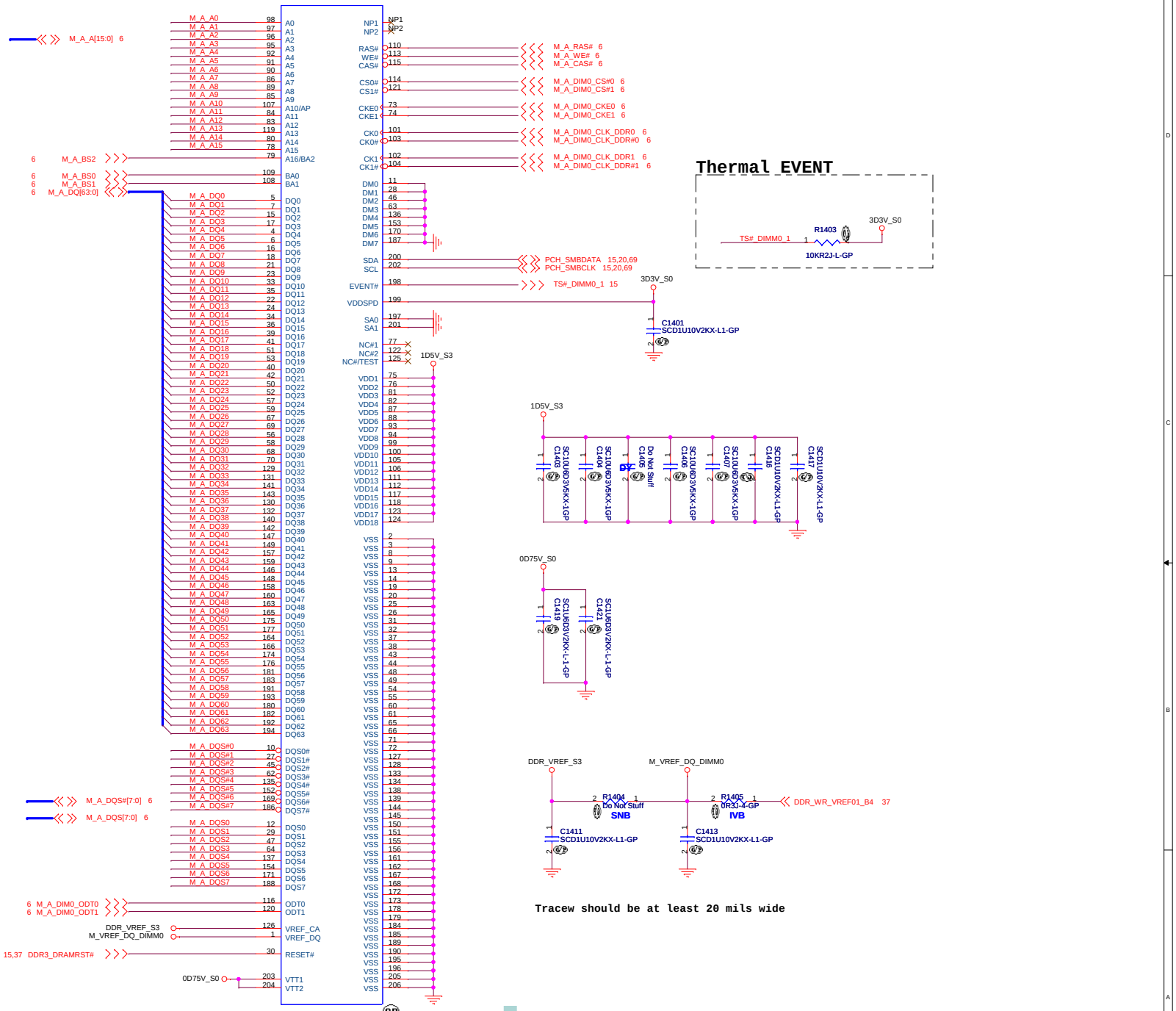
Title: ***Reserved***

Size	Document Number	Rev
A4	Husk/Petra	-2

Date: Thursday, April 19, 2012 Sheet 13 of 103

SSID = MEMORY



Thermal EVENT

C1401 SCD1U10V2KX-L1-GP

C1403 SC10U6D3V5KX-1GP
C1404 SC10U6D3V5KX-1GP
C1405 Do Not Stuff
C1406 SC10U6D3V5KX-1GP
C1407 SC10U6D3V5KX-1GP
C1416 SCD1U10V2KX-L1-GP
C1417 SCD1U10V2KX-L1-GP
DY

C1419 SC1U6D3V2KX-L1-GP
C1421 SC1U6D3V2KX-L1-GP

R1404 Do Not Stuff SNB
R1405 0R3J-4-GP IVB
C1411 SCD1U10V2KX-L1-GP
C1413 SCD1U10V2KX-L1-GP
DDR_WR_VREF01_B4 37

Tracew should be at least 20 mils wide

IVB

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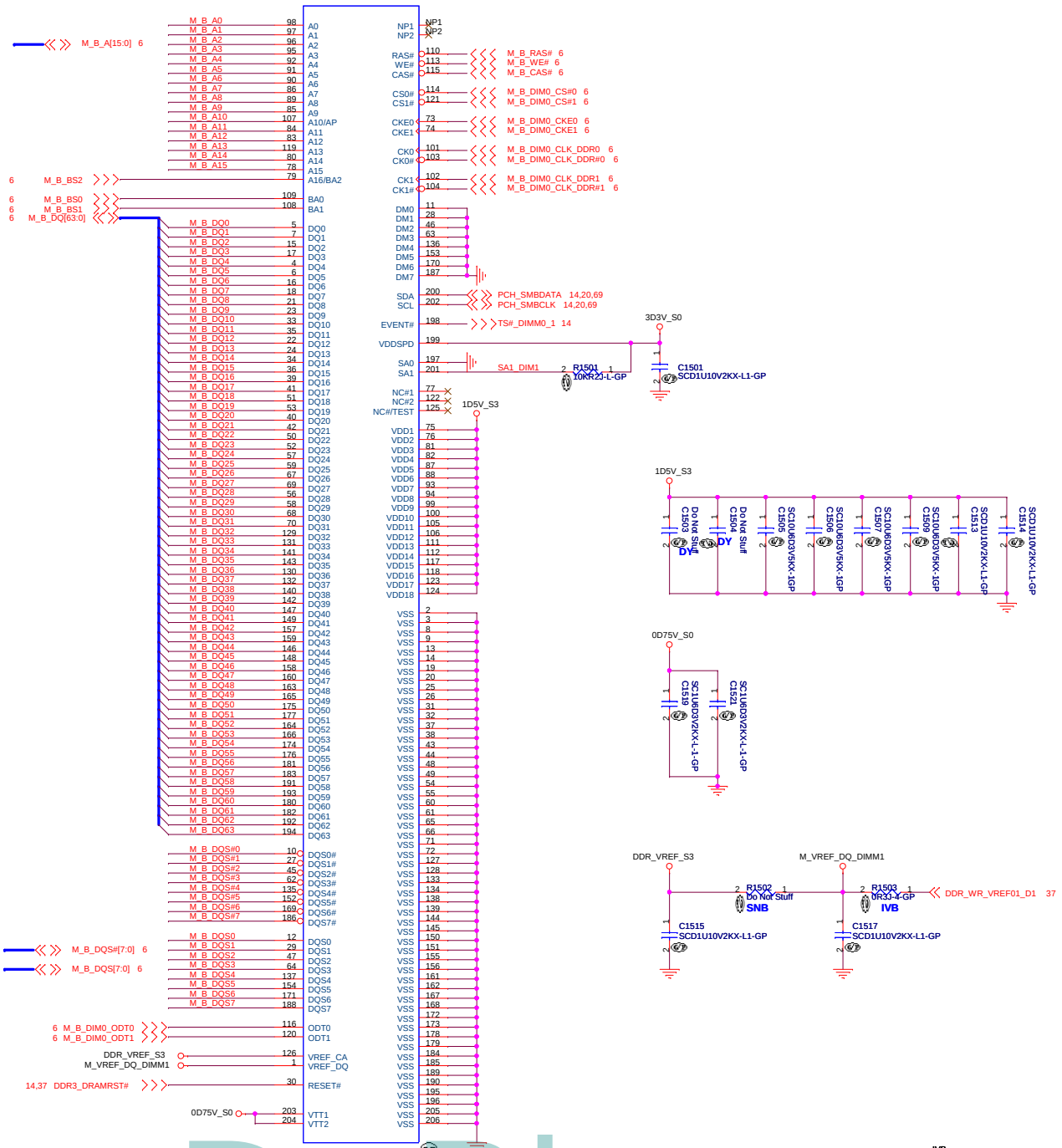
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: DDR3-SODIMM1	
Size: Custom	Document Number: Husk/Petra
Rev: -2	
Date: Thursday, April 19, 2012	Sheet 14 of 103

SSID = MEMORY



IVB

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Title: ***DDR3-SODIMM2***

Size: Custom | Document Number: **Husk/Petra** | Rev: **-2**

Date: Thursday, April 19, 2012 | Sheet 15 of 102

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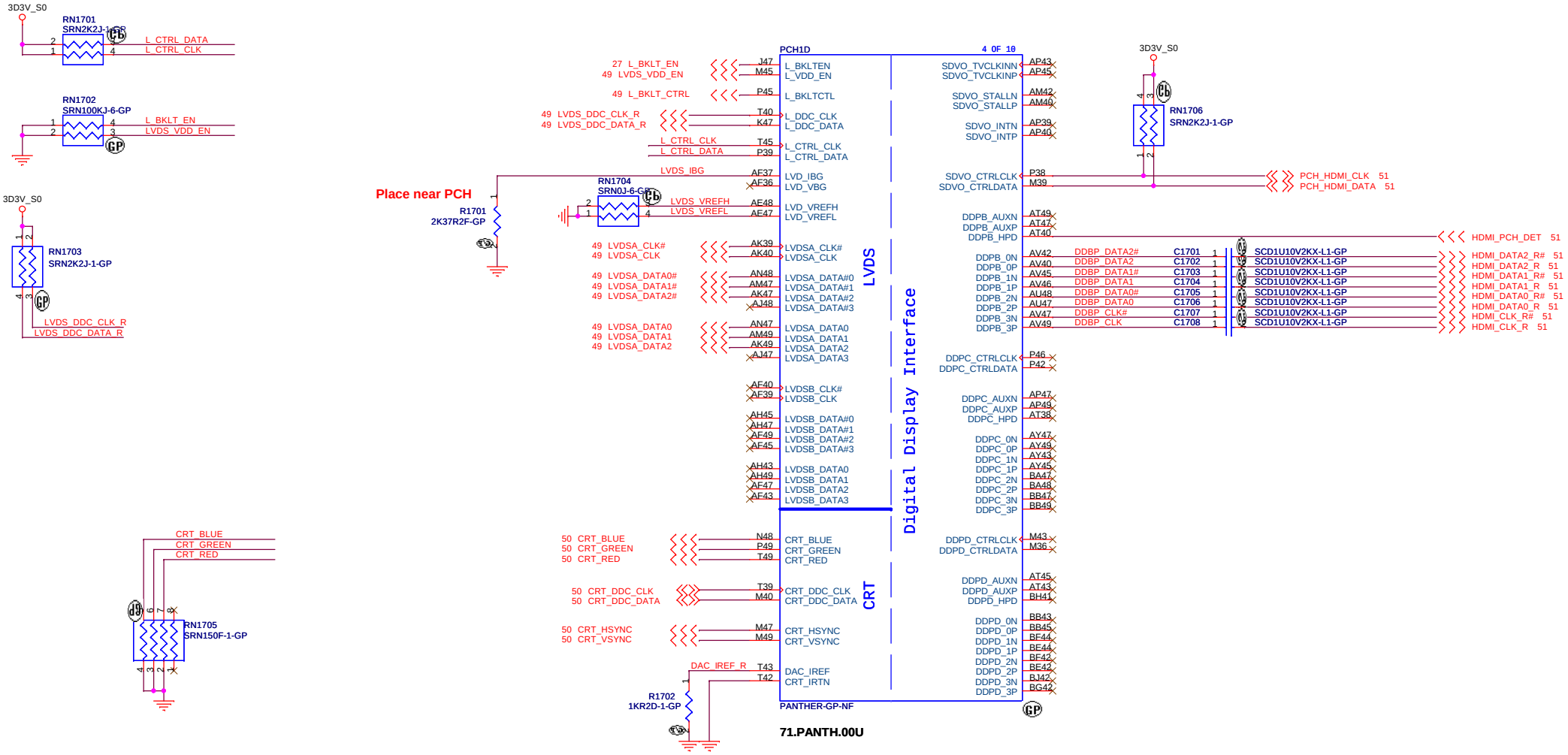
Title: ***DDR3-SODIMM2***

Size	Document Number	Rev
A4	**Husk/Petra**	**-2**

Date: Thursday, April 19, 2012 Sheet 16 of 103



IVB

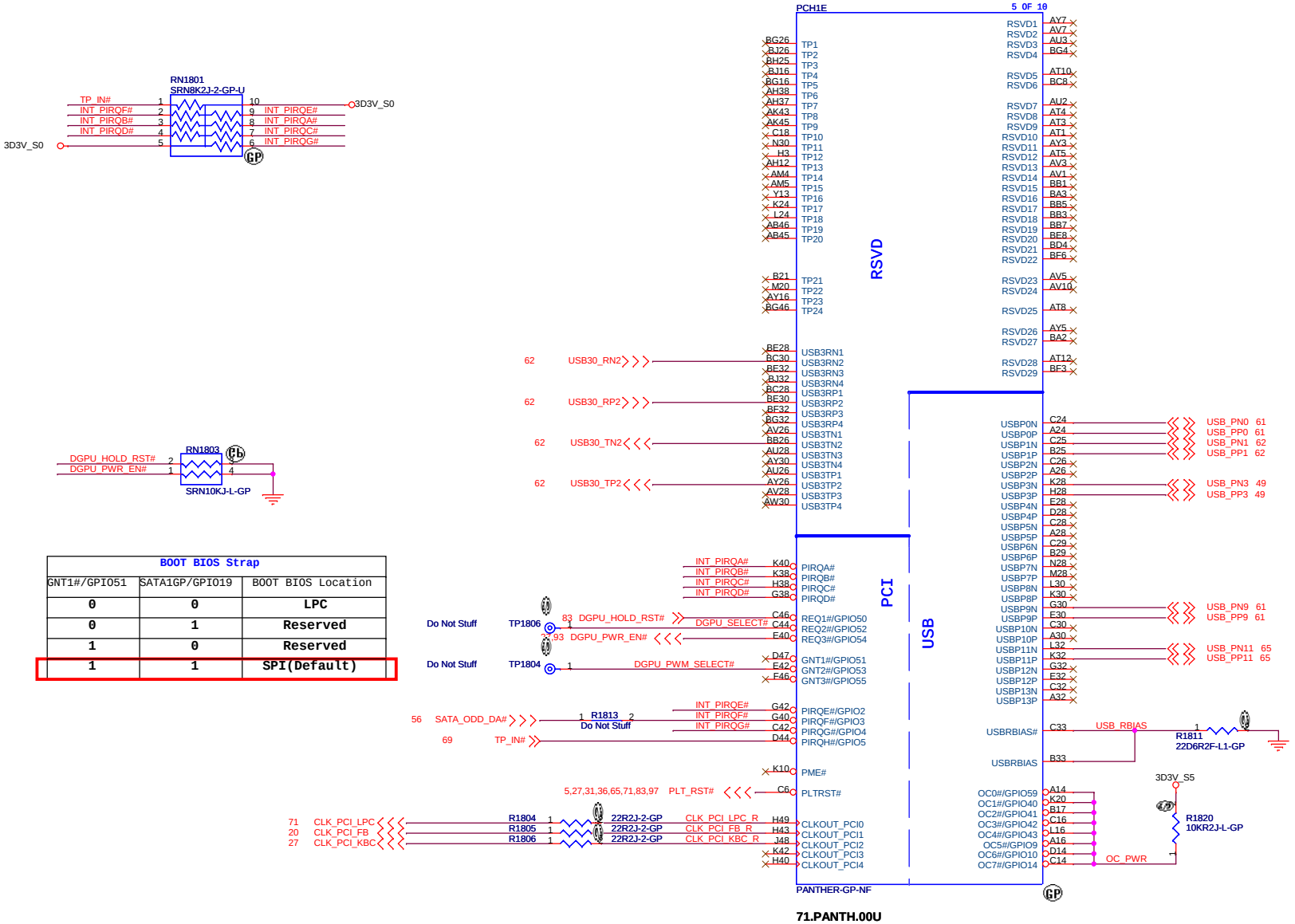
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (LVDS/CRT/DDI)**

Size	Document Number	Rev
A3	Husk/Petra	-2

Date: Thursday, April 19, 2012 Sheet 17 of 103

SSID = PCH



BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

USB Table

Pair	Device
0	USB2.0 Ext. port 1
1	USB3.0/USB2.0 Ext. port 2
2	
3	CCD
4	
5	
6	may not be available
7	may not be available
8	
9	USB2.0 Ext. port 3
10	
11	Mini Card1 (WLAN+BT)
12	
13	

IVB

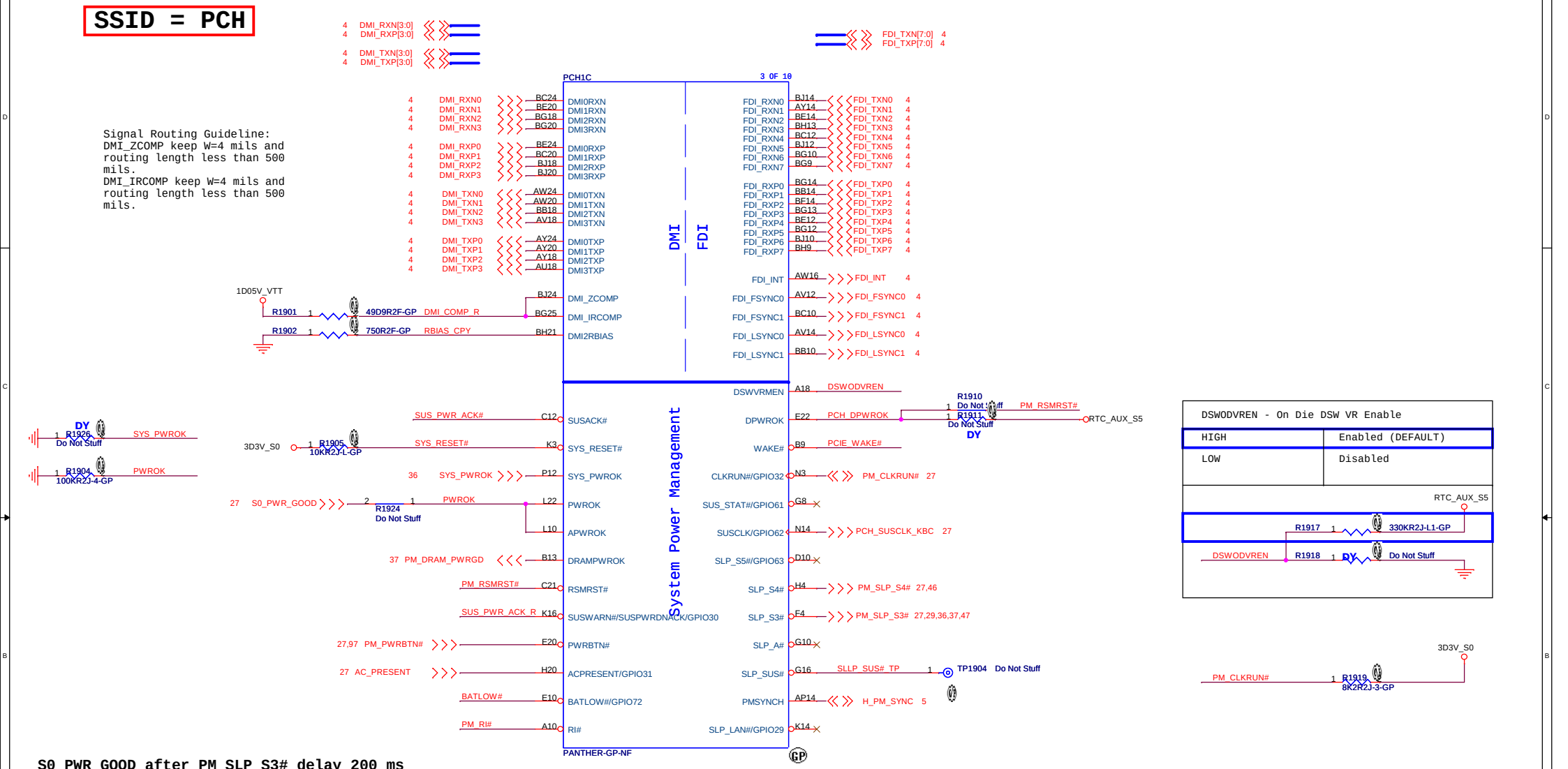
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI/USB/NVRAM)

Size: Custom | Document Number: Husk/Petra | Rev: -2

Date: Thursday, October 11, 2012 | Sheet 18 of 103

SSID = PCH



IVB

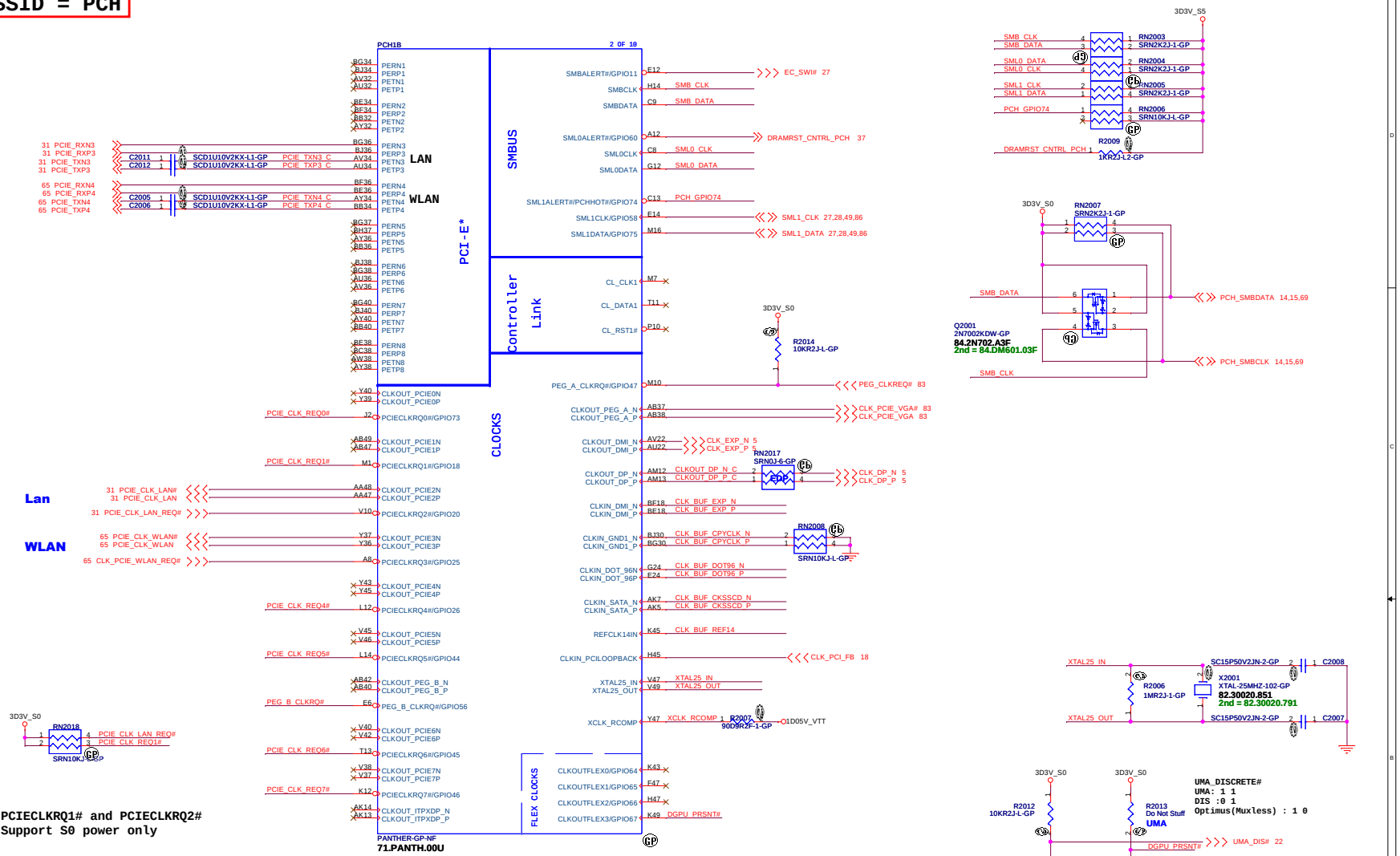
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (DM I/FDI/PM)

Size	Document Number	Rev
A3	Husk/Petra	-2

Date: Tuesday, October 09, 2012 Sheet 19 of 103

SSID = PCH



IVB

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI-E/SMBUS/CLOCK/CL)

Size: Custom | Document Number: Husk/Petra | Rev: -2

Date: Tuesday, October 09, 2012 | Sheet 20 of 103

SSID = PCH

RTC_AUX_S5

R2115 20KR2F-L-GP
R2116 20KR2F-L-GP
C2103 SC1U16V3KX-5GP

INTVRMEN- Integrated SUS 1.05V VRM Enable
High - Enable internal VRs
Low - Enable external VRs

RTC_X1 RTC_X2
R2101 10MR2J-L-GP
X2101 X-32D768KHZ-34GPU
82.30001.661
2nd = 82.30001.B21
C2101 SC6P50V2CN-1GP
C2102 SC6P50V2CN-1GP

C2104 SC1U16V3KX-5GP
G2101 Do Not Stuff
R2104 1MR2J-L-GP
R2105 330KR2F-L-GP
RTC_AUX_S5

RTC Reset

27 RTCRST_ON
Q2102 2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031
RTC_RST#
R2106 100KR2F-L1-GP
R2111 2KR2F-3-GP

PCH1A 1 OF 10

RTC_X1 A20 RTCX1
RTC_X2 C20 RTCX2
RTC_RST# D20 RTCRST#
SRTC_RST# G22 SRTCRST#
SM_INTRUDER# K22 INTRUDER#
PCH_INTVRMEN C17 INTVRMEN
RTC

LPC
FWH0/LAD0 C38 LPC_AD0
FWH1/LAD1 A38 LPC_AD1
FWH2/LAD2 B37 LPC_AD2
FWH3/LAD3 C37 LPC_AD3
LPC_AD[0..3] 27,71
FWH4/LFRAME# D36 LPC_FRAME# 27,71
LDRQ0# E36
LDRQ1#/GPIO23 K36
SERIRQ V5 INT_SERIRQ 27

HDA_BITCLK N34 HDA_BCLK
HDA_SYNC L34 HDA_SYNC
29 HDA_SPKR T10 SPKR
HDA_RST# K34 HDA_RST#
29 HDA_SDIN0 E34 HDA_SDIN0
G34 HDA_SDIN1
C34 HDA_SDIN2
A34 HDA_SDIN3
27 ME_UNLOCK R2107 1KR2J-L2-GP
HDA_SDOUT A36 HDA_SDO
C36 HDA_DOCK_EN#/GPIO33
N32 HDA_DOCK_RST#/GPIO13
IHDA

SATA 6G
SATA0RXN AM3
SATA0RXP AM1
SATA0TXN AP7
SATA0TXP AP5
SATA_RXN0 56
SATA_RXP0 56
SATA_TXN0 56
SATA_TXP0 56
HDD1
SATA1RXN AM10
SATA1RXP AM8
SATA1TXN AP11
SATA1TXP AP10
SATA2RXN AD7
SATA2RXP AD5
SATA2TXN AH5
SATA2TXP AH4
SATA3RXN AB8
SATA3RXP AB10
SATA3TXN AF3
SATA3TXP AF1
SATA4RXN Y7
SATA4RXP Y5
SATA4TXN AD3
SATA4TXP AD1
SATA_RXN4 56
SATA_RXP4 56
SATA_TXN4 56
SATA_TXP4 56
ODD
SATA5RXN Y3
SATA5RXP Y1
SATA5TXN AB3
SATA5TXP AB1
SATA

R2121 4K7R2J-L-GP
PCH_JTAG_TCK_BUF J3 JTAG_TCK
H7 JTAG_TMS
K5 JTAG_TDI
H1 JTAG_TDO
JTAG

SATAICOMPO Y11
SATAICOMPI Y10
SATA_COMP R2112 37D4R2F-GP
1D05V_VTT
SATA3RCOMPO AB12
SATA3COMPI AB13
SATA3_COMP R2113 49D9R2F-GP
1D05V_VTT
SATA3RBIAS AH1
RBIAS_SATA3 R2114 750R2F-GP

27,60 SPI_CLK_R R2108 33R2J-L1-GP
PCH_SPI_CLK T3 SPI_CLK
27,60 SPI_CS0#_R R2109 33R2J-L1-GP
PCH_SPI_CS0# Y14 SPI_CS0#
T1 SPI_CS1#
27,60 SPI_SI_R R2110 33R2J-L1-GP
PCH_SPI_SI V4 SPI_MOSI
27,60 SPI_SO_R U3 SPI_MISO
SPI

SATALED# P3 SATA_LED#
SATA0GP/GPIO21 V14 SATA_DET#0
SATA1GP/GPIO19 P1

PANTHER-GP-NF

71.PANTH.00U

29 HDA_CODEC_SYNC R2122 DY 1 Do Not Stuff HDA_SYNC
29 HDA_CODEC_SDOUT R2123 33R2J-L1-GP HDA_SDOUT
29 HDA_CODEC_RST# HDA_RST#
29 HDA_CODEC_BITCLK HDA_BITCLK
RN2102 SRN33J-5-GP-U

Flash Descriptor Security Overide	
HDA_SDOUT	Low = Default High = Enable

+3VS_+1.5VS_HDA_IO
R2102 Do Not Stuff DY HDA_SDOUT

PLL ODVR VOLTAGE	
HDA_SYNC	Low = 1.8V (Default) High = 1.5V

+3VS_+1.5VS_HDA_IO
R2103 1KR2J-L2-GP HDA_SYNC

5V_S0
HDA_CODEC_SYNC
Q2101 2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031
3rd = 84.2N702.W31
HDA_SYNC_R
R2124 33R2J-L1-GP HDA_SYNC

HDA_CODEC_BITCLK EC2102 Do Not Stuff DY
HDA_CODEC_SDOUT EC2103 Do Not Stuff DY
SPI_CS0#_R EC2101 Do Not Stuff DY

3D3V_S0
RN2103 SRN10KJ-6-GP
22 PSW_CLR#
SATA_LED#
INT_SERIRQ
SATA_DET#0

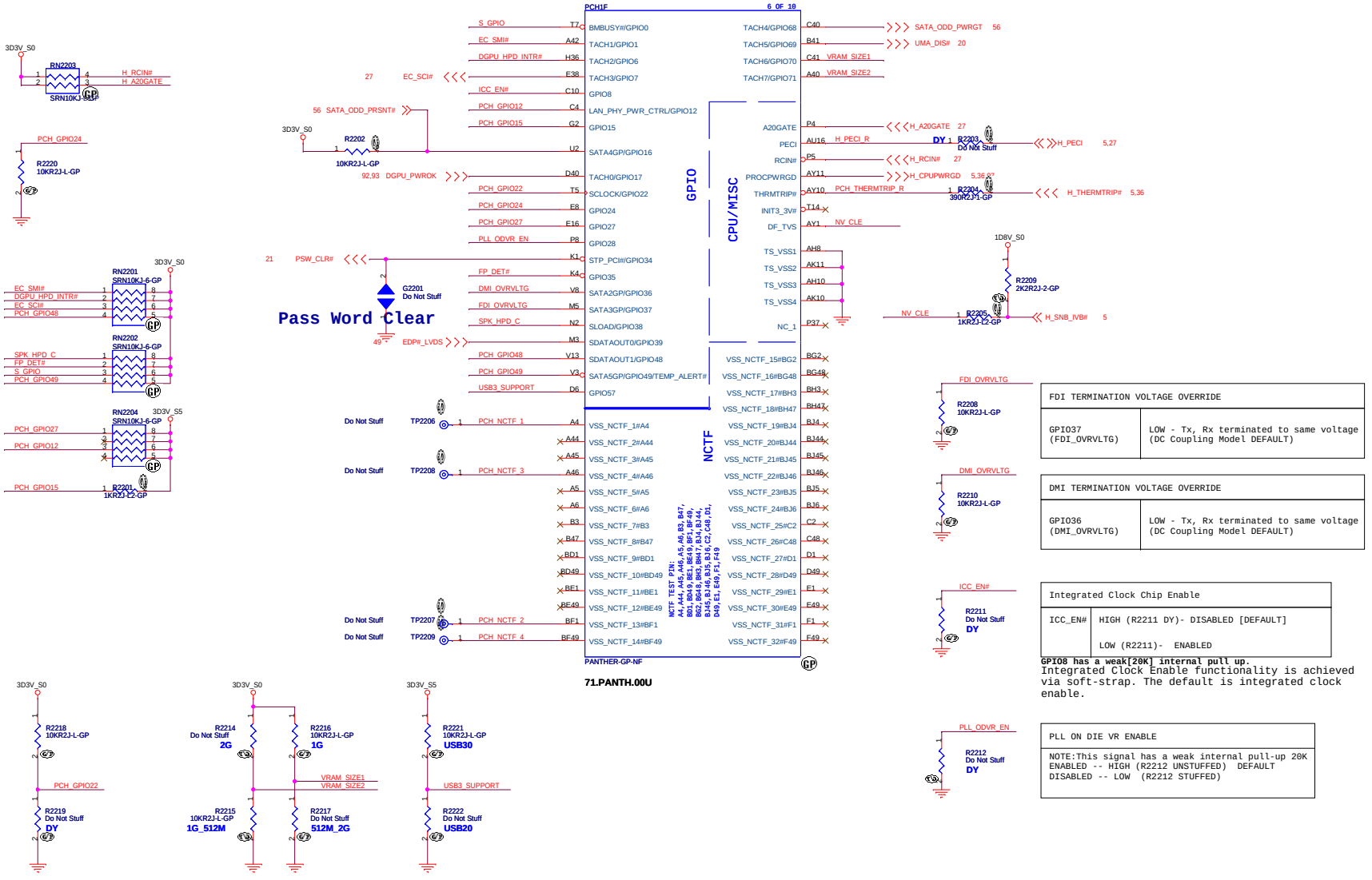
HDA_SYNC: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.

IVB

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (SPI/RTC/LPC/SATA/IHDA)
Size: Custom
Document Number: Husk/Petra
Rev: -2
Date: Tuesday, October 09, 2012
Sheet 21 of 103

SSID = PCH



FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY)- DISABLED [DEFAULT] LOW (R2211)- ENABLED

GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

PLL ON DIE VR ENABLE
NOTE:This signal has a weak internal pull-up 20K ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT DISABLED -- LOW (R2212 STUFFED)

IVB

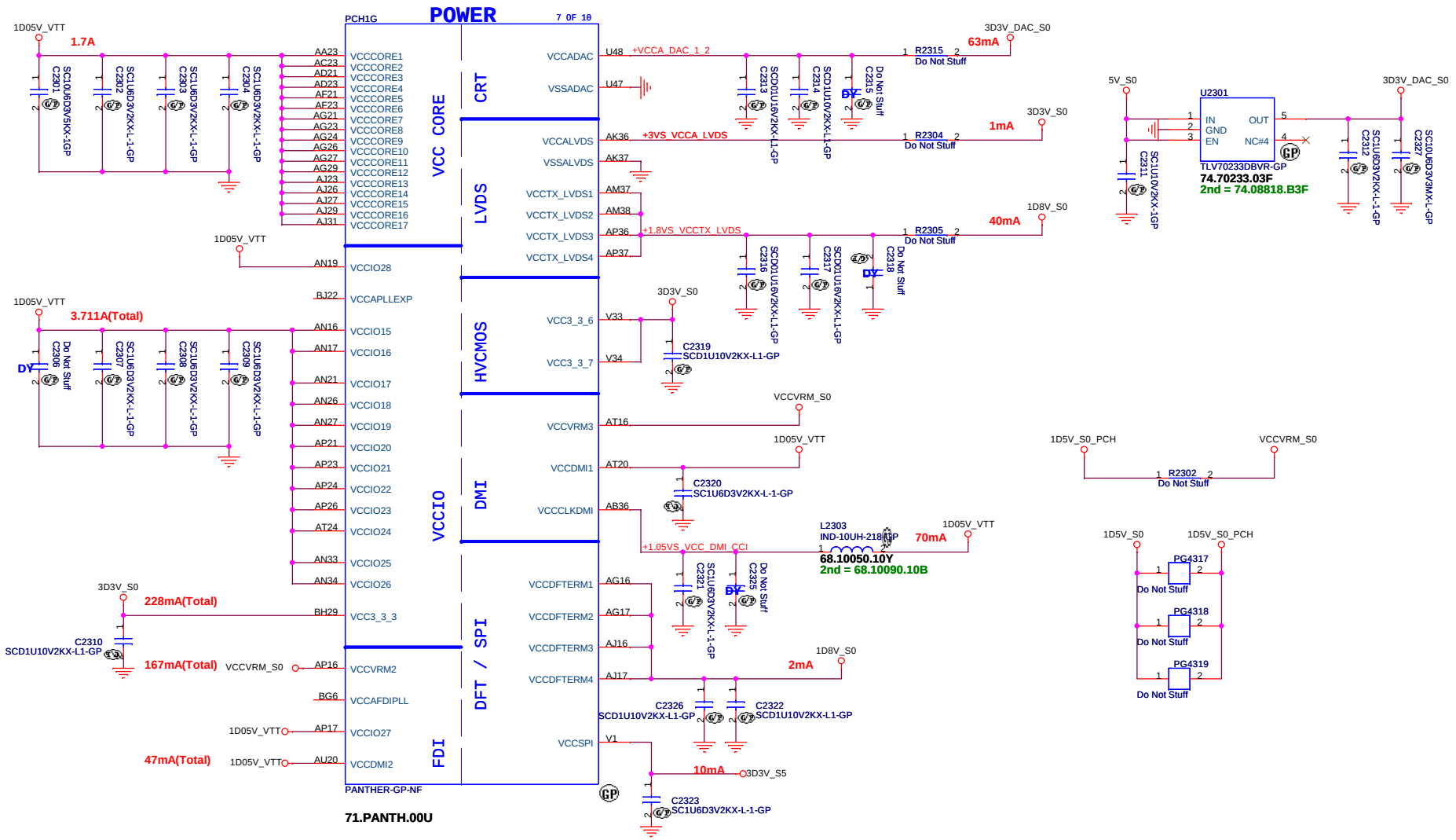
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (GPIO/CPU)

Size: Custom | Document Number: Husk/Petra | Rev: -2

Date: Tuesday, October 09, 2012 | Sheet 22 of 103

SSID = PCH



SSID = PCH

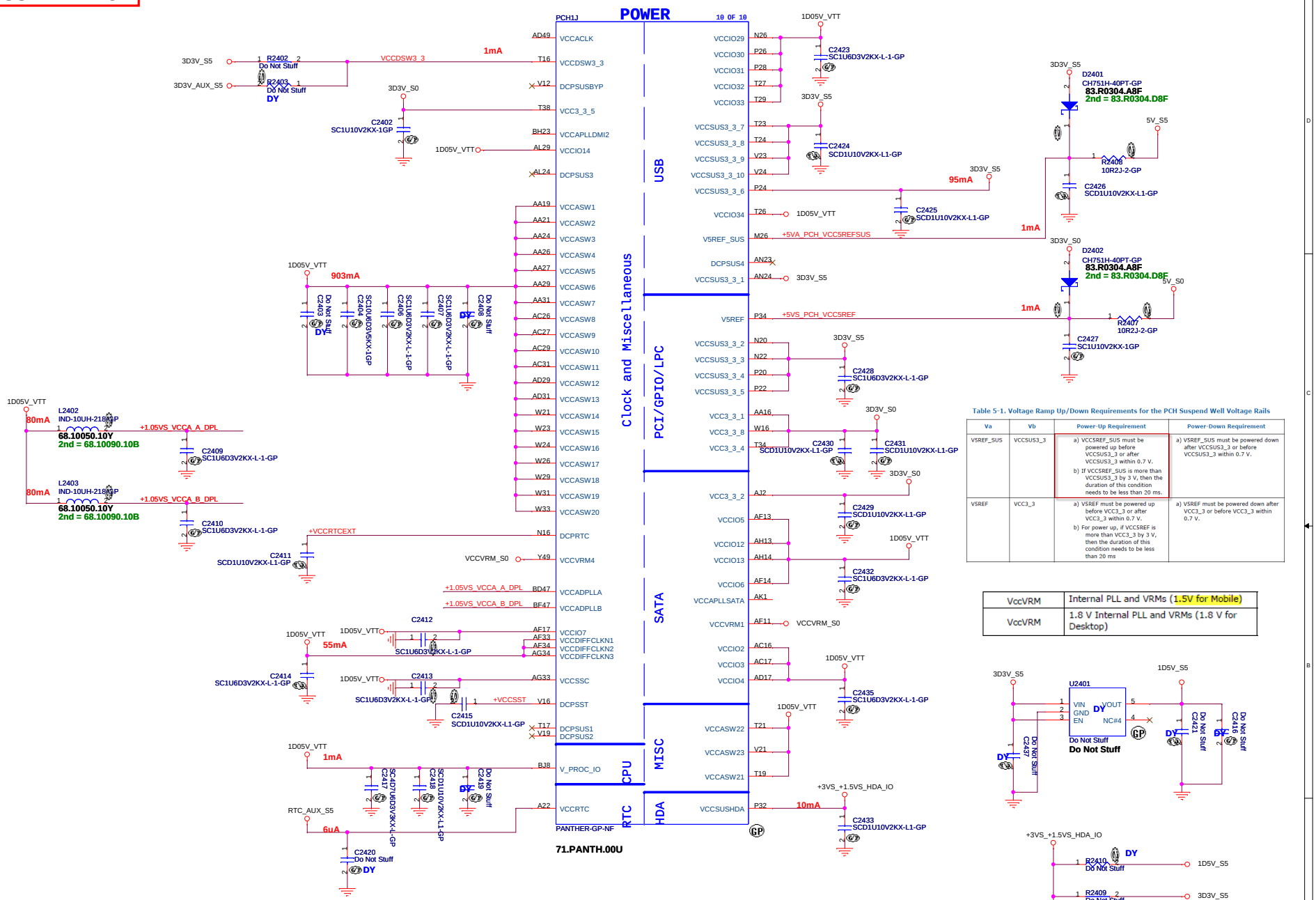
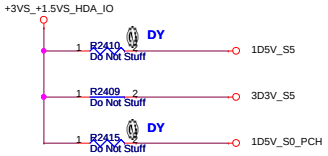


Table 5-1. Voltage Ramp Up/Down Requirements for the PCH Suspend Well Voltage Rails

Va	Vb	Power-Up Requirement	Power-Down Requirement
VSREF_SUS	VCCSUS3_3	a) VCC5REF_SUS must be powered up before VCCSUS3_3 or after VCCSUS3_3 within 0.7 V. b) If VCC5REF_SUS is more than VCCSUS3_3 by 3 V, then the duration of this condition needs to be less than 20 ms.	a) VSREF_SUS must be powered down after VCCSUS3_3 or before VCCSUS3_3 within 0.7 V.
VSREF	VCC3_3	a) VSREF must be powered up before VCC3_3 or after VCC3_3 within 0.7 V. b) For power up, if VCC5REF is more than VCC3_3 by 3 V, then the duration of this condition needs to be less than 20 ms	a) VSREF must be powered down after VCC3_3 or before VCC3_3 within 0.7 V.

VccVRM	Internal PLL and VRMs (1.5V for Mobile)
VccVRM	1.8 V Internal PLL and VRMs (1.8 V for Desktop)



IVB

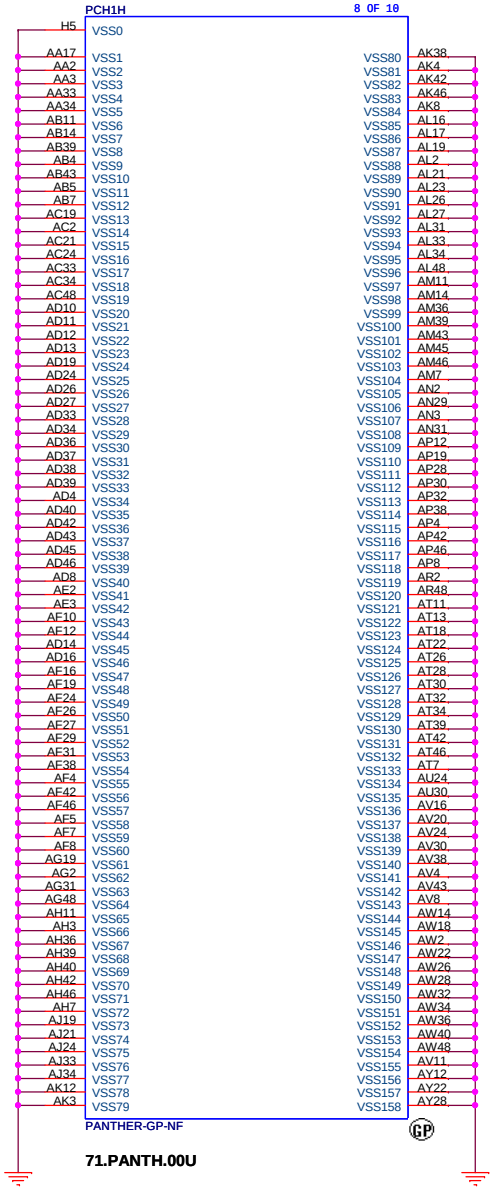
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

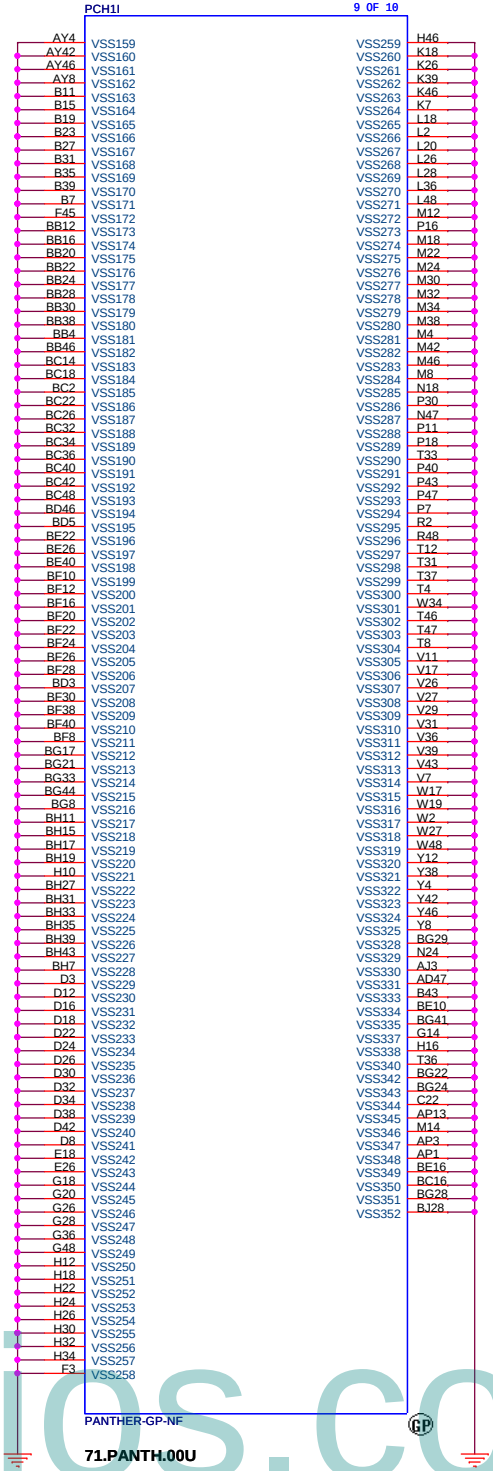
Title: PCH (POWER2)

Size	Document Number	Rev
Custom	Husk/Petra	-4M

Date: Thursday, October 11, 2012 Sheet 24 of 103

SSID = PCH





IVB

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***PCH (VSS)***

Size	Document Number	Rev
A3	Husk/Petra	-2

Date: Thursday, April 19, 2012 Sheet 25 of 103

IVB

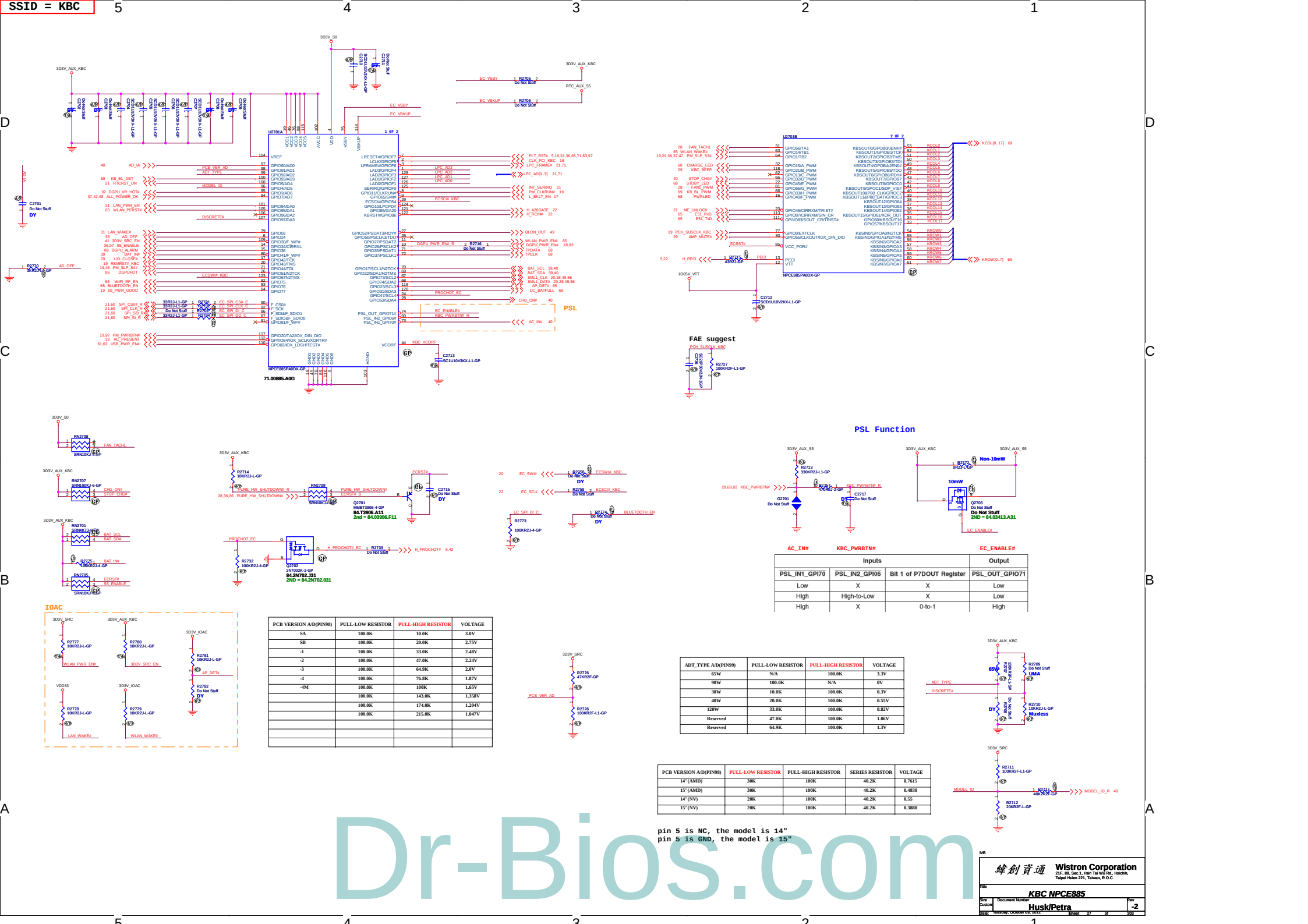
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Clock(colay)***

Size	Document Number	Rev
A4	**Husk/Petra**	**-2**

Date: Thursday, April 19, 2012 Sheet 26 of 103

SSID = KBC



PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
-1	100.0K	33.0K	2.48V
-2	100.0K	47.0K	2.24V
-3	100.0K	64.9K	2.0V
-4	100.0K	76.8K	1.87V
-4M	100.0K	100K	1.65V
	100.0K	143.0K	1.358V
	100.0K	174.0K	1.204V
	100.0K	215.0K	1.047V

ADT_TYPE A/D(PIN99)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
65W	N/A	100.0K	3.3V
90W	100.0K	N/A	0V
30W	10.0K	100.0K	0.3V
40W	20.0K	100.0K	0.55V
120W	33.0K	100.0K	0.82V
Reserved	47.0K	100.0K	1.06V
Reserved	64.9K	100.0K	1.3V

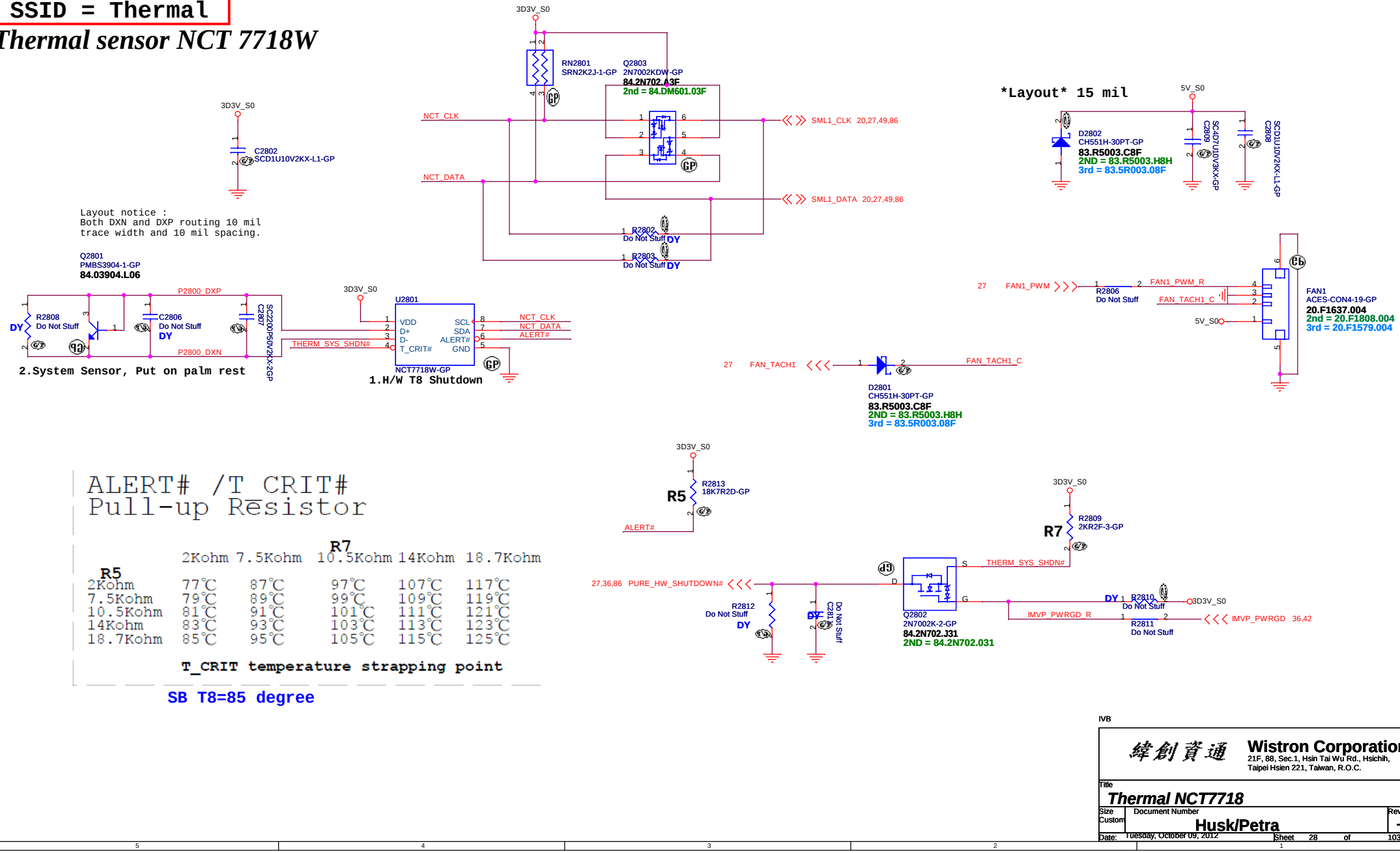
PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	SERIES RESISTOR	VOLTAGE
14"(AMD)	30K	100K	40.2K	0.7615
15"(AMD)	30K	100K	40.2K	0.4838
14"(NV)	20K	100K	40.2K	0.55
15"(NV)	20K	100K	40.2K	0.3888

Inputs			Output
PSL_IN1_GPI70	PSL_IN2_GPI06	Bit 1 of P7DOUT Register	PSL_OUT_GPIO71
Low	X	X	Low
High	High-to-Low	X	Low
High	X	0-to-1	High

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	KBC NPCE885
Size: Custom	Document Number: Husk/Petra
Rev	-2
Date: Tuesday, October 04, 2011	Sheet 27 of 103

SSID = Thermal

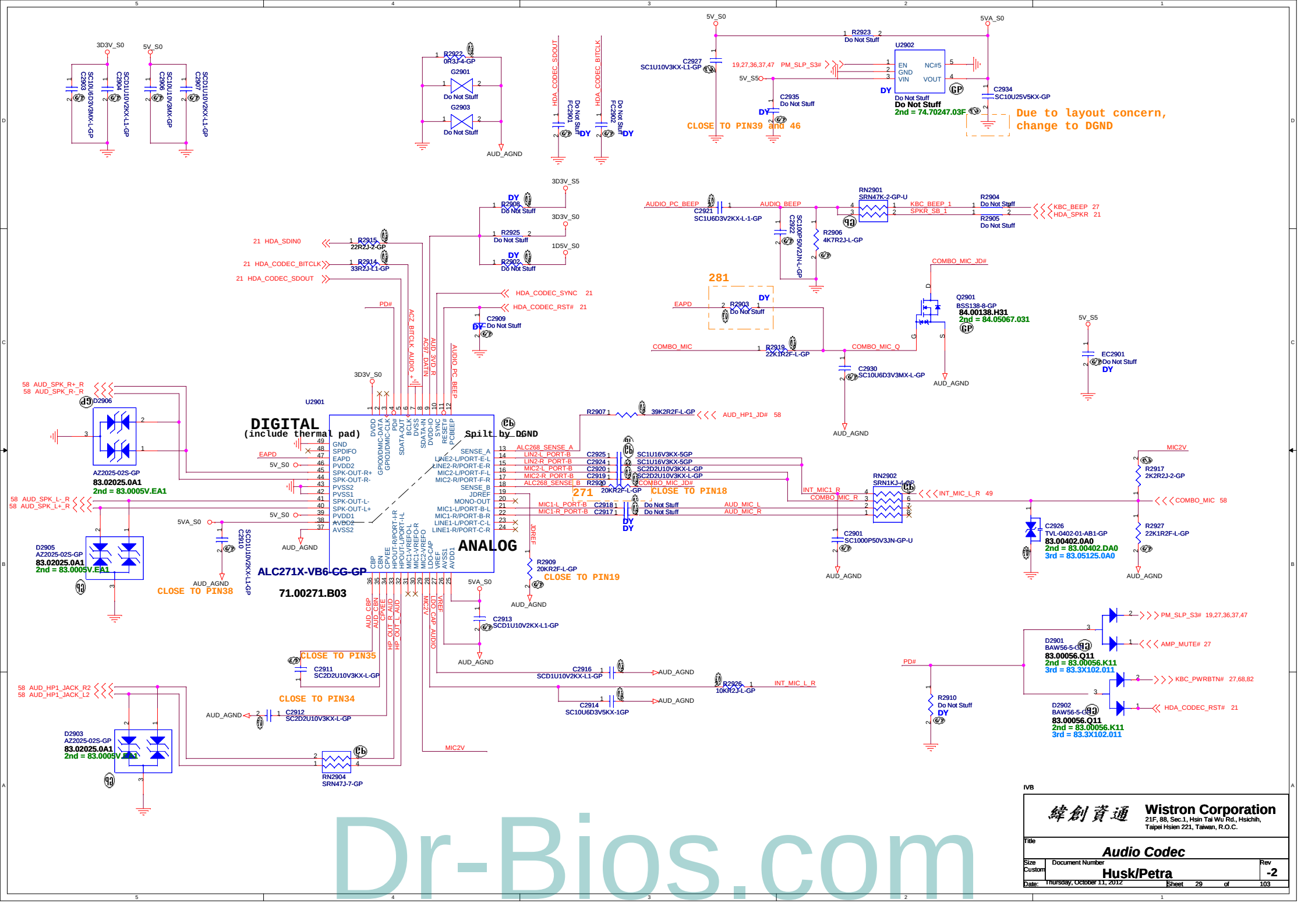
Thermal sensor NCT 7718W



IVB

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Thermal NCT7718*		
Size: Custom	Document Number: Husk/Petra	Rev: -2
Date: Tuesday, October 09, 2012	Sheet 28 of 103	


DIGITAL
(include thermal pad)
Spilt by DGND
ANALOG
ALC271X-VB6-CG-GP
71.00271.B03
U2901
U2902
CLOSE TO PIN39 and 46
CLOSE TO PIN38
CLOSE TO PIN35
CLOSE TO PIN34
CLOSE TO PIN18
CLOSE TO PIN19
Due to layout concern, change to DGND
281
271
Dr-Bios.com
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Audio Codec
Husk/Petra
Rev -2
Thursday, October 11, 2012
Sheet 29 of 103

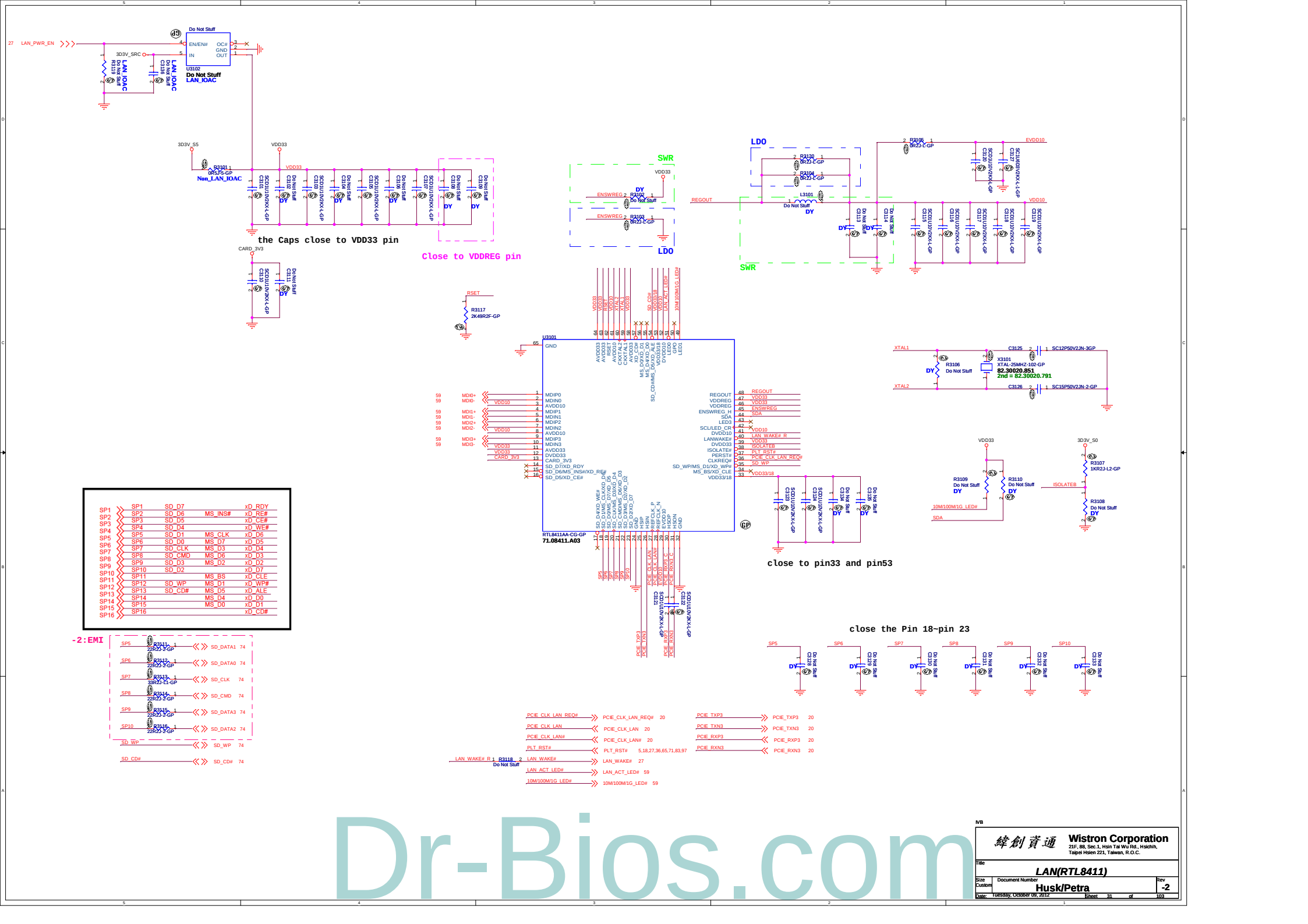
IVB

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Audio AMP***

Size	Document Number	Rev
A3	**Husk/Petra**	**-2**

Date: Thursday, April 19, 2012 Sheet 30 of 103



IVB

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN(RTL8411)

Size: Custom | Document Number: Husk/Petra | Rev: -2

Date: Tuesday, October 09, 2012 | Sheet 31 of 103

IVB

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***RTS5159 (CARD READER)***

Size	Document Number	Rev
Custom	**Husk/Petra**	**-2**

Date: Thursday, April 19, 2012 Sheet 32 of 103

(Blanking)

IVB

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	**Husk/Petra**	**-2**

Date: Thursday, April 19, 2012 Sheet 33 of 103

(Blanking)

IVB

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	Husk/Petra	-2

Date: Thursday, April 19, 2012 Sheet 34 of 103

IVB

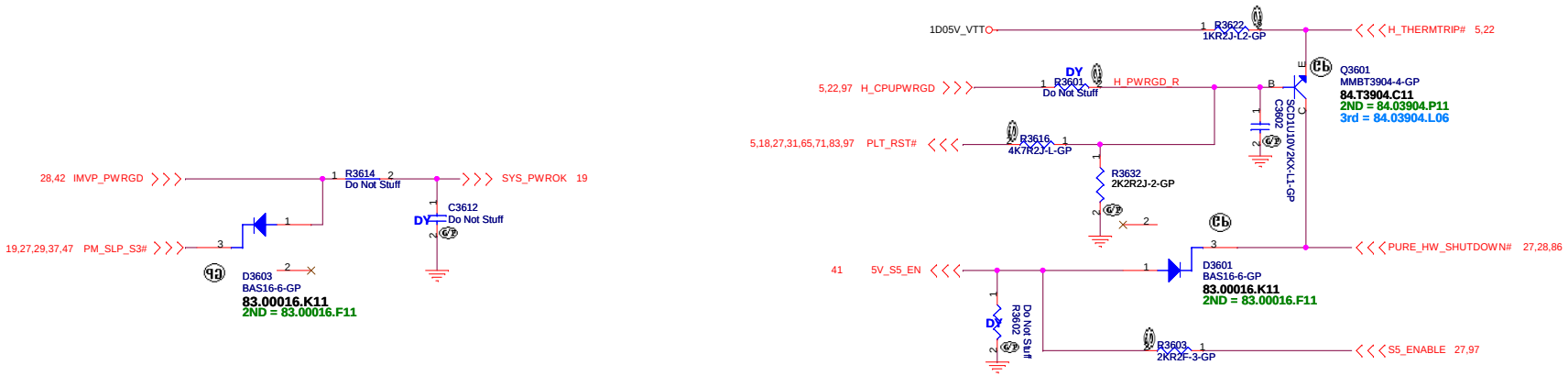
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

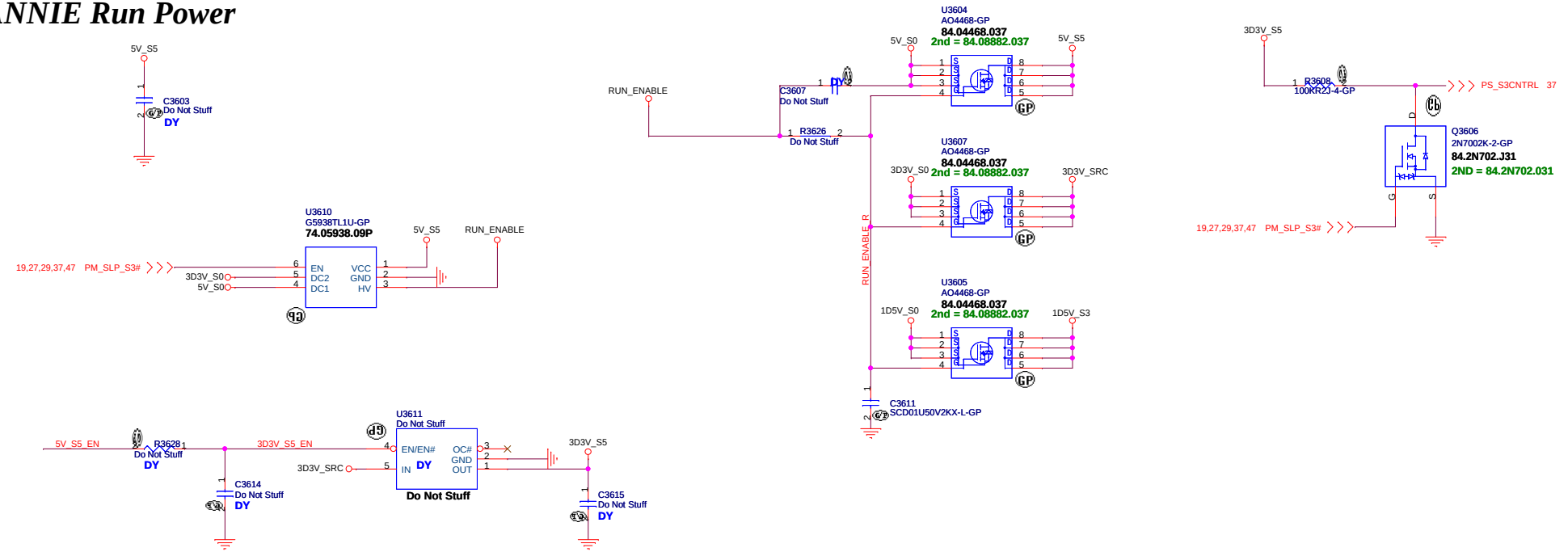
USB 3.0 Controller

Size	Document Number	Rev
Custom	**Husk/Petra**	-2
Date: Thursday, April 19, 2012	Sheet 35 of 103	

Power Sequence



ANNIE Run Power



IVB

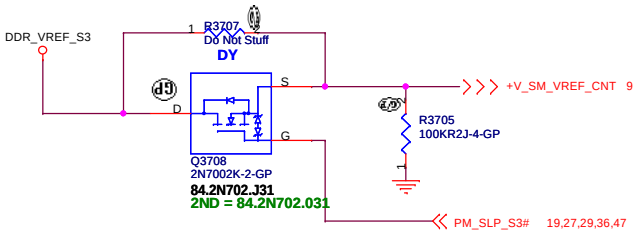
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

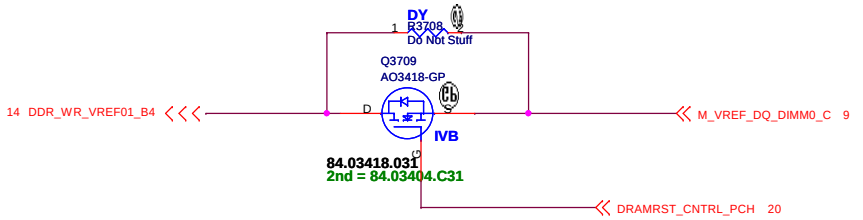
Title: **Power Plane Enable**

Size: Custom | Document Number: **Husk/Petra** | Rev: -2

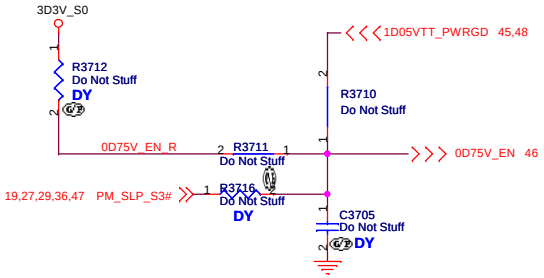
Date: Tuesday, October 09, 2012 | Sheet 36 of 103

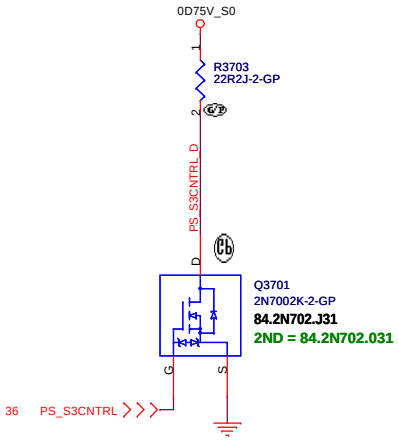
Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation

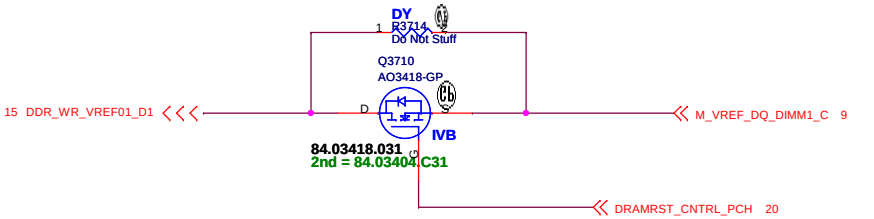




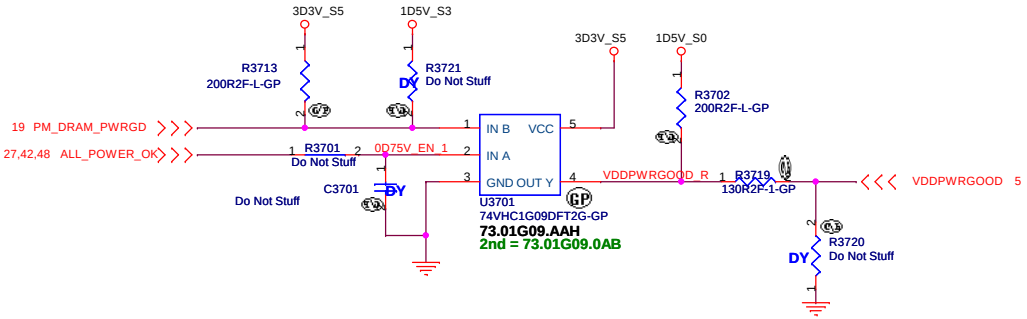
Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK



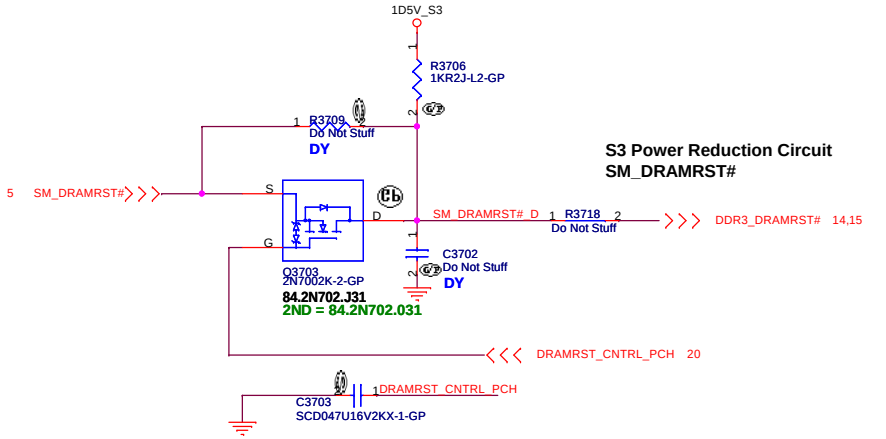




Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



S3 Power Reduction Circuit
SM_DRAMRST#

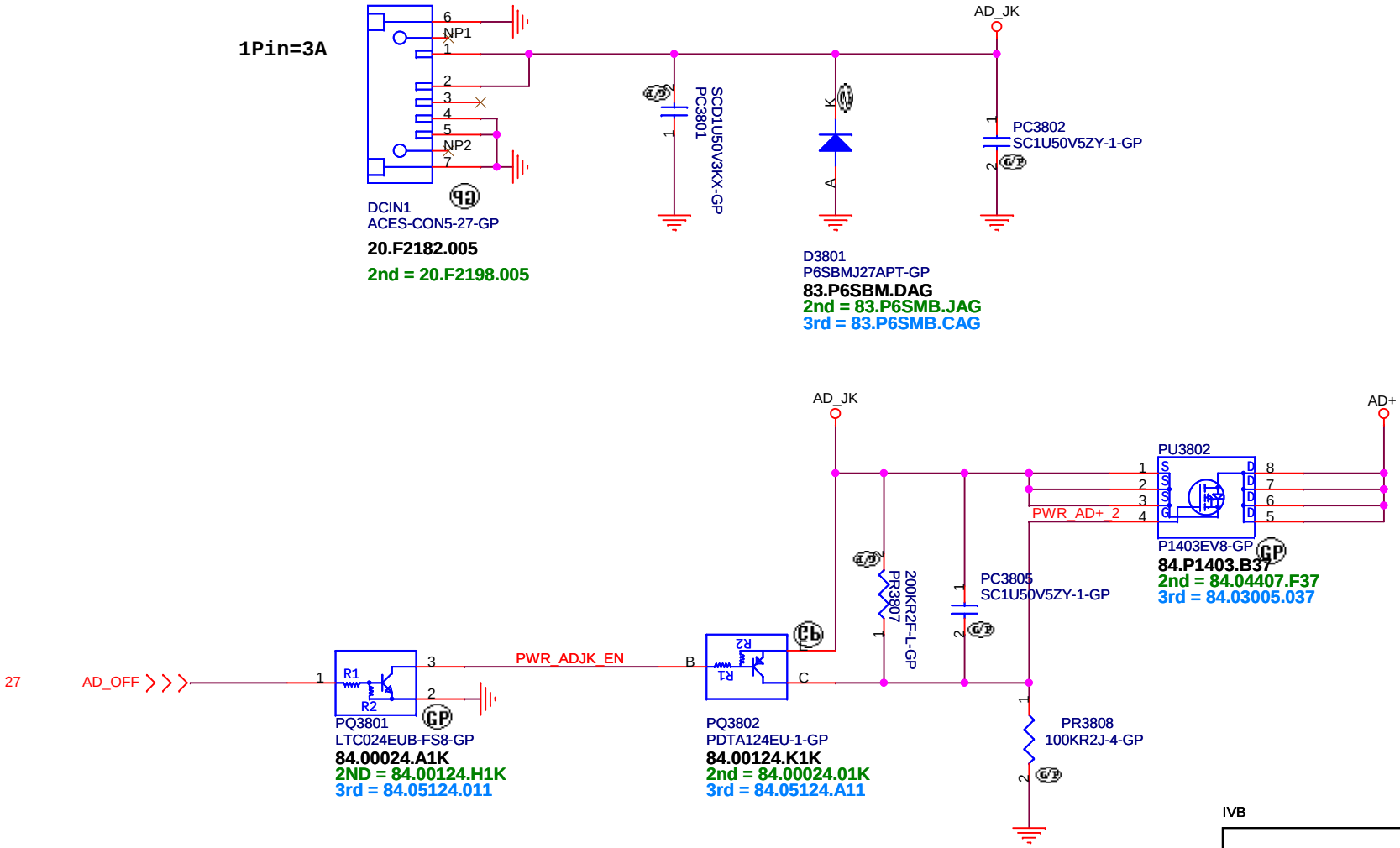
IVB

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ADAPTER**

Size	Document Number	Rev
A3	Husk/Petra	-2

Date: Tuesday, October 09, 2012 Sheet 37 of 103

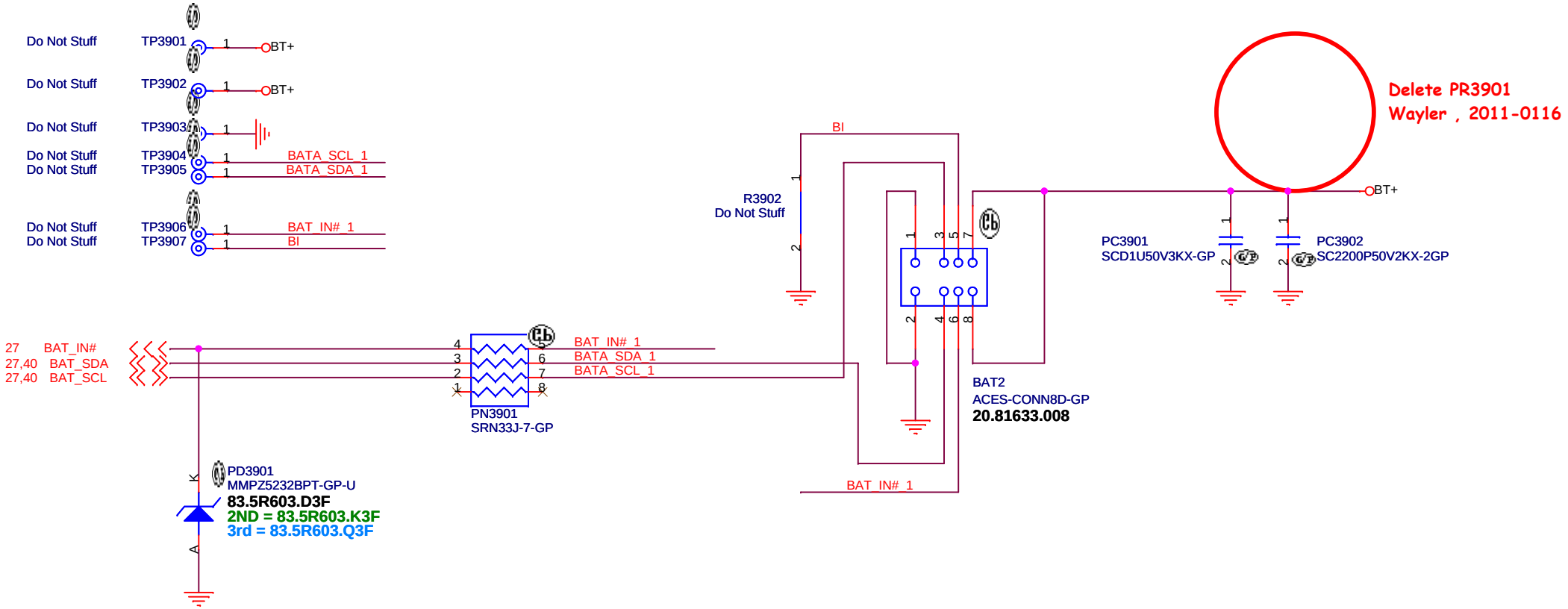


IVB

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***DCIN JACK***	
Size A4	Document Number **Husk/Petra**	Rev **-2**
Date: Thursday, June 14, 2012	Sheet 38 of 103	

BATTERY CONNECTOR



IVB

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***BATT CONN***

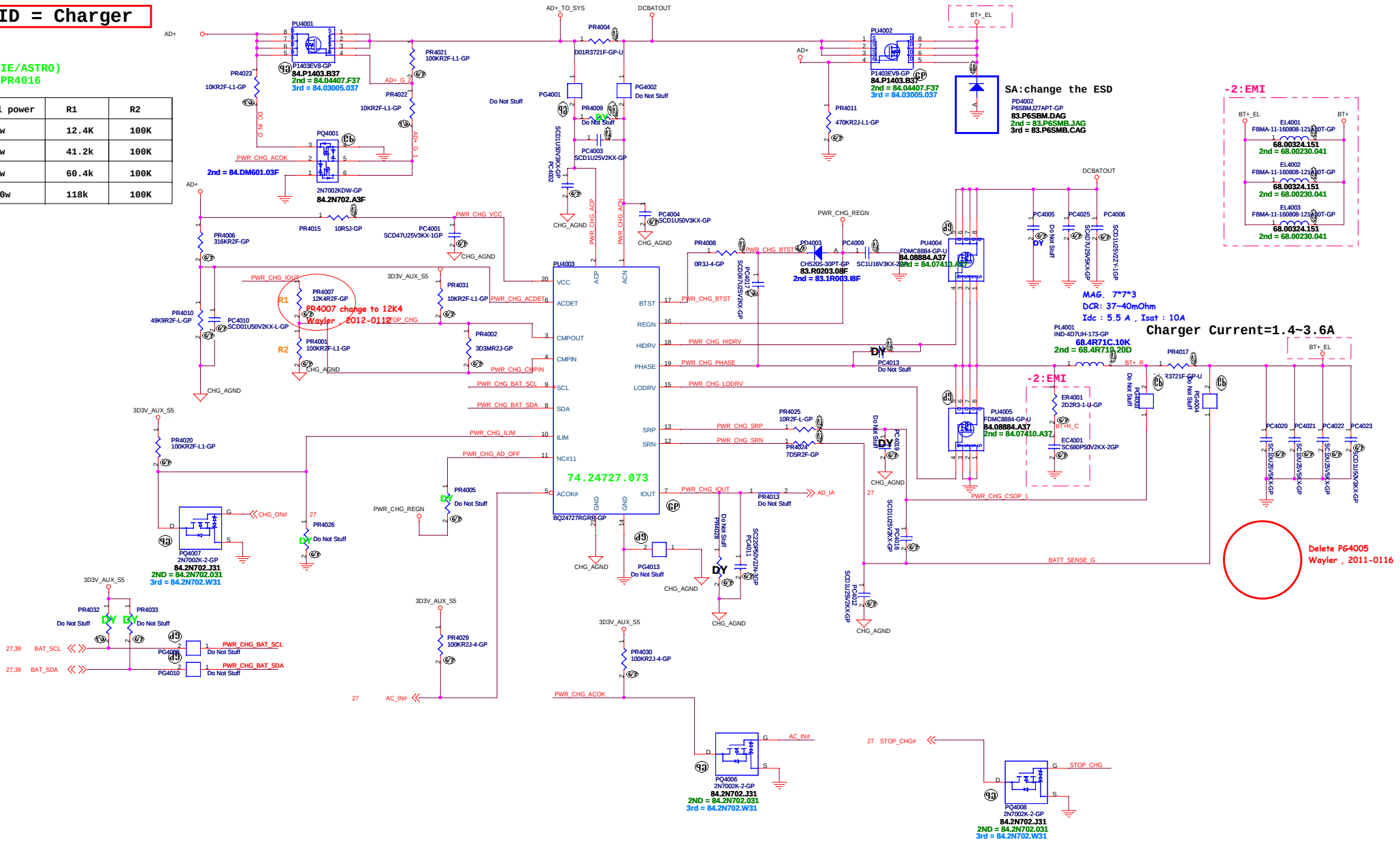
Size	Document Number	Rev
A4	**Husk/Petra**	**-2**

Date: Tuesday, October 09, 2012 Sheet 39 of 103

SSID = Charger

A8(ANNIE/ASTRO)
PR4014,PR4016

AD+ total power	R1	R2
65w	12.4K	100K
80w	41.2k	100K
90w	60.4k	100K
120w	118k	100K



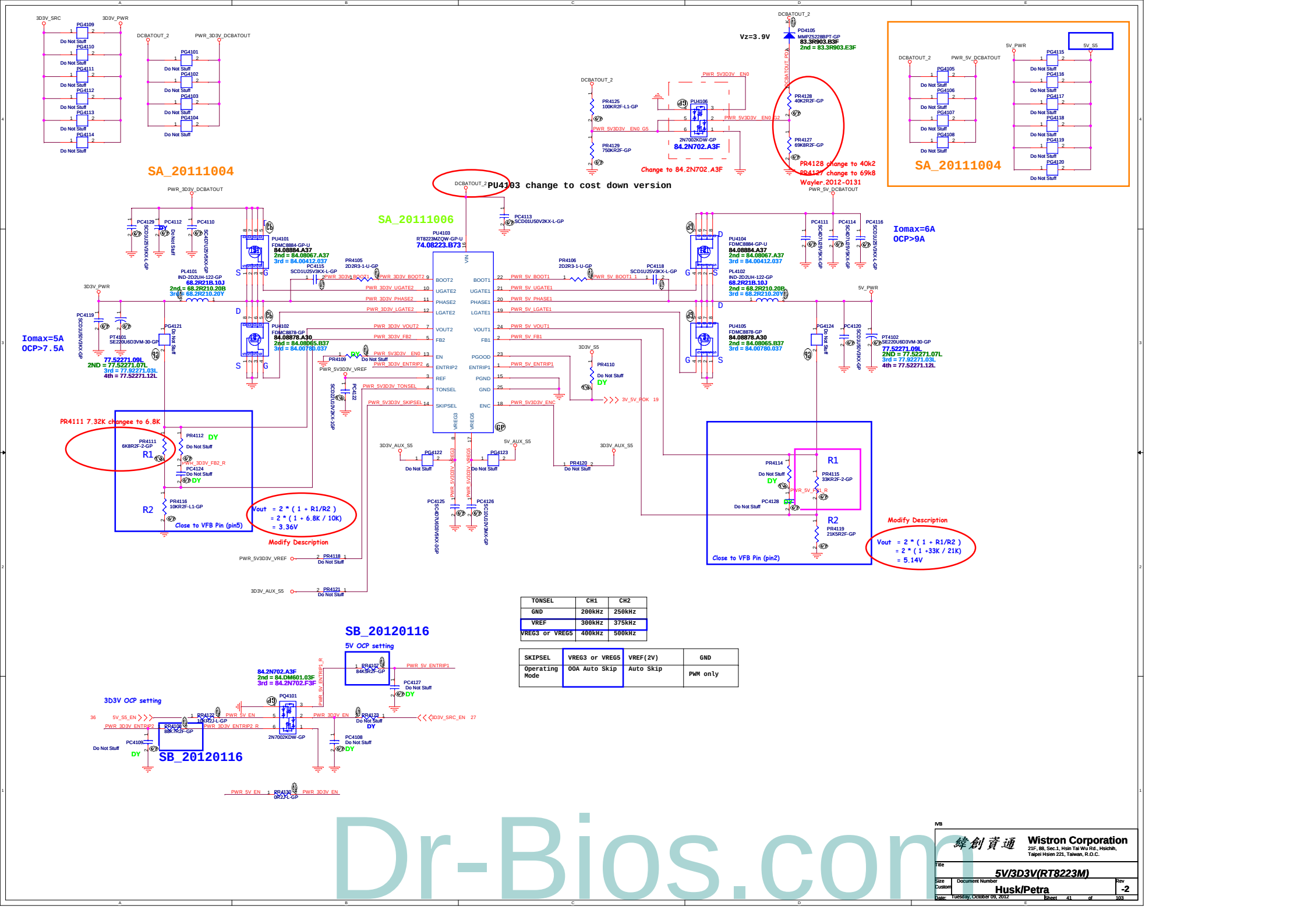
IVB

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

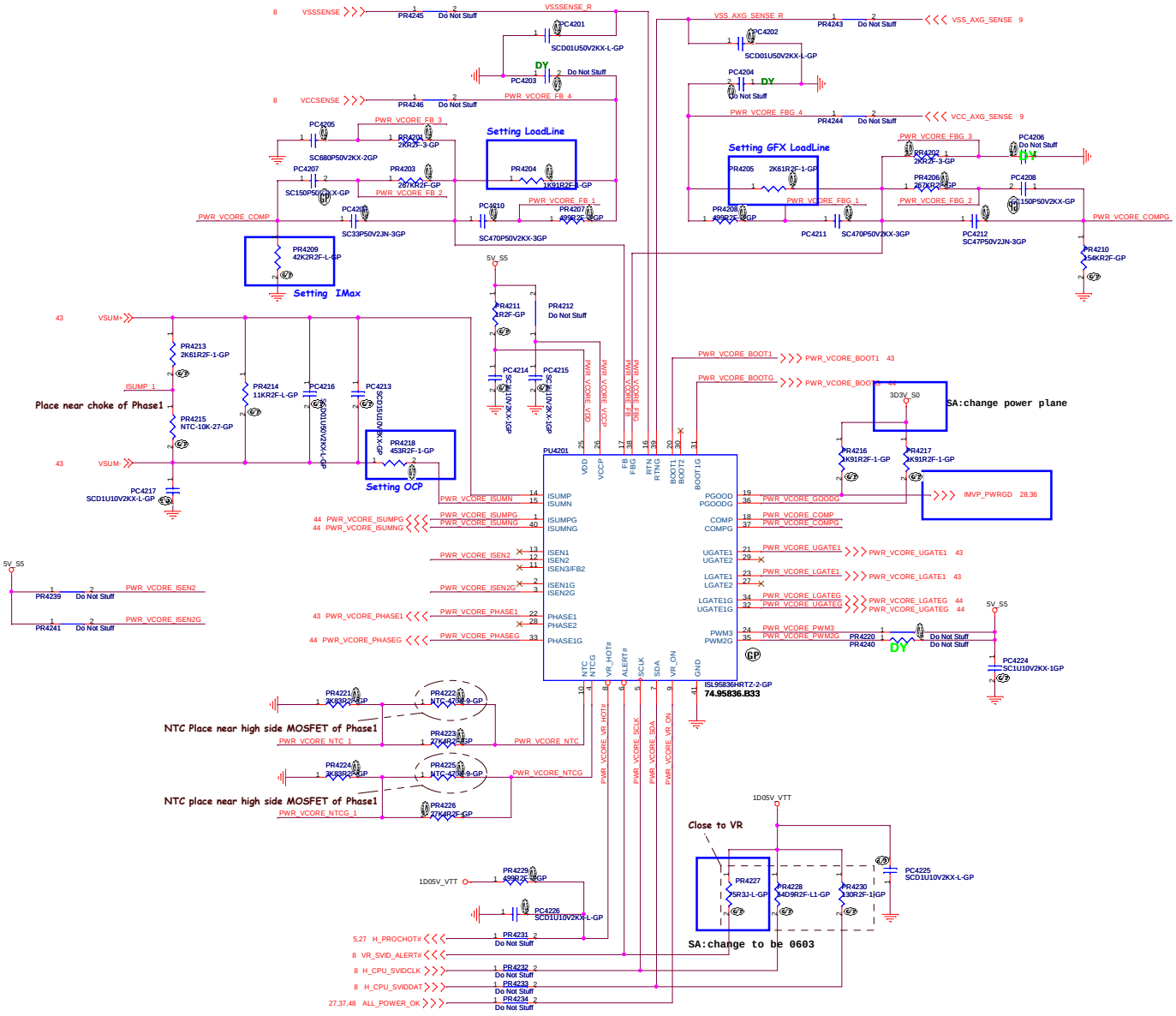
Title: CHARGER BQ24707A

Size: Custom | Document Number: Husk/Petra | Rev: -2

Date: Tuesday, October 09, 2012 | Sheet 40 of 108


SA_20111004
SA_20111006
SB_20120116
PU4103 change to cost down version
Vz=3.9V
PD4105
MMPZ5228BPT-GP
83.3R903.B3F
2nd = 83.3R903.E3F
PR4128 change to 40k2
PR4127 change to 69k8
Wayler.2012-0131
Change to 84.2N702.A3F
84.2N702.A3F
RT8223MZQW-GP-U
74.08223.B73
Iomax=6A
OCP>9A
Iomax=5A
OCP>7.5A
PR4111 7.32K change to 6.8K
Vout = 2 * (1 + R1/R2)
= 2 * (1 + 6.8K / 10K)
= 3.36V
Close to VFB Pin (pin5)
Modify Description
Vout = 2 * (1 + R1/R2)
= 2 * (1 +33K / 21K)
= 5.14V
Close to VFB Pin (pin2)
5V OCP setting
3D3V OCP setting
84.2N702.A3F
2nd = 84.DM601.03F
3rd = 84.2N702.F3F
TONSEL | CH1 | CH2
GND | 200kHz | 250kHz
VREF | 300kHz | 375kHz
VREG3 or VREG5 | 400kHz | 500kHz
SKIPSEL | VREG3 or VREG5 | VREF(2V) | GND
Operating Mode | OOA Auto Skip | Auto Skip | PWM only
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
5V/3D3V(RT8223M)
Husk/Petra
-2
Tuesday, October 09, 2012
41
103

SSID = CPU.Regulator



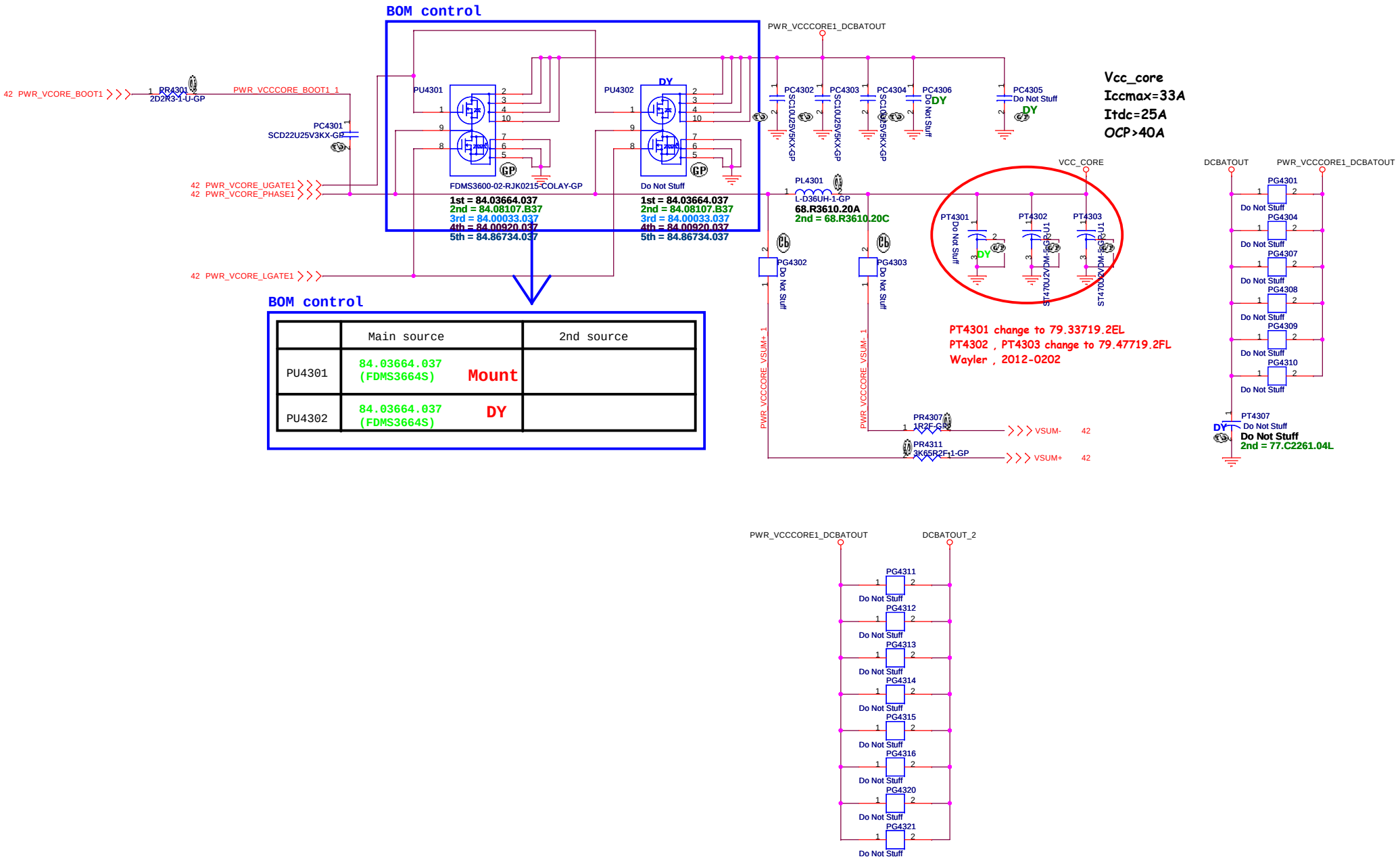
IVB

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL95836_CPU_CORE(1/3)

Size: Custom | Document Number: Husk/Petra | Rev: -2

Date: Thursday, October 11, 2012 | Sheet 42 of 102



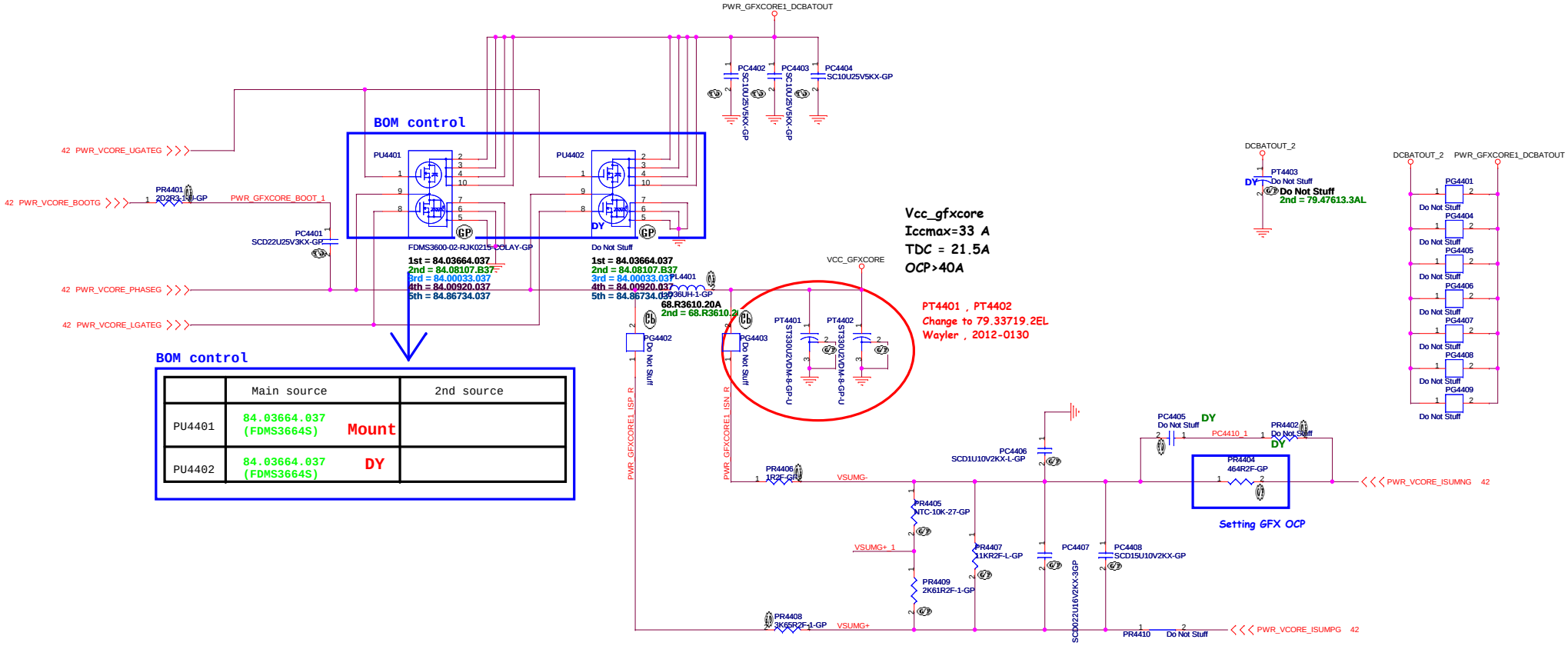
IVB

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL95836_CPU_CORE(2/3)

Size: A3 | Document Number: Husk/Petra | Rev: -4M

Date: Thursday, October 11, 2012 | Sheet 43 of 102



BOM control

	Main source	2nd source
PU4401	84.03664.037 (FDMS3664S) Mount	
PU4402	84.03664.037 (FDMS3664S) DY	

IVB

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

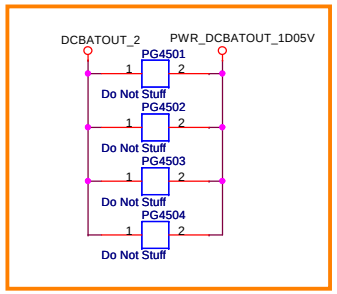
Title: ISL95836_CPU_CORE(3/3)

Size	Document Number	Rev
Custom	Husk/Petra	-4M

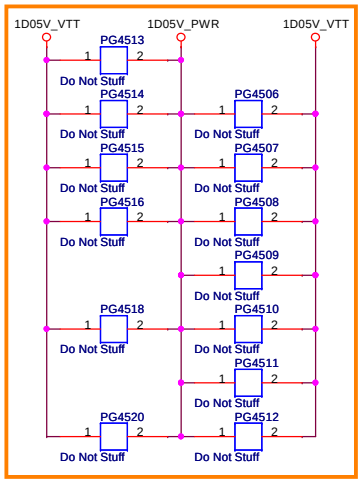
Date: Thursday, October 11, 2012 Sheet 44 of 102

TPS51218D for 1D05V

SA_20111004



SA_20111013



PR4504 change to 54K9 , OCP > 27A
2012-0130 , Wayler.

Freq=360KHz

Iomax = 20.645A
TDC = 14.45 A
OCP > 26.83A

Pana. 0.42uH 7*7*4
DCR=1.5mohm

OCP setting

Vout=0.704*(1+R1/R2)

SB

IVB

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	DC to DC 1D05V(TPS51218D)
Size A3	Document Number Husk/Petra
Rev	-2
Date: Tuesday, October 09, 2012	Sheet 45 of 103

SSID = PWR.Plane.Regulator_1p5v0p75v

Change power source

SA_20111004

SC:delete PT4601

RT8207L for 1D5V

OCP setting

PR4603 change to 8K87 , OCP>24A
2012 - 0111 - Wayler

Close to pin23

Close to pin23

20100728

Iomax=1A
OCP>1.5A

Close to output cap pin1, not inside of the output cap

PU4601 change to 74.08207.D73
2012 - 0111 - Wayler

PR4608 change to 30.9K
2012 - 0111 - Wayler

Close to PIN9

Vout=0.75*(1+R1/R2)

CYNTEC. 0.68uH 7*7*3
DCR= 5 ~ 5.5 mohm
Idc=15.5A, Isat=25A

IccMAX = 18.38A
IccTDC = 12.86A
OCP > 23.89A

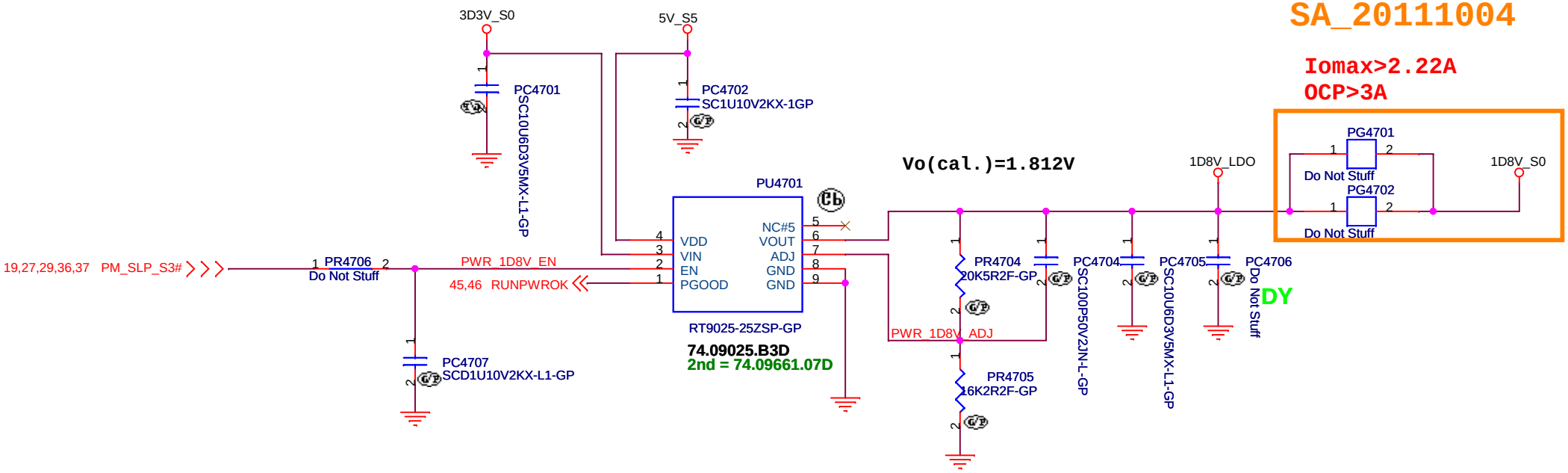
SD:暫時先換7x7mm

+0.75VS
Iomax: 1.2A

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	RT8207
Size: Custom	Document Number: Husk/Petra
Rev	-2
Date: Tuesday, October 09, 2012	Sheet 46 of 103

SSID = PWR.Plane.Regulator_1p8v

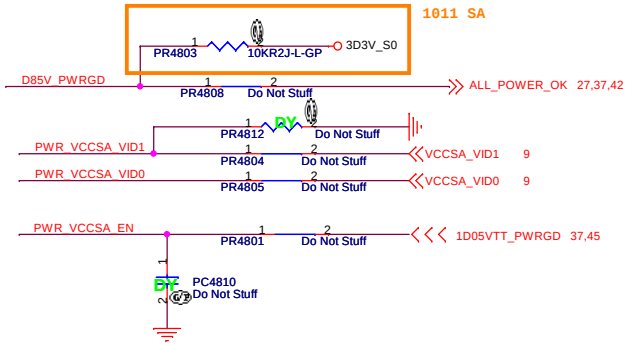
RT9025 for 1D8V_S0



IVB

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *LDO_1D8V(RT9025)*		
Size: A4	Document Number: Husk/Petra	Rev: -2
Date: Thursday, April 19, 2012	Sheet 47 of 103	

LDO G978 for VCCSA



D0, D1 V_0 Selection Table

D0	D1	V_0 MODE=0	V_0 MODE=1
0	0	0.9V	0.9V
0	1	0.8V	0.85V
1	0	0.725V	0.775V
1	1	0.675V	0.75V

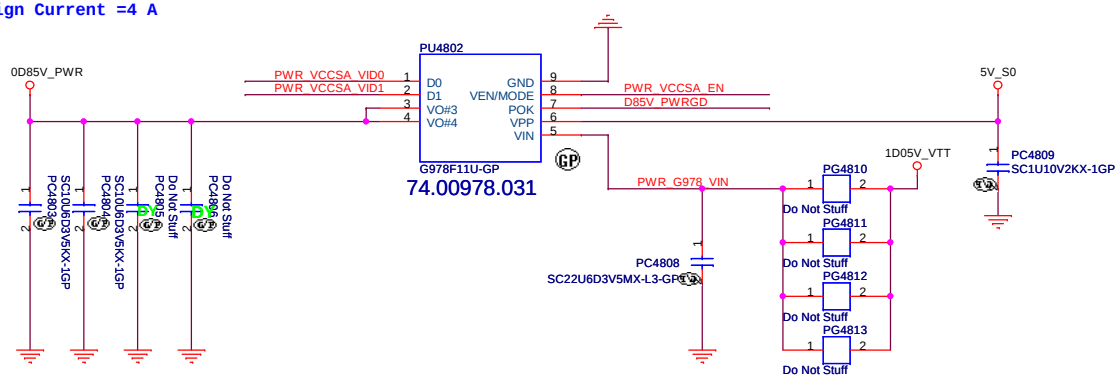
"x" means "don't care".

VEN/MODE Logic

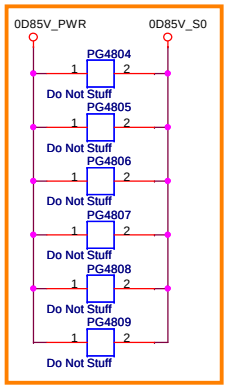
VEN/MODE (VPP=5V)	EN logic
<0.6V	0
>1.0V	1

VEN/MODE (VPP=5V)	MODE logic
<2.0V	0
>2.6V	1

Design Current =4 A



1011 SA



IVB

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

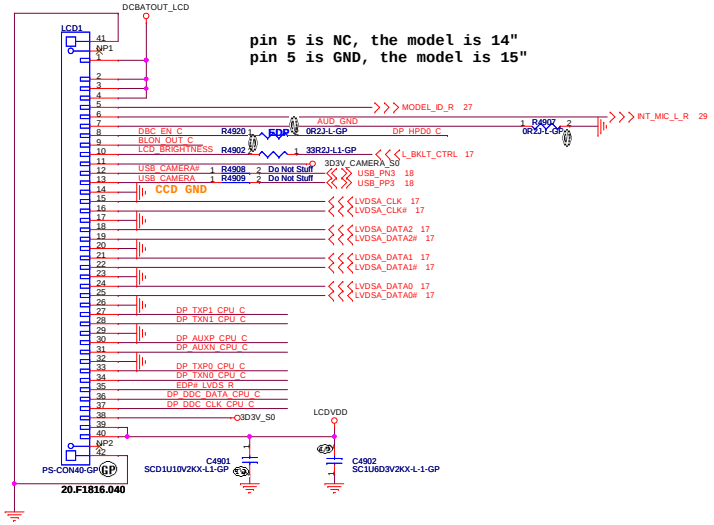
Title: ***VCCSA LDO G978***

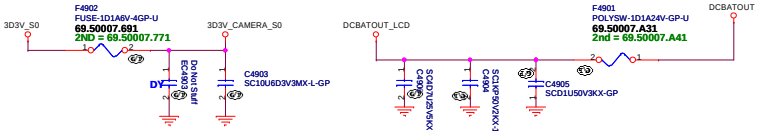
Size	Document Number	Rev
A3	Husk/Petra	-2

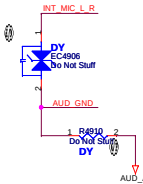
Date: Thursday, April 19, 2012 Sheet 48 of 103

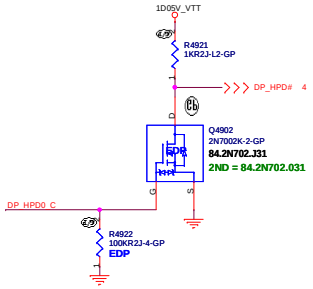
SSID = VIDEO

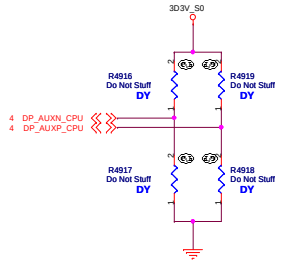
pin 5 is NC, the model is 14"
pin 5 is GND, the model is 15"

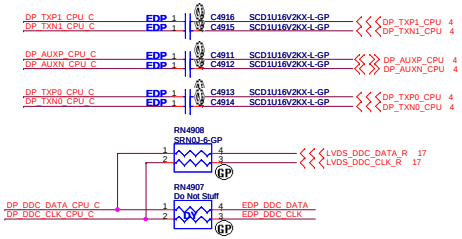


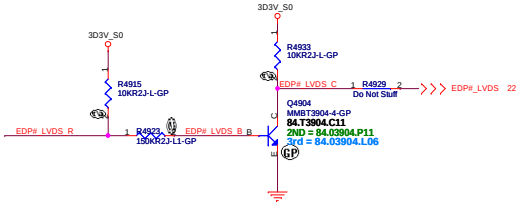




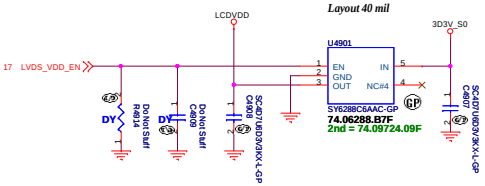


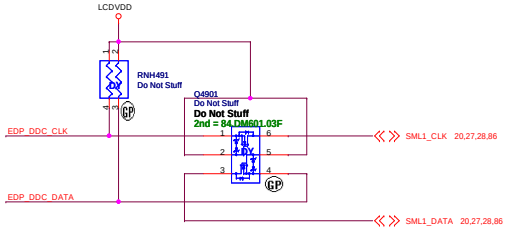


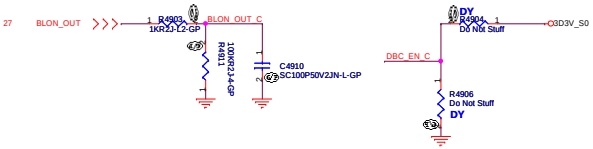


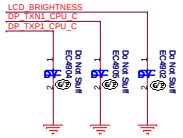


EDP: pin35 NC
LVDS: pin35 GND





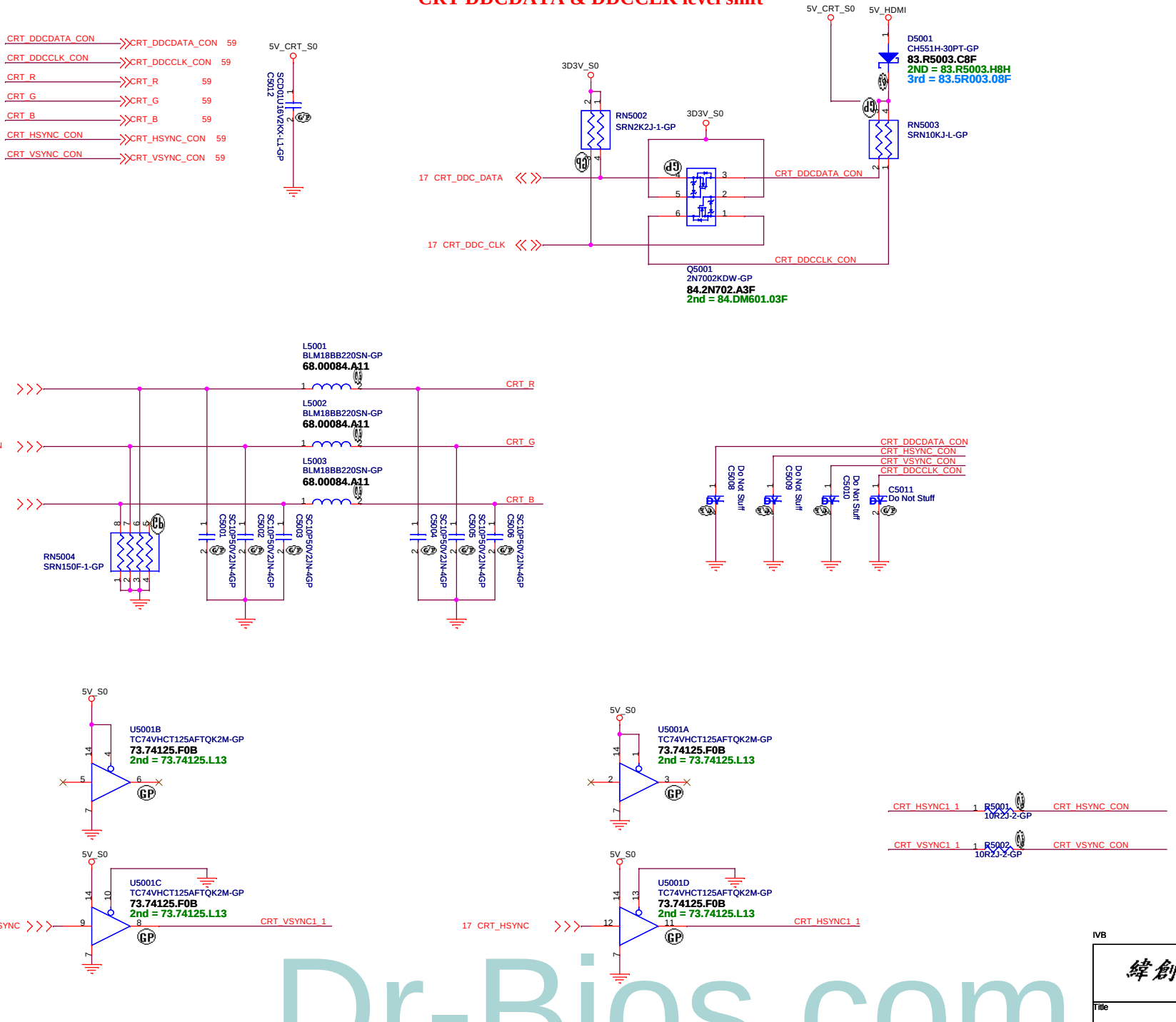




IVB

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: LCD Connector		
Size: A2	Document Number: Husk/Petra	Rev: -2
Date: Thursday, April 19, 2012	Sheet 49 of 103	

CRT DDCDATA & DDCCLK level shift



IVB

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRT Connector**

Size	Document Number	Rev
A3	Husk/Petra	-2

Date: Thursday, October 11, 2012 Sheet 50 of 103

SSID = VIDEO

HDMI Level Shifter & CONNECTOR

Close to HDMI Connector

change = DIS:499 ohm
Fist = UMA Muxless:680 ohm

17 HDMI_CLK_R#
17 HDMI_CLK_R
17 HDMI_DATA0_R#
17 HDMI_DATA0_R
17 HDMI_DATA1_R#
17 HDMI_DATA1_R
17 HDMI_DATA2_R#
17 HDMI_DATA2_R

HDMI_DATA2_R#
HDMI_DATA2_R
HDMI_DATA0_R#
HDMI_DATA0_R
HDMI_DATA1_R
HDMI_DATA1_R#
HDMI_CLK_R
HDMI_CLK_R#

RN5114
SRN499F-GP

RN5115
SRN499F-GP

HDMI_PLL_GND

Q5105
2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031

5V_S0

HDMI1
SKT-HDMI23-45-GP
22.10296.631
2nd = 22.10296.821

HDMI_DATA2_R
HDMI_DATA2_R#
HDMI_DATA1_R
HDMI_DATA1_R#
HDMI_DATA0_R
HDMI_DATA0_R#
HDMI_CLK_R
HDMI_CLK_R#
DDC_CLK_HDMI
DDC_DATA_HDMI
5V_HDMI

5V_HDMI
5V_S0
F5101
FUSE-1D1A6V-4GP-U
69.50007.691
2nd = 69.50007.771

HPD_HDMI_CON
R5111
150KR2J-L1-GP
HDMI_HPD_B

3D3V_S0
Q5102
MMBT3904-4-GP
84.T3904.C11
2ND = 84.03904.P11
3rd = 84.03904.L06

R5110
Do Not Stuff

HDMI_HPD_E
R5129
Do Not Stuff
HDMI_PCH_DET 17

R5112
10KR2J-L-GP

D5103
BAW56-5-GP
83.00056.Q11
2nd = 83.00056.K11
3rd = 83.3X102.011

5V_S0_D1
5V_S0_D2
5V_S0

RN5102
SRN2K2J-1-GP

Q5106
2N7002KDW-GP
84.2N702.A3F
2nd = 84.DM601.03F

3D3V_S0

17 PCH_HDMI_CLK
17 PCH_HDMI_DATA

DDC_CLK_HDMI
DDC_DATA_HDMI

IVB

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter/Connector

Size: A3 | Document Number: Husk/Petra | Rev: -2

Date: Friday, August 24, 2012 | Sheet 51 of 103

LED BACKLIGHT CONVERTER POWER

IVB

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: eDP

Size: A3 | Document Number: Husk/Petra | Rev: -2

Date: Thursday, April 19, 2012 | Sheet 52 of 103

(Blanking)

IVB

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***S-VIDEO***

Size	Document Number	Rev
A4	Husk/Petra	-2

Date: Thursday, April 19, 2012 Sheet 53 of 103

(Blanking)

IVB

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

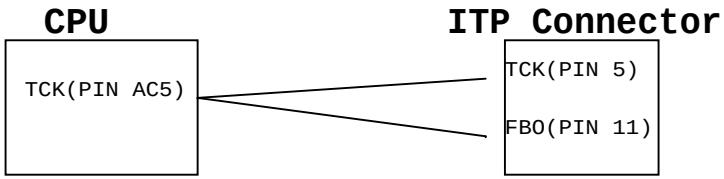
Size	Document Number	Rev
A4	Husk/Petra	-2

Date: Thursday, April 19, 2012 Sheet 54 of 103

SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



IVB

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

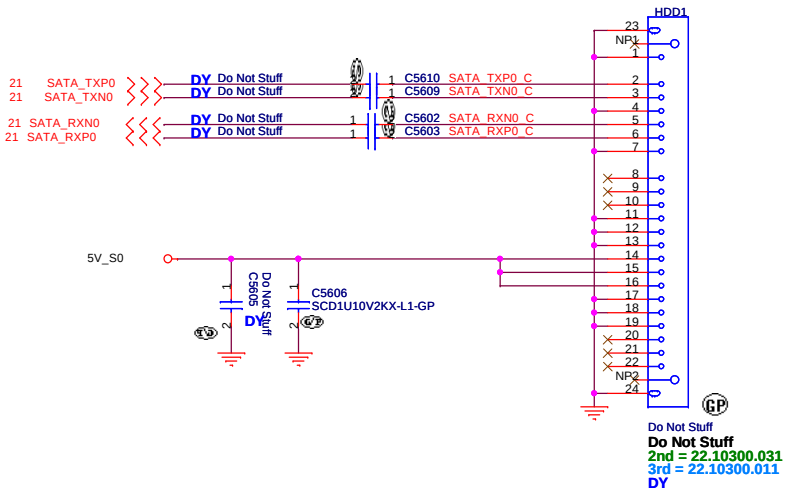
Title: ITP

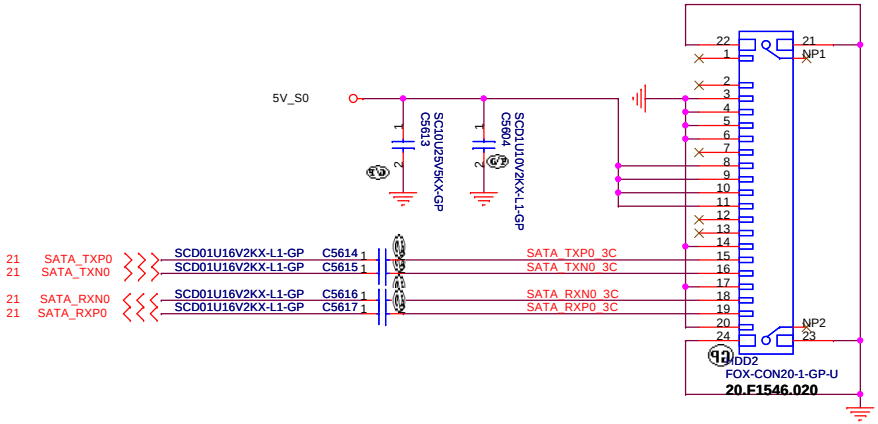
Size: A4 | Document Number: Husk/Petra | Rev: -2

Date: Thursday, April 19, 2012 | Sheet 55 of 103

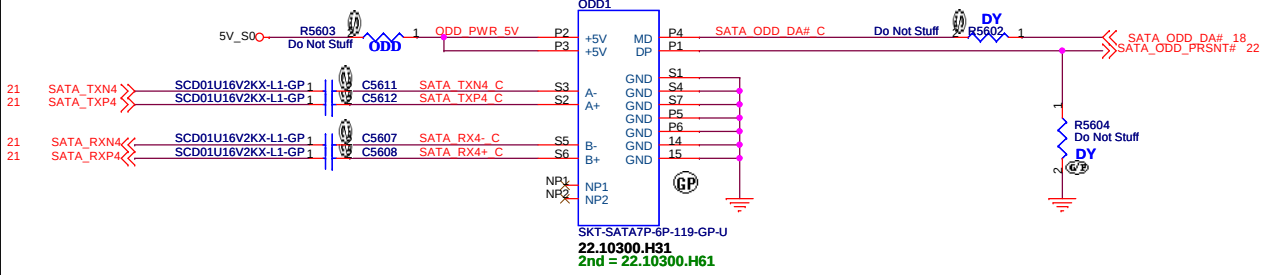
SSID = SATA

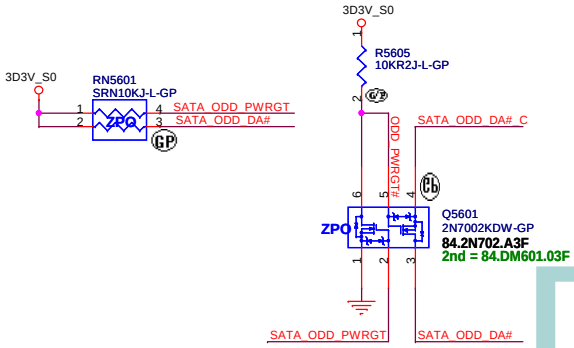
SATA HDD Connector



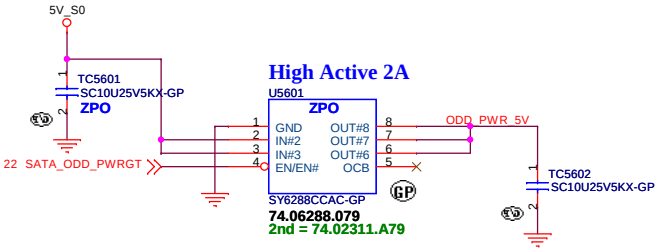


ODD Connector





SATA Zero Power ODD



IVB

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/ODD

Size	Document Number	Rev
A3	Husk/Petra	-2

Date: Thursday, April 19, 2012 Sheet 56 of 103

IVB

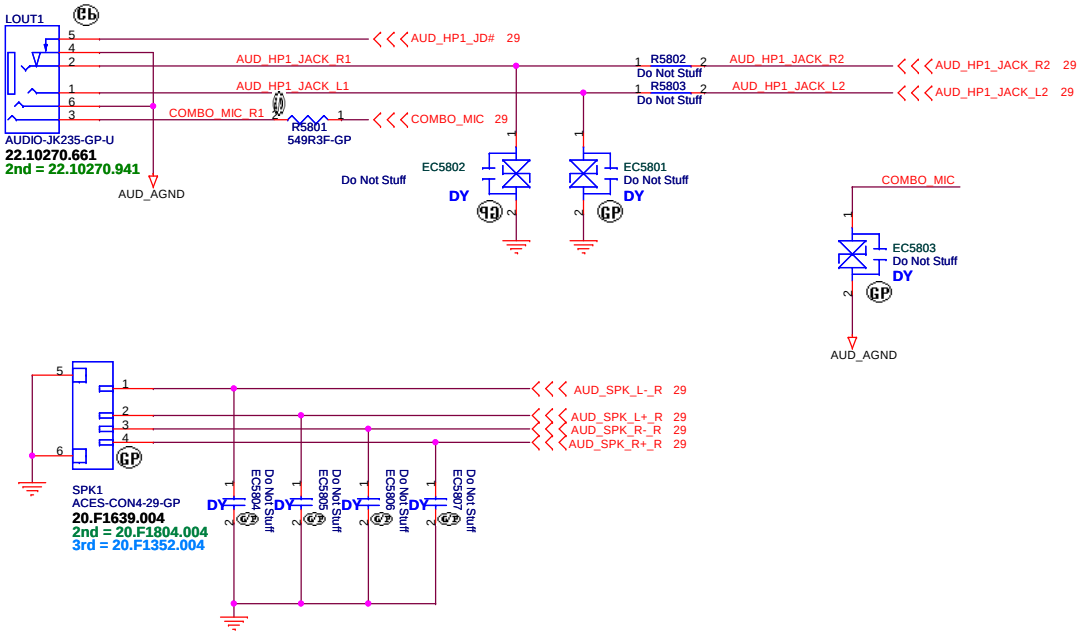
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***E-SATA/USB CHARGER***

Size	Document Number	Rev
A3	**Husk/Petra**	**-2**

Date: Thursday, April 19, 2012 Sheet 57 of 103

SSID = AUDIO



IVB

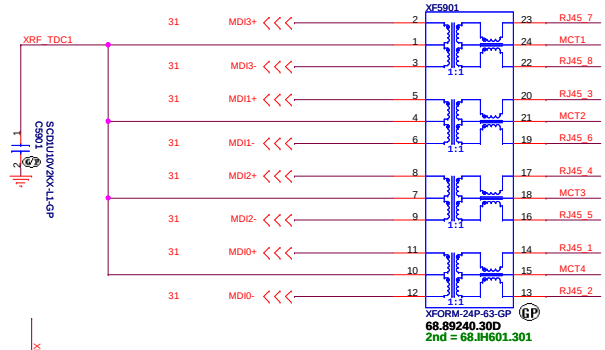
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

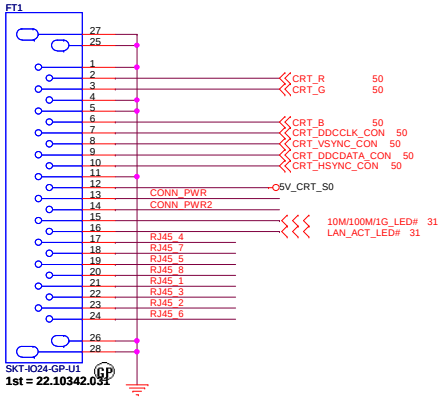
Title: ***Audio Jack***

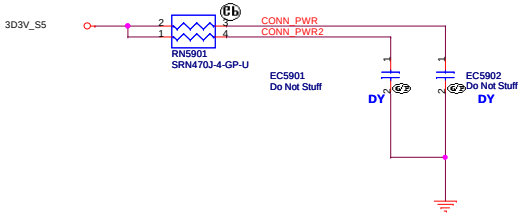
Size	Document Number	Rev
A3	Husk/Petra	-2

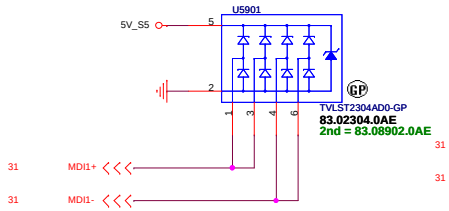
Date: Thursday, April 19, 2012 Sheet 58 of 103

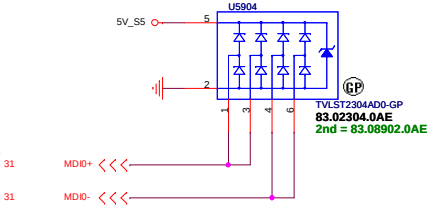
SSID = LAN

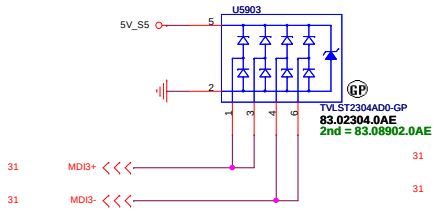


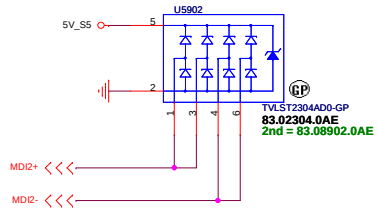


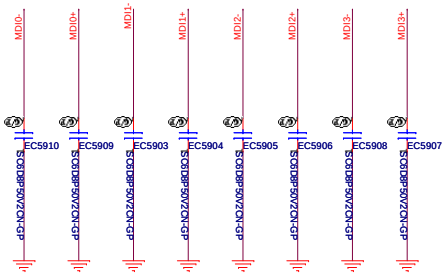


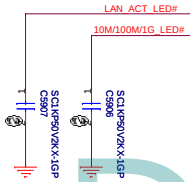


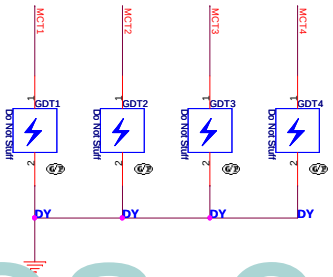


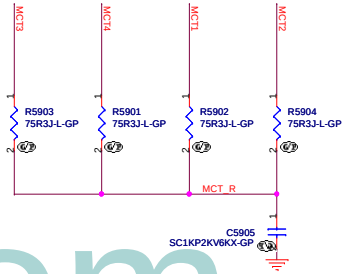












IVB

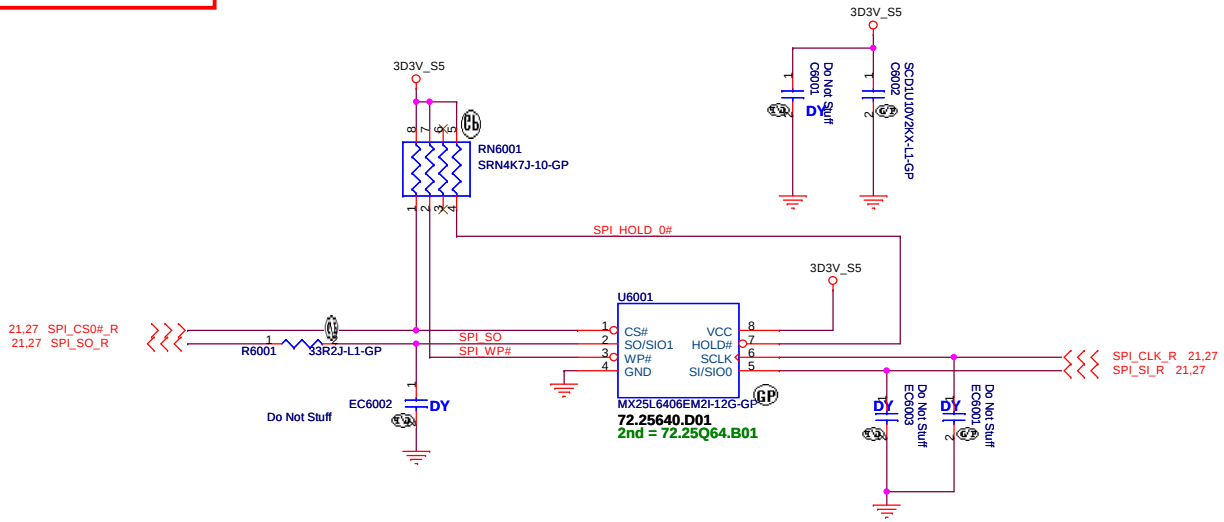
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN CONNECTOR**

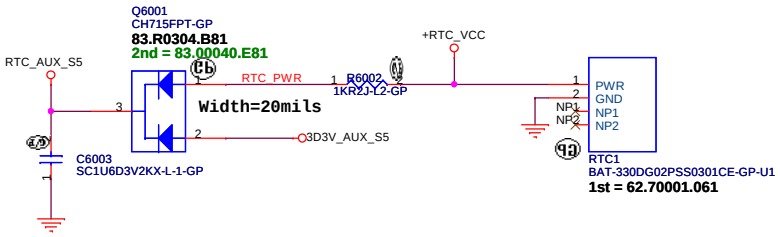
Size: Custom | Document Number: Husk/Petra | Rev: -2

Date: Monday, November 12, 2012 | Sheet 59 of 103

SSID = Flash.ROM



SSID = RTC



IVB

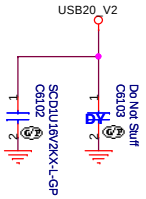
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

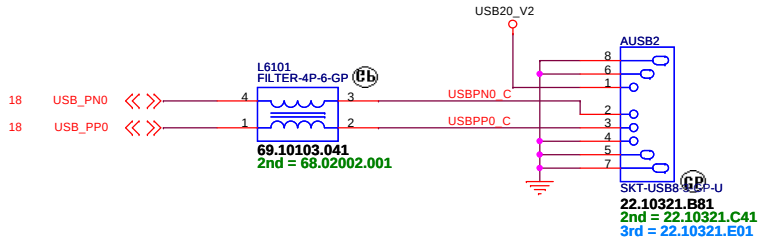
Title: ***Flash/RTC***

Size	Document Number	Rev
Custom	**Husk/Petra**	**-2**

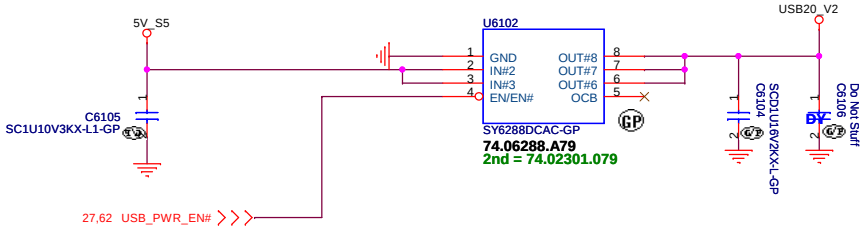
Date: Monday, June 11, 2012 Sheet 60 of 103

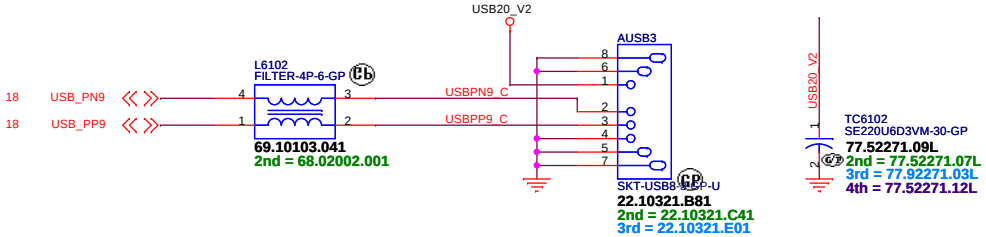
SSID = USB





Low Active 2A





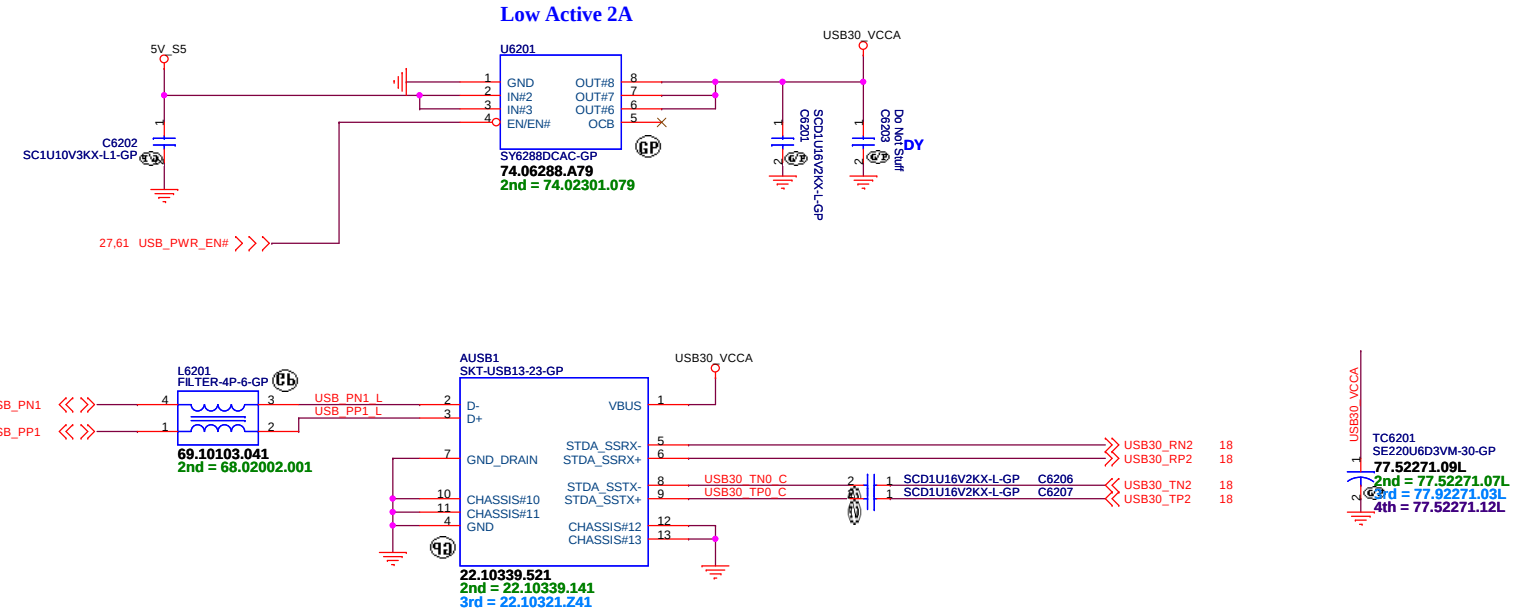
IVB

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB Power SW***

Size	Document Number	Rev
A3	Husk/Petra	-2

Date: Thursday, September 13, 2012 Sheet 61 of 103



USB 3.0 Connector Pin definition		
1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	

IVB

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB 3.0 Port

Size: A3 | Document Number: Husk/Petra | Rev: -2

Date: Thursday, September 13, 2012 | Sheet 62 of 103

SSID = User.Interface

Bluetooth Module conn.

ANNIE Bluetooth Module

IVB

緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Bluetooth***

Size	Document Number	Rev
A4	Husk/Petra	-2

Date: Thursday, April 19, 2012 Sheet 63 of 103

IVB

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

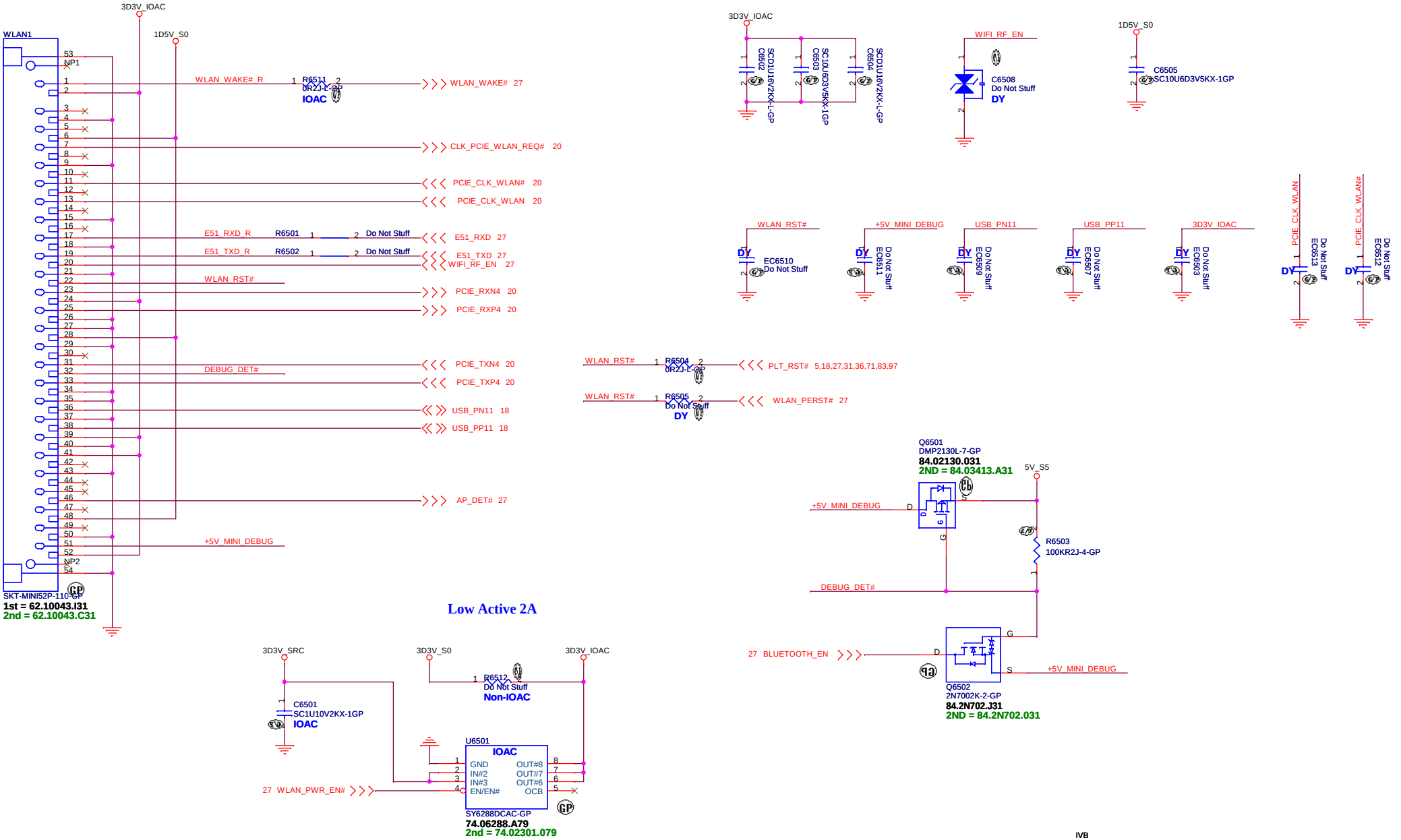
Title: ***RESERVED***

Size	Document Number	Rev
A4	**Husk/Petra**	**-2**

Date: Thursday, April 19, 2012 Sheet 64 of 103

SSID = Wireless

Mini Card Connector(802.11a/b/g/n)



IVB

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINICARD(WLAN)/ITP CONN

Size: A3 | Document Number: Husk/Petra | Rev: -2

Date: Tuesday, October 09, 2012 | Sheet 65 of 103

SSID = Wireless

Mini Card Connector(WWAN)

IVB

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: WWAN Connector

Size	Document Number	Rev
A4	Husk/Petra	-2

Date: Thursday, April 19, 2012 Sheet 66 of 103

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IVB

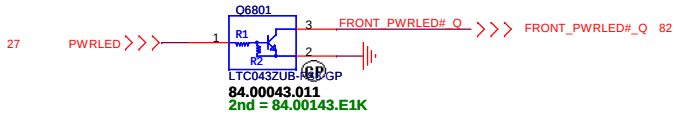
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

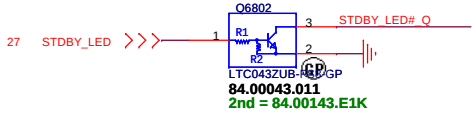
Size	Document Number	Rev
A4	Husk/Petra	-2

Date: Thursday, April 19, 2012 Sheet 67 of 103

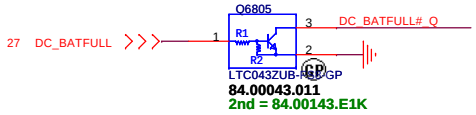
Power button LED



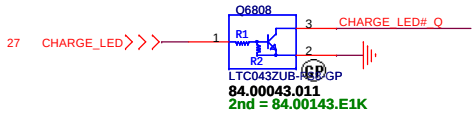
Power STDBY_LED

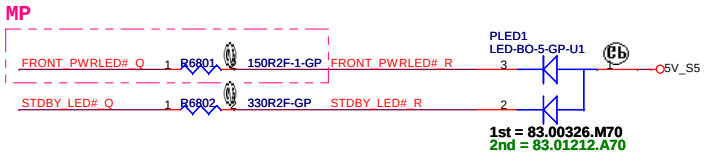


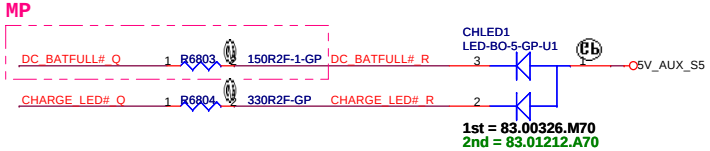
Battery LED2(DC_BATFULL)

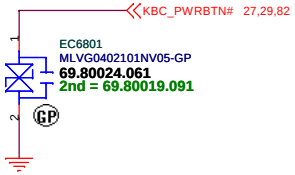


Battery LED1(CHARGE)







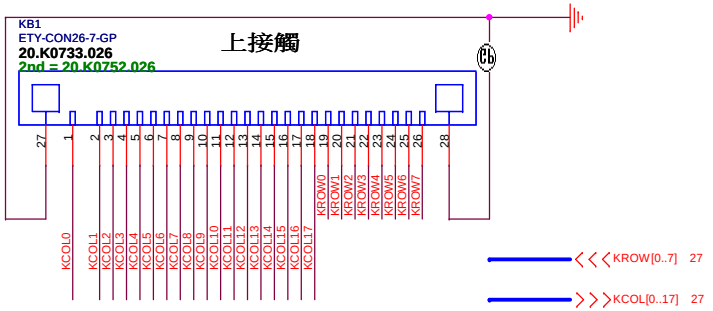


IVB

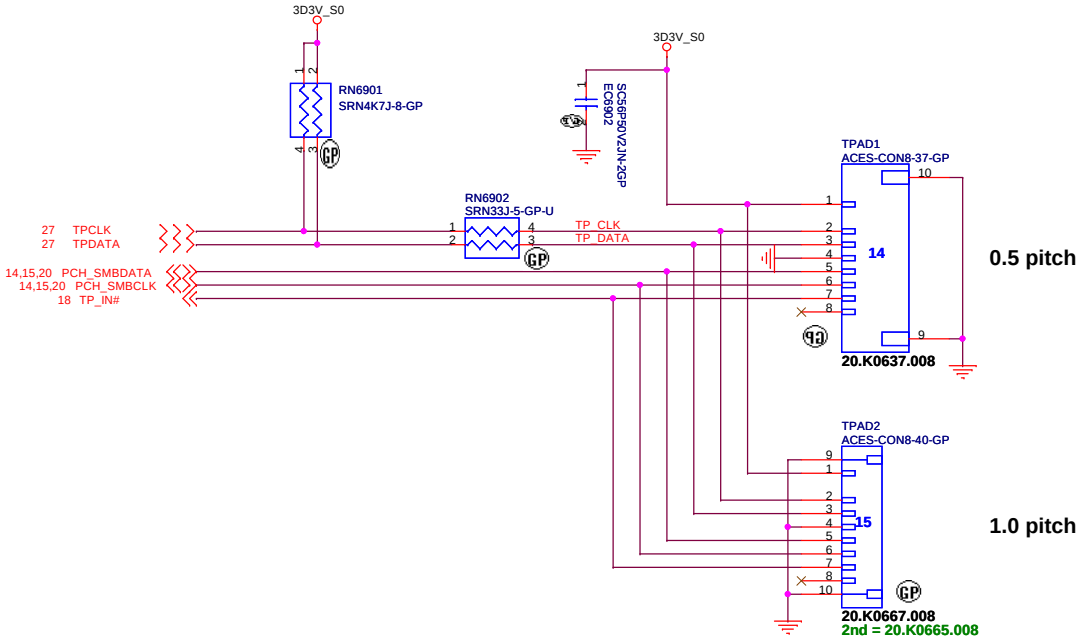
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *LED Bard/Power Button*		
Size: Custom	Document Number: Husk/Petra	Rev: -2
Date: Tuesday, October 09, 2012	Sheet 68 of 103	

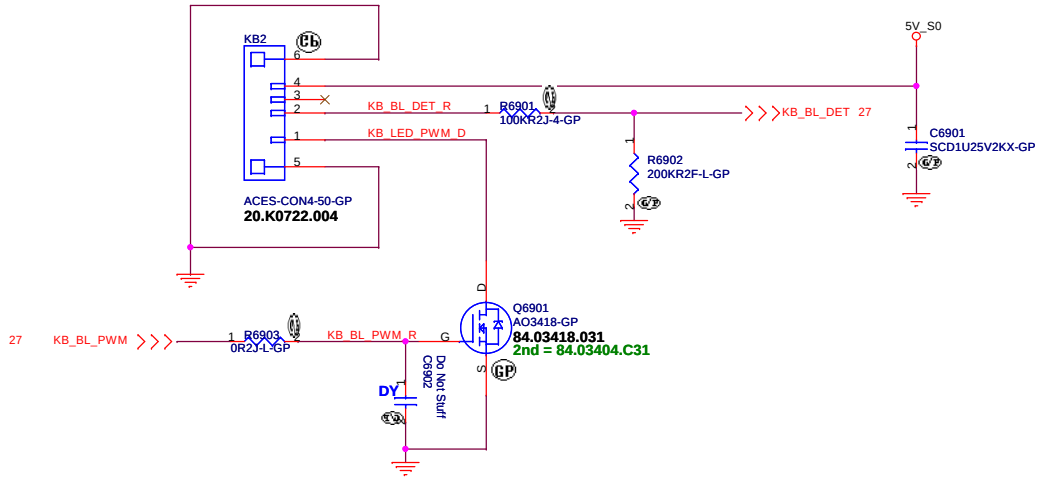
SSID = KBC

Internal KeyBoard Connector



TOUCH PAD





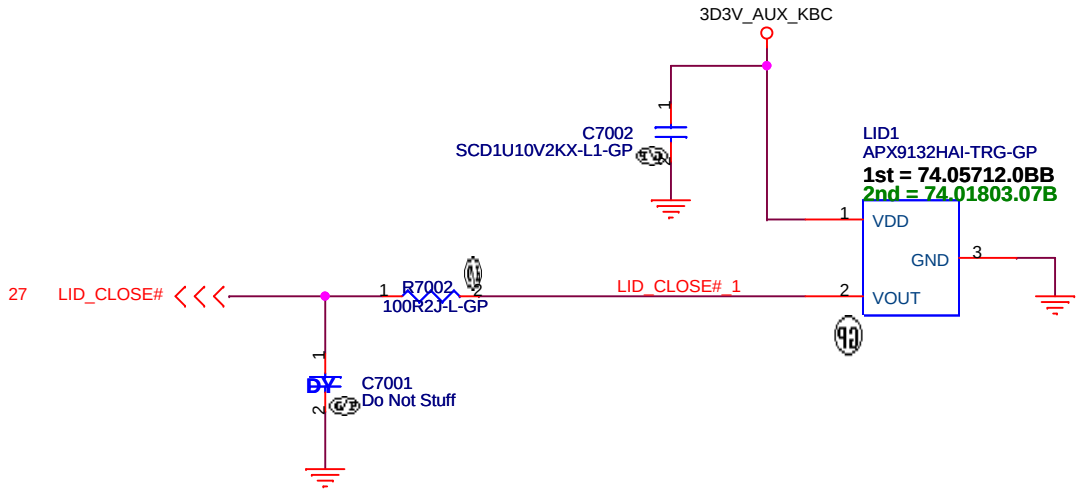
IVB

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Key Board/Touch Pad***

Size	Document Number	Rev
A3	Husk/Petra	-2

Date: Wednesday, May 09, 2012 Sheet 69 of 103



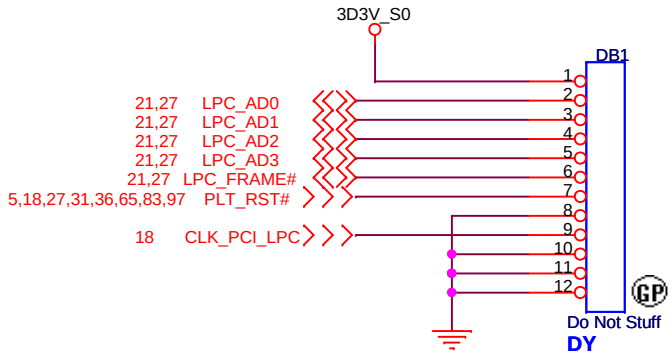
IVB

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Hall Sensor***

Size	Document Number	Rev
A4	Husk/Petra	-2

Date: Thursday, April 19, 2012 Sheet 70 of 103



IVB

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Dubug connector***

Size	Document Number	Rev
A4	**Husk/Petra**	**-2**

Date: Thursday, April 19, 2012 Sheet 71 of 103

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IVB

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: Husk/Petra | Rev: -2

Date: Thursday, April 19, 2012 | Sheet 72 of 103

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IVB

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

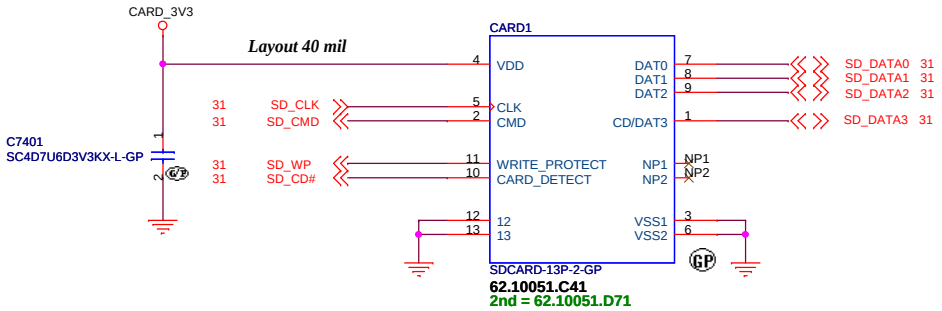
Title: *Reserved*

Size: A3 | Document Number: Husk/Petra | Rev: -2

Date: Thursday, April 19, 2012 | Sheet 73 of 103

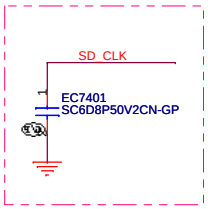
SSID = SDIO

SD/MMC Card Reader



SP1	SP1	SD_D7		xD_RDY
SP2	SP2	SD_D6	MS_INS#	xD_RE#
SP3	SP3	SD_D5		xD_CE#
SP4	SP4	SD_D4		xD_WE#
SP5	SP5	SD_D1	MS_CLK	xD_D6
SP6	SP6	SD_D0	MS_D7	xD_D5
SP7	SP7	SD_CLK	MS_D3	xD_D4
SP8	SP8	SD_CMD	MS_D6	xD_D3
SP9	SP9	SD_D3	MS_D2	xD_D2
SP10	SP10	SD_D2		xD_D7
SP11	SP11		MS_BS	xD_CLE
SP12	SP12	SD_WP	MS_D1	xD_WP#
SP13	SP13	SD_CD#	MS_D5	xD_ALE
SP14	SP14		MS_D4	xD_D0
SP15	SP15		MS_D0	xD_D1
SP16	SP16			xD_CD#

-2:EMI



IVB

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CARD Reader CONN

Size: Custom | Document Number: Husk/Petra | Rev: -2

Date: Thursday, April 19, 2012 | Sheet 74 of 103

SSID = ExpressCard

+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA

IVB

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: New Card

Size: A3 | Document Number: Husk/Petra | Rev: -2

Date: Thursday, April 19, 2012 | Sheet 75 of 103

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IVB

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	Husk/Petra	-2

Date: Thursday, April 19, 2012 Sheet 76 of 103

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IVB

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title ***Reserved***

Size	Document Number	Rev
A4	**Husk/Petra**	**-2**

Date: Thursday, April 19, 2012 Sheet 77 of 103

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IVB

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	Husk/Petra	-2

Date: Thursday, April 19, 2012 Sheet 78 of 103

SSID = User.Interface

Free Fall Sensor

Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

IVB

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***G- Sensor***

Size	Document Number	Rev
A4	Husk/Petra	-2

Date: Thursday, April 19, 2012 Sheet 79 of 103

IVB

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	**Husk/Petra**	**-2**

Date: Thursday, April 19, 2012 Sheet 80 of 103

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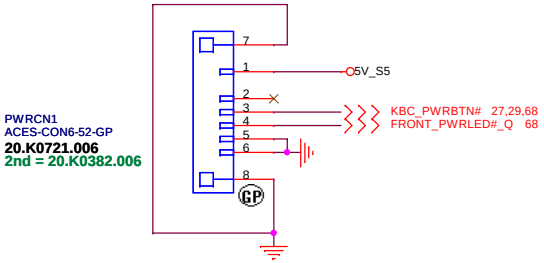
IVB

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	Husk/Petra	-2

Date: Thursday, April 19, 2012 Sheet 81 of 103



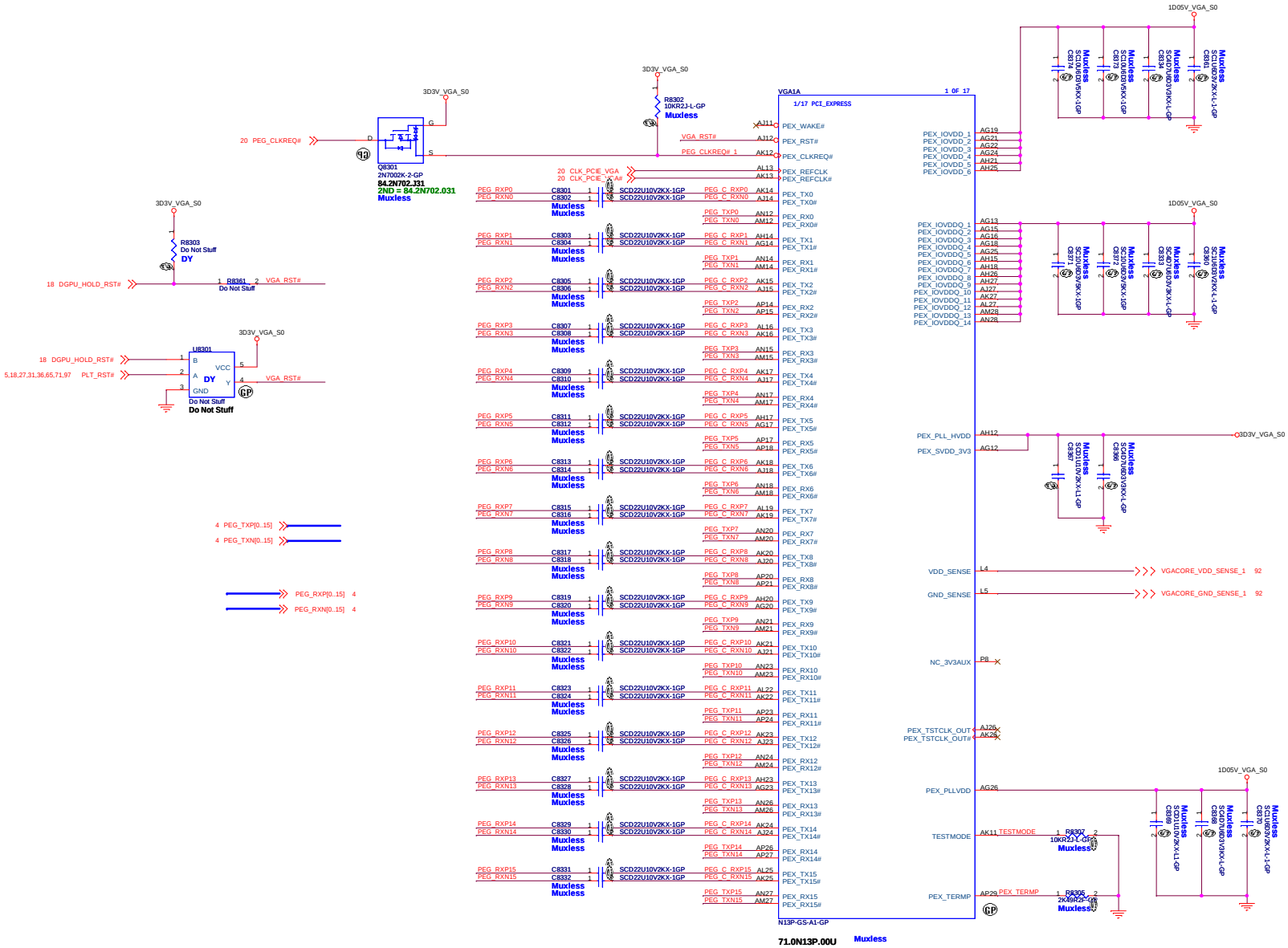
IVB

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***IO Board Connector***

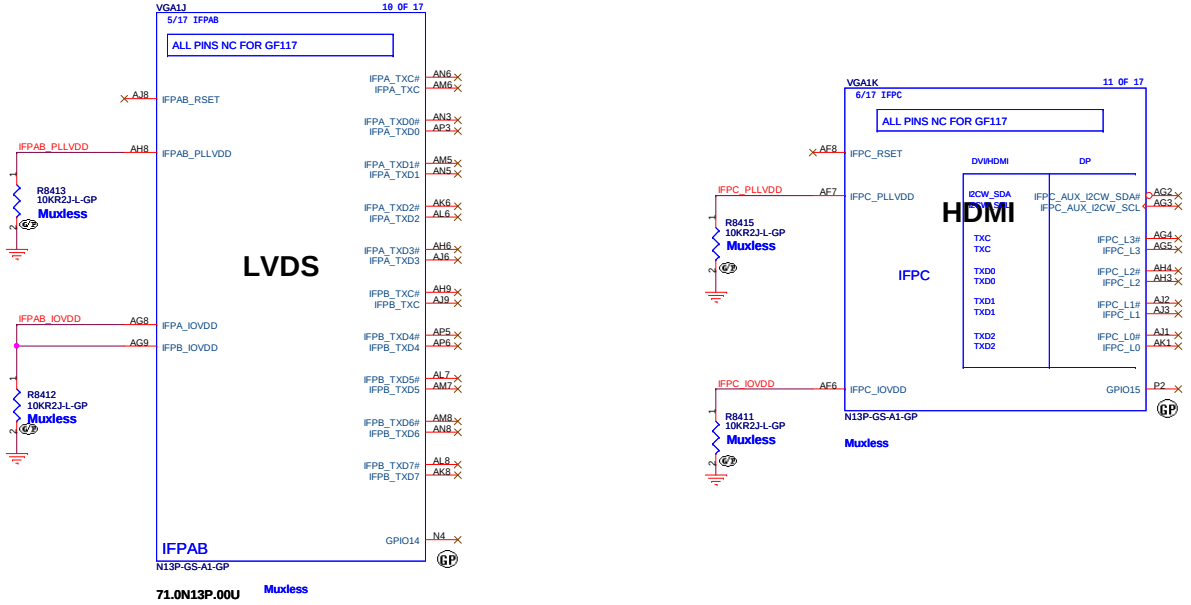
Size	Document Number	Rev
A3	Husk/Petra	-2

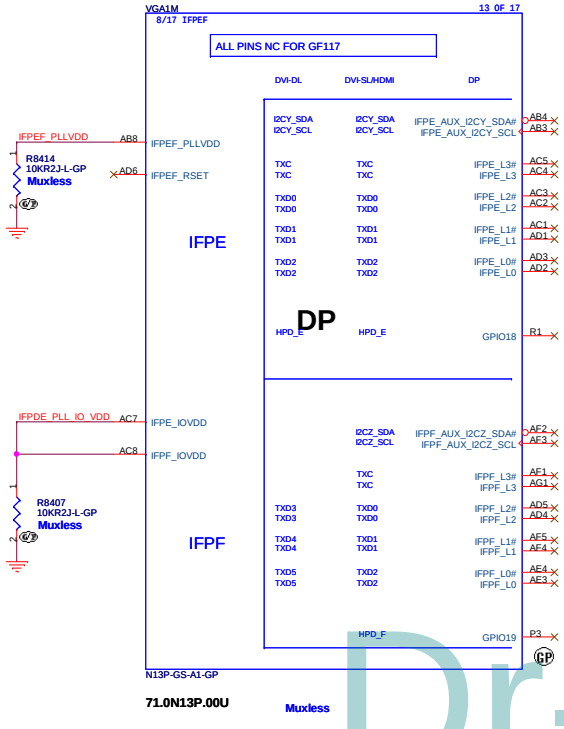
Date: Thursday, April 19, 2012 Sheet 82 of 103

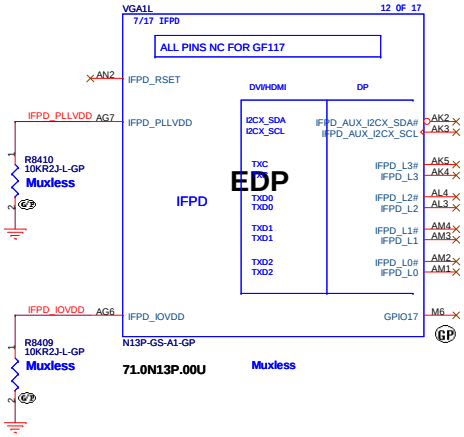


IVB

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	GPU_PCIE/STRAPPING(1/5)	
Size: A2	Document Number: Husk/Petra	Rev: -2
Date: Thursday, April 19, 2012	Sheet 83 of 103	







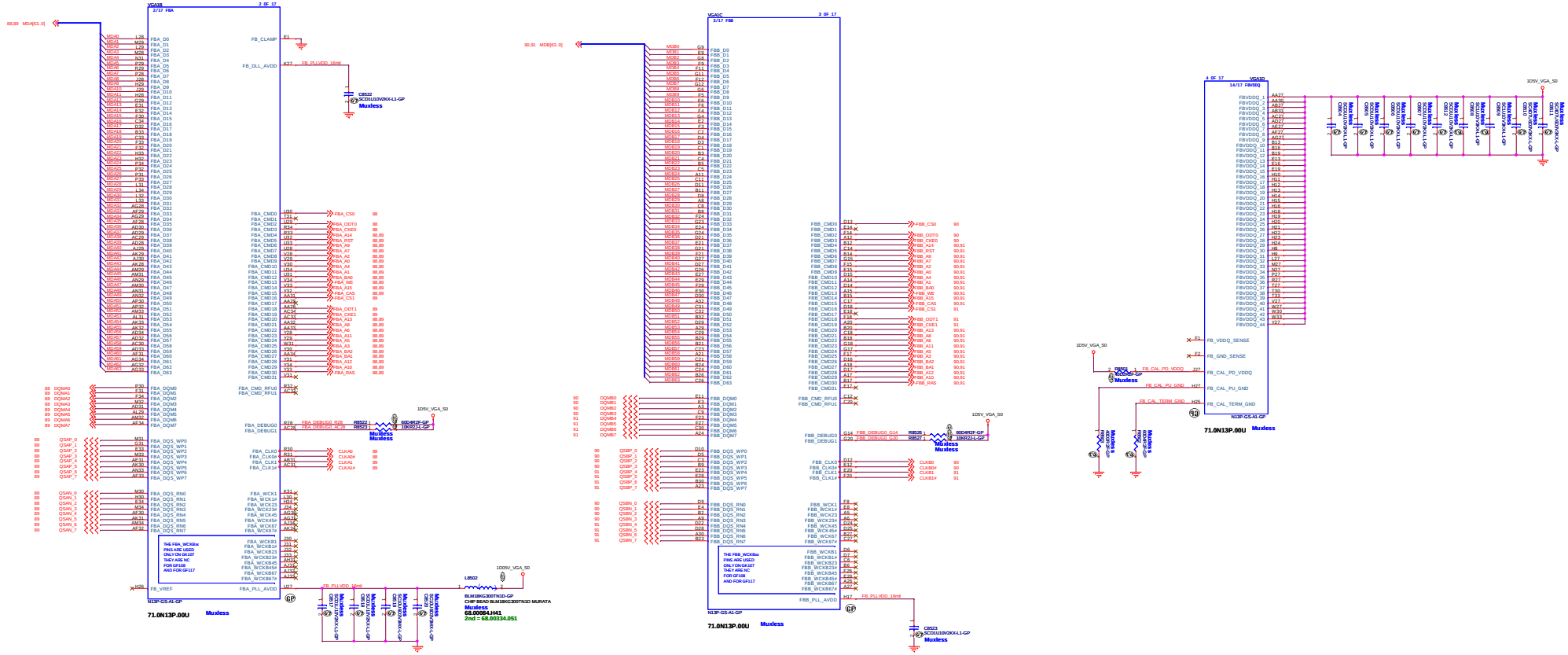
IVB

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

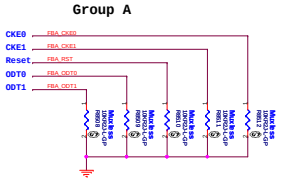
Title: ***GPU Memory(2/5)***

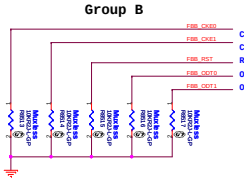
Size: Custom | Document Number: **Husk/Petra** | Rev: **-2**

Date: Thursday, April 19, 2012 | Sheet 84 of 103



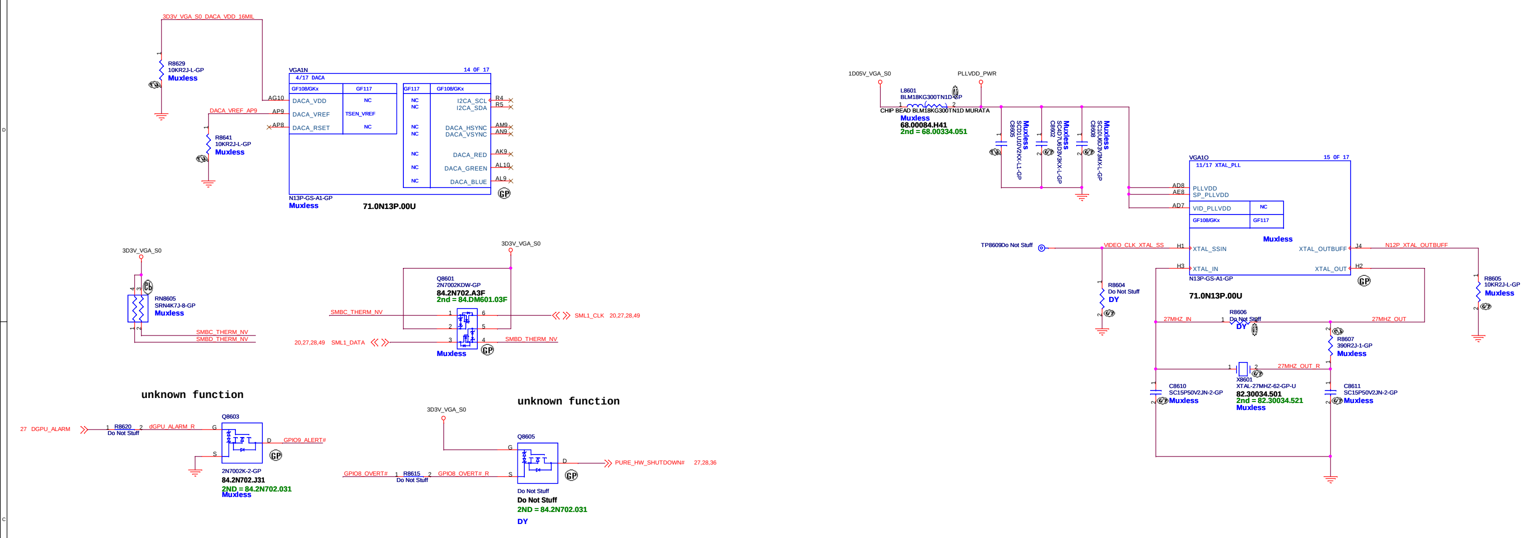
FBCLK Termination place on VRAM side

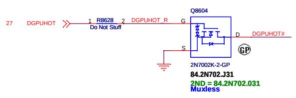




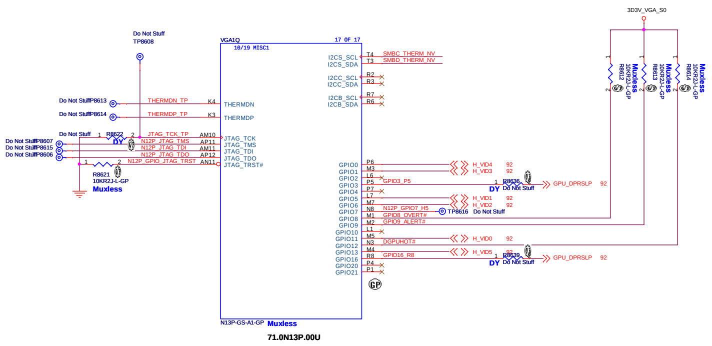
FBCLK Termination place on VRAM side

緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: GPU_DP/LVDS/CRT/GPIO(3/5)		
Size: A1	Document Number: Husk/Petra	Rev: -2
Date: Thursday, April 19, 2007	Sheet 65 of 103	





GPIO	Name	I/O	Description
GPIO8	OVERT	I/O	Active Low Thermal Catastrophic Over Temperature
GPIO9	ALERT	I/O	Active Low Thermal Alert
GPIO10	MEM_VREF_CTL	O	Memory VREF Control
GPIO11	GPU_VID0	O	GPU Core VDD VID0
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input



VRAM Table(N13P-GS/GT/LP/GL/GLP/NS/GE)

	Hynix 2G_B-Die 0110(0x6) 128*16	Hynix 1G_D-die 0010(0x2) 64*16	Samsung 2G_C-Die 0111(0x7) 128*16	Samsung 1G_G-die 0011(0x3) 64*16
ROM_SI R8627	34.8Kohm 64.34825.6DL	15Kohm 64.15025.6DL	45Kohm 64.45325.6DL	20Kohm 64.20025.6DL

5Kohm
64.49915.6DL

10Kohm
64.10025.L0L

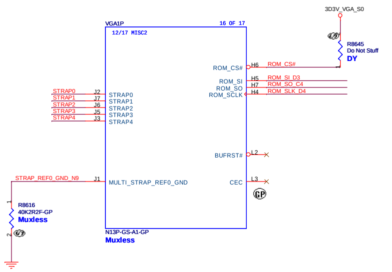
VRAM Table(N13M-GS/NS)

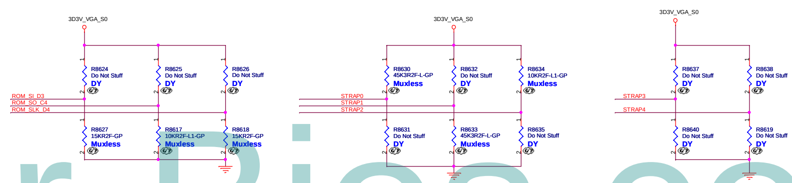
Hynix 2G_D-die 1100(0xC) 128*16	Hynix 2G_B-die 0110(0x6) 128*16

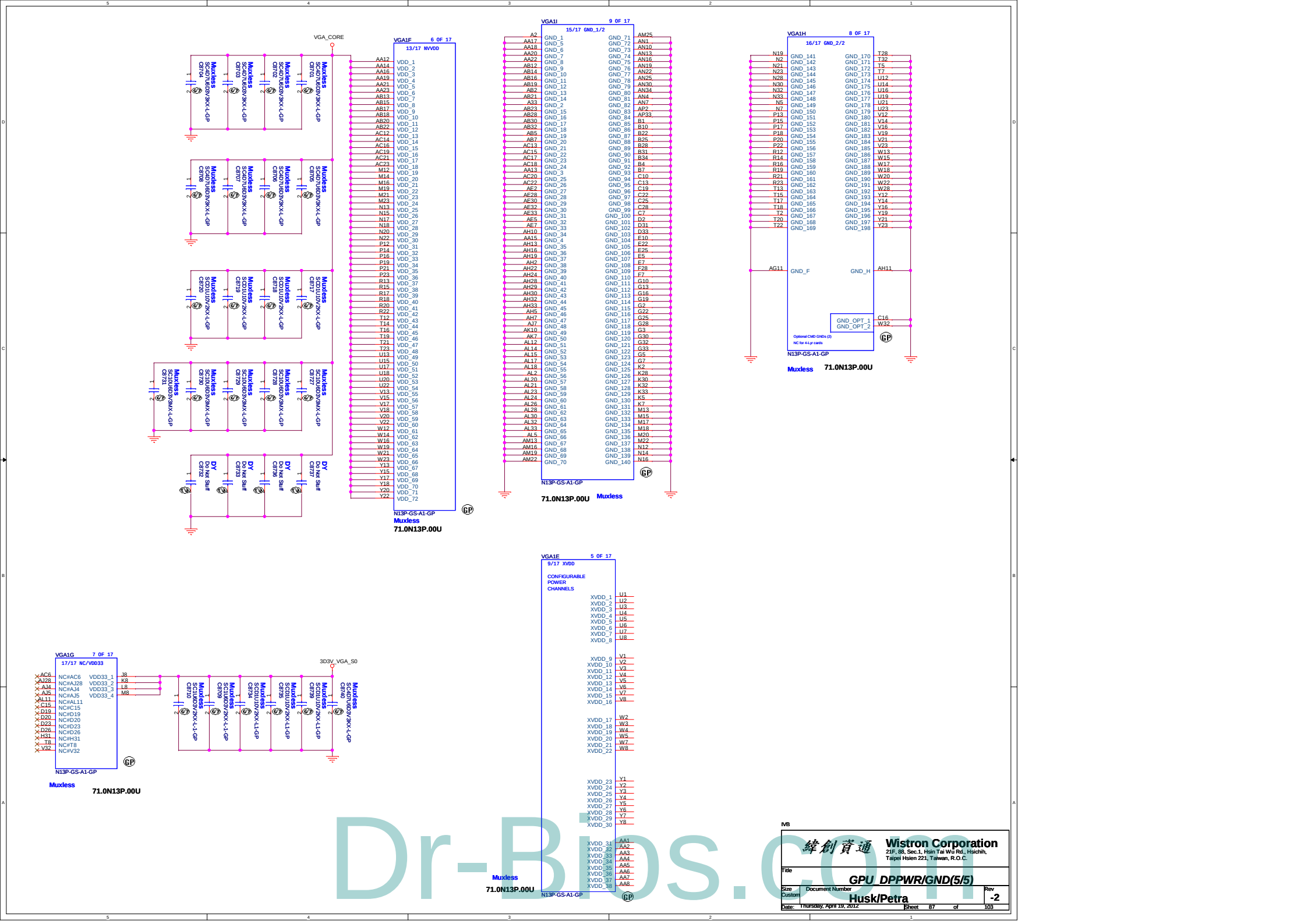
```
Logical Strap Bit Mapping
Resistor  Pull-up Pull-down
 5Kohms    1000    0000
 10Kohms   1001    0001
 15Kohms   1010    0010
 20Kohms   1011    0011
 25Kohms   1100    0100
 30Kohms   1101    0101
 35Kohms   1110    0110
 45Kohms   1111    0111
```

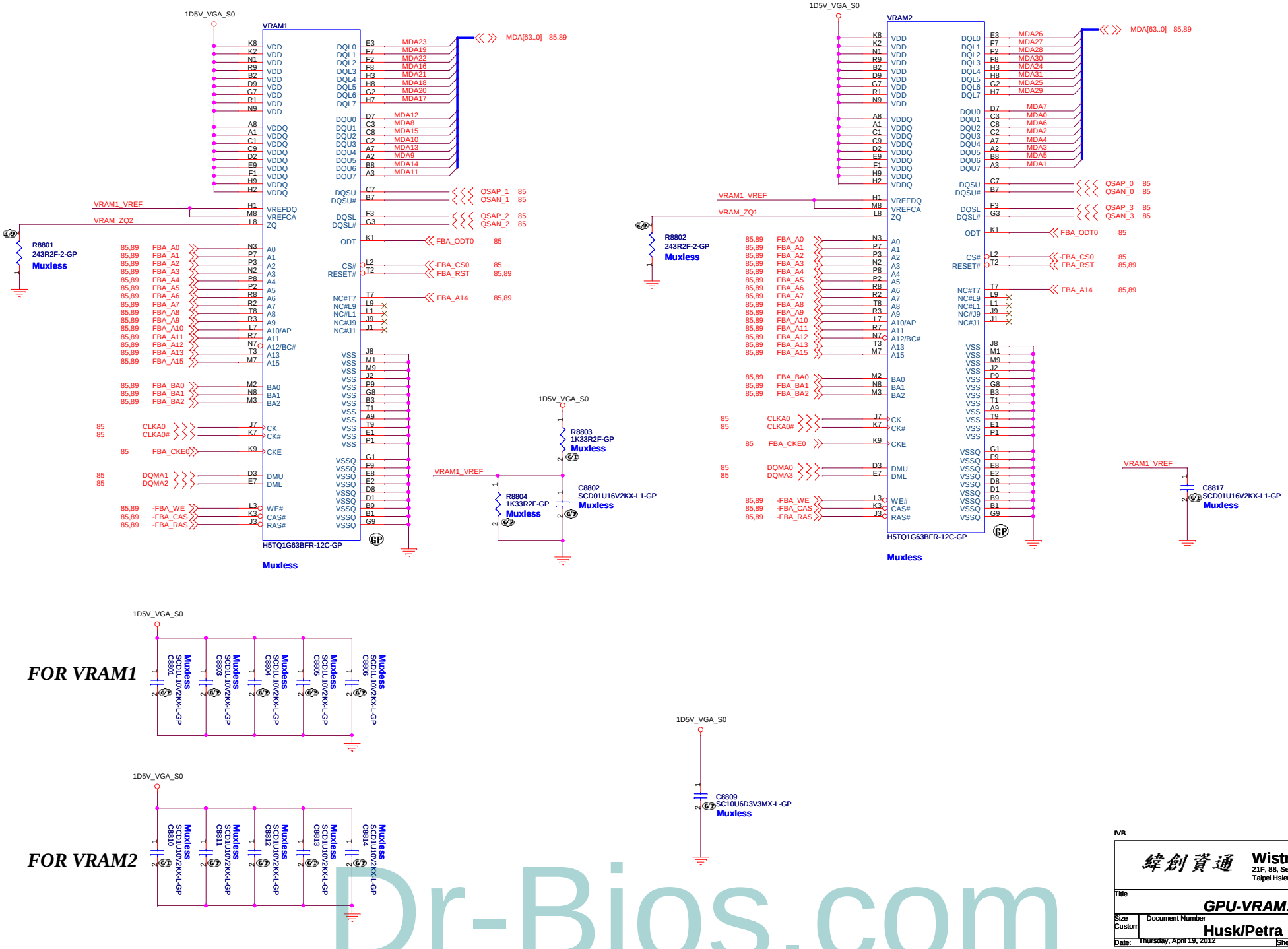
Mode	Product	NVCLK (MHz)	MCLK (MHz)	NVVDD (V)
MAX Point (MP)	N13P-GL/-NS1	800	900	–
	N13P-GLP	660	900	–
TDP Point (TP)	N13P-GL/-NS1	660	900	–
	N13P-GLP	475	900	–
HW Boot Voltage	N13P-GL/-NS1	–	–	0.95
	N13P-GLP	–	–	0.90

Strap Pin Nmae	Logical strapping name bit#3	Logical strapping name bit#2	Logical strapping name bit#1	Logical strapping name bit#0	
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG/	PEX_PLL_EN_TERM	
	0	0	1	0	15K ohm pull-down
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[2]	RAMCFG[0]	
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	
	0	0	0	1	10K ohm pull-down
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	
	1	1	1	1	45K ohm pull-up
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	
	0	1	1	1	45K ohm pull-down
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	
	1	0	0	1	10K ohm pull-up
STRAP3	N/A	N/A	N/A	N/A	
STRAP4	N/A	N/A	N/A	N/A	






VGA_CORE
VGA1F 6 OF 17
13/17 NVVDD
VDD_1 VDD_2 VDD_3 VDD_4 VDD_5 VDD_6 VDD_7 VDD_8 VDD_9 VDD_10 VDD_11 VDD_12 VDD_13 VDD_14 VDD_15 VDD_16 VDD_17 VDD_18 VDD_19 VDD_20 VDD_21 VDD_22 VDD_23 VDD_24 VDD_25 VDD_26 VDD_27 VDD_28 VDD_29 VDD_30 VDD_31 VDD_32 VDD_33 VDD_34 VDD_35 VDD_36 VDD_37 VDD_38 VDD_39 VDD_40 VDD_41 VDD_42 VDD_43 VDD_44 VDD_45 VDD_46 VDD_47 VDD_48 VDD_49 VDD_50 VDD_51 VDD_52 VDD_53 VDD_54 VDD_55 VDD_56 VDD_57 VDD_58 VDD_59 VDD_60 VDD_61 VDD_62 VDD_63 VDD_64 VDD_65 VDD_66 VDD_67 VDD_68 VDD_69 VDD_70 VDD_71 VDD_72
N13P-GS-A1-GP
Muxless
71.0N13P.00U
VGA1I 9 OF 17
15/17 GND_1/2
GND_1 GND_5 GND_6 GND_7 GND_8 GND_9 GND_10 GND_11 GND_12 GND_13 GND_14 GND_2 GND_15 GND_16 GND_17 GND_18 GND_19 GND_20 GND_21 GND_22 GND_23 GND_24 GND_3 GND_25 GND_26 GND_27 GND_28 GND_29 GND_30 GND_31 GND_32 GND_33 GND_34 GND_4 GND_35 GND_36 GND_37 GND_38 GND_39 GND_40 GND_41 GND_42 GND_43 GND_44 GND_45 GND_46 GND_47 GND_48 GND_49 GND_50 GND_51 GND_52 GND_53 GND_54 GND_55 GND_56 GND_57 GND_58 GND_59 GND_60 GND_61 GND_62 GND_63 GND_64 GND_65 GND_66 GND_67 GND_68 GND_69 GND_70
GND_71 GND_72 GND_73 GND_74 GND_75 GND_76 GND_77 GND_78 GND_79 GND_80 GND_81 GND_82 GND_83 GND_84 GND_85 GND_86 GND_87 GND_88 GND_89 GND_90 GND_91 GND_92 GND_93 GND_94 GND_95 GND_96 GND_97 GND_98 GND_99 GND_100 GND_101 GND_102 GND_103 GND_104 GND_105 GND_106 GND_107 GND_108 GND_109 GND_110 GND_111 GND_112 GND_113 GND_114 GND_115 GND_116 GND_117 GND_118 GND_119 GND_120 GND_121 GND_122 GND_123 GND_124 GND_125 GND_126 GND_127 GND_128 GND_129 GND_130 GND_131 GND_132 GND_133 GND_134 GND_135 GND_136 GND_137 GND_138 GND_139 GND_140
N13P-GS-A1-GP
71.0N13P.00U
Muxless
VGA1H 8 OF 17
16/17 GND_2/2
GND_141 GND_142 GND_143 GND_144 GND_145 GND_146 GND_147 GND_148 GND_149 GND_150 GND_151 GND_152 GND_153 GND_154 GND_155 GND_156 GND_157 GND_158 GND_159 GND_160 GND_161 GND_162 GND_163 GND_164 GND_165 GND_166 GND_167 GND_168 GND_169
GND_170 GND_171 GND_172 GND_173 GND_174 GND_175 GND_176 GND_177 GND_178 GND_179 GND_180 GND_181 GND_182 GND_183 GND_184 GND_185 GND_186 GND_187 GND_188 GND_189 GND_190 GND_191 GND_192 GND_193 GND_194 GND_195 GND_196 GND_197 GND_198
GND_F
GND_H
GND_OPT_1
GND_OPT_2
Optional CMD GNDs (2)
NC for 4-Ly cards
N13P-GS-A1-GP
Muxless
71.0N13P.00U
VGA1G 7 OF 17
17/17 NC/VDD33
NC#AC6 NC#AJ28 NC#AJ4 NC#AJ5 NC#L11 NC#AL11 NC#C15 NC#D19 NC#D20 NC#D23 NC#D26 NC#H31 NC#T8 NC#V32
VDD33_1 VDD33_2 VDD33_3 VDD33_4
J8 K8 L8 M8
3D3V_VGA_S0
N13P-GS-A1-GP
Muxless
71.0N13P.00U
VGA1E 5 OF 17
9/17 XVDD
CONFIGURABLE POWER CHANNELS
XVDD_1 XVDD_2 XVDD_3 XVDD_4 XVDD_5 XVDD_6 XVDD_7 XVDD_8
XVDD_9 XVDD_10 XVDD_11 XVDD_12 XVDD_13 XVDD_14 XVDD_15 XVDD_16
XVDD_17 XVDD_18 XVDD_19 XVDD_20 XVDD_21 XVDD_22
XVDD_23 XVDD_24 XVDD_25 XVDD_26 XVDD_27 XVDD_28 XVDD_29 XVDD_30
XVDD_31 XVDD_32 XVDD_33 XVDD_34 XVDD_35 XVDD_36 XVDD_37 XVDD_38
N13P-GS-A1-GP
Muxless
71.0N13P.00U
IVB
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
GPU_DPPWR/GND(5/5)
Size Custom
Document Number
Husk/Petra
Rev -2
Date: Thursday, April 19, 2012
Sheet 87 of 103



FOR VRAM1

FOR VRAM2

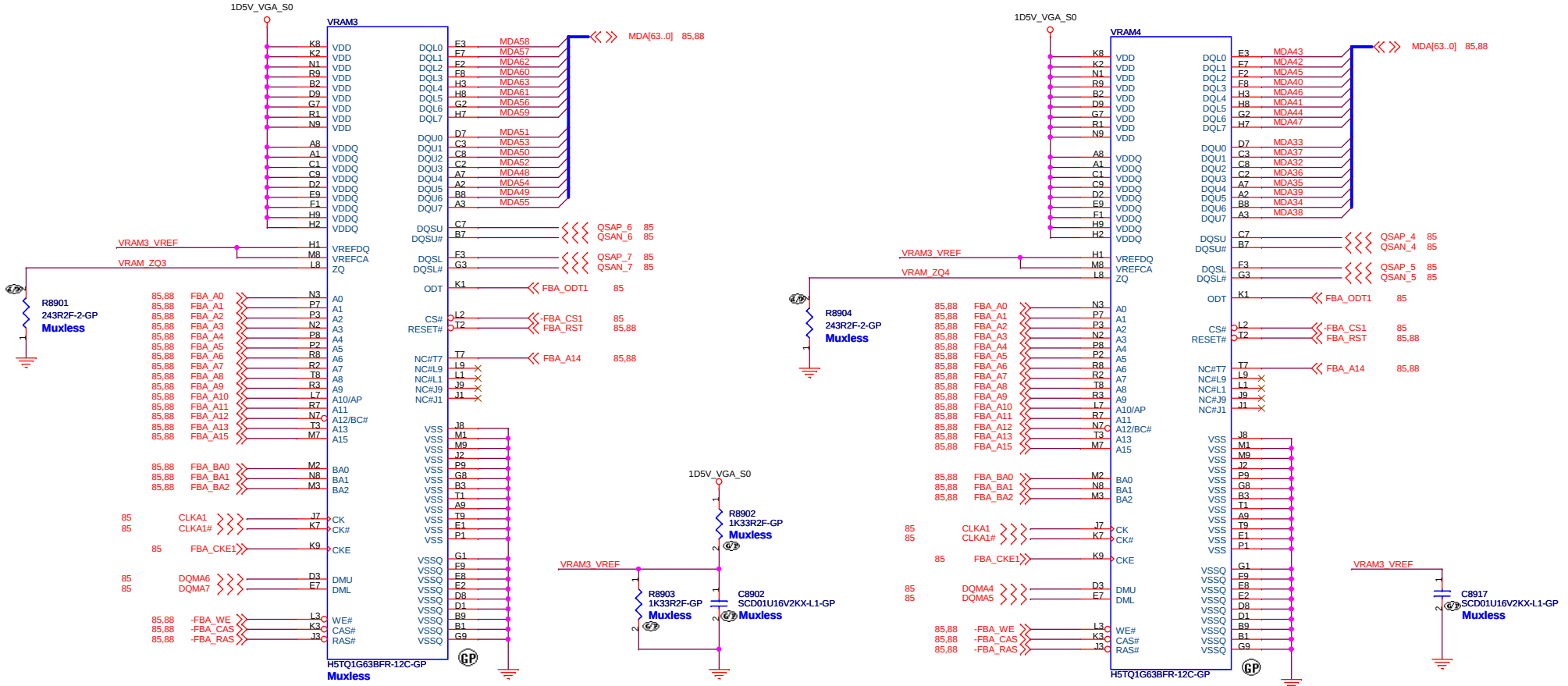
IVB

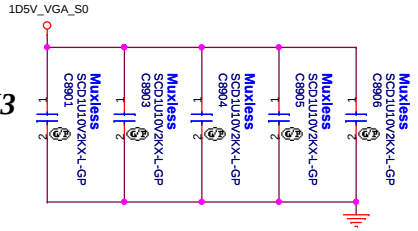
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GPU-VRAM1,2 (1/4)***

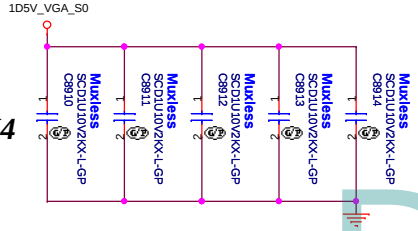
Size	Document Number	Rev
Custom	**Husk/Petra**	-2

Date: Thursday, April 19, 2012 Sheet 88 of 103

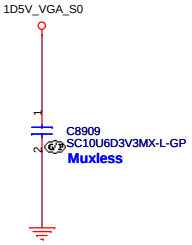




FOR VRAM3

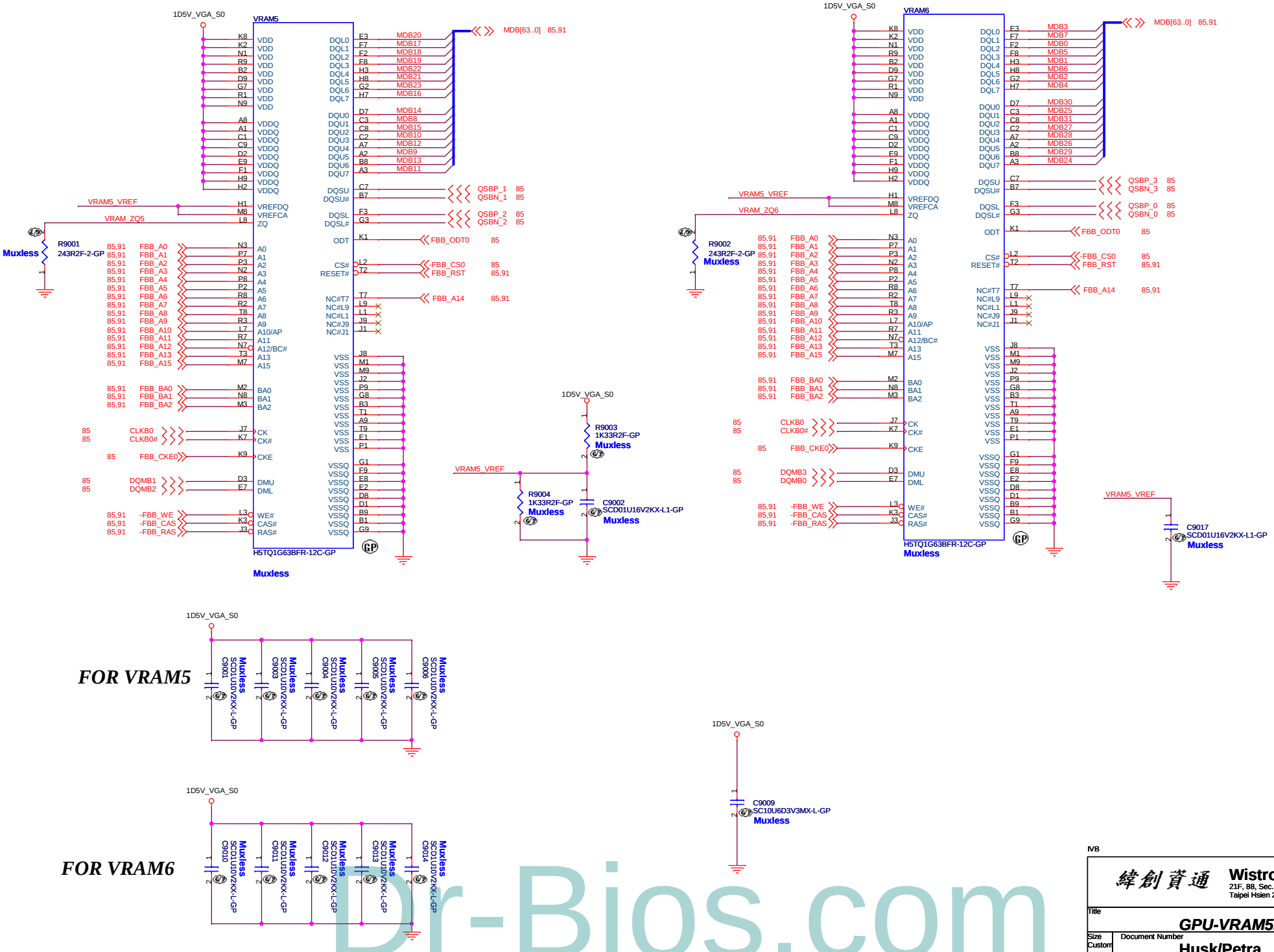


FOR VRAM4



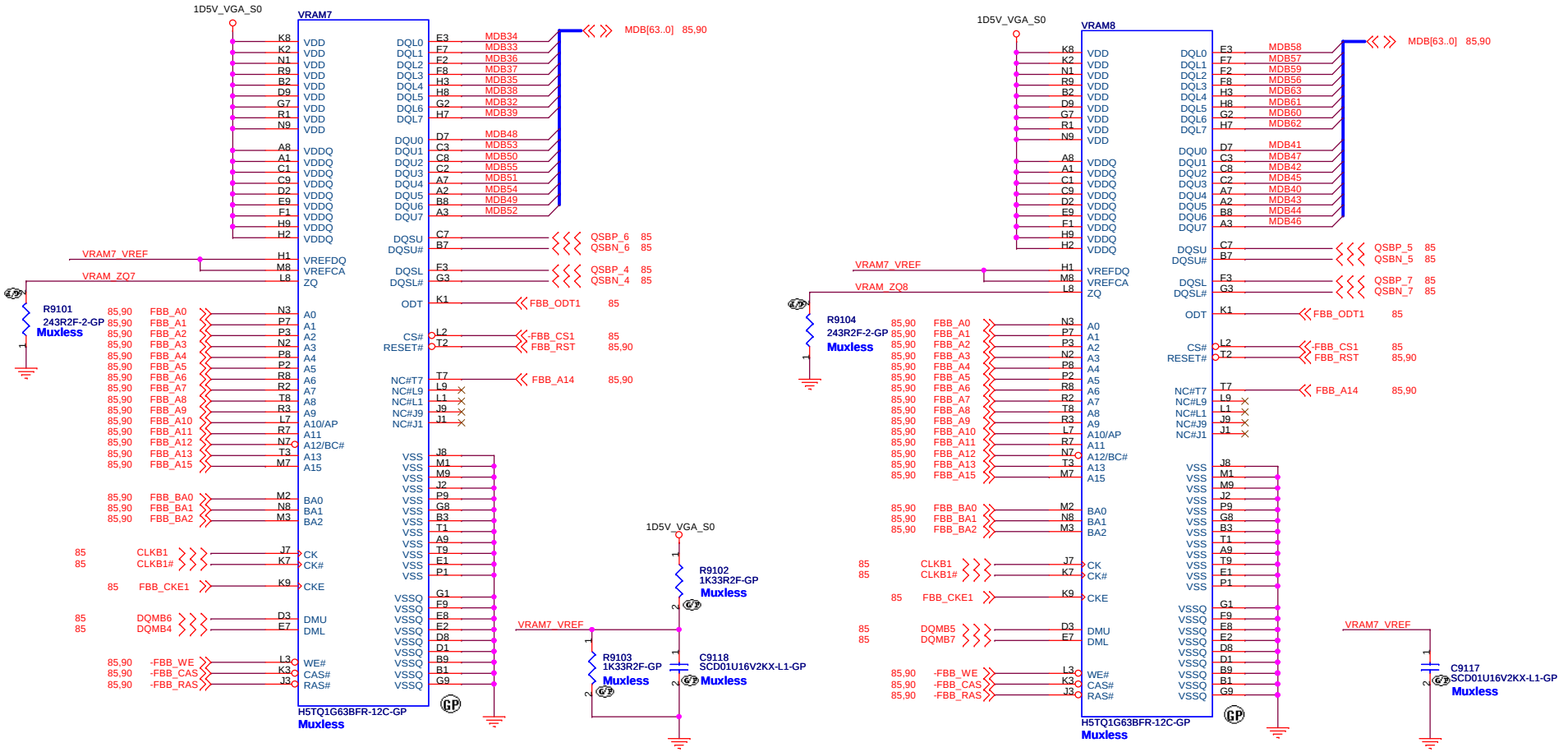
IVB

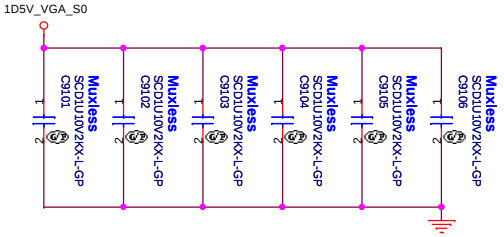
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: **GPU-VRAM3,4 (2/4)**		
Size: Custom	Document Number: **Husk/Petra**	Rev: **-2**
Date: Thursday, April 19, 2012	Sheet 89 of 103	



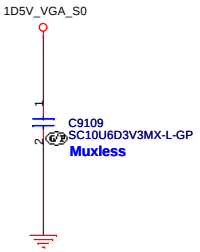
IVB

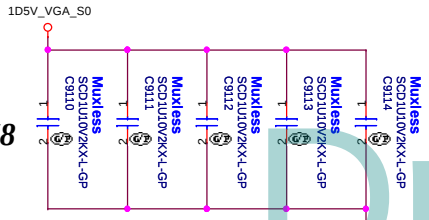
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***GPU-VRAM5,6 (3/4)***
Size: Custom	Document Number: **Husk/Petra**
Rev	**-2**
Date: Thursday, April 19, 2012	Sheet 90 of 103





FOR VRAM7





FOR VRAM8

IVB

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GPU-VRAM7,8 (4/4)***

Size	Document Number	Rev
Custom	Husk/Petra	-2

Date: Thursday, April 19, 2012 Sheet 91 of 103

SSID = PWR.Plane.Regulator_GFX

		N13P-GS-LP 71.0N13P.00U	N13P-GL 71.0N13P.B0U	N13M-GS 71.0N13M.E0U
NVVDD Boot Voltage		0.9V VID[6:0]=0110000	0.95V VID[6:0]=0101100	0.875V VID[6:0]0110010
NV_VID1	PR9215	DY	DY	63.10334.L0L
	PR9230	63.10334.L0L	63.10334.L0L	DY
NV_VID3	PR9217	DY	63.10334.L0L	DY
	PR9232	63.10334.L0L	DY	63.10334.L0L
NV_VID4	PR9218	63.10334.L0L	DY	63.10334.L0L
	PR9233	DY	63.10334.L0L	DY

PR9218 Mount , PR9233 DY For N13M-GS Vboot = 0.875V

Change power source Net
Wayler 12/07

1 phase change 0ohm

Panasonic. 0.36uH 10*11.5*4
DCR=1.1mohm
Idc=17A, Isat=24A

Vga_core
Iccmax=24A
OCP>40A

Panasonic. 0.36uH 10*11.5*4
DCR=1.1mohm
Idc=17A, Isat=24A

1phase PR9261 mount
2phase PR9261 DY

1phase PR9259 , PR9260 mount
2phase PR9259 , PR9260 DY

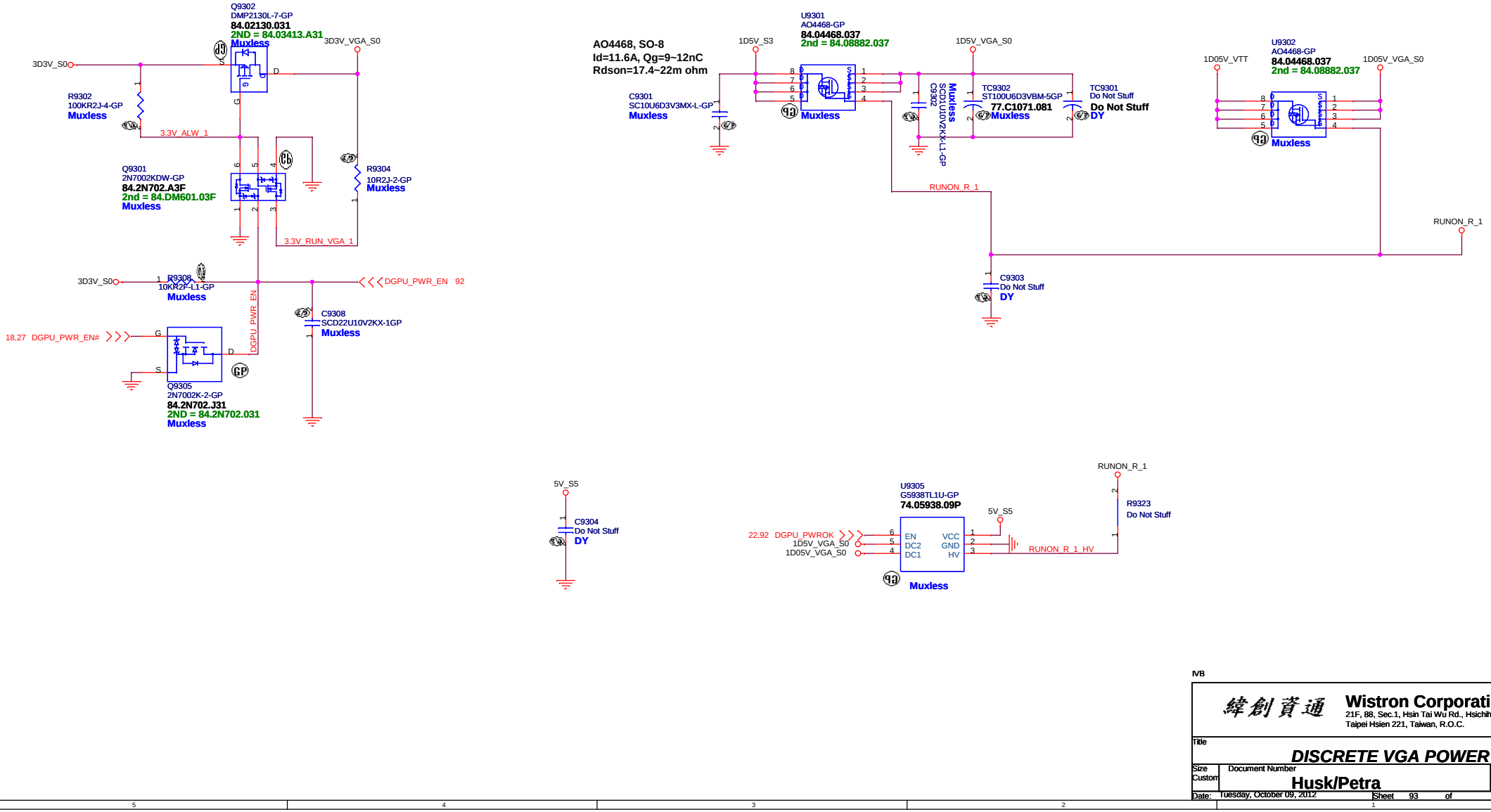
IVB

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51728_VGA_CORE

Size | Document Number: Husk/Petra | Rev: -2

Date: Tuesday, May 08, 2012 | Sheet 92 of 103



IVB

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	DISCRETE VGA POWER	
Size: Custom	Document Number: Husk/Petra	Rev: -2
Date: Tuesday, October 09, 2012	Sheet 93 of 103	

IVB

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***LVDS_Switch***

Size	Document Number	Rev
A4	**Husk/Petra**	**-2**

Date: Thursday, April 19, 2012 Sheet 94 of 103

IVB

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CRT_Switch***

Size: A3 | Document Number: **Husk/Petra** | Rev: **-2**

Date: Thursday, April 19, 2012 | Sheet 95 of 103

SSID = SDIO

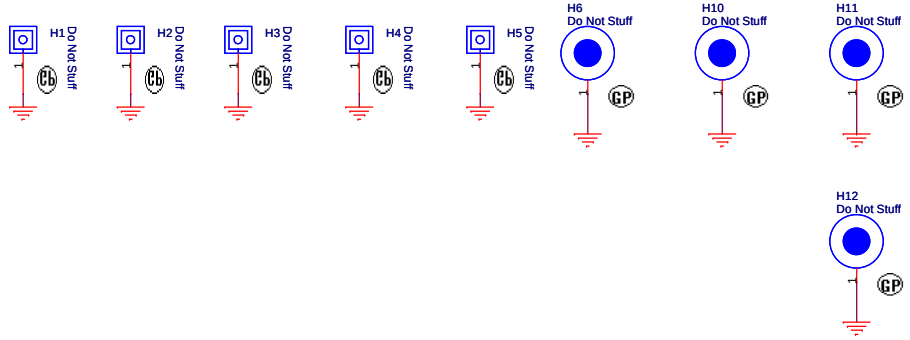
IVB

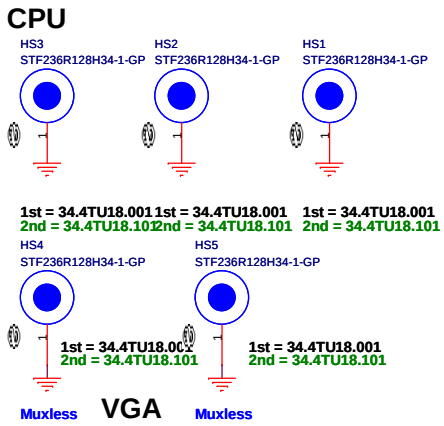
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

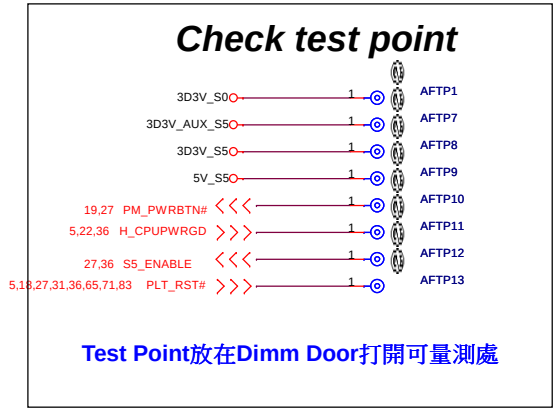
Title: ***TOUCH PANEL***

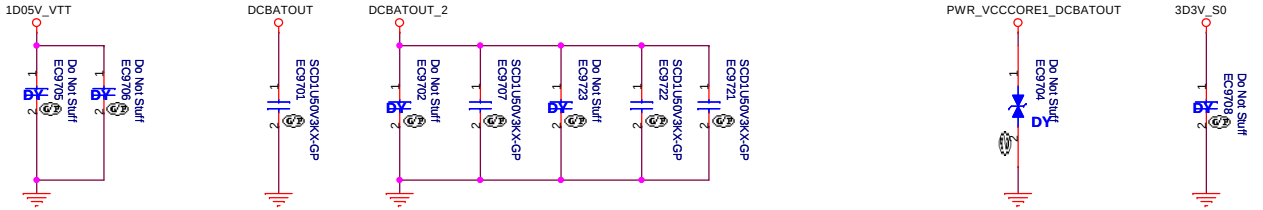
Size	Document Number	Rev
A2	Husk/Petra	-2

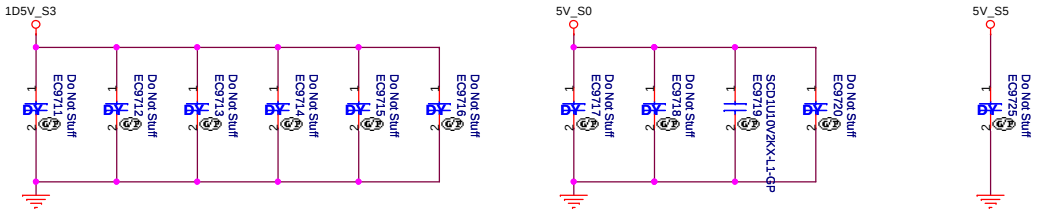
Date: Thursday, April 19, 2012 Sheet 96 of 103

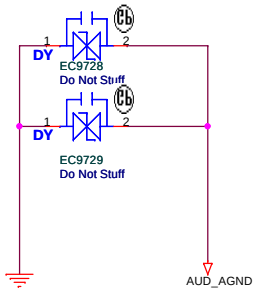


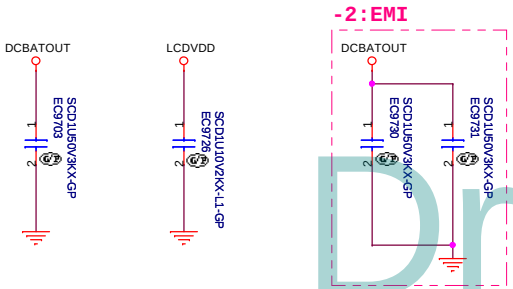












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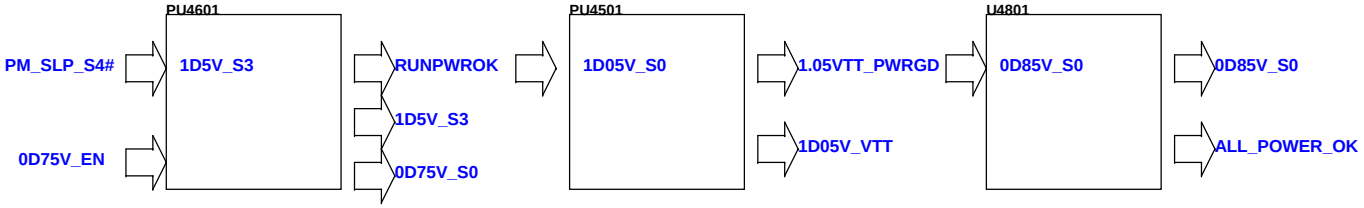
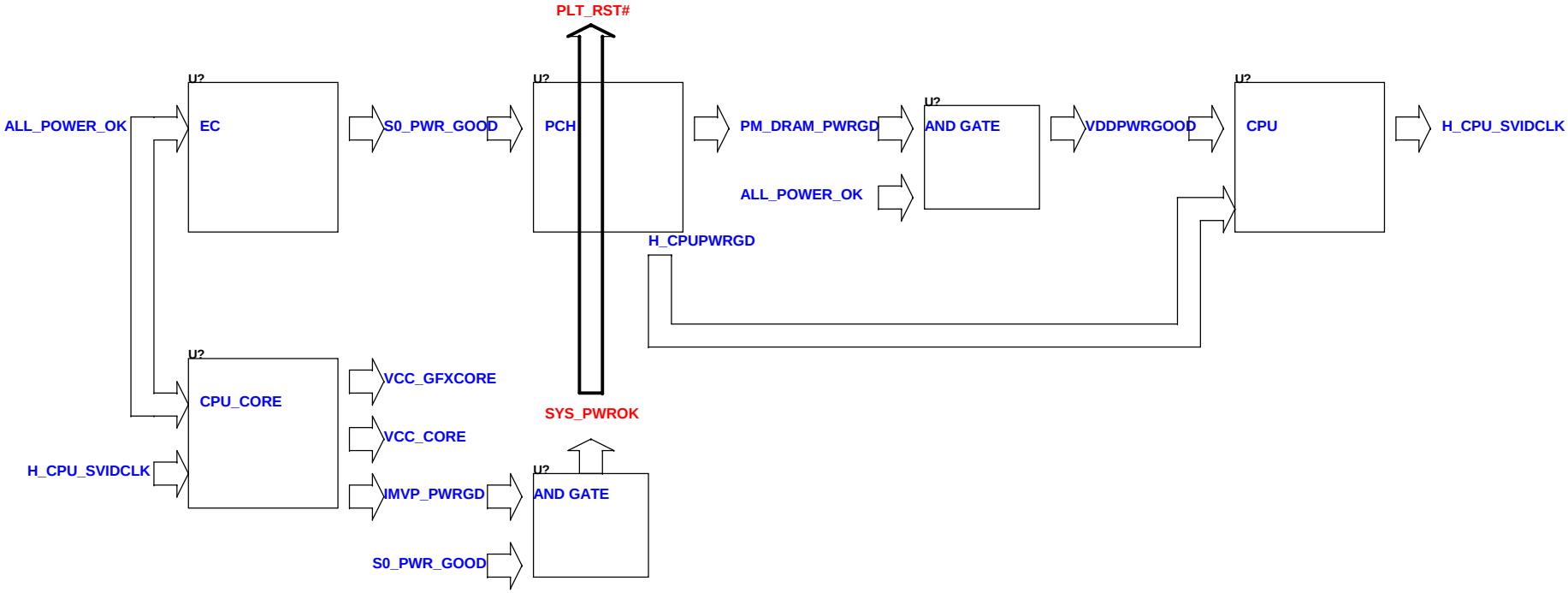
Title: ***UNUSED PARTS/EMI Capacitors***

Size	Document Number	Rev
A3	Husk/Petra	-2

Date: Tuesday, August 14, 2012 Sheet 97 of 103

Power Sequence





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Title: ***Change History***

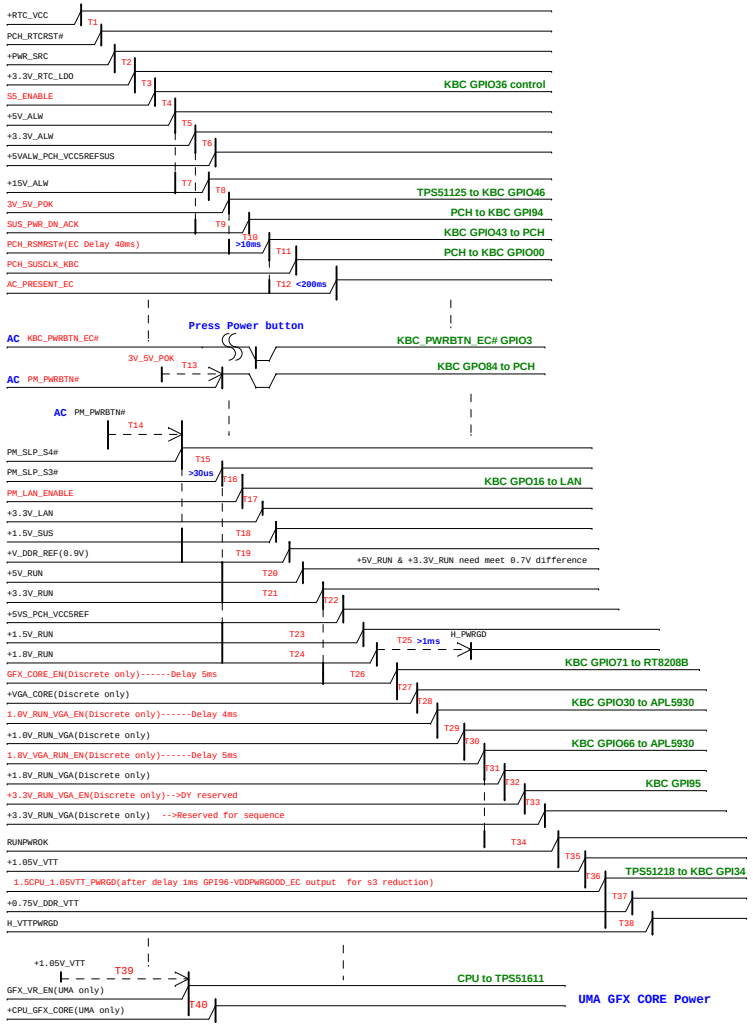
Size	Document Number	Rev
A3	Husk/Petra	-2

Date: Thursday, April 19, 2012 Sheet 98 of 103

Intel-Power Up Sequence

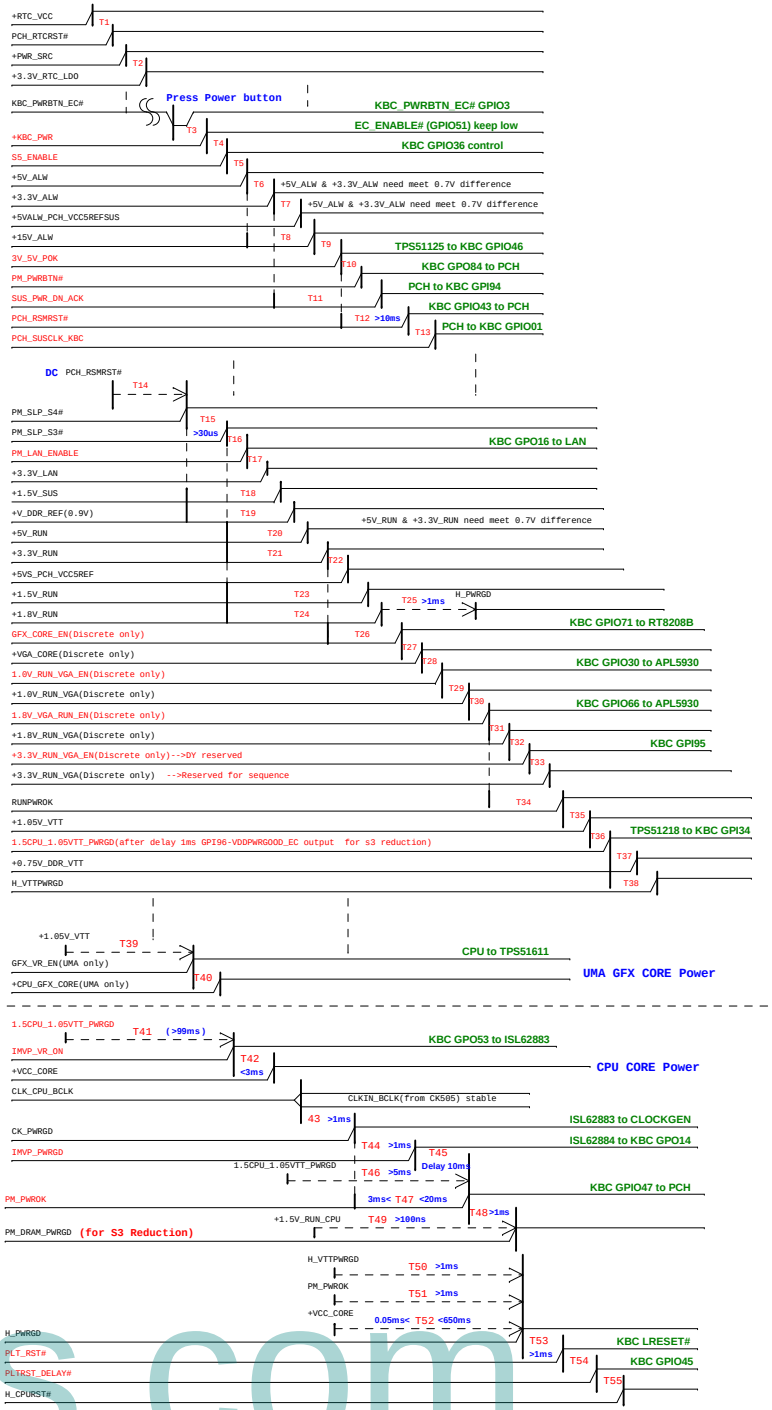
(AC mode)

red word: KBC GPIO



(DC mode)

red word: KBC GPIO



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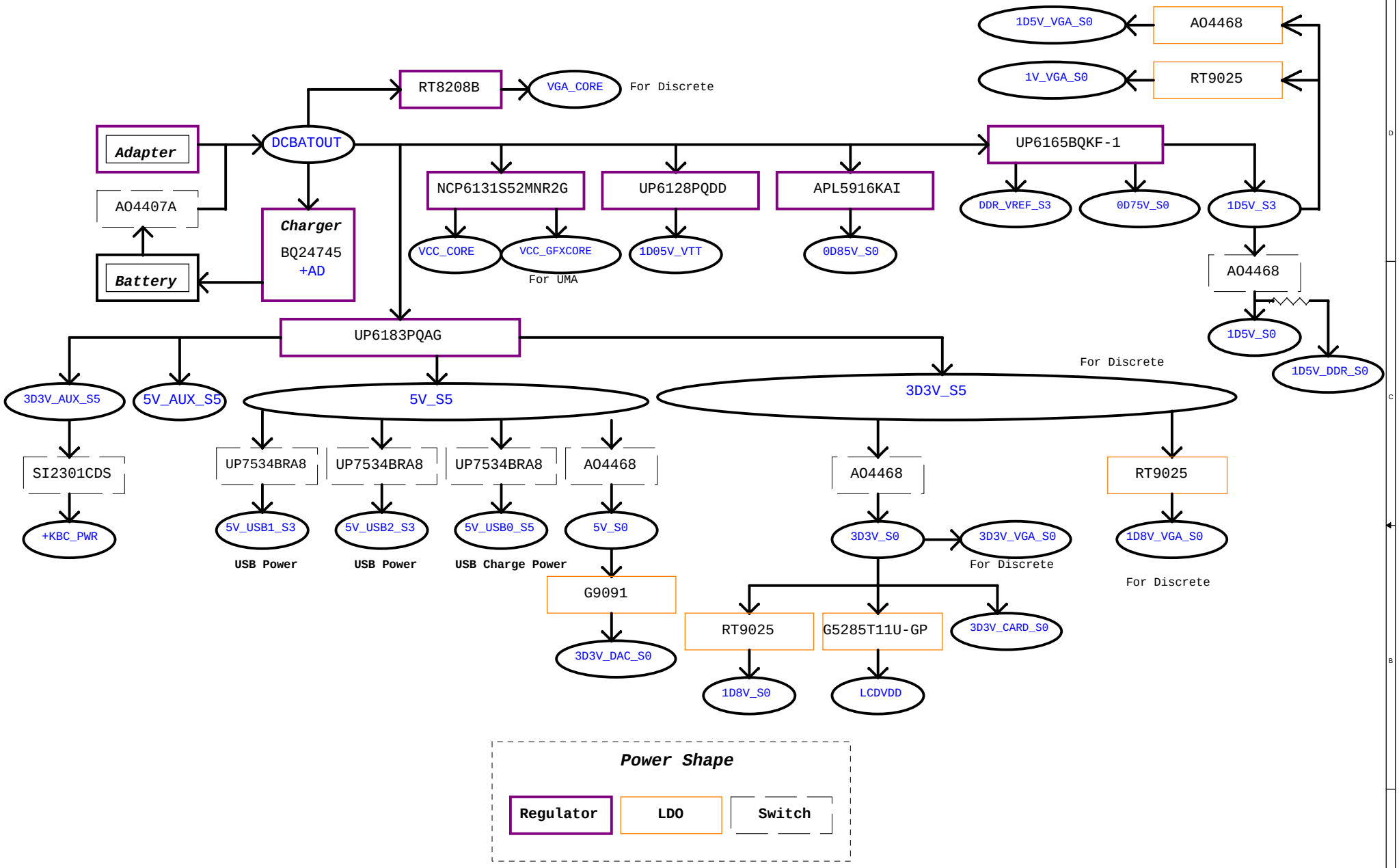
Title: Power Sequence		
Size: A3	Document Number: Husk/Petra	Rev: -2
Date: Thursday, April 10, 2014	Sheet 59 of 103	



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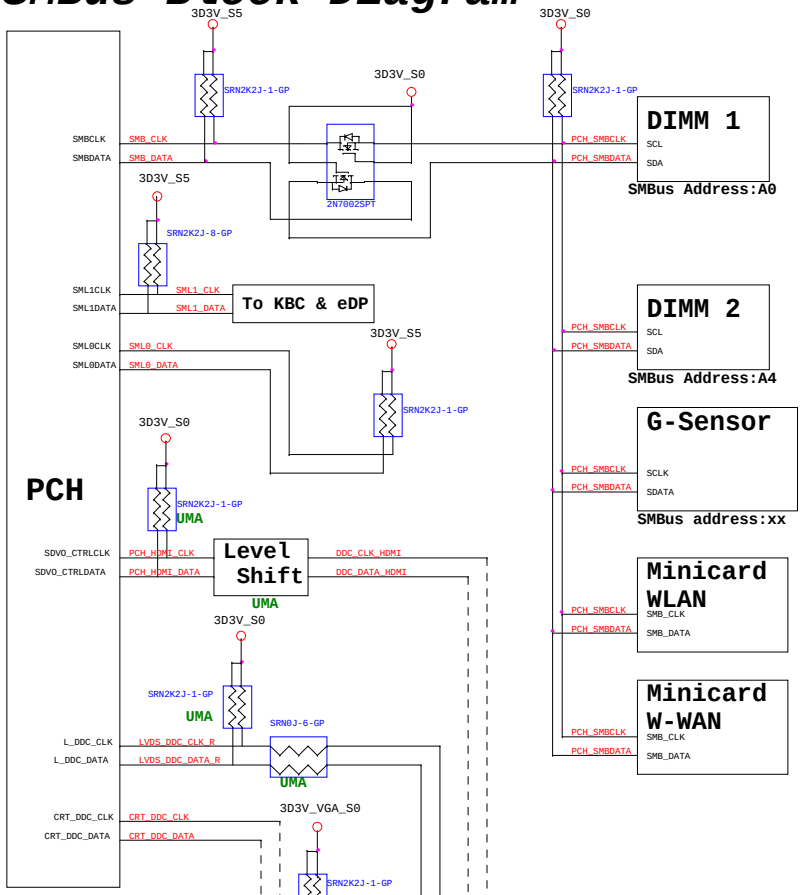
Title: Power Block Diagram

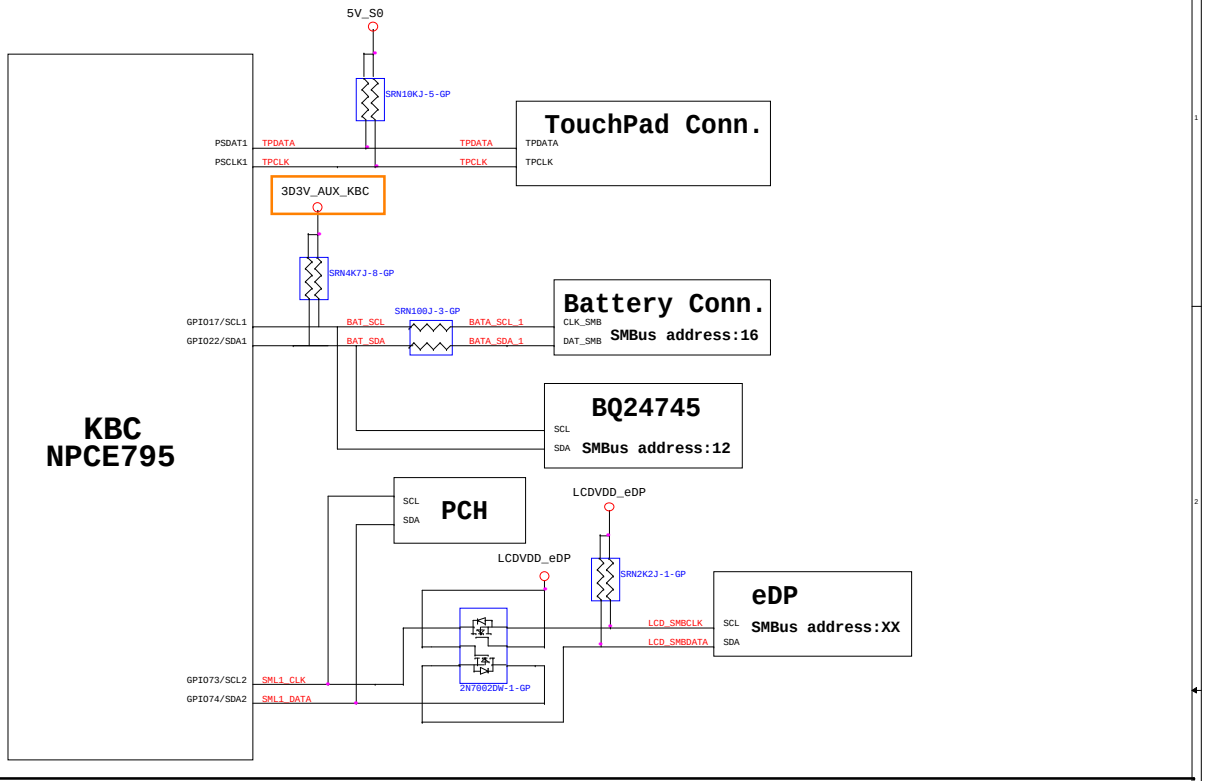
Size	Document Number	Rev
A3	Husk/Petra	-2

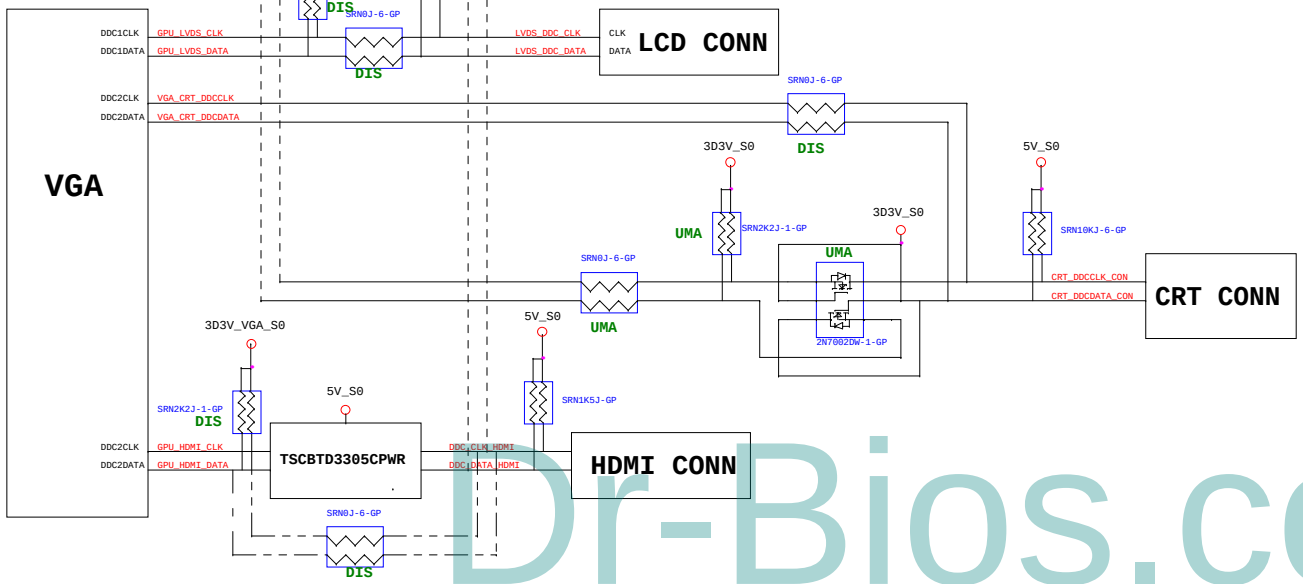
Date: Thursday, April 19, 2012 Sheet 100 of 103

PCH SMBus Block Diagram



KBC SMBus Block Diagram





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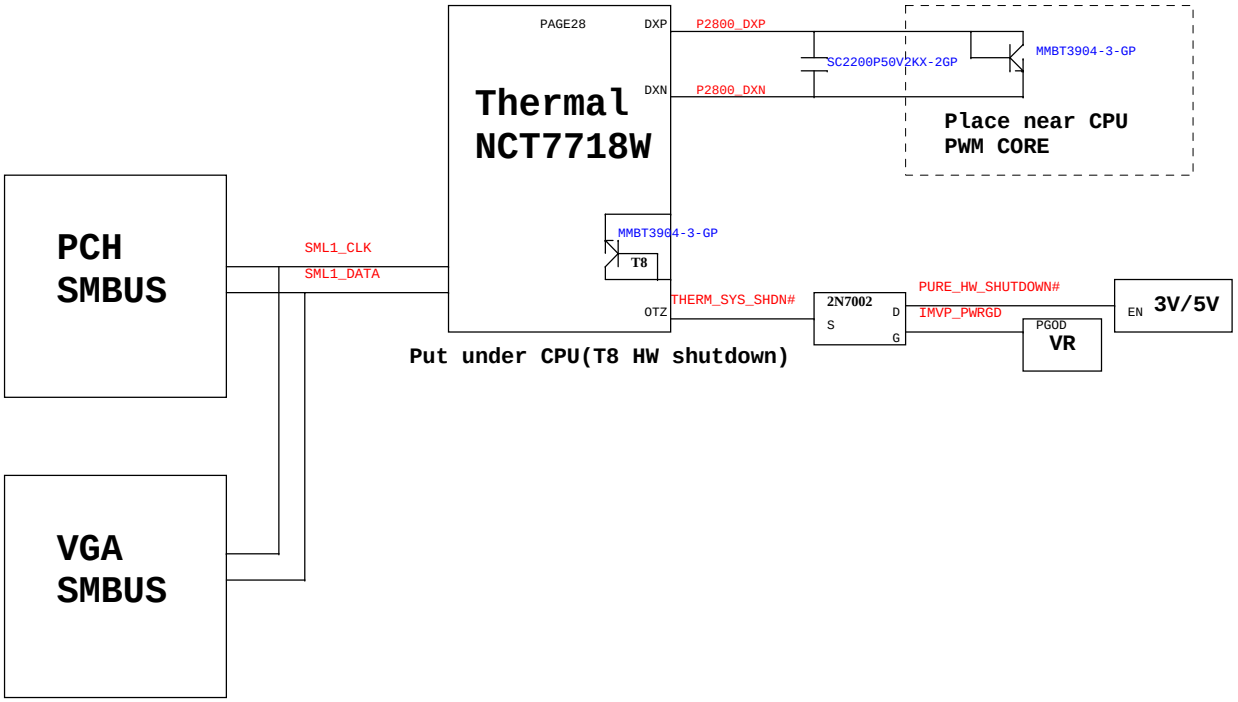
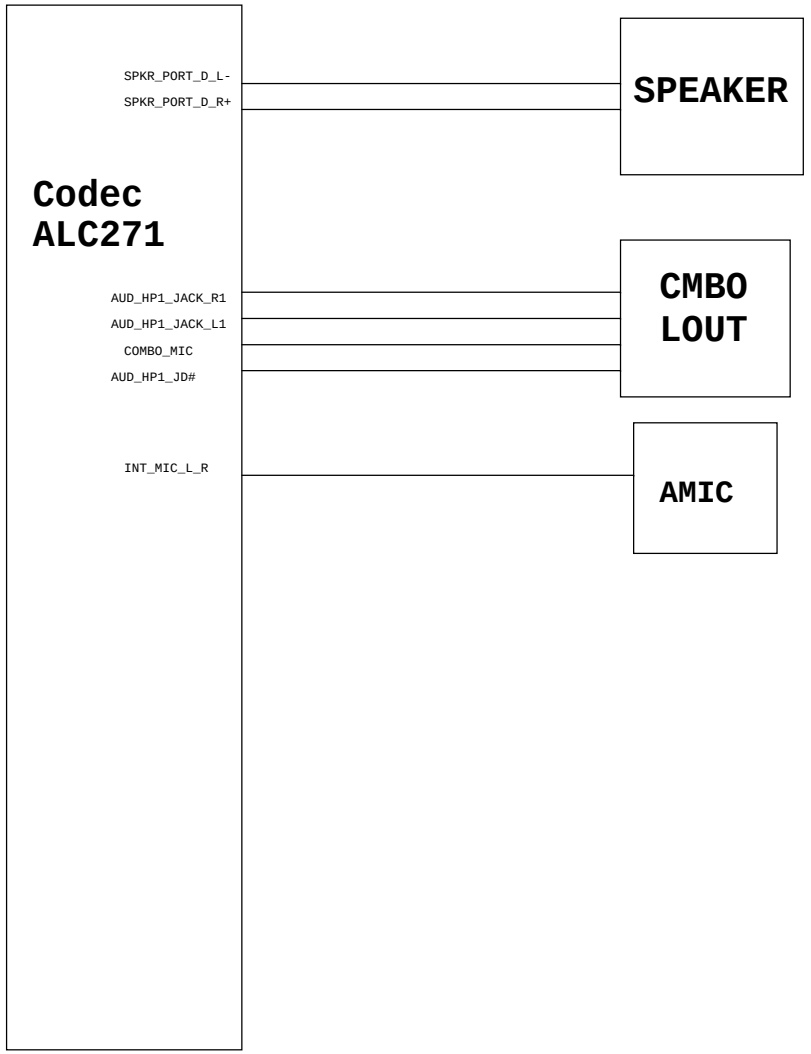
Title: SMBUS Block Diagram		
Size: A2	Document Number: Husk/Petra	Rev: -2
Date: Thursday, April 19, 2012	Sheet 101 of 103	

Thermal Block Diagram



Audio Block Diagram



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Title: Thermal/Audio Block Diagram

Size	Document Number	Rev
Custom	Husk/Petra	-2

Date: Thursday, April 19, 2012 Sheet 102 of 103