JM41/JM51 UMA Block Diagram

Project code: 91.4CQ01.001
PCB P/N : 48.4CQ01.021
REVISION : 08266-2

PCB STACKUP

TOP		L1
S		L2
VCC/GND		L3
S		L4
VCC/GND		L5
GND/VCC		L6
S		L7
BOTTOM		L8

CLK GEN.
ICS9LPRS365B 3

Intel CPU
Penryn SFF 4,5,6

Thermal Sensor
SMSC
EMC2103 32

HOST BUS 667/800/1066MHz@1.05V

DDR3
800/1066 MHz 17,18

DDR3
800/1066 MHz 17,18

Cantiga-GS SFF
AGTL+ CPU I/F
DDR Memory I/F
INTEGRATED GRAHPICS
LVDS, CRT I/F
7,8,9,10,11,12

LVDS → LCD 19
RGB CRT → CRT BD / HDMI Level Shift 20 → CRT
PCIex16 → HDMI

X4 DMI 400MHz
C-Link0

ICH9M SFF
6 PCIe ports
PCI/PCI BRIDGE
ACPI 2.0
4 SATA
12 USB 2.0/1.1 ports
ETHERNET (10/100/1000MbE)
High Definition Audio
LPC I/F
Serial Peripheral I/F
Matrix Storage Technology(DO)
Active Managemnet Technology(DO)
13,14,15,16

23
INT.SPKR
1.5W

Int MIC
19

Codec
Realtek
ALC269Q 22

AZALIA

Line Out

MIC In

CRT
BD
20

SATA

HDD SATA

ODD SATA

CARDREADER
BD 24

SSD/HDD SATA 21

PCIe → LAN Giga LAN Atheros AR8131 26 → TXFM 27 → RJ45 27

PCIe → Mini 1 Card WLAN 31

USB → Mini 2 Card 3G 31

LPC BUS → LPC DEBUG CONN.

USB

CRT BD 2 Port 20 → Camera 17

POWER BD 1 Port 26 → MINI BD 3 Port 25 → USB Blue Tooth 24

CARDREADER BD 2 Port 24 → MS/MS Pro/xD /MMC/SD

KBC
Winbond
WPCE773LA0DG 28
SPI → BIOS (2MB) 29

Touch Pad 30

INT. KB 28

SYSTEM DC/DC
TPS51125 36

INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(5A) 5V_AUX_S5 3D3V_AUX_S5

RT8202 37

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(10A)

RT8202 38

INPUTS	OUTPUTS
DCBATOUT	1D5V_S3(11A)

RT9026 39

INPUTS	OUTPUTS
5V_S5	DDR_VREF_S3 (1.2A)

CHARGER
MAX8731A 41

INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A

CPU DC/DC
ADP3207A 35

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0~1.3V 64A

VGA
ISL6263A 40

INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE (7A)

UMA

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Title: BLOCK DIAGRAM
Size: Custom | Document Number: JM41/JM51_UMA | Rev: -2
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ICH9M Functional Strap Definitions

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/ GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9M Integrated Pull-up and Pull-down Resistors

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) **1=The iTPM Host Interface is disalbed(default)**
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality (default)**
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1= Disabled (default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) **11 = Disabled (default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation(Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 =Digital display Port and PCIe are operting simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	**0 =No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG/12/CFG13 straps can be enabled at any time.

UMA

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Title: Reference
Size: A3 | Document Number: JM41/JM51_UMA | Rev: -2
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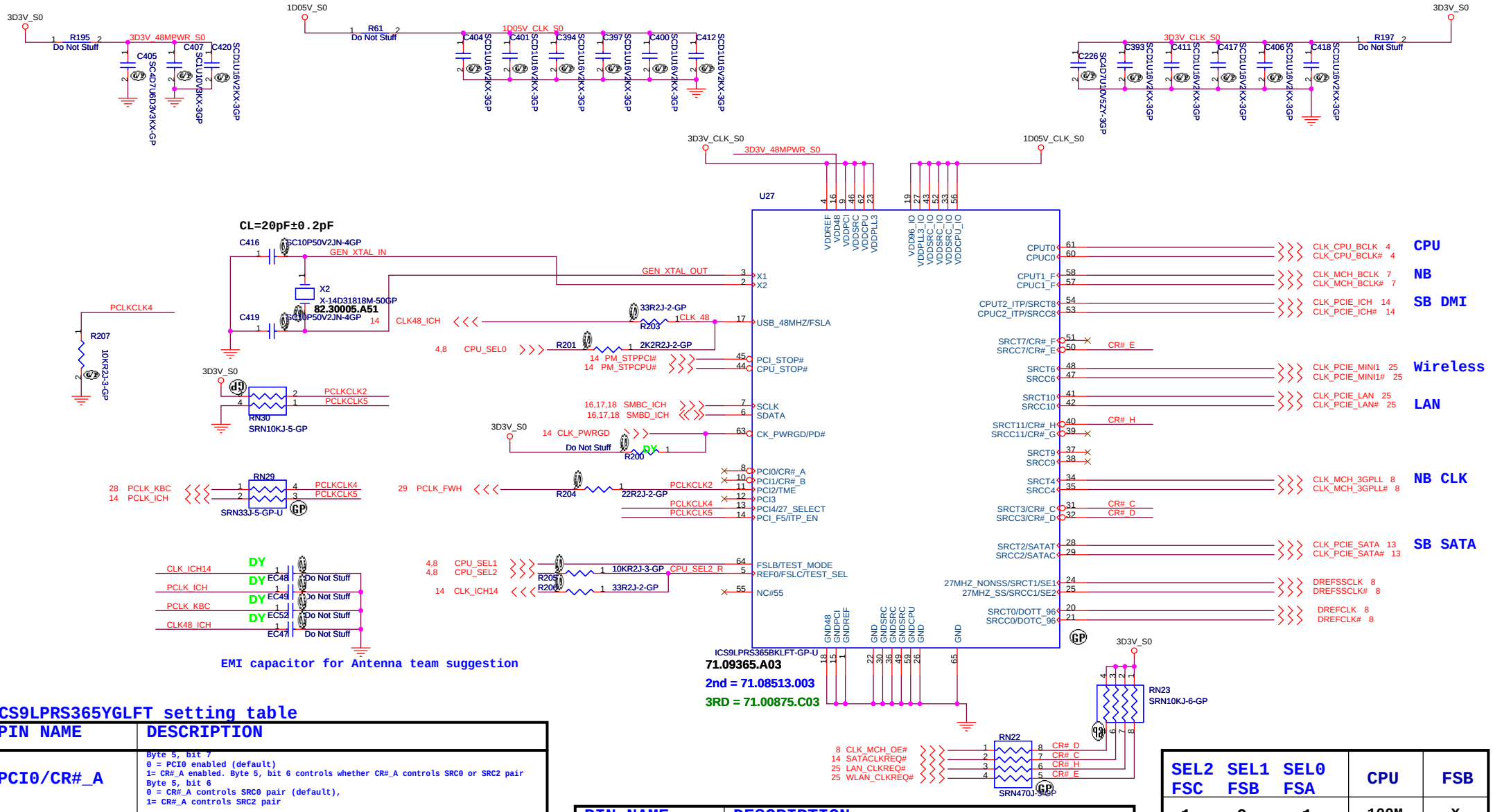

ICS9LPRS365YGLFT setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3	
PCI4/27M_SEL	0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96# 1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0#
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#
SRCT3/CR#_C	Byte 5, bit 3 0 = SRC3 enabled (default) 1= CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair Byte 5, bit 2 0 = CR#_C controls SRC0 pair (default), 1= CR#_C controls SRC2 pair

PIN NAME	DESCRIPTION
SRCC3/CR#_D	Byte 5, bit 1 0 = SRC3 enabled (default) 1= CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default) 1= CR#_D controls SRC4 pair
SRCC7/CR#_E	Byte 6, bit 7 0 = SRC7# enabled (default) 1= CR#_F controls SRC6
SRCT7/CR#_F	Byte 6, bit 6 0 = SRC7 enabled (default) 1= CR#_F controls SRC8
SRCC11/CR#_G	Byte 6, bit 5 0 = SRC11# enabled (default) 1= CR#_G controls SRC9
SRCT11/CR#_H	Byte 6, bit 4 0 = SRC11 enabled (default) 1= CR#_H controls SRC10

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M

UMA

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Title: Clock Generator

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	JM41/JM51_UMA	-2

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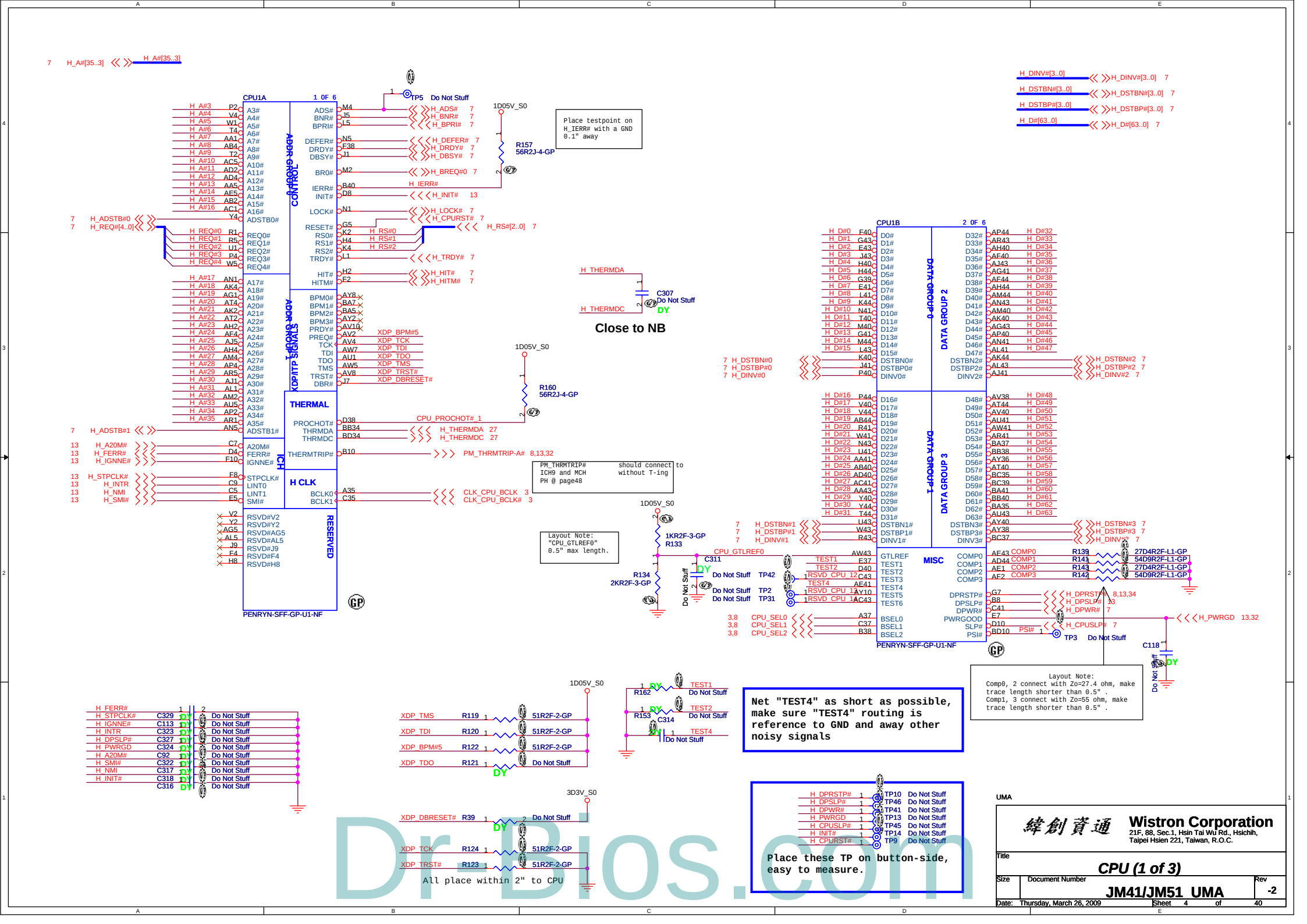
CPU1A
1 OF 6
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERMAL
H CLK
ICH
RESERVED
PENRYN-SFF-GP-U1-NF
CPU1B
2 OF 6
DATA GROUP 0
DATA GROUP 1
DATA GROUP 2
DATA GROUP 3
MISC
PENRYN-SFF-GP-U1-NF
Close to NB
Place testpoint on H_IERR# with a GND 0.1" away
PM_THRMTRIP# should connect to ICH9 and MCH PH @ page48
Layout Note: "CPU_GTLREF0" 0.5" max length.
Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" . Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .
Net "TEST4" as short as possible, make sure "TEST4" routing is reference to GND and away other noisy signals
Place these TP on button-side, easy to measure.
All place within 2" to CPU
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Title
CPU (1 of 3)
Size
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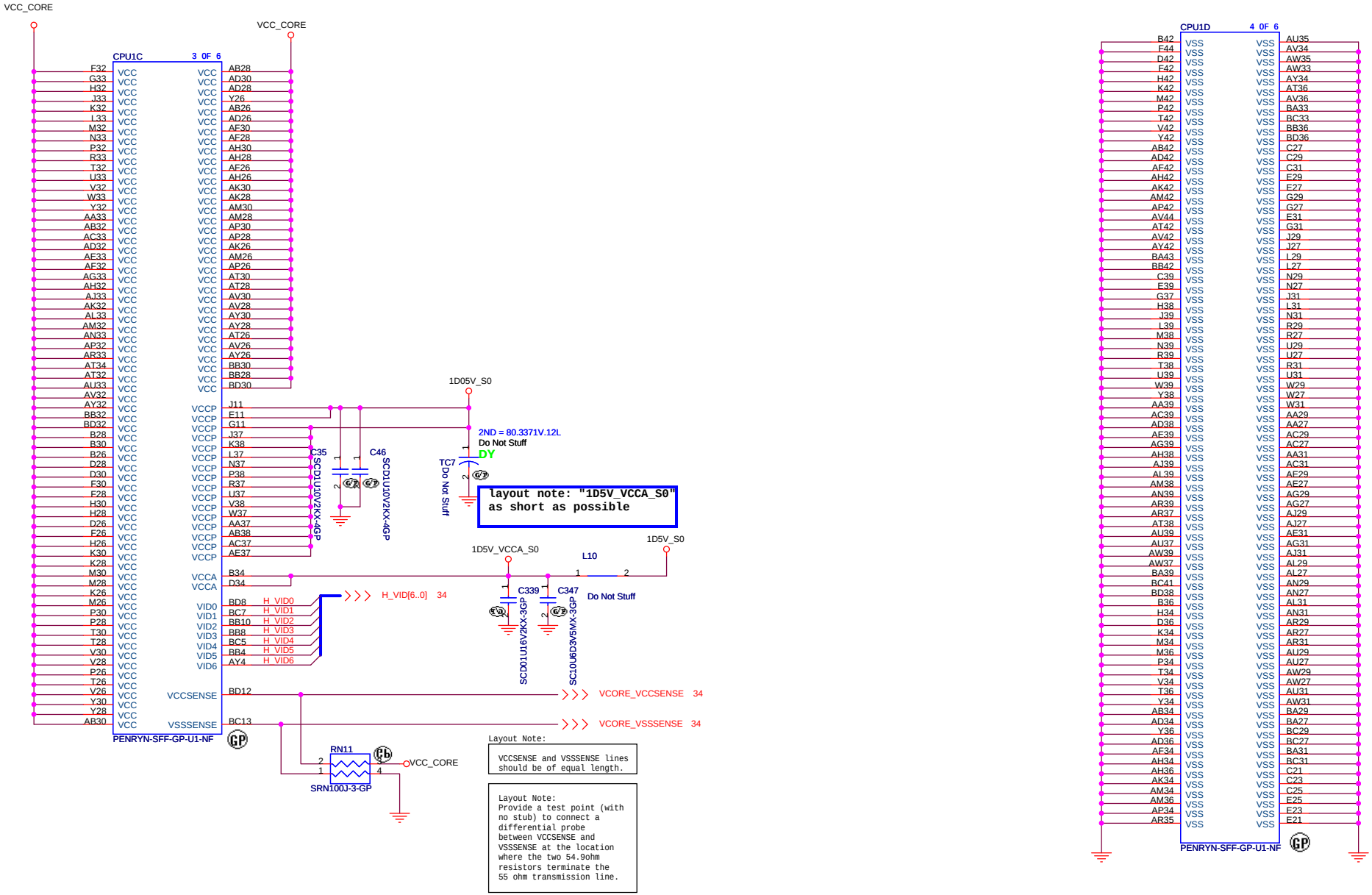

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Title	CPU (2 of 3)	
Size	Document Number: JM41/JM51_UMA	Rev: -2
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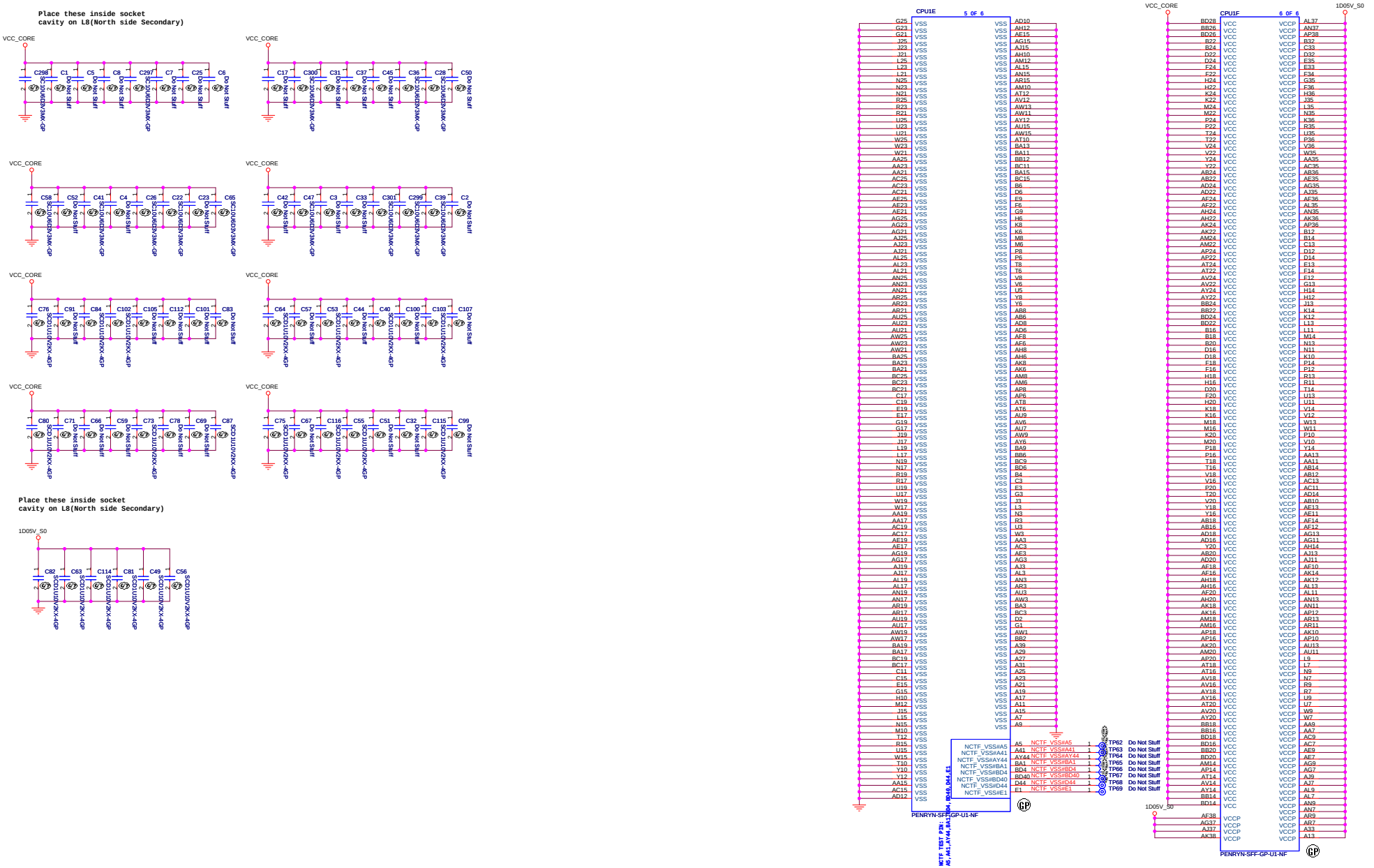

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Title	CPU (3 of 3)	
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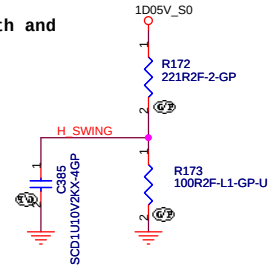
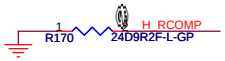
H_SWING routing Trace width and Spacing use 10 / 20 mil

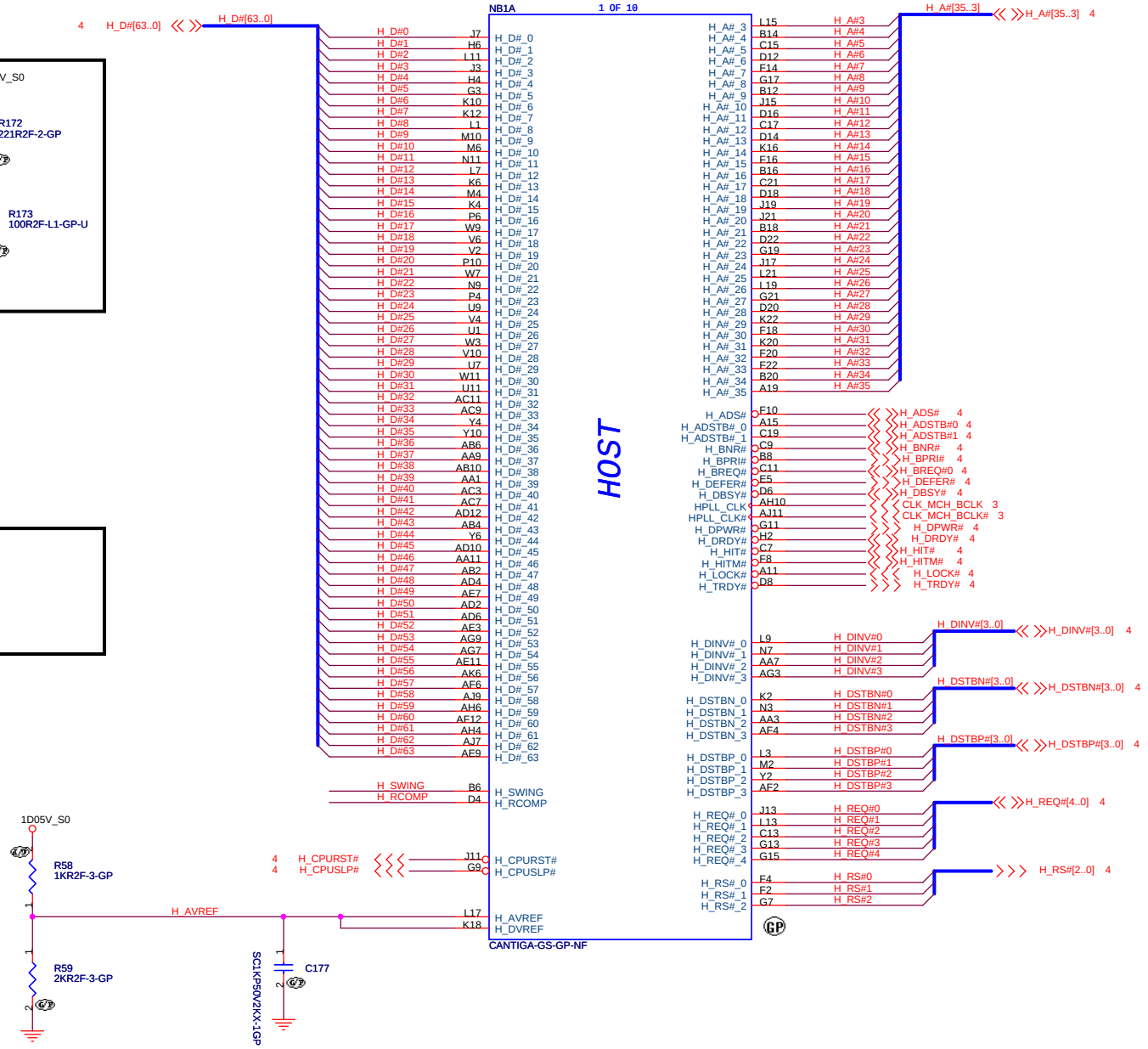
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")



UMA

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Title: ***Cantiga (1 of 6)***

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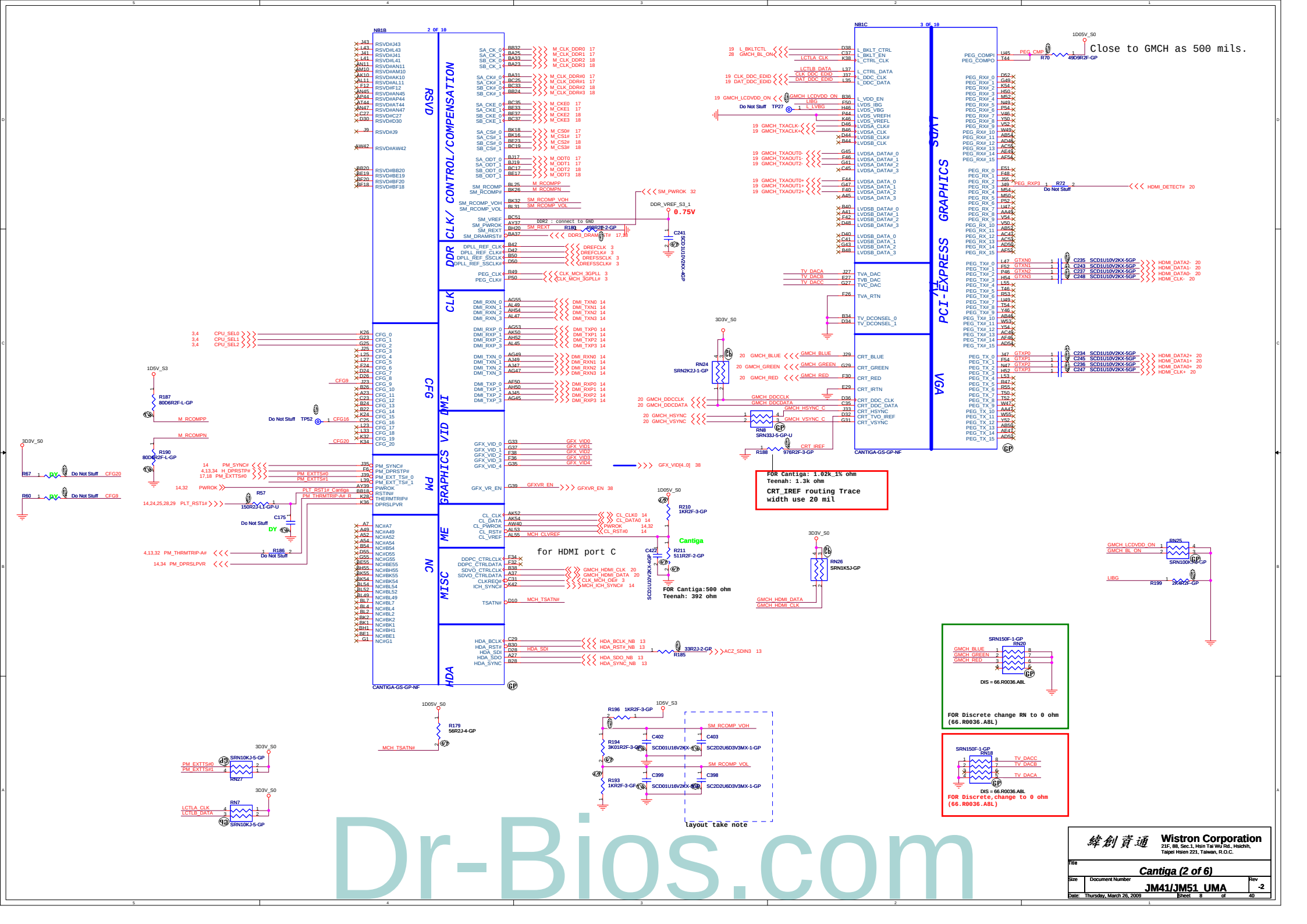
NB1B
2 OF 10
RSVD
CLK/ CONTROL/COMPENSATION
DDR
CLK
CFG
DMI
GRAPHICS VID
PM
ME
NC
MISC
HDA
NB1C
3 OF 10
PCI-EXPRESS GRAPHICS
VGA
CANTIGA-GS-GP-NF
Close to GMCH as 500 mils.
for HDMI port C
Cantiga
FOR Cantiga:500 ohm
Teenah: 392 ohm
FOR Cantiga: 1.02K_1% ohm
Teenah: 1.3k ohm
CRT_IREF routing Trace
width use 20 mil
FOR Discrete change RN to 0 ohm
(66.R0036.A8L)
FOR Discrete,change to 0 ohm
(66.R0036.A8L)
layout take note
0.75V
Do Not Stuff
DDR2 : connect to GND
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Cantiga (2 of 6)
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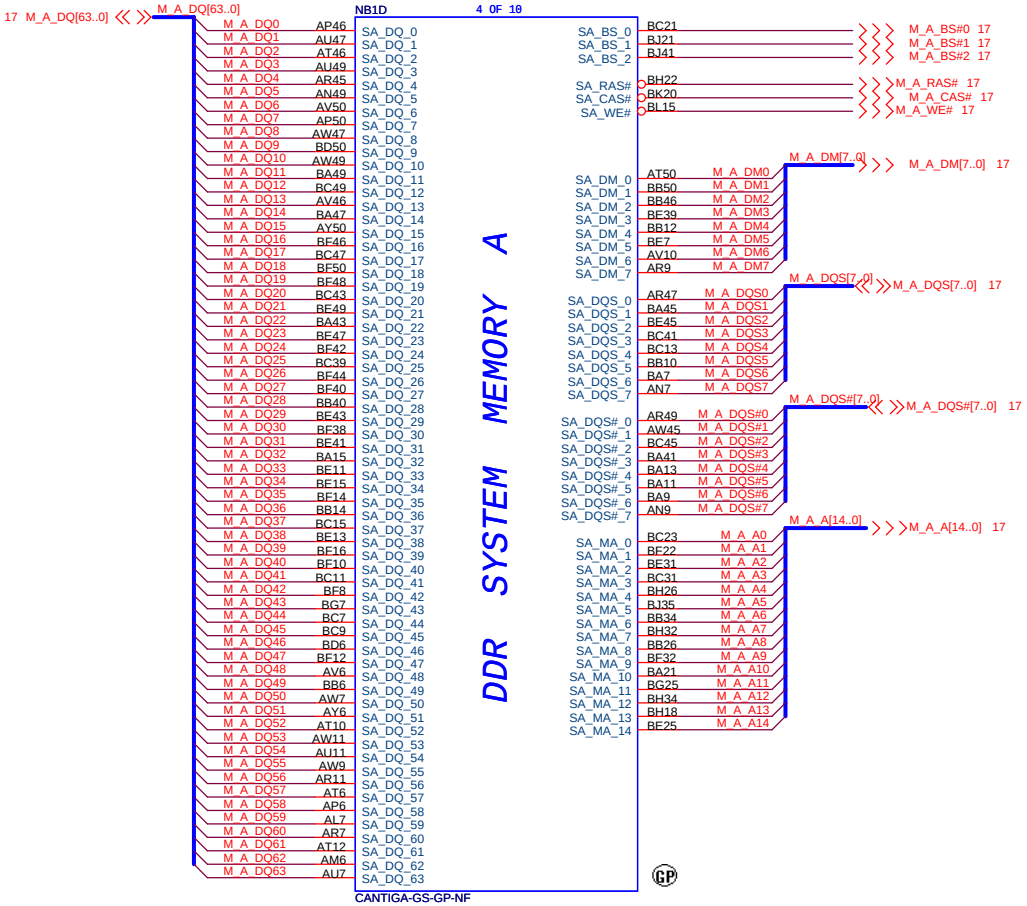

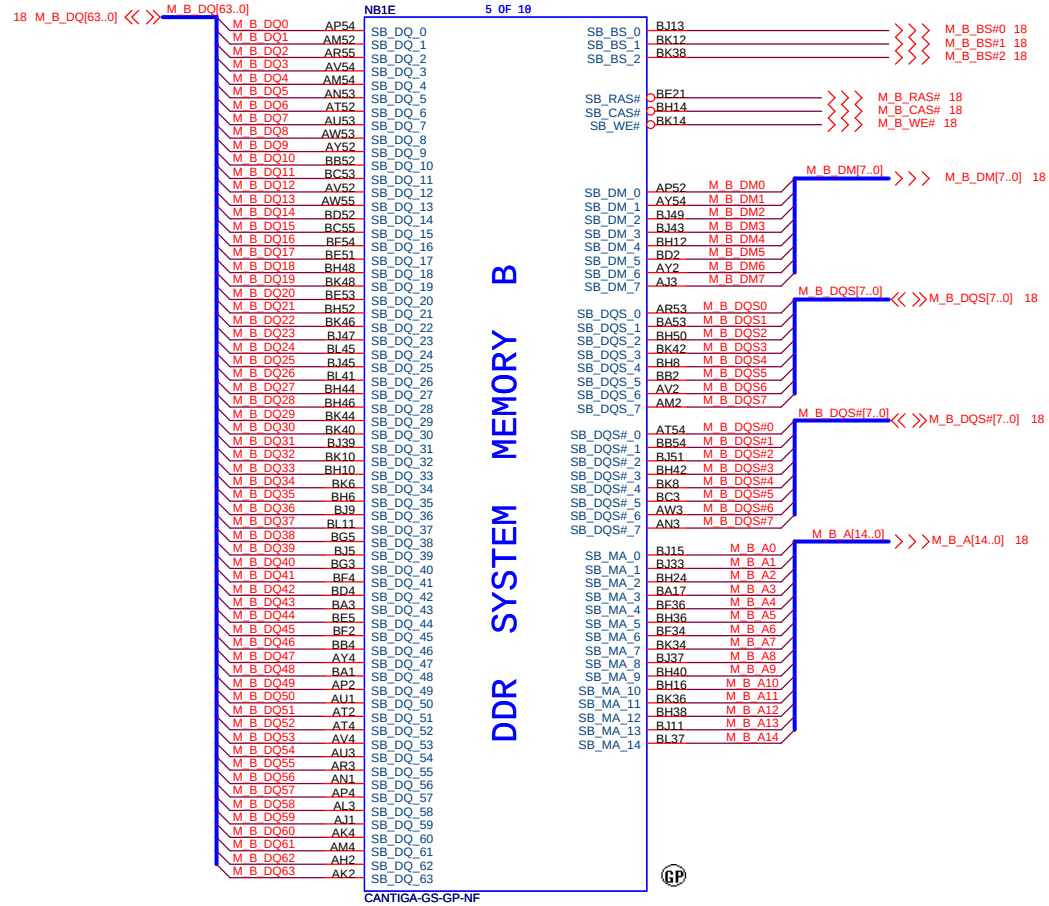

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Title: ***Cantiga (3 of 6)***

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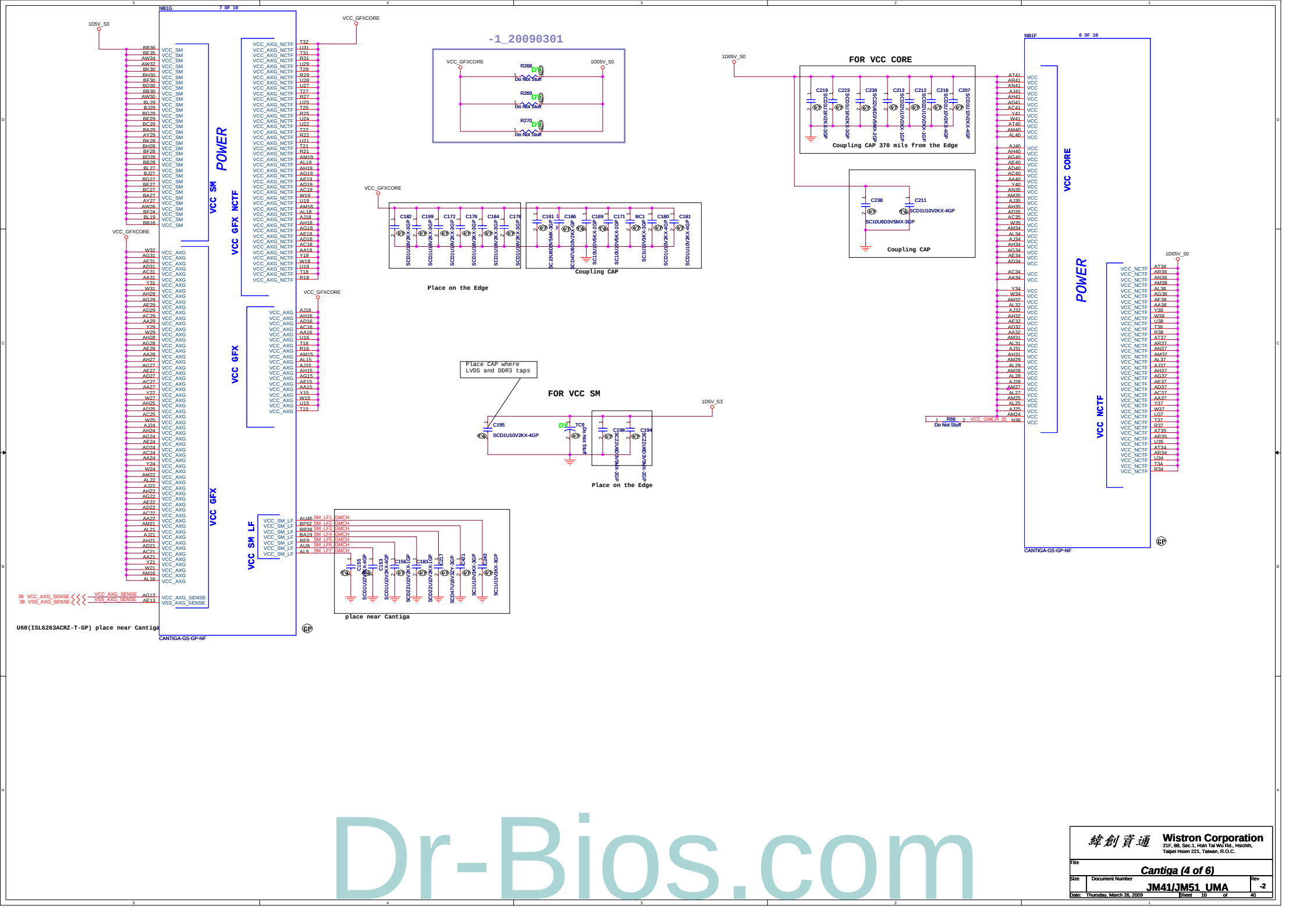

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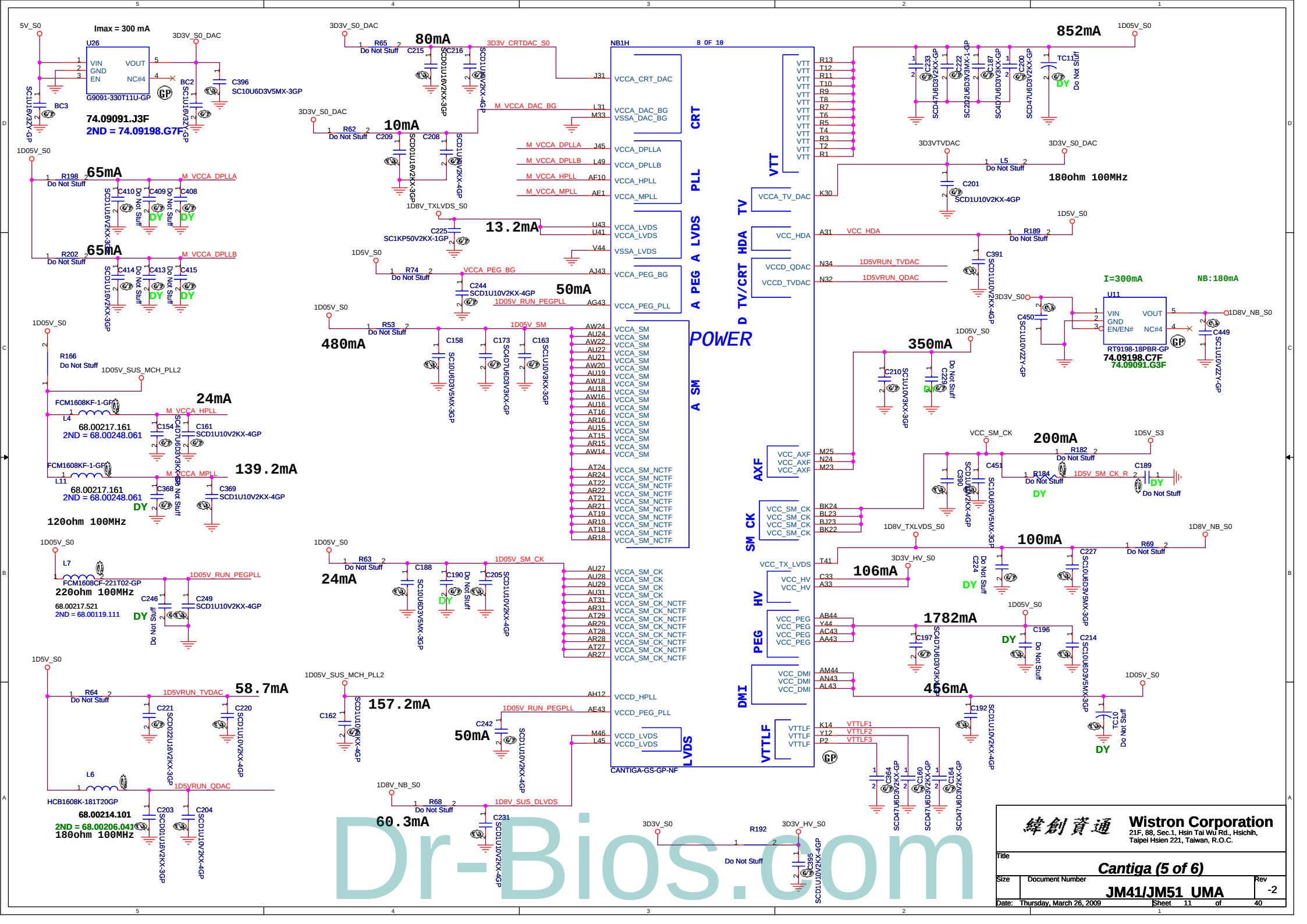
Imax = 300 mA
74.09091.J3F
2ND = 74.09198.G7F
80mA
10mA
13.2mA
65mA
65mA
24mA
139.2mA
120ohm 100MHz
50mA
480mA
24mA
220ohm 100MHz
58.7mA
157.2mA
50mA
60.3mA
180ohm 100MHz
852mA
180ohm 100MHz
I=300mA
NB:180mA
350mA
74.09198.C7F
74.09091.G3F
200mA
100mA
106mA
1782mA
456mA
NB1H
8 OF 10
CRT
PLL
A LVDS
A PEG
D TV/CRT HDA
POWER
A SM
AXF
SM CK
HV
PEG
DMI
VTTLF
VTT
TV
LVDS
CANTIGA-GS-GP-NF
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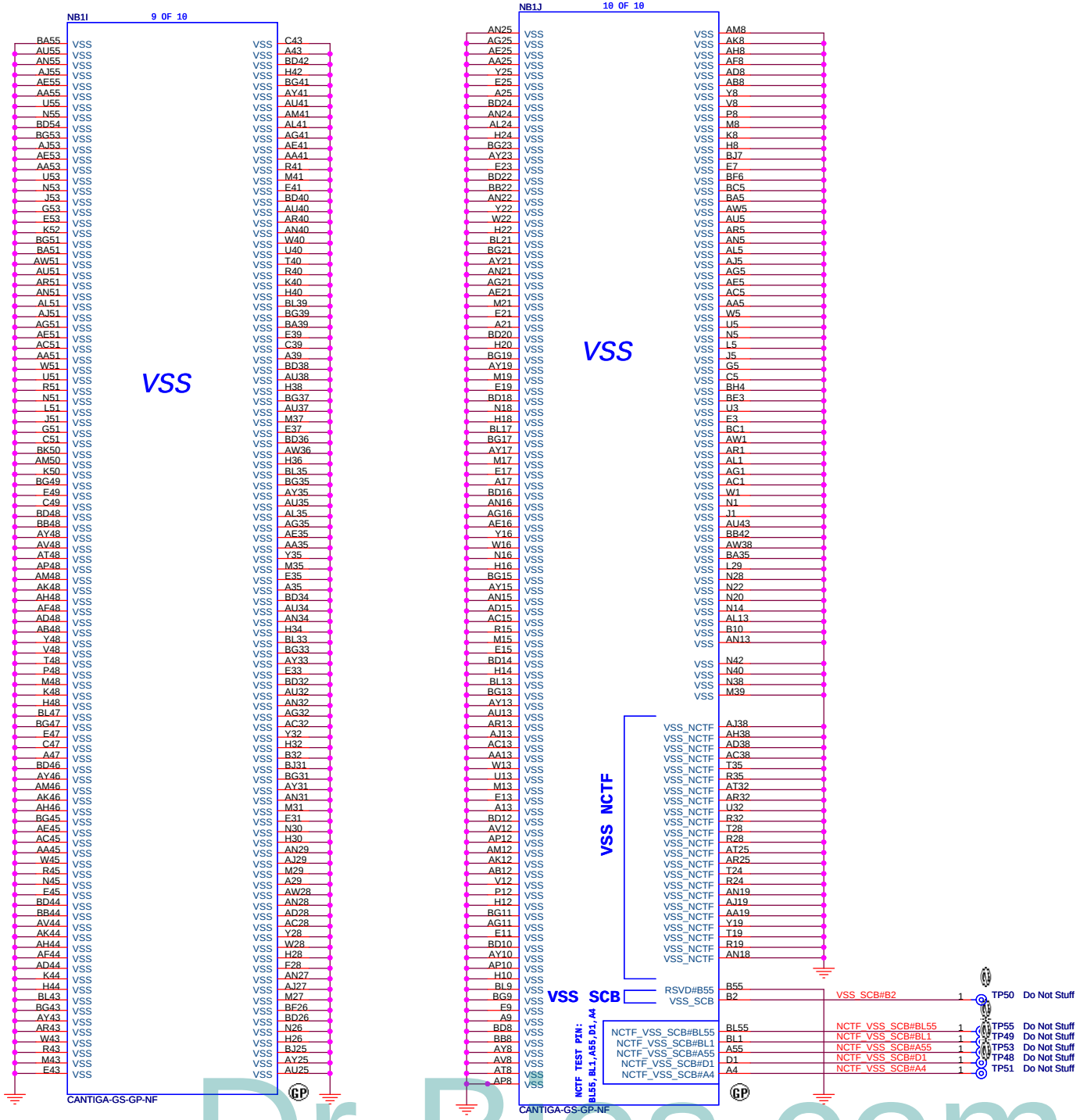
40



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Title	Cantiga (6 of 6)	
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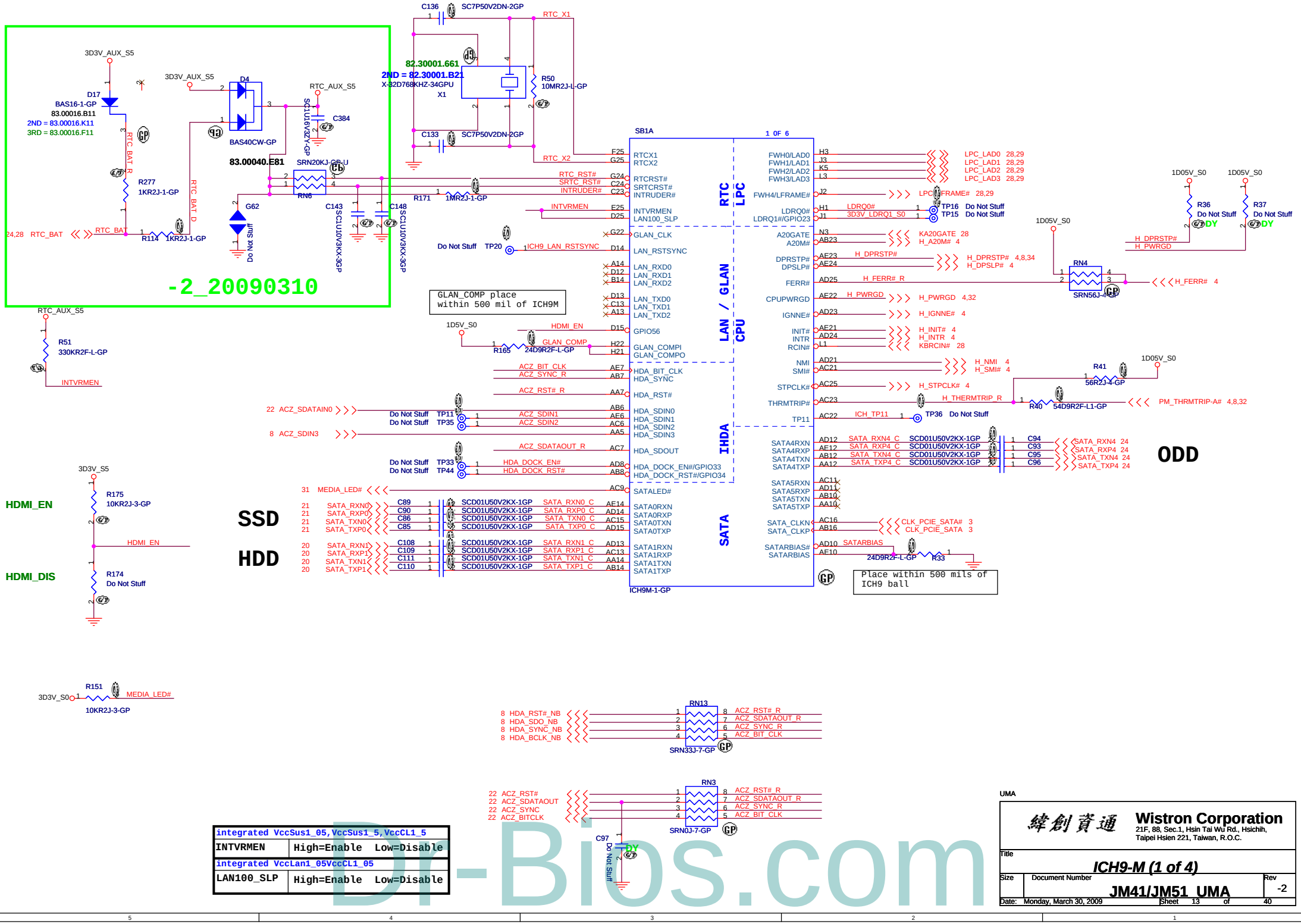
-2_20090310
82.30001.661
2ND = 82.30001.B21
X-32D768KHZ-34GPU
X1
SB1A
1 0F 6
ICH9M-1-GP
RTC
LPC
LAN / GLAN
CPU
IHDA
SATA
GLAN_COMP place within 500 mil of ICH9M
Place within 500 mils of ICH9 ball
SSD
HDD
ODD
HDMI_EN
HDMI_DIS
integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP High=Enable Low=Disable
UMA
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ICH9-M (1 of 4)
JM41/JM51 UMA
-2
Date: Monday, March 30, 2009
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Dr-Bios.com

PCI_GNT#0 and SPI_CS1#
have weak internal Pull up

BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

A16 swap override strap	
PCI_GNT#3	low = A16 swap override enable high = default

GPIO49 should be pulled down to GND only when using Teenah. When using Cantiga, this ball should be left as No Connect.

No Reboot Strap	
SPKR	LOW = Defaule High=No Reboot

USB	
Pair	Device
0	USB2
1	USB3
2	USB4
3	WiMAX
4	WEBCAM
5	NC
6	NC
7	BLUETOOTH
8	NC
9	USB1
10	MINIC2
11	Cardreader

These R need close SB
within 600 mils

-1 20090305

83.00016.B11
2ND = 83.00016.K11
3RD = 83.00016.F11

83.BAT54.D81
2ND = 83.BAT54.X81
3RD = 83.00054.S81

UMA

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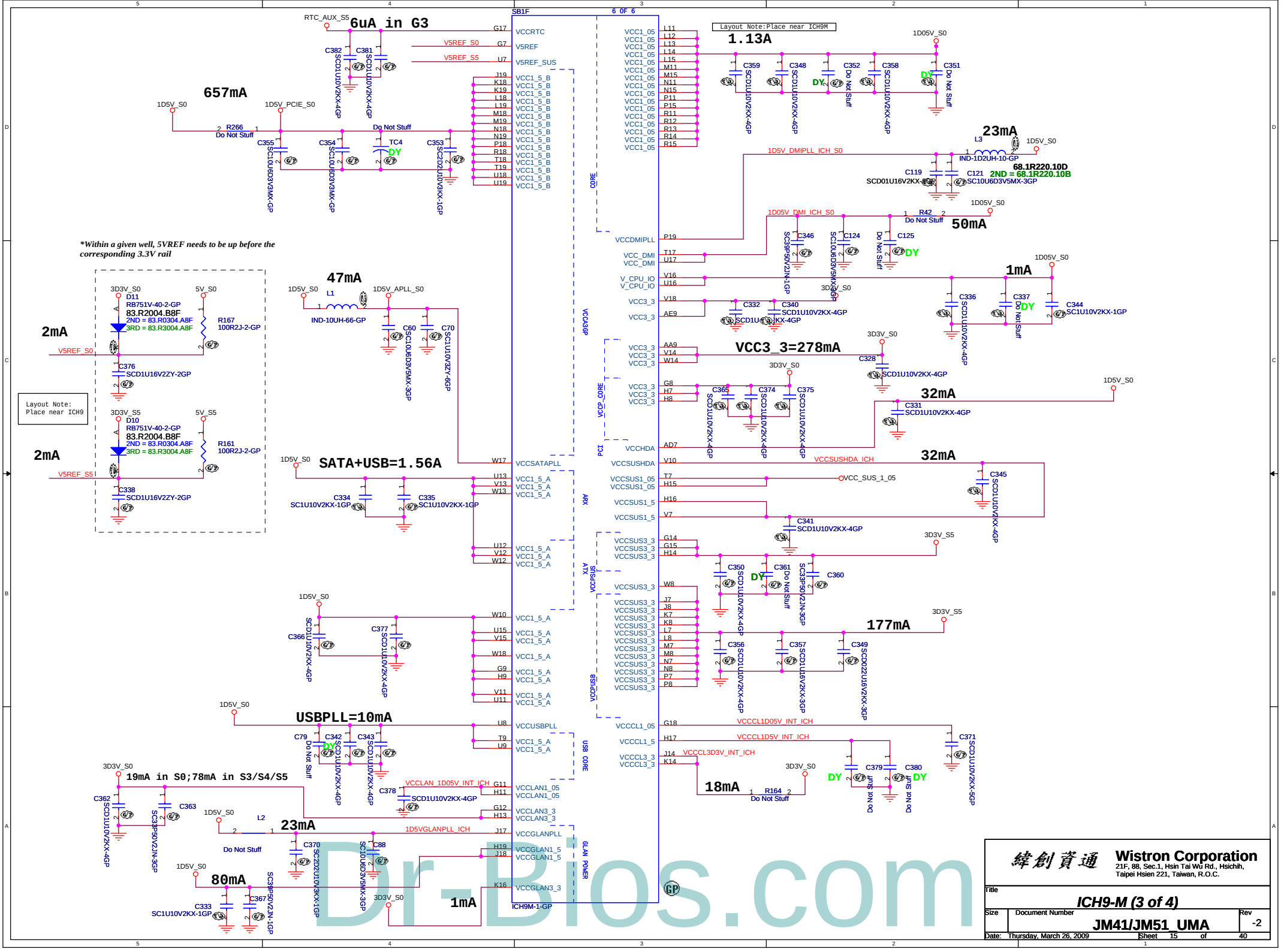
6uA in G3
657mA
1.13A
23mA
50mA
1mA
2mA
2mA
47mA
SATA+USB=1.56A
VCC3_3=278mA
32mA
32mA
177mA
USBPLL=10mA
19mA in S0;78mA in S3/S4/S5
23mA
80mA
1mA
18mA
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
Layout Note:Place near ICH9M
Layout Note: Place near ICH9
ICH9M-1-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
ICH9-M (3 of 4)
JM41/JM51_UMA
Rev -2
Date: Thursday, March 26, 2009
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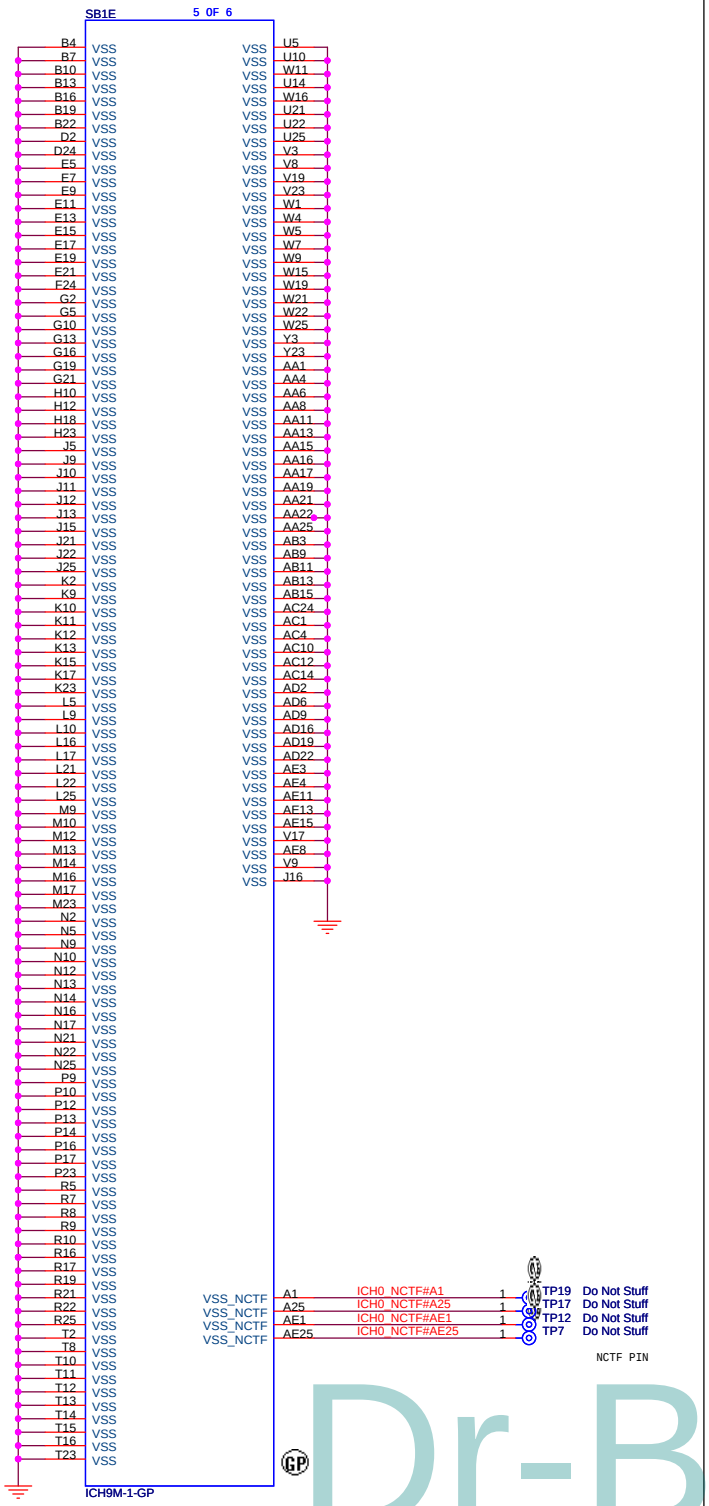

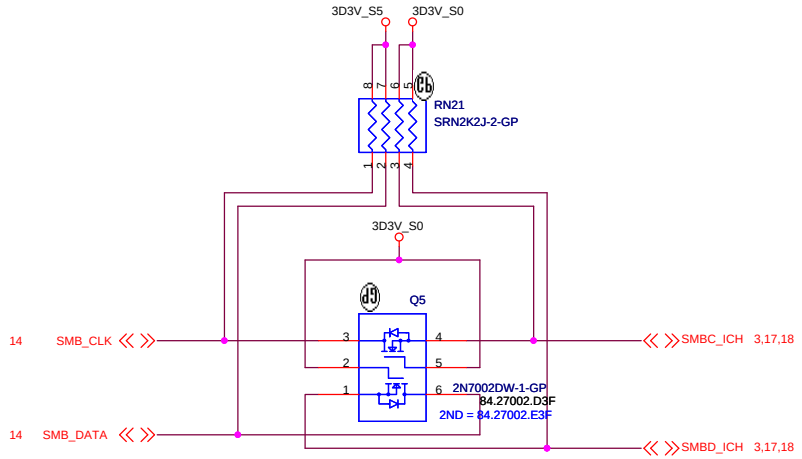

SMBUS

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Title: ***ICH9-M (4 of 4)***

Size | Document Number: **JM41/JM51_UMA** | Rev: -2

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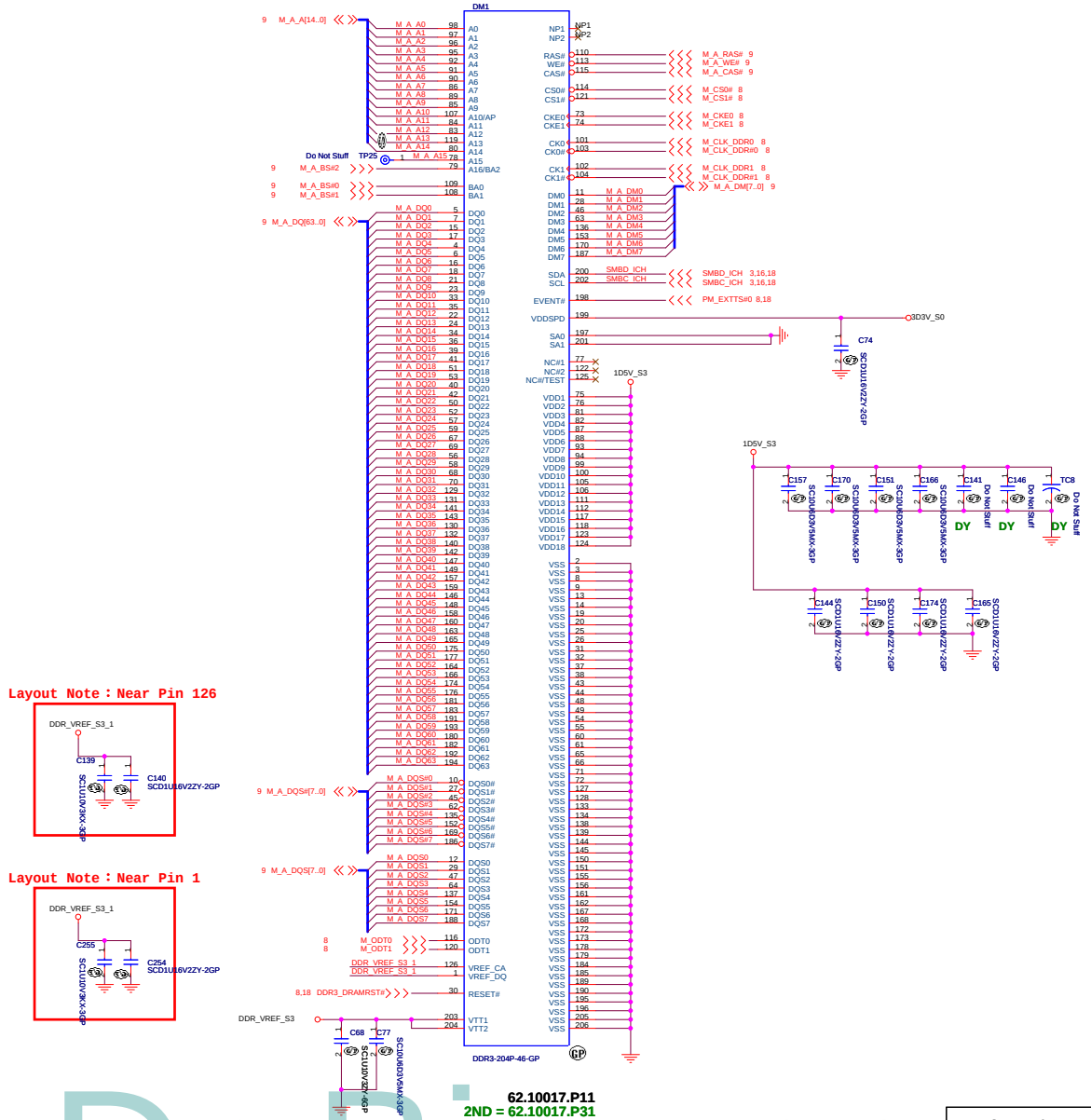
DDR3 SOCKET_1



62.10017.P11
2ND = 62.10017.P31

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title	DDR3 Socket1	
Size	Document Number	Rev
	JM41/JM51_UMA	-2
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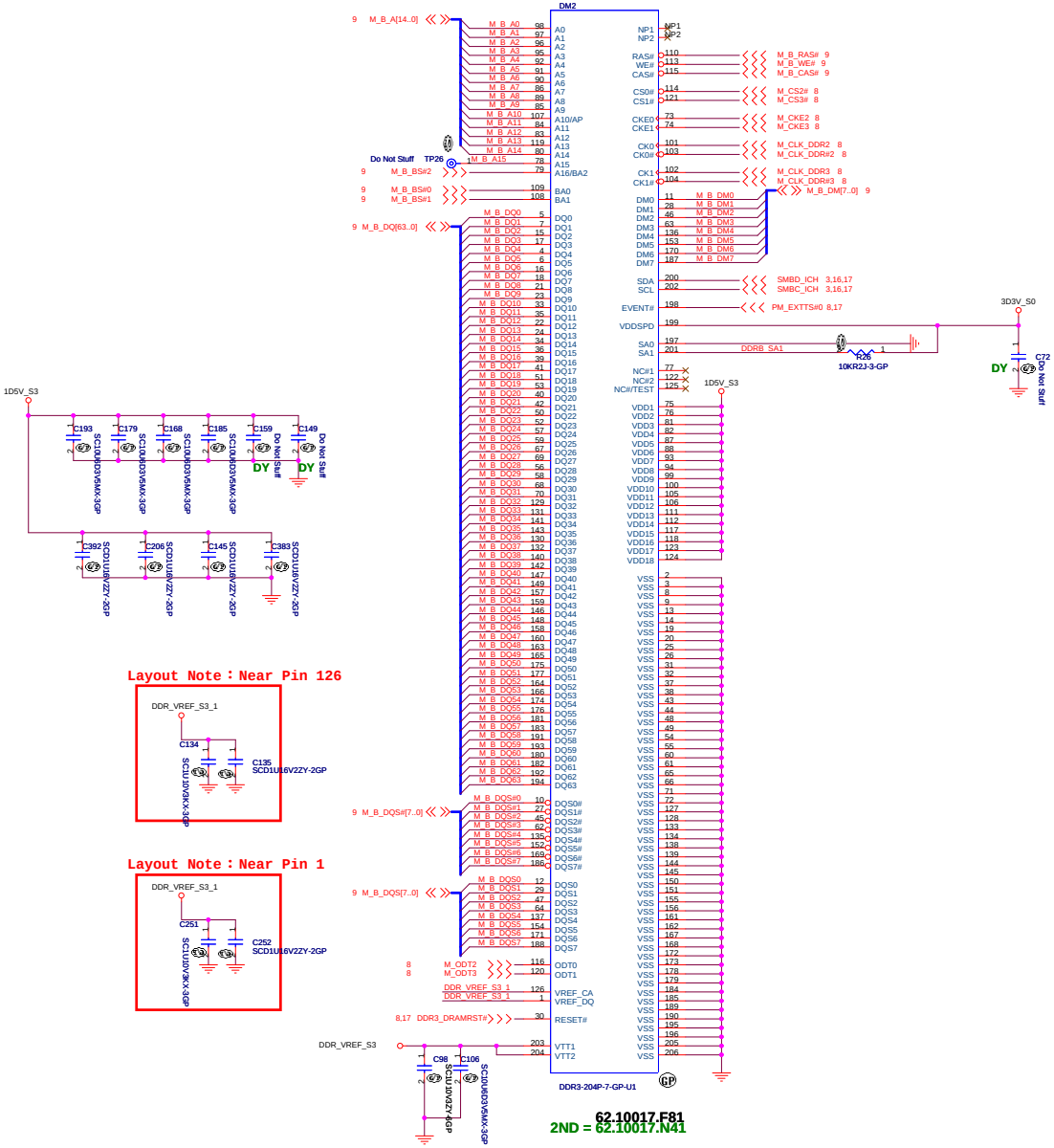
DDR3 SOCKET_2



緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: DDR3 Socket2			
Size	Document Number: JM41/JM51_UMA	Rev: -2	
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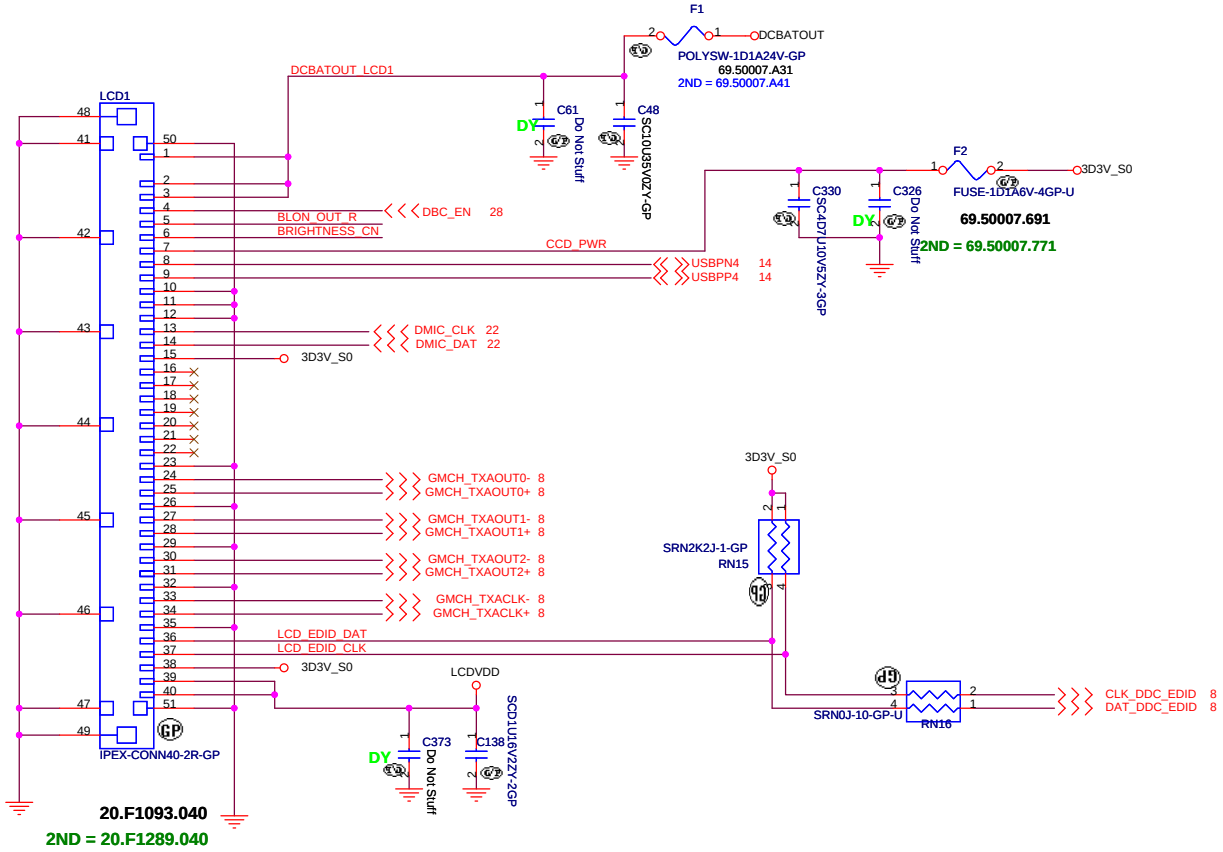
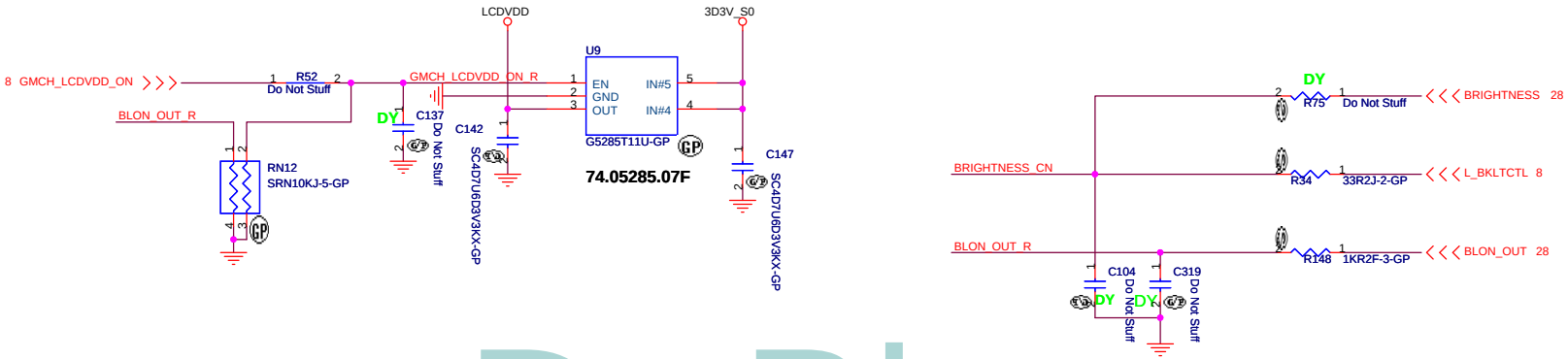
LCD/CCD CONN

Internal MIC



Layout 40 mil



UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	LCD CONN	
Size	Document Number: JM41/JM51 UMA	Rev: -2
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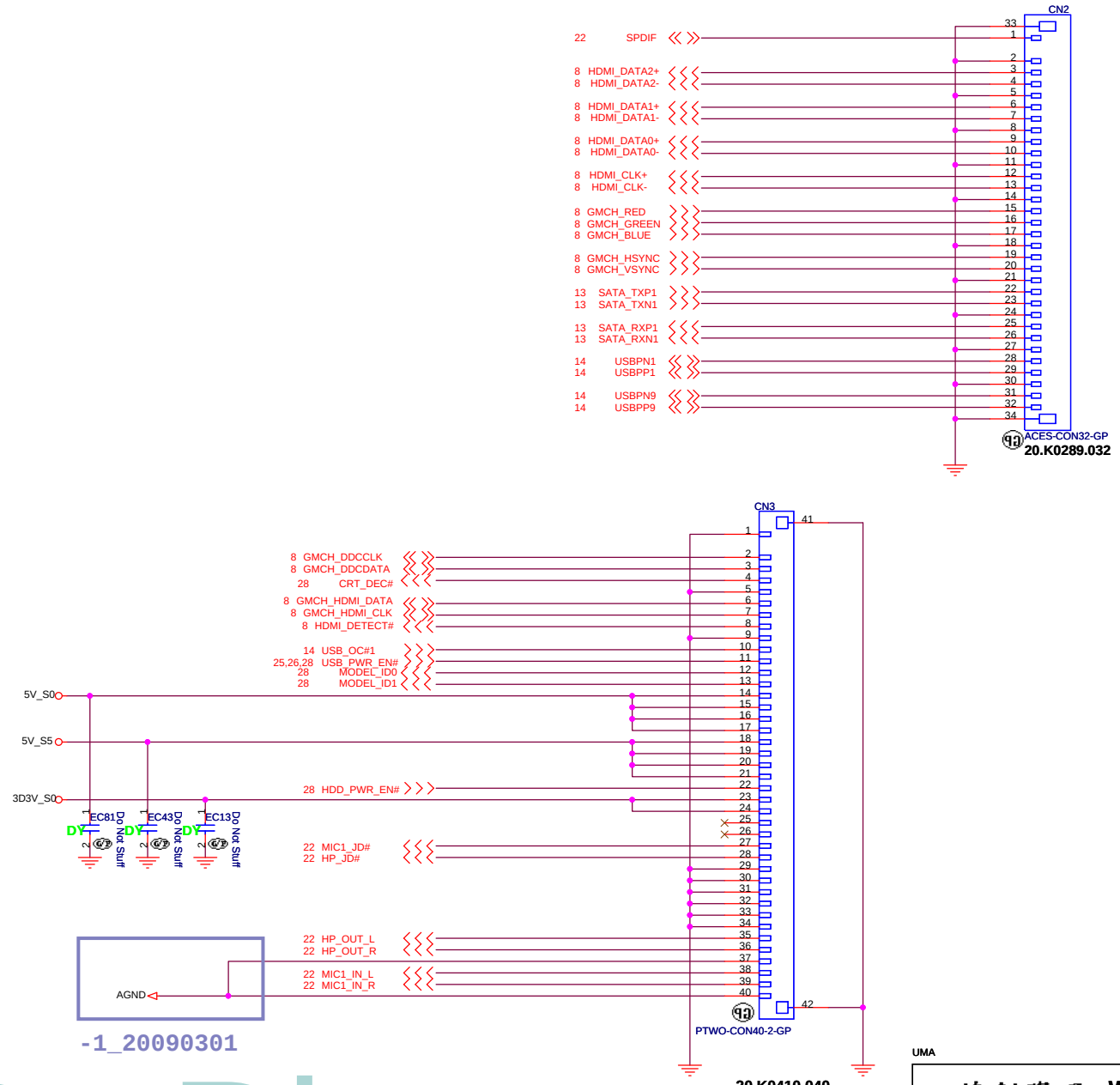

UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title	*CRT BD CONN*	
Size	Document Number: JM41/JM51 UMA	Rev: -2
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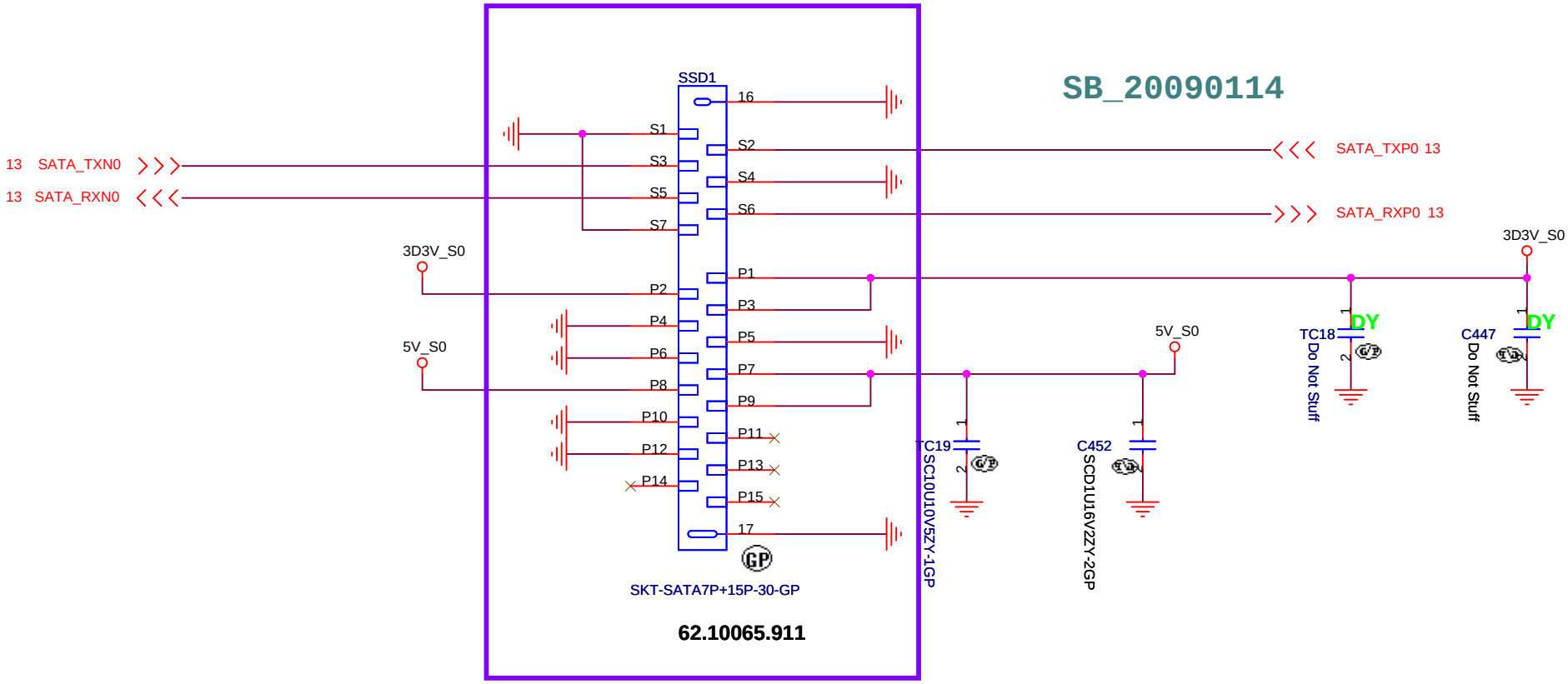
SSD SATA Connector



UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	HDD CONN	
Size	Document Number: JM41/JM51 UMA	Rev: -2
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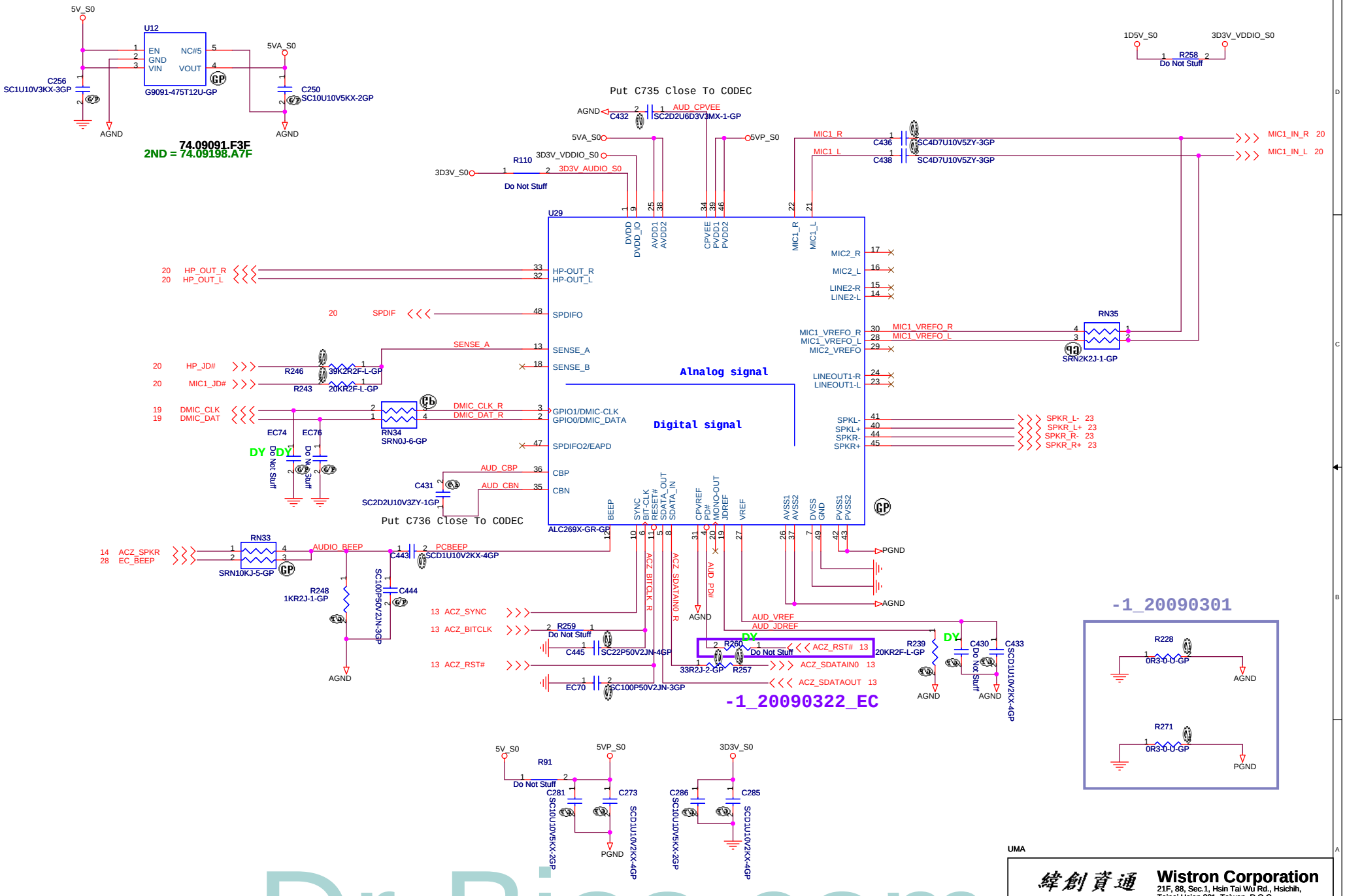

UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *AUDIO CODEC REALTEK ALC269*

Size	Document Number	Rev
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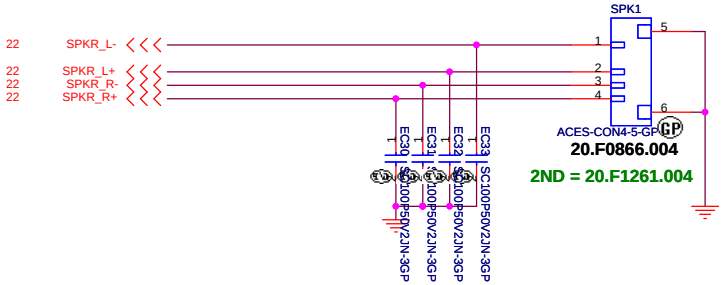
Internal Speaker



UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title	*AUDIO JACK*	
Size	Document Number JM41/JM51 UMA	Rev -2
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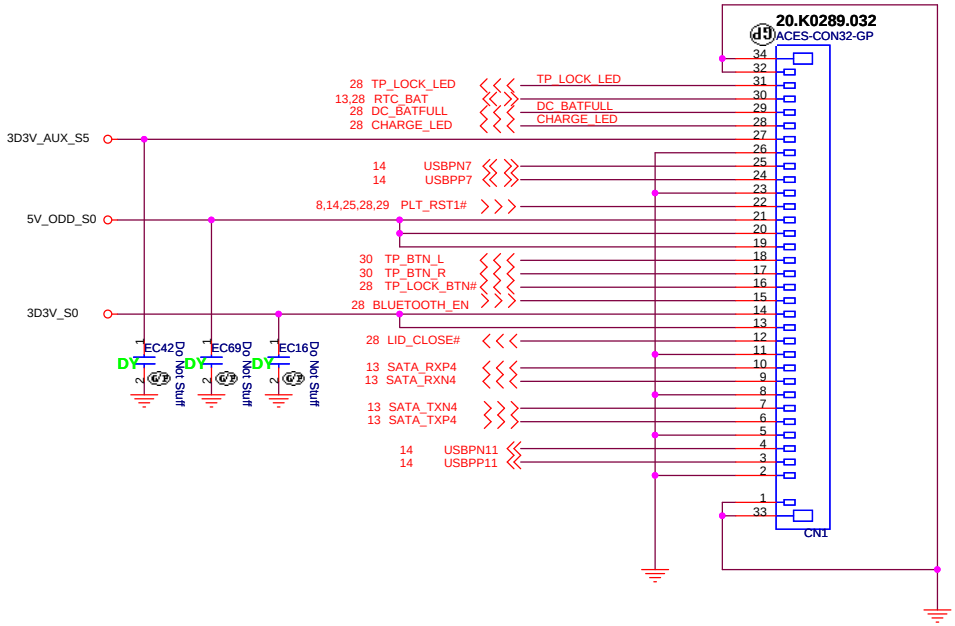

UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*CARDREADER BD CONN*	
Size	Document Number: JM41/JM51 UMA	Rev: -2
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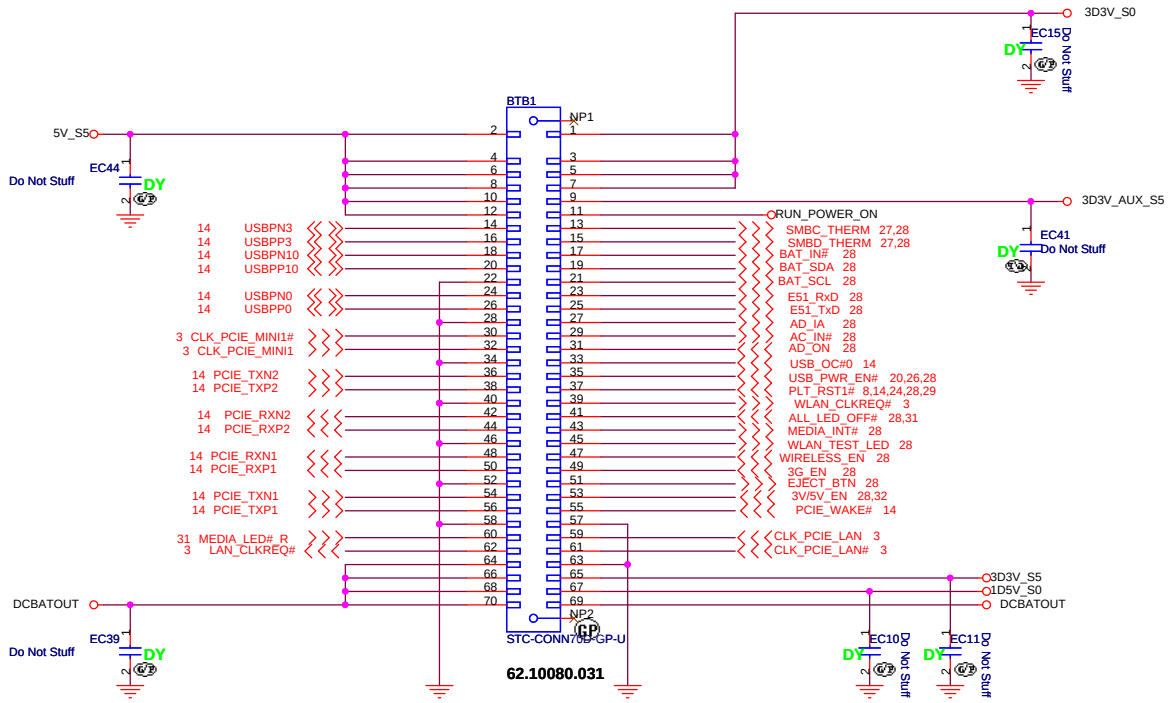

UMA

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***MINI BD CONN***

Size	Document Number	Rev
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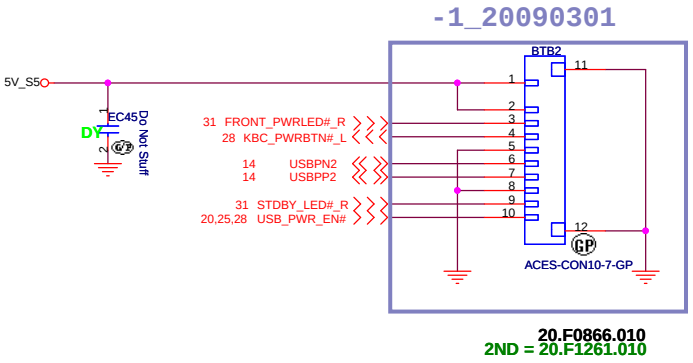

UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***POWER BUTTON CONN***

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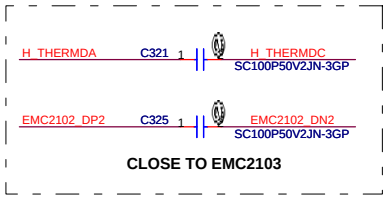
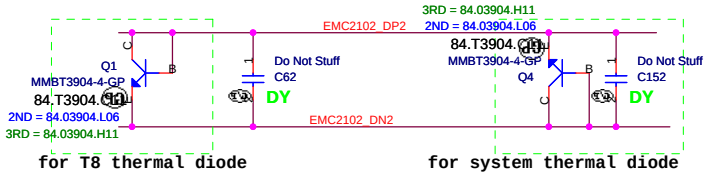
CPU TEMP:

H_THERMDA and H_THERMDC routing 10mil trace width and spacing. Locate Capacity near thermal diode

for CPU thermal diode

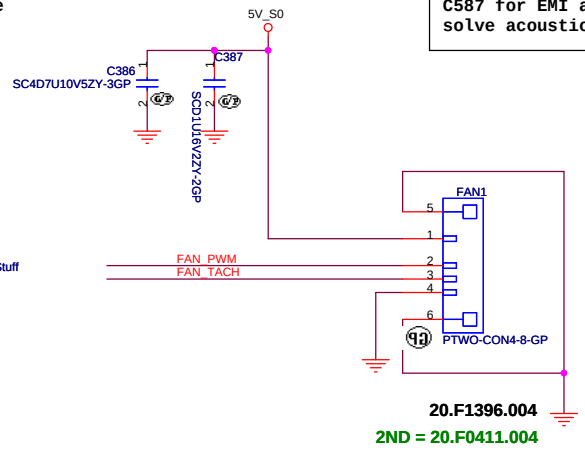
C587 for EMI and solve acoustic noise

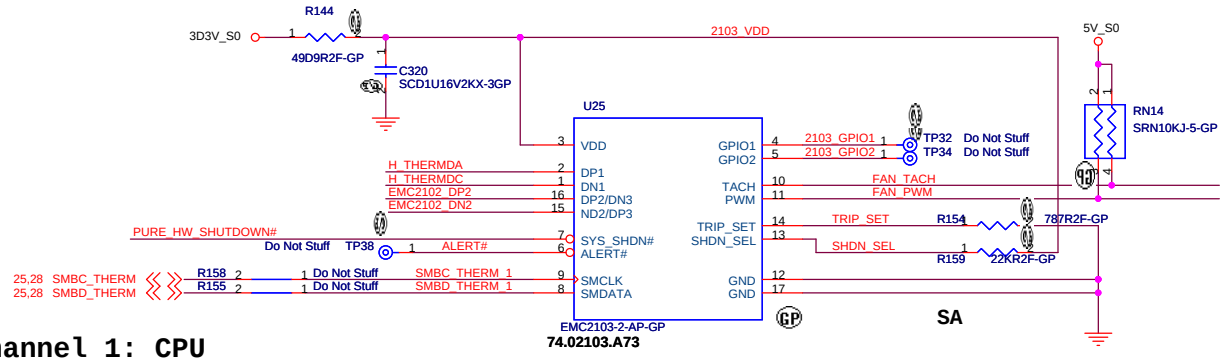




for T8 thermal diode

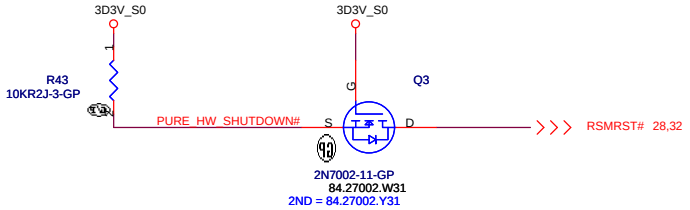
for system thermal diode





ps. FAN1 POWER TRACE WIDTH MAY BE IN 25 MIL

Channel 1: CPU
Channel 2: Palmrest
Channel 3: T8



SHDN_SEL

PULL UP RESISTOR	MODE OF OPERATION
<=4.7K OHM	EXTERNAL DIODE 1 SIMPLE MODE-BETA COMPENSATION DISABLED,REC DISABLED
6.8K OHM	EXTERNAL DIODE 1 DIODE MODE-BETA COMPENSATION DISABLED,REC ENABLED
10K OHM	EXTERNAL DIODE 1 TRANSISTOR MODE-BETA COMPENSATION ENABLED,REC ENABLED
15K OHM	INTERNAL DIODE
22K OHM	EXTERNAL DIODE 2 TRANSISTOR MODE-BETA COMPENSATION ENABLED,REC ENABLED
>=33K OHM	EXTERNAL DIODE 1 TRANSISTOR MODE-BETA COMPENSATION ENABLED,REC ENABLED

TRIP_SET

Ttrip(degree)	RSET(1%)
85	562
86	604
87	649
88	698
89	750
90	787
91	845
92	909
93	953
94	1020
95	1100

UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor

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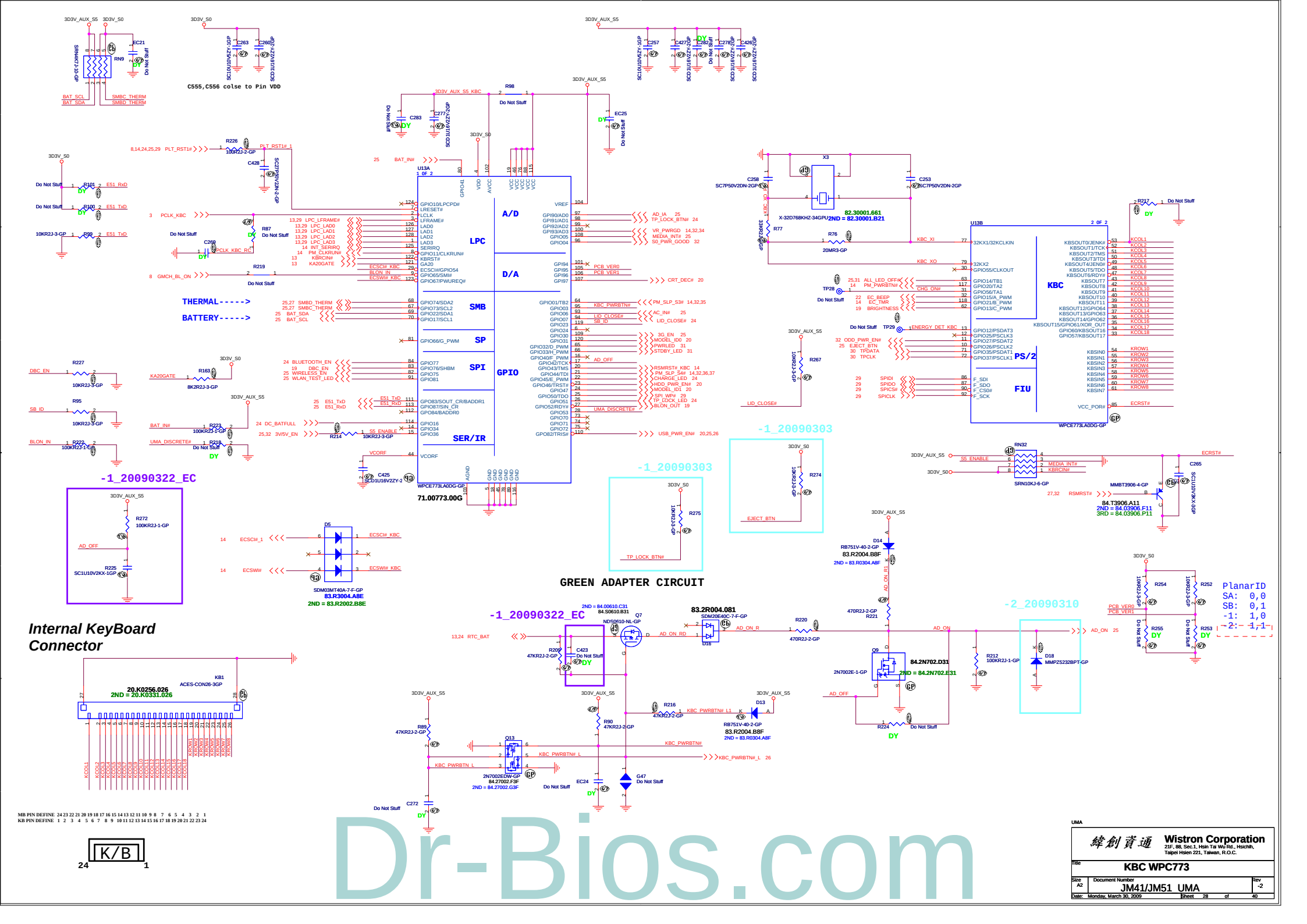
C555,C556 colse to Pin VDD
THERMAL----->
BATTERY----->
-1_20090322_EC
-1_20090303
-1_20090310
GREEN ADAPTER CIRCUIT
Internal KeyBoard Connector
U13A
U13B
WPCE773LA0DG-GP
71.00773.00G
KBC
PS/2
FIU
A/D
D/A
LPC
SMB
SP
SPI
GPIO
SER/IR
X-32D768KHZ-34GPU
82.30001.661
2ND = 82.30001.B21
20.K0256.026
2ND = 20.K0331.026
SDM03MT40A-7-F-GP
83.R3004.A8E
2ND = 83.R2002.B8E
RB751V-40-2-GP
83.R2004.B8F
2ND = 83.R0304.A8F
NDS0610-NL-GP
84.S0610.B31
2ND = 84.00610.C31
2N7002E-1-GP
84.2N702.D31
2ND = 84.2N702.E31
MMBT3906-4-GP
84.T3906.A11
2ND = 84.03906.F11
3RD = 84.03906.P11
2N7002EDW-GP
84.27002.F3F
2ND = 84.27002.G3F
SDM20E40C-7-F-GP
83.2R004.081
MMPZ5232BPT-GP
PlanarID
SA: 0,0
SB: 0,1
-1: 1,0
-2: 1,1
MB PIN DEFINE 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
KB PIN DEFINE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
K/B
24 1
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
KBC WPC773
Size A2
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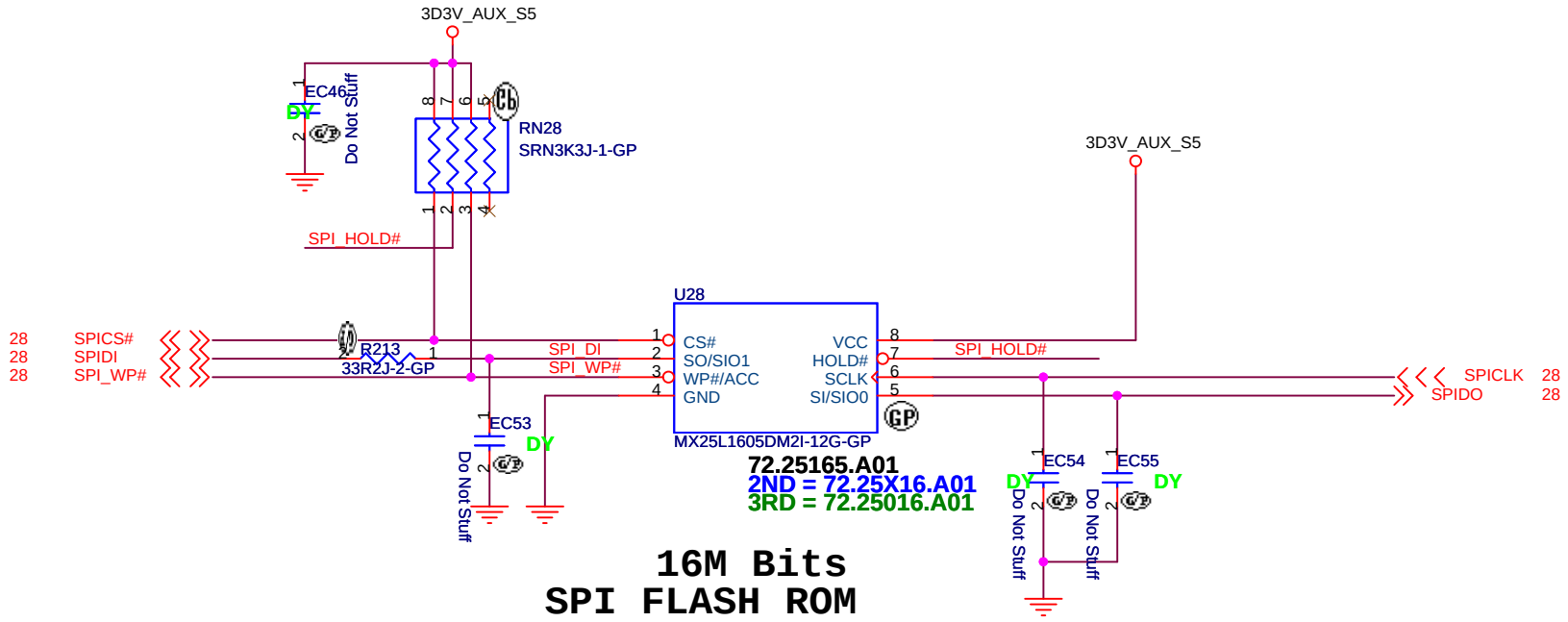
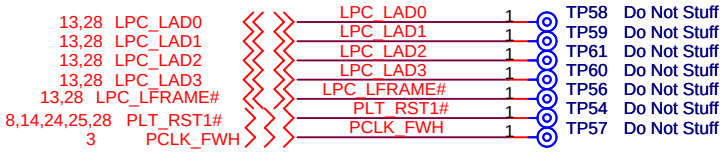
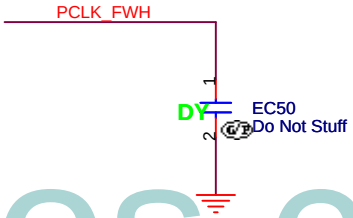


GOLDEN FINGER FOR DEBUG BOARD





UMA

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Title: ***BIOS***		
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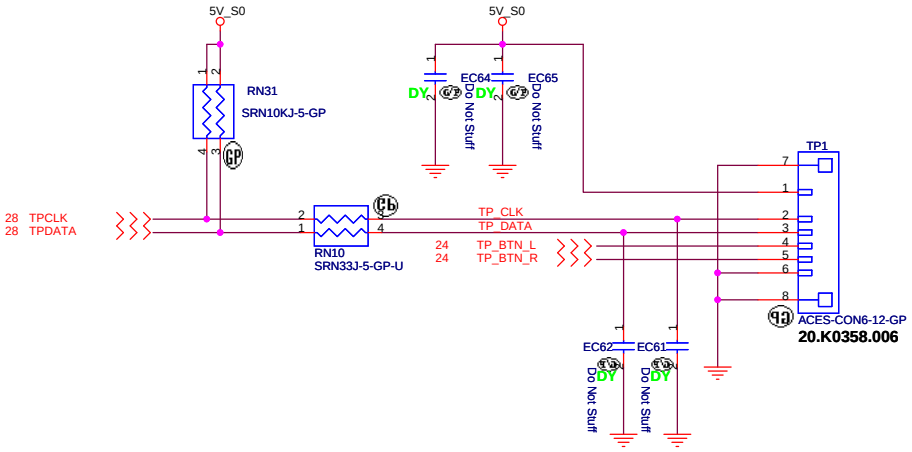
TOUCH PAD



UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title	*Touch PAD*	
Size	Document Number: JM41/JM51 UMA	Rev: -2
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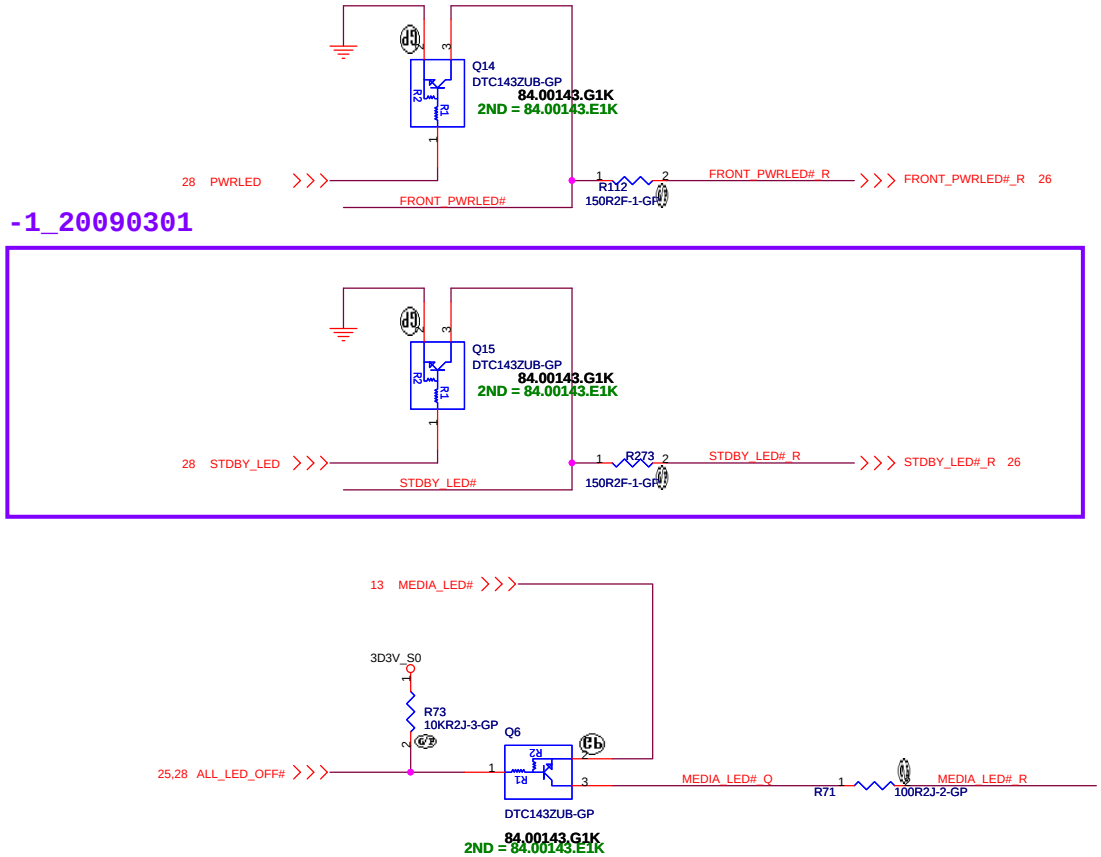

UMA

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Title: **LED**

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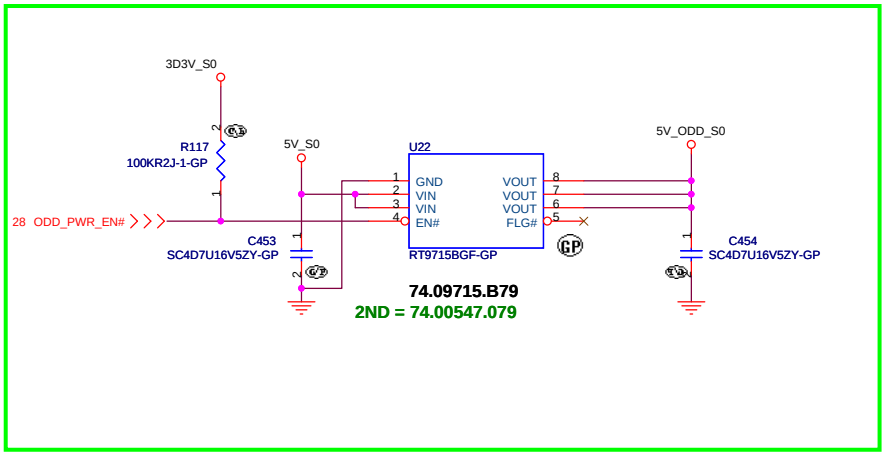
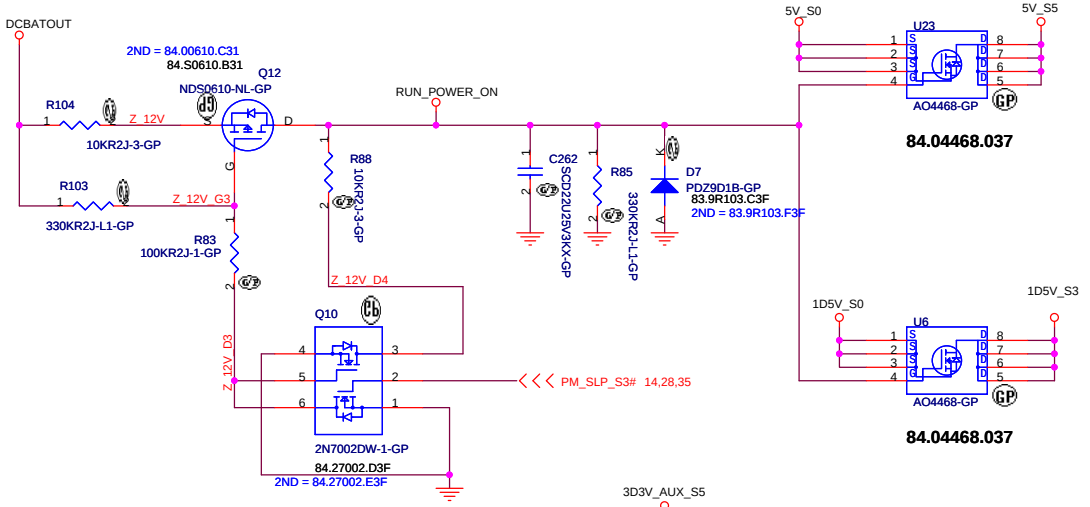
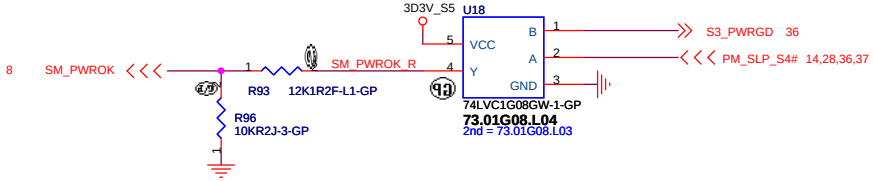
ODD Power

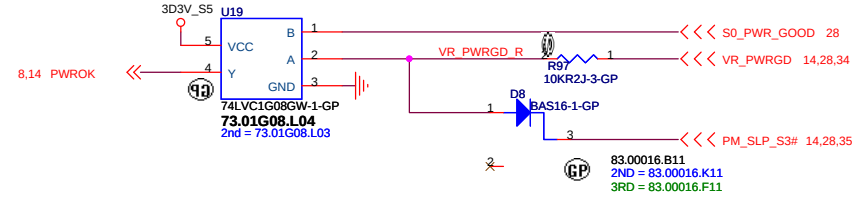


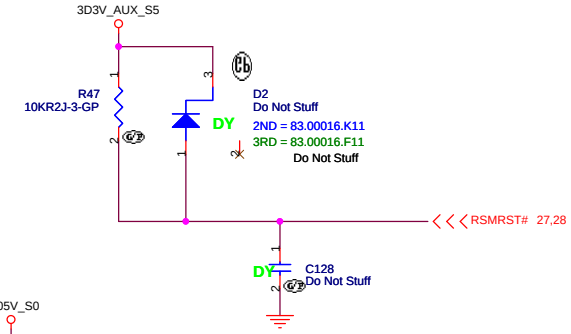
-2_20090310

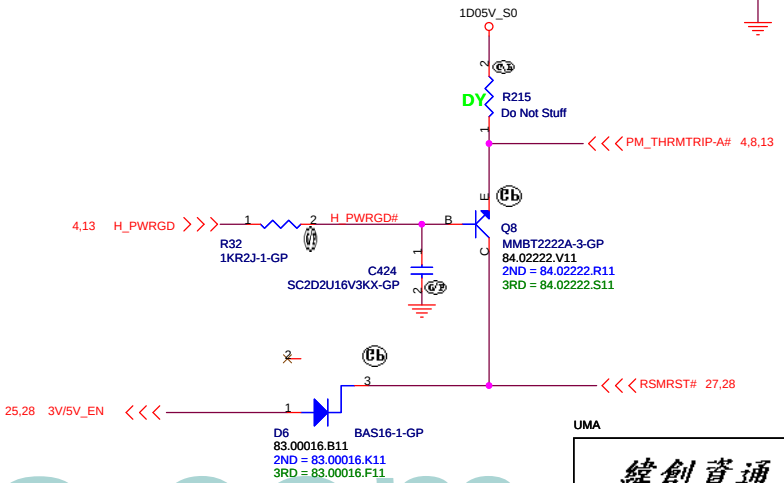
Run Power











UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	RUN & ODD POWER	
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CPU_CORE
ISL6261A

VID0
VID1
VID2
VID3
VID4
VID5
VID6

CPUCORE_ON

VCC_SENSE
VSS_SENSE

DCBATOUT_6261A
5V_S0
3D3V_S0

VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
VID5(I / 3.3V)
VID6(I / 3.3V)

Input Signal
EN (I / 3.3V)

Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)

Input Power
VCC(I)
VCC(I)
VCC(I)

Output Signal
PGOOD

VR_PWROK

Output Power
VCC_CORE_PWR(O)

VCC_CORE(Imax=18A)

RT8202 1D05V_S0

DCBATOUT_8202_1D05V
PM_SLP_S3#

VIN
EN
1D5V(O)
PGOOD

1D05V_S0 (10A)
CPUCORE_ON

RT8202 1D5V_S3

DCBATOUT_8202_1D5V
PM_SLP_S4#

VIN
EN
1D5V(O)
PGOOD

1D5V_S3 (11A)
CPUCORE_ON

GFX_CORE
ISL6263A

VID0
VID1
VID2
VID3
VID4

5V_S0
DCBATOUT_6263A

PM_SLP_S3#
GFXVR_EN

VCC_AXG_SENSE
VSS_AXG_SENSE

VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)

Input Power
VDD
VIN

Input Signal
VR_ON

Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)

Output Signal
PGOOD

CPUCORE_ON

Output Power
VGFXCORE (O)

VCC_GFXCORE(7A)

RT9026 0D9V_S0

5V_S5
1D5V_S3
PM_SLP_S4#

VIN
VLDOIN
S3
S5
VTT
VTTREF

0D75V_S3 (1.2A)
0D75V_S3_1

Charger MAX8731A

CHG_ON#
24750_CELLS

AD+

Input Signal
CHGEN#
CELLS

Input Power
ACN

Output Signal
ACGOOD#
SRSET

Output Power
VOUT (O)
VOUT (O)

AC_IN#
AD_IA

BT+
DCBATOUT

TPS51125
5V/3D3V

DCBATOUT_51125
S5_ENABLE
ALW_PWRGD_3V_5V

Input Power
VIN

Input Signal
EN0

Output Signal
PGOOD

Output Power
5V(O)
3D3V(O)
5V(O)
3D3V(O)

5V_S5 (6A)
3D3V_S5 (5A)
5V_AUX_S5
3D3V_AUX_S5

Adapter

AD_OFF
AD_JK
5V_AUX_S5

Input Signal
(I)

Input Power
VCC(I)
VCC(I)

Output Signal
(O)

Output Power
VCC(O)

AD_IN#
AD+

UMA

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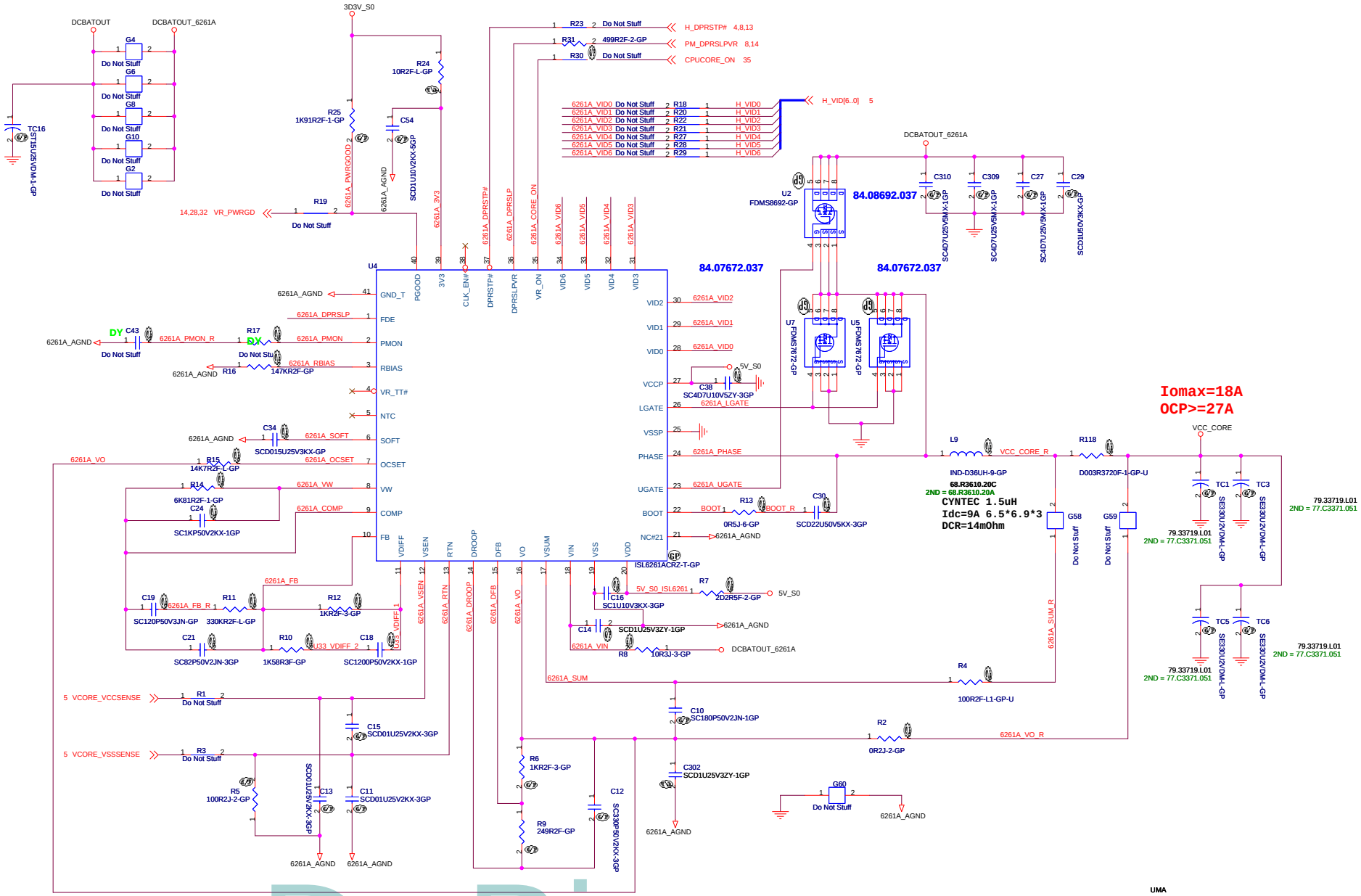
Title: **Power Sequence Logic**

Size: B | Document Number: JM41/JM51_UMA | Rev: -2

Date: Thursday, March 19, 2009 | Sheet 33 of 40



UMA

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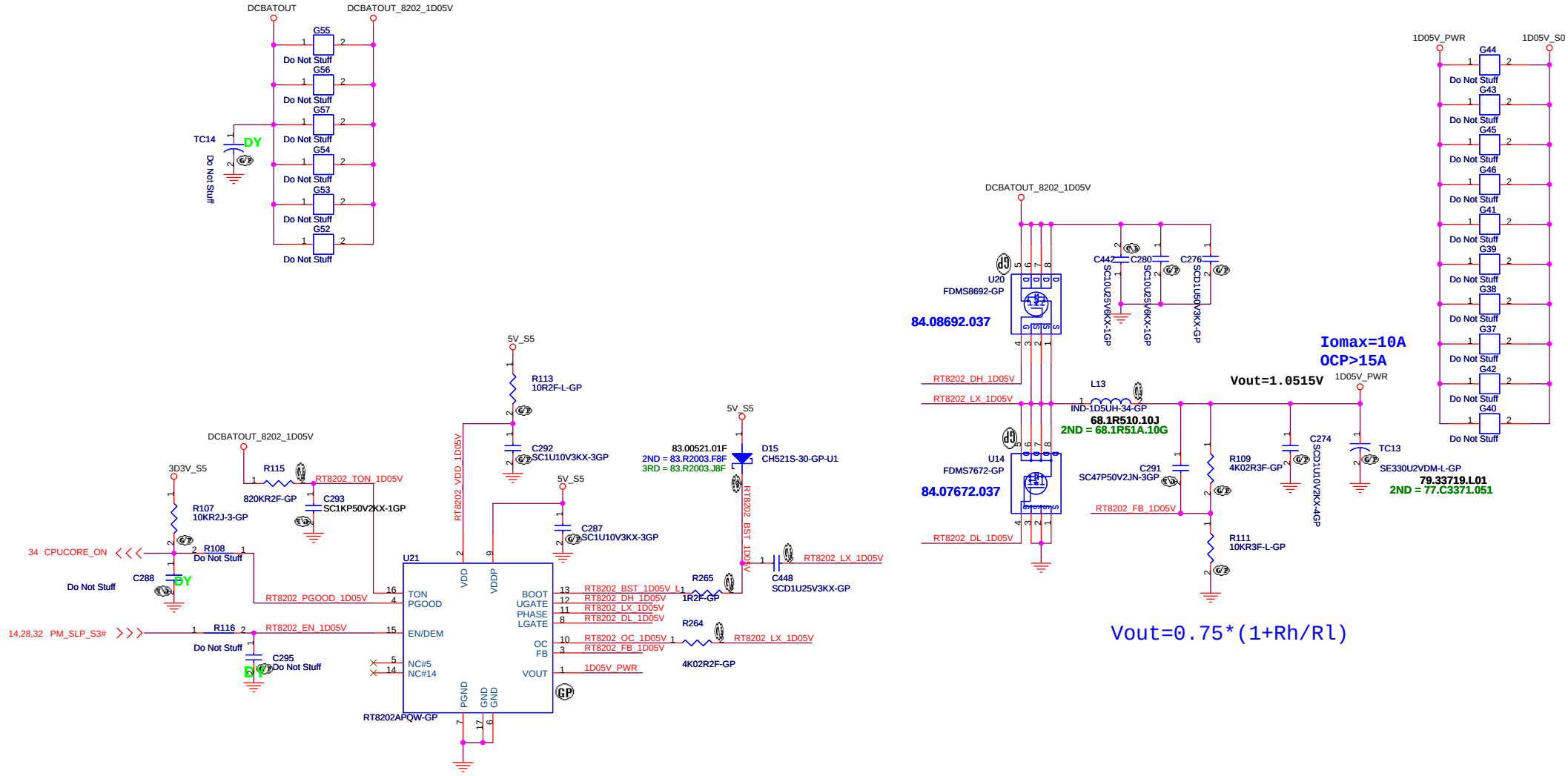
Title: ISL6261A_CPU CORE

Size: Custom | Document Number: JM41/JM51_UMA | Rev: -2

Date: Monday, March 30, 2009 | Sheet 34 of 40



UMA

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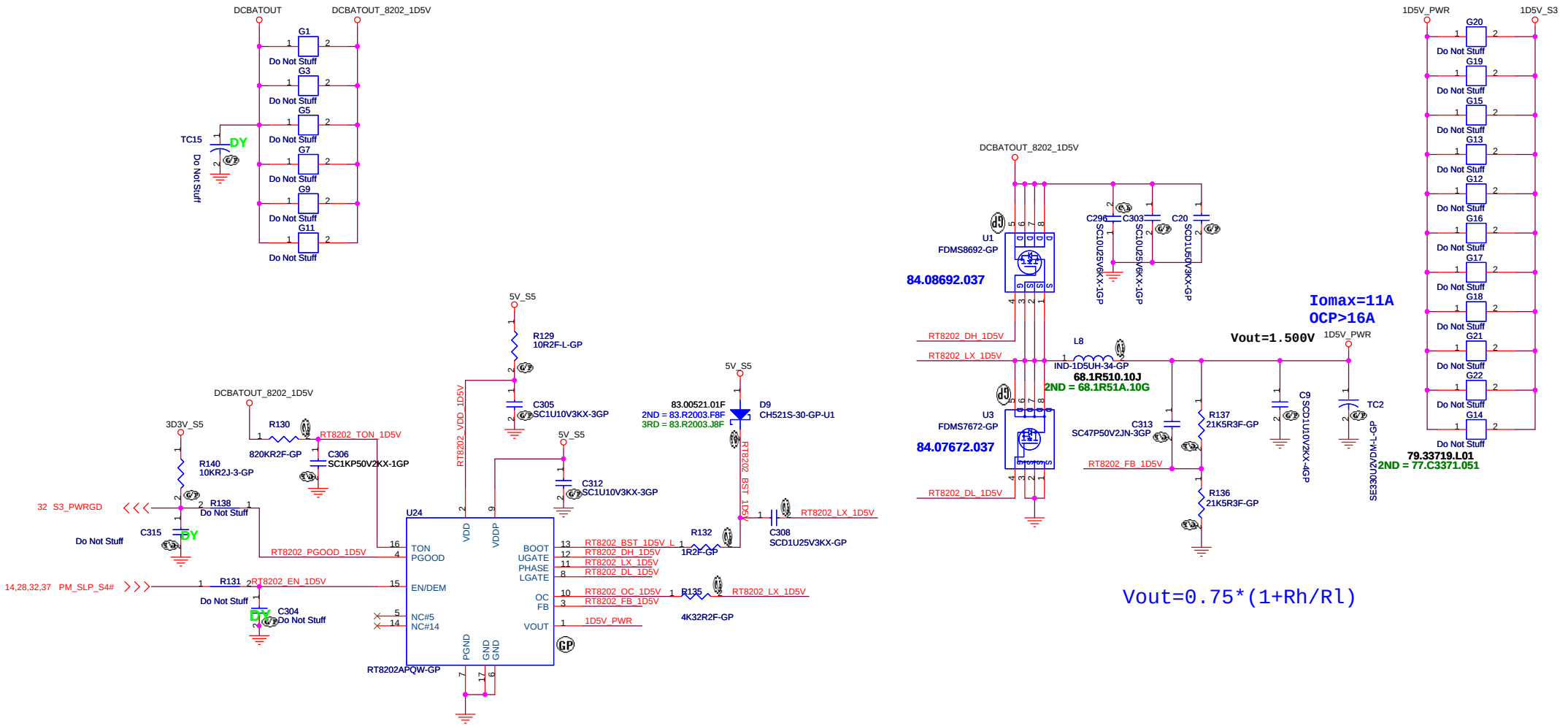
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8202_1D05V

Size	Document Number	Rev
A3	JM41/JM51_UMA	-2

Date: Thursday, March 26, 2009 Sheet 35 of 40



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Title: RT8202_1D5V

Size	Document Number	Rev
A3	JM41/JM51_UMA	-2

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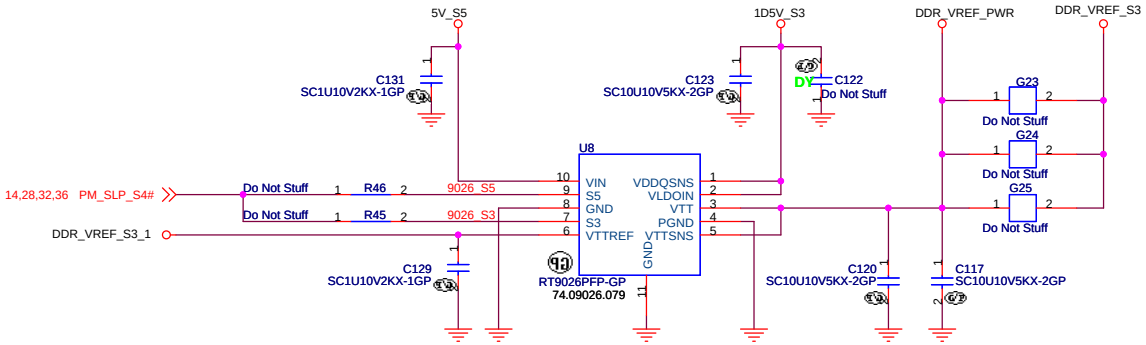
OCP>2A



UMA

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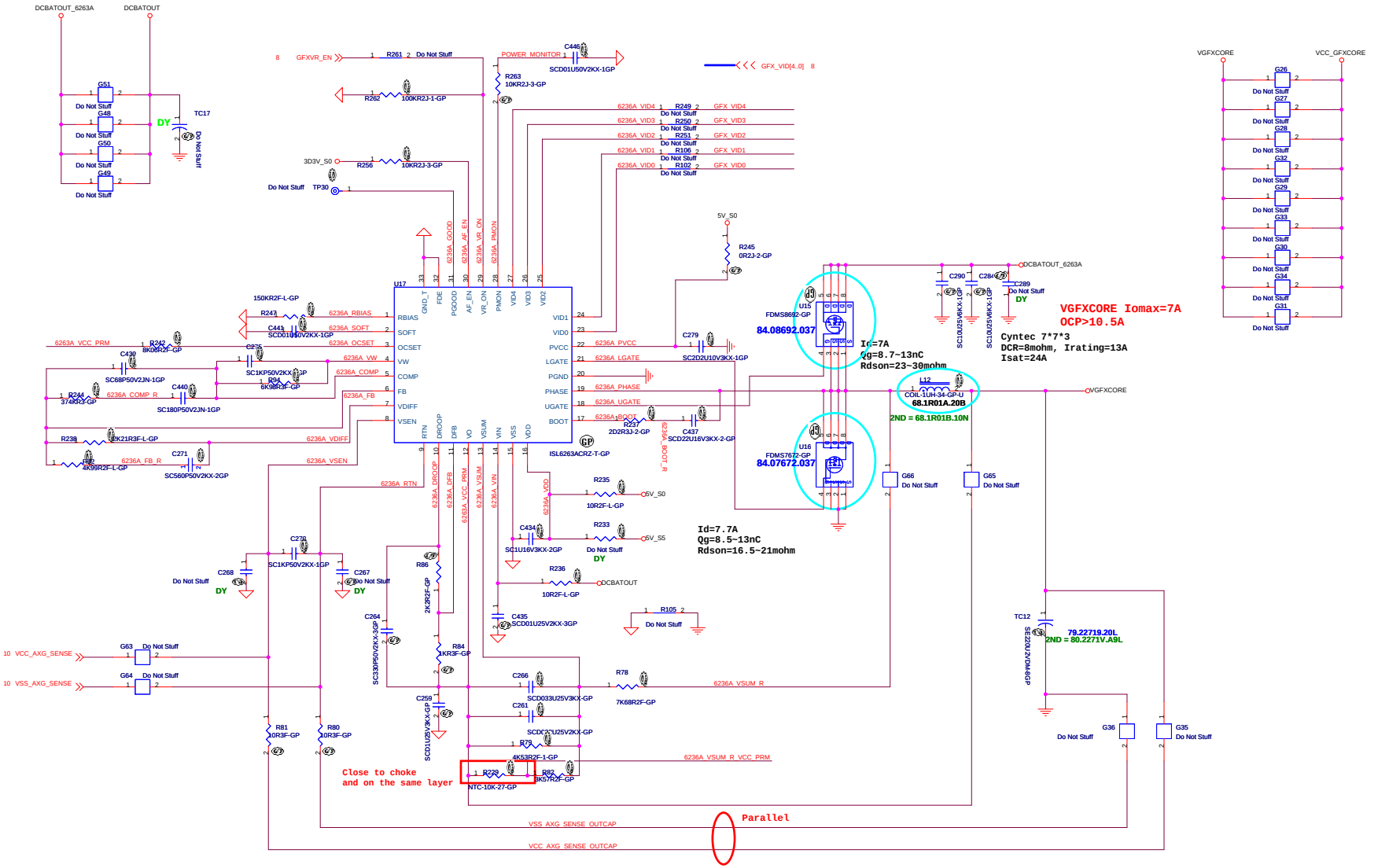
Title: ***RT9026_0D75V***

Size: A3 | Document Number: **JM41/JM51_UMA** | Rev: -2

Date: Thursday, March 26, 2009 | Sheet 37 of 40



UMA

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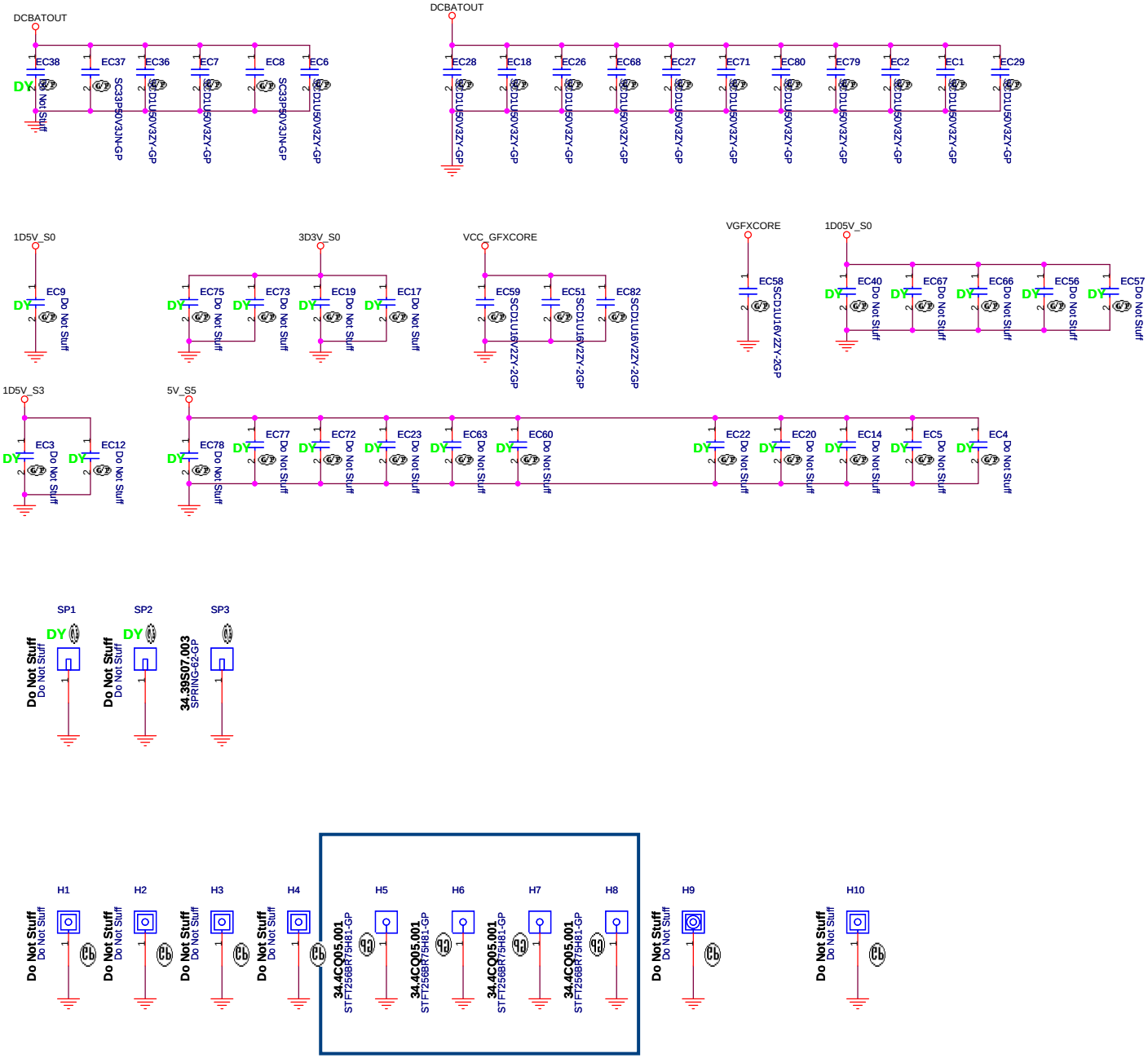
Title: ISL6263A_GFX CORE

Size: A2 | Document Number: JM41/JM51_UMA | Rev: -2

Date: Thursday, March 26, 2009 | Sheet 38 of 40



UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *EMI/Spring/Boss*

Size | Document Number: JM41/JM51 UMA | Rev: -2

Date: Thursday, March 26, 2009 | Sheet 39 of 40