Storm
UMA Schematics Document
Chief River
Intel PCH

8G:FOR 8G DIMM

STORM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cover Page

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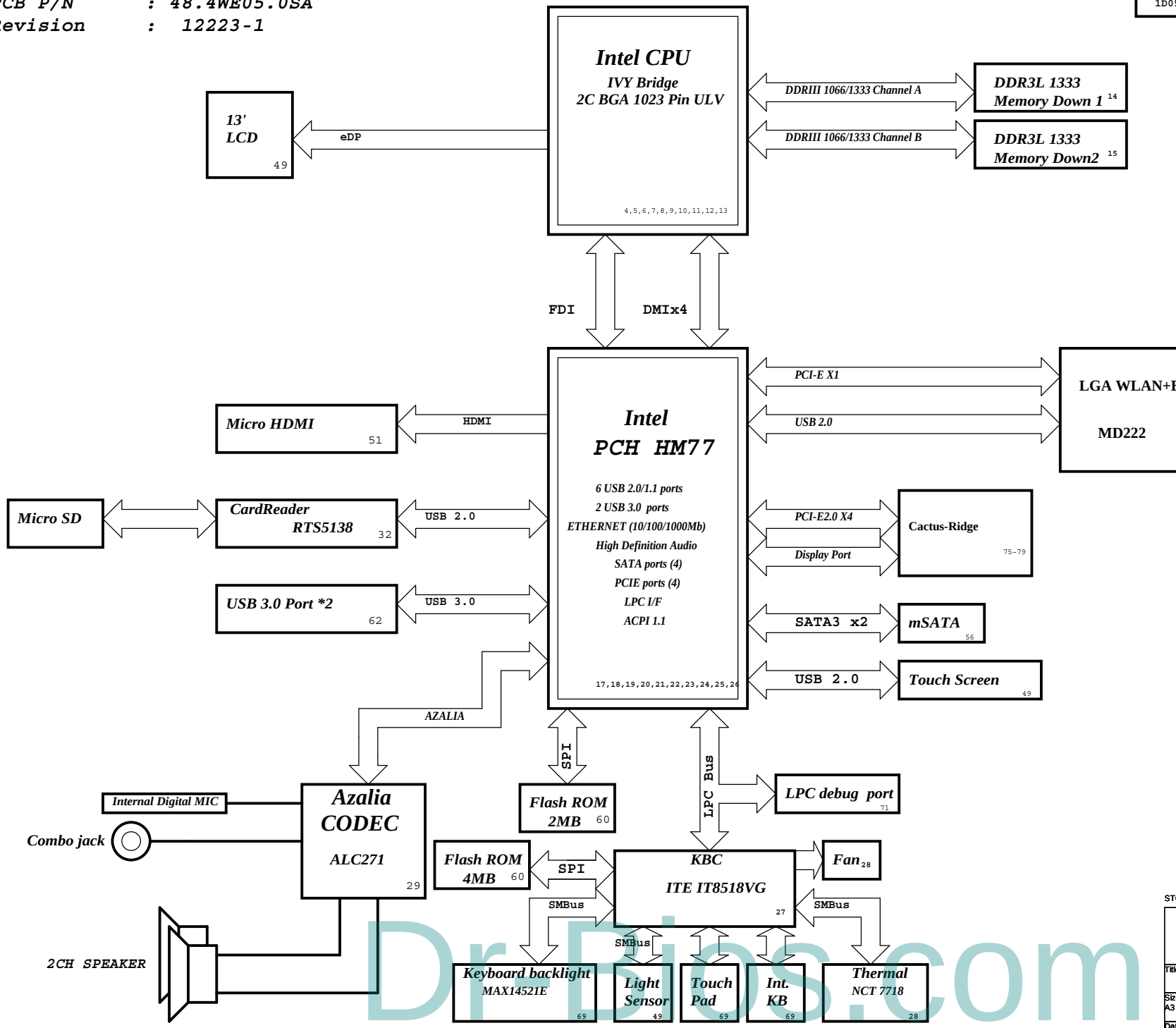
Project code : 91.4WE01.001
PCB P/N : 48.4WE05.0SA
Revision : 12223-1

Storm Block Diagram



SYSTEM DC/DC APL5916KAI 48	
INPUTS	OUTPUTS
1D05V_PWR	0D85V_S0

CPU DC/DC NCP6131S52MNR 42~43	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC UP6128PQDD 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC UP6183PQAG 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC UP6165BQKF 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

SYSTEM DC/DC NCP5911MNTBG 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE_PWR

VGA RT8208BGQW 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

TI CHARGER BQ24745RHDR 40	
INPUTS	OUTPUTS
DCBATOUT	BT+

SYSTEM DC/DC RT9025 47	
INPUTS	OUTPUTS
3D3V_S0	1D8V_S0

SYSTEM DC/DC RT9025-25PSP 93	
INPUTS	OUTPUTS
1D5V_S3	1V_VGA_S0
3D3V_S5	1D8V_VGA_S0

Switches	
INPUTS	OUTPUTS
1D5V_S3	1D5V_VGA_S0
3D3V_S0	3D3V_VGA_S0

PCB LAYER

L1:Top	L6:Signal
L2:VCC	L7:GND
L3:Signal	L8:Signal
L4:VCC	L9:GND
L5:Signal	L10:Bottom

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PCH Strapping

Huron River Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN#/GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Huron River Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	0
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	1

POWER PLANE	VOLTAGE	Voltage Rails ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

PCIE Routing

LANE1	N/A
LANE2	N/A
LANE3	N/A
LANE4	WLAN
LANE5	Thunderbolt
LANE6	Thunderbolt
LANE7	Thunderbolt
LANE8	Thunderbolt

SATA Table

SATA	
Pair	Device
0	mSATA1
1	mSATA2
2	N/A
3	N/A
4	N/A
5	N/A

USB Table

Pair	Device
0	USB3.0 Ext. port 1
1	USB3.0 Ext. port 2
2	NC
3	NC
4	Card Reader
5	WLAN+BT
6	CCD
7	X
8	X
9	NC
10	NC
11	NC
12	NC

SMBus ADDRESSES

I² C / SMBus Addresses Device	Ref Des	HURON RIVER ORB Address	Hex	Bus
EC SMBus 1 Battery CHARGER				BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP				SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI				PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

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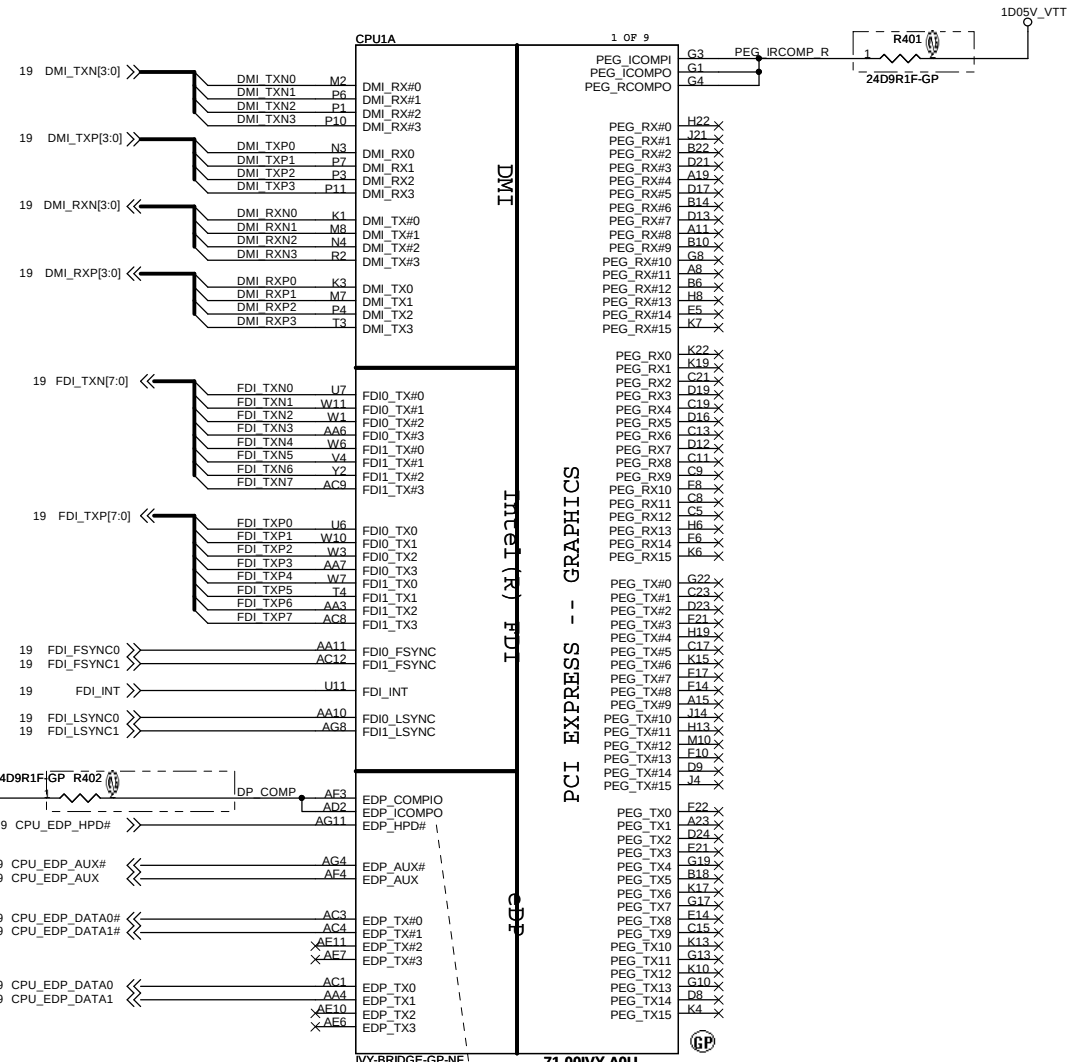
SSID = CPU

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.



Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Lane reversal does not apply to FDI sideband signals.

Impedance:85 ohm

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE:
Select a Fast FET similar to 2N7002E whose rise/ fall time is less than 6 ns. If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up resistor on the motherboard.

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Title: **CPU (PCIE/DMI/FDI)**

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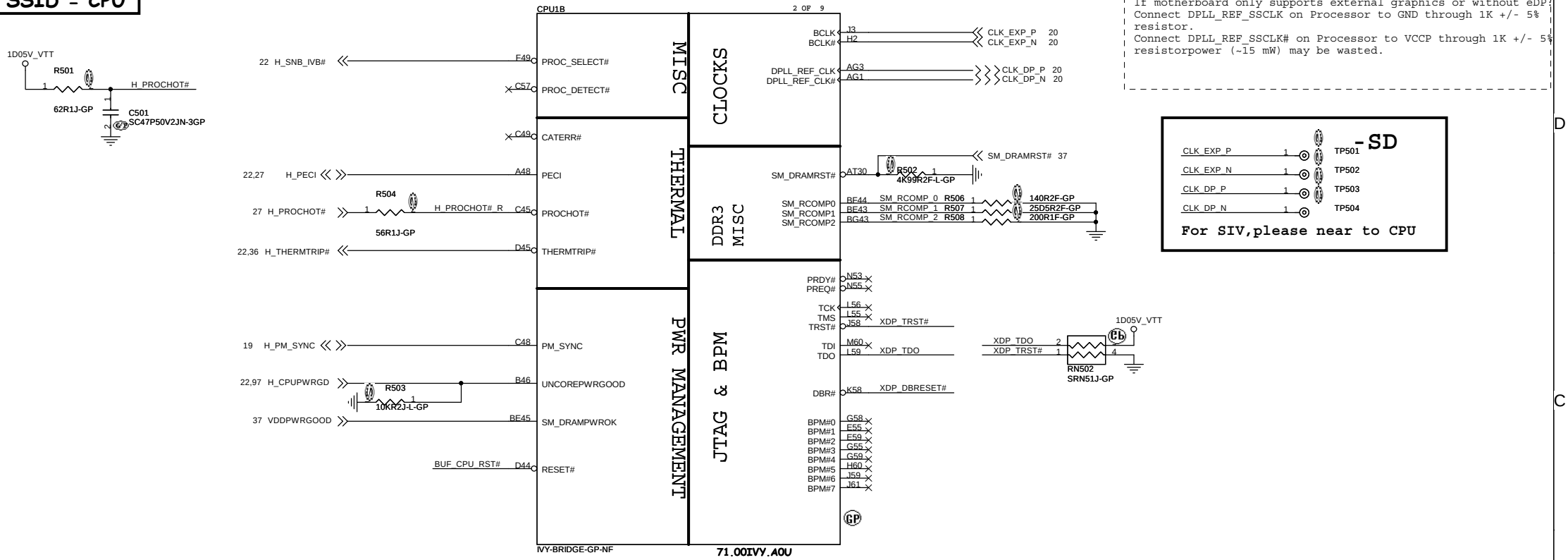
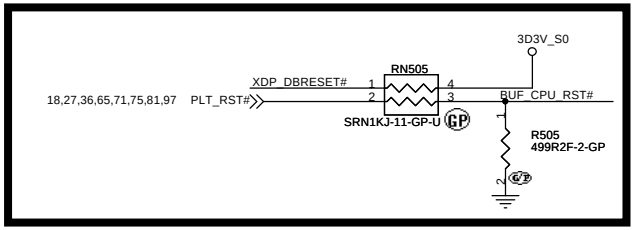
SSID = CPU

Disabling Guidelines:
If motherboard only supports external graphics or without eDP:
Connect DPLL_REF_SSCLK on Processor to GND through 1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K +/- 5% resistorpower (~15 mW) may be wasted.





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Title	CPU (THERMAL/CLOCK/PM)
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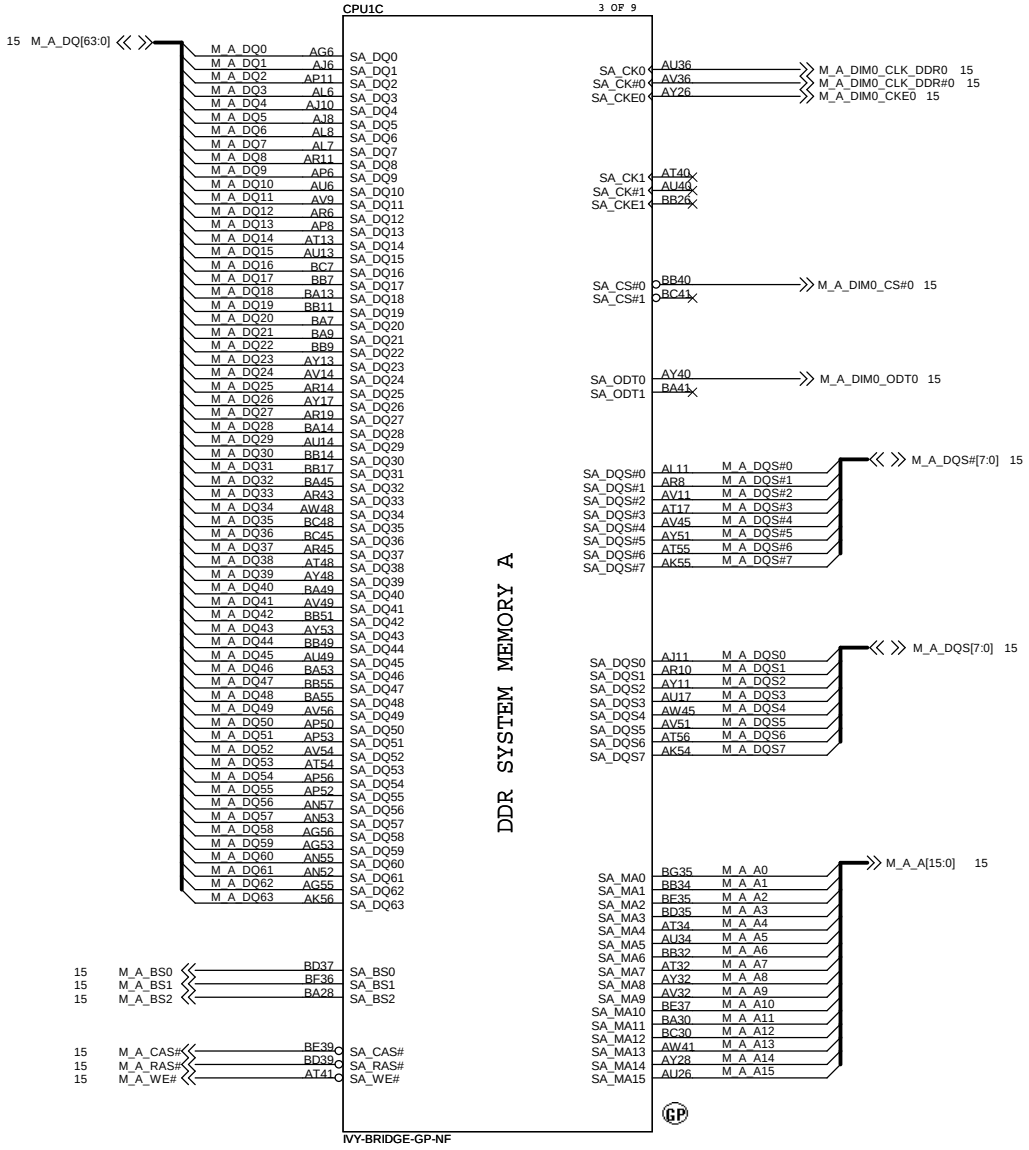
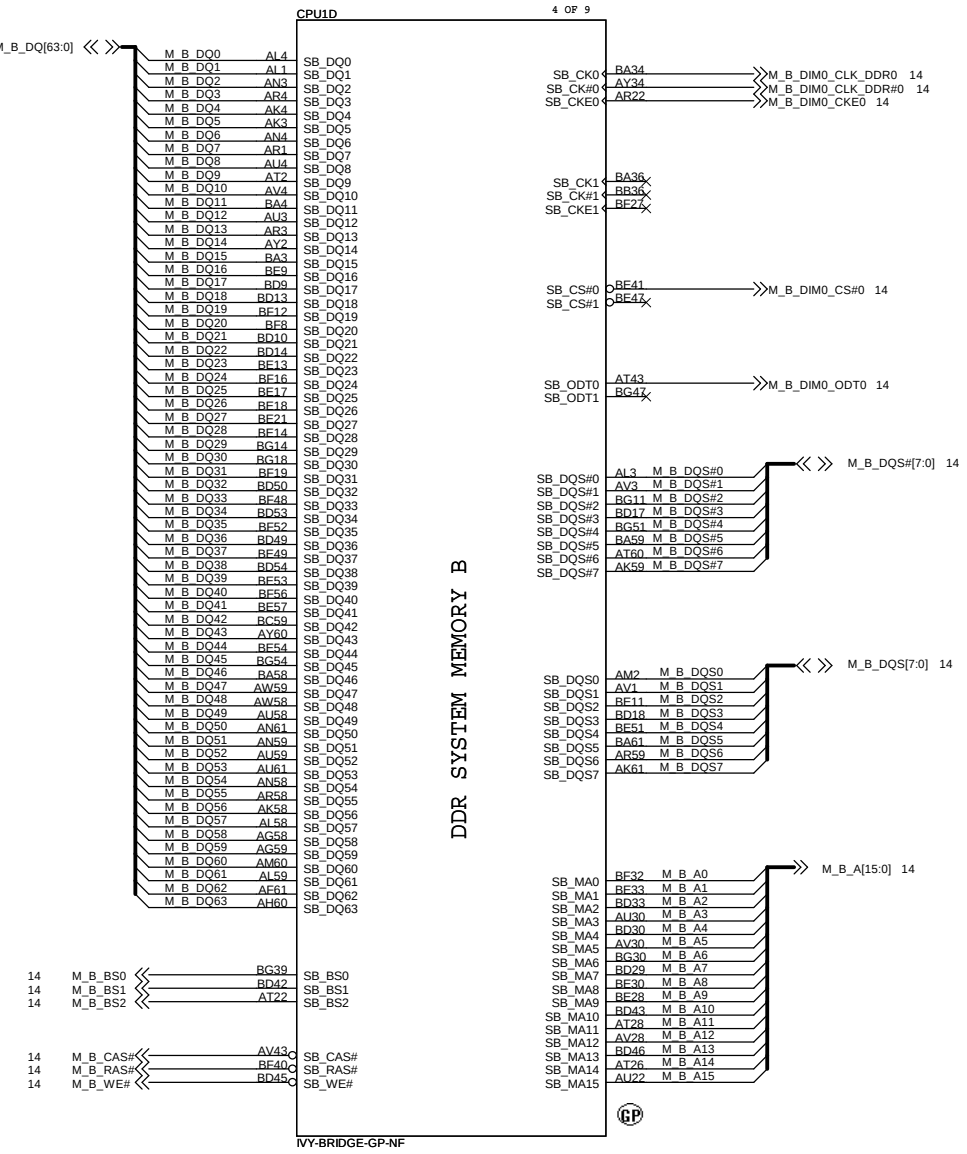
SSID = CPU





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Title: CPU (DDR)

Size: A3 | Document Number: Storm | Rev: -1

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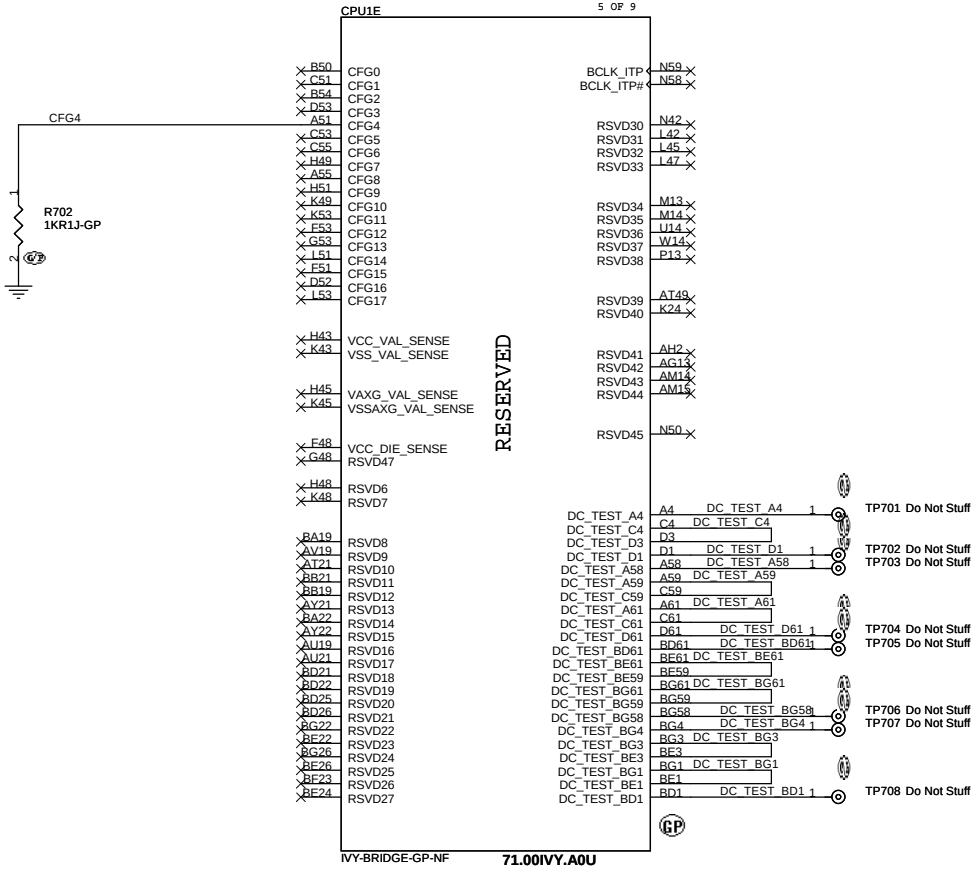
SSID = CPU



Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[0]		Connect a series 1 kOhms resistor on the critical CFG[0 trace in a manner which does not introduce any stubs to CFG[0] trace. Route as needed from the opposite side of this series isolation resistor to the debug port. ITP will drive the net to GND.	
CFG[2]	PCIe Static x16 Lane Numbering Reversal.	1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed	0
CFG[4]	Display Port Presence strap	1:Disabled - No Physical Display Port attached to Embedded DisplayPort No connect for disable 0:Enabled - An external Display Port device is connected to the Embedded Display Port Pull-down to GND through a 1KΩ ± 5% resistor to enable port	0
CFG[6:5]	PCI-Express Port Bifurcation Straps	00 = 1 x 8, 2 x 4 PCI Express 01 = reserved 10 = 2 x 8 PCI Express 11 = 1 x 16 PCI Express	00
CFG[17:7]	Reserved configuration lands. A test point may be placed on the board for these lands.		

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Title: CPU (RESERVED)

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SSID = CPU

POWER

ULV:14W
Iccmax:33A
ICC_TDC:25A

Iccmax:8.5A
ICC_TDC:8.5A

CPU1F

6 OF 9

CORE SUPPLY

PEG IO AND DDR IO

QUIET RAILS

SVID

SENSE LINES

VCC_CORE

1D05V_VTT

change 0603 to 0402

Layout Note: 2.2u Cap place under CPU

6 2D2U to 3 4D7U

	PIn BC22	CPU
1.05V	H	SNB
1V	L	IVB

1.05V_VTT Power rail

CPU EDS desing guide Rev change 1 V to 1.05V

PROCESSOR 1.05V Quiet rail for DDR block (BGA only)
+V1.05S_VCCPQE should be short to +V1.05S_VCCP_DDR_R on board

Place near processor

Place near processor

IVY-BRIDGE-GP-NF

71.00IVY.A0U

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Title: CPU (VCC_CORE)

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SSID = CPU

POWER

CPU1G

7 OF 9

Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT should have 10 mils trace width.

VREF

SM_VREF AY43 +V_SM_VREF_CNT → +V_SM_VREF_CNT 37

SA_DIMM_VREFDQ BE7 M_VREF_DQ_DIMM0_C → M_VREF_DQ_DIMM0_C 37
SB_DIMM_VREFDQ BG7 M_VREF_DQ_DIMM1_C → M_VREF_DQ_DIMM1_C 37

RN901 Do Not Stuff DY

DDR3 - 1.5V RAILS

VDDQ1 AJ28
VDDQ2 AJ33
VDDQ3 AJ36
VDDQ4 AJ40
VDDQ5 AL30
VDDQ6 AL34
VDDQ7 AL38
VDDQ8 AL42
VDDQ9 AM33
VDDQ10 AM36
VDDQ11 AM40
VDDQ12 AN30
VDDQ13 AN34
VDDQ14 AN38
VDDQ15 AR26
VDDQ16 AR28
VDDQ17 AR30
VDDQ18 AR32
VDDQ19 AR34
VDDQ20 AR36
VDDQ21 AR40
VDDQ22 AV41
VDDQ23 AW26
VDDQ24 BA40
VDDQ25 BB28
VDDQ26 BG33

1D35V_S0

Iccmax:5A

C912 SC10U06D3V2MX-GP-U
C911 SC10U06D3V2MX-GP-U
C910 SC10U06D3V2MX-GP-U
C909 SC10U06D3V2MX-GP-U
C928 SC10U06D3V2MX-GP-U
C927 SC10U06D3V2MX-GP-U
C929 SC10U06D3V2MX-GP-U

1D35V_S0

C931 C932 C933 C934 C935 C936 C937 C938 C939 C940 SC1U10V2KX-1GP

GRAPHICS

VAXG1 AA46
VAXG2 AB47
VAXG3 AB50
VAXG4 AB51
VAXG5 AB52
VAXG6 AB53
VAXG7 AB55
VAXG8 AB56
VAXG9 AB58
VAXG10 AB59
VAXG11 AC61
VAXG12 AD47
VAXG13 AD48
VAXG14 AD50
VAXG15 AD51
VAXG16 AD52
VAXG17 AD53
VAXG18 AD55
VAXG19 AD56
VAXG20 AD58
VAXG21 AD59
VAXG22 AE46
VAXG23 N45
VAXG24 P47
VAXG25 P48
VAXG26 P50
VAXG27 P51
VAXG28 P52
VAXG29 P53
VAXG30 P55
VAXG31 P56
VAXG32 P61
VAXG33 T48
VAXG34 T58
VAXG35 T59
VAXG36 T61
VAXG37 U46
VAXG38 V47
VAXG39 V48
VAXG40 V50
VAXG41 V51
VAXG42 V52
VAXG43 V53
VAXG44 V55
VAXG45 V56
VAXG46 V58
VAXG47 V59
VAXG48 W50
VAXG49 W51
VAXG50 W52
VAXG51 W53
VAXG52 W55
VAXG53 W56
VAXG54 W61
VAXG55 Y48
VAXG56 Y61

Iccmax:18A(GT1)
ICC_TDC:12A(GT1)

VCC_GFXCORE

C901 Do Not Stuff DY
C902 SC1U10V2KX-1GP
C903 Do Not Stuff DY
C904 C905 C906 C907 SC1U10V2KX-1GP

C908 C920 C921 C922 C926 SC1U10V2KX-1GP

C944 Do Not Stuff DY
C943 Do Not Stuff DY
C930 SC10U06D3V2MX-GP-U
C945 SC10U06D3V2MX-GP-U

SENSE LINES

VAXG_SENSE VAXG_SENSE F45
VSSAXG_SENSE VSS_AXG_SENSE G45

42 VCC_AXG_SENSE
42 VSS_AXG_SENSE

VCC_GFXCORE
R901 100R1F-GP
R902 100R1F-GP

1.8V RAIL

1D8V_S0

ICC_MAX:1.2A

VCCPLL1 BB3
VCCPLL2 BC1
VCCPLL3 BC4

C963 C964 SC10U06D3V2MX-GP-U SC1U10V2KX-1GP

SA RAIL

0D85V_S0

ICC_MAX:6A

VCCSA1 L17
VCCSA2 L21
VCCSA3 N16
VCCSA4 N20
VCCSA5 N22
VCCSA6 P17
VCCSA7 P20
VCCSA8 R16
VCCSA9 R18
VCCSA10 R21
VCCSA11 U15
VCCSA12 V16
VCCSA13 V17
VCCSA14 V18
VCCSA15 V21
VCCSA16 W20

C942 C941 C940 C939 C938 C937 C936 C935 C934 SC1U10V2KX-1GP
C918 SC10U06D3V2MX-GP-U

QUIET RAILS

VCCDQ1 AM28
VCCDQ2 AN26

+1.5S_VCCD_Q

1D35V_S0

R907 Do Not Stuff
C919 SC1U6D3V2KX-L-1-GP

PROCESSOR DDR 1.5V QUIET RAIL (BGA only)
+V1.5S_VCCD_Q should be short to +V1.5S_VCCDDQ on board

SENSE LINES

VDDQ_SENSE BC43 TP_VDDQ_SENSE
VSS_SENSE_VDDQ BA43 TP_VDDQ_SENSE

TP901 Do Not Stuff
TP902 Do Not Stuff

Pull up page 48 R

VCCSA_SENSE U10 → VCCSA_SENSE 48

VCCSA VID lines

VCCSA_VID0 D48 VCCSA_VID0
VCCSA_VID1 D49 VCCSA_VID1

Here Del Pull up R

VCCSA_VID0 → VCCSA_VID0 48
VCCSA_VID1 → VCCSA_VID1 48

R904 1KR1F-GP
R906 1KR1F-GP

VID0	VID1	VCCSA ULV
L	L	0.9V
L	H	0.85V
H	L	0.775V
H	H	0.75V

IVY-BRIDGE-GP-NF

71.00IVY.A0U

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Title: CPU (VCC_GFXCORE)

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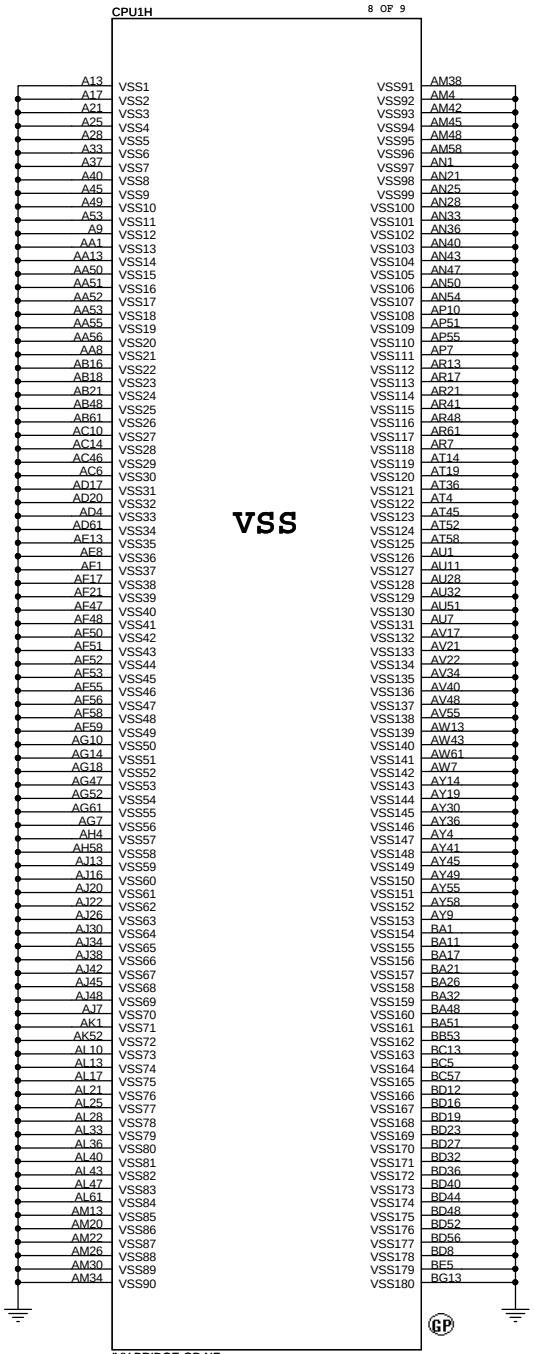
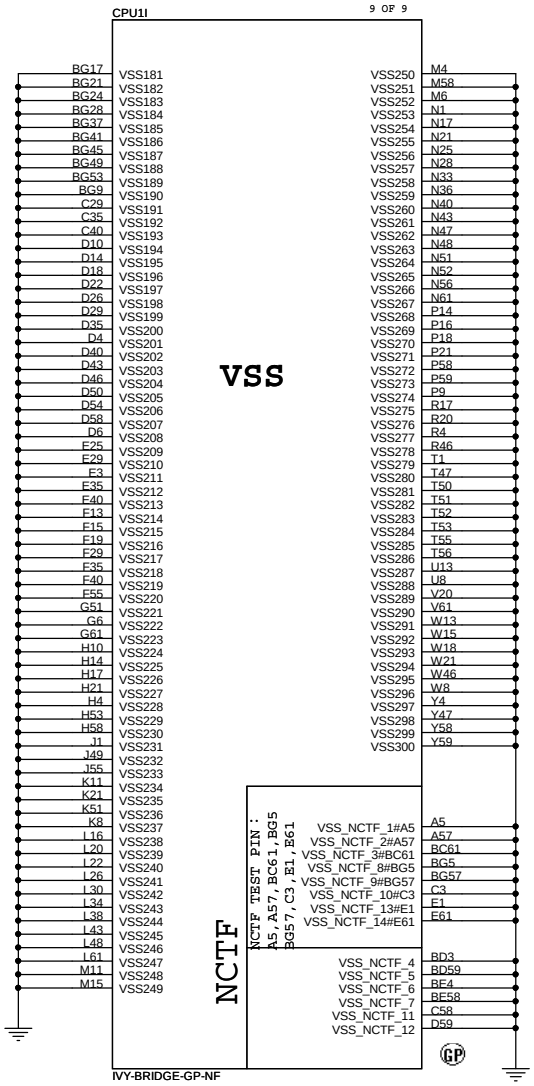
SSID = CPU





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Title: CPU (VSS)

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reserve

JE40 delete XDP function

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Title: ***XDP***

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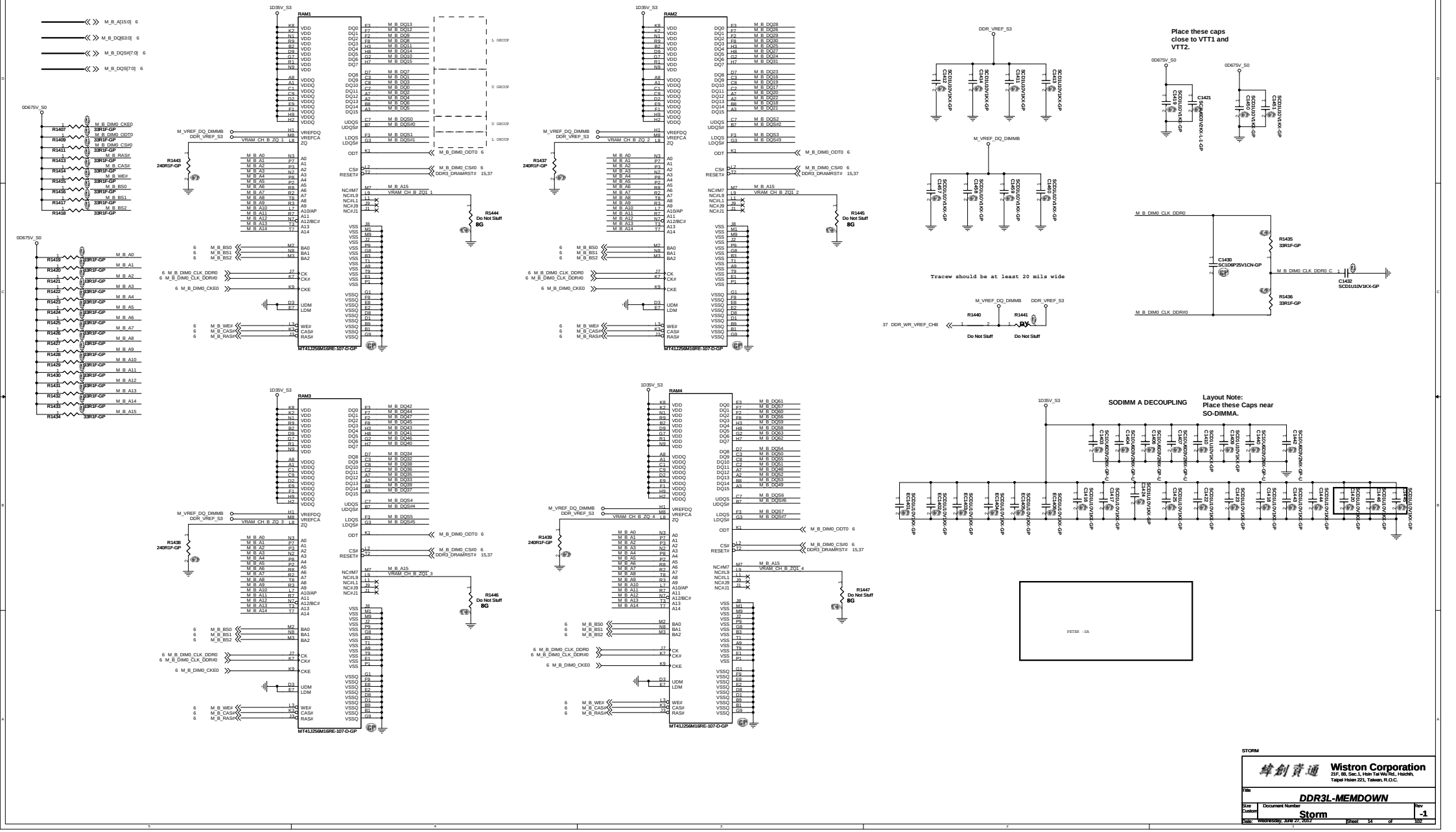
SSID = MEMORY



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Title: DDR3L-MEMDOWN

Size: Custom | Document Number: Storm | Rev: -1

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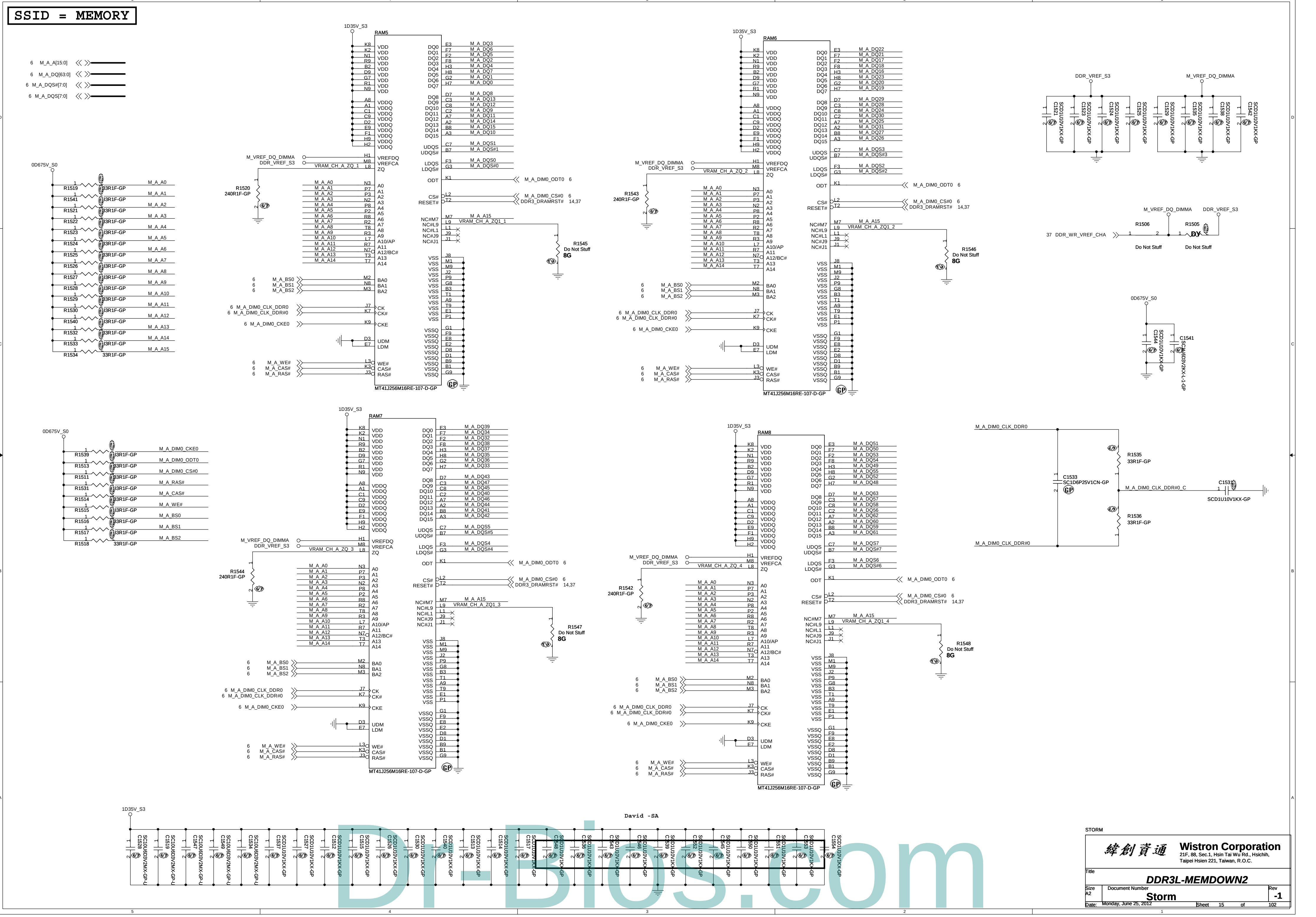
SSID = MEMORY
M_A_A[15:0]
M_A_DQ[63:0]
M_A_DQS#[7:0]
M_A_DQS[7:0]
RAM5
RAM6
RAM7
RAM8
MT41J256M16RE-107-D-GP
1D35V_S3
0D675V_S0
DDR_VREF_S3
M_VREF_DQ_DIMMA
DDR_WR_VREF_CHA
M_A_DIM0_CLK_DDR0
M_A_DIM0_CLK_DDR#0
M_A_DIM0_CLK_DDR#0_C
Do Not Stuff
David -SA
STORM
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDR3L-MEMDOWN2
Size A2
Document Number
Storm
Rev -1
Date: Monday, June 25, 2012
Sheet 15 of 102

(Blanking)

STORM

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Taipei Hsien 221, Taiwan, R.O.C.

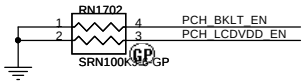
Title: ***DDR3-SODIMM3***

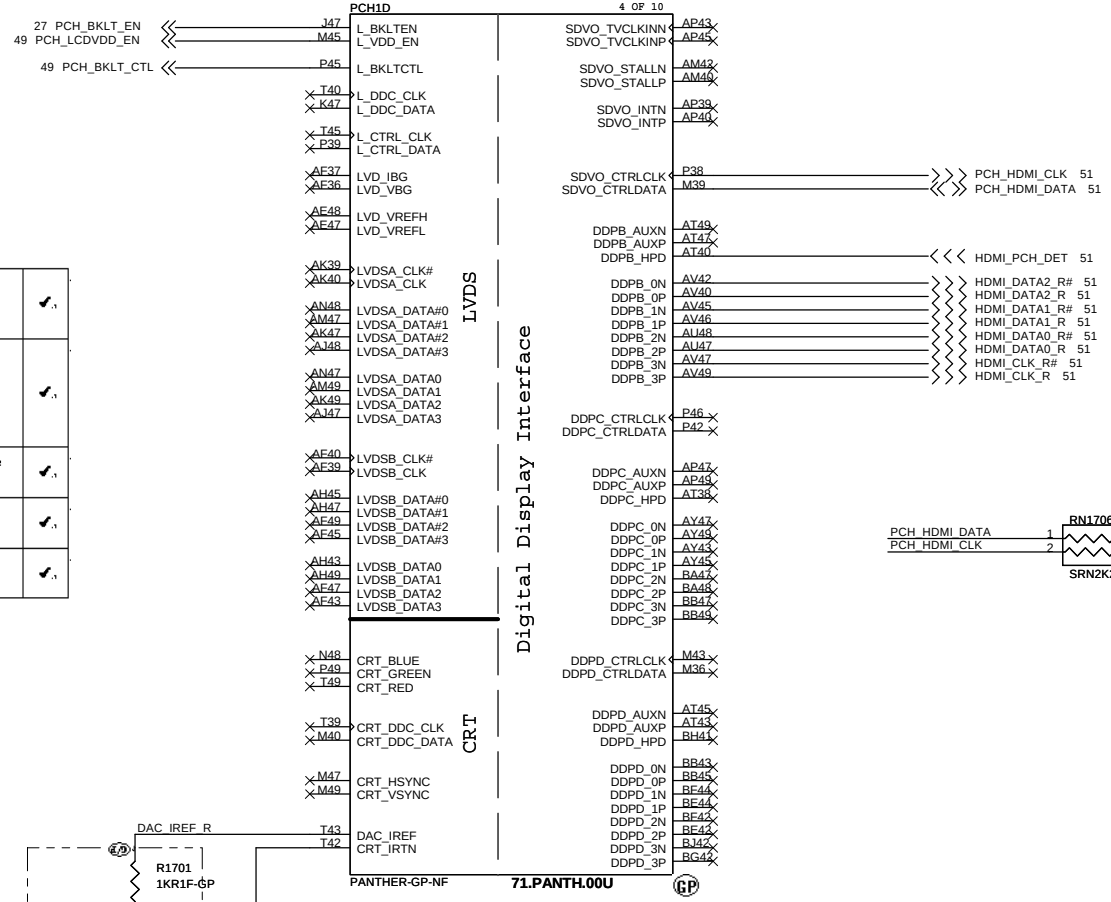
Size	Document Number	Rev
A4	**Storm**	**-1**

Date: Monday, June 25, 2012 Sheet 16 of 102

3.24.2 LVDS Disable Guidelines

Pin Name	System ↓ Pull-up/↓ Pull-down	Schematic Notes	✔
Data/Clock/Control		All signals associated with the interface can be left as No Connect.	✔
Power Supply		The supply pins VCC_TX_LVDS, and VCCA_LVDS can be connected to GND.	✔





if use CRT change 1K to +/- 0.5%
(64.10016.6DL)

3.24.4 CRT Disable

Name	System ↓ Pull-up/↓ Pull-down	Schematics Notes	✔
CRT_RED CRT_GREEN↓ CRT_BLUE↓ CRT_HSYCN↓ CRT_VSYNC		Leave as No Connect	✔
CRT_ITRN		Connect directly to GND plane on the motherboard	✔
DAC_IREF	1-kΩ± 5% pull-down to GND.		✔
VCCADAC	Connect to +V3.3 power-rail		✔

STORM

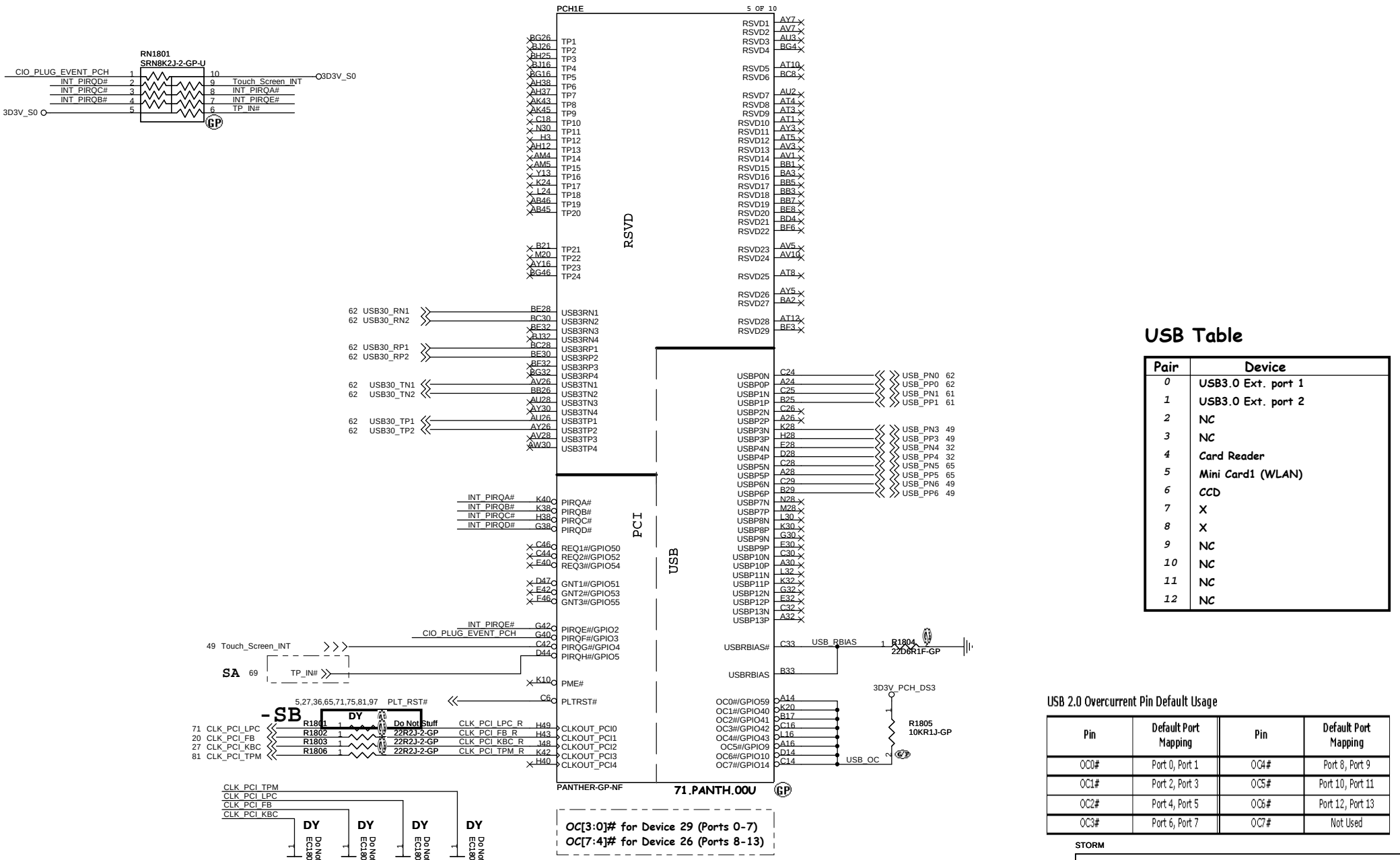
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (LVDS/CRT/DDI)

Size	Document Number	Rev
A3	Storm	-1

Date: Tuesday, June 26, 2012 Sheet 17 of 102

SSID = PCH



USB Table

Pair	Device
0	USB3.0 Ext. port 1
1	USB3.0 Ext. port 2
2	NC
3	NC
4	Card Reader
5	Mini Card1 (WLAN)
6	CCD
7	X
8	X
9	NC
10	NC
11	NC
12	NC

USB 2.0 Overcurrent Pin Default Usage

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

STORM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

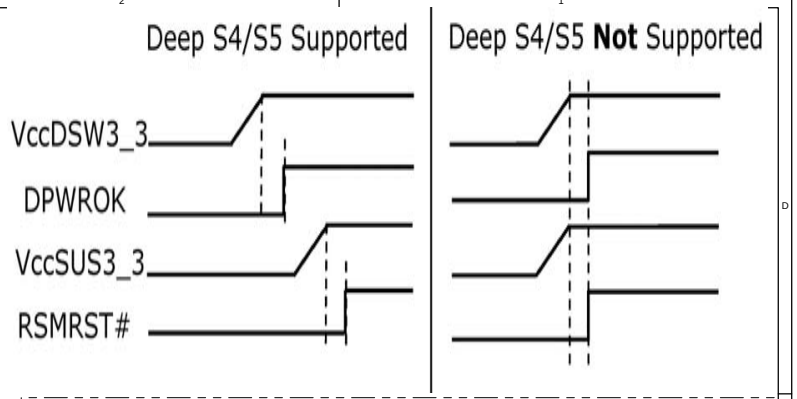
Title: **PCH (PCI/USB/NVRAM)**

Size: A3 | Document Number: Storm | Rev: -1

Date: Monday, June 25, 2012 | Sheet 18 of 102

SSID = PCH

Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.



For platforms not supporting Deep S4/S5
1.VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
2.DPWROK and RSMRST# will rise at the same time (connected on board)
3.SLP_SUS# and SUSACK# are left as 'no connect'
4.SUSWARN# used as SUSPWRDNACK/GPIO30

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

RTC_AUX_S5
DSWODVREN R1915 330KR2J-L1-GP

PCH1C — 3 OF 10 — DMI / FDI / System Power Management — PANTHER-GP-NF

DMI_RXN[3:0] → DMI_RXN0 BC24, DMI_RXN1 BE20, DMI_RXN2 BG18, DMI_RXN3 BG20 → DMI0RXN, DMI1RXN, DMI2RXN, DMI3RXN
DMI_RXP[3:0] → DMI_RXP0 BE24, DMI_RXP1 BC20, DMI_RXP2 BJ18, DMI_RXP3 BJ20 → DMI0RXP, DMI1RXP, DMI2RXP, DMI3RXP
DMI_TXN[3:0] → DMI_TXN0 AW24, DMI_TXN1 AW20, DMI_TXN2 BB18, DMI_TXN3 AV18 → DMI0TXN, DMI1TXN, DMI2TXN, DMI3TXN
DMI_TXP[3:0] → DMI_TXP0 AY24, DMI_TXP1 AY20, DMI_TXP2 AY18, DMI_TXP3 AU18 → DMI0TXP, DMI1TXP, DMI2TXP, DMI3TXP

1D05V_VTT
R1901 1 49D9R1F-GP DMI_COMP_R → BJ24 DMI_ZCOMP
R1902 1 750R2F-GP RBIAS_CPY → BG25 DMI_IRCOMP, BH21 DMI2RBIAS

FDI_RXN0 BJ14 FDI_TXN0 … FDI_RXN7 BG9 FDI_TXN7 → FDI_TXN[7:0] 4
FDI_RXP0 BG14 FDI_TXP0 … FDI_RXP7 BH9 FDI_TXP7 → FDI_TXP[7:0] 4
FDI_INT AW16 → FDI_INT 4
FDI_FSYNC0 AV12 → FDI_FSYNC0 4
FDI_FSYNC1 BC10 → FDI_FSYNC1 4
FDI_LSYNC0 AV14 → FDI_LSYNC0 4
FDI_LSYNC1 BB10 → FDI_LSYNC1 4

DSWVRMEN A18 DSWODVREN
DPWROK E22 PCH_DPWROK_R
WAKE# B9 PCH_PCIE_WAKE#
CLKRUN#/GPIO32 N3 PM_CLKRUN#
SUS_STAT#/GPIO61 G8 → PM_SUS_STAT# 81
SUSCLK/GPIO62 N14
SLP_S5#/GPIO63 D10
SLP_S4# H4 → PM_SLP_S4# 27,46
SLP_S3# F4 → PM_SLP_S3# 27
SLP_A# G10
SLP_SUS# G16 → PM_SLP_SUS# 27,80
PMSYNCH AP14 → H_PM_SYNC 5
SLP_LAN#/GPIO29 K14

27 PM_SUSACK# → C12 SUSACK#
3D3V_S0 R1905 1 10KR1J-GP SYS_RESET# → K3 SYS_RESET#
36 SYS_PWROK → P12 SYS_PWROK
27 S0_PWR_GOOD → R1903 2 1 PWROK (Do Not Stuff) → L22 PWROK
L10 APWROK
37 PM_DRAM_PWRGD → B13 DRAMPWROK
PM_RSMRST# → C21 RSMRST#
27 PM_SUSWARN# → K16 SUSWARN#/SUSPWRDNACK/GPIO30
27,97 PM_PWRBTN# → E20 PWRBTN#
27 AC_PRESENT → H20 ACPRESENT/GPIO31
BATLOW# → E10 BATLOW#/GPIO72
PM_RI# → A10 RI#

DY
R1906 1 Do Not Stuff SYS_PWROK
R1904 1 100KR1J-GP PWROK

DY
R1910 1 Do Not Stuff PM_RSMRST#
R1911 1 2 Do Not Stuff
PCH_DPWROK 27
R1929 100KR1J-GP DS3

-SD
H_PM_SYNC 1 TP1905

3D3V_PCH_DS3
R1925 10KR2J-L-GP BATLOW#
R1926 10KR2J-L-GP PM_RI#
R1907 10KR1J-GP PCH_PCIE_WAKE#
R1928 DY Do Not Stuff PM_SUSACK#
R1923 DY Do Not Stuff PM_SUSWARN#

3D3V_S5
R1932 DY Do Not Stuff AC_PRESENT
R1924 DY Do Not Stuff PM_SUSWARN#
R1927 DY Do Not Stuff BATLOW#

R1908 PM_RSMRST# 100KR1J-GP

3D3V_AUX_S5
R1916 10KR1J-GP
3V_5V_POK_#

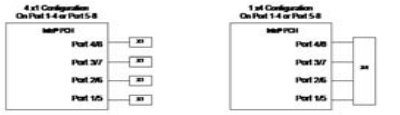
PM_RSMRST# → R1917 1KR2J-L2-GP → RSMRST#_KBC 27
Q1901 FK3303010L-GP 84.33030.031
Q1902 84.33030.031 FK3303010L-GP
3D3V_PCH_DS3
R1909 10KR2J-L-GP
R1912
PM_SLP_SUS#_R
3V_5V_POK 41
Do Not Stuff
R1918 DY Do Not Stuff PM_SLP_SUS#
C1901 SCD1U10V1KX-GP

3D3V_S0
PM_CLKRUN# → R1913 DY Do Not Stuff
R1914 100KR1J-GP

STORM

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: PCH (DM I/FDI/PM)		
Size: A3	Document Number: Storm	Rev: -1
Date: Monday, June 25, 2012	Sheet 19 of 102	

SSID = PCH



FOR SIV,PLS near PCH

Do Not Stuff TP2003 PCIE_RXN4
Do Not Stuff TP2004 PCIE_RXP4

PCH1B

2 OF 10

PCI-E*

NC
NC
WLAN
Thunderbolt

65 PCIE_RXN4
65 PCIE_RXP4
65 PCIE_TXN4
65 PCIE_TXP4
C2001 SCD1U10V1KX-GP PCIE_TXN4_C
C2002 SCD1U10V1KX-GP PCIE_TXP4_C

PERN1 PERP1 PETN1 PETP1
PERN2 PERP2 PETN2 PETP2
PERN3 PERP3 PETN3 PETP3
PERN4 PERP4 PETN4 PETP4
PERN5 PERP5 PETN5 PETP5
PERN6 PERP6 PETN6 PETP6
PERN7 PERP7 PETN7 PETP7
PERN8 PERP8 PETN8 PETP8

SMBUS

SMBALERT#/GPIO11 E12 EC_SW#
SMBCLK H14 SMB_CLK
SMBDATA C9 SMB_DATA
SML0ALERT#/GPIO60 A12 DRAMRST_CNTRL_PCH 37
SML0CLK C8 SML0_CLK
SML0DATA G12 SML0_DATA
SML1ALERT#/PCHHOT#/GPIO74 C13 PCH_GPIO74
SML1CLK/GPIO58 E14 SML1_CLK 27,28
SML1DATA/GPIO75 M16 SML1_DATA 27,28

Controller Link

CL_CLK1 M7
CL_DATA1 T11
CL_RST1# P10

CLOCKS

CLKOUT_PCIE0N Y40
CLKOUT_PCIE0P Y39
PCIE_CLK_REQ0# PCIECLKRQ0#/GPIO73 J2
CLKOUT_PCIE1N AB49
CLKOUT_PCIE1P AB47
PCIE_CLK_REQ1# PCIECLKRQ1#/GPIO18 M1
CLKOUT_PCIE2N AA48
CLKOUT_PCIE2P AA47
PCIE_CLK_REQ2# PCIECLKRQ2#/GPIO20 V10
CLKOUT_PCIE3N Y37
CLKOUT_PCIE3P Y36
65 PCIE_CLK_WLAN#
65 PCIE_CLK_WLAN
65 PCIE_WLAN_CLKREQ# PCIECLKRQ3#/GPIO25 AB
CLKOUT_PCIE4N Y43
CLKOUT_PCIE4P Y45
PCIE_CLK_REQ4# PCIECLKRQ4#/GPIO26 L12
CLKOUT_PCIE5N V45
CLKOUT_PCIE5P V46
PCIE_LAN_CLKREQ# PCIECLKRQ5#/GPIO44 L14
CLKOUT_PEG_B_N AB42
CLKOUT_PEG_B_P AB40
PEG_B_CLKRQ# PEG_B_CLKRQ#/GPIO56 E6
CLKOUT_PCIE6N V40
CLKOUT_PCIE6P V42
PCIE_CLK_REQ6# PCIECLKRQ6#/GPIO45 T13
CLKOUT_PCIE7N V38
CLKOUT_PCIE7P V37
PCIE_CLK_REQ7# PCIECLKRQ7#/GPIO46 K12
CLKOUT_ITPXDP_N AK14
CLKOUT_ITPXDP_P AK13

PEG_A_CLKRQ#/GPIO47 M10 PEG_CLKREQ#_R
CLKOUT_PEG_A_N AB37
CLKOUT_PEG_A_P AB36
CLKOUT_DMI_N AV22 CLK_EXP_N 5
CLKOUT_DMI_P AU22 CLK_EXP_P 5
CLKOUT_DP_N AM12 CLK_DP_N 5
CLKOUT_DP_P AM13 CLK_DP_P 5
CLKIN_DMI_N BF18 CLK_BUF_EXP_N
CLKIN_DMI_P BE18 CLK_BUF_EXP_P
CLKIN_GND1_N BJ30 CLK_BUF_CPYCLK_N
CLKIN_GND1_P BG30 CLK_BUF_CPYCLK_P
CLKIN_DOT_96N G24 CLK_BUF_DOT96_N
CLKIN_DOT_96P E24 CLK_BUF_DOT96_P
CLKIN_SATA_N AK7 CLK_BUF_CKSSCD_N
CLKIN_SATA_P AK5 CLK_BUF_CKSSCD_P
REFCLK14IN K45 CLK_BUF_REF14
CLKIN_PCILOOPBACK H45 CLK_PCI_FB 18
XTAL25_IN V47 XTAL25_IN
XTAL25_OUT V49 XTAL25_OUT
XCLK_RCOMP Y47 XCLK_RCOMP 1 R2007 90D9K2F-1-GP 2 VDD33_VTT

FLEX CLOCKS

CLKOUTFLEX0/GPIO64 K43 CLK48
CLKOUTFLEX1/GPIO65 F47 DRAM_TYPE2
CLKOUTFLEX2/GPIO66 H47 DRAM_TYPE3
CLKOUTFLEX3/GPIO67 K49 DGPU_PRSNT#

PANTHER-GP-NF

71.PANTH.00U

As Flex clocks, can be configured as 48 MHz/ 24 MHz, 33 MHz, 27 MHz (Spread or Nonspread), 14.318 MHz. Refer to the PCH External Design Specification (EDS) for configuration options of Flex Clocks.

3D3V_PCH_DS3

RN3008 SRN2K2J-1-GP
SMB_DATA
SMB_CLK
RN2004 SRN2K2J-1-GP
SML0_DATA
SML0_CLK
RN2005 SRN2K2J-1-GP
SML1_CLK
SML1_DATA
PCH_GPIO74
EC_SW#
R2010 10KR2J-L-GP
R2015 10KR2J-L-GP
DRAMRST_CNTRL_PCH
R2009 1KR1J-GP

3D3V_S0

RN2007 SRN2K2J-1-GP
Q2001 DTN702KDW-GP
84.2N702.A3F
2nd = 84.DM601.03F
SMB_DATA
SMB_CLK
PCH_SMBDATA 69
PCH_SMBCLK 69

3D3V_S0

R2004 10KR1J-GP
PEG_CLKREQ#_R

3D3V_S0

R2011 10KR1J-GP
R2012 10KR1J-GP
DGPU_PRSNT#
UMA_DISCRETE#
UMA: 1 1
DIS :0 1
SG(PX) : 0 0
Optimus(Muxless) : 1 0
UMA_DIS# 22

3D3V_PCH_DS3

RN2001 SRN10KJ-10-GP-U
PCIE_CLK_REQ4#
PCIE_LAN_CLKREQ#
PCIE_CLK_REQ6#
RN2002 SRN10KJ-10-GP-U
PCIE_CLK_REQ0#
PCIE_CLK_REQ7#
PEG_B_CLKRQ#
PCIE_WLAN_CLKREQ#

3D3V_S0

RN2011
PCIE_CLK_REQ1#
PCIE_CLK_REQ2#
SRN10KJ-11-GP-U

PCIECLKRQ1# and PCIECLKRQ2#
Support S0 power only

WLAN

Check 48Mhz

Y2014 32.002J-L1-GP
48MHZ
CLK48_Cardreader 32
EC2001 DY
DO NOT INSTALL

CLK_BUF_CKSSCD_P
CLK_BUF_CKSSCD_N
RN2009 SRN10KJ-11-GP-U
CLK_BUF_CPYCLK_P
CLK_BUF_CPYCLK_N
RN2012 SRN10KJ-11-GP-U
CLK_BUF_EXP_P
CLK_BUF_EXP_N
RN2013 SRN10KJ-11-GP-U
CLK_BUF_DOT96_N
CLK_BUF_DOT96_P
RN2014 SRN10KJ-11-GP-U

2012/01/05 For DRAM

3D3V_S0

ELPIDA_8G R2018 Do Not Stuff
Hynix_4G R2016 10KR1J-GP
DY R2017 Do Not Stuff
22 DRAM_TYPE1
DRAM_TYPE2
DRAM_TYPE3
R2020 10KR1J-GP
Hynix_ELPIDA_4G_4G
R2019 Do Not Stuff
ELPIDA_4G_8G
R2022 10KR1J-GP
Hynix_ELPIDA_4G_8G

0	0	0	ELPIDA 2GB PER Channel(chip is 4Gbit RAM)
0	0	1	Hynix A 2GB PER Channel(chip is 4Gbit RAM)
0	1	0	
0	1	1	
1	0	0	ELPIDA 4GB PER Channel(chip is 8Gbit RAM)
1	0	1	
1	1	0	
1	1	1	

XTAL25_IN
C2006 SC15P50V2JN-2-GP
X2001 XTAL-25MHZ-202-GP
82.30020.I61
R2006 1MR1J-GP
XTAL25_OUT
C2005 SC15P50V2JN-2-GP

STORM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI-E/SMBUS/CLOCK/CL)
Size: A2 Document Number: Storm Rev: -1
Date: Monday, June 25, 2012 Sheet 20 of 102

SSID = PCH

INTVRMEN- Integrated SUS
1.05V VRM Enable
High - Enable internal VRs
Low - Enable external VRs

-SB
height concern,do not change to 0603,
so change C from 1uF to 0.1uF
change R from 20K to 200K for AFR

Layout Note:
Place close together.

RTC Reset

Layout Note:
HDA_SDO and HDA_BCLK must be
length matched to within 500 mils

Flash Descriptor Security Overide	
HDA_SDOUT	Low = Default High = Enable

No Reboot Strap	
HDA_SPKR	Low = Default High = No Reboot

PLL ODVR VOLTAGE	
HDA_SYNC	Low = 1.8V (Default) High = 1.5V

HDA_SYNC:
This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode.
1K external pull-up resistor is required on this signal on the board.
Signal may have leakage paths via powered off devices(Audio Codec)
and hence contend with the external pull-up.
A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.

PCH1A — 1 OF 10 — PANTHER-GP-NF — 71.PANTH.00U

Strap pin ,Internal PU

mSATA

mSATA

STORM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (SPI/RTC/LPC/SATA/IHDA)

Size: A3 | Document Number: Storm | Rev: -1

Date: Tuesday, June 26, 2012 | Sheet 21 of 102

SSID = PCH

3D3V_S0 — RN2203 (SRN10KJ-11-GP-U): 1 — 4 H_RCIN#; 2 — 3 H_A20GATE

PCH1F — 6 OF 10 — PANTHER-GP-NF — 71.PANTH.00U

S_GPIO	T7	BMBUSY#/GPIO0		C40	TACH4/GPIO68
EC_SMI#	A42	TACH1/GPIO1		B41	TACH5/GPIO69 → UMA_DIS# 20
DGPU_HPD_INTR#	H36	TACH2/GPIO6		C41	TACH6/GPIO70
27 EC_SCI#	E38	TACH3/GPIO7		A40	TACH7/GPIO71
ICC_EN#	C10	GPIO8			
PCH_GPIO12	C4	LAN_PHY_PWR_CTRL/GPIO12			
PCH_GPIO15	G2	GPIO15		P4	A20GATE — H_A20GATE# 27
3D3V_S0 — R2202 10KR1J-GP	U2	SATA4GP/GPIO16		AU16	PECI — H_PECI R — R2203 DX Do Not Stuff — H_PECI 5,27
	D40	TACH0/GPIO17		P5	RCIN# — H_RCIN# — H_RCIN# 27
56 SATA_RAID0	T5	SCLOCK/GPIO22		AY11	PROCPWRGD — H_CPUPWRGD 5,97
27 PCH_GPIO27# — R2223 DX Do Not Stuff	E8 / E16	GPIO24 / GPIO27		AY10	THRMTRIP# — PCH_THERMTRIP_R — R2204 390R2F-2GP — H_THERMTRIP# 5,36
PLL_ODVR_EN	P8	GPIO28		AY1	INIT3_3V#
PSW_CLR#	K1	STP_PCI#/GPIO34		T14	DF_TVS — NV_CLE
FP_DET#	K4	GPIO35		AH8 / AK11 / AH10 / AK10	TS_VSS1 / TS_VSS2 / TS_VSS3 / TS_VSS4
DMI_OVRVLTG	V8	SATA2GP/GPIO36		P37	NC_1
FDI_OVRVLTG	M5	SATA3GP/GPIO37			
MFG_MODE	N2	SLOAD/GPIO38			
EDP# LVDS	M3	SDATAOUT0/GPIO39			
20 DRAM_TYPE1	V13	SDATAOUT1/GPIO48		BG2	VSS_NCTF_15#BG2
PCH_TEMP_ALERT#	V3	SATA5GP/GPIO49/TEMP_ALERT#		BG48	VSS_NCTF_16#BG48
USB3_PWR_ON	D6	GPIO57		BH3	VSS_NCTF_17#BH3
				BH47	VSS_NCTF_18#BH47
A4		VSS_NCTF_1#A4		BJ4	VSS_NCTF_19#BJ4
A44		VSS_NCTF_2#A44		BJ44	VSS_NCTF_20#BJ44
A45		VSS_NCTF_3#A45		BJ45	VSS_NCTF_21#BJ45
A46		VSS_NCTF_4#A46		BJ46	VSS_NCTF_22#BJ46
A5		VSS_NCTF_5#A5		BJ5	VSS_NCTF_23#BJ5
A6		VSS_NCTF_6#A6		BJ6	VSS_NCTF_24#BJ6
B3		VSS_NCTF_7#B3		C2	VSS_NCTF_25#C2
B47		VSS_NCTF_8#B47		C48	VSS_NCTF_26#C48
BD1		VSS_NCTF_9#BD1		D1	VSS_NCTF_27#D1
BD49		VSS_NCTF_10#BD49		D49	VSS_NCTF_28#D49
BE1		VSS_NCTF_11#BE1		E1	VSS_NCTF_29#E1
BE49		VSS_NCTF_12#BE49		E49	VSS_NCTF_30#E49
BF1		VSS_NCTF_13#BF1		F1	VSS_NCTF_31#F1
BF49		VSS_NCTF_14#BF49		F49	VSS_NCTF_32#F49

NCTF TEST PIN: A4,A44,A45,A46,A5,A6,B3,B47, BD1,BD49,BE1,BE49,BF1,BF49, BG2,BG48,BH3,BH47,BJ4,BJ44, BJ45,BJ46,BJ5,BJ6,C2,C48,D1, D49,E1,E49,F1,F49

PCH:no Turbo control via PECI

KBC(Recommended):EC collect all thermal data and Performs Turbo power control

Pass Word Clear: G2201 Do Not Stuff

Layout Note: Trace length 500 mil

3D3V_S0 — RN2201 SRN10KJ-10-GP-U: EC_SMI#, EC_SCI#, DGPU_HPD_INTR#, PCH_TEMP_ALERT#

RN2202 SRN10KJ-10-GP-U: PSW_CLR#, FP_DET#, MFG_MODE, S_GPIO

EDP# LVDS — R2214 10KR1J-GP

3D3V_PCH_DS3 — RN2206 SRN10KJ-11-GP-U: USB3_PWR_ON, PCH_GPIO12 — R2201 1KR1J-GP — PCH_GPIO15

3D3V_S5 — R2213 10KR1J-GP — PCH_GPIO27

1D8V_S0 — R2207 2K2R1J-GP — NV_CLE — R2229 1KR1J-GP — H_SNB_IVB# 5

FDI_OVRVLTG — R2208 10KR1J-GP

DMI_OVRVLTG — R2209 10KR1J-GP

Internal Pull Down

FDI TERMINATION VOLTAGE OVERRIDE(Reserved)	
FDI_OVRVLTG (GPIO37)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE(Reserved)	
DMI_OVRVLTG (GPIO36)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

ICC_EN# — R2211 1KR1J-GP

Integrated Clock Chip Enable(Reserved)	
ICC_EN# (GPIO8)	HIGH- DISABLED [DEFAULT]
	LOW - ENABLED

Internal PU

PLL_ODVR_EN — R2212 Do Not Stuff DY

PLL ON DIE VR ENABLE	
PLL_ODVR_EN (GPIO28)	HIGH- DISABLED [DEFAULT]
	LOW - ENABLED

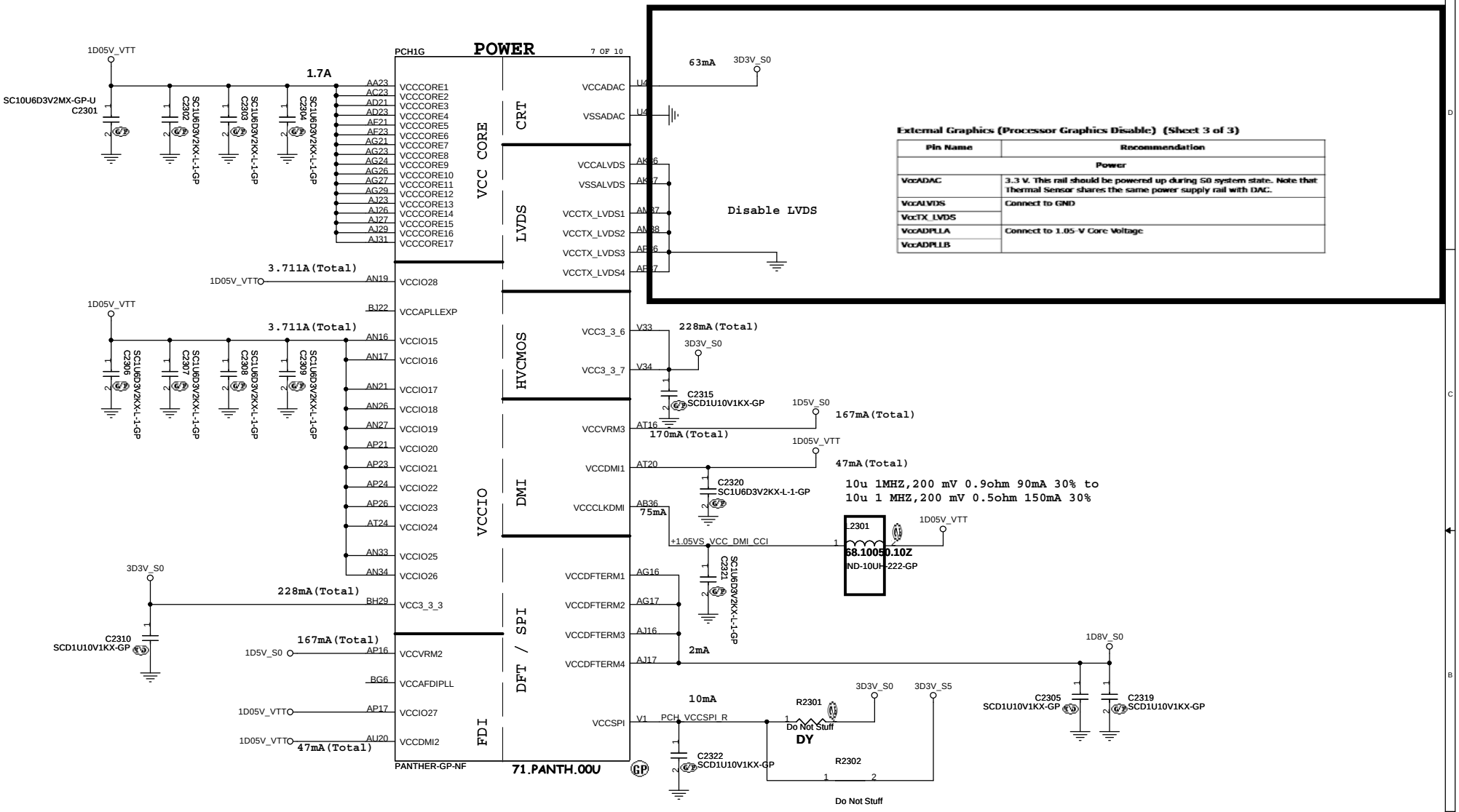
STORM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (GPIO/CPU)**

Size: A3 | Document Number: Storm | Rev: -1

Date: Monday, June 25, 2012 | Sheet 22 of 102



External Graphics (Processor Graphics Disable) (Sheet 3 of 3)

Pin Name	Recommendation
	Power
VccADAC	3.3 V. This rail should be powered up during S0 system state. Note that Thermal Sensor shares the same power supply rail with DAC.
VccALVDS	Connect to GND
VccTX_LVDS	
VccADPLLA	Connect to 1.05 V Core Voltage
VccADPLLB	

STORM

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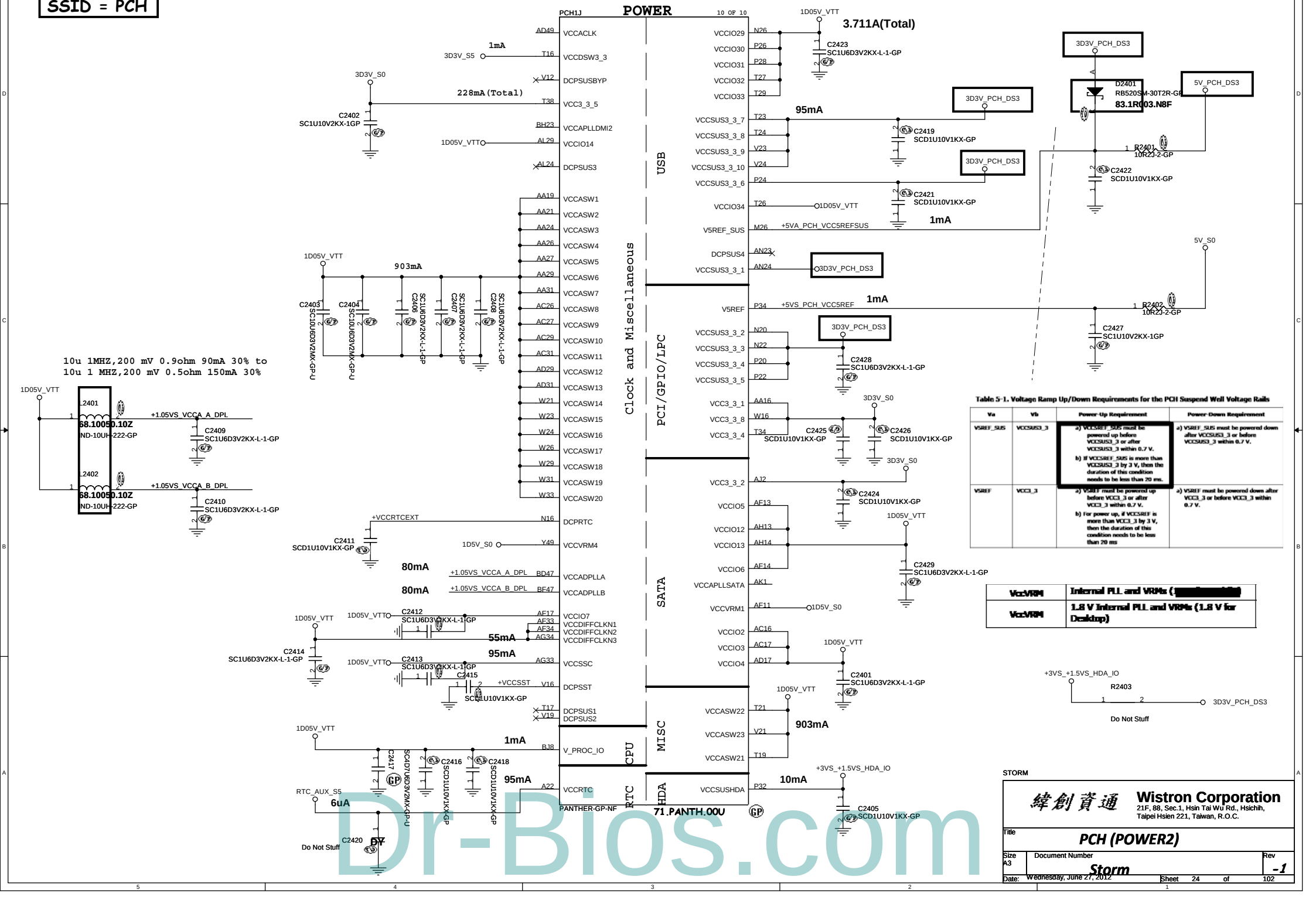
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (POWER1)

Size: A3 | Document Number: Storm | Rev: -1

Date: Wednesday, June 27, 2012 | Sheet 23 of 102

SSID = PCH



STORM

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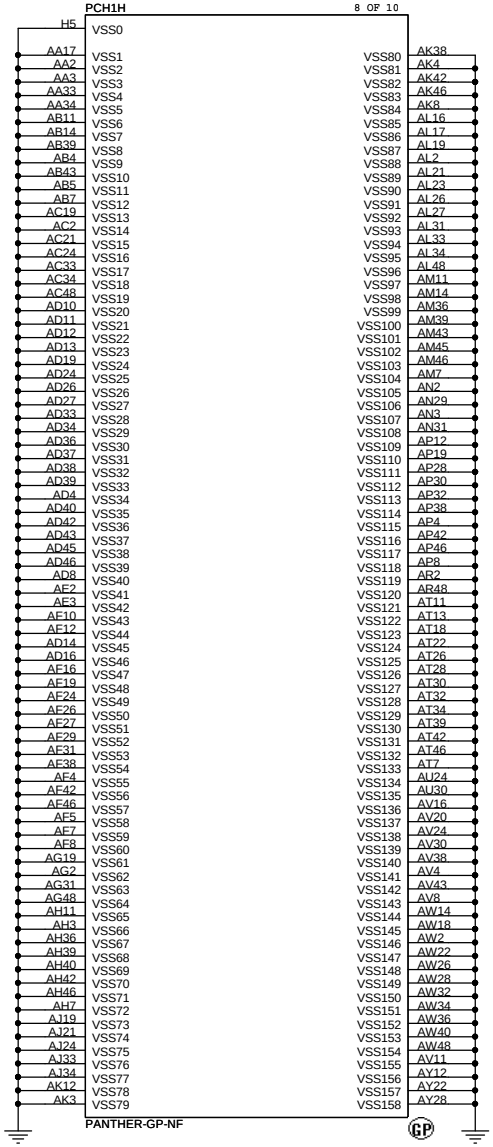
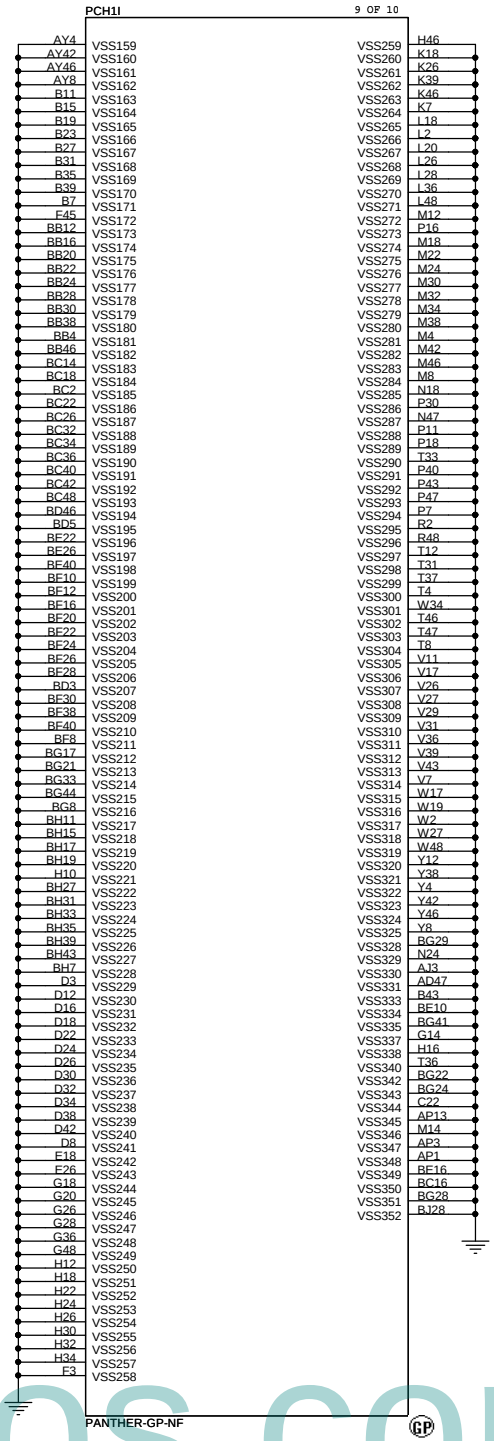
Title: PCH (POWER2)

Size: A3 | Document Number: Storm | Rev: -1

Date: Wednesday, June 27, 2012 | Sheet 24 of 102

SSID = PCH





STORM

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (VSS)**

Size	Document Number	Rev
A3	Storm	-1

Date: Monday, June 25, 2012 Sheet 25 of 102

STORM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Clock(colay)***

Size	Document Number	Rev
A3	**Storm**	**-1**

Date: Monday, June 25, 2012 Sheet 26 of 102

SSID = KBC

SB_20120129_IOAC

-SC

layout concern

WLAN_VDD

R2781 100KR1J-GP

AP_DET# 65

R2782 Do Not Stuff

C2724 C2725 C2726 C2727 C2728 C2729 SCD1U16V1KX-GP

C2722 SCD1U16V1KX-GP

R2736 Do Not Stuff

AVCC

C2723 SCD1U10V2KX-GP

C2703 SCD1U10V2KX-GP

3DV_S0

3DV_AUX_S5

R2701 Do Not Stuff

KBC_VSTBY_127

C2719 SCD1U16V1KX-GP

BAT_SCL

BAT_SDA

BAT_IN#

ECRST#

EC_DRAMRST_GATE

LID_CLOSE#

R2708 49.9KR1J-GP

R2709 49.9KR1J-GP

R2711 100KR1J-GP

R2712 100KR1J-GP

R2713 100KR1J-GP

DY Do Not Stuff

SB_20120129_IOAC

R2729 100KR1J-GP

3DV_SRC_EN

Do Not Stuff TP2702

CLK_PCI_KBC

3DV_S0

RN2723 SRN10KJ-11-GP-U

3FAN_TACH2

3FAN_TACH3

R2722 100KR1J-GP

S5_ENABLE

KBC1 ITE IT8518VG-HX-GP

LPC_AD0 LPC_AD1 LPC_AD2 LPC_AD3

LAD0/GPM0 LAD1/GPM1 LAD2/GPM2 LAD3/GPM3

LPCRST#/WUI4/GPD2

CLKRUN#/WUI16/GPH0/ID0

LPCCLK/GPM4

LFRAME#/GPM5

GA20/GPB5

SERIRQ/GPM6

ECSCI#/GPD3

ECSMI#/GPD4

WRST#

KBRST#/GPB6

PWUREQ#/BBO/SMCLK2/ALT/GPC7

PLT_RST# KBC_R

LID_CLOSE#

CLK_PCI_KBC

CLK_PWM/ID2

H_A20GATE

H_RCIN#

ECSCI# KBC

ECRST#

PM_SUSACK# R_EC

PCH_GPIO27#

STOP_CHG#

CHG_DN#

ESI_TxD

ESI_RXD_KBC

KBC_SPI_CLK_R

KBC_SPI_CS#_R

KBC_SPI_SI_R

KBC_SPI_SO

PCH_DPWROK

3DV_SRC_EN

PROCHOT_EC

KSO0/PD0 KSO1/PD1 KSO2/PD2 KSO3/PD3 KSO4/PD4 KSO5/PD5 KSO6/PD6 KSO7/PD7 KSO8/BACK# KSO9/BUSY KSO10/PE KSO11/ERR# KSO12/SLCT KSO13 KSO14 KSO15

KCOL0 KCOL1 KCOL2 KCOL3 KCOL4 KCOL5 KCOL6 KCOL7 KCOL8 KCOL9 KCOL10 KCOL11 KCOL12 KCOL13 KCOL14 KCOL15

KROW0 KROW1 KROW2 KROW3 KROW4 KROW5 KROW6 KROW7

KSI0 KSI1 KSI2 KSI3 KSI4 KSI5 KSI6 KSI7

KCOL[0..15]

KROW[0..7]

EC_SLP_S3# EC_SLP_S4# EC_DRAMRST_GATE SS_ENABLE PCH_SPI_MOSI_KBC PCH_SPI_MISO_KBC PCH_SPI_CLK_KBC PCH_SPI_CS#_SW S0_PWR_GOOD_KBC_R S0_PWR_GOOD PM_PWRBTN#_R_EC PM_PWRBTN#

SMCLK0/GPB1 SMDAT0/GPB2 SMCLK1/GPC1 SMDAT1/GPC2 SMCLK2/PECI/WUI22/GPF6 SMDAT2/PECIRQ/T4/WUI23/GPF7

PS2CLK0/TMB0/GPF0 PS2DAT0/TMB1/GPF1 PS2CLK1/DTR0#/GPF2 PS2DAT1/RTS0#/GPF3 PS2CLK2/WUI20/GPF4 PS2DAT2/WUI21/GPF5

BAT_SCL BAT_SDA SML1_CLK SML1_DATA H_PECI BLON_OUT

H_PECI_KBC

20111208-SA

BATTERY / CHARGER

AD_OFF USB_PWR_EN ECH_BKLT_EN WIFI_RF_EN TPCLK TPDATA

WIFI_RF_EN_KBC_R R2732 2 Do Not Stuff

PWM0/GPA0 PWM1/GPA1 PWM2/GPA2 PWM3/GPA3 PWM4/GPA4 PWM5/GPA5 PWM6/SSCK/GPA6 PWM7/RIG1#/GPA7

PWRLED CHARGE_LED STORY_LED TPDATA FAN1_PWM FAN2_PWM KBC_UNLOCK KBC_BEEP#

TACH0A/GPD6 TACH1A/TMA1/GPD7

FAN_TACH1

TMR0/WUI3/GPC4 TMR1/WUI3/GPC5

AC_INT BAT_IN#

PWRSW/GPE4 RI1#/WUI0/GPD0 RI2#/WUI1/GPD1

KBC_PWRBTN#_R PM_SLP_S3# KBC_R PM_SLP_S4# KBC_R

PM_SLP_S3# PM_SLP_S4#

RING#/PWRFAIL#/CK32KOUT/LPCRST#/GPB7

RSMRST#_KBC

ADC0/GPI0 ADC1/GPI1 ADC2/GPI2 ADC3/GPI3 ADC4/WUI28/GPI4 ADC5/DCD1#/WUI29/GPI5 ADC6/DSR1#/WUI30/GPI6 ADC7/CTS1#/WUI31/GPI7

PCB_VER_AD ADP_TYPE ALL_POWER_OK_KBC

R2743 1 Do Not Stuff

ALL_POWER_OK ADP_TYPE

TACH2/GPJ0 GPJ1 DAC2/TACH6/GPJ2 DAC3/TACH5/GPJ3 DAC4/DCD0#/GPJ4 DAC5/RIG0#/GPJ5

AC_PRESENT_R_EC R2723 1 Do Not Stuff

AC_PRESENT BLUETOOTH_EN PITCRST_ON FAN_TACH2 WLAN_PWR_EN# USB_CHG_EN

CK32K/GPJ6 CK32K/GPJ7

KBC_CK32K

R2758 1 Do Not Stuff

PLT_RST#_RST

SC

R2768 100KR1J-GP

SB_20120129_IOAC

WLAN_VDD

R2716 1 WLAN_PCIE_WAKE#

10KR1F-GP

-SC

3DV_S0

R2717 100KR1J-GP

R2757 33R2J-1-GP

SENSOR_INT

ESI_RXD_KBC

20111208-SA

D2701 83.1R003.N8F

RB520SM-30T26-GP

EC_SCI#

3DV_AUX_S5

RN2703

STOP_CHG#

CHG_DN#

Do Not Stuff

-SC

U2702 DY

GND VCC RESET#/RESET MR#

R2745 Do Not Stuff

PURE_HW_SHUTDOWN#

PURE_HW_SHUTDOWN#_R

3DV_AUX_S5

20111208_SA

RN2709 SRN10KJ-11-GP-U

PURE_HW_SHUTDOWN#_R

ECRST#

C2715 SC1U10V2KX-1GP

Q2705 MMBT3906-1-GP

84.T3906.A11

2nd = 84.03906.F11

-SC

R2715 1KR1J-GP

AD_OFF

SB_20120129_IOAC

WLAN_VDD

R2716 1 WLAN_PCIE_WAKE#

10KR1F-GP

PCB VER AD(GPIO91)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
Reserved	100.0K	10.0K	3.0V
Reserved	100.0K	20.0K	2.75V
Reserved	100.0K	33.0K	2.48V
Strom MP	100.0K	47.0K	2.24V
Strom PD	100.0K	64.9K	2.0V
Strom ENG	100.0K	82K	2.07V
Helium MP	100.0K	100.0K	1.65V
Helium PD	100.0K	143.0K	1.358V
Helium ENG	100.0K	174.0K	1.204V
Helium LAB	100.0K	215.0K	1.048V

R2735 82KR1F-GP

PCB_VER_AD

DY C2717 SCD1U16V1KX-GP

R2758 100KR1F-GP

EC_AGND

GPIO0 High Active

20111208-SA

H_PROCHOT# 5

PROCHOT_EC

Q2702 PK3000016-GP 84.S3030.031

R2748 100KR1J-GP

3DV_S0

R2772 Do Not Stuff

R2773 Do Not Stuff 1ROM

0R2J-1-GP 2ROM

PCH_SPI_CS#_SW

21,60 PCH_SPI_CS0#_R

21 PCH_SPI_CS1#_R

DS3 R2747

EC_SLP_S3#

PM_SLP_S3#

Do Not Stuff

Non-DS3

R2706

EC_PM_SLP_S3#

For crystal circuit design, please refer to below block diagram

External Crystal

Internal Crystal

-SD

AD_3K

R2753 100KR2F-GP

<--Check ADT_TYPE V

19Vx100K/(590+100)K=2.75V

ADT_TYPE

C2720 SCD1U16V1KX-GP

R2751 100KR1F-GP

Vz=2.85-3.15V

D2702 MMBZ5229BPT-GP 83.3R003.B3F

EC_AGND

SB_20120129_IOAC

3DV_AUX_S5

DY R2777 Do Not Stuff

WLAN_PWR_EN#

STORM

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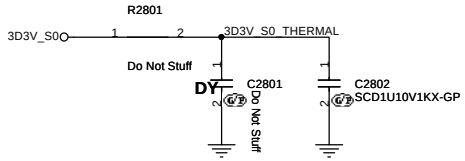
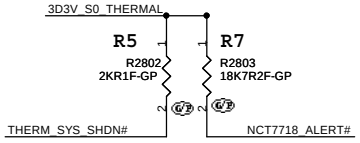
Title: KBC ITE IT8518VG

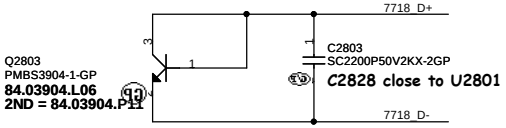
Size: Custom | Document Number: Storm | Rev: -1

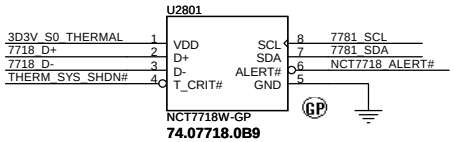
Date: Monday, June 25, 2012 | Sheet 27 of 102

SSID = Thermal

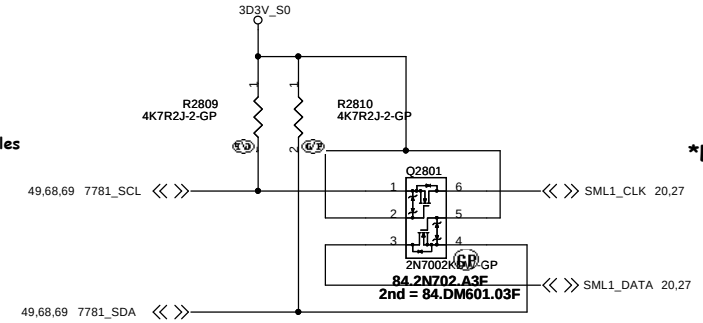




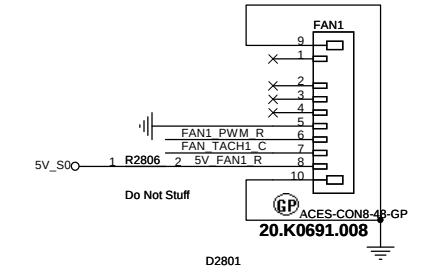


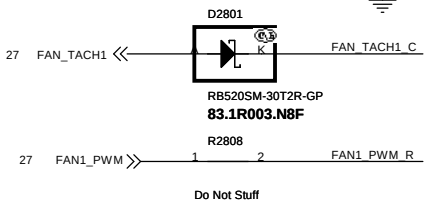


Layout notice :
* Put the C1 2200pF to close the nct7718W
* Add ground shielding for D+ and D- traces
* D+/D- route has to be away from the high noise area
* The recommended traces width and ground shielding spacing are 10miles

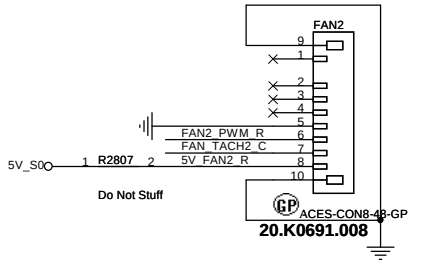


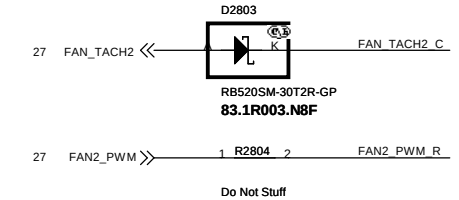
Layout 15 mil

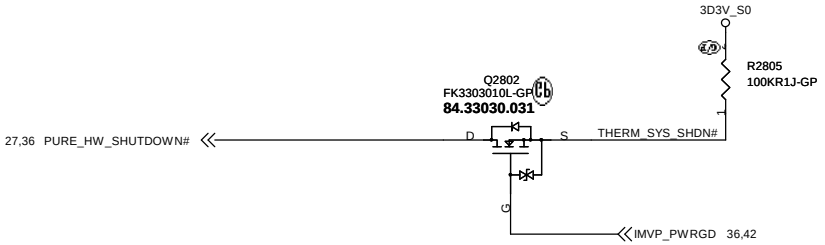




Layout 15 mil







Setting 85℃

ALERT# /T_CRIT#
Pull-up Resistor

R5 \ R7	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
2Kohm	77℃	87℃	97℃	107℃	117℃
7.5Kohm	79℃	89℃	99℃	109℃	119℃
10.5Kohm	81℃	91℃	101℃	111℃	121℃
14Kohm	83℃	93℃	103℃	113℃	123℃
18.7Kohm	85℃	95℃	105℃	115℃	125℃

T_CRIT temperature strapping point

The default value is trapping after power up 100ms by different pull-up resistors of T_CRIT# and ALERT# pin:

TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

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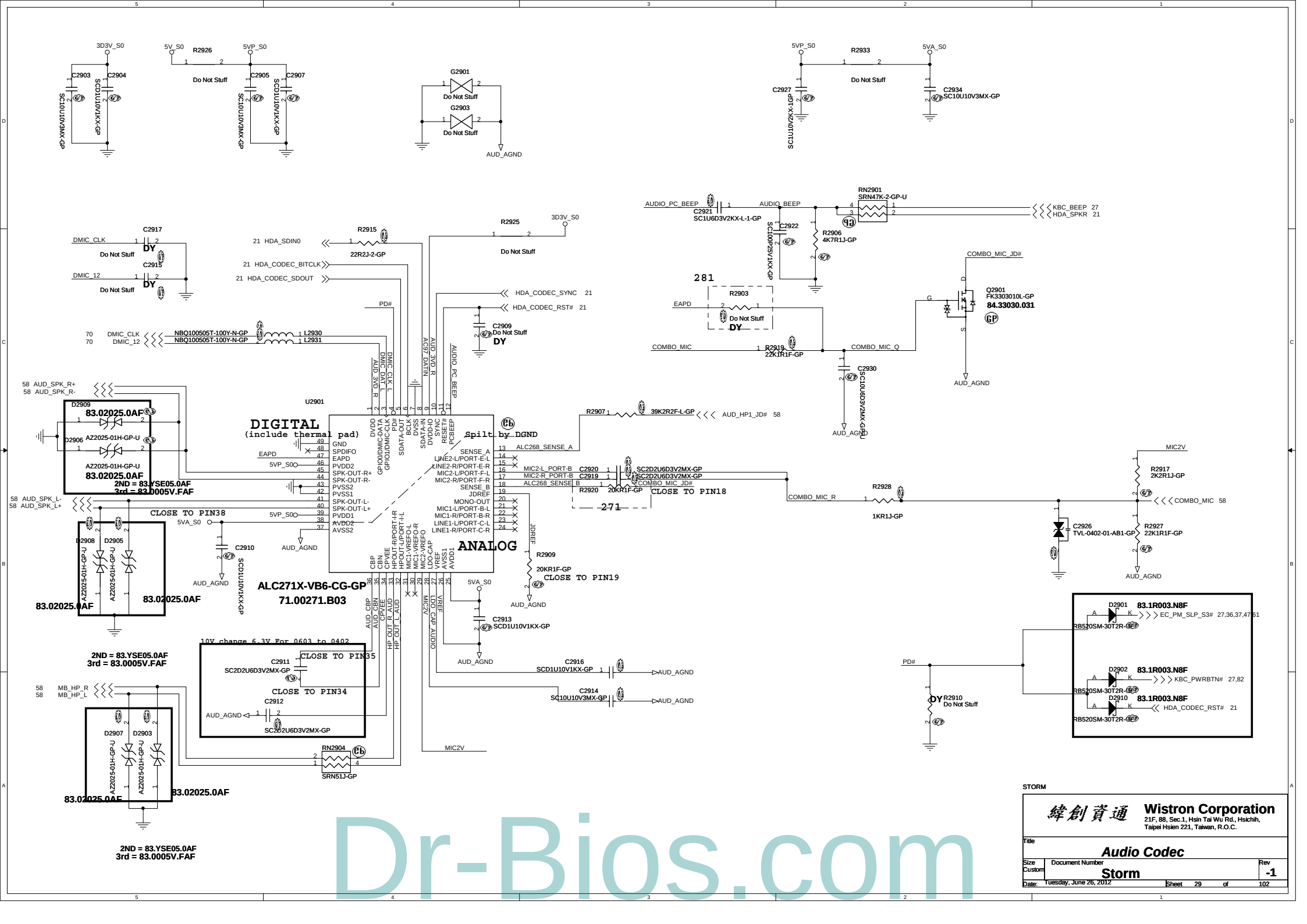
Taipei Hsien 221, Taiwan, R.O.C.

Title: NUVOTON_NCT7718W

Size: A3 | Document Number: Storm | Rev: -1

Date: Wednesday, June 27, 2012 | Sheet 28 of 102



STORM

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Audio Codec**

Size	Document Number	Rev
Custom	Storm	-1

Date: Tuesday, June 26, 2012 Sheet 29 of 102

AUDIO OP AMPLIFIER

JE40 delete AMP function

STORM

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Audio AMP***

Size	Document Number	Rev
A4	Storm	-1

Date: Monday, June 25, 2012 Sheet 30 of 102

Blanking

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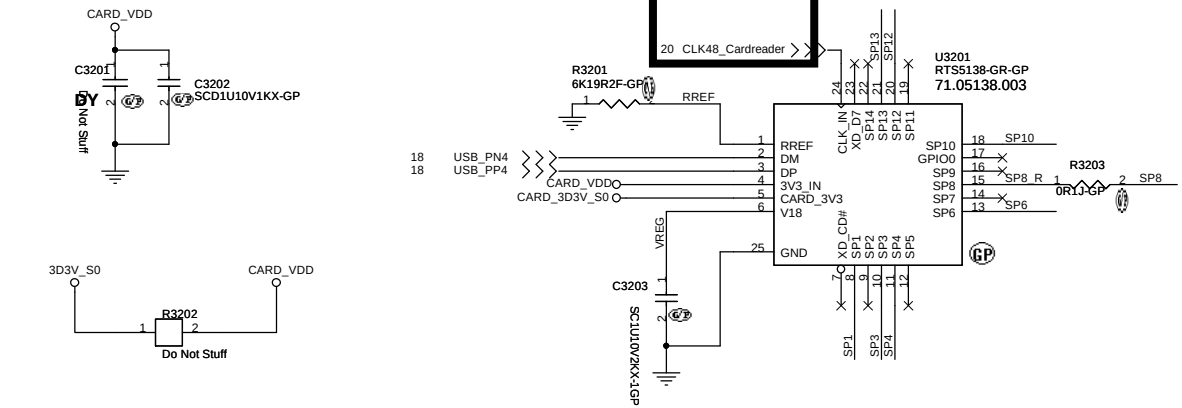
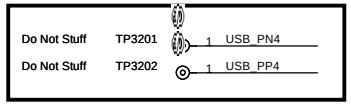
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

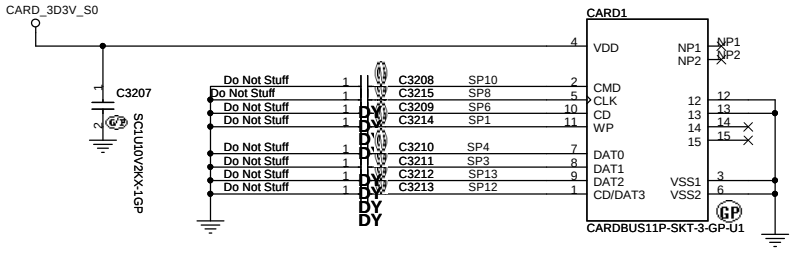
Title	AR8158	
Size A3	Document Number Storm	Rev -1
Date: Monday, June 25, 2012	Sheet 31 of 102	



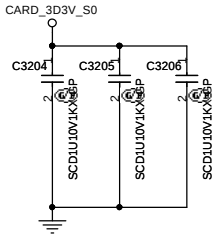
1	RREF	I	Connect external resistor (6.2K ± 1%) to reference ground
2	DM	I/O	USB D- signal
3	DP	I/O	USB D+ signal
4	3V3_IN	I	3.3V power input
5	CARD_3V3	O	3.3V power for all cards
6	V18	O	Regulated supply voltage (1.8V ±10%) from internal 3.3V to 1.8V regulator; supplies internal digital circuits. An external capacitance should be connected
7	XD_CD#	I	xD Card Detect (xD_CD#)
8	SP1	I/O	xD Ready Signal (xD_RDY), SD Write Protect (SD_WP) and MS Clock (MS_CLK)
9	SP2	I/O	xD RE# and MS Card Detect (MS_INS#)
10	SP3	I/O	xD CE# and SD Data 1 (SD_DAT1)
11	SP4	I/O	xD_CLE, SD Data 0 (SD_DAT0) and MS Data 7 (MS_D7)
12	SP5	I/O	xD ALE, SD Data 7 (SD_DAT7) and MS Data 3 (MS_D3)
13	SP6	I/O	xD_WE# and SD Card Detect (SD_CD#)
14	SP7	I/O	xD Write Protect (xD_WP), SD_Data 6 (SD_DAT6) and MS Data 6 (MS_D6)
15	SP8	I/O	xD_Data 0 (xD_D0), SD_Clock (SD_CLK) and MS_Data 2 (MS_D2)
16	SP9	I/O	xD Data 1 (xD_D1), SD Data 5 (SD_D5) and MS Data 0 (MS_D0)
17	GPIO0	I/O	General purpose input/output with interrupt ability
18	SP10	I/O	xD Data 2 (xD_D2) and SD command signal (SD_CMD)
19	SP11	I/O	xD Data 3 (xD_D3), SD Data 4 (SD_DAT4) and MS Data 4 (MS_D4)
20	SP12	I/O	xD Data 4 (xD_D4), SD Data 3 (SD_DAT3) and MS Data 1 (MS_D1)
21	SP13	I/O	xD Data 5 (xD_D5), SD Data 2 (SD_DAT2) and MS Data 5 (MS_D5)
22	SP14	I/O	xD Data 6 (xD_D6) and MS BS
23	XD_D7	I/O	xD Data 7 (xD_D7)
24	CLK_IN	I	48MHz clock directly input

FOR SIV,PLS near U3201





62.10051.E11



Near CARD1 Pin11, Pin18, Pin22

STORM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CARDREADER

Size: A3 | Document Number: Storm | Rev: -1

Date: Monday, June 25, 2012 | Sheet 32 of 102

Reserved

STORM

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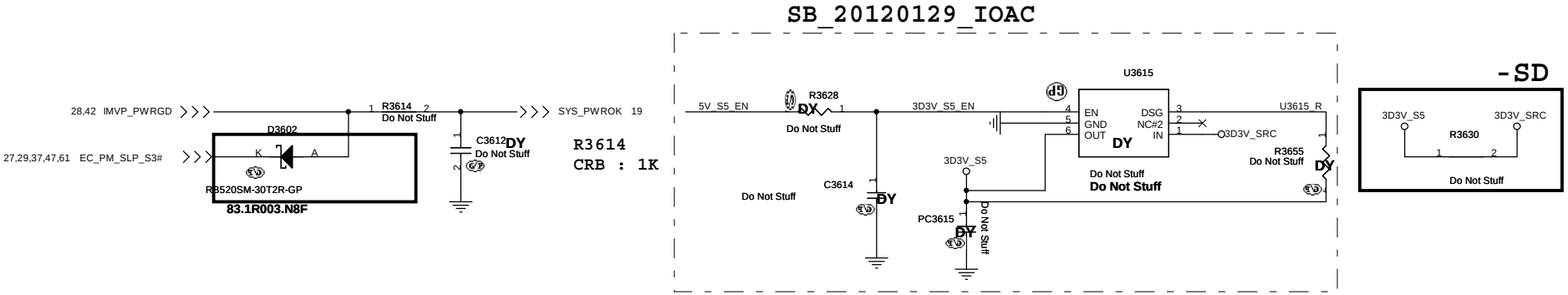
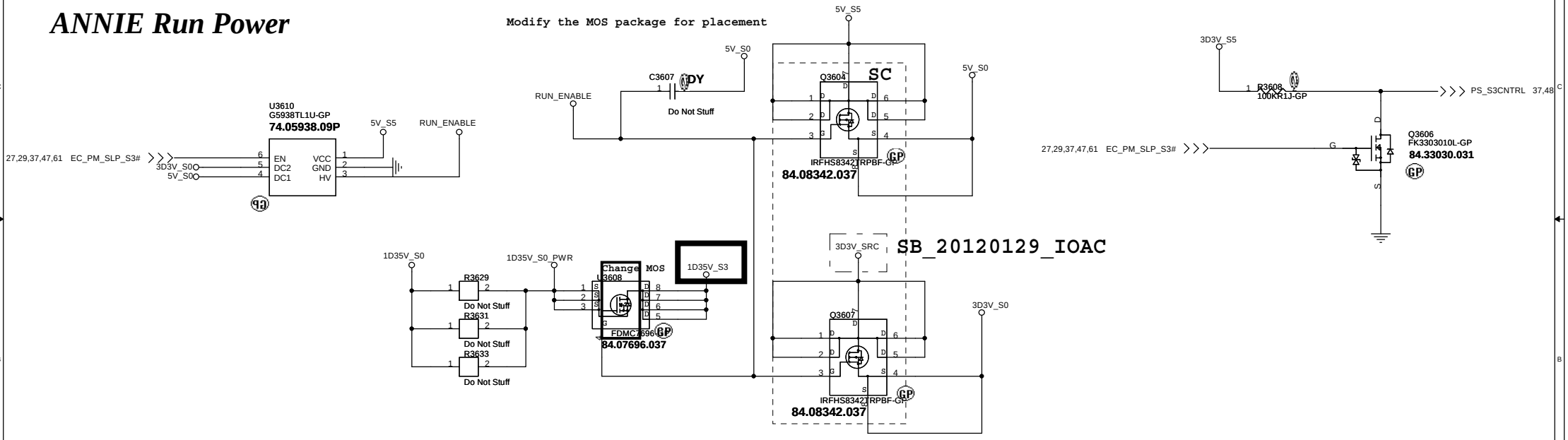
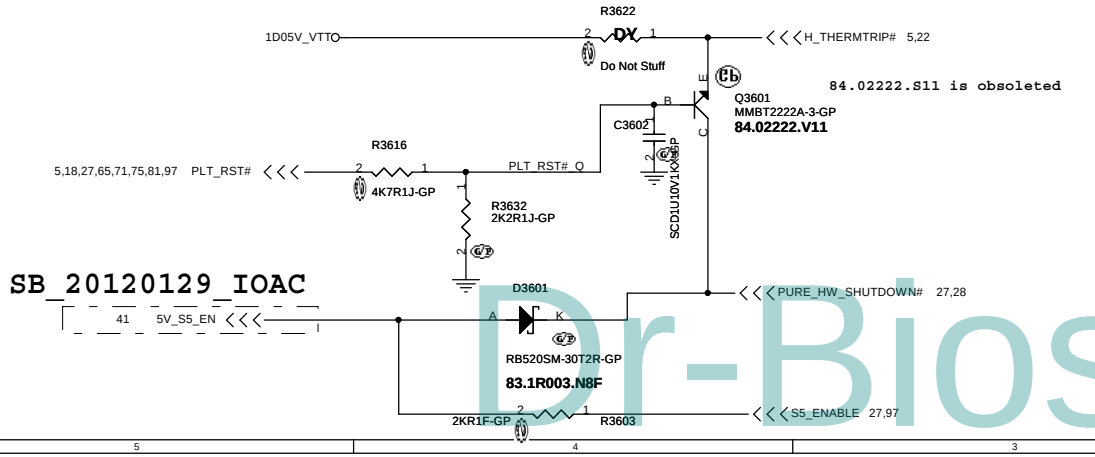
Title: *Reserved*	
Size: A3	Document Number: Storm — Rev: -1
Date: Monday, June 25, 2012	Sheet 33 of 102

Power Sequence



ANNIE Run Power





STORM

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Title	***Power Plane Enable***
Size A3	Document Number: **Storm** — Rev: **-1**
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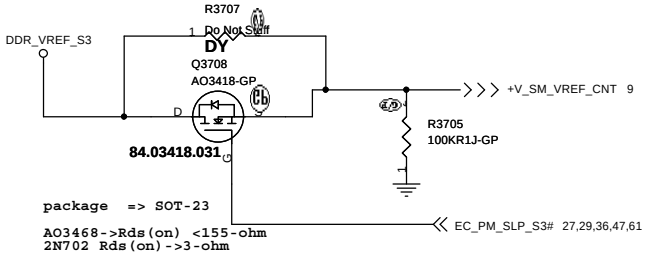
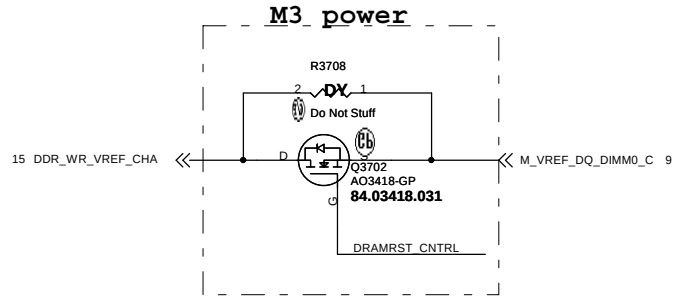
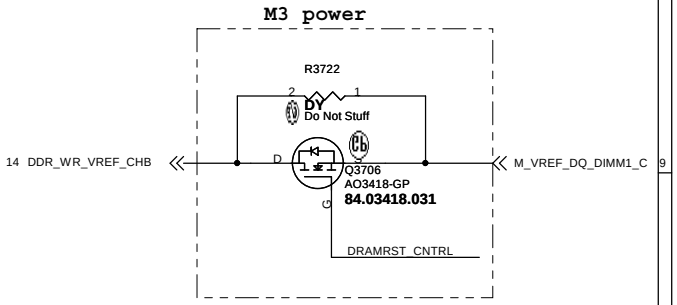
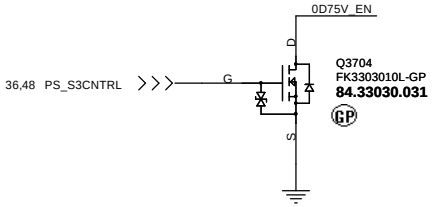
Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation

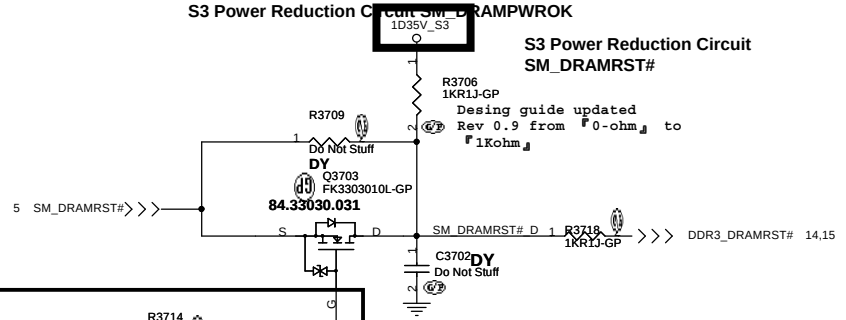


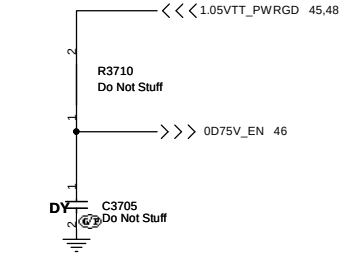


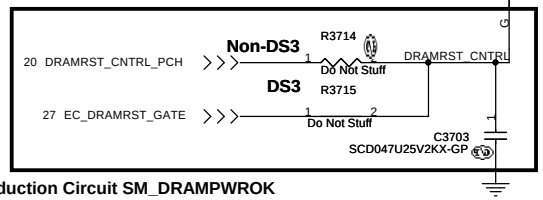




Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK

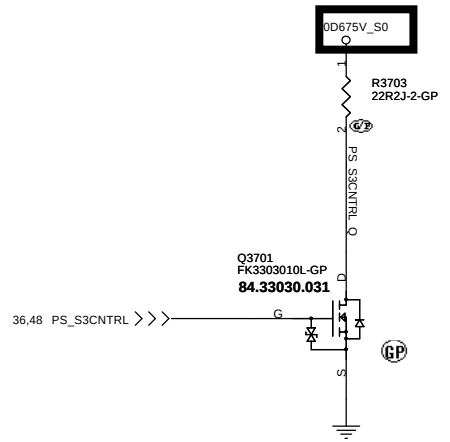


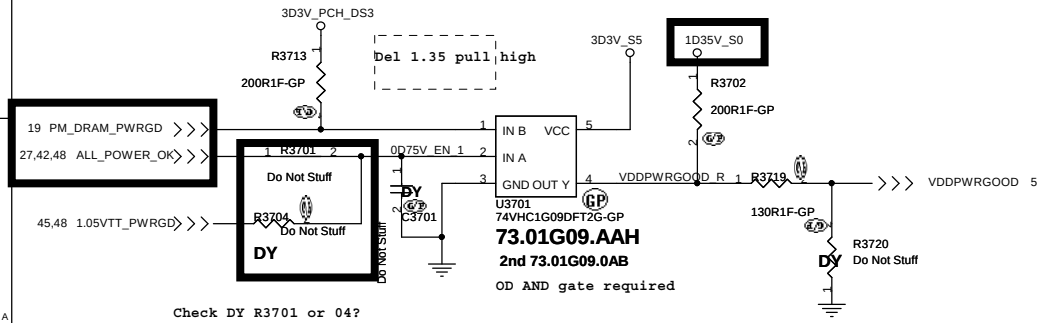




Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK

Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK





Check DY R3701 or 04?

For U3701 not OD AND gate
R3719 to 64.15015.6DL
R3720 to 64.75005.6DL
R3702 to DY

SM_DRAMPWROK must have a maximum of 15ns rise or fall time
over VDDQ * 0.55± 200mV and the edge must be monotonic

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Title: ADAPTER

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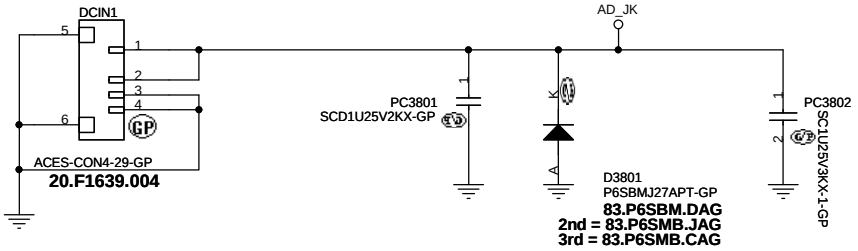
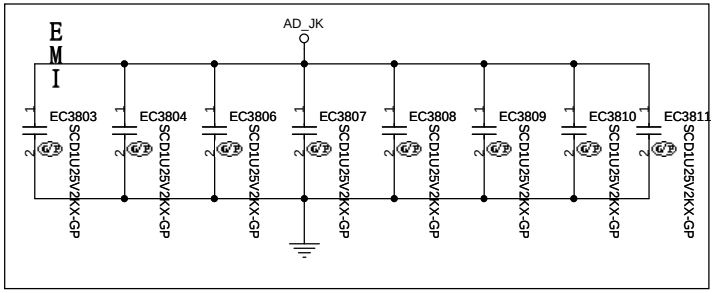
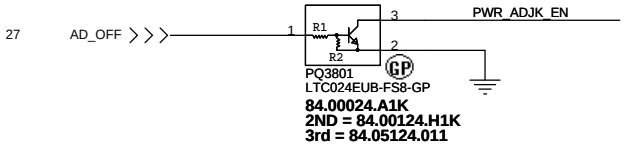
ANNIE solution

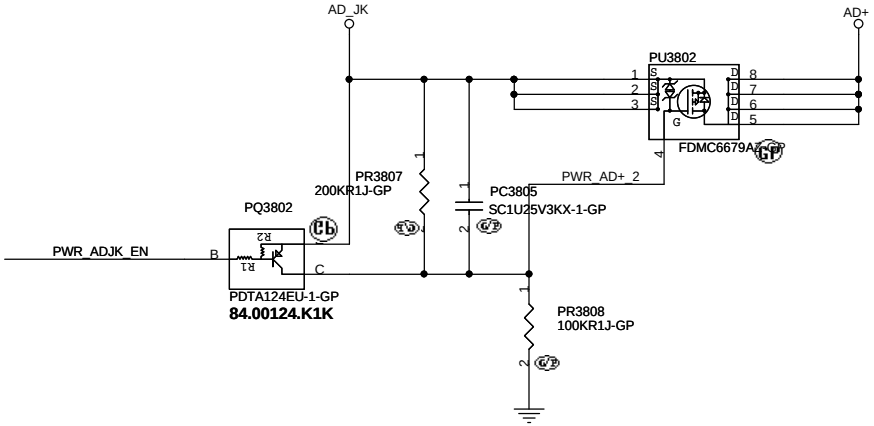
1Pin=3A

Adaptor in to generate DCBATOUT









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Title: ***DCIN JACK***

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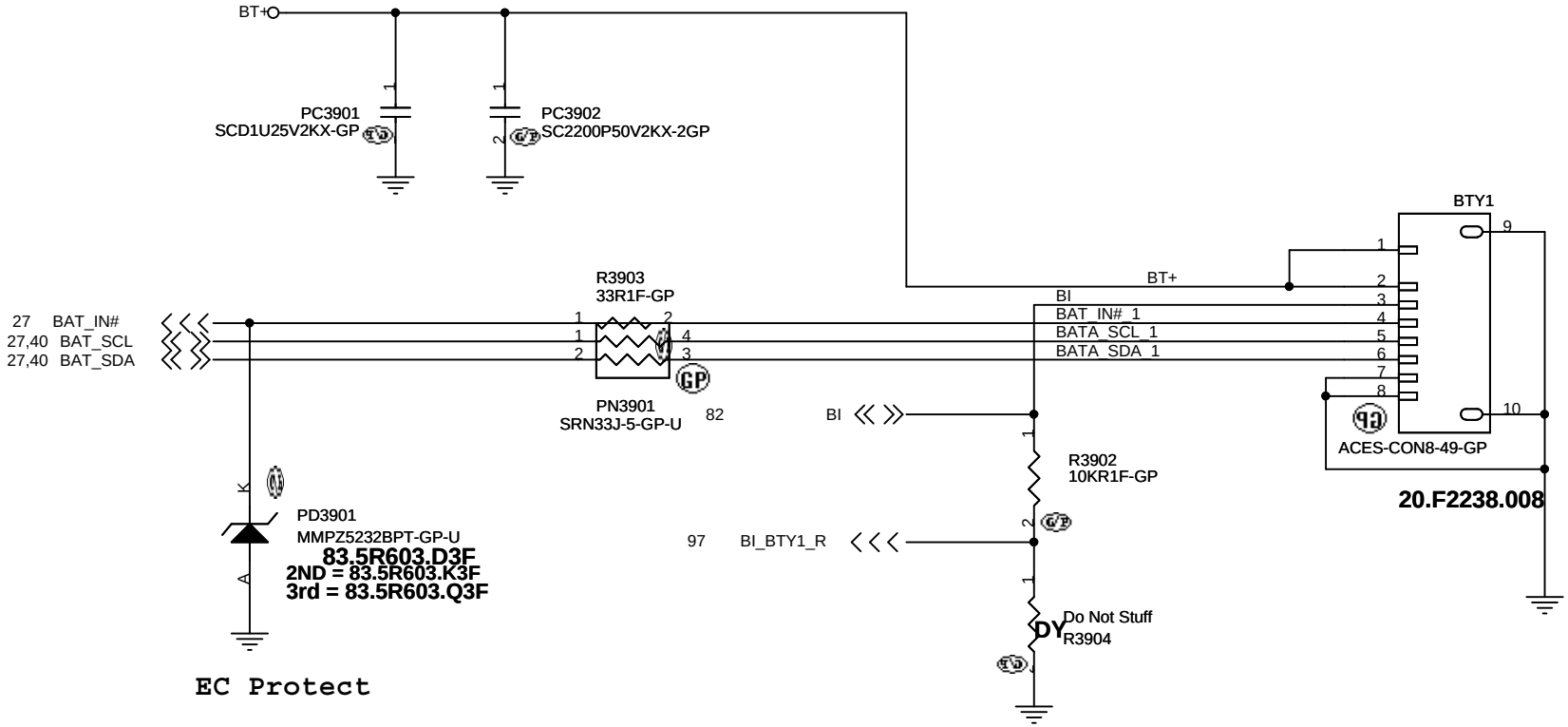
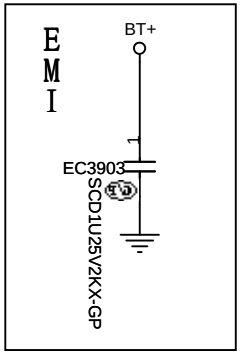
BATTERY CONNECTOR





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Title: **BATT CONN**		
Size: A4	Document Number: **Storm**	Rev: **-1**
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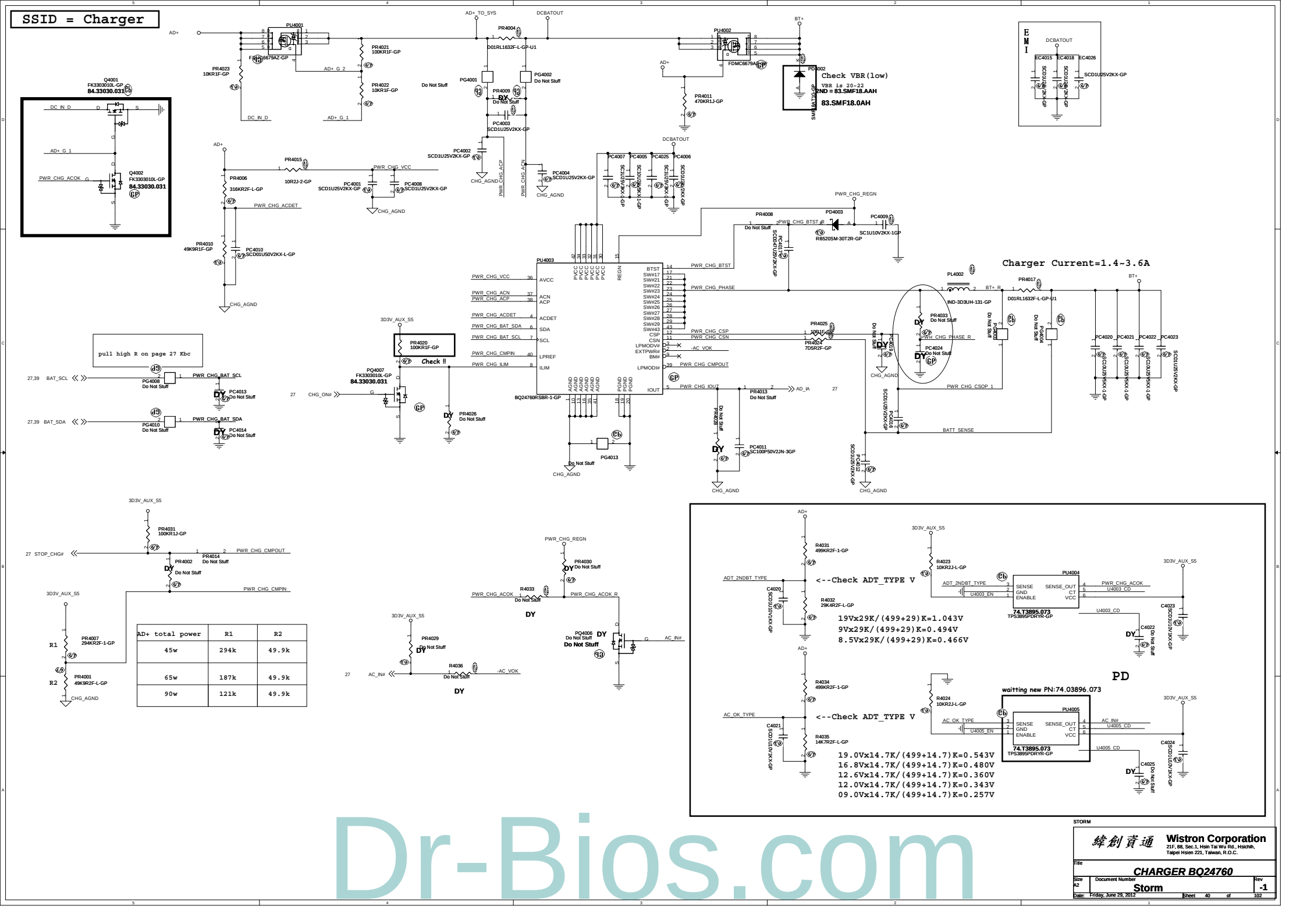
SSID = Charger



AD+ total power	R1	R2
45w	294k	49.9k
65w	187k	49.9k
90w	121k	49.9k

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Title: CHARGER BQ24760

Size: A2 | Document Number: Storm | Rev: -1

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SSID = PWR.Plane.Regulator_3p3v5v

BOM control

	Main source	2nd source
PU4101	84.03664.037 (FDMS3664S) Mount	84.00038.A37 (RJK03P8DPA) Mount

DEL OUTPUT GAP

PU4103 need change to TPS51275A
PN:74.51275.003
waiting for symbol

Design Current = 15A
25.1A<OCP< 29.3A

For Power concern

77.C2271.39L
2nd = 77.22271.33L
3nd= 77.52271.13L

77.22271.27L
2nd=79.22710.20L

Del TP4702 by placement

See Table 1

TPS51275RUKR-GP

Iomax=5A
OCP>7.5A

Vout = 2 * (1 + R1/R2)
= 2 * (1 + 6.8K / 10K)
= 3.36V

Close to VFB Pin (pin5)

Vout = 2 * (1 + R1/R2)
= 2 * (1 +33K / 21K)
= 5.14V

Close to VFB Pin (pin2)

Close Pu4106 Pin3

Vo=1.25*(1+(R1/R2))

Table 1. SKIP mode operation (51275/A)

	SKIPSEL	Skip mode operation
51275	n/a	Auto-skip
51275A	Hi	OOA
	Lo	Auto-skip

SB_20120113_IOAC

3D3V OCP setting PR4107
5V OCP setting PR4103

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Title: TPS51125A 5V/3D3V

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SSID = CPU.Regulator

Volterra's suggestion:
VCC 31x22uF(0603) for 1-PHASE VCC
VCCAXG 28x22uF(0603) for 1-PHASE VCCAXG

Boot Voltage	PR4265	PR4204
0V	825ohm	825ohm
1V	191ohm	191ohm

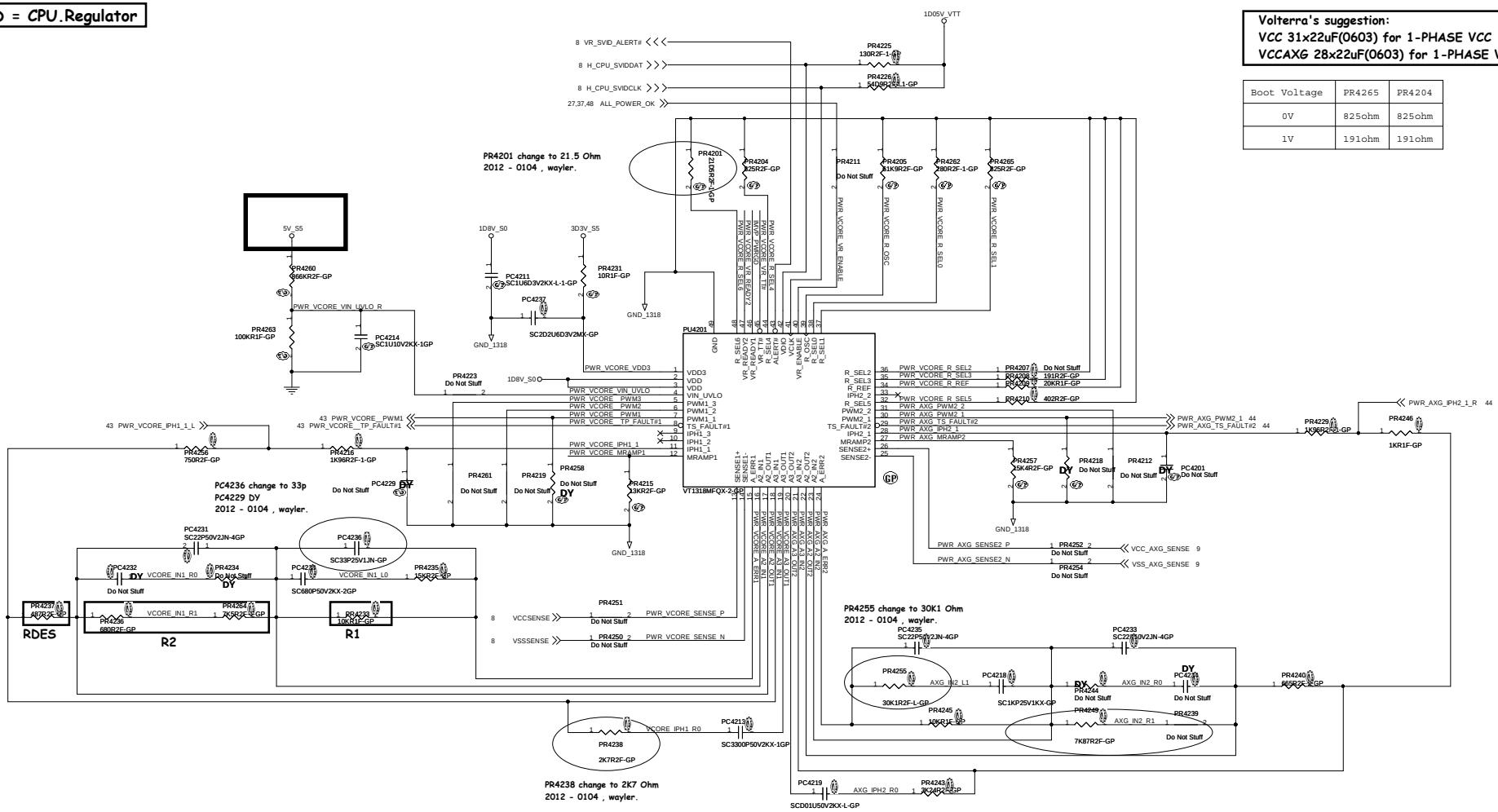

Table 1: R_{DES} Selection Table

1	20	20	1150
1	24	32	976
1	28	36	845
1	32	40	732
1	36	44	649
1	40	52	590
1	44	56	536
1	48	64	487
2	40	48	590
2	48	64	976
2	56	72	845
2	64	80	732
2	72	96	649
2	80	104	590
2	88	112	536
2	96	128	487
3	60	72	787
3	72	96	787
3	84	108	665
3	96	120	590
3	108	144	523
3	120	156	475
3	132	168	432
3	144	192	392

R_1 and R_2 Selection

Along with R_{DES}, The values of R_1 and R_2 determine the load line according to Equation 4.

Equation 4

$$R_{LL}[\Omega] = \frac{R_1}{R_2} * \frac{1}{22} * R_{DES} * \frac{1}{K_f}$$

→ RLL is inverse proportion to R2

Kf=95000

With K_f being the slave current feedback gain and R_1 having a typical value of 10kΩ. Next, the required value of R_2 can be calculated to achieve the desired load line via Equation 4 and previously selected values for R_1 and R_{DES}.

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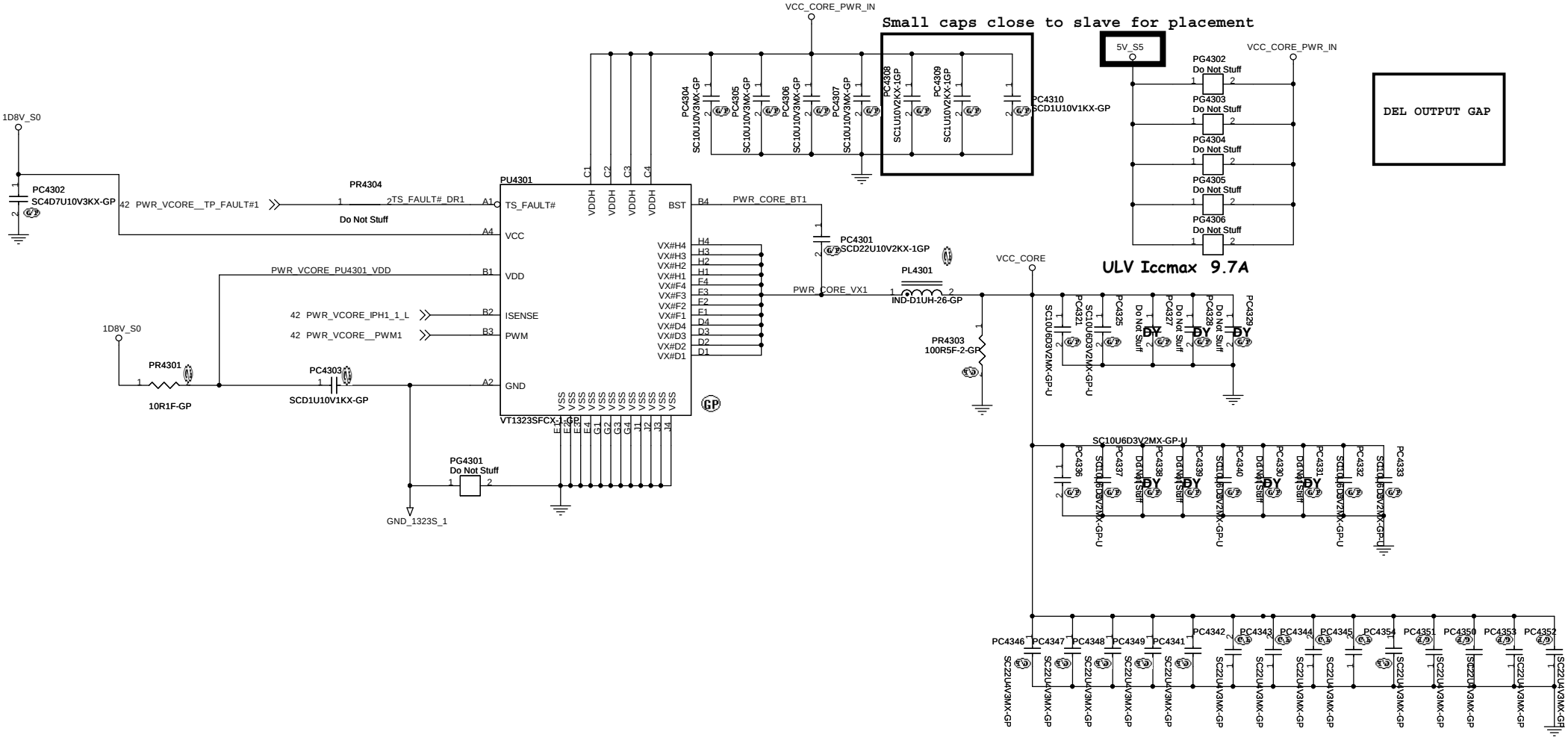
Title: VT1318+1323_CPU_CORE2+1(1/3)

Size: Document Number: Storm Rev: -1

Date: Wednesday, June 27, 2012 Sheet 42 of 102



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Title: *VT1318+1323 CPU CORE2+1(2/3)*

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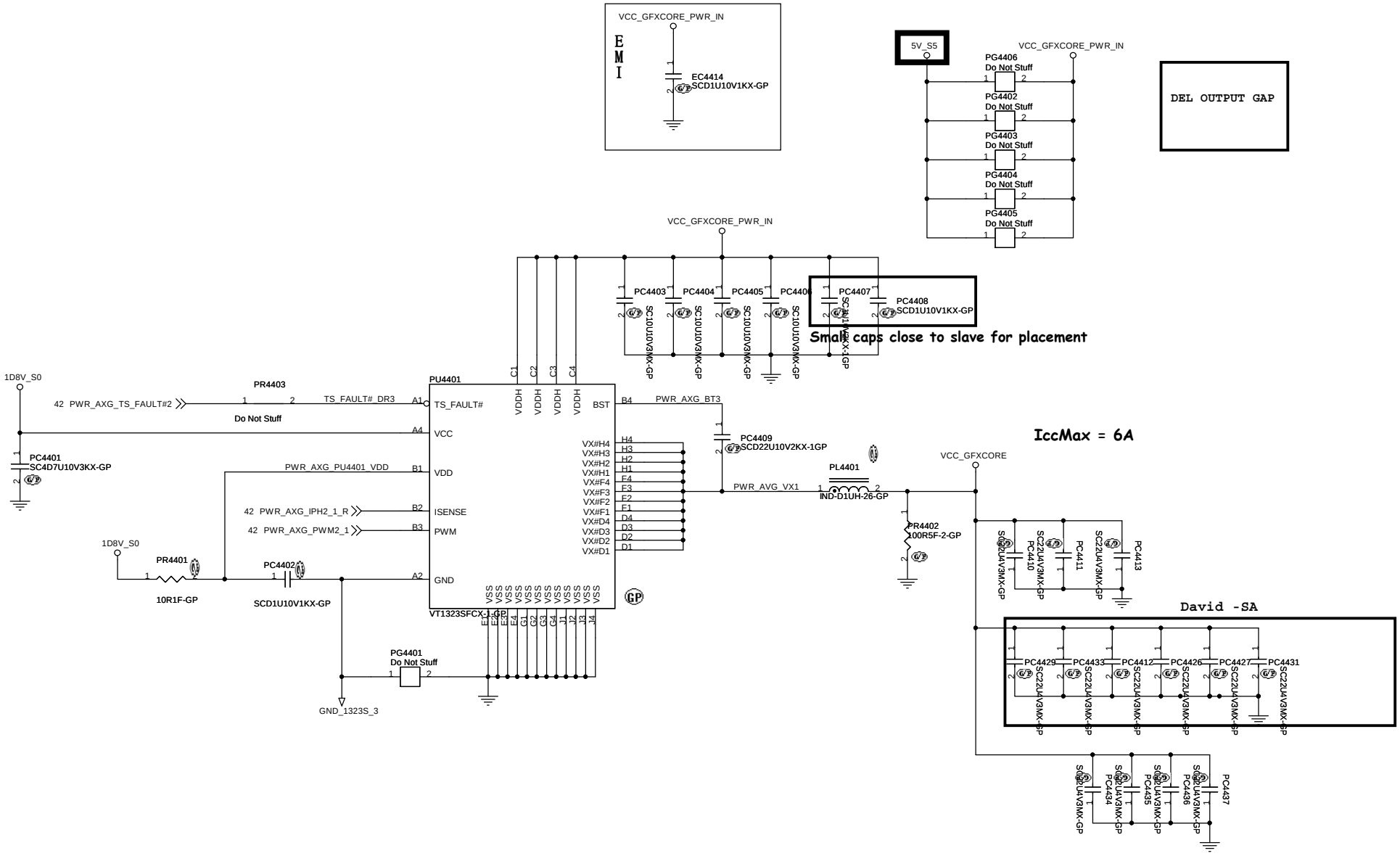

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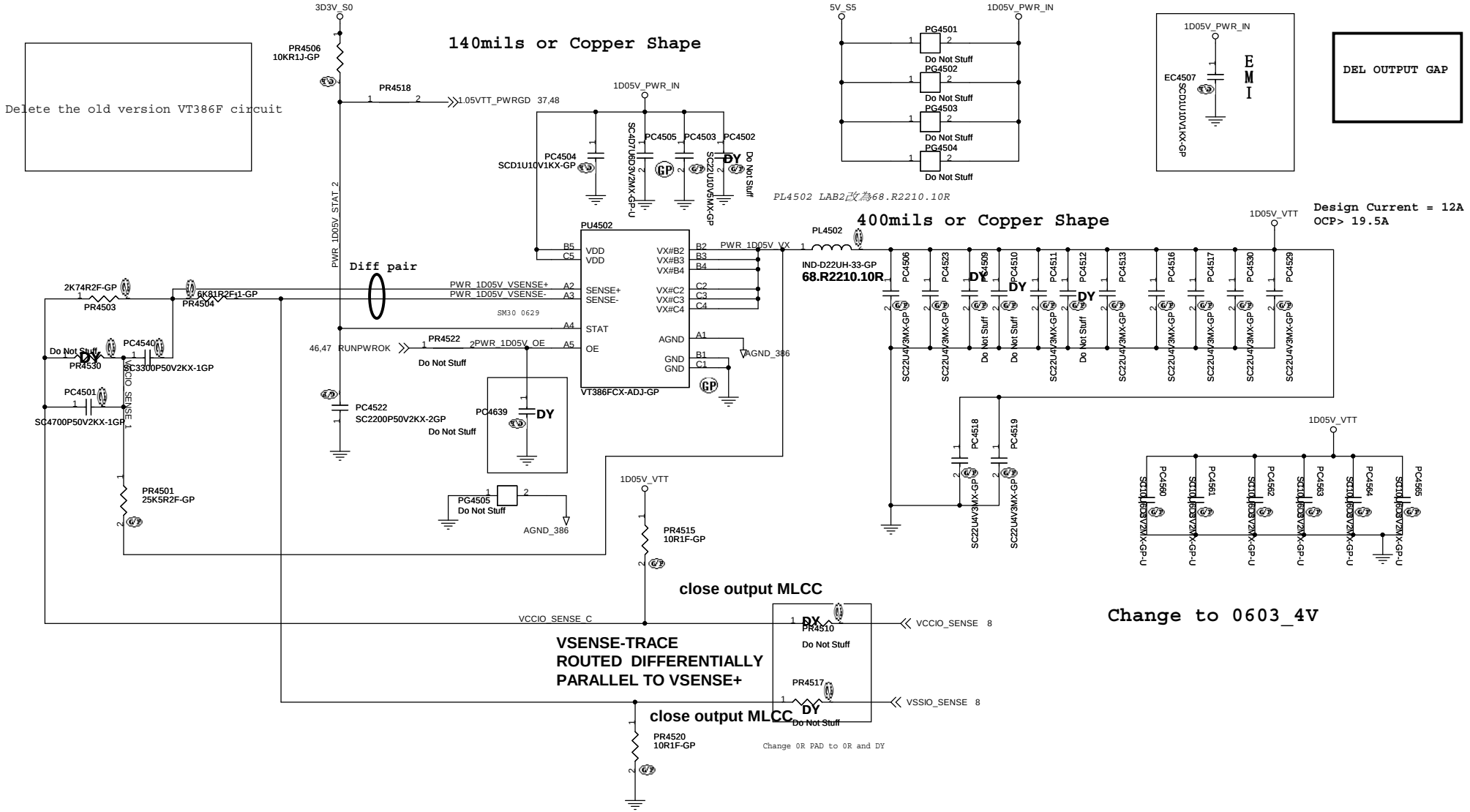
Title: VT1318+1323_CPU_CORE2+1(3/3)

Size	Document Number	Rev
	Storm	-1

Date: Monday, June 25, 2012 Sheet 44 of 102



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Title: VT386 +1.05V VTT

Size: A3 | Document Number: Storm | Rev: -1

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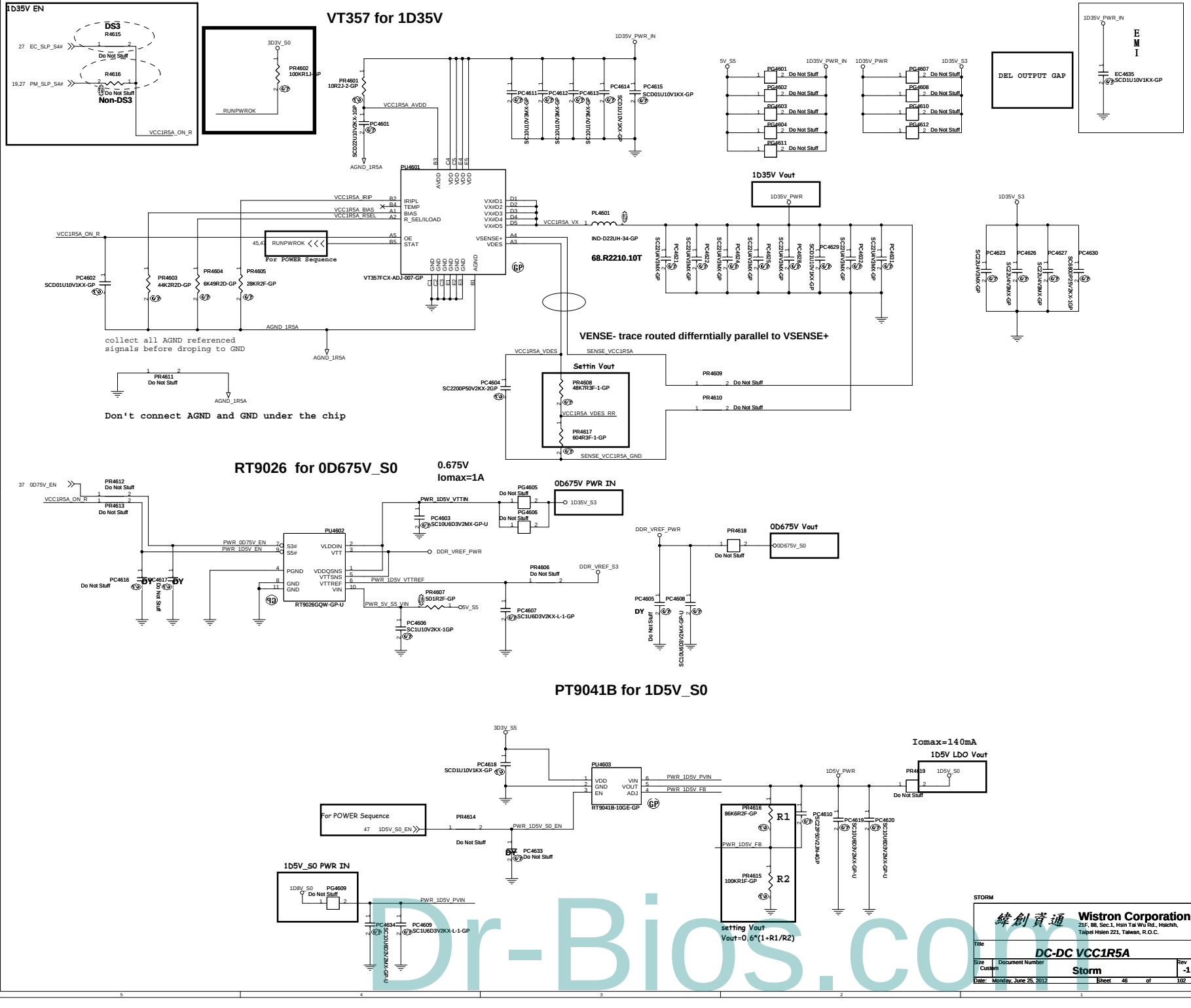

STORM

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Title: **DC-DC VCC1R5A**

Size	Document Number	Rev
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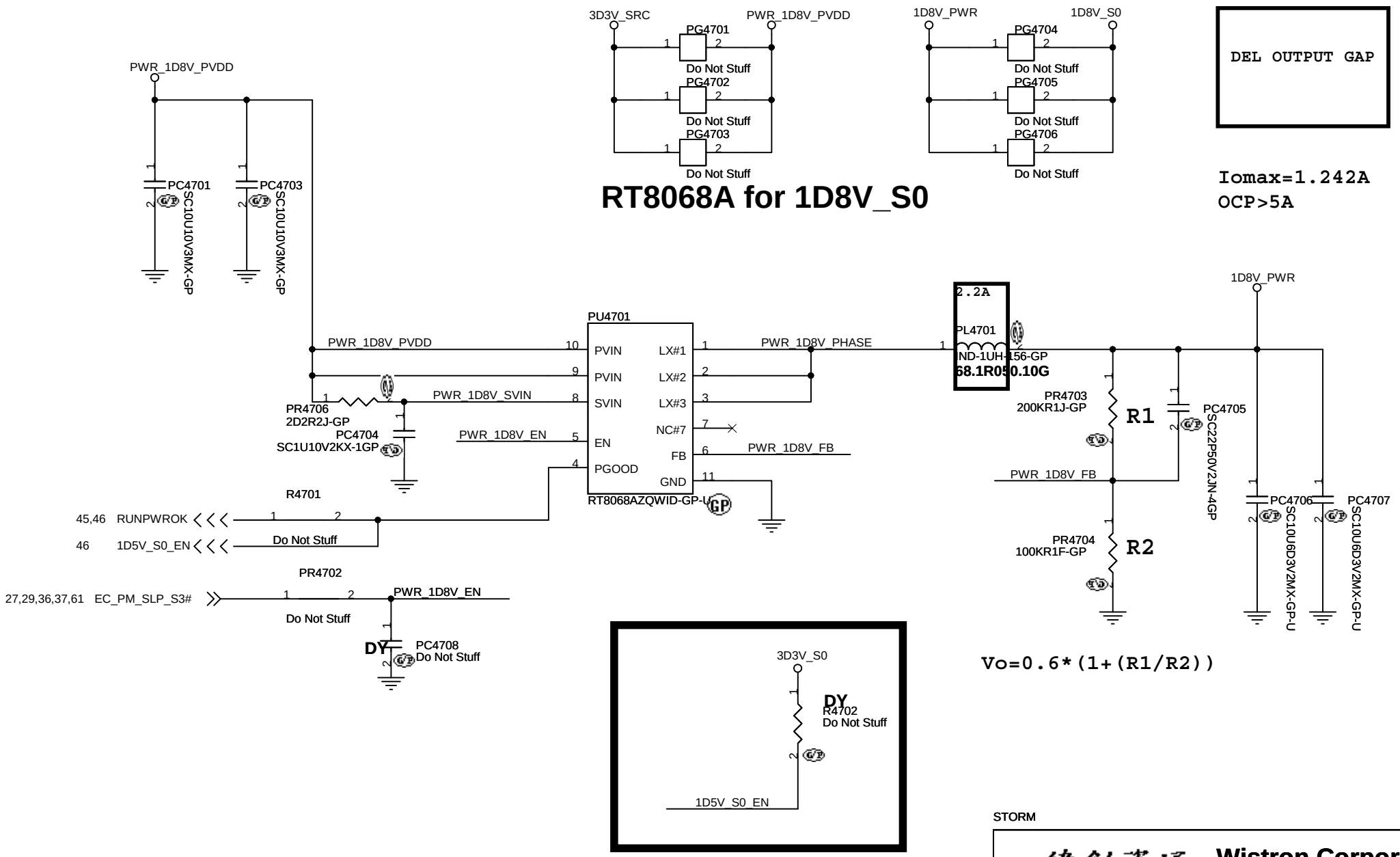

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Title: 1D8V_S0 SYW231

Size	Document Number	Rev
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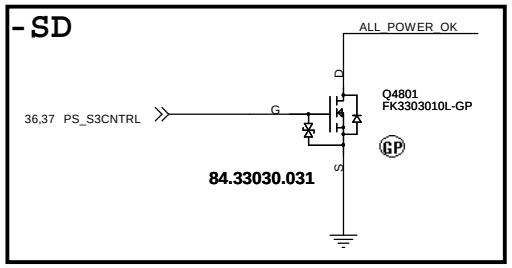
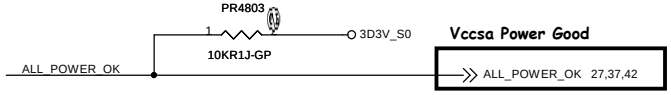
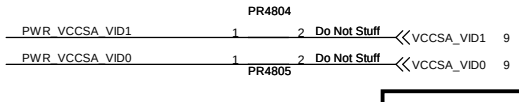
SY8037 for VCCSA

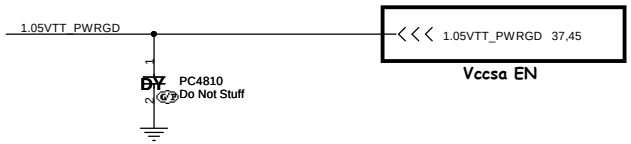


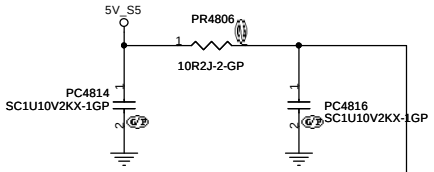
VID0	VID1	VCCSA ULV
L	L	0.9V
L	H	0.85V
H	L	0.775V
H	H	0.75V





DEL OUTPUT GAP

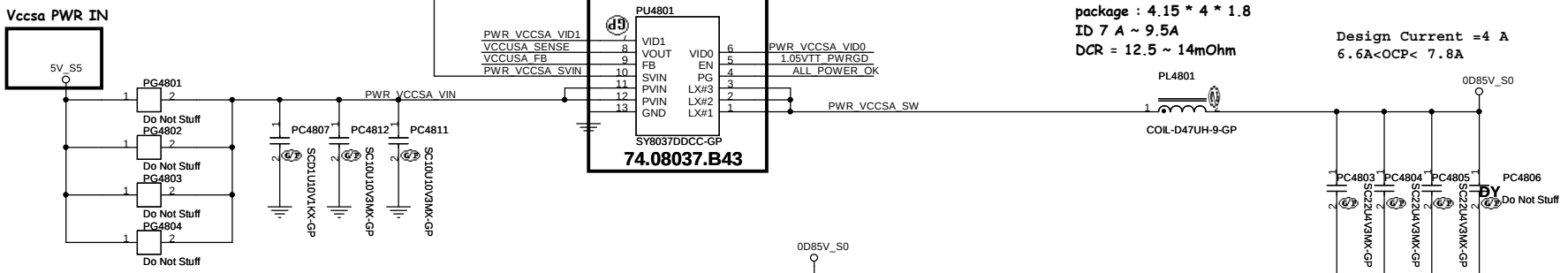


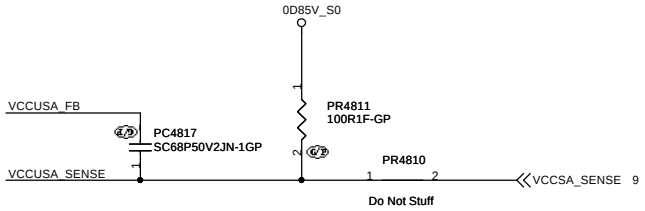


1227 SA

CYNTEC - PCMB042T-R47MS
package : 4.15 * 4 * 1.8
ID 7 A ~ 9.5A
DCR = 12.5 ~ 14mOhm

Design Current =4 A
6.6A<OCP< 7.8A





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Title	SY8037_VCCSA
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SSID = VIDEO

EDP CONNECTOR

EDP1

IPEX-CON30-4-GP-U

20.F1407.030

CPU_EDP_DATA1# C C4913 — SCD1U10V1KX-GP — CPU_EDP_DATA1# 4
CPU_EDP_DATA1 C C4912 — SCD1U10V1KX-GP — CPU_EDP_DATA1 4
CPU_EDP_DATA0# C C4908 — SCD1U10V1KX-GP — CPU_EDP_DATA0# 4
CPU_EDP_DATA0 C C4907 — SCD1U10V1KX-GP — CPU_EDP_DATA0 4
CPU_EDP_AUXP C C4901 — SCD1U10V1KX-GP — CPU_EDP_AUX 4
CPU_EDP_AUXN C C4906 — SCD1U10V1KX-GP — CPU_EDP_AUX# 4

LCD DD — R4909 Do Not Stuff — LCDVDD
LCD_Self_Test — TP4901 Do Not Stuff
DBC_EN_C — R4908 33R1J-GP — DP_HPD0_C
BLON_OUT_C
LCD_BRIGHTNESS — R4907 33R2J-L1-GP — PCH_BKLT_CTL 17
DCBATOUT_LCD

DCBATOUT_LCD — F4901 POLYSW-1D1A24V-GP-U 69.50007.A31 2nd = 69.50007.A41 — DCBATOUT
C4914 SC10U25V5KX-1-GP
C4916 SC1KP25VJKX-GP
C4915 SCD1U25V2KX-GP

CPU_EDP_HPD# 4
DP_HPD0_C — R4922 100KR1J-GP — Q4901 FK3303010L-GP 84.33030.031

3D3V_S0
DY R4923 Do Not Stuff — DY R4924 Do Not Stuff
4 CPU_EDP_AUX#
4 CPU_EDP_AUX
DY R4926 Do Not Stuff — DY R4925 Do Not Stuff

27 BLON_OUT — R4904 1KR2J-L2-GP — BLON_OUT_C
R4911 100KR1J-GP
C4917 SC100P25V1KX-GP

Camera Power

3D3V_S0 — F4902 69.4R500.141 2nd = 69.4R500.151 — 3D3V_CAMERA_S0
C4903 SC10U10V3MX-GP
6V 0.5A

output turn-0n Rising TIme:1.3ms~2.7ms
current limit:2~3.3A
Previous parts(74.05285.07F)rise time:1.5ms ~5ms
current limit:1.5ms~ 3.5ms

CCD1
IPEX-CON20-3-GP
20.F1407.020

7781_SDA 28,68,69
7781_SCL 28,68,69
SENSOR_INT 27,68
TS_INT
Light Sensor
USB_PP3 18
USB_PN3 18
USB_PP6 18
USB_PN6 18
TS_AGND
Touch
CCD
5V_TS_S0
3D3V_CAMERA_S0

3D3V_S0 — R4913 DY Do Not Stuff — 5V_TS_S0
5V_S0 — F4903 FUSE-D5A6V-2-GP 69.4R500.141 2nd = 69.4R500.151
C4904 SC10U10V3MX-GP

3D3V_S0
U4901 G5244A31U-GP 74.05244.073
IN, NC#2, DSG — OUT, GND, EN
U4901_R
PCH_LCDVDD_EN 17
LCDVDD
Layout 40 mil
C4911 SC4D7U10V3KX-GP
R4905 100R1F-GP
DY C4909 Do Not Stuff
C4910 SC4D7U10V3KX-GP

R4912 — 33R2J-L1-GP — Touch_Screen_INT 18
TS_INT — Q4902 Do Not Stuff Do Not Stuff — DY
R4914 Do Not Stuff
TS_AGND

STORM

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Title: LCD/Inverter CONN
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Date: Friday, June 29, 2012 | Sheet 49 of 102

Pull High 5V Design on CRT Board

CRT DDCDATA & DDCCLK level shift

STORM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

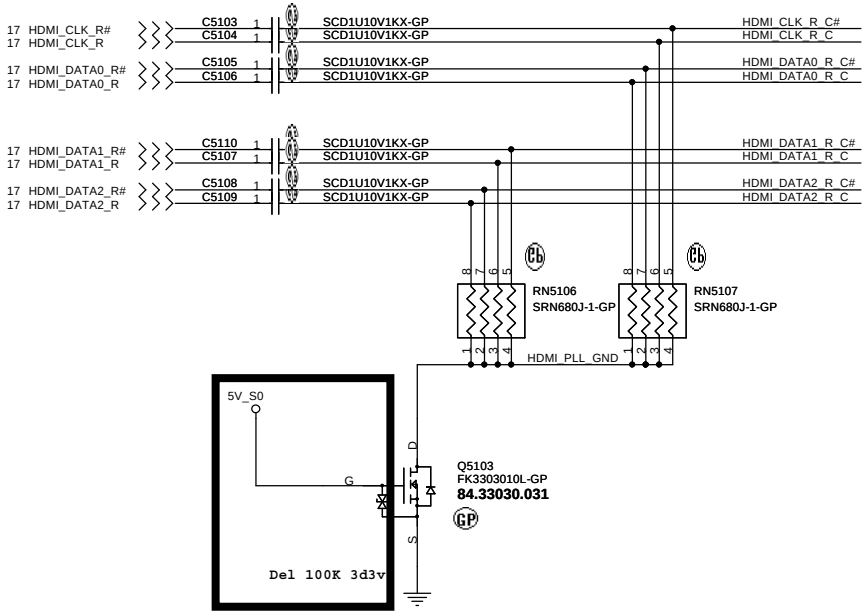
Title: CRT Connector

Size	Document Number	Rev
A3	Storm	-1

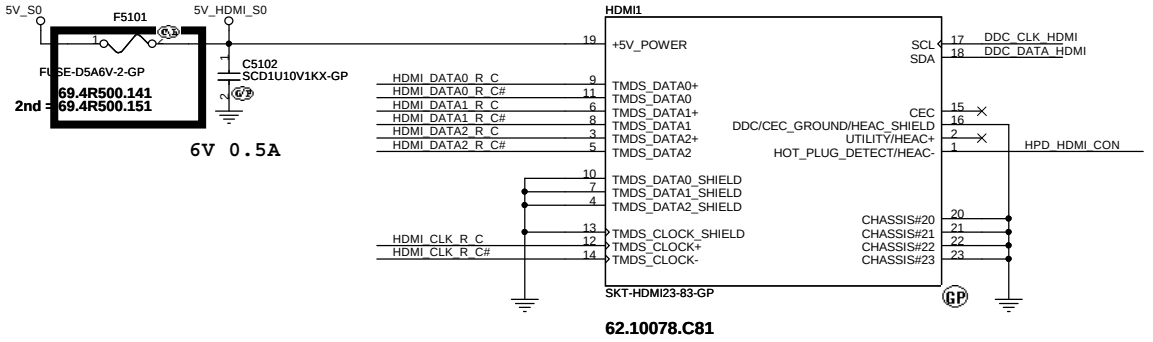
Date: Monday, June 25, 2012 Sheet 50 of 102

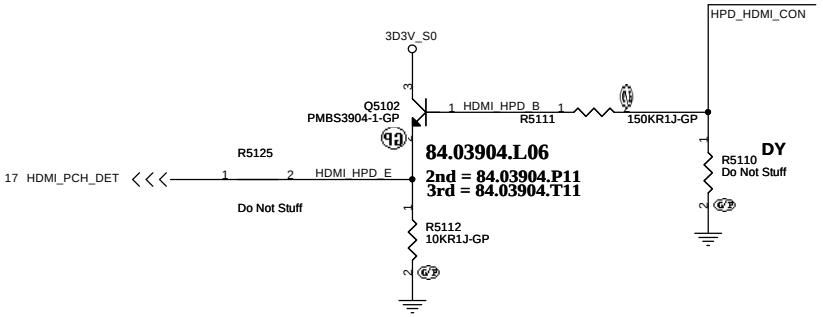
SSID = VIDEO

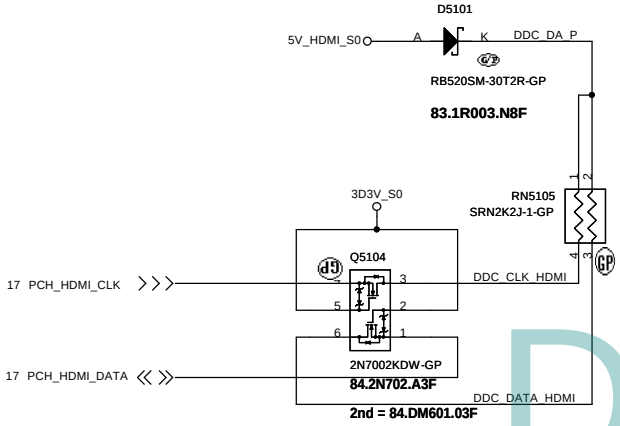
HDMI Level Shifter

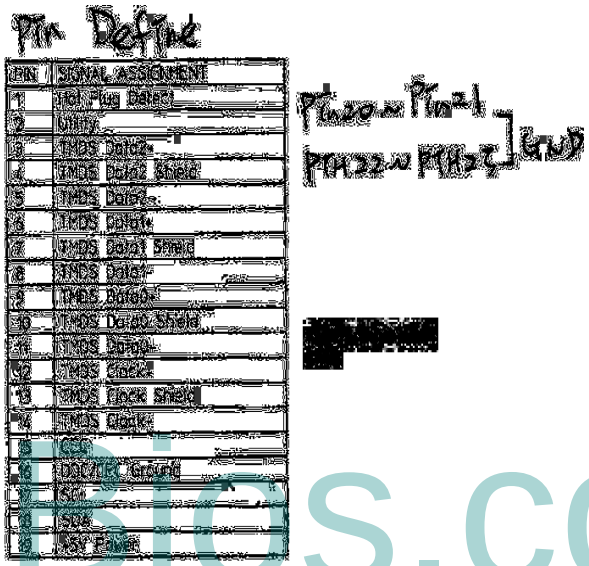


Micro HDMI CONN









STORM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	HDMI Level Shifter/Conn	
Size A3	Document Number: Storm	Rev: -1
Date: Monday, June 25, 2012	Sheet 51 of 102	

LED BACKLIGHT CONVERTER POWER

STORM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *eDP*

Size: A3 | Document Number: Storm | Rev: -1

Date: Monday, June 25, 2012 | Sheet 52 of 102

(Blanking)

STORM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***S-VIDEO***

Size	Document Number	Rev
A4	**Storm**	**-1**

Date: Monday, June 25, 2012 Sheet 53 of 102

(Blanking)

STORM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	**Storm**	**-1**

Date: Monday, June 25, 2012 Sheet 54 of 102

SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.

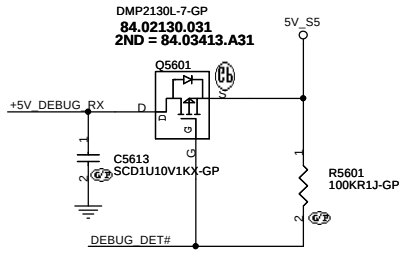
STORM

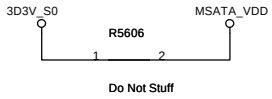
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ITP		
Size: A4	Document Number: Storm	Rev: -1
Date: Monday, June 25, 2012	Sheet 55 of 102	

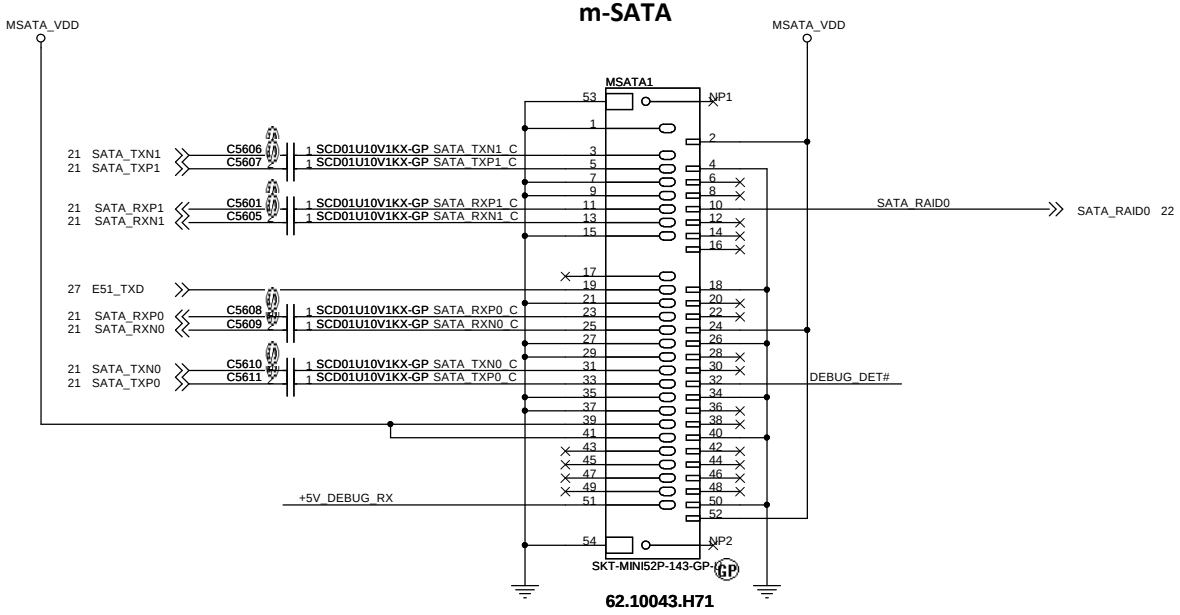
SSID = SATA

MSATA Connector

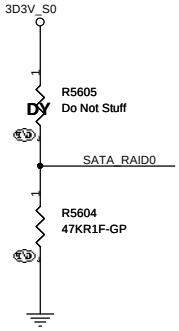


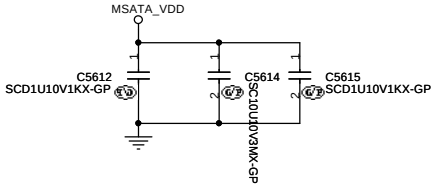


m-SATA



DEBUG CARD





STORM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/ODD

Size	Document Number	Rev
A3	Storm	-1

Date: Monday, June 25, 2012 Sheet 56 of 102

ESATA Power

USB CHARGER

STORM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

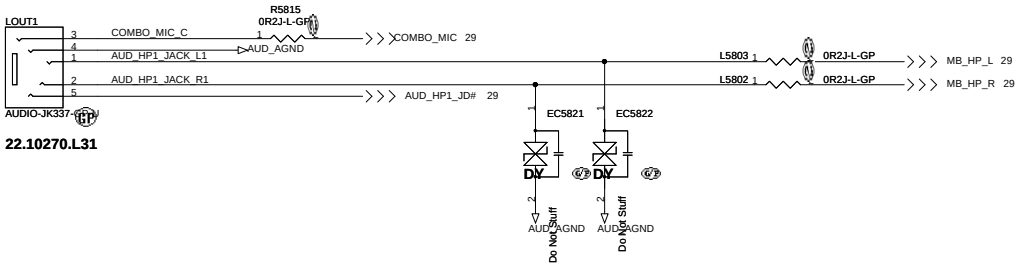
Title: E-SATA/USB CHARGER

Size	Document Number	Rev
A3	Storm	-1

Date: Monday, June 25, 2012 Sheet 57 of 102

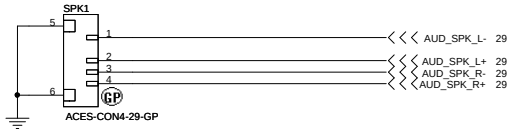
SSID = AUDIO

LINE OUT



22.10270.L31

Speaker Connector



20.F1639.004

STORM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Jack

Size: Custom | Document Number: Storm | Rev: -1

Date: Monday, June 25, 2012 | Sheet 58 of 102

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

Without LAN

STORM

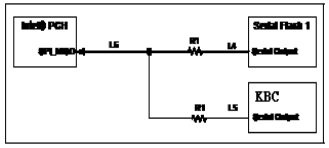
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

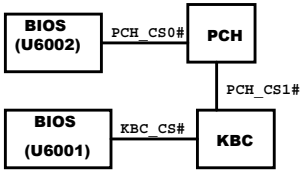
Title: **LAN CONNECTOR**

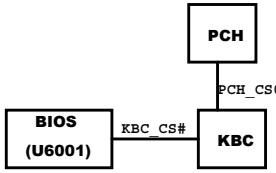
Size	Document Number	Rev
A4	Storm	-1

Date: Monday, June 25, 2012 Sheet 59 of 102

SSID = Flash.ROM

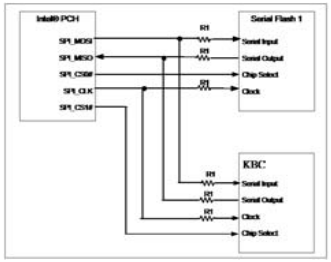


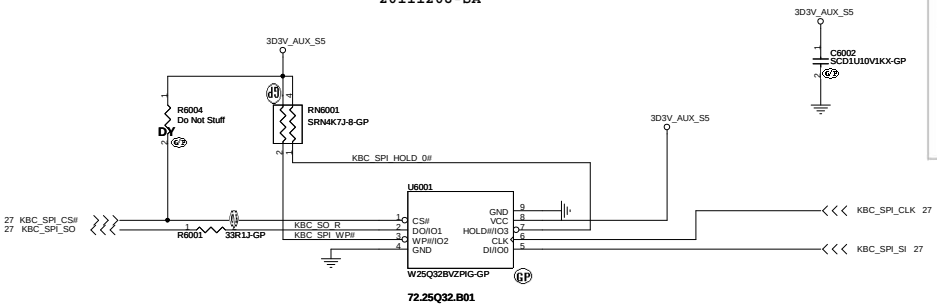




SPI Flash ROM(4M) for KBC

20111208-SA

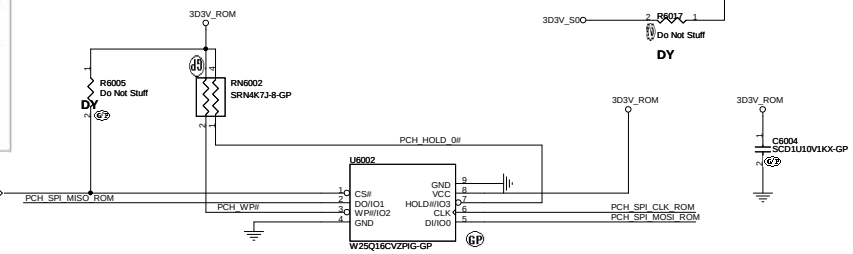




72.25Q32.B01

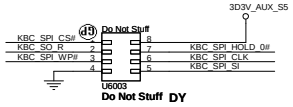
Flash ROM:72.25Q32.B01(4M)

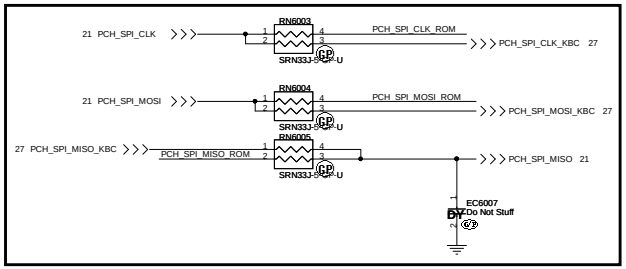
SPI Flash ROM(2M) for PCH

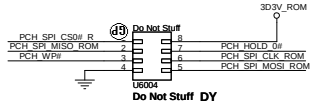


72.25Q16.G01

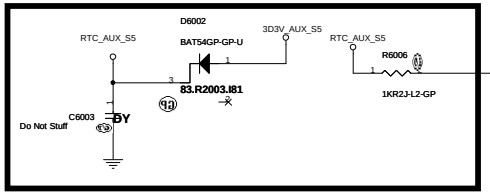
Flash ROM:72.25Q16.G01(2M)

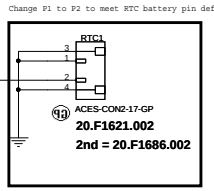






SSID = RBATT





RTC battery charger sircuit

STORM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

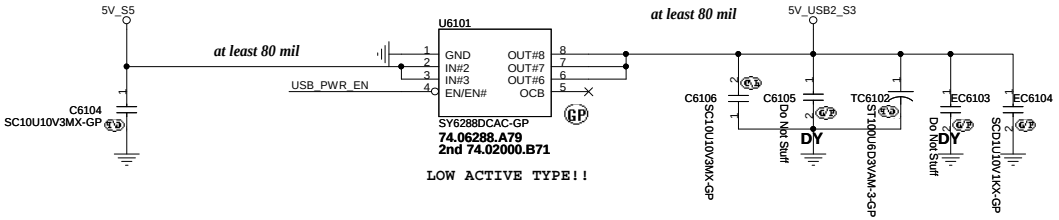
Title: *Flash(KBC+PCH)/RTC*

Size: Custom | Document Number: Storm | Rev: -1

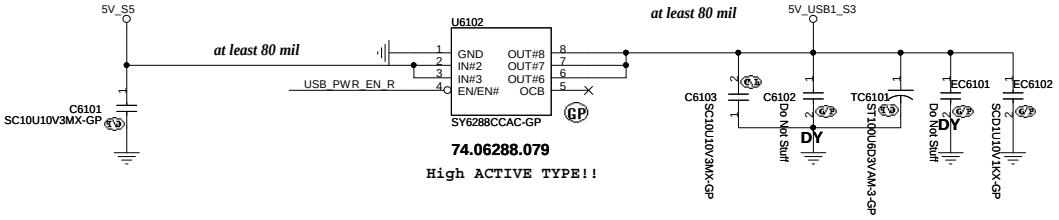
Date: Monday, June 25, 2012 | Sheet 60 of 102

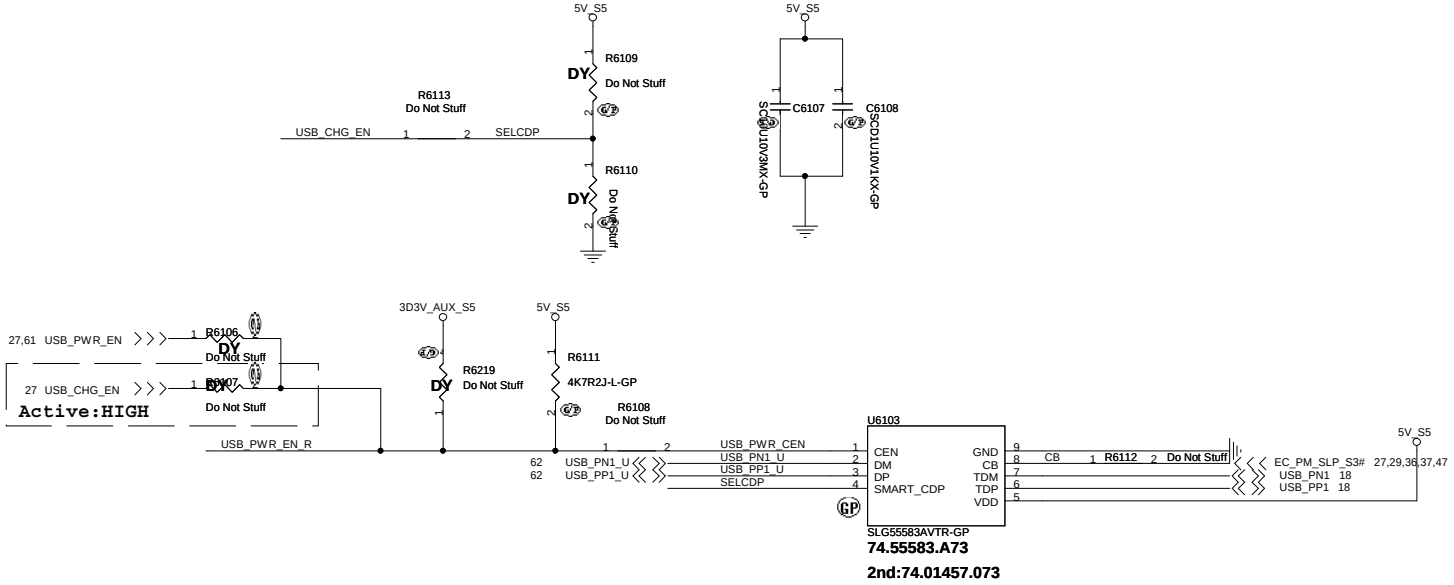
SSID = USB

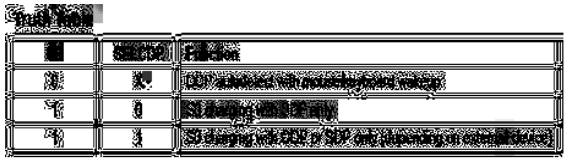
Change Main source
Support 2.45A



Change Main source
Support 2.45A







Pin #	Name	Type	Description
1	CEN#	Output	P-FET Open Drain Output. Current Limit Switch (CLS) Control Output. CB changes from 0 to 1 or 1 to 0. CEN# will be high for 2 seconds (typ)
4	SMART-CDP	Input	Input Control logic (see truth table)
8	CB	Input	Switch Control Bit 0 = autodetection charger identification active 1 = charging downstream port with active USB2.0 data communication mode with 1.5A support

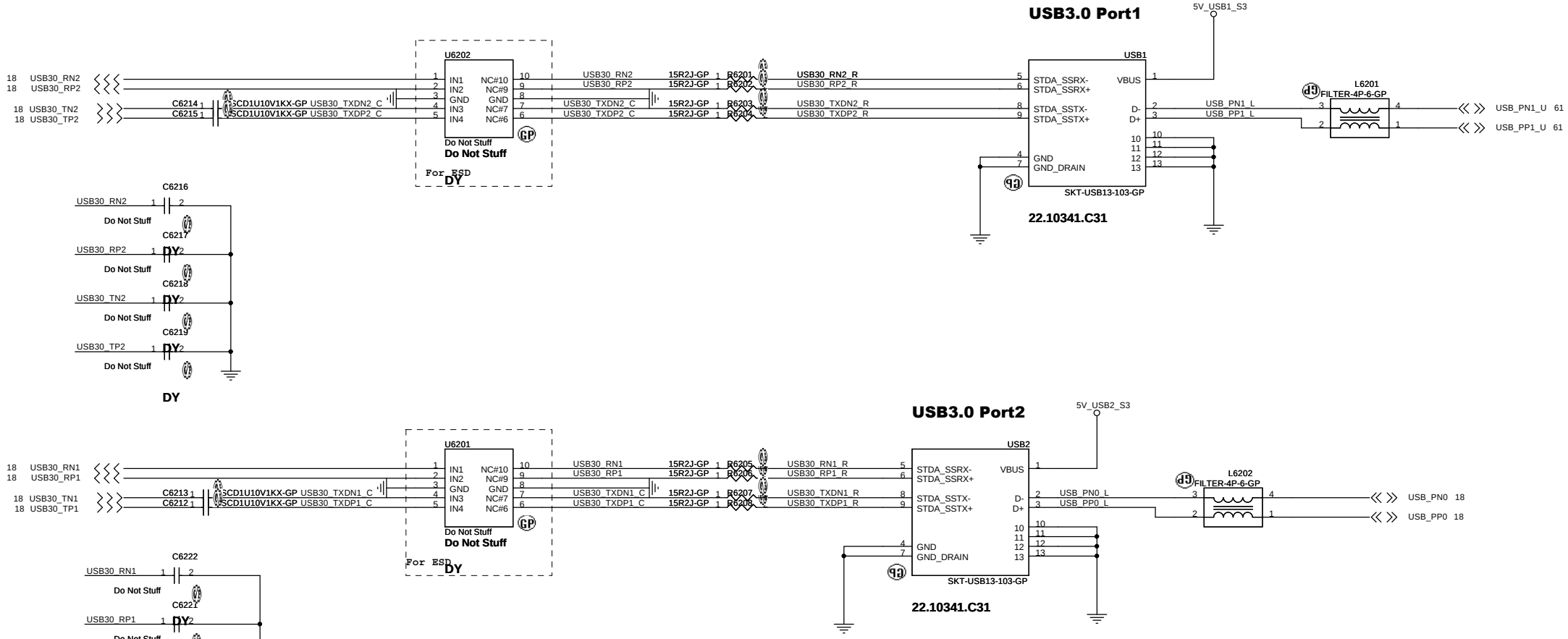
STORM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB Power SW**

Size: Custom | Document Number: Storm | Rev: -1

Date: Monday, June 25, 2012 | Sheet 61 of 102



JE40 modify

USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX-
6	StdA_SSRX+
7	GND
8	StdA_SSTX-
9	StdA_SSTX+

STORM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB 3.0 Port**

Size	Document Number	Rev
A3	Storm	-1

Date: Tuesday, June 26, 2012 Sheet 62 of 102

SSID = User.Interface

Bluetooth Module conn.

Without BT

STORM

緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

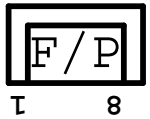
Title: ***Bluetooth***

Size	Document Number	Rev
A4	Storm	-1

Date: Monday, June 25, 2012 Sheet 63 of 102

Finger printer

JE40 delete FP function



STORM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title ***RESERVED***

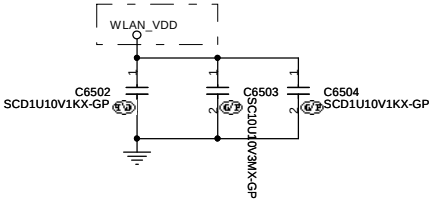
Size	Document Number	Rev
A4	**Storm**	**-1**

Date: Monday, June 25, 2012 Sheet 64 of 102

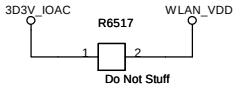
SSID = Wireless

Mini Card Connector(802.11a/b/g/n)

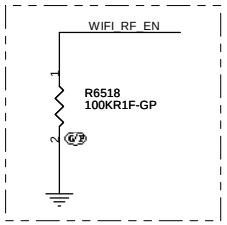
SB_20120113_IOAC



SB_20120113_IOAC

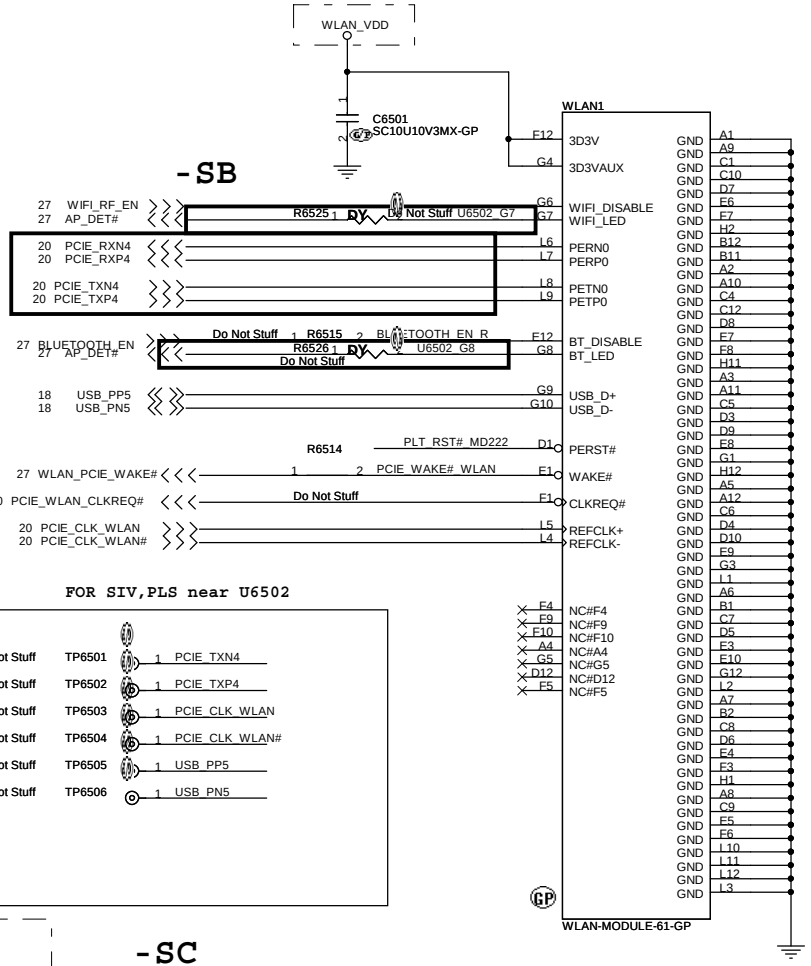


RF_SC



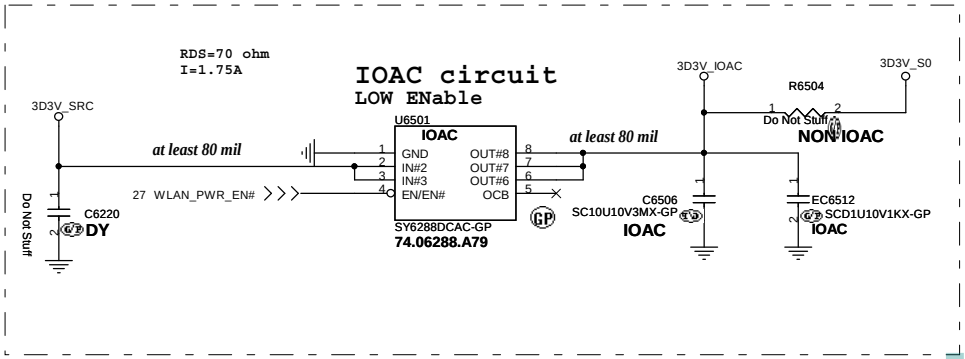
-SB

SB_20120113_IOAC

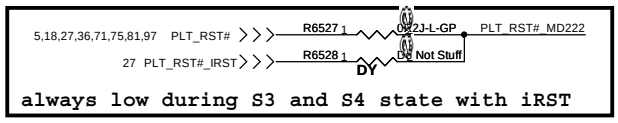


FOR SIV,PLS near U6502

SB_20120129_IOAC



-SC



STORM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINICARD(WLAN)/ITP CONN

Size: A3 | Document Number: Storm | Rev: -1

Date: Monday, June 25, 2012 | Sheet 65 of 102

STORM

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***WWAN Connector(mSATA)***

Size	Document Number	Rev
A4	**Storm**	**-1**

Date: Monday, June 25, 2012 Sheet 66 of 102

Blanking

STORM

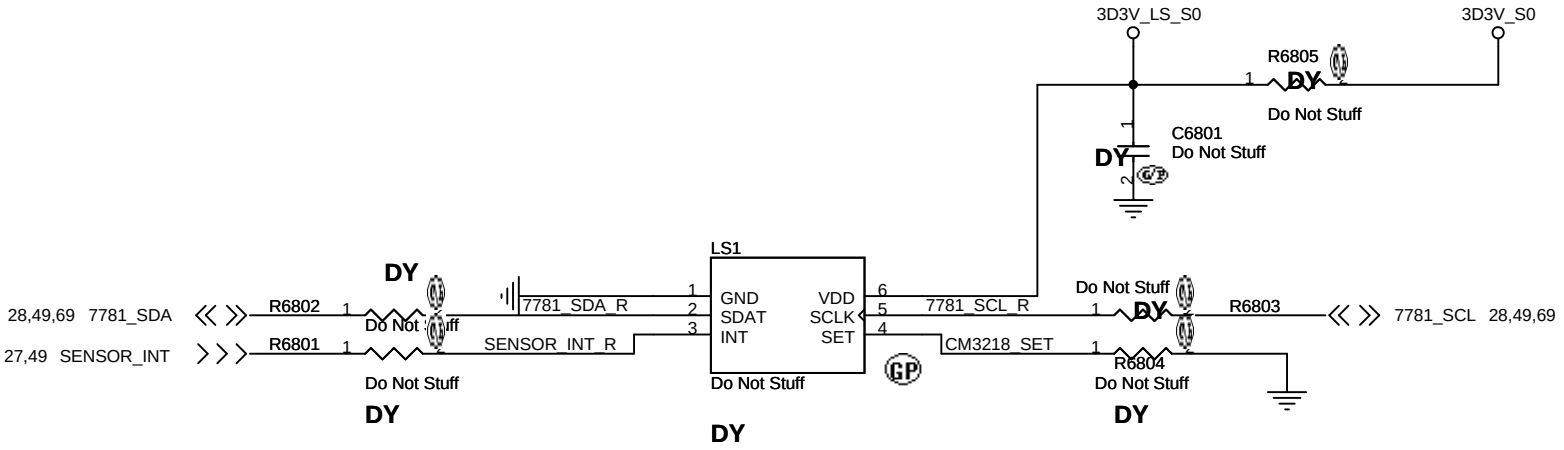
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***M-SATA***

Size	Document Number	Rev
A4	**Storm**	**-1**

Date: Monday, June 25, 2012 Sheet 67 of 102

SSID = User.Interface



STORM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Light SENSOR

Size	Document Number	Rev
A4	Storm	-1

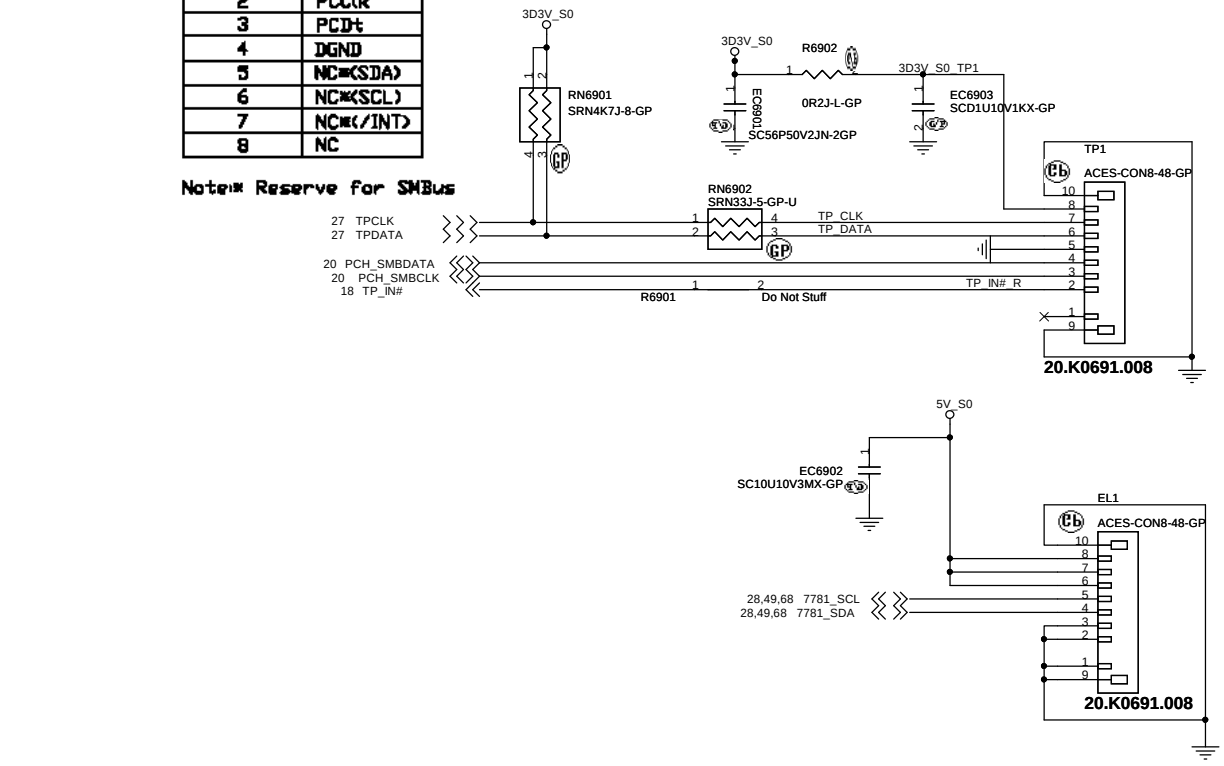
Date: Monday, June 25, 2012 Sheet 68 of 102

SSID = KBC

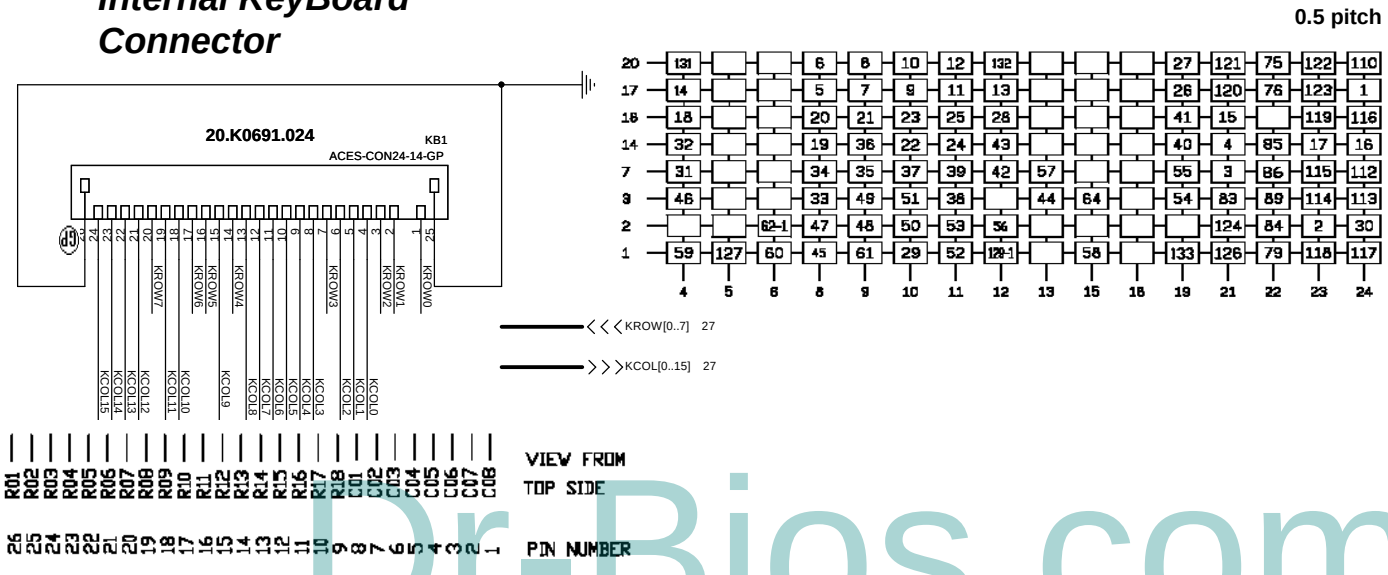
Pin number	Pin Define
1	VDD(3.3V)
2	PCClk
3	PCDt
4	DGND
5	NC#(SDA)
6	NC#(SCL)
7	NC#(/INT)
8	NC

Note# Reserve for SMBus

TOUCH PAD



Internal KeyBoard Connector



0.5 pitch

VIEW FROM TOP SIDE

PIN NUMBER

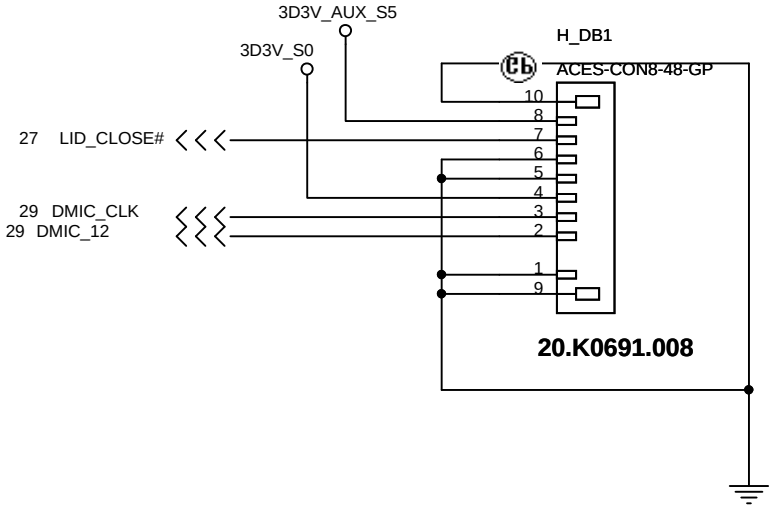
STORM

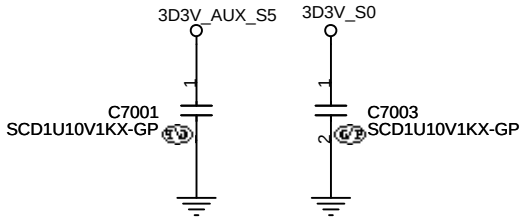
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Key Board/Touch Pad

Size	Document Number	Rev
A3	Storm	-1

Date: Wednesday, June 27, 2012 Sheet 69 of 102





STORM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Hall Sensor/DMIC CONN***

Size	Document Number	Rev
A4	**Storm**	**-1**

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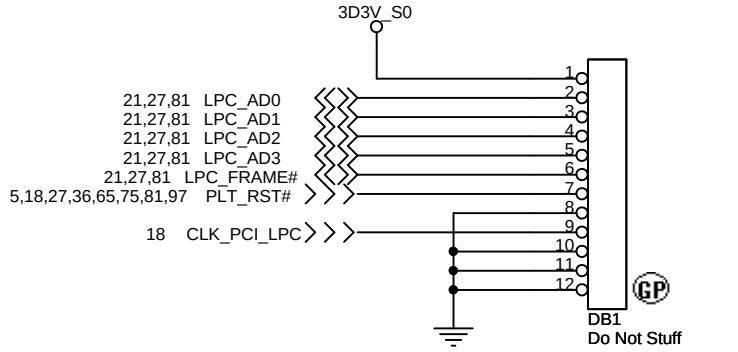

Do Not Stuff

DY

STORM

緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Dubug connector***

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A4	**Storm**	**-1**

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STORM

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Title: ***Reserved***

Size	Document Number	Rev
A4	**Storm**	**-1**

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STORM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: ***Reserved***

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Micro SD Card Reader

STORM

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Micro SD Card Reader***

Size	Document Number	Rev
A4	**Storm**	**-1**

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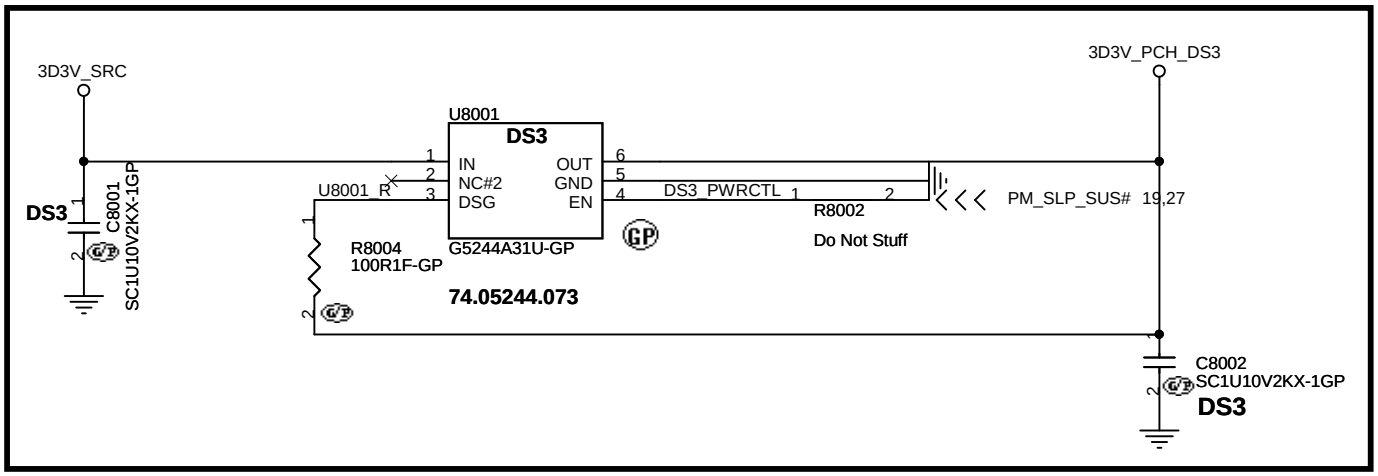

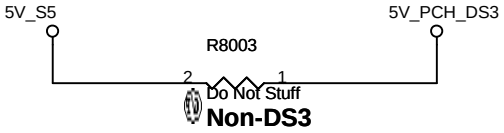

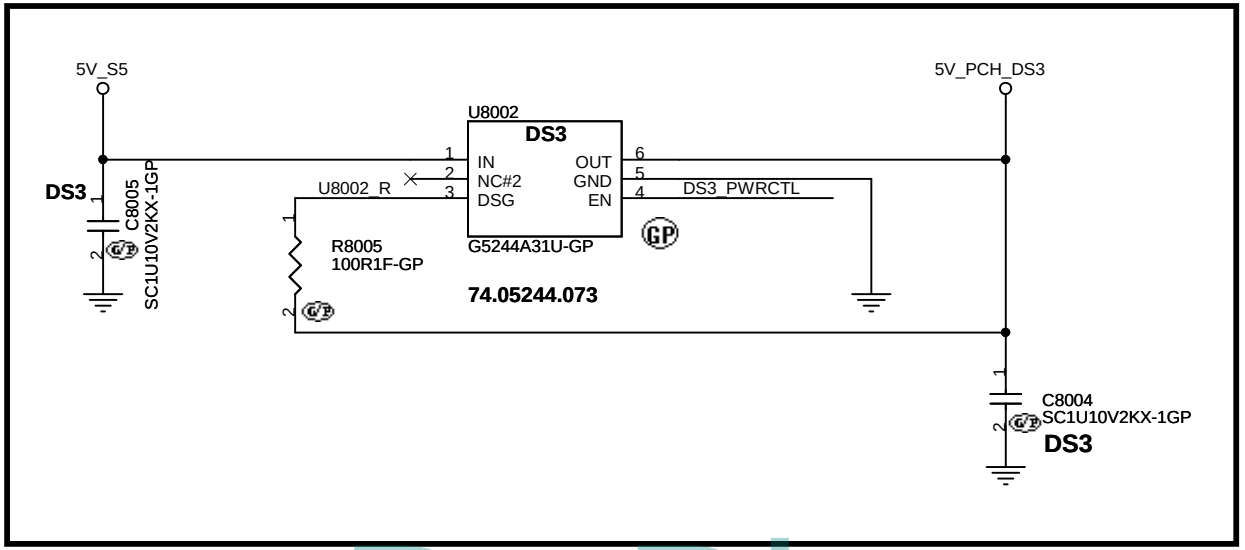

STORM

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Deep Standby***

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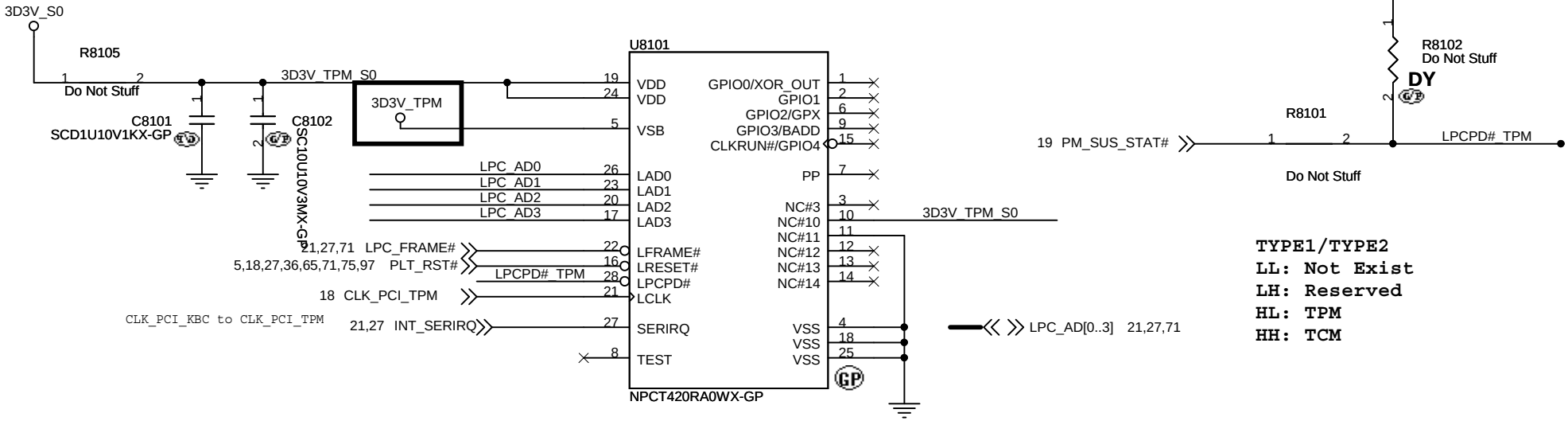
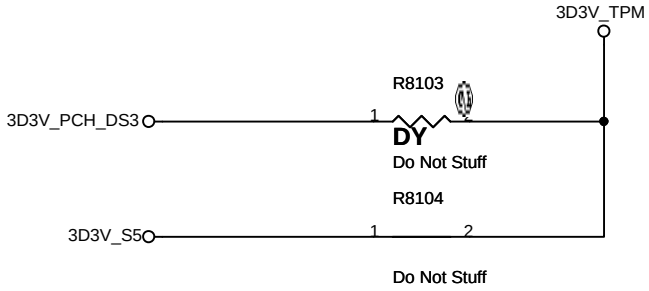


TYPE1/TYPE2
LL: Not Exist
LH: Reserved
HL: TPM
HH: TCM



STORM

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

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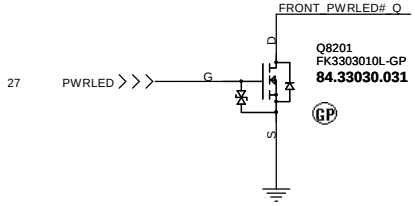
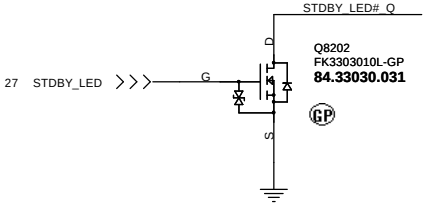
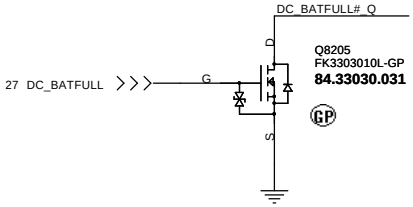
Power button LED



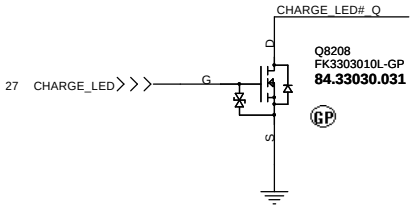
Power STDBY_LED

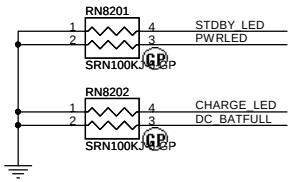


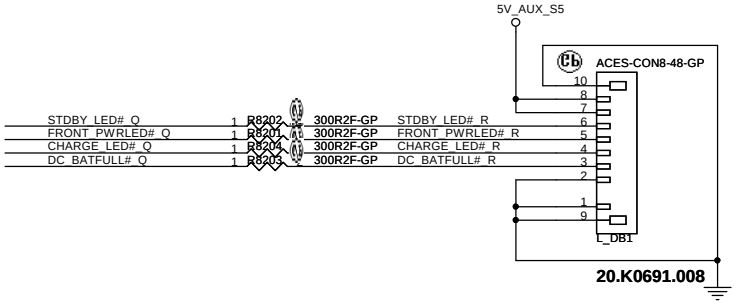
Battery LED2(DC_BATFULL)

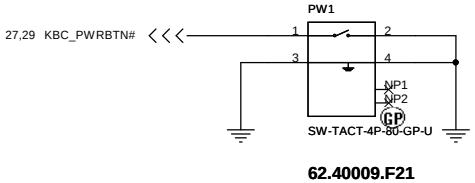


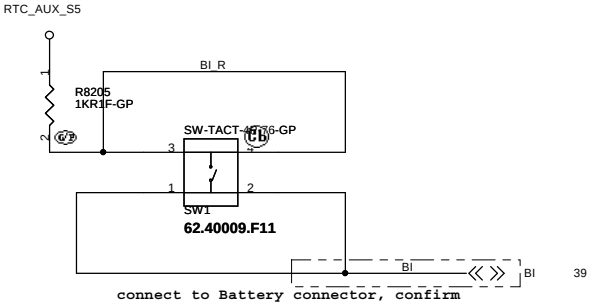
Battery LED1(CHARGE)











STORM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***LED Bard/Power Button***
Size A3	Document Number **Storm** Rev **-1**
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SSID = SDIO

STORM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***TOUCH PANEL***

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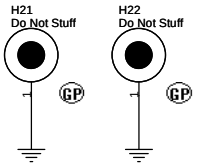
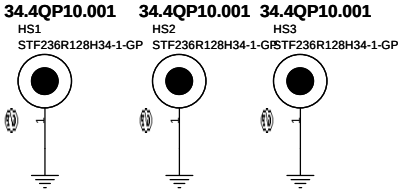
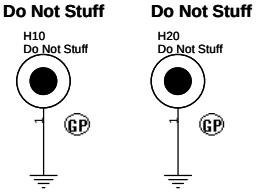
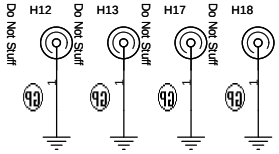
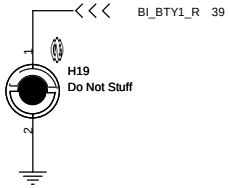
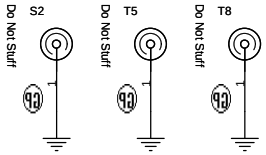




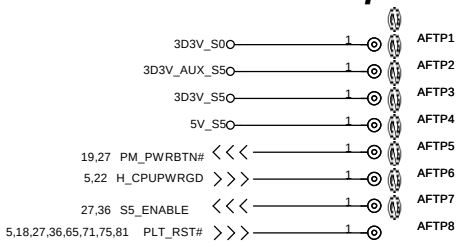








Check test point



Test Point放在Dimm Door打開可量測處

STORM

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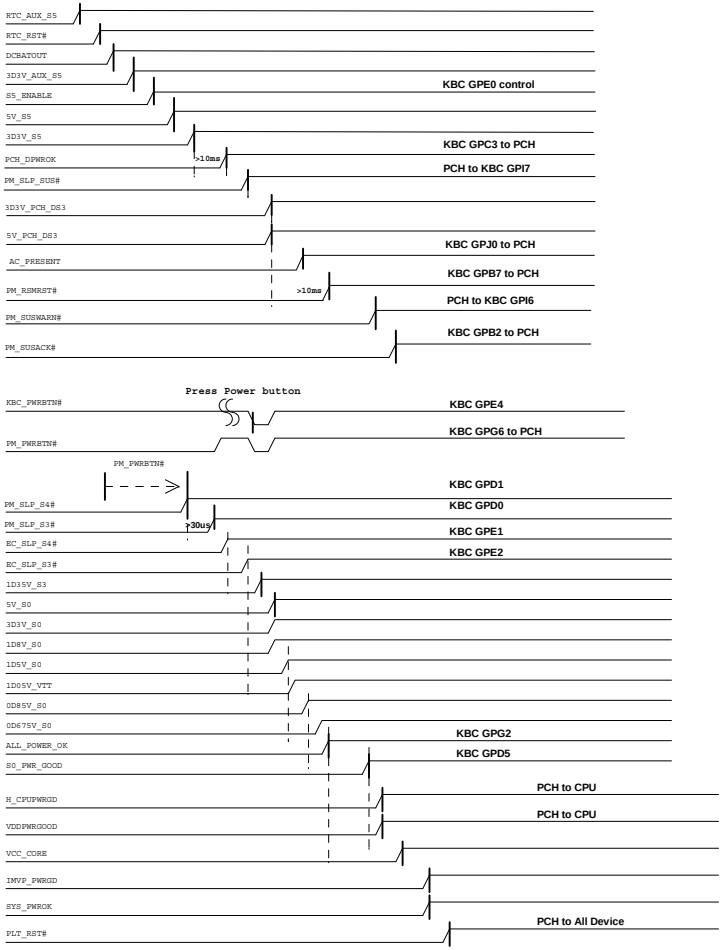
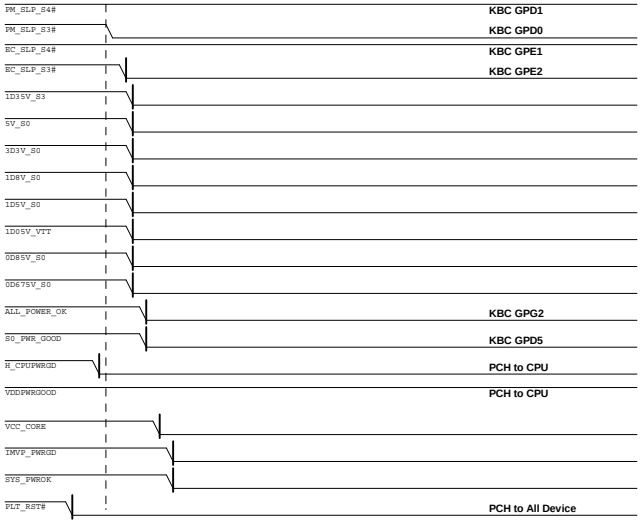
Title: *UNUSED PARTS/EMI Capacitors*	
Size: A3	Document Number: Storm — Rev: -1
Date: Tuesday, June 26, 2012	Sheet 97 of 102

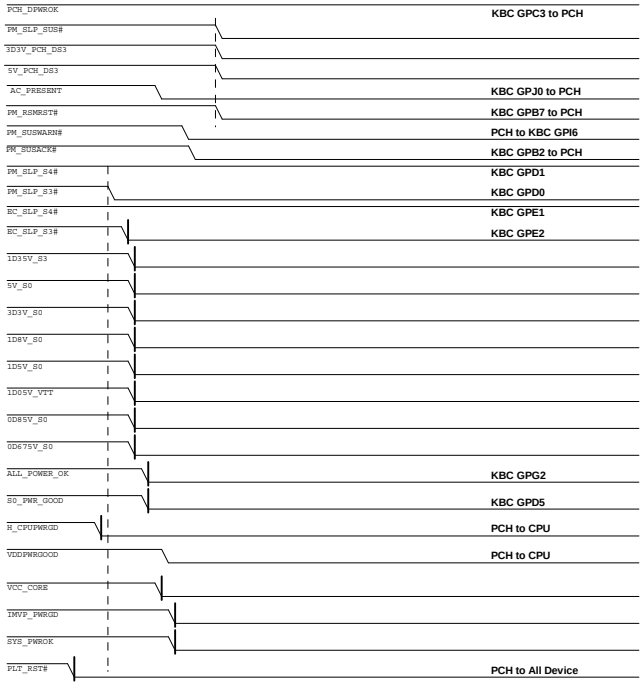
Intel Power Up Sequence



Intel S3 Sequence



Intel Deep S3 Sequence



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Title: Power Sequence

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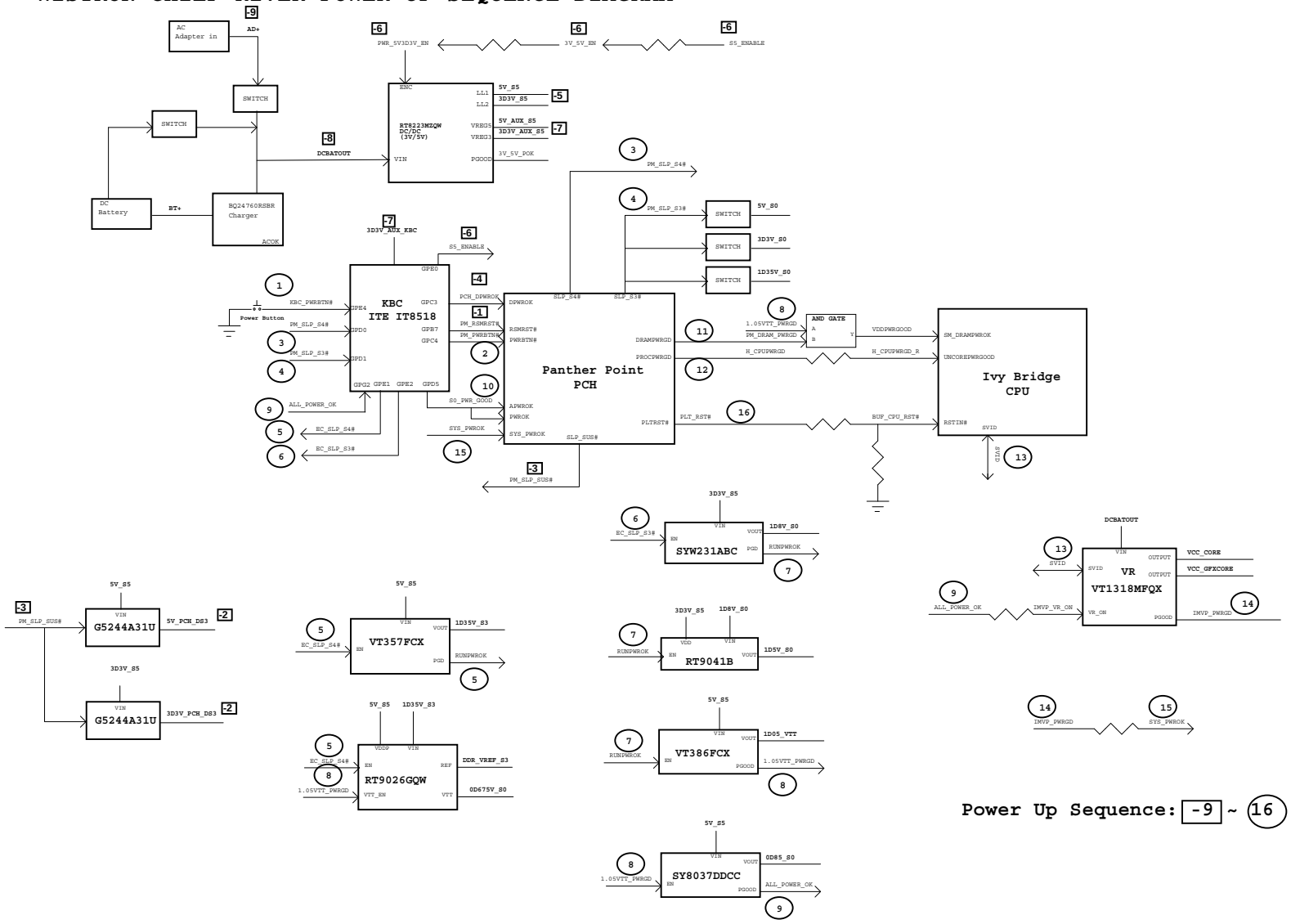
WISTRON CHIEF RIVER POWER UP SEQUENCE DIAGRAM



Power Up Sequence: -9 ~ 16

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Title: Power Sequence Diagram

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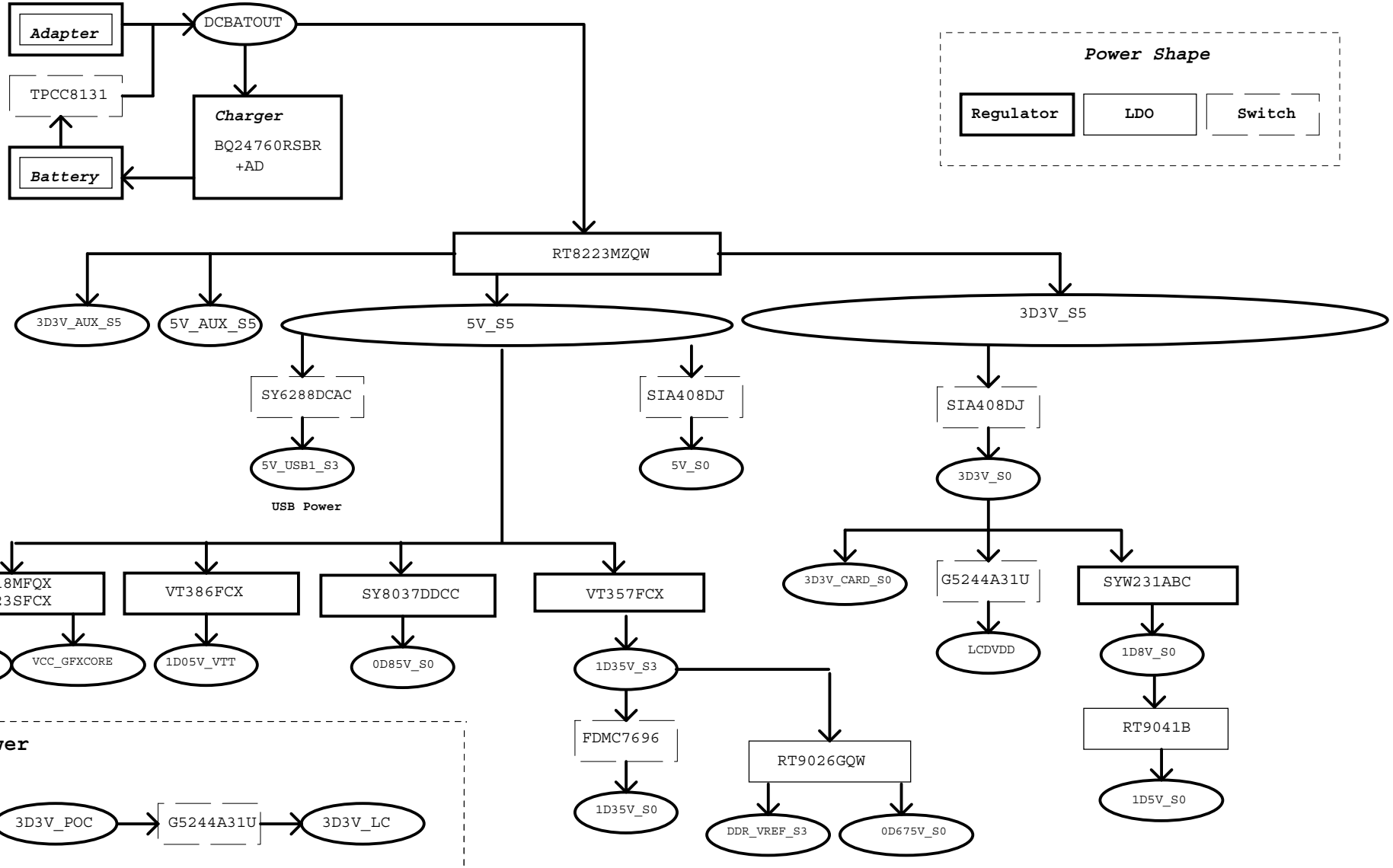
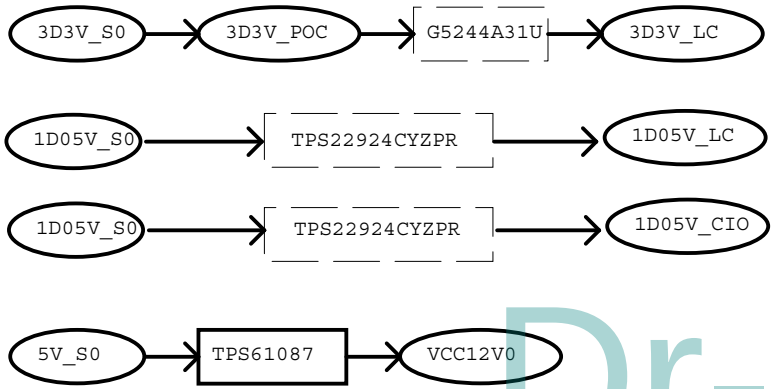


Thunderbolt Power



STORM

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

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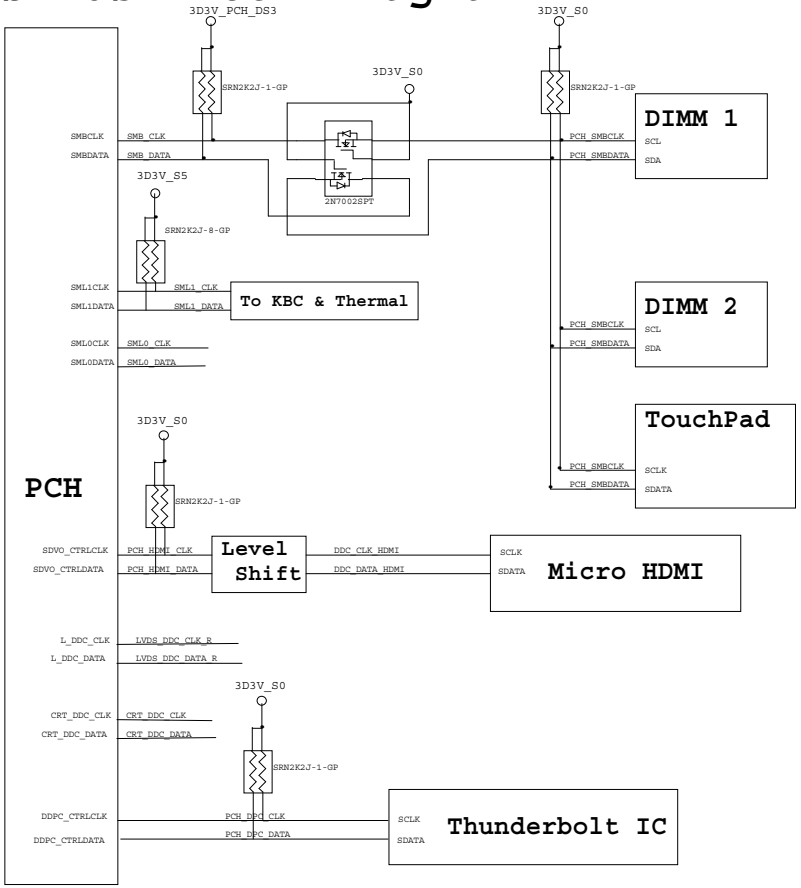
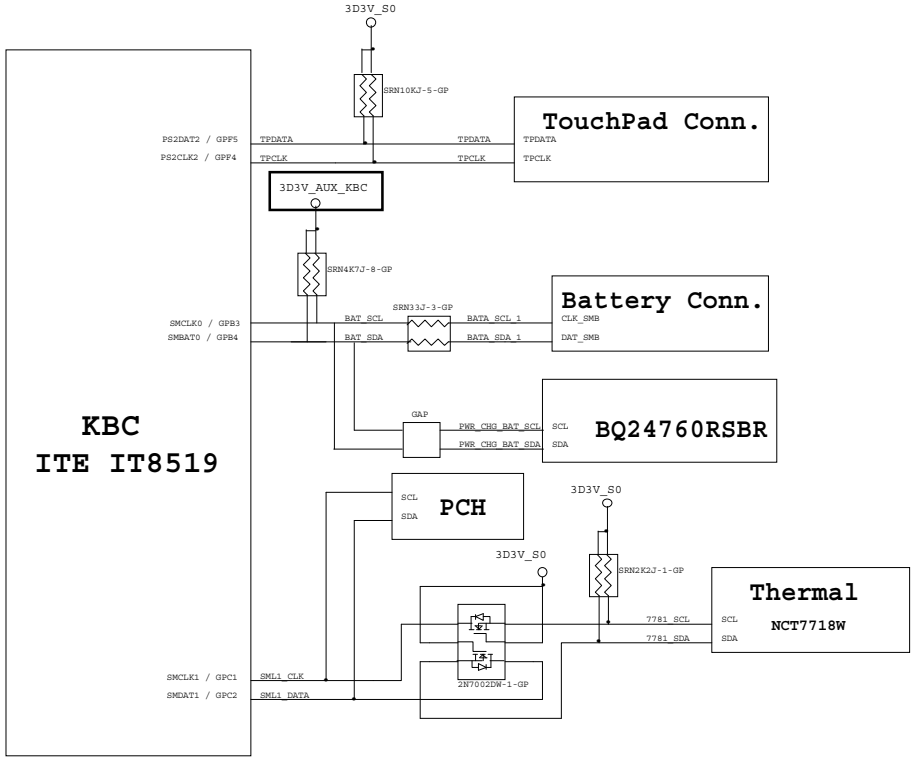
PCH SMBus Block Diagram



KBC SMBus Block Diagram



STORM

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Taipei Hsien 221, Taiwan, R.O.C.

Title: SMBUS Block Diagram

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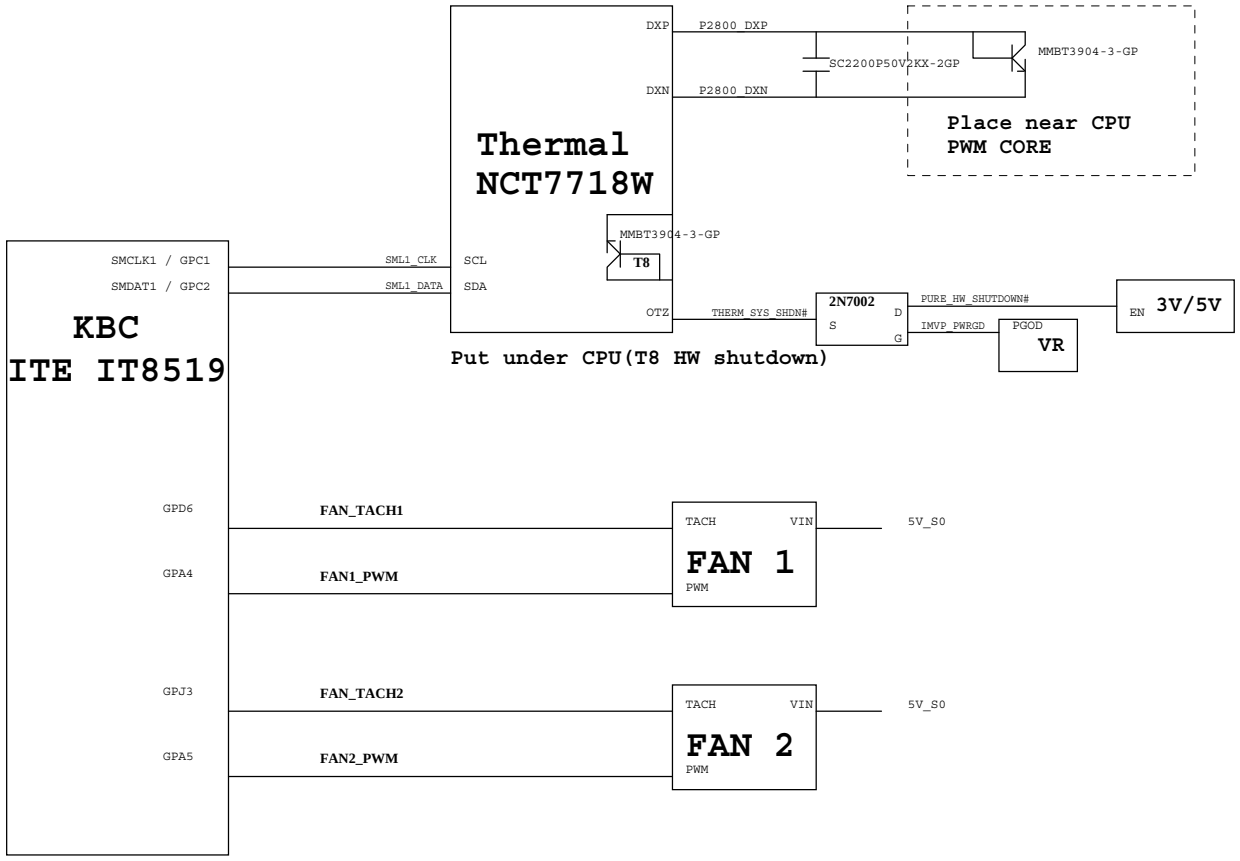
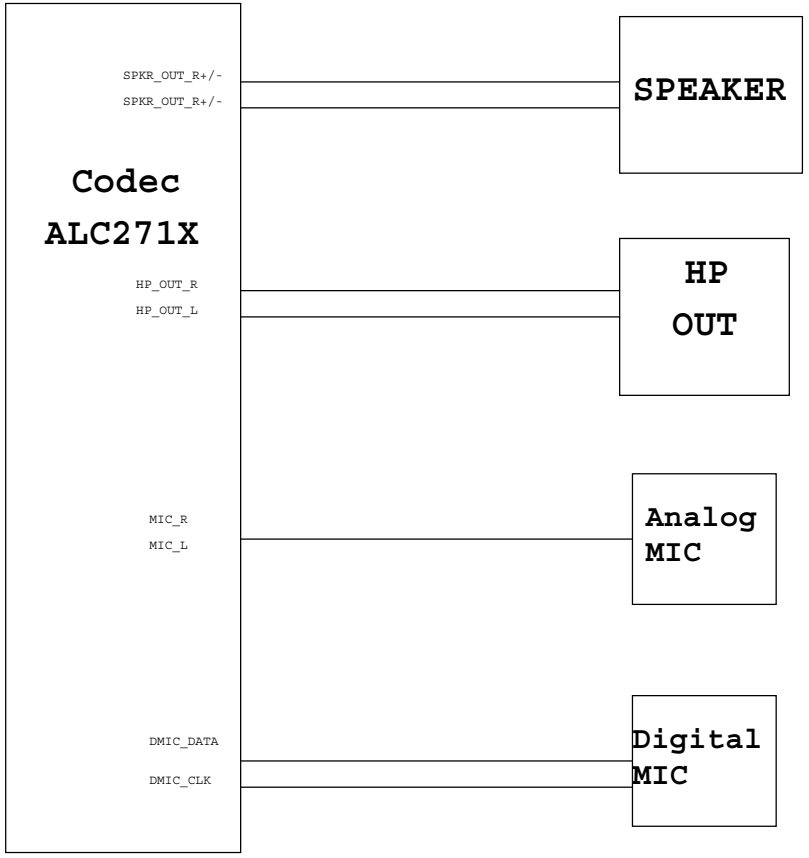
Thermal Block Diagram



Audio Block Diagram



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Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Audio Block Diagram

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