

Weebill HW UMA-MUXLESS Schematics Document Haswell ULT Processor

DY :None Installed

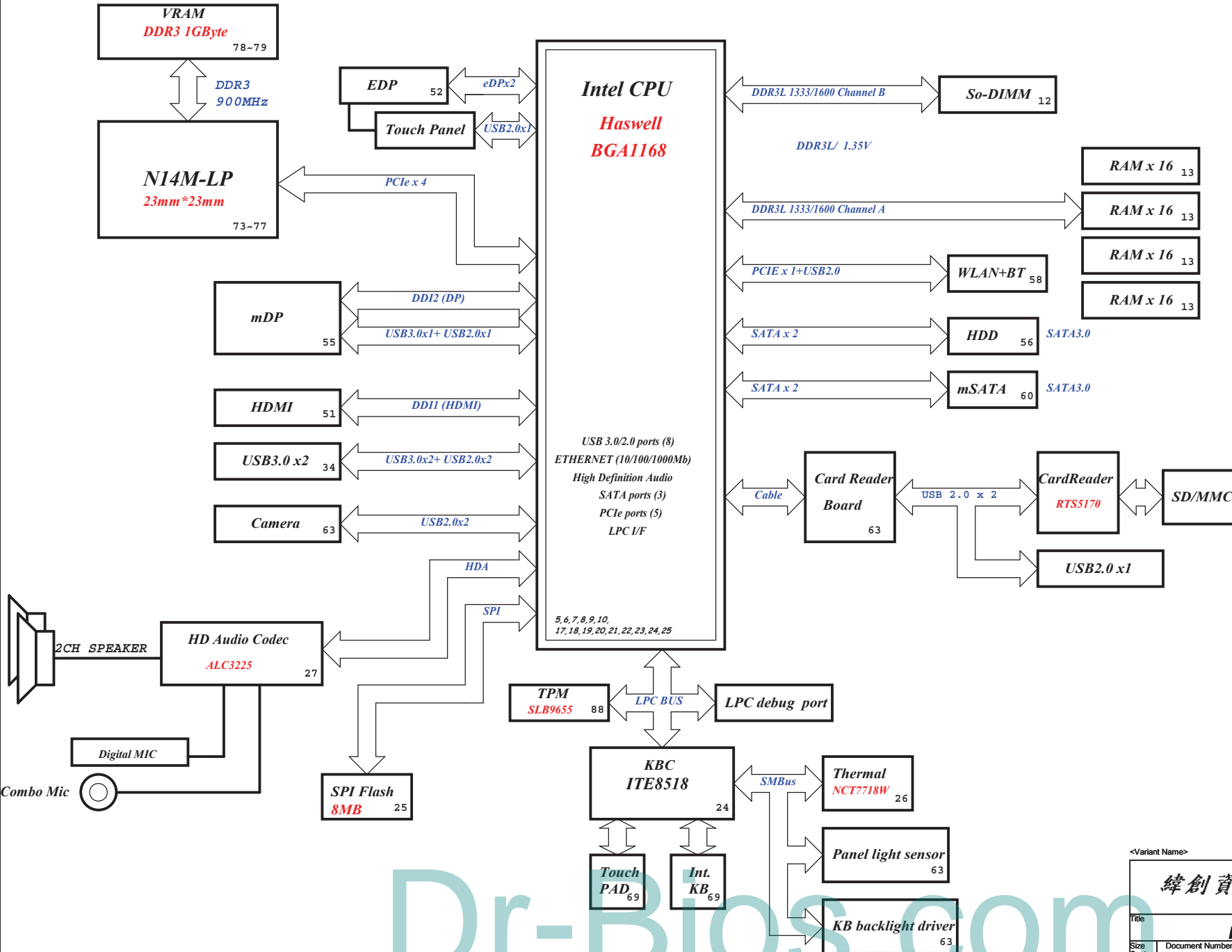
*ANNIE: ONLY FOR ANNIE solution.
65W: for 65W adaptor installed.
90W: for 90W adaptor installed.*

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<Variant Name>		
緯創資通 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title Cover Page		
Size A3	Document Number WEEBILL_HW	Rev SA
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WEEBILL_HW ULT Board Block Diagram

Project code : 91.4L501.A01
 PCB P/N :
 Revision : 12265-SB



CHARGER	
BQ24760	44
INPUTS	OUTPUTS
DCBATOUT	BT+
SYSTEM DC/DC	
SYN258B/C	45
INPUTS	OUTPUTS
DCBATOUT	5V_s5
	3D3V_s5
CPU DC/DC	
TPS51622	46-47
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
SYSTEM DC/DC	
SYS8208A	48
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT
SYSTEM DC/DC	
TPS51367+TPS51206	49
INPUTS	OUTPUTS
DCBATOUT	1D35V_S3
1D35V_S3	0D675V_S0
	DDR_VREF_S3
SYSTEM DC/DC	
SYW232	51
INPUTS	OUTPUTS
3D3V_s5	1D5V_S0
PCB LAYER	
L1: Top	L6: Signal
L2: GND	L7: GND
L3: Signal	L8: Signal
L4: GND	L9: GND
L5: Signal	L10: Bottom

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Title: Block Diagram	
Size: Custom	Document Number: WEEBILL_HW
Date: Wednesday, September 18, 2013	Rev: SA
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D

C

B

A

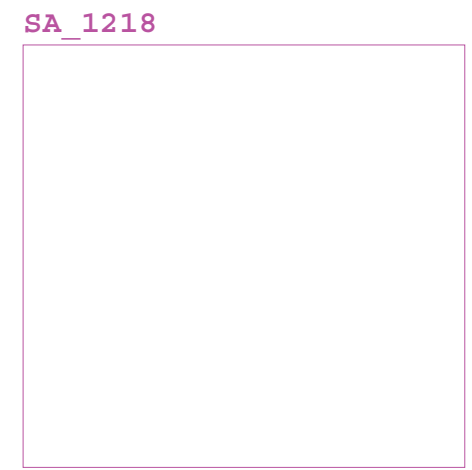
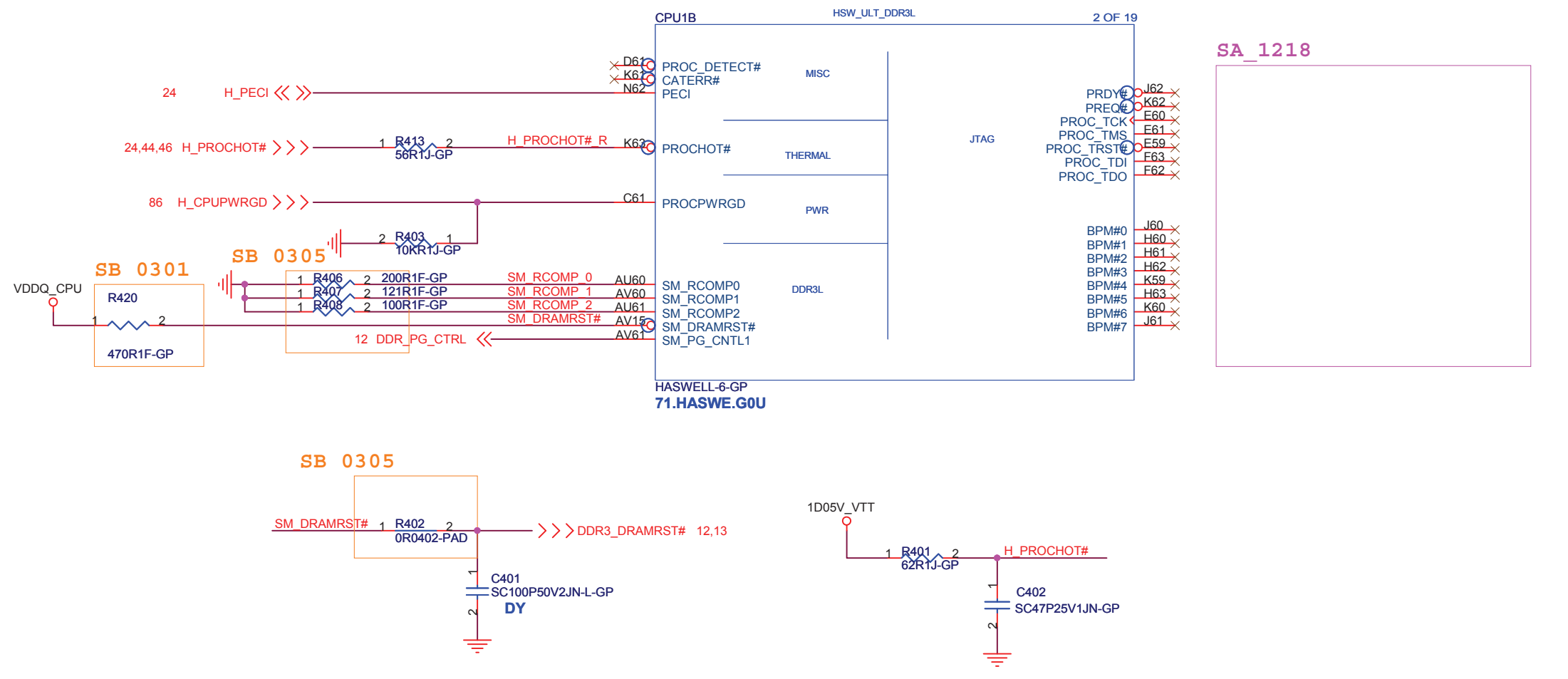
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CPU (Reserved)	SA
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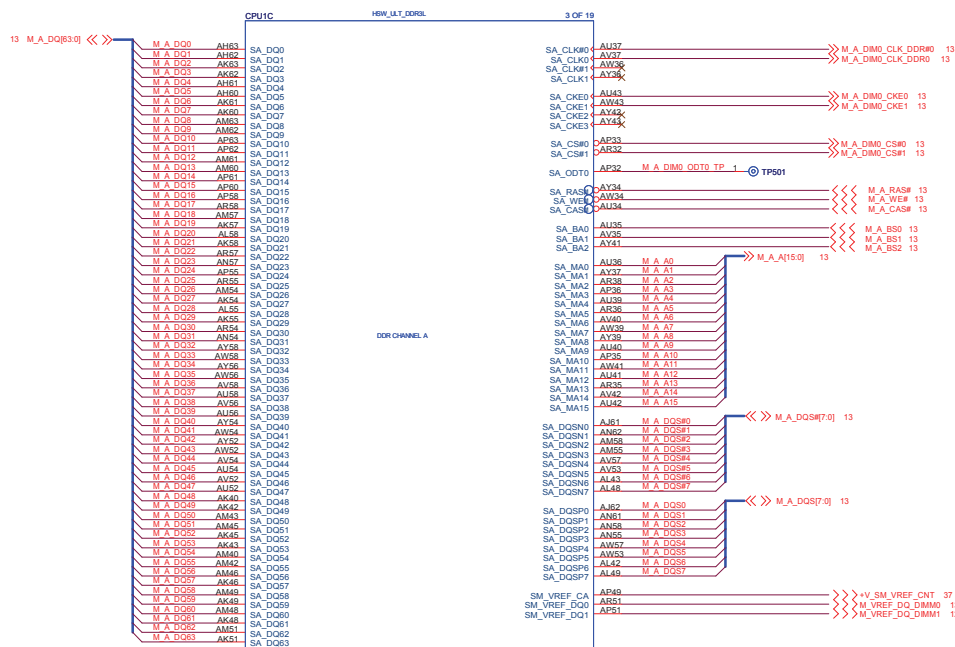


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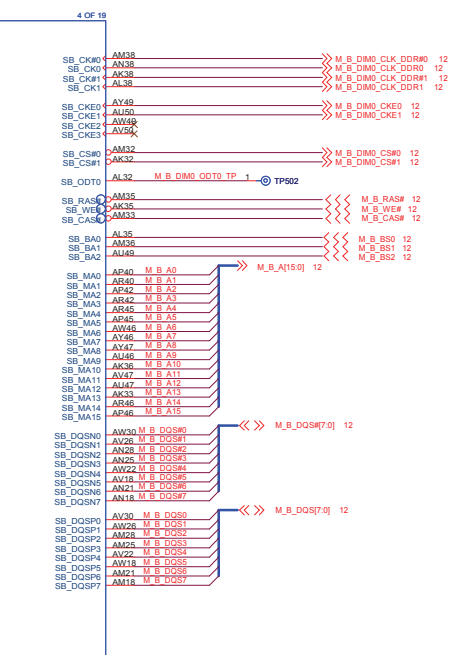
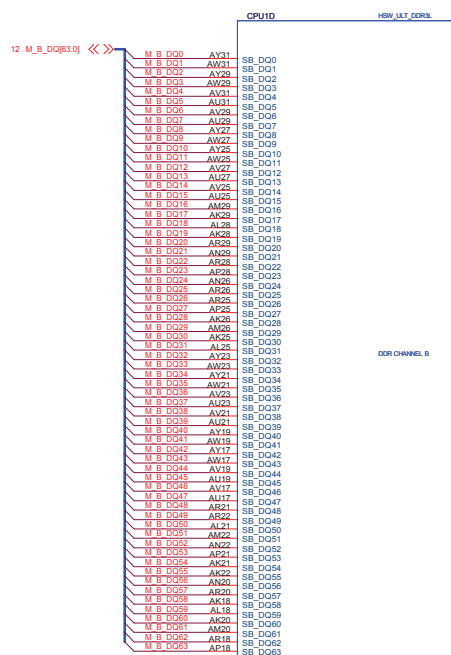
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Title	CPU (THERMAL/CLOCK/PM)		Rev
Size	Document Number	SA	
A4	WEEBILL HW		
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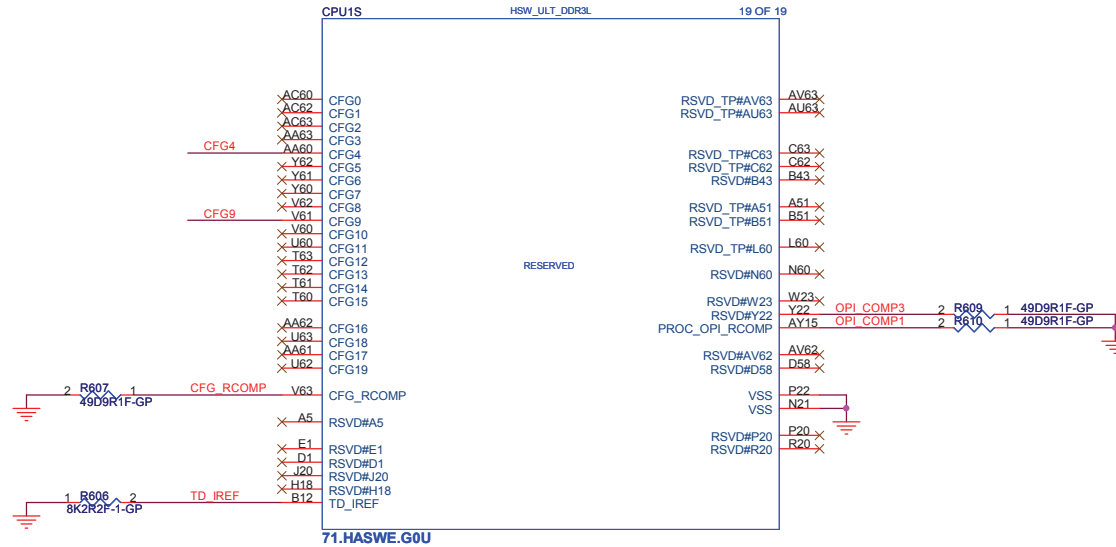
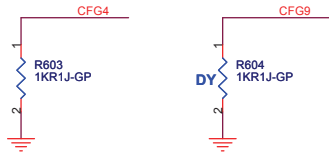
HASWELL-6GP
71.HASWE.G0U



HASWELL-6GP



eDP Enable	
CFG4	1:Disable
	0:Enable



7.4 Reserved or Unused Signals

The following are the general types of reserved (RSVD) signals and connection guidelines:

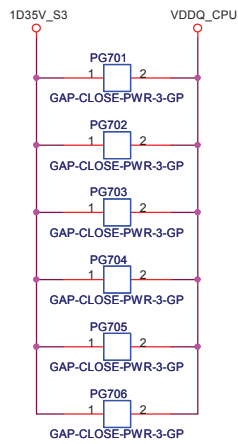
- RSVD – these signals should not be connected
- RSVD_TP – these signals should be routed to a test point
- RSVD_NCTF – these signals are non-critical to function and may be left unconnected

Signal Name	Description	Direction/ Buffer Type
CFG[19:0]	<p>Configuration Signals:</p> <p>The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired.</p> <ul style="list-style-type: none"> • CFG[3:0]: Reserved configuration lane. A test point may be placed on the board for these lanes. • PCI Express* Static x16 Lane Numbering Reversal. – – • CFG[4]: eDP enable <ul style="list-style-type: none"> – 1 = Disabled – 0 = Enabled • [19:5]: Reserved configuration lanes. A test point may be placed on the board for these lands. 	I/O GTL
CFG_RCOMP	Configuration resistance compensation.	-
FC_x	FC signals are signals that are available for compatibility with other processors. A test point may be placed on the board for these lands. Refer to the appropriate platform design guide for implementation details.	

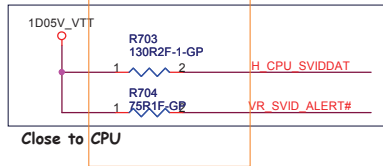
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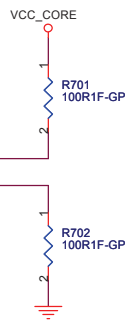
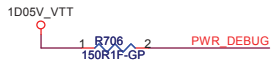
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Title		
CPU (CFG)		
Size A3	Document Number	Rev SA
WEEBILL HW		
Date: Wednesday, September 18, 2013	Sheet 6	of 102



SB 0305

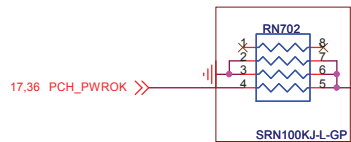


Close to CPU

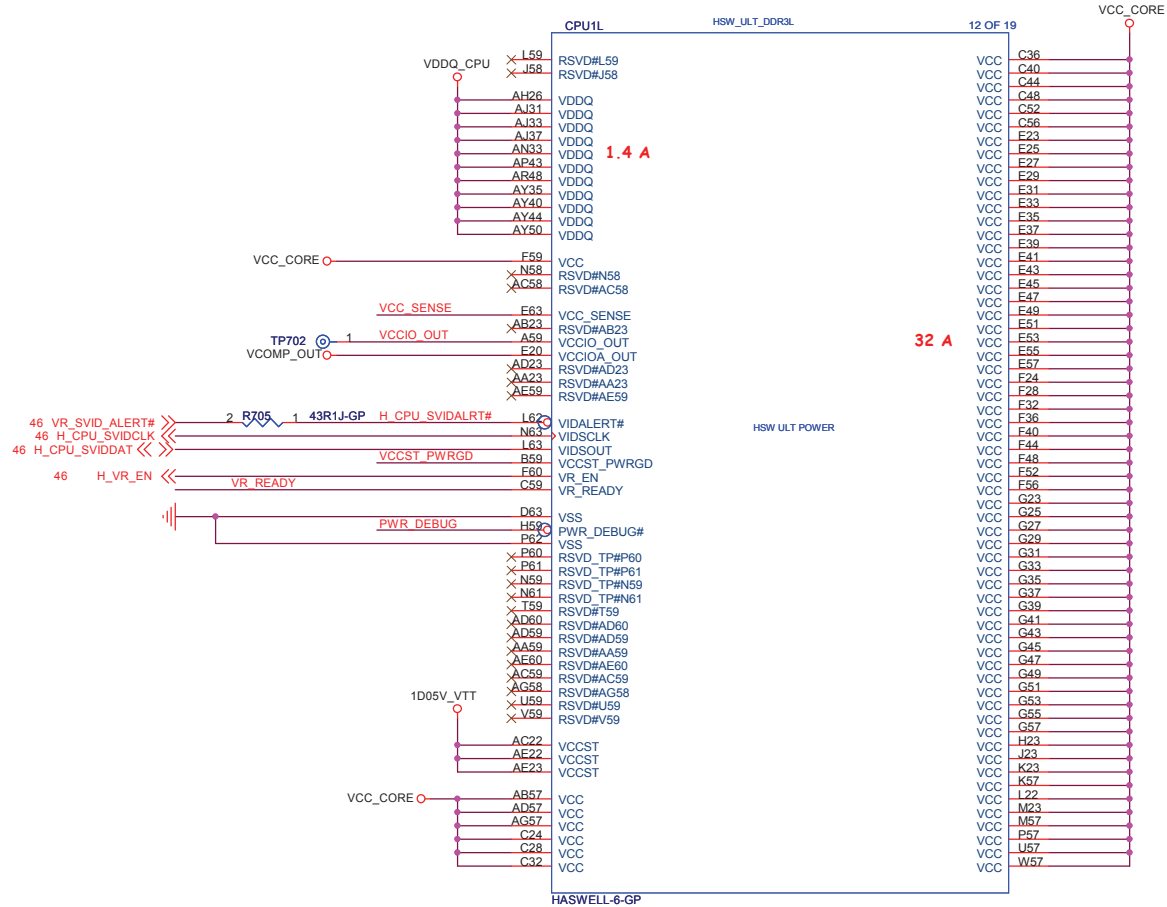
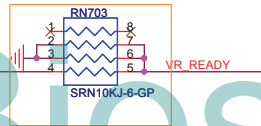


46 VCC_SENSE <<<
9,46 VSS_SENSE <<<

-1_0507



SB 0305



1.4 A

32 A

HSW ULT POWER

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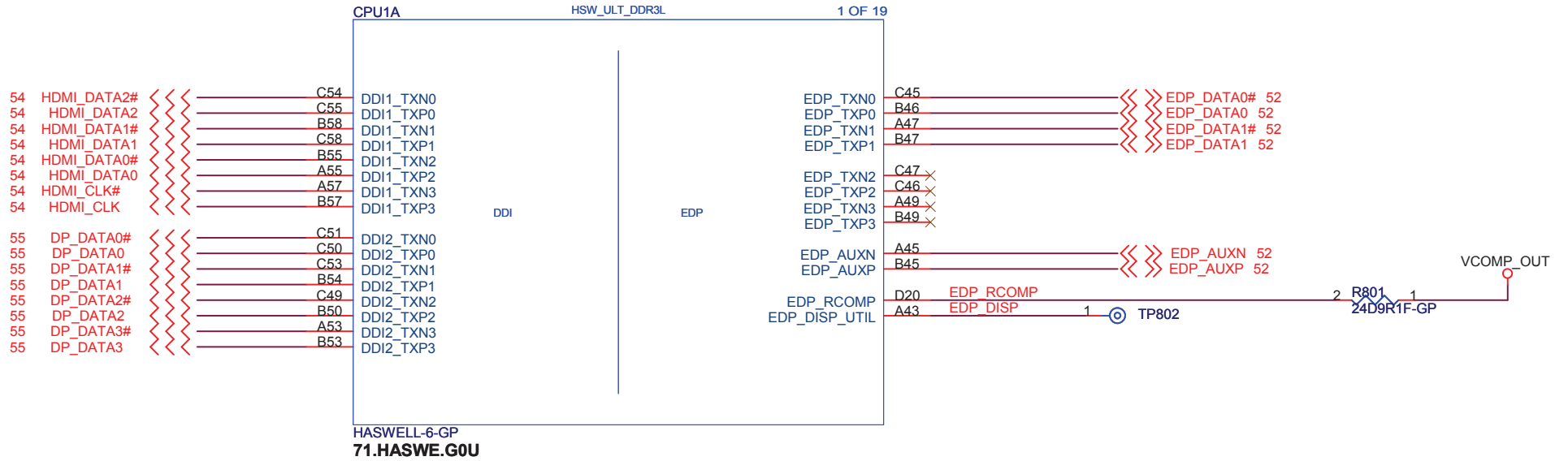
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緯創資通 Wistron Corporation
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Title: **CPU (VCC CORE)**

Size A3 Document Number: **WEEBILL_HW** Rev: **SA**

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<Variant Name>

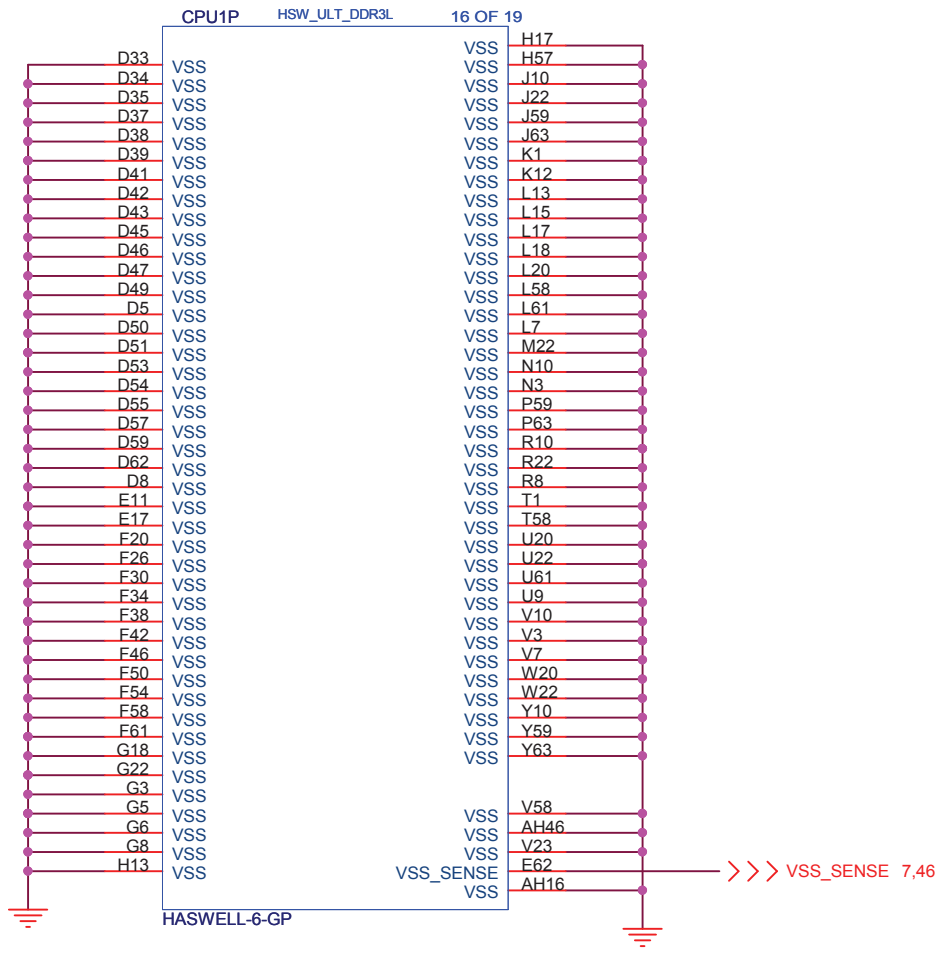
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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	

Title: **CPU (DDI/EDP)**

Size: A4	Document Number: WEEBILL_HW	Rev: SB
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Date: Wednesday, September 18, 2013 Sheet 8 of 102

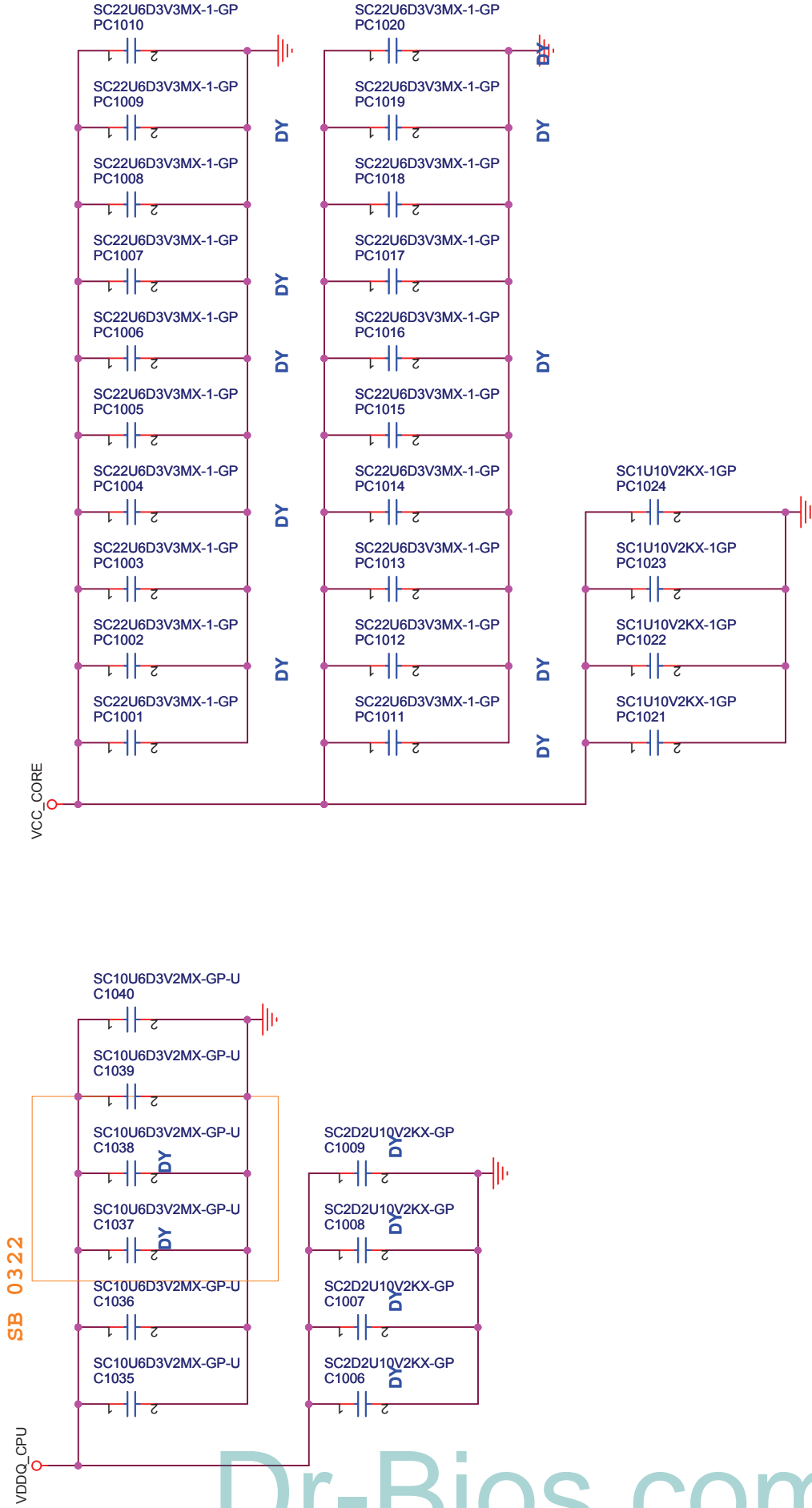
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CPU (VSS)			
Size A4	Document Number WEEBILL_HW		Rev SA
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VCC_CORE

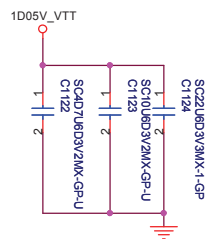
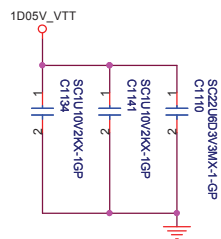
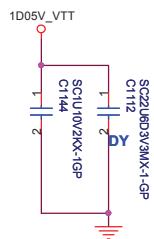
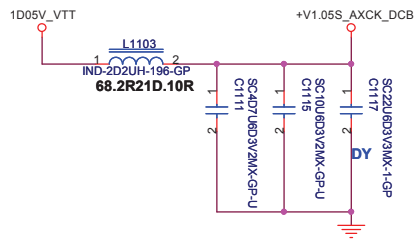
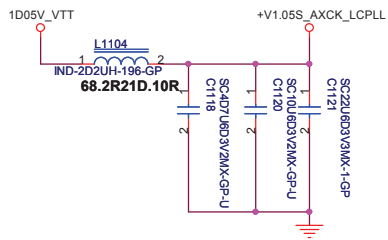
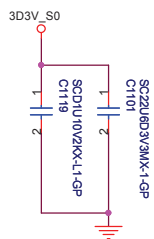
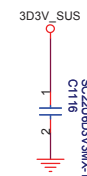
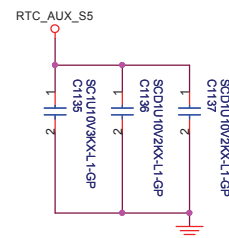
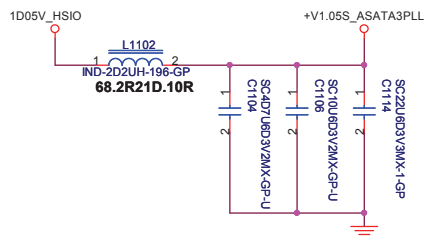
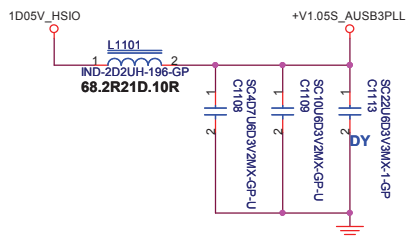
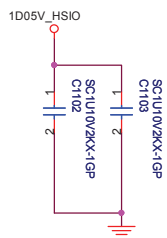
PT1001
ST330U2D5VBM-1-GP
80.3371V.A2L

NEC/TOKIN. B2
ESR: 9 mOhm
Cap : 330 uF

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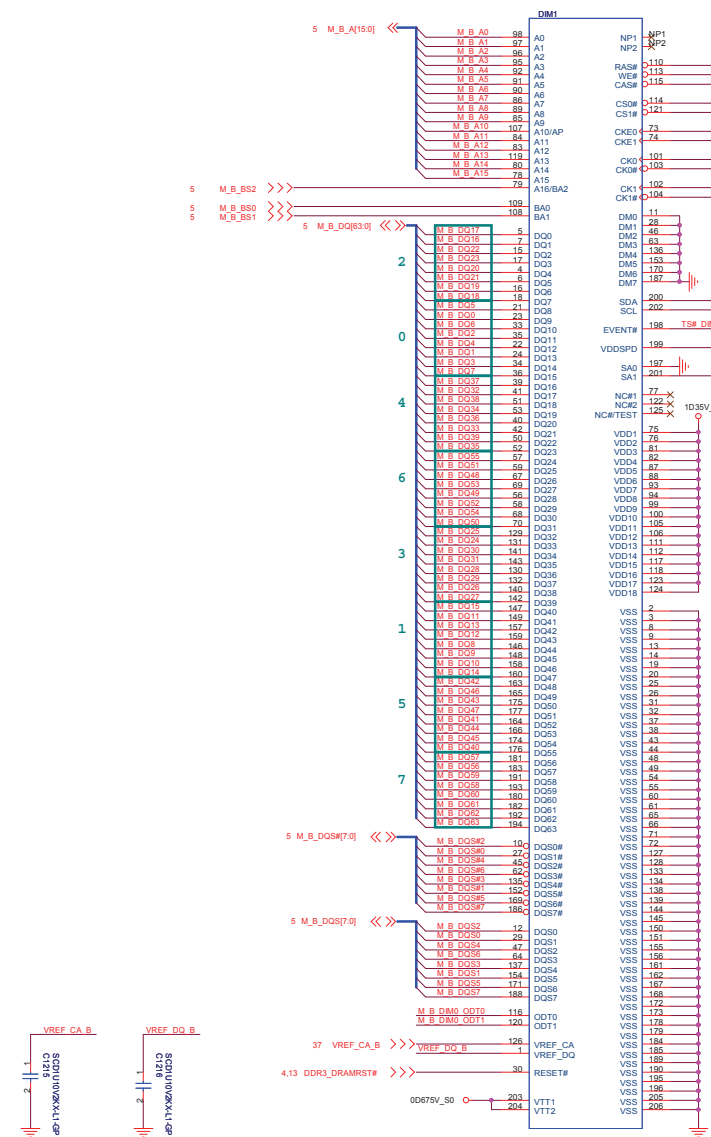
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Title		CPU (Power CAP1)	
Size	Document Number	Rev	SA
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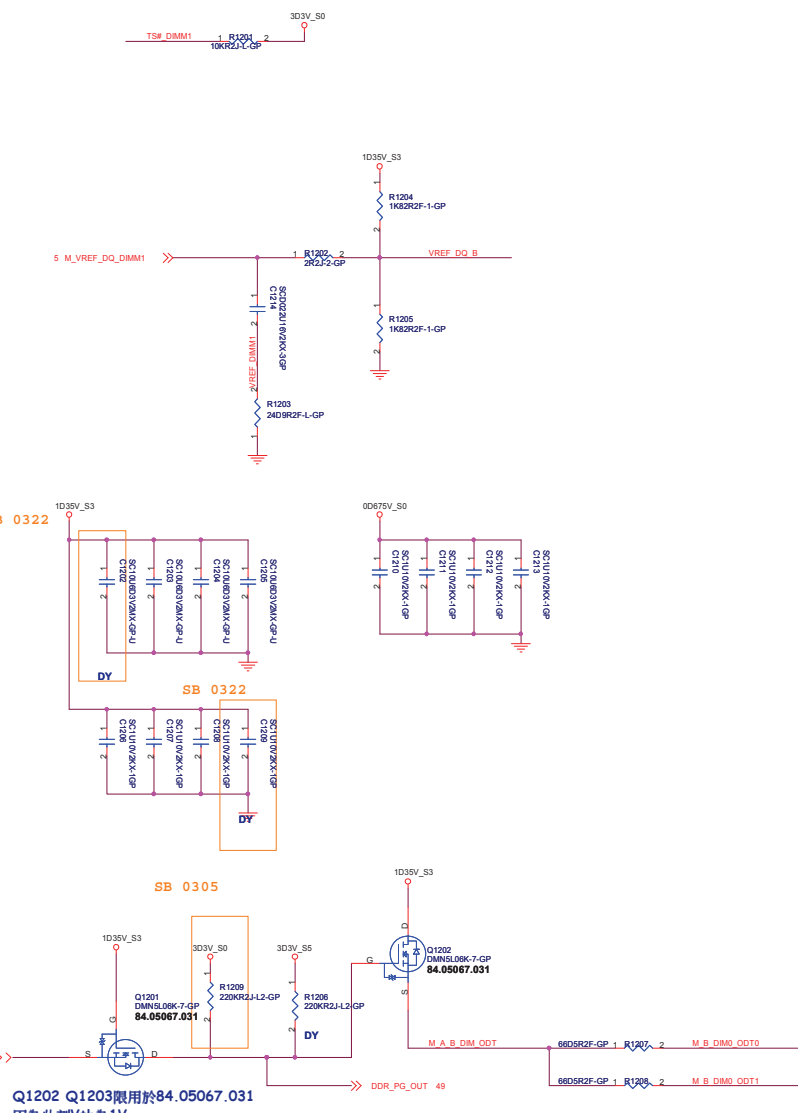


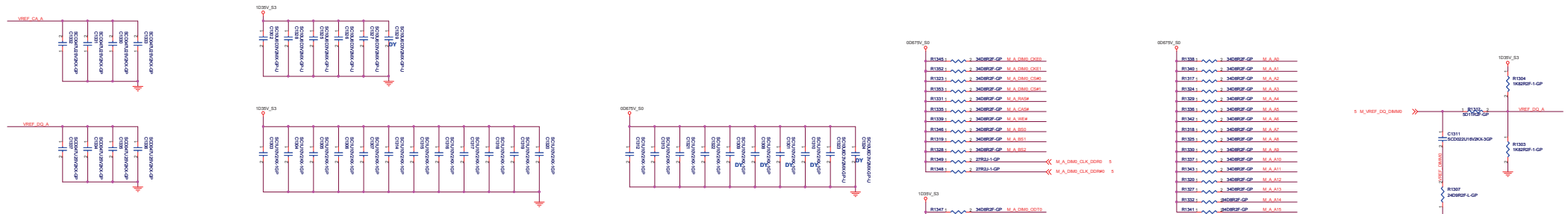
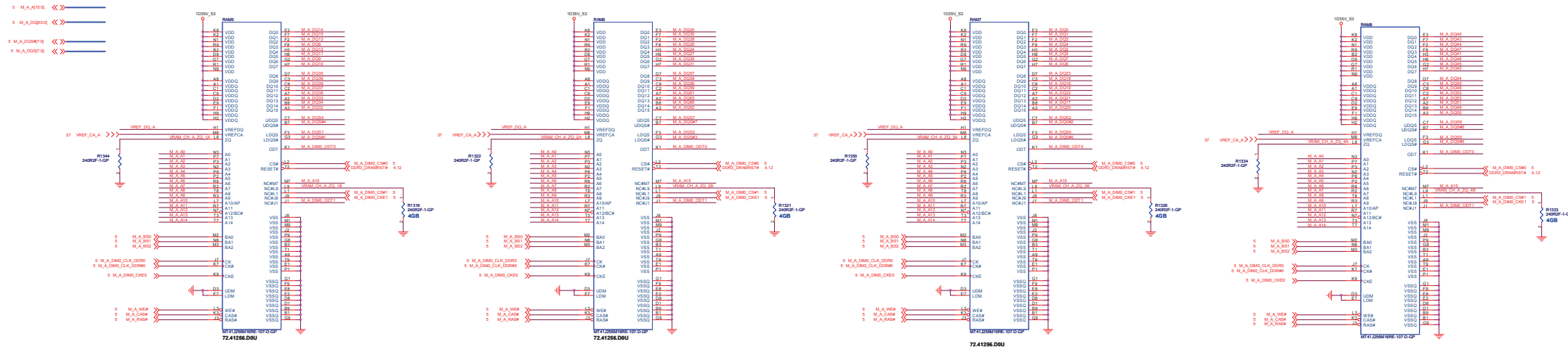
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<Variant Name>		
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Title		
CPU (Power CAP2)		
Size	Document Number	Rev
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DDRS-204P-123-GP
62.10017.Z81
 Z81 = **62.10024.M51**
3RD = 62.10024.G11





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DDR3-SDRAM2
WEEBILL HW
 SA

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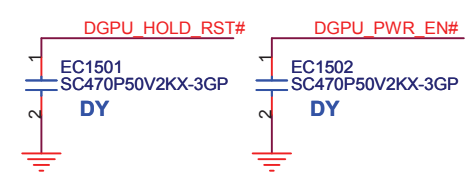
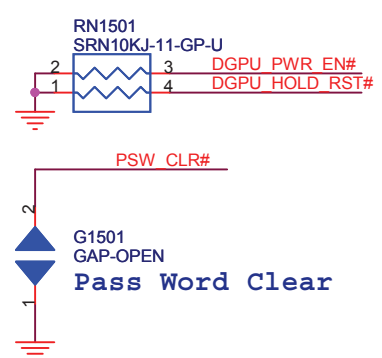
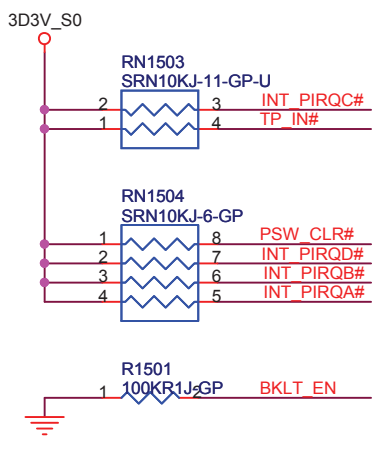
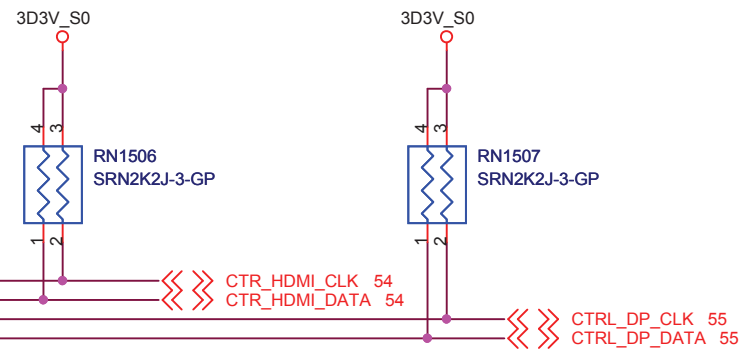
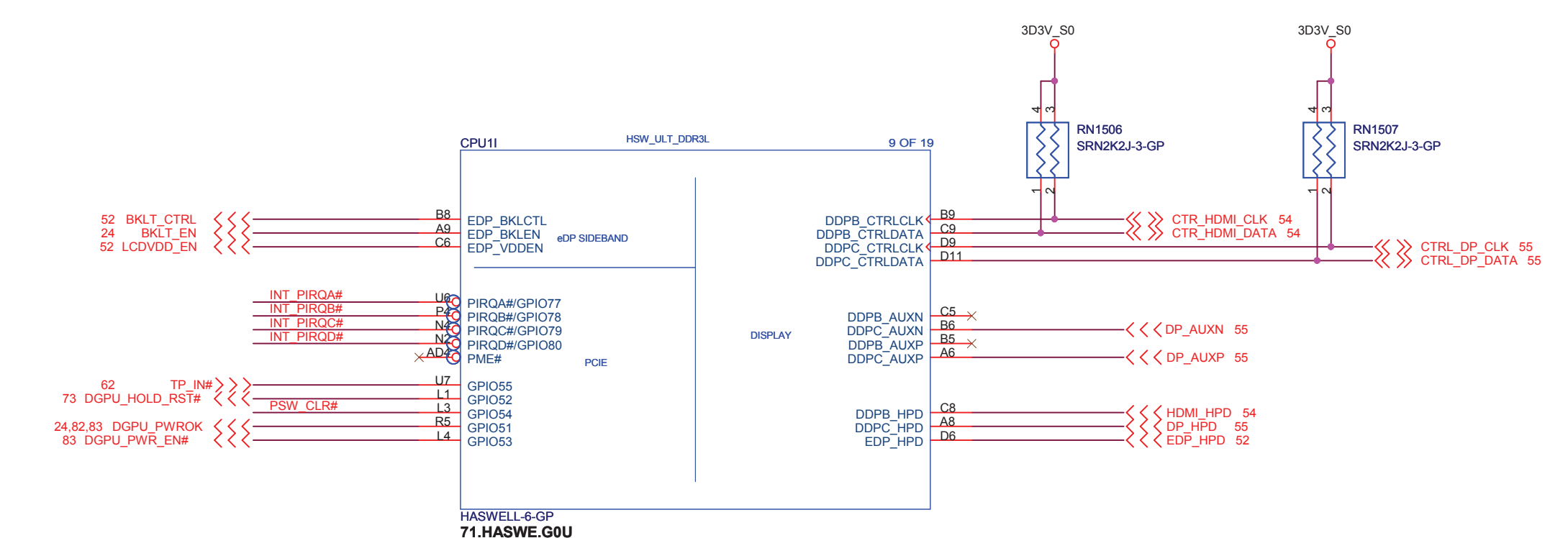
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Title
(Reserved) SODIMM SODIMM4

Size A4 Document Number **WEEBILL_HW** Rev **SA**

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Title		CPU(EDP SIDE BAND/GPIO/DDI)	
Size	Document Number	Rev	SA
A4	WEEBILL_HW		
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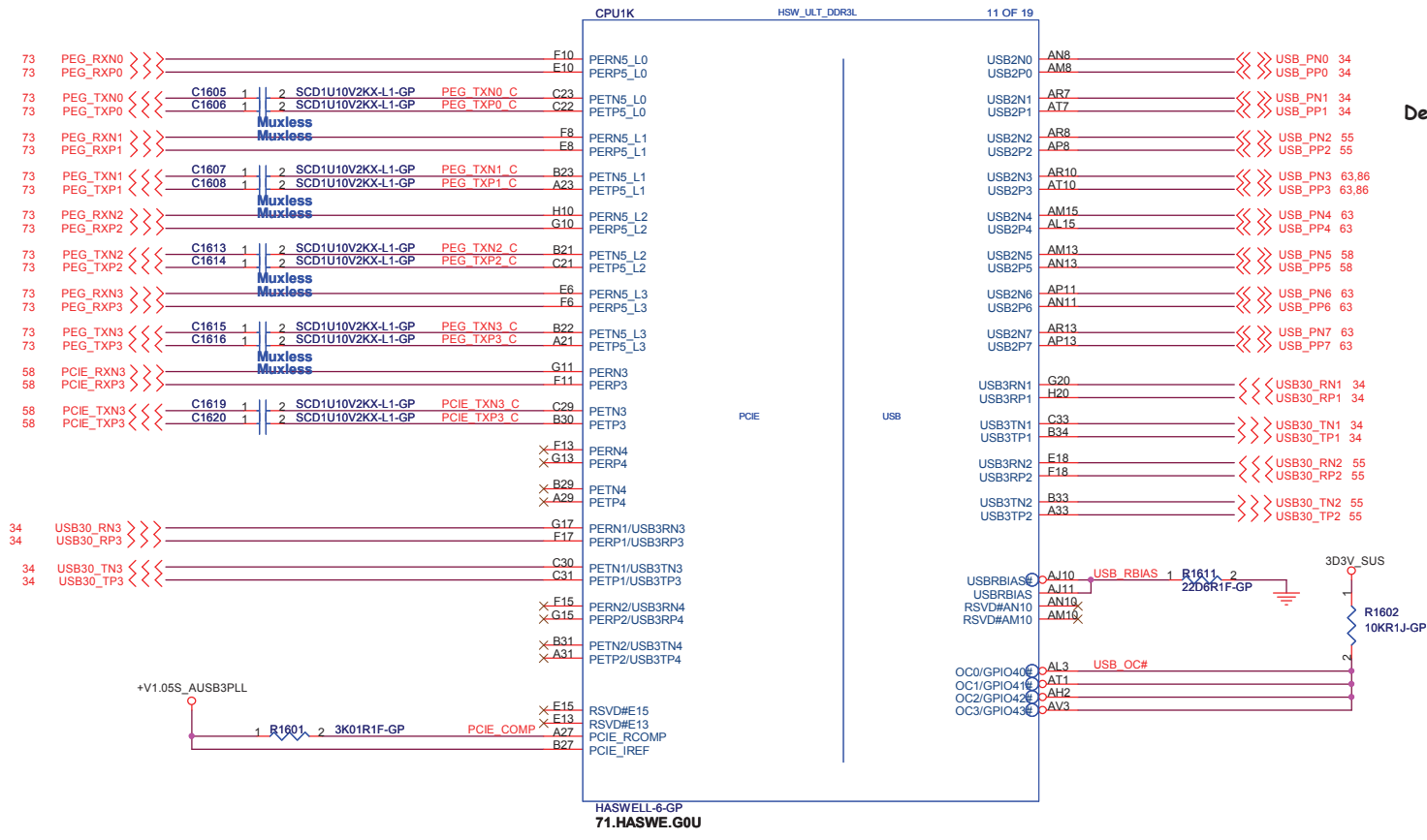
USB2.0 Table

Pair	Device
0	USB3.0 Port 2
1	USB3.0 Port 1
2	DP
3	Cardreader
4	CCD
5	WLAN(Bluetooth)
6	Touch Penal
7	USB2.0 Port 1

Debug Port

USB3.0 Table

Pair	Device
1	USB3.0 Port 1
2	DP
3	USB3.0 Port 2
4	



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<Variant Name>

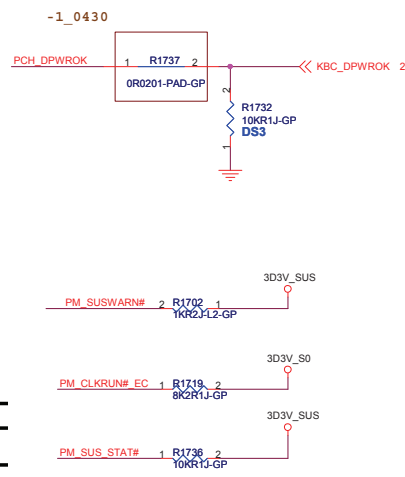
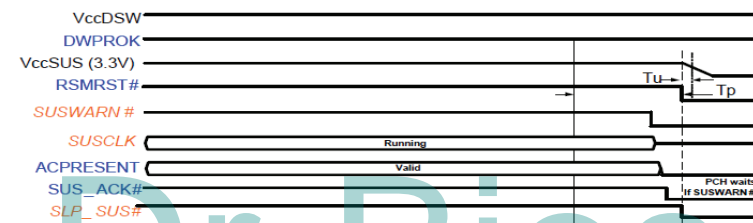
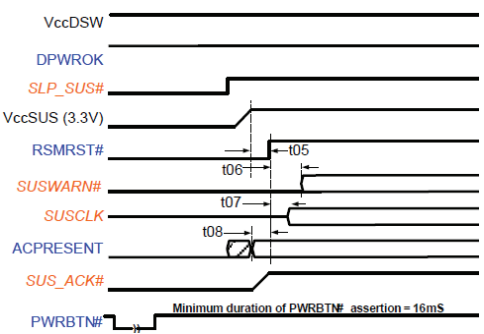
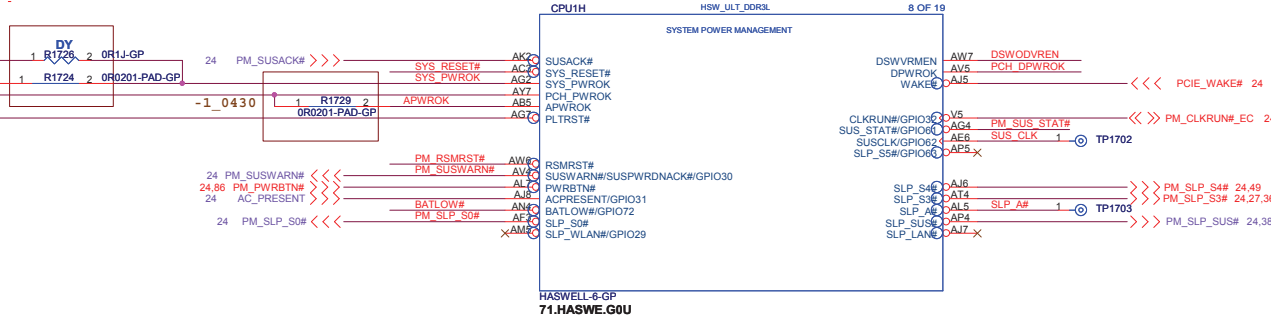
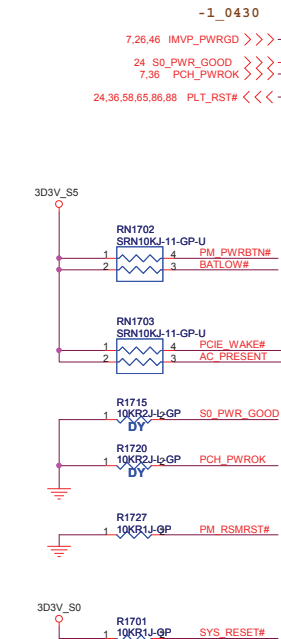
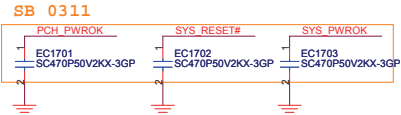
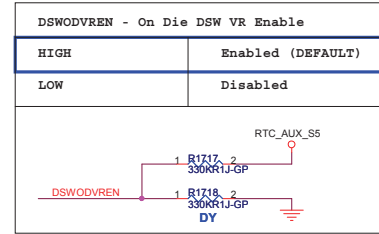
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Title: **CPU (PCI/USB)**

Size A3 Document Number: **WEEBILL_HW** Rev: **SA**

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Bit	Description
31:3	Reserved
2	<p>WAKE# Pin Deep Sx Enable (WAKE_PIN_DSX_EN) - R/W. When this bit is '1', the PCI Express WAKE# pin is monitored while in Deep Sx, supporting wake from Deep Sx due to assertion of this pin. In this case the platform must externally pull-up the pin to the DSW (instead of pulling-up to the SUS as historically been the case). When this bit is '0':</p> <ul style="list-style-type: none"> Deep Sx configurations: The PCH internal pull-down on the WAKE# pin is enabled in Deep Sx and during G3 exit and the pin is not monitored during this time. Deep Sx disabled configurations: The PCH internal pull-down on the WAKE# pin is never enabled. <p>NOTE: Deep Sx disabled configuration must leave this bit at '0'.</p>



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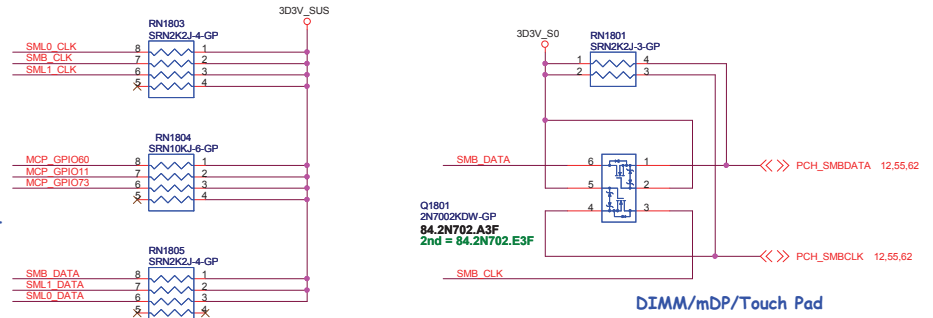
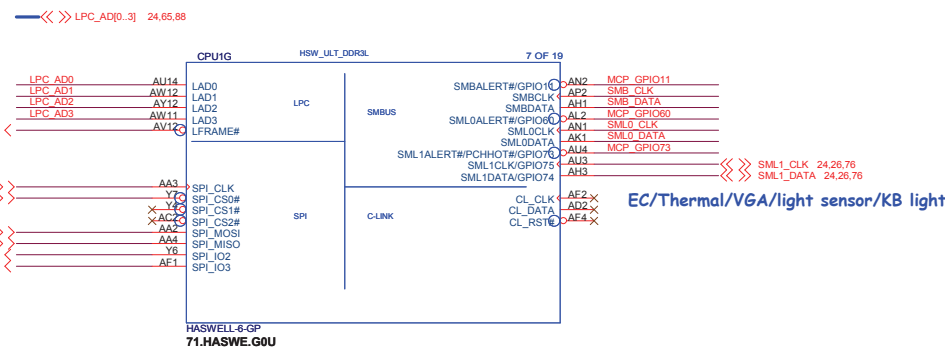
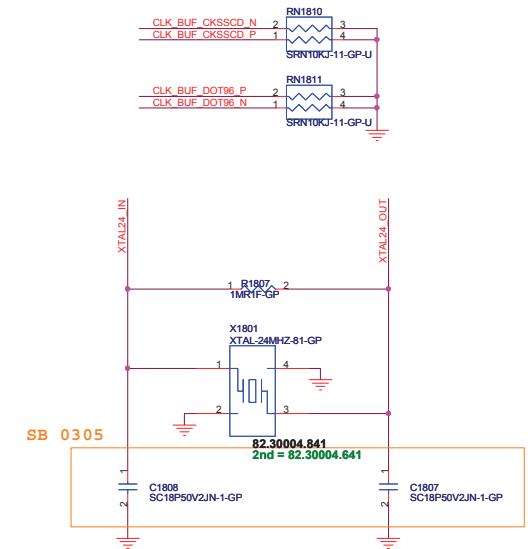
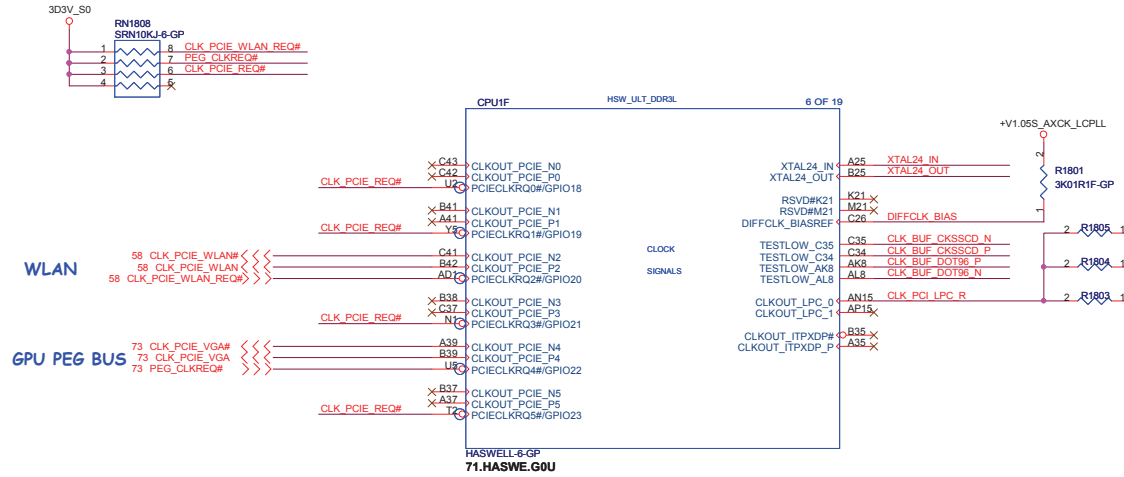
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Title: **CPU (DMI/FDI/PM)**

Size: Custom Document Number: **WEBBILL_HW** Rev: **SA**

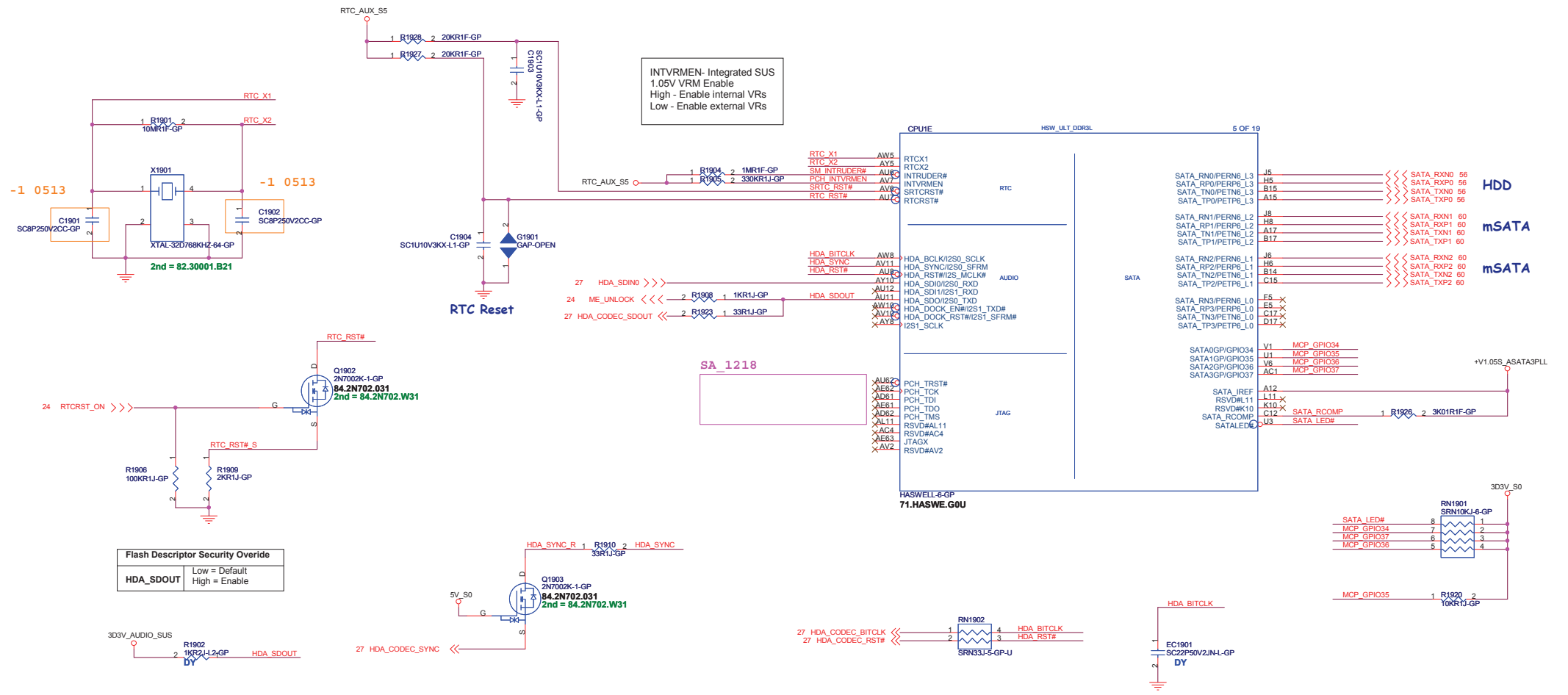
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<Variant Name>

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CPU (PCI-E/SMBUS/CLOCK/CL)			
Size	Document Number	Rev	SA
Custom	WEEBILL_HW		
Date:	Wednesday, September 18, 2013	Sheet	18 of 102

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<Variant Name>

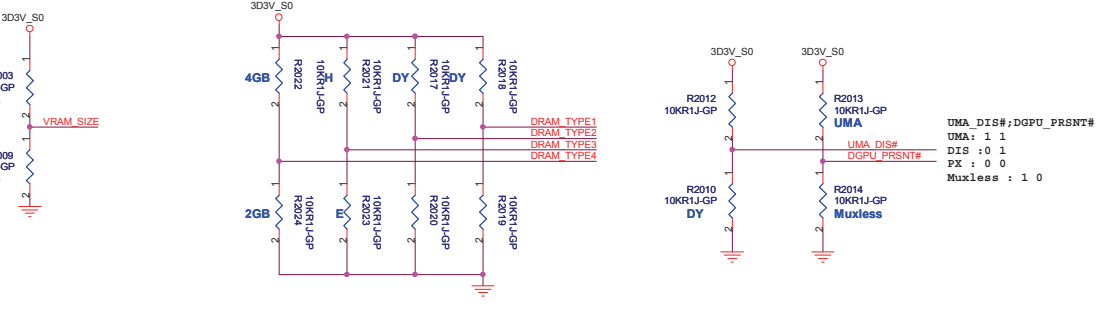
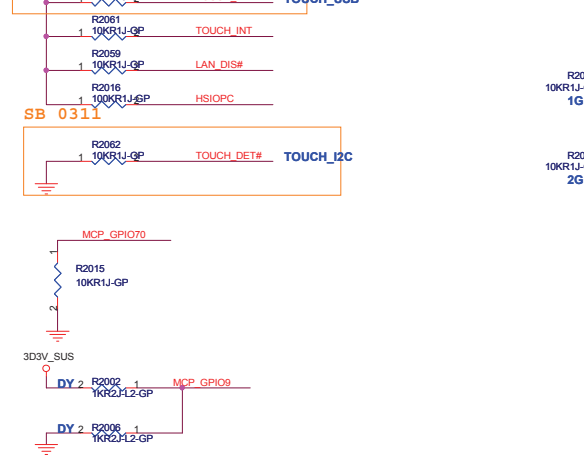
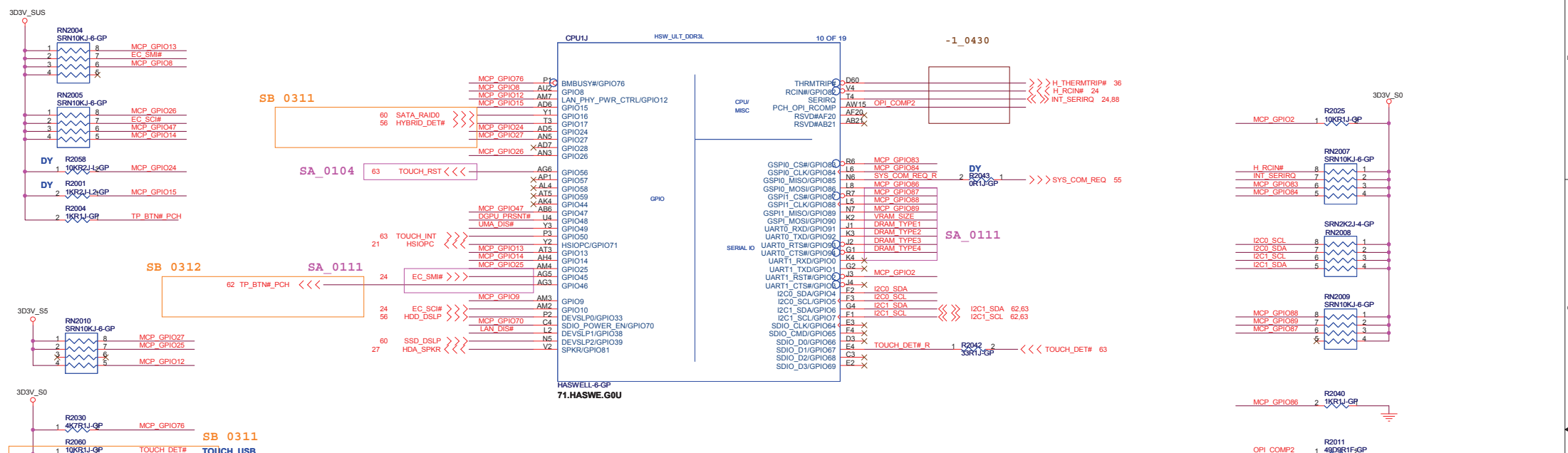
緯創資通 Wistron Corporation
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Title: **CPU (RTC/LPC/SATA/HDA)**

Size: Custom Document Number: **WEEBILL HW** Rev: **SB**

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GPIO#1	GPIO#2	GPIO#3	GPIO#4	Status
DRAM_Type1	DRAM_Type2	DRAM_Type3	DRAM_Type4	
0	0	0	0	ELPIDA DDR3L 1600 2GB (4Gb EDJ4216EFBG-GNL-F LF+HF 256*16)
0	0	0	1	ELPIDA DDR3L 1600 4GB (8Gb EDJ8416E6MB-GNL-F LF+HF 512*16)
0	0	1	0	HYNIX DDR3L 1600 2GB (4Gb H5TC4G63AFR-PBA LF+HF 256*16)
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	

<Variant Name>

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Title: **CPU (GPIO/MISC)**

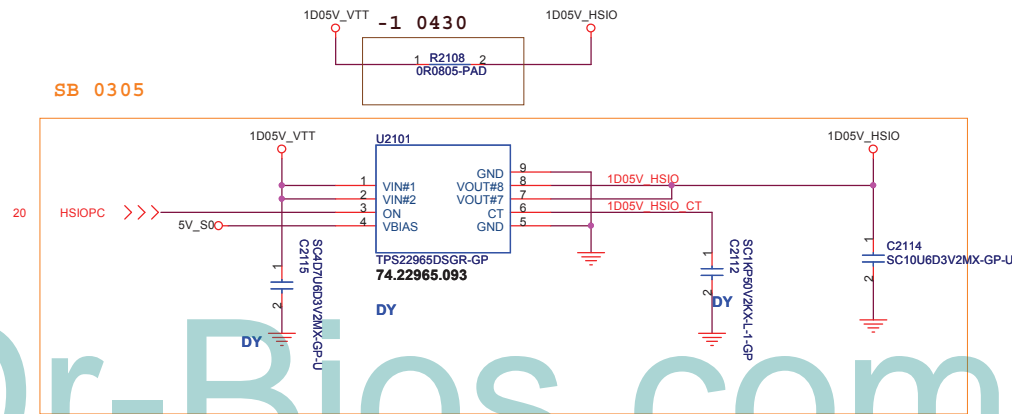
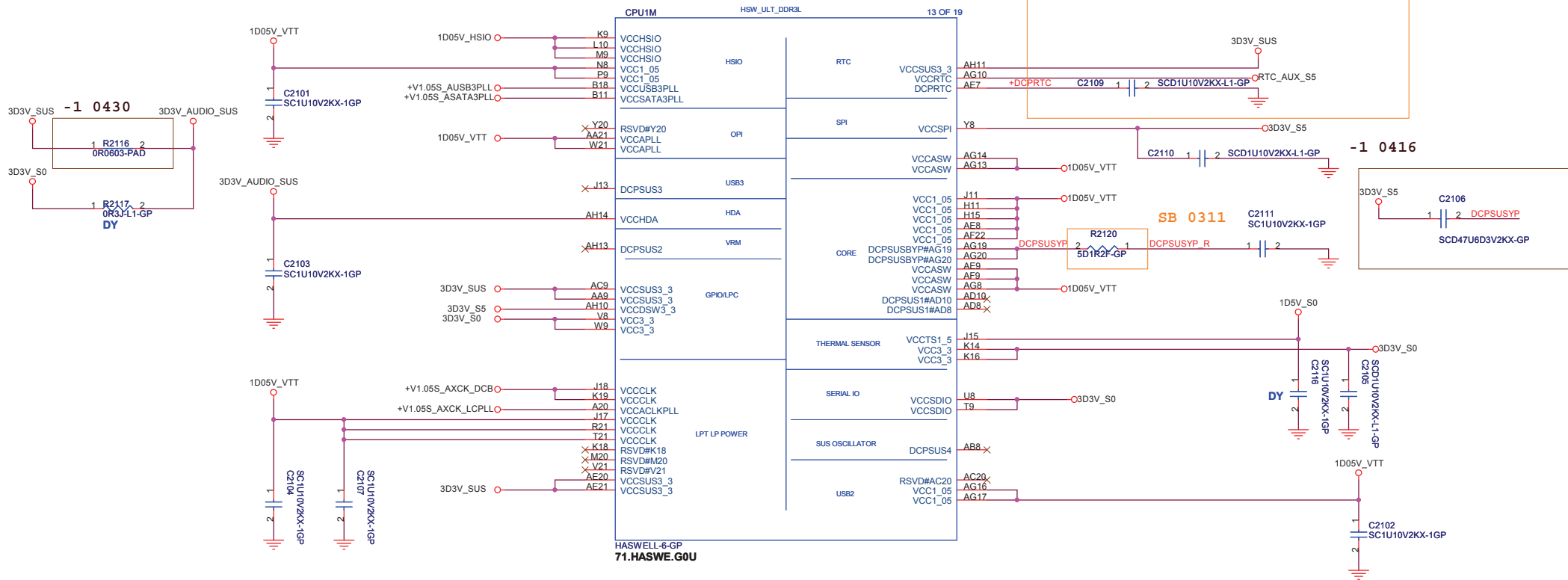
Size: Custom Document Number: **WEEBILL_HW** Rev: SA

Date: Wednesday, September 16, 2013 Sheet: 20 of 102



Notes:

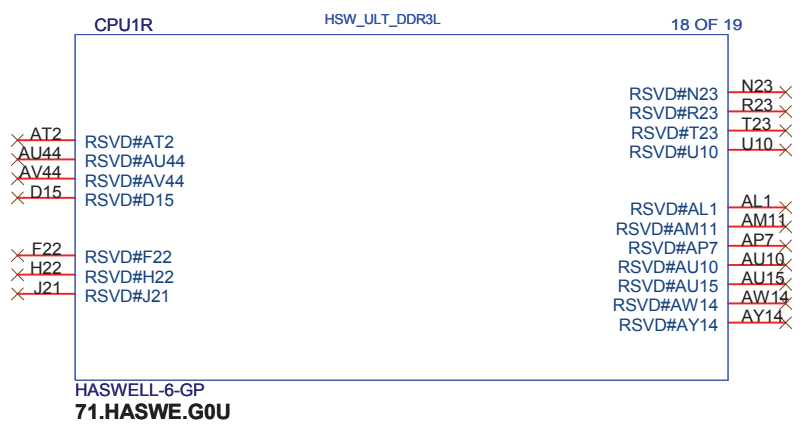
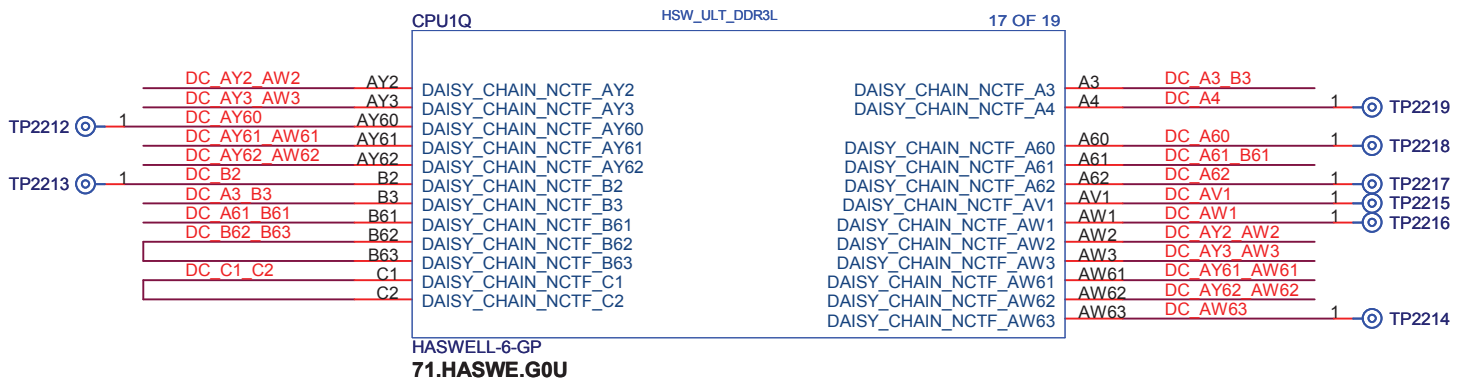
1. Required only on external SUS.
2. Placeholder only. Does not need to be stuffed.
3. The following pins are not to be connected and be left floating. Test point is optional on these pins: AC20, Y20, K18, M20, V21.
4. Note that some decoupling capacitors are shared between more than 1 rail. Follow the "Place capacitors near balls" instructions above to ensure this sharing is optimized.
5. Capacitors should be placed less than 100 mils (2.54 mm) from the edge of package.
6. For description of (R)unway, and (E)dge decoupling capacitor placement, please refer to Section 41.3, "Loop Inductance Reduction Decoupling" on page 532.



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Title		CPU (POWER1)	
Size A3	Document Number	WEEBILL_HW	
Date: Wednesday, September 18, 2013	Sheet	21	of 102
Rev		SA	

緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

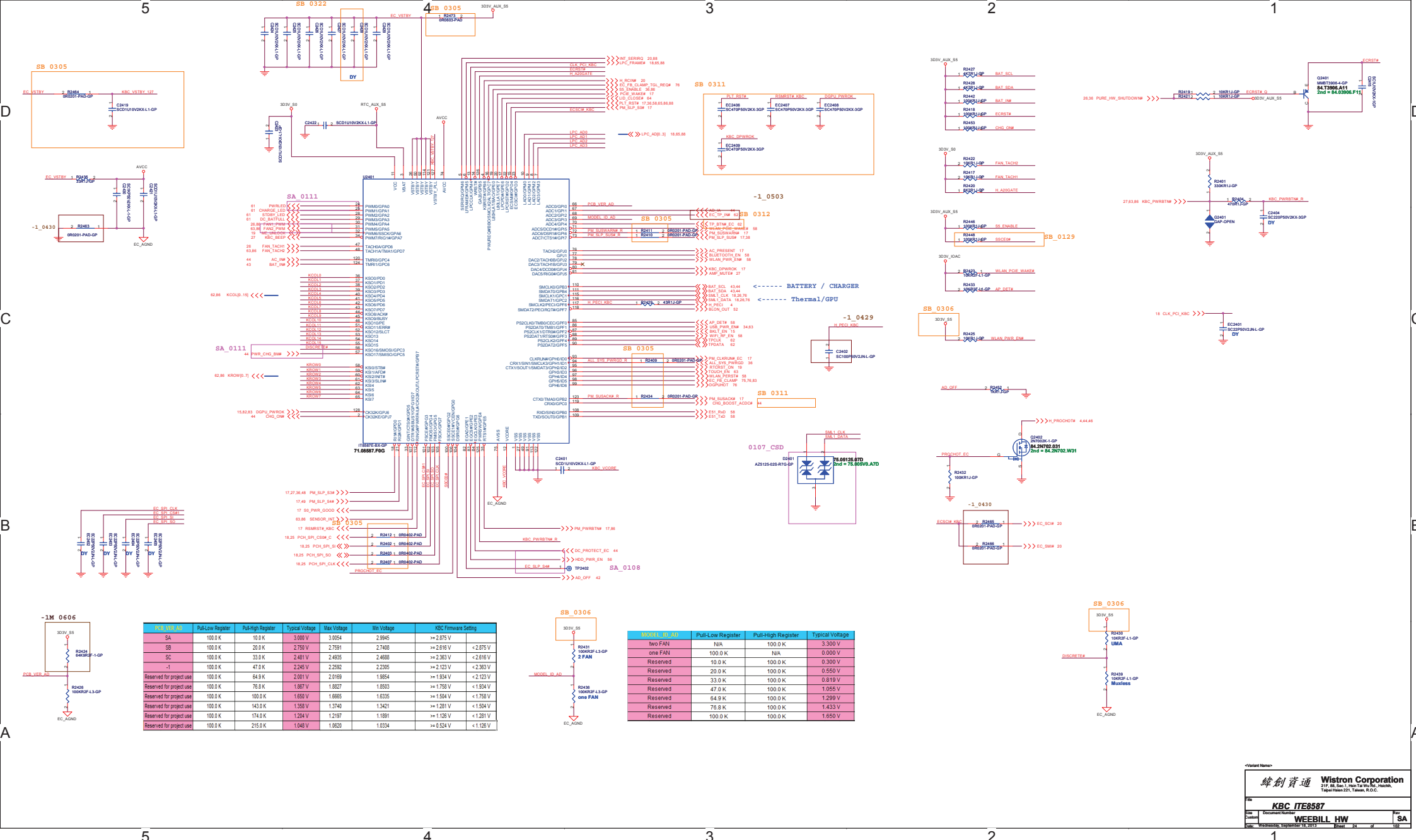


<Variant Name>

	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
---	---

Title		CPU (RSVD)	
Size	Document Number	Rev	
A4	WEEBILL_HW	SA	
Date:	Wednesday, September 18, 2013	Sheet	22 of 102

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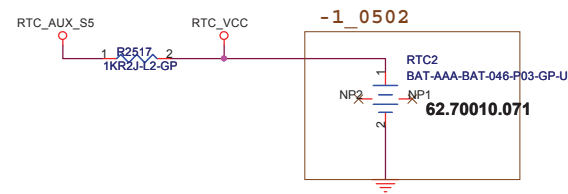
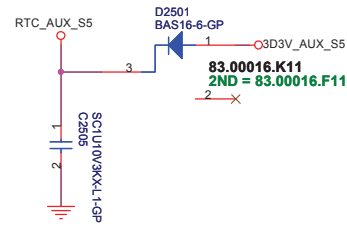
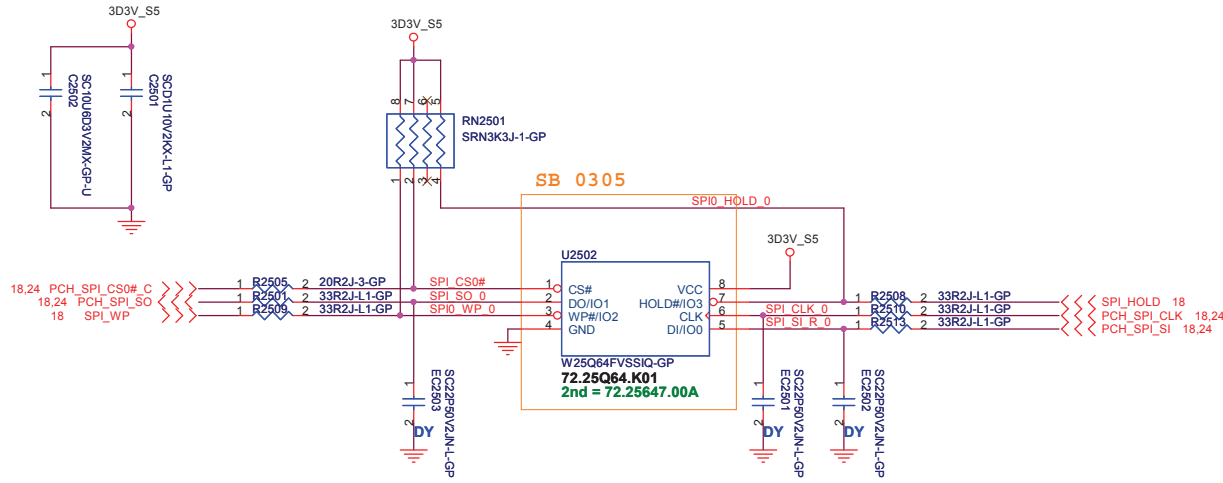


VDD_VDD_IN	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	Min Voltage	KBC Firmware Setting
SA	100.0 K	10.0 K	3.000 V	3.0054	2.9945	>> 2.875 V
SB	100.0 K	20.0 K	2.750 V	2.7591	2.7408	>> 2.616 V << 2.875 V
SC	100.0 K	33.0 K	2.481 V	2.4935	2.4688	>> 2.383 V
-1	100.0 K	47.0 K	2.245 V	2.2592	2.2305	>> 2.123 V << 2.383 V
Reserved for project use	100.0 K	64.9 K	2.001 V	2.0169	1.9854	>> 1.934 V
Reserved for project use	100.0 K	76.8 K	1.867 V	1.8827	1.8503	>> 1.750 V << 1.934 V
Reserved for project use	100.0 K	100.0 K	1.650 V	1.6665	1.6335	>> 1.544 V << 1.750 V
Reserved for project use	100.0 K	143.0 K	1.358 V	1.3740	1.3421	>> 1.281 V << 1.544 V
Reserved for project use	100.0 K	174.0 K	1.204 V	1.2197	1.1891	>> 1.128 V << 1.281 V
Reserved for project use	100.0 K	215.0 K	1.048 V	1.0620	1.0334	>> 0.924 V << 1.128 V

00301_IN_00	Pull-Low Register	Pull-High Register	Typical Voltage
two FAN	N/A	100.0 K	3.300 V
one FAN	100.0 K	N/A	0.000 V
Reserved	10.0 K	100.0 K	0.300 V
Reserved	20.0 K	100.0 K	0.550 V
Reserved	33.0 K	100.0 K	0.819 V
Reserved	47.0 K	100.0 K	1.055 V
Reserved	64.9 K	100.0 K	1.299 V
Reserved	76.8 K	100.0 K	1.433 V
Reserved	100.0 K	100.0 K	1.650 V

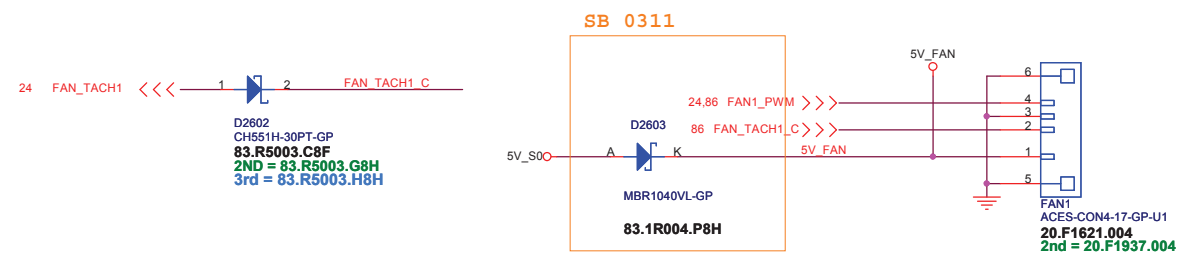
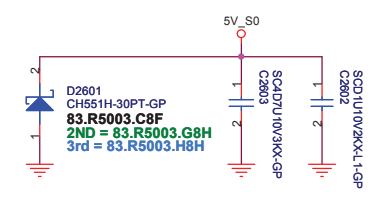
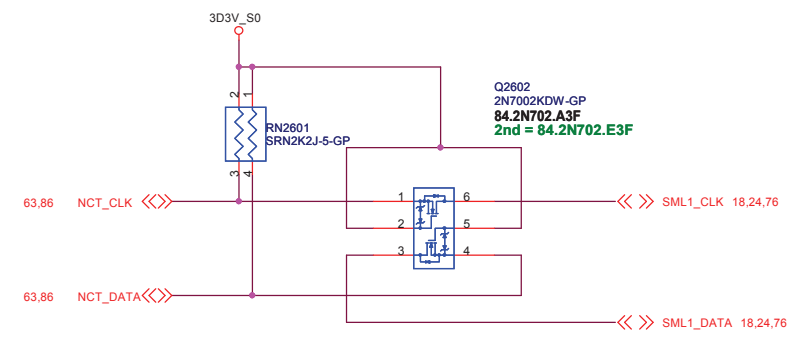
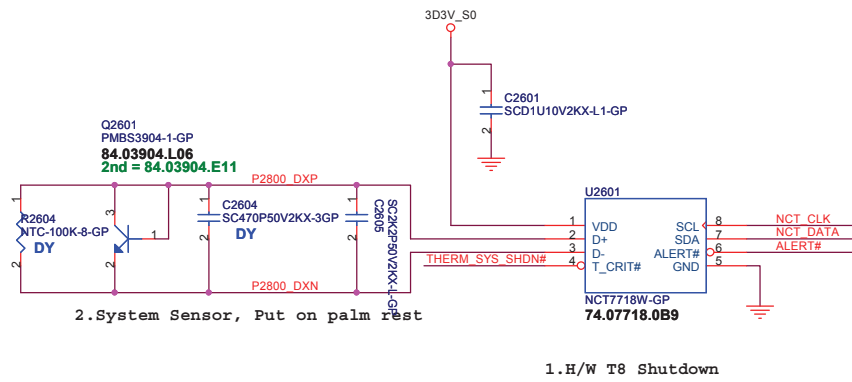
Wistron Corporation
 緯創資通
 2/F, 88 Sec. 1, Hsin Ta Hsi, Rd., Hsuehshan, Taipei Hsin 221, Taiwan, R.O.C.
 KBC ITE887
 WE8BILL_HW
 SA

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<Variant Name>		
緯創資通 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
Flash(KBC+PCH)/RTC		
Size	Document Number	Rev
A3	WEEBILL_HW	SB
Date:	Wednesday, September 18, 2013	Sheet 25 of 102

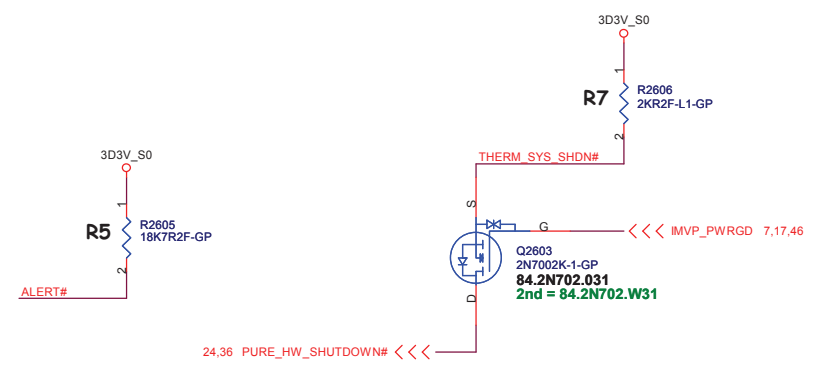


ALERT# /T CRIT#
Pull-up Resistor

R5	R7				
	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
2Kohm	77°C	87°C	97°C	107°C	117°C
7.5Kohm	79°C	89°C	99°C	109°C	119°C
10.5Kohm	81°C	91°C	101°C	111°C	121°C
14Kohm	83°C	93°C	103°C	113°C	123°C
18.7Kohm	85°C	95°C	105°C	115°C	125°C

T_CRIT temperature strapping point

T8=85 degree



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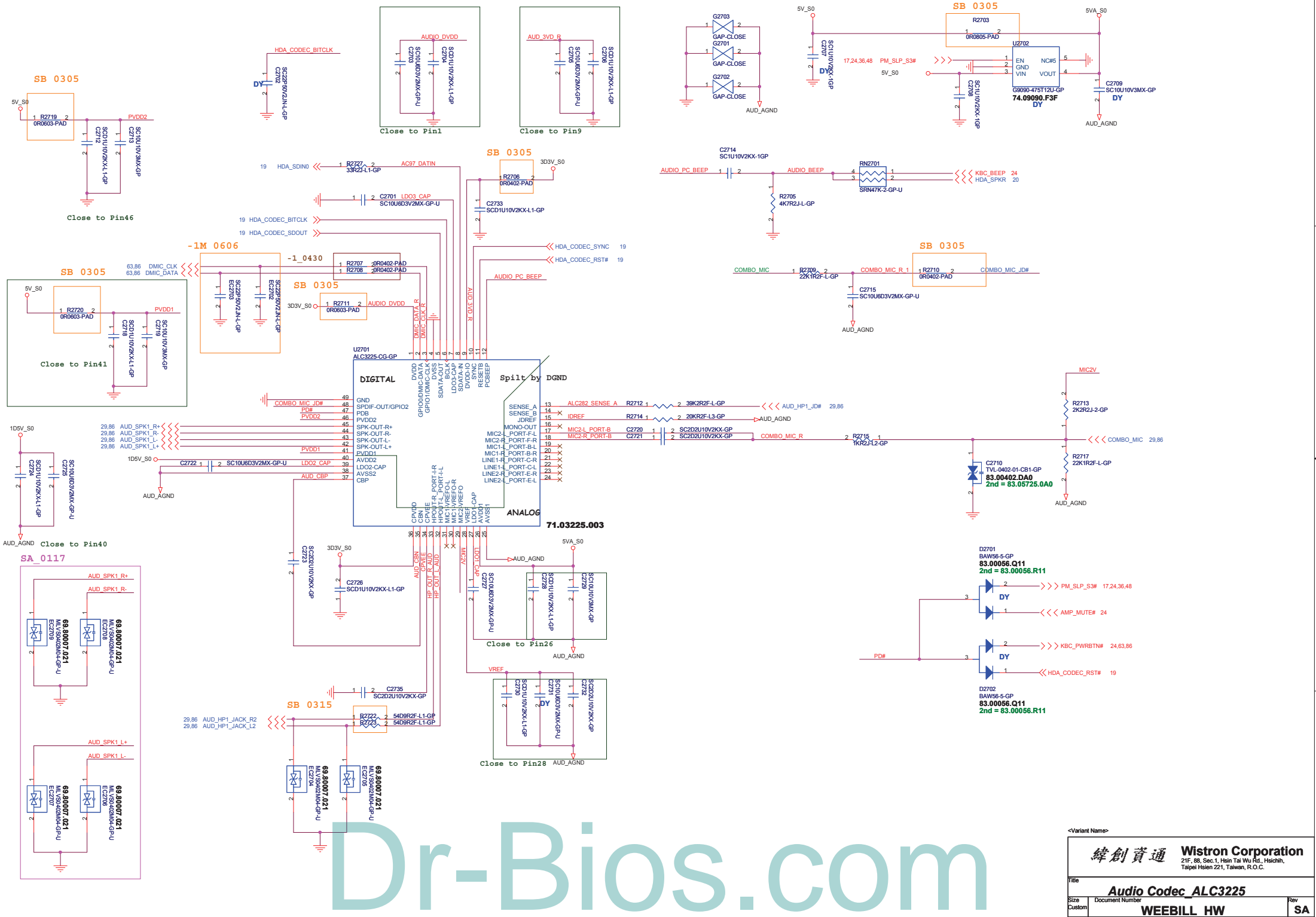
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緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Thermal 7718/Fan Controller P2793**

Size A3 Document Number: **WEEBILL_HW** Rev: **SA**

Date: Wednesday, September 18, 2013 Sheet 26 of 102



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Blanking

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<Variant Name>

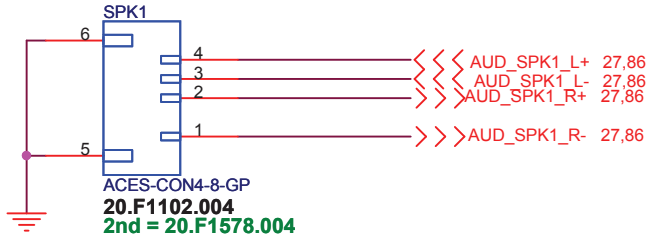
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

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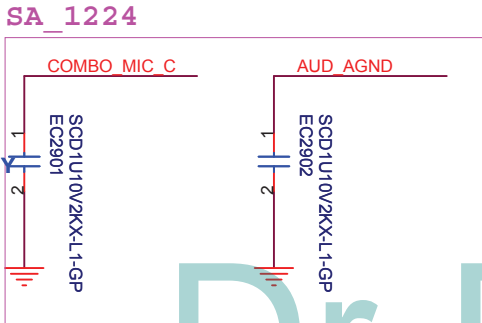
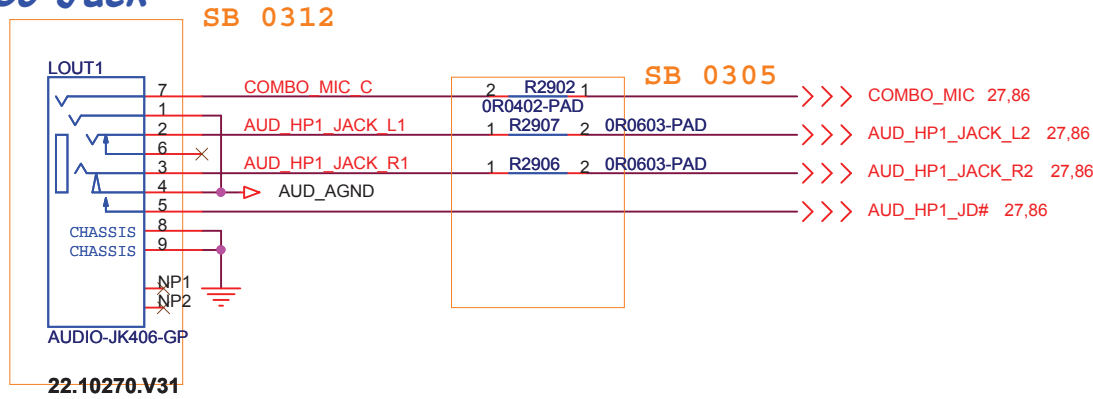
Size A4 Document Number **WEEBILL_HW** Rev **SA**

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Speaker



Combo Jack

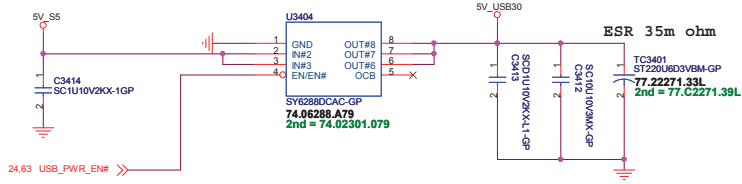


<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title Audio Jack		
Size A4	Document Number WEEBILL_HW	Rev SA
Date: Wednesday, September 18, 2013	Sheet 29 of 102	

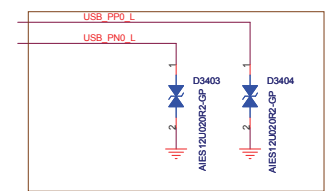
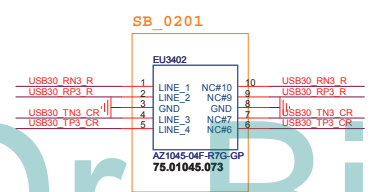
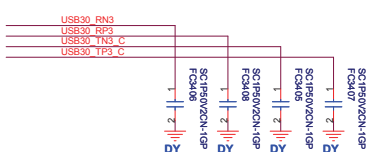
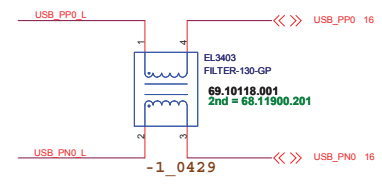
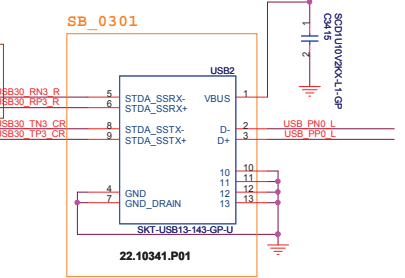
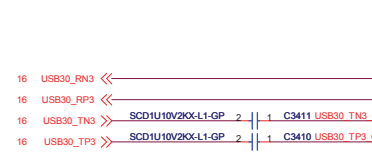
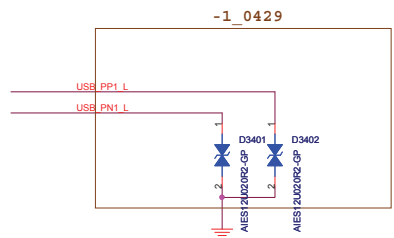
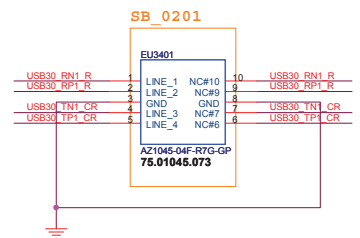
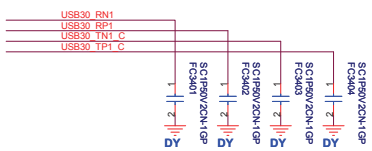
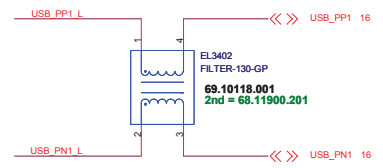
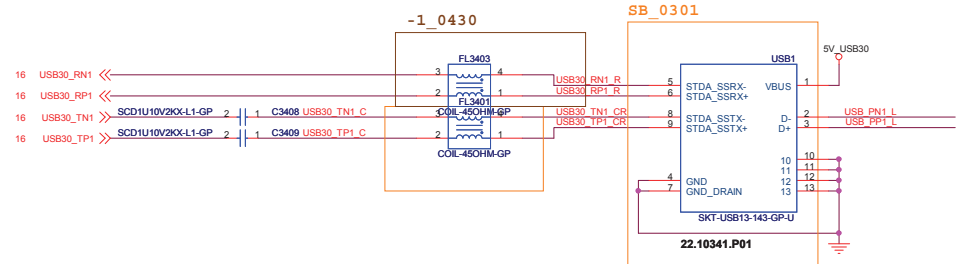
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**USB 3.0 Connector
Pin definition**

1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+ SuperSpeed RX
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+ SuperSpeed TX

SB_0315



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緯創資通

Wistron Corporation

21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB 2.0 / 3.0 Port**

Size: Document Number

Custom: **WEEBILL HW**

Date: Wednesday, September 18, 2013

Rev: **SB**

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Blanking

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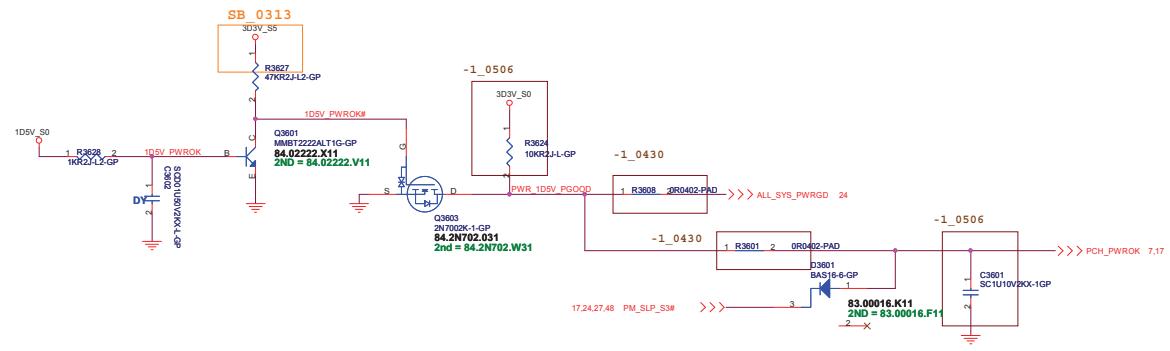
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **USB CHARGER**

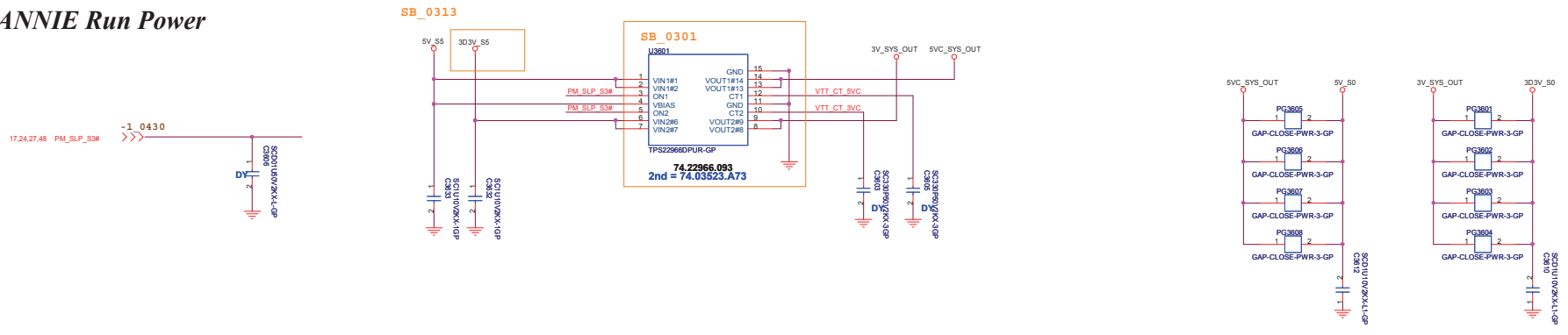
Size A4 Document Number **WEEBILL_HW** Rev **SA**

Date: Wednesday, September 18, 2013 Sheet 35 of 102

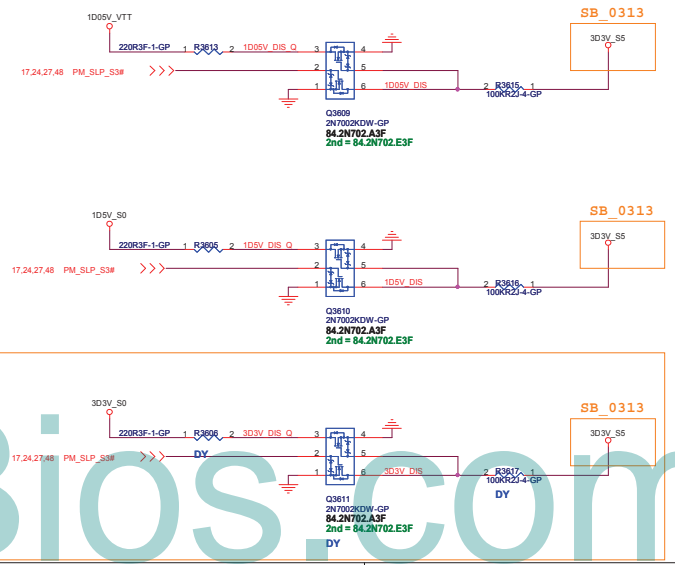
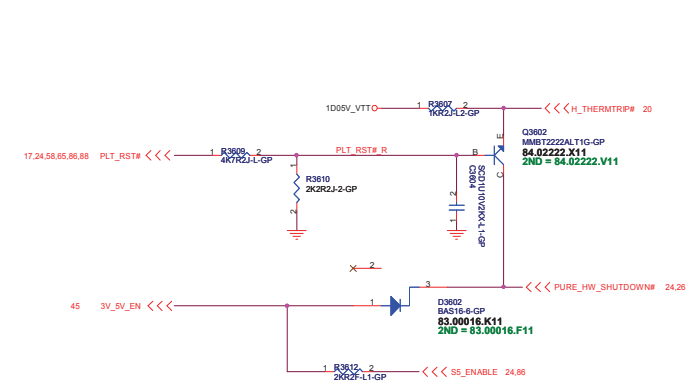
Power Sequence



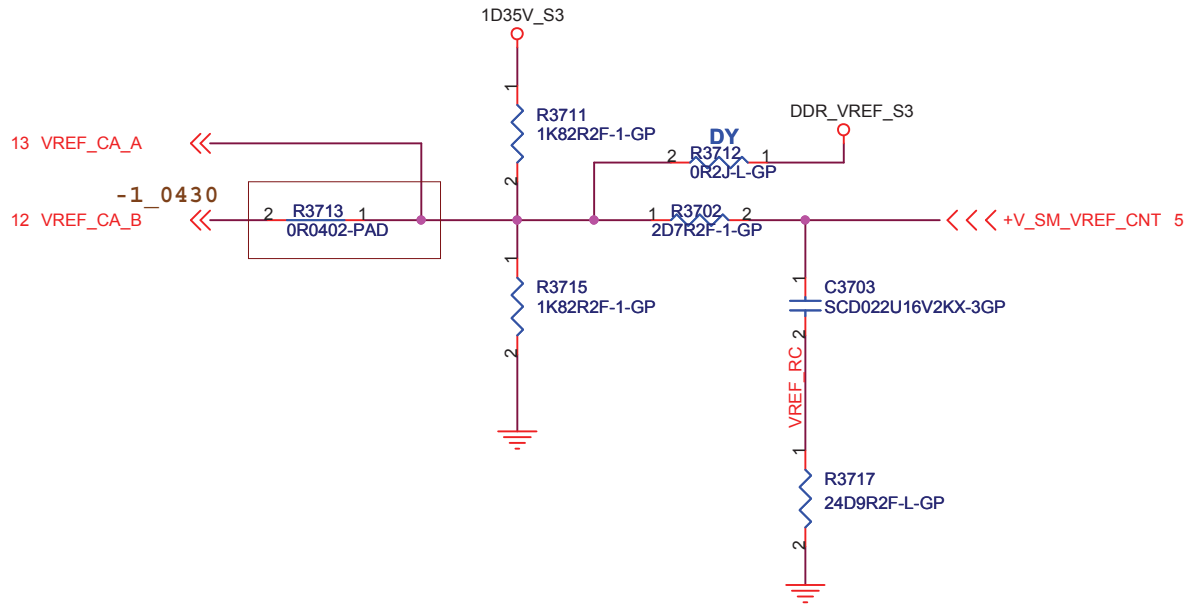
ANNIE Run Power



Discharge circuit



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<Variant Name>

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 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

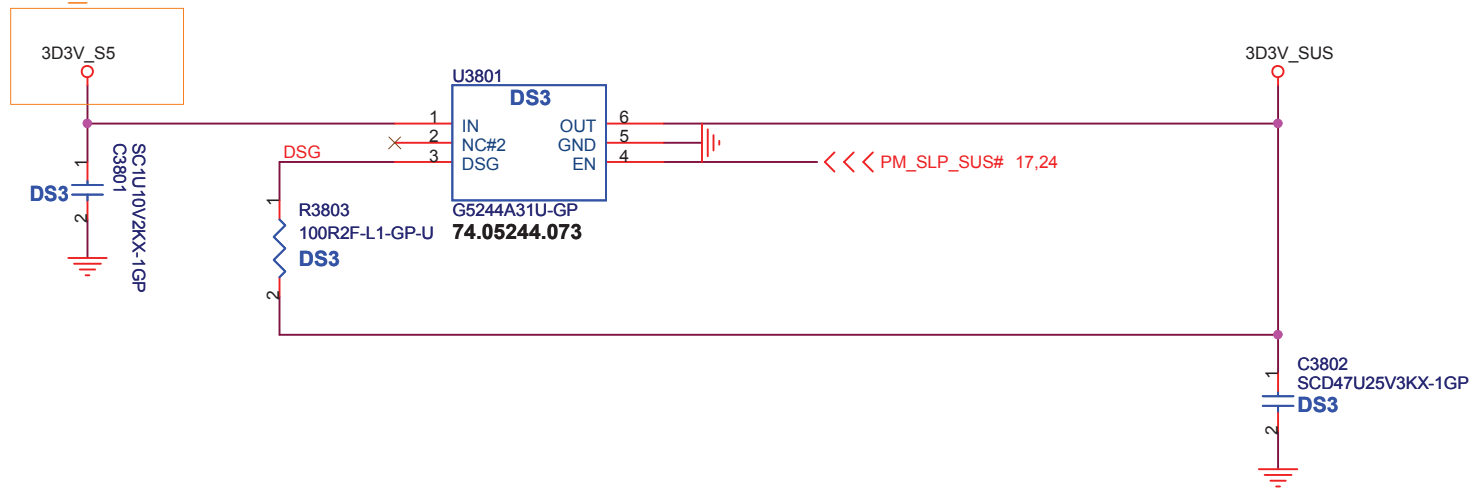
Title **ADAPTER OCP / S3 reduction**

Size A4 Document Number **WEEBILL_HW** Rev **SA**

Date: Wednesday, September 18, 2013 Sheet 37 of 102

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SB_0313



<Variant Name>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

DS3

Size
A4

Document Number

WEEBILL_HW

Rev

SA

Date: Wednesday, September 18, 2013

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Power Sequence

Blanking

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<Variant Name>

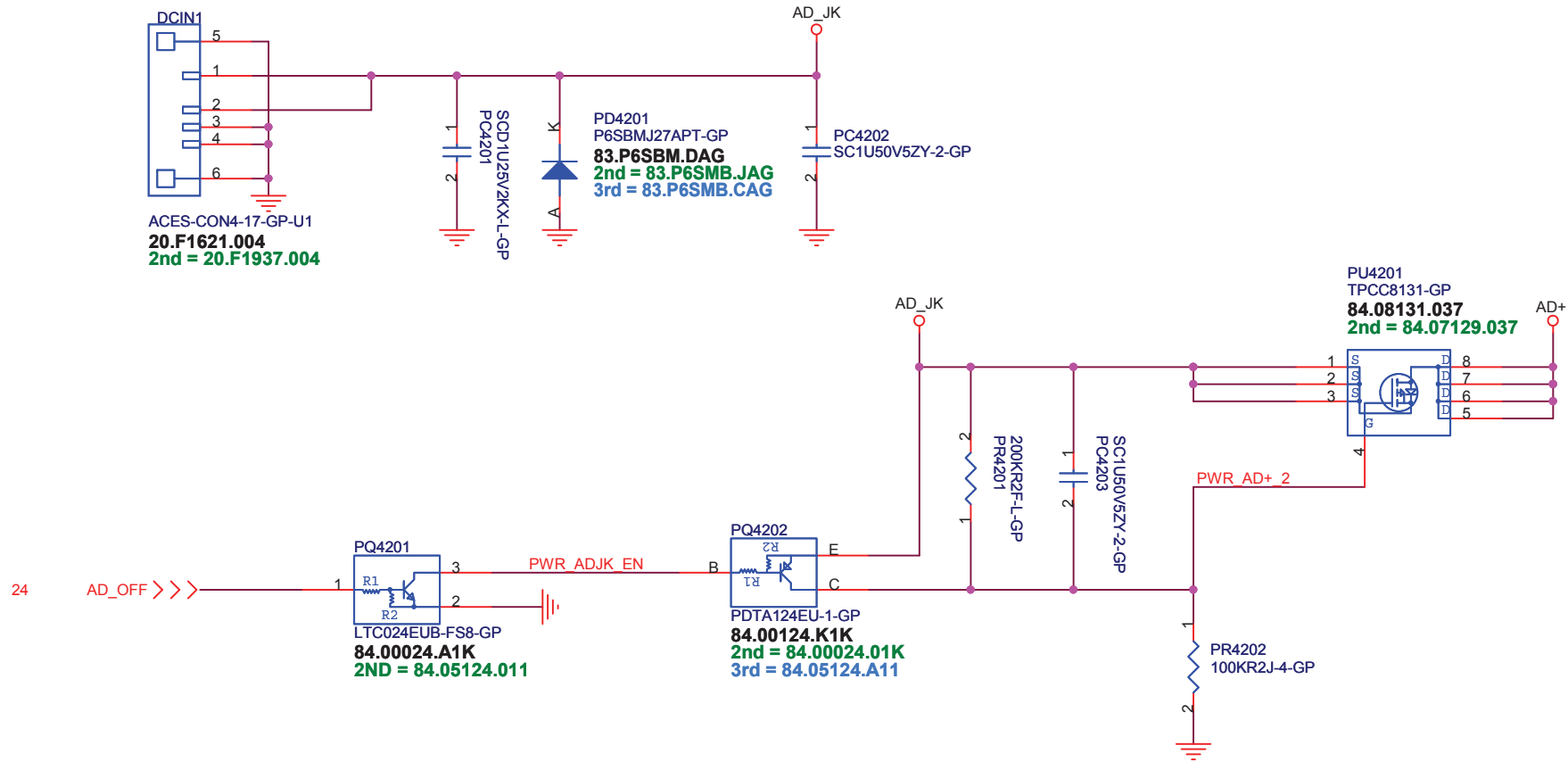
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **1D05_M**

Size A4 Document Number **WEEBILL_HW** Rev **SA**

Date: Wednesday, September 18, 2013 Sheet 39 of 102

0.4 pitch, AWG#28:2.0 A/pin



<Variant Name>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

DCIN JACK

Size
A4

Document Number

WEEBILL_HW

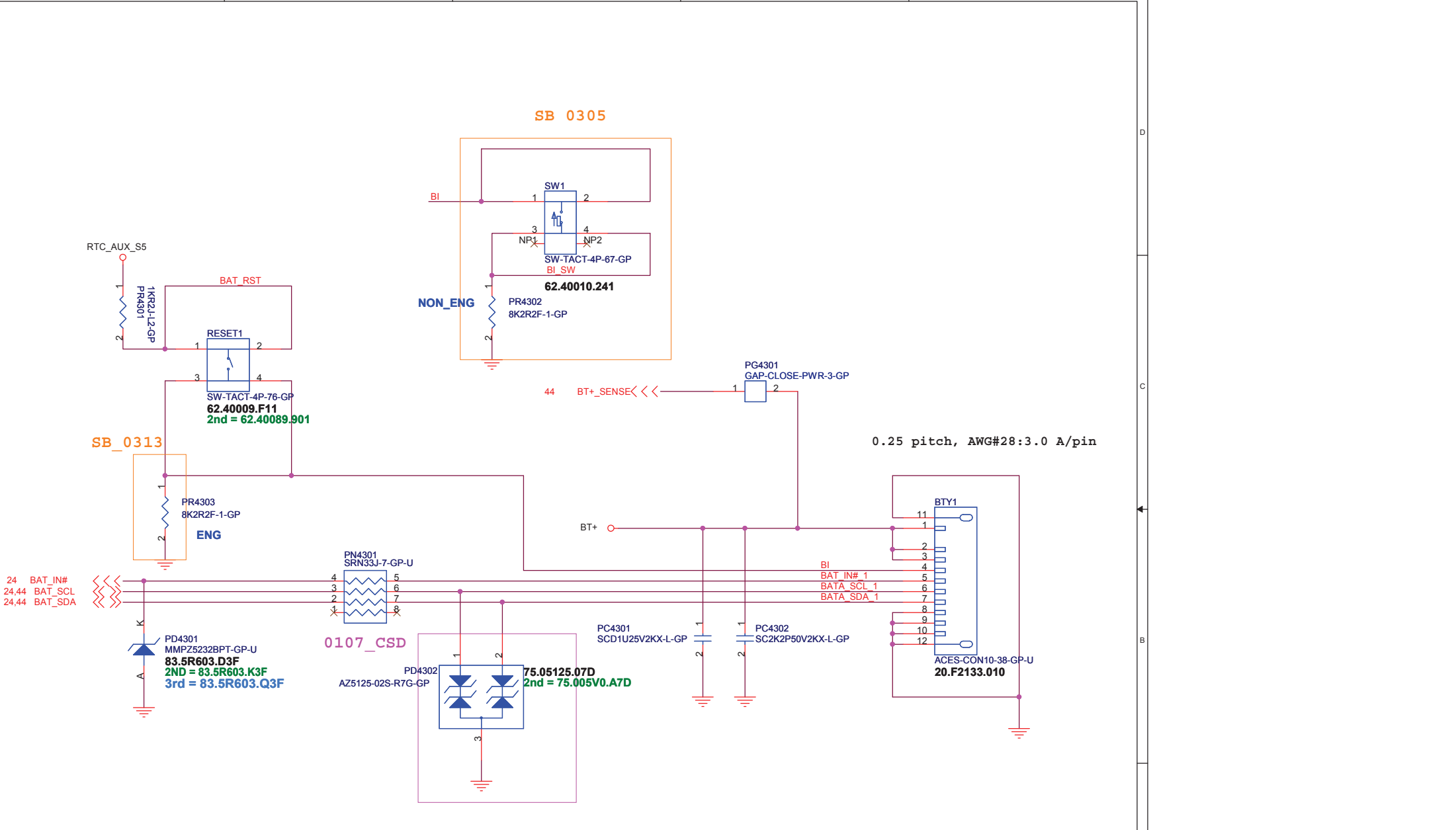
Rev

SA

Date: Wednesday, September 18, 2013

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24 BAT_IN#
24,44 BAT_SCL
24,44 BAT_SDA

86 BI >>>
86 BAT_IN#_1 >>>
86 BATA_SCL_1 >>>
86 BATA_SDA_1 >>>

0.25 pitch, AWG#28:3.0 A/pin

<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
BATT CONN	
Size	Document Number
Custom	WEEBILL_HW
Date: Wednesday, September 18, 2013	Rev SA
Sheet 43	of 102

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SSID = Charger

modify schematic
2012-1218 - wayler

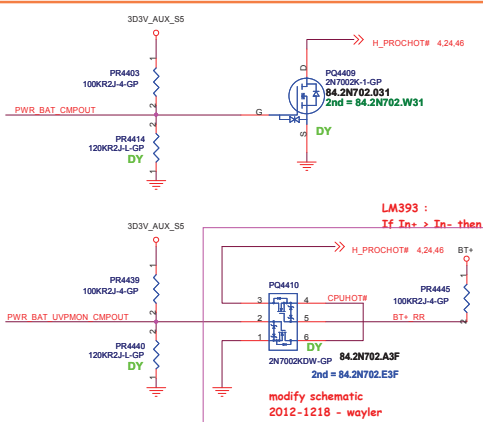
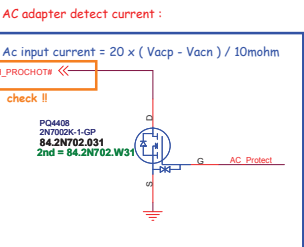
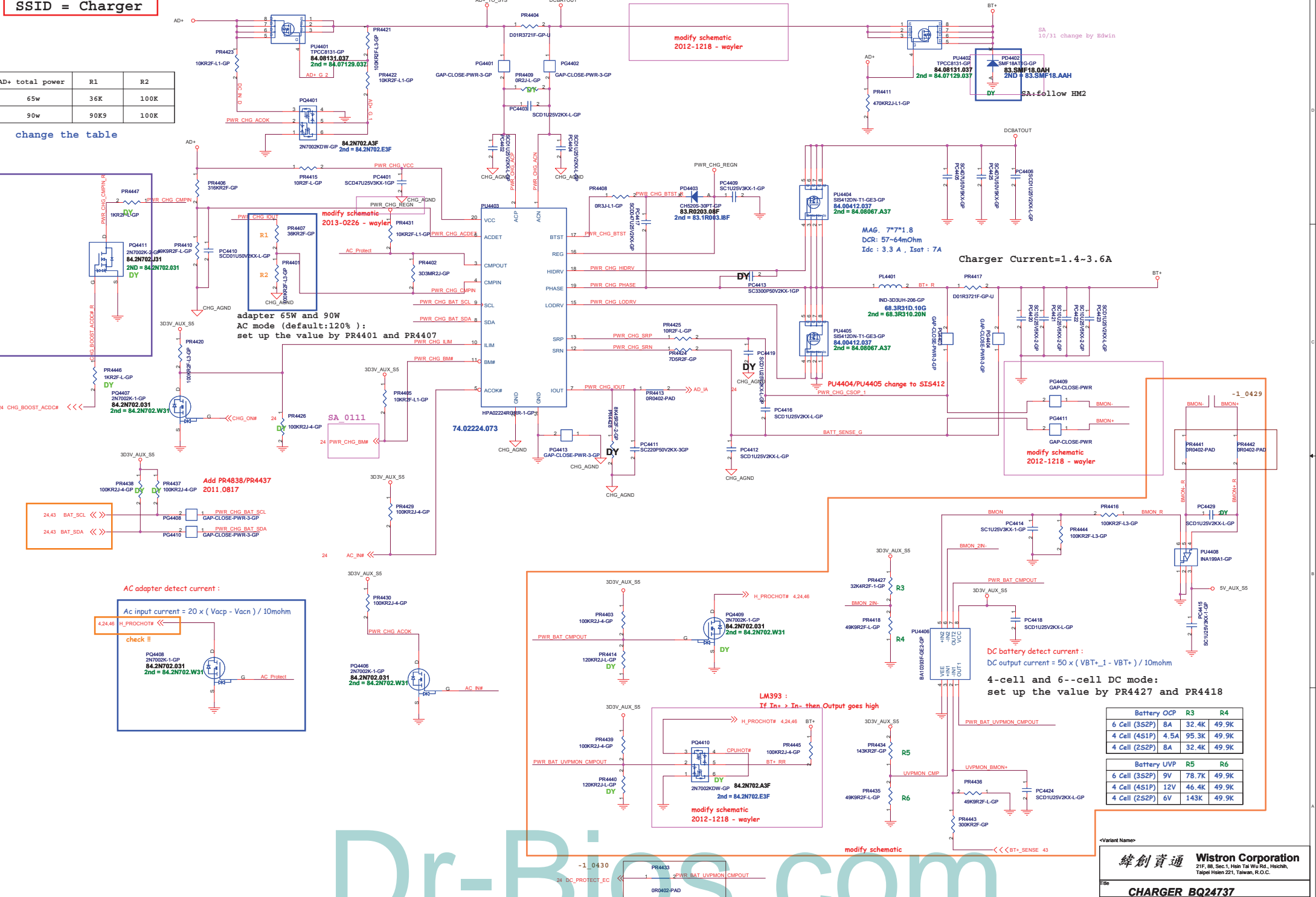
SA 10/31 change by Edwin

AD+ total power	R1	R2
65w	36K	100K
90w	90K9	100K

change the table

adapter 65W and 90W
AC mode (default:120%) :
set up the value by PR4401 and PR4407

Charger Current=1.4-3.6A

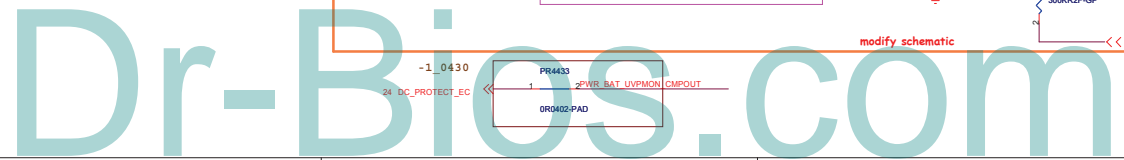


DC battery detect current :
DC output current = $50 \times (V_{BT+1} - V_{BT+}) / 10\text{mohm}$

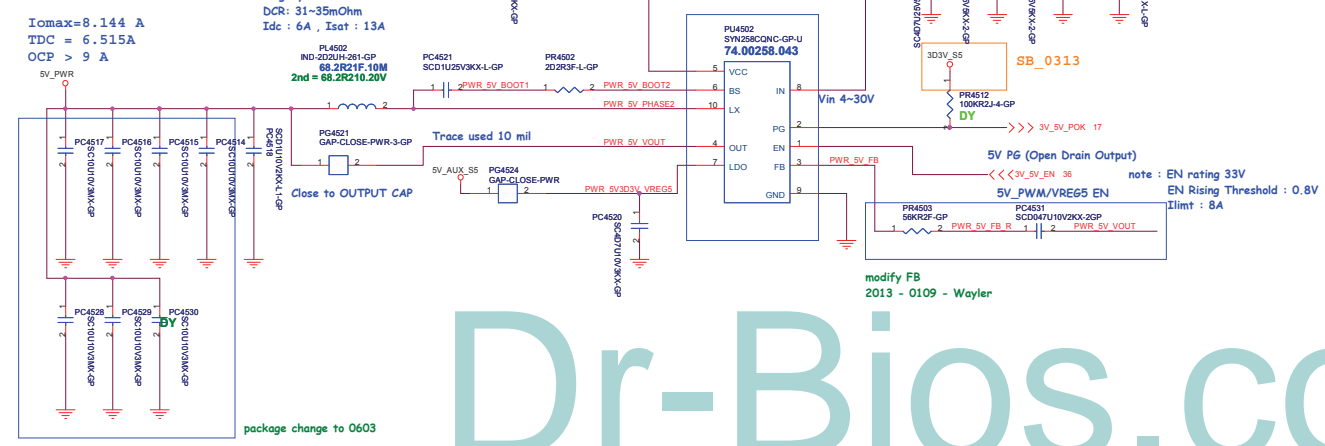
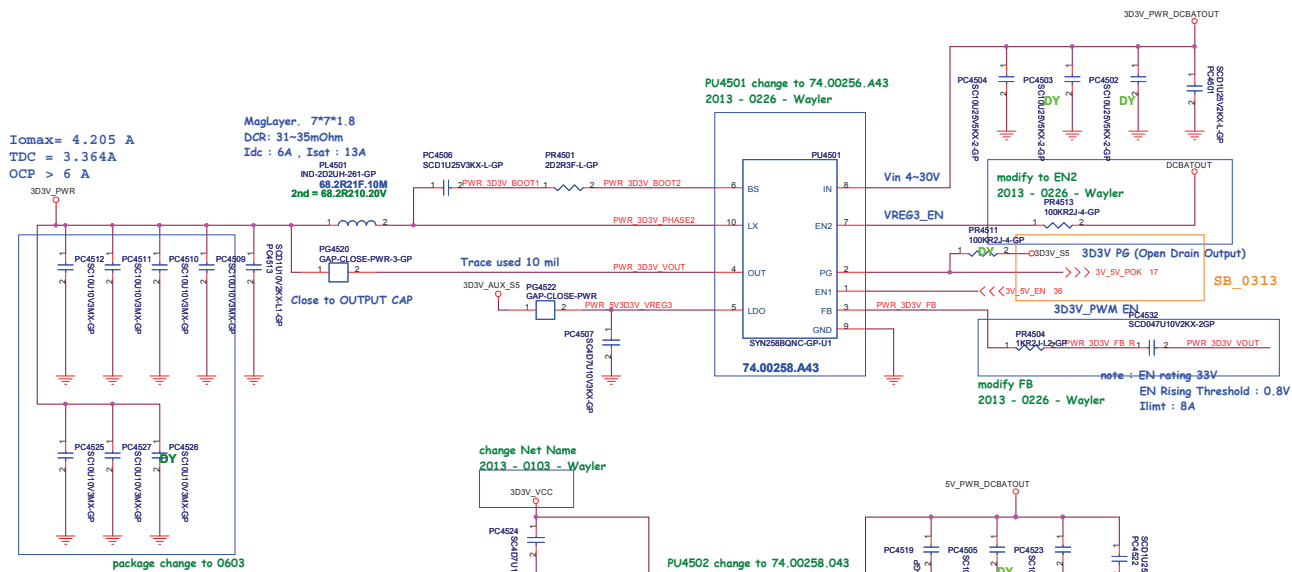
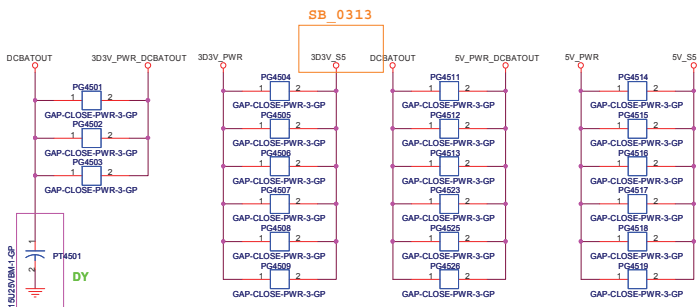
4-cell and 6--cell DC mode:
set up the value by PR4427 and PR4418

Battery OCP	R3	R4	
6 Cell (3S2P)	8A	32.4K	49.9K
4 Cell (4S1P)	4.5A	95.3K	49.9K
4 Cell (2S2P)	8A	32.4K	49.9K

Battery UVP	R5	R6	
6 Cell (3S2P)	9V	78.7K	49.9K
4 Cell (4S1P)	12V	46.4K	49.9K
4 Cell (2S2P)	6V	143K	49.9K

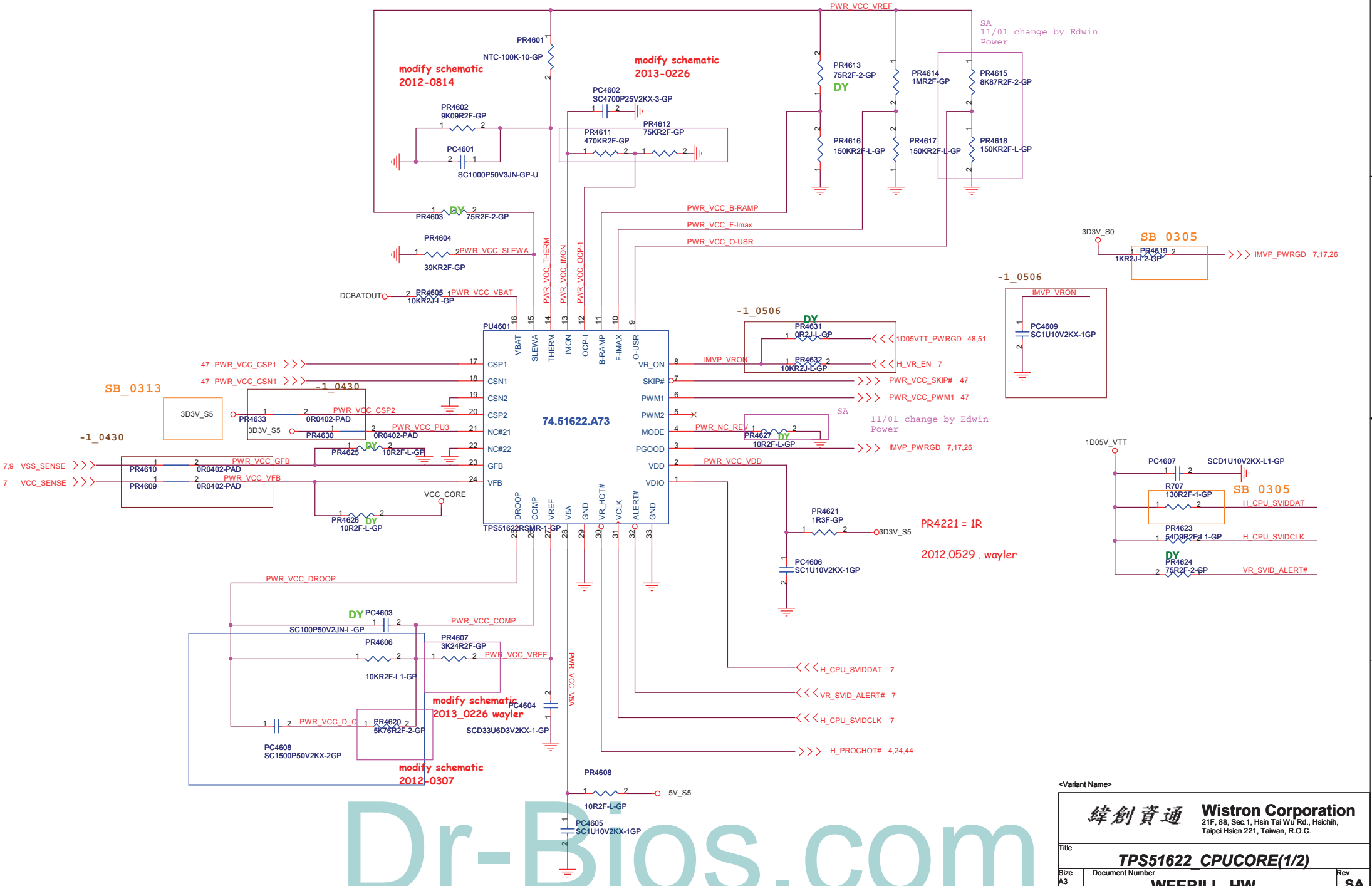


SSID = PWR.Plane.Regulator 3p3v5v



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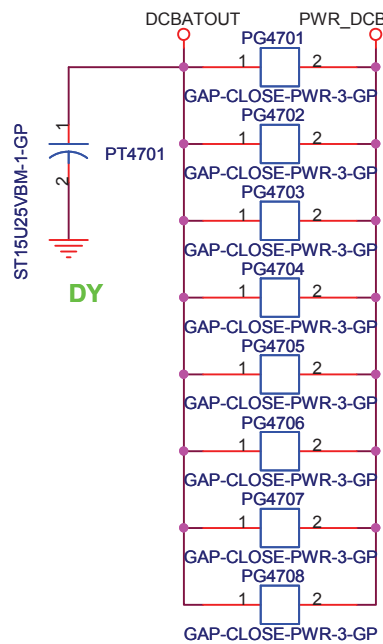
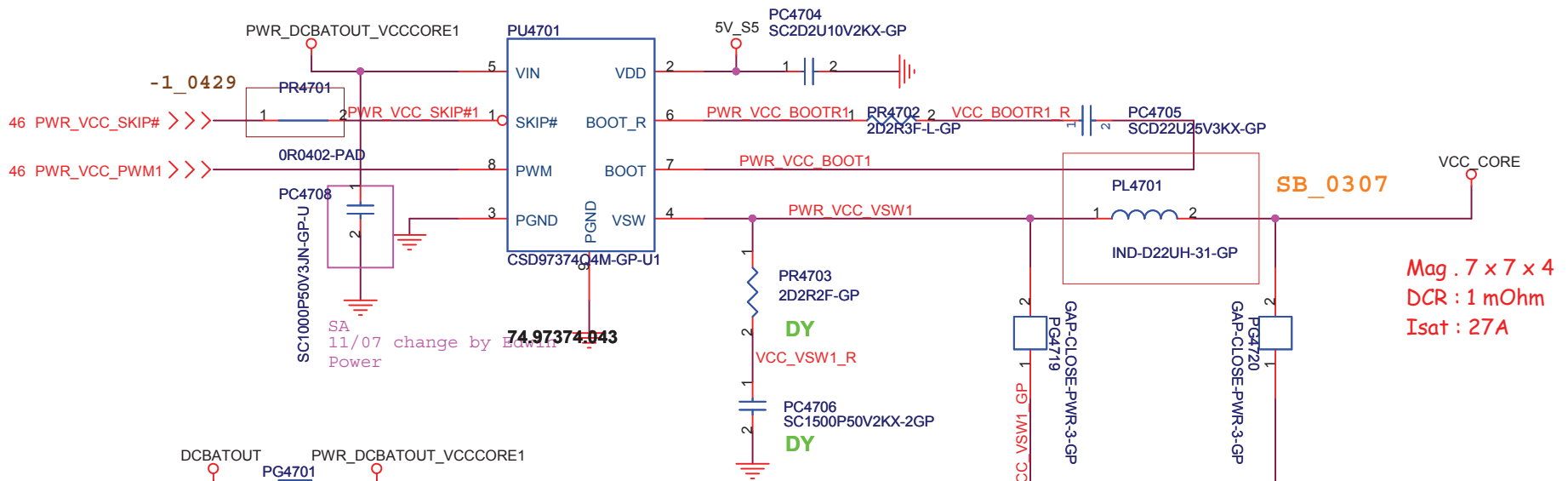
SSID = CPU.Regulator



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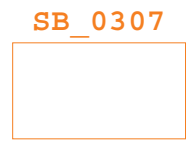
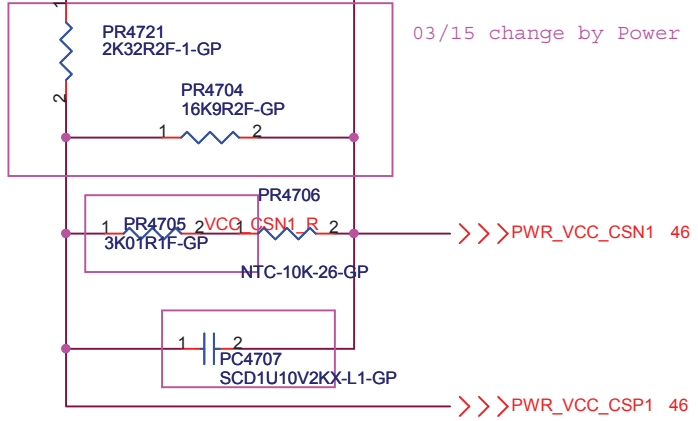
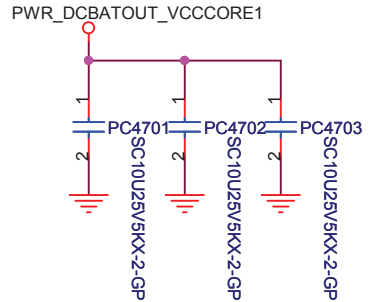
Title		
TPS51622 CPUCORE(1/2)		
Size A3	Document Number	Rev SA
Date: Wednesday, September 18, 2013		
Sheet 46 of 102		

緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.



PR4704

15W	25W
16.9Kohm	17.8Kohm
64.16925.6DL	64.17825.6DL

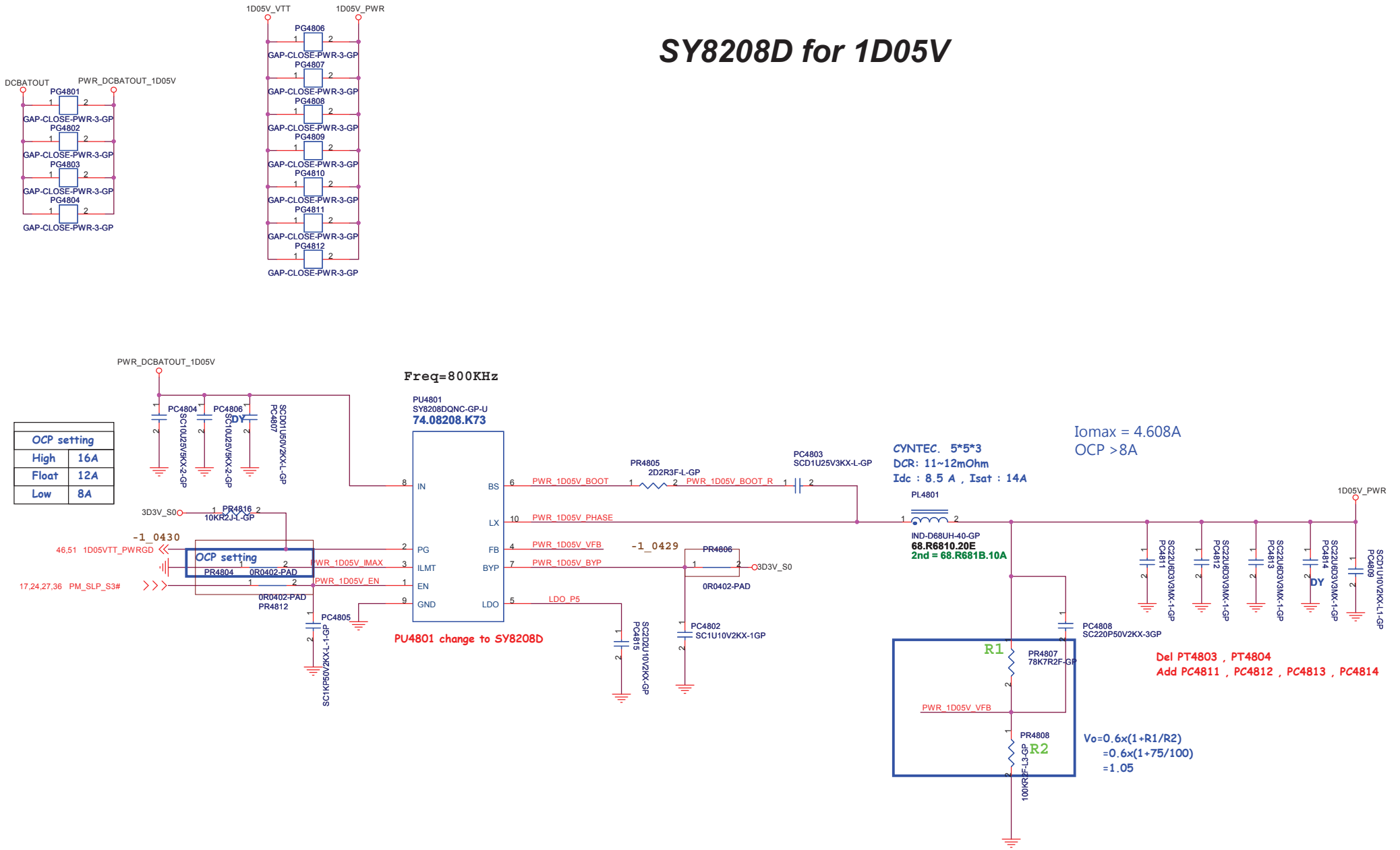


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<Variant Name>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
TPS51622_CPUCORE(2/2)			
Size	Document Number		Rev
A4	WEEBILL_HW		SB
Date:	Wednesday, September 18, 2013		Sheet 47 of 102

SY8208D for 1D05V



OCP setting	
High	16A
Float	12A
Low	8A

OCP setting	
PR4804	0R0402-PAD

Iomax = 4.608A
OCP > 8A

CYNTEC. 5*5*3
DCR: 11~12mOhm
Idc : 8.5 A , Isat : 14A

Del PT4803 , PT4804
Add PC4811 , PC4812 , PC4813 , PC4814

$$V_o = 0.6 \times (1 + R1/R2) = 0.6 \times (1 + 75/100) = 1.05$$

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<Variant Name>

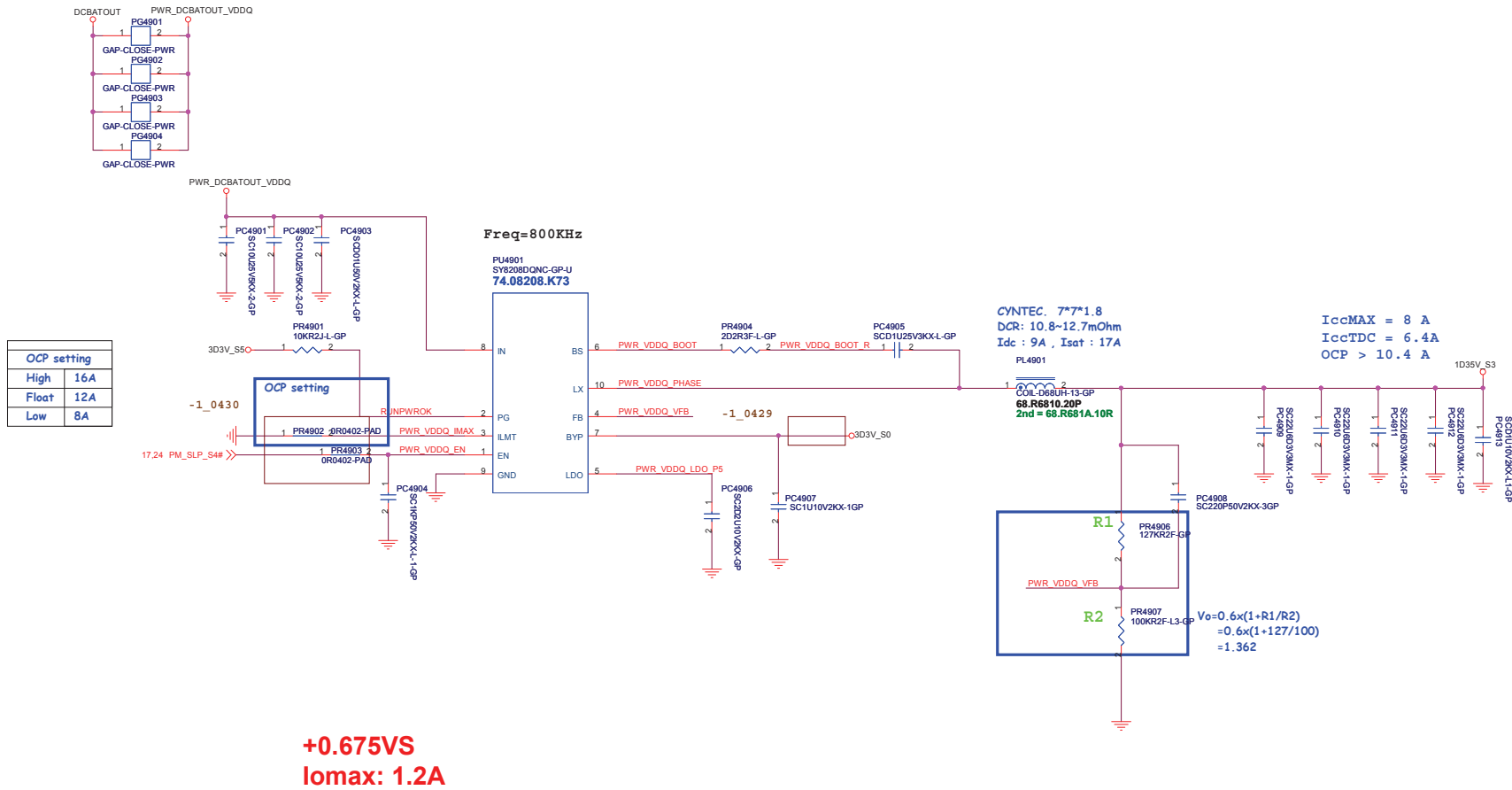
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **DC to DC 1D05V(SY8208D)**

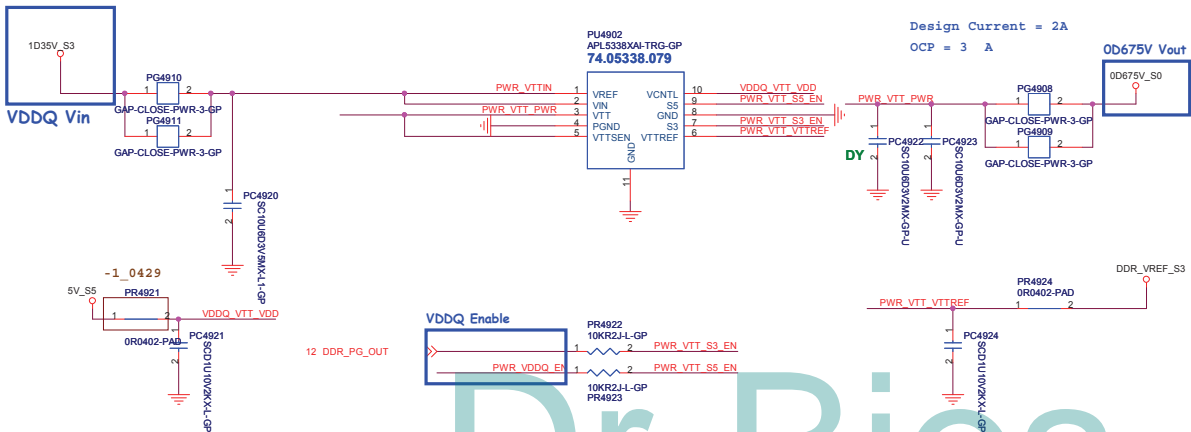
Size A3 Document Number **WEEBILL HW** Rev **SA**

Date: Wednesday, September 18, 2013 Sheet 48 of 102

SSID = PWR.Plane.Regulator_lp35v0p675v



+0.675VS
Iomax: 1.2A



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Wistron Corporation	
21F, 88, Sec.1, Hei Tai Wu Rd., Hsiehch, Taipei Hsien 221, Taiwan, R.O.C.	
Title	SY8208D+G2997(VDDQ VTT)
Size	Custom
WEEBILL HW SA	
Date	Wednesday, September 18, 2013
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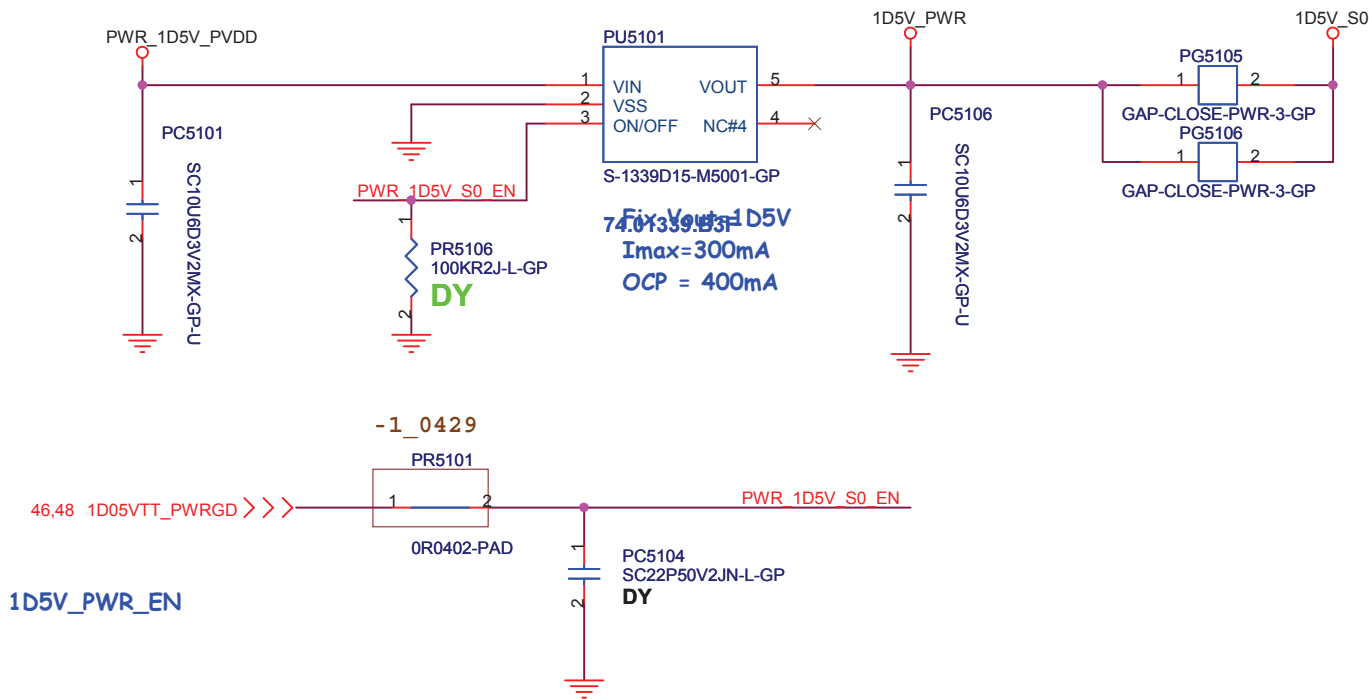
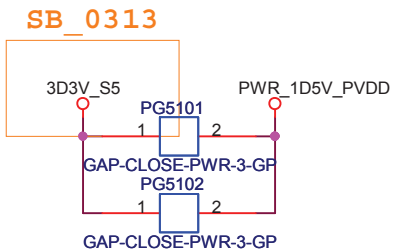
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<Variant Name>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		<i>iSSD power</i>	
Size	Document Number	Rev	
A4	WEEBILL_HW	SA	
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SYW232 for 1D5V_S0

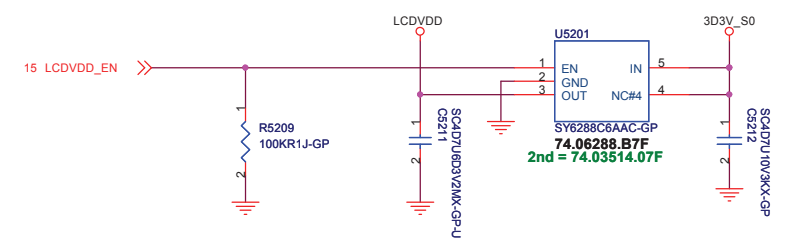
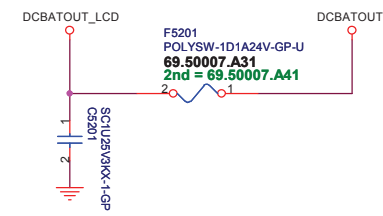
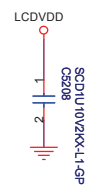
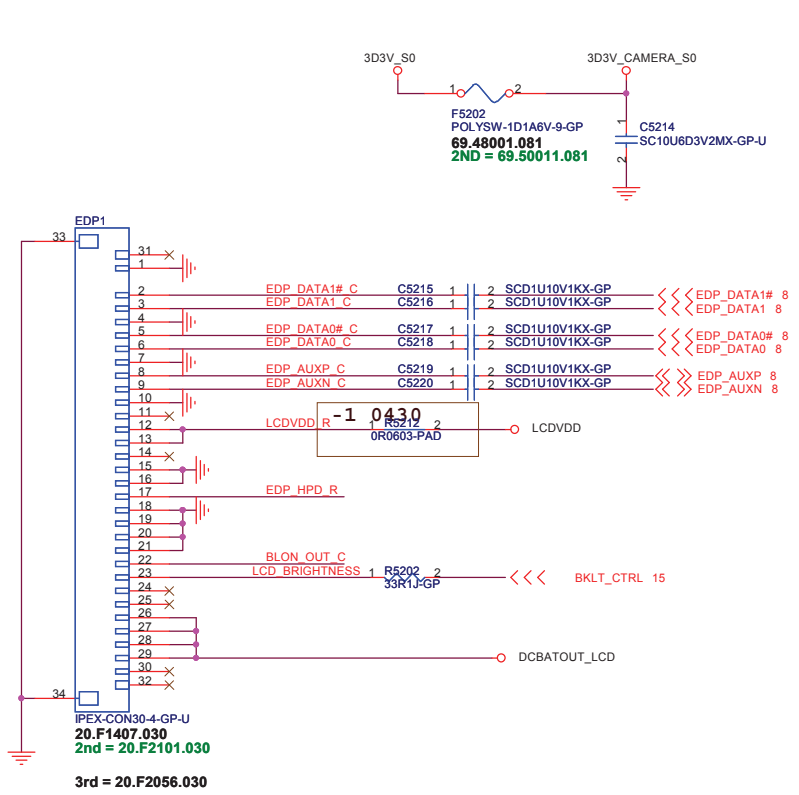


<Variant Name>

緯創資通 **Wistron Corporation**
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title		1D5V_S0 SYW232	
Size	Document Number	Rev	
A4	WEEBILL_HW	SA	
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<p><Variant Name></p> <p>緯創資通 Wistron Corporation</p> <p>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</p>		
<p>Title LCD Connector</p>		
Size A3	Document Number WEEBILL HW	Rev SA
Date: Wednesday, September 16, 2013	Sheet 52	of 102

Blanking

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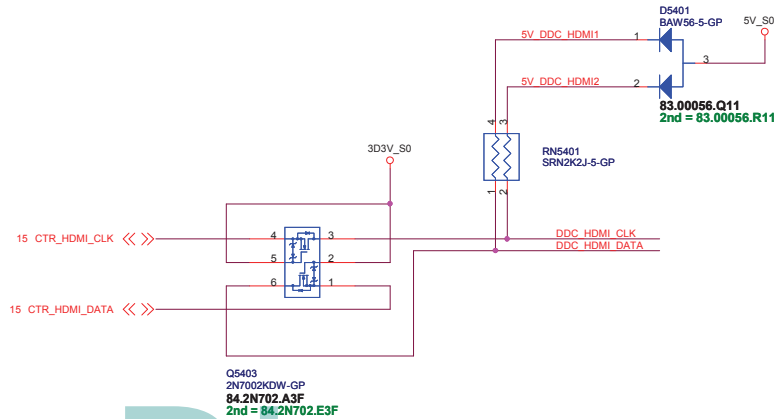
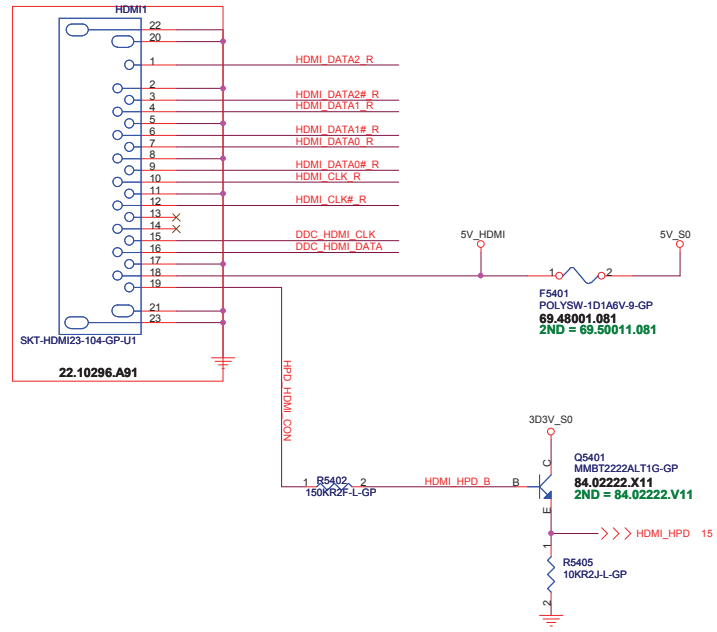
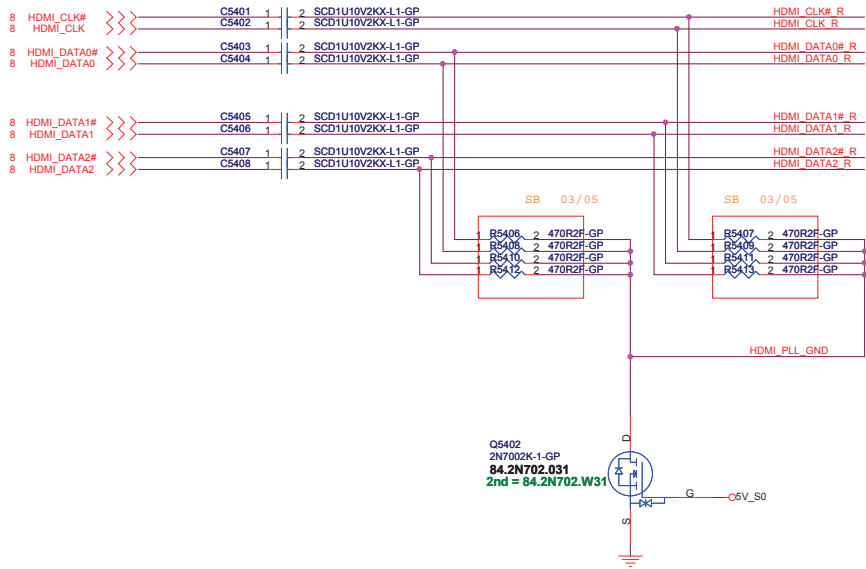
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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **CRT Board Connector**

Size A4 Document Number **WEEBILL_HW** Rev **SA**

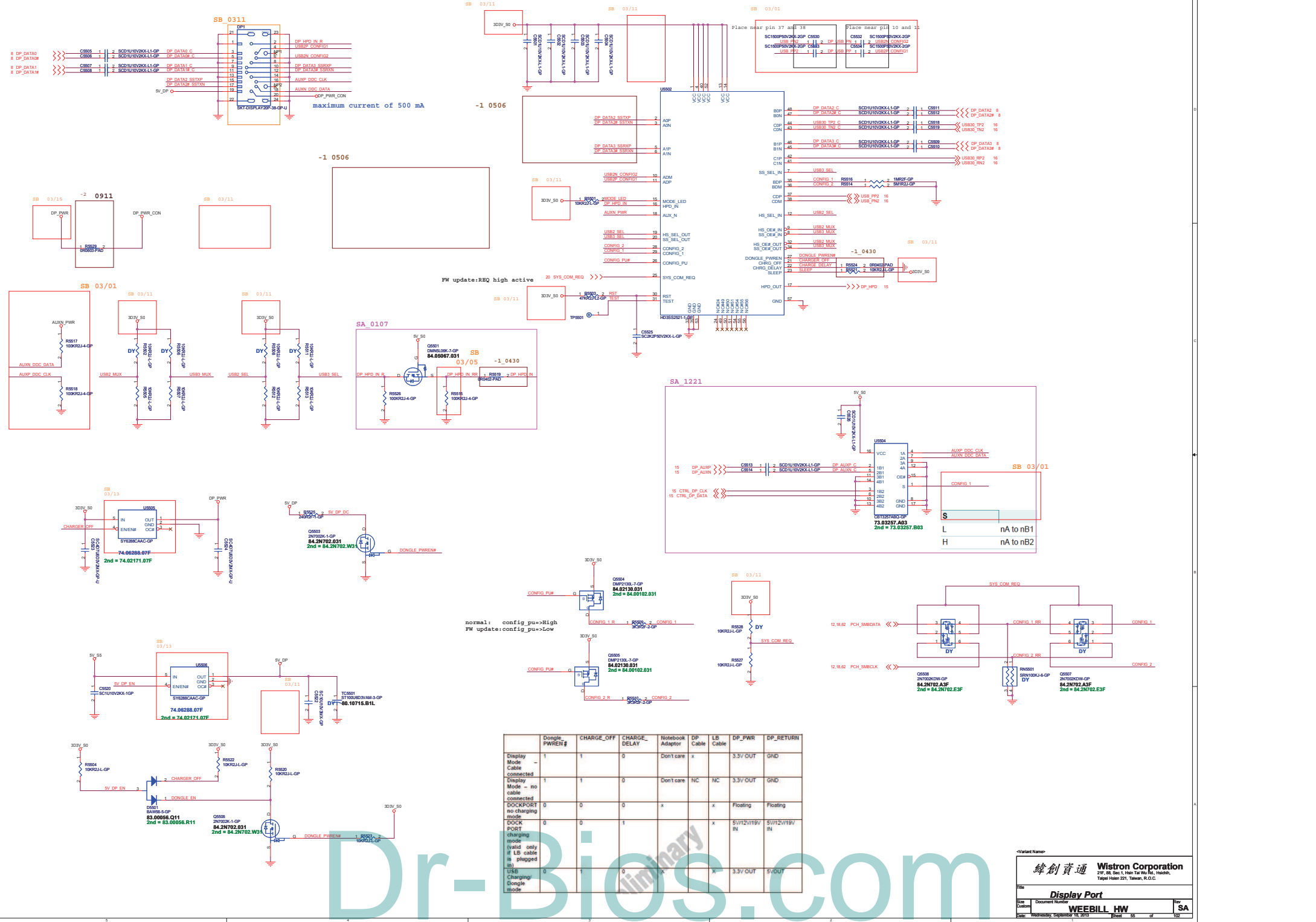
Date: Wednesday, September 18, 2013 Sheet 53 of 102



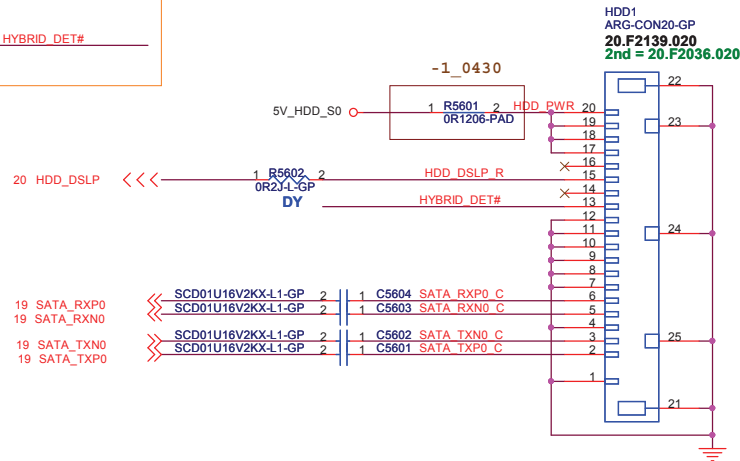
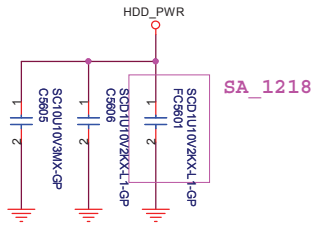
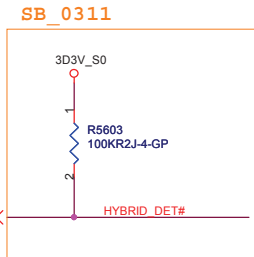
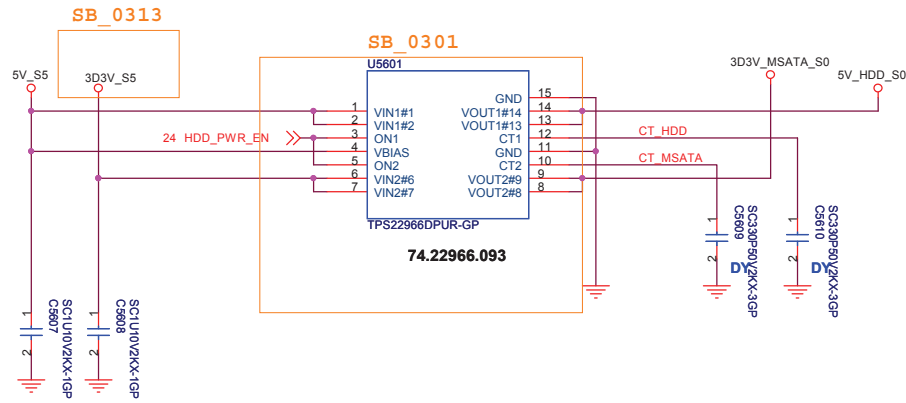
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Title		
HDMI Level Shifter/Connector		
Size	Document Number	Rev
Custom	WEEBILL HW	SA
Date:	Wednesday, September 18, 2013	Sheet 54 of 102

緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.



	Dongle PWREN#	CHARGE_OFF	CHARGE_DELAY	Notebook Adaptor	DP Cable	LB Cable	DP_PWR	DP_RETURN
Display Mode connected	1	1	0	Don't care	x		3.3V/OUT	GND
Cable connected	1	1	0	Don't care	NC	NC	3.3V/OUT	GND
Display Mode - no cable connected	1	1	0	Don't care	NC	NC	3.3V/OUT	GND
DOCKPORT no-charging mode	0	0	0	x	x	Floating	Floating	Floating
DOCKPORT charging mode (valid only if LB cable is plugged in)	0	0	1		x	5V/12V/18V/IN	5V/12V/18V/IN	
USB Charging Dongle mode	0	1	0	x	x	3.3V/OUT	5V/OUT	



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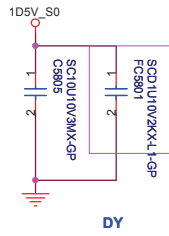
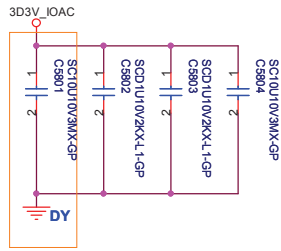
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<Variant Name>

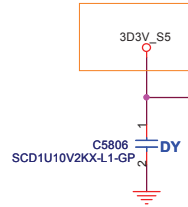
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
E-SATA			
Size	Document Number		Rev
A4	WEEBILL_HW		SA
Date:	Wednesday, September 18, 2013		Sheet 57 of 102

SB 0322

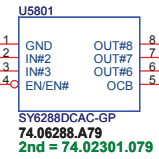


SB 03/01

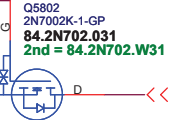
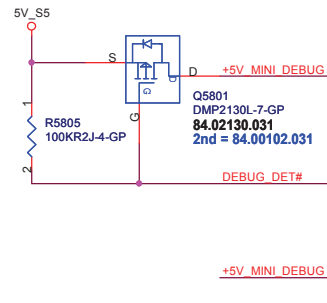
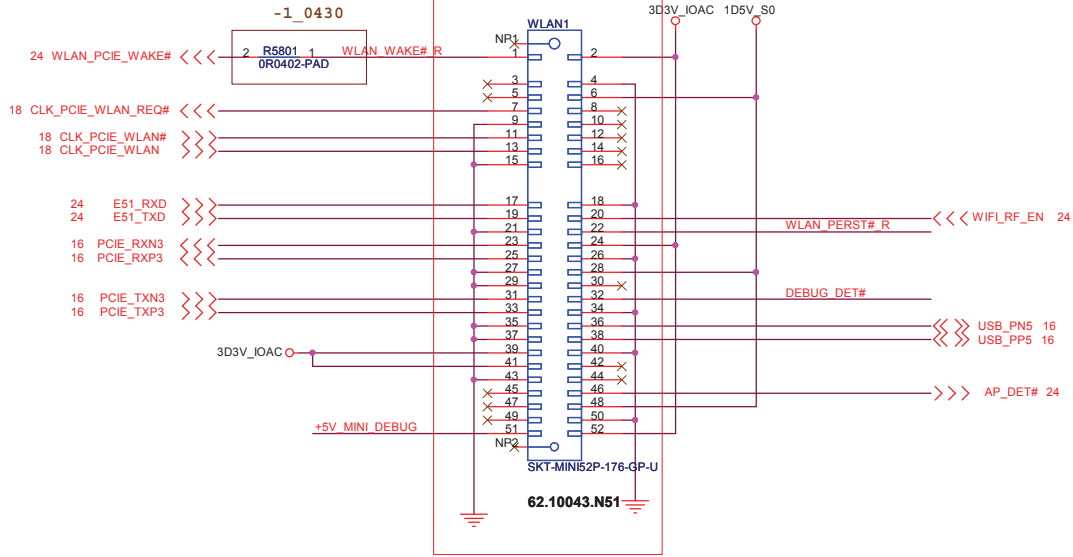
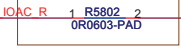
SB 0313



24 WLAN_PWR_EN# >>>



-1 0430



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Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hstchih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MINICARD(WLAN)		
Size A3	Document Number: WEEBILL_HW	Rev: SA
Date: Wednesday, September 18, 2013	Sheet 58	of 102

5

4

3

2

1

D

D

C

C

B

B

A

A

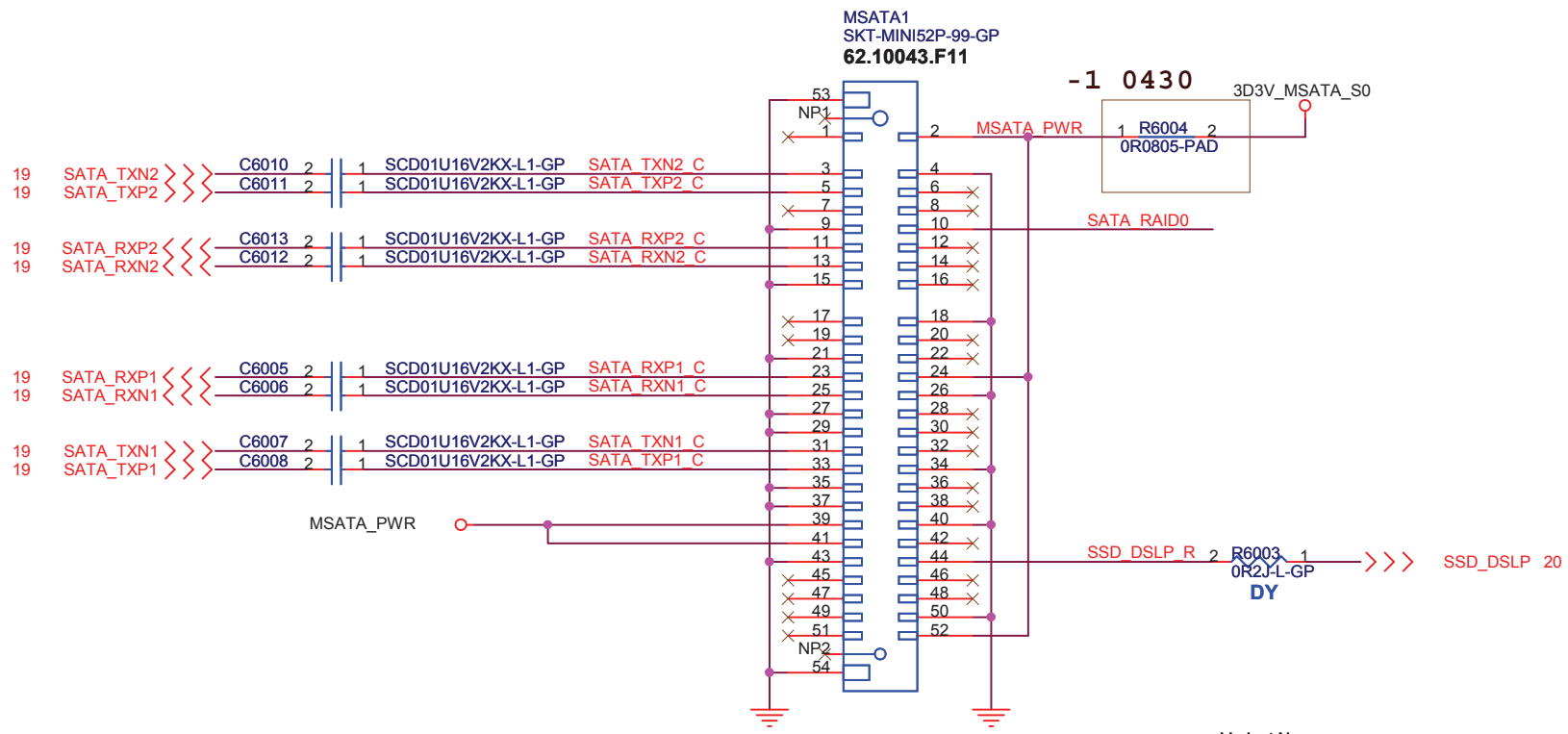
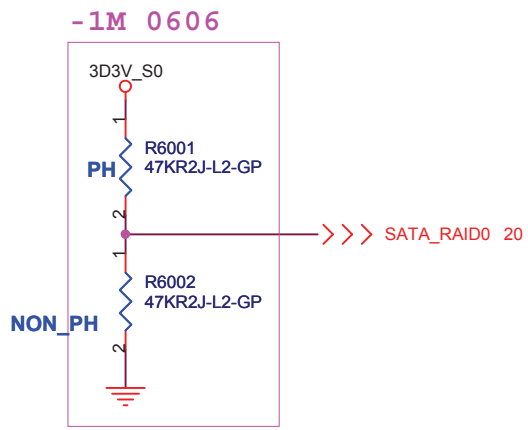
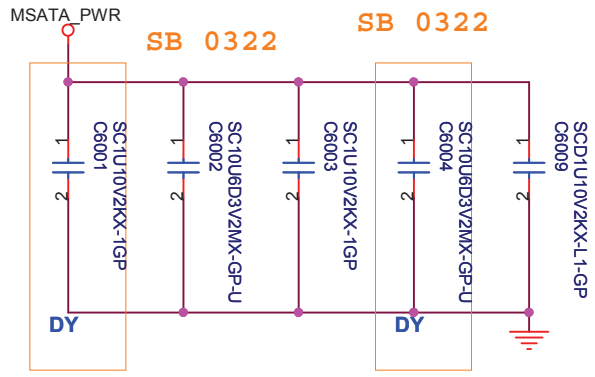
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<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
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Title		WWAN CONN	
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Size	Document Number	Rev
A4	WEEBILL_HW	SA



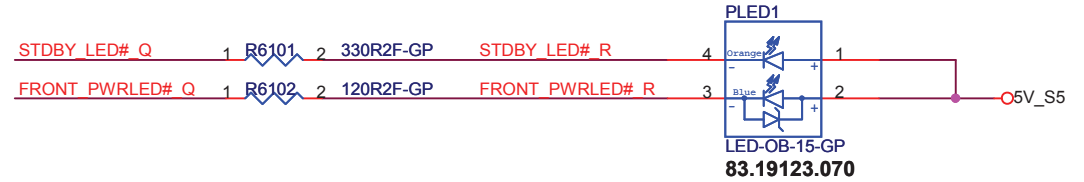
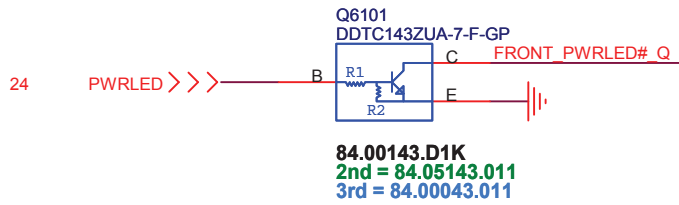
<Variant Name>


Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

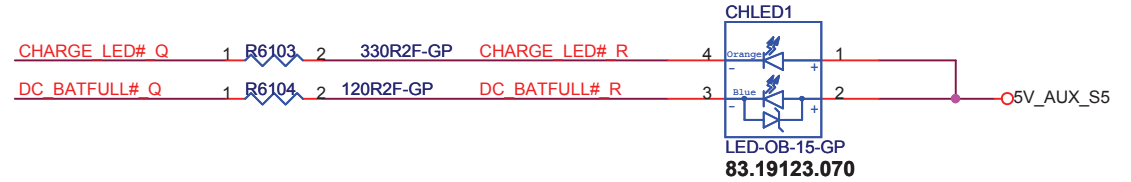
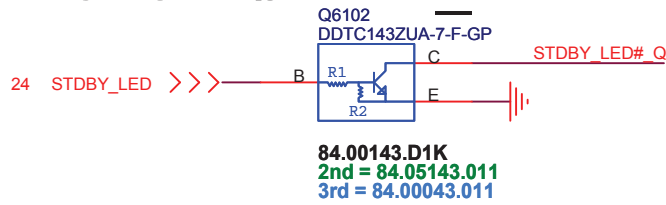
Title			mSATA Connector		
Size	Document Number				Rev
A4	WEEBILL_HW				SA
Date:	Wednesday, September 18, 2013		Sheet	60	of 102

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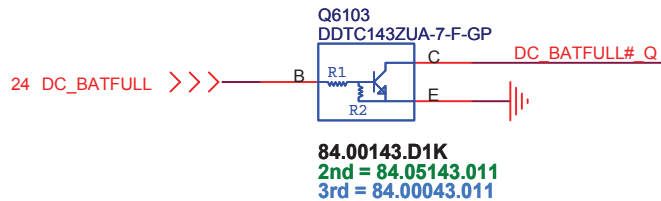
Power LED



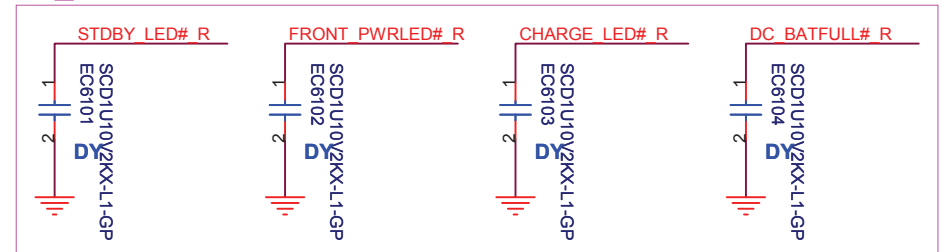
Power STDBY_LED



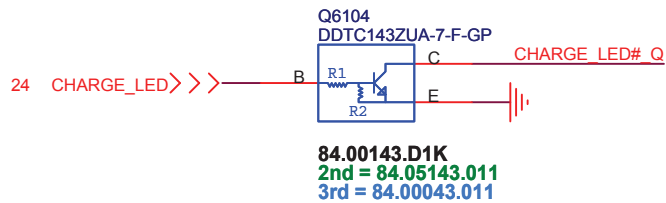
Battery LED (DC_BATFULL)



SA_1224



Battery LED (CHARGE)



<Variant Name>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

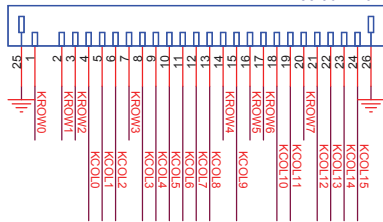
Title LED Bard/Power Button		
Size A4	Document Number WEEBILL_HW	Rev SA
Date: Wednesday, September 18, 2013	Sheet 61	of 102

Dr-Bios.com

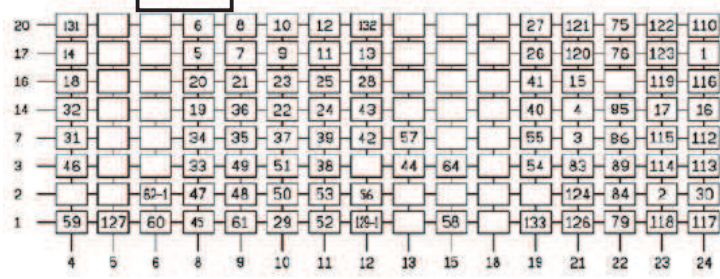
Internal Keyboard Connector

下接觸

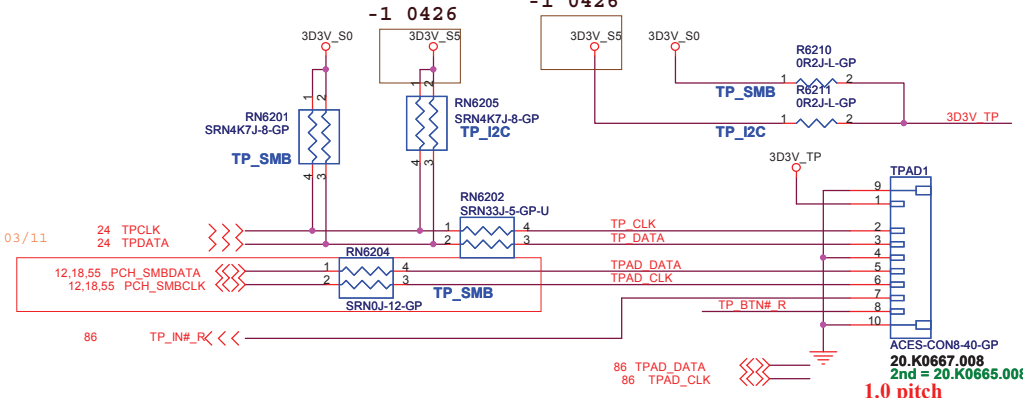
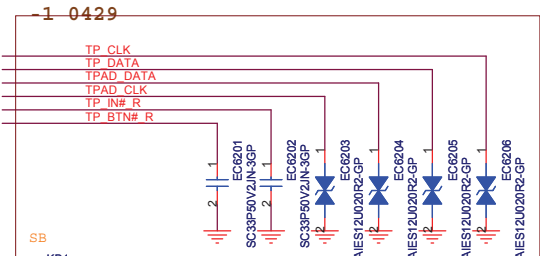
20.K0785.024
2nd = 20.K0786.024



up side



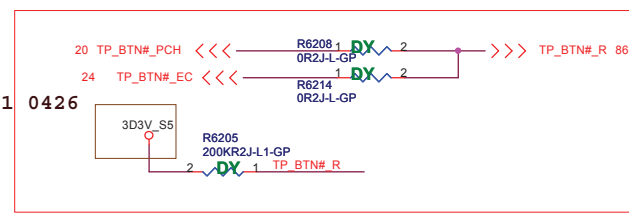
<<< KROW[0..7] 24,86
>>> KCOL[0..15] 24,86



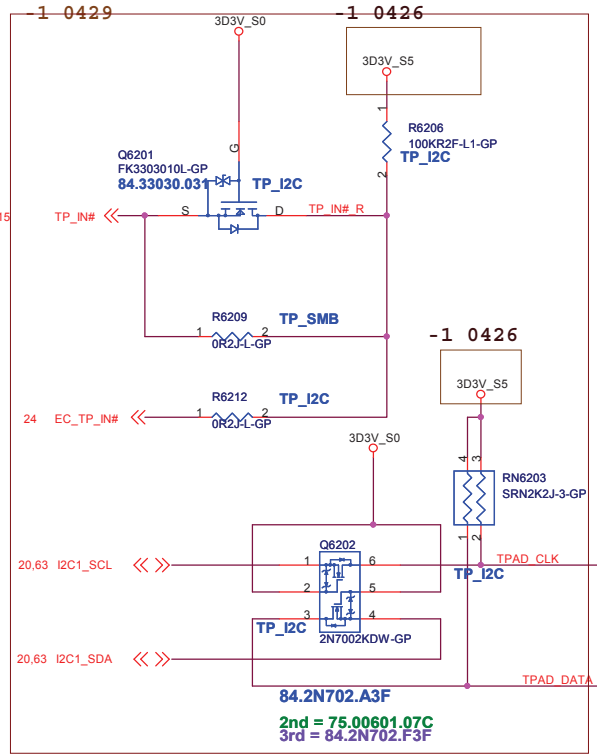
1.0 pitch

下接觸

SB 03/11



86 TP_DATA >>>
86 TP_CLK >>>



84.2N702.A3F
2nd = 75.00601.07C
3rd = 84.2N702.F3F

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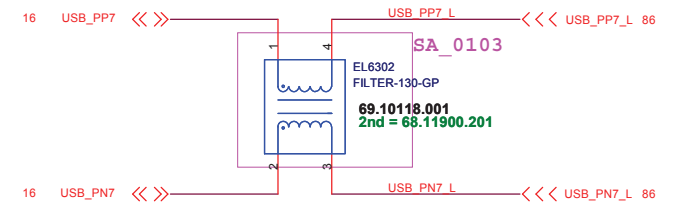
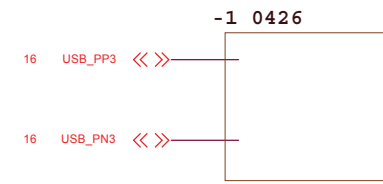
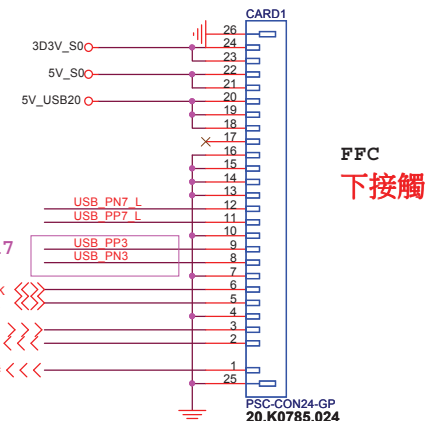
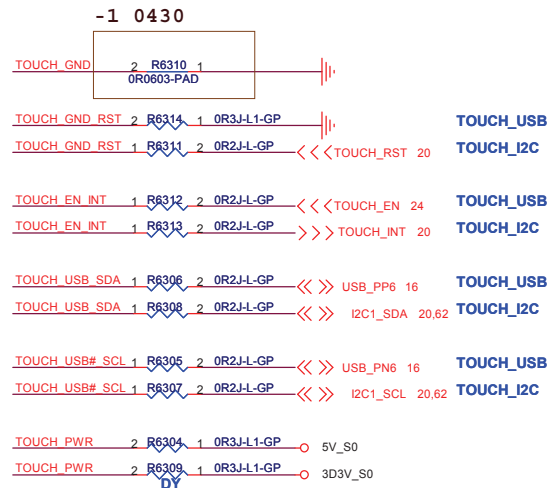
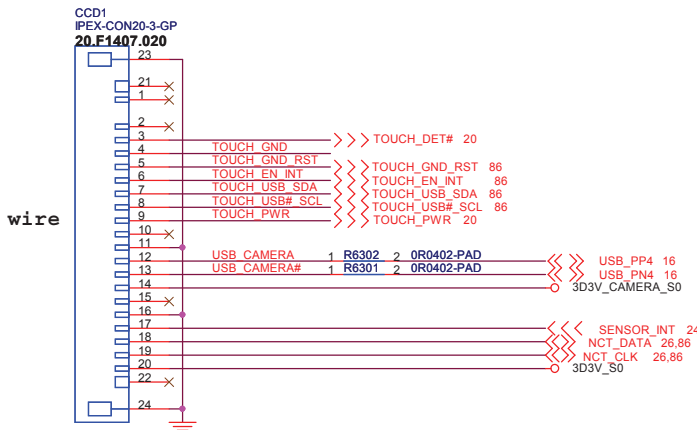
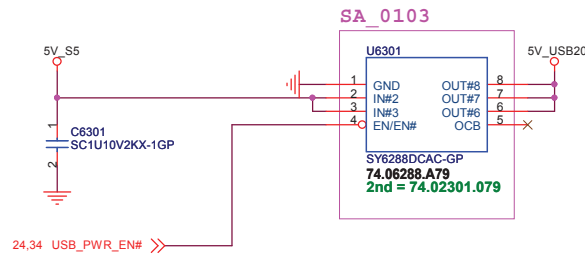
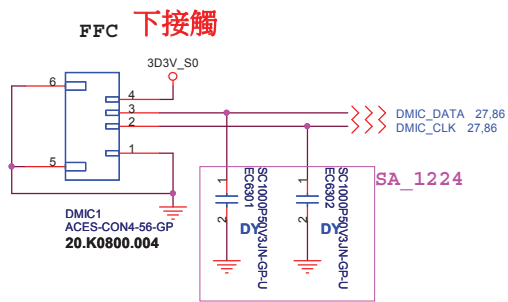
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hstchih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Key Board/Touch Pad**

Size A3 Document Number: **WEEBILL_HW** Rev: **SA**

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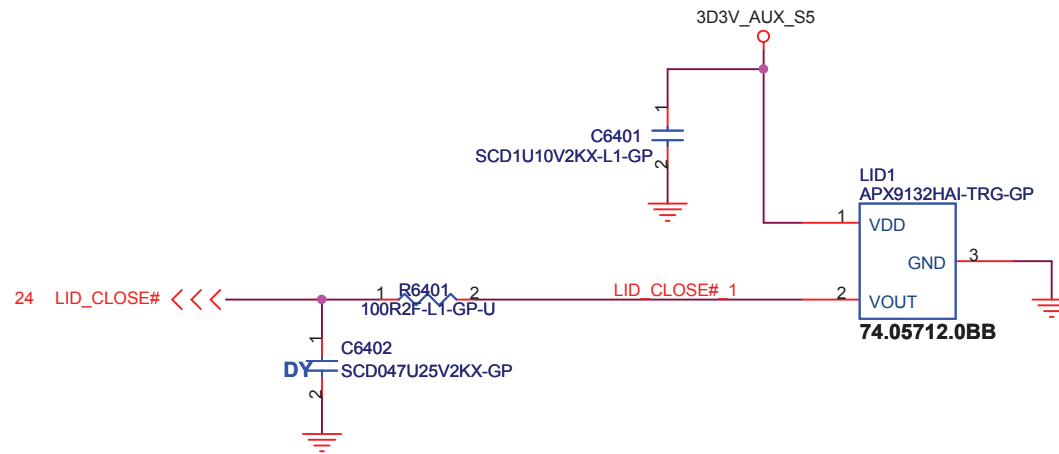
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緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hstchih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **IO Board Connector**

Size A3 Document Number: **WEEBILL_HW** Rev: **SA**

Date: Wednesday, September 18, 2013 Sheet 63 of 102



<Variant Name>

緯創資通

Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title

Hall Sensor

Size

Document Number

Rev

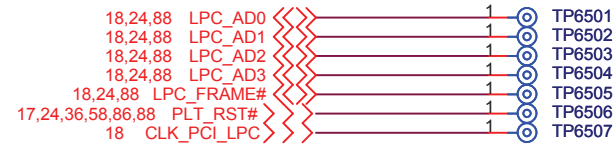
WEEBILL_HW

SA

Date: Wednesday, September 18, 2013

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<Variant Name>

緯創資通

Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title

Dubug connector

Size
A4

Document Number

WEEBILL_HW

Rev
SA

Date: Wednesday, September 18, 2013

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Blanking

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<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **SENSOR HUB**

Size A4 Document Number **WEEBILL_HW** Rev **SA**

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Free Fall Sensor

Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

Blanking

```
SDO="H"; address="3Ah"  
*SDO="L"; address="38h"
```

```
*CS="H"; mode="I2C"  
CS="L"; mode="SPI"
```

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

G Sensor

Size

Document Number

Rev

A4

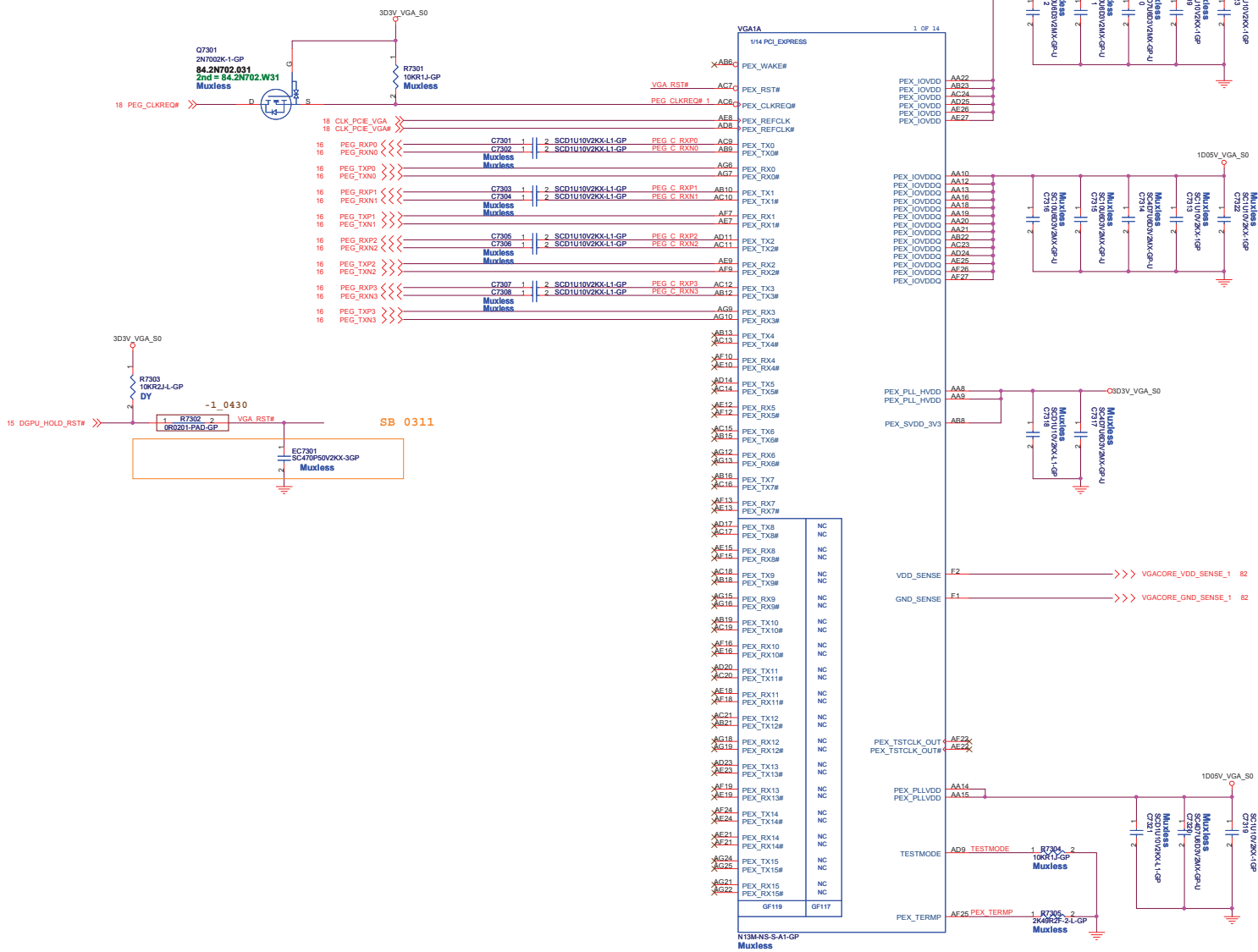
WEEBILL_HW

SA

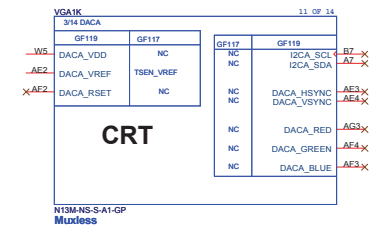
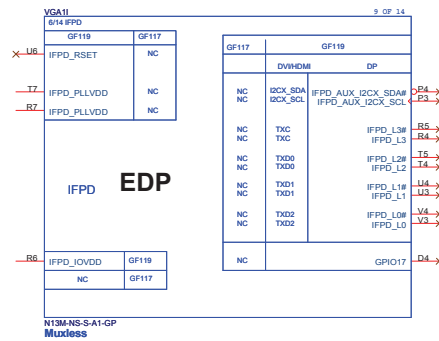
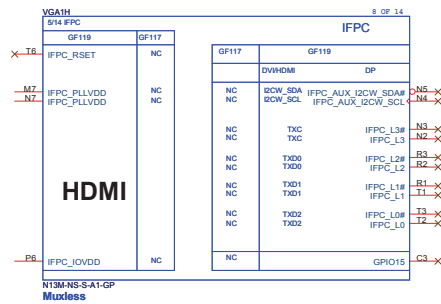
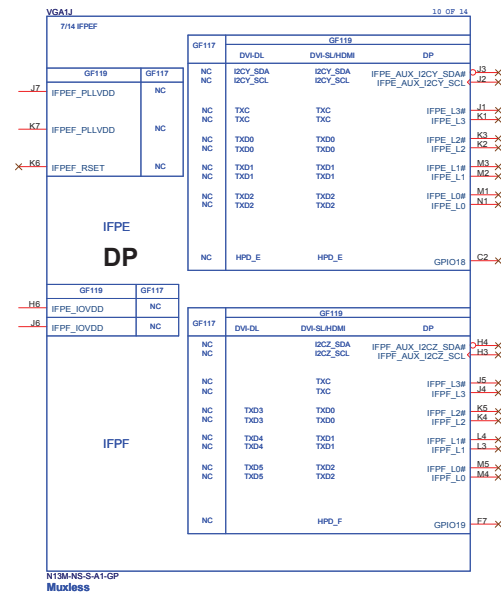
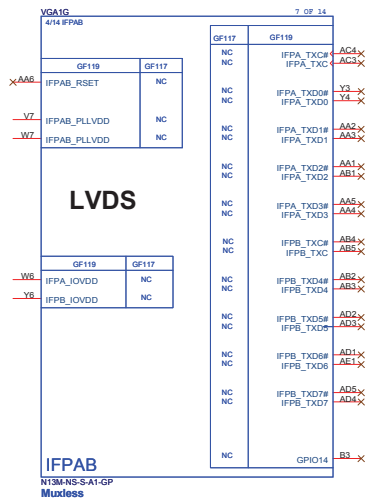
Date: Wednesday, September 18, 2013

Sheet 67 of 102

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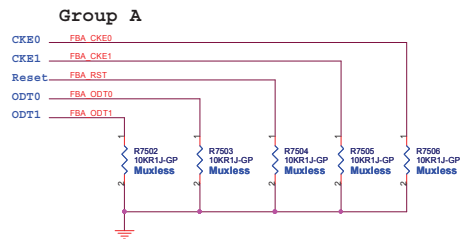
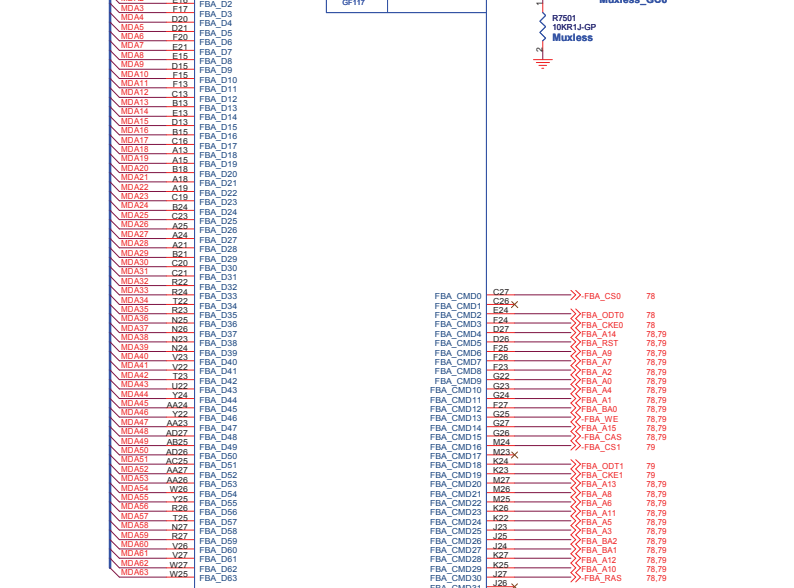


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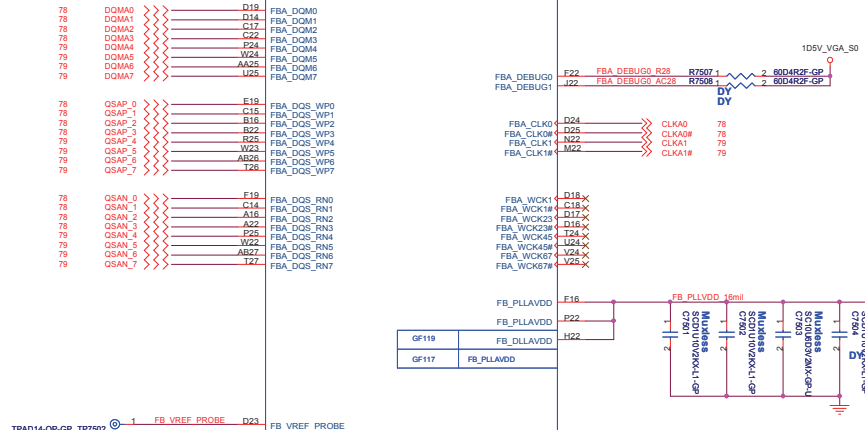


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78.79 MDAD0_63] << GF119 NC FB_CLAMP GF117 FB_CLAMP GF119 NC FB_CLAMP GF117 FB_CLAMP



N14x DDR3 mode D	Data Bits [31:0]	Data Bits [63:32]
FbX_CMD11	A1	A1
FbX_CMD12	BA0	BA0
FbX_CMD13	WE*	WE*
FbX_CMD14	A15	A15
FbX_CMD15	CA5*	CA5*
FbX_CMD16		CS0*
FbX_CMD17		
FbX_CMD18		ODT
FbX_CMD19		CKE
FbX_CMD20	A13	A13
FbX_CMD21	A8	A8
FbX_CMD22	A6	A6
FbX_CMD23	A11	A11
FbX_CMD24	A5	A5
FbX_CMD25	A3	A3
FbX_CMD26	BA2	BA2
FbX_CMD27	BA1	BA1
FbX_CMD28	A12	A12
FbX_CMD29	A10	A10
FbX_CMD30	RA5*	RA5*
FbX_CMD31		



TPAD14-OP-GP TP7902 1 FB_VREF_PROBE D23 FB_VREF_PROBE N13MNS-A1-GP Muxless

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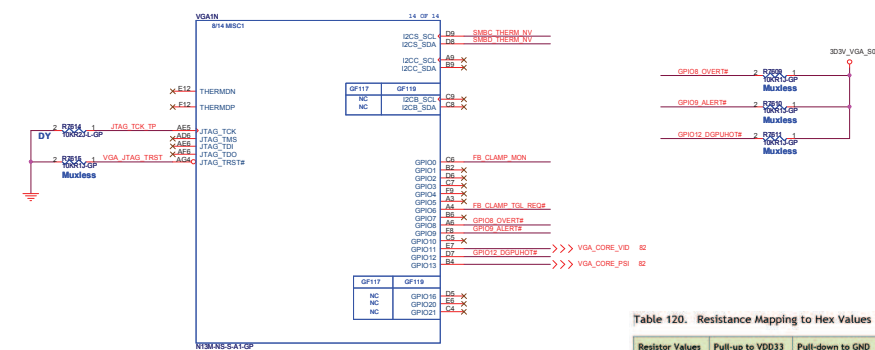
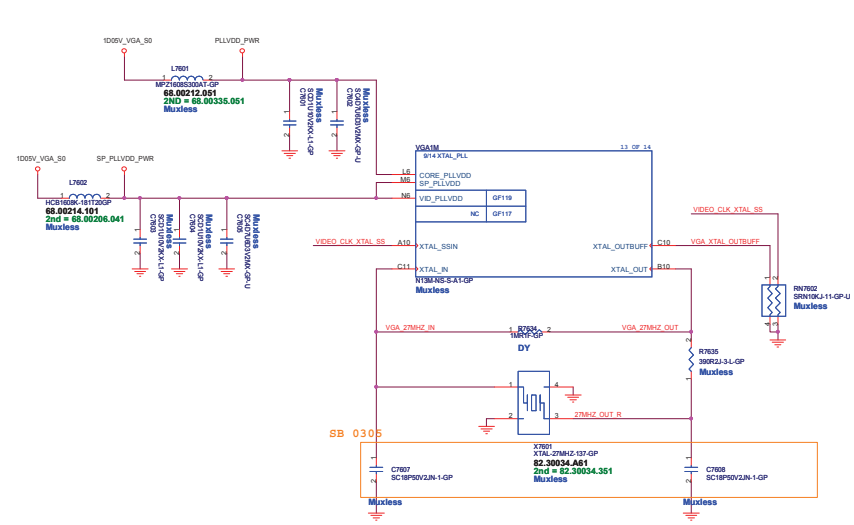
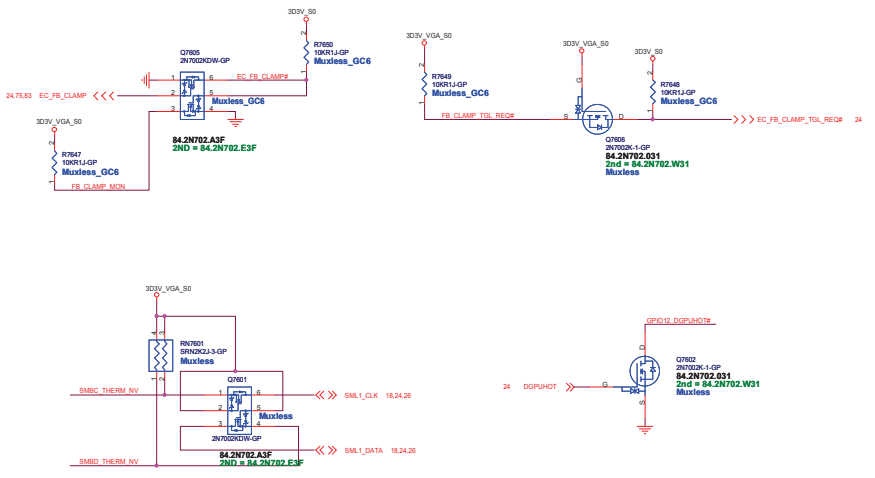


Table 120. Resistance Mapping to Hex Values

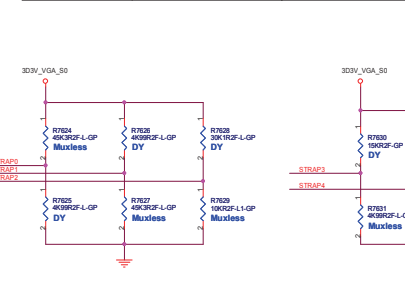
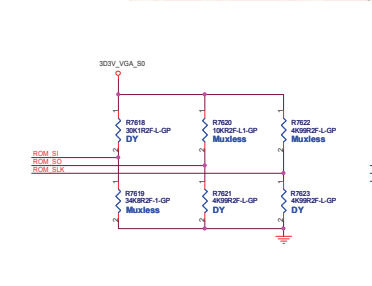
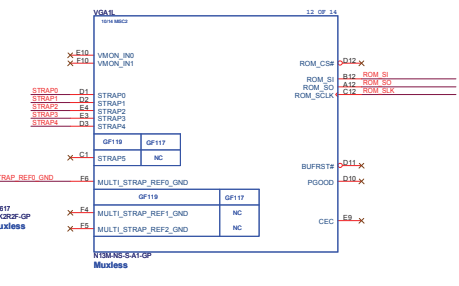
Resistor Values	Pull-up to VDD33	Pull-down to GND
4.99 k	1000	0000
10.0 k	1001	0001
15.0 k	1010	0010
20.0 k	1011	0011
24.9 k	1100	0100
30.1 k	1101	0101
34.8 k	1110	0110
45.3 k	1111	0111

VRAM Table(N14M-LP)

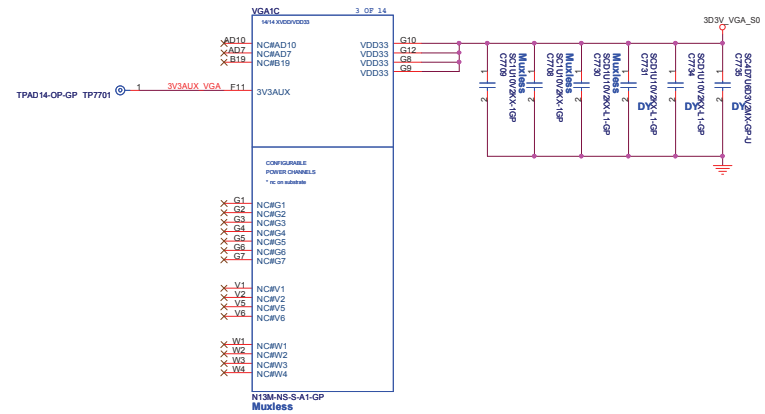
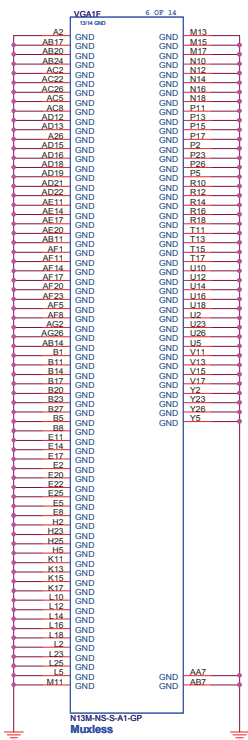
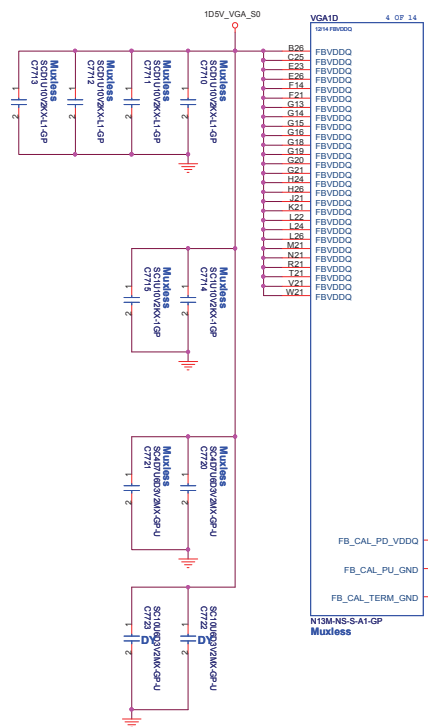
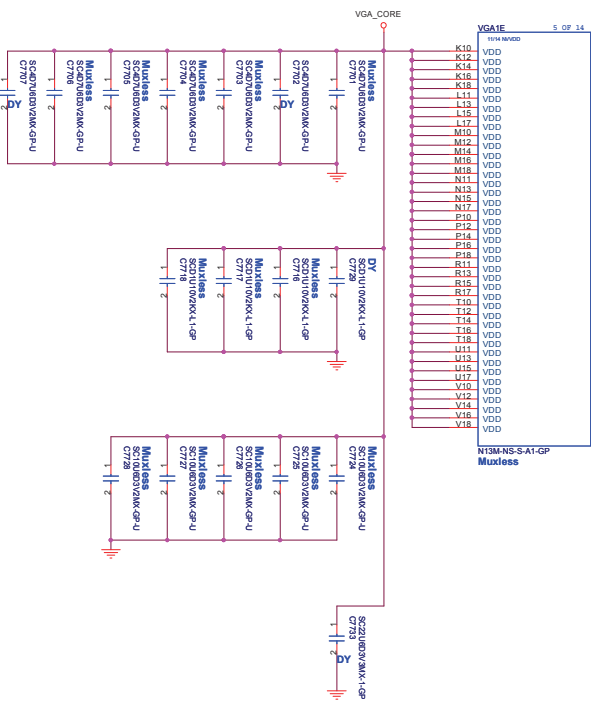
	Hynix 2G 0110(0x6) H5T2CG	Hynix 2G 0100(0x4) H5T2CG
ROM_SI	34.8Kohm 64.34825.GDL	24.9Kohm 64.24925.GDL

Table 114. GB2-64 and GB4-128 GPIO Description

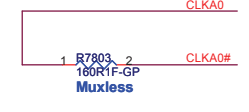
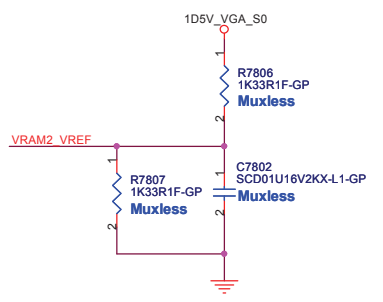
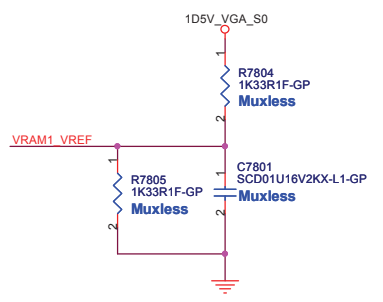
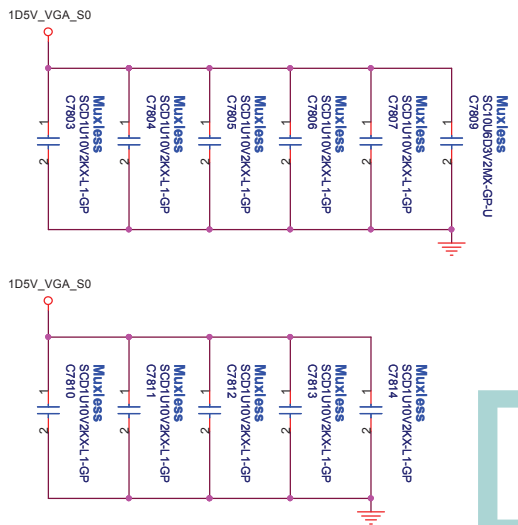
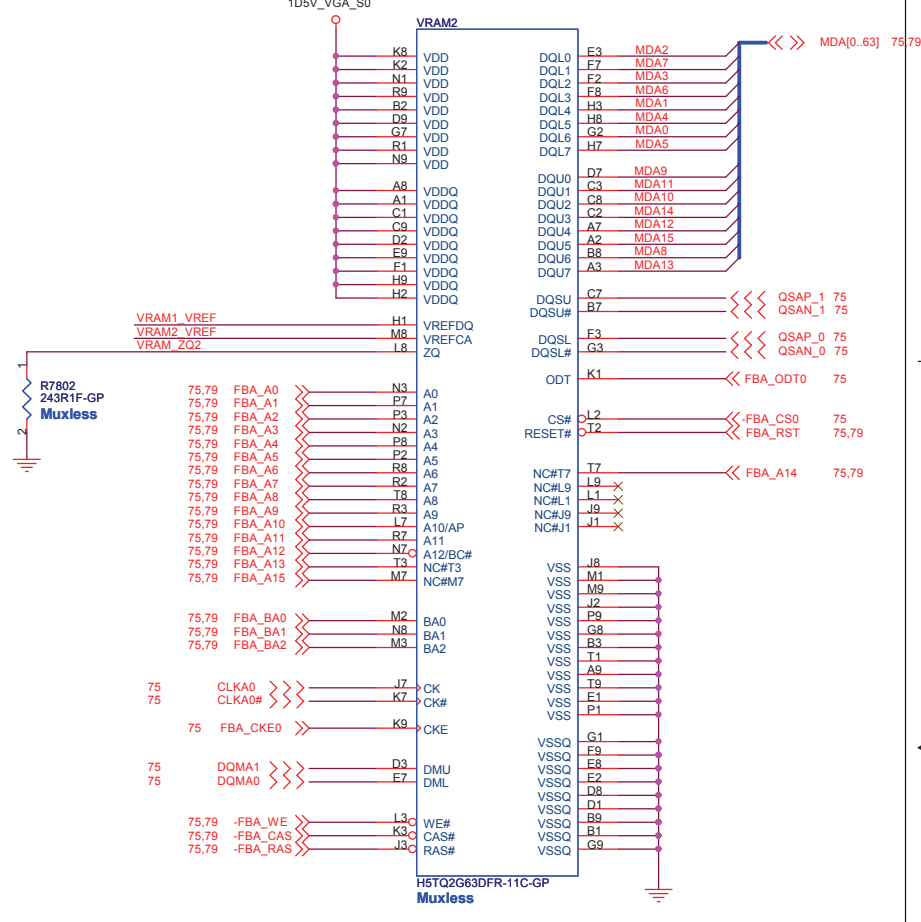
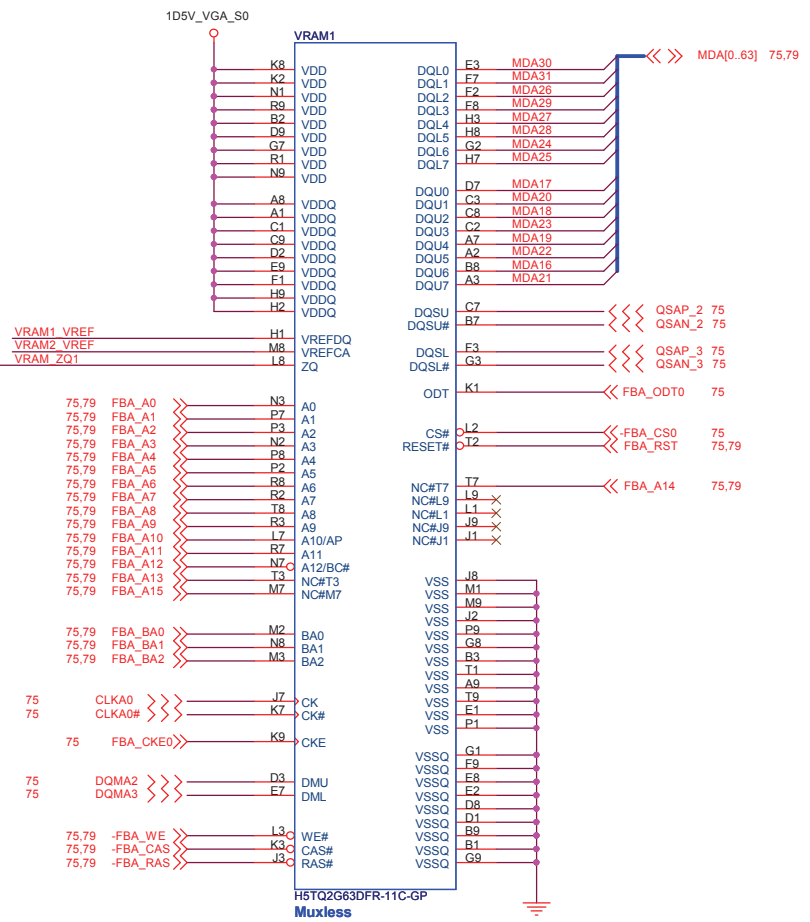
Pin Name	Normal Function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	FB_CLAMP_MON	I	FB Clamp monitor	
GPIO1	MEM_VDD_CTL	O	Memory VDD VID	MEM VID: Strap to boot FBVDD/Q
GPIO2	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control	100 K pull-down
GPIO3	LCD_VCC	O	Panel Power Enable	LCD_VCC: 100k pull-down
GPIO4	LCD_BLEH	O	Panel Backlight Enable	100 K pull-down
GPIO5	Reserved			
GPIO6	FB_CLAMP_TGL_REQ	O	Active low FB Clamp toggle request	
GPIO7	3DVision	O	3D Vision L/R signal	100 K pull-down
GPIO8	OVERT	I/O	Active Low Thermal Catastrophic Over Temperature	100 K pull-up
GPIO9	ALEXT	I/O	Active Low Thermal Alert	100 K pull-up
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100 K pull-down
GPIO11	PWM_VID	O	GPU Core VDD PWM control signal	
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100 K pull-up
GPIO13	PSI	O	Phase Shedding	PSI: 10k pull-up to enable two phase.
GPIO14	HPD_A	I	Hot Plug Detect for IFFA used as DisplayPort or for IFFA3 when used as Dual Link DVI	See Figure 73
GPIO15	HPD_C	I	Hot Plug Detect for IFFC	See Figure 73
GPIO16	FRM_LCK	O	JT Frame Lock signal	See Figure 73
GPIO17	HPD_D	I	Hot Plug Detect for IFFD	See Figure 73
GPIO18	HPD_E	I	Hot Plug Detect for IFFE	See Figure 73
GPIO19	HPD_F or HPD_B	I	Hot Plug Detect for IFFB or for IFFB used as DisplayPort	See Figure 73
GPIO20	Reserved			
GPIO21	Reserved			



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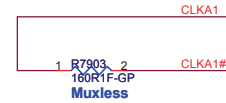
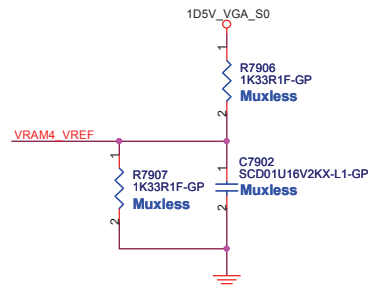
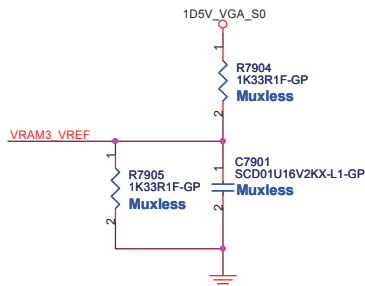
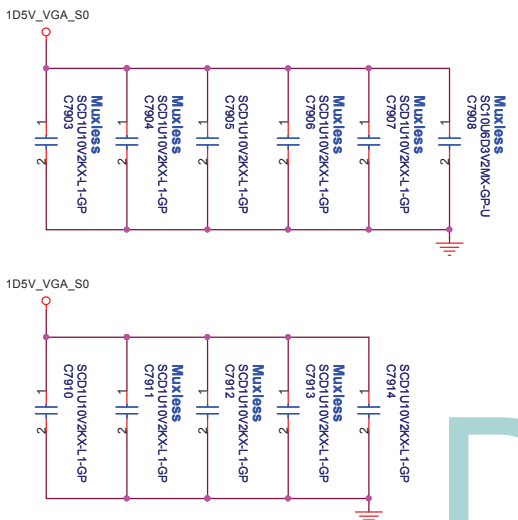
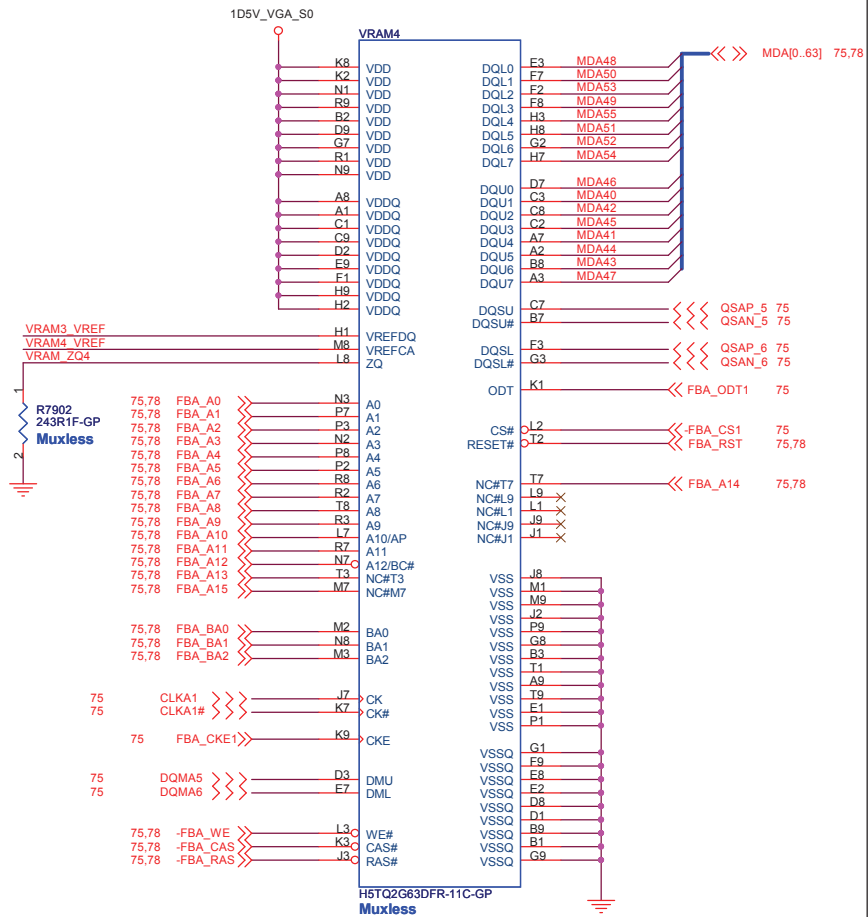
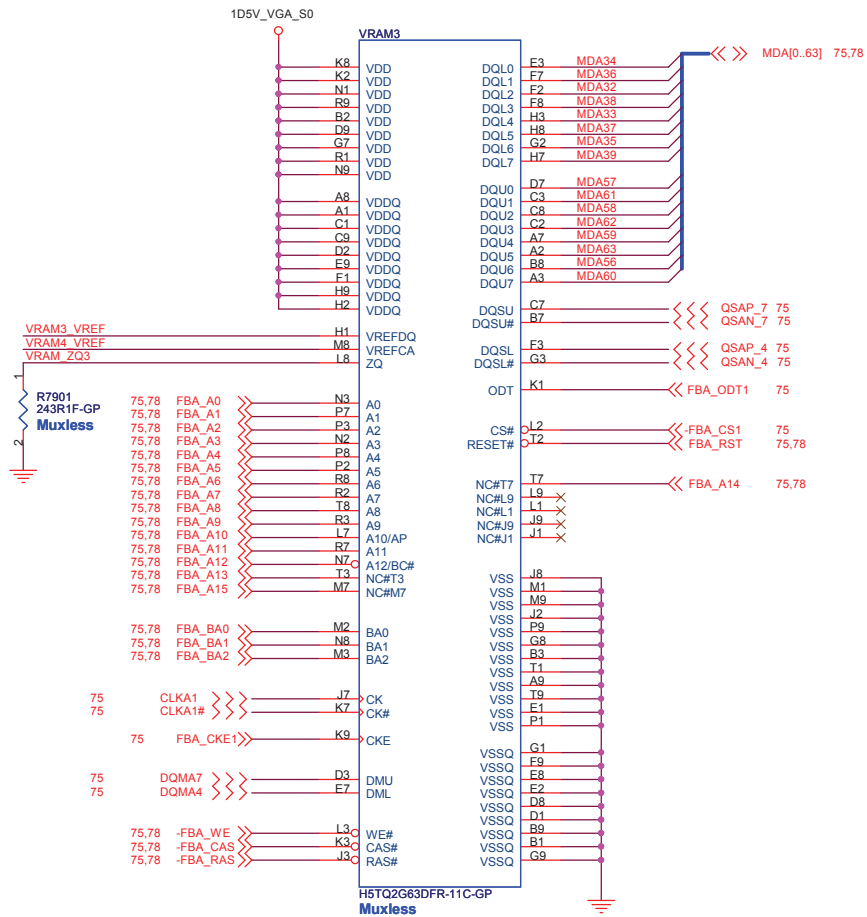
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Title: **GPU-VRAM1,2 (1/4)**

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Title: **GPU-VRAM3,4 (2/4)**

Size A3 Document Number: **WEEBILL HW** Rev: **SA**

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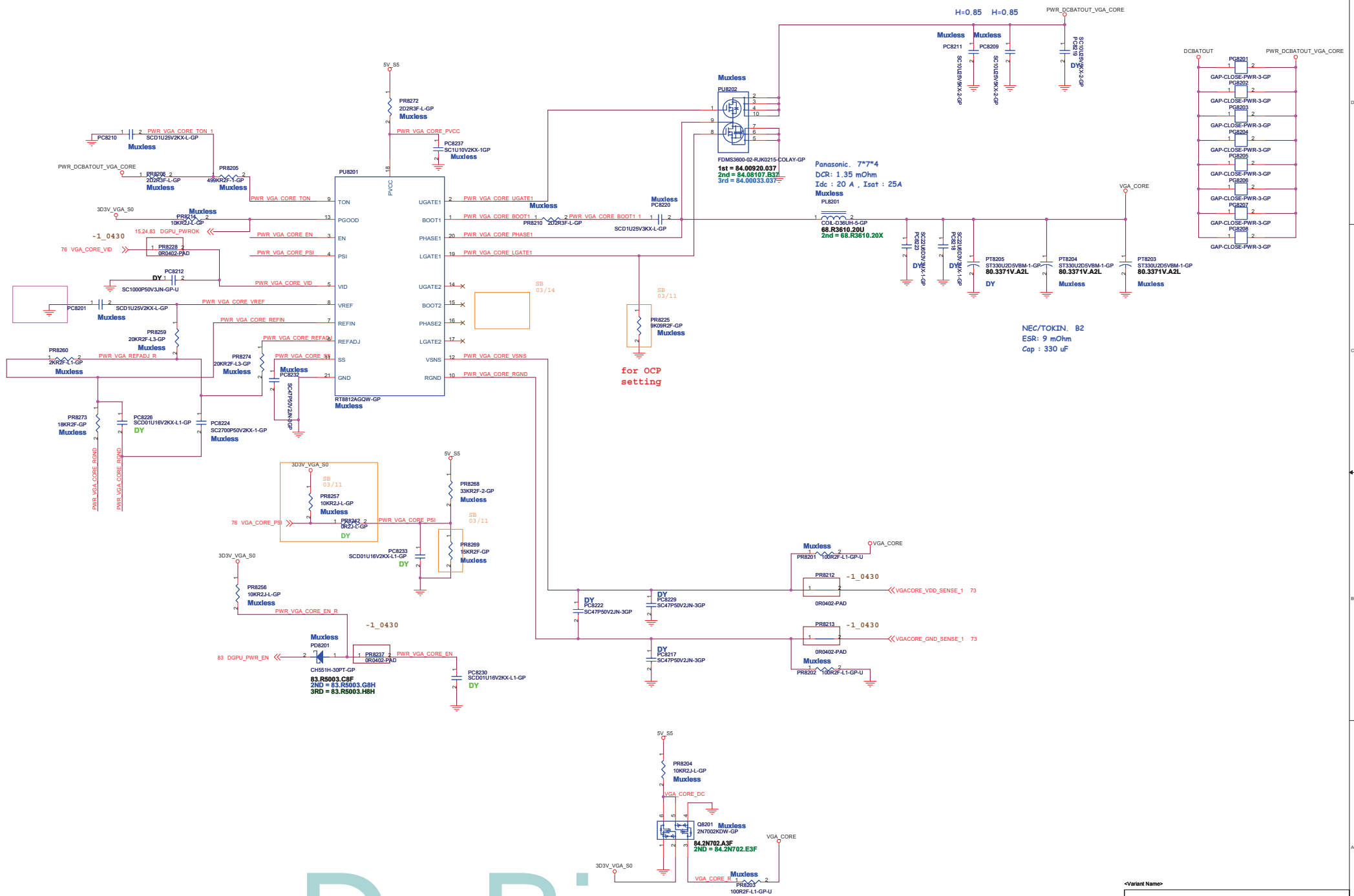
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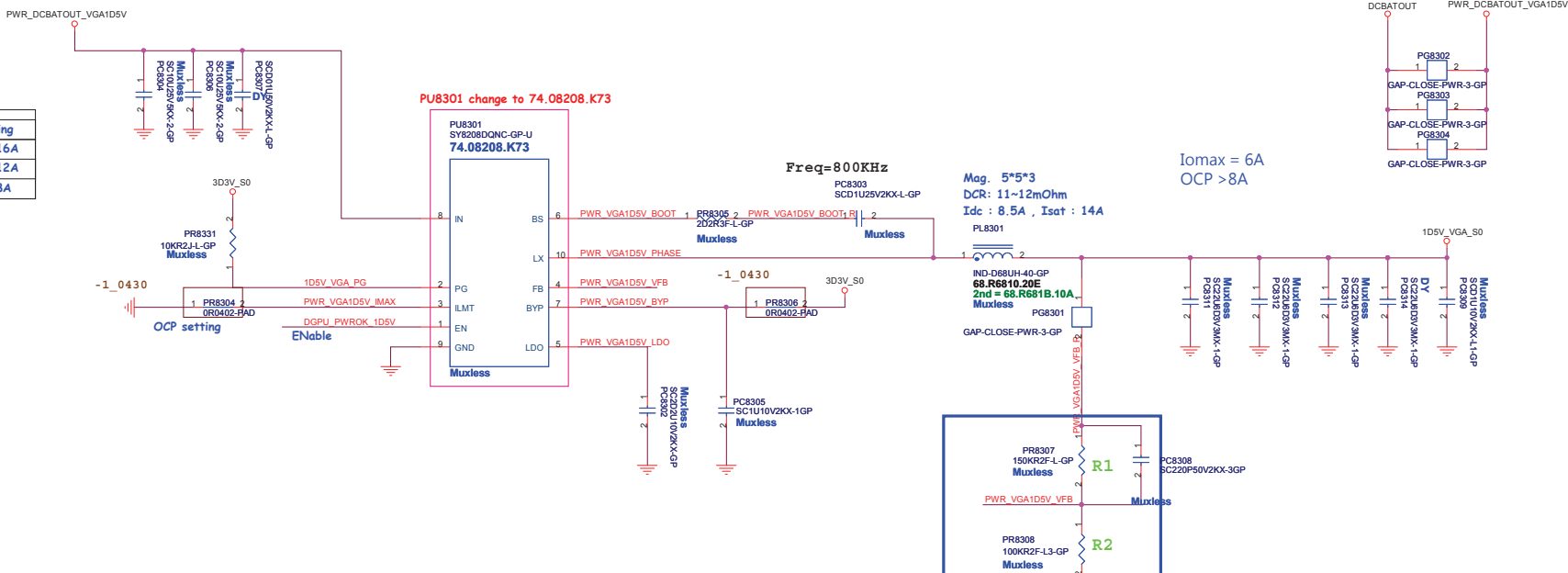
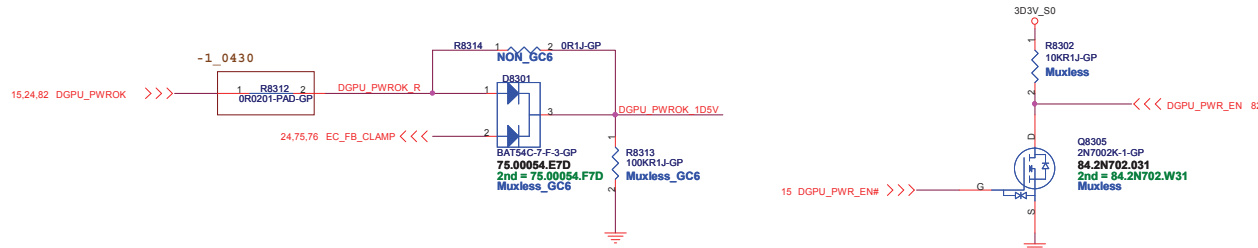
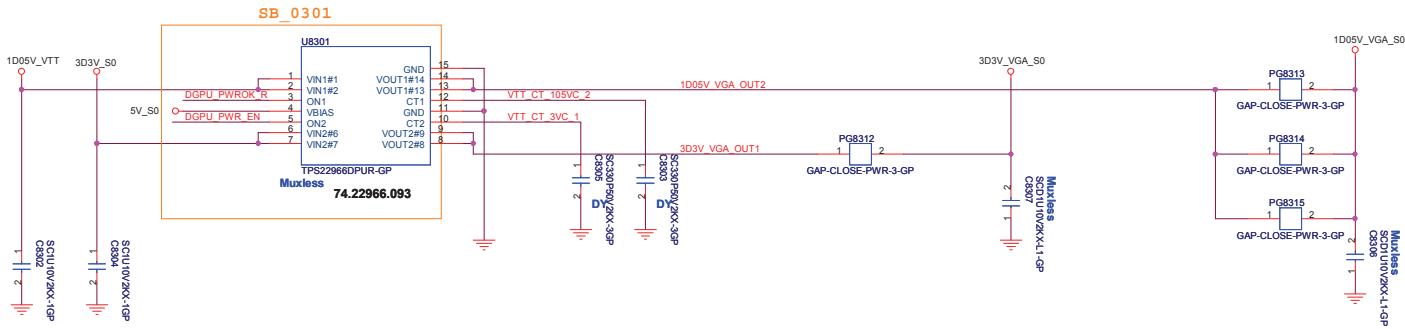
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OCP setting	
High	16A
Float	12A
Low	8A

$$V_o = 0.6 \times (1 + R1/R2) = 0.6 \times (1 + 150/100) = 1.5$$

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Title: **DISCRETE VGA POWER**

Size: Custom Document Number: **WEEBILL_HW** Rev: **SA**

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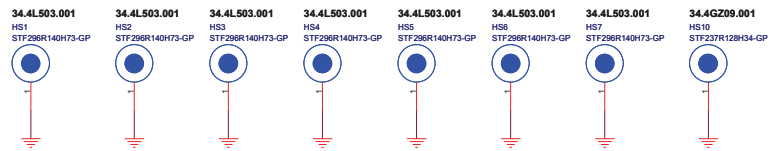
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Taipei Hsien 221, Taiwan, R.O.C.

Title **Switchable GFX LCD(1/2)**

Size A4 Document Number **WEEBILL_HW** Rev **SA**

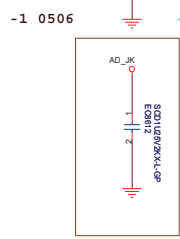
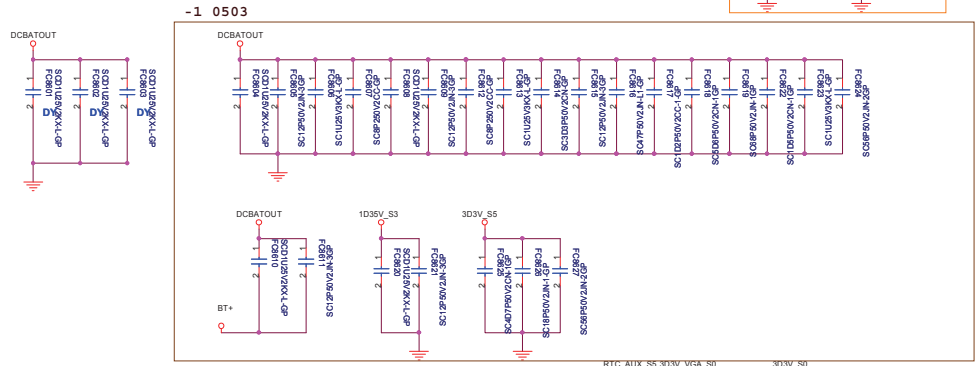
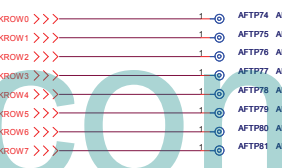
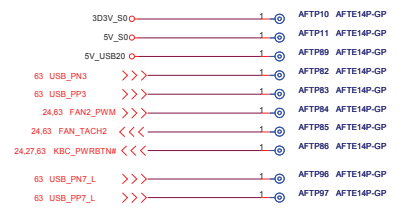
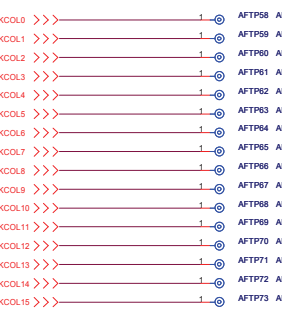
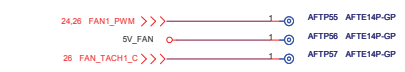
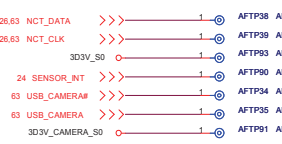
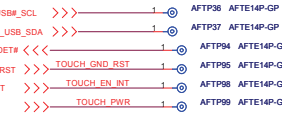
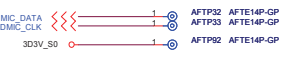
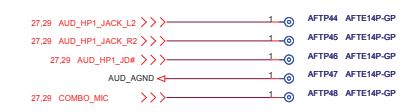
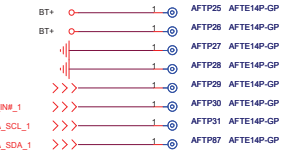
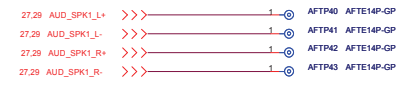
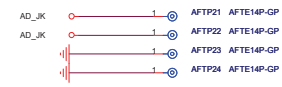
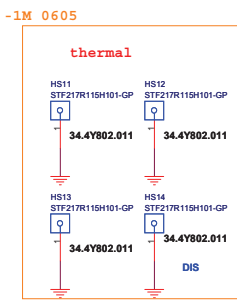
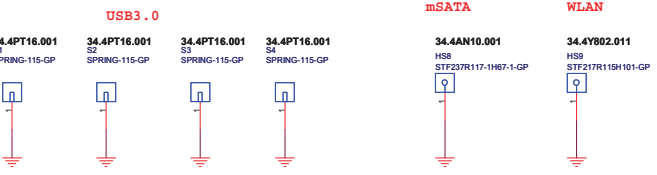
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Check test point



Test Point放在Dimm Door打開可量測處



-1 0506

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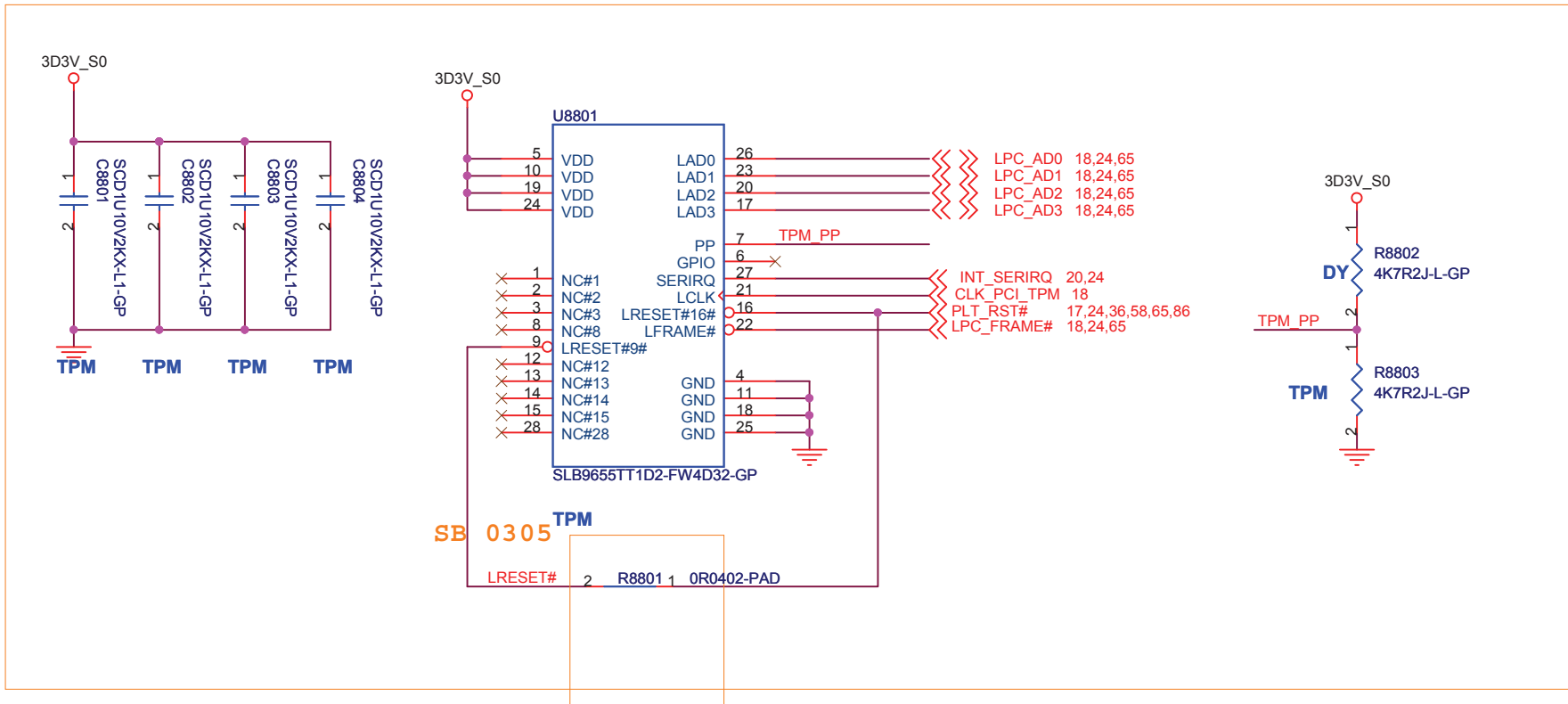
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-1M 0606



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Title		TPM	
Size	Document Number	Rev	
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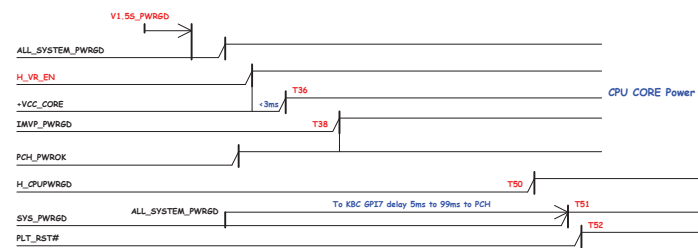
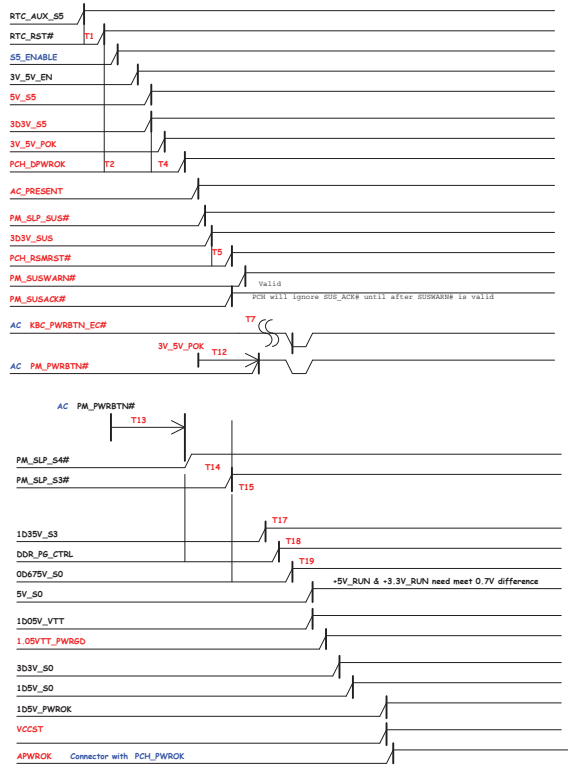
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1	OBSFN_A0	Open	I/O		2	OBSFN_A1	Open	I/O	
3	GND	GND	NA		4	OBSDATA_A[0]	Open	I/O	
5	OBSDATA_A[1]	Open	I/O		6	GND	GND	NA	
7	OBSDATA_A[2]	Open	I/O		8	OBSDATA_A[3]	Open	I/O	
9	GND	GND	NA		10	HOOK0 ¹	RSMRST#	I	System
11	HOOK1	BP_PWRGD_RST# ¹	O	System	12	HOOK2	Open	NA	
13	HOOK3	Open	NA		14	HOOK4 ¹	1.05V core	NA	
15	HOOK5	Open	NA		16	VCCOBS_AB	3.3V SUS	I	System
17	HOOK6	RSMRST# ¹	O	System	18	HOOK7	DBR# ¹	O	System
19	GND	GND	NA		20	TDO	JTAG_TDO	I	PCH
21	TRSTn	Open	NA		22	TDI	JTAG_TDI	O	PCH
23	TMS	JTAG_TMS	O	PCH	24	TCK1	Open	NA	
25	GND	GND	NA		26	TCK0	JTAG_TCK	O	PCH

<Variant Name>

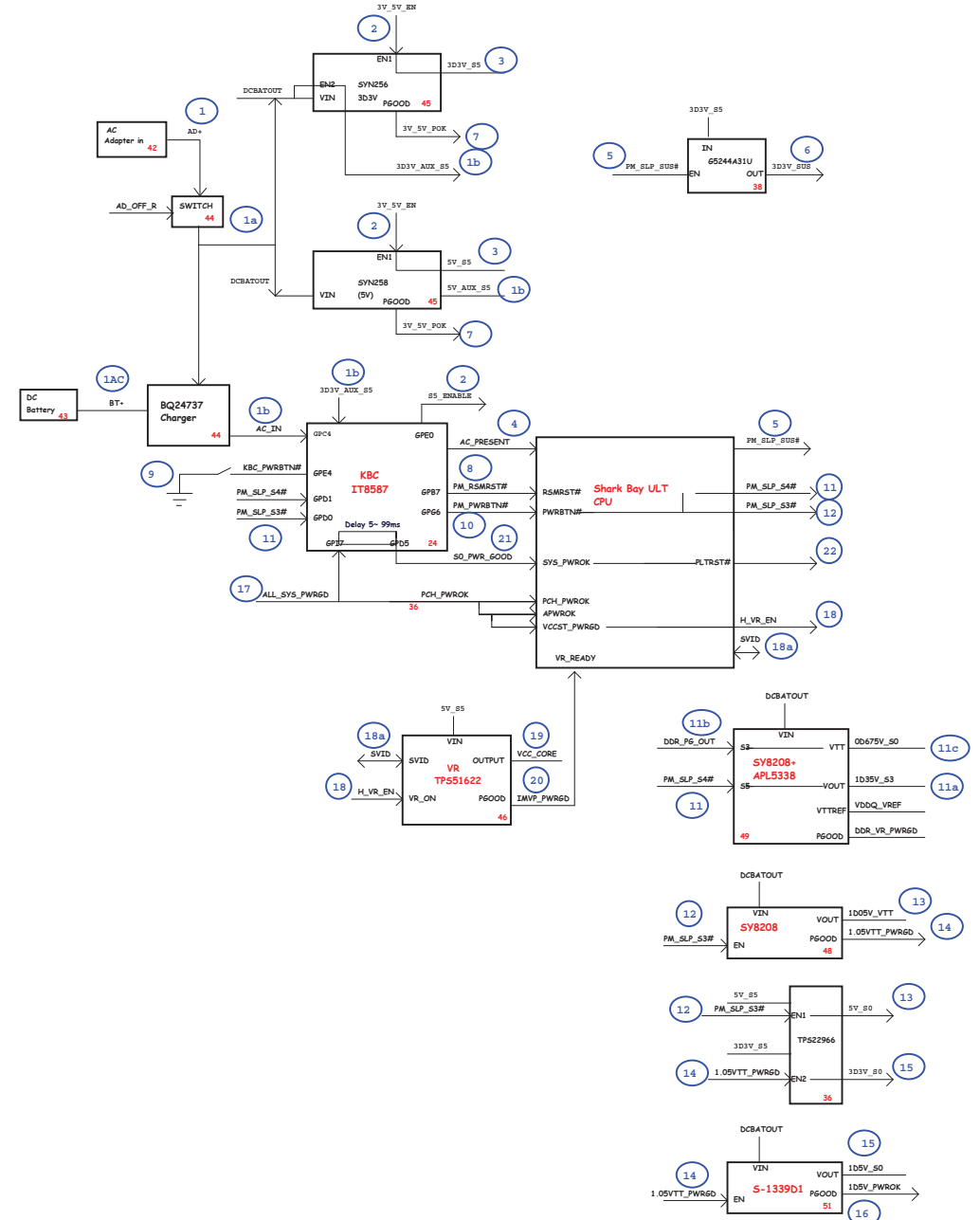
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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title PCH_XDP			
Size A4	Document Number	Rev SA	
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Intel-Power Up Sequence

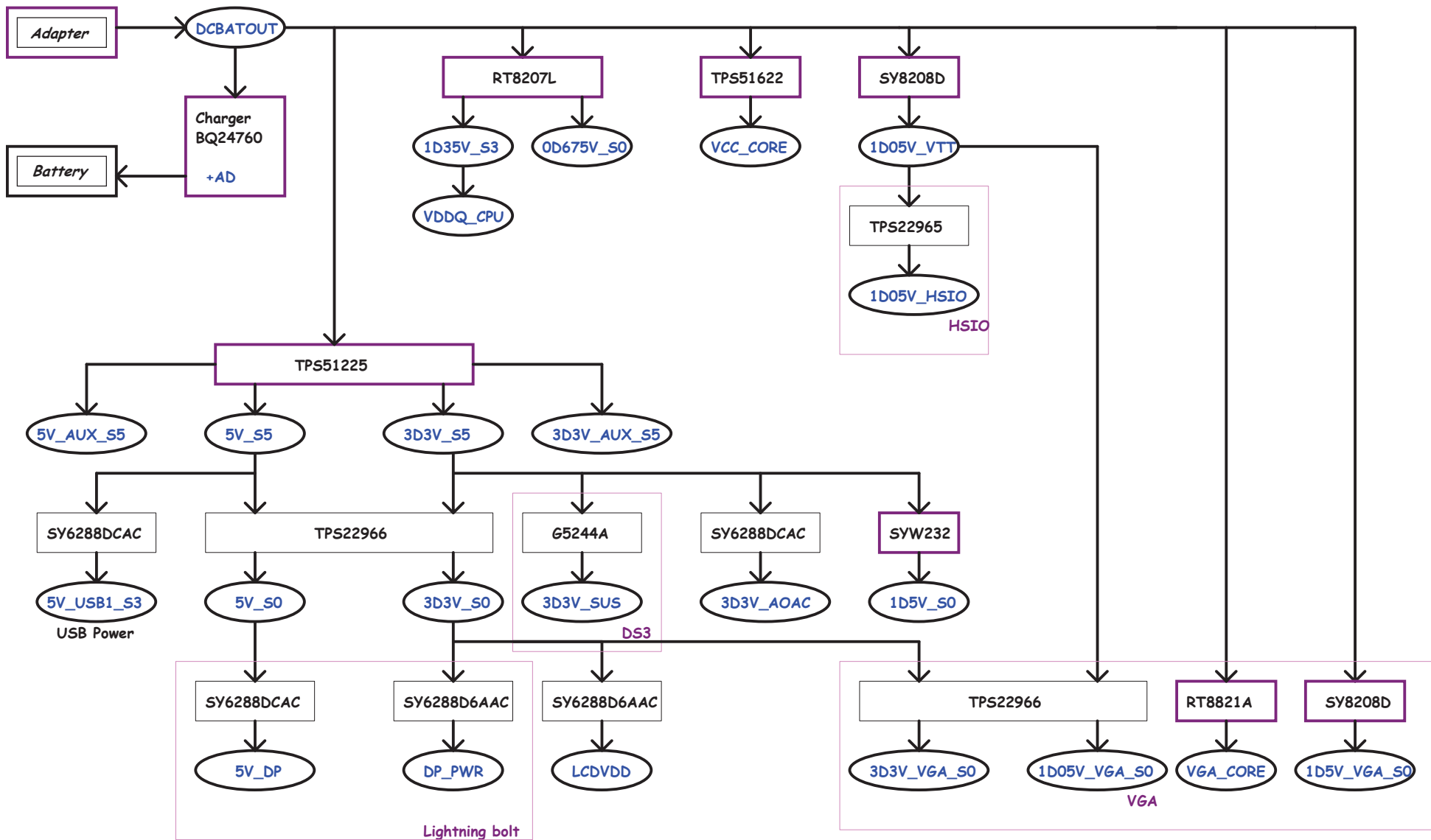
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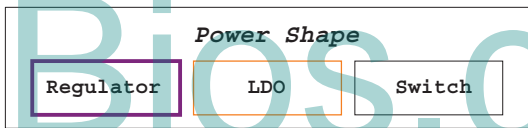
SHARK BAY POWER UP SEQUENCE DIAGRAM



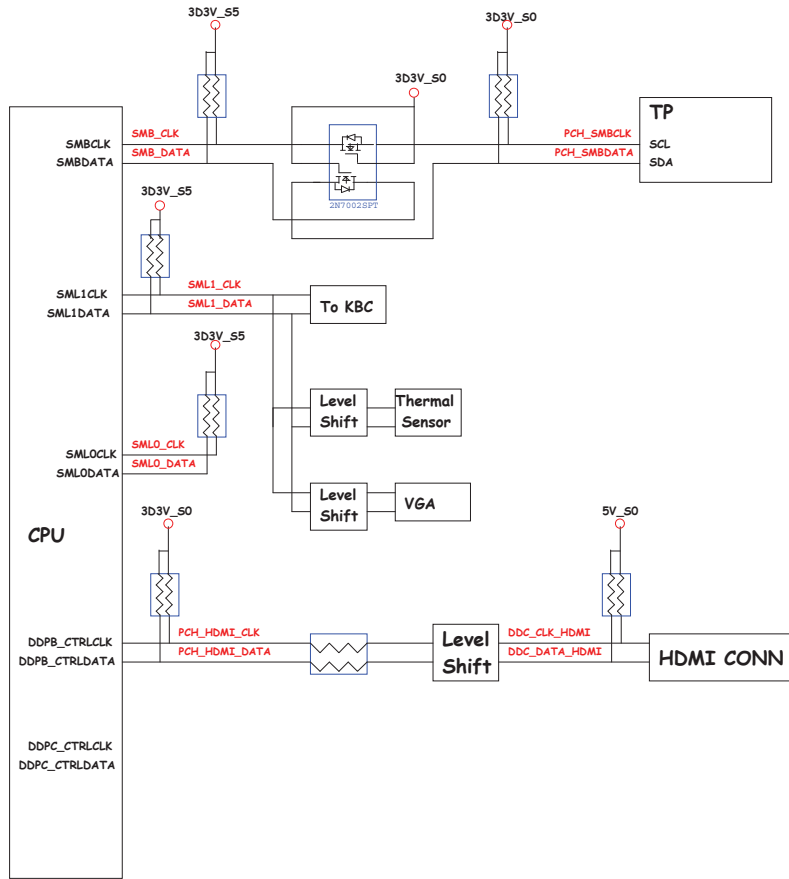
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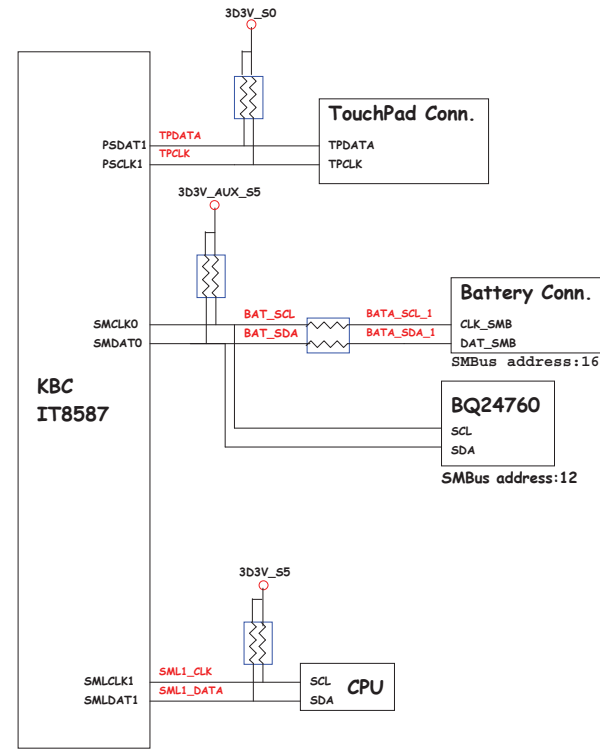
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PCH SMBus Block Diagram

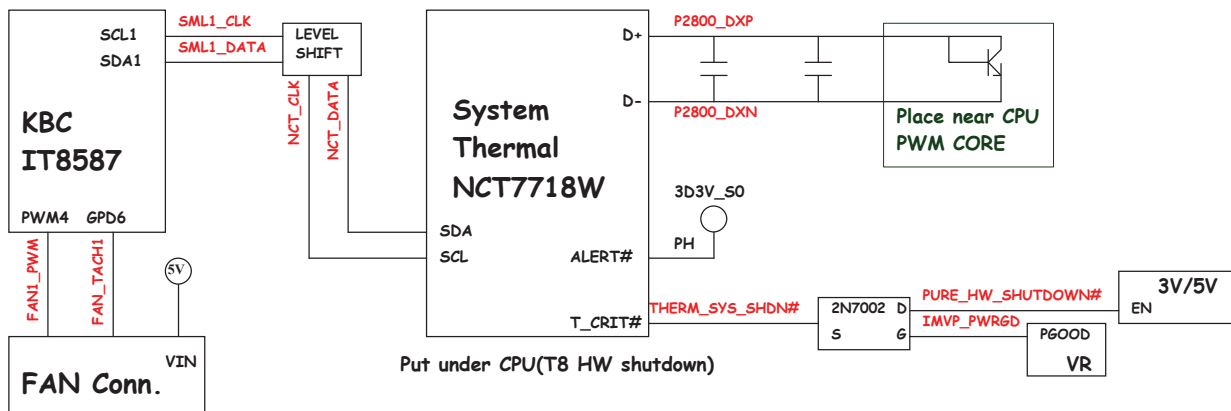


KBC SMBus Block Diagram

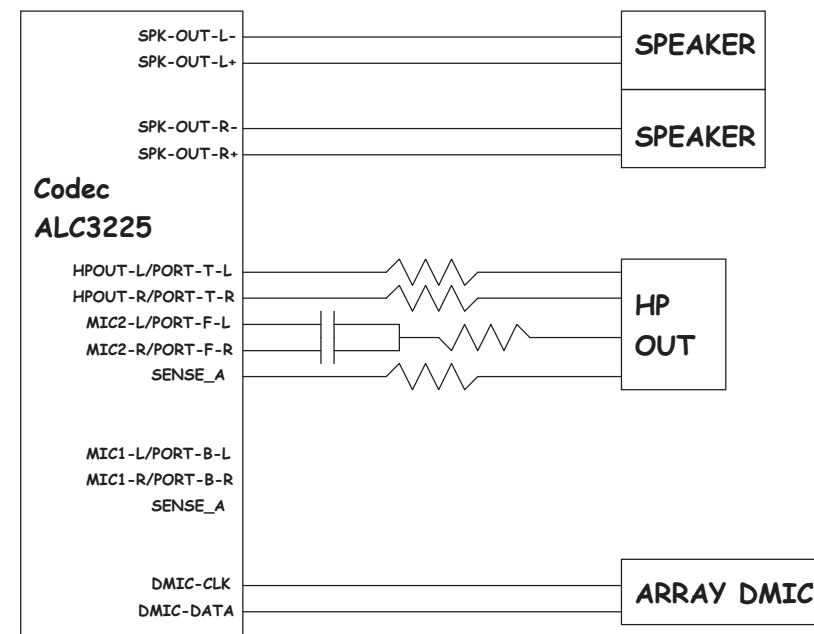


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Thermal Block Diagram



Audio Block Diagram



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