Compal Confidential

Model Name : Ezel_CX

Board NO: LA-A001P

PCB

ZZZ

DA8000WC200 PCB 0YO LA-A001P REV0 M/B 5 S

* DA8000WC210 PCB 0YO LA-A001P REV1 M/B 5 S

LA-A001P REV0 M/B 5 S

DA8000WC210

updated for new panelization

Compal Confidential

V5MM1 M/B Schematics Document

Intel Chief River (Ivy Bridge 2C BGA+ Pather Point)
with On Board DRAM, 1Rx8, 8 pcs

Nvidia N14P-GT with GDDR5*8

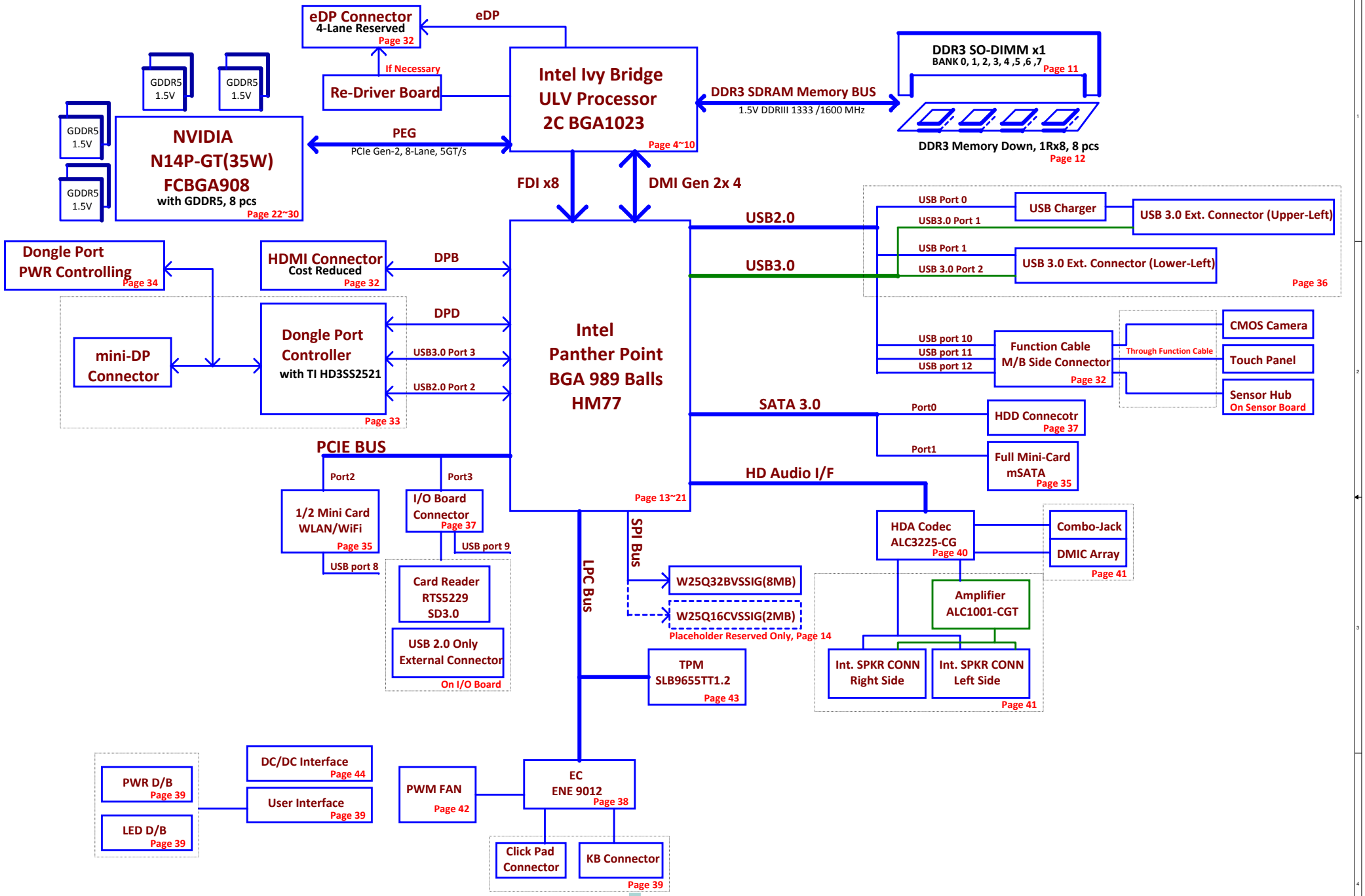
2012-03-12

REV:1.0

Panelization Information	
Main Board	LA-A001P
I/O Board	LS-A001P
Sensor Board	LS-A002P
Re-driver Board	LS-A003P
LAN Board	LS-A004P
LED Board	LS-A005P
PWR Board	LS-A006P
E-Compass Board	LS-A007P

Security Classification	Compal Secret Data		
Issued Date	2011/12/13	Deciphered Date	Date of EOP

Compal Electronics, Inc.			
Title: Cover Page			
Size: Custom	Document Number: Ezel_CX MB_LA-A001P		Rev: 1.0
Date: Wednesday, March 13, 2013	Sheet 1 of 64		



Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	Date of EOP

Compal Electronics, Inc.			
Title: Block Diagrams			
Size: Custom	Document Number: Ezel_CX MB_LA-A001P		Rev: 1.0
Date: Wednesday, March 13, 2013	Sheet 2 of 64		

System Power Rails

Power Plane	Description	S0	S3	S4	S5
+RTCVCC	RTC power	ON	ON	ON	ON
VIN	Adapter power supply (19V)	N/A	ON	ON	ON
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	ON	ON	ON	ON
+VSB	+VSB for power rails to control sequence	ON	ON	ON	ON
+CPU_CORE	Power Supply for CPU Core Power Well	ON	OFF	OFF	OFF
+VGFX_CORE	Power Supply for incorporated GPU	ON	OFF	OFF	OFF
+5VALW	5V Power Source from 3V/5V IC	ON	ON	ON	ON
+5VALW_PCH	5V Power Supply for PCH VccSus Power Well	ON	ON	ON*	ON*
+5VS	from 5VALW, power supply for 5V device	ON	OFF	OFF	OFF
+3VALW	3V Power Source from 3V/5V IC	ON	ON	ON	ON
+3VALW_PCH	3V Power Supply for PCH VccSus Powr Well	ON	ON	ON*	ON*
+3VS	from 3VALW, power supply for 3V device	ON	OFF	OFF	OFF
+VCCSA	power supply for CPU System Agent Voltage	ON	OFF	OFF	OFF
+1.8VS	use 3VALW source, for CPU VDDPLL and PCH LVDS power	ON	OFF	OFF	OFF
+1.5V	use 5VALW source, for DDR3 and for 1.5VS Gate	ON	ON	OFF	OFF
+1.5VS	from 1.5V, power supply for CPU memory controller and PCH	ON	OFF	OFF	OFF
+1.05VS_VTT	source from 5VALW, for CPU VCCIO and PCH Core Power Well	ON	OFF	OFF	OFF
+0.75VS	source from internal LDO of PU501, for DDR3 terminator	ON	OFF	OFF	OFF
+3V_LAN	3V power supply for RTL8111GS-CG LAN IC(on D/B)	ON	ON	OFF*	OFF*
+3VS_WLAN	3V power supply for WLAN	ON	OFF*	OFF*	OFF*
+3VS_DGPU	3V powr source for dGPU	ON	OFF	OFF	OFF
VGA_CORE	Core power for dGPU	ON	OFF	OFF	OFF
+1.5VSDGPU	1.5V for VRAM and memory controller of dGPU	ON*	OFF	OFF	OFF
+1.05VSDGPU	1.05V power source for dGPU	ON	OFF	OFF	OFF

ON*: if no need to disable for Erp Lot 6

OFF*: always connected is not supported by default

ON*: 1.5VSDGPU will be switched off by GC6 toggleed

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
with dGPU	dGPU@
UMA Only	UMAO@
with GC6	GC6@
w/o GC6	NGC6@
daul-mode suppored	DM@
EMI solution	EMI@
ESD solution	ESD@
RF solution	RF@
reserved for EMC	XEMC@
daul-mode not suppored	NDM@
IOAC supported	IOAC@
no stuff	@
Connector	CONN@
i3-3227U	3227@
i5-3337U	3337@
i7-3537U	3537@
PCH HM77	HM77@
ELPIDA DRAM Chip	ELPIDA@
VRAM Hynix-MFR	HYNMFR@
VRAM Hynix-AFR	HYNAFR@

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
Charger IC	0001 0010 b

EC SM Bus2 address

Device	Address
On Board Thermal Senser	1001_101xb

PCH SM Bus address

Device			Address	
ChannelA	DIMM0	A0	1010 000X	JDIMM1(SPD)

USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB3.0 port with charging (upper)
		1	USB3.0 port (lower)
	UHCI1	2	Lightning-Bolt with TI solution
		3	
	UHCI2	4	
		5	
	UHCI3	6	
		7	
EHCI2	UHCI4	8	Mini-Card for WiFi
		9	External port- USB 2.0 only
	UHCI5	10	CMOS Camera
		11	Touch Panel
	UHCI6	12	Sensor Hub
		13	

USB 3.0	Port	
XHCI	1	USB external port (upper)
	2	USB external port (lower)
	3	Lightning-Bolt with TI solution
	4	

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/12/13	Deciphered Date	Date of EOP	Title: Notes List

Size: Custom	Document Number: Ezel_CX MB_LA-A001P		Rev: 1.0
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1. PEG_RCOMPO and PEG_ICOMPI should be connected together with 4-mil width first. Then be connected to R1 from ball of PEG_ICOMPI.
2. PEG_ICOMPO should be connected to R1 with width 12-mil.
3. No longer than 500-mil to above two.

to improve thermal problem and base upon request from our end-customer, change PEG CFG to 8X

on 2013/03/10

CPU

UCPU1 — 3227@ — S IC AV8063801119500 SR0XF L1 1.9G ABO! — SA00006D990

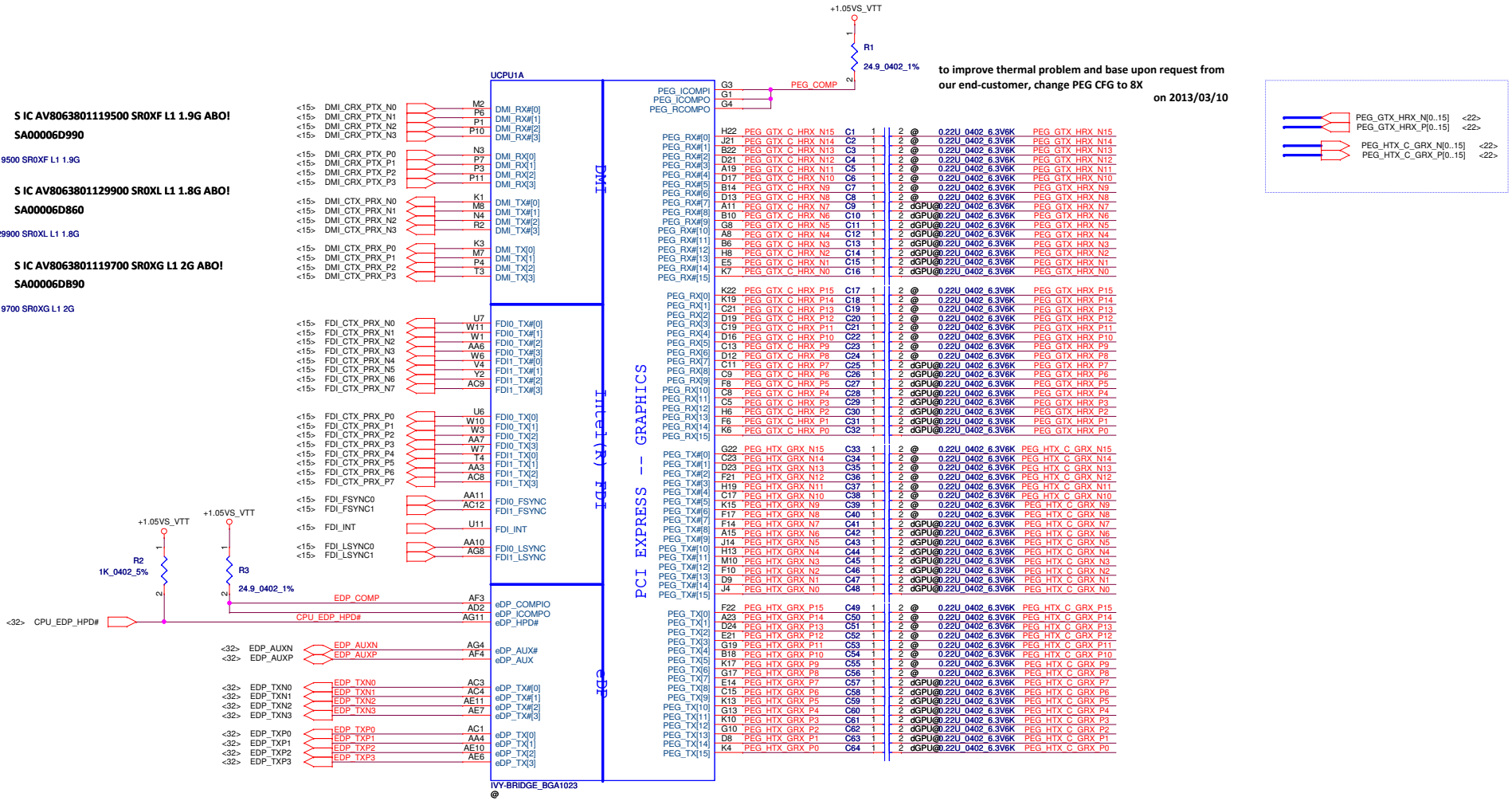
AV8063801119500 SR0XF L1 1.9G

UCPU1 — 3337@ — S IC AV8063801129900 SR0XL L1 1.8G ABO! — SA00006D860

AV8063801129900 SR0XL L1 1.8G

UCPU1 — 3537@ — S IC AV8063801119700 SR0XG L1 2G ABO! — SA00006DB90

AV8063801119700 SR0XG L1 2G



eDP_COMPIO and eDP_ICOMPO should be connected to R3 respectively.

eDP_COMPIO
Trace Width to R3= 4-mil
Trace Spacing to Other Signals= 15-mil
Max. Routing Length= 500-mil

eDP_ICOMPO
Trace Width to R3= 12-mil
Trace Spacing to Other Signals= 15-mil
Routing Length= 500-mil

Security Classification	Compal Secret Data		
Issued Date	2012/07/29	Deciphered Date	Date of EOP

Compal Electronics, Inc.			
Title	PROCESSOR(1/7) DMI,FDI,PEG		
Size: Custom	Document Number: Ezel_CX MB_LA-A001P		Rev: 1.0
Date: Wednesday, March 13, 2013	Sheet 4 of 64		

C572 should be as close as possible to CPU

Reserved by ESD

H_PECI

XEMC@ C572
0.1U_0402_16V7K

Reserved by ESD

H_CPUPWRGD

XEMC@ C66
0.1U_0402_16V7K

C66 should be as close as possible to CPU

For 2nd Generation IntelR Core processor family mobile, the output will be high.
For Mobile 3rd Generation IntelR Core processor family, the output will be low.

<17> H_SNB_IVB#

UCPU1B

MISC
PROC_SELECT# F49
PROC_DETECT# C57

THERMAL
CATERR# C49
PECI A48
PROCHOT# C45
THERMTRIP# D45

PWR MANAGEMENT
PM_SYNC C48
UNCOREPWRGOOD B46
SM_DRAMPWROK BE45
RESET# D44

JTAG & BPM
PRDY# N53
PREQ# N55
TCK L56
TMS L55
TRST# J58
TDI M60
TDO L59
DBR# K58
BPM#[0] G58
BPM#[1] E55
BPM#[2] E59
BPM#[3] G55
BPM#[4] G59
BPM#[5] H60
BPM#[6] J59
BPM#[7] J61

DDR3 MISC
SM_DRAMRST# AT30
SM_RCOMP[0] BF44
SM_RCOMP[1] BE43
SM_RCOMP[2] BG43

IVY-BRIDGE_BGA1023
@

T1 PAD @ H_CATERR#

<37> H_PECI H_PECI

+1.05VS_VTT R4 62_0402_5%
<37,51> H_PROCHOT# H_PROCHOT# R5 56_0402_5% H_PROCHOT# R

XEMC@ C551
0.1U_0402_16V7K
Reserved by ESD

<18> H_THRMTRIP#

THERMALTRIP# will be asserted when CPU junction temperature exceeds approximately 130 °C

care should be taken to no stub caused by R10

<15> H_PM_SYNC
R10 10K_0402_5%
<18> H_CPUPWRGD H_CPUPWRGD

PM_DRAM_PWRGD_R PM_DRAM_PWRGD_R

BUF_CPU_RST# BUF_CPU_RST#

CLOCKS
BCLK J3
BCLK# H2
CLK_CPU_DMI <14>
CLK_CPU_DMI# <14>

DPLL_REF_CLK AG3
DPLL_REF_CLK# AG1
DPLL_REF_CLK <14>
DPLL_REF_CLK# <14>

Reference Clock for eDP Panel

SM_DRAMRST# <6>

SM_RCOMP0 R6 140_0402_1%
SM_RCOMP1 R7 25.5_0402_1%
SM_RCOMP2 R8 200_0402_1%

	Width	Spacing	Length
SM_RCOMP0	20-mil	20-mil	< 500-mil
SM_RCOMP1	20-mil	20-mil	< 500-mil
SM_RCOMP2	15-mil	20-mil	< 500-mil

XDP_TCK PAD T2
XDP_TMS PAD T3
XDP_TRST# PAD T4
XDP_TDI PAD T5
XDP_TDO PAD T6

+3VS
R9 1K_0402_5%
XDP_DBRESET# <15>

C65 XEMC@
0.1U_0402_16V7K
Reserved by ESD

SM_DRAMRST#
XEMC@ C573
0.1U_0402_16V7K
Reserved by ESD

C573 should be as close as possible to CPU

SM_DRAMPWROK

+3VALW
C67 0.1U_0402_16V7K
+1.5VS
R11 200_0402_5%
<15> SYS_PWROK
<15> PM_DRAM_PWRGD
U15
MC74VHC1G09DFT2G_SC70-5
PM_SYS_PWRGD_BUF
R13 130_0402_5%
PM_DRAM_PWRGD_R

Buffered Reset to CPU

+3VS
C68 0.1U_0402_16V7K
U16
SN74LVC1G07DCKR_SC70-5
+1.05VS_VTT
R12 75_0402_5%
R15 43_0402_1%
<17,36,37,42> PLT_RST#
PLT_RST#
BUFO_CPU_RST#
BUF_CPU_RST#

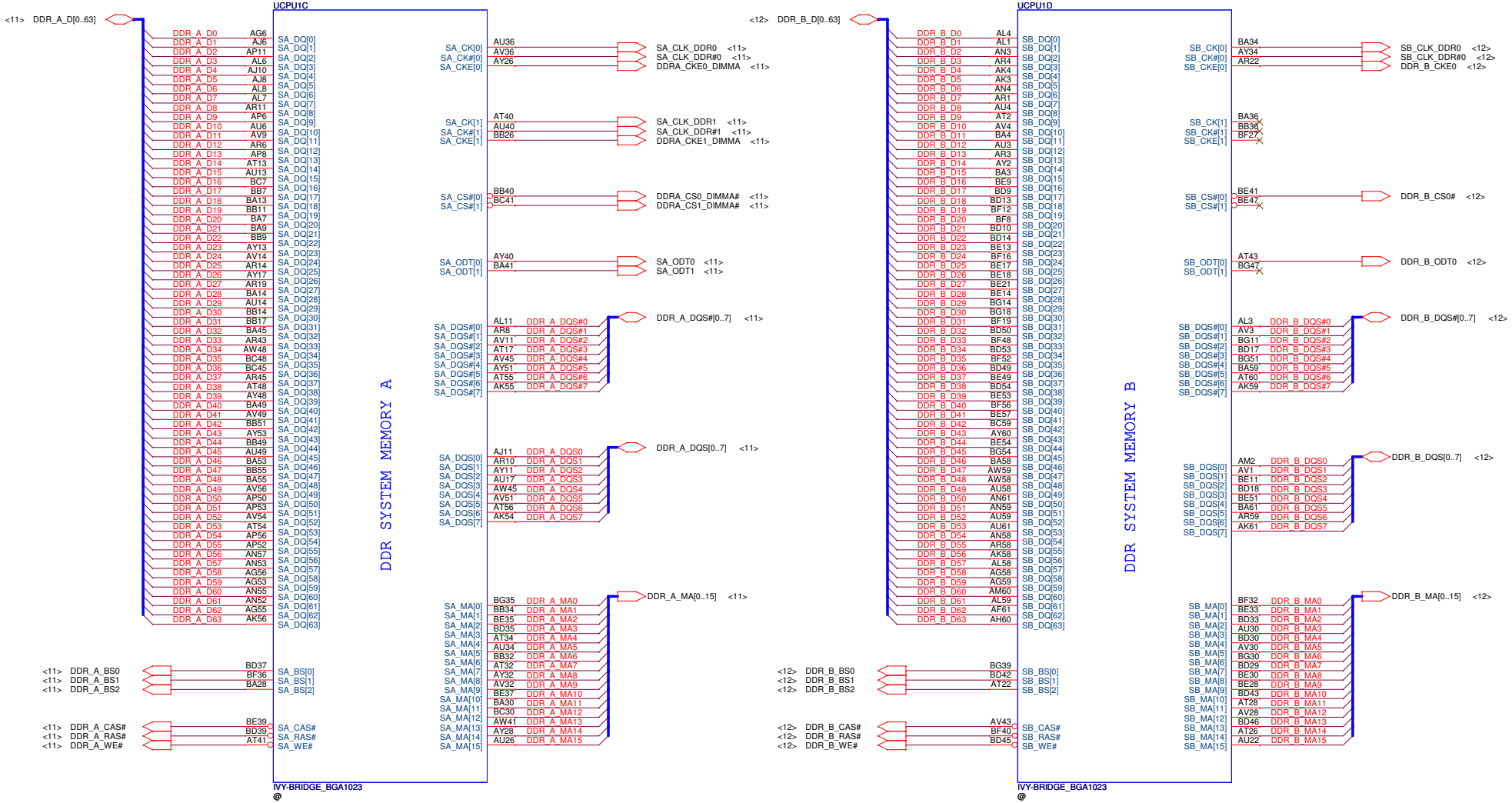
Security Classification	Compal Secret Data		
Issued Date	2012/07/29	Deciphered Date	Date of EOP

Compal Electronics, Inc.

Title: PROCESSOR(3/7) DDRIII

Size	Document Number	Rev
Custom	Ezel_CX MB_LA-A001P	1.0

Date: Wednesday, March 13, 2013 Sheet 5 of 64



Security Classification	Compal Secret Data		
Issued Date	2012/07/29	Deciphered Date	Date of EOP

Compal Electronics, Inc.			
Title	PROCESSOR(3/7) DDRIII		
Size: Custom	Document Number: Ezel_CX MB_LA-A001P		Rev: 1.0
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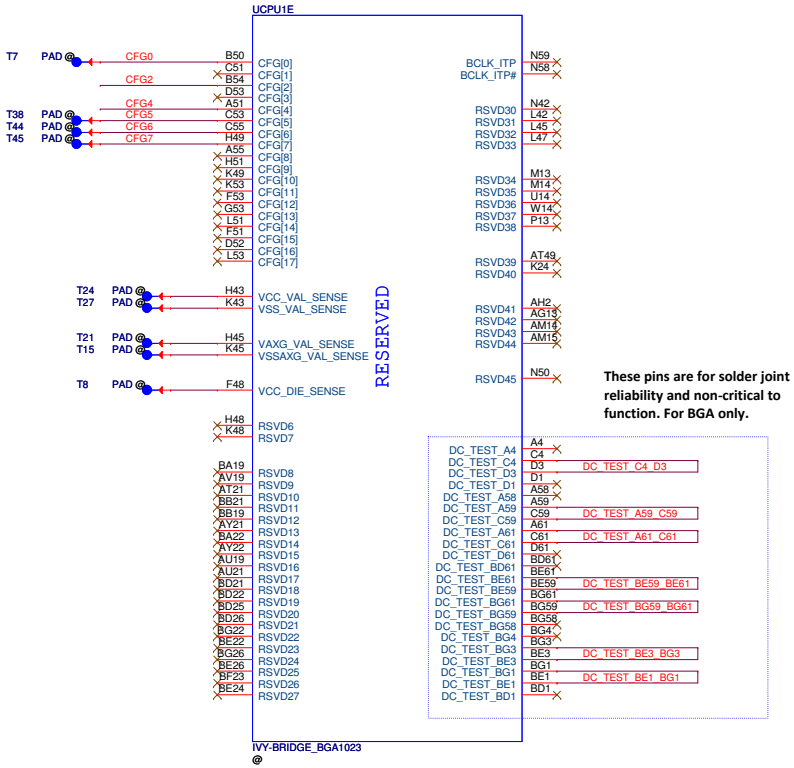
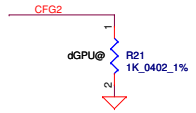
PEG DEFER TRAINING	
CFG7	* 1: (Default) PEG Trains immediately and follows xxRESETB de-assertion 0: PEG Wait for BIOS for training

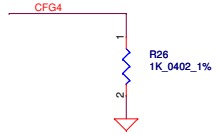


These pins are for solder joint reliability and non-critical to function. For BGA only.

CFG Straps for Processor



PCIe Static x16 Lane Numbering Reversal	
CFG2	1: (Default)Normal Operation Lane # definition matches socket pin map definition * 0: Lane Reversed

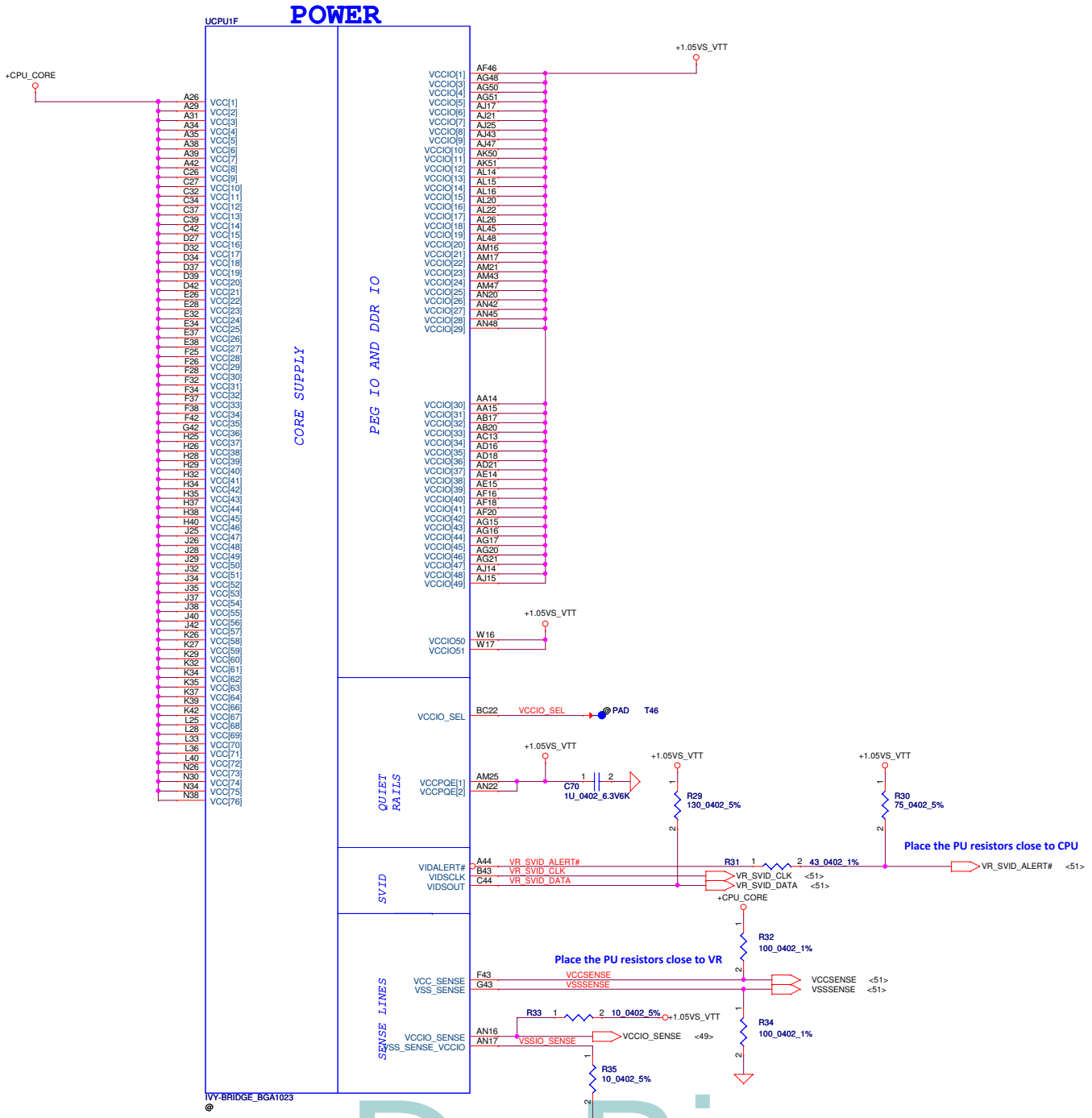


eDP Enable Strap	
CFG4	1: (Default)Disable *0: Enable

PCIE Port Bifurcation Straps	
CFG[6:5]	* 11: (Default) 1x16 PCI Express 10: 2x8 PCI Express 01: Reserved 00: 1x8,2x4 PCI Express

Security Classification	Compal Secret Data		
Issued Date	2012/07/29	Deciphered Date	Date of EOP

Compal Electronics, Inc.			
Title	PROCESSOR(4/7) RSVD,CFG		
Size: Custom	Document Number: Ezel_CX MB_LA-A001P		Rev: 1.0
Date: Wednesday, March 13, 2013	Sheet 7 of 64		



CPU Power Rail Table			
Voltage Rail	Voltage	S0 Iccmax Current(A)	
VCC	0.65~1.2	33	Processor Core Voltage
VCCIO	1.05	8.5	Processor Uncore Voltage
VDDQ	1.5	5	Memory Controller Voltage
VCCSA	0.675~0.9	4	System Agent Voltage
VCCPLL	1.8	1.2	Processor PLL Voltage
VAXG	0.65~1.25	29	Processor Graphics Voltage

Refer to Mobile 3rd Generation IntelR Core Processor Family External Design Specification (EDS) Volume 1 of 2 Revision 2.2

Security Classification	Compal Secret Data		
Issued Date	2012/07/29	Deciphered Date	Date of EOP

Compal Electronics, Inc.			
Title	PROCESSOR(5/7) PWR,BYPASS		
Size: Custom	Document Number: Ezel_CX MB_LA-A001P		Rev: 1.0
Date: Wednesday, March 13, 2013	Sheet 8 of 64		

POWER

UCPU1G

+VGFX_CORE

DC 29A

AA46 AB47 AB50 AB51 AB52 AB53 AB55 AB56 AB58 AB59 AC61 AD47 AD48 AD50 AD51 AD52 AD53 AD55 AD56 AD58 AD59 AE46 N45 P47 P48 P50 P51 P52 P53 P55 P56 P61 T48 T58 T59 T61 U46 V47 V48 V50 V51 V52 V53 V55 V56 V58 V59 W50 W51 W52 W53 W55 W56 W61 Y48 Y61

VAXG[1] VAXG[2] VAXG[3] VAXG[4] VAXG[5] VAXG[6] VAXG[7] VAXG[8] VAXG[9] VAXG[10] VAXG[11] VAXG[12] VAXG[13] VAXG[14] VAXG[15] VAXG[16] VAXG[17] VAXG[18] VAXG[19] VAXG[20] VAXG[21] VAXG[22] VAXG[23] VAXG[24] VAXG[25] VAXG[26] VAXG[27] VAXG[28] VAXG[29] VAXG[30] VAXG[31] VAXG[32] VAXG[33] VAXG[34] VAXG[35] VAXG[36] VAXG[37] VAXG[38] VAXG[39] VAXG[40] VAXG[41] VAXG[42] VAXG[43] VAXG[44] VAXG[45] VAXG[46] VAXG[47] VAXG[48] VAXG[49] VAXG[50] VAXG[51] VAXG[52] VAXG[53] VAXG[54] VAXG[55] VAXG[56]

GRAPHICS

VREF

SM_VREF — AY43 — +V_SM_VREF

+V_SM_VREF should be 20-mil trace width and 20-mil spacing

+1.5VS

R36 1K_0402_5%

R37 1K_0402_5%

C71 0.1U_0402_16V7K

SA_DIMM_VREFDQ — BE7 — SA_DIMM_VREFDQ — PAD T47

SB_DIMM_VREFDQ — BG7 — SB_DIMM_VREFDQ — PAD T48

DDR3 - 1.5V RAILS

5A

AJ28 AJ33 AJ36 AJ40 AL30 AL34 AL38 AL42 AM33 AM36 AM40 AN30 AN34 AN38 AR26 AR28 AR30 AR32 AR34 AR36 AR40 AV41 AW26 BA40 BB28 BG33

VDDQ[1] VDDQ[2] VDDQ[3] VDDQ[4] VDDQ[5] VDDQ[6] VDDQ[7] VDDQ[8] VDDQ[9] VDDQ[10] VDDQ[11] VDDQ[12] VDDQ[13] VDDQ[14] VDDQ[15] VDDQ[16] VDDQ[17] VDDQ[18] VDDQ[19] VDDQ[20] VDDQ[21] VDDQ[22] VDDQ[23] VDDQ[24] VDDQ[25] VDDQ[26]

stuff for first version then check the feasibility to remove them

Place TOP IN BGA

C72 C73 C74 C75 C76 C77 C78 C79 C80 C81 1U_0402_6.3V6K

C589 100U_1206_6.3V6M

Place BOT OUT BGA

C83 C84 C85 C86 C87 C88 C89 C90 10U_0603_6.3V6M

stuff for first version then check the feasibility to remove them

Follow VDDQ 1.5V-Rail Decoupling Recommendation from Intel PDDG Rev 1.0,
1. 1x 330uF
2. 8x 10uF (0603)
3. 10x 1uF (0402)

SENSE LINES

VAXG_SENSE — F45

VSSAXG_SENSE — G45

<51> VCC_AXG_SENSE

<51> VSS_AXG_SENSE

R40 100_0402_5%

R41 100_0402_5%

1.2A

QUIET RAILS

VCCDQ[1] — AM28

VCCDQ[2] — AN26

+1.5VS

C91 1U_0402_6.3V6K

1.8V RAIL

+1.8VS

BB3 VCCPLL[1]

BC1 VCCPLL[2]

BC4 VCCPLL[3]

C92 100U_1206_6.3V6M

C94 C95 1U_0402_6.3V6K

VCCPLL Plane Decoupling Recommendation from Intel PDDG Rev 1.0,
1. 1x 330uF
2. 2x 1uF (0402)

SENSE LINES

VDDQ_SENSE — BC43

VSS_SENSE_VDDQ — BA43

VCCSA_SENSE — U10

SA RAIL

6A

L17 L21 N16 N20 N22 P17 P20 R16 R18 R21 U15 V16 V17 V18 V21 W20

VCCSA[1] VCCSA[2] VCCSA[3] VCCSA[4] VCCSA[5] VCCSA[6] VCCSA[7] VCCSA[8] VCCSA[9] VCCSA[10] VCCSA[11] VCCSA[12] VCCSA[13] VCCSA[14] VCCSA[15] VCCSA[16]

*For ULV Only

VID[0] ball D48	VID[1] ball D49	VCCSA Output
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

VCCSA VID lines

VCCSA_VID[0] — D48 — H_VCCSA_VID0 — H_VCCSA_VID0 <50>

VCCSA_VID[1] — D49 — H_VCCSA_VID1 — H_VCCSA_VID1 <50>

+VCCSA

Place TOP IN BGA

C96 100U_1206_6.3V6M

C97 C98 C99 C100 C101 1U_0402_6.3V6K

Place BOT OUT BGA

C102 C103 C104 C105 C106 10U_0603_6.3V6M

stuff for first version then check the feasibility to remove them

Follow VCCSA Plane Decoupling Recommendations from Intel PDDG Rev 1.0,
1. 1x 330uF
2. 5x 10uF (0603)
3. 5x 1uF (0402)

IVY-BRIDGE_BGA1023

Security Classification	Compal Secret Data		
Issued Date	2012/07/29	Deciphered Date	Date of EOP

Compal Electronics, Inc.	
Title	PROCESSOR(6/7) PWR
Size: Custom	Document Number: Ezel_CX MB_LA-A001P
Rev	1.0
Date:	Wednesday, March 13, 2013
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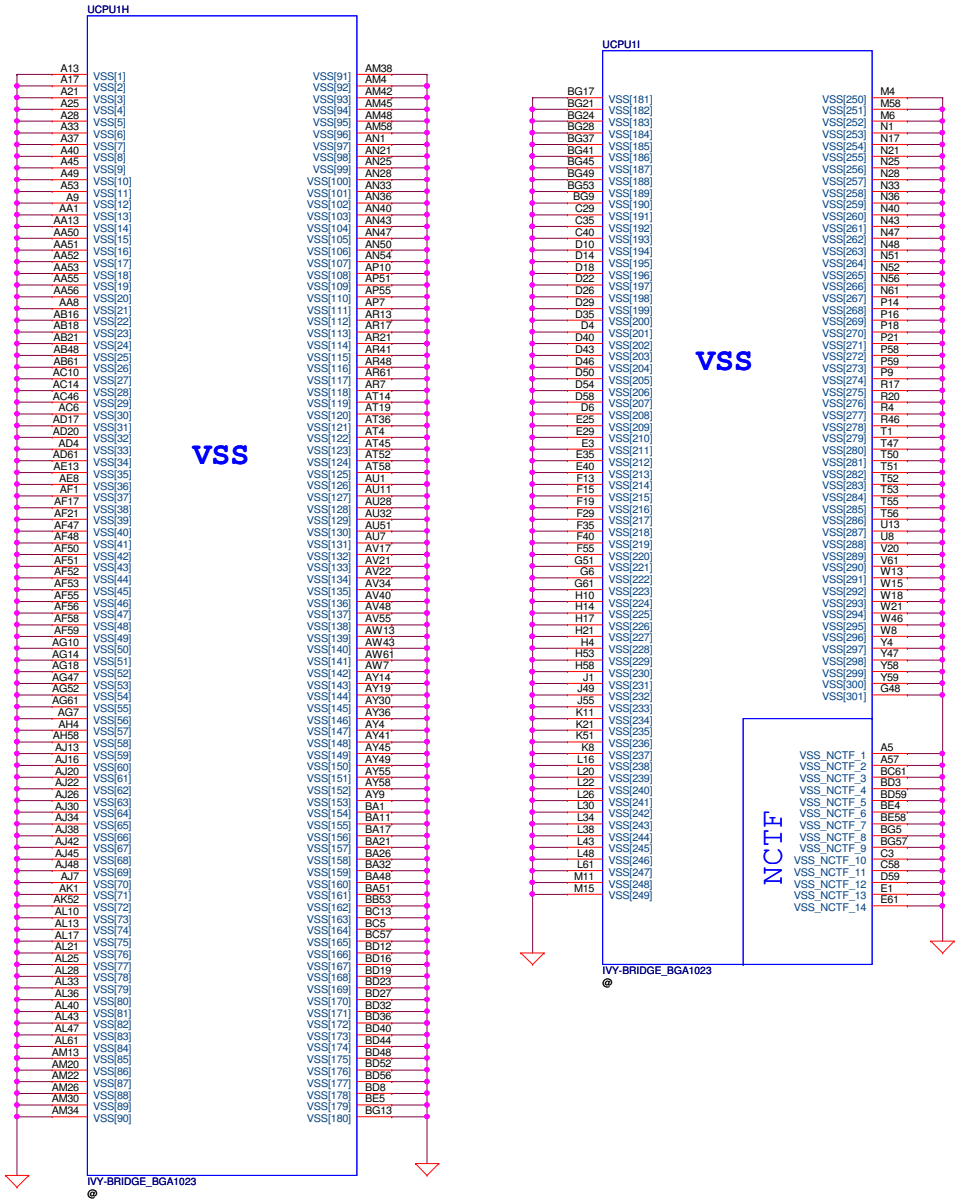
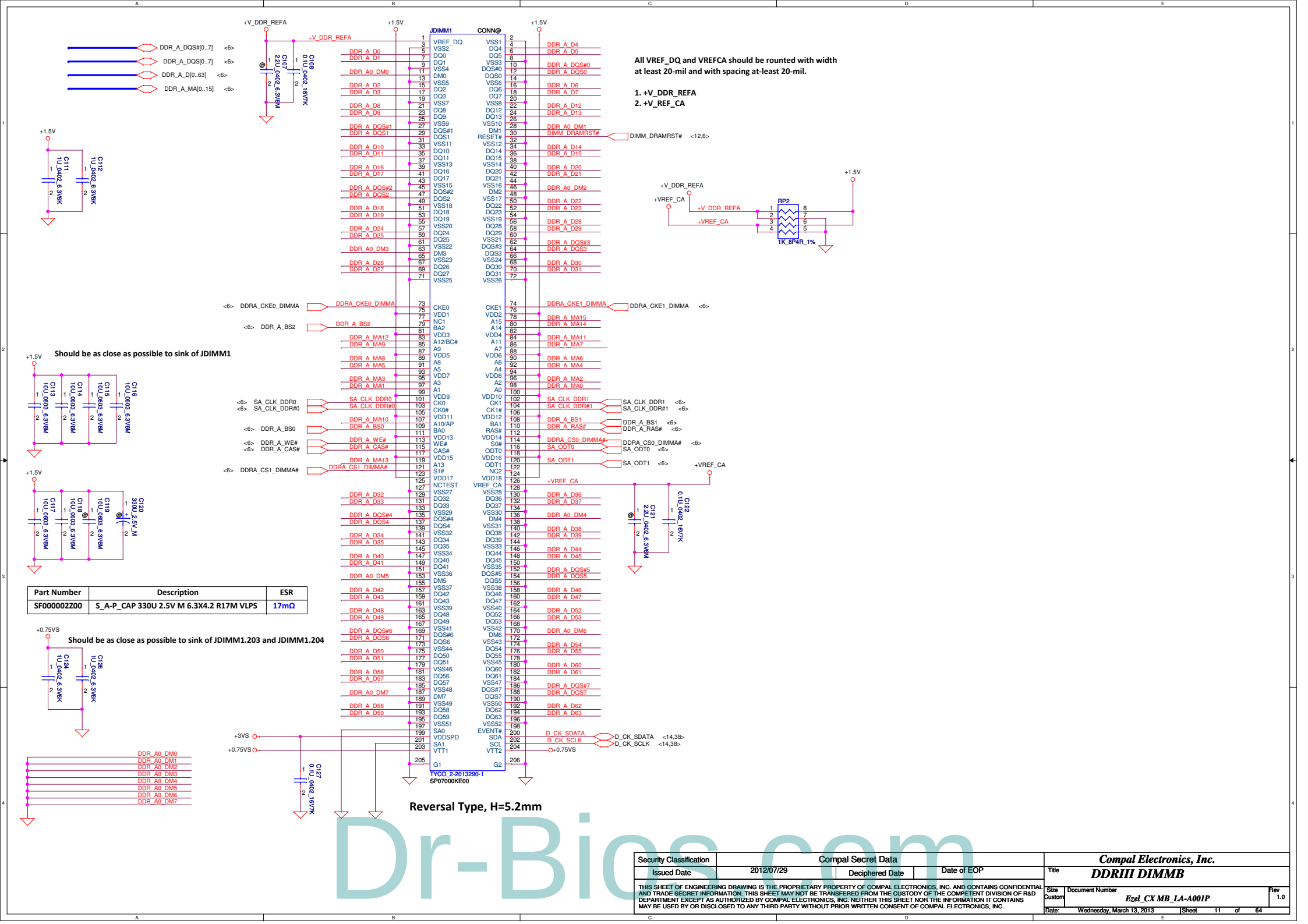


Security Classification	Compal Secret Data		
Issued Date	2012/07/29	Deciphered Date	Date of EOP

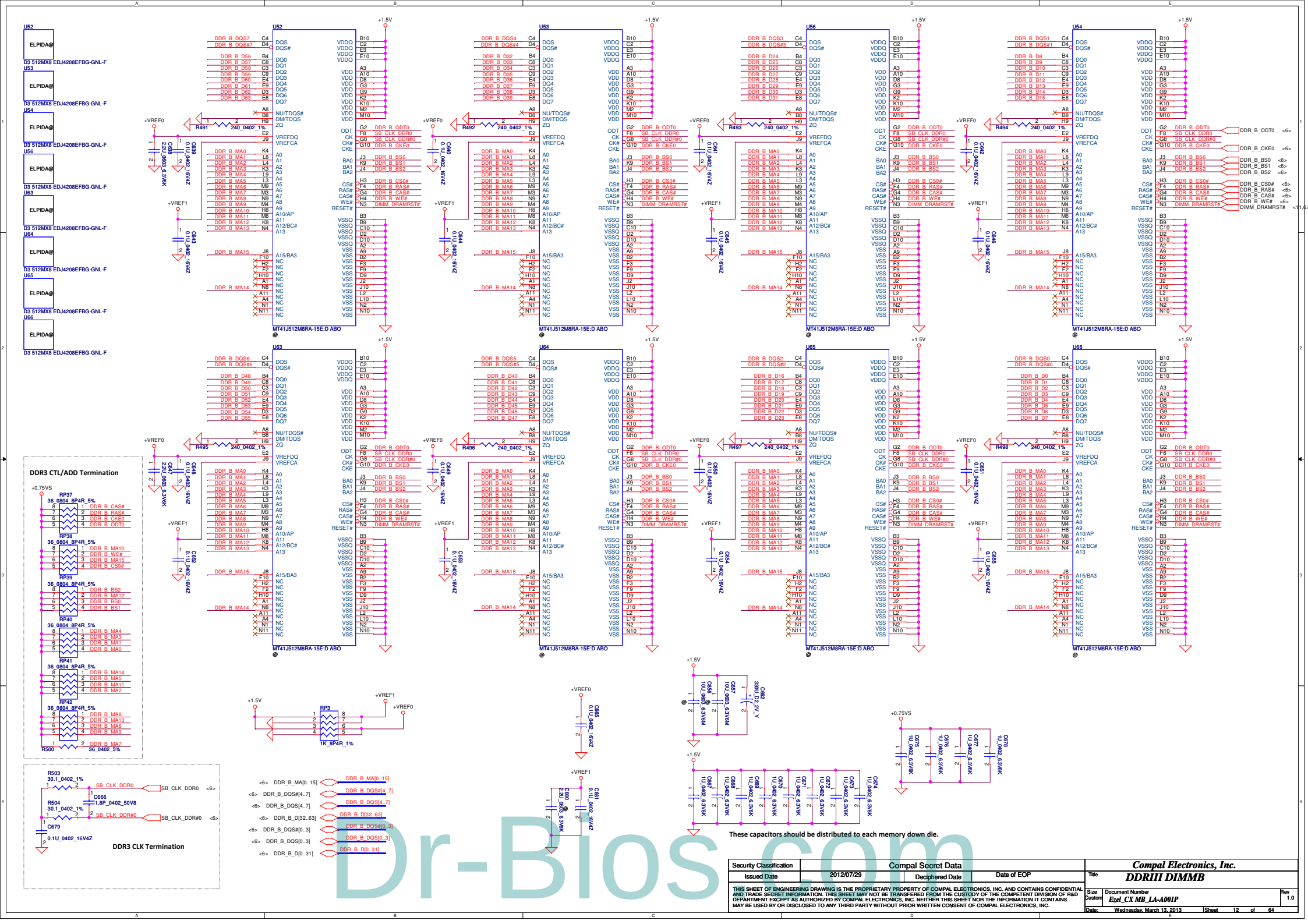
Compal Electronics, Inc.		
Title	PROCESSOR(7/7) VSS	
Size: Custom	Document Number: Ezel_CX MB_LA-A001P	Rev: 1.0
Date: Wednesday, March 13, 2013	Sheet 10 of 64	



Part Number	Description	ESR
SF000002Z00	S_A-P_CAP 330U 2.5V M 6.3X4.2 R17M VLPS	17mΩ

Security Classification	Compal Secret Data		
Issued Date	2012/07/29	Deciphered Date	Date of EOP

Compal Electronics, Inc.			
Title: DDRIII DIMMB			
Size: Custom	Document Number: Ezel_CX MB_LA-A001P		Rev: 1.0
Date: Wednesday, March 13, 2013	Sheet 11 of 64		


U52
ELPIDA@
D3 512MX8 EDJ4208EFBG-GNL-F
U53
U54
U56
U63
U64
U65
U66
MT41J512M8RA-15E:D ABO
DDR B DQS7
DDR B DQS#7
DDR B D56
DDR B D57
DDR B D58
DDR B D59
DDR B D60
DDR B D61
DDR B D62
DDR B D63
DDR B MA0
DDR B MA1
DDR B MA2
DDR B MA3
DDR B MA4
DDR B MA5
DDR B MA6
DDR B MA7
DDR B MA8
DDR B MA9
DDR B MA10
DDR B MA11
DDR B MA12
DDR B MA13
DDR B MA15
DDR B MA14
DDR B ODT0
DDR B CKE0
DDR B BS0
DDR B BS1
DDR B BS2
DDR B CS0#
DDR B RAS#
DDR B CAS#
DDR B WE#
DIMM_DRAMRST#
SB_CLK_DDR0
SB_CLK_DDR#0
+1.5V
+VREF0
+VREF1
R491
240_0402_1%
C639
0.1U_0402_16V4Z
C643
C666
1.8P_0402_50V8
C679
R503
30.1_0402_1%
R504
SB_CLK_DDR0
SB_CLK_DDR#0
DDR3 CLK Termination
DDR3 CTL/ADD Termination
+0.75VS
RP37
36_0804_8P4R_5%
RP38
RP39
RP40
RP41
RP42
R500
RP3
1K_8P4R_1%
DDR_B_MA[0..15]
DDR_B_DQS#[4..7]
DDR_B_DQS[4..7]
DDR_B_D[32..63]
DDR_B_DQS#[0..3]
DDR_B_DQS[0..3]
DDR_B_D[0..31]
C665
10U_0603_6.3V6M
C657
C682
330U_D2_2V_Y
C675
C676
C677
C678
C667
C669
C670
C671
C672
C673
C674
These capacitors should be distributed to each memory down die.
Security Classification
Compal Secret Data
Issued Date
2012/07/29
Deciphered Date
Date of EOP
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Compal Electronics, Inc.
Title
DDRIII DIMMB
Size
Custom
Document Number
Ezel_CX MB_1A-A001P
Rev
1.0
Date:
Wednesday, March 13, 2013
Sheet
12
of
64

+RTCBATT
20mil
D1
BAS40-04_SOT23-3
+RTCVCC
+CHGRTC
20mil
C167
0.1U_0402_16V4Z
20mil

+RTCVCC
R55 1 2 1M_0402_5% SM_INTRUDER#
R56 1 2 330K_0402_5% PCH_INTVRMEN
INTVRMEN(Internal Voltage Regulator Enable)
for DcpSus well
* H: Integrated VRM enable
L: Integrated VRM disable

PCH
UPCH1
HM77@
S IC BD82HM77 SLJ8C C1 BGA 989P PCH ABO!
SA00005AGI0
BD82HM77 SLJ8C C1 BGA 989P

32.768 for Real Time Clock
PCH_RTCX1
PCH_RTCX2
R58 10M_0402_5%
Y1
32.768K 12.5PF 1TJF125DP1A000D
C170 18P_0402_50V8J
C171 18P_0402_50V8J

+3VALW_PCH
R61 2 1 1K_0402_5% HDA_SYNC_PCH
On-Die PLL Voltage Regulator Voltage Select
for VccVRM
* H: 1.5V for VccVRM (for Mobile platform)
L: 1.8V for VccVRM (for Desktop platform), weak internal pull low

Both JCMOS1 and JME2 should be placed close to JDIMM1
+RTCVCC
C168 1U_0603_10V6K
JCMOS1 SHORT PADS @
C169 1U_0603_10V6K
JME2 SHORT PADS @
not be shown on mask layer
R57 1 2 20K_0402_5%
R59 1 2 20K_0402_5%

UPCH1A @
PCH_RTCX1 A20 RTCX1
PCH_RTCX2 C20 RTCX2
PCH_RTCRST# D20 RTCRST#
PCH_SRTCRST# G22 SRTCRST#
SM_INTRUDER# K22 INTRUDER#
PCH_INTVRMEN C17 INTVRMEN
RTC
HDA_BITCLK_PCH N33 HDA_BCLK
HDA_SYNC_PCH L34 HDA_SYNC
PCH_SPKR T10 SPKR
HDA_RST_PCH# K34 HDA_RST#
<39> PCH_SPKR
<39> HDA_SDIN0_PCH HDA_SDIN0_PCH E34 HDA_SDIN0
G34 HDA_SDIN1
C34 HDA_SDIN2
A34 HDA_SDIN3
<37> HDA_SDOUT_PCH HDA_SDOUT_PCH A36 HDA_SDO
C36 HDA_DOCK_EN# / GPIO33
N32 HDA_DOCK_RST# / GPIO13
IHDA
PAD T9 @ PCH_JTAG_TCK J3 JTAG_TCK
PAD T10 @ PCH_JTAG_TMS H7 JTAG_TMS
PAD T11 @ PCH_JTAG_TDI K5 JTAG_TDI
PCH_JTAG_TDO H1 JTAG_TDO
JTAG
PCH_SPI_CLK_2 R67 33_0402_5% XEMC@
PCH_SPI_CLK_1 R68 33_0402_5% EMI@
PCH_SPI_CLK T3 SPI_CLK
PCH_SPI_CS0# Y14 SPI_CS0#
PCH_SPI_CS1# T1 SPI_CS1#
PCH_SPI_MOSI V4 SPI_MOSI
PCH_SPI_MISO U3 SPI_MISO
SPI
COUGARPOINT_FCBGA989

LPC
FWH0 / LAD0 C38 LPC_AD0
FWH1 / LAD1 A38 LPC_AD1
FWH2 / LAD2 B37 LPC_AD2
FWH3 / LAD3 C37 LPC_AD3
FWH4 / LFRAME# D36 LPC_FRAME#
LDRQ0# E36
LDRQ1# / GPIO23 K36 PCH_GPIO23
SERIRQ V5 SERIRQ
<37,42> LPC_AD0 LPC_AD1 LPC_AD2 LPC_AD3 LPC_FRAME# SERIRQ
PCH_GPIO23 <18> ←On Board DRAM Flag

SATA 6G
SATA0RXN AM3
SATA0RXP AM1
SATA0TXN AP7
SATA0TXP AP5
SATA_PRX_DTX_N0 <36>
SATA_PRX_DTX_P0 <36>
SATA_PTX_DRX_N0 <36>
SATA_PTX_DRX_P0 <36>
SATA Port 0 is for HDD Connector
SATA1RXN AM10
SATA1RXP AM8
SATA1TXN AP11
SATA1TXP AP10
SATA_PRX_DTX_N1 <34>
SATA_PRX_DTX_P1 <34>
SATA_PTX_DRX_N1 <34>
SATA_PTX_DRX_P1 <34>
SATA Port 0 is for SSD
SATA2RXN AD7
SATA2RXP AD5
SATA2TXN AH5
SATA2TXP AH4
SATA3RXN AB8
SATA3RXP AB10
SATA3TXN AF3
SATA3TXP AF1
SATA4RXN Y7
SATA4RXP Y5
SATA4TXN AD3
SATA4TXP AD1
SATA5RXN Y3
SATA5RXP Y1
SATA5TXN AB3
SATA5TXP AB1
SATAICOMPO Y11
SATAICOMPI Y10 SATA_COMP R63 1 2 37.4_0402_1%
+1.05VS_VTT
SATA3RCOMPO AB12
SATA3COMPI AB13 SATA3_COMP R66 1 2 49.9_0402_1%
+1.05VS_VTT
SATA3RBIAS AH1 RBIAS_SATA3 R69 1 2 750_0402_1%
SATALED# P3 PCH_SATALED#
SATA0GP / GPIO21 V14 PCH_GPIO21
SATA1GP / GPIO19 P1 PCH_GPIO19
SATA

SATAICOMPO and SATACOMPI should be connected together then to R63.
SATA3ICOMPO and SATA3COMPI should be connected together then to R66.
Trace Impedance= 50-ohm
Keep-out to other Signals, especially to CLK= 15-mil

<18,34> mSATA_DET#
<14,34> MINI1_CLKREQ#
RP10
mSATA_DET# 1 8
MINI1_CLKREQ# 2 7
SERIRQ 3 6
PCH_SATALED# 4 5
10K_8P4R_5%
+3VS

<39> HDA_BITCLK_AUDIO
<39> HDA_SYNC_AUDIO
<39> HDA_RST_AUDIO#
<39> HDA_SDOUT_AUDIO
RP11 EMI@
HDA_BITCLK_PCH 1 8
HDA_SYNC_PCH_R 2 7
HDA_RST_PCH# 3 6
HDA_SDOUT_PCH 4 5
33_8P4R_5%
R64 1M_0402_5%
for HDA_SYNC Potential Leakage Concern
+5VS
Q2
LBSS138LT1G_SOT-23-3
HDA_SYNC_PCH

R62 51_0402_5%
follow design guide 2.0 to cancel series resistor

PCH_SPI_MISO_1 R302 0_0402_5% PCH_SPI_MISO
PCH_SPI_MISO_2 R300 0_0402_5% PCH_SPI_MISO
PCH_SPI_MOSI_2 R301 0_0402_5% PCH_SPI_MOSI
PCH_SPI_MOSI_1 R303 0_0402_5% PCH_SPI_MOSI

U18
PCH_SPI_CS0# /CS
PCH_SPI_MISO_1 DO(IO1)
SPI_WP1# /WP(IO2)
GND
VCC
/HOLD(IO3)
CLK
DI(IO0)
SPI_HOLD1# 3.3K_0402_5% R73
PCH_SPI_CLK_1
PCH_SPI_MOSI_1
R72 3.3K_0402_5%
8MB SPI ROM for System BIOS
W25Q64FVSSIQ_SO8

U19 @
PCH_SPI_CS1# /CS
PCH_SPI_MISO_2 DO(IO1)
SPI_WP2# /WP(IO2)
GND
VCC
/HOLD(IO3)
CLK
DI(IO0)
SPI_HOLD2# 3.3K_0402_5% R76
PCH_SPI_CLK_2
PCH_SPI_MOSI_2
R75 3.3K_0402_5%
placeholder for U19 is just reserved as back-up
W25Q16CVSSIG_SO8
S IC FL 8M W25Q80BVSSIG SOIC 8P

R74 4.7K_0402_5%
PCH_GPIO19
keep R still be stuff for safety SMT, then check if it is okay to remove or not

R275 10K_0402_5%
PCH_GPIO21
@ R276 10K_0402_5%

Swichable Graphic Supported	
YES	Low
NO	High

Check with SW if this selection is still required

In accordance with design guide 2.0 page 274, if default boot destination is SPI, no external pull-up/-down resistors on the board are necessary.

Boot BIOS Destination Selection		
Routing	GTN1#/GPIO51 (BBS1)	SATA1GP/GPIO19 (BBS0)
Reserved	0	1
Reserved	1	0
LPC	0	0
* SPI	1	1

Security Classification	Compal Secret Data		
Issued Date	2012/07/29	Deciphered Date	Date of EOP

Compal Electronics, Inc.
Title: PCH (1/9) SATA,HDA,SPI, LPC, XDP
Size: Custom
Document Number: Ezel_CX MB_LA-A001P
Rev: 1.0
Date: Wednesday, March 13, 2013
Sheet 13 of 64

since no need PCIe to LAN,
1. let PCIe TX/RX as NC
2. PU WAKE# to 3V_Sus with 10k

Mini-Card for WiFi

Card Reader

UPCH1B @

PCI-E*

SMBUS

Controller Link

CLOCKS

FLEX CLOCKS

COUGARPOINT_FCBGA989

Directly to WLAN on JMINI1

for S3 Power Reduction

Below items had been assigned to function field 2.3, which is for DRAM

1. SO-DIMM
2. Click-Pad

1. Thermal Sensor for DRAM
2. Thermal Sensor for VRAM
3. dGPU
4. EC

blocking circuit, for dGPU SRC request

for WLAN(JMIN1)

Card Reader on D/B

dGPU, N14P-GT

NOT used in Full Clock Integration mode

CLKIN_GND1_P (BG30) and CLKIN_GND1_N (BJ30) can share the same PD resistor. <Design Guide 2.0 Page 395>

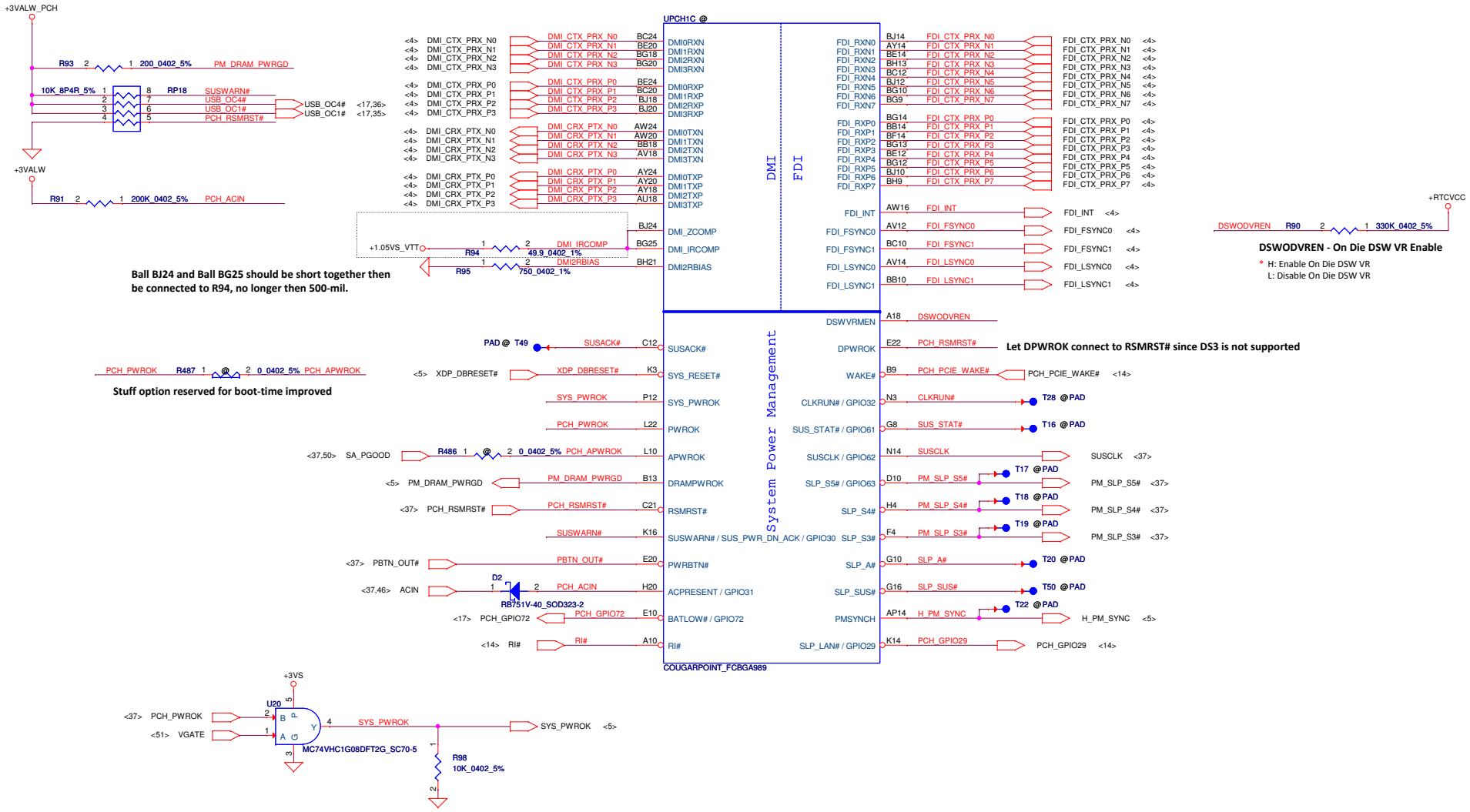
need to align with SW team to see how to deal with these if no clock output required

ALL Unused GPIO will be set asto GPO, and PU/PD resistors are only stuff for first version

dGPU is present or not	
UMA	High
W/dGPU	Low

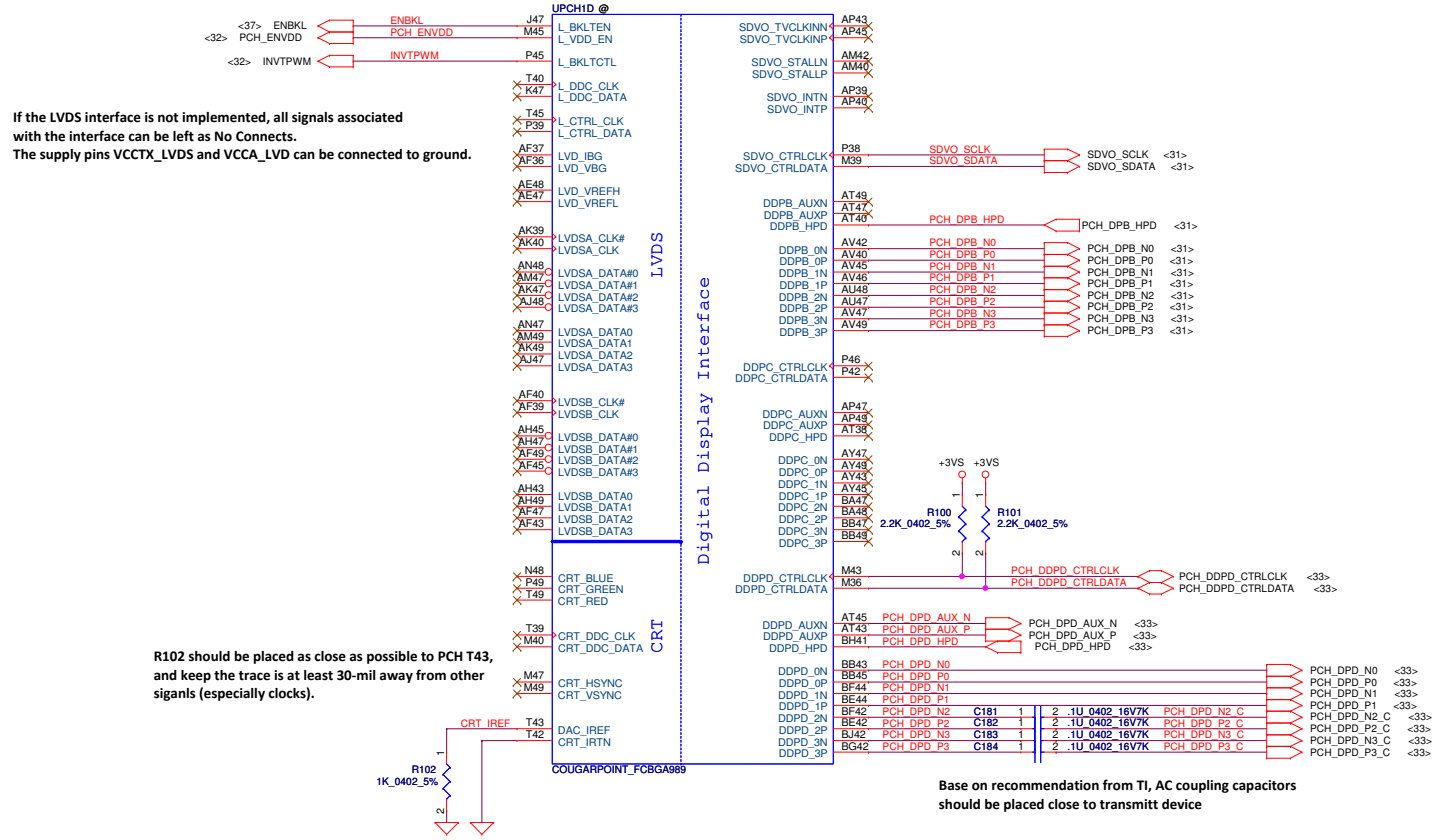
Security Classification	Compal Secret Data		
Issued Date	2012/07/29	Deciphered Date	Date of EOP

Compal Electronics, Inc.			
Title: PCH (2/9) PCIE, SMBUS, CLK			
Size: Custom	Document Number: Ezel_CX MB_LA-A001P		Rev: 1.0
Date: Wednesday, March 13, 2013	Sheet 14 of 64		



Security Classification	Compal Secret Data		
Issued Date	2012/07/29	Deciphered Date	Date of EOP

Compal Electronics, Inc.			
Title	PCH (3/9) DMI,FDI,PM		
Size: Custom	Document Number: Ezel_CX MB_LA-A001P		Rev: 1.0
Date: Wednesday, March 13, 2013	Sheet 15 of 64		



Security Classification	Compal Secret Data		
Issued Date	2012/07/29	Deciphered Date	Date of EOP

Compal Electronics, Inc.			
Title	PCH (4/9) LVDS,CRT,DP,HDMI		
Size: Custom	Document Number: Ezel_CX MB_LA-A001P		Rev: 1.0
Date: Wednesday, March 13, 2013	Sheet 16 of 64		

ALL Unused GPIO will be set asto GPO,
and PU/PD resistors are only stuff for first version

+3VS

10K_8P4R_5% RP19 PCH_GPIO55 PCH_GPIO54 PCH_GPIO52 PCH_GPIO51

10K_8P4R_5% RP20 PCH_GPIO3 PCH_GPIO2 PCH_GPIO53

10K_8P4R_5% RP21 PCI_PIRQA# PCI_PIRQB# PCI_PIRQD# PCI_PIRQC#

+3VS

10K_0402_5% R103 dGPU@ VGA_ON — VGA_ON <14,22,37,43,54>

10K_0402_5% R105 TOUCH_PANEL_INT#

UPCH1E @

RSVD: TP1 TP2 TP3 TP4 TP5 TP6 TP7 TP8 TP9 TP10 TP11 TP12 TP13 TP14 TP15 TP16 TP17 TP18 TP19 TP20 TP21 TP22 TP23 TP24

NVRAM: NV_CE#0 NV_CE#1 NV_CE#2 NV_CE#3 NV_DQS0 NV_DQS1 NV_DQ0 / NV_IO0 NV_DQ1 / NV_IO1 NV_DQ2 / NV_IO2 NV_DQ3 / NV_IO3 NV_DQ4 / NV_IO4 NV_DQ5 / NV_IO5 NV_DQ6 / NV_IO6 NV_DQ7 / NV_IO7 NV_DQ8 / NV_IO8 NV_DQ9 / NV_IO9 NV_DQ10 / NV_IO10 NV_DQ11 / NV_IO11 NV_DQ12 / NV_IO12 NV_DQ13 / NV_IO13 NV_DQ14 / NV_IO14 NV_DQ15 / NV_IO15 NV_ALE NV_CLE NV_RCOMP NV_RB# NV_RE#_WRB0 NV_RE#_WRB1 NV_WE#_CK0 NV_WE#_CK1

DMI,FDI Termination Voltage		
DF_TVS	PU, Set to 1	HR CPU NC
	PD, Set to 0	CR CPU PD

+1.8VS

R104 2.2K_0402_5%

DF_TVS R106 1K_0402_5% H_SNB_IVB# <5>

PCH_USB3_RX1_N PCH_USB3_RX2_N PCH_USB3_RX3_N

PCH_USB3_RX1_P PCH_USB3_RX2_P PCH_USB3_RX3_P

PCH_USB3_TX1_N PCH_USB3_TX2_N PCH_USB3_TX3_N_C C185 .1U_0402_16V7K

PCH_USB3_TX1_P PCH_USB3_TX2_P PCH_USB3_TX3_P_C C186 .1U_0402_16V7K

Base on recommendation from TI, AC coupling capacitors
should be placed close to transmitt device

PCI: PCI_PIRQA# PCI_PIRQB# PCI_PIRQC# PCI_PIRQD# — PIRQA# PIRQB# PIRQC# PIRQD#

PCH_GPIO50 PCH_GPIO52 PCH_GPIO54 — REQ1# / GPIO50 REQ2# / GPIO52 REQ3# / GPIO54

PCH_GPIO51 PCH_GPIO53 PCH_GPIO55 — GNT1# / GPIO51 GNT2# / GPIO53 GNT3# / GPIO55

PCH_GPIO2 PCH_GPIO3 TOUCH_PANEL_INT# PCH_GPIO5 — PIRQE# / GPIO2 PIRQF# / GPIO3 PIRQG# / GPIO4 PIRQH# / GPIO5

<32> TOUCH_PANEL_INT#

PAD T23 @ — PME#

PLT_RST# — PLTRST#

<36,37,42,5> PLT_RST#

<14> CLK_PCI_LPBACK
<37> CLK_PCI_LPC
<42> CLK_PCI_TPM

CLK_PCI_LPBACK R109 22_0402_5%
CLK_PCI_LPC R110 22_0402_5%
CLK_PCI_TPM R132 22_0402_5%
EMI@

CLK_PCI0 CLK_PCI1 CLK_PCI2 CLK_PCI3 CLK_PCI4

PAD T25 @
PAD T26 @

CLKOUT_PCI0 CLKOUT_PCI1 CLKOUT_PCI2 CLKOUT_PCI3 CLKOUT_PCI4

USB: USBP0N USBP0P USBP1N USBP1P USBP2N USBP2P USBP3N USBP3P USBP4N USBP4P USBP5N USBP5P USBP6N USBP6P USBP7N USBP7P USBP8N USBP8P USBP9N USBP9P USBP10N USBP10P USBP11N USBP11P USBP12N USBP12P USBP13N USBP13P

USB20_N0 USB20_P0 USB20_N1 USB20_P1 USB20_N2 USB20_P2 — USB20 External Port (Far Away from End-User) / USB30 External Port (Close to End-User) / Docking Port

USB20_N8 USB20_P8 USB20_N9 USB20_P9 USB20_N10 USB20_P10 USB20_N11 USB20_P11 USB20_N12 USB20_P12 — Mini Card (WLAN) / USB 2.0 Only External Port (on I/O Board) / CMOS Camera / Touch Panel / Sensor Hub

USBRBIAS# USBRBIAS R108 22.6_0402_1%

Connect USBRBIAS and USBRBIAS# (impedance= 50-ohm single-end) together first, then connect to R158 from USBRBIAS# (no longer than 500-mil). Keep-out 15-mil to other signals.

OC0# / GPIO59 OC1# / GPIO40 OC2# / GPIO41 OC3# / GPIO42 OC4# / GPIO43 OC5# / GPIO9 OC6# / GPIO10 OC7# / GPIO14

USB_OC0# USB_OC1# PCH_GPIO41 PCH_GPIO42 USB_OC4# PCH_GPIO9 PCH_GPIO10 PCH_GPIO14

<14,35> <15,35> <15,36> <14>

COUGARPOINT_FCBGA989

In accordance with design guide 2.0 page 274, if default boot destination is SPI, no external pull-up/-down resistors on the board are necessary.

need to set GPIO50 and GPIO54 as GPO to reduce external PU resistors

Boot BIOS Destination Selection		
Routing	GTN1#/GPIO51 (BBS1)	SATA1GP/GPIO19 (BBS0)
Reserved	0	1
Reserved	1	0
LPC	0	0
* SPI	1	1

+3VALW_PCH

<18> PCH_GPIO57
<18> PCH_GPIO12
<15> PCH_GPIO72
<14> PCH_GPIO73

PCH_GPIO57 PCH_GPIO12 PCH_GPIO72 PCH_GPIO73 RP22 10K_8P4R_5%

PCH_GPIO14 PCH_GPIO42 PCH_GPIO9 PCH_GPIO41 RP23 10K_8P4R_5%

ALL Unused GPIO will be set asto GPO,
and PU/PD resistors are only stuff for first version

Default for iRST supported

+3VS

PLT_RST# R481 0_0402_5% — PLT_RST_BUF# <34>

<37> iRST_RST# R482 0_0402_5% iRST_RST#_R

U21 MC74VHC1G08DFT2G_SC70-5 R112 100K_0402_5%

+3VS

<37> DGPU_HOLD_RST# R107 10K_0402_5% dGPU@ — DGPU_HOLD_RST# — PLTRST_VGA# <22>

U22 MC74VHC1G08DFT2G_SC70-5 R113 100K_0402_5% dGPU@

Security Classification	Compal Secret Data		
Issued Date	2012/07/29	Deciphered Date	Date of EOP

Compal Electronics, Inc.

Title: PCH (5/9) PCI, USB, NVRAM

Size	Document Number	Rev
Custom	Ezel_CX MB_LA-A001P	1.0
Date: Wednesday, March 13, 2013	Sheet 17 of 64	

+3VALW_PCH

R114 4.7K_0402_5%

PCH_GPIO28

On-Die PLL Voltage Regulator

for VccVRM

* H: enable On-Die PLL Voltage Regulator
L: disable On-Die PLL Voltage Regulator

Debug Port DG 1.2 PH 4.7K +3VALW_PCH

+3VALW_PCH

R272 10K_0402_5%

PCH_GPIO24

@R273 10K_0402_5%

Check with SW if this selection is still required

DDR3/DDR3L	
DDR3	High
DDR3L	Low

+3VS

R277 10K_0402_5%

PCH_GPIO71

@R278 10K_0402_5%

Check with SW if this selection is still required

GDDR3/GDDR5	
GDDR3	Low
GDDR5	High

+3VS

R115 10K_0402_5% @

PCH_GPIO69

R118 10K_0402_5%

+3VS

R116 10K_0402_5%

PCH_GPIO70

R119 10K_0402_5% @

For common BIOS code need to define

Project Code	GPIO69	GPIO70
	0	0
w/TPM	0	1
	1	0
	1	1

Currently, to be the same configuration as Sage, use GPIO69 and GPIO70 to define SKUs has TPM solution or not. updated on 2013/01/15

mSATA_DET#

ESD@ C472 0.1U_0402_16V4Z

Request from ESD need to place this compnent as close to PCH as possible

ALL Unused GPIO will be set asto GPO, and PU/PD resistors are only reserved for first version

+3VS

10K_0402_5% R125 EC_KBRST#

10K_8P4R_5% RP25 PCH_GPIO6 PCH_GPIO1 PCH_GPIO48

10K_8P4R_5% RP28 PCH_GPIO0 PCH_GPIO36

10K_8P4R_5% RP43 PCH_GPIO49 PCH_GPIO34 PCH_GPIO37 PCH_GPIO27

GPIO71 is for GDDR3/GDDR5 selection. PU for GDDR5 only.

ALL Unused GPIO will be set asto GPO, and PU/PD resistors are only stuff for first version

+3VALW_PCH

PU resisotr for GPIO8 will be disabled after RSMRST# de-assertion.

R134 1K_0402_5% EC_LID_OUT#

+3VS

R271 UMA@ 10K_0402_5%

R270 dGPU@ 10K_0402_5%

OPTIMUS_EN#

NV Optimus Enable	
W/Optimus	Low
W/O Optimus	High

UPCH1F @

PCH_GPIO0	T7	BMBUSY# / GPIO0	
PCH_GPIO1	A42	TACH1 / GPIO1	
PCH_GPIO6	H36	TACH2 / GPIO6	
<37> EC_SCI#	EC_SCI#	E38	TACH3 / GPIO7
		C10	GPIO8
<17> PCH_GPIO12	PCH_GPIO12	C4	LAN_PHY_PWR_CTRL / GPIO12
<37> EC_LID_OUT#	EC_LID_OUT#	G2	GPIO15
<13,34> mSATA_DET#	mSATA_DET#	U2	SATA4GP / GPIO16
<37,53,54> VGA_PWROK	VGA_PWROK	D40	TACH0 / GPIO17
On Board DRAM Flag→	PCH_GPIO22	T5	SCLOCK / GPIO22
	PCH_GPIO24	E8	GPIO24 / MEM_LED
	PCH_GPIO27	E16	GPIO27
	PCH_GPIO28	P8	GPIO28
	PCH_GPIO34	K1	STP_PCI# / GPIO34
<32> SNSR_HUB_PWR_GATE	SNSR_HUB_PWR_GATE	K4	GPIO35
	PCH_GPIO36	V8	SATA2GP / GPIO36
	PCH_GPIO37	M5	SATA3GP / GPIO37
	OPTIMUS_EN#	N2	SLOAD / GPIO38
On Board DRAM Flag→	PCH_GPIO39	M3	SDATAOUT0 / GPIO39
	PCH_GPIO48	V13	SDATAOUT1 / GPIO48
	PCH_GPIO49	V3	SATA5GP / GPIO49
<17> PCH_GPIO57	PCH_GPIO57	D6	GPIO57

GPIO

		A4	VSS_NCTF_1
		A44	VSS_NCTF_2
		A45	VSS_NCTF_3
		A46	VSS_NCTF_4
		A5	VSS_NCTF_5
		A6	VSS_NCTF_6
		B3	VSS_NCTF_7
		B47	VSS_NCTF_8
		BD1	VSS_NCTF_9
		BD49	VSS_NCTF_10
		BE1	VSS_NCTF_11
		BE49	VSS_NCTF_12
		BF1	VSS_NCTF_13
		BF49	VSS_NCTF_14

NCTF

		BG2	VSS_NCTF_15
		BG48	VSS_NCTF_16
		BH3	VSS_NCTF_17
		BH47	VSS_NCTF_18
		BJ4	VSS_NCTF_19
		BJ44	VSS_NCTF_20
		BJ45	VSS_NCTF_21
		BJ46	VSS_NCTF_22
		BJ5	VSS_NCTF_23
		BJ6	VSS_NCTF_24
		C2	VSS_NCTF_25
		C48	VSS_NCTF_26
		D1	VSS_NCTF_27
		D49	VSS_NCTF_28
		E1	VSS_NCTF_29
		E49	VSS_NCTF_30
		F1	VSS_NCTF_31
		F49	VSS_NCTF_32

COUGARPOINT_FCBGA989

TACH4 / GPIO68	C40	SNSR_HUB_DFU_EN#	SNSR_HUB_DFU_EN# <32>
TACH5 / GPIO69	B41	PCH_GPIO69	
TACH6 / GPIO70	C41	PCH_GPIO70	
TACH7 / GPIO71	A40	PCH_GPIO71	
A20GATE	P4		
PECI	AU16		
RCIN#	P5	EC_KBRST#	EC_KBRST# <37> **Ctrl+Alt+Del**
PROCPWRGD	AY11	H_CPUPWRGD	H_CPUPWRGD <5>
THRMTRIP#	AY10	PCH_THRMTRIP# R124 390_0402_5% H_THRMTRIP#	H_THRMTRIP# <5>
INIT3_3V#	T14		
NC_1	AH8		
NC_2	AK11		
NC_3	AH10		
NC_4	AK10		
NC_5	P37		

CPU/MISC

add definition for ELPIDA B-Die (old die)

On Board DRAM Configuration	GPIO23	GPIO22
ELPIDA(F-Die) 512MbX8	0	0
ELPIDA(B-Die) 512MbX8	0	1

updated on 2013/01/15

+3VS

R126 10K_0402_5%

PCH_GPIO39

R133 10K_0402_5% @

+3VS

R127 10K_0402_5% @

PCH_GPIO23

R130 10K_0402_5% @

PCH_GPIO23

+3VS

R128 10K_0402_5% @

<13> PCH_GPIO22

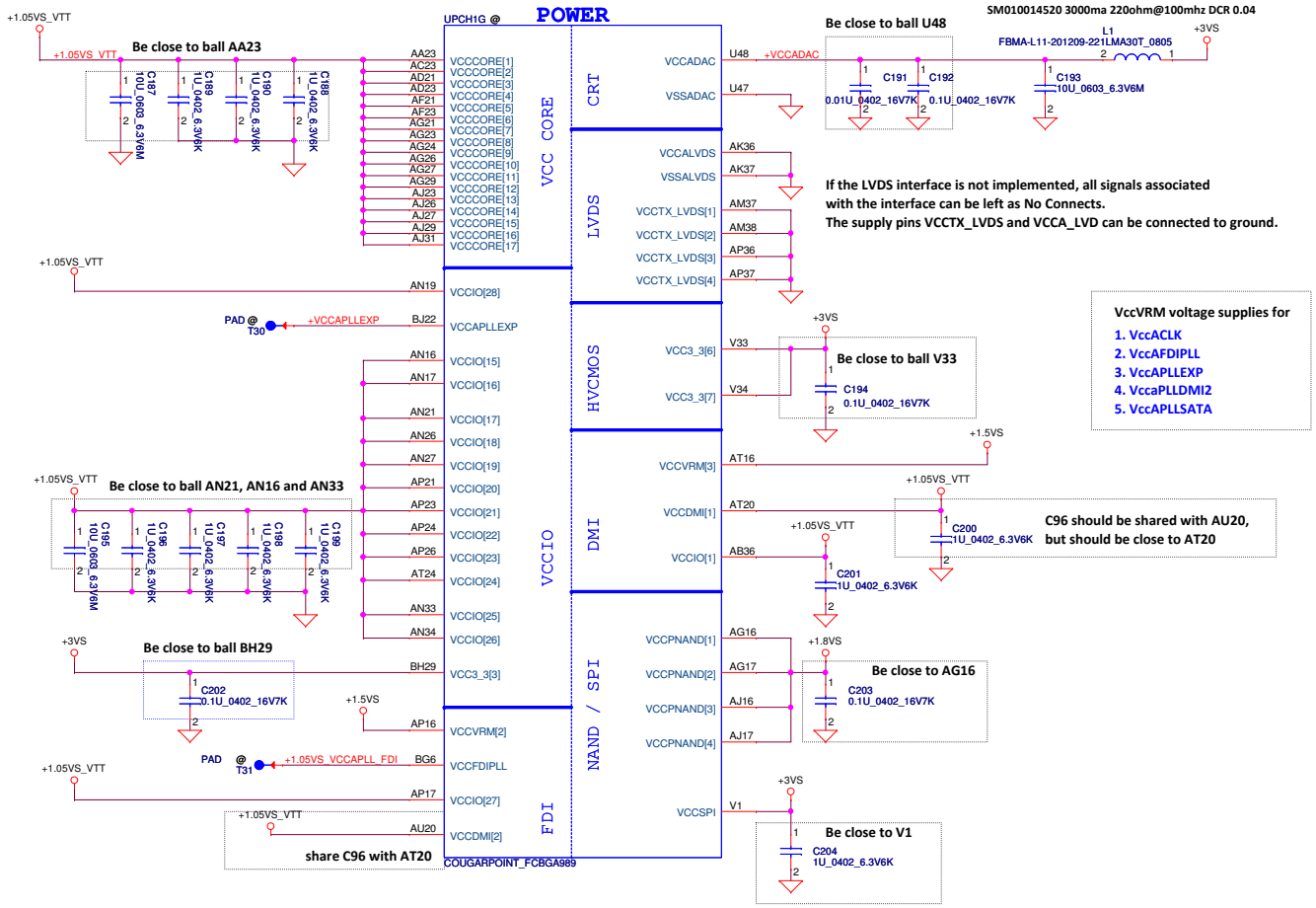
R131 10K_0402_5% @

PCH_GPIO39 is reserved only for first version

Being configured by ALT Group

Security Classification	Compal Secret Data		
Issued Date	2012/07/29	Deciphered Date	Date of EOP

Compal Electronics, Inc.			
Title	PCH (6/9) GPIO, CPU, MISC		
Size: Custom	Document Number: Ezel_CX MB_LA-A001P		Rev: 1.0
Date: Wednesday, March 13, 2013	Sheet 18 of 64		



Refer to IntelR 7 Series / C216 Chipset Family Platform Controller Hub (PCH) External Design Specification (EDS) Revision 2.1

PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current(A)	
V_PROC_IO	1.05	0.002	Processor I/O
V5REF	5	0.001	PCH Core Well Reference Voltage
V5REF_Sus	5	0.001	Suspend Well Reference Voltag
Vcc3_3	3.3	0.178	I/O Buffer Voltage
VccADAC	3.3	0.063	Display DAC Analog Power. This power is supplied by the core well.
VccADPLLA	1.05	0.075	Display PLL A power
VccADPLLB	1.05	0.075	Display PLL B power
VccCore	1.05	1.73	Internal Logic Voltage
VccDMI	1.05	0.047	DMI Voltage
VccIO	1.05	3.799	Core Well I/O buffers
VccASW	1.05	0.803	1.05 V Supply for Intel Management Engine and Integrated LAN
VccSPI	3.3	0.01	3.3 V Supply for SPI Controller Logic
VccDSW3_3	3.3	0.001	3.3v supply for Deep Sx well
VccDFTERN (VccPNAND)	1.8	0.002	1.8V power supply for DF_TVS
VccRTC	3.3	6 uA	RTC Battery Voltage
VccSus3_3	3.3	0.065	Suspend Well I/O Buffer Voltage
VccSusHDA	3.3	0.01	High Definition Audio Controller Suspend Voltage
VccVRM	1.5	0.147	1.5 V Internal PLL and VRMs
VccCLKDMI	1.05	0.075	DMI differential Clock Buffer Voltage
VccSSC	1.05	0.095	Spread Modulators Power Supply
VccDIFFCLKN	1.05	0.05	Differential Clock Buffers Power Supply
VccALVDS	3.3	0.001	Analog power supply for LVDS (Mobile Only)
VccTX_LVDS	1.8	0.04	I/O power supply for LVDS (Mobile Only)

Security Classification	Compal Secret Data		
Issued Date	2012/07/29	Deciphered Date	Date of EOP

Compal Electronics, Inc.			
Title	PCH (7/9) PWR		
Size: Custom	Document Number: Ezel_CX MB_LA-A001P		Rev: 1.0
Date: Wednesday, March 13, 2013	Sheet 19 of 64		

C205is only stuff for first version,
then check the feasibility to remove them

VccVRM voltage supplies for
1. VccACLK
2. VccAFDIPLL
3. VccAPLLEXP
4. VccaPLLDMI2
5. VccAPLLSATA

AL29 should be connected to shared with C80, C86, C87, C88, C89 and 90.

Change to OS-CON

Part Number	Description	ESR
SF000002Z00	S_A-P_CAP 330U 2.5V M 6.3X4.2 R17M VLPS	17mΩ

C224 and C224 is only stuff for first version,
then check the feasibility to remove them

short J16 and J17 for suspend power well of PCH as default, then check Erp Lot 6 result to see if Q39 and U28 are required or not

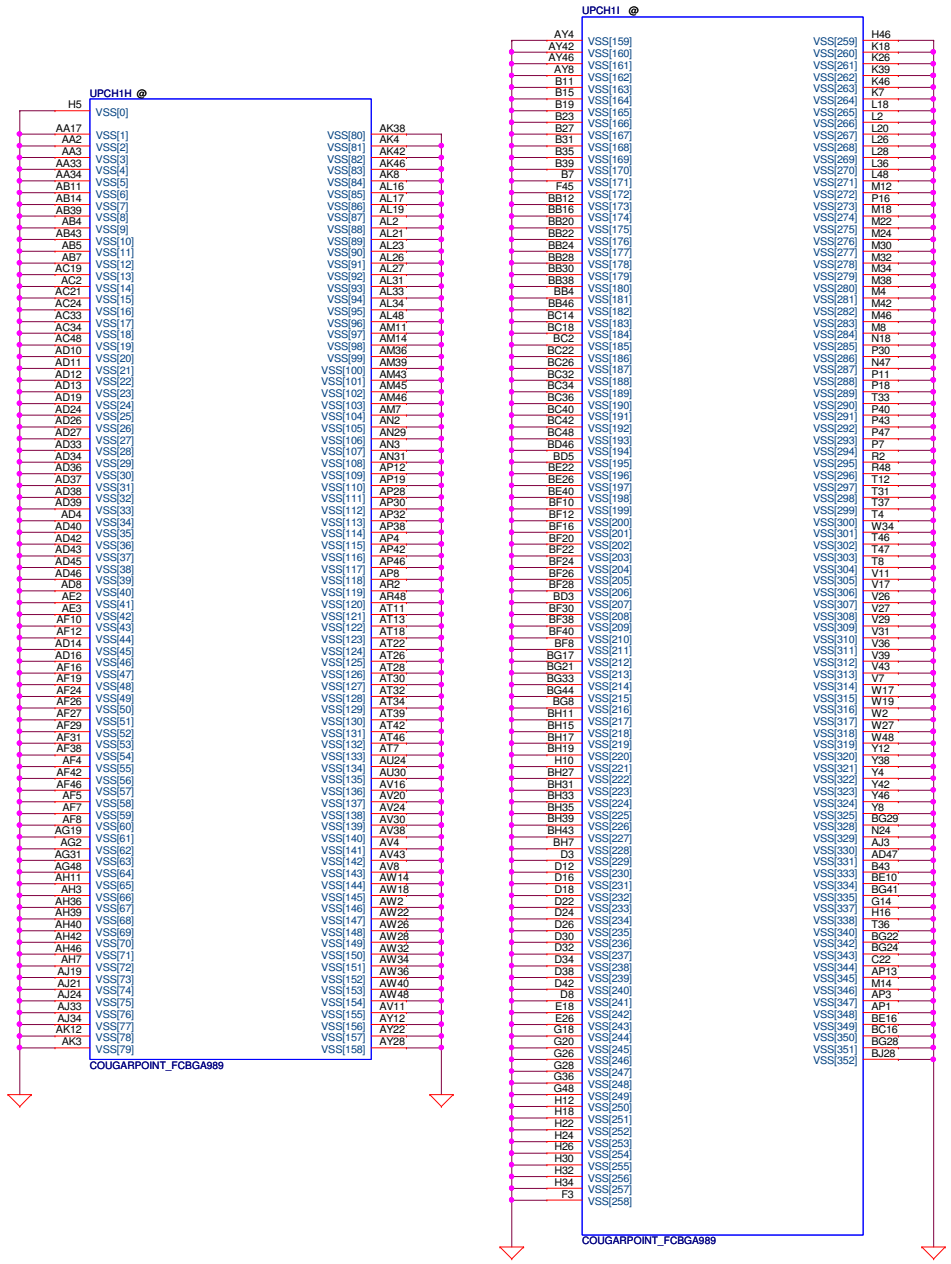
remove R479 if no any sequence issue

Check sequence between VCC5REF_SUS and VCCSUS3_3

C235 and C238is only stuff for first version,
then check the feasibility to remove them

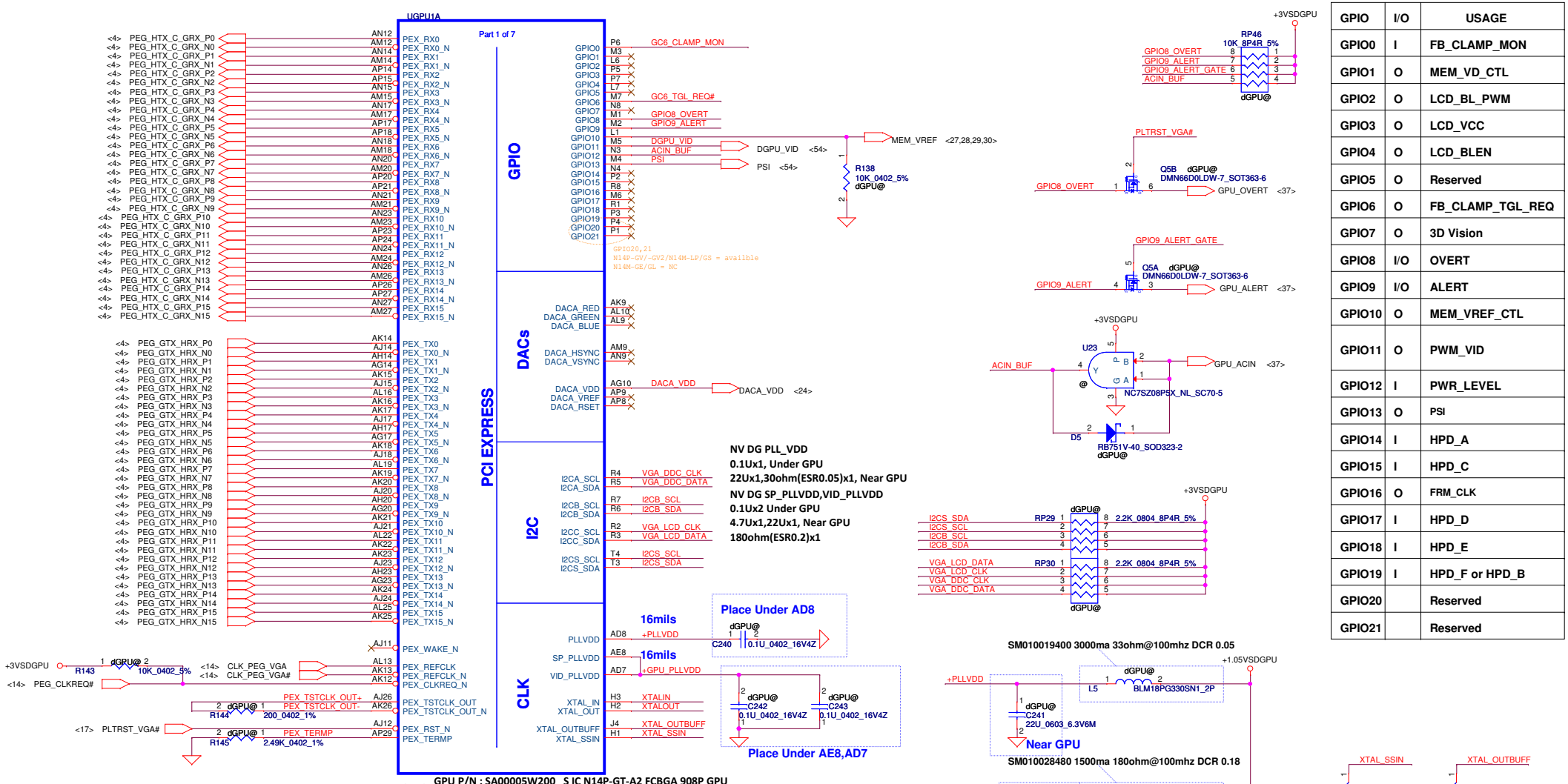
Security Classification	Compal Secret Data		
Issued Date	2012/07/29	Deciphered Date	Date of EOP

Compal Electronics, Inc.			
Title: PCH (8/9) PWR			
Size: Custom	Document Number: Ezel_CX MB_LA-A001P		Rev: 1.0
Date: Wednesday, March 13, 2013	Sheet 20 of 64		



Security Classification	Compal Secret Data		
Issued Date	2012/07/29	Deciphered Date	Date of EOP

Compal Electronics, Inc.			
Title	PCH (9/9) VSS		
Size	Document Number		Rev
Custom	Ezel_CX MB_LA-A001P		1.0
Date:	Wednesday, March 13, 2013	Sheet	21 of 64

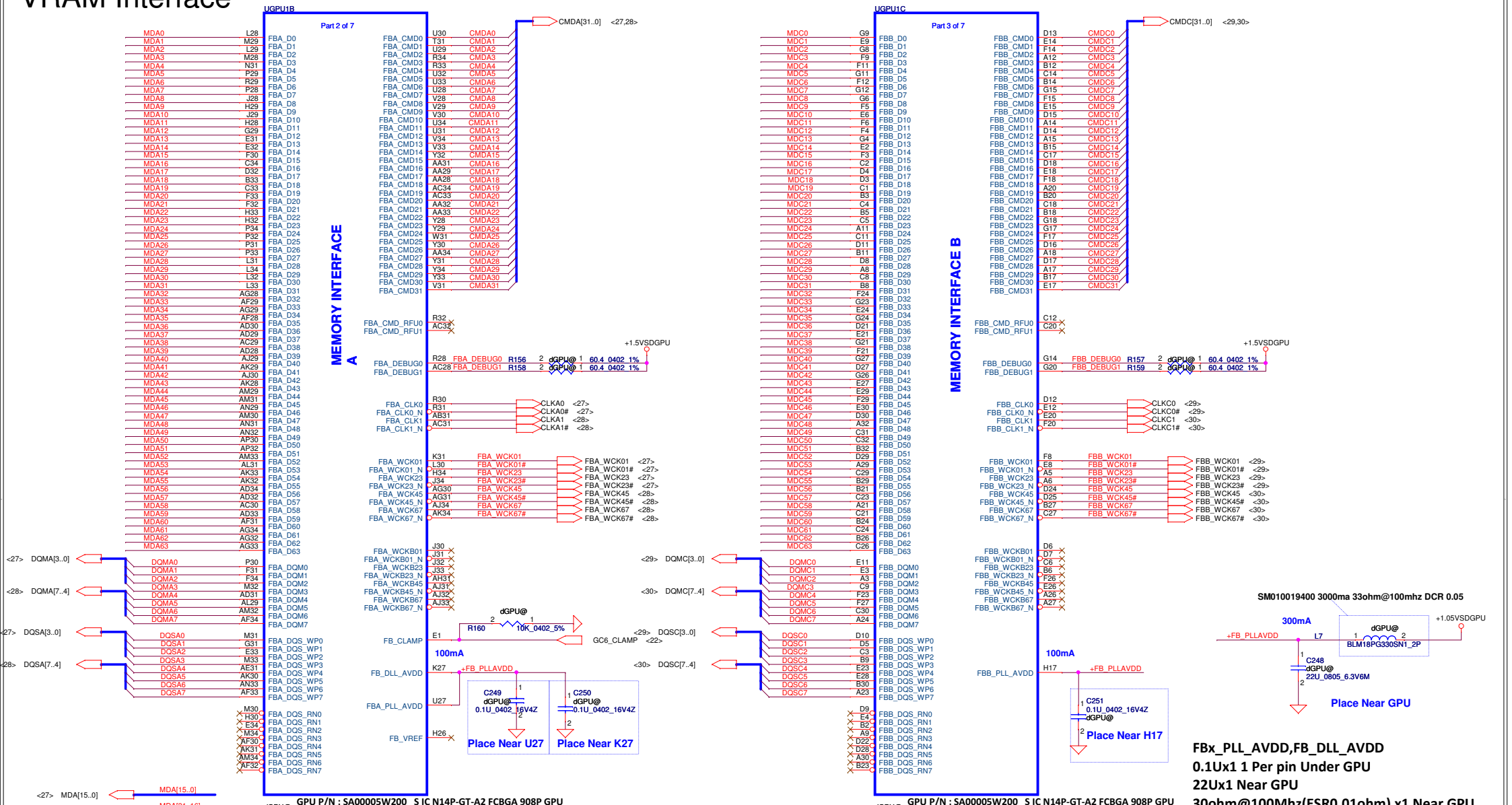


GPIO	I/O	USAGE
GPIO0	I	FB_CLAMP_MON
GPIO1	O	MEM_VD_CTL
GPIO2	O	LCD_BL_PWM
GPIO3	O	LCD_VCC
GPIO4	O	LCD_BLEN
GPIO5	O	Reserved
GPIO6	O	FB_CLAMP_TGL_REQ
GPIO7	O	3D Vision
GPIO8	I/O	OVERT
GPIO9	I/O	ALERT
GPIO10	O	MEM_VREF_CTL
GPIO11	O	PWM_VID
GPIO12	I	PWR_LEVEL
GPIO13	O	PSI
GPIO14	I	HPD_A
GPIO15	I	HPD_C
GPIO16	O	FRM_CLK
GPIO17	I	HPD_D
GPIO18	I	HPD_E
GPIO19	I	HPD_F or HPD_B
GPIO20		Reserved
GPIO21		Reserved

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	Deciphered Date	Date of EOP	Title: N14P PEG 1/9

Size: Custom	Document Number: Ezel_CX MB_LA-A001P		Rev: 1.0
Date: Wednesday, March 13, 2013	Sheet 22 of 64		

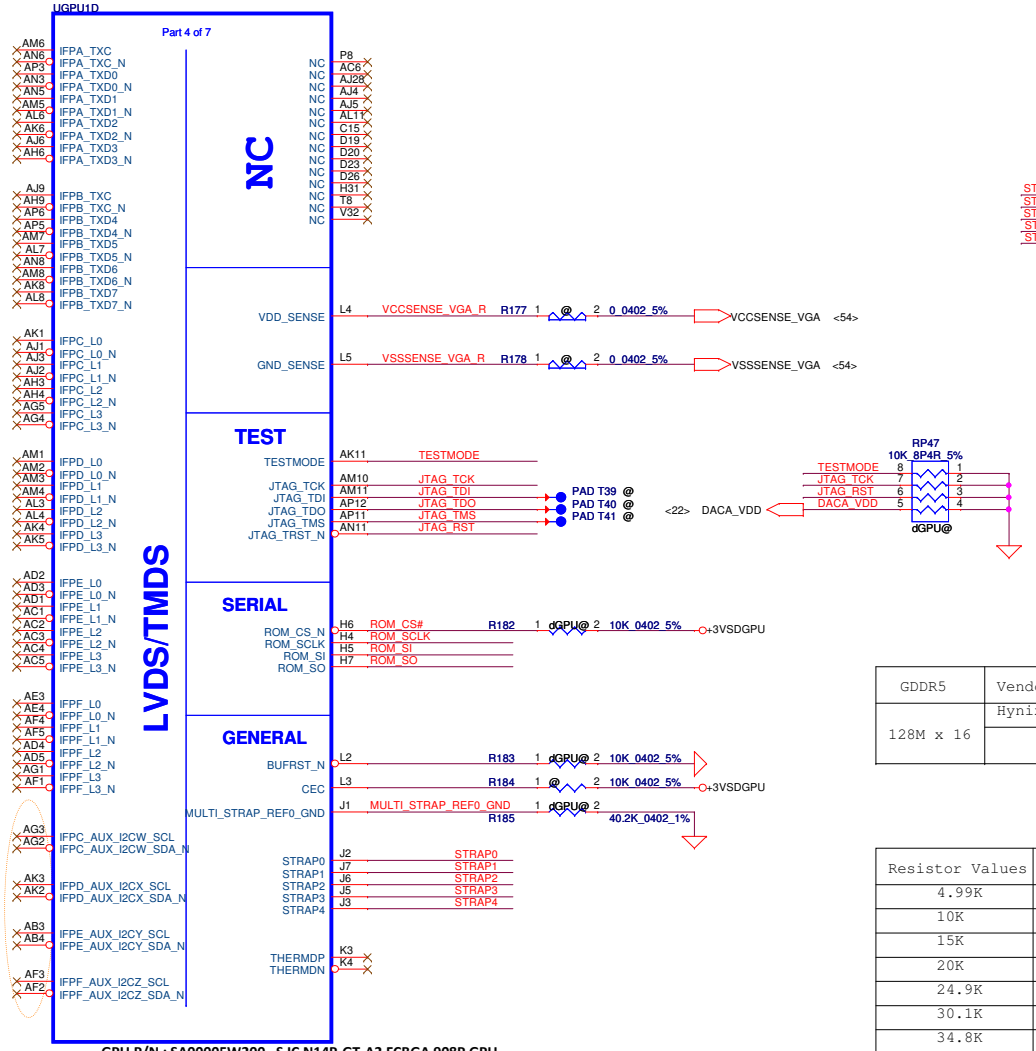
VRAM Interface



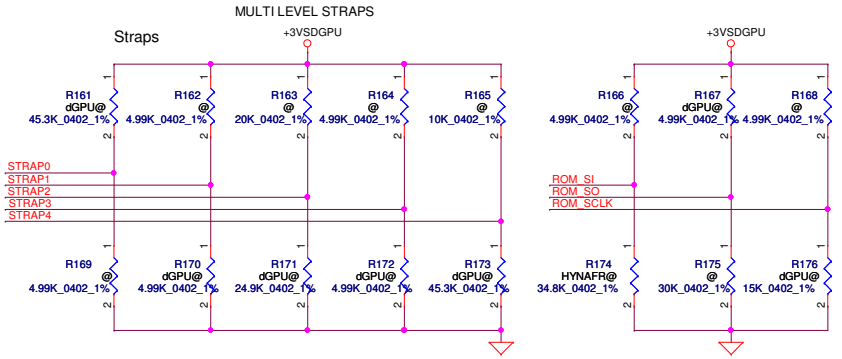
FBx_PLL_AVDD,FB_DLL_AVDD
0.1Ux1 1 Per pin Under GPU
22Ux1 Near GPU
30ohm@100Mhz(ESR0.01ohm) x1 Near GPU

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/24	Deciphered Date	Date of EOP	Title: N14P VRAM 2/9

Size: Custom	Document Number: Ezel_CX MB_LA-A001P		Rev: 1.0
Date: Wednesday, March 13, 2013	Sheet 23 of 64		



dGPU@ GPU P/N : SA00005W200 S IC N14P-GT-A2 FCBGA 908P GPU
Use N13P symbol.



VRAM BOM Config **VRAM P/N**

128Mx16x8 **HYN** **64*32** SA00004GD50(S IC D5 64M32/2.5G H5GQ2H24AFR-T2C ABO!)

GDDR5	Vendor	Strap	ROM_SI
128M x 16	Hynix	0x4	24.9K

For N14P-GT-A2(QS) strap table **Device ID : 0xFE4**

GPU	WCK Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N14P-GT	2.5GHZ	128M*16	Hynix	R PU 45K	R PD 5K	R PD 25K	R PD 5K	R PD 45K	R PD 25K	R PU 5K	R PD 15K

Resistor Values	Pull-up	Pull-down
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

STRAP0	USER[3:0]
STRAP1	3GIO_PADCFG_LUT_ADR[3:0]
STRAP2	PCI_DEVID[3:0]
STRAP3	SOR[3:0]
STRAP4	PEG_SPEED_CHANGE_GEN3, PEX_MAX_SPEED,DP_PLLVDD33V
ROM_SCLK	PCI_DEV[4],SUB_VENDOR, PCI_DEV[5],PEX_PLL_EN_TERM
ROM_SI	RAM_CFG[3:0]
ROM_SO	FB_BAR_SIZE[1:0],SMB_ ALT_ADDR, VGA_DEVICE

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	Date of EOP

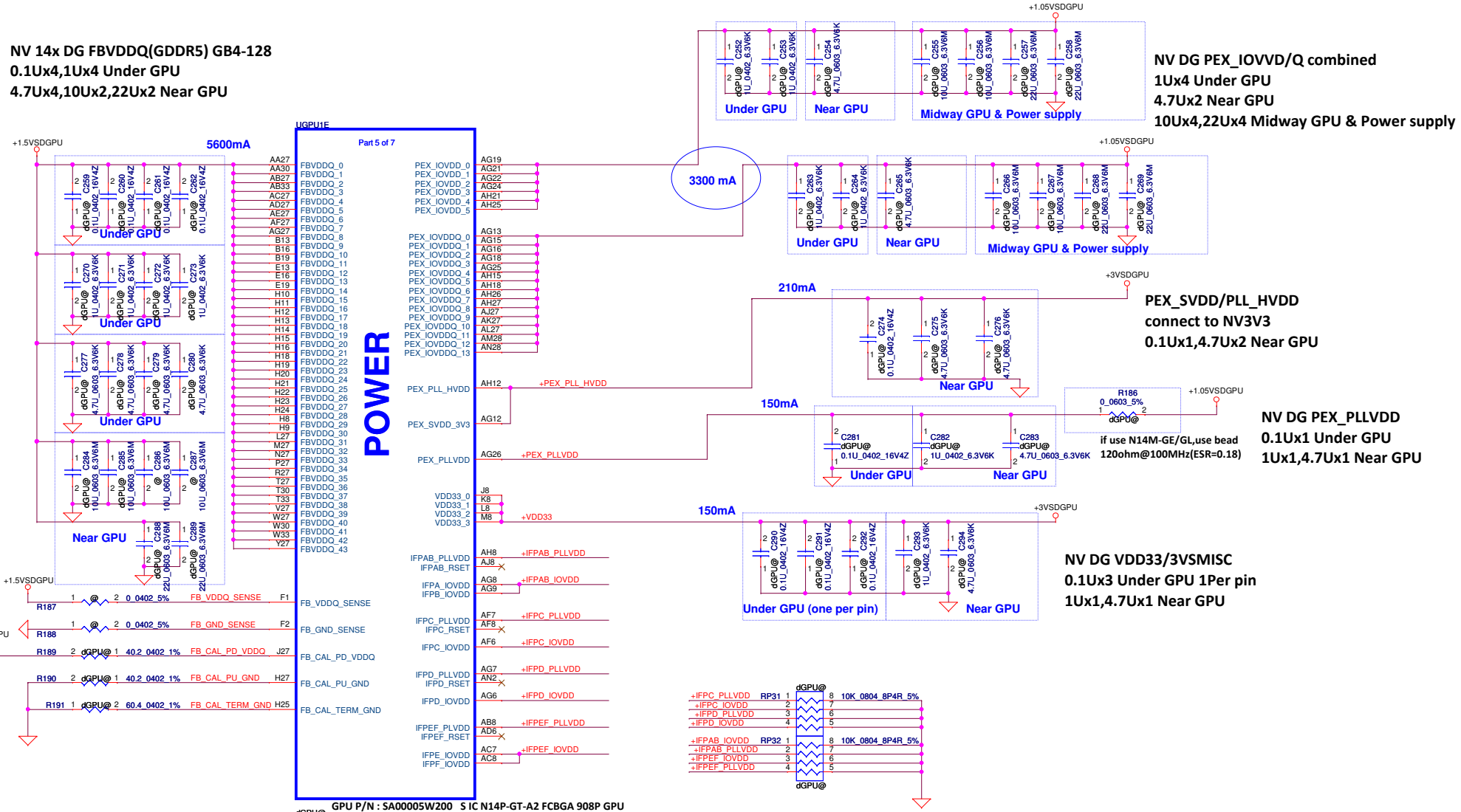
Compal Electronics, Inc.

Title: N14P LVDS 3/9

Size: Custom | Document Number: Ezel_CX MB_LA-A001P | Rev: 1.0

Date: Wednesday, March 13, 2013 | Sheet 24 of 64

NV 14x DG FBVDDQ(GDDR5) GB4-128
0.1Ux4,1Ux4 Under GPU
4.7Ux4,10Ux2,22Ux2 Near GPU



dGPU@ GPU P/N : SA00005W200 S IC N14P-GT-A2 FCBGA 908P GPU
Use N13P symbol.

NV DG PEX_IOVVD/Q combined
1Ux4 Under GPU
4.7Ux2 Near GPU
10Ux4,22Ux4 Midway GPU & Power supply

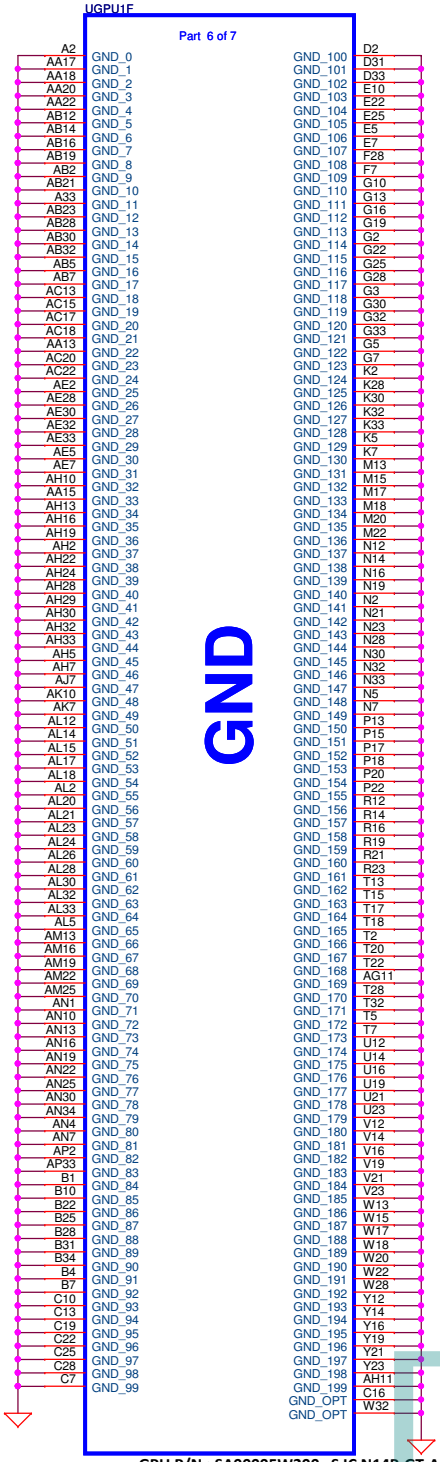
PEX_SVDD/PLL_HVDD
connect to NV3V3
0.1Ux1,4.7Ux2 Near GPU

NV DG PEX_PLLVDD
0.1Ux1 Under GPU
1Ux1,4.7Ux1 Near GPU
if use N14M-GE/GL,use bead 120ohm@100MHz(ESR=0.18)

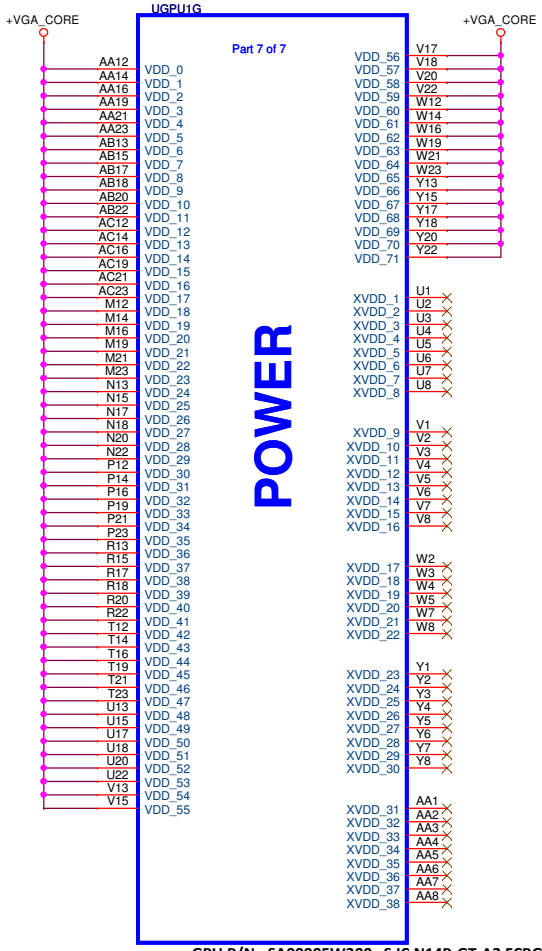
NV DG VDD33/3VSMISC
0.1Ux3 Under GPU 1Per pin
1Ux1,4.7Ux1 Near GPU

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	Date of EOP

Compal Electronics, Inc.			
Title: N14P POWER & GND 4/9			
Size: Custom	Document Number: Ezel_CX MB_LA-A001P		Rev: 1.0
Date: Wednesday, March 13, 2013	Sheet 25 of 64		



dGPU@ GPU P/N : SA00005W200 S IC N14P-GT-A2 FCBGA 908P GPU
Use N13P symbol.



N14P-GT EDP 45A

dGPU@ GPU P/N : SA00005W200 S IC N14P-GT-A2 FCBGA 908P GPU
Use N13P symbol.

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	Date of EOP

Compal Electronics, Inc.

Title: N14P POWER & GND 5/9

Size	Document Number	Rev
Custom	Ezel_CX MB_LA-A001P	1.0

Date: Wednesday, March 13, 2013 Sheet 26 of 64

Memory Partition A Lower 32 Bit

TOP / M3

BOT / M501

GDDR5 Mode H Mapping

Address	DATA Bus 0..31	DATA Bus 32..63
CMD0	CS#	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE#	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI#	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS#	
CMD13	RST#	
CMD14	CKE#	
CMD15	CAS#	
CMD16		CS#
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE#
CMD22		A7_A8
CMD23		A6_A11
CMD24		ABI#
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS#
CMD29		RST#
CMD30		CKE#
CMD31		CAS#

U5 — HYNAFR@ SA00004GD50 — S IC D5 64M32/2.5G H5GQ2H24AFR-T2C ABO!

U6 — HYNAFR@ SA00004GD50 — S IC D5 64M32/2.5G H5GQ2H24AFR-T2C ABO!

U7 — HYNAFR@ SA00004GD50 — S IC D5 64M32/2.5G H5GQ2H24AFR-T2C ABO!

U8 — HYNAFR@ SA00004GD50 — S IC D5 64M32/2.5G H5GQ2H24AFR-T2C ABO!

U5 / U6: H5GQ1H24AFR-T2L_BGA170, SA00004GD50 @, 170-BALL SGRAM GDDR5

建議線路
0.1ux6,1ux4,10ux1 FBVDDQ
1ux4,10ux1 FBVDD
for 2pcs VRAM

External VRAM Thermal Sensor

SA00003PU00
S IC W83L771AWG-2 TSSOP 8P SENSOR

U24 — W83L771AWG-2 TSSOP8P — SA00003PU00 — dGPU@

EC_SMB_CK2 <14,22,37>
EC_SMB_DA2 <14,22,37>

Security Classification	Compal Secret Data	
Issued Date	2011/06/24	Deciphered Date / Date of EOP

Compal Electronics, Inc.

Title: N14P GDDR5 6/9

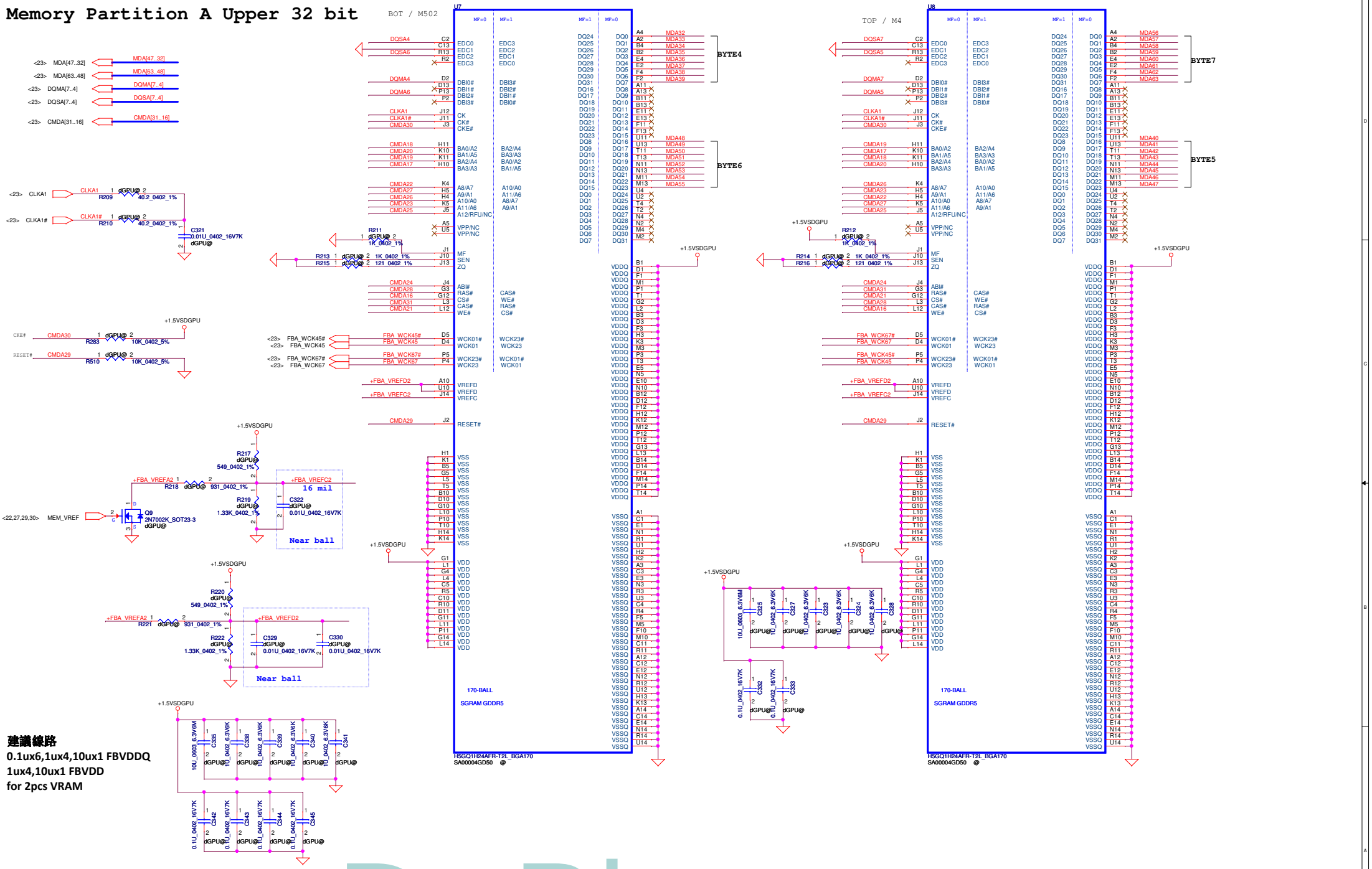
Size: Custom | Document Number: Ezel CX MB LA-A001P | Rev: 1.0

Date: Wednesday, March 13, 2013 | Sheet 27 of 64

Memory Partition A Upper 32 bit

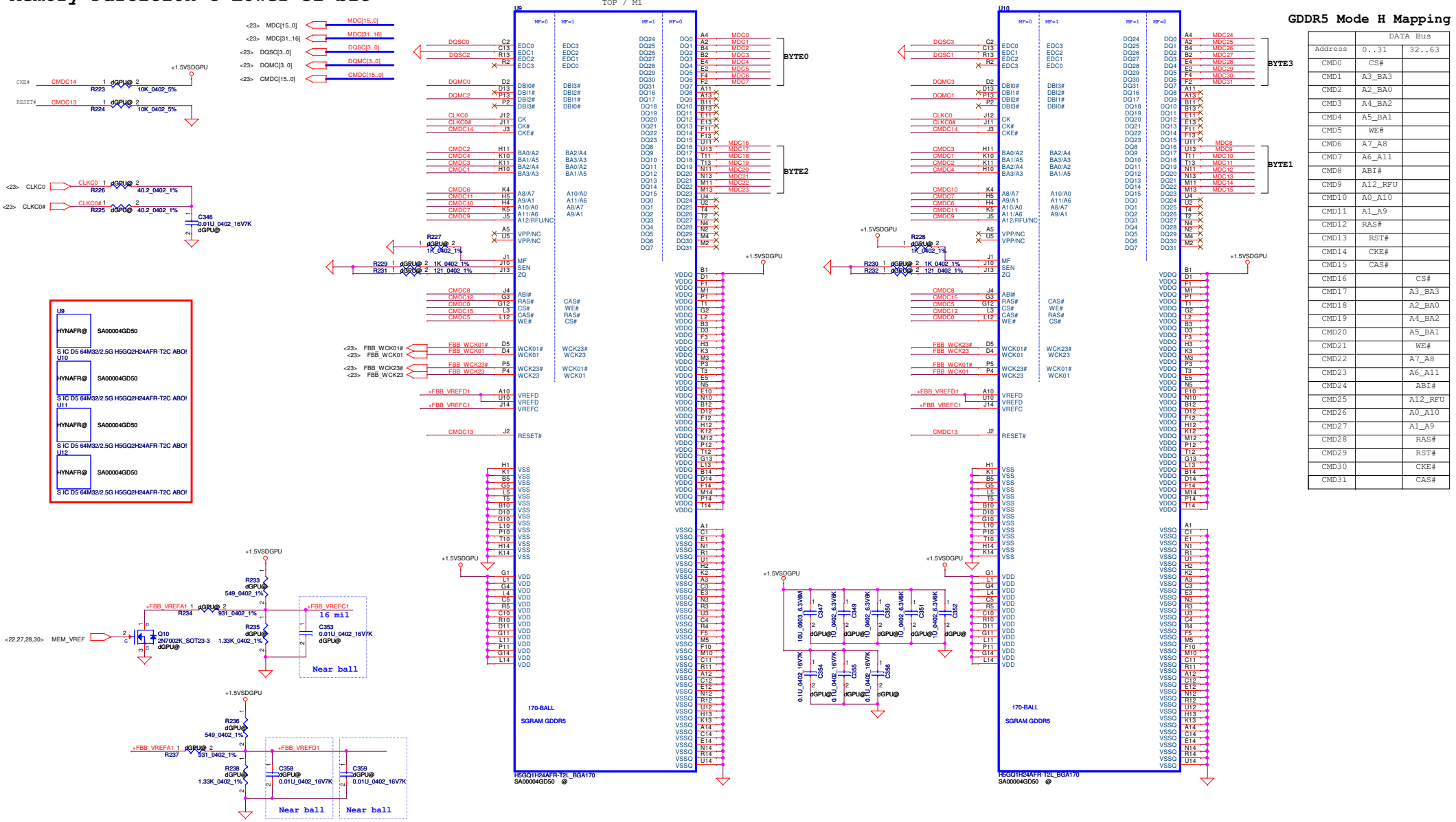
BOT / M502

TOP / M4



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	Deciphered Date	Date of EOP	Title: N14P GDDR5 7/9
			Size: Custom; Document Number: Ezel_CX MB_LA-A001P; Rev: 1.0
			Date: Wednesday, March 13, 2013; Sheet 28 of 64

Memory Partition C Lower 32 bit



GDDR5 Mode H Mapping

Address	DATA Bus 0..31	DATA Bus 32..63
CMD0	CS#	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE#	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI#	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS#	
CMD13	RST#	
CMD14	CKE#	
CMD15	CAS#	
CMD16		CS#
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE#
CMD22		A7_A8
CMD23		A6_A11
CMD24		ABI#
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS#
CMD29		RST#
CMD30		CKE#
CMD31		CAS#

建議線路
0.1ux6,1ux4,10ux1 FBVDDQ
1ux4,10ux1 FBVDD
for 2pcs VRAM

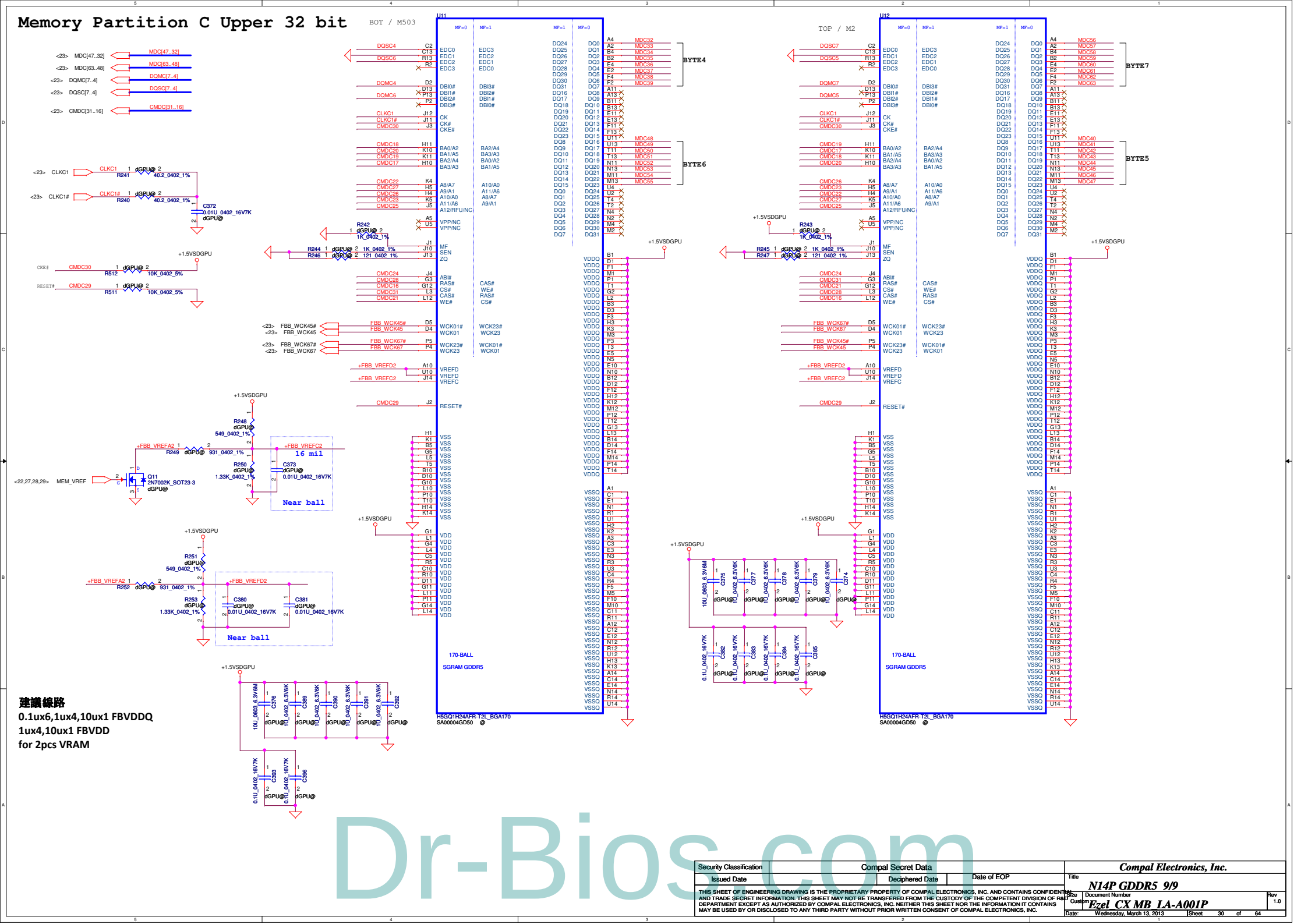
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	Deciphered Date	Date of EOP	Title: N14P GDDR5 8/9

Size: Custom	Document Number: Ezel_CX MB_LA-A001P		Rev: 1.0
Date: Wednesday, March 13, 2013	Sheet 29 of 64		

Memory Partition C Upper 32 bit

BOT / M503

TOP / M2



建議線路

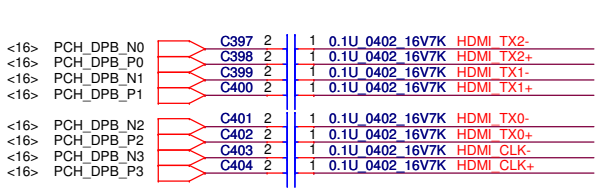
0.1ux6,1ux4,10ux1 FBVDDQ

1ux4,10ux1 FBVDD

for 2pcs VRAM

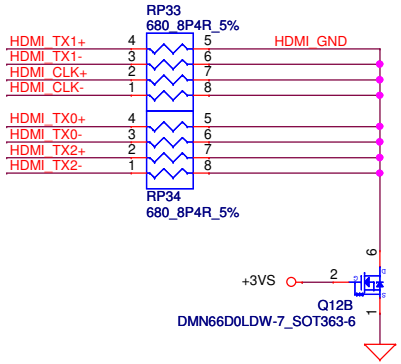
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	Deciphered Date	Date of EOP	Title: N14P GDDR5 9/9
			Size: Custom; Document Number: Ezel_CX MB_LA-A001P; Rev: 1.0
			Date: Wednesday, March 13, 2013; Sheet 30 of 64

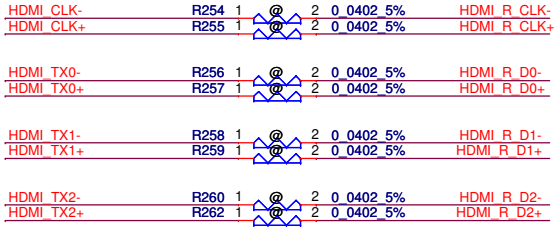
Cost Reduced Level Shifter Topology



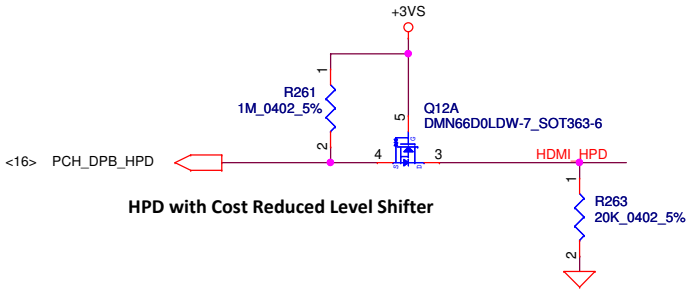
Pin Mapping for HDMI by Port B

PCH Pin Name	HDMI O/P
DDPB_[0]P	TMDSB_DATA2
DDPB_[0]N	TMDSB_DATA2#
DDPB_[1]P	TMDSB_DATA1
DDPB_[1]N	TMDSB_DATA1#
DDPB_[2]P	TMDSB_DATA0
DDPB_[2]N	TMDSB_DATA0#
DDPB_[3]P	TMDSB_CLK
DDPB_[3]N	TMDSB_CLK#
DDPB_AUXP	NA
DDPB_AUXN	NA
DDPB_HPD	HDMIB_HPD
SDVO_CTRLCLK	HDMIB_CTRLCLK
SDVO_CTRLDATA	HDMIB_CTRLDATA

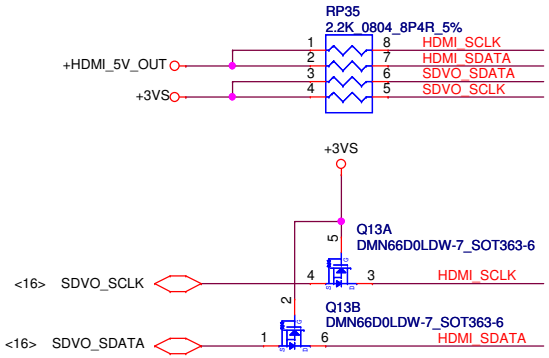


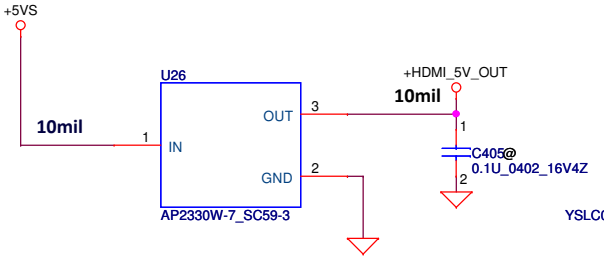


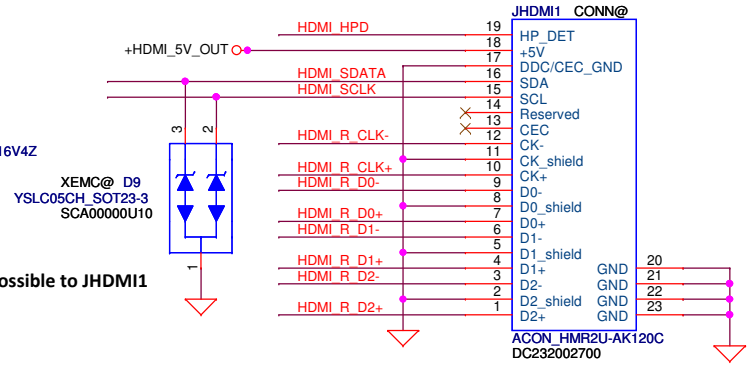
Change to short pad for experiment for the first PCB version , request by EMI



HPD with Cost Reduced Level Shifter







D9 should be as close as possible to JHDMI1

Security Classification	Compal Secret Data		
Issued Date	2012/07/10	Deciphered Date	Date of EOP

Compal Electronics, Inc.

Title: HDMI Connector

Size	Document Number	Rev
Custom	Ezel_CX MB_LA-A001P	1.0

Date: Wednesday, March 13, 2013 Sheet 31 of 64

eDP Panel Power Circuit

4-Lane eDP panel should be taken into account

80mil

+3VS

+LCDVDD

U27

G5243T11U_SOT23-5

C412 1U_0402_6.3V6K

C406 4.7U_0603_6.3V6K

<16> PCH_ENVDD

PU Resistor for inverting level shifter is on CPU site

<4> CPU_EDP_HPD#

Q14 2N7002K_SOT23-3

R298 0_0402_5% EDP_HPD

R521 150K_0402_5%

R391 100K_0402_5%

C129@ 1U_0402_6.3V6K

the circuits surrounded by red rectangle is only for cable which should pass via re-driver board

Purpose: no any increasement for cable's gauge

eDP PANEL Connector

+INVPWR_B+

W=60mils

JEDP1 CONN@

<16> INVTPWM

BKOFF#

EDP_HPD

+LCDVDD

W=60mils

C409 0.1U_0402_16V4Z

<4> EDP_AUXN / EDP_AUXP

<4> EDP_TXP0 / EDP_TXN0

<4> EDP_TXP1 / EDP_TXN1

<4> EDP_TXP2 / EDP_TXN2

<4> EDP_TXP3 / EDP_TXN3

ACES_50406-03071-001

SP010015L00

<37> BKOFF# R267 @ 10K_0402_5%

+INVPWR_B+ 60mil

EMI@ L12 FBMA-L11-201209-221LMA30_2P

B+ 60mil

EMI@ C410 1000P_0402_50V7K

For CMOS Camera

R307 EMI@ 0_0402_5%

L15 XEMC@

<17> USB20_N10

<17> USB20_P10

USB20_N10_R

USB20_P10_R

WCM2012F2SF-670T04_0805

R308 EMI@ 0_0402_5%

after confirming, home key will not support wake-up function by Ezel_CX

+3VS

C441 0.1U_0402_16V4Z

+3VALW

+3VLP

JSNSR1 CONN@

USB20_N10_R

USB20_P10_R

USB20_P12

USB20_N12

SNSR_HUB_PWR_GATE

SNSR_HUB_DFU_EN#

For Sensor Hub

<18> SNSR_HUB_PWR_GATE

<18> SNSR_HUB_DFU_EN#

<37> HK_INT#

<37> HK_I2C_SDATA

<37> HK_I2C_SCLK

HK_INT#

HK_I2C_SDATA

HK_I2C_SCLK

+5VS

C439 0.1U_0402_16V4Z

C440 10U_0603_6.3V6M

For Touch Screen

<17> USB20_N11

<17> USB20_P11

<17> TOUCH_PANEL_INT#

USB20_N11

USB20_P11

TOUCH_PANEL_INT#

ACES_50406-02071-001

SP010016L00

SNSR_HUB_DFU_EN#

ESD@ C446 100P_0402_50V8J

request from ESD

need to put close to JSNSR1

Security Classification	Compal Secret Data		
Issued Date	2012/07/10	Deciphered Date	Date of EOP

Compal Electronics, Inc.

Title: *eDP Connector*

Size: Custom | Document Number: *Ezel_CX MB_LA-A001P* | Rev: 1.0

Date: Wednesday, March 13, 2013 | Sheet 32 of 64

mDP Connecotr

SM070002O10 HSF2012F2SF 90ohm @100MHz

SM070002O10 HSF2012F2SF 90ohm @100MHz

these RF solutions should be placed as close as possible JMDP1

no wake-up function supported requirement, short J12 for DVT

these RF solutions should be placed as close as possible to U30

PIN22, CHRG_DELAY can be left NC for no battery charge mode supported.

no wake-up function supported requirement, un-stuff R324

Preliminary Power Output for mDP		
DNGLE_PWR_EN#	LB_PWR_RTN	LB_PWR_CNN
1	GND	3.3V
0	5V	3.3V

"DM@": supports Dual-Mode, such as HDMI

to connector via D39

reserve J13 if no any safety concern

plan to change to 100U/25V for 19V power voltage input

follow AE's comment, put the back drive current protection FET between IC and connector

ESD Component

these ESD diodes should be put close to JMDP1

follow TI's recommendation, change all PU/PD resistance to 10k

RST/TEST

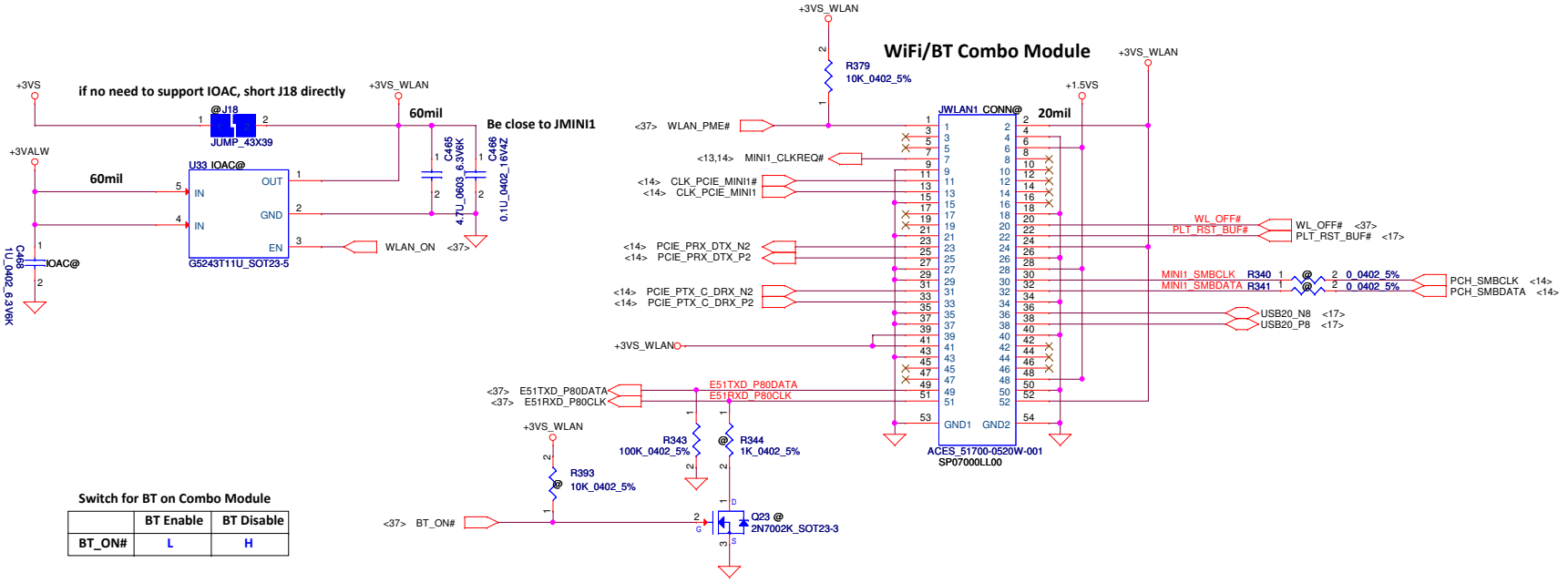
RST: need to ull up to 47K

TEST: reserve test point for FW update

Control Signals and Miscellaneous

		Docking Port Mode		Acer
Pin Number	DP Mode	USB3.0 (2-Lane Mode)	Full DP Mode (4-Lane Mode)	mDP DNGLE Mode
PIN1	GND	GND	GND	GND
PIN2	HPD	HPD	HPD	HPD
PIN3	DP_ML_0P	DP_ML_0P	DP_ML_0P	DP_ML_0P
PIN4	CONFIG1	USB20_P	CONFIG1	USB20_P
PIN5	DP_ML_0N	DP_ML_0N	DP_ML_0N	DP_ML_0N
PIN6	CONFIG2	USB20_N	CONFIG2	USB20_N
PIN7	GND	GND	GND	GND
PIN8	GND	GND	GND	GND
PIN9	DP_ML_1P	DP_ML_1P	DP_ML_1P	DP_ML_1P
PIN10	DP_ML_3P	USB30_TXP	DP_ML_3P	USB30_TXP
PIN11	DP_ML_1N	DP_ML_1N	DP_ML_1N	DP_ML_1N
PIN12	DP_ML_3N	USB30_TXN	DP_ML_3N	USB30_TXN
PIN13	GND	GND	GND	GND
PIN14	GND	GND	GND	GND
PIN15	DP_ML_2P	USB30_RXP	DP_ML_2P	USB30_RXP
PIN16	AUX_P	AUX_P	AUX_P	AUX_P
PIN17	DP_ML_2N	USB30_RXN	DP_ML_2N	USB30_RXN
PIN18	AUX_N	AUX_N	AUX_N	AUX_N
PIN19	DP_PWR_RTN	DP_PWR_RTN	DP_PWR_RTN	PWR 5V 1.5A
PIN20	PWR 3V 500mA			PWR 3V 500mA

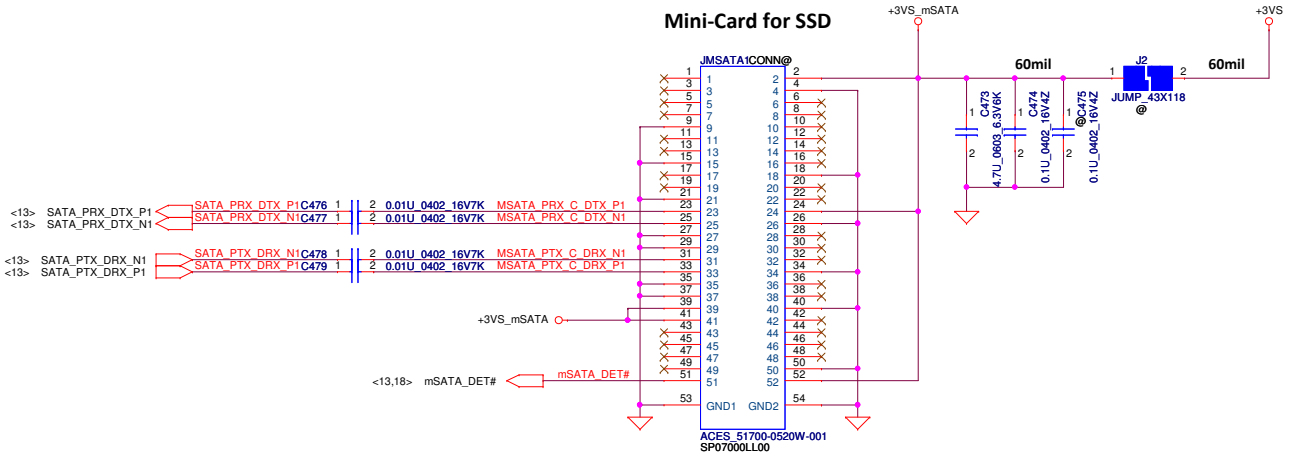
Security Classification		Compal Secret Data	Compal Electronics, Inc.
Issued Date	2012/09/06	Deciphered Date	Date of EOP
Title	Lightning-Bolt Controller		
Size	Custom	Document Number	Ezel_CX MB_LA-A001P
Rev	1.0	Date: Wednesday, March 13, 2013	Sheet 33 of 64



Switch for BT on Combo Module

	BT Enable	BT Disable
BT_ON#	L	H

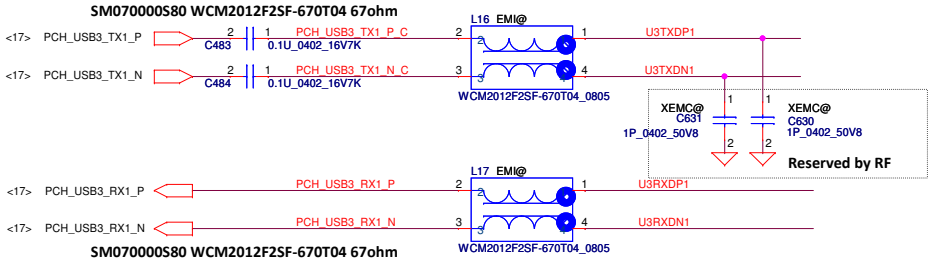
if no space for components, move these to be close to EC side

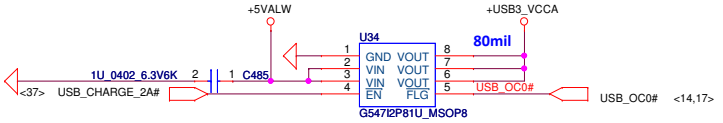


Pin Definition			
PIN1	NC	PIN2	3.3V
PIN3	NC	PIN4	GND
PIN5	NC	PIN6	+1.5V(No Use)
PIN7	NC	PIN8	NC
PIN9	GND	PIN10	NC
PIN11	NC	PIN12	NC
PIN13	NC	PIN14	NC
PIN15	GND	PIN16	NC
PIN17	NC	PIN18	GND
PIN19	NC	PIN20	NC
PIN21	GND	PIN22	NC
PIN23	Host RX+	PIN24	3.3V
PIN25	Host RX-	PIN26	GND
PIN27	GND	PIN28	+1.5V(No Use)
PIN29	GND	PIN30	NC
PIN31	Host TX-	PIN32	NC
PIN33	Host TX+	PIN34	GND
PIN35	GND	PIN36	NC
PIN37	GND	PIN38	NC
PIN39	3.3V	PIN40	GND
PIN41	3.3V	PIN42	NC
PIN43	NC	PIN44	NC
PIN45	By Vendor	PIN46	NC
PIN47	By Vendor	PIN48	+1.5V(No Use)
PIN49	DA/DSS	PIN50	GND
PIN51	Detection	PIN52	3.3V

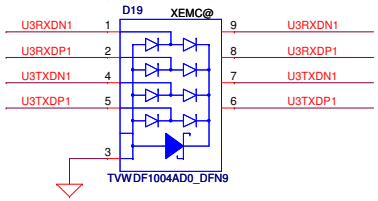
Security Classification	Compal Secret Data		
Issued Date	2011/12/13	Deciphered Date	Date of EOP

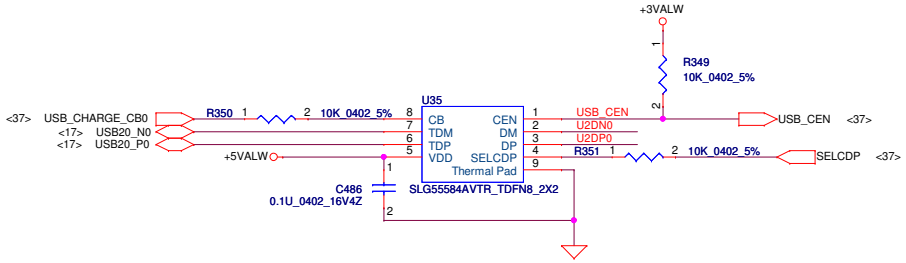
Compal Electronics, Inc.			
Title: Mini-Card for WiFi&BT/SSD			
Size: Custom	Document Number: Ezel_CX MB_LA-A001P		Rev: 1.0
Date: Wednesday, March 13, 2013	Sheet 34 of 64		



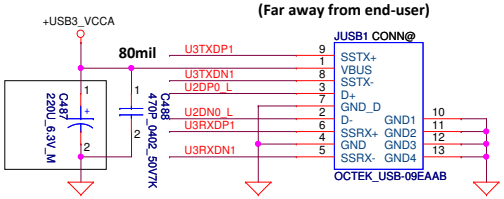


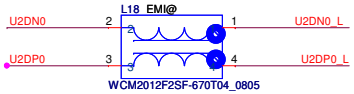
D19 should be put as close as possble to JUSB1





USB 3.0 External Connector
(Far away from end-user)





SM070000S80 WCM2012F2SF-670T04 67ohm

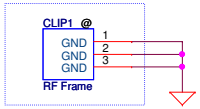
Part Number	Description	ESR
SF000002Y00	S_A-P_CAP 220U 6.3V M 6.3X4.2 R17M VLPS	17mΩ

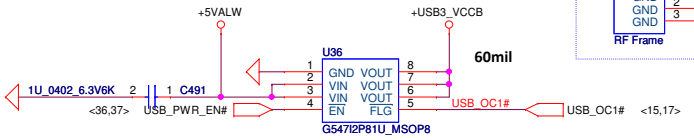
Truth Table for Inserted Device

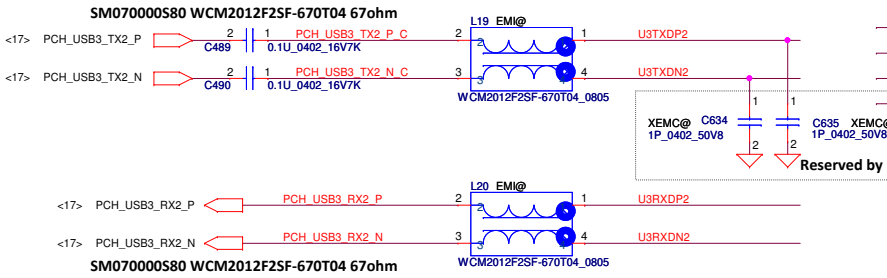
CB	SELCDP	
0	X	DCP autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP only
1	1	S0 charging with CDP or SDP only, to distinguish if Fast Charging should be supported or not

Exteranl USB-IF Device Type	
DCP	Dedicated Charging Port
SDP	Standard Downstream Port
CDP	Charging Downstream Port

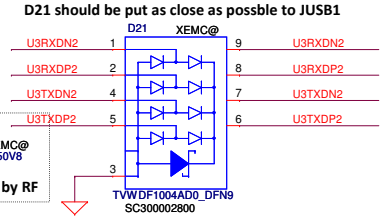
add Frame for RF



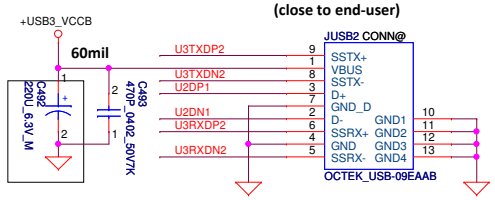




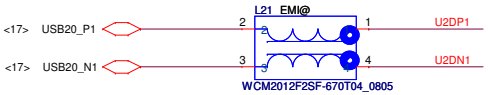
D21 should be put as close as possble to JUSB1



USB 3.0 Exteranl Connector
(close to end-user)



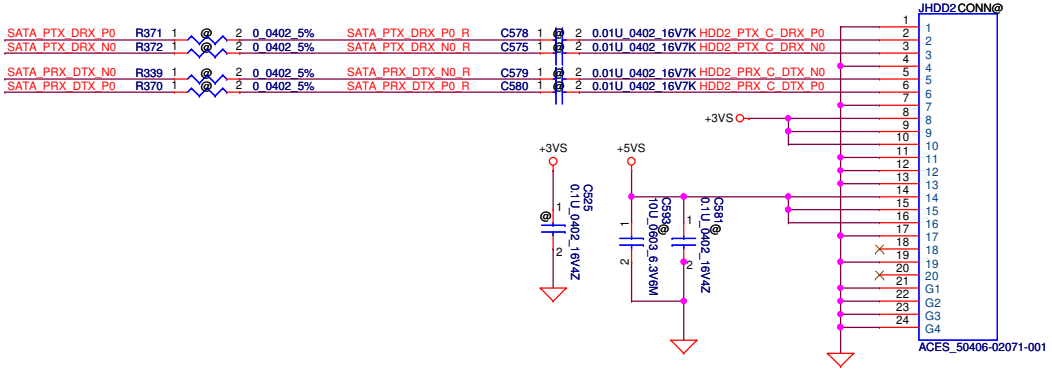
Part Number	Description	ESR
SF000002Y00	S_A-P_CAP 220U 6.3V M 6.3X4.2 R17M VLPS	17mΩ



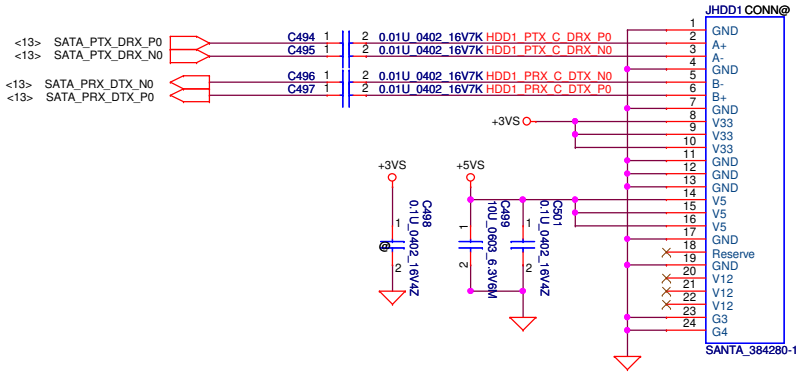
Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	Date of EOP

Title	USB3.0 External Ports		
Size: Custom	Document Number: Ezel_CX MB_LA-A001P		Rev: 1.0
Date: Wednesday, March 13, 2013	Sheet 35 of 64		

SATA HDD Connector (SMD Type)

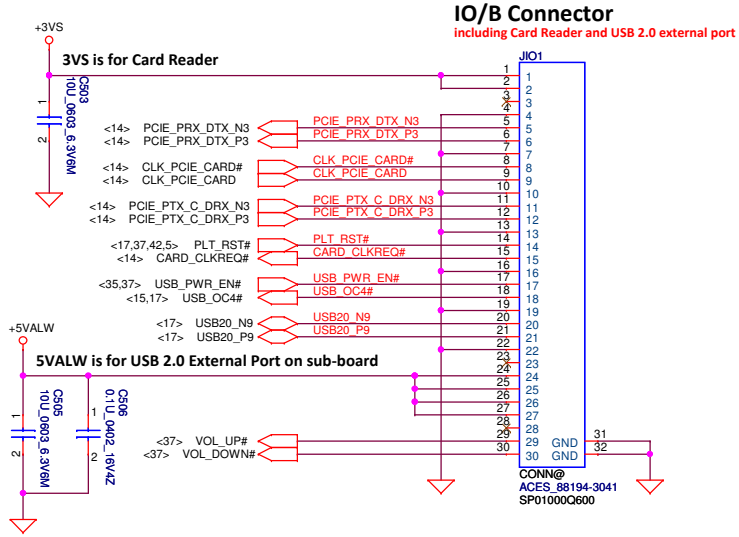


SATA HDD Connector(DIP Type)



IO/B Connector

including Card Reader and USB 2.0 external port



Security Classification	Compal Secret Data		
Issued Date	2011/12/13	Deciphered Date	Date of EOP

Compal Electronics, Inc.

Title: SATA HDD & IO/B Connector

Size: Custom | Document Number: Ezel_CX MB_LA-A001P | Rev: 1.0

Date: Wednesday, March 13, 2013 | Sheet 36 of 64

use +3VLP power for EC for DVT build

SM010015410 300ma 80ohm@100mhz DCR 0.3

L22 FBMA-L11-160808-800LMT_0603

U37 KB9012QF-A3_LQFP128_14X14

20mil

Q24A DMN66D0LDW-7_SOT363-6

Q24B DMN66D0LDW-7_SOT363-6

X1 32.768K 12.5PF 1TJF125DP1A000D

check if PU for GPU_TGLREQ# can be dGPU@ or not

change from inductor to short pad for experiment

SMBus-1 is for,
a. Power Charger IC
b. Smart Battery

SMBus-2 is for,
1. GPU
2. PCH
3. VRAM and DRAM Thermal Sensor

Board ID

See definition on notes page, NEED to check EVERY TIME before new gerber-out

Phase	Revision	BID0
EVT	0.1	0
DVT	0.2	1
PVT	0.3	2
* MP	1.0	3

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	Date of EOP

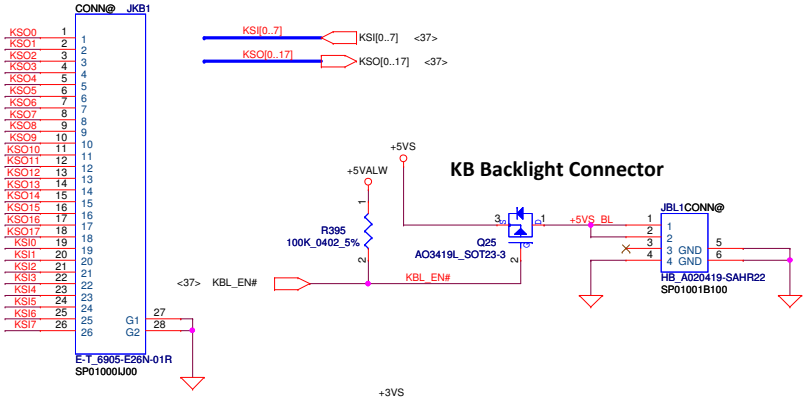
Compal Electronics, Inc.

Title: EC ENE-KB9012

Size: Custom | Document Number: Ezel_CX MB_LA-A001P | Rev: 1.0

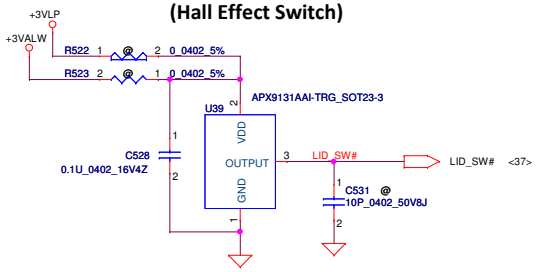
Date: Wednesday, March 13, 2013 | Sheet 37 of 64

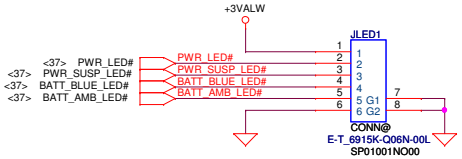
KB Connector



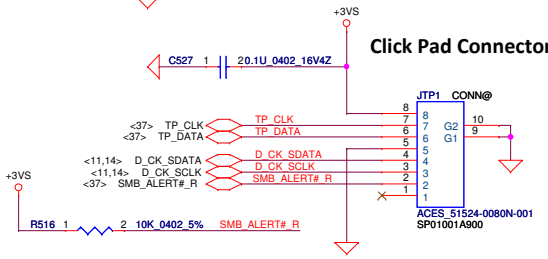
KB Backlight Connector

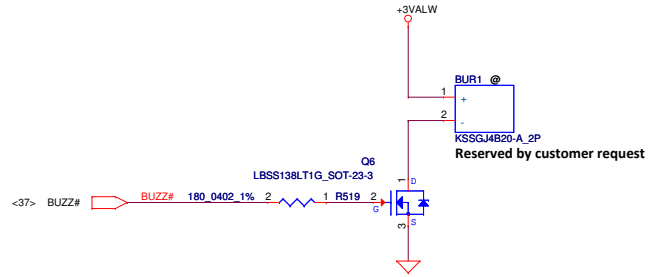
Lid Switch (Hall Effect Switch)

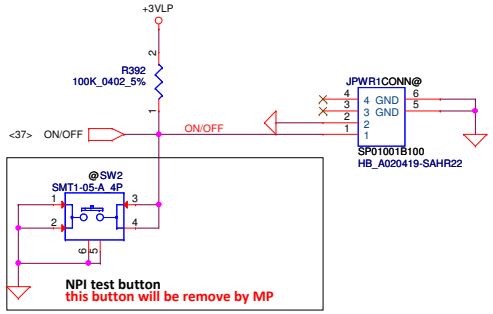




Click Pad Connector

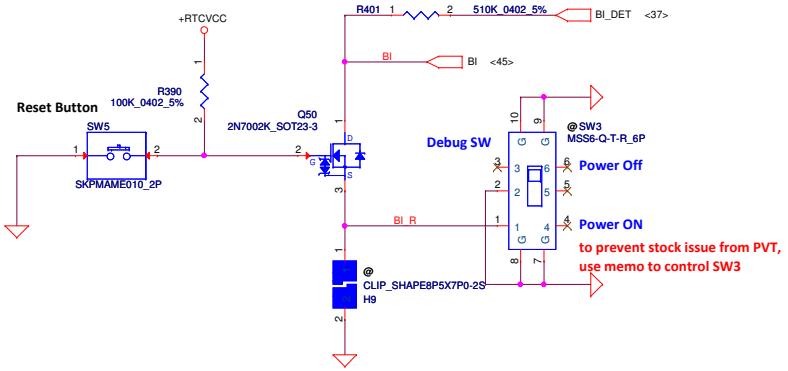






Embeded Battery Reset Button

Debug switch will be removed after MP.



Security Classification	Compal Secret Data		
Issued Date	2011/12/13	Deciphered Date	Date of EOP

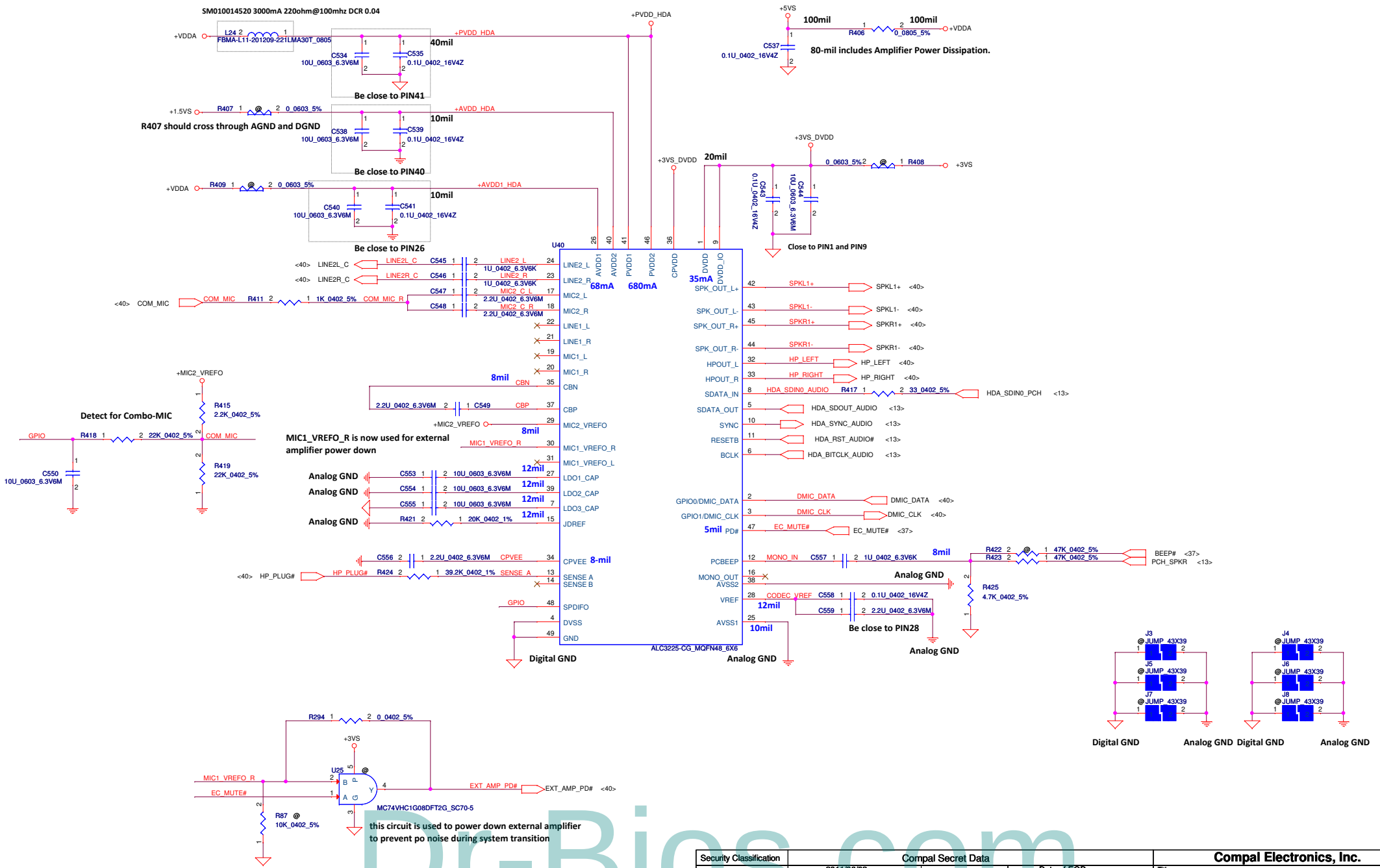
Compal Electronics, Inc.

Title: *User Interface*

Size	Document Number	Rev
Custom	*Ezel_CX MB_LA-A001P*	1.0

Date: Wednesday, March 13, 2013 | Sheet 38 of 64

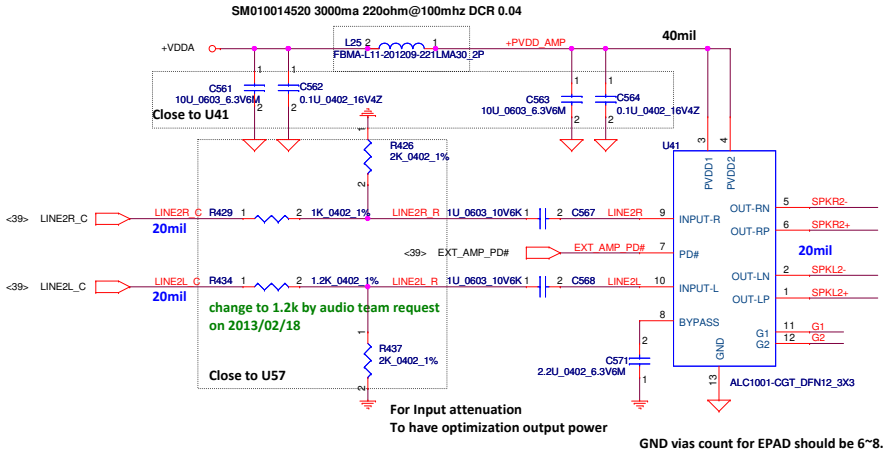
HD Audio Codec- ALC3225 with Embedded Speaker Amplifier

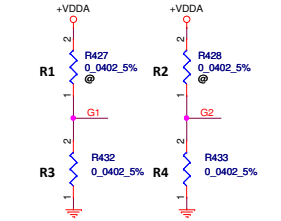


Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	Date of EOP

Compal Electronics, Inc.

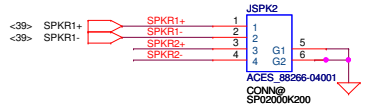
Title	HD Audio Codec ALC3225X + ALC1001		
Size	Document Number		Rev
Custom	Ezel_CX MB_LA-A001P		1.0
Date:	Wednesday, March 13, 2013	Sheet	39 of 64



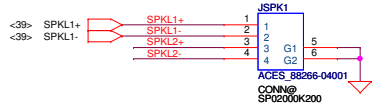


R1	R2	R3	R4	Gain (Differential)
NC	NC	0	0	11dB
0	NC	NC	0	14dB
NC	0	0	NC	19dB
0	0	NC	NC	25dB

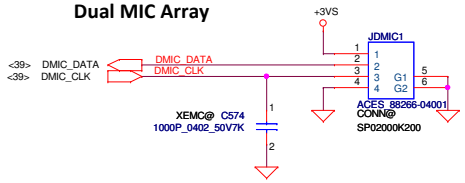
Speaker Connector (Right)



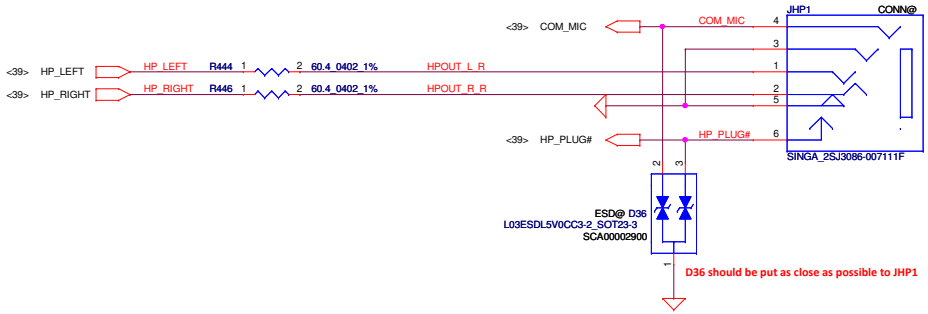
Speaker Connector (Left)



Dual MIC Array

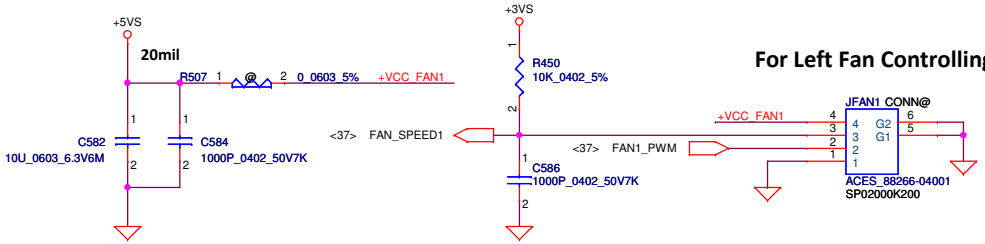


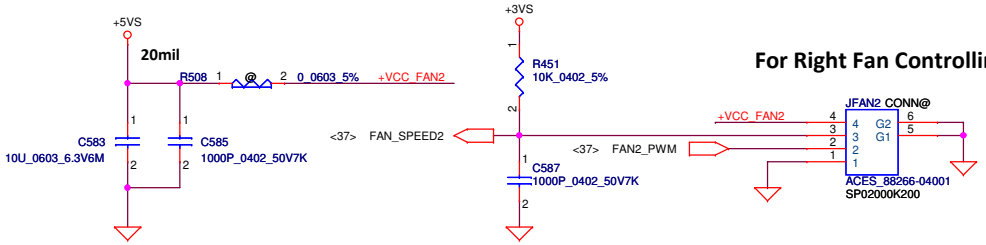
Headphone Out/Mic Combo (Noraml-Open Type)

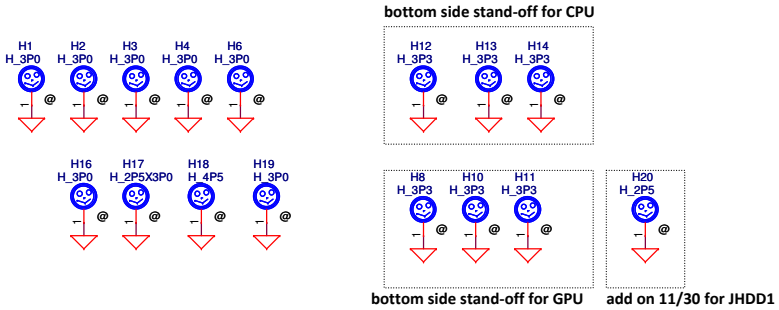


Security Classification	Compal Secret Data		
Issued Date	2011/12/13	Deciphered Date	Date of EOP

Compal Electronics, Inc.			
Title: Amplifier & I/O Ports			
Size: Custom	Document Number: Ezel_CX MB_LA-A001P		Rev: 1.0
Date: Wednesday, March 13, 2013	Sheet 40 of 64		





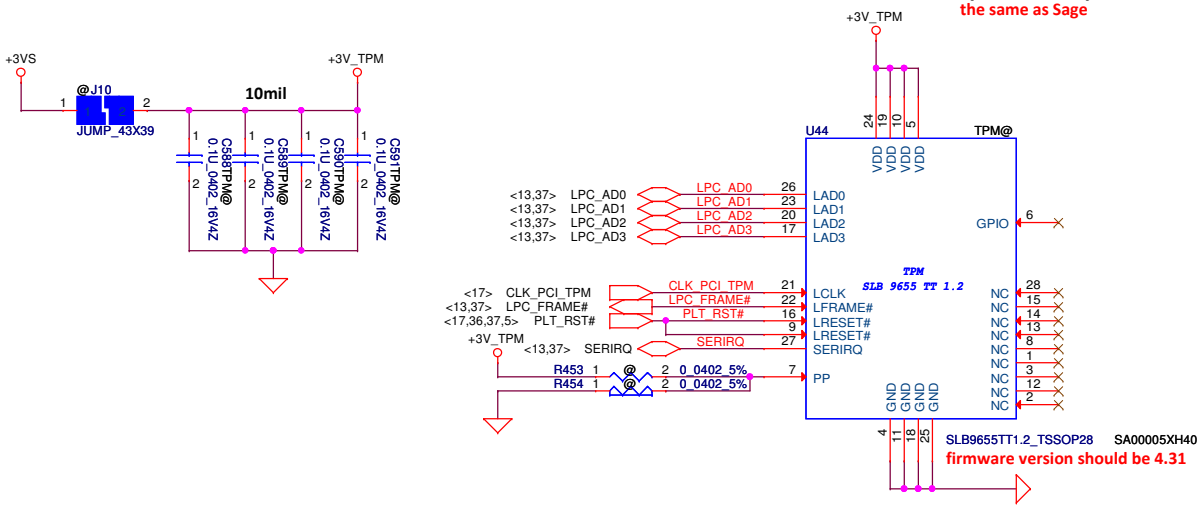


Security Classification	Compal Secret Data		
Issued Date	2011/12/13	Deciphered Date	Date of EOP

Compal Electronics, Inc.		
Title: FAN & Screw Hole		
Size: Custom	Document Number: Ezel_CX MB_LA-A001P	Rev: 1.0
Date: Wednesday, March 13, 2013	Sheet 41 of 64	

TPM on board solution (INFINEON)

the same as Sage

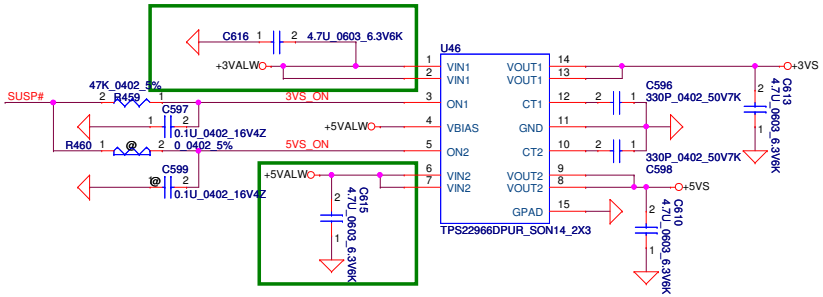


firmware version should be 4.31

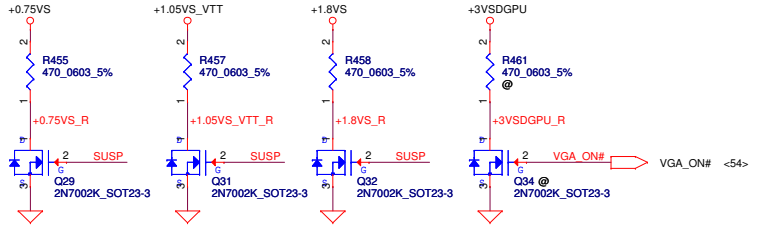
Security Classification	Compal Secret Data		
Issued Date	2011/12/13	Deciphered Date	Date of EOP

Compal Electronics, Inc.		
Title: P43- TPM\LOM DB Connector		
Size: Custom	Document Number: Ezel_CX MB_LA-A001P	Rev: 1.0
Date: Wednesday, March 13, 2013	Sheet 42 of 64	

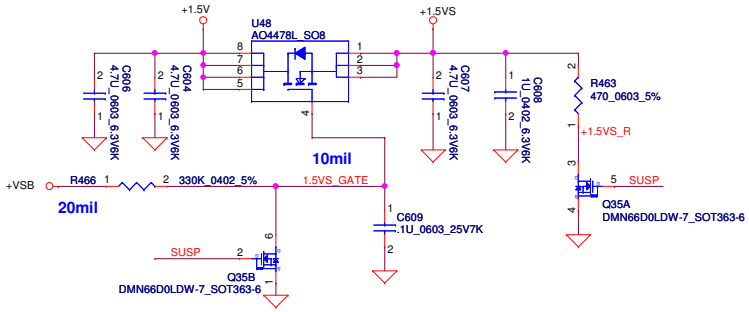
Use Dual Load Switch for 3VS/5VS Power Supply

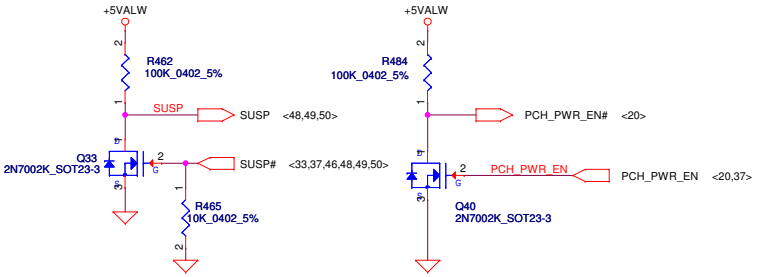


C615 and C616 are ≦4.7uF hence it is okay for APE8990GN3B

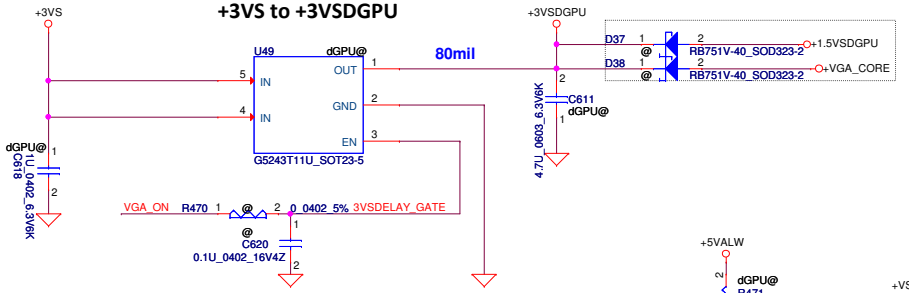


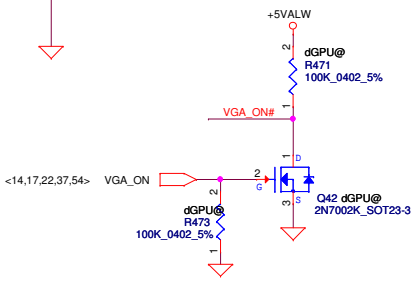
+1.5V to +1.5VS



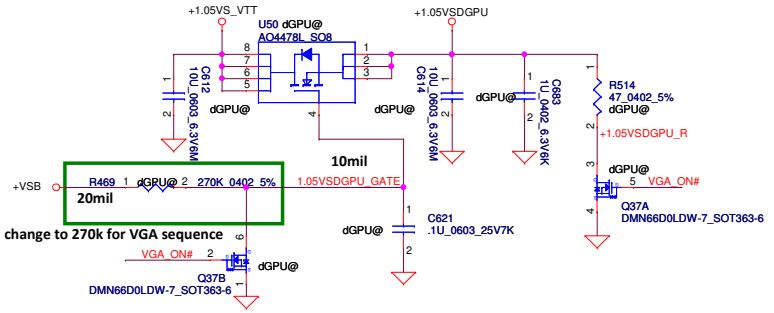


+3VS to +3VSDGPU



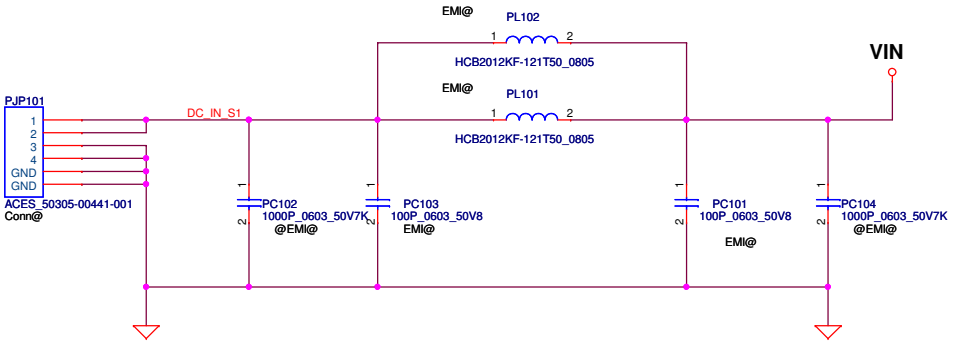


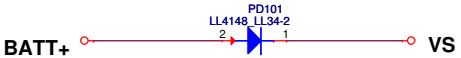
+1.05VS_VTT TO +1.05VSDGPU

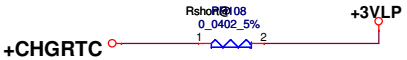


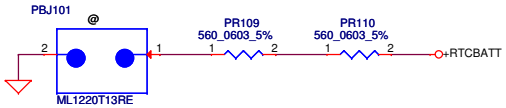
Security Classification	Compal Secret Data		
Issued Date	2011/12/13	Deciphered Date	Date of EOP

Compal Electronics, Inc.			
Title: DC Interface			
Size: Custom	Document Number: Ezel_CX MB_LA-A001P		Rev: 1.0
Date: Wednesday, March 13, 2013	Sheet 43 of 64		







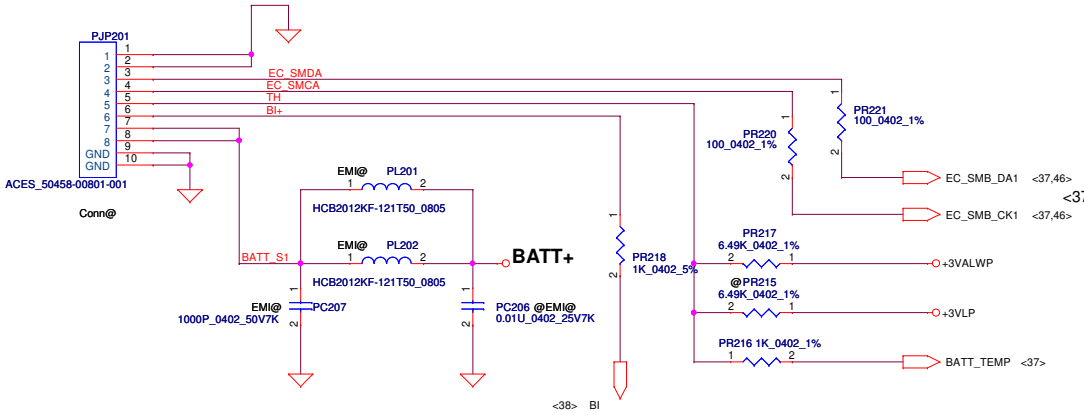


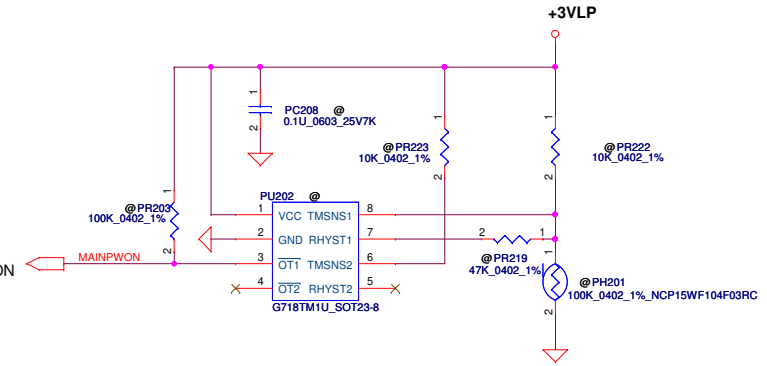
Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	Date of EOP

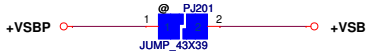
Compal Electronics, Inc.

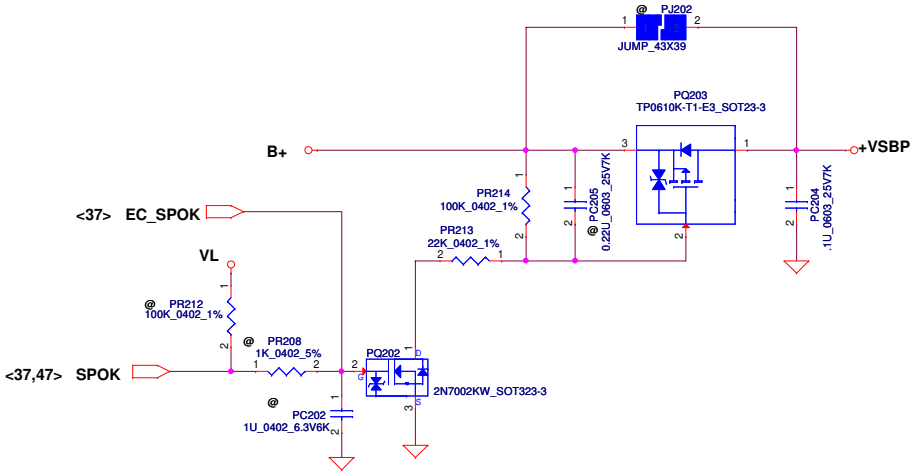
Title: ***DCIN/PRECHARGE***

Size	Document Number	Rev
Custom	*Ezel M/B Schematics_LAA001P*	1.0
Date:	Sheet 44 of 64	







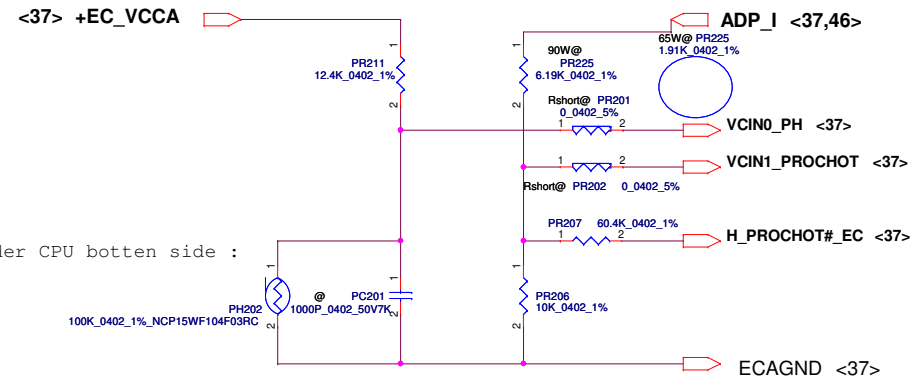


For KB9012 OTP	
92℃	1.2V, Active
56℃	2.255V, Recovery

For KB9012 sense 10mΩ	Active	Recovery
65W	70W,0.61V	54W,0.46V
90W	96W,0.63V	75W,0.46V

CPU thermal protection at 92 degree C (shutdown)
Recovery at 56 degree C

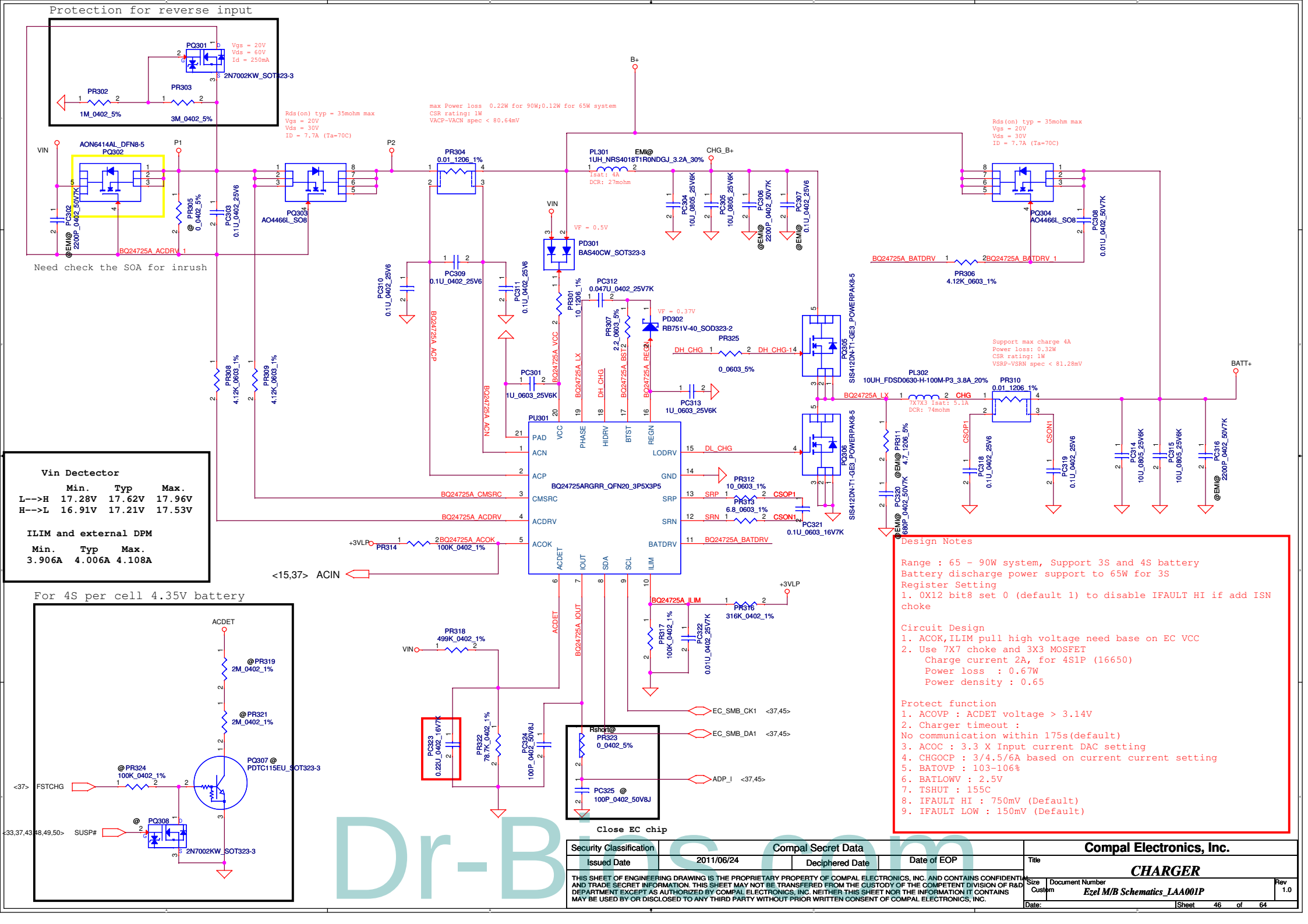
ADP_I >1.2V ,
CPU will throttling



PH202 under CPU botten side :

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/24	Deciphered Date	Date of EOP

Title	BATTERY CONN / OTP		
Size	Document Number		Rev
Custom	Ezel M/B Schematics_LAA001P		1.0
Date:		Sheet 45 of 64	


Protection for reverse input
PQ301
2N7002KW_SOT323-3
Vgs = 20V
Vds = 60V
Id = 250mA
PR302
1M_0402_5%
PR303
3M_0402_5%
Rds(on) typ = 35mohm max
Vgs = 20V
Vds = 30V
ID = 7.7A (Ta=70C)
max Power loss 0.22W for 90W;0.12W for 65W system
CSR rating: 1W
VACP-VACN spec < 80.64mV
VIN
AON6414AL_DFN8-5
PQ302
P1
P2
PR304
0.01_1206_1%
PL301
EMI@
1UH_NRS4018T1R0NDGJ_3.2A_30%
Isat: 4A
DCR: 27mohm
CHG_B+
B+
PC304
10U_0805_25V6K
PC305
10U_0805_25V6K
PC306
2200P_0402_50V7K
PC307
0.1U_0402_25V6
PR305
0_0402_5%
PC302
2200P_0402_50V7K
PC303
0.1U_0402_25V6
PQ303
AO4466L_SO8
BQ24725A_ACDRV_1
Need check the SOA for inrush
VF = 0.5V
PD301
BAS40CW_SOT323-3
PC309
0.1U_0402_25V6
PC310
0.1U_0402_25V6
PC311
0.1U_0402_25V6
PC312
0.047U_0402_25V7K
PR301
10_1206_1%
PR307
2.2_0603_5%
VF = 0.37V
PD302
RB751V-40_SOD323-2
PR325
0_0603_5%
DH_CHG
DH_CHG-1
PC313
1U_0603_25V6K
PC301
1U_0603_25V6K
PR308
4.12K_0603_1%
PR309
4.12K_0603_1%
BQ24725A_ACP
BQ24725A_VCC
BQ24725A_LX
BQ24725A_BST
BQ24725A_REGN
PU301
BQ24725ARGRR_QFN20_3P5X3P5
PAD
ACN
ACP
CMSRC
ACDRV
ACOK
VCC
PHASE
HIDRV
BTST
REGN
LODRV
GND
SRP
SRN
BATDRV
ACDET
IOUT
SDA
SCL
ILIM
DL_CHG
PR312
10_0603_1%
PR313
6.8_0603_1%
PC321
0.1U_0603_16V7K
CSOP1
CSON1
BQ24725A_CMSRC
BQ24725A_ACDRV
BQ24725A_ACOK
BQ24725A_BATDRV
+3VLP
PR314
100K_0402_1%
<15,37> ACIN
PQ305
SIS412DN-T1-GE3_POWERPAK8-5
PQ306
SIS412DN-T1-GE3_POWERPAK8-5
Rds(on) typ = 35mohm max
Vgs = 20V
Vds = 30V
ID = 7.7A (Ta=70C)
PQ304
AO4466L_SO8
PC308
0.01U_0402_50V7K
BQ24725A_BATDRV_1
PR306
4.12K_0603_1%
Support max charge 4A
Power loss: 0.32W
CSR rating: 1W
VSRP-VSRN spec < 81.28mV
BATT+
PL302
10UH_FDSD0630-H-100M-P3_3.8A_20%
7X7X3 Isat: 5.1A
DCR: 74mohm
BQ24725A_LX
CHG
PR310
0.01_1206_1%
PR311
4.7_1206_5%
PC320
680P_0402_50V7K
@EMI@
PC318
0.1U_0402_25V6
PC319
0.1U_0402_25V6
PC314
10U_0805_25V6K
PC315
10U_0805_25V6K
PC316
2200P_0402_50V7K
Vin Dectector
Min. Typ Max.
L-->H 17.28V 17.62V 17.96V
H-->L 16.91V 17.21V 17.53V
ILIM and external DPM
Min. Typ Max.
3.906A 4.006A 4.108A
For 4S per cell 4.35V battery
ACDET
@PR319
2M_0402_1%
@PR321
2M_0402_1%
@PR324
100K_0402_1%
PQ307 @
PDTC115EU_SOT323-3
<37> FSTCHG
@
PQ308
<33,37,43,48,49,50> SUSP#
2N7002KW_SOT323-3
PR318
499K_0402_1%
PR317
100K_0402_1%
PC322
0.01U_0402_25V7K
PR316
316K_0402_1%
BQ24725A_ILIM
PC323
0.22U_0402_16V7K
PR322
78.7K_0402_1%
PC324
100P_0402_50V8J
Rshort@
PR323
0_0402_5%
PC325 @
100P_0402_50V8J
EC_SMB_CK1 <37,45>
EC_SMB_DA1 <37,45>
ADP_I <37,45>
Close EC chip
Design Notes
Range : 65 - 90W system, Support 3S and 4S battery
Battery discharge power support to 65W for 3S
Register Setting
1. 0X12 bit8 set 0 (default 1) to disable IFAULT HI if add ISN choke
Circuit Design
1. ACOK,ILIM pull high voltage need base on EC VCC
2. Use 7X7 choke and 3X3 MOSFET
Charge current 2A, for 4S1P (16650)
Power loss : 0.67W
Power density : 0.65
Protect function
1. ACOVP : ACDET voltage > 3.14V
2. Charger timeout :
No communication within 175s(default)
3. ACOC : 3.3 X Input current DAC setting
4. CHGOCP : 3/4.5/6A based on current current setting
5. BATOVP : 103-106%
6. BATLOWV : 2.5V
7. TSHUT : 155C
8. IFAULT HI : 750mV (Default)
9. IFAULT LOW : 150mV (Default)
Security Classification
Compal Secret Data
Issued Date
2011/06/24
Deciphered Date
Date of EOP
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Compal Electronics, Inc.
Title
CHARGER
Size
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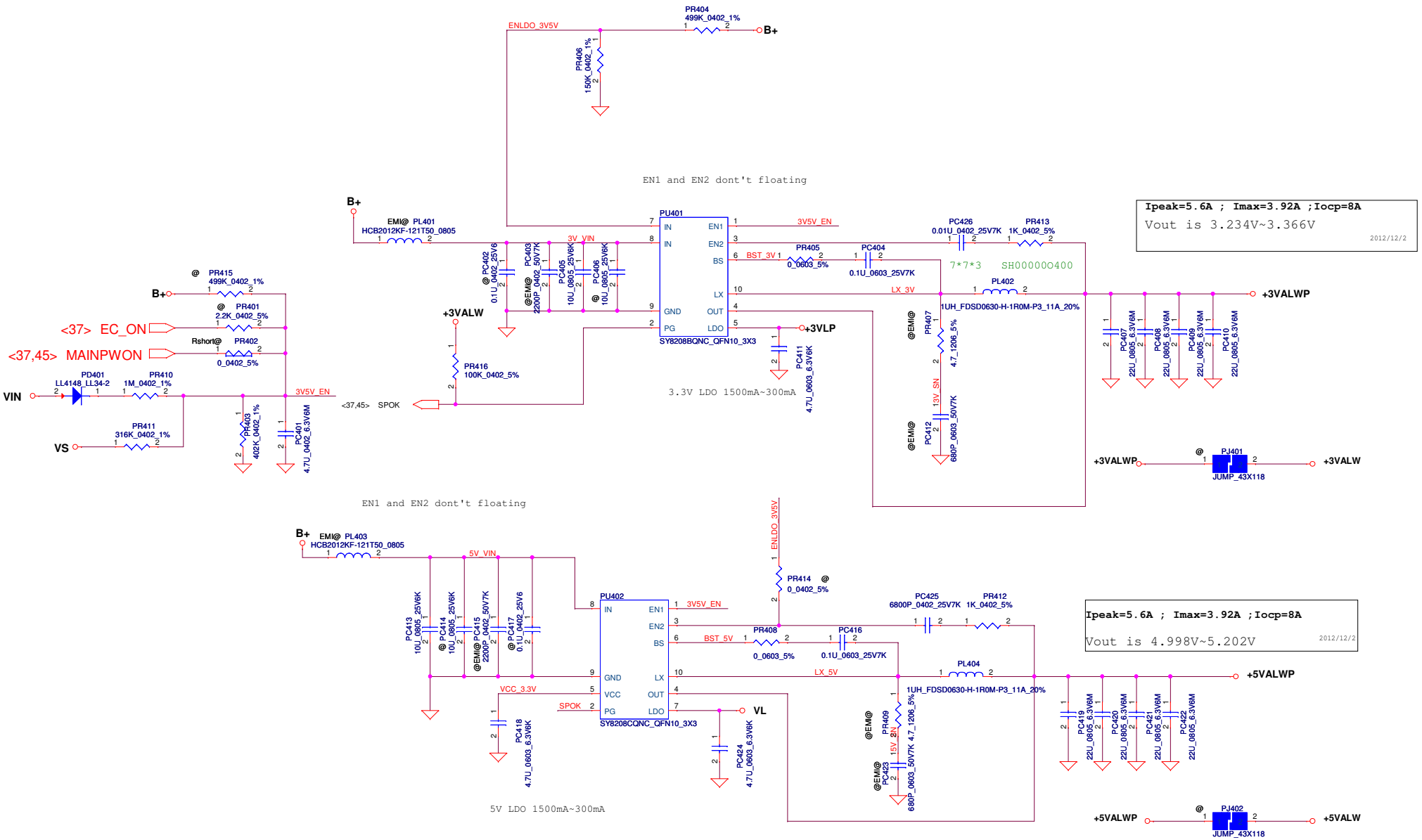
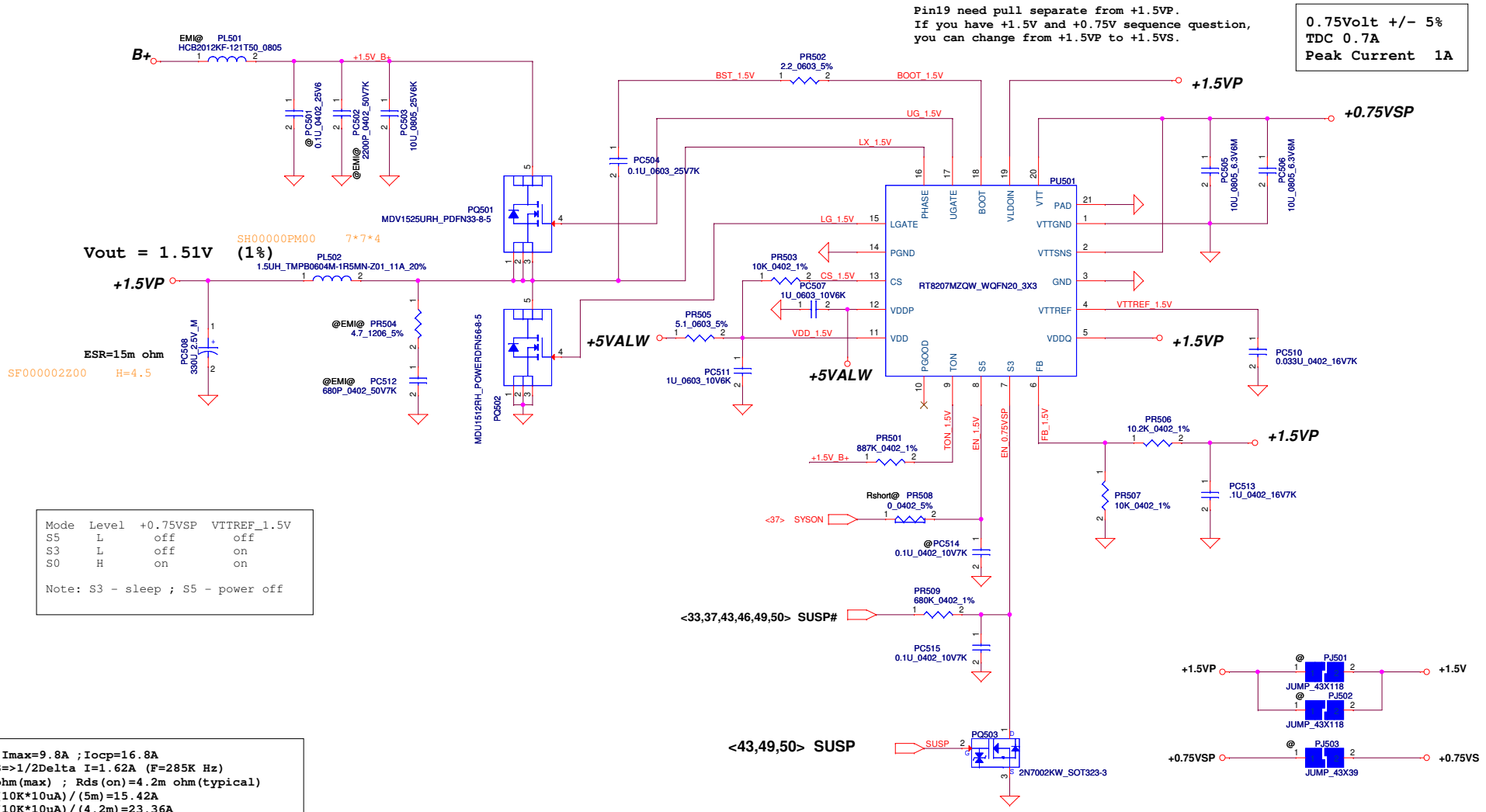
Document Number
Ezel M/B Schematics_LAA001P
Rev
1.0
Date:
Sheet 46 of 64



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	Date of EOP

Compal Electronics, Inc.			
Title	+3VALW/+5VALW		
Size Custom	Document Number		Rev 1.0
Date: Wednesday, March 13, 2013	Sheet 47 of 64		



Mode	Level	+0.75VSP	VTTREF_1.5V
S5	L	off	off
S3	L	off	on
S0	H	on	on

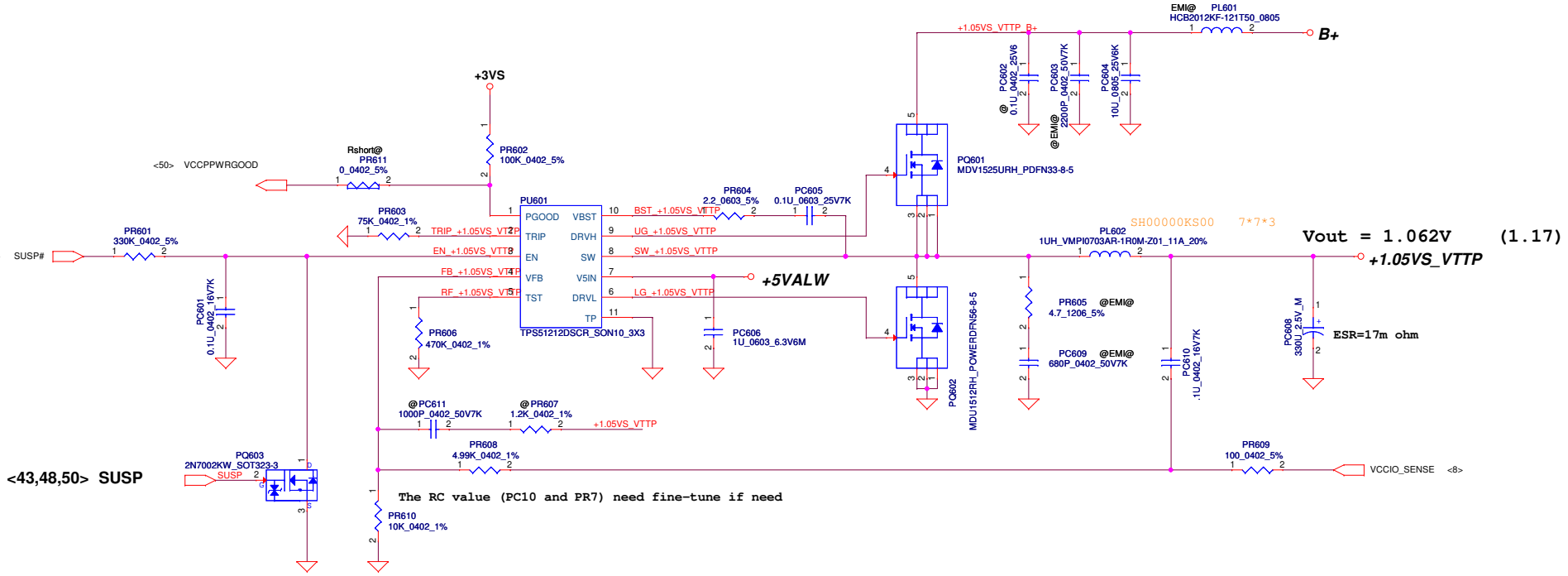
Note: S3 - sleep ; S5 - power off

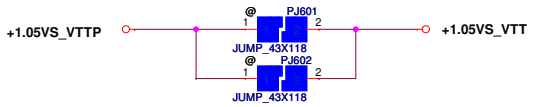
Ipeak=14A ; Imax=9.8A ;Iocp=16.8A
Delta I=3.23=>1/2Delta I=1.62A (F=285K Hz)
Rds(on)=5m ohm(max) ; Rds(on)=4.2m ohm(typical)
Ilimit_min=(10K*10uA)/(5m)=15.42A
Ilimit_max=(10K*10uA)/(4.2m)=23.36A
Iocp=Ilimit+1/2Delta I =17.03~24.98A

2012/12/2

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/24	Deciphered Date	Date of EOP

Title	1.5VP/0.75VSP/1.8VSP		
Size	Document Number		Rev
Custom	Ezel M/B Schematics_LAA001P		1.0
Date:		Sheet 48 of 64	





VFB= 0.704V
Vo=VFB*(1+PR116+PR118/PR119)= 1.05V
Freq= 266~314KHz , 290KHz(typ)

+1.05VS
Ipeak=15.37A ;Iocp=18.44A ;Imax=10.76A
1/2Delta I=1.71A (F=290K Hz)
choose PR603=75Kohm
Rds(on)=5m ohm(max) ; Rds(on)=4.2m ohm(typical)
Iocp=Ilimit+1/2Delta I=18.88~26.4A

2012/12/02

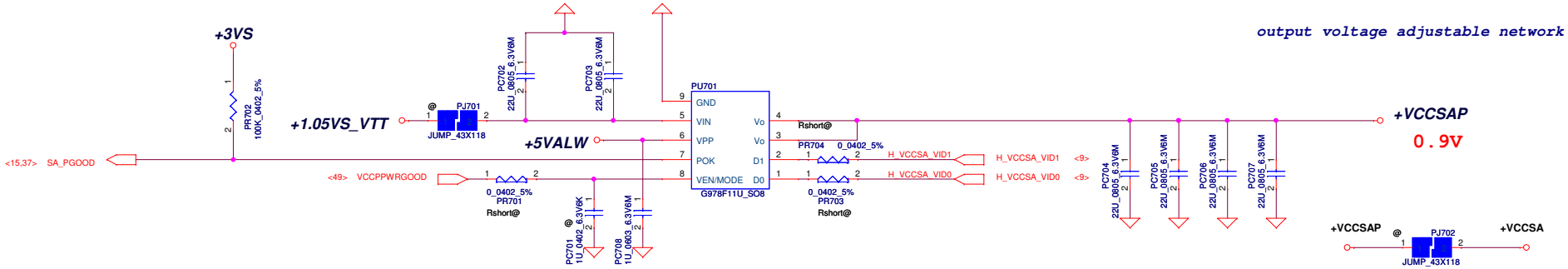
UMA Ipeak value equal to discrete

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	Date of EOP

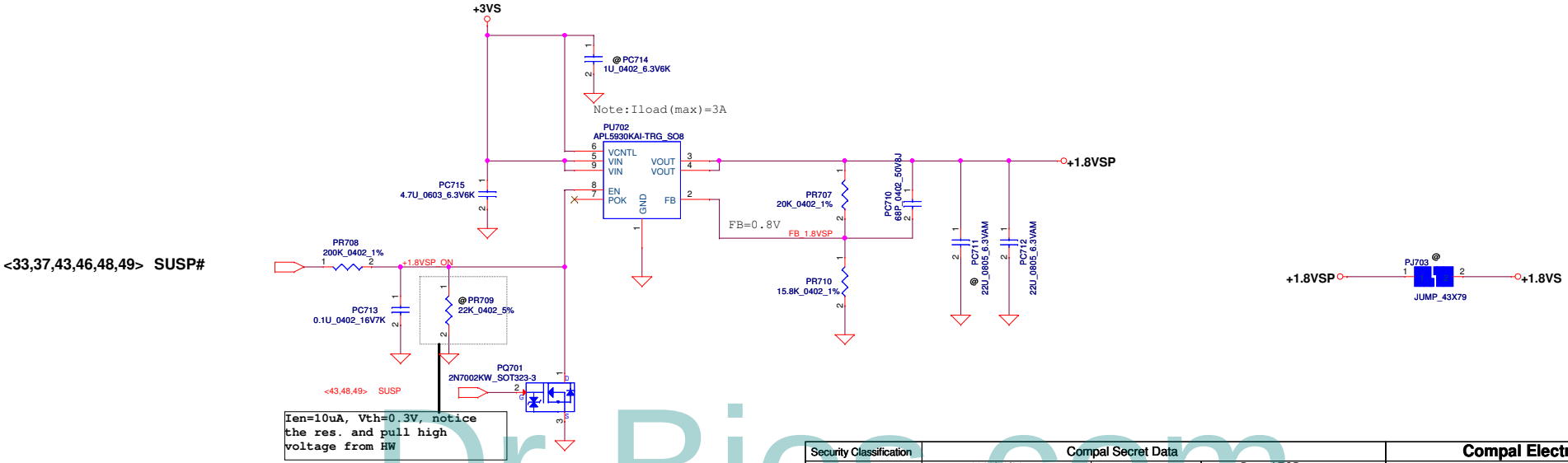
Compal Electronics, Inc.			
Title	+1.05VS_VTTP		
Size: Custom	Document Number: Ezel M/B Schematics_LAA001P		Rev: 1.0
Date:	Sheet 49 of 64		

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

output voltage adjustable network



Imax= 2A, Ipeak= 3A
FB=0.6V



Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	Date of EOP

Compal Electronics, Inc.			
Title	VCC_SAP/1.8VSP		
Size: Custom	Document Number: Ezel M/B Schematics_LAA001P		Rev: 1.0
Date:	Sheet 50 of 64		

Layout Note
SVID routing
1. Alert# signal must be routed between the Clock and Date lines to reduce the cross talk between them. Signal order arrangement: mobile order is Clock-Alert-Date.
2. SVID spacing requirement is 18mils(0.475mm).
3. Maximum total microstrip routing length of each SVID signal must not exceed 6000mils(152.4mm).
4. The SVID bus must be ground reference, It cannot be referenced to input (Vbat or 12V) power plans as they can couple noise into the SVID bus as power states change.
5. Avoid routing under noisy circuit, e.g. switch node , Gate driver, B+, Vin, high speed signal.
6. When SVID signal changes Layer, GND return path may be changed also. We need add GND via for GND reference.

Layout Note
Reduce Acoustic Noise
1. The AL bulk capacitor of B+ should be very close to CPU_CORE MOSFET.
2. Input ceramic caps must place on symmetry same location on top side and bottom side.

VDD source use +5VS and PGOOD source use +3VS
Please confirm power on and down sequence, make sure VGATE after CPU_CORE on.

OCP setting=39.9~44.99A

MDV1525 Vds=30V
Rds(on)=11.5~14m ohm@Vgs=4.5V

0.22uH DCR= 0.97+-5% m ohm, Idc~Isat= 25~34A

MDU1511 Vds=30V
Rds(on)=2.7~3.3m ohm@Vgs=4.5V

0.36uH DCR= 1.4+-5% m ohm, Idc~Isat= 25~34A

OCP setting=39.9~44.99A

Close GFX choke

Close GFX L/S MOS

Close CPU L/S MOS

Close CPU choke

PR18 and PR30
27.4K ohm for 100 degree
61.9K ohm for 110 degree

ISL95833HRTZ-T_TQFN32_4X4

PL701 PL702 Footprint用SH00000HQ00代替,因為SH00000NM00_R22為2PIN 2012/07/05

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	Date of EOP

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Compal Electronics, Inc.

Title: CPU_CORE/VGFX_CORE

Size: Custom | Document Number: Ezel M/B Schematics_LAA001P | Rev: 1.0

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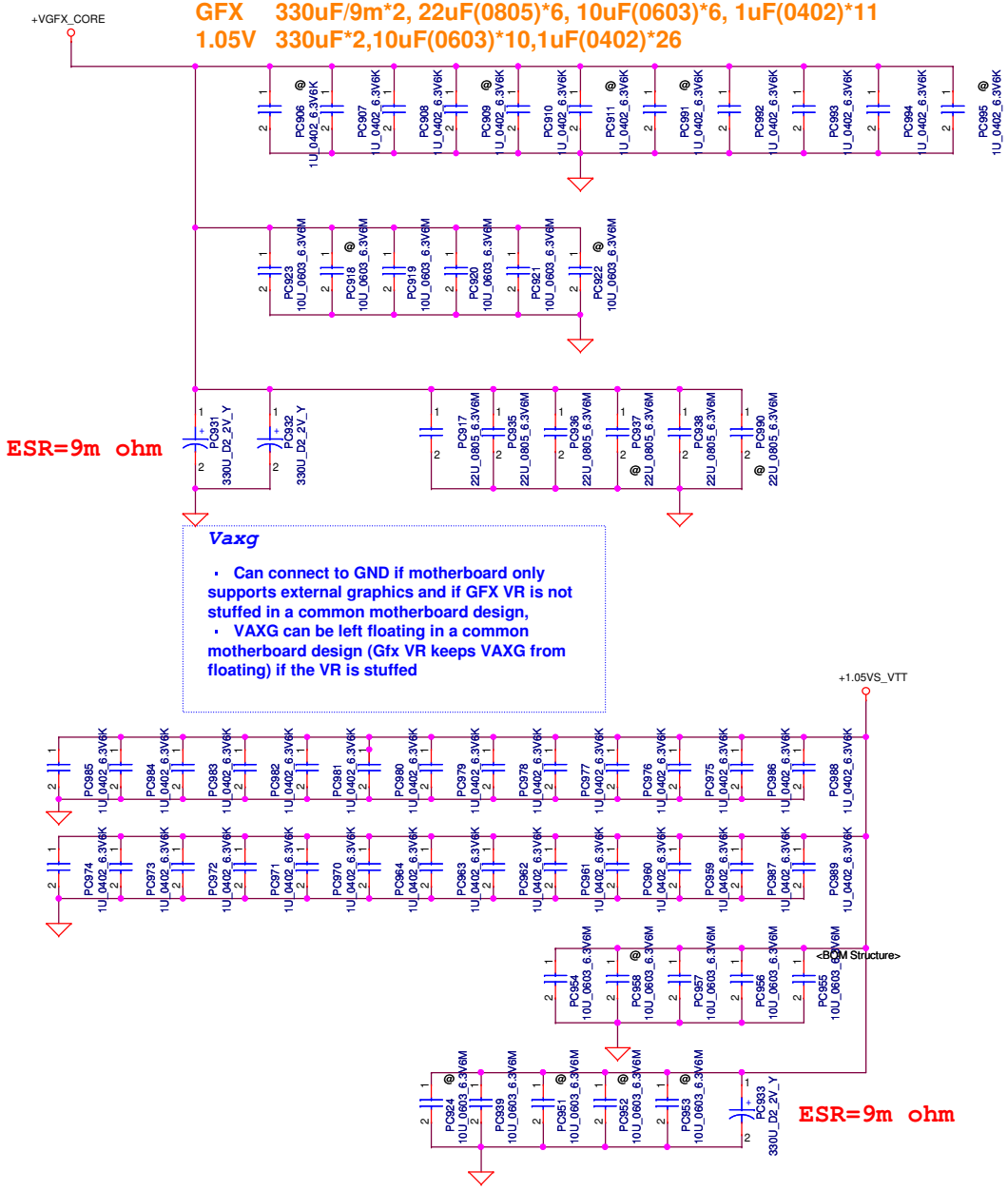
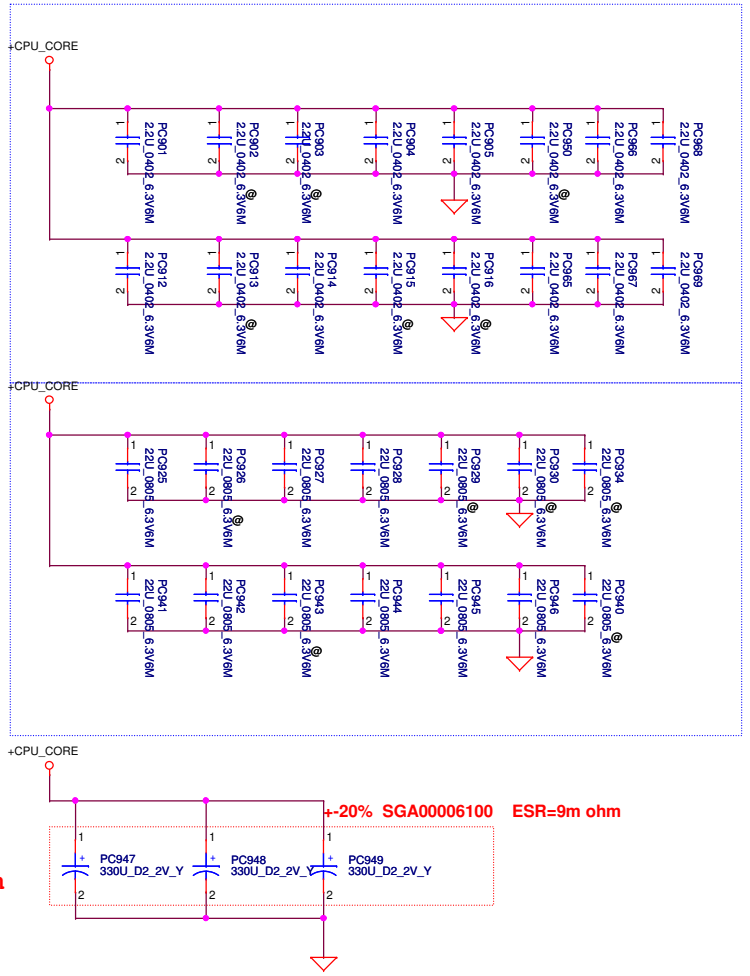
PWR Rule 17W@ULV(CR BGA1023_GT2) CPU2.9m GFx3.9m
CPU 330uF/9m *3, 22uF(0805) *12, 2.2uF(0402)*16
GFX 330uF/9m*2, 22uF(0805)*6, 10uF(0603)*6, 1uF(0402)*11
1.05V 330uF*2,10uF(0603)*10,1uF(0402)*26





ESR=9m ohm

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	Date of EOP

Compal Electronics, Inc.

Title: *CPU_CORE_CAP*

Size: Custom | Document Number: *Ezel M/B Schematics_LAA001P* | Rev: 1.0

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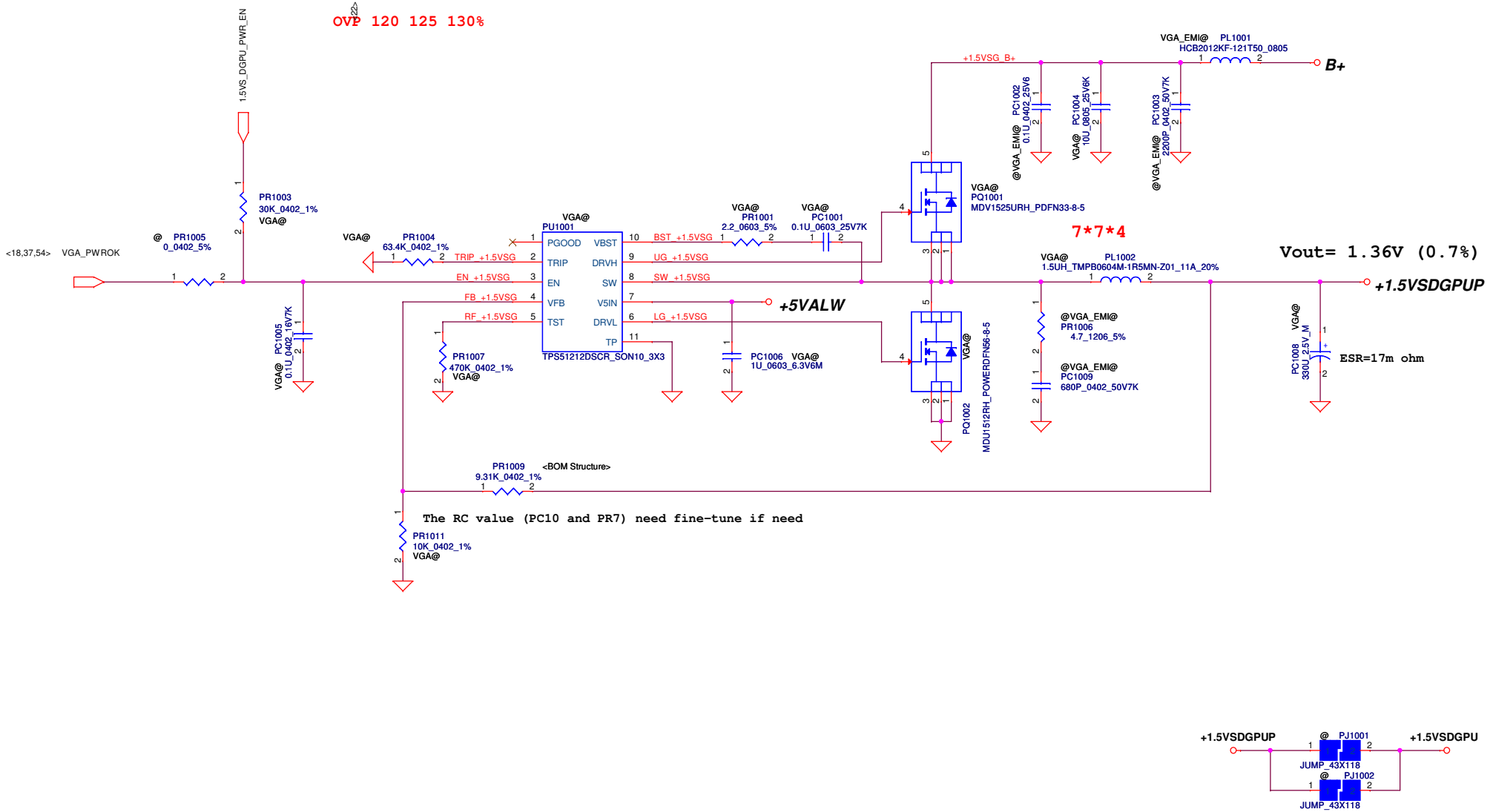
+1.5VSDGPU
Ipeak=12.5A ;1.2Ipeak=15A ;Imax=8.75A
1/2Delta I=1.08A (F=290K Hz)
PR1004=63.4Kohm
Rds(on)=5m ohm(max) ; Rds(on)=4.2m ohm(typical)
Iocp=Ilimit+1/2Delta I=15.16~21.5A
Iocp(min)>1.2Ipeak
2013/03/13



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/04/22	Deciphered Date	Date of EOP
Title	+1.5VSDGPUP		
Size Custom	Document Number		Rev 1.0
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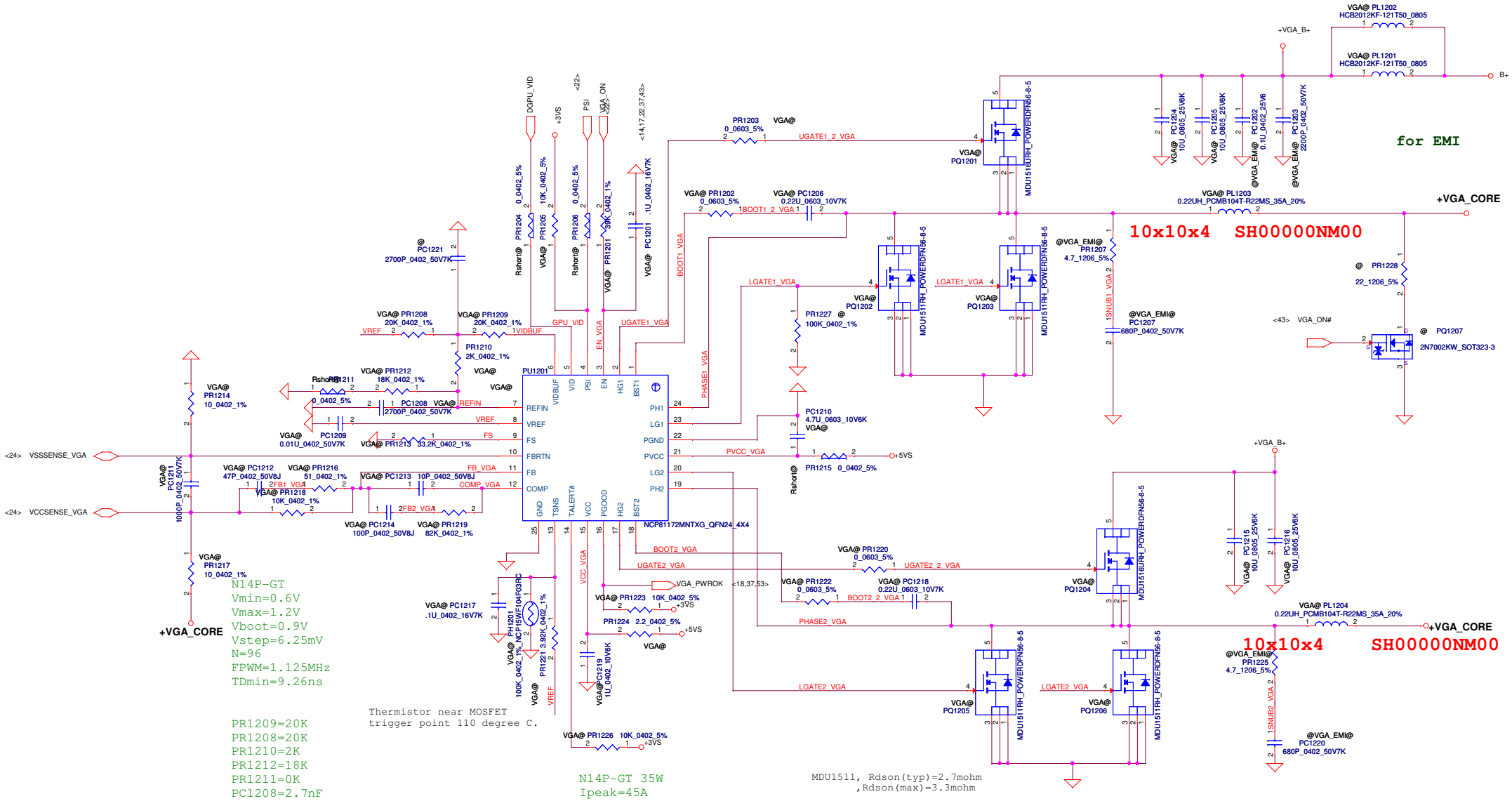


Security Classification	Compal Secret Data		
Issued Date	2011/12/05	Deciphered Date	Date of EOP

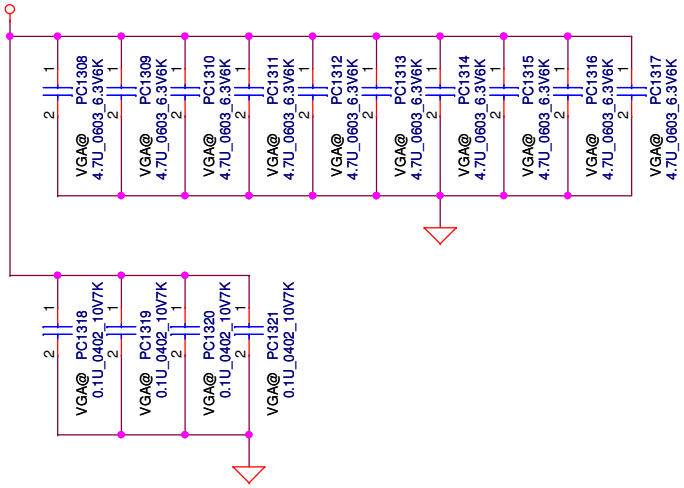
Compal Electronics, Inc.

Title: VGA_COREP

Size | Document Number | Rev 1.0

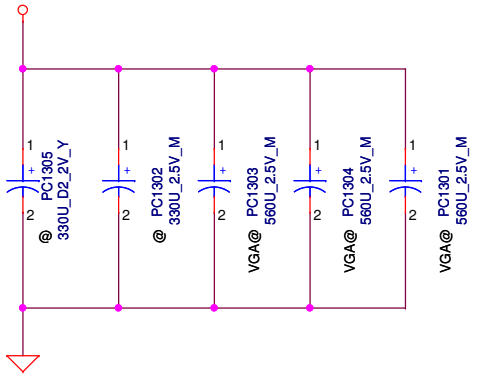
Date: Wednesday, March 13, 2013 | Sheet 54 of 64

+VGA_CORE Under VGA Core

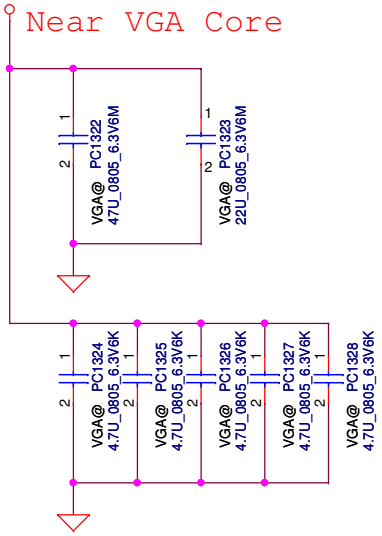


GB4-128
Under
4.7uF_0603_10pcs
0.1uF_0402_4pcs
Near
47uF_0805_1pcs
22uF_0805_1pcs
4.7uF_0805_5pcs

+VGA_CORE



+VGA_CORE
Near VGA Core



Compal Electronics, Inc.	
Title	VGA_CORE CAP
Size: Custom	Document Number: Rev 1.0
Date: Wednesday, March 13, 2013	Sheet 55 of 64

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Acoustic noise	3V 5V light load efficiency improvement		3V/5V	1.Add 2pcs 1K_0402_5% (PR412 PR413) 1pcs 4700P_0402_25V7K (PC425) 1pcs 0.047U_0402_25V7K (PC426) 2.Add 4.7u_0402_6.3V6M (PC401)	01/03	EVT
2	Silergy update revision	3V 5V enable control for Rev0.7. But un-pop.		3V/5V	Add un-pop 2pcs 0402 resistors(PR415 PR414)	01/03	EVT
3		UMA SKU VGA_CORE IC un-pop		VGA	PU1201 change to VGA@	01/03	EVT
4		Reduce part count		VGA	Change to R-short (PR1211 PR1204 PR1206 PR1215)	01/03	EVT
5		DFB: PC1305 PC1304 PC1303 PC1301 too close.		VGA	330U_2.5V_M_SF000002Z00 change to 330U_D2_2V_Y_SGA20331E10 (PC1305)	01/03	EVT
6		EMI risk fot CPU/GFX H-Side		CPU	Change 2pcs 0_0603_5% (PR809 PR827)	01/03	EVT
7		The modify values for CPU transition test		CPU	1. 422_0402_1% change to 604_0402_1% (PR807) 2. 0.22uH_SH000000200 change to 0.36uH_SH00000OJ00 (PL803)	01/03	EVT
8		modify charger current to meet battery charge time.		Charger	0.02_1206_1%_SD00000S110 charger to 0.01_1206_1%_SD00000K820	01/10	EVT
9		AC Mode no rest function		3V/5V	Del PQ401 2N7002KW_SOT323-3	02/18	DVT
10		VRAM efficiency improvement		1.5VDGPU	1.PQ1002 AON7702A_SB00000T600 change to MDU1512RH_POWERDFN56-8-5_SB00000SY00 2.PQ1001 AON7408L 1N DFN_SB00000H800 change to MDV1525URH 1N PDFN33-8_SB00000S600	02/18	DVT
11		When pwm IC shutdown on S0, EC could detect SLP_S5#, but cannot detect PCH was no power.		3V/5V	PR416 add 100K_0402_5%_SD028100380	02/18	DVT
12		The discharge time may cause GC6 entry/exit quickly fail, worry about the off time too long problem cause the GC6 fail.		VGA	PR1228 add un-pop 22_1206_5%_SD001220A80 PQ1207 add un-pop 2N7002KW_SOT323-3_SB000009Q80	02/18	DVT
13		The 5VALW will fast than 3VALW and the rising time will under 2mS.		3V/5V	PC426 4700P_0402_25V7K_SE075472K80 change to 0.01U_0402_25V7K_SE075103K80 PC425 0.047U_0402_25V7K_SE00000MJ00 change to 6800P_0402_25V7K_SE075682K80	02/18	DVT

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
14		VCIN1_function		OTP	1.90W@ PR225 3.3K_0402_1%_SD00000GW80 change to 6.19K_0402_1%_SD034619180 2.65W@ PR225 1.02K_0402_1%_SD034102180 change to 1.91K_0402_1%_SD000009O80 3.PR207 10K_0402_1%_SD034100280 change to 60.4K_0402_1%_SD034604280	02/18	DVT
15		VGA enable sequence for NV suggest.		VGA	PR1003 22K_0402_1%_SD034220280 change to 30K_0402_1%_SD034300280 PR1201 22K_0402_1%_SD034220280 change to 39K_0402_1%_SD034390280	02/18	DVT
16		VRAM voltage change to 1.35V.		1.5VDGPU	PR100911.5K_0402_1%_SD034115280 change to 9.31K_0402_1%_SD034931180 PR1004 137K_0402_1%_SD034137380 change to 63.4K_0402_1%_SD03463K280 PR318 499K_0402_0.1%_SD00000U380 change to 499K_0402_1%_SD034499380	03/13	PVT

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Title	PIR (PWR)		
Size: Custom	Document Number: Ezel M/B Schematics_LAA001P		Rev: 1.0
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Item	Page #	Function	Date	Request Owner	Issue Description	Solution Description	Rev.
1	33	HW	12/27/2012	Customer	To reserve DP++ circuitry to support dual-mode	reserve placeholder of Q46, Q48, Q49, R499, R501	Rev02
2	33	HW	12/27/2012	Compal	output from mDP connector cannot be normally transition	change R389 from 100k to 10k	Rev02
3	33	HW	12/27/2012	Compal	for safety concern	a. change U29 from AP2330W-7 to RB491D-YS b. also reserve one jump, J11, then track DVT result	Rev02
4	39	HW	12/27/2012	Compal	change PU domain for LID_SW#	change PU domain of R361 from +3VALW to +3VALW_EC	Rev02
5	39	HW	12/27/2012	Customer	remove LAN board	remove JLAN1, add JPWR1(A020419-SAHR22, the same as JBL1)	Rev02
6	39	HW	12/27/2012	Compal	add NPI test on/off button on M/B	add SW6	Rev02
7	39	HW	12/27/2012	Compal	update driving circuit for buzzer	add R519 and Q6	Rev02
8	33	HW	12/28/2012	Compal	recommandation from vendor	follow AE's comment, put the back drive current protection FET, Q16, between IC and connector	Rev02
9	34	HW	12/28/2012	Compal	recommandation from vendor	follow AE's comment, change R338 from 100k to 0ohm, and base on DVT's test result to see if okay to remove it or not	Rev02
10	9	HW	12/28/2012	Compal	ME height limit, caused by click-pad structure	remove C82, then reserve placeholder for C689 and C690	Rev02
11	38	HW	12/28/2012	Compal	to prevent back drive from WLAN module, change the PU power domain from 3VALW to 3V_WLAN	connect 3V_WLAN to R379 then move this component to the page related WLAN	Rev02
12	38	HW	12/28/2012	Compal	to avoid 0.02V leakage voltage on 3VS	change the connection direction of Q24A	Rev02
13	38	HW	12/28/2012	Compal	update board ID for DVT build	stuff R384(100k) and change R388 to 8.2k	Rev02
14	14,38	HW	12/28/2012	Customer	LAN/B request had been cancelled by customer	1. delete the connection of LAN_PWR_EN and EC_PME# 2. remove C628, C530, C682, C629 and JLAN1 3. remove C173 and C174	Rev02
15	38	HW	12/28/2012	Compal	no PU for Home-Key related signals	add RP45 for I2C and INT# signals to PU to 3VALW_EC	Rev02
16	38	HW	12/28/2012	Compal	wrong control signal for buzzer	swap pin connection for BT_ON# and BUZZ#	Rev02

Item	Page #	Function	Date	Request Owner	Issue Description	Solution Description	Rev.
17	38	HW	12/28/2012	Compal	no PU for volume tuning button	PU VOL_UP# and VOL_DOWN# to 3VS by RP45 and RP44 respectively	Rev02
18	32	HW	12/28/2012	Compal	1. abnormal display via redriver board 2. to solve the probelm without any gauge increased	add R521 and C129, then connects PIN27 fo JEDP1 to 3VS, this solution is only for cable which need to pass via re-drvier board	Rev02
19	38	HW	12/28/2012	Compal	for keyboard back light auto-negotiation	swap the pin connected for EC_SPOK and KB_BKL	Rev02
20	17	HW	12/28/2012	Compal	to reduce 0-ohm usage	1. remove R488 and R485 becuase GC6 is ready 2. remove R489 and R490 because GC6 is ready	Rev02
21	13	HW	12/30/2012	Compal	for long-term solution, use 64Mb to replace 32Mb+16Mb	change U18 as 8MB ROM part, and only reserve placeholder for U19	Rev02
22	14	HW	12/30/2012	Compal	to pervent potential back drive from PCH	correct PU domain for OC6# from 3VS to 3VALW_PCH	Rev02
23	20	HW	12/30/2012	Compal	to reduce 0-ohm usage	change R480 to J16 and change R78 to J17	Rev02
24	39	HW	12/30/2012	Compal	to reserve power source from 3VLP for LID	add R522 and R523	Rev02
25	39	HW	12/30/2012	Compal	short-term solution for battery no output with PMOS	add R376 and R299	Rev02
26	13	HW	01/03/2013	Compal	to trial-run single 8MB SPI ROM	add R300, R301, R302 and R303 and only stuff R302 and R303	Rev02
27	35	HW	01/03/2013	Compal	add PU resistor for A4 EC's GPIO5B's pin type	Add R393 as PU resistor, PU to 3VS_WLAN	Rev02
28	42	HW	01/03/2013	Compal	hole with diameter 6mm do not need screw hole footprint	remove H5	Rev02
29	33	HW	01/07/2013	Compal	change the CFG pin of Lightning-Bolt from 2 PMOS to 1 2 in 1 NMOS and one single channel NMOS	delete Q17 and Q18, then add Q50 and Q47	Rev02

Item	Page #	Function	Date	Request Owner	Issue Description	Solution Description	Rev.
30	33	HW	01/07/2013	Compal	to reduce the usage of 0-ohm	replace R309 and R310 by jumps (J11 and J12)	Rev02
31	38	HW	01/07/2013	Compal	change the power domain of EC	connects EC power from +3VALW to +3VLP, stuff R513 and also change the power domain of lid switch as EC--> stuff R522	Rev02
32	6	HW	01/07/2013	Compal	for known issue from DM meeting about RST_GATE#	change R520 from 0-ohm to 100k	Rev02
33	32	HW	01/07/2013	Compal	to reduce EDP cable's gauge	add R521 and C129 to replace HPD signal by +LCDVDD, but still reserve R298 and R391 as back-up	Rev02
34	20	HW	01/07/2013	Compal	default as no Erp Lot 6 concern for PCH power	remove R479	Rev02
35	13	HW	01/07/2013	Compal	SPI uses single device topology	remove R67 and RP12	Rev02
36	39	HW	01/07/2013	Compal	no need to PU twice for LID_SW#	remove R400	Rev02
37	33	HW	01/07/2013	Compal	PU LB_RST when not in debug mode	add R324 with 47k	Rev02
38	18	HW	01/15/2013	Compal	to identify SKUs have TPM solution or not	after aligning with SW team, add R116 and R118 for DVT	Rev02
39	39	HW	01/15/2013	Compal	let lid swich has the same power domain as EC	stuff R522, and de-pop R523	Rev02
40	33	HW	01/17/2013	Compal	update the config1 and config2 control circuit	remove Q50, Q47 and R390 and replaced by Q36 and Q38	Rev03
41	33	HW	01/29/2013	Compal	to reduce 0-ohm usage	remove R316 and R317	Rev03
42	33	HW	01/29/2013	Compal	to remove placeholder for depop. components	remove SW1	Rev03
42	33	HW	01/29/2013	Compal	to remove placeholder for depop. components	remove LED3 and R318	Rev03

Item	Page #	Function	Date	Request Owner	Issue Description	Solution Description	Rev.
43	33	HW	01/29/2013	Compal	to remove placeholder for depop. components	remove R375--> back-dirve just depends on the configuration of external device. for this unexpected situation, we need to keep protect FET present	Rev03
44	33	HW	01/29/2013	Compal	to reduce components which might interfered by RF frame	remove R400, R517 and change R522 and R523 to 0402 size	Rev03
45	32	HW	01/30/2013	Compal	ESD test fail	add C446 (22p capacitor) close to sensor connector for ESD	Rev03
46	13	HW	01/30/2013	Compal	8MB SPI ROM ready	change BOM structure of R75 and R76 to "@"	Rev03
47	38	HW	01/30/2013	Compal	normally update board ID for PVT PCB	change R338 from 8.2k to 18k	Rev03
48	40	HW	01/31/2013	Compal	no need to connect BEEP# from EC	depop R422 first then track PVT result	Rev03
49	41	HW	02/01/2013	Compal	no too many problems from EC, change EC power domain to +3VLP	change R513 to short pad	Rev03
50	44	HW	02/03/2013	Compal	for VGA sequence	R469 change from 47k to 270k	Rev03
51	18	HW	02/03/2013	Compal	ESD test fail	add C472, 0.1uF, on mSATA_DET# and close to PCH	Rev03
52	33.34	HW	02/05/2013	Compal	for cost saving and USB safety concern	add U38 (USB power switch) and C526 change R338 from 0-ohm to 100-ohm for discharge circuit replace C457 by C691 and C692 then stuff one of them remove Q19,Q20,R333,R447,Q45,U31,R337,R334,R476 change connection of LB_CHARGE_OFF to test point only	Rev03
53	42	HW	02/05/2013	Compal	request from ME	change H18 from 3P0 to 4P5	Rev03
54	32,38	HW	02/05/2013	Compal	no need to support wake-up function by home-key	change power to home key from +3VALW to +3VS, change PU domain for home key related signals to +3VS	Rev03
55	39	HW	02/05/2013	Compal	to prevent worse contact for safety screw hole	change H9 footprint to CLIP_SHAPE8P5X7P0-S	Rev03

Item	Page #	Function	Date	Request Owner	Issue Description	Solution Description	Rev.
56	9	HW	02/05/2013	Compal	to reduce depop. components	remove C93, C689, C128, C109, C110, C123, C125, C407 , C467, C470, C471, R92, C502, C500, R365, C524, C536 ,C592, C542, C560, C658, C659, C660, C661, C664, R70, R71, R111, R117 change to stuff C111, C112, C126	Rev03
57	34	HW	02/05/2013	Compal	for part count reduction, idea from EC	depop R393, R344 and Q23 first then track PVT result	Rev03
58	36	HW	02/06/2013	Compal	to avoid assembly interfere	remove C504	Rev03
59	36	HW	02/06/2013	Compal	to reduce 0-ohm usage	change R407, R408 and R409 from 0-ohm to R-Shotr	Rev03
60	35	HW	02/06/2013	Compal	add Frame for RF, for USB 3.0 signal noise	add CLIP1	Rev03
61	20	HW	02/18/2013	Compal	to reduce system power under S4/S5	stuff Q39 and U28 for 3V/5V PCH power	Rev03
62	38	HW	02/18/2013	Compal	reset battery is defined and toggled only by battery only & and change the design circuit to prevent battery no output caused by PMOS	del Q28, R403 and D29 add R390, 100k and PU to +RTCVCC remove C533	Rev03
63	43	HW	02/18/2013	Compal	after checking VGA sequence, discharge circuit is not needed for 3VSDGPU	no stuff R461 and Q34	Rev03
64	14	HW	02/18/2013	Compal	for part count reduction	remove R515 and let SMB_ALERT# connect to RP16	Rev03
65	36	HW	02/18/2013	Compal	to avoid components' interfere	no stuff C593, C581, C575, C578, C579, C580	Rev03
66	38	HW	02/18/2013	Compal	to correct switch button type	remove SW6	Rev03
67	40	HW	02/18/2013	Compal	to solve the not balance volume output from R/L speaker	change R434 from 1k to 1.2k	Rev03

Item	Page #	Function	Date	Request Owner	Issue Description	Solution Description	Rev.
68	38	HW	02/18/2013	Compal	not request from EMC and no reason to keep	no stuff C531	Rev03
69	32	HW	02/18/2013	Compal	to avoid unstable configuration for HPD cause anything wrong	stuff R298 and R391, then depop. R521 and C129	Rev03
70	40	HW	02/23/2013	Customer	to avoid too large deviation cause problems for speaker volume	keep resistance of R434,R437,R426,R429 as before but change the tolerance from 5% to 1%	Rev03
71	4,6	HW	03/10/2013	Customer	to improve thermal problem and base upon request from our end-customer, change PEG CFG to 8X	depop C1,C2,C3,C4,C5,C6,C7,C8,C17,C18,C19,C20, C21,C22,C23,C24,C33,C34,C35,C36,C37,C38,C39,C40, C49,C50,C51,C52,C53,C54,C55,C56 add R27 and R28 for PEG CFG to strap to 8-Lane	Rev10
72	34	HW	03/10/2013	Customer	cancel the request to for IOAC supported	add J18 then depop. C468 and U33	Rev10
73	33	HW	03/10/2013	Comapl	to prevent HD3SS2521 only works on DP mode after system cold-boot	swap pin-3 and pin-4 of Q48A	Rev10
74	39	HW	03/11/2013	Comapl	to prevent pop noise	add U25, R294 and R87	Rev10
75	33	HW	03/12/2013	Comapl	follow TI AE's recommendation	chagne R320 to 100k and remove R319 then connected the signal directly	Rev10
75	32	EMI	03/12/2013	Comapl	to fix EMI solution and remove unnecessary items	del R293, R297 and L13 then pass the signal directly del R304, R305 and L14 then pass the signal directly del R410, R412, R413, R414 then pass the signals directly del R430, R431, R435, R436 then pass the signals directly del R440, R445, R447 then pass the signals directly	Rev10
76	32	ESD	03/12/2013	Comapl	request from ESD	change R446 from 22p to 100p	Rev10
77	32	ESD	03/12/2013	Comapl	to fix ESD solution and remove unnecessary items	remove D30, D31, D32, D33	Rev10

Item	Page #	Function	Date	Request Owner	Issue Description	Solution Description	Rev.
1	22,44	HW	01/23/2013	Compal	to meet VGA sequence	1.change R154 to 10k 2.change R469 to 270k	Rev02
2	27~30	HW	01/23/2013	Compal	to reduce 0.1uF usage for VRAM	de-pop C303,C306,C331,C334,C357,C370,C394,C395	Rev02
3	22,23	HW	01/23/2013	Compal	to reduce 0 ohm usage	change R153,R177,R178 to R-short	Rev03
4	22,24	HW	01/23/2013	Compal	to reduce part count	1.change R137,R139,R140,R141 to RP46 2.change R142,R180,R181,R269 to RP47 3.remove R149	Rev03
5	22	HW	01/23/2013	Compal	simplefy GC6 function circuit	1.change to Diode for GC6_CLAMP_MON remove R509,R268,Q43,Q44B. add D7, R360 2.change Q44A to Q45(single MOS)	Rev03
6	27~30	HW	02/02/2013	Compal	to reduce de-pop part count	1.De-pop C296,C361,C386 and pop C311,C362,C376 for 10uF. 2.remove C296,C297,C303,C306,C312,C326,C331,C334,C336,C337, C348,C357,C361,C363,C370,C386,C387,C388,C394,C395.	Rev03
7	24	HW	02/23/2013	Compal	for thermal issue	downgrade the frequeceny by change R174 from 24.9k to 34.8k	Rev03

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