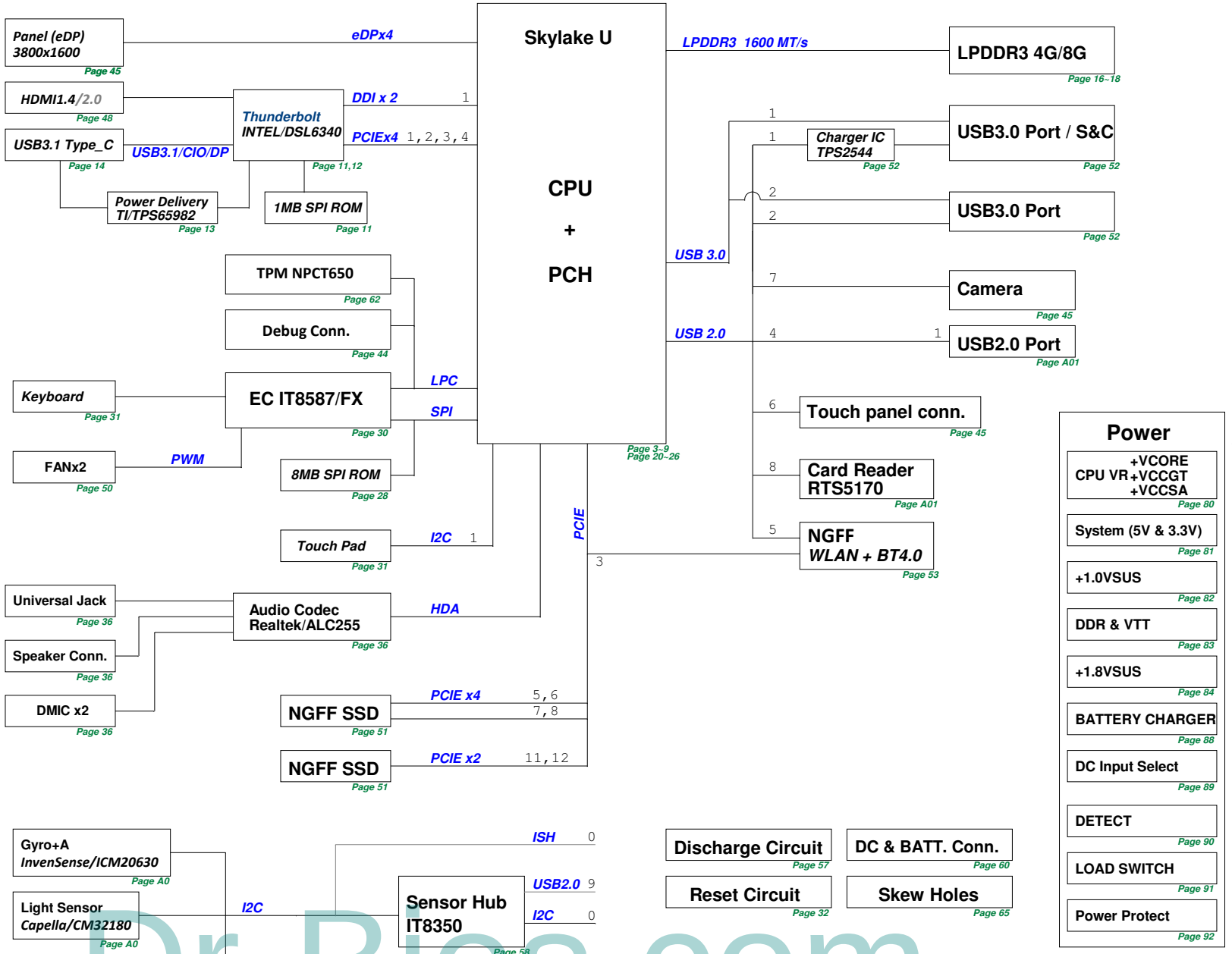
SKI2 Schematics for SKL-U Platform pre Rev 2.0

BLOCK DIAGRAM

SYSTEM PAGE REF.



PEGATRON Title : Block Diagram
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1/HW2
Engineer: Dep.3/Sec.3
Size C | Project Name P3HCJ | Rev 2.0
Date: Thursday, September 03, 2015 | Sheet 1 of 100

EC GPIO	Use As	Signal Name

EC GPIO	Use As	Signal Name

PEGATRON Title : GPIO Setting

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW2 Engineer: Dep.3/Sec.3

Size	Project Name	Rev
C	P3HCJ	2.0

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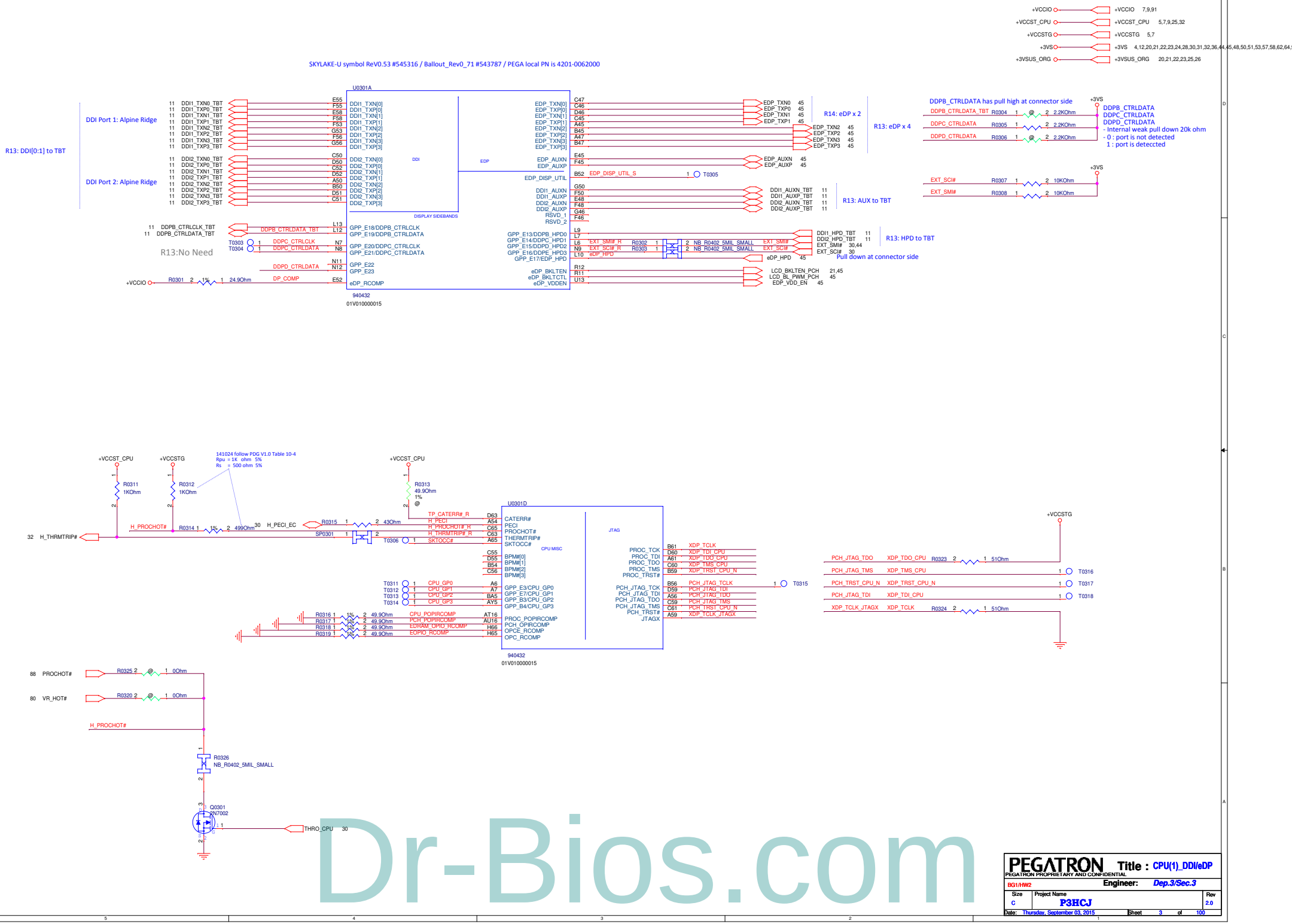
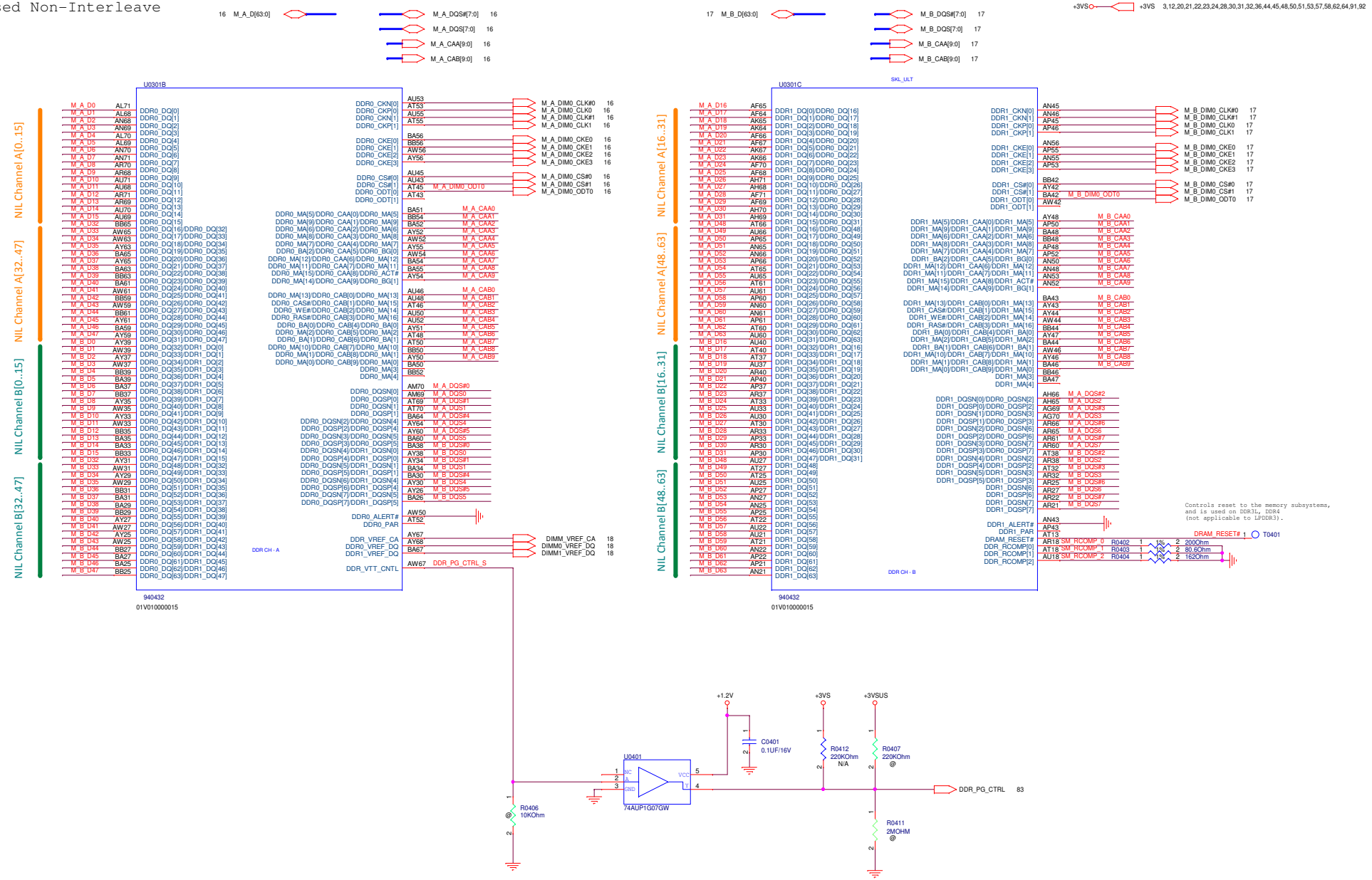

+VCCIO 7,9,91
+VCCST_CPU 5,7,9,25,32
+VCCSTG 5,7
+3VS 4,12,20,21,22,23,24,28,30,31,32,36,44,45,48,50,51,53,57,58,62,64,91,92
+3VSUS_ORG 20,21,22,23,25,26
SKYLAKE-U symbol ReV0.53 #545316 / Ballout_Rev0_71 #543787 / PEGA local PN is 4201-0062000
U0301A
DDI Port 1: Alpine Ridge
DDI Port 2: Alpine Ridge
R13: DDI[0:1] to TBT
DDI
EDP
DISPLAY SIDEBANDS
940432
01V010000015
R14: eDP x 2
R13: eDP x 4
DDPB_CTRLDATA has pull high at connector side
DDPB_CTRLDATA
DDPC_CTRLDATA
DDPD_CTRLDATA
- Internal weak pull down 20k ohm
- 0 : port is not detected
1 : port is deteccted
R13: AUX to TBT
R13: HPD to TBT
Pull down at connector side
R13:No Need
141024 follow PDG V1.0 Table 10-4
Rpu = 1K ohm 5%
Rs = 500 ohm 5%
U0301D
CPU MISC
JTAG
940432
01V010000015
THRO_CPU 30
Dr-Bios.com
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : CPU(1)_DDI/eDP
Engineer: Dep.3/Sec.3
BG1/HW2
Size C
Project Name P3HCJ
Rev 2.0
Date: Thursday, September 03, 2015
Sheet 3 of 100

T25S used Non-Interleave



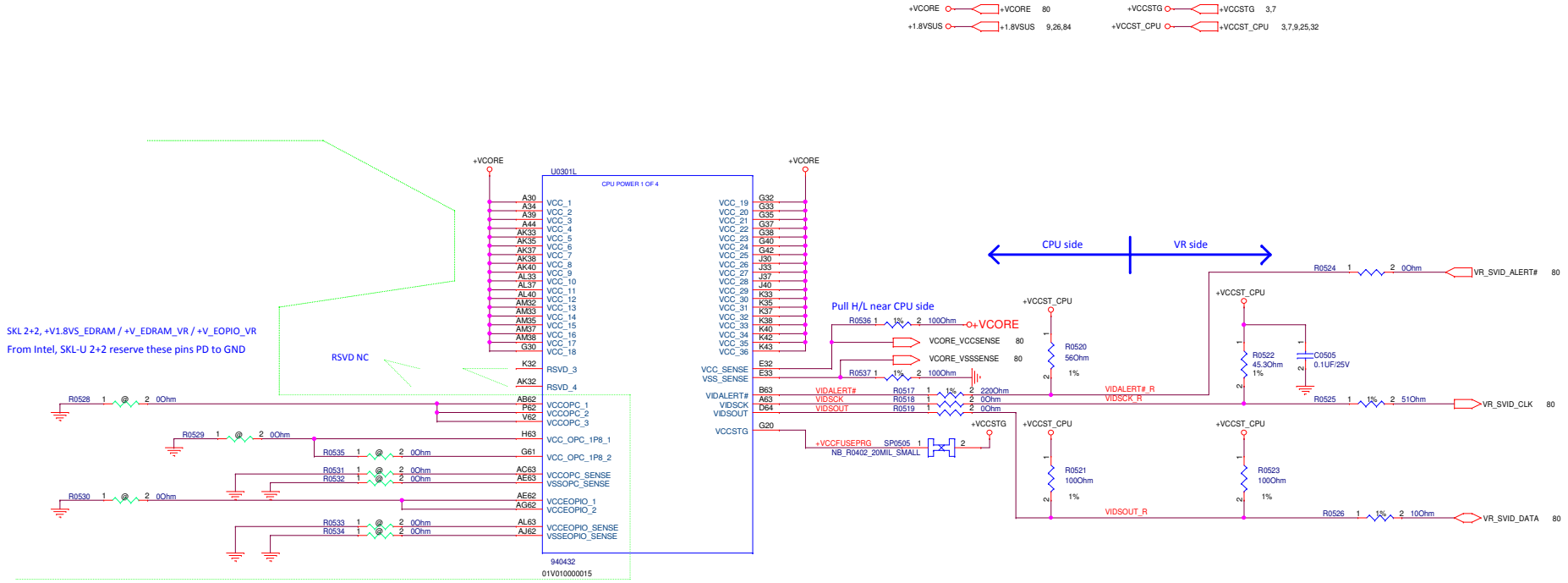
PEGATRON Title : CPU(2)_DDR3L

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1 Engineer: Dep.3/Sec.3

Size	Project Name	Rev
C	P3HCJ	2.0

Date: Thursday, September 03, 2015 Sheet 4 of 100



PEGATRON
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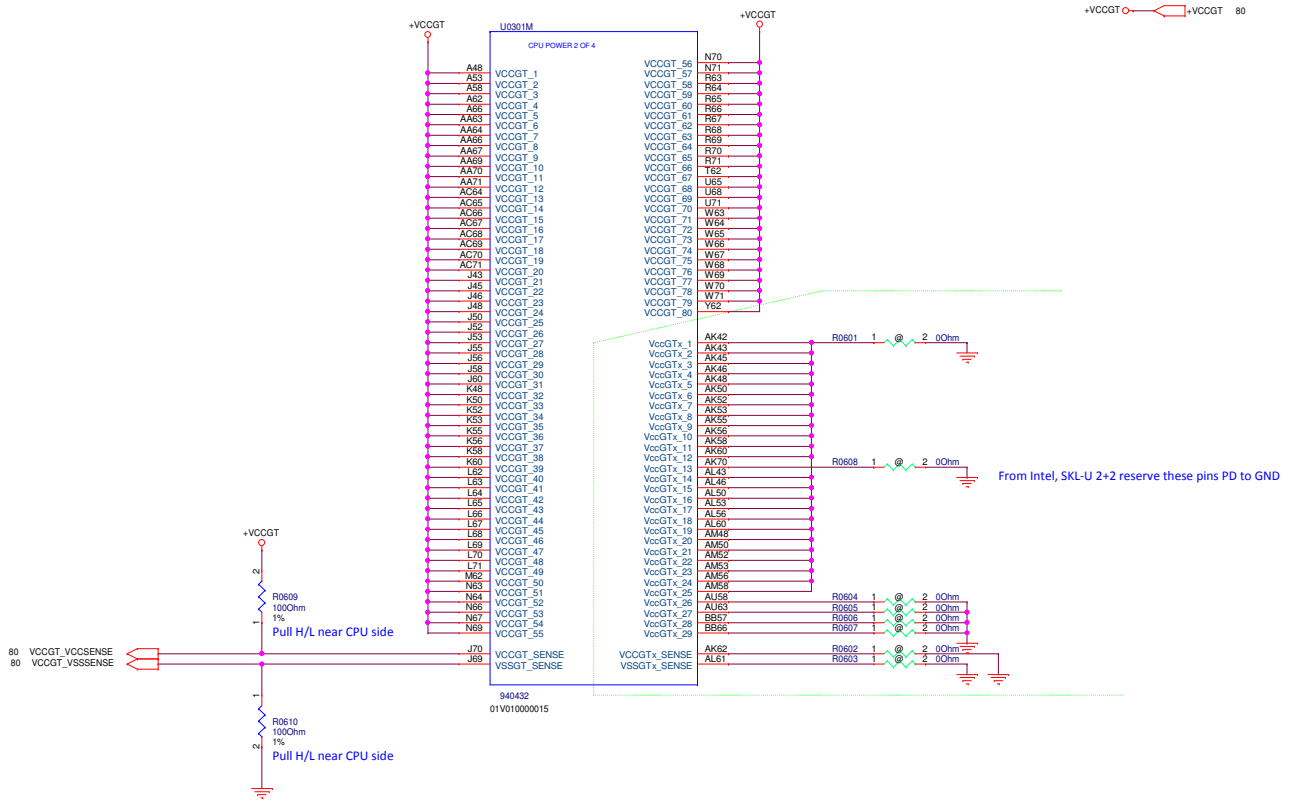
Title : CPU(3)_+VCCCORE

BG1/HW2

Engineer: Dep.3/Sec.3

Size	Project Name	Rev
C	P3HCJ	2.0

Date: Thursday, September 03, 2015 Sheet 5 of 100



PEGATRON Title : CPU(4)_+VCCGT

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW2 Engineer: Dep.3/Sec.3

Size	Project Name	Rev
C	P3HCJ	2.0

Date: Thursday, September 03, 2015 Sheet 6 of 100

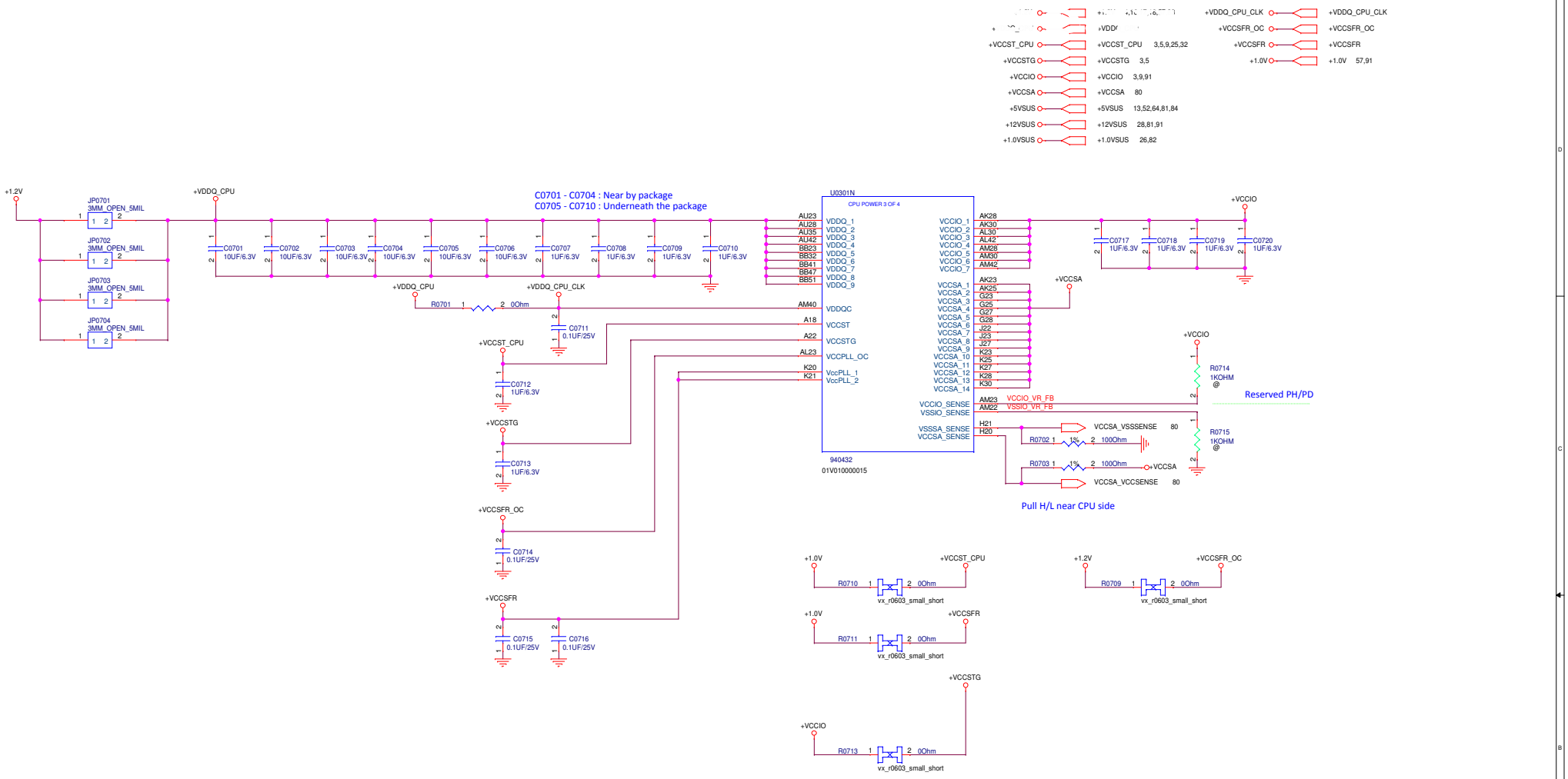
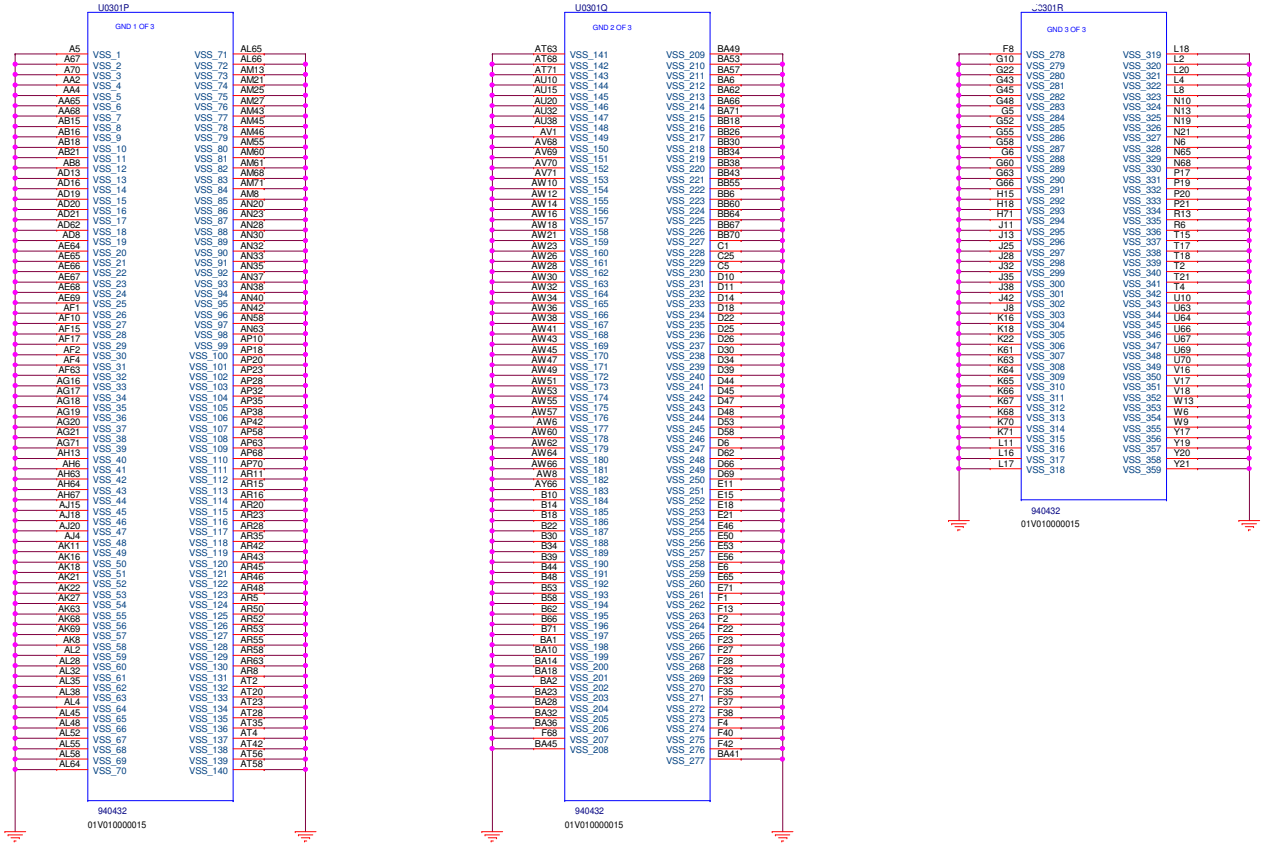


Table 5-1. Power Rail Requirements — Volume Segment — U-Line

Load switch (LS)	LS ENABLE	Load/Rail name	Imax (A)
<= 65usec full load ready (Note 16)	SLP_S4#	Vcc_{ST}	0.04
		Vcc_{PLL}(Vcc_{SFR})	0.12
<= 65usec full load ready	SLP_S3# AND SLP_S0#	VccIO	3.0
		Vcc_{STG}	0.04

16. VCCST ramp time can potentially be slowed than listed, depending on platform design. However, all timings documented in the PSS chapter must be met, specifically Tcpu_04

reference 543977_543977_SKL_PDDG_Rev0_91



PEGATRON Title : CPU(6)_CPU GND

PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: Dep.3/Sec.3

BG1/HW2

Size	Project Name	Rev
C	P3HCJ	2.0

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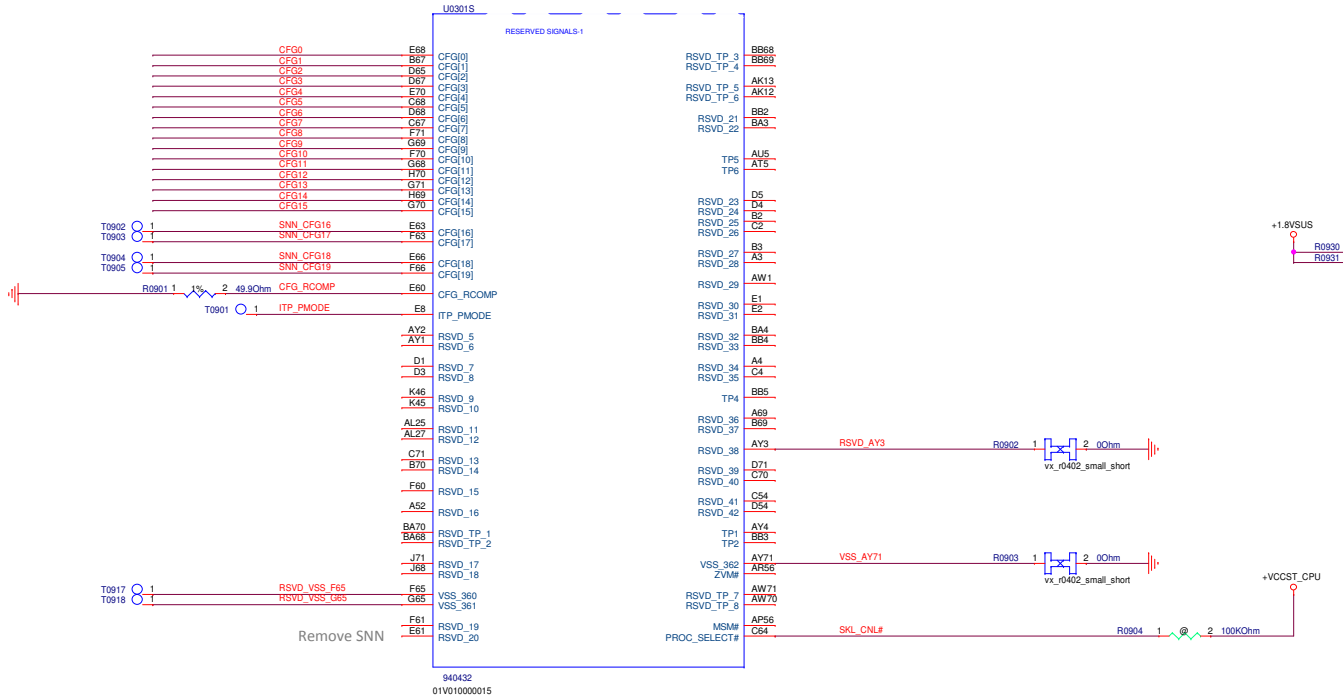

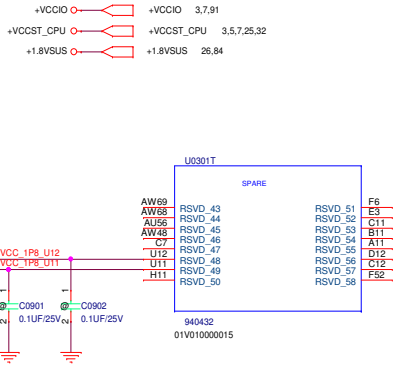

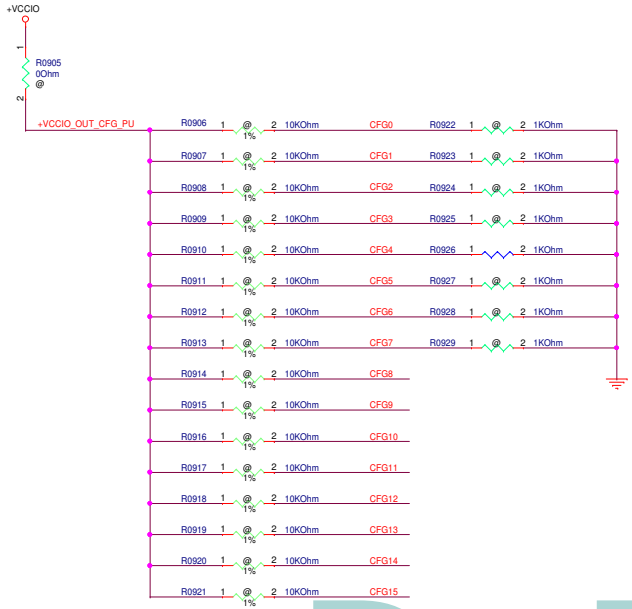

6.4 Reset and Miscellaneous Signals

Table 6-8. Reset and Miscellaneous Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. Intel recommends placing test points on the board for CFG pins. • **CFG[0]:** Stall reset sequence after PCU PLL lock until de-asserted: — 1 = (Default) Normal Operation; No stall. — 0 = Stall. • **CFG[1]:** Reserved configuration lane. • **CFG[2]:** PCI Express* Static x16 Lane Numbering Reversal. — 1 = Normal operation — 0 = Lane numbers reversed. • **CFG[3]:** Reserved configuration lane. • **CFG[4]:** eDP enable: — 1 = Disabled. — 0 = Enabled. • **CFG[6:5]:** PCI Express* Bifurcation — 00 = 1 x8, 2 x4 PCI Express* — 01 = reserved — 10 = 2 x8 PCI Express* — 11 = 1 x16 PCI Express* • **CFG[7]:** PEG Training: — 1 = (default) PEG Train immediately following RESET# de assertion. — 0 = PEG Wait for BIOS for training. • **CFG[19:8]:** Reserved configuration lanes.	I/O	GTL	SE	All processor lines. CFG[2], CFG[6:5] and CFG[7] are relevant for H and S-processor line only and test point may be placed on the board for them.

PEGATRON Title :CPU(7)_CFG/RSVD
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1/HW2 Engineer: Dep.3/Sec.3
Size C | Project Name P3HCJ | Rev 2.0
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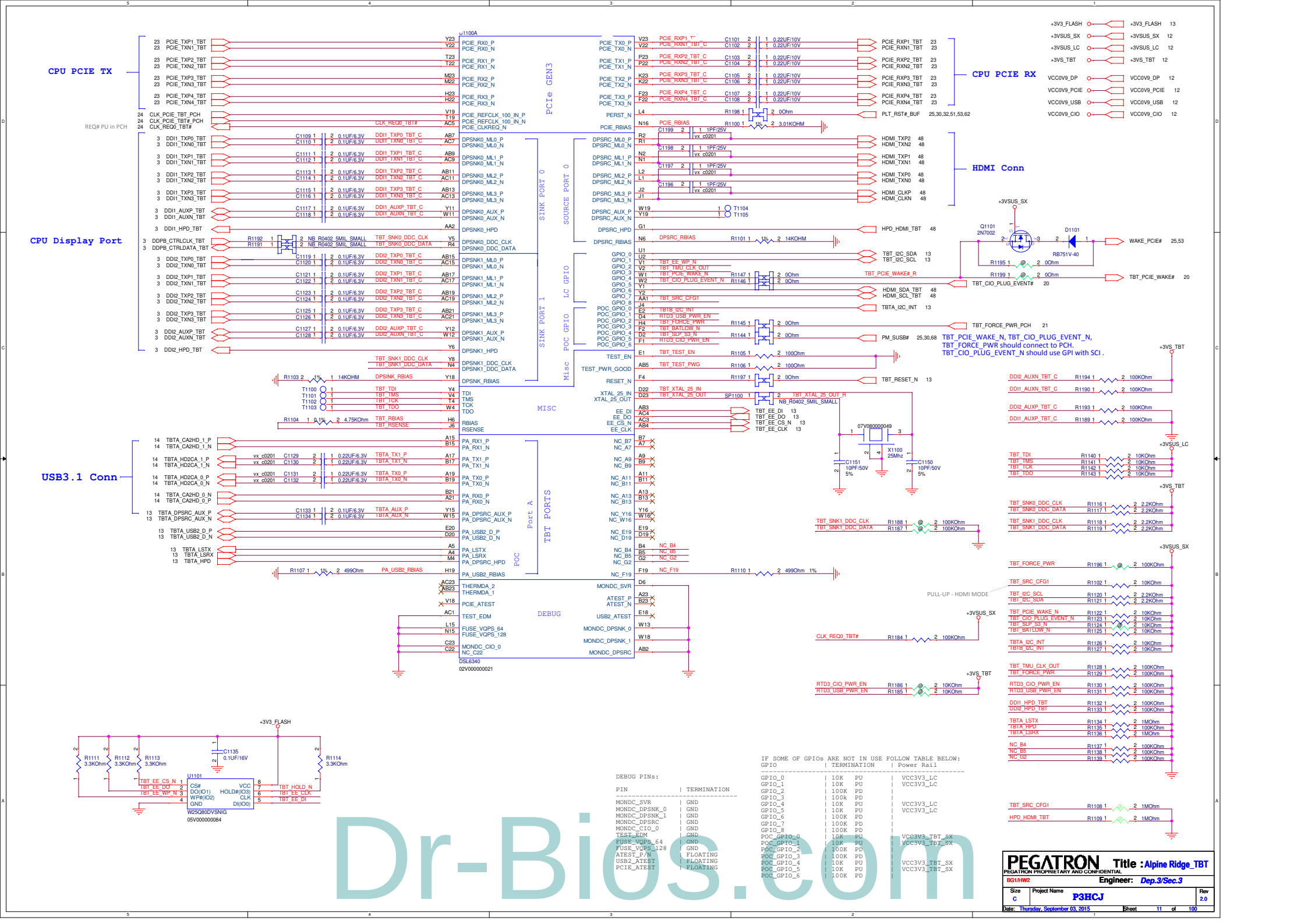
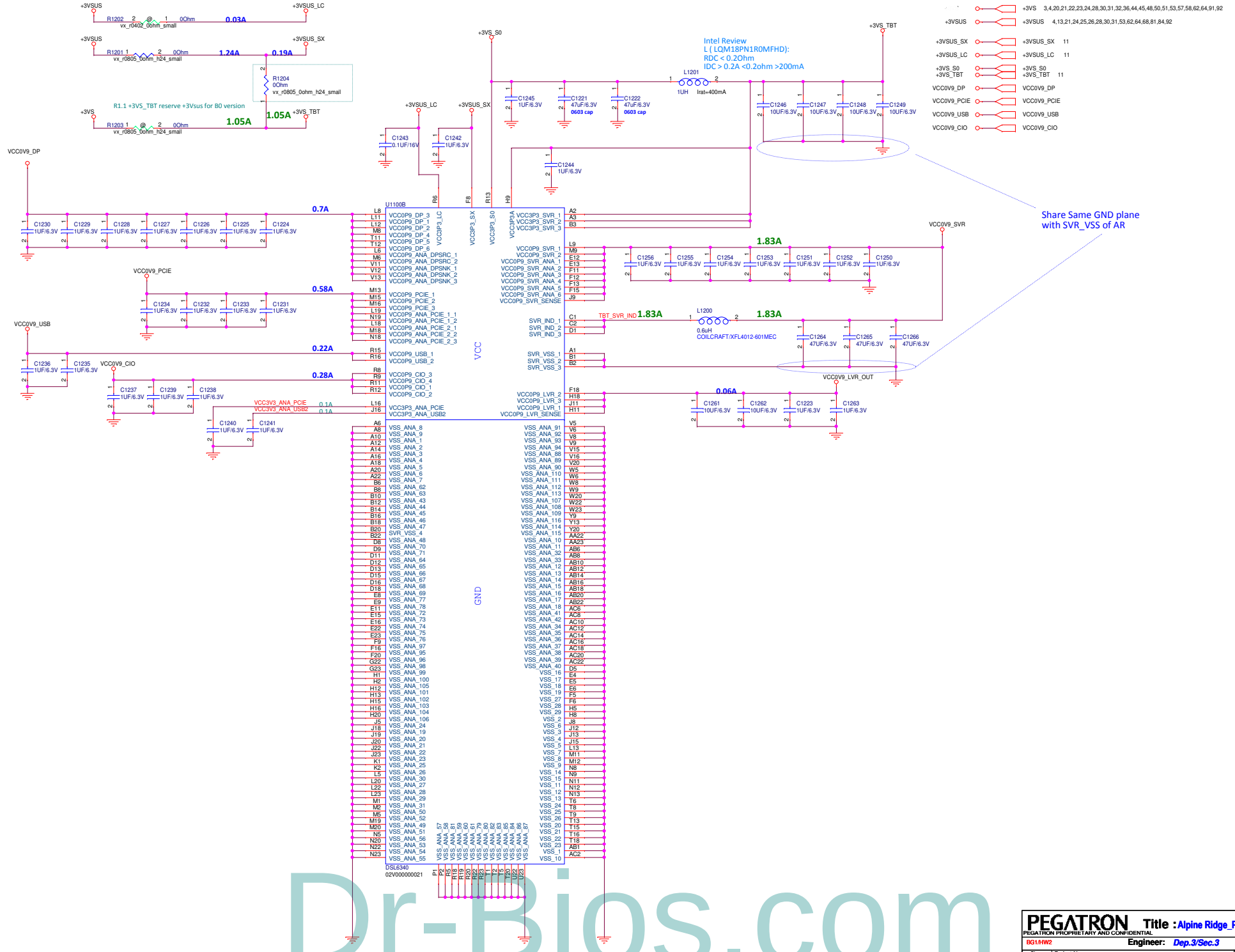

CPU PCIE TX
CPU PCIE RX
CPU Display Port
HDMI Conn
USB3.1 Conn
PCIe GEN3
SINK PORT 0
SOURCE PORT 0
SINK PORT 1
LC GPIO
POC GPIO
Misc
MISC
TBT PORTS
Port A
POC
DEBUG
U1100A
DSL6340
02V000000021
PEGATRON
Title : Alpine Ridge_TBT
Engineer: Dep.3/Sec.3
P3HCJ
Dr-Bios.com



PEGATRON Title : Alpine Ridge_PWR
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1/HW2 Engineer: Dep.3/Sec.3
Size C | Project Name P3HCJ | Rev 2.0
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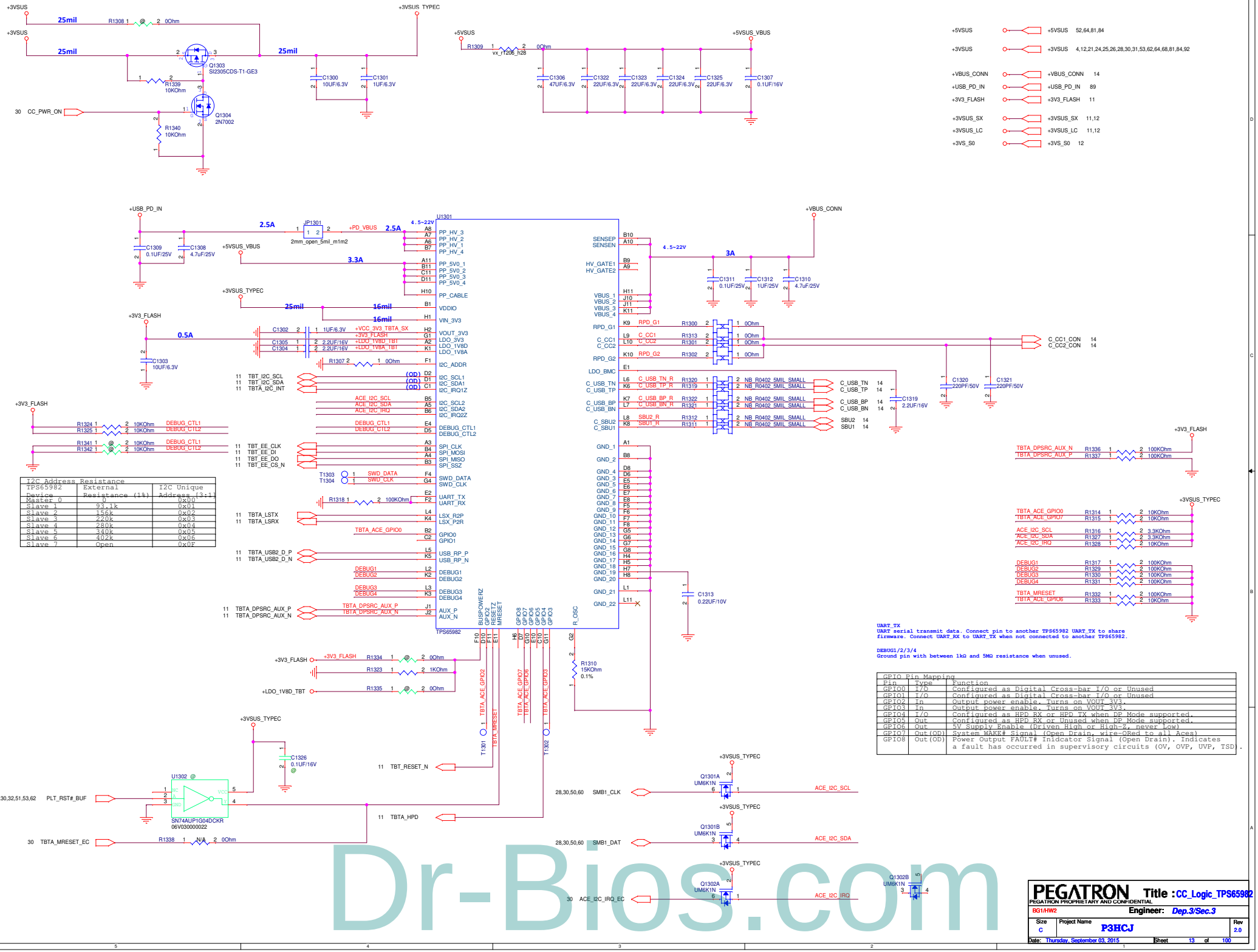
+3VSUS
25mil
R1308 0Ohm
+3VSUS_TYPEC
Q1303 SI2305CDS-T1-GE3
R1339 10KOhm
C1300 10UF/6.3V
C1301 1UF/6.3V
30 CC_PWR_ON
R1340 10KOhm
Q1304 2N7002
+5VSUS
R1309 0Ohm
+5VSUS_VBUS
C1306 47UF/6.3V
C1322 22UF/6.3V
C1323 22UF/6.3V
C1324 22UF/6.3V
C1325 22UF/6.3V
C1307 0.1UF/16V
+5VSUS 52,64,81,84
+3VSUS 4,12,21,24,25,26,28,30,31,53,62,64,68,81,84,92
+VBUS_CONN 14
+USB_PD_IN 89
+3V3_FLASH 11
+3VSUS_SX 11,12
+3VSUS_LC 11,12
+3VS_S0 12
+USB_PD_IN
2.5A
JP1301
2mm_open_5mil_m1m2
+PD_VBUS
C1309 0.1UF/25V
C1308 4.7uF/25V
+5VSUS_VBUS
3.3A
U1301
4.5~22V
PP_HV_3
PP_HV_2
PP_HV_1
PP_HV_4
PP_5V0_1
PP_5V0_2
PP_5V0_3
PP_5V0_4
PP_CABLE
+3VSUS_TYPEC
25mil
16mil
VDDIO
VIN_3V3
+3V3_FLASH
0.5A
C1303 10UF/6.3V
C1302 1UF/6.3V
C1305 2.2UF/16V
C1304 2.2UF/16V
+VCC_3V3_TBTA_SX
+3V3_FLASH
+LDO_1V8D_TBT
+LDO_1V8A_TBT
VOUT_3V3
LDO_3V3
LDO_1V8D
LDO_1V8A
I2C_ADDR
R1307 0Ohm
11 TBT_I2C_SCL
11 TBT_I2C_SDA
11 TBTA_I2C_INT
I2C_SCL1
I2C_SDA1
I2C_IRQ1Z
ACE_I2C_SCL
ACE_I2C_SDA
ACE_I2C_IRQ
I2C_SCL2
I2C_SDA2
I2C_IRQ2Z
DEBUG_CTL1
DEBUG_CTL2
11 TBT_EE_CLK
11 TBT_EE_DI
11 TBT_EE_DO
11 TBT_EE_CS_N
SPI_CLK
SPI_MOSI
SPI_MISO
SPI_SSZ
T1303
T1304
SWD_DATA
SWD_CLK
R1318 100KOhm
UART_TX
UART_RX
11 TBTA_LSTX
11 TBTA_LSRX
LSX_R2P
LSX_P2R
TBTA_ACE_GPIO0
GPIO0
GPIO1
11 TBTA_USB2_D_P
11 TBTA_USB2_D_N
USB_RP_P
USB_RP_N
DEBUG1
DEBUG2
DEBUG3
DEBUG4
11 TBTA_DPSRC_AUX_P
11 TBTA_DPSRC_AUX_N
AUX_P
AUX_N
TPS65982
BUSPOWERZ
GPIO2
RESETZ
MRESET
GPIO8
GPIO7
GPIO6
GPIO5
GPIO4
GPIO3
R_OSC
R1310 15KOhm 0.1%
SENSEP
SENSEN
HV_GATE1
HV_GATE2
VBUS_1
VBUS_2
VBUS_3
VBUS_4
RPD_G1
C_CC1
C_CC2
RPD_G2
LDO_BMC
C_USB_TN
C_USB_TP
C_USB_BP
C_USB_BN
C_SBU2
C_SBU1
GND_1
GND_2
GND_4
GND_3
GND_5
GND_6
GND_7
GND_8
GND_9
GND_10
GND_11
GND_12
GND_13
GND_14
GND_15
GND_16
GND_17
GND_18
GND_19
GND_20
GND_21
GND_22
+VBUS_CONN
4.5~22V
3A
C1311 0.1UF/25V
C1312 1UF/25V
C1310 4.7uF/25V
R1300 0Ohm
R1313 0Ohm
R1301 0Ohm
R1302 0Ohm
C_CC1_CON 14
C_CC2_CON 14
C_USB_TN_R
C_USB_TP_R
C_USB_BP_R
C_USB_BN_R
SBU2_R
SBU1_R
R1320
R1319
R1322
R1321
R1312
R1311
NB_R0402_5MIL_SMALL
C_USB_TN 14
C_USB_TP 14
C_USB_BP 14
C_USB_BN 14
SBU2 14
SBU1 14
C1319 2.2UF/16V
C1320 220PF/50V
C1321 220PF/50V
C1313 0.22UF/10V
+3V3_FLASH
R1324 10KOhm
R1325 10KOhm
DEBUG_CTL1
DEBUG_CTL2
R1341 10KOhm
R1342 10KOhm
I2C Address Resistance
TPS65982 Device | External Resistance (1%) | I2C Unique Address [3:1]
Master 0 | 0 | 0x00
Slave 1 | 93.1k | 0x01
Slave 2 | 156k | 0x02
Slave 3 | 220k | 0x03
Slave 4 | 280k | 0x04
Slave 5 | 340k | 0x05
Slave 6 | 402k | 0x06
Slave 7 | Open | 0x0F
+3V3_FLASH
+3VSUS_TYPEC
TBTA_DPSRC_AUX_N
TBTA_DPSRC_AUX_P
R1336 100KOhm
R1337 100KOhm
TBTA_ACE_GPIO0
TBTA_ACE_GPIO7
R1314 10KOhm
R1315 10KOhm
ACE_I2C_SCL
ACE_I2C_SDA
ACE_I2C_IRQ
R1316 3.3KOhm
R1327 3.3KOhm
R1328 10KOhm
DEBUG1
DEBUG2
DEBUG3
DEBUG4
R1317 100KOhm
R1329 100KOhm
R1330 100KOhm
R1331 100KOhm
TBTA_MRESET
TBTA_ACE_GPIO8
R1332 100KOhm
R1333 10KOhm
UART_TX
UART serial transmit data. Connect pin to another TPS65982 UART_TX to share firmware. Connect UART_RX to UART_TX when not connected to another TPS65982.
DEBUG1/2/3/4
Ground pin with between 1kΩ and 5MΩ resistance when unused.
GPIO Pin Mapping
Pin | Type | Function
GPIO0 | I/O | Configured as Digital Cross-bar I/O or Unused
GPIO1 | I/O | Configured as Digital Cross-bar I/O or Unused
GPIO2 | In | Output power enable. Turns on VOUT 3V3.
GPIO3 | In | Output power enable. Turns on VOUT 3V3.
GPIO4 | I/O | Configured as HPD_RX or HPD_TX when DP Mode supported.
GPIO5 | Out | Configured as HPD_RX or Unused when DP Mode supported.
GPIO6 | Out | 5V Supply Enable (Driven High or High-Z, never Low)
GPIO7 | Out(OD) | System WAKE# Signal (Open Drain, wire-ORed to all Aces)
GPIO8 | Out(OD) | Power Output FAULT# Indicator Signal (Open Drain). Indicates a fault has occurred in supervisory circuits (OV, OVP, UVP, TSD).
+3V3_FLASH
+3VSUS_TYPEC
+LDO_1V8D_TBT
R1334 0Ohm
R1323 1KOhm
R1335 0Ohm
T1301
T1302
TBTA_ACE_GPIO2
TBTA_MRESET
TBTA_ACE_GPIO7
TBTA_ACE_GPIO8
TBTA_ACE_GPIO3
C1326 0.1UF/16V
11 TBT_RESET_N
11 TBTA_HPD
U1302
SN74AUP1G04DCKR
06V030000022
25,30,32,51,53,62 PLT_RST#_BUF
30 TBTA_MRESET_EC
R1338 N/A 0Ohm
28,30,50,60 SMB1_CLK
28,30,50,60 SMB1_DAT
Q1301A UM6K1N
Q1301B UM6K1N
ACE_I2C_SCL
ACE_I2C_SDA
Q1302A UM6K1N
Q1302B UM6K1N
30 ACE_I2C_IRQ_EC
ACE_I2C_IRQ
PEGATRON
Title : CC_Logic_TPS65982
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1/HW2
Engineer: Dep.3/Sec.3
Size C
Project Name P3HCJ
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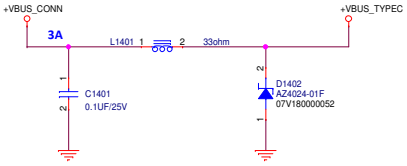
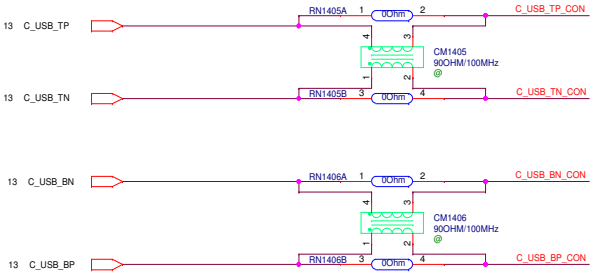
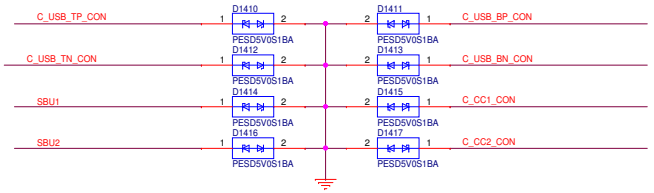
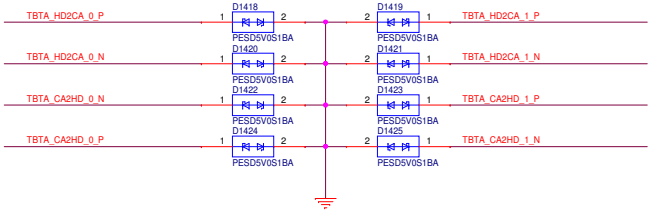
Date: Thursday, September 03, 2015
Sheet 13 of 100

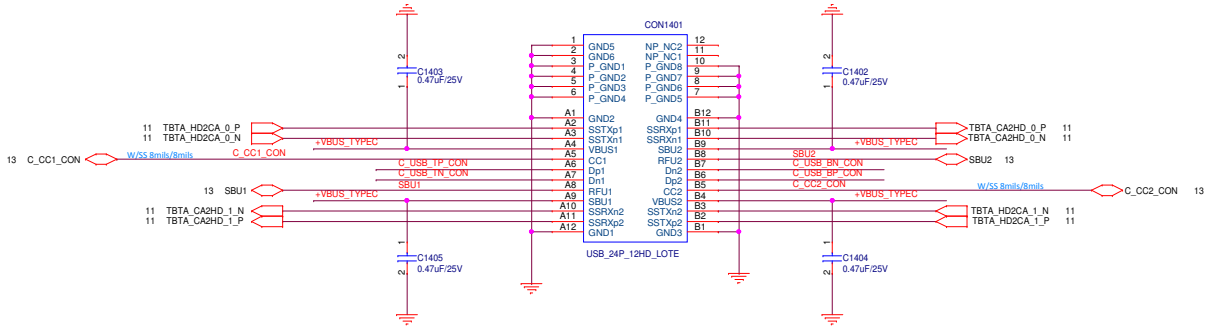


A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1-	Vbus	CC1	D+	D-	SBU1	Vbus	RX2-	RX2+	GND
GND	RX1+	RX1-	Vbus	SBU2	D-	D+	CC2	Vbus	TX2-	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1









PEGATRON Title : USB Type_C
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1/HW2 Engineer: Dep.3/Sec.3

Size	Project Name	Rev
C	P3HCJ	2.0

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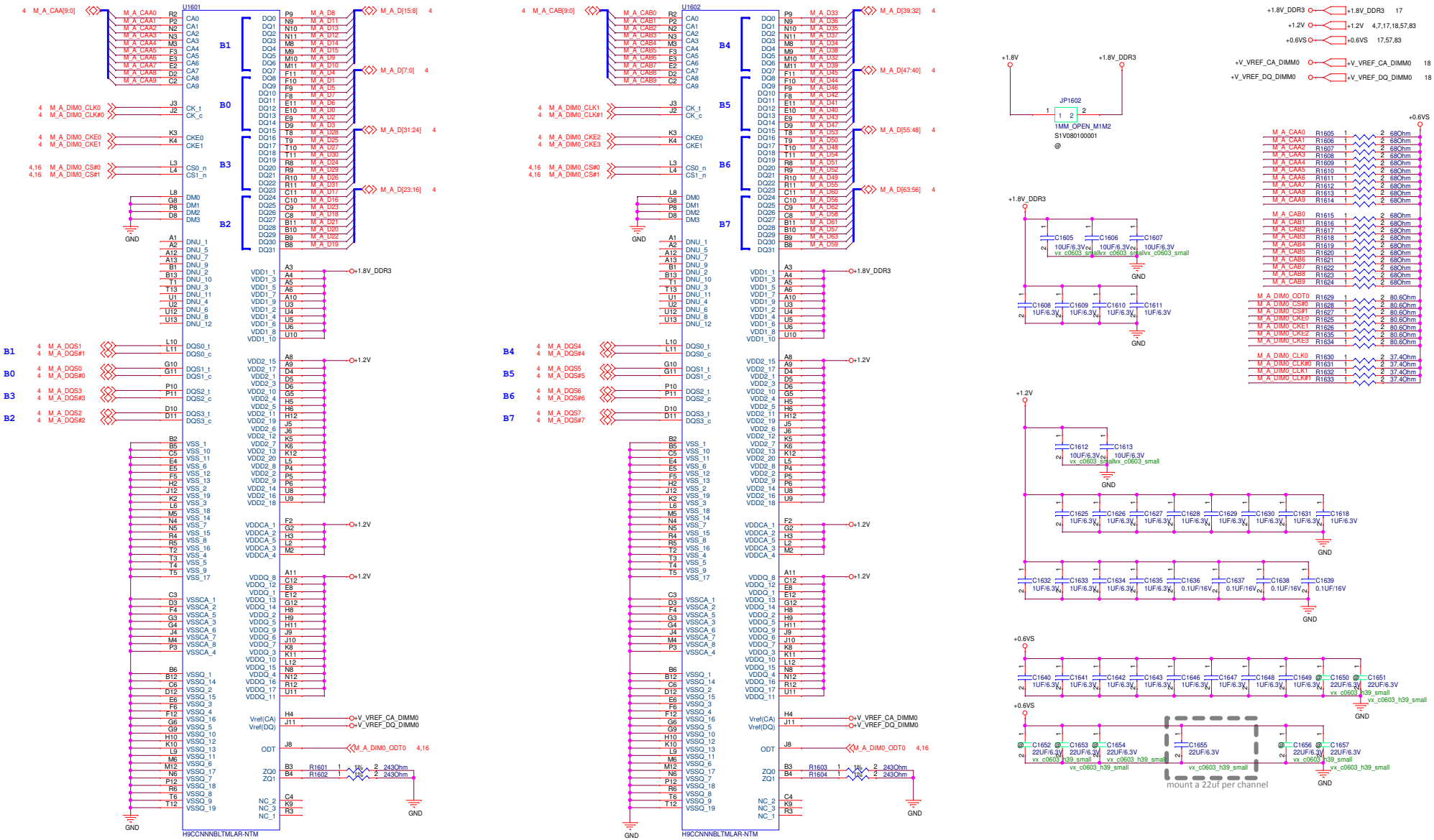
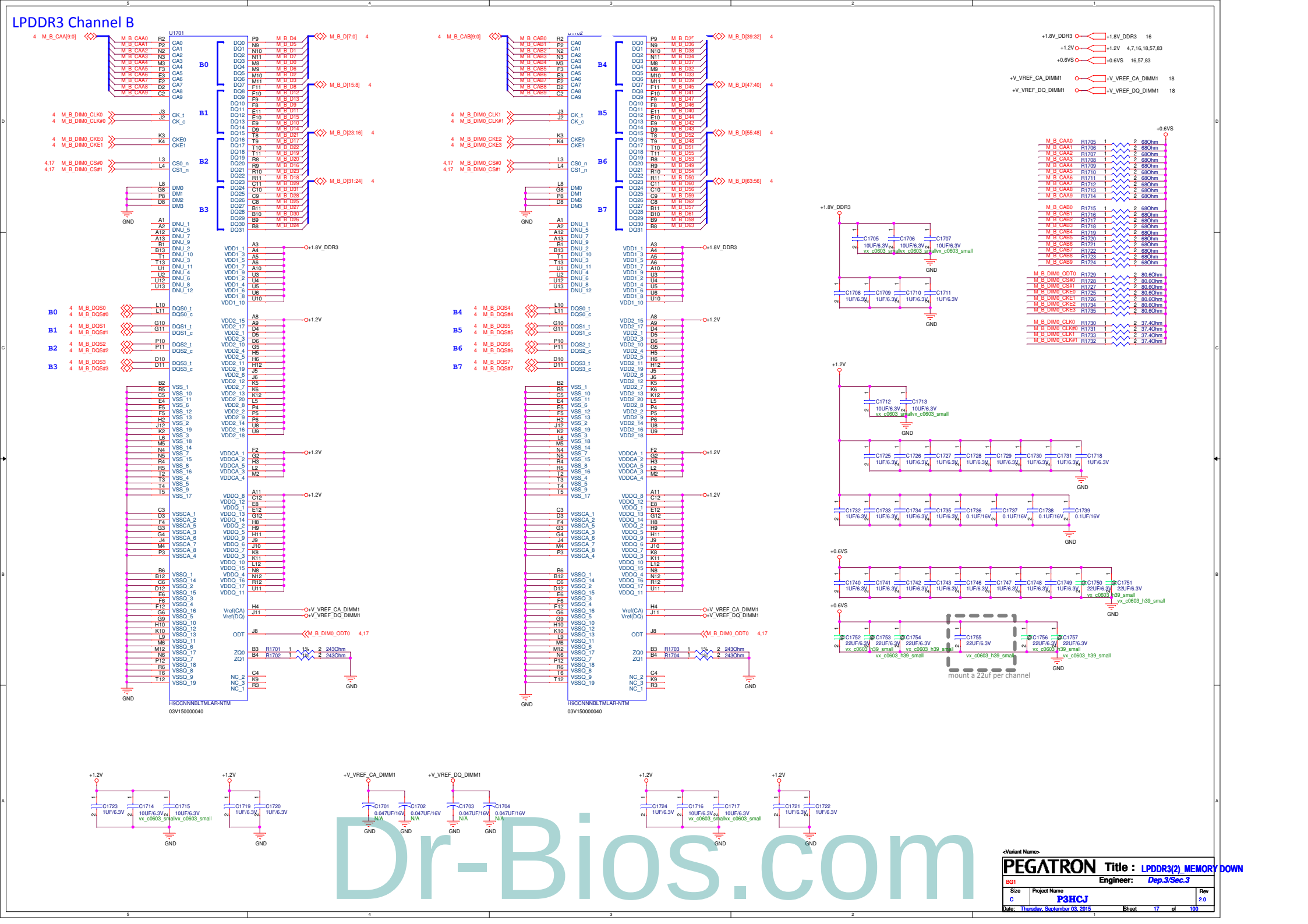
LPDDR3 Channel A



LPDDR3 Channel B



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PEGATRON Title : LPDDR3(2)_MEMORY DOWN

BG1 Engineer: Dep.3/Sec.3

Size	Project Name	Rev
C	P3HCJ	2.0

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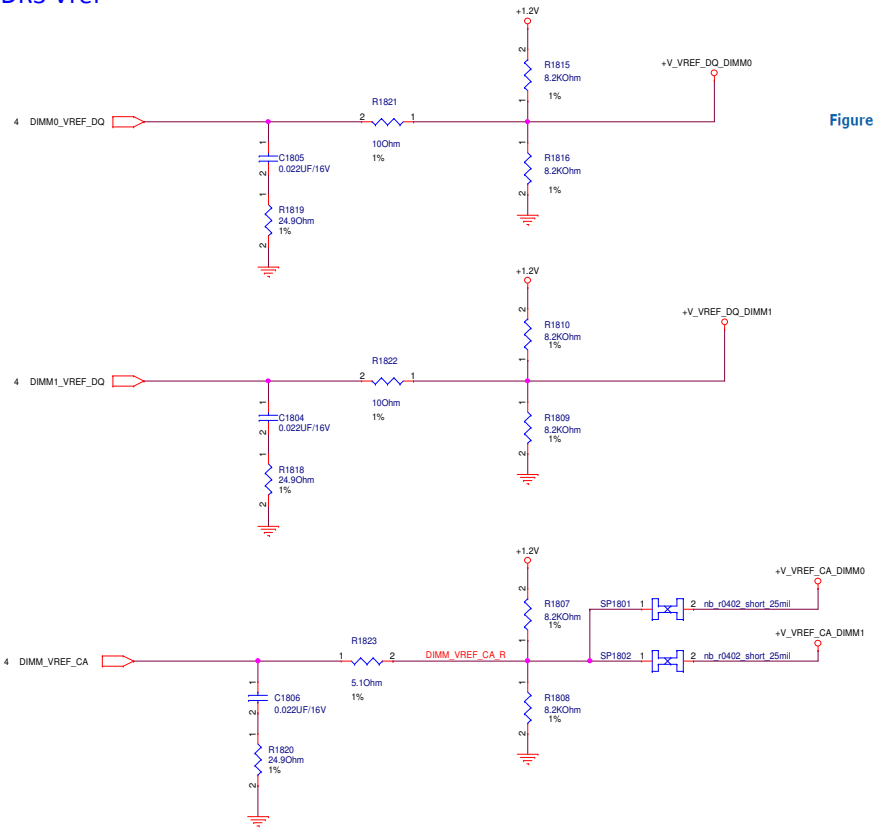
LPDDR3 Vref



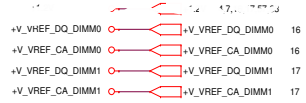
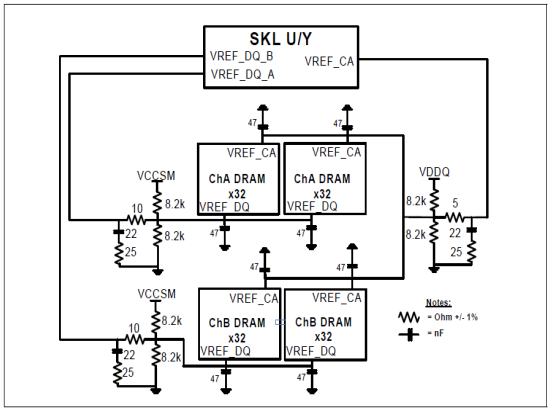
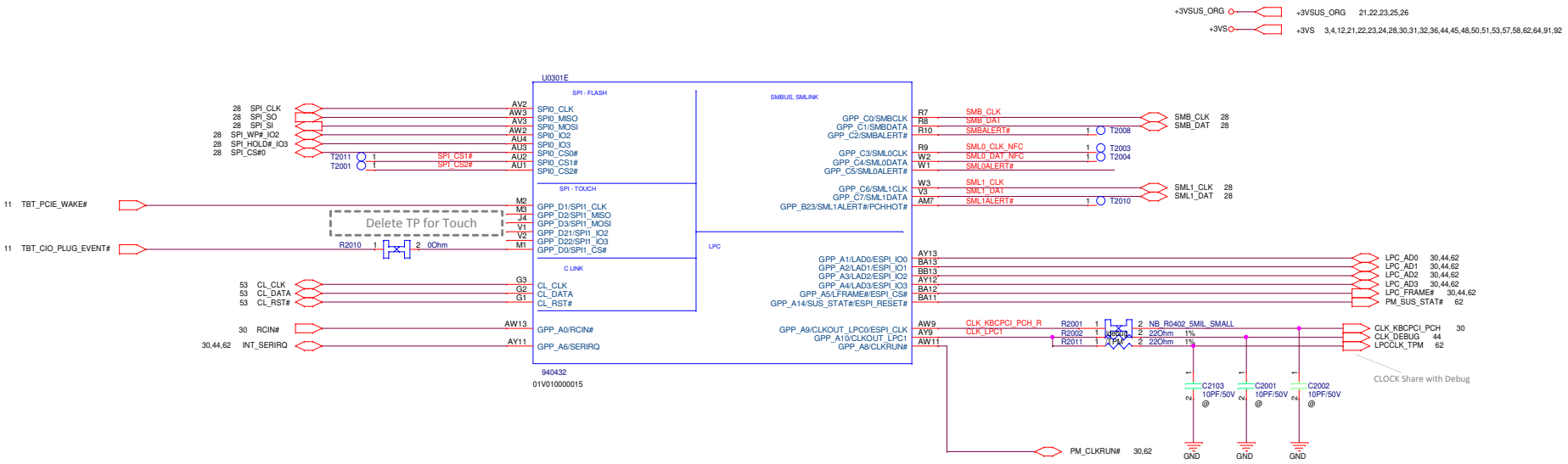


Figure 4-46. SKL U and SKL Y LPDDR3 x32 Memory Down V_{REF-DQ} and V_{REF-CA} Overview

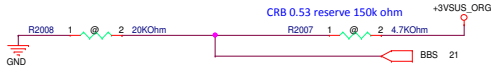


PEGATRON	Title : LPDDR3(3)_CA/DQ		
BG1	Engineer: Dep.3/Sec.3		
Size: C	Project Name: P3HCJ		Rev: 2.0
Date: Thursday, September 03, 2015	Sheet 18 of 100		

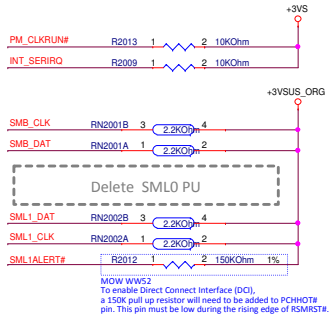


SMBALERT# - Internal weak pull down 20k ohm
TLS Confidentiality
0 : Disable (default)
1 : Enable

SML0ALERT# - Internal weak pull down 20 kohm
0 : LPC EC (default)
1 : eSPI EC



BBS - Internal weak pull down 20k ohm
Boot BIOS Strap
0 : SPI destination (default)
1 : LPC destination



PEGATRON Title : PCH(1)_SPI/LPC
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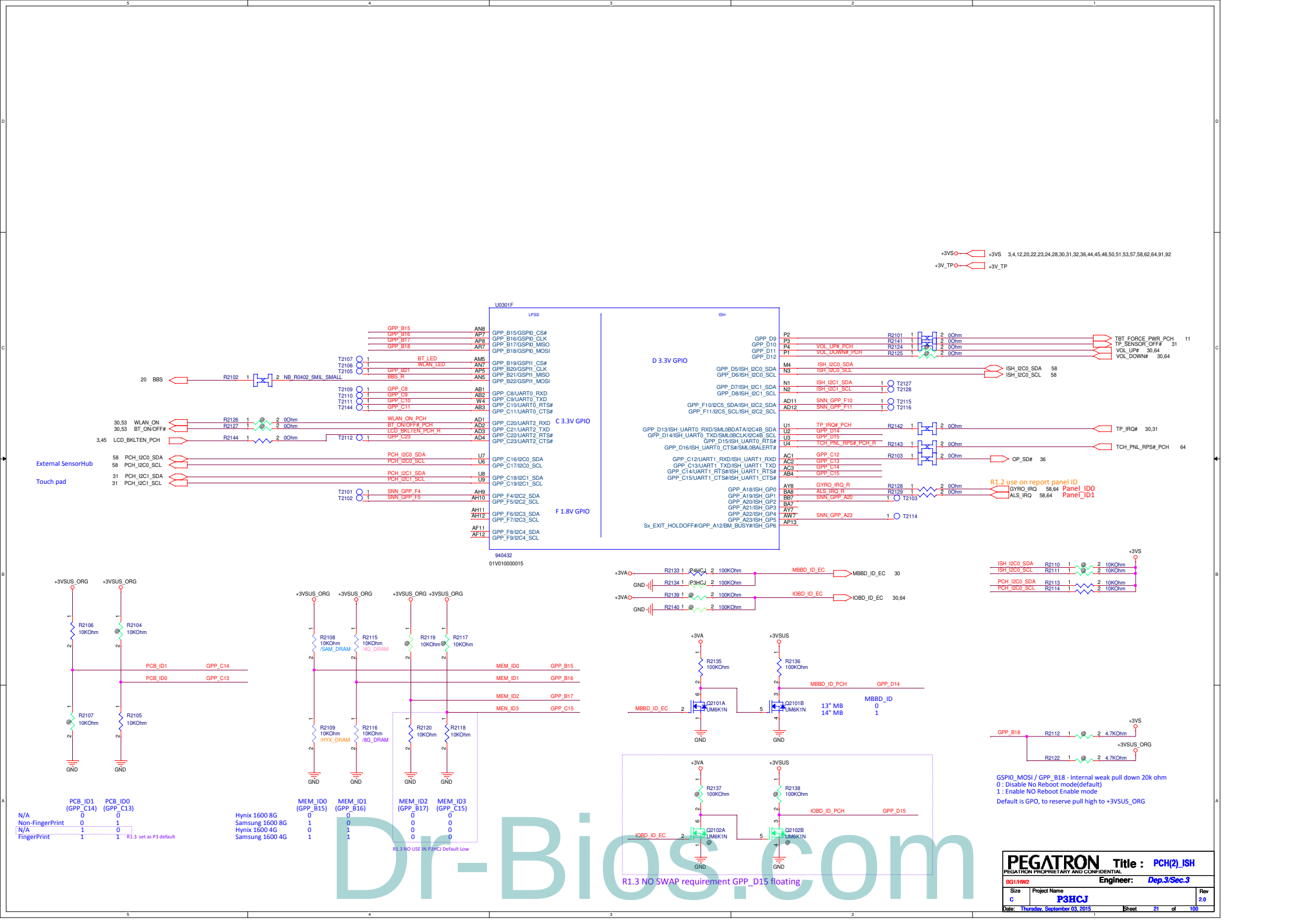
BG1/HW2 Engineer: Dep.3/Sec.3
Size C | Project Name P3HCJ | Rev 2.0
Date: Thursday, September 03, 2015 | Sheet 20 of 100


+3VS
+3VS 3,4,12,20,22,23,24,28,30,31,32,36,44,45,48,50,51,53,57,58,62,64,91,92
+3V_TP
+3V_TP
U0301F
LPSS
ISH
D 3.3V GPIO
C 3.3V GPIO
F 1.8V GPIO
GPP_B15/GSPI0_CS#
GPP_B16/GSPI0_CLK
GPP_B17/GSPI0_MISO
GPP_B18/GSPI0_MOSI
GPP_B19/GSPI1_CS#
GPP_B20/GSPI1_CLK
GPP_B21/GSPI1_MISO
GPP_B22/GSPI1_MOSI
GPP_C8/UART0_RXD
GPP_C9/UART0_TXD
GPP_C10/UART0_RTS#
GPP_C11/UART0_CTS#
GPP_C20/UART2_RXD
GPP_C21/UART2_TXD
GPP_C22/UART2_RTS#
GPP_C23/UART2_CTS#
GPP_C16/I2C0_SDA
GPP_C17/I2C0_SCL
GPP_C18/I2C1_SDA
GPP_C19/I2C1_SCL
GPP_F4/I2C2_SDA
GPP_F5/I2C2_SCL
GPP_F6/I2C3_SDA
GPP_F7/I2C3_SCL
GPP_F8/I2C4_SDA
GPP_F9/I2C4_SCL
940432
01V010000015
20 BBS
R2102 2 NB_R0402_5MIL_SMALL
T2107 BT_LED
T2106 WLAN_LED
T2105 GPP_B21 BBS_R
T2109 GPP_C8
T2110 GPP_C9
T2111 GPP_C10
T2144 GPP_C11
30,53 WLAN_ON
30,53 BT_ON/OFF#
R2126 0Ohm
R2127 0Ohm
WLAN_ON_PCH
BT_ON/OFF#_PCH
LCD_BKLTEN_PCH_R
3,45 LCD_BKLTEN_PCH
R2144 0Ohm
T2112 GPP_C23
External SensorHub
58 PCH_I2C0_SDA
58 PCH_I2C0_SCL
PCH_I2C0_SDA
PCH_I2C0_SCL
Touch pad
31 PCH_I2C1_SDA
31 PCH_I2C1_SCL
PCH_I2C1_SDA
PCH_I2C1_SCL
T2101 SNN_GPP_F4
T2102 SNN_GPP_F5
GPP_D9
GPP_D10
GPP_D11
GPP_D12
VOL_UP#_PCH
VOL_DOWN#_PCH
R2101 0Ohm
R2124 0Ohm
R2125 0Ohm
TBT_FORCE_PWR_PCH 11
TP_SENSOR_OFF# 31
VOL_UP# 30,64
VOL_DOWN# 30,64
GPP_D5/ISH_I2C0_SDA
GPP_D6/ISH_I2C0_SCL
ISH_I2C0_SDA
ISH_I2C0_SCL
ISH_I2C0_SDA 58
ISH_I2C0_SCL 58
GPP_D7/ISH_I2C1_SDA
GPP_D8/ISH_I2C1_SCL
ISH_I2C1_SDA
ISH_I2C1_SCL
T2127
T2128
GPP_F10/I2C5_SDA/ISH_I2C2_SDA
GPP_F11/I2C5_SCL/ISH_I2C2_SCL
SNN_GPP_F10
SNN_GPP_F11
T2115
T2116
GPP_D13/ISH_UART0_RXD/SML0BDATA/I2C4B_SDA
GPP_D14/ISH_UART0_TXD/SML0BCLK/I2C4B_SCL
GPP_D15/ISH_UART0_RTS#
GPP_D16/ISH_UART0_CTS#/SML0BALERT#
TP_IRQ#_PCH
GPP_D14
GPP_D15
TCH_PNL_RPS#_PCH_R
R2142 0Ohm
R2143 0Ohm
TP_IRQ# 30,31
TCH_PNL_RPS#_PCH 64
GPP_C12/UART1_RXD/ISH_UART1_RXD
GPP_C13/UART1_TXD/ISH_UART1_TXD
GPP_C14/UART1_RTS#/ISH_UART1_RTS#
GPP_C15/UART1_CTS#/ISH_UART1_CTS#
GPP_C12
GPP_C13
GPP_C14
GPP_C15
R2103 0Ohm
OP_SD# 36
R1.2 use on report panel ID
GPP_A18/ISH_GP0
GPP_A19/ISH_GP1
GPP_A20/ISH_GP2
GPP_A21/ISH_GP3
GPP_A22/ISH_GP4
GPP_A23/ISH_GP5
Sx_EXIT_HOLDOFF#/GPP_A12/BM_BUSY#/ISH_GP6
GYRO_IRQ_R
ALS_IRQ_R
SNN_GPP_A20
SNN_GPP_A23
R2128 0Ohm
R2129 0Ohm
T2103
T2114
GYRO_IRQ 58,64 Panel_ID0
ALS_IRQ 58,64 Panel_ID1
+3VSUS_ORG
R2106 10KOhm
R2104 10KOhm
R2107 10KOhm
R2105 10KOhm
PCB_ID1 GPP_C14
PCB_ID0 GPP_C13
GND
R2108 10KOhm /SAM_DRAM
R2115 10KOhm /4G_DRAM
R2109 10KOhm /HYX_DRAM
R2116 10KOhm /8G_DRAM
R2119 10KOhm
R2117 10KOhm
R2120 10KOhm
R2118 10KOhm
MEM_ID0 GPP_B15
MEM_ID1 GPP_B16
MEM_ID2 GPP_B17
MEN_ID3 GPP_C15
+3VA
R2133 P4HCJ 2 100KOhm
R2134 P3HCJ 2 100KOhm
R2139 2 100KOhm
R2140 2 100KOhm
MBBD_ID_EC
IOBD_ID_EC
MBBD_ID_EC 30
IOBD_ID_EC 30,64
+3VSUS
R2135 100KOhm
R2136 100KOhm
Q2101A UM6K1N
Q2101B UM6K1N
MBBD_ID_PCH
MBBD_ID
13" MB 0
14" MB 1
R2137 100KOhm
R2138 100KOhm
Q2102A UM6K1N
Q2102B UM6K1N
IOBD_ID_PCH
R1.3 NO SWAP requirement GPP_D15 floating
ISH_I2C0_SDA R2110 2 10KOhm
ISH_I2C0_SCL R2111 2 10KOhm
PCH_I2C0_SDA R2113 2 10KOhm
PCH_I2C0_SCL R2114 2 10KOhm
GPP_B18
R2112 4.7KOhm
R2122 4.7KOhm
GSPI0_MOSI / GPP_B18 - Internal weak pull down 20k ohm
0 : Disable No Reboot mode(default)
1 : Enable NO Reboot Enable mode
Default is GPO, to reserve pull high to +3VSUS_ORG
PCB_ID1 (GPP_C14) PCB_ID0 (GPP_C13)
N/A 0 0
Non-FingerPrint 0 1
N/A 1 0
FingerPrint 1 1 R1.3 set as P3 default
MEM_ID0 (GPP_B15) MEM_ID1 (GPP_B16) MEM_ID2 (GPP_B17) MEM_ID3 (GPP_C15)
Hynix 1600 8G 0 0 0 0
Samsung 1600 8G 1 0 0 0
Hynix 1600 4G 0 1 0 0
Samsung 1600 4G 1 1 0 0
R1.3 NO USE IN P3HCJ Default Low
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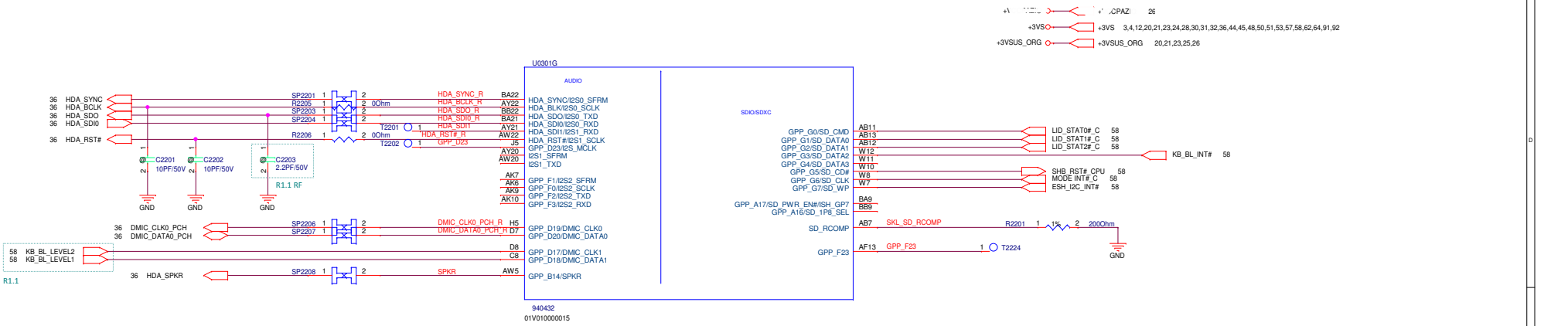
Title : PCH(2)_ISH
Engineer: Dep.3/Sec.3
BG1/HW2
Size C
Project Name P3HCJ
Rev 2.0
Date: Thursday, September 03, 2015
Sheet 21 of 100



PEGATRON Title : PCH(3)_HDA/SDIO

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BG1/HW2 Engineer: Dep.3/Sec.3

Size	Project Name	Rev
C	P3HCJ	2.0

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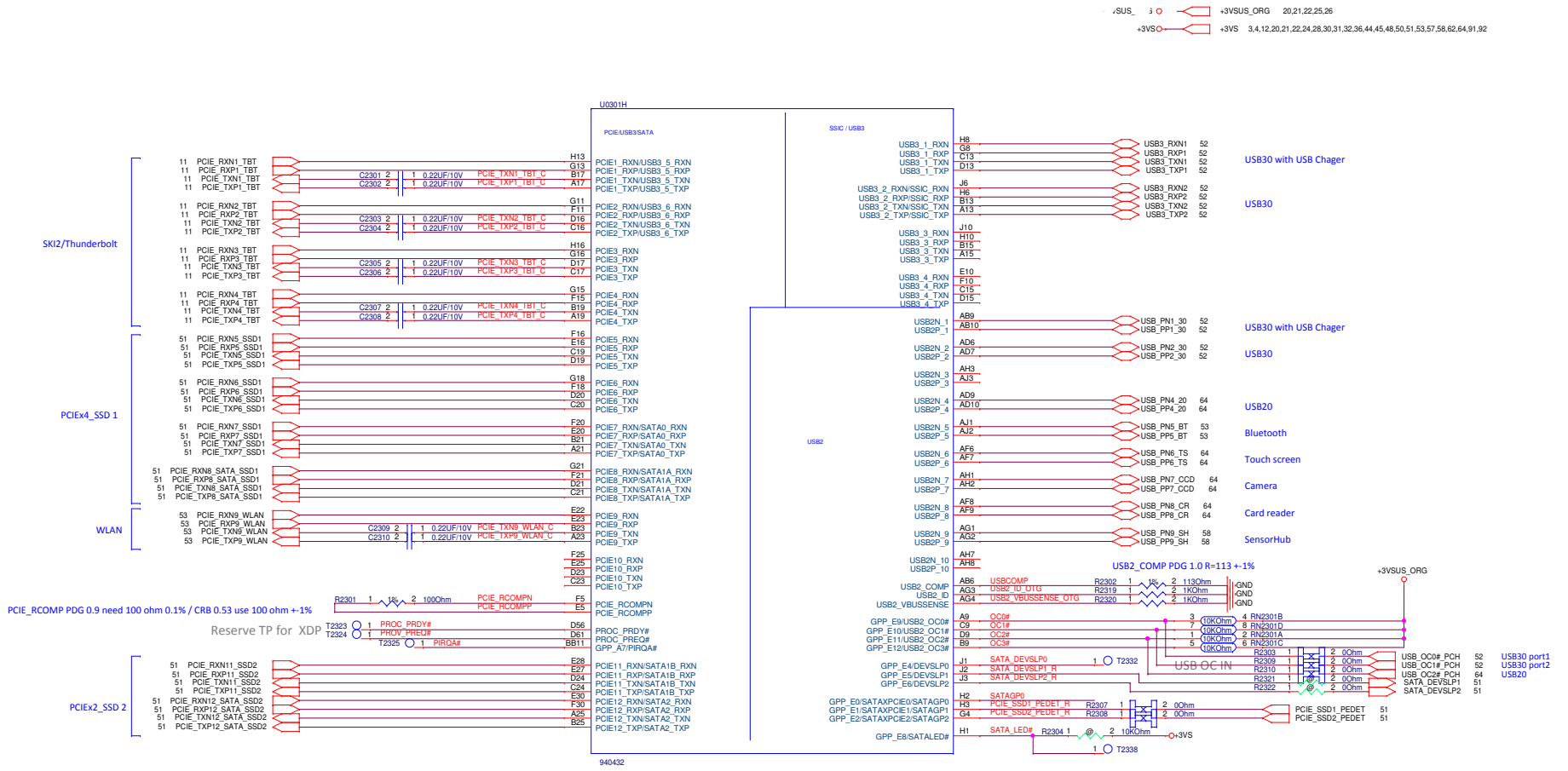


Table 1-2. PCH-LP SKUs (Sheet 2 of 2)

Features	Base-U	Premium-U	Premium-Y
Total Intel® RST capable PCIe and SATA Express[4] Storage Devices	0	2	2

Notes:
1. USB 2.0 port numbers: 1-8
2. USB 2.0 port numbers: 1-10
3. USB 2.0 port numbers: 1-6
4. SATA Express Capable Ports (x2)

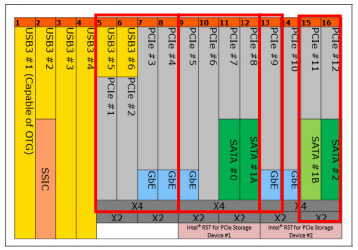
Table 1-3. PCH-LP HSIO Detail

SKU	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Base-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe	PCIe	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	SATA	SATA	PCIe/ LAN	PCIe/ LAN	N/A	N/A
Premium-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe/ USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe/ SATA	PCIe/ SATA	PCIe/ LAN	PCIe/ LAN	PCIe/ SATA	PCIe/ SATA
Premium-Y	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe/ USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe/ SATA	PCIe/ SATA	PCIe/ LAN	PCIe/ LAN	N/A	N/A

Capture from 545659_545659_SKL_PCH_LP_EDS_Rev1_0_pub
Please refer the latest Doc.

3.4.1 SKL PCH U Flexible I/O

Figure 3-1. HSIO Muxing on SKL PCH U



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Title: PCH(4)_USB/PCIE/SATA
Engineer: Dep.3/Sec.3
BG1/HW2
Size: C | Project Name: P3HCJ | Rev: 2.0
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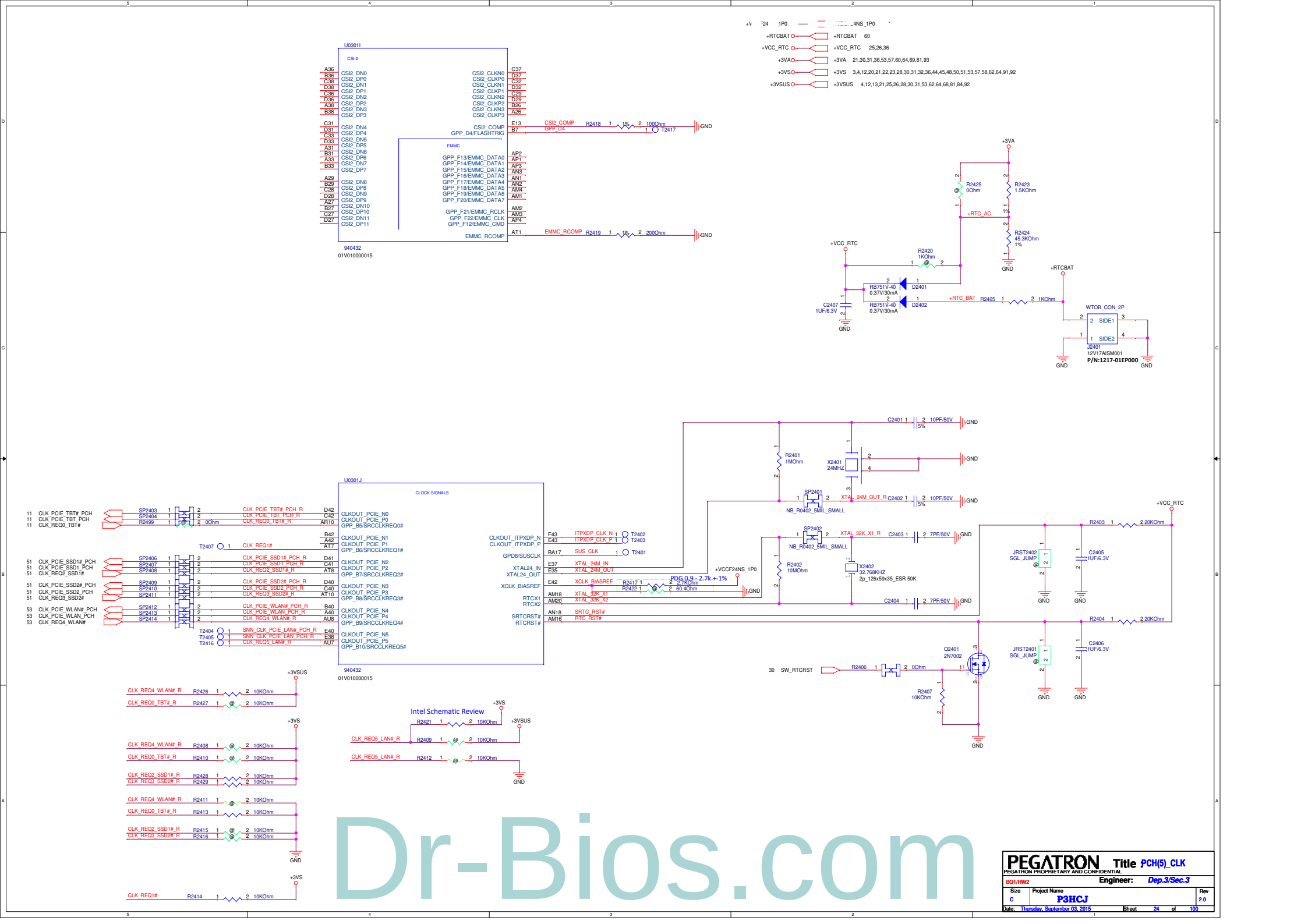
+V 24 1P0
+RTCBAT +RTCBAT 60
+VCC_RTC +VCC_RTC 25,26,36
+3VA +3VA 21,30,31,36,53,57,60,64,69,81,93
+3VS +3VS 3,4,12,20,21,22,23,28,30,31,32,36,44,45,48,50,51,53,57,58,62,64,91,92
+3VSUS +3VSUS 4,12,13,21,25,26,28,30,31,53,62,64,68,81,84,92
U0301I
CSI-2
CSI2_DN0 CSI2_DP0 CSI2_DN1 CSI2_DP1 CSI2_DN2 CSI2_DP2 CSI2_DN3 CSI2_DP3
CSI2_DN4 CSI2_DP4 CSI2_DN5 CSI2_DP5 CSI2_DN6 CSI2_DP6 CSI2_DN7 CSI2_DP7
CSI2_DN8 CSI2_DP8 CSI2_DN9 CSI2_DP9 CSI2_DN10 CSI2_DP10 CSI2_DN11 CSI2_DP11
CSI2_CLKN0 CSI2_CLKP0 CSI2_CLKN1 CSI2_CLKP1 CSI2_CLKN2 CSI2_CLKP2 CSI2_CLKN3 CSI2_CLKP3
CSI2_COMP
GPP_D4/FLASHTRIG
EMMC
GPP_F13/EMMC_DATA0 GPP_F14/EMMC_DATA1 GPP_F15/EMMC_DATA2 GPP_F16/EMMC_DATA3 GPP_F17/EMMC_DATA4 GPP_F18/EMMC_DATA5 GPP_F19/EMMC_DATA6 GPP_F20/EMMC_DATA7
GPP_F21/EMMC_RCLK GPP_F22/EMMC_CLK GPP_F12/EMMC_CMD
EMMC_RCOMP
CSI2_COMP R2418 1 2 100Ohm 1% T2417 GND
GPP_D4 R2418
EMMC_RCOMP R2419 1 2 200Ohm 1% GND
940432
01V010000015
+3VA
R2425 0Ohm
R2423 1.5KOhm 1%
+RTC_AC
R2424 45.3KOhm 1%
GND
+VCC_RTC
R2420 1KOhm
RB751V-40 0.37V/30mA D2401
RB751V-40 0.37V/30mA D2402
C2407 1UF/6.3V
+RTCBAT
+RTC_BAT R2405 1KOhm
WTOB_CON_2P
SIDE1 SIDE2
J2401
12V17AISM001
P/N:1217-01EP000
U0301J
CLOCK SIGNALS
CLKOUT_PCIE_N0 CLKOUT_PCIE_P0 GPP_B5/SRCCLKREQ0#
CLKOUT_PCIE_N1 CLKOUT_PCIE_P1 GPP_B6/SRCCLKREQ1#
CLKOUT_PCIE_N2 CLKOUT_PCIE_P2 GPP_B7/SRCCLKREQ2#
CLKOUT_PCIE_N3 CLKOUT_PCIE_P3 GPP_B8/SRCCLKREQ3#
CLKOUT_PCIE_N4 CLKOUT_PCIE_P4 GPP_B9/SRCCLKREQ4#
CLKOUT_PCIE_N5 CLKOUT_PCIE_P5 GPP_B10/SRCCLKREQ5#
CLKOUT_ITPXDP_N CLKOUT_ITPXDP_P
GPD8/SUSCLK
XTAL24_IN XTAL24_OUT
XCLK_BIASREF
RTCX1 RTCX2
SRTCRST# RTCRST#
940432
01V010000015
CLK_PCIE_TBT# CLK_PCIE_TBT_PCH CLK_REQ0_TBT#
SP2403 SP2404 R2499 0Ohm
CLK_PCIE_TBT#_PCH_R CLK_PCIE_TBT_PCH_R CLK_REQ0_TBT#_R
T2407 CLK_REQ1#
CLK_PCIE_SSD1# CLK_PCIE_SSD1_PCH CLK_REQ2_SSD1#
SP2406 SP2407 SP2408
CLK_PCIE_SSD1#_PCH_R CLK_PCIE_SSD1_PCH_R CLK_REQ2_SSD1#_R
CLK_PCIE_SSD2# CLK_PCIE_SSD2_PCH CLK_REQ3_SSD2#
SP2409 SP2410 SP2411
CLK_PCIE_SSD2#_PCH_R CLK_PCIE_SSD2_PCH_R CLK_REQ3_SSD2#_R
CLK_PCIE_WLAN#_PCH CLK_PCIE_WLAN_PCH CLK_REQ4_WLAN#
SP2412 SP2413 SP2414
CLK_PCIE_WLAN#_PCH_R CLK_PCIE_WLAN_PCH_R CLK_REQ4_WLAN#_R
T2404 T2405 T2416
SNN_CLK_PCIE_LAN#_PCH_R SNN_CLK_PCIE_LAN_PCH_R CLK_REQ5_LAN#_R
ITPXDP_CLK_N T2402 ITPXDP_CLK_P T2403
SUS_CLK T2401
XTAL_24M_IN XTAL_24M_OUT
XCLK_BIASREF R2417 2.7KOhm 1% R2422 60.4Ohm 1%
PDG 0.9 - 2.7k +-1%
+VCCF24NS_1P0
XTAL_32K_X1 XTAL_32K_X2
SRTC_RST# RTC_RST#
C2401 10PF/50V 5%
R2401 1MOhm
X2401 24MHZ
SP2401 NB_R0402_5MIL_SMALL
XTAL_24M_OUT_R C2402 10PF/50V 5%
SP2402 NB_R0402_5MIL_SMALL
XTAL_32K_X1_R C2403 7PF/50V
R2402 10MOhm
X2402 32.768KHZ 2p_126x59x35_ESR 50K
C2404 7PF/50V
+VCC_RTC
R2403 20KOhm
R2404 20KOhm
JRST2402 SGL_JUMP
JRST2401 SGL_JUMP
C2405 1UF/6.3V
C2406 1UF/6.3V
Q2401 2N7002
30 SW_RTCRST
R2406 0Ohm
R2407 10KOhm
+3VSUS
CLK_REQ4_WLAN#_R R2426 10KOhm
CLK_REQ0_TBT#_R R2427 10KOhm
+3VS
CLK_REQ4_WLAN#_R R2408 10KOhm
CLK_REQ0_TBT#_R R2410 10KOhm
CLK_REQ2_SSD1#_R R2428 10KOhm
CLK_REQ3_SSD2#_R R2429 10KOhm
CLK_REQ4_WLAN#_R R2411 10KOhm
CLK_REQ0_TBT#_R R2413 10KOhm
CLK_REQ2_SSD1#_R R2415 10KOhm
CLK_REQ3_SSD2#_R R2416 10KOhm
GND
CLK_REQ1# R2414 10KOhm
Intel Schematic Review
R2421 10KOhm
CLK_REQ5_LAN#_R R2409 10KOhm
CLK_REQ5_LAN#_R R2412 10KOhm
PEGATRON
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Title PCH(5)_CLK
Engineer: Dep.3/Sec.3
BG1/HW2
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+3VSUS_ORG +3VSUS_ORG 20,21,22,23,26
+VCC_RTC +VCC_RTC 24,26,36
+VCCDSW +VCCDSW 26,30
+VCCST_CPU +VCCST_CPU 3,5,7,9,32
+3V +3V 31,53,57,58,64,91
+3VSUS +3VSUS 4,12,13,21,24,26,28,30,31,53,62,64,68,81,84,92

+3VSUS_ORG
R2501 3KOhm 1%
U0301K
SYSTEM POWER MANAGEMENT
30 PM_RSMRST#
T2501 H_CPUPWRGD_TP
SP2501 R2503 1KOhm
PLT_RST# AN10
PM_SYS_RESET#_R B5
PM_RSMRST_R AY17
H_CPUPWRGD A68
H_VCCST_PWRGD_MCP B65
GPP_B13/PLTRST#
SYS_RESET#
RSMRST#
PROCPWRGD
VCCST_PWRGD
ALL_SYS_PWRGD delay 99 ms from EC 30,68 SYS_PWROK
R2504 R2505 R2506 0Ohm
PM_PWROK
PM_HSMRST_H
SYS_PWROK_R B6
PM_PCH_PWROK_R BA20
PCH_DPWROK BB20
SYS_PWROK
PCH_PWROK
DSW_PWROK
30 SUSWARN#/SUSPWRDNACK
DSW function / non-AMT
R2508 R2509 R2510 0Ohm
SUS_PWR_ACK_H
SUS_PWR_ACK_R AR13
SUSACK#_R AP11
GPP_A13/SUSWARN#/SUSPWRDNACK
GPP_A15/SUSACK#
30 SUSACK#
11,53 WAKE_PCIE#
LAN_WAKE# BB15
AM15
GPD11 AW17
GPD7 AT15
WAKE#
GPD2/LAN_WAKE#
GPD11/LANPHYPC
GPD7/RSVD
T2502
T2508
940432
01V010000015
GPP_B12/SLP_S0# AT11
GPD4/SLP_S3# AP15
GPD5/SLP_S4# BA16
GPD10/SLP_S5# AY16
SLP_S0#
SLP_S3#_R
SLP_S4#_R
GPD10
SP2502 SP2503
T2503 T2504
PM_SUSB# 11,30,68
PM_SUSC# 30,68
SLP_SUS# AN15
SLP_LAN# AW15
GPD9/SLP_WLAN# BB17
GPD6/SLP_A# AN16
SLP_SUS#
SLP_LAN#
SLP_WLAN#
ME_PM_SLP_M#_PCH
T2530 T2505 T2506 T2507
To EC
GPD3/PWRBTN# BA15
GPD1/ACPRESENT AY15
GPD0/BATLOW# AU13
AC_PRESENT_R R2532 0Ohm
BATLOW#
PM_PWRBTN# 30
ME_AC_PRESENT 30
+VCC_RTC
GPP_A11/PME# AU11
INTRUDER# AP16
PME#
SM_INTRUDER# R2513 1MOhm
GPP_B11/EXT_PWR_GATE# AM10
GPP_B2/VRALERT# AM11
MPHY_EXT_PWR_GATEB_R
VR_ALERT#
T2529

+3V
U2501
SN74LVC1G08DCKR
PLT_RST#
C2502 100PF/50V
R2515 0Ohm
GND
C2503 100PF/50V
R2516 10KOhm
PLT_RST#_BUF
11,13,30,32,51,53,62,25,30 DELAY_ALL_SYSTEM_PWRGD
25,30,92 ALL_SYSTEM_PWRGD
80,92 VRM_PWRGD
R2531 SP2506 SP2507 0Ohm
ALL_SYSTEM_PWRGD_PMOK
VR_READY_PMOK
+3VSUS
U2502
Vcc=2~5.5
R2517 0Ohm
PM_PWROK
R2519 10KOhm

+VCCDSW
BATLOW# R2522 10KOhm
LAN_WAKE# R2523 10KOhm
GPD7 R2524 10KOhm
WAKE_PCIE# R2525 1KOhm
AC_PRESENT_R R2526 10KOhm
+3VSUS_ORG
internal pull high
PME# R2527 10KOhm
Set to GPI
VR_ALERT# R2528 10KOhm

EC delay ALL_SYSTEM_PWRGD 2ms
25,30 DELAY_ALL_SYSTEM_PWRGD
25,30,92 ALL_SYSTEM_PWRGD
R2529 R2530 0Ohm
H_VCCST_PWRGD_L
U2503
74AUP1G07GW
06V030000021
+3VSUS
+VCCST_CPU
C2504 0.1UF/16V
R2520 1KOhm
H_VCCST_PWRGD_R
R2521 1% 60.4Ohm
H_VCCST_PWRGD_MCP
C2505 0.1UF/16V
+VDDQ/+VCCST_CPU/+VCCSTG to VCCST_PWRGD must > 1ms

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title: SCH(6)_POWER MANAGE
Engineer: Dep.3/Sec.3
BG1/HW2
Size C | Project Name P3HCJ | Rev 2.0
Date: Thursday, September 03, 2015 | Sheet 25 of 100

Table 10-5. SKL U / SKL Y PCH-LP VCCMPHY_1p0 Icc Adder Per HSIO Lane

Icc (A)	Details
0.064	All HSIO disabled.
0.154	Each PCIe Gen3 Lane
0.102	Each PCIe Gen2 Lane
0.132	Each USB3 Port
0.099	SSIC
0.044	GbE Port
0.132	Each SATA Gen3 Port

SATA Gen3 Port X 10
PCIe Gen2 Lane X 1
USB3 Port X 2
All HSIO disabled (basic comsunption)
=0.154x10+0.102+0.132x2+0.064 = 1.97A

Decoupling cap for internal power

1.97A

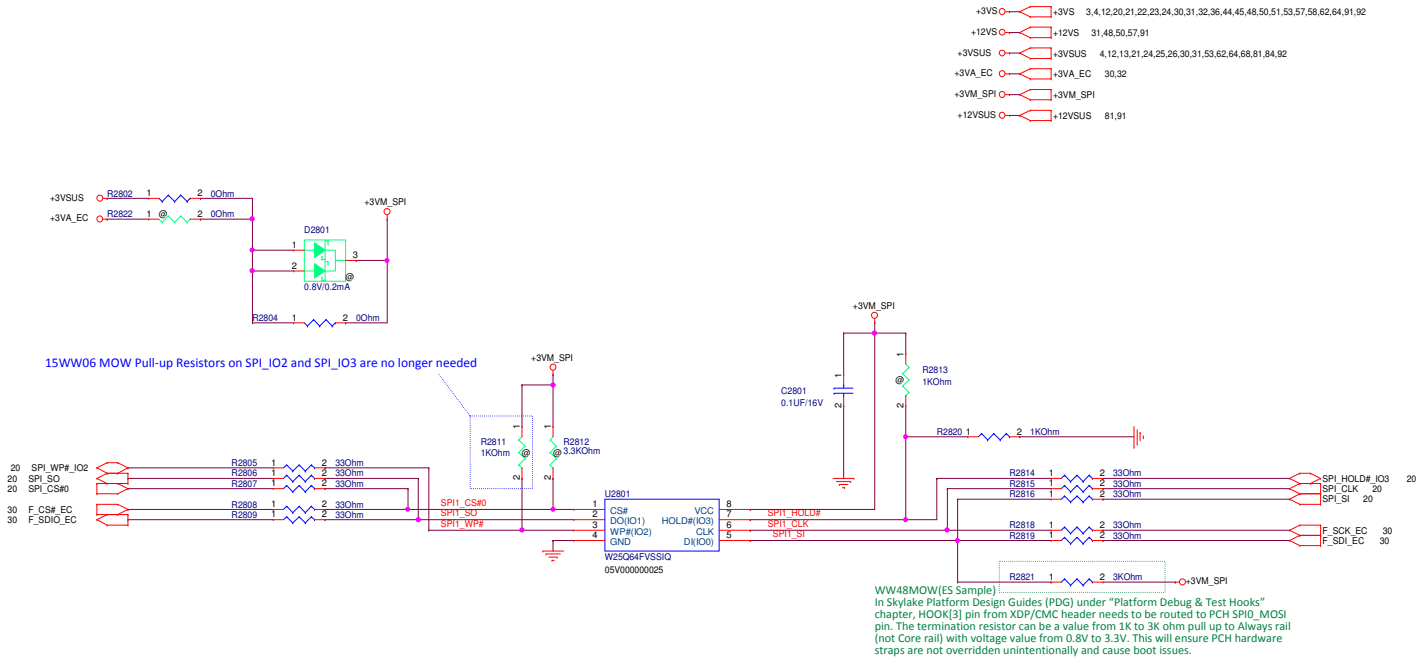
Intel confirm pull down 1k

+3VSUS_ORG/+1.8VSUS to +1.0VSUS >200us (tPCH06)

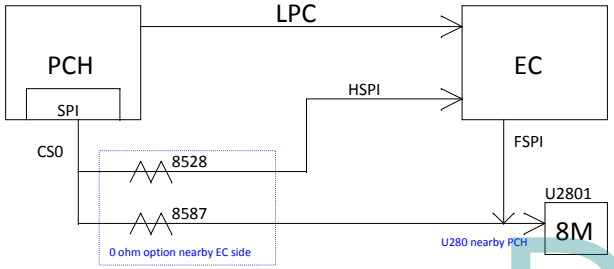
w/o DSW

if need choke, gate power should be disabled

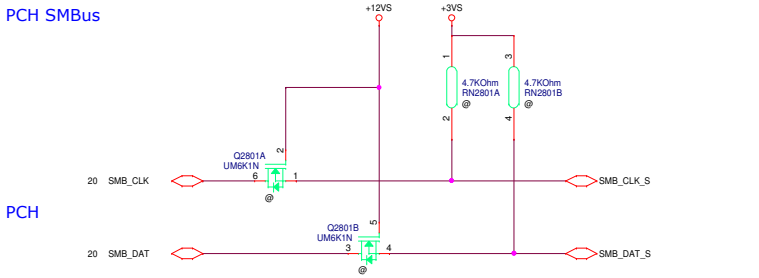
PEGATRON Title PCH(7)_POWER
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1/HW2 Engineer: Dep.3/Sec.3
Size C | Project Name P3HCJ | Rev 2.0
Date: Thursday, September 03, 2015 | Sheet 26 of 100

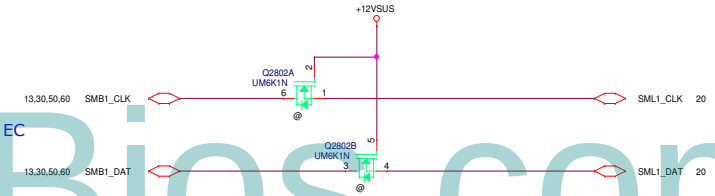


EC co-lay 8528/8587
SPI Structure

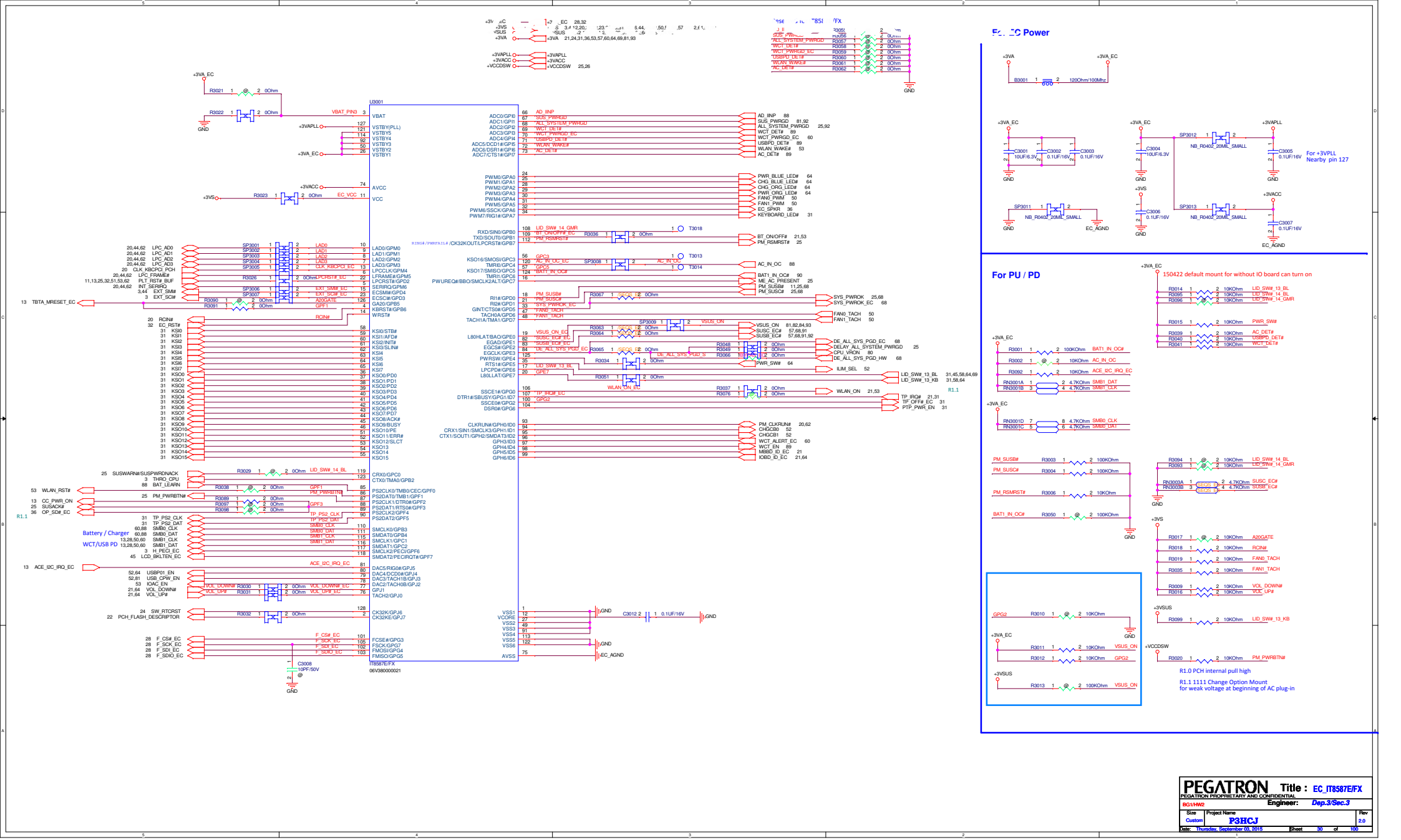


PCH SMBus

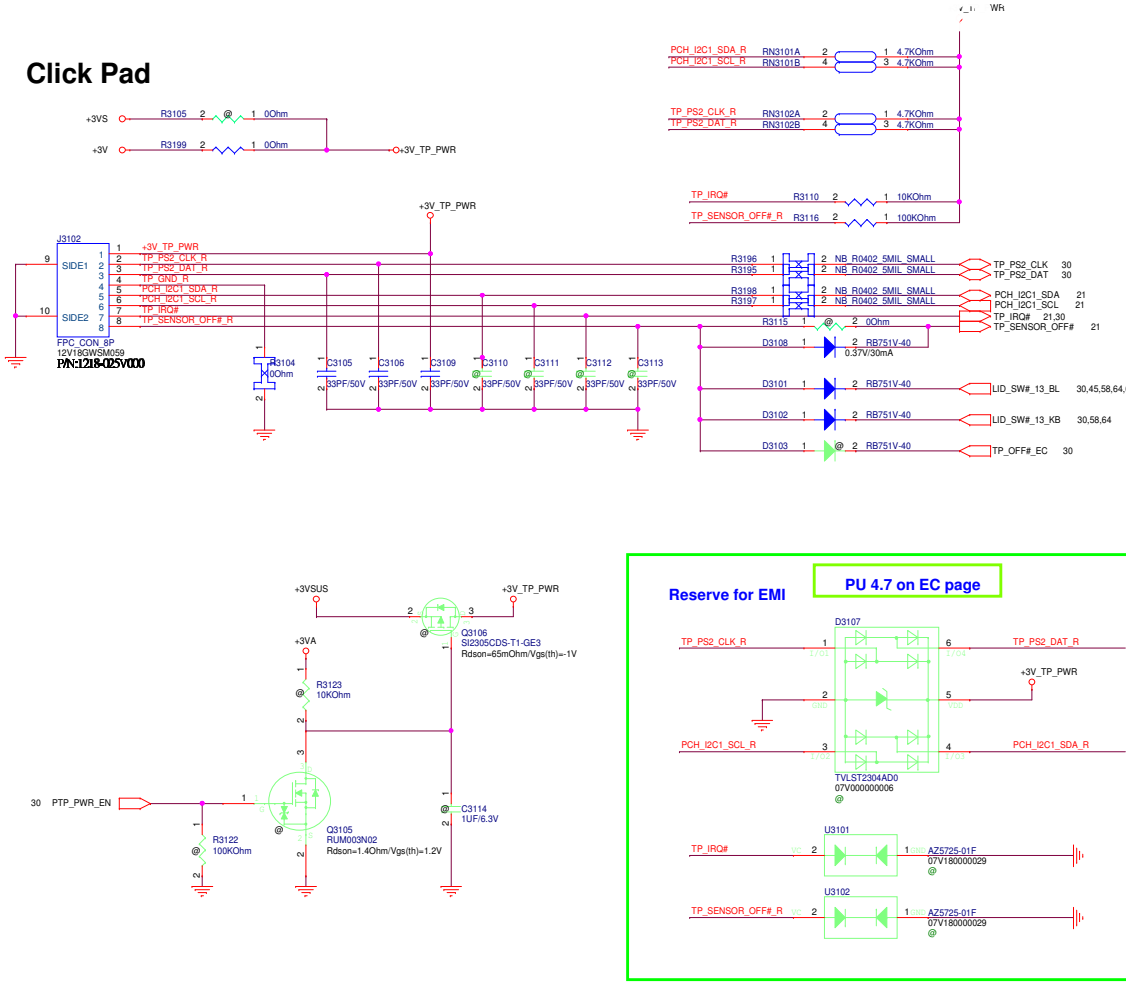




PEGATRON Title : PCH(9)_SPI,SMB
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1/HW2 Engineer: Dep.3/Sec.3
Size C | Project Name P3HCJ | Rev 2.0
Date: Thursday, September 03, 2015 | Sheet 28 of 100


U3001
IT8587E/FX
06V380000021
EC Power
For PU / PD
150422 default mount for without IO board can turn on
R1.0 PCH internal pull high
R1.1 1111 Change Option Mount
for weak voltage at beginning of AC plug-in
Battery / Charger
WCT/USB PD
PEGATRON
Title : EC_IT8587E/FX
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer: Dep.3/Sec.3
BG1/HW2
Size: Custom
Project Name: P3HCJ
Rev: 2.0
Date: Thursday, September 03, 2015
Sheet 30 of 100

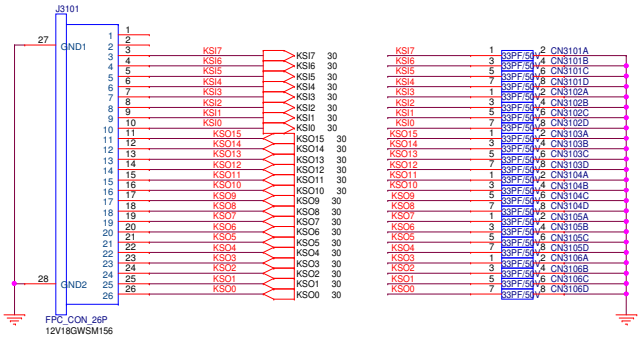
Click Pad



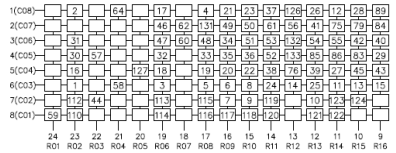
Reserve for EMI

PU 4.7 on EC page

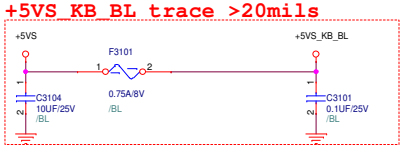
Keyboard



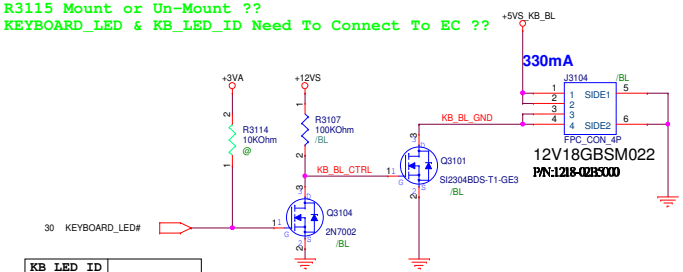
The pin define is checked to keyboard spec. R is KSO, C is KSI. The connector pin define is the same the KB.



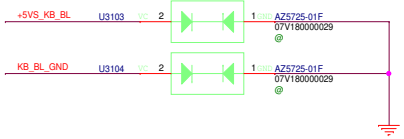
+5VS_KB_BL trace >20mils



R3115 Mount or Un-Mount ??
KEYBOARD_LED & KB_LED_ID Need To Connect To EC ??

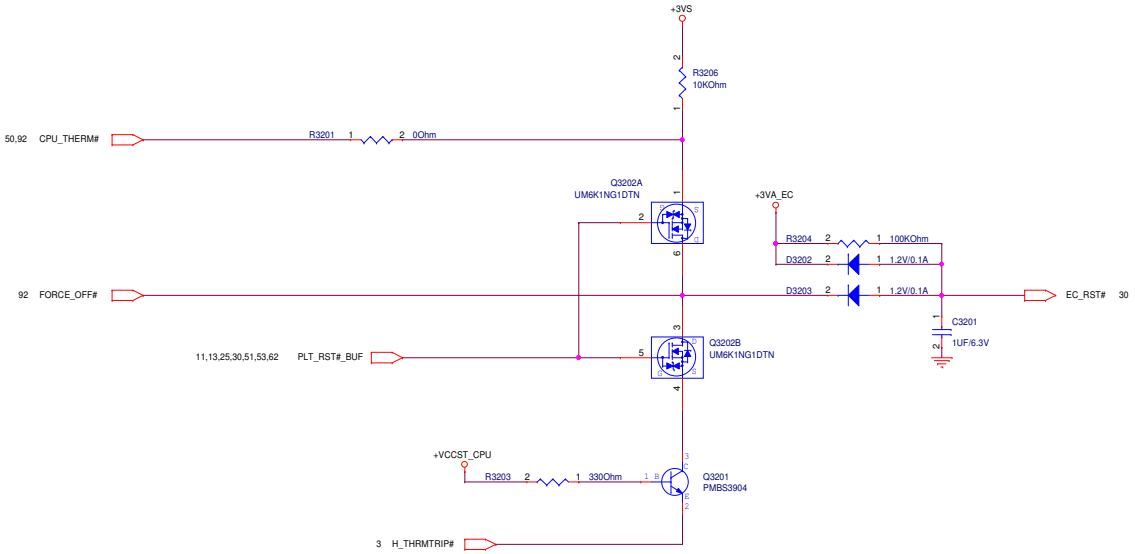


KB_LED_ID	
1	KB w/o BL
0	KB w/ BL



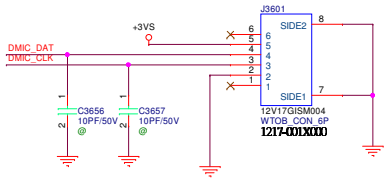
PEGATRON Title : KB/TP
BG1\CORE Engineer: Dep.3/Sec.3
Size C | Project Name P3HCJ | Rev 2.0
Date: Thursday, September 03, 2015 | Sheet 31 of 100

+VCCST_CPU +VCCST_CPU 3,5,7,9,25
+3VA_EC +3VA_EC 28,30
+3VS +3VS 3,4,12,20,21,22,23,24,28,30,31,36,44,45,48,50,51,53,57,58,62,64,91,92

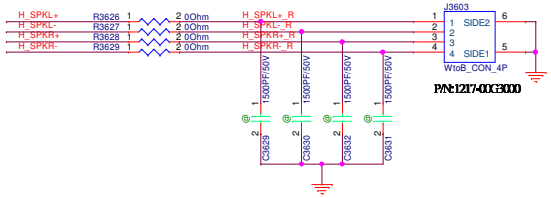


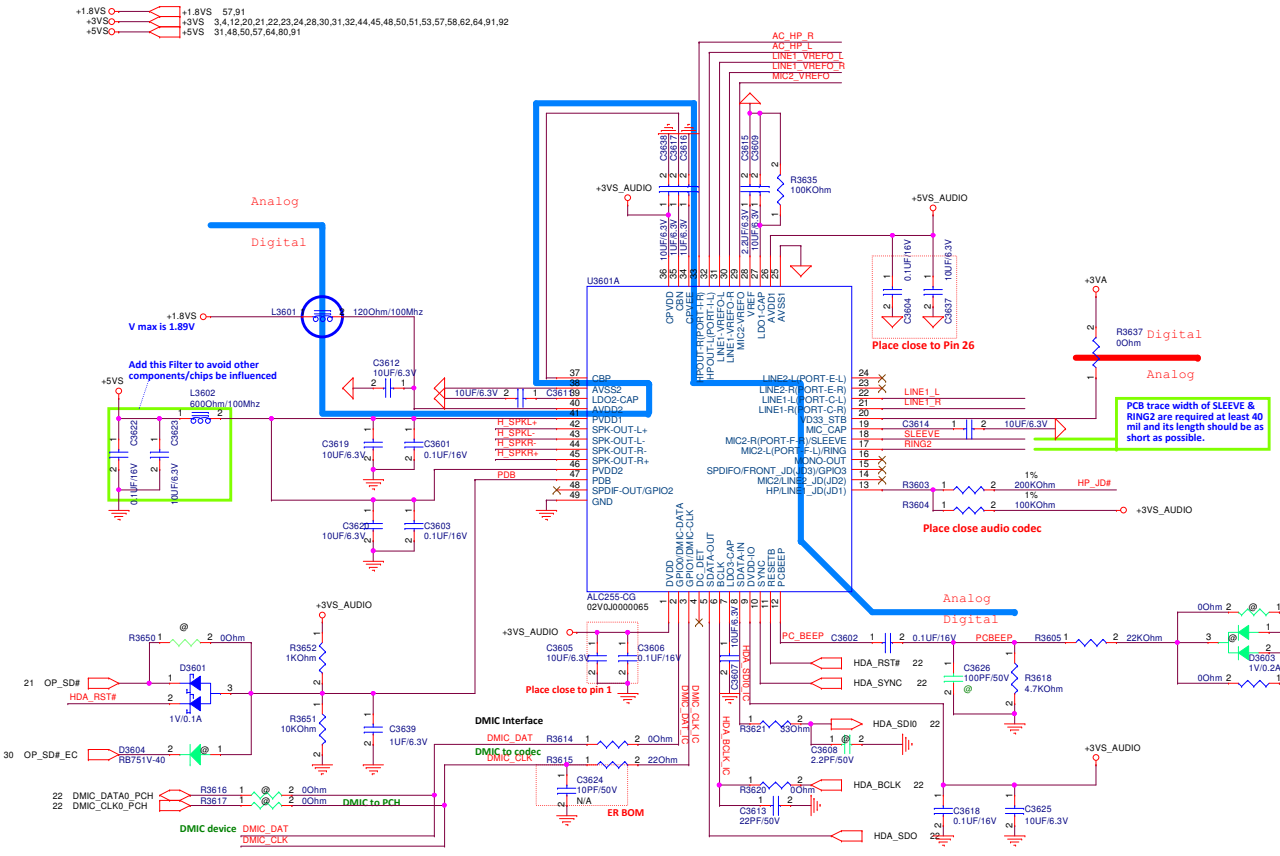
PEGATRON Title : RST_Reset Circuit
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1/HW2 Engineer: Dep.3/Sec.3
Size C | Project Name P3HCJ | Rev 2.0
Date: Thursday, September 03, 2015 | Sheet 32 of 100

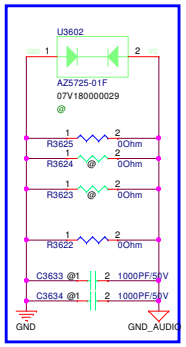
DMIC

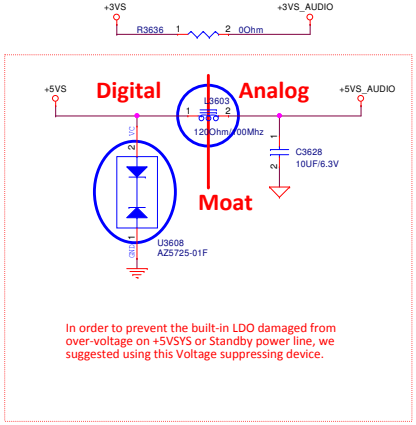


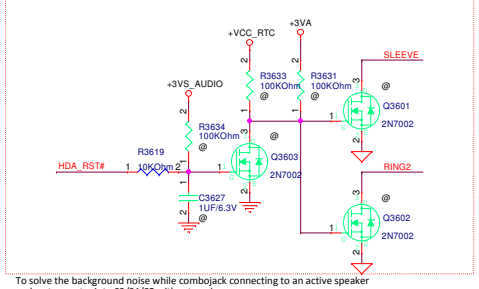
Internal Speaker

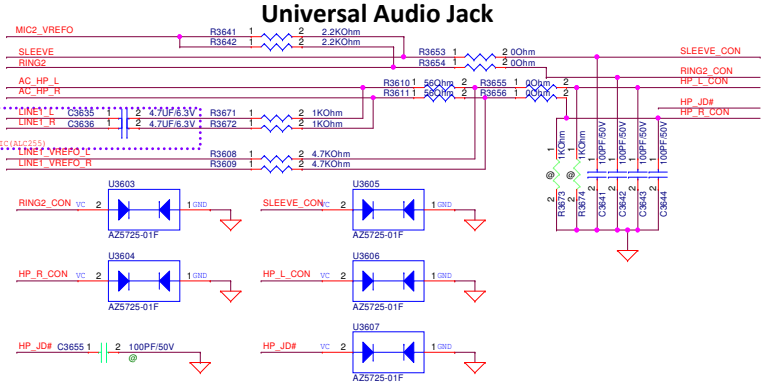






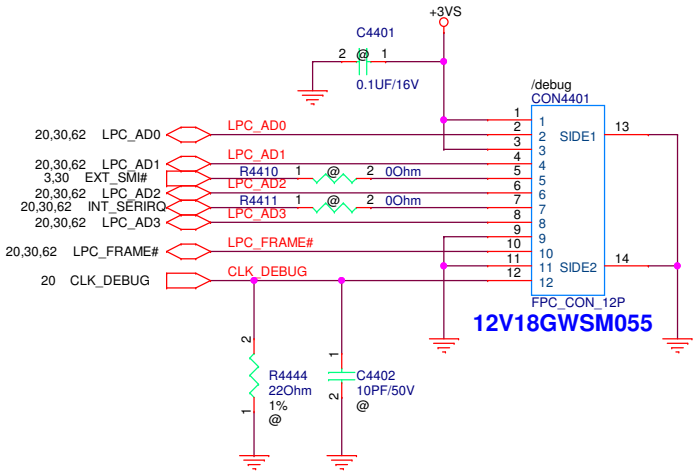






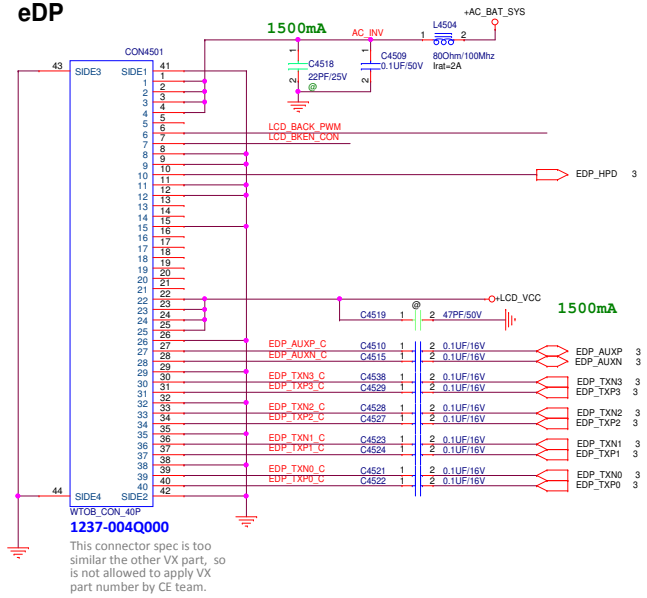
PEGATRON	Title :	AUD(1)_ALC283
BG1\CORE	Engineer:	Dep.3/Sec.3
Size: Custom	Project Name: P3HCJ	Rev: 2.0
Date: Thursday, September 03, 2015	Sheet 36 of 100	

DEBUG CARD CONN.



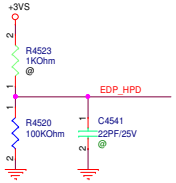
PEGATRON PROPRIETARY AND CONFIDENTIAL	Title : DEBUG CONN.	
BG1/HW2	Engineer: Dep.3/Sec.3	
Size: B	Project Name: P3HCJ	Rev: 2.0
Date: Thursday, September 03, 2015	Sheet 44 of 100	

eDP

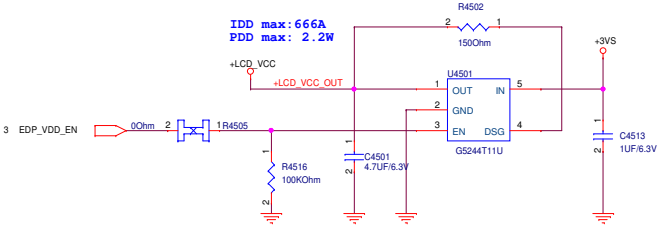


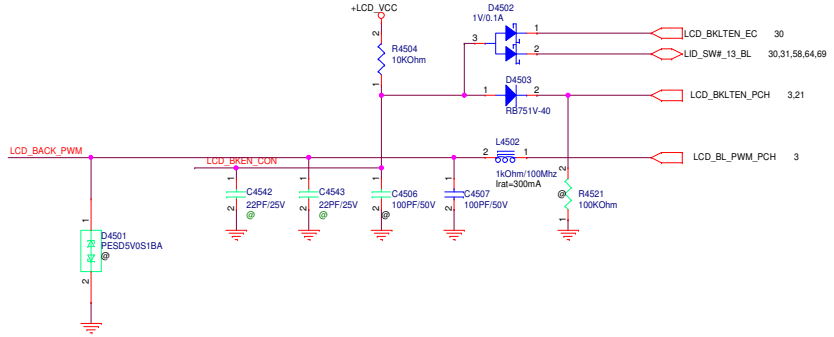
1237-004Q000

This connector spec is too similar the other VX part, so is not allowed to apply VX part number by CE team.



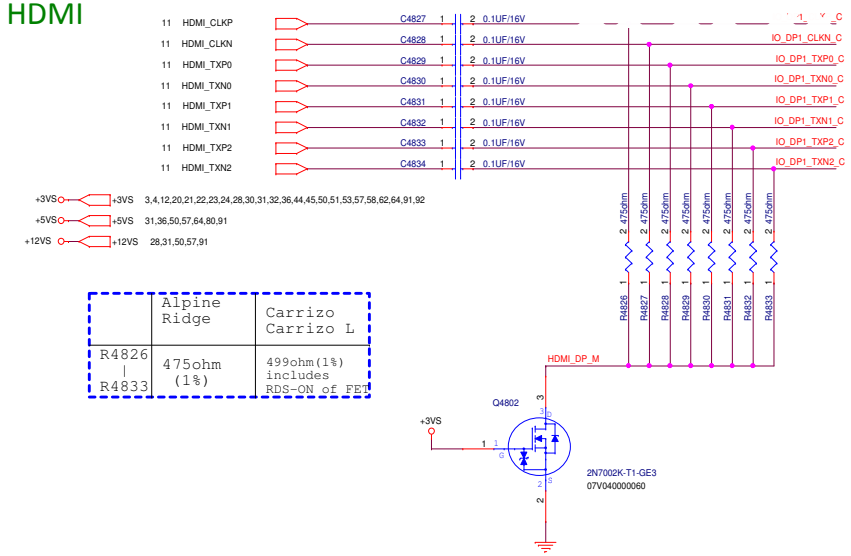
LCD VDDEN / +LED_VCC



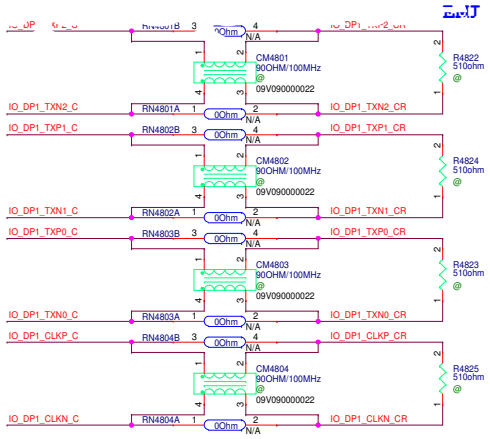


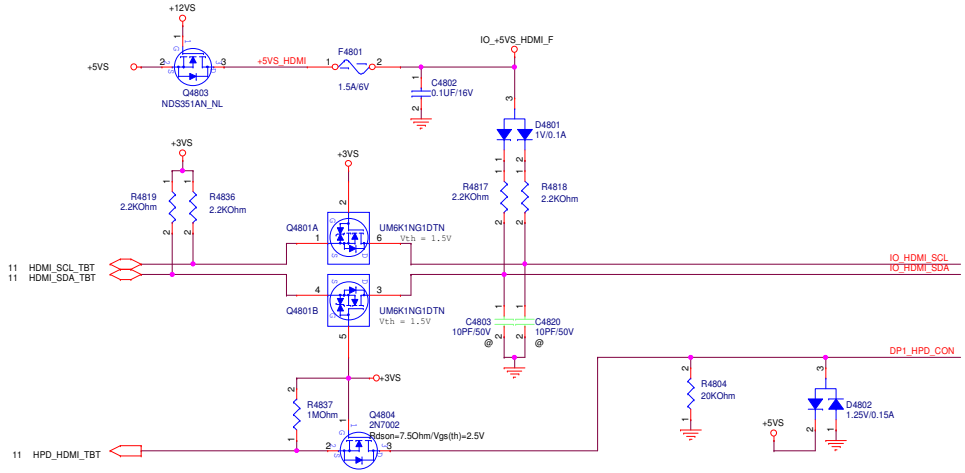
PEGATRON	Title : eDP CONN	
BG1\CORE	Engineer: Dep.3/Sec.3	
Size: C	Project Name: P3HCJ	Rev: 2.0
Date: Thursday, September 03, 2015	Sheet 45 of 100	

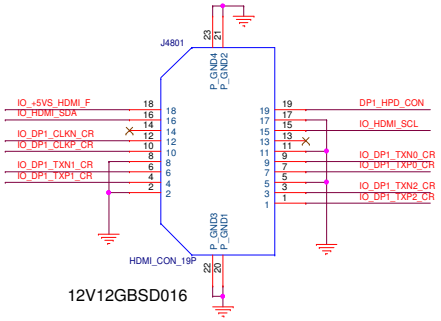
HDMI



	Alpine Ridge	Carrizo Carrizo L
R4826 | R4833	475ohm (1%)	499ohm(1%) includes RDS-ON of FET







12V12GBSD016

PEGATRON Title : HDMI-4K2K

PEGATRON PROPRIETARY AND CONFIDENTIAL

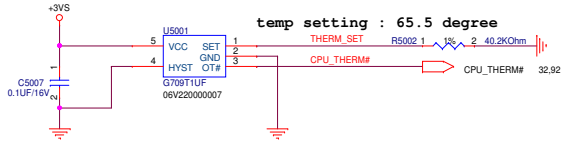
Engineer: Dep.3/Sec.3

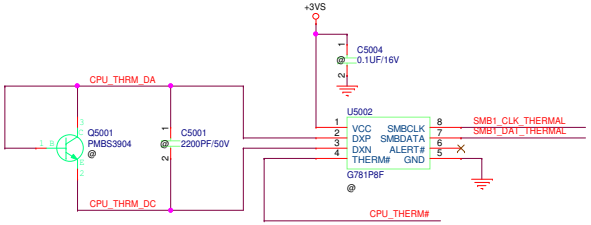
BG1/HW3

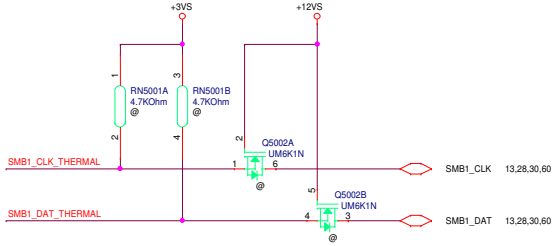
Size	Project Name	Rev
C	P3HCJ	2.0

Date: Thursday, September 03, 2015 Sheet 48 of 100

G709Thermal Sensor

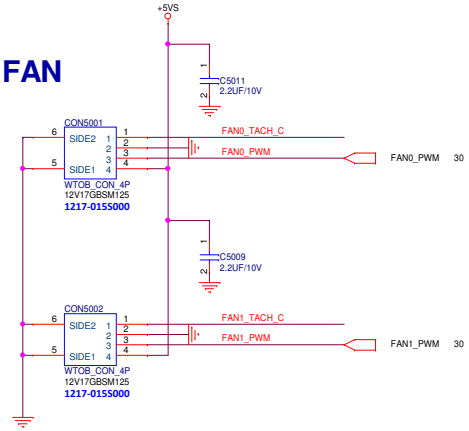


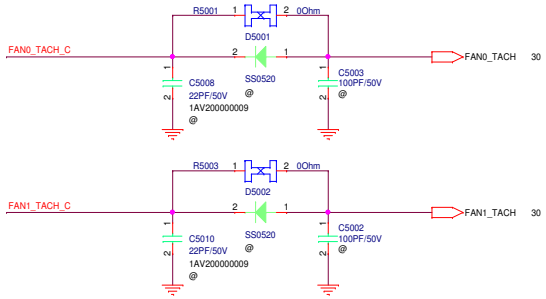




PWM FAN

FAN





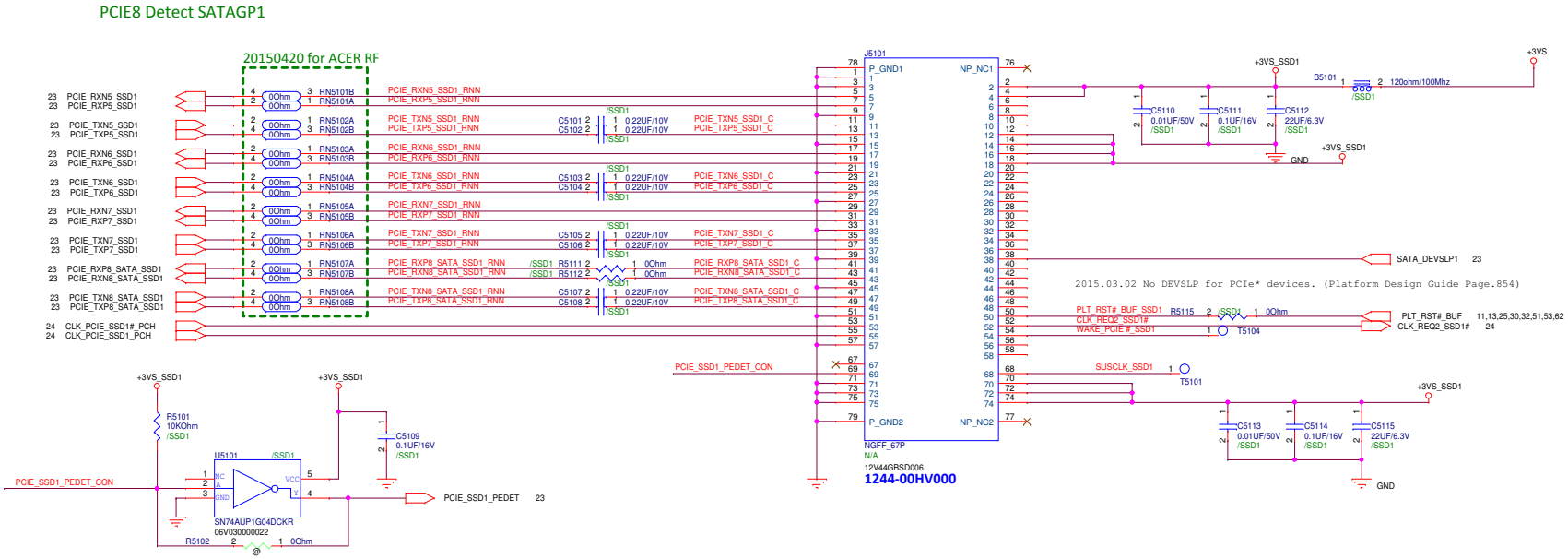
PEGATRON Title : Thermal/Fan

BG1\CORE Engineer: Dep.3/Sec.3

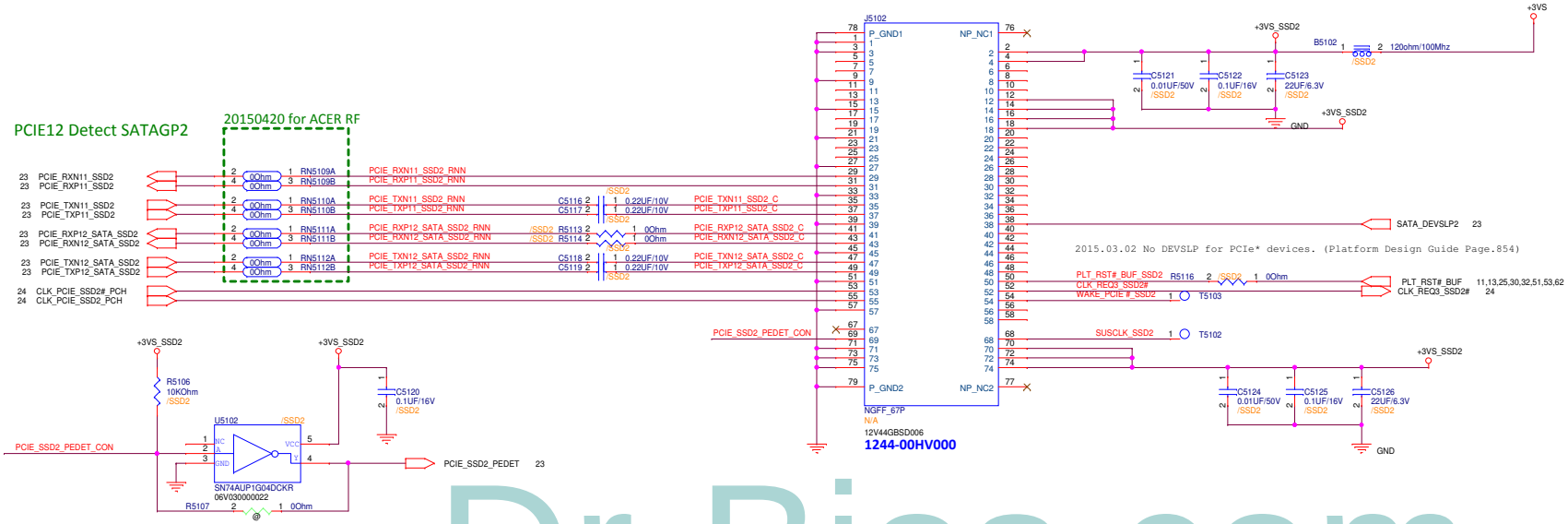
Size	Project Name	Rev
C	P3HCJ	2.0

Date: Thursday, September 03, 2015 Sheet 50 of 100

NGFF socket M -- PCIEx4 SSD1

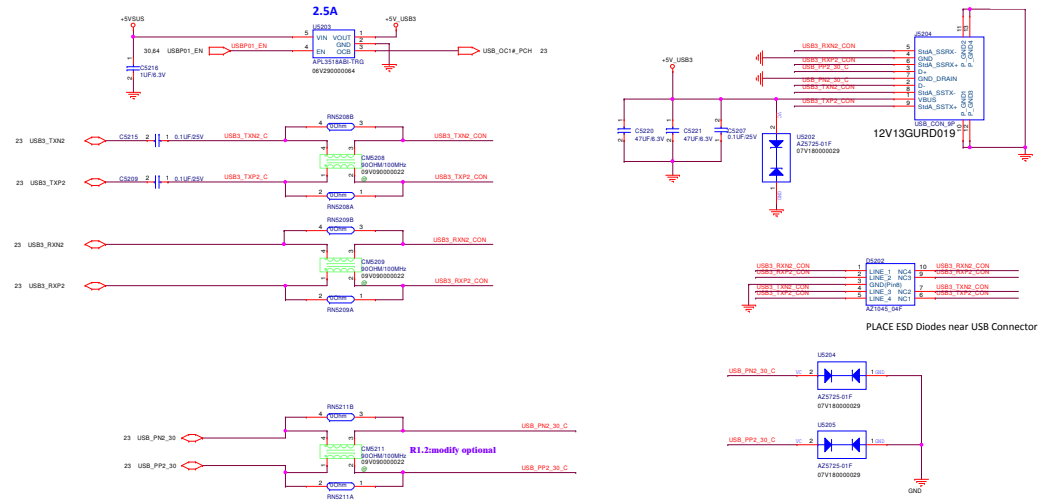


NGFF socket M -- PCIEx2 SSD2

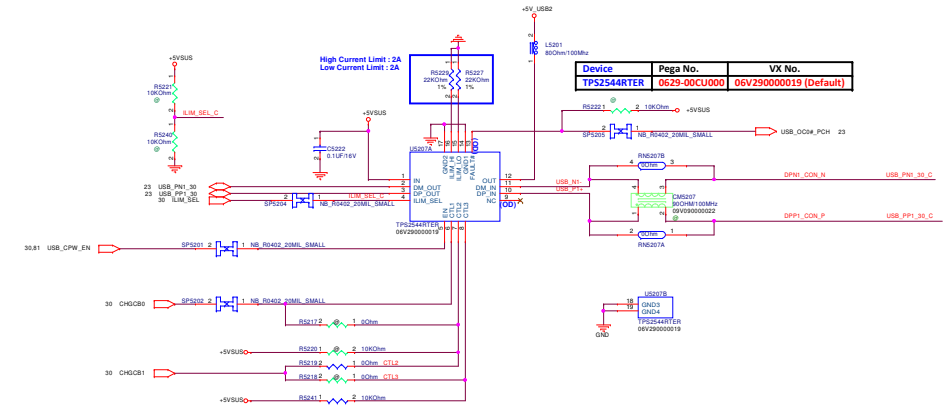


PEGATRON	Title : SSD & HDD	
PEGATRON PROPRIETARY AND CONFIDENTIAL	Engineer: Dep.3/Sec.3	
BG1/HW2		
Size: C	Project Name: P3HCJ	Rev: 2.0
Date: Thursday, September 03, 2015	Sheet 51 of 100	

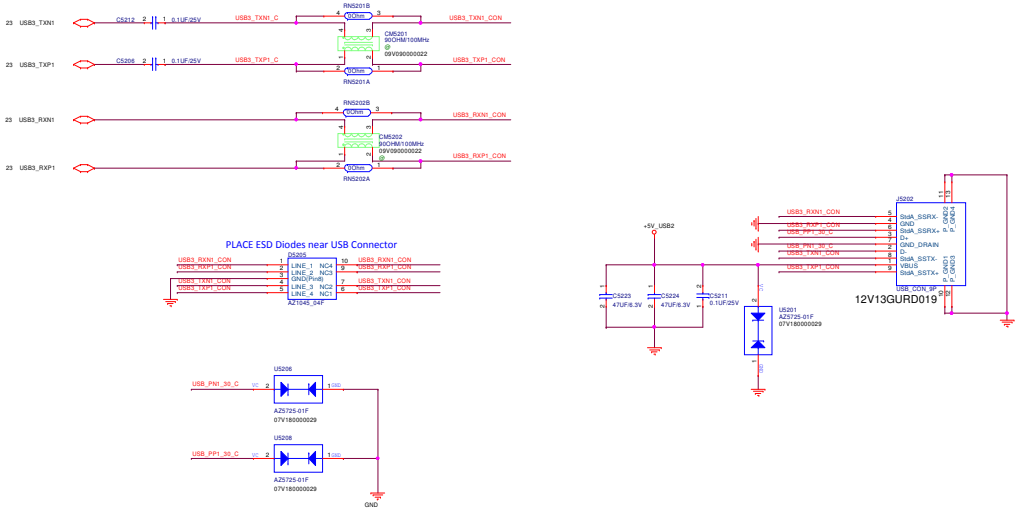
USB 3.0 ports x 1



USB 3.0 ports x 1 with Sleep & Charge Left_Down

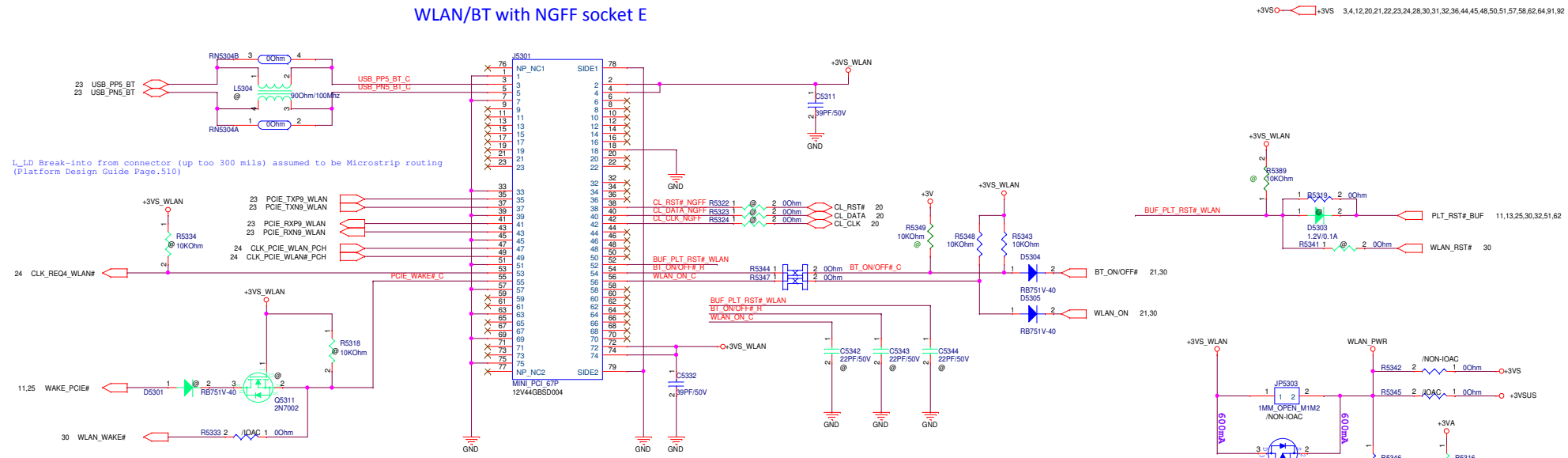


Device	Pega No.	VX No.
TPS2544RTER	0629-00CU000	06V290000019 (Default)



PEGATRON Title : USB JACK
Engineer: Dep.3/Sec.3
Project Name: P3HCJ
Rev: 2.0
Date: Thursday, September 03, 2015 Sheet 52 of 109

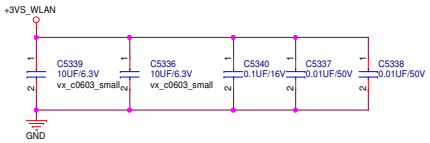
WLAN/BT with NGFF socket E



+3V_WLAN_WP1 bypass capactor:

Place 0.1UF near pin 2,4

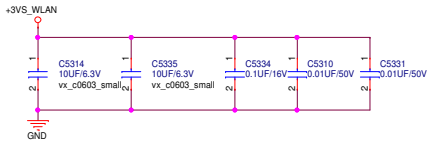
Place 10UF near +3V_WLAN_WP1 source side.



+3V_WLAN_WP1 bypass capactor:

Place 0.1UF near pin 72,74.

Place 10UF near +3V_WLAN_WP1 source side.



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : [illegible] UMI,PCIE,CLK,RTC,LPC

Engineer: Dep.3/Sec.3

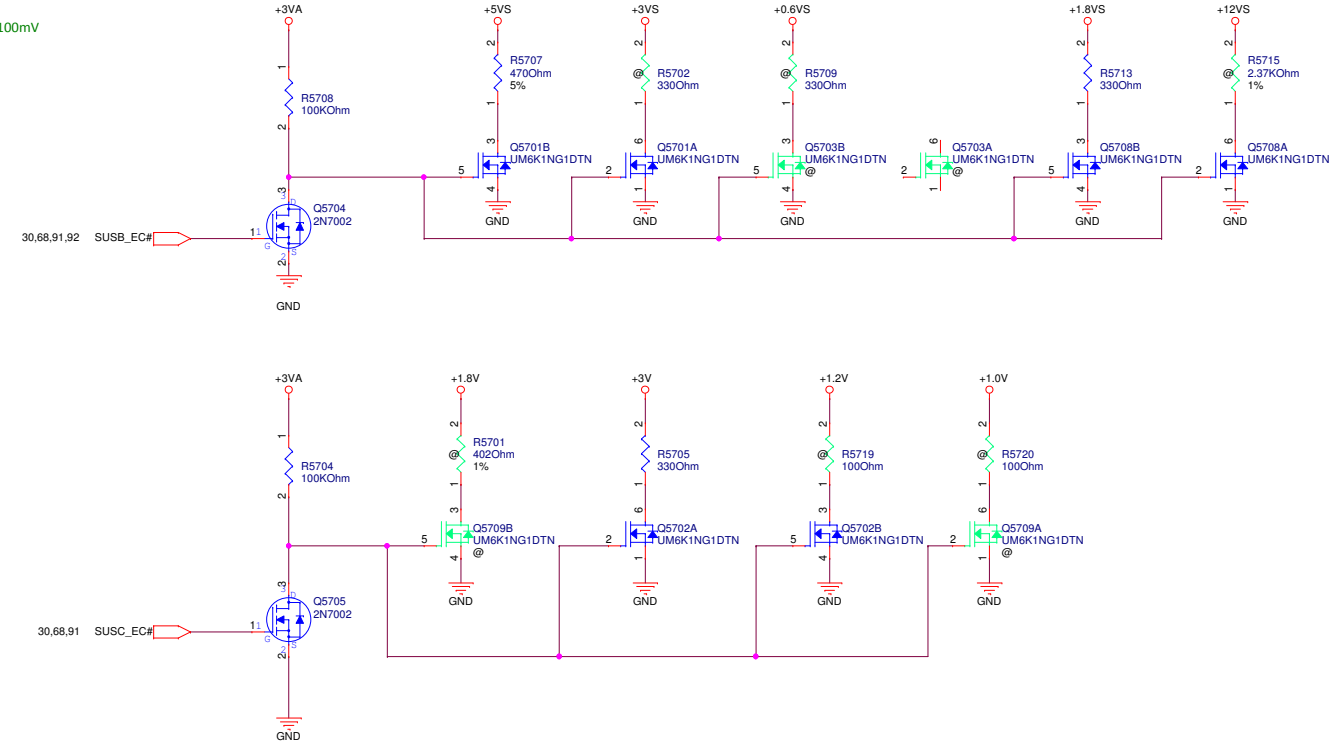
Size	Project Name	Rev
C	P3HCJ	2.0

BG1/HW3

Date: Thursday, September 03, 2015 Sheet 53 of 100

Discharge Circuit

100ms --->100mV



PEGATRON Title : DISCHARGE CKT

PEGATRON PROPRIETARY AND CONFIDENTIAL

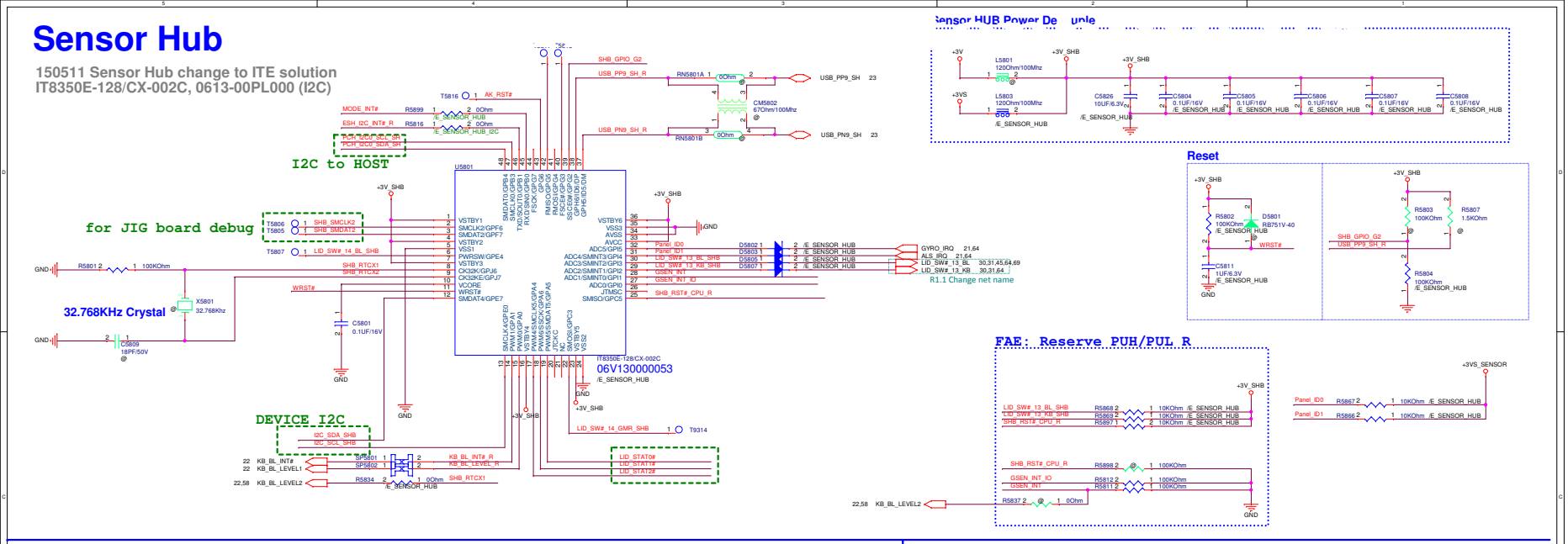
BG1/HW2 Engineer: Dep.3/Sec.3

Size	Project Name	Rev
Custom	P3HCJ	2.0

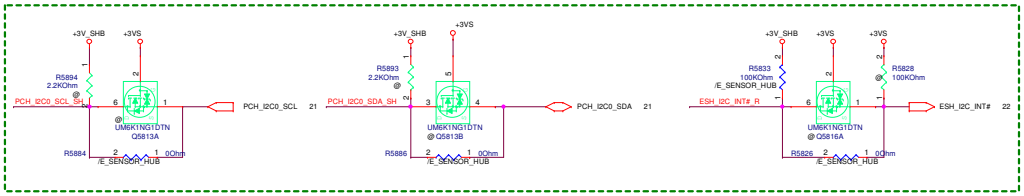
Date: Thursday, September 03, 2015 Sheet 57 of 100

Sensor Hub

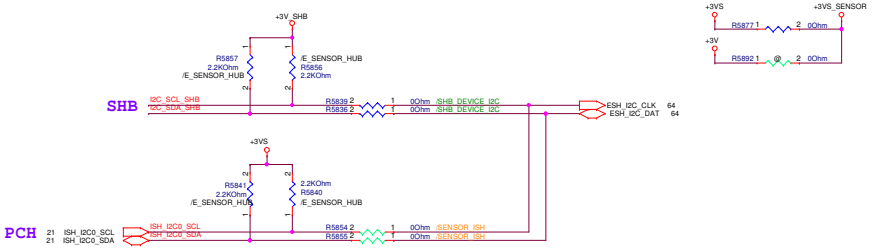
150511 Sensor Hub change to ITE solution
IT8350E-128/CX-002C, 0613-00PL000 (I2C)



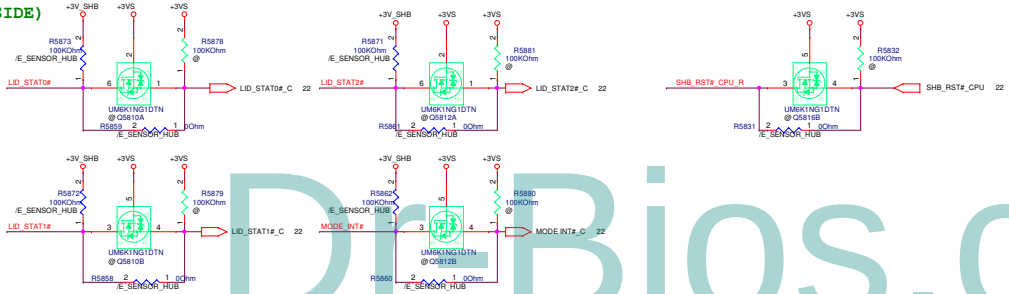
HOST I2C to SHB



DEVICE OPTION SHB / PCH_ISH



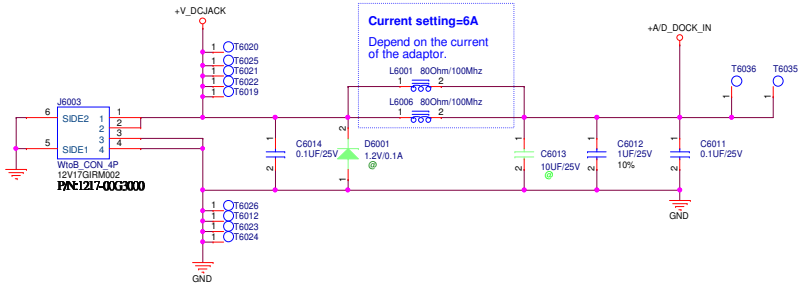
MODE GPIO(RESERVE PUH @ CPU SIDE)



PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : SHB_Sensor Hub
Engineer: Dep.3/Sec.3
BG1-HW BDC-HW2
Size: Custom | Project Name: P3HCJ | Rev: 2.0
Date: Thursday, September 03, 2015 | Sheet 58 of 100

DC Jack WtoB CONN



+VCC_RTC 24,25,26,36
+3VA_EC 28,30,32
+3VA 21,24,30,31,36,53,57,64,69,81,93
+5VA 64,81

+1.0VSUS 26,82
+1.8VSUS 9,26,84
+3VSUS 4,12,13,21,24,25,26,28,30,31,53,62,64,68,81,84,92
+5VSUS 13,52,64,81,84
+12VSUS 28,81,91

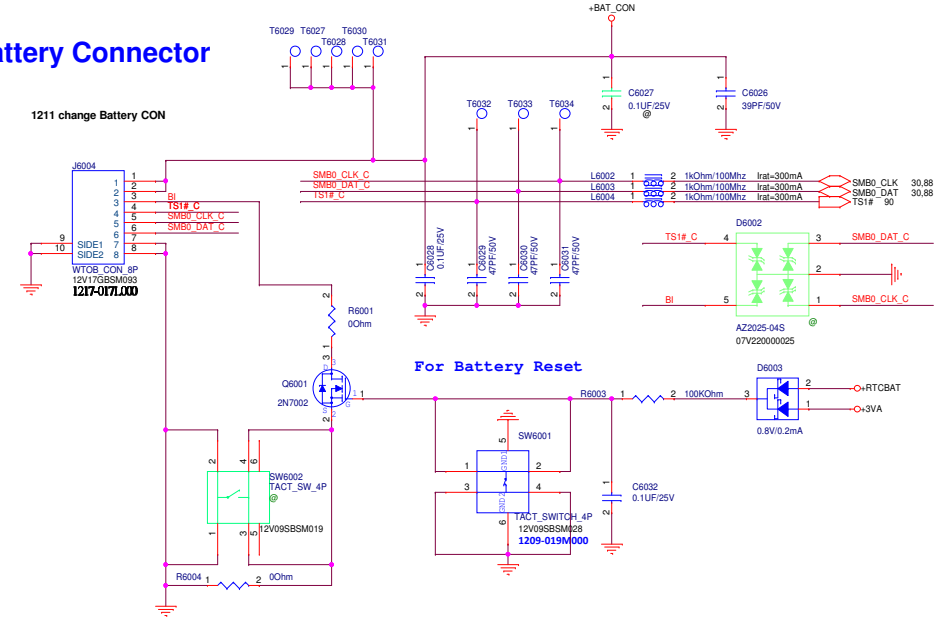
+3V 25,31,53,57,58,64,91

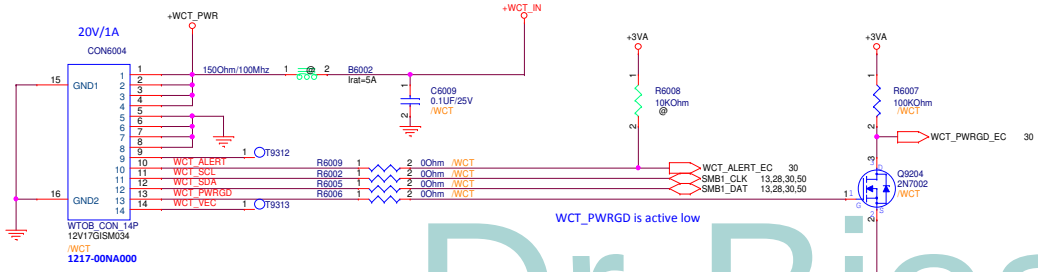
+12V 91

+1.8VS 36,57,91
+3VS 3,4,12,20,21,22,23,24,28,30,31,32,36,44,45,48,50,51,53,57,58,62,64,91,92
+5VS 31,36,48,50,57,64,80,91
+12VS 28,31,48,50,57,91

+AC_BAT_SYS 45,80,81,82,83,88
+A/D_DOCK_IN 89
+BAT_CON 88
+WCT_IN 89
+VCORE 5,80
+VCCGT 6,80
+VCCSA 7,80
+VCCIO 3,7,9,91

Battery Connector

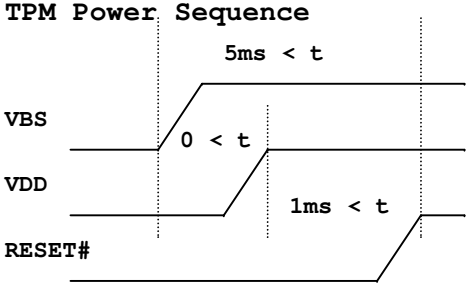




PEGATRON Title : DC_DC/BAT CONN
PEGATRON COMPUTER INC Engineer: Dep.3/Sec.3
Size C | Project Name P3HCJ | Rev 2.0
Date: Thursday, September 03, 2015 | Sheet 60 of 100

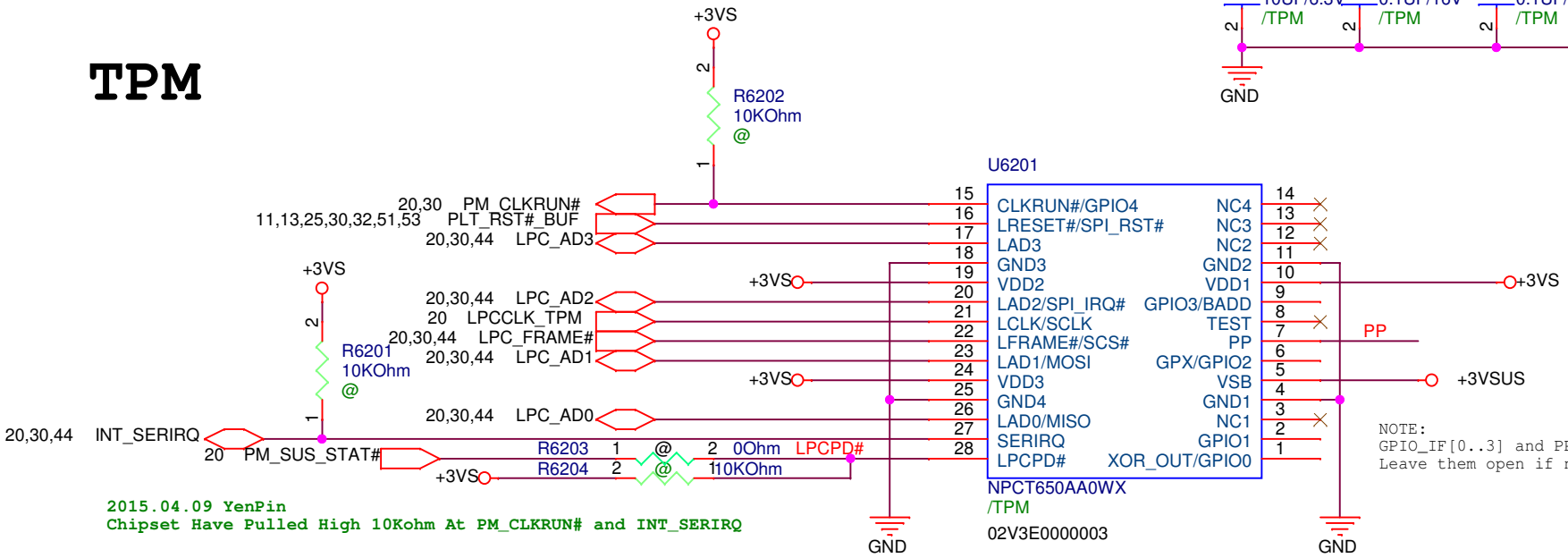
TPM

TPM Power Sequence



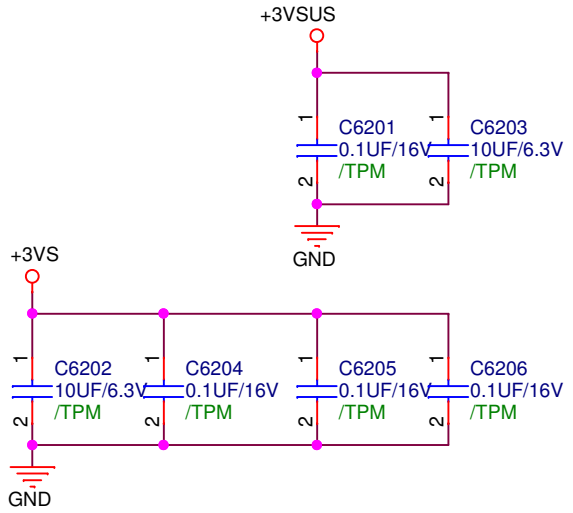
NOTE: RESET# is LRESET#, SPI_RST# or SRESET#.

NOTE:
1) For TPM 1.2:
The TPM VSB pin must be connected to the system's standby voltage (existing at S3 power state).
2) For TPM 2.0:
It is recommended to connect the TPM VSB pin to the system's standby voltage to improve performance.
3) TPM VDD pins should be connected to the same power rail that feeds the Chipset LPC interface.
4) RESET# must be asserted for at least 5 msec after VSB power-up.
5) VSB may come up anytime before VDD power-up, but not after VDD power-up.
6) RESET# may be asserted together with VDD power negation, but should not at any point exceed 0.5V above the VDD power level.



NOTE:
GPIO_IF[0..3] and PP are optional.
Leave them open if not used.

2015.04.09 YenPin
Chipset Have Pulled High 10Kohm At PM_CLKRUN# and INT_SERIRQ



PP 1 T6201

NOTE:
1) The PP is an input signal with configurable polarity.
2) By default the PP functionality is disabled.

LPCPD# 1 T6202

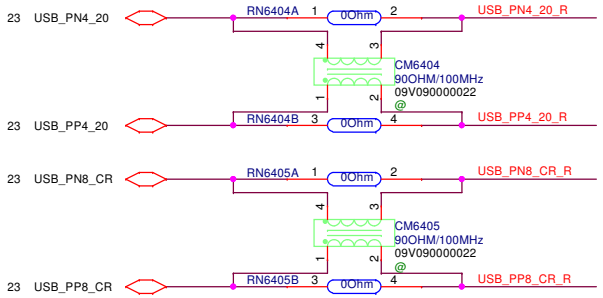
Note:
When LPCPD# functionality is not required, an internal pull-up resistor allows this pin to be left floating.

PEGATRON	Title : TPM CONN	
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Dep.3/Sec.3	
Size: A	Project Name: P3HCJ	Rev: 2.0
Date: Thursday, September 03, 2015	Sheet 62 of 100	

I/O Board

MB Connector Pin Define

	P3HCJ/P4HCJ
1	+5VSUS
2	+5VSUS
3	+5VSUS
4	+5VSUS
5	SWAP_ID1
6	USB_PN4_20
7	USB_PP4_20_R
8	GND
9	GND
10	GND
11	USBP01_EN
12	USB_OC2#_PCH
13	+3VA
14	PWR_SW#
15	VOL_UP#
16	VOL_DOWN#
17	+3VS
18	+3VS_CR
19	+3VS_CR
20	USB_PN8_CR
21	USB_PP8_CR
22	GND
23	GND
24	GND

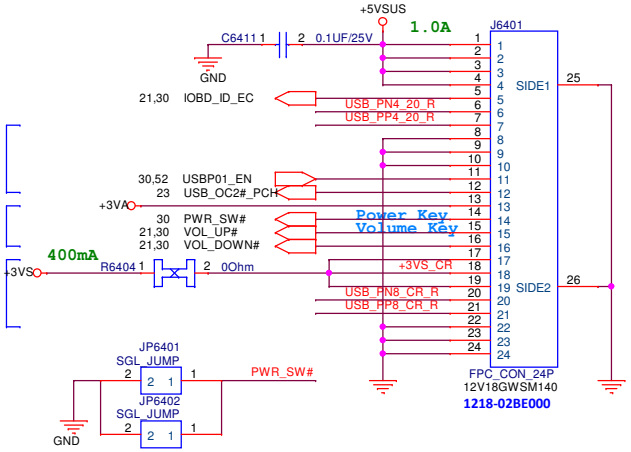


IO BD ID

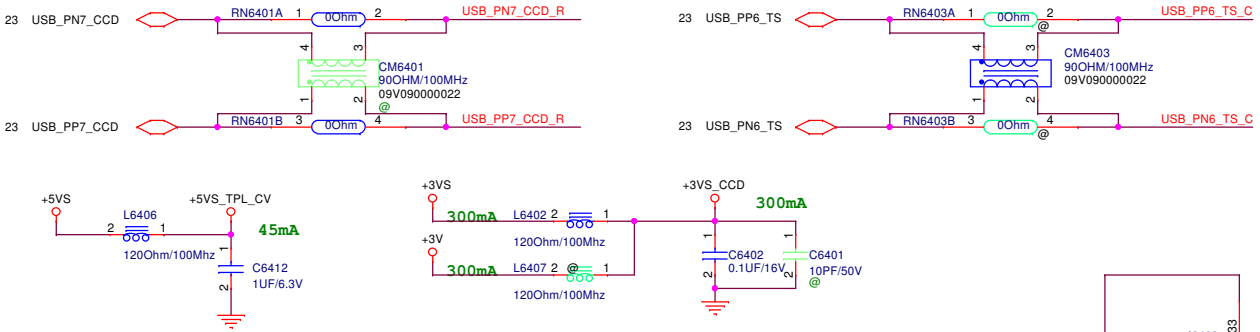
USB2.0

PWR/VOL KEY

Card Reader



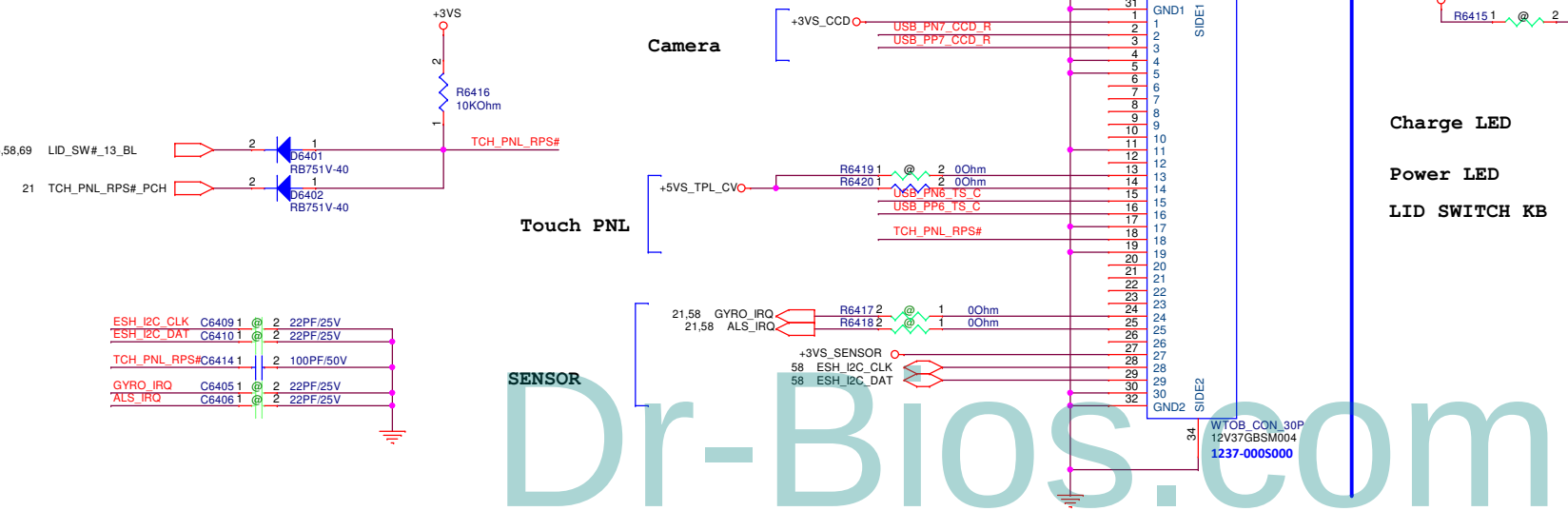
Sensor Board



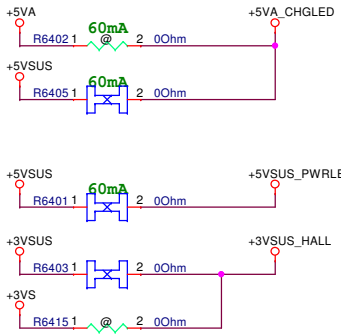
Camera

Touch PNL

SENSOR



LED Board



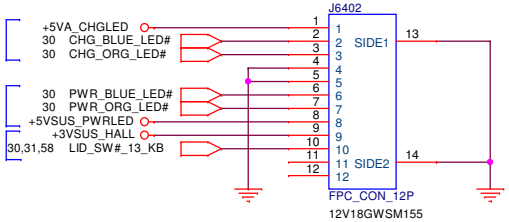
MB Connector Pin Define

	P3HCJ/P4HCJ
1	+5VSUS_LED
2	PWR_BLUE_LED#
3	PWR_ORG_LED#
4	GND
5	GND
6	CHG_BLUE_LED#
7	CHG_ORG_LED#
8	NC
9	+3VA_ALS
10	LID_SW#_IO

Charge LED

Power LED

LID SWITCH KB



PEGATRON Title : IO Board Conn.

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW2 Engineer: Dep.3/Sec.3

Size	Project Name	Rev
A3	P3HCJ	2.0

Date: Thursday, September 03, 2015 Sheet 64 of 100

TOP CPU NUT

H6501 CT217B136ID106 1308-0082000
H6502 CT217B136ID106 1308-0082000
H6503 CT217B136ID106 1308-0082000
H6504 CT217B136ID106 1308-0082000

BOT ME NUT

H6523 CT217B136ID106 1308-0082000
H6524 CT217B136ID106 1308-0082000
H6525 CT217B136ID106 1308-0082000

A x1

H6531 CR276X295D98

B x1

H6532 C276D98 S1V1XDCCLY00

F x2

H6535 S315D98 S1V3XFSSVY00
H6536 S315D98 S1V3XFSSVY00

C TOP x4

H6560 CRT236X193D102N
H6561 CRT236X193D102N
H6562 CRT236X193D102N

N TOP x1

H6543 RT236X150D71N

TOOLING HOLE

H6558 O118X98DO118X98N
H6568 C98D98N

M BOT x4

H6539 CB236D106
H6540 CB236D106
H6541 CB236D106
H6542 CB236D106

D BOT x2 Ex1 Gx1

H6564 CRT236X193D102N
H6565 CRT236X193D102N
H6566 CRT236X193D102N
H6567 CRT236X193D102N

Lx1 Ox1

H6555 SP276D98
H6556 SP276D98

SC x 33+28

SC6501 SC6502 SC6503 SC6504 SC6505 SC6506 SC6507 SC6508 SC6509 SC6510
SC6511 SC6512 SC6513 SC6514 SC6515 SC6516 SC6517 SC6518 SC6519 SC6520
SC6521 SC6522 SC6523 SC6524 SC6525 SC6526 SC6527 SC6528 SC6529 SC6530
SC6531 SC6532 SC6533 SC6535 SC6536 SC6537 SC6538 SC6539
SC6541 SC6542 SC6543 SC6544 SC6545 SC6546 SC6547 SC6548 SC6549 SC6550
SC6551 SC6552 SC6553 SC6554 SC6555 SC6556 SC6557 SC6558 SC6559 SC6560
SC6561 SC6562 SC6563
RHC-CP-13T09

H6544 SP276D98

PEGATRON Title : ME_CONN,Screw Hole
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer: HW2
BG1/HW2
Size C | Project Name ADLER | Rev 2.0
Date: Thursday, September 03, 2015 | Sheet 65 of 99

11,25,30 PM_SUSB# — R6801 1 2 0Ohm /BYPAS_EC — SUSB_EC# 30,57,91,92

25,30 PM_SUSC# — R6802 1 2 0Ohm /BYPAS_EC — SUSC_EC# 30,57,91

+3VSUS — +3VSUS 4,12,13,21,24,25,26,28,30,31,53,62,64,81,84,92

For Intel power sequence requestment
ALL_SYS_PWRGD to Delay_ALL_SYS_PGD >2ms

Delay By EC(2ms+ EC processing time (3ms~33ms)

30 DE_ALL_SYS_PGD_EC — R6809 1 2 0Ohm /BYPAS_EC — DE_ALL_SYS_PGD_EC_R

+3VSUS

U6802
1 A VCC 5
PM_SUSB# 2 B
3 GND Y 4
Vcc=2~5.5
/BYPAS_EC

For shut down Sequence
Tplt17 < 1us

R6808 1 2 @100KOhm 10V240000005 — GND

C6804 1 2 @0.1UF/25V — GND

4 — DE_ALL_SYS_PGD_HW 30

+3VSUS

For shut down Sequence Tplt17 < 1us
Due to PDG1.2 Figure 43-5. SYS_PWROK drop after PM_SUSB# before CPU_VRON to add this solution

U6803
PM_SUSB# 1 A VCC 5
30 SYS_PWROK_EC — SP6802 1 2 — SYS_PWROK_EC_G 2 B
3 GND Y 4
Vcc=2~5.5
/BYPAS_EC

R6804 1 2 0Ohm /BYPAS_EC — SYS_PWROK 25,30

R6806 1 2 @100KOhm 10V240000005 — GND

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : POWER Sequence

BG1/HW2

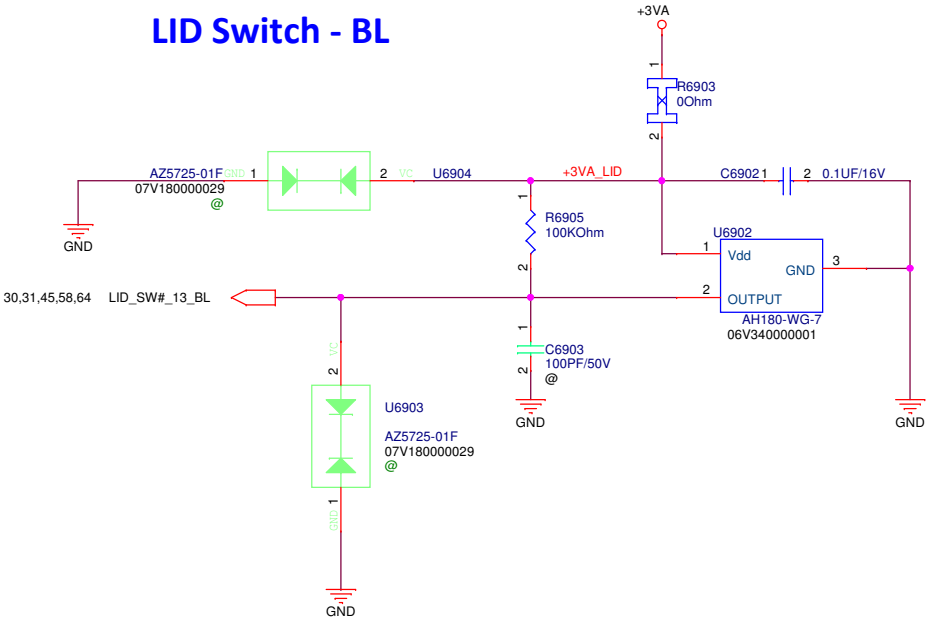
Engineer: Dep.3/Sec.3

Size	Project Name	Rev
B	P3HCJ	2.0

Date: Thursday, September 03, 2015 Sheet 68 of 100

+3VA 21,24,30,31,36,53,57,60,64,81,93
+3VSUS 4,12,13,21,24,25,26,28,30,31,53,62,64,68,81,84,92
+3VS 3,4,12,20,21,22,23,24,28,30,31,32,36,44,45,48,50,51,53,57,58,62,64,91,92

LID Switch - BL



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

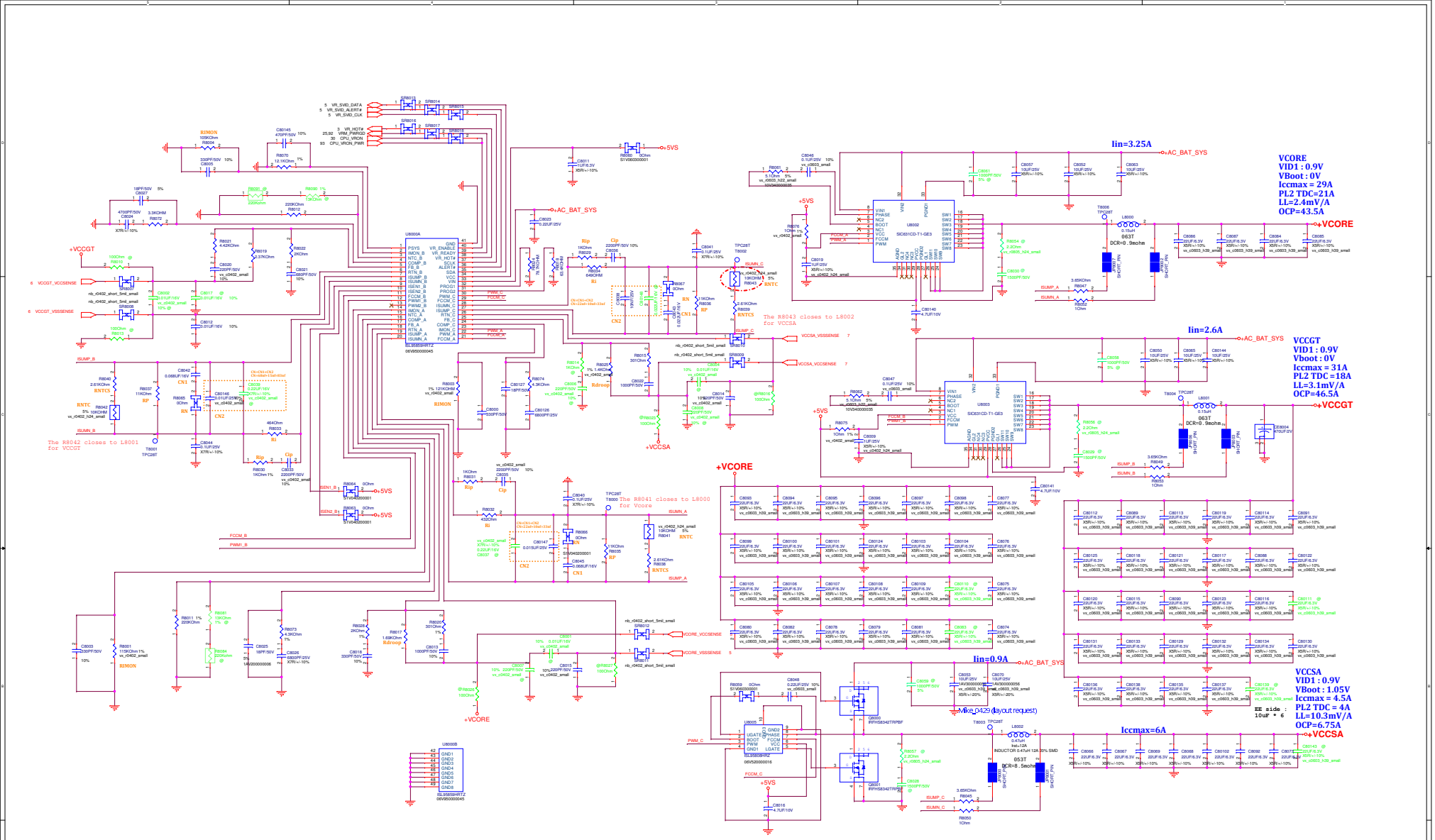
Title : Power SW Board

BG1/HW2

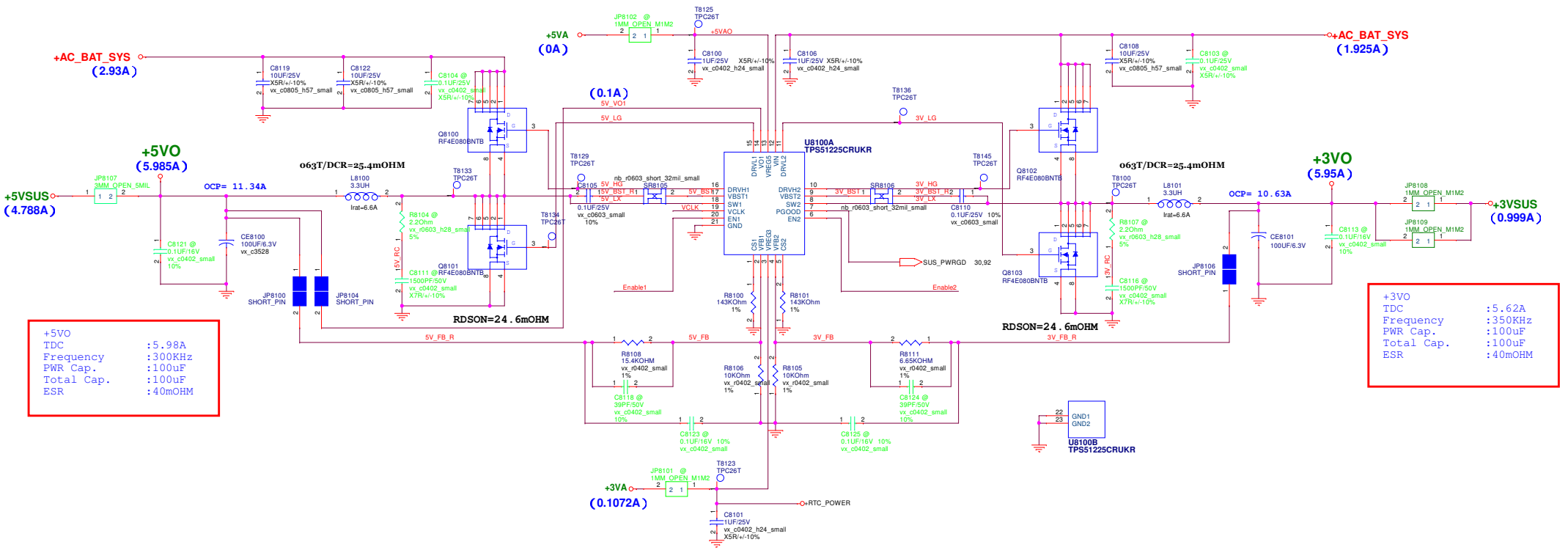
Engineer: Dep.3/Sec.3

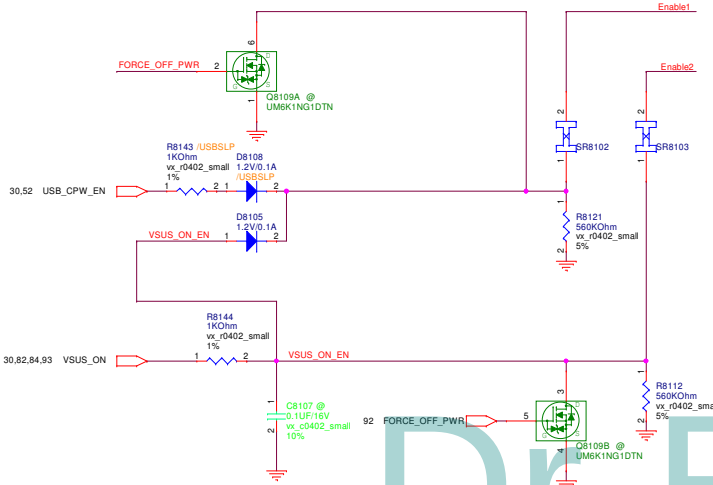
Size	Project Name	Rev
B	P3HCJ	2.0

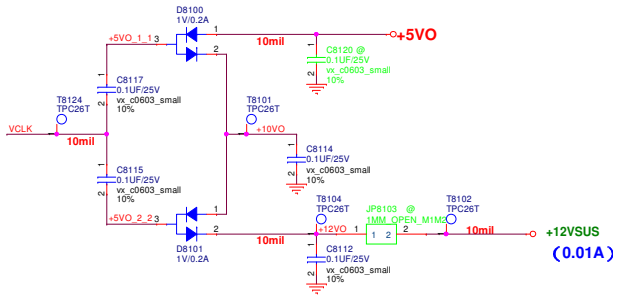
Date: Thursday, September 03, 2015 Sheet 69 of 100

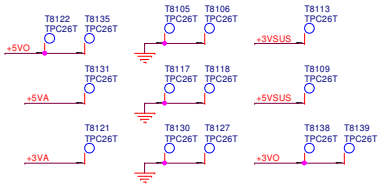

lin=3.25A
VCORE
VID1 : 0.9V
VBoot : 0V
Iccmax = 29A
PL2 TDC=21A
LL=2.4mV/A
OCP=43.5A
+VCORE
lin=2.6A
VCCGT
VID1 : 0.9V
Vboot : 0V
Iccmax = 31A
PL2 TDC =18A
LL=3.1mV/A
OCP=46.5A
+VCCGT
lin=0.9A
VCCSA
VID1 : 0.9V
VBoot : 1.05V
Iccmax = 4.5A
PL2 TDC = 4A
LL=10.3mV/A
OCP=6.75A
+VCCSA
Iccmax=6A
+AC_BAT_SYS
+5VS
+VCCGT
+VCCSA
The R8042 closes to L8001 for VCCGT
The R8043 closes to L8002 for VCCSA
The R8041 closes to L8000 for Vcore
Mike_0429 (layout request)
EE side : 10uF * 6

+5VO & +3VO POWER SUPPLY









<variant_name>

PEGATRON PROPRIETARY AND CONFIDENTIAL

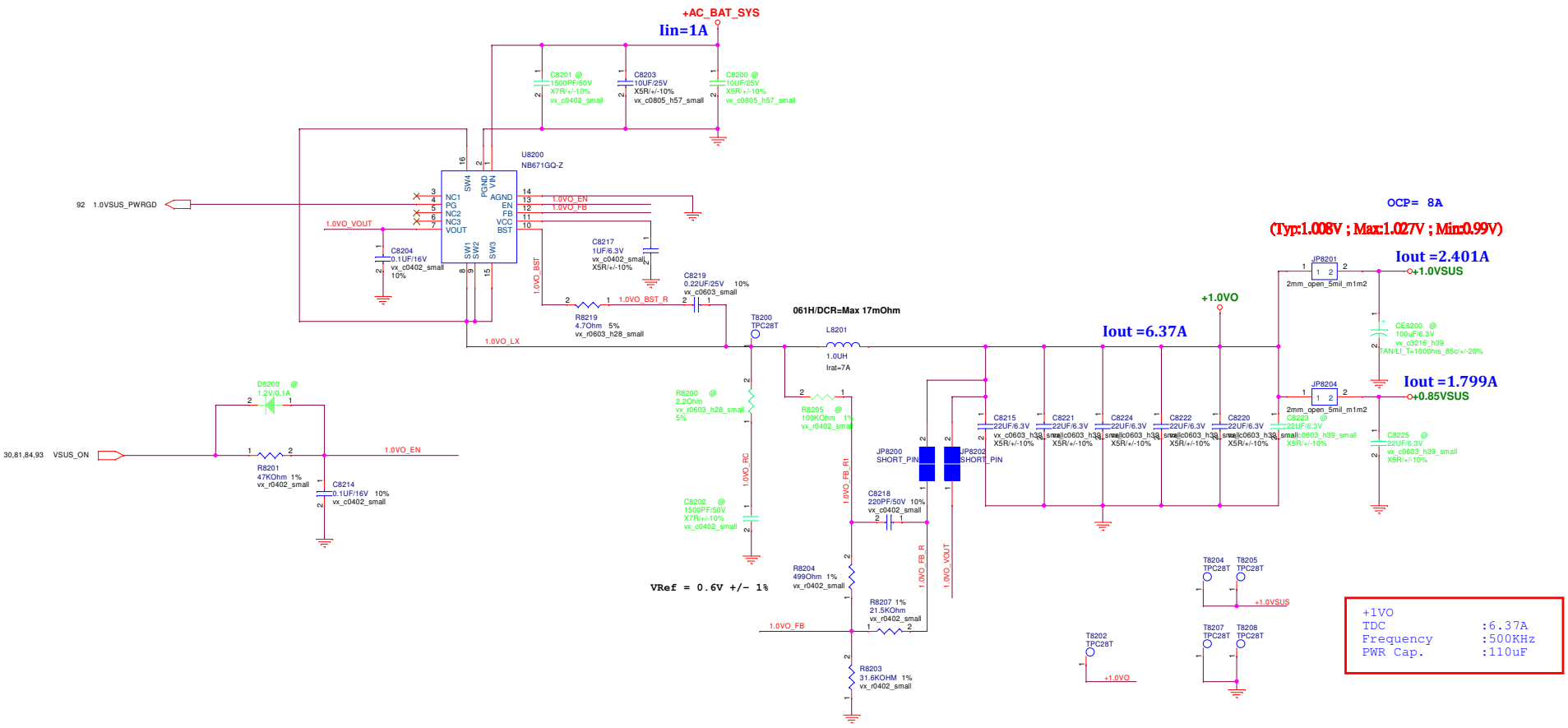
Title : POWER_SYSTEM

Engineer: Mike_Ke

Size	Project Name	Rev
Custom	P3HCJ	2.0

Date: Thursday, September 03, 2015 Sheet 81 of 96

+1.0VSUS POWER SUPPLY



+1VO	
TDC	:6.37A
Frequency	:500KHz
PWR Cap.	:110uF

<Variant Name>

PEGATRON Title : POWER_+1.0VSUS

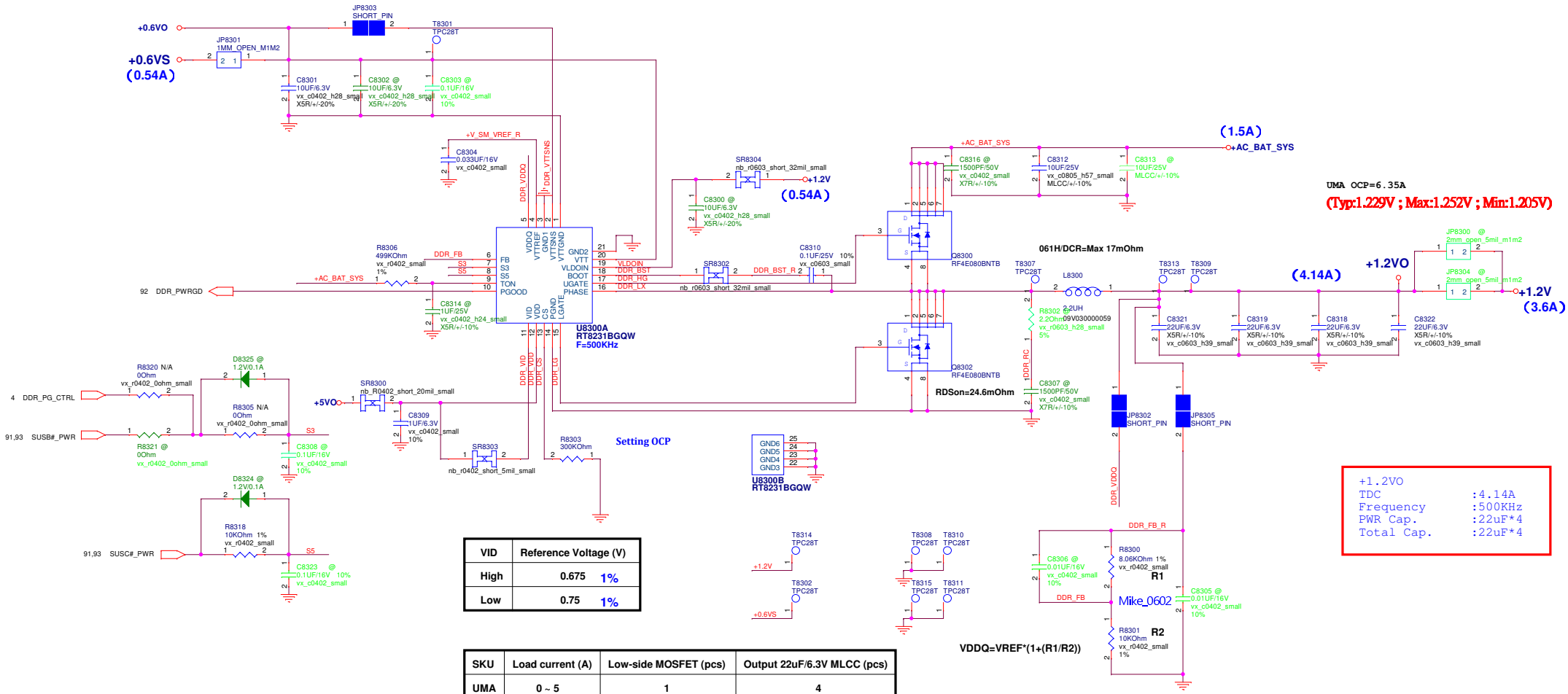
PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: Mike_Ke

Size	Project Name	Rev
Custom	P3HCJ	2.0

Date: Thursday, September 03, 2015 Sheet 82 of 96

DDR & VTT POWER SUPPLY

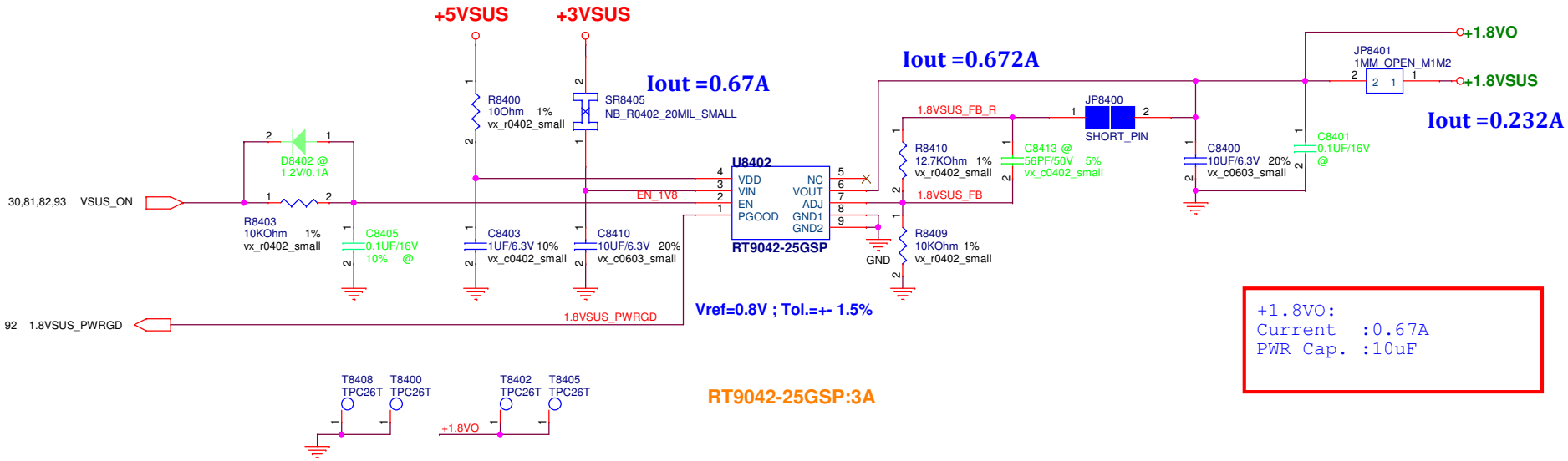


VID	Reference Voltage (V)
High	0.675 1%
Low	0.75 1%

SKU	Load current (A)	Low-side MOSFET (pcs)	Output 22uF/6.3V MLCC (pcs)
UMA	0 ~ 5	1	4
DSC	0 ~ 8	2	5

PEGATRON Title : POWER_DDR & VTT
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer: Mike_Ke
Size Custom | Project Name P3HCJ | Rev 2.0
Date: Thursday, September 03, 2015 Sheet 83 of 96

1.8VSUS POWER SUPPLY



<Variant Name>

PEGATRON Title : PAGE 84 POWER

PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: Mike_Ke

Size	Project Name	Rev
B	P3HCJ	2.0

Date: Thursday, September 03, 2015 Sheet 84 of 96

BQ24717_NVDC BATTERY CHARGER

Adapter :2.37A/19V/(45W)

RDSON:
Id:8.8A
Typ:14.2m ohm
Max:17.5m ohm
H:2mm

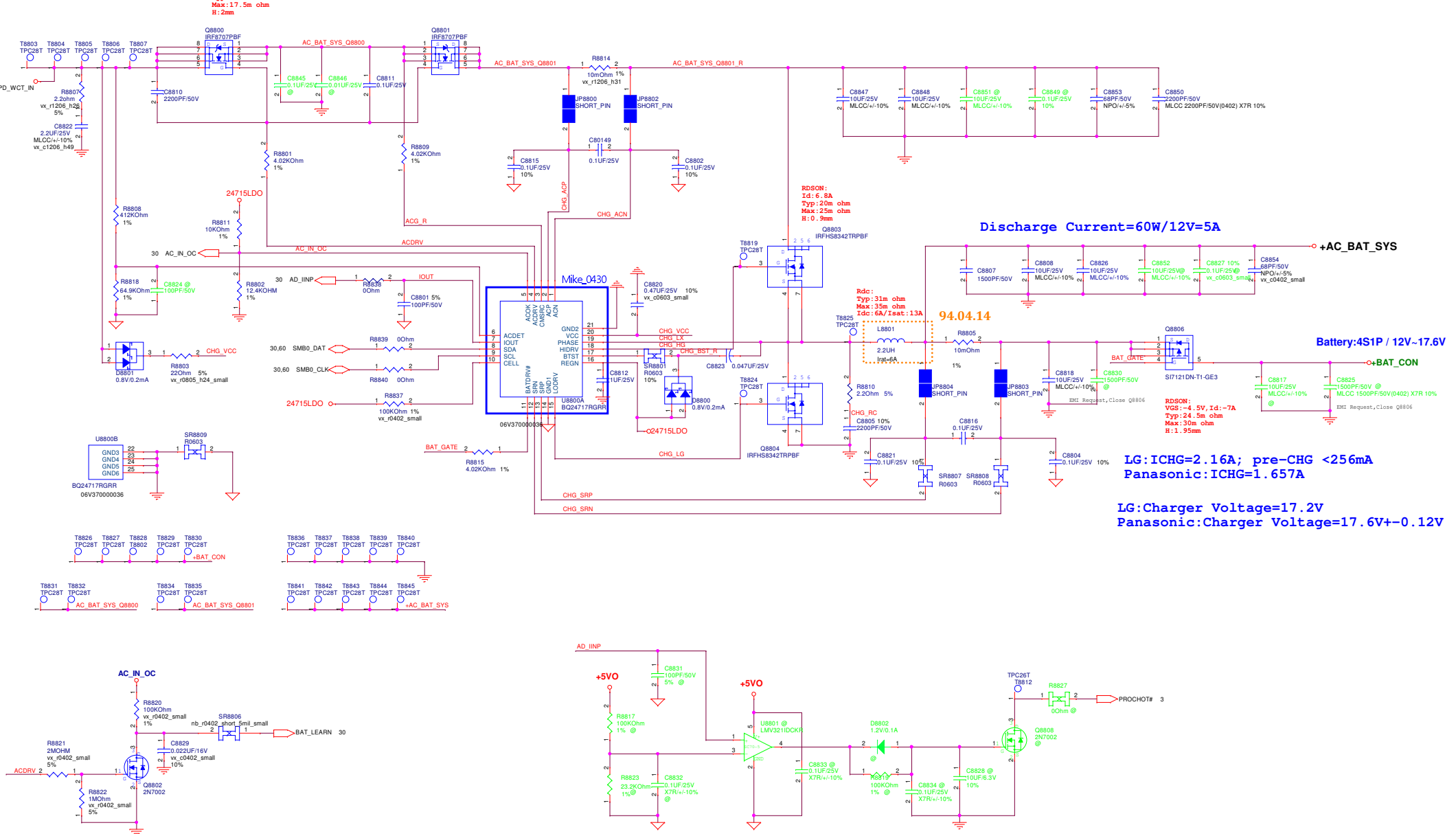
Discharge Current=60W/12V=5A

Battery:4S1P / 12V~17.6V

94.04.14

LG:ICHG=2.16A; pre-CHG <256mA
Panasonic:ICHG=1.657A

LG:Charger Voltage=17.2V
Panasonic:Charger Voltage=17.6V+-0.12V



<Variant Name>

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : POWER_CHARGER

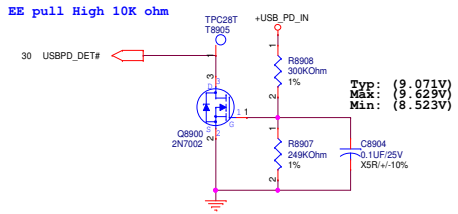
Engineer: Mike_Ke

Size	Project Name	Rev
Custom	P3HCJ	2.0

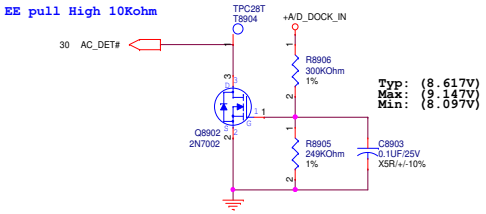
Date: Thursday, September 03, 2015 Sheet 88 of 96

AC & USB_PD & Wireless Charger Detect

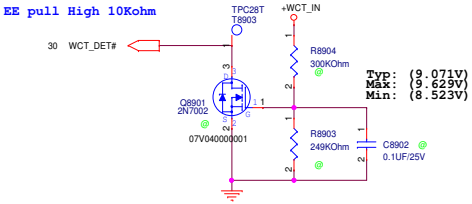
+USB PD_IN DETECT 45W(5V-20V)



+AC_IN DETECT(45W,19V)



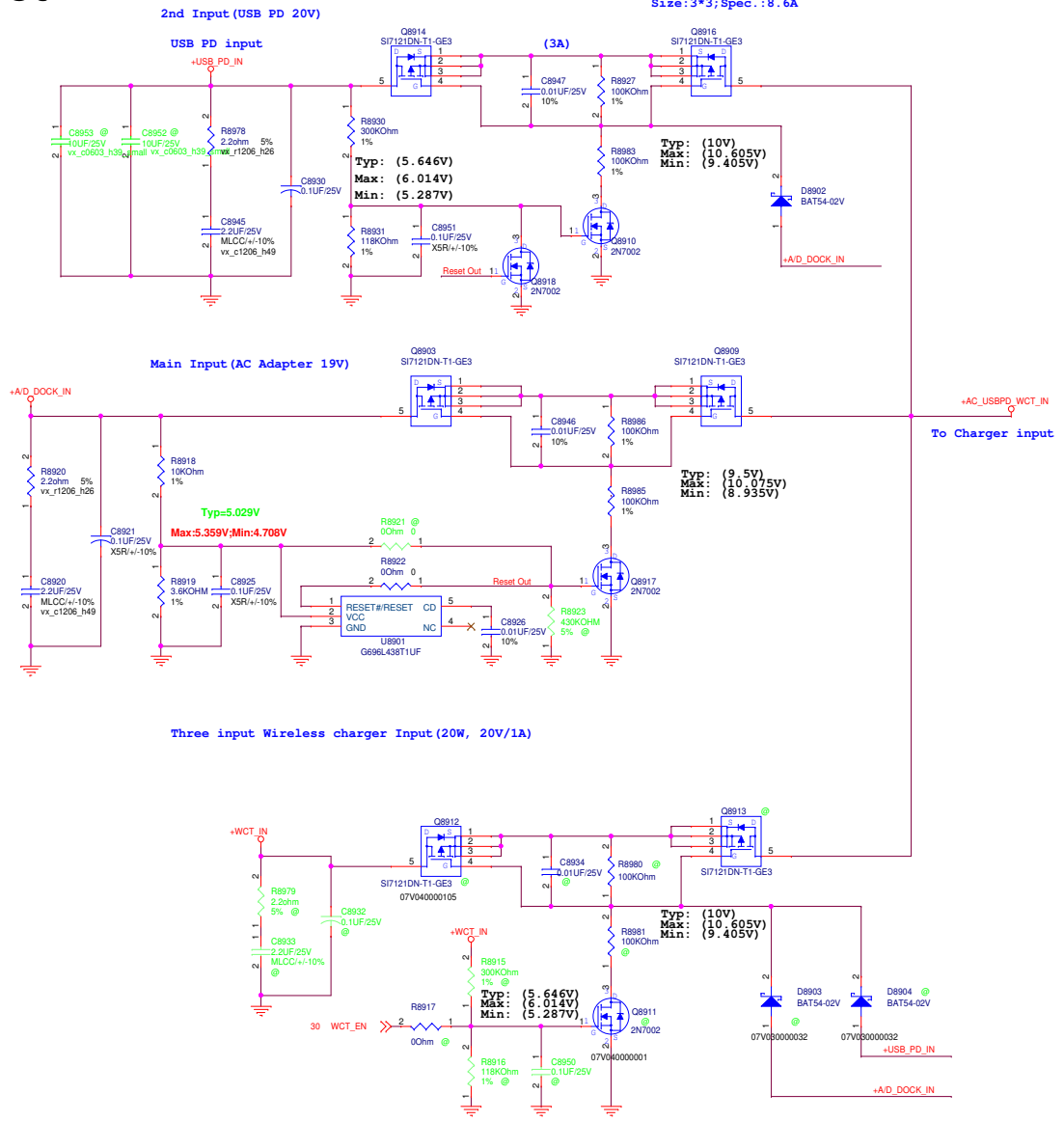
+Wireless charger_IN DETECT(20W, 20V/1A)



USBPD_DET#	AC_DET#	WCT_DET#	WCT_EN	BQ24715 Charger EN DAT&CLK	DPM	Power Limit
0	0	0	L	H	AC_Adapter	45W*90%
0	0	1	L	H	AC_Adapter	45W*90%
0	1	0	L	H	USB_PD	45W*90%??
0	1	1	L	H	USB_PD	45W*90%??
1	0	0	L	H	AC_Adapter	45W*90%
1	0	1	L	H	AC_Adapter	45W*90%
1	1	0	H	H	WCT	20W*90%
1	1	1	X	X	X	X

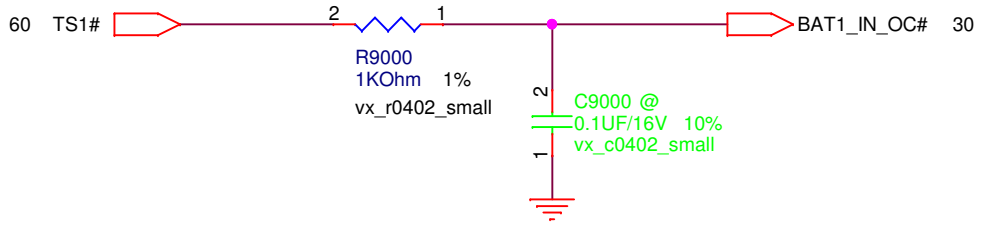
3 Input Switch Circuit

Size:3*3;Spec.:8.6A



PEGATRON Title : AC&PD&Wireless S.W.
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer: Mike_Ke
Size C | Project Name P3HCJ | Rev 2.0
Date: Thursday, September 03, 2015 | Sheet 89 of 96

BATTERY IN DETECT



<Variant Name>

PEGATRON

Title : POWER_DETECT

Engineer: Mike_Ke

Size	Project Name	Rev
A	P3HCJ	2.0

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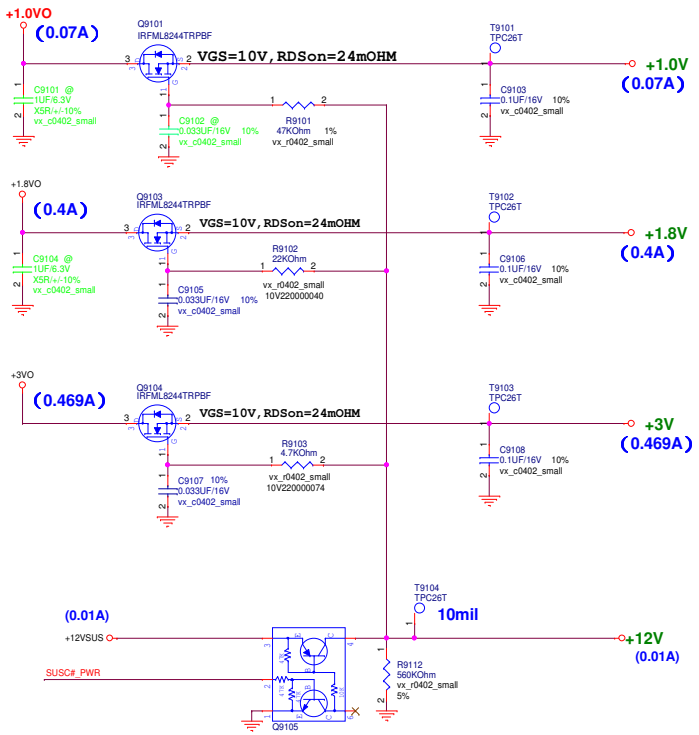
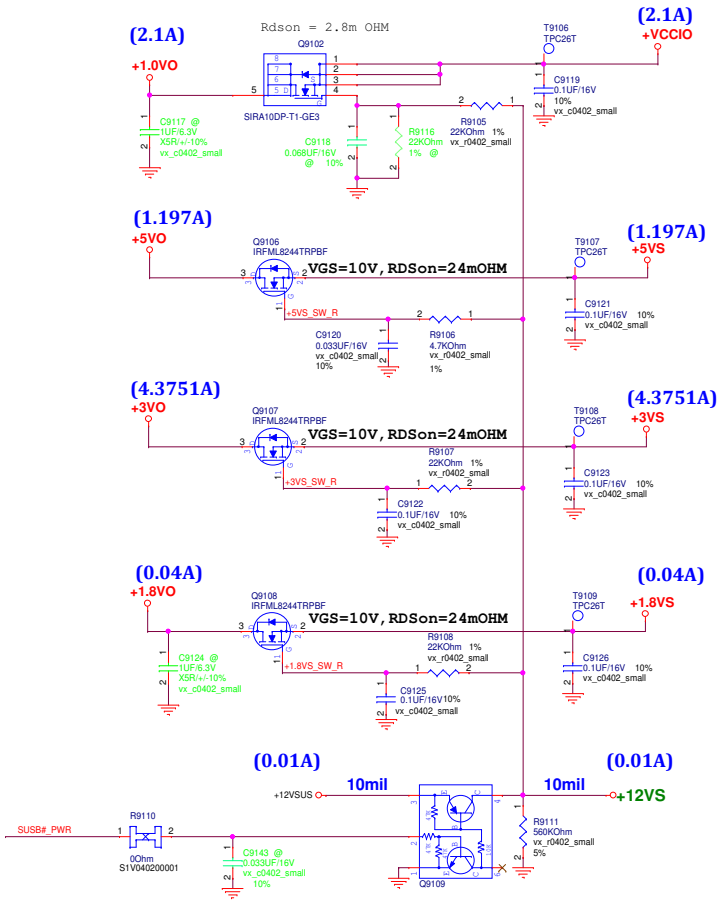
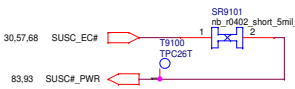
SUSC#_PWR POWER



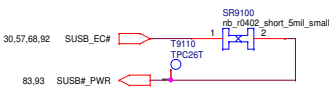
SUSB#_PWR POWER



SUSC#_PWR POWER Control



SUSB#_PWR POWER Control



<Variant Name>

PEGATRON Title : POWER_LOAD SWITCH

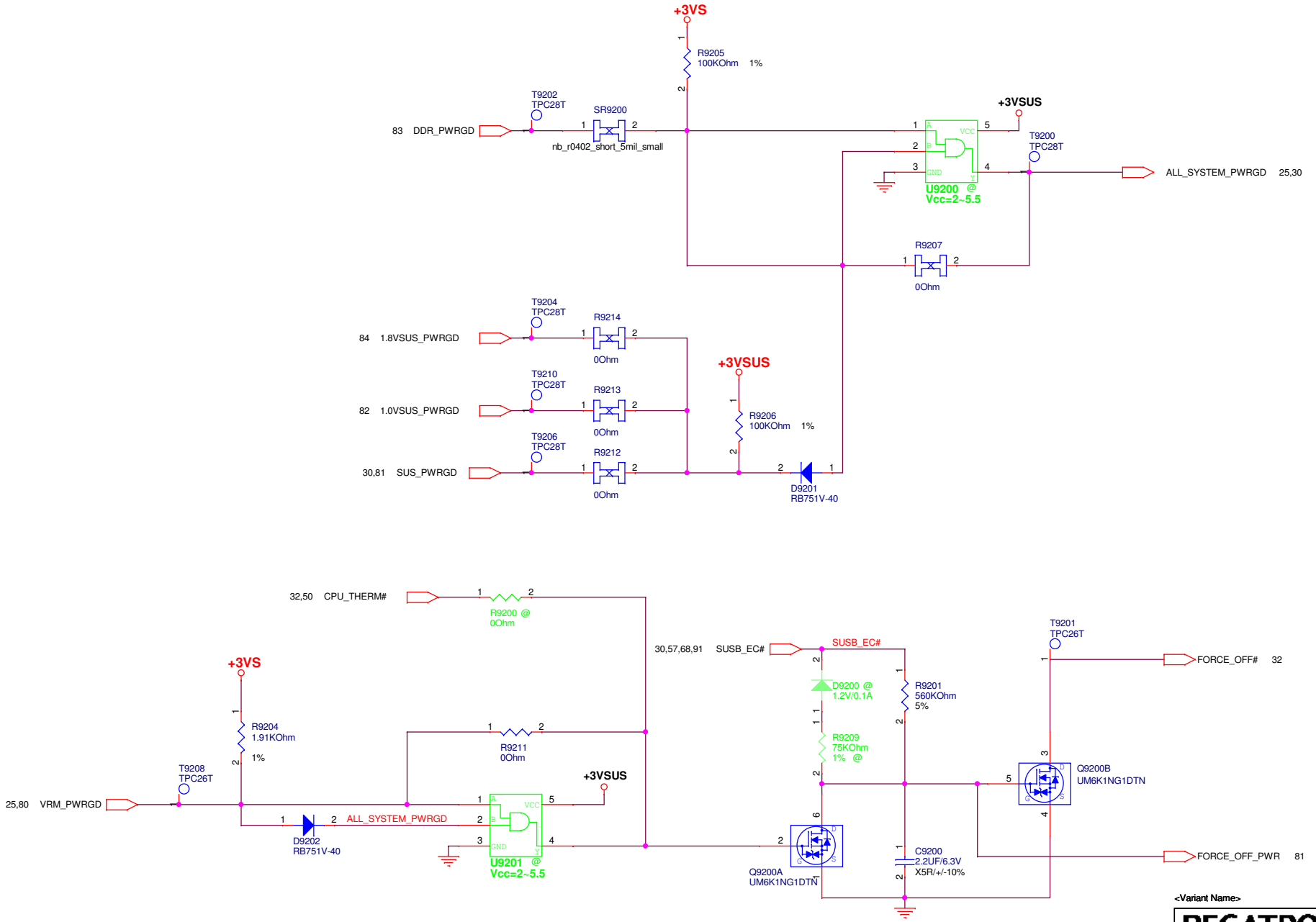
PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: Mike_Ke

Size	Project Name	Rev
C	P3HCJ	2.0

Date: Thursday, September 03, 2015 Sheet 91 of 96

POWER GOOD DETECTER



<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : POWER_PROTECT

Engineer: Mike_Ke

Size	Project Name	Rev
Custom	P3HCJ	2.0

Date: Thursday, September 03, 2015 Sheet 92 of 96

+A/D_DOCK_IN → +A/D_DOCK_IN 60,89

+AC_BAT_SYS → +AC_BAT_SYS 45,80,81,82,83,88

+BAT_CON → +BAT_CON 60,88

+BAT → +BAT

+5VA → +5VA 64,81

+3VA → +3VA 21,24,30,31,36,53,57,60,64,69,81

+5VO → +5VO 81,83,88,91

+3VO → +3VO 81,91

+1.8VO → +1.8VO 84,91

+1.2VO → +1.2VO 83

+1.0VO → +1.0VO 82,91

+0.6VO → +0.6VO 83

+12VSUS → +12VSUS 28,81,91

+5VSUS → +5VSUS 13,52,64,81,84

+3VSUS → +3VSUS 4,12,13,21,24,25,26,28,30,31,53,62,64,68,81,84,92

+3V → +3V 25,31,53,57,58,64,91

+1.2V → +1.2V 4,7,16,17,18,57,83

+12VS → +12VS 28,31,48,50,57,91

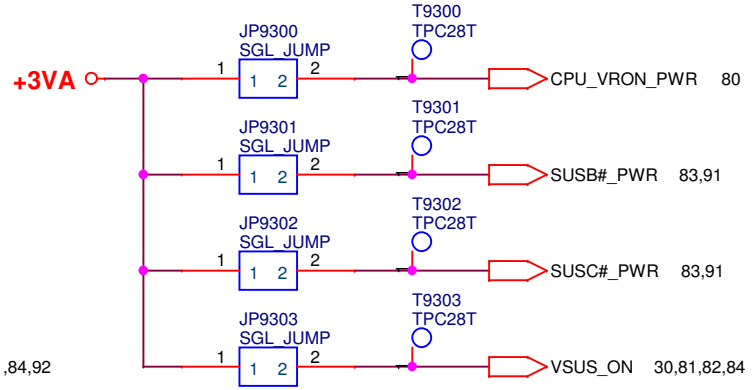
+5VS → +5VS 31,36,48,50,57,64,80,91

+3VS → +3VS 3,4,12,20,21,22,23,24,28,30,31,32,36,44,45,48,50,51,53,57,58,62,64,91,92

+0.6VS → +0.6VS 16,17,57,83

+VCORE → +VCORE 5,80

FOR POWER TEST



<Variant Name>

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : POWER_SIGNAL

Engineer: Mike_Ke

Size	Project Name	Rev
Custom	P3HCJ	2.0

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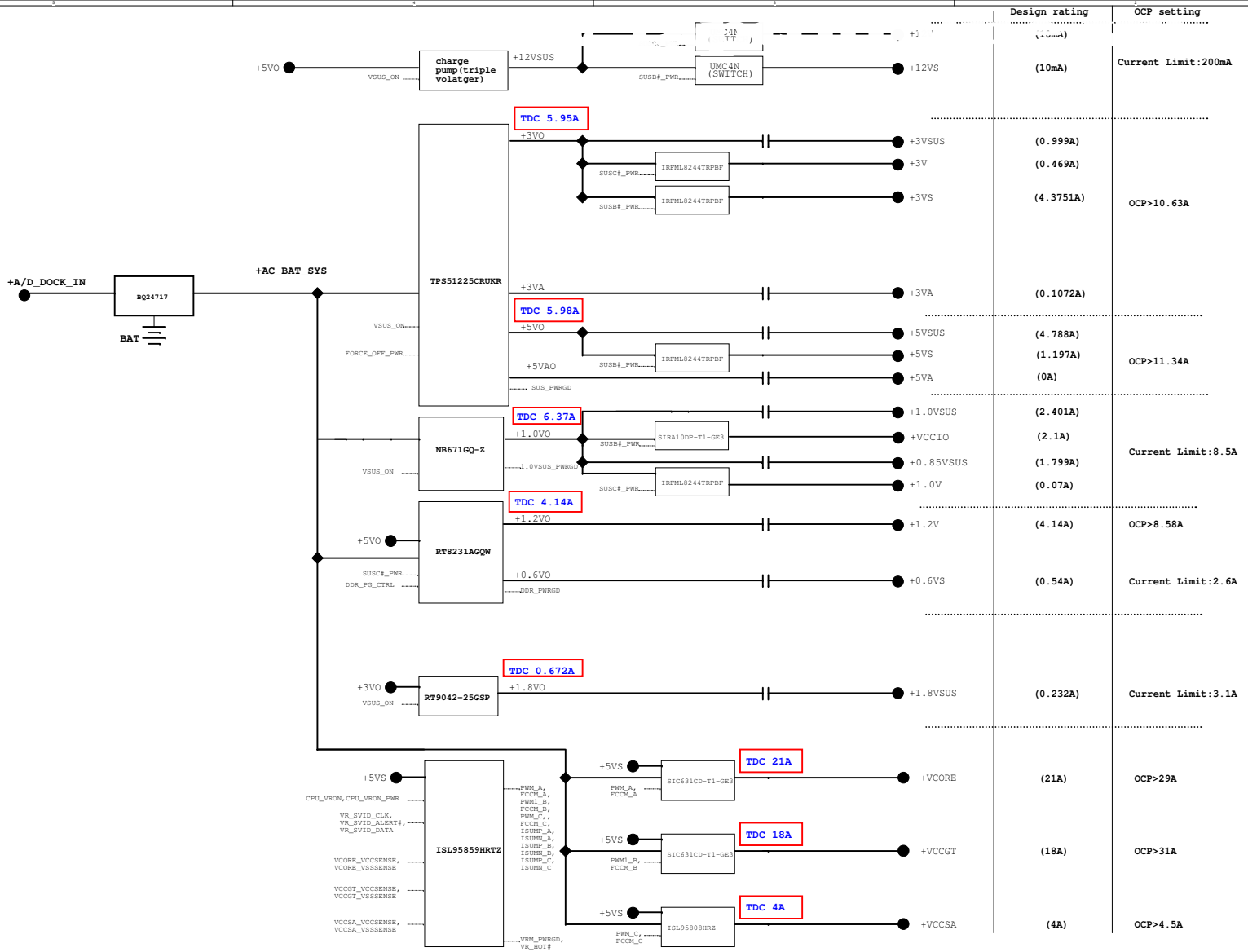


<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title: POWER_FLOWCHART

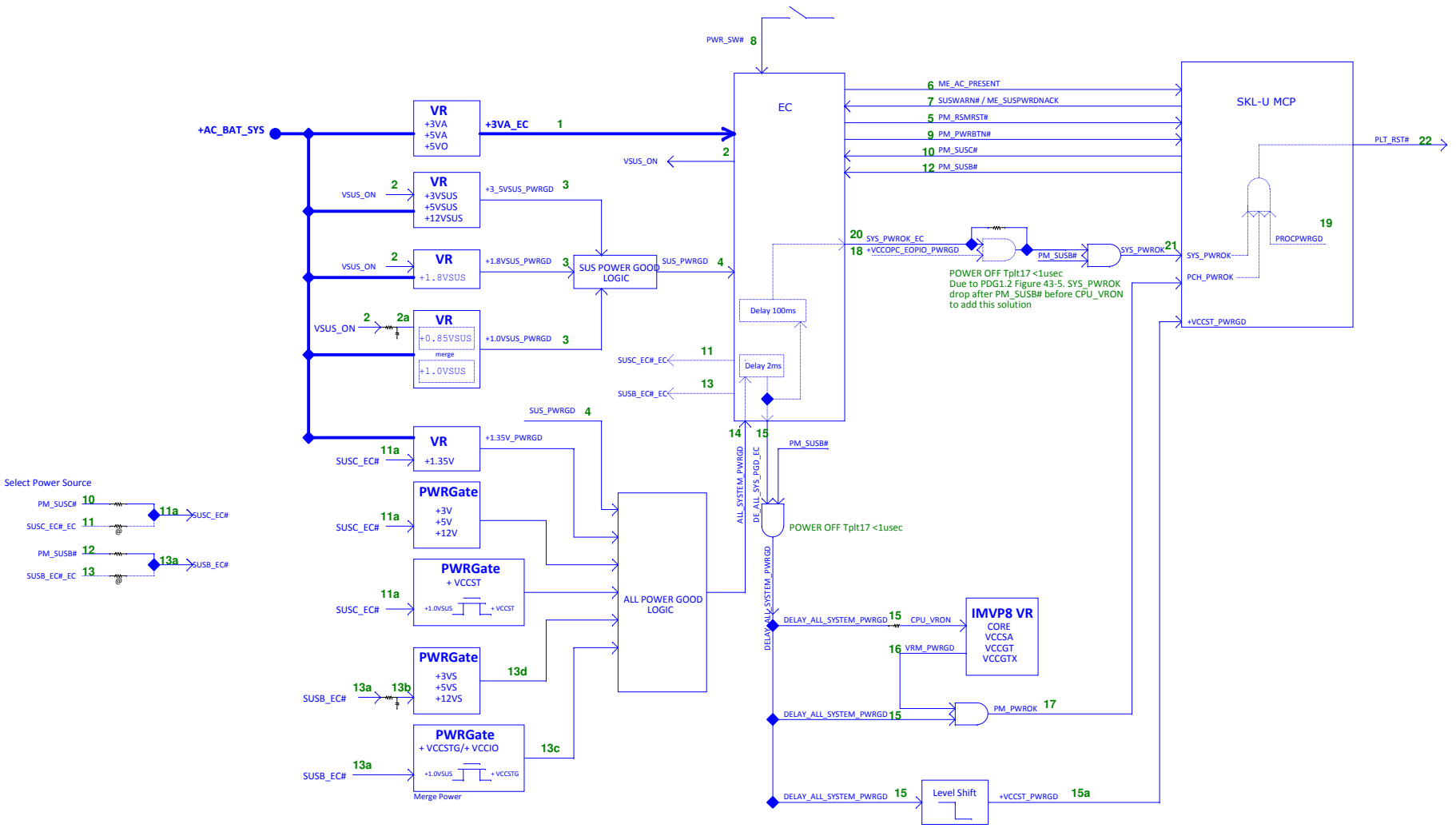
Engineer: Mike_Ke

Size	Project Name	Rev
D	P3HCJ	2.0

Date: Thursday, September 03, 2015 Sheet 94 of 96

Power On Sequence Diagram G3-S0 R0.1 (non-Deep Sx)

Power On Sequence
1 → 22



PEGATRON
Title : Power On Sequence
Engineer: Dep.3-Sec.3
Project Name: P3HCJ
Size: D
Rev: 2.0
Date: Thursday, September 03, 2015
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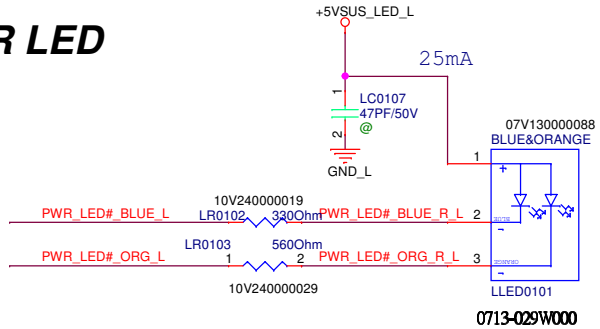
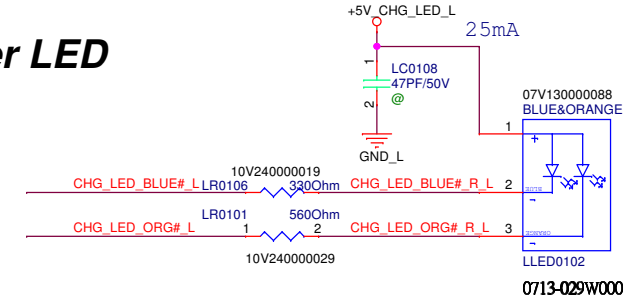
POWER LED



0713-029W000

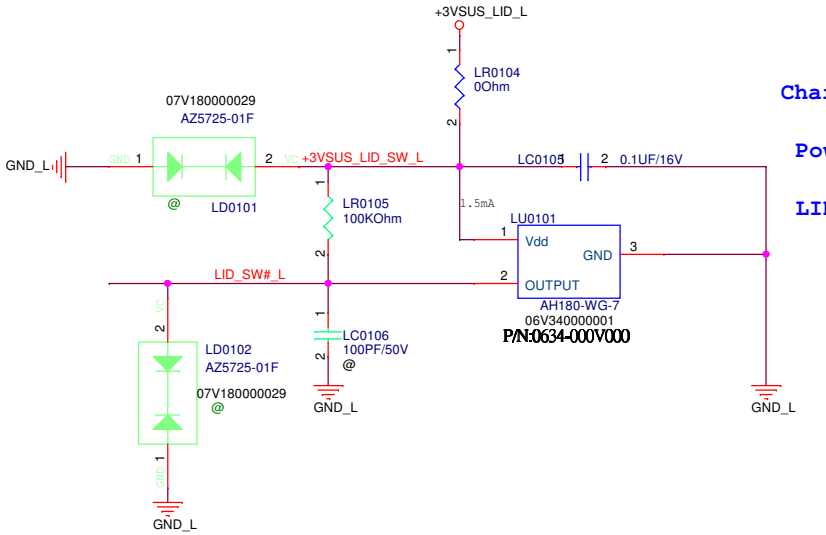
Charger LED



0713-029W000

Acer spec of power & charge LED: Blue/Orange

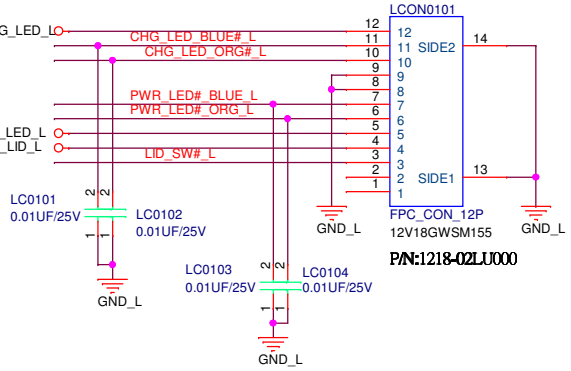
LID Switch



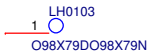
Charge LED

Power LED

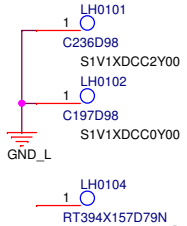
LID SWITCH



TOOLING HOLE



SCREW HOLE



MB Connector Pin Define

	P3HCJ/P4HCJ
1	+5VA_CHGLED
2	CHG_BLUE_LED#
3	CHG_ORG_LED#
4	GND
5	GND
6	PWR_BLUE_LED#
7	PWR_ORG_LED#
8	+5VSUS_PWRLED
9	+3VSUS_HALL
10	LID_SW#_13_KB
11	NC
12	NC

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : LED Board

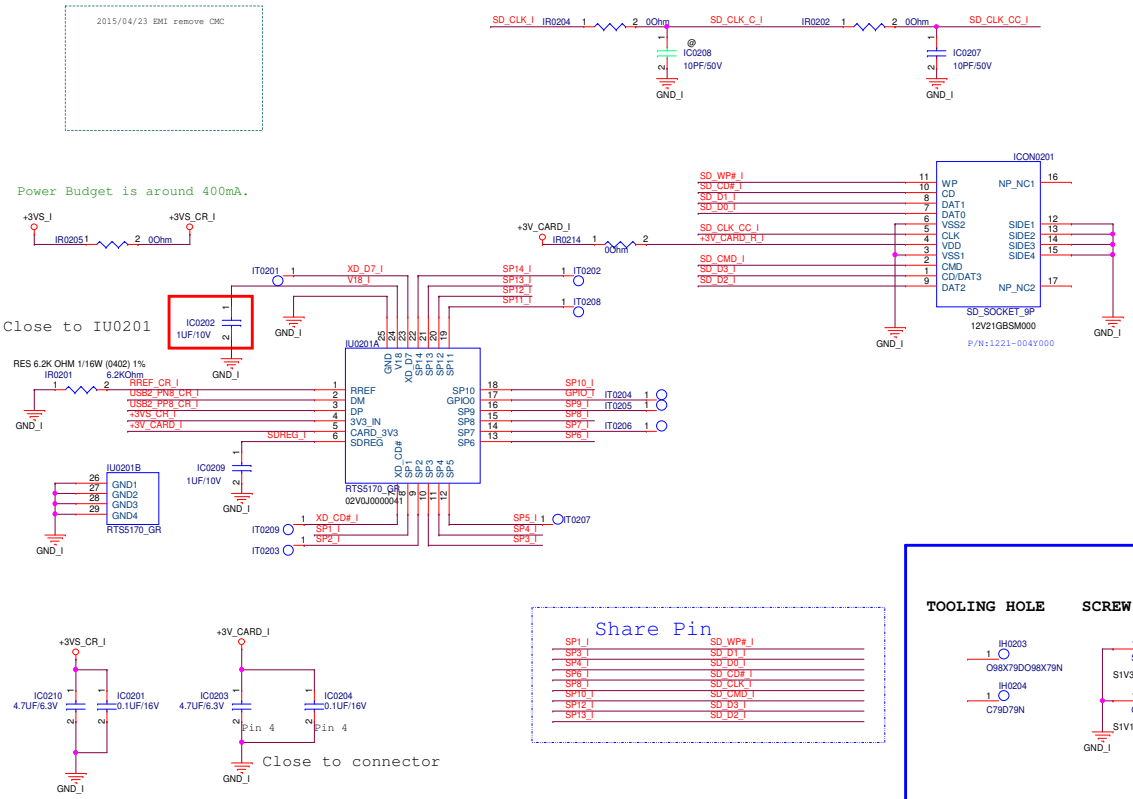
BG1/HW2

Engineer: Ricky Lee

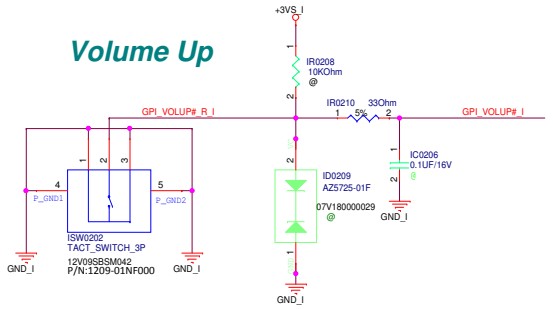
Size	Project Name	Rev
B	P3HCJ	1.0

Date: Thursday, September 03, 2015 Sheet 101 of 110

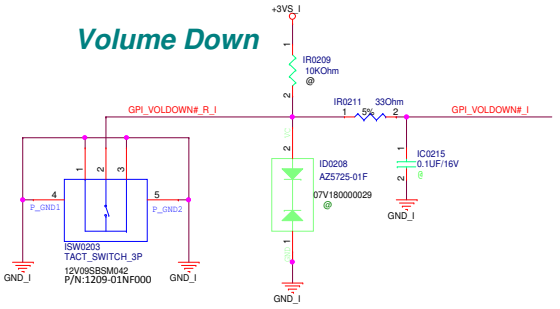
Card Reader



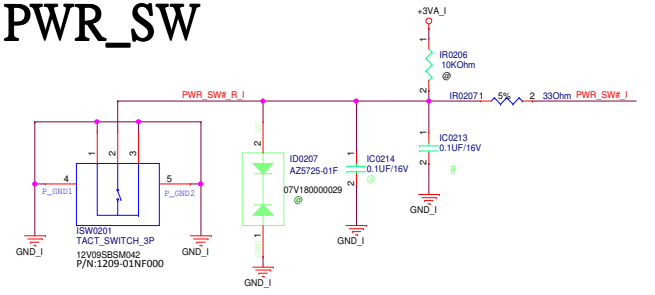
Volume Up



Volume Down



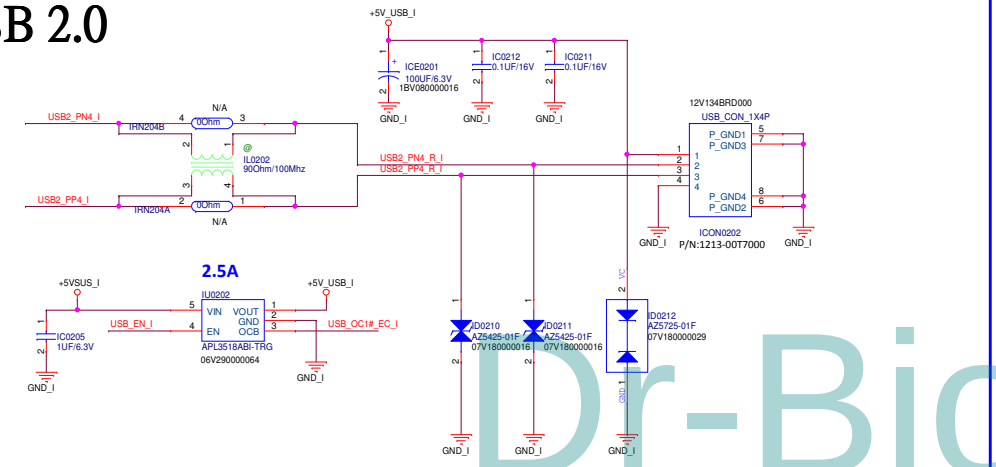
PWR_SW



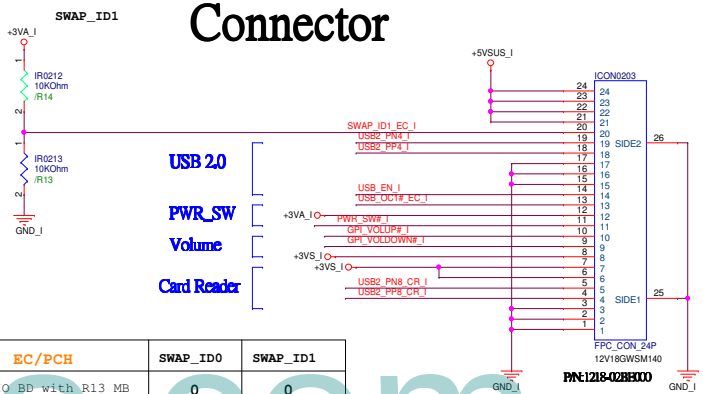
TOOLING HOLE

SCREW HOLE

USB 2.0



Connector



MB Connector Pin Define

	P3HCJ/P4HCJ
1	+5VSUS
2	+5VSUS
3	+5VSUS
4	+5VSUS
5	SWAP_ID1
6	USB_PN4_20
7	USB_PP4_20_R
8	GND
9	GND
10	GND
11	USBP01_EN
12	USB_OC7#_PCH
13	+3VA
14	PWR_SW#
15	VOL_UP#
16	VOL_DOWN#
17	+3VS
18	+3VS_CR
19	+3VS_CR
20	USB_PN8_CR
21	USB_PP8_CR
22	GND
23	GND
24	GND

EC/PCH	SWAP_ID0	SWAP_ID1
R13 IO BD with R13 MB	0	0
R13 IO BD with R14 MB	0	1
R14 IO BD with R13 MB	1	0
R14 IO BD with R14 MB	1	1

PEGATRON Title : IO Board

PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: HW2

BG1/HW2

Size	Project Name	Rev
C	P3HCJ	1.0

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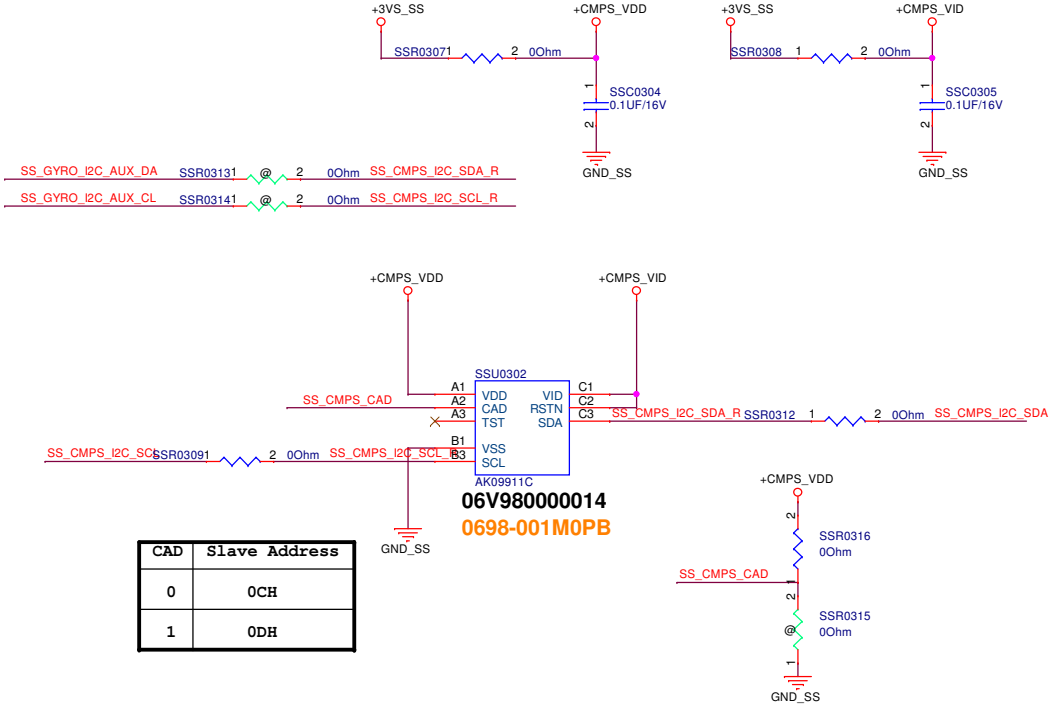
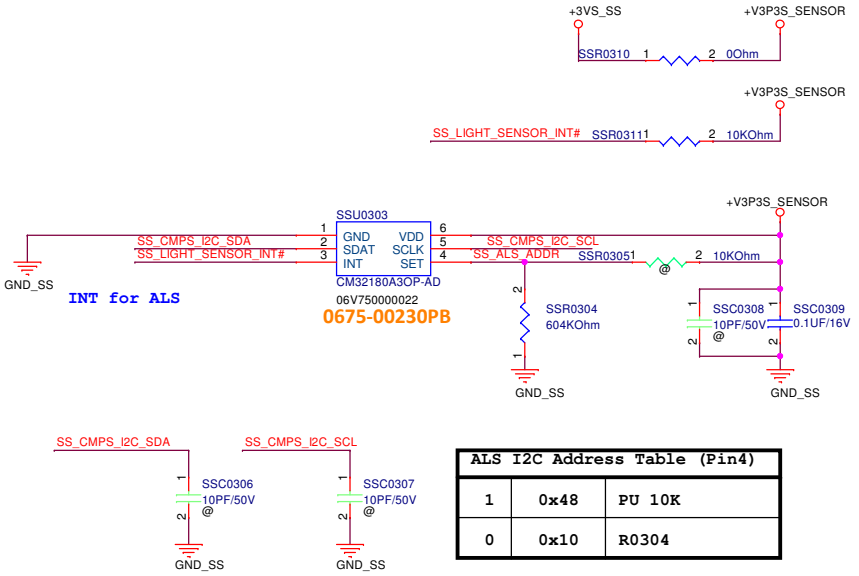
e-Compass



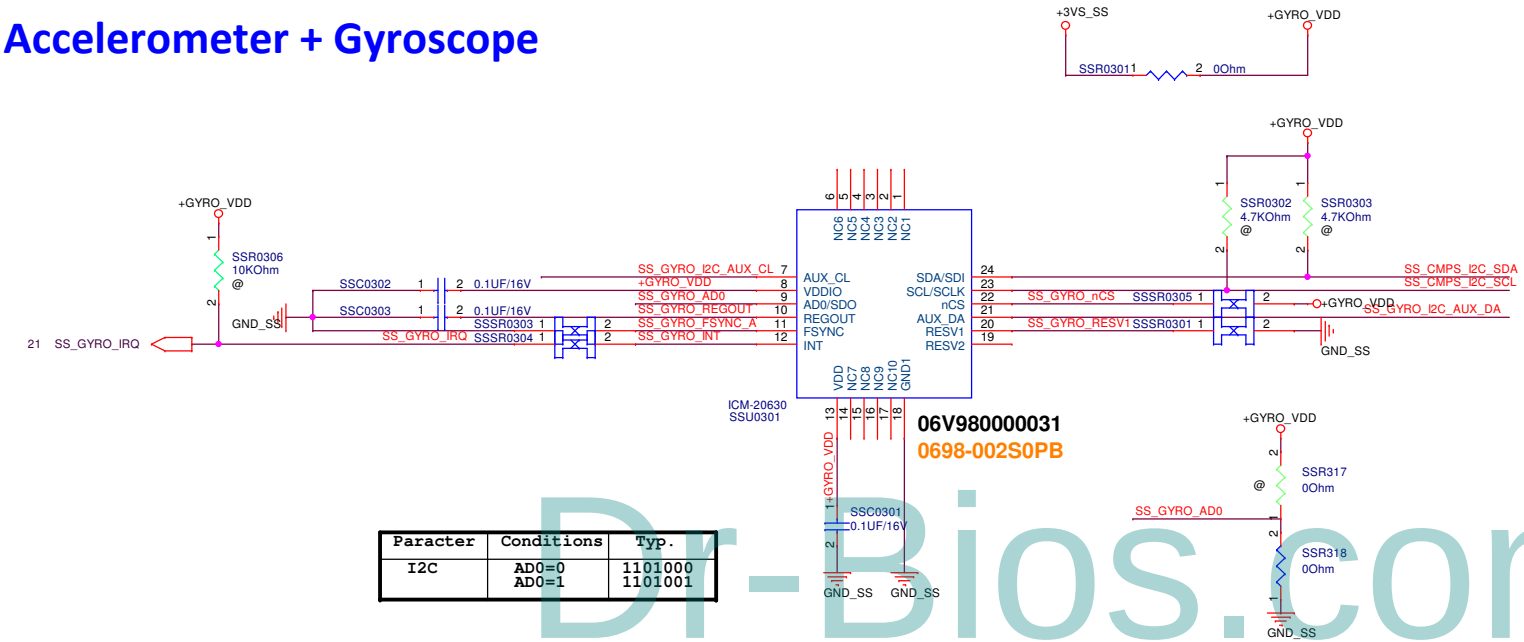
CAD	Slave Address
0	0CH
1	0DH

Light Sensor

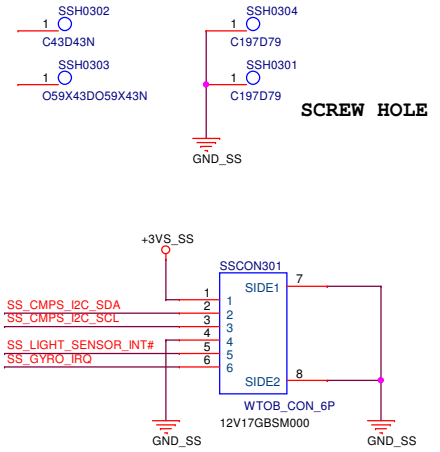


ALS I2C Address Table (Pin4)		
1	0x48	PU 10K
0	0x10	R0304

Accelerometer + Gyroscope



Paracter	Conditions	Typ.
I2C	AD0=0 AD0=1	1101000 1101001



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : Sensor Board

BG1/HW2

Engineer: Hank Zheng

Size	Project Name	Rev
A3	P3HCJ	1.0

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