JV10-NL Block Diagram

Project code: 91.4HX01.001
PCB P/N : 48.4HX01.0SB
REVISION : SB

Clock Generator
ICS9LPRS480BKLFT 3

DDRIII 800 Slot 0 18
DDRIII 800 Slot 1 17
DDRIII Channel A
DDRIII Channel B

AMD
ASB2 CPU 4,5,6,7

OUT
IN
HyperTransport
LINK0
16x16

FRAME BUFFER
DRR3 1GMBIT 10
Side port

RS880M
HyperTransport LINK0 CPU I/F
DX10 IGP
LVDS/TVOUT/TMDS
DISPLAY PORT X2
Side Port Memory
1 X16 PCIE I/F
1 X4 PCIE I/F WITH SB
6 X1 PCIE I/F
8,9,10,11

RGB CRT
CRT 20
LVDS 2CH
LCD
WXGA+ 19
Digital Display
HDMI 21

RJ45
CONN 24
MDI
Giga LAN
AR8151 23
PCIE

PCIE
Mini-Card
WLAN & 3G 26
PCIE+USB 2.0
USB 2.0

A-Link
4X4

SB800
USB2.0 (14)+1.1(2)
SATA III (6 PORTS)
4 X1 PCIE GEN2 I/F
INT. CLK GEN.
GB MAC
HW MONITOR
PCI/PCI BDGE
INT. RTC
EC
HD AUDIO
LPC I/F
SPI I/F
ACPI 1.1 12,13,14,15,16

WEBCAM 19
BLUETOOTH 31
USB 2.0
USB x 3 31

Card Reader
RTS 5138 25
SD/MMC
MS/MS Pro/xD 25

SATA
SATA HDD 31

MIC IN
INT MIC
HD AUDIO
CODEC
ALC271 22
AZALIA

LINE OUT
2CH SPEAKER

LPC Bus
LPC debug 30

KBC
NPCE781B 29

CPU FAN
SPI
SMB
PS/2
KBC

Flash ROM
2MB 30
Thermal
Sensor
G792 28
Touch
PAD 31
Int.
KB 29

PCB STACKUP

TOP	
GND	
S	
S	
GND	
BOTTOM	

SYSTEM DC/DC RT8223 34	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(6A)

SYSTEM DC/DC RT8209E 35	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3(7.5A)

SYSTEM DC/DC RT8209E 36	
INPUTS	OUTPUTS
DCBATOUT	1D1V_S0(11A)

RT9026 35	
5V_S5	DDR_VREF_S3

RT9025 37	
3D3V_S5	1D1V_S5

RT9025 37	
3D3V_S5	CPU_VDDR

CHARGER ISL88731A 38	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A UP+5V 5V 100mA

CPU DC/DC ISL6265AHR 33	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0_0 0~1.55V 18A VCC_CORE_S0_1 0~1.55V 18A VDDNB 0~1.55V 18A

SJV10-NL

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Title: Block Diagram

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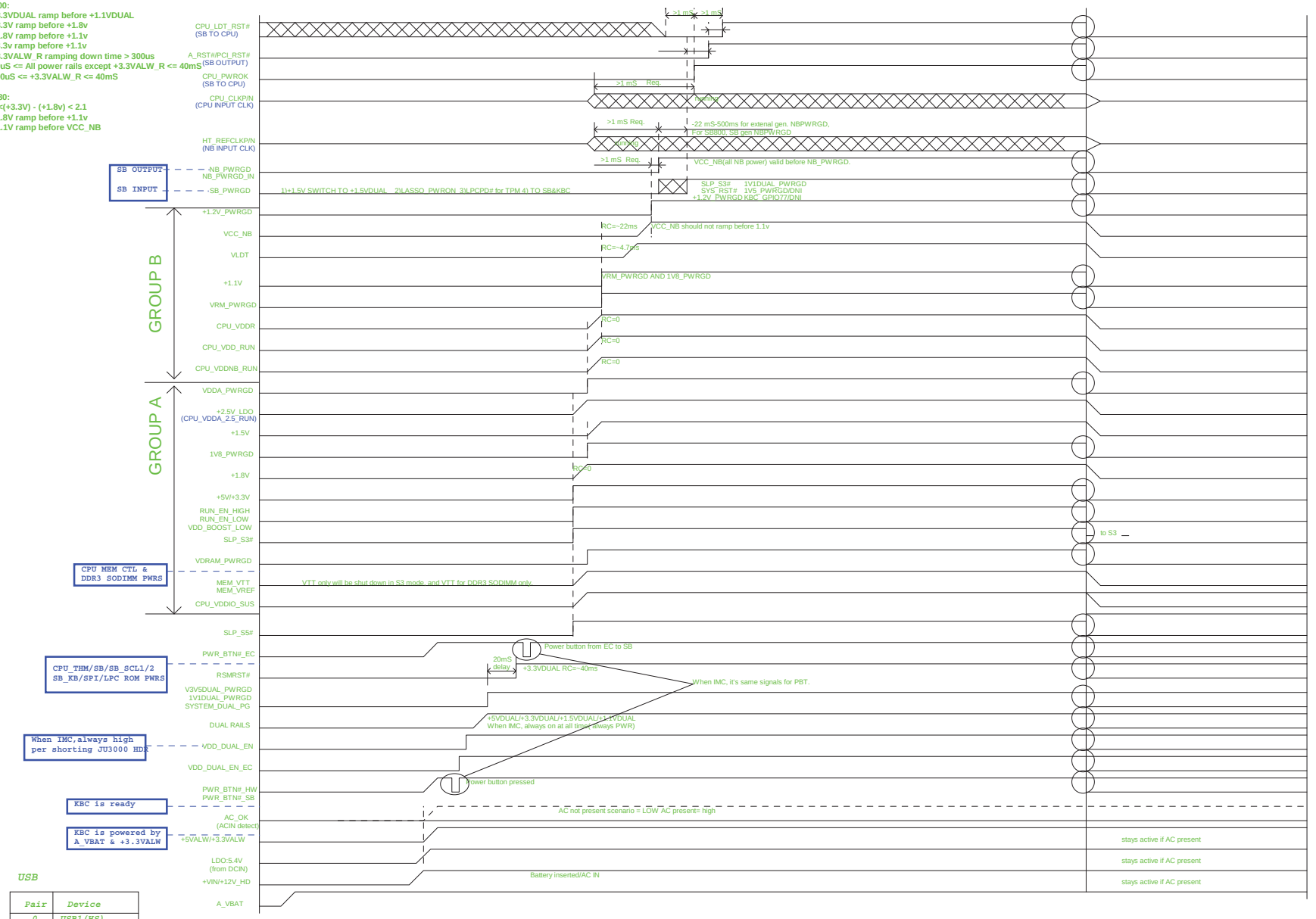
Date: Tuesday, January 05, 2010 Sheet 1 of 42

Power on Sequence required:

SB800:
1, +3.3VDUAL ramp before +1.1VDUAL
2, +3.3V ramp before +1.8v
3, +1.8V ramp before +1.1v
4, +3.3v ramp before +1.1v
5, +3.3VALW_R ramping down time > 300us
6, 50uS <= All power rails except +3.3VALW_R <= 40mS
7, 100uS <= +3.3VALW_R <= 40mS

RS880:
1, 0 <(+3.3V) - (+1.8v) < 2.1
2, +1.8V ramp before +1.1v
3. +1.1V ramp before VCC_NB



USB

Pair	*Device*
0	*USB1(HS)*
1	*MINICARD1*
2	*NC*
3	*NC*
4	*Cardreader*
5	*USB2*
6	*USB3*
7	*Blue Tooth*
8	*NC*
9	*WECAM*
10	*NC*
11	*MINIC2(3G sim)*
12	*MINIC2(3G)*
13	*NC*

PCIE Routing

LANE1	LAN
LANE2	MiniCard1
LANE3	MiniCard2

SJV10-NL

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Title: ***Table of Content***

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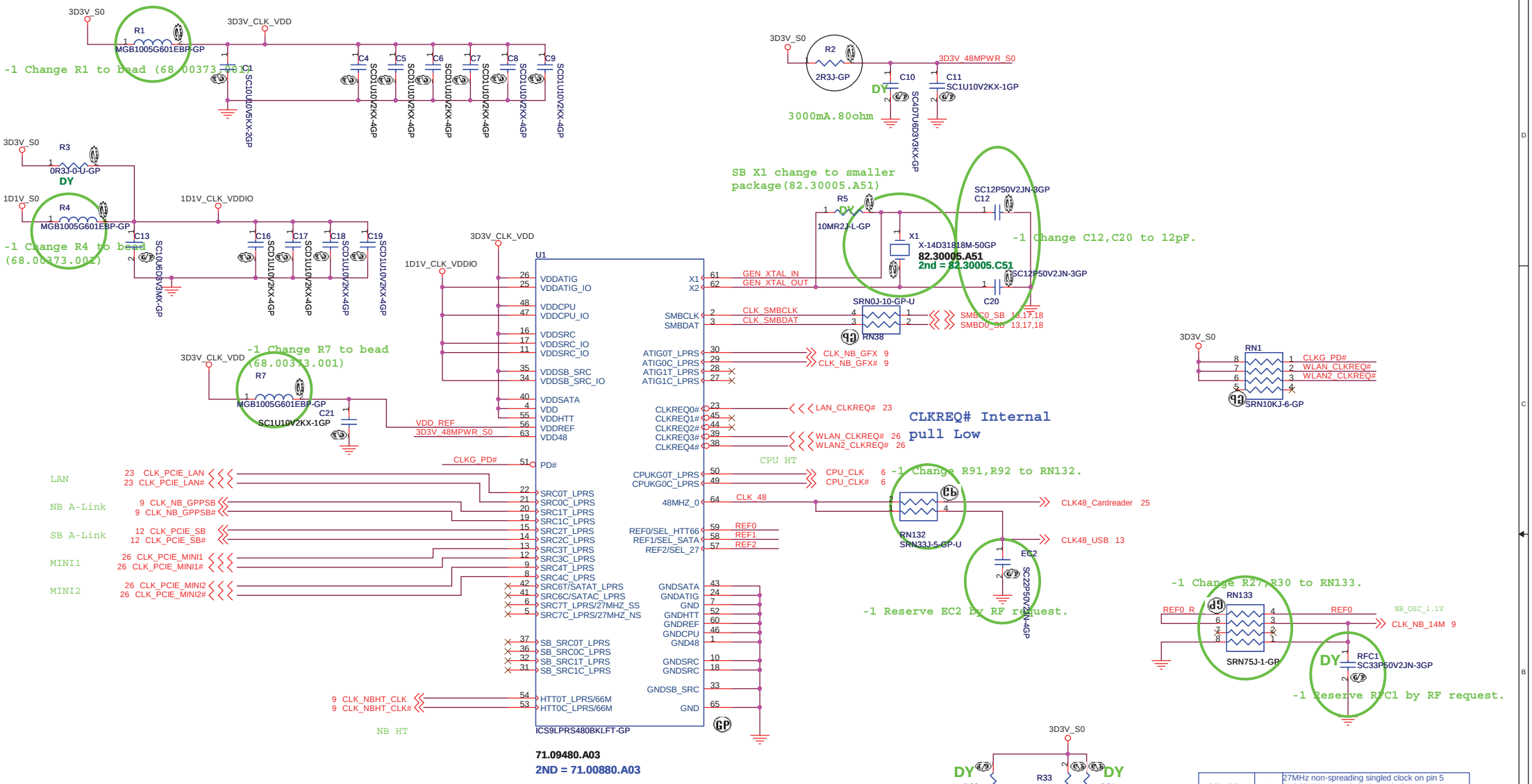

NB CLOCK INPUT TABLE

NB CLOCKS	RS880M
HT_REFCLKP	100M DIFF
HT_REFCLKN	100M DIFF
REFCLK_P	14M SE (1.1V)
REFCLK_N	vref
GFX_REFCLK	100M DIFF(IN/OUT)*
GPP_REFCLK	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF

* RS880M can be used as clock buffer to output two PCIE refererence clocks
By deault, chip will configured as input mode, BIOS can program it to output mode.

SEL_27 REF2	1	27MHz non-spreading singled clock on pin 5 and 27MHz spread clock on pin 6
	0*	100MHz differential spreading SRC clock
SEL_SATA REF1	1	100MHz non-spreading differential SATA clock
	0*	100MHz differential spreading SRC clock
SEL_HTT66 REF0	1	66MHz 3.3V single ended HTT clock
	0 *	100MHz differential HTT clock

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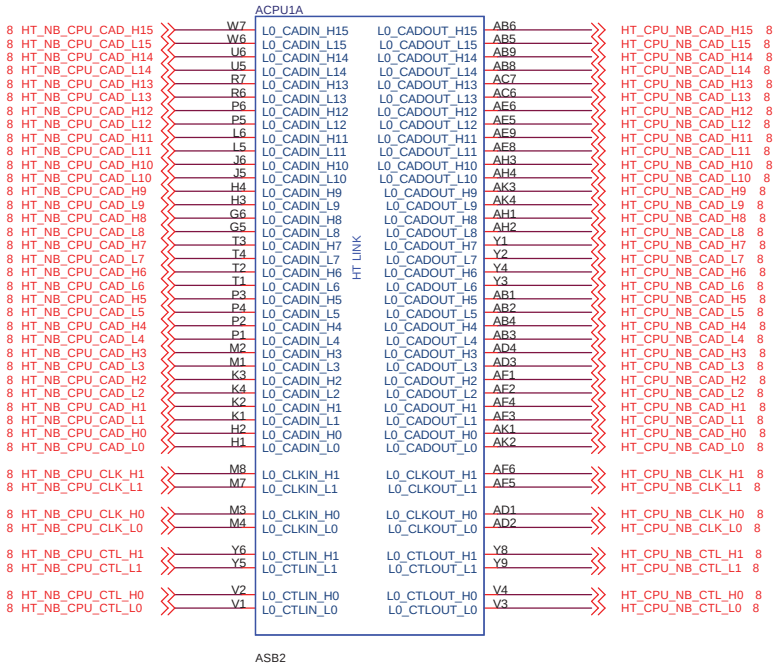
Title: CLKGEN ICS9LPRS480

Size	Document Number	Rev
A3	SJV10-NL	-1

Date: Friday, January 29, 2010 Sheet 3 of 42



71.TURON.B0U

SJV10-NL

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU_HT_LINK I/F (1/4)**

Size	Document Number	Rev
A3	SJV10-NL	-1

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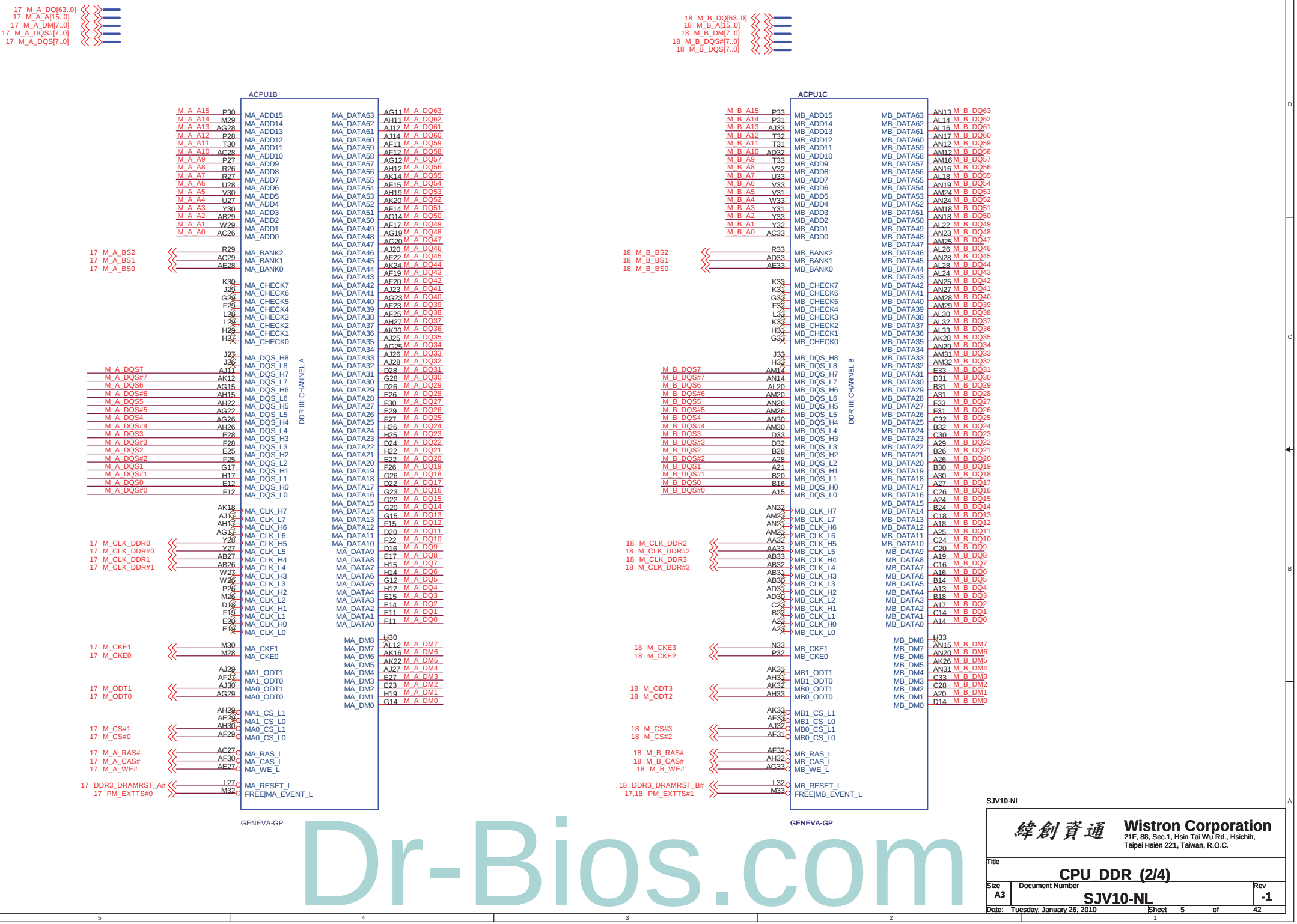

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Title: **CPU_DDR_(2/4)**

Size	Document Number	Rev
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2D5V
Iomax=0.2A

Place near to CPU
IF 0 ohm IS NOT GOOD ENOUGH, TRY 68.00082.491

LYAOUT:ROUTE VDDA TRACE APPROX.
50mils WIDE(USE 2X25 mil TRACES TO
EXIT BALL FIELD) AND 500 mils LONG.

Cloce To CPU

Route as 80ohm, diff
R value is TBD

CPU exceeds to 125℃

HDT Connectors

CPU_DBREQ#	TP109
CPU_DBRDY	TP102
CPU_TCK	TP104
CPU_TMS	TP105
CPU_TDI	TP106
CPU_TRST#	TP107
CPU_TDO	TP108

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Title: CPU_Control&Debug_(3/4)

Size: A3 | Document Number: SJV10-NL | Rev: -1

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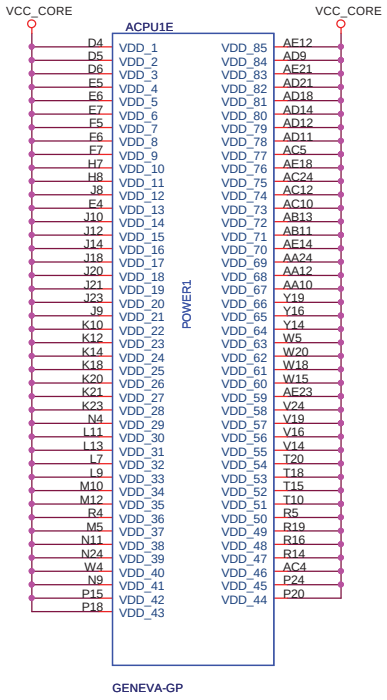
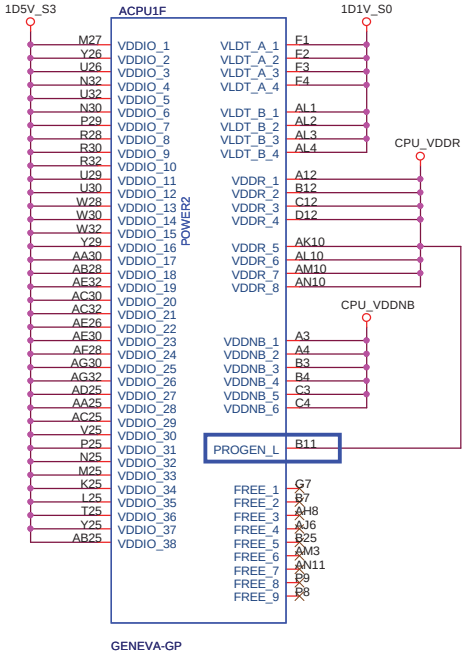
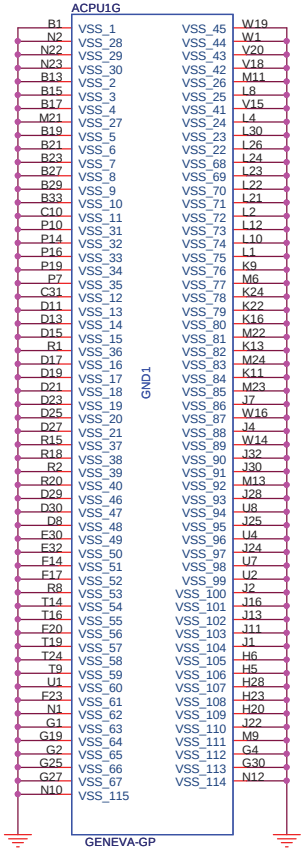
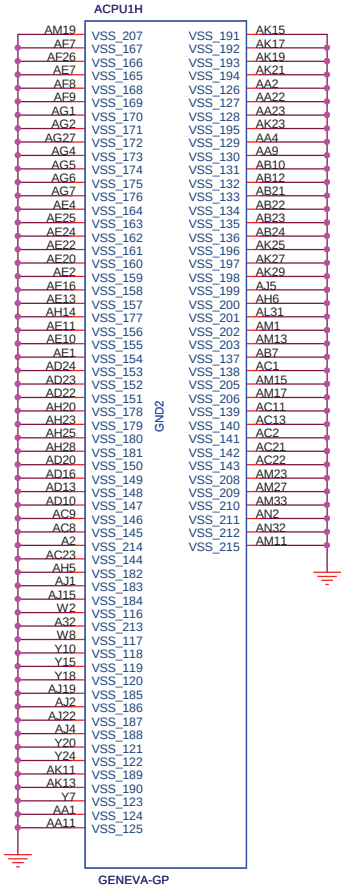
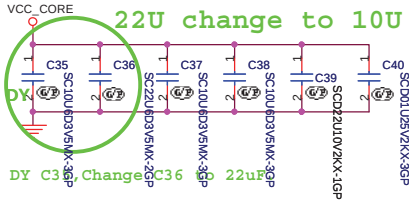


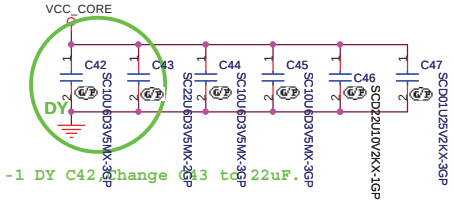




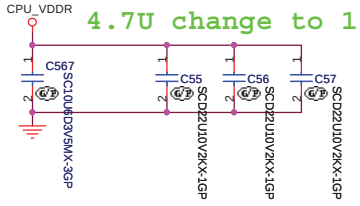


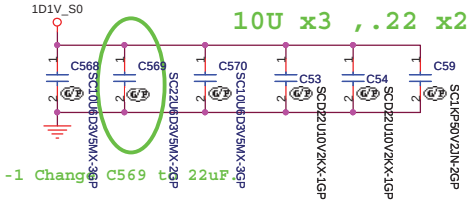
BOTTOM SIDE DECOUPLING

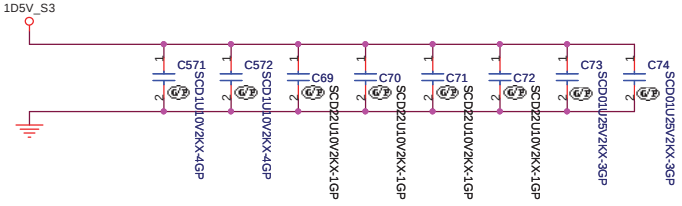




DECOUPLING betweem CPU and DIMMs
PLACE CLOSE TO CPU AS POSSIBLE

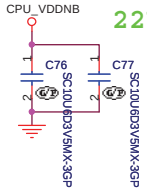


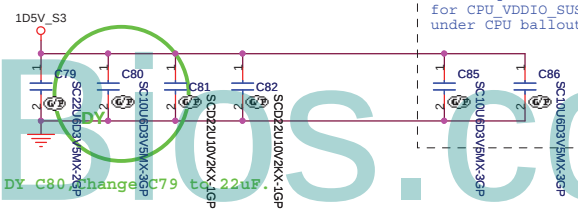




10U x4 ,.22 x5 ,.1ux2 ,.01ux1

It's required to add two 10uF/0603 size for CPU_VDDIO_SUS,move 2x180pf from under CPU ballout by Beker, Ben.





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Title: CPU_Power_(4/4)

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RS880M Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

SJV10-NL

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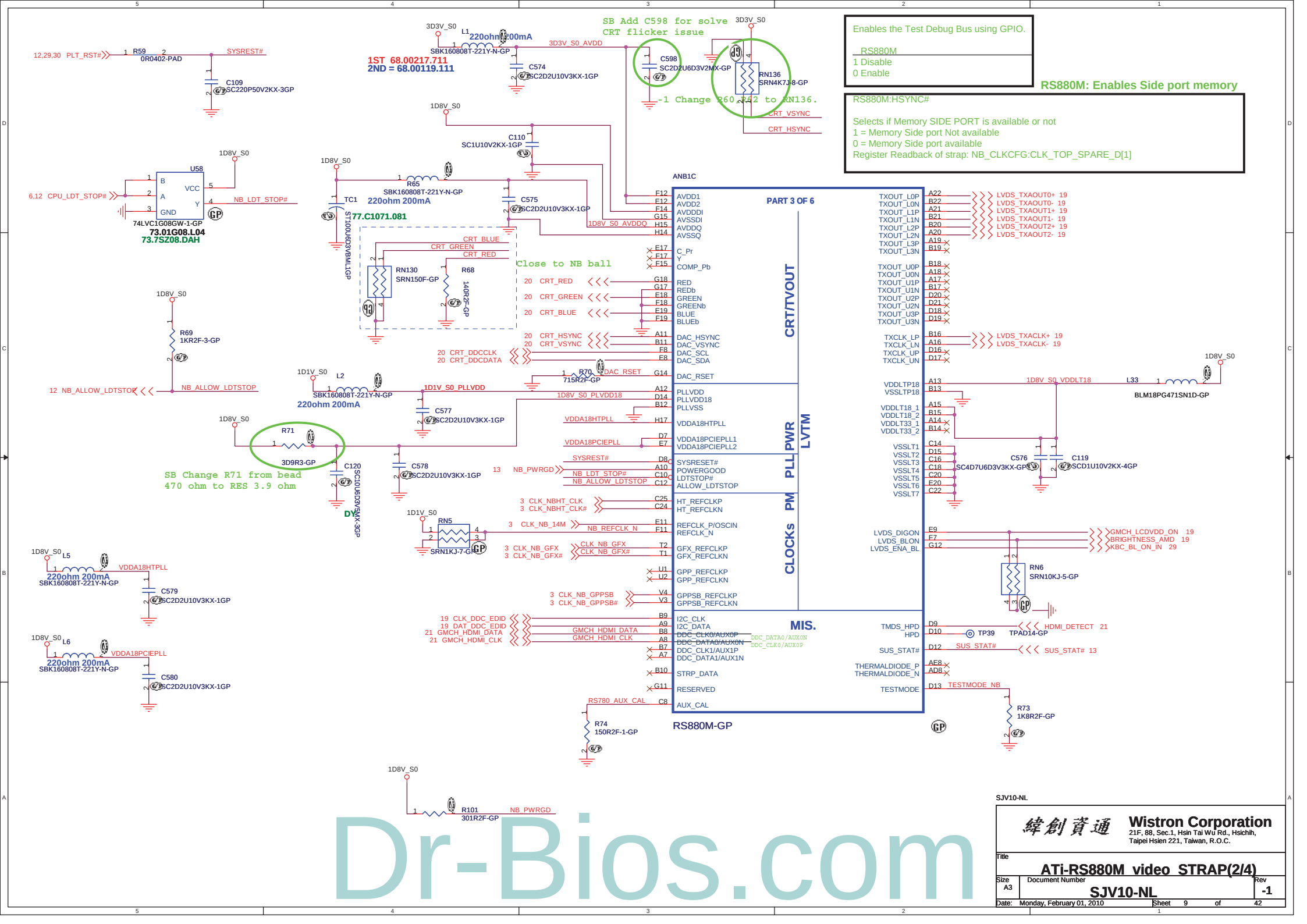
Title: **ATi-RS880M_HT LINK&PCIe(1/4)**

Size	Document Number	Rev
A3	SJV10-NL	-1

Date: Tuesday, January 26, 2010 Sheet 8 of 42



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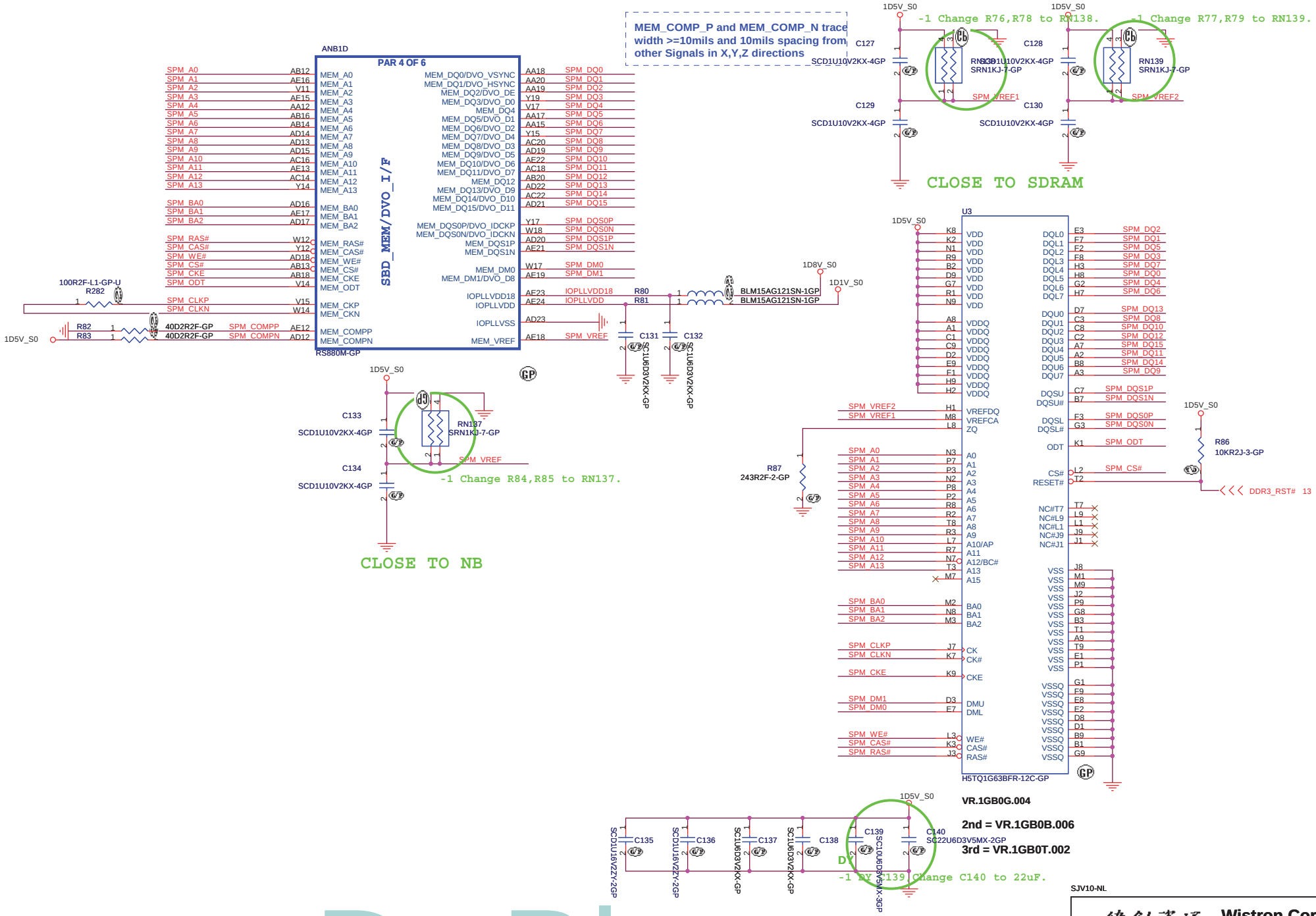
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-RS880M video STRAP(2/4)

Size	Document Number	Rev
A3	SJV10-NL	-1

Date: Monday, February 01, 2010 Sheet 9 of 42


MEM_COMP_P and MEM_COMP_N trace width >=10mils and 10mils spacing from other Signals in X,Y,Z directions
-1 Change R76,R78 to RN138.
-1 Change R77,R79 to RN139.
CLOSE TO SDRAM
ANB1D
PAR 4 OF 6
SBD_MEM/DVO_I/F
RS880M-GP
100R2F-L1-GP-U
R282
R82
R83
40D2R2F-GP
SPM_COMPP
SPM_COMPN
1D5V_S0
1D8V_S0
1D1V_S0
BLM15AG121SN-1GP
C131
C132
SC1U6D3V2KX-GP
C133
C134
SCD1U10V2KX-4GP
RN137
SRN1KJ-7-GP
-1 Change R84,R85 to RN137.
CLOSE TO NB
C127
C128
C129
C130
RN138
RN139
SRN1KJ-7-GP
SCD1U10V2KX-4GP
SPM_VREF1
SPM_VREF2
U3
H5TQ1G63BFR-12C-GP
R87
243R2F-2-GP
R86
10KR2J-3-GP
DDR3_RST# 13
C135
C136
C137
C138
C139
C140
SCD1U16V2Y-2GP
SC1U6D3V2KX-GP
SC22U6D3V5MX-2GP
VR.1GB0G.004
2nd = VR.1GB0B.006
3rd = VR.1GB0T.002
-1 BY F139 Change C140 to 22uF.
SJV10-NL
Wistron Corporation
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Title
ATi-RS880M SIDE PORT(3/4)
Size A3
Document Number
SJV10-NL
Rev -1
Date: Wednesday, January 27, 2010
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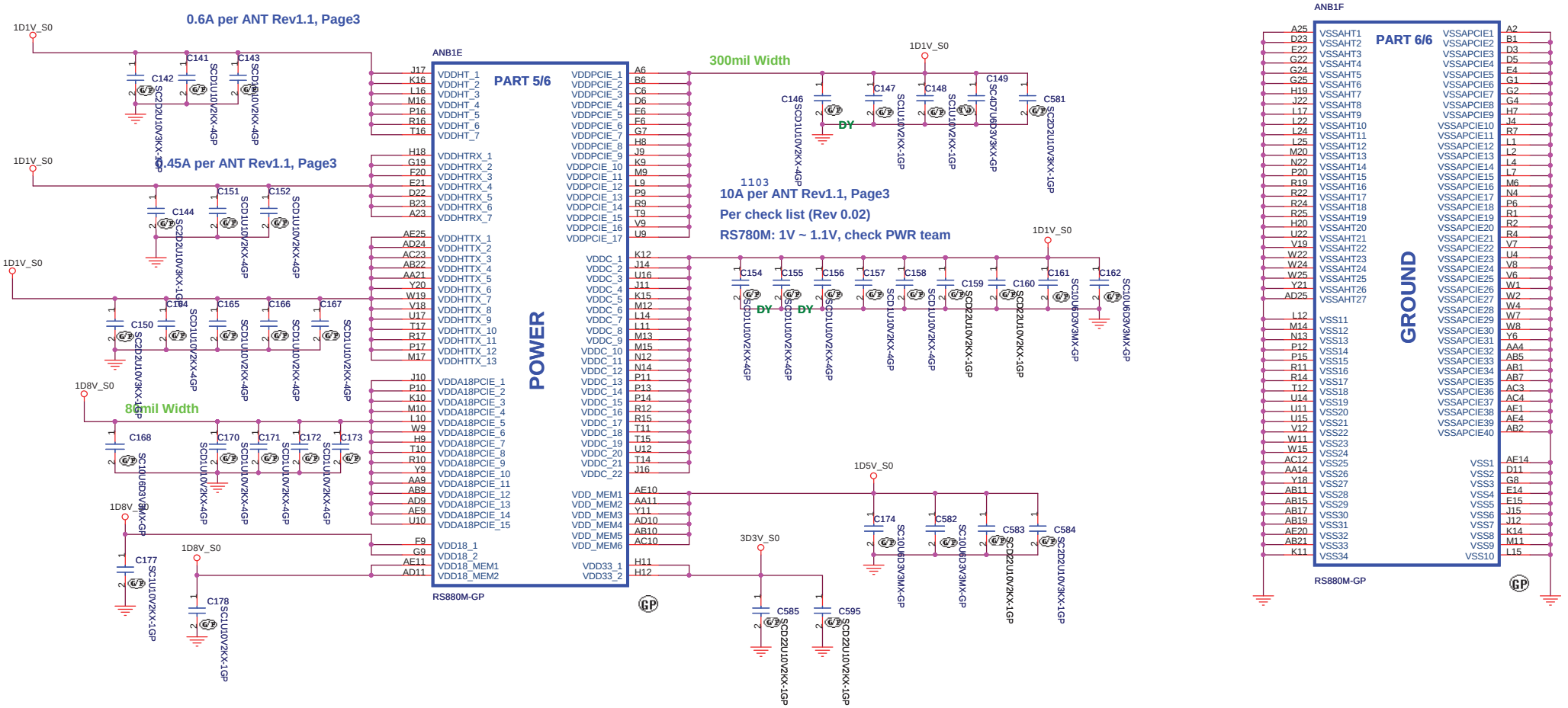

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Title: ATi-RS880M PWR&GND(4/4)

Size	Document Number	Rev
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-1 Change R89,R88 to RN140.

SRN33J-5-GP-U
RN140

23,26 PCIE_RST#_R
9,29,30 PLT_RST#
PCIE_RST#
A_RST#

ASB1A
Part 1 of 5

PCI CLKS
PCIE_RST#
A_RST#

PCICLK0 W2 PCI_CLK0_R → TP38 TPAD14-GP
PCICLK1/GPO36 W1 PCI_CLK1 → PCI_CLK1 16
PCICLK2/GPO37 W3 PCI_CLK2 → PCI_CLK2 16
PCICLK3/GPO38 W4 PCI_CLK3 → PCI_CLK3 16
PCICLK4/14M_OSC/GPO39 Y1 PCI_CLK4 → PCI_CLK4 16
PCIRST# V2

PCI EXPRESS INTERFACES

8 ALINK_NBRX_SBTX_P0 C181 SCD1U16V2KX-3GP ALINK_NBRX_C_SBTX_P0 AD26
8 ALINK_NBRX_SBTX_N0 C186 SCD1U16V2KX-3GP ALINK_NBRX_C_SBTX_N0 AD27
8 ALINK_NBRX_SBTX_P1 C187 SCD1U16V2KX-3GP ALINK_NBRX_C_SBTX_P1 AC28
8 ALINK_NBRX_SBTX_N1 C182 SCD1U16V2KX-3GP ALINK_NBRX_C_SBTX_N1 AC29
8 ALINK_NBRX_SBTX_P2 C183 SCD1U16V2KX-3GP ALINK_NBRX_C_SBTX_P2 AB29
8 ALINK_NBRX_SBTX_N2 C184 SCD1U16V2KX-3GP ALINK_NBRX_C_SBTX_N2 AB28
8 ALINK_NBRX_SBTX_P3 C188 SCD1U16V2KX-3GP ALINK_NBRX_C_SBTX_P3 AB26
8 ALINK_NBRX_SBTX_N3 C185 SCD1U16V2KX-3GP ALINK_NBRX_C_SBTX_N3 AB27

A_TX0P
A_TX0N
A_TX1P
A_TX1N
A_TX2P
A_TX2N
A_TX3P
A_TX3N

8 ALINK_NBTX_C_SBRX_P0 AE24 A_RX0P
8 ALINK_NBTX_C_SBRX_N0 AE23 A_RX0N
8 ALINK_NBTX_C_SBRX_P1 AD25 A_RX1P
8 ALINK_NBTX_C_SBRX_N1 AD24 A_RX1N
8 ALINK_NBTX_C_SBRX_P2 AC24 A_RX2P
8 ALINK_NBTX_C_SBRX_N2 AC25 A_RX2N
8 ALINK_NBTX_C_SBRX_P3 AB25 A_RX3P
8 ALINK_NBTX_C_SBRX_N3 AB24 A_RX3N

PCIE_VDDR
R94 562R2F-GP PCIE_CALRP AD29 PCIE_CALRP
R90 2K05R2F-GP PCIE_CALRN AD28 PCIE_CALRN
Place R <100mils form pins T25,T24

GPP_TX0P AA28
GPP_TX0N AA29
GPP_TX1P Y29
GPP_TX1N Y28
GPP_TX2P Y26
GPP_TX2N Y27
GPP_TX3P W28
GPP_TX3N W29

GPP_RX0P AA22
GPP_RX0N Y21
GPP_RX1P AA25
GPP_RX1N AA24
GPP_RX2P W23
GPP_RX2N V24
GPP_RX3P W24
GPP_RX3N W25

SB820 CSL 25-35:* Note: If PCI interface is not used, then these balls can be used for alternate GPIO/GPO function or left not connected.

PCI_AD23 AE9 PCI_AD23 → PCI_AD23 16
PCI_AD24 AD9 PCI_AD24 → PCI_AD24 16
PCI_AD25 AC11 PCI_AD25 → PCI_AD25 16
PCI_AD26 AE6 PCI_AD26 → PCI_AD26 16
PCI_AD27 AE4 PCI_AD27 → PCI_AD27 16
PCI_AD28 AE3 PCI_AD28 → PCI_AD28 16
PCI_AD29 AH2 PCI_AD29 → PCI_AD29 16

AD0/GPIO0 AA1
AD1/GPIO1 AA4
AD2/GPIO2 AA3
AD3/GPIO3 AB1
AD4/GPIO4 AA5
AD5/GPIO5 AB2
AD6/GPIO6 AB6
AD7/GPIO7 AB5
AD8/GPIO8 AA6
AD9/GPIO9 AC2
AD10/GPIO10 AC3
AD11/GPIO11 AC4
AD12/GPIO12 AC1
AD13/GPIO13 AD1
AD14/GPIO14 AD2
AD15/GPIO15 AC6
AD16/GPIO16 AE2
AD17/GPIO17 AE1
AD18/GPIO18 AF8
AD19/GPIO19 AE3
AD20/GPIO20 AF1
AD21/GPIO21 AG1
AD22/GPIO22 AF2
AD23/GPIO23 AE9
AD24/GPIO24 AD9
AD25/GPIO25 AC11
AD26/GPIO26 AE6
AD27/GPIO27 AE4
AD28/GPIO28 AE3
AD29/GPIO29 AH2
AD30/GPIO30 AG2
AD31/GPIO31 AH3

-1 Add VRAM identify pins.

3D3V_S0
R331 1KR2F-3-GP DY_HYNIX_ATI VRAM_IDENT1
R332 1KR2F-3-GP DY_SAMSUNG
R334 1KR2F-3-GP DY_SAMSUNG_ATI VRAM_IDENT2
R333 1KR2F-3-GP DY_HYNIX

3D3V_AUX_S5
D31 BAS16-1-GP 83.00016.B11
2ND = 83.00016.K11
3RD = 83.00016.F11
RTC_BAT_R
R861 1KR2J-1-GP
D30 BAS40CW-GP 83.00040.E81
RTC_AUX_S5
RTC_BAT_DR
RTC_BAT_D
R99 510R2J-1-GP
MLX-CON2-13-GP RTC1
20.F1035.002
20.F0772.002
SB Add RTC charge circuit.

CBE0# AA8
CBE1# AD5
CBE2# AD8
CBE3# AA10
FRAME# AE8
DEVSEL# AB9
IRDY# AJ3
TRDY# AE7
PAR AC5
STOP# AE5
PERR# AE6
SERR# AE4
REQ0# AE11
REQ1#/GPIO40 AH5
REQ2#/CLK_REQ8#/GPIO41 AH4
REQ3#/CLK_REQ5#/GPIO42 AC12
GNT0# AD12
GNT1#/GPO44 AJ5
GNT2#/GPO45 AH6
GNT3#/CLK_REQ7#/GPIO46 AB12
CLKRUN# AB11 → PM_CLKRUN# 29
LOCK# AD7

PCI INTERFACE

GPIO34,35 internal pull high

R96 10KR2J-3-GP DY

INTE#/GPIO32 AJ6
INTF#/GPIO33 AG6
INTG#/GPIO34 AG4 VRAM_IDENT1
INTH#/GPIO35 AJ4 VRAM_IDENT2

3 CLK_PCIE_SB M23 PCIE_RCLKP/NB_LNK_CLKP
3 CLK_PCIE_SB# P23 PCIE_RCLKN/NB_LNK_CLKN

U29 NB_DISP_CLKP
U28 NB_DISP_CLKN
T26 NB_HT_CLKP
T27 NB_HT_CLKN
V21 CPU_HT_CLKP
T21 CPU_HT_CLKN
V23 SLT_GFX_CLKP
T23 SLT_GFX_CLKN
L29 GPP_CLK0P
L28 GPP_CLK0N
N29 GPP_CLK1P
N28 GPP_CLK1N
M29 GPP_CLK2P
M28 GPP_CLK2N
T25 GPP_CLK3P
V25 GPP_CLK3N
L24 GPP_CLK4P
L23 GPP_CLK4N
P25 GPP_CLK5P
M25 GPP_CLK5N
P29 GPP_CLK6P
P28 GPP_CLK6N
N26 GPP_CLK7P
N27 GPP_CLK7N
T29 GPP_CLK8P
T28 GPP_CLK8N
L25 14M_25M_48M_OSC

CLOCK GENERATOR

LPC
LPCCLK0 H24 LPCCLK0_R → LPCCLK0_R 16
LPCCLK1 H25 LPCCLK1_R → LPCCLK1_R 16
LAD0 J27 LPC_LAD0 29,30
LAD1 J26 LPC_LAD1 29,30
LAD2 H29 LPC_LAD2 29,30
LAD3 H28 LPC_LAD3 29,30
LFRAME# G28 LPC_LFRAME# 29,30
LDRQ0# J25 LDRQ0# → TP53 TPAD14-GP
LDRQ1#/CLK_REQ6#/GPIO49 AA18
SERIRQ/GPIO48 AB19 → INT_SERIRQ 29

RN7 SRN22-3-GP
PCLK_FWH 30
PCLK_KBC 29
EC3 EC4 SC22P50V2JN-4GP DY

CPU
ALLOW_LDTSTP/DMA_ACTIVE# G21 NB_ALLOW_LDTSTOP 9
PROCHOT# H21 PROCHOT#_SB 6
LDT_PG K19 CPU_PWRGD 6,41
LDT_STP# G22 CPU_LDT_STOP# 6,9
LDT_RST# J24 CPU_LDT_RST# 6,41

RTC
32K_X1 C1 RTC_X1
32K_X2 C2 RTC_X2
RTCCLK D2 → RTC_CLK 28
INTRUDER_ALERT# B2
VDDBT_RTC_G B1 RTC_AUX_S5

C189 SC15P50V2JN-2-GP
C190 SC15P50V2JN-2-GP
R97 10MR2J-L-GP
X2 X-32D768KHZ-34GPU 82.30001.661 82.30001.B21
SB Change C189 to 22pF, C190 to 15pF.
-1 Change C189 to 15pF.

SB Change R43 from Dummy to 1M ohm.
R43 1MR2F-GP
25M_X1 L26 25M_X1
25M_X2 L27 25M_X2
X3 XTAL-25MHZ-102-GP 82.30020.851
2ND = 82.30020.A31
-1 Change C193 to 12pF.
C193 SC12P50V2JN-3GP
C191 SC15P50V2JN-2-GP

SB820M-GP
71.SB820.M03

G122 GAP-OPEN
SB Add G122.
C192 SCU10U16V2KX-1GP
C194 SCD1U16V2ZY-2GP

	HYNIX VR.1GB0G.004	SAMSUNG VR.1GB0B.006	ATI VR.1GB0T.002
VRAM_IDENT1	HIGH	LOW	HIGH
VRAM_IDENT2	LOW	HIGH	HIGH

DEFAULT

SJV10-NL

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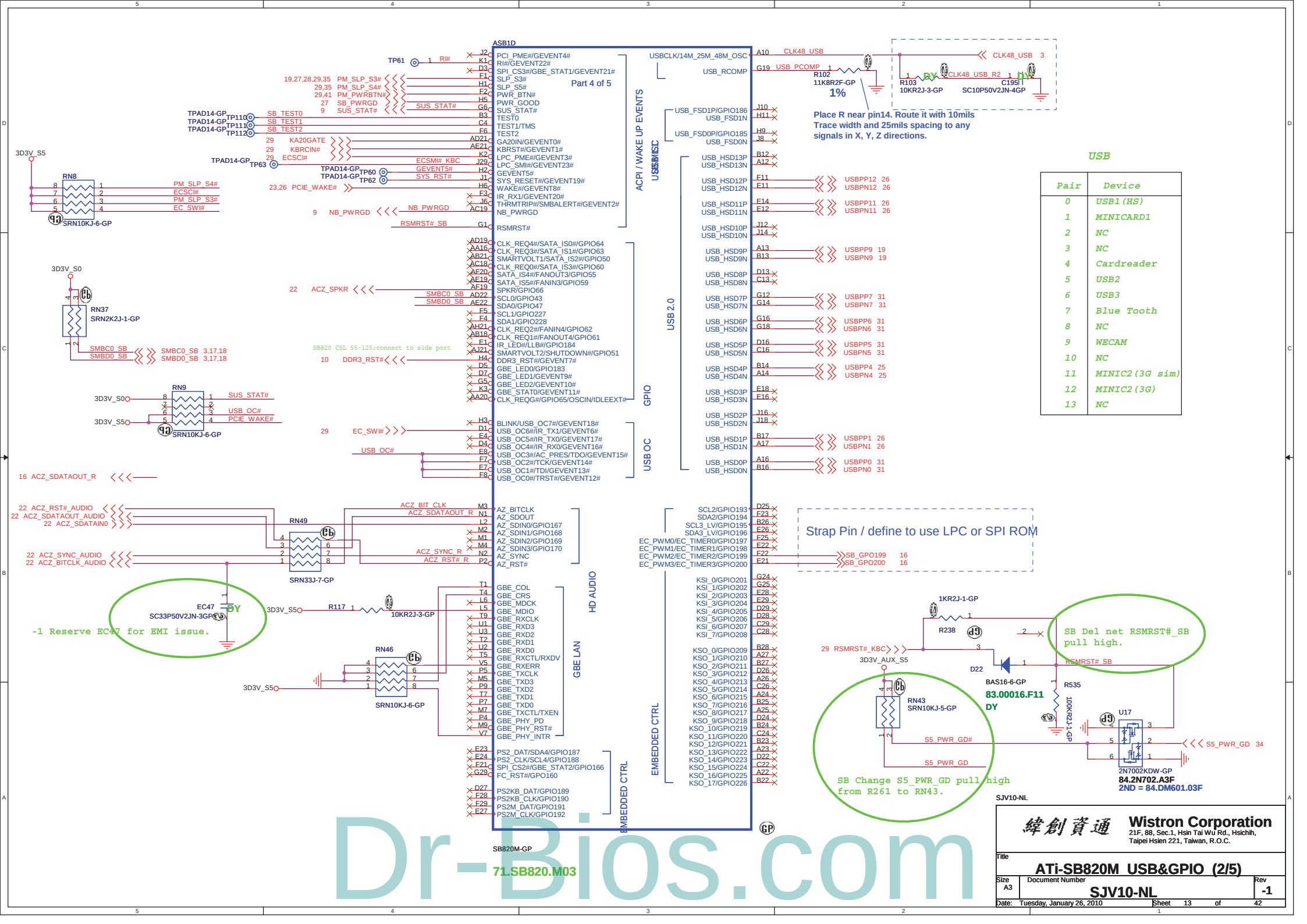
Title: ATi-SB820M PCIE&PCI (1/5)
Size: A3
Document Number: SJV10-NL
Rev: -1
Date: Monday, February 01, 2010
Sheet 12 of 42


ASB1D
Part 4 of 5
SB820M-GP
71.SB820.M03
ACPI / WAKE UP EVENTS
USB MISC
USB 2.0
GPIO
USB OC
HD AUDIO
GBE LAN
EMBEDDED CTRL
USB
Pair Device
0 USB1(HS)
1 MINICARD1
2 NC
3 NC
4 Cardreader
5 USB2
6 USB3
7 Blue Tooth
8 NC
9 WECAM
10 NC
11 MINIC2(3G sim)
12 MINIC2(3G)
13 NC
Strap Pin / define to use LPC or SPI ROM
Place R near pin14. Route it with 10mils Trace width and 25mils spacing to any signals in X, Y, Z directions.
-1 Reserve EC47 for EMI issue.
SB Del net RSMRST#_SB pull high.
SB Change S5_PWR_GD pull high from R261 to RN43.
SB820 CSL 55-125:connect to side port
Wistron Corporation
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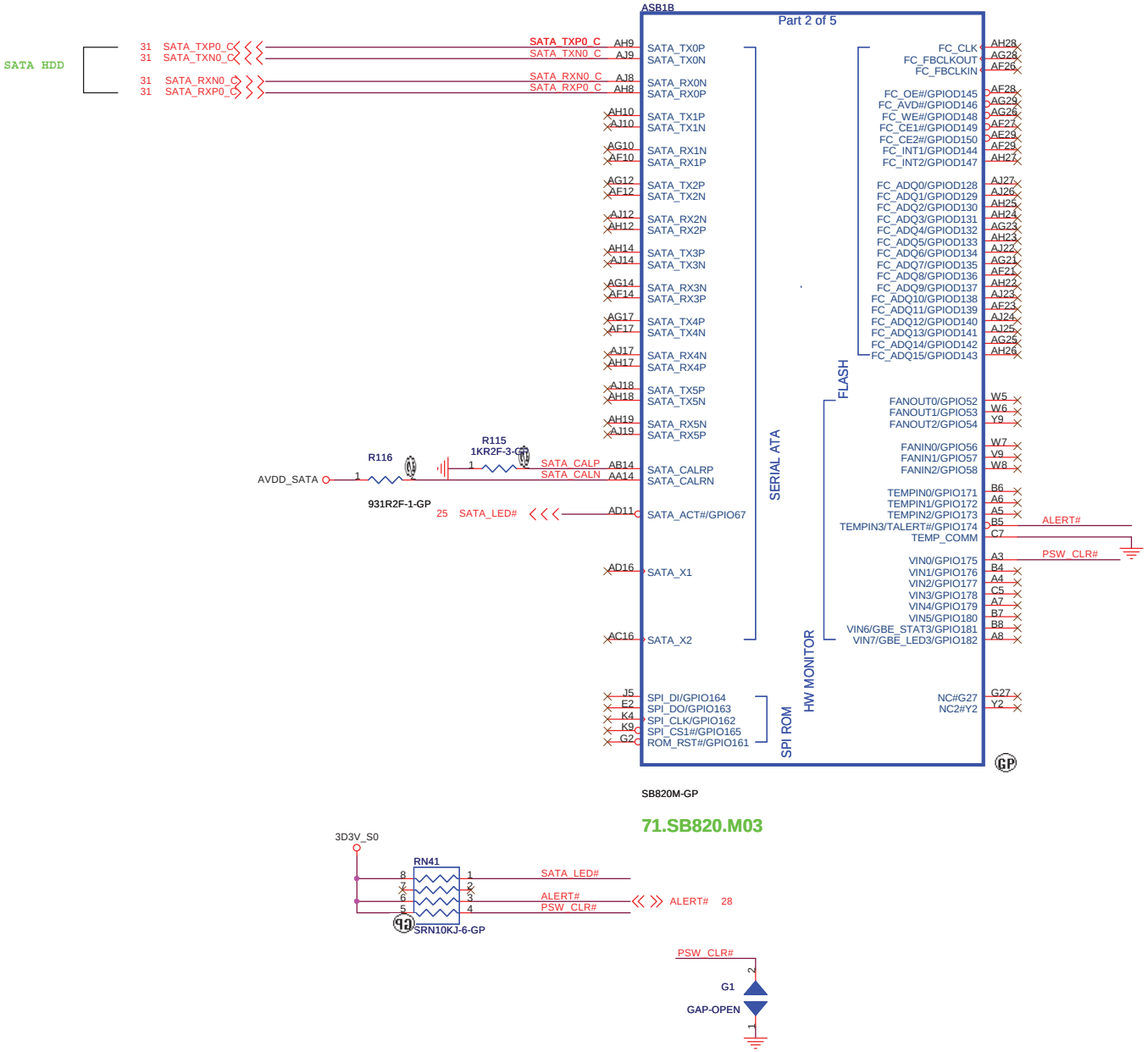
Title
ATi-SB820M USB&GPIO (2/5)
Size A3
Document Number SJV10-NL
Rev -1
Date: Tuesday, January 26, 2010
Sheet 13 of 42

PLACE SATA AC DECOUPLING
CAPS CLOSE TO SB710



71.SB820.M03

SJV10-NL

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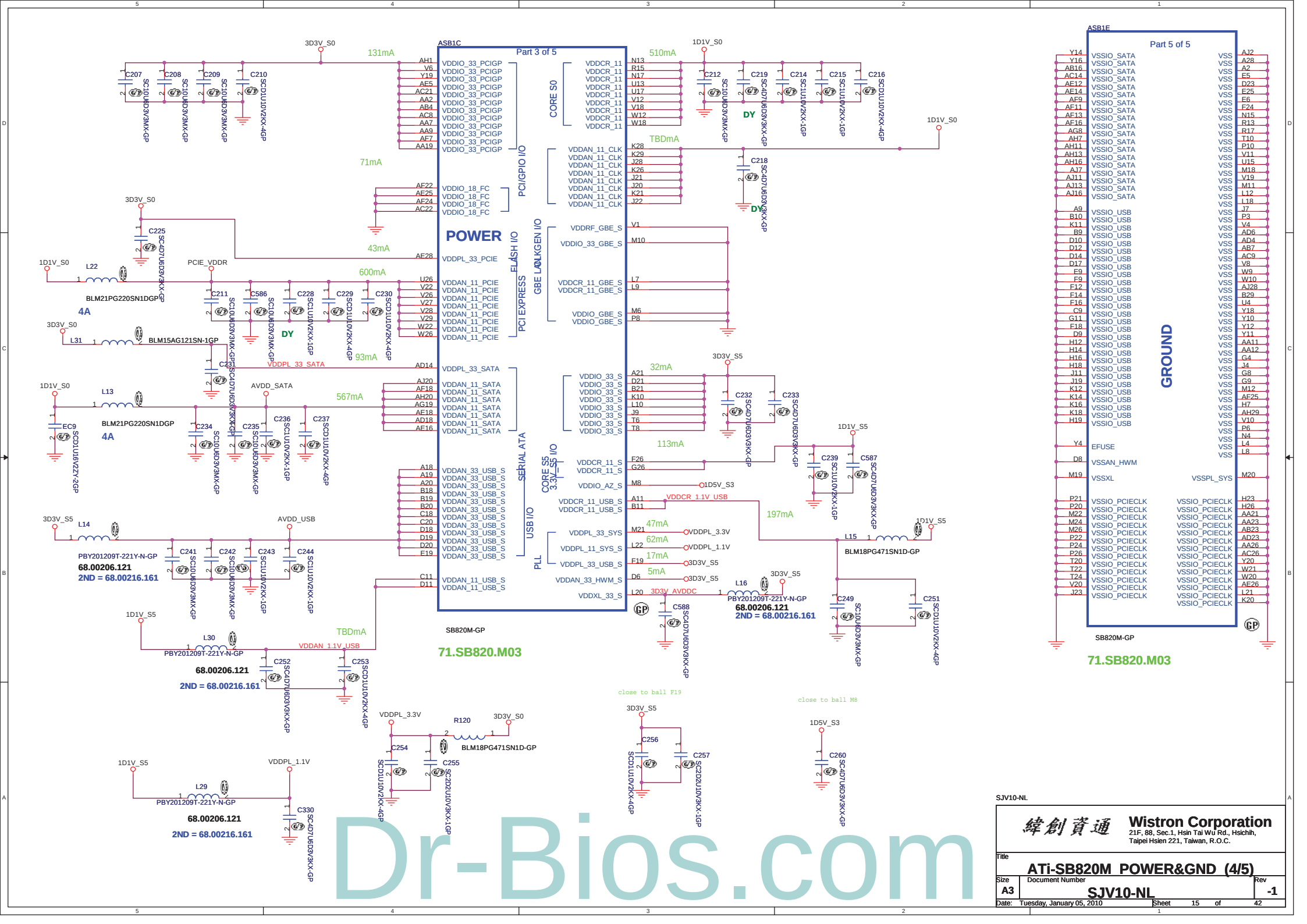
Title: ATi-SB820M SATA-FC (3/5)

Size	Document Number	Rev
A3	SJV10-NL	-1

Date: Tuesday, January 26, 2010 Sheet 14 of 42



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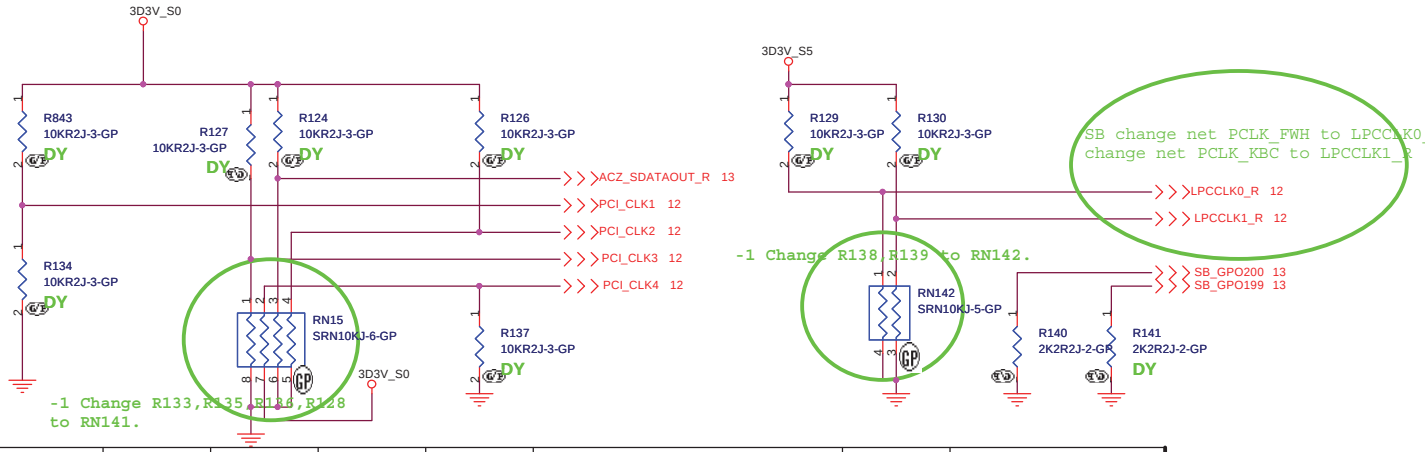
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB820M POWER&GND (4/5)

Size	Document Number	Rev
A3	SJV10-NL	-1

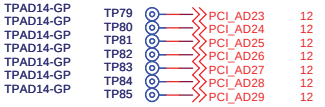
Date: Tuesday, January 05, 2010 Sheet 15 of 42



REQUIRED STRAPS

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200 GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED	H,H = Reserved H,L = SPI ROM
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	L,H = LPC ROM (Default) L,L = FWH ROM

DEBUG STRAPS



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

SJV10-NL

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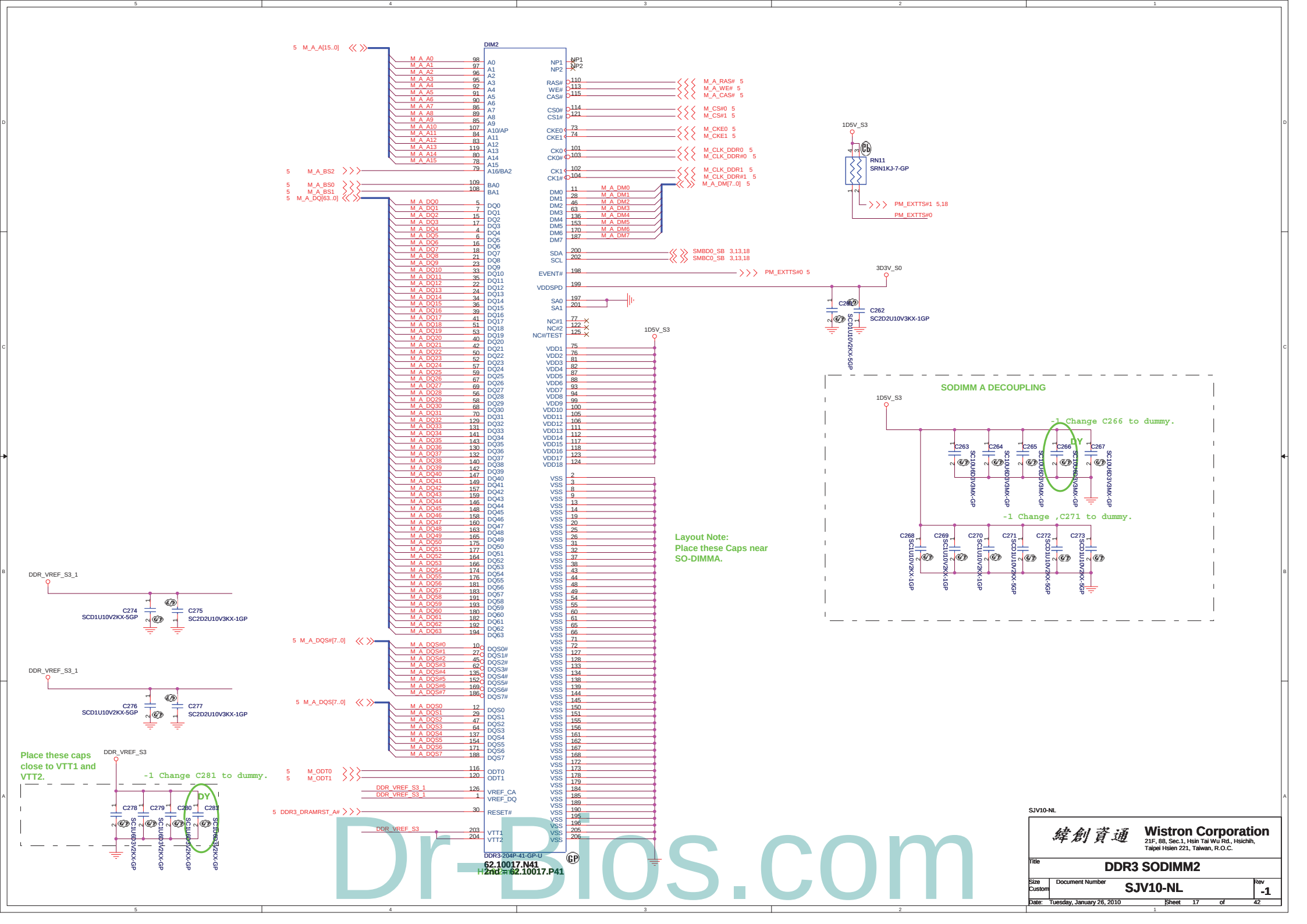
Title: ATi-SB820M STRAPPING (5/5)

Size: A3 | Document Number: SJV10-NL | Rev: -1

Date: Tuesday, January 26, 2010 | Sheet 16 of 42


DIM2
DDR3-204P-41-GP-U
62.10017.N41
2nd = 62.10017.P41
SODIMM A DECOUPLING
-1 Change C266 to dummy.
-1 Change ,C271 to dummy.
Layout Note:
Place these Caps near
SO-DIMMA.
Place these caps
close to VTT1 and
VTT2.
-1 Change C281 to dummy.
RN11
SRN1KJ-7-GP
SJV10-NL
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DDR3 SODIMM2
SJV10-NL
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Tuesday, January 26, 2010
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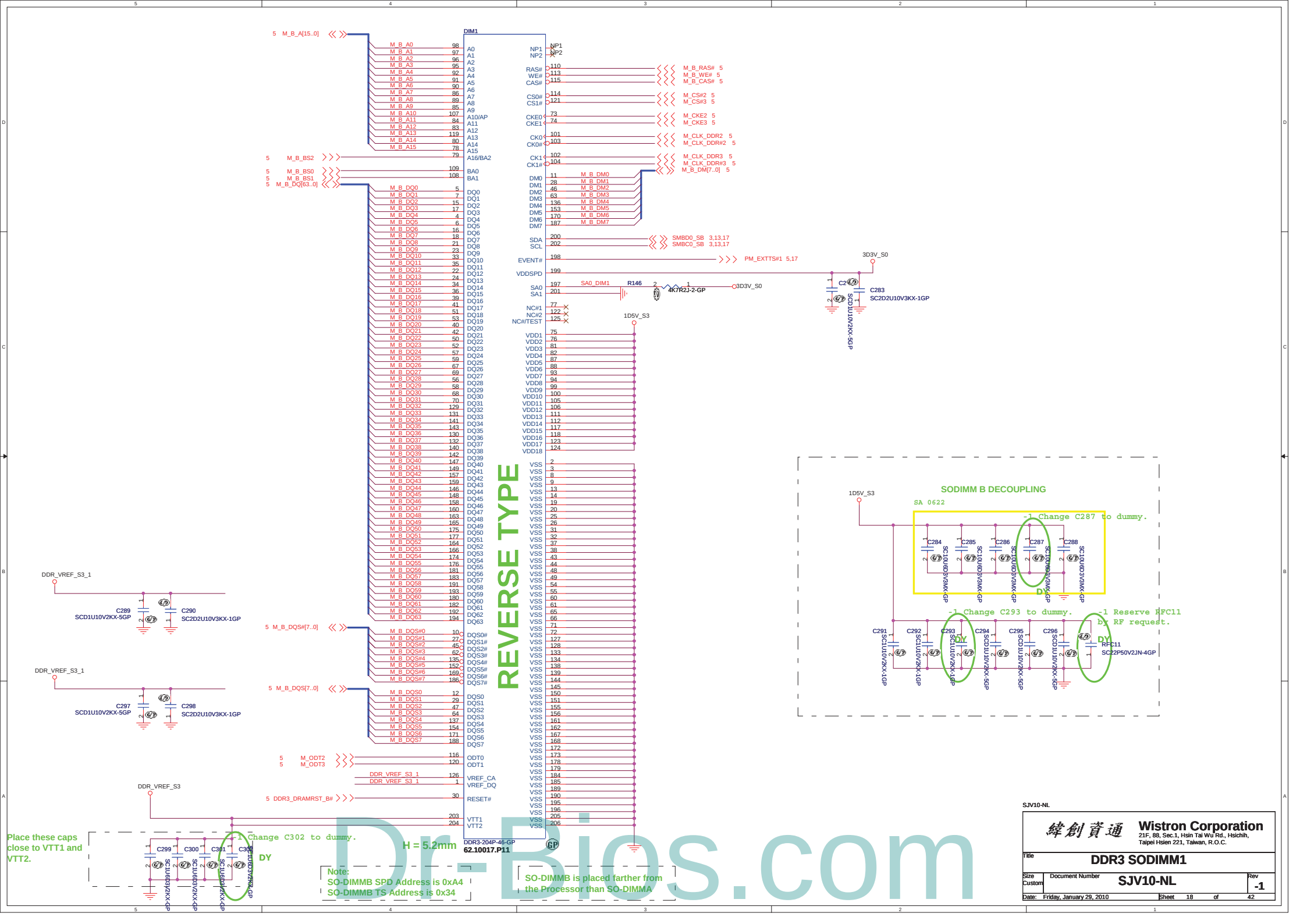
DIM1
REVERSE TYPE
DDR3-204P-46-GP
62.10017.P11
SODIMM B DECOUPLING
SA 0622
-1 Change C287 to dummy.
-1 Change C293 to dummy.
-1 Reserve RFC11 by RF request.
-1 Change C302 to dummy.
Place these caps close to VTT1 and VTT2.
H = 5.2mm
Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34
SO-DIMMB is placed farther from the Processor than SO-DIMMA
Dr-Bios.com
SJV10-NL
Wistron Corporation
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DDR3 SODIMM1
SJV10-NL
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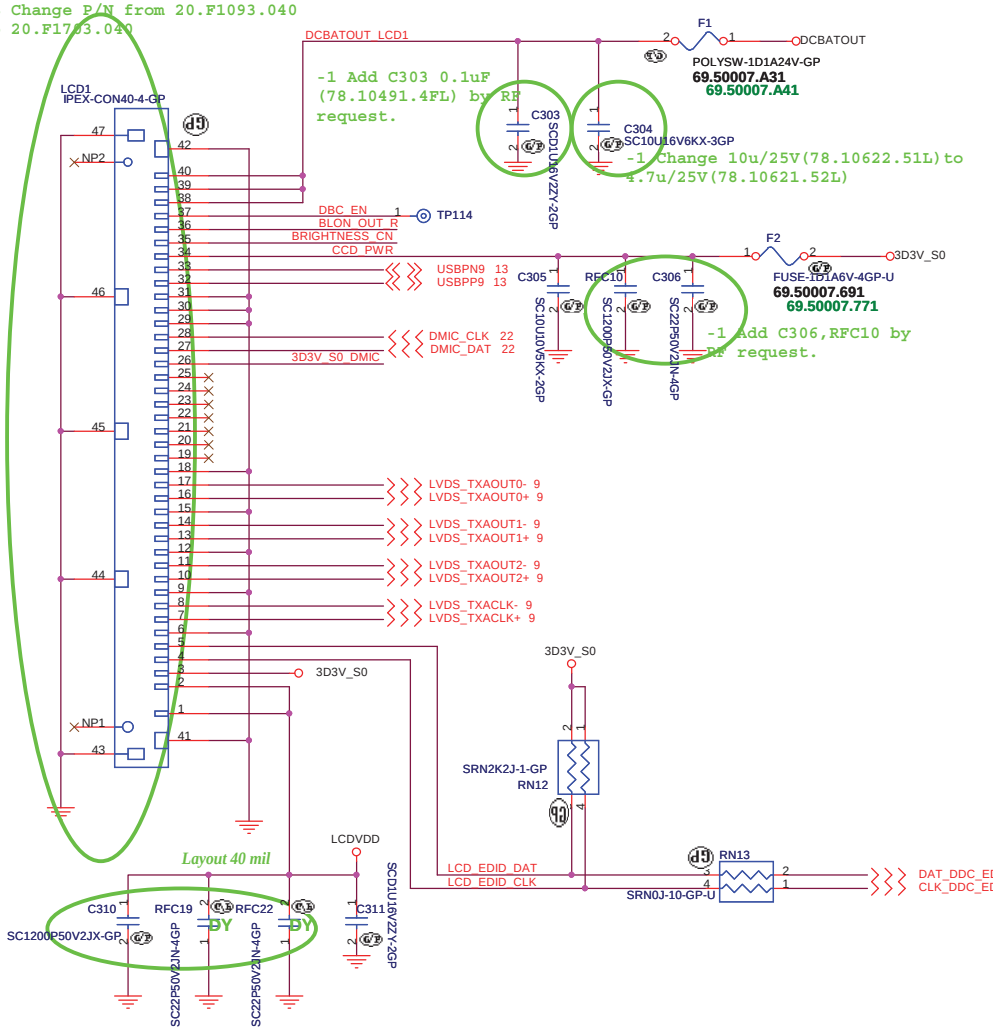
SB Change P/N from 20.F1093.040
to 20.F1703.040

CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	NC

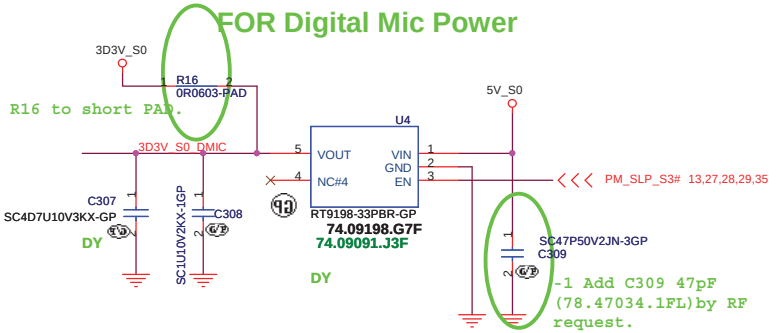
D MIC Pin	
Pin	Symbol
1	DMIC_DAT
2	3D3V_S0_DMIC
3	DMIC_CLK
4	GND

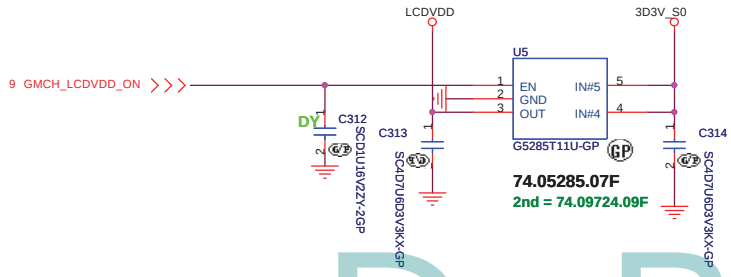


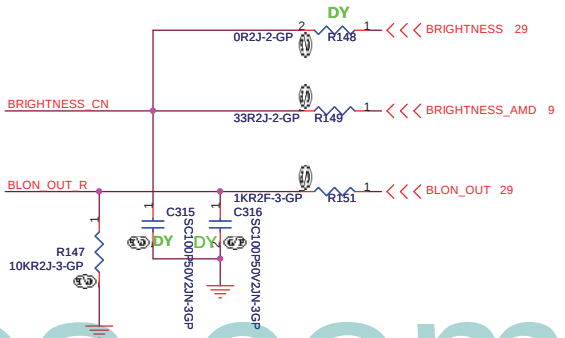
-1 Add C310,Reserve RFC19,RFC22 by RF request.

FOR Digital Mic Power

-1 Change R16 to short PAD.







SJV10-NL

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Title: LCD Conn

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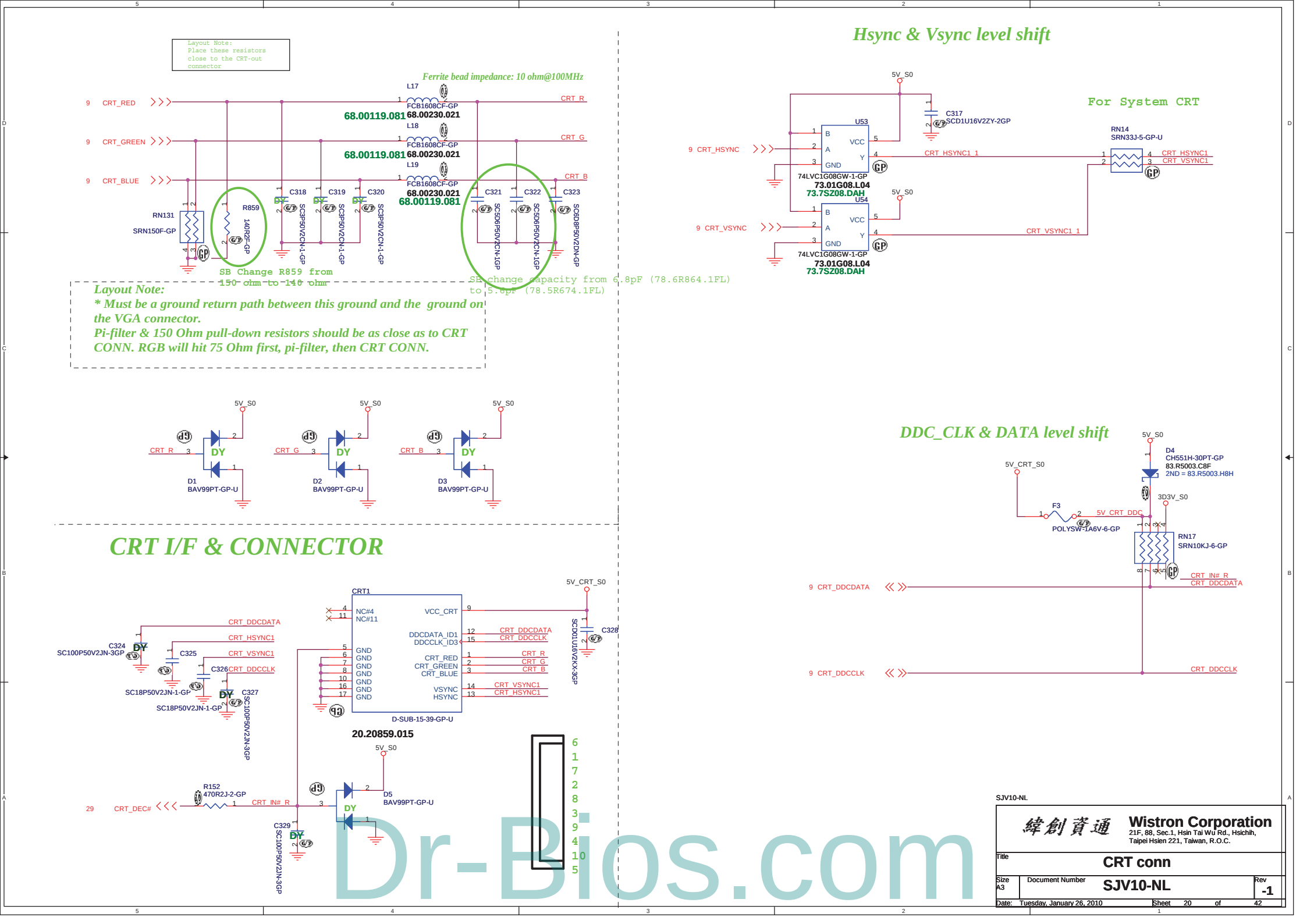
Date: Sunday, January 31, 2010 Sheet 19 of 42


Layout Note:
Place these resistors close to the CRT-out connector
Ferrite bead impedance: 10 ohm@100MHz
9 CRT_RED
9 CRT_GREEN
9 CRT_BLUE
L17
L18
L19
FCB1608CF-GP
68.00119.081
68.00230.021
CRT_R
CRT_G
CRT_B
RN131
SRN150F-GP
R859
140R2F-GP
C318
C319
C320
C321
C322
C323
SC3P50V2CN-1-GP
SC5D6P50V2CN-1GP
SC6D8P50V2DN-GP
SB Change R859 from 150 ohm to 140 ohm
SB change capacity from 6.8pF (78.6R864.1FL) to 5.6pF (78.5R674.1FL)
Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.
5V_S0
CRT_R
CRT_G
CRT_B
D1
D2
D3
BAV99PT-GP-U
CRT I/F & CONNECTOR
CRT1
D-SUB-15-39-GP-U
NC#4
NC#11
VCC_CRT
DDCDATA_ID1
DDCCLK_ID3
CRT_RED
CRT_GREEN
CRT_BLUE
VSYNC
HSYNC
GND
5V_CRT_S0
C328
SCD01U16V2KX-3GP
CRT_DDCDATA
CRT_HSYNC1
CRT_VSYNC1
CRT_DDCCLK
C324
SC100P50V2JN-3GP
C325
C326
C327
SC18P50V2JN-1-GP
SC100P50V2JN-3GP
20.20859.015
R152
470R2J-2-GP
29 CRT_DEC#
CRT_IN# R
D5
BAV99PT-GP-U
C329
Hsync & Vsync level shift
For System CRT
9 CRT_HSYNC
9 CRT_VSYNC
U53
U54
B
A
GND
VCC
Y
74LVC1G08GW-1-GP
73.01G08.L04
73.7SZ08.DAH
C317
SCD1U16V2ZY-2GP
RN14
SRN33J-5-GP-U
CRT_HSYNC1_1
CRT_VSYNC1_1
CRT_HSYNC1
CRT_VSYNC1
DDC_CLK & DATA level shift
5V_CRT_S0
D4
CH551H-30PT-GP
83.R5003.C8F
2ND = 83.R5003.H8H
3D3V_S0
F3
POLYSW-1A6V-6-GP
5V_CRT_DDC
RN17
SRN10KJ-6-GP
9 CRT_DDCDATA
9 CRT_DDCCLK
CRT_IN# R
SJV10-NL
緯創資通
Wistron Corporation
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Title
CRT conn
Size
A3
Document Number
SJV10-NL
Rev
-1
Date: Tuesday, January 26, 2010
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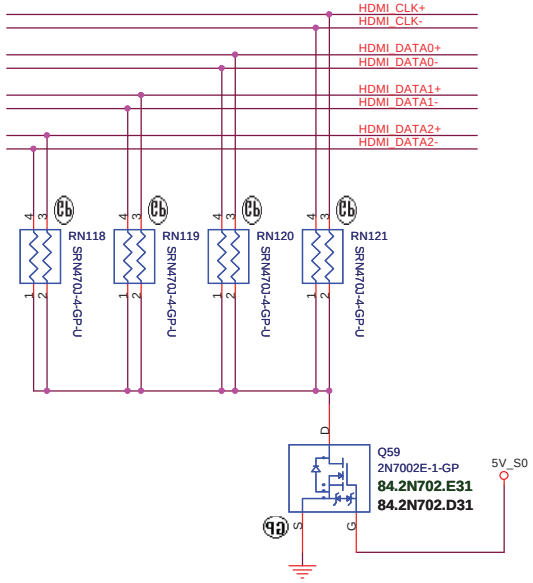
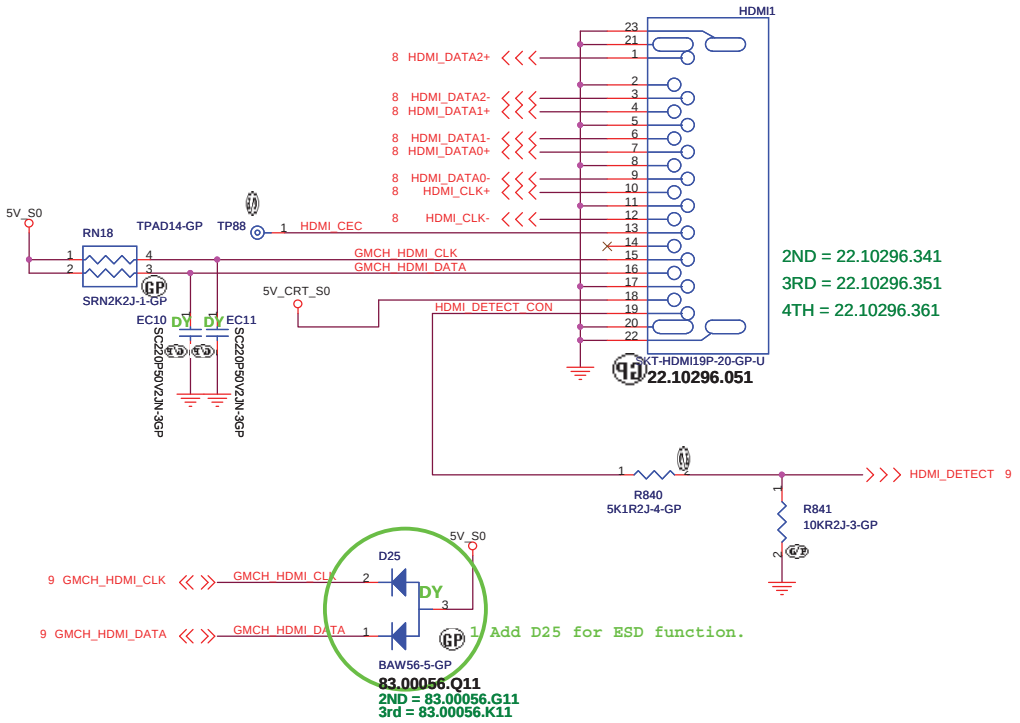


HDMI CONNECTOR



SJV10-NL

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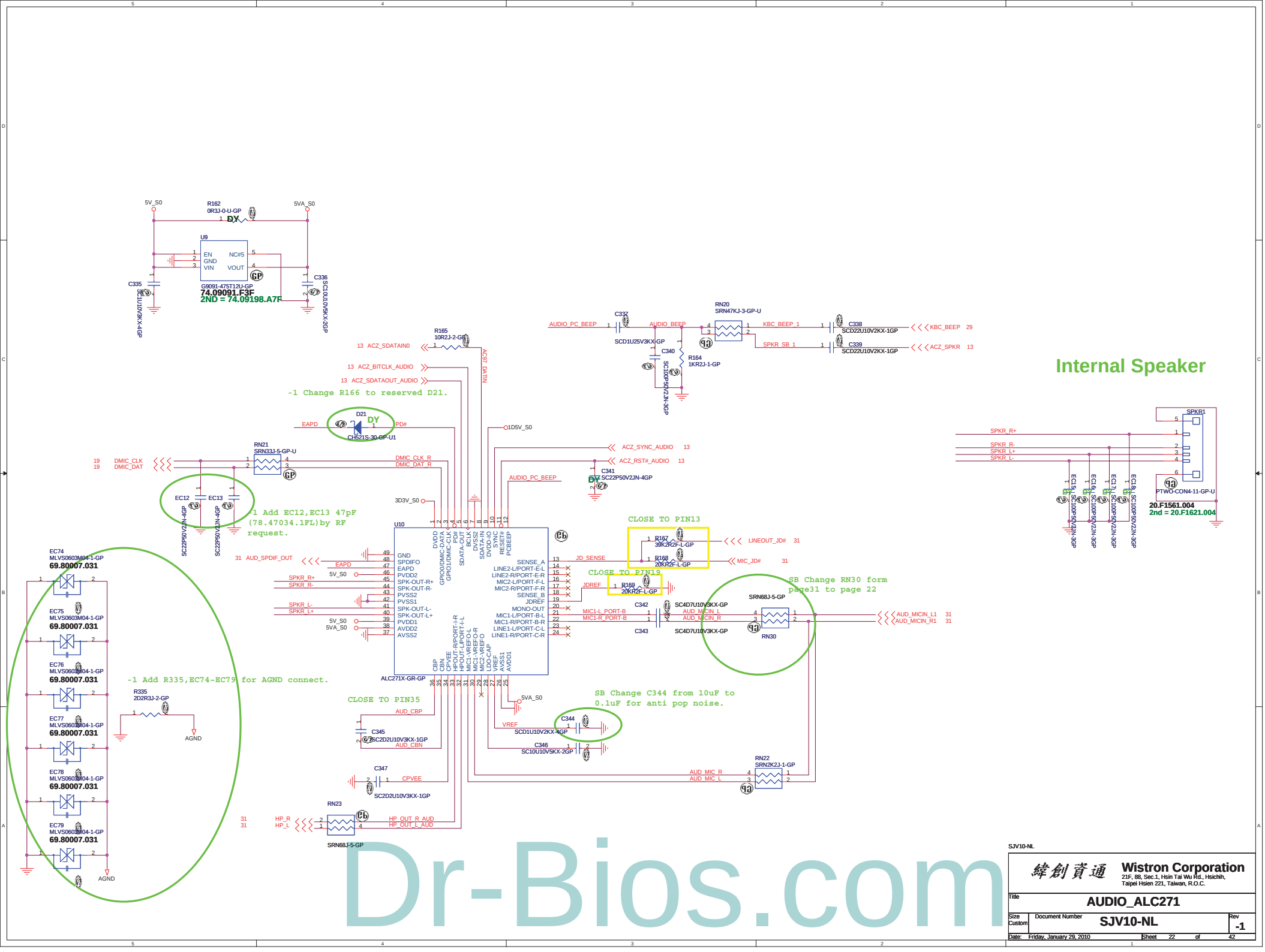
Title: HDMI conn		
Size: A3	Document Number: SJV10-NL	Rev: -1
Date: Tuesday, February 02, 2010	Sheet 21 of 42	


Internal Speaker
-1 Change R166 to reserved D21.
-1 Add EC12,EC13 47pF (78.47034.1FL)by RF request.
-1 Add R335,EC74~EC79 for AGND connect.
CLOSE TO PIN13
CLOSE TO PIN19
CLOSE TO PIN35
SB Change RN30 form page31 to page 22
SB Change C344 from 10uF to 0.1uF for anti pop noise.
U9
G9091-475T12U-GP
74.09091.F3F
2ND = 74.09198.A7F
U10
ALC271X-GR-GP
SPKR1
PTWO-CON4-11-GP-U
20.F1561.004
2nd = 20.F1621.004
SJV10-NL
Wistron Corporation
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AUDIO_ALC271
SJV10-NL
-1
Friday, January 29, 2010
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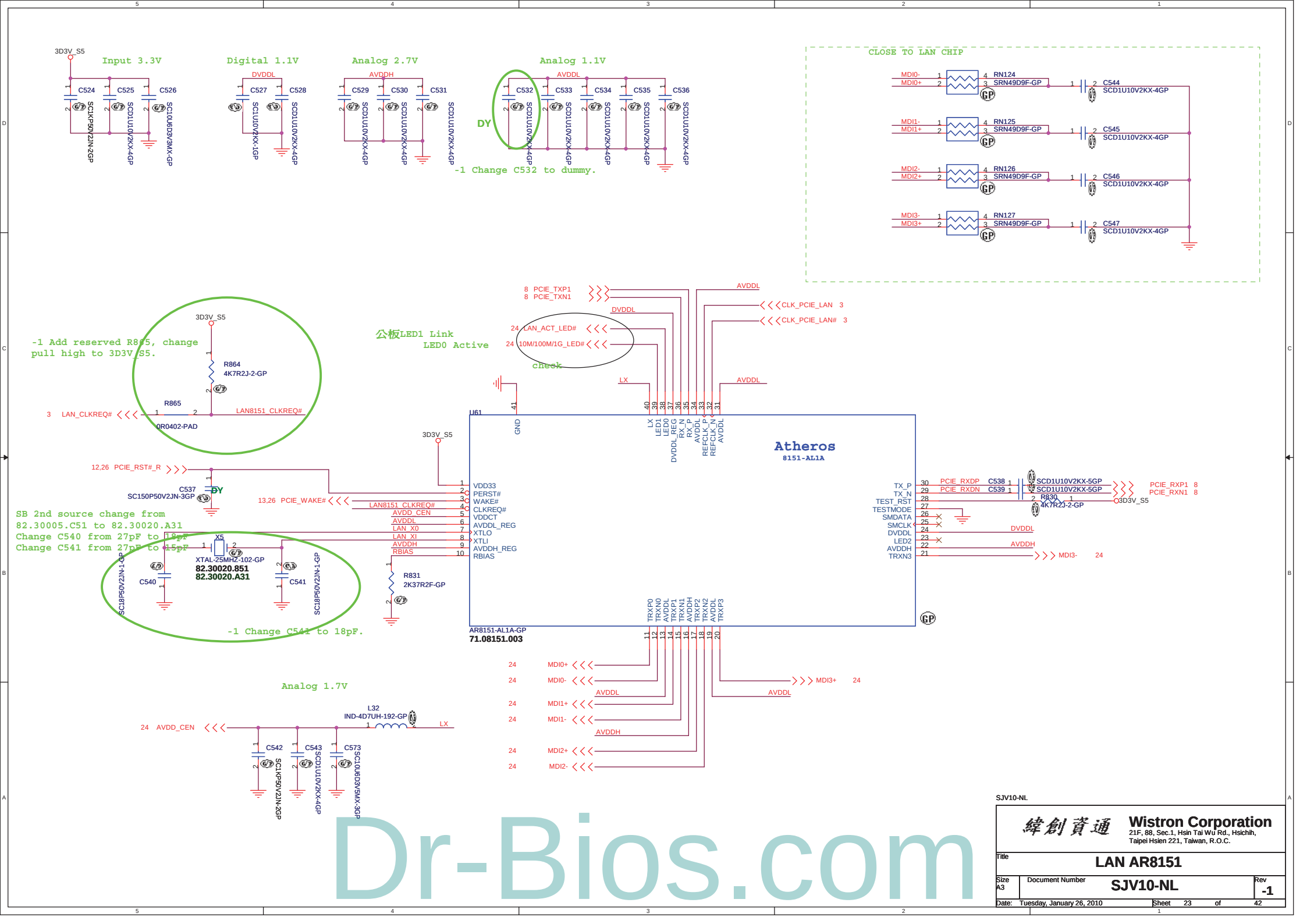

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Title: LAN AR8151

Size: A3 | Document Number: SJV10-NL | Rev: -1

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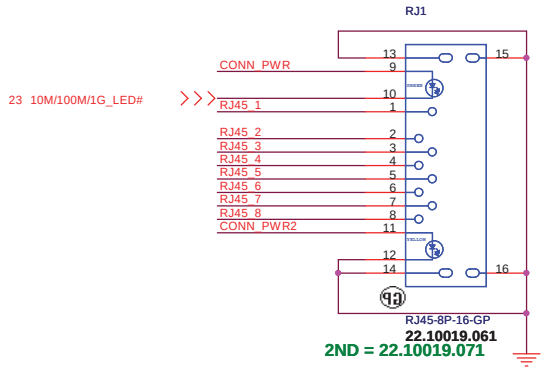
LAN Connector

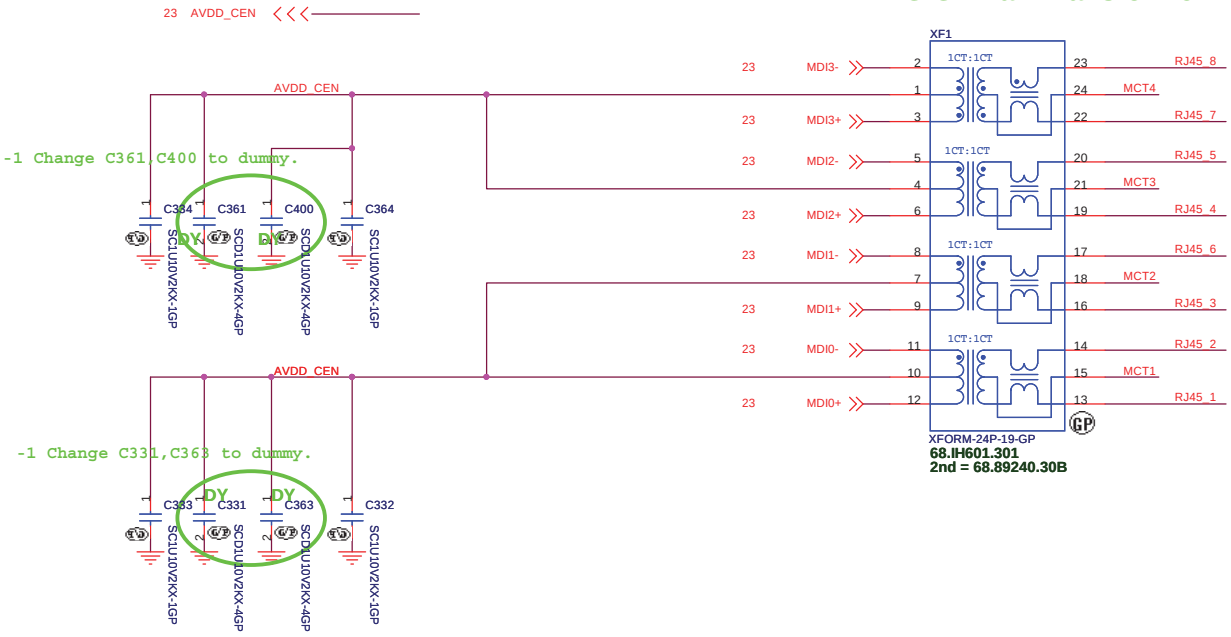
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

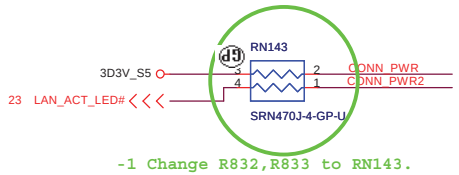


LED COLOR
B1(+) B2(-)::GREEN

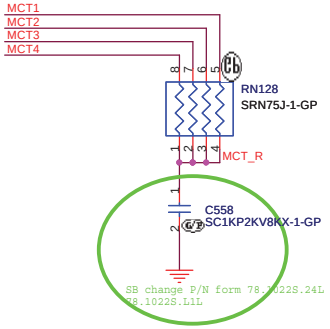
A1(+) A2(-):YELLOW
Green(A3), behavior is the same for 10/100/1000 bits
Yellow(B2), when LAN is transfering data.

Change 單顆
GIGA Lan Transformer

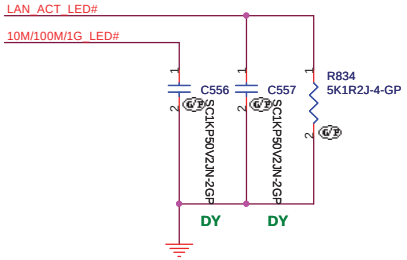




-1 Change R832,R833 to RN143.



SB change P/N form 78.1022S.24L to 78.1022S.L1L



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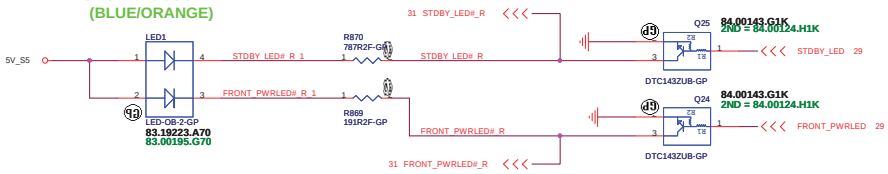
Title	LAN CONN	
Size A3	Document Number SJV10-NL	Rev -1
Date: Tuesday, January 26, 2010	Sheet 24 of 42	

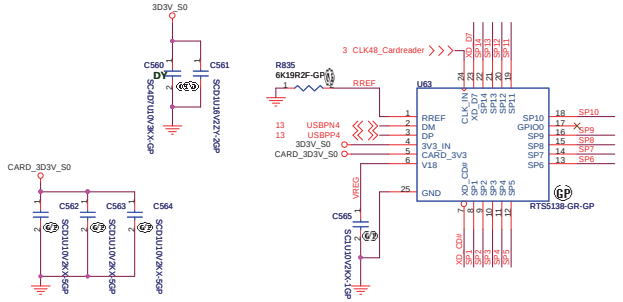
Conn<----------KBC

SYSTEM LED
(BLUE/ORANGE)

Power Button LED
(BLUE/ORANGE)

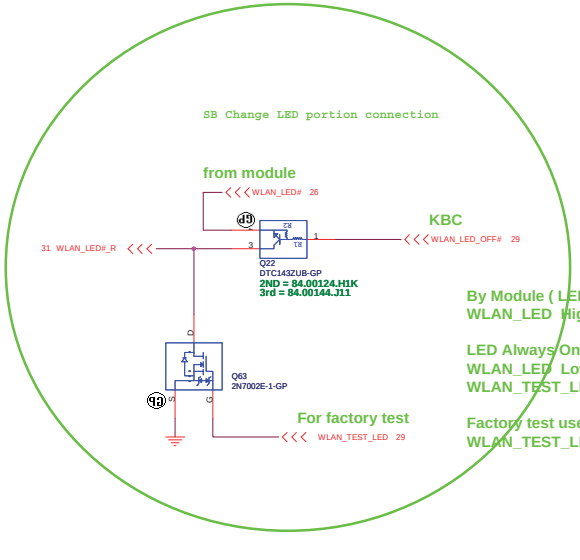


5 IN1 CARD-READER

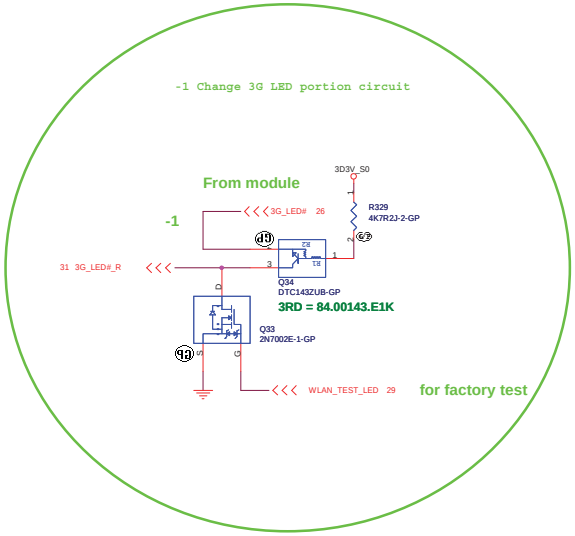


C51,C52,C53 near CARD1 pin23, Pin14, Pin33

SB Change LED portion connection

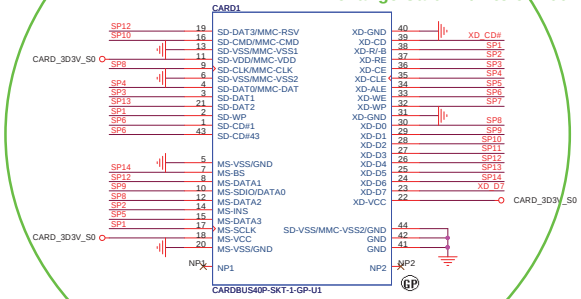


-1 Change 3G LED portion circuit

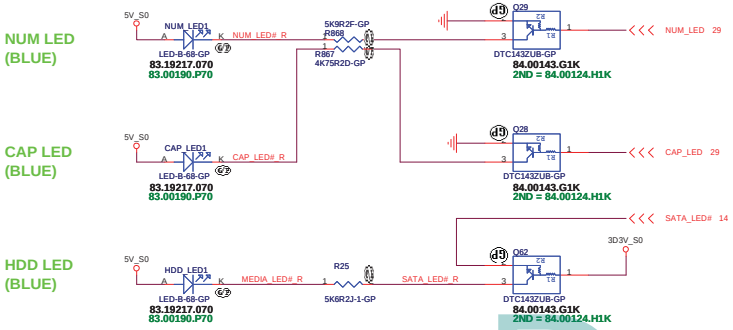


SB change P/N to 20.I0087.011

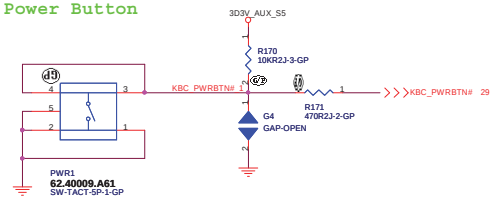
-1 change Card1 P/N to 62.10024.B41



LED Function



Power Button



SJV10-NL

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

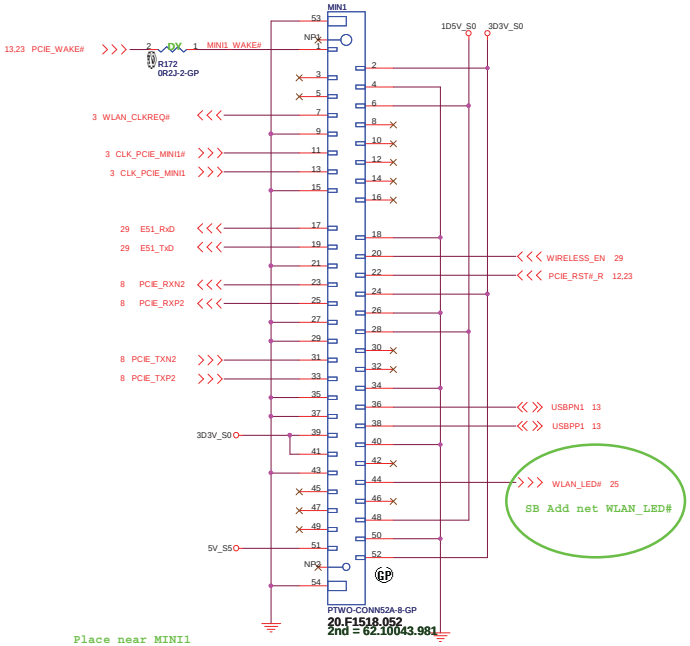
Title: LED_CARD reader

Size: A2 | Document Number: SJV10-NL | Rev: -1

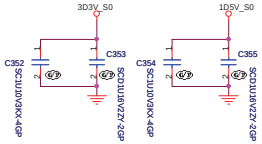
Date: Monday, February 01, 2010 | Sheet 25 of 42

Mini Card Connector(WLAN)

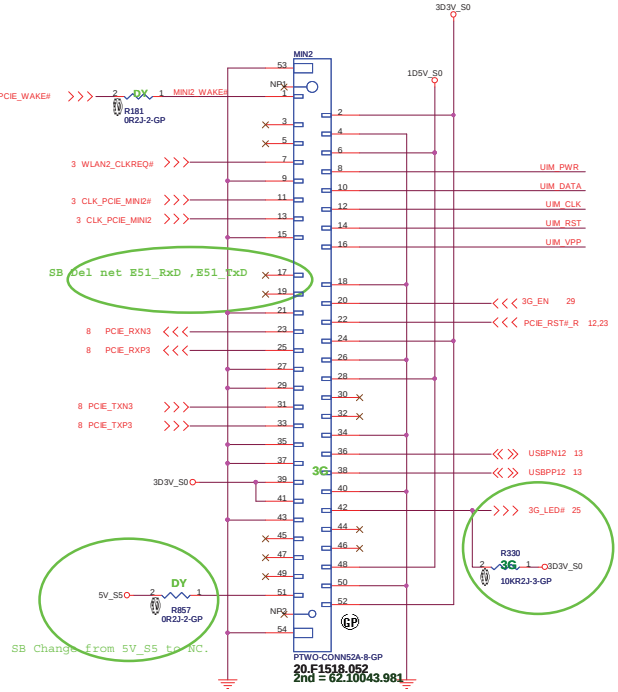
Support debug-card



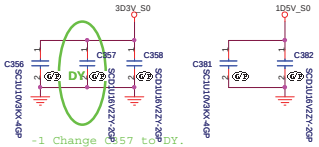
Place near MINI1



Mini Card Connector(3G)

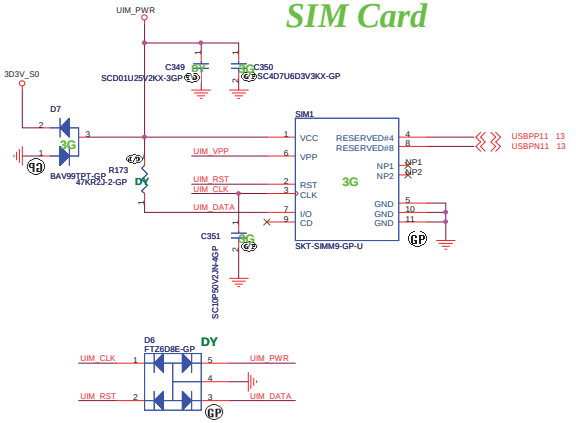


Place near MINIC2



-1 Change C357 to DY.

SIM Card



SJV10-NL

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MINI Conn		
Size: Custom	Document Number: SJV10-NL	Rev: -1
Date: Tuesday, January 26, 2010	Sheet 26 of 42	

Aux Power

3D3V_AUX_S5

5V_AUX_S5

I min = 150 mA

U12

VIN DY VOUT
GND
SHDN# NC#4

G909-330T1U-GP
74.00909.03F

replace :74.09091.J3F

3D3V_AUX_S5_G

G5

GAP-CLOSE-PWR

3D3V_AUX_S5

3D3V_S0

D20

CH521S-30-GP-U1

BC1 SC1U16V2ZY-GP DY

BC2 SC1U16V2ZY-GP DY

Run Power

DCBATOUT

84.S0610.B31
2ND = 84.00610.C31

R174 10KR2J-3-GP Z_12V

Q7 NDS0610-NL-GP

R177 330KR2J-L1-GP Z_12V_G3

RUN_POWER_ON

R175 10KR2J-3-GP

C360 SCD22U25V3KX-GP

R176 330KR2J-L1-GP

D8 PDZ9D1B-GP

83.9R103.C3F
2ND = 83.9R103.F3F

C359 SCD1U25V3KX-GP DY

5V_S0

5V_S5

U13 AO4468-GP GP
84.04468.037

3D3V_S0

3D3V_S5

U14 AO4468-GP GP
84.04468.037

R178 100KR2J-1-GP

Z_12V_D4

R179 100R5J-3-GP DY

3D3V_runpwr

Z_12V_D3

Q8 2N7002E-1-GP
84.2N702.E31
84.2N702.D31
DY

U15 2N7002KDW-GP
84.2N702.A3F
2ND = 84.DM601.03F

PM_SLP_S3# 13,19,28,29,35

R839 1MR2F-GP

1D5V_S0_ON

C566 SC22P50V2JN-4GP

1D5V_S0

1D5V_S3

U16 AO4468-GP GP
84.04468.037

RFC46 RFC47 RFC48 SC22P50V2JN-4GP DY

-1 Reserve RFC46~RFC48
by RF request.

CPU_VDDA_S0

3D3V_S0

RN122 SRN100KJ-6-GP

C503 SC1U10V2KX-1GP

2D5V_S0_PG

D23 BAW56-5-GP

VCORE_EN 33,37

13,19,28,29,35 PM_SLP_S3#

83.00056.Q11
2ND = 83.00056.G11
3rd = 83.00056.K11

3D3V_S0

D24 BAS16-6-GP

28 RUNPWROK

83.00016.F11

R236 10KR2J-3-GP

13,19,28,29,35 PM_SLP_S3#

ALL_PWRGD

U55 74LVC1G08GW-1GP

3D3V_S5

SB_PWRGD 13

73.01G08.L04
73.7SZ08.DAH

Q21 2N7002E-1-GP
84.2N702.E31
84.2N702.D31

3D3V_S0

R180 10KR2J-3-GP

1D1V_S0_PG_1

C511 SC1U10V2KX-1GP

SB change R180,R104,Q4 to placed.

1D1V_S0

R104 2K2R2J-2-GP

1D1V_S0_PG

Q4 MMBT3904-4-GP
84.T3904.C11
2ND = 84.03904.K11

SJV10-NL

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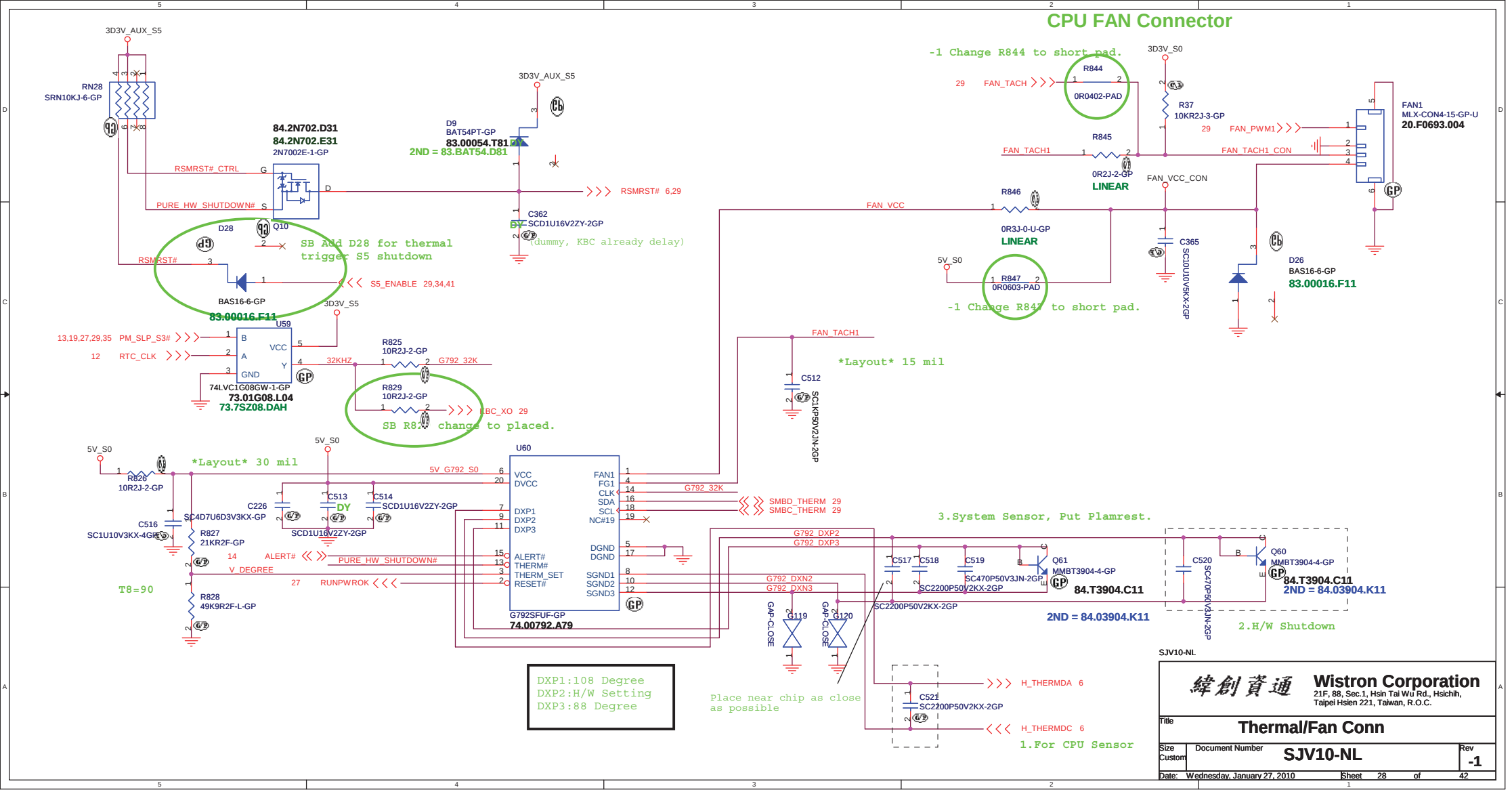
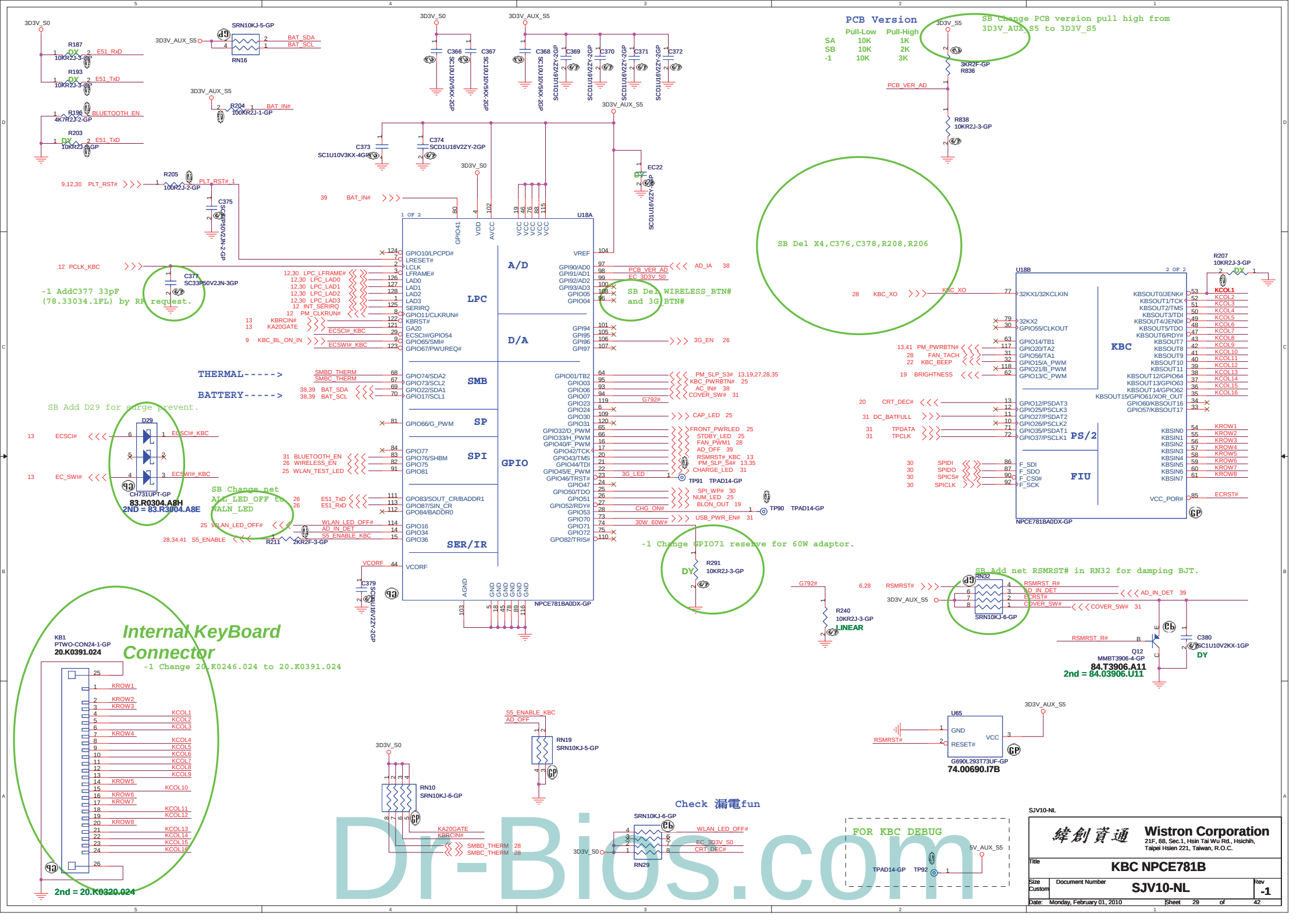
Taipei Hsien 221, Taiwan, R.O.C.

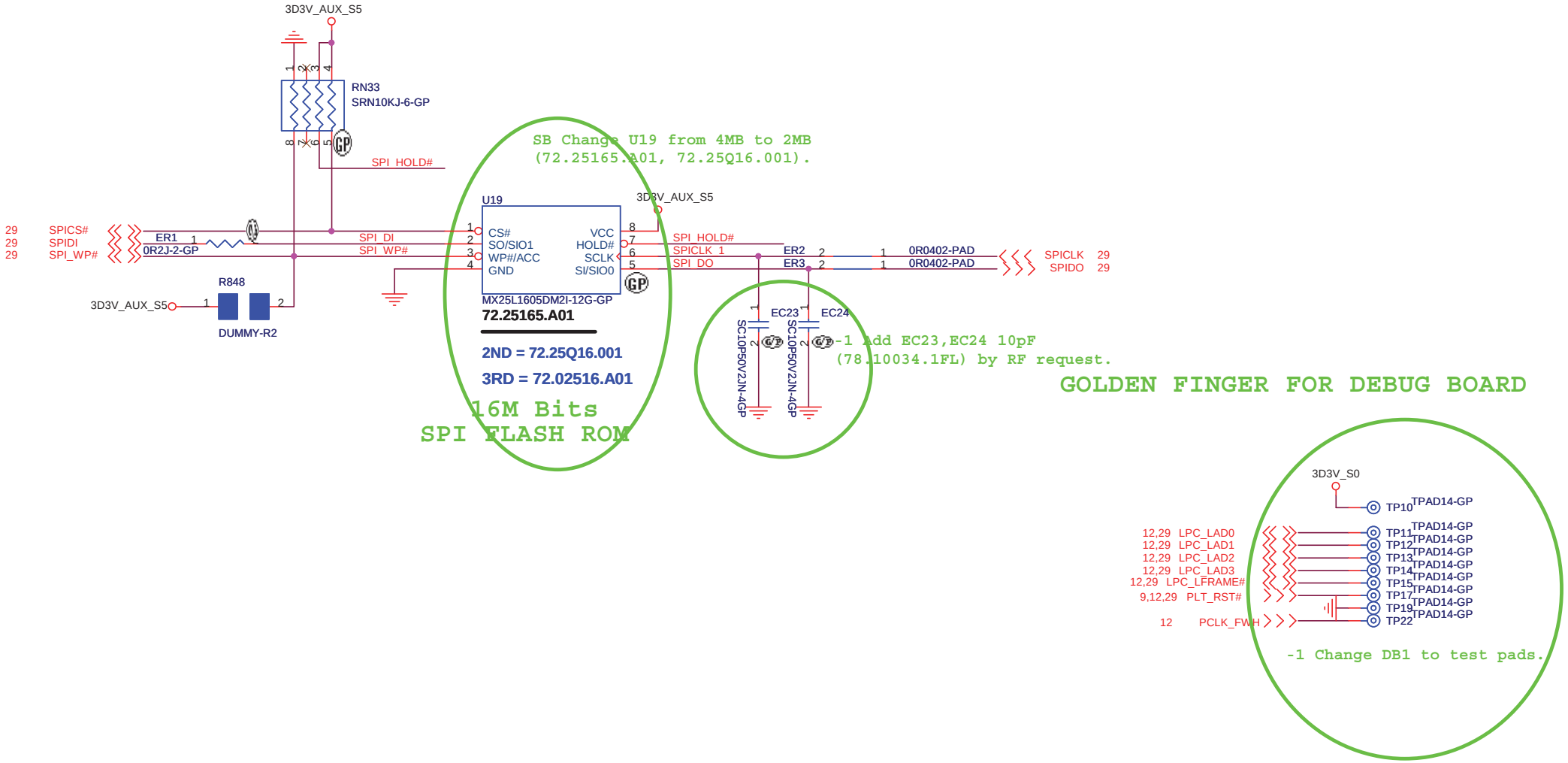
Title: RUN AND AUX POWER

Size	Document Number	Rev
A3	SJV10-NL	-1

Date: Sunday, January 31, 2010 Sheet 27 of 42


CPU FAN Connector
-1 Change R844 to short pad.
-1 Change R847 to short pad.
SB Add D28 for thermal trigger S5 shutdown
SB R829 change to placed.
Layout 15 mil
Layout 30 mil
3.System Sensor, Put Plamrest.
2.H/W Shutdown
1.For CPU Sensor
Place near chip as close as possible
T8=90
DXP1:108 Degree
DXP2:H/W Setting
DXP3:88 Degree
84.2N702.D31
84.2N702.E31
2N7002E-1-GP
83.00054.T81
2ND = 83.BAT54.D81
83.00016.F11
73.01G08.L04
73.7SZ08.DAH
74.00792.A79
84.T3904.C11
2ND = 84.03904.K11
20.F0693.004
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Thermal/Fan Conn
Size Custom
Document Number
SJV10-NL
Rev -1
Date: Wednesday, January 27, 2010
Sheet 28 of 42


PCB Version
Pull-Low Pull-High
SA 10K 1K
SB 10K 2K
-1 10K 3K
SB Change PCB version pull high from 3D3V_AUX_S5 to 3D3V_S5
SB Del X4,C376,C378,R208,R206
SB Del WIRELESS_BTN# and 3G_BTN#
-1 AddC377 33pF (78.33034.1FL) by RF request.
SB Add D29 for surge prevent.
SB Change net ALL_LED_OFF to WALN_LED
-1 Change GPIO71 reserve for 60W adaptor.
SB Add net RSMRST# in RN32 for damping BJT.
Internal KeyBoard Connector
-1 Change 20.K0246.024 to 20.K0391.024
2nd = 20.K0320.024
Check 漏電fun
FOR KBC DEBUG
THERMAL------>
BATTERY------>
U18A
NPCE781BA0DX-GP
KBC
PS/2
FIU
LPC
A/D
D/A
SMB
SP
SPI
GPIO
SER/IR
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
KBC NPCE781B
SJV10-NL
-1
Monday, February 01, 2010
Sheet 29 of 42



SJV10-NL

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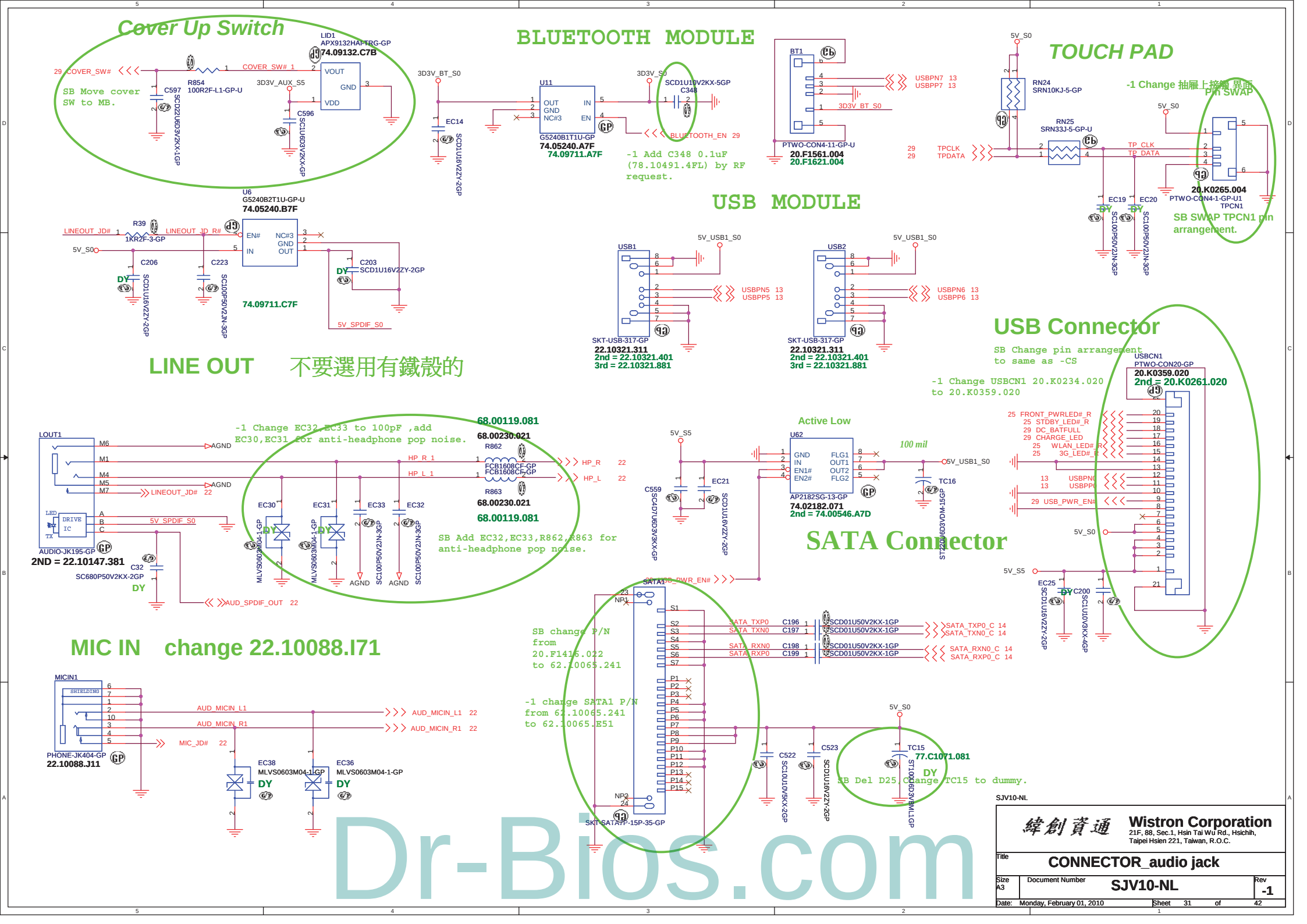
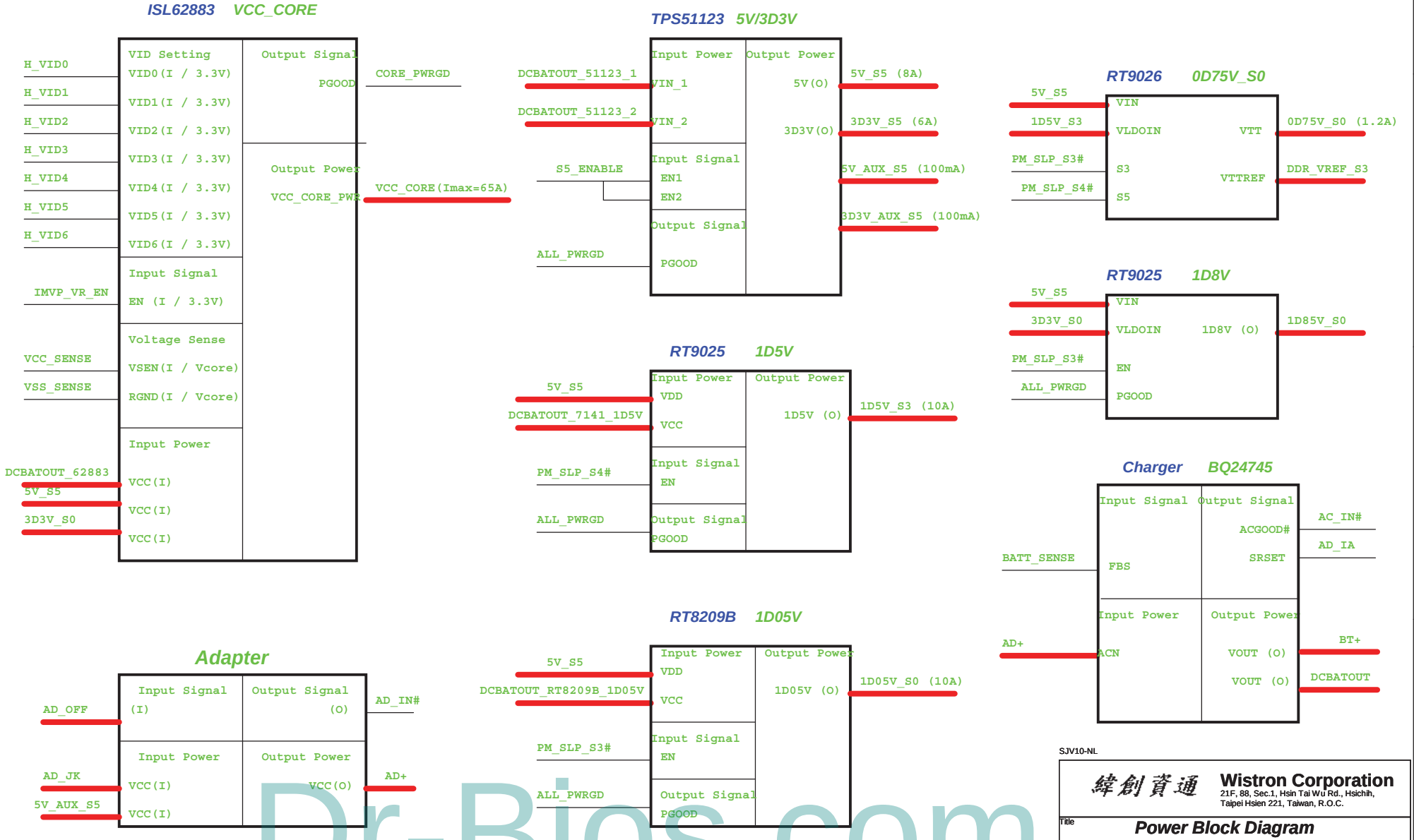
Taipei Hsien 221, Taiwan, R.O.C.

Title: **BIOS**

Size	Document Number	Rev
Custom	SJV10-NL	-1

Date: Friday, January 29, 2010 Sheet 30 of 42


Cover Up Switch
SB Move cover SW to MB.
LID1
APX9132HAFTRG-GP
74.09132.C7B
29 COVER_SW#
COVER_SW# 1
R854
100R2F-L1-GP-U
C597
SCD2U6D3V2KX-1GP
3D3V_AUX_S5
C596
SC1U6D3V2KX-GP
VOUT
GND
VDD
BLUETOOTH MODULE
3D3V_BT_S0
EC14
SCD1U16V2ZY-2GP
U11
G5240B1T1U-GP
74.05240.A7F
74.09711.A7F
OUT
GND
NC#3
IN
EN
3D3V_S0
SCD1U10V2KX-5GP
C348
BLUETOOTH_EN 29
-1 Add C348 0.1uF (78.10491.4FL) by RF request.
BT1
USBPN7 13
USBPP7 13
3D3V_BT_S0
PTWO-CON4-11-GP-U
20.F1561.004
20.F1621.004
TOUCH PAD
5V_S0
RN24
SRN10KJ-5-GP
RN25
SRN33J-5-GP-U
29 TPCLK
29 TPDATA
TP_CLK
TP_DATA
-1 Change 抽屜上接觸 異面 Pin SWAP
20.K0265.004
PTWO-CON4-1-GP-U1
TPCN1
EC19
EC20
SC100P50V2JN-3GP
SB SWAP TPCN1 pin arrangement.
U6
G5240B2T1U-GP-U
74.05240.B7F
LINEOUT_JD#
LINEOUT_JD_R#
R39
1KR2F-3-GP
C206
C223
C203
SCD1U16V2ZY-2GP
SC100P50V2JN-3GP
74.09711.C7F
5V_SPDIF_S0
USB MODULE
USB1
USB2
5V_USB1_S0
USBPN5 13
USBPP5 13
USBPN6 13
USBPP6 13
SKT-USB-317-GP
22.10321.311
2nd = 22.10321.401
3rd = 22.10321.881
USB Connector
SB Change pin arrangement to same as -CS
-1 Change USBCN1 20.K0234.020 to 20.K0359.020
USBCN1
PTWO-CON20-GP
20.K0359.020
2nd = 20.K0261.020
LINE OUT 不要選用有鐵殼的
LOUT1
AUDIO-JK195-GP
2ND = 22.10147.381
C32
SC680P50V2KX-2GP
DY
AGND
LINEOUT_JD# 22
5V_SPDIF_S0
AUD_SPDIF_OUT 22
-1 Change EC32,EC33 to 100pF ,add EC30,EC31 for anti-headphone pop noise.
68.00119.081
68.00230.021
R862
R863
FCB1608CF-GP
HP_R_1
HP_L_1
HP_R 22
HP_L 22
EC30
EC31
EC33
EC32
MLVS0603M04-1-GP
SC100P50V2JN-3GP
SB Add EC32,EC33,R862,R863 for anti-headphone pop noise.
Active Low
U62
AP2182SG-13-GP
74.02182.071
2nd = 74.00546.A7D
100 mil
5V_USB1_S0
TC16
ST220U6D3VDM-15GP
C559
SC4D7U6D3V3KX-GP
EC21
SCD1U16V2ZY-2GP
SATA Connector
SATA1
SKT-SATA7P-15P-35-GP
SATA_TXP0
SATA_TXN0
SATA_RXN0
SATA_RXP0
C196
C197
C198
C199
SCD01U50V2KX-1GP
SATA_TXP0_C 14
SATA_TXN0_C 14
SATA_RXN0_C 14
SATA_RXP0_C 14
SB change P/N from 20.F1416.022 to 62.10065.241
-1 change SATA1 P/N from 62.10065.241 to 62.10065.E51
C522
C523
SC10U10V5KX-2GP
SCD1U16V2ZY-2GP
TC15
77.C1071.081
SB Del D25,Change TC15 to dummy.
MIC IN change 22.10088.I71
MICIN1
PHONE-JK404-GP
22.10088.J11
AUD_MICIN_L1
AUD_MICIN_R1
MIC_JD# 22
EC38
EC36
MLVS0603M04-1-GP
SJV10-NL
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
CONNECTOR_audio jack
Size A3
Document Number
SJV10-NL
Rev -1
Date: Monday, February 01, 2010
Sheet 31 of 42
Dr-Bios.com



SJV10-NL

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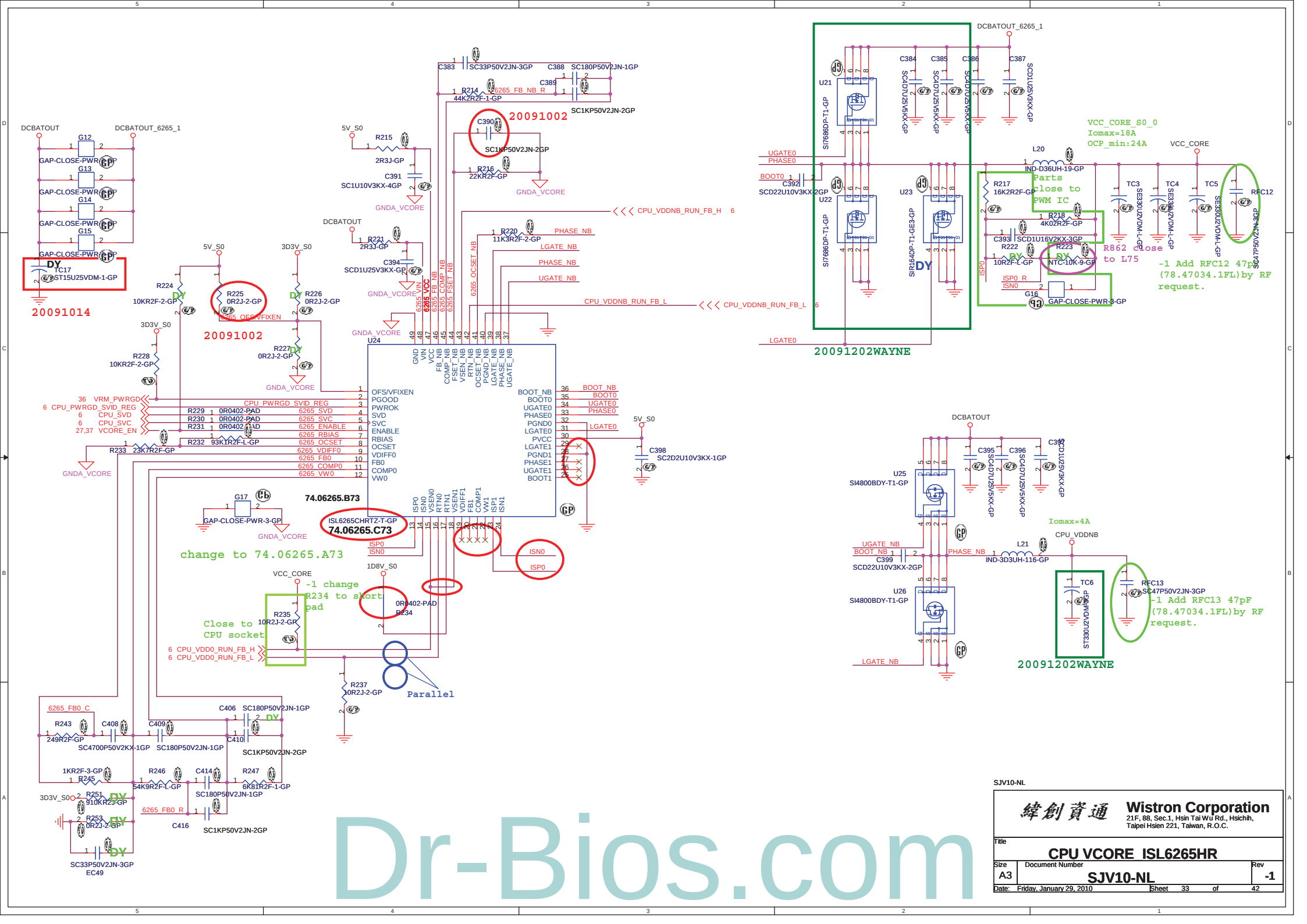
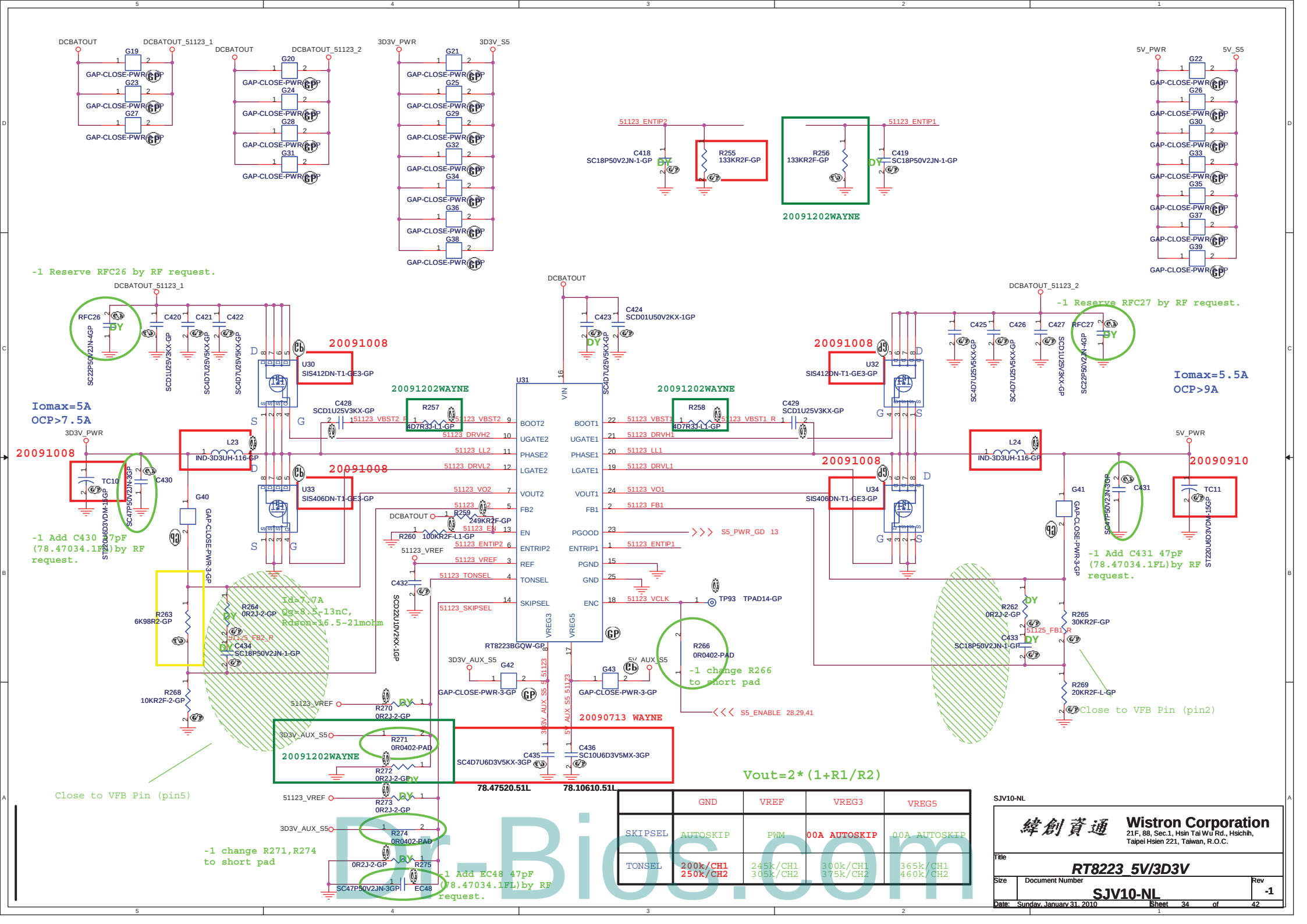
Title: Power Block Diagram

Size	Document Number	Rev
	SJV10-NL	-1

Date: Tuesday, January 05, 2010 Sheet 32 of 42


DCBATOUT
DCBATOUT_6265_1
GAP-CLOSE-PWR-GP
DY
ST15U25VDM-1-GP
20091014
5V_S0
3D3V_S0
R224 10KR2F-2-GP
R225 0R2J-2-GP
R226 0R2J-2-GP
R227 0R2J-2-GP
R228 10KR2F-2-GP
6265_OFS_VFIXEN
20091002
GNDA_VCORE
U24
OFS/VFIXEN
PGOOD
PWROK
SVD
SVC
ENABLE
RBIAS
OCSET
VDIFF0
FB0
COMP0
VW0
BOOT_NB
BOOT0
UGATE0
PHASE0
PGND0
LGATE0
PVCC
LGATE1
PGND1
PHASE1
UGATE1
BOOT1
ISL6265CHRTZ-T-GP
74.06265.C73
74.06265.B73
G17
GAP-CLOSE-PWR-3-GP
change to 74.06265.A73
1D8V_S0
VCC_CORE
-1 change R234 to short pad
0R0402-PAD R234
R235 10R2J-2-GP
Close to CPU socket
R237 10R2J-2-GP
Parallel
6 CPU_VDD0_RUN_FB_H
6 CPU_VDD0_RUN_FB_L
6265_FB0_C
R243 249R2F-GP
C408 SC4700P50V2KX-1GP
C409 SC180P50V2JN-1GP
C406 SC180P50V2JN-1GP
C410 SC1KP50V2JN-2GP
R245 1KR2F-3-GP
R246 54K9R2F-L-GP
C414 SC180P50V2JN-1GP
R247 6K81R2F-1-GP
R251 910KR2J-GP
R253 0R2J-2-GP
6265_FB0_R
C416 SC1KP50V2JN-2GP
SC33P50V2JN-3GP EC49
C383 SC33P50V2JN-3GP
C388 SC180P50V2JN-1GP
C389 SC1KP50V2JN-2GP
R214 44K2R2F-1-GP
6265_FB_NB_R
C390 SC1KP50V2JN-2GP
R216 22KR2F-GP
R215 2R3J-GP
C391 SC1U10V3KX-4GP
R221 2R3J-GP
C394 SCD1U25V3KX-GP
R220 11K3R2F-2-GP
PHASE_NB
LGATE_NB
UGATE_NB
CPU_VDDNB_RUN_FB_H 6
CPU_VDDNB_RUN_FB_L 6
6265_VIN
6265_VCC
6265_FB_NB
6265_COMP_NB
6265_FSET_NB
6265_OCSET_NB
C398 SC2D2U10V3KX-1GP
ISP0
ISN0
DCBATOUT_6265_1
U21 SI7686DP-T1-GP
U22 SI7686DP-T1-GP
U23 SIR164DP-T1-GE3-GP
C384 SC4D7U25V5KX-GP
C385 SC4D7U25V5KX-GP
C386 SC4D7U25V5KX-GP
C387 SCD1U25V3KX-GP
UGATE0
PHASE0
BOOT0
C392 SCD22U10V3KX-2GP
LGATE0
20091202WAYNE
VCC_CORE_S0_0
Iomax=18A
OCP_min:24A
L20 IND-D36UH-19-GP
VCC_CORE
Parts close to PWM IC
R217 16K2R2F-GP
R218 4K02R2F-GP
C393 SCD1U16V2KX-3GP
R222 10R2F-L-GP
R223 NTC-10K-9-GP
R862 close to L75
ISP0_R
ISN0
G16 GAP-CLOSE-PWR-8-GP
TC3 SE330U2VDM-L-GP
TC4 SE330U2VDM-L-GP
TC5 SE330U2VDM-L-GP
RFC12 SC47P50V2JN-3GP
-1 Add RFC12 47pF (78.47034.1FL)by RF request.
U25 SI4800BDY-T1-GP
U26 SI4800BDY-T1-GP
C395 SC4D7U25V5KX-GP
C396 SC4D7U25V5KX-GP
C397 SCD1U25V3KX-GP
Iomax=4A
CPU_VDDNB
L21 IND-3D3UH-116-GP
C399 SCD22U10V3KX-2GP
UGATE_NB
BOOT_NB
PHASE_NB
LGATE_NB
TC6 ST330U2VDM-GP
RFC13 SC47P50V2JN-3GP
-1 Add RFC13 47pF (78.47034.1FL)by RF request.
20091202WAYNE
SJV10-NL
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU VCORE ISL6265HR
Size A3
Document Number SJV10-NL
Rev -1
Date: Friday, January 29, 2010
Sheet 33 of 42



	GND	VREF	VREG3	VREG5
SKIPSEL	AUTOSKIP	PWM	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

SJV10-NL

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **RT8223_5V/3D3V**

Size	Document Number	Rev
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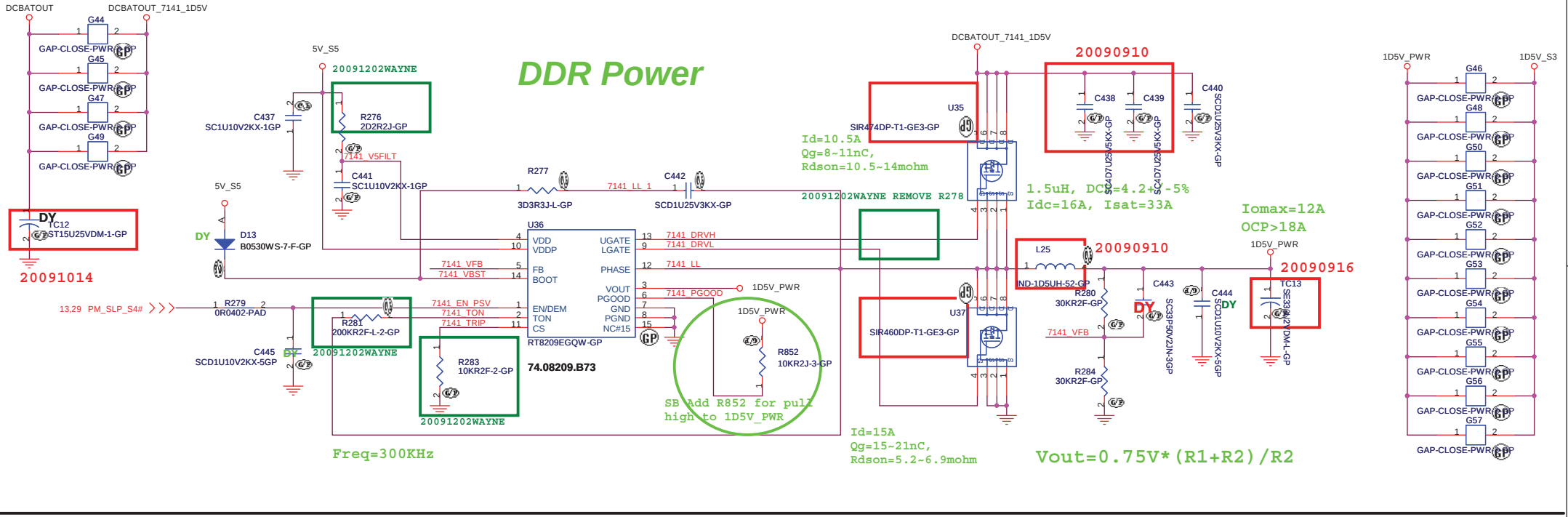
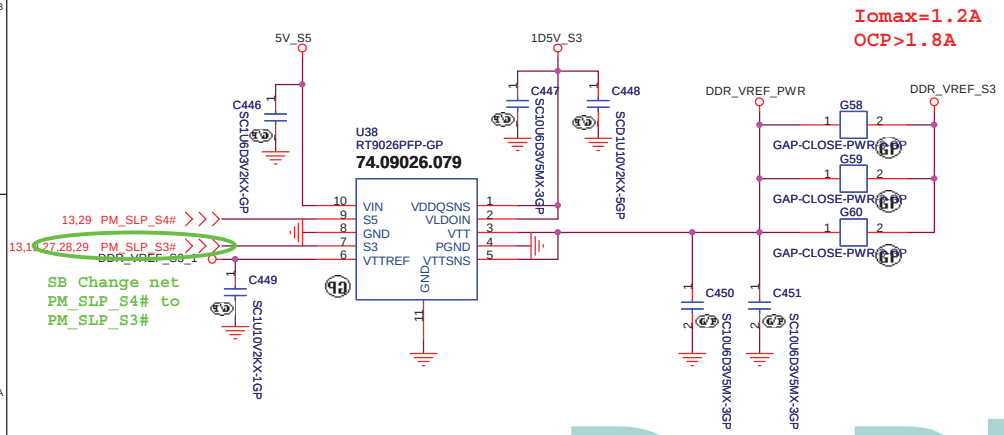


RT9026 for DDR_VREF_S3_1

DDR_VREF_S3



SJV10-NL

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title	*RT8209E_1D5V/RT9026_0D75V*	
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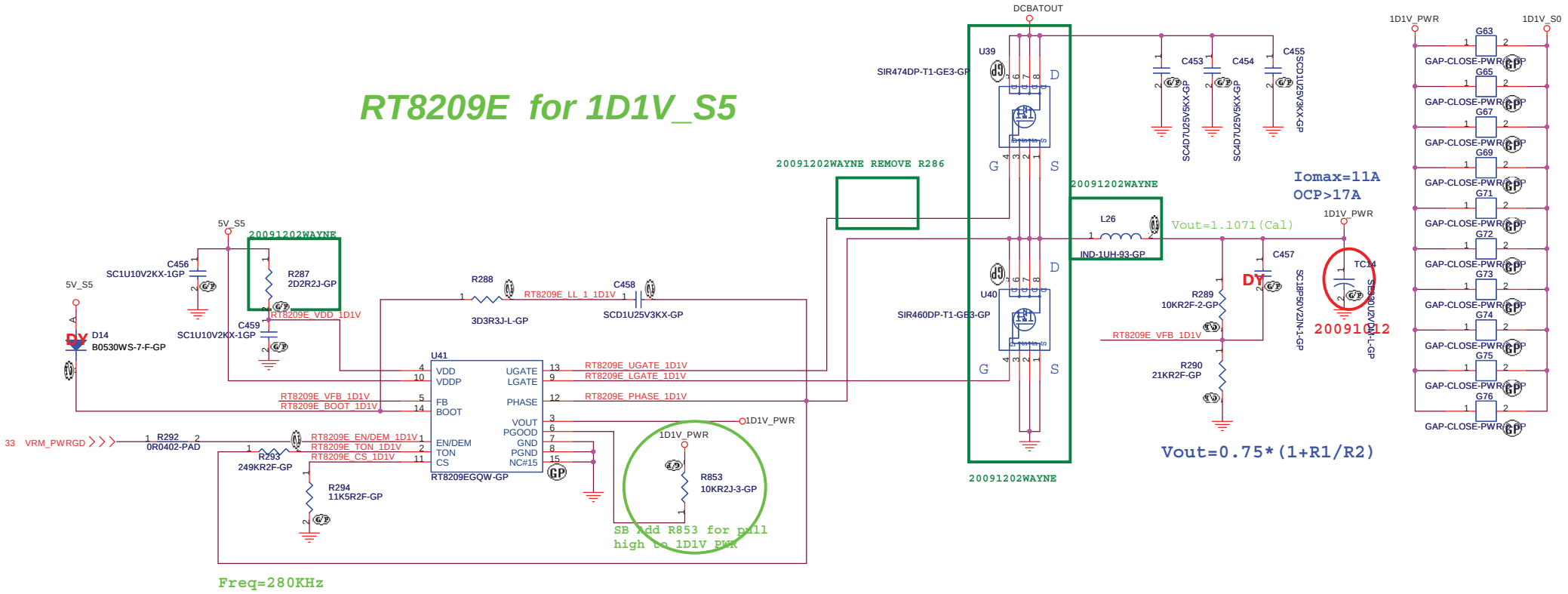
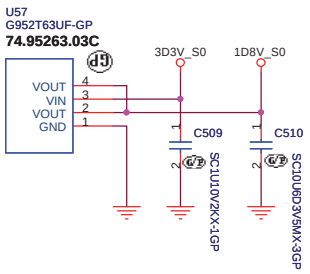
RT8209E for 1D1V_S5



1.8V_S0 1.8V 1A Regulator



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Title: **RT8209E_1D1V/LDO 1D8V**

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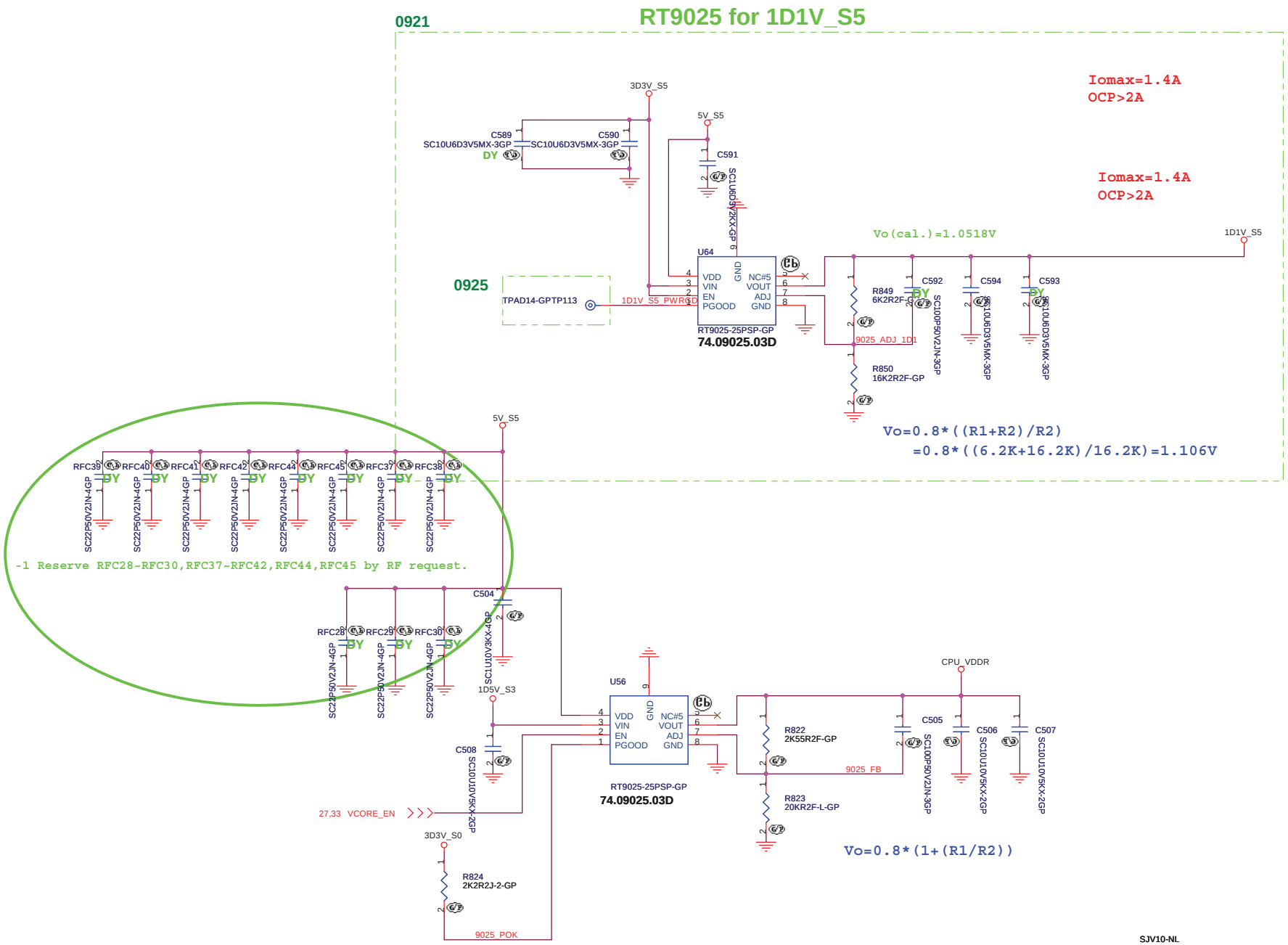

SJV10-NL

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Taipei Hsien 221, Taiwan, R.O.C.

Title: LDO 1D5_S0 0D9_S0

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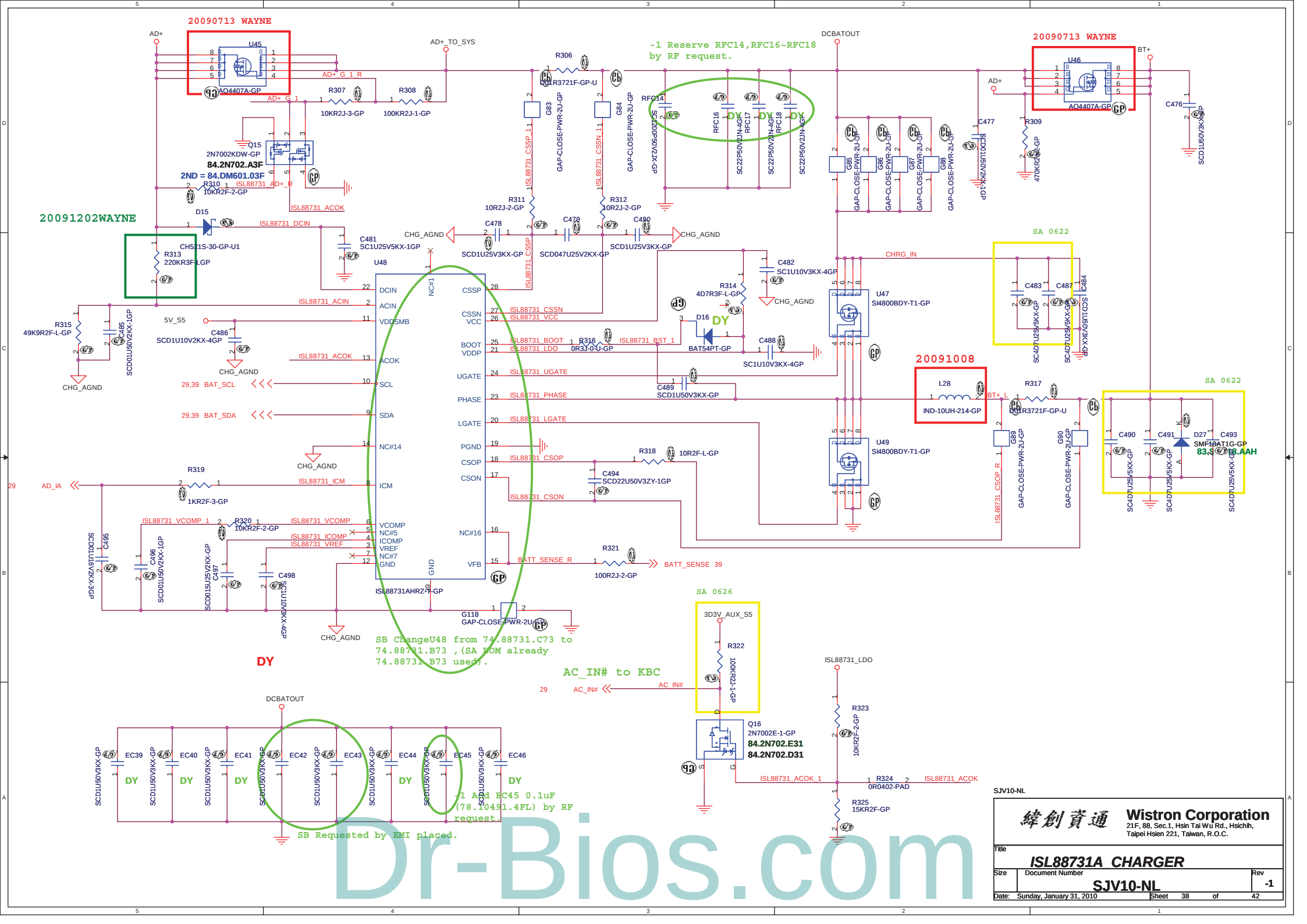
20090713 WAYNE
AD+
U45
AO4407A-GP
AD+_TO_SYS
AD+_G_1_R
AD+_G_1
R307
10KR2J-3-GP
R308
100KR2J-1-GP
R306
0R3721F-GP-U
-1 Reserve RFC14,RFC16~RFC18
by RF request.
DCBATOUT
20090713 WAYNE
U46
AO4407A-GP
BT+
C476
SCD1U50V3KX-GP
Q15
2N7002KDW-GP
84.2N702.A3F
2ND = 84.DM601.03F
R310
10KR2F-2-GP
ISL88731_AD+_R
ISL88731_ACOK
20091202WAYNE
D15
ISL88731_DCIN
CH571S-30-GP-U1
R313
220KR3F-1-GP
C481
SC1U25V5KX-1GP
CHG_AGND
R311
10R2J-2-GP
R312
10R2J-2-GP
C478
SCD1U25V3KX-GP
C479
SCD047U25V2KX-GP
C480
SCD1U25V3KX-GP
ISL88731_CSSP
ISL88731_CSSN
G83
GAP-CLOSE-PWR-2U-GP
G84
GAP-CLOSE-PWR-2U-GP
RFC14
SCD220P50V2JX-GP
RFC16
SC22P50V2JN-4GP
RFC17
SC22P50V2JN-4GP
RFC18
SC22P50V2JN-4GP
DY
G85
G86
G87
G88
GAP-CLOSE-PWR-2U-GP
C477
SCD001U50V2KX-1GP
R309
470KR2J-GP
SA 0622
CHRG_IN
C482
SC1U10V3KX-4GP
R314
4D7R3F-L-GP
D16
BAT54PT-GP
C488
SC1U10V3KX-4GP
U47
SI4800BDY-T1-GP
U49
SI4800BDY-T1-GP
C483
C487
C484
SC4D7U25V5KX-GP
SCD1U50V3KX-GP
20091008
L28
IND-10UH-214-GP
BT+_L
R317
0R3721F-GP-U
C490
C491
D27
SMF18AT1G-GP
C493
SC4D7U25V5KX-GP
83.SCF18.AAH
R315
49K9R2F-L-GP
C485
SCD01U50V2KX-1GP
5V_S5
C486
SCD1U10V2KX-4GP
ISL88731_ACIN
ISL88731_ACOK
29,39 BAT_SCL
29,39 BAT_SDA
U48
DCIN
ACIN
VDDSMB
SCL
SDA
NC#14
ICM
VCOMP
NC#5
ICOMP
VREF
NC#7
GND
NC#1
CSSP
CSSN
VCC
BOOT
VDDP
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC#16
VFB
ISL88731AHRZ-T-GP
ISL88731_CSSN
ISL88731_VCC
ISL88731_BOOT
ISL88731_LDO
ISL88731_BST_1
R316
0R3J-0-U-GP
ISL88731_UGATE
ISL88731_PHASE
ISL88731_LGATE
C489
SCD1U50V3KX-GP
R318
10R2F-L-GP
C494
SCD22U50V3ZY-1GP
ISL88731_CSOP
ISL88731_CSON
R319
1KR2F-3-GP
AD_IA
ISL88731_ICM
ISL88731_VCOMP_1
R320
10KR2F-2-GP
ISL88731_VCOMP
ISL88731_ICOMP
ISL88731_VREF
C495
SCD01U50V2KX-1GP
C496
SCD01U50V2KX-1GP
C497
SCD015U25V2KX-GP
C498
SC1U10V3KX-4GP
R321
100R2J-2-GP
BATT_SENSE_R
BATT_SENSE 39
G118
GAP-CLOSE-PWR-2U-GP
CHG_AGND
SB ChangeU48 from 74.88731.C73 to
74.88731.B73 ,(SA ROM already
74.88731.B73 used).
DY
SA 0626
3D3V_AUX_S5
R322
100KR2J-1-GP
AC_IN# to KBC
AC_IN#
Q16
2N7002E-1-GP
84.2N702.E31
84.2N702.D31
ISL88731_ACOK_1
R323
10KR2F-2-GP
R324
0R0402-PAD
R325
15KR2F-GP
DCBATOUT
EC39
EC40
EC41
EC42
EC43
EC44
EC45
EC46
SCD1U50V3KX-GP
DY
Add EC45 0.1uF
(78.10491.4FL) by RF
request.
SB Requested by EMI placed.
SJV10-NL
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL88731A CHARGER
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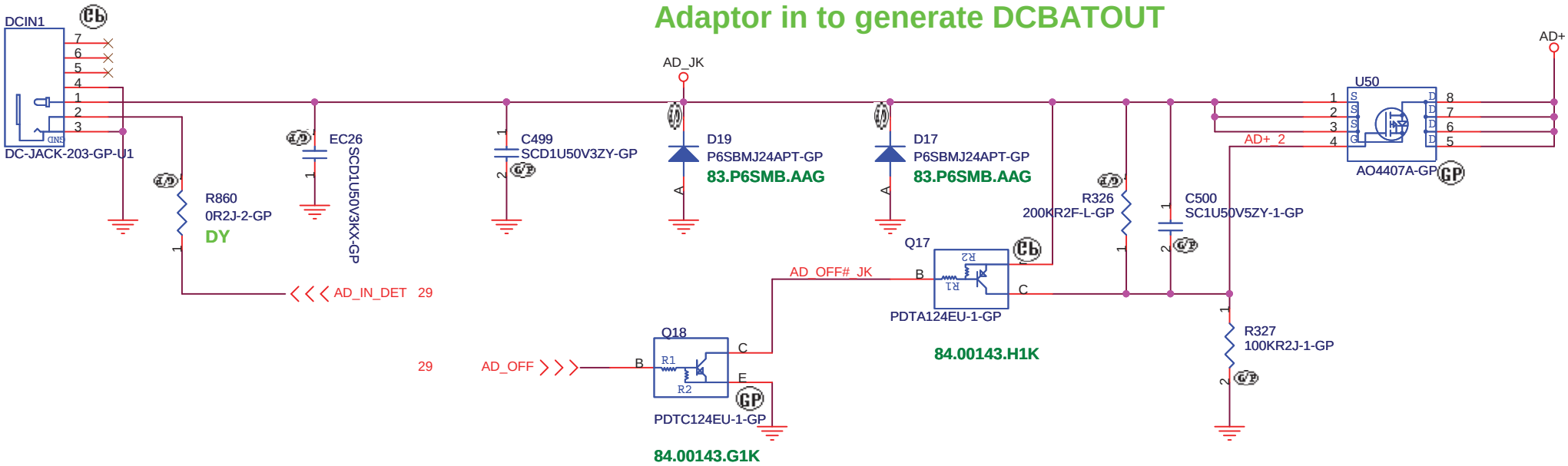
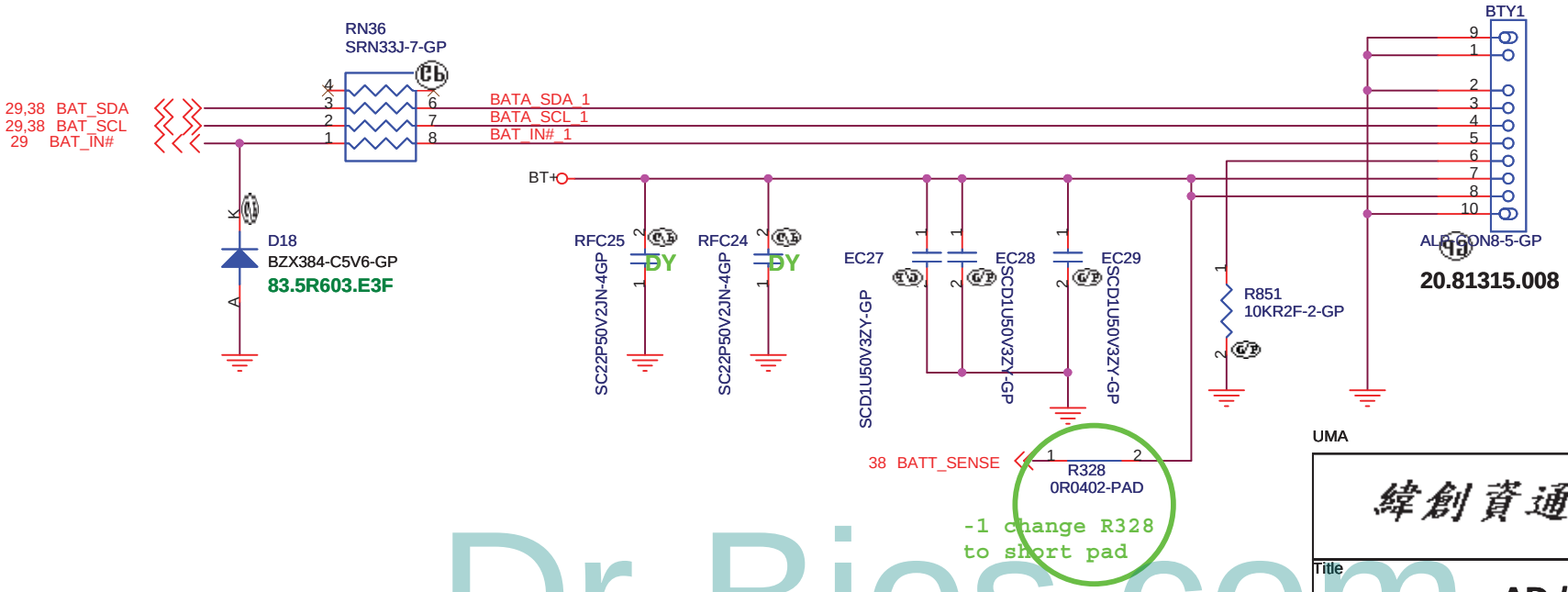
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
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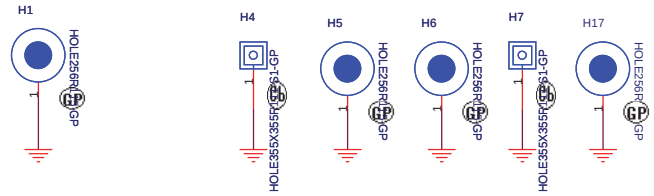
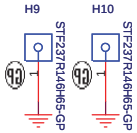


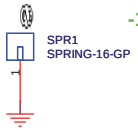
MB HOLE

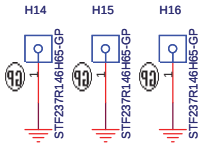


MINI CARD BOSS

SPRING

-1 Add SPR1 for RTC battery.

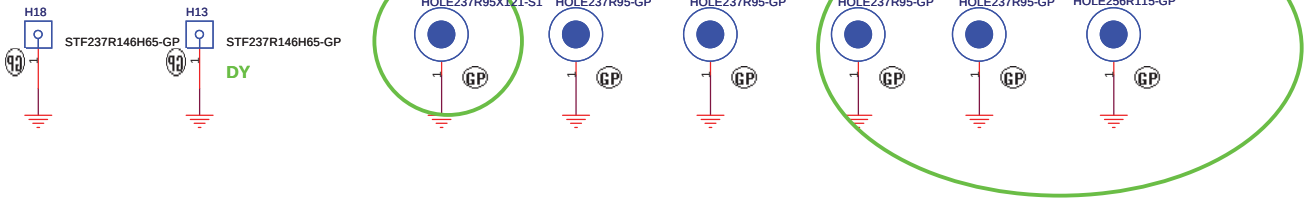




CPU NB BOSS

-1 Change H19 shape

SB Add H22,H23,H24 for ME request.



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Title: ***EMI/Spring/Boss***

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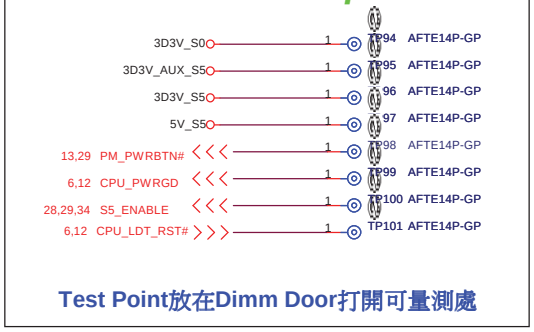
Check test point



Test Point放在Dimm Door打開可量測處

SJV10-NL

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Title	***AFTE_TP***	
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SB Change notice:
1. Change C344 from 10uF to 0.1uF for anti pop noise.(Page 22)
2. ChangeU48 circuit from 74.88731.C73 to 74.88731.B73 ,(SA BOM already 74.88731.B73 used.).(Page 38)
3. SWAP TPCN1pin arrangement.(Page 31)
4. Change U19 to 2MB(72.25165.A01, 72.25016.A01).(Page 30)
5. X1 need to change to the same as JV10-CS (82.30005.A51).(Page 3)
6. Del X4,C376,C378,R208,R206 ,R829 change to placed.(Page 28,29)
7. Add G122 (Page 12).
8. Add net RSMRST# in RN32 for damping BJT.(Page 29)
9. X5 2nd source change from 82.30005.C51 to 82.30020.A31,Change C540 from 27pF to 18pF,Change C541 from 27pF to 15pF(Page 23)
10. R272 change to dummy.(Page 34)
11. Change R43 from Dummy to 1M ohm.(Page 12)
12. Del R285, Add R852,R853 for pull high to 1D1V_PWR and 1D5V_PWR.(Page 35,36)
13. Change RN30 form page31 to page 22.
14. Add D28 for thermal trigger S5 shutdown.(Page 28)
15. Del net RSMRST#_SB pull high , Change S5_PWR_GD pull high from R261 to RN43.(Page 13)
16. Change pin arrangement to same as -CS, move cover SW to MB,Del WIRELESS_BTN# and 3G_BTN#. (Page 29,31)
17. Change PCB version pull high from 3D3V_AUX_S5 to 3D3V_S5,R836 1K change to 2K (page29).
18. Change GPIO16 net name from ALL_LED_OFF to WLAN_LED .(page29)
19. Change C558 1000pF P/N form 78.1022S.24L to 78.1022S.L1L.(page24)
20. Change capacity from 6.8pF (78.6R864.1FL) to 5.6pF (78.5R674.1FL)(page20).
21. Change net PCLK_FWH to LPCCLK0_R change net PCLK_KBC to LPCCLK1_R(page16).
22. Change R180,R104,Q4 to placed(page27).
23. Change P/N from 20.F1416.022 to 62.10065.241(page31).
24. Add D29 for surge prevent.(page29).
25. Change Mini card 3G pin41 from 5V_S5 to NC.(page26).
26. Add C598 for solve CRT flicker issue (page9).
27. Change R859 from 150 ohm to 140 ohm (page20).
28. Add H22,H23,H24 for ME request. (page40).
29. Del net E51_RxD ,E51_TxD (page26).
30. Change R71 from bead 470 ohm to RES 3.9 ohm(page9).
31. Del D25.(page31).
32. Add RTC charge circuit.(page12).
33. EC42,EC43 requested by EMI placed.(page38).
34. Change LCD1 P/N from 20.F1093.040 to 20.F1703.040(page19).
35. Change net PM_SLP_S4# to PM_SLP_S3#.(page35).
36. Add EC32,EC33,R862,R863 for anti-headphone pop noise.(page31)
37. Change C189 to 22pF, C190 to 15pF.(page12)
38. Change TC15 to dummy.(page31)

-1 change notices:
1. Change R91,R92 to RN132,R27,R30 to RN133,R34~R36 to RN134.(Page 3)
2. DY C35,C42,C80,Change C36,C43,C569,C79 to 22uF.(Page 7)
3. Change R60,R62 to RN136.(Page 9)
4. Change R84,R85 to RN137,R76,R78 to RN138,R22,R79 to RN139.DY C139,Change C140 to 22uF.(Page 10)
5. Change R89,R88 to RN140.(Page 12)
6. Change R133,R135,R136,R128 to RN141,R138,R139 to RN142.(Page 16)
7. Change C266,C281 to dummy.(Page 17)
8. Change C287,C293,C302 to dummy.(Page 18)
9. Change R16 to short PAD.(Page 19)
10. Change C532 to dummy.(Page 23)
11. Change C331,C400,C361,C363 to dummy,change R832,R833 to RN143.(Page 24)
12. Change C357 to dummy.(Page 26)
13. Change R844,R847 to short pad.(Page 28)
14. Add reserved R865, change pull high to 3D3V_S5.(Page 23)
15. Change 10u/25V(78.10622.51L)to 4.7u/25V(78.47522.51L)(Page 19)
16. Change C483,C423,C487,C490,C491,C493. 10u/25V(78.10622.51L)to 4.7u/25V(78.47522.51L)(Page 34,38)
17. Change USBCN1 20.K0234.020 to 20.K0359.020 (Page 31)
18. Change KB1 20.K0246.024 to 20.K0391.024(Page 29)
19. Change R234 to short pad.(Page 33)
20. Change R266,R271,R274 to short pads.(Page 34)
21. Change R328 to short pad.(Page 39)
22. Change 3G LED portion circuit.(Page 26)
23. Change R166 to reserved D21.(Page 22)
24. Change 抽屜上接觸 異面.(Page 31)
25. Add SPR1 for RTC battery.(Page 40)
26. Add VRAM identify pins.(Page 12)
27. Change EC32,EC33 to 100pF,add EC30,EC31 for anti-headphone pop noise(Page 31)
28. Change GPIO71 reserve for 60W adaptor.(Page 29)
29. Reserve EC47 for EMI issue.(Page 13)
30. Change DB1 to test pads.(Page 30)
31. Change C12,C20,C193 to 12pF,C541 to 18pF.(Page 3,12,23)
32. Add R335,EC74~EC79 for AGND connect.(Page 22)
33. Change Card1 P/N to 62.10024.B41(Page 25)
34. Change 10u/25V(78.10622.51L)to 10u/16V(78.10621.52L)(Page 19)
35. Change SATA1 P/N from 62.10065.241 to 62.10065.E51.(Page 31)
36. Add F4,D25 for ESD function.(Page 21)
37. Reserve C310,RFC1,RFC11,RFC14,RFC16~RFC19,RFC22,RFC24~RFC30,RFC37~RFC42,RFC44~RFC48 by RF request.(Page 3,18,1

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Title: Modify History

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