

Compal Confidential

NAV70 Schematics Document

Intel Pineview Processor with Tigerpoint + DDRII

2010-04-29

REV: 2.0

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File Name : LA-5651P

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To I/O Board Conn.
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To I/O board
Card Reader
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page 20

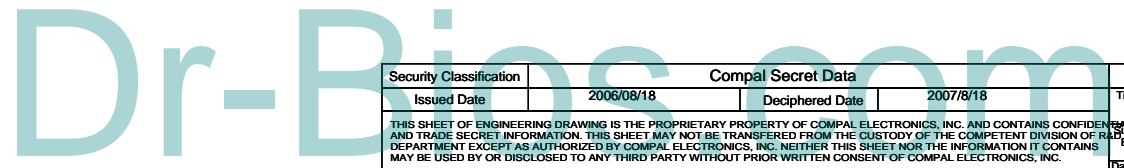
AMP & INT
Speaker

INT MIC

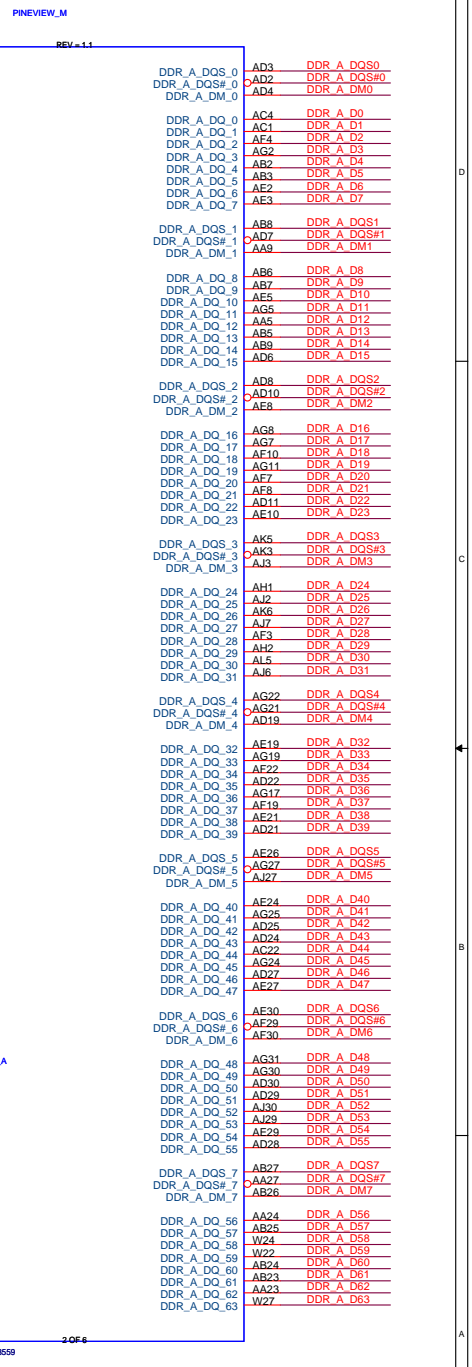
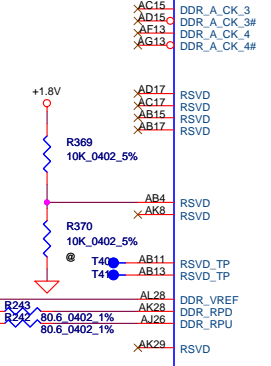
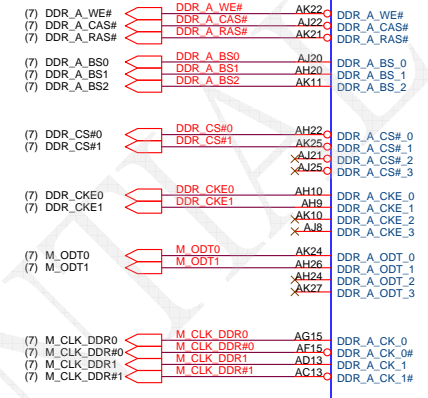
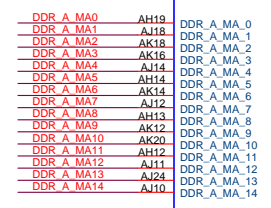
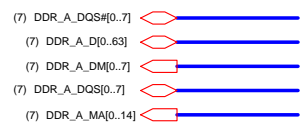
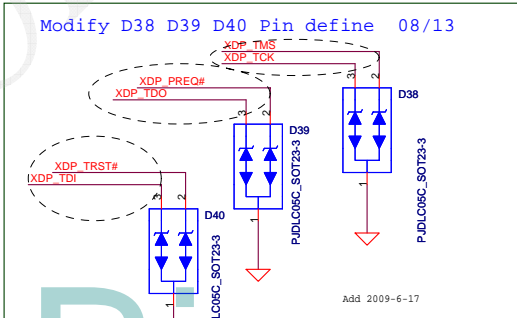
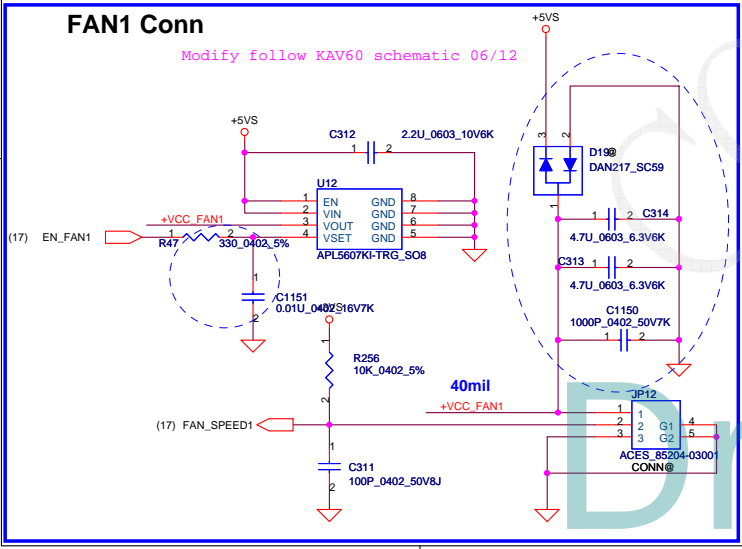
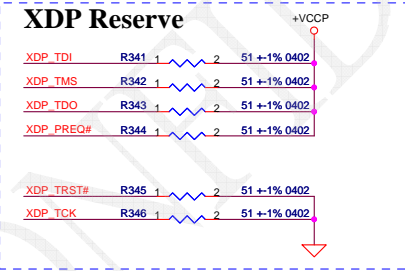
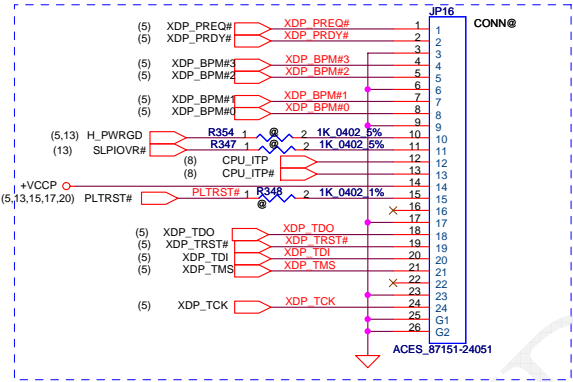
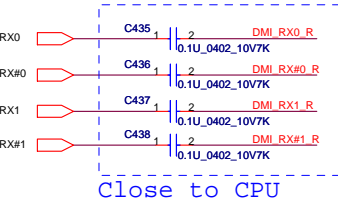
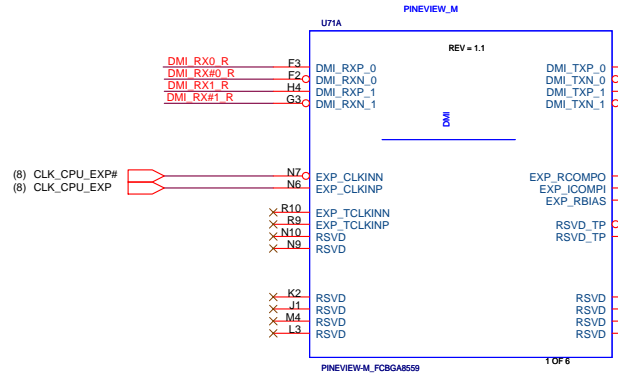
HeadPhone &
MIC Jack

SD/MMC/MS
CONN

I/O Board



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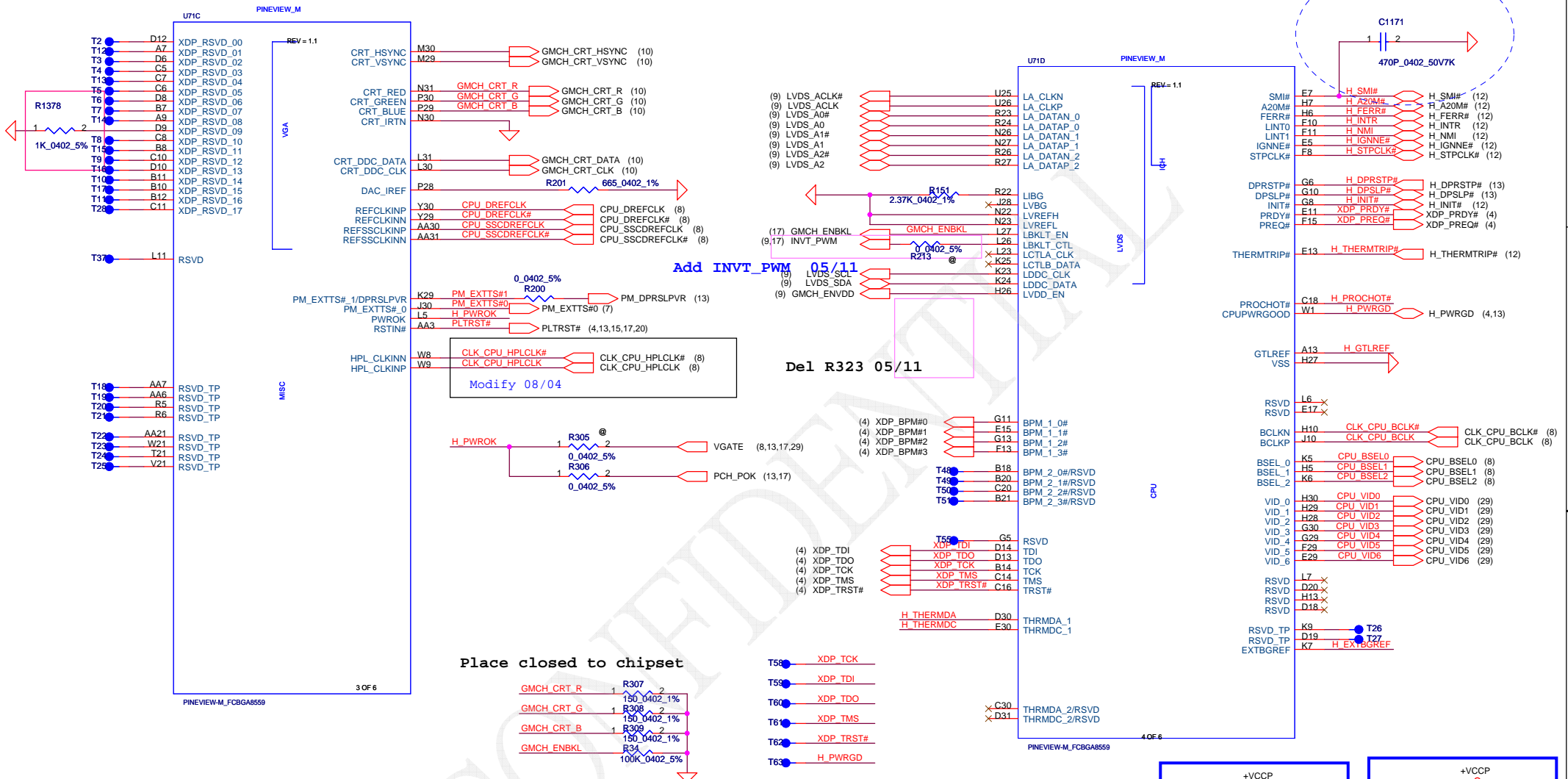


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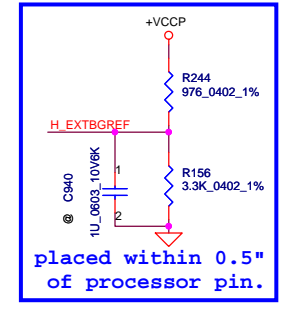
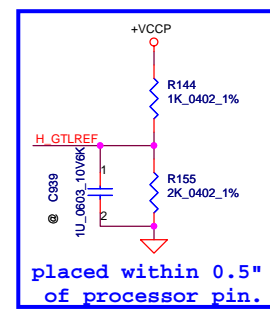
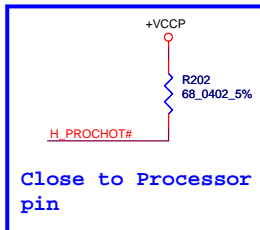
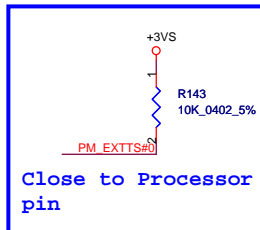
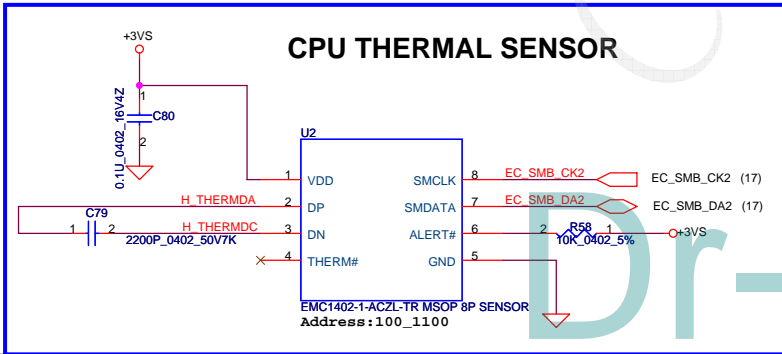
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Add 470PF on H_SMI# for known issue 07/08



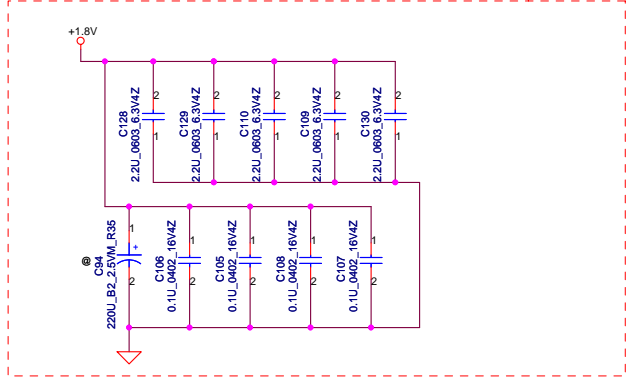
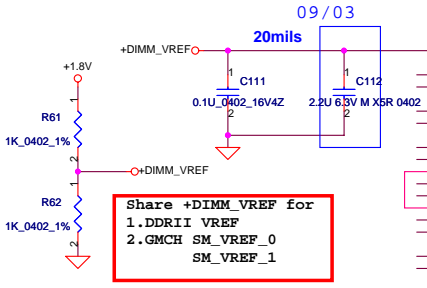
H_THERMDA, H_THERMDC routing together.
Trace width / Spacing = 10 / 10 mil



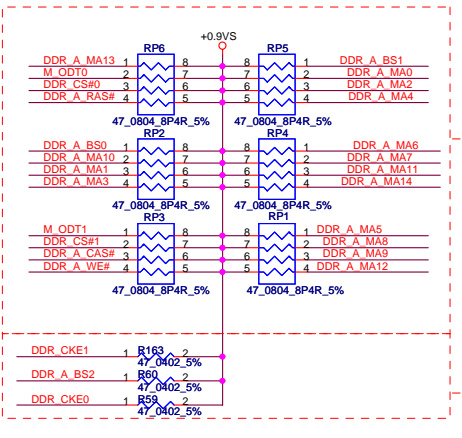
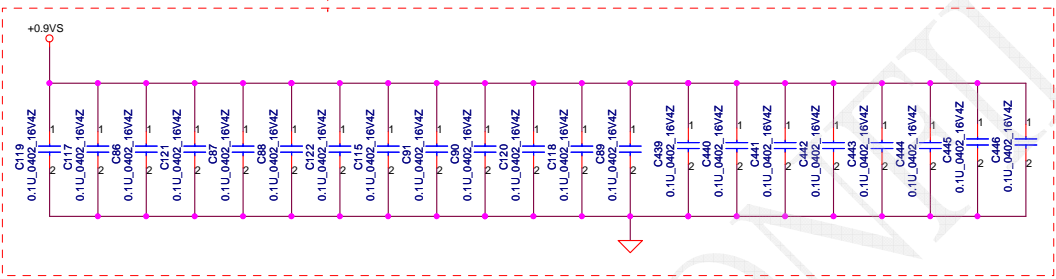
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- (4) DDR_A_DQS#[0..7]
- (4) DDR_A_D[0..63]
- (4) DDR_A_DM[0..7]
- (4) DDR_A_DQS#[0..7]
- (4) DDR_A_MA[0..14]

Layout Note:
Place near JDIM1

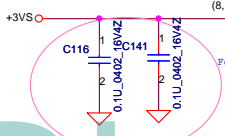


Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS

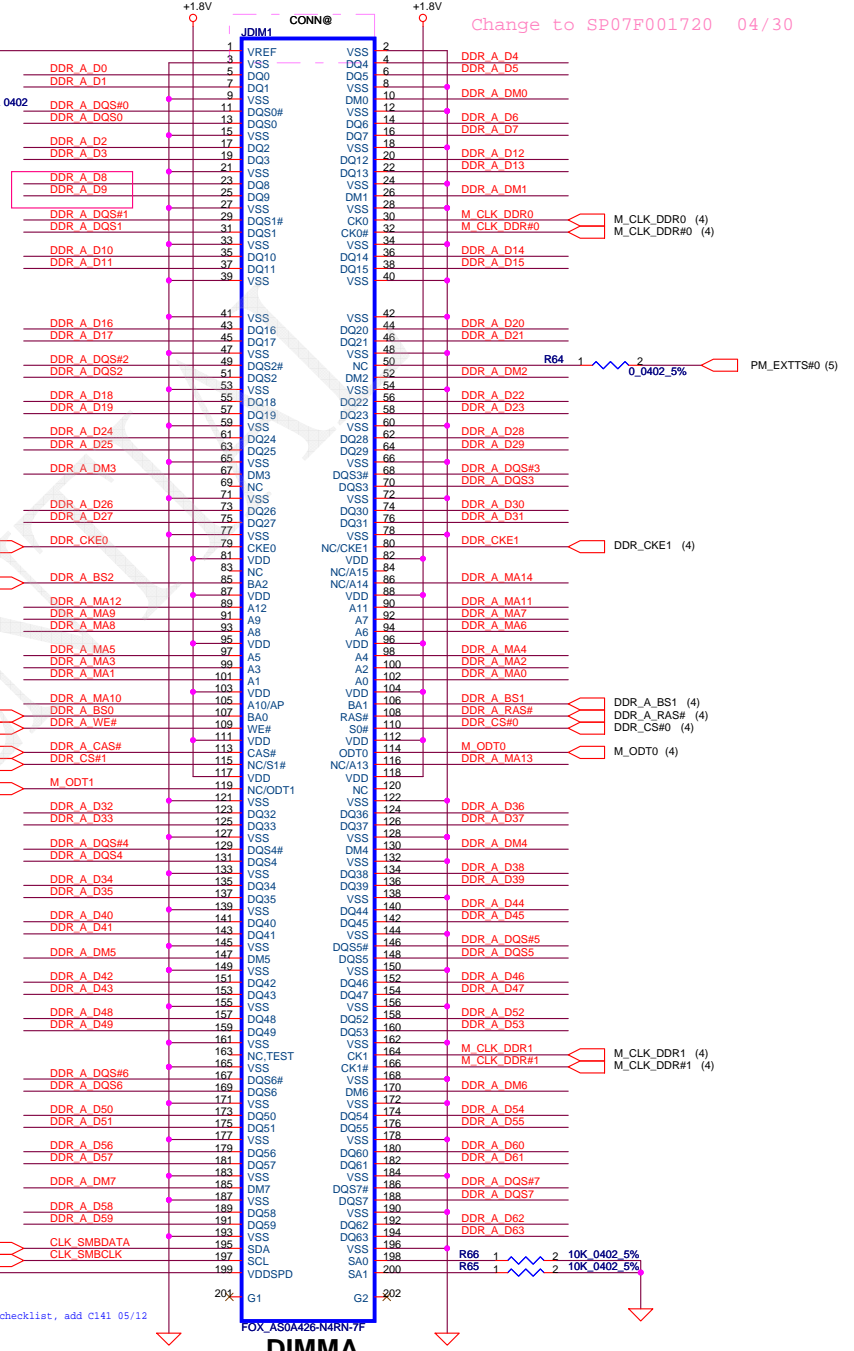


Layout Note:
Place these resistor closely DIMMA, all trace length < 750 mil

Layout Note:
Place these resistor closely DIMMA, all trace length Max=1.3"



Follow Intel Layout checklist, add C141 05/12

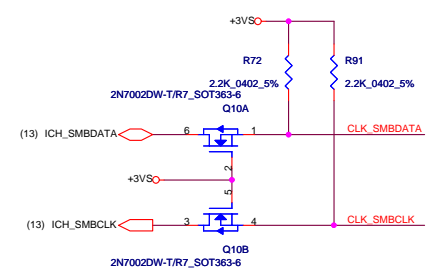
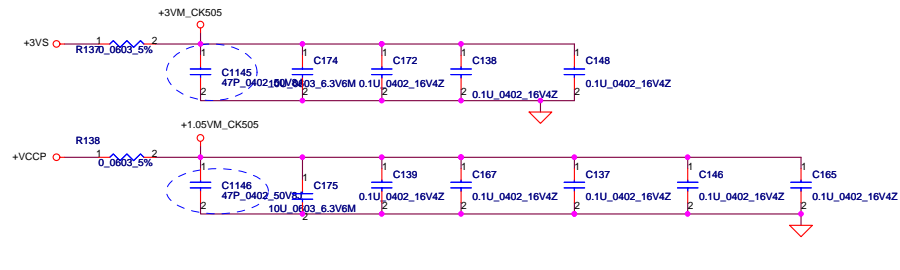


Change to SP07P001720 04/30

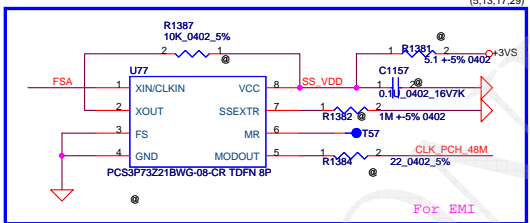
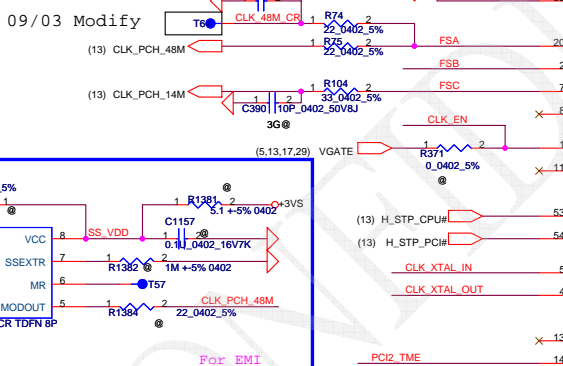
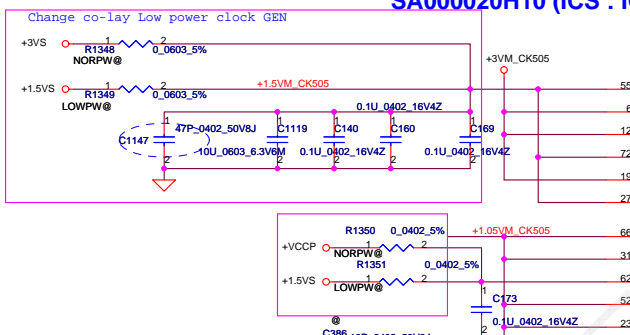
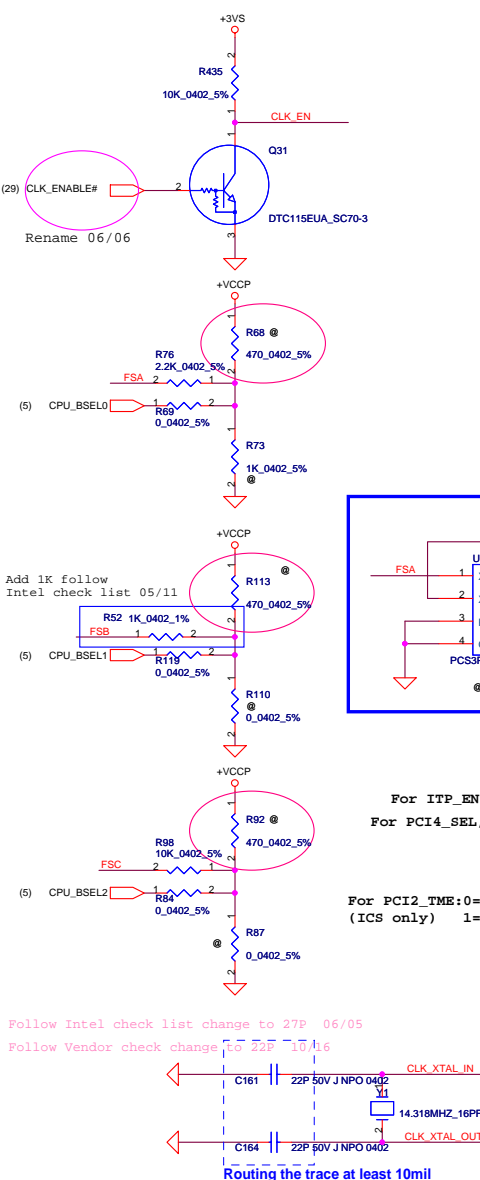
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FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1						
Reserved								

Change C174 C175 to 10U_0603 05/14

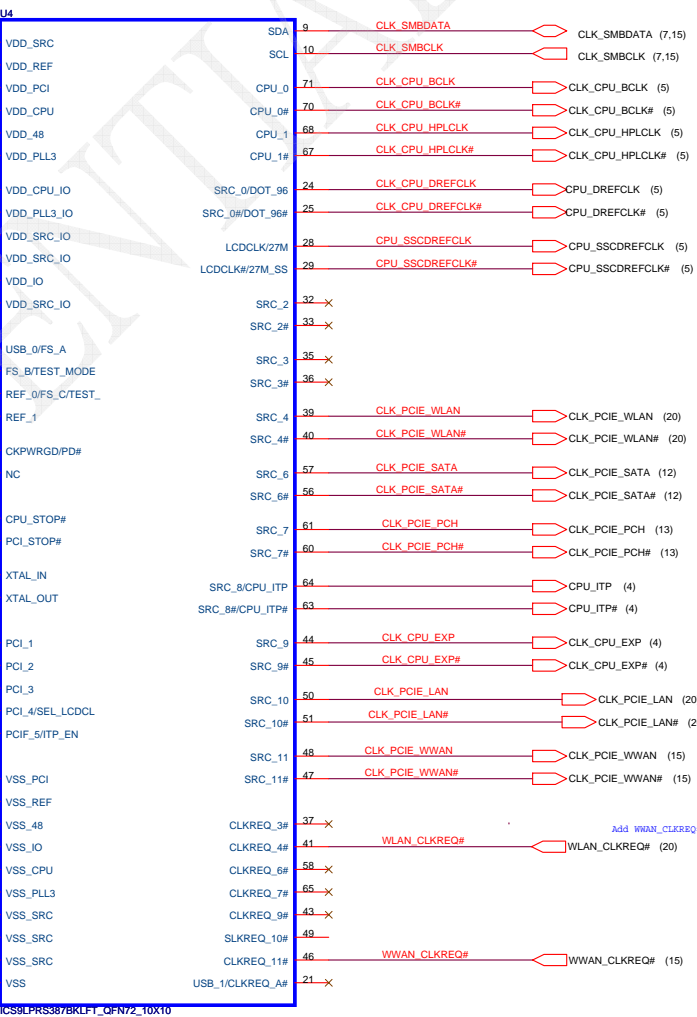
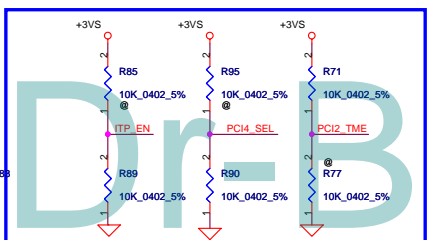


SA000020N00 (Realtek : RTM875N-397-GRT)
SA000020H10 (ICS : ICS9LPRS387BKLF)



For ITP_EN, 0 = SRC8/SRC8#; 1 = ITP/ITP#
 For PCI4_SEL, 0 = Pin24/25 : DOT96 / DOT96#
 Pin28/29 : LCDCLK / LCDCLK#
 1 = Pin24/25 : SRC_0 / SRC_0#
 Pin28/29 : 27M/27M_SS

For PCI2_TME:0=Overclocking of CPU and SRC allowed (ICS only) 1=Overclocking of CPU and SRC NOT allowed



SRC PORT LIST

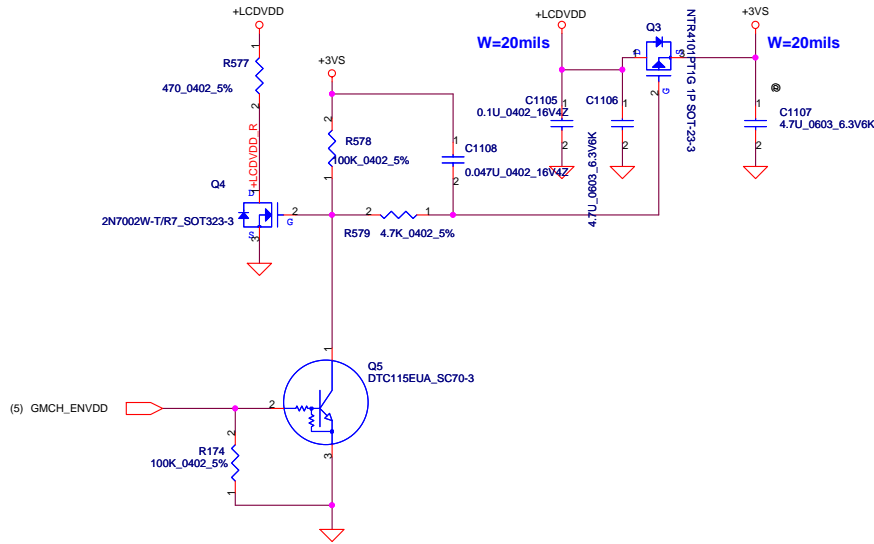
PORT	DEVICE
SRC1	CPU_SSCDREFCLK
SRC2	
SRC3	
SRC4	PCIE_WLAN
SRC6	PCIE_SATA
SRC7	PCIE_PCH
SRC8	CPU_ITP
SRC9	CLK_CPU_EXP
SRC10	PCIE_LAN
SRC11	PCIE_WWAN

REQ PORT LIST

PORT	DEVICE
REQ_3#	
REQ_4#	PCIE_WLAN
REQ_6#	
REQ_7#	
REQ_9#	
REQ_10#	
REQ_11#	PCIE_WWAN
REQ_A#	

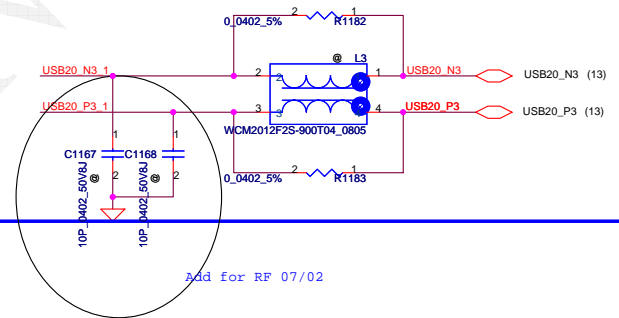
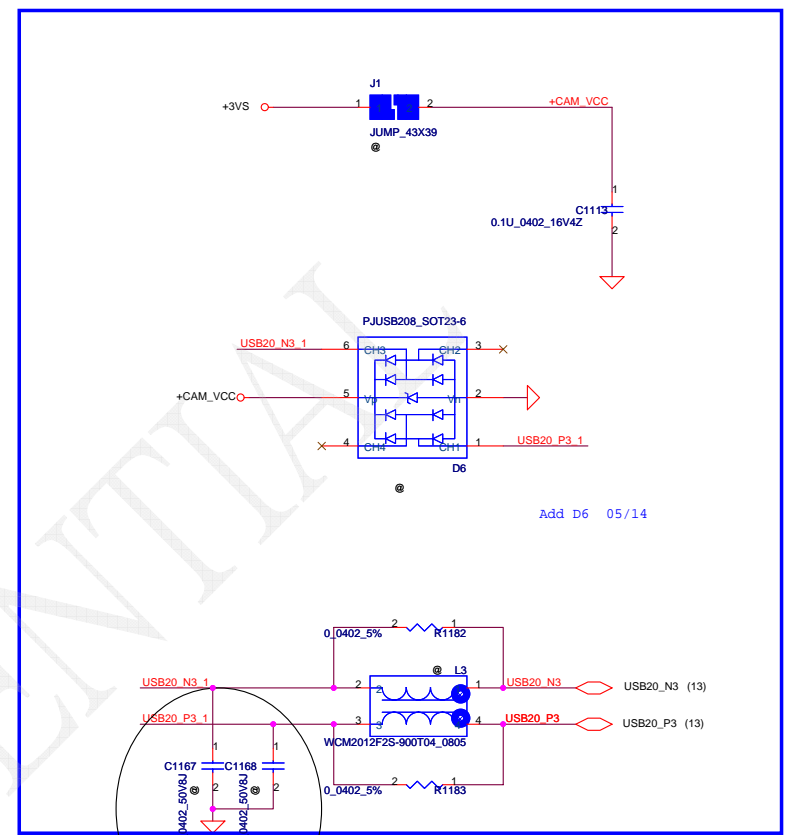
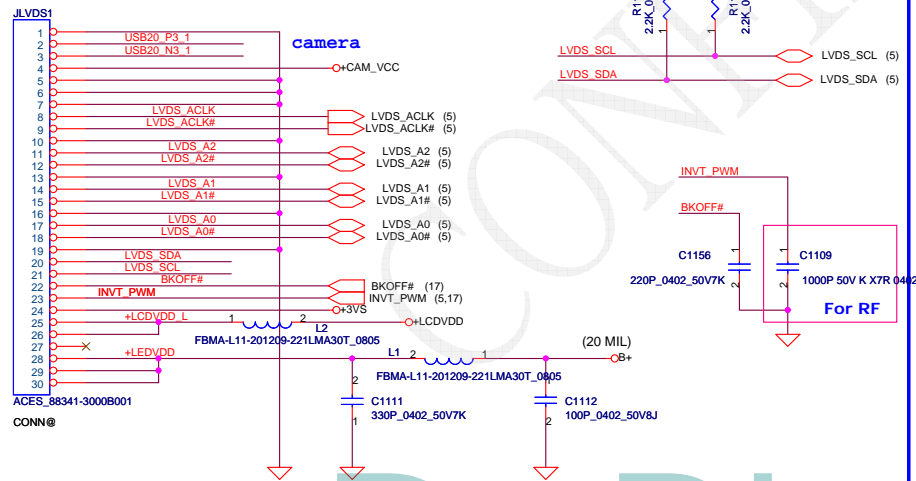
Follow Intel check list change to 27P 06/05
 Follow Vendor check change to 27P 10/16
 Routing the trace at least 10mil

LCD POWER CIRCUIT

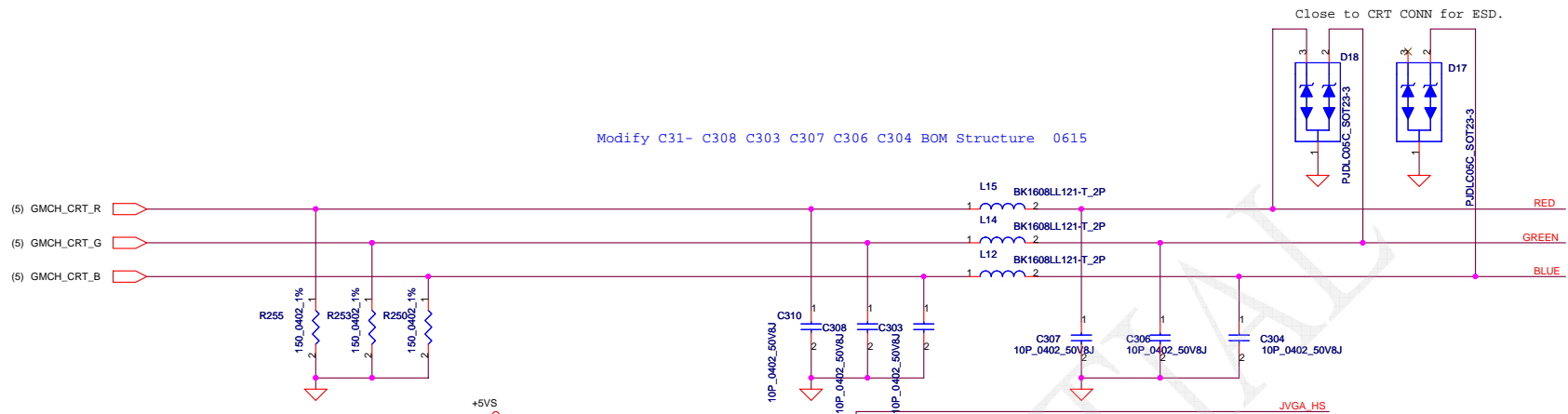


CMOS & LCD/PANEL BD. Conn.

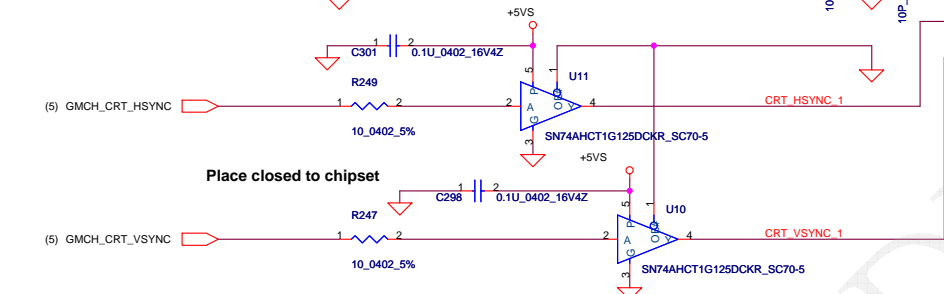
Modify JLVDS1 08/04



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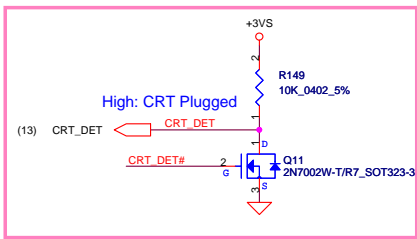


Modify C31- C308 C303 C307 C306 C304 BOM Structure 0615



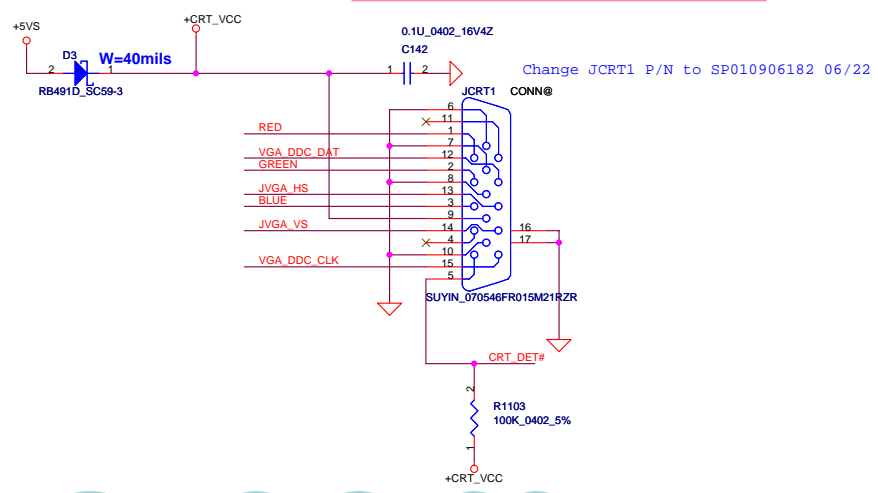
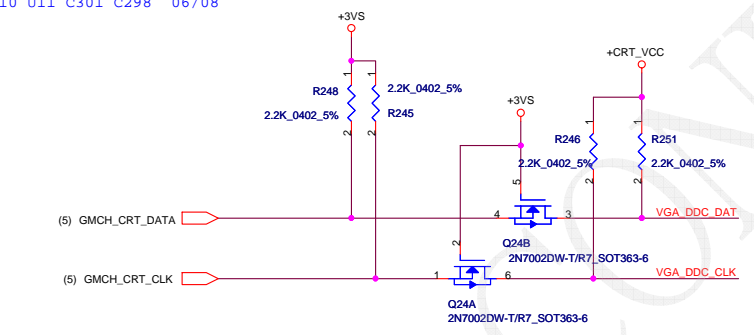
Place closed to chipset

Change CRT_DET# From Page 13 to Page 10 06/12

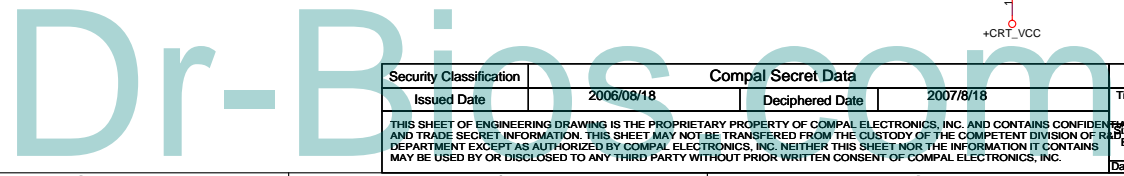


Add R1283 R1284
Change R247 R249 to 10 ohm
Add @ on U10 U11 C301 C298 06/08

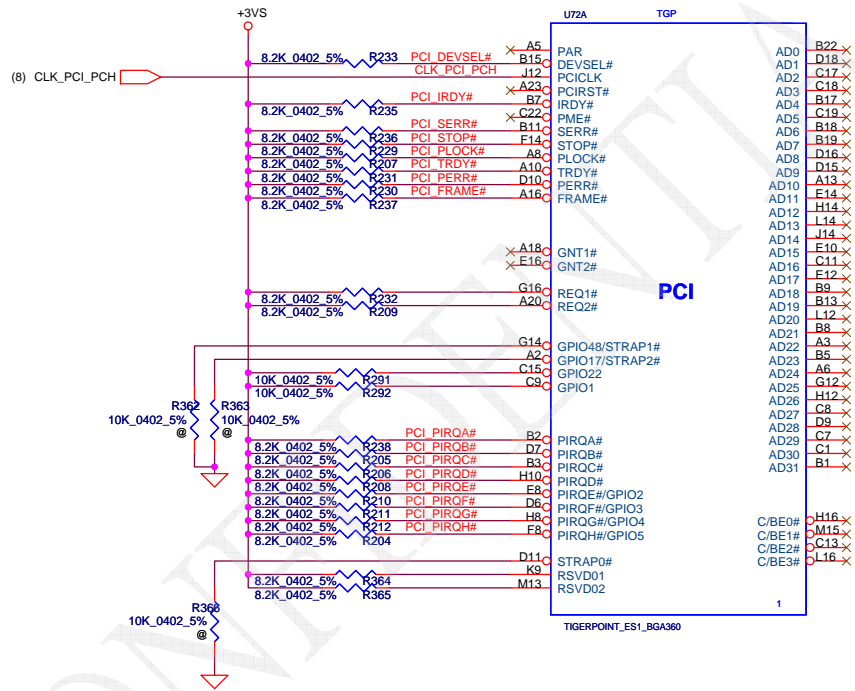
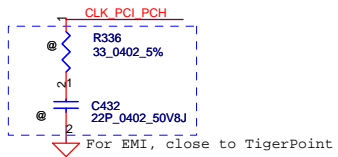
CRT PORT



Change JCRT1 P/N to SP010906182 06/22

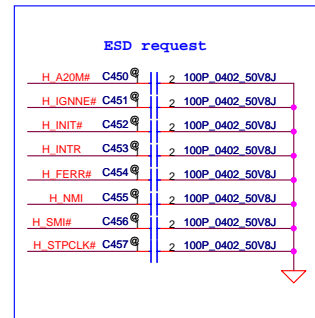
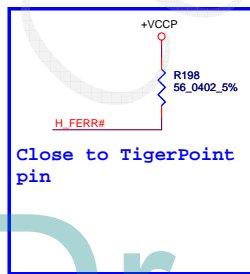
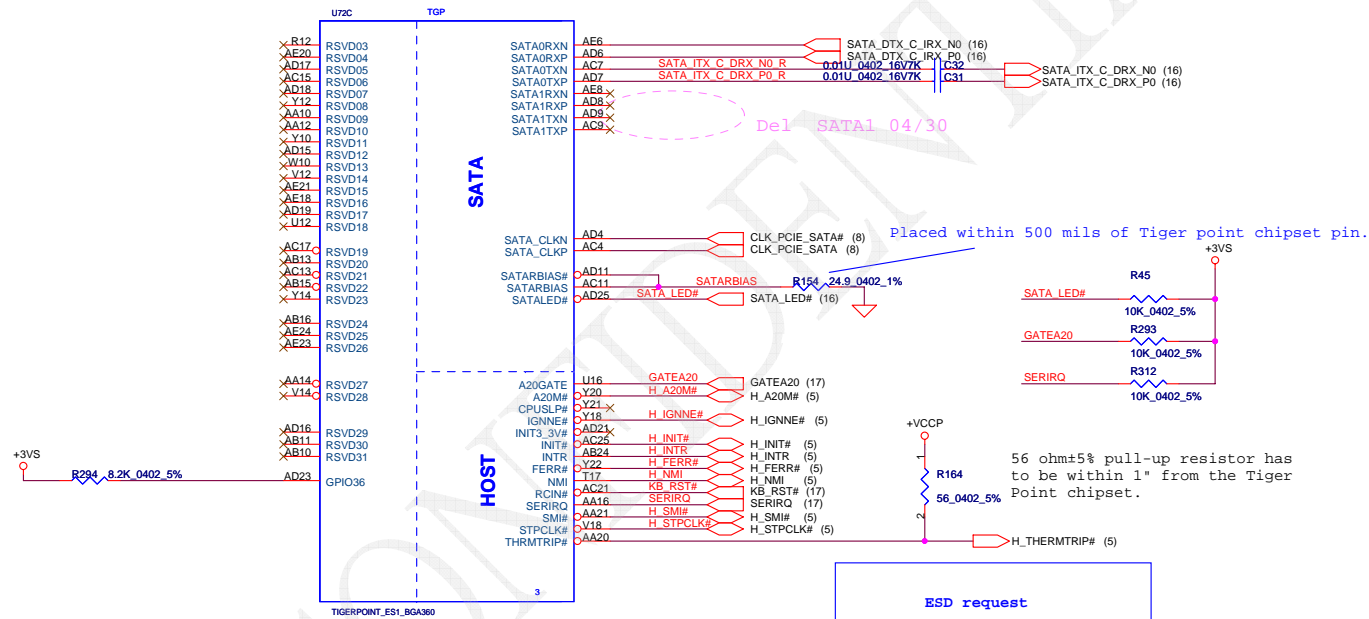


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STRAP2# GPIO17	STRAP1# GPIO48	Boot BIOS
0	1	SPI
1	0	PCI
1	1	LPC

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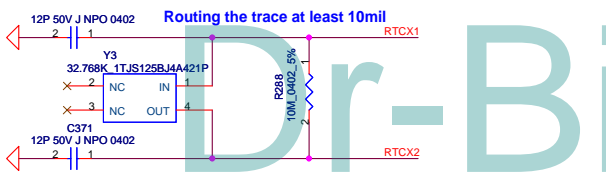
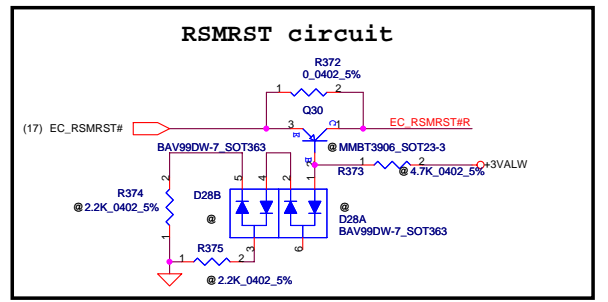
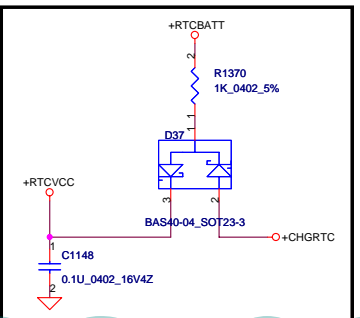
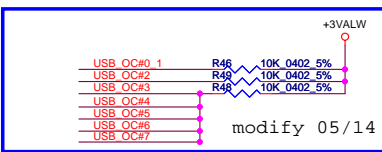
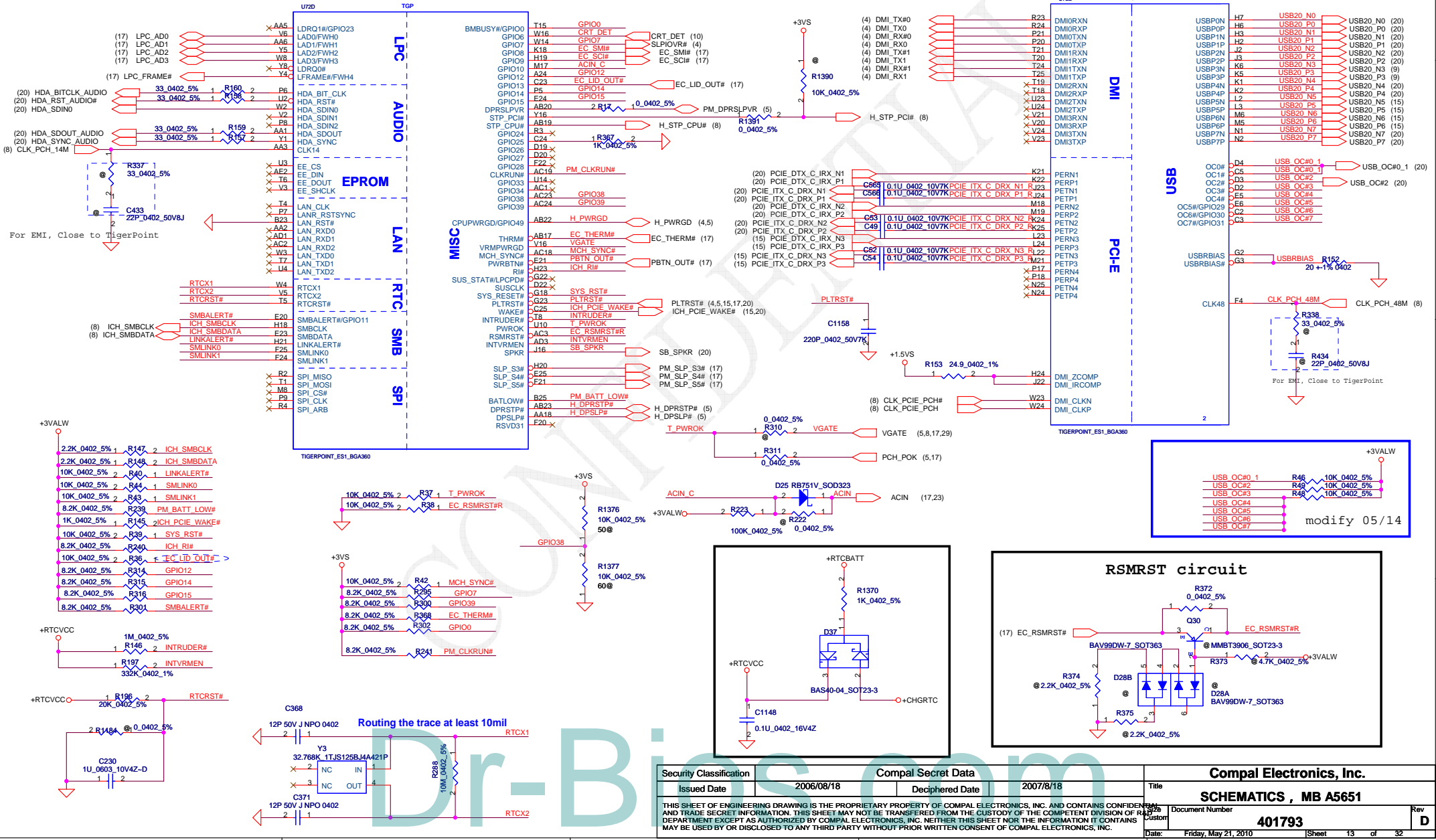


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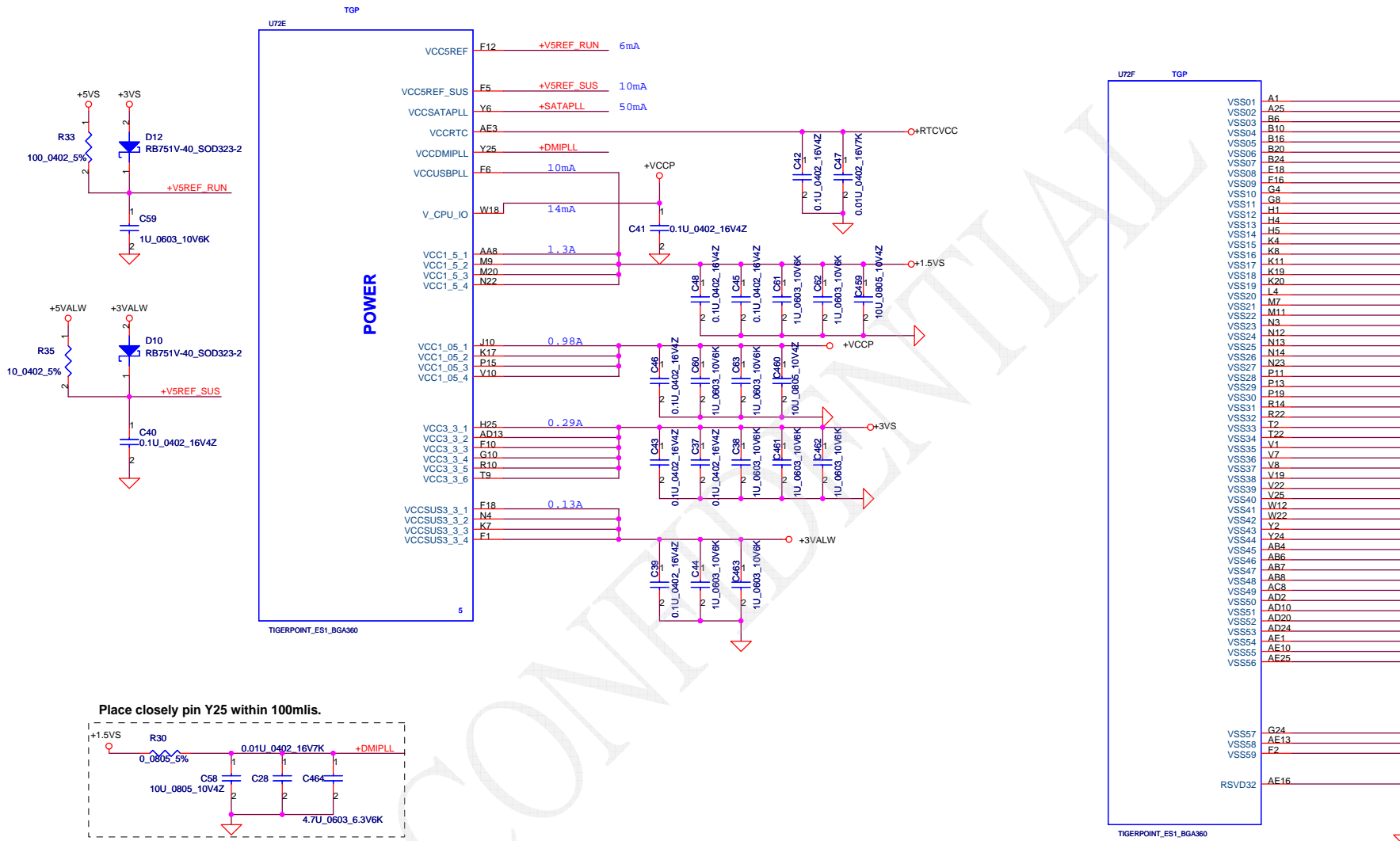
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PCIe Port List	
1	LAN
2	WLAN
3	WWAN
4	

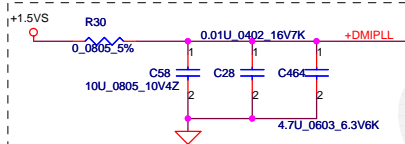
USB Port List	
0	USB Left1
1	USB Left2
2	USB Right2
3	CMOS
4	CardReader
5	WWAN
6	BT
7	WIMAX



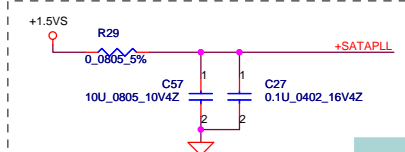
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Place closely pin Y25 within 100mils.

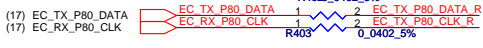


Place closely pin Y6 within 100mils.



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Mini-Express Card for WWAN



Change JMINI1 to FOX_AS0B246-S50U-7F_52P-T 06/29

(13,20) ICH_PCIE_WAKE# ↔ ICH_PCIE_WAKE#

(8) WWAN_CLKREQ# ↔ WWAN_CLKREQ#

(8) CLK_PCIE_WWAN# ↔ CLK_PCIE_WWAN#

(8) CLK_PCIE_WWAN ↔ CLK_PCIE_WWAN

(13) PCIE_DTX_C_IRX_N3 ↔ PCIE_DTX_C_IRX_N3

(13) PCIE_DTX_C_IRX_P3 ↔ PCIE_DTX_C_IRX_P3

Change to PCIE_P3 05/13

(13) PCIE_ITX_C_DRX_N3 ↔ PCIE_ITX_C_DRX_N3

(13) PCIE_ITX_C_DRX_P3 ↔ PCIE_ITX_C_DRX_P3

+3VS_WWAN ↔ +3VS_WWAN

UIM_VPP ↔ UIM_VPP

UIM_DATA ↔ UIM_DATA

EC_TX_P80_DATA ↔ EC TX_P80_DATA

EC_RX_P80_CLK ↔ EC RX_P80_CLK

UIM_VPP ↔ UIM_VPP

UIM_RST ↔ UIM_RST

UIM_VPP ↔ UIM_VPP

UIM_RST ↔ UIM_RST

UIM_DATA ↔ UIM_DATA

UIM_VPP ↔ UIM_VPP

UIM_RST ↔ UIM_RST

UIM_DATA ↔ UIM_DATA

UIM_VPP ↔ UIM_VPP

UIM_RST ↔ UIM_RST

UIM_DATA ↔ UIM_DATA

UIM_VPP ↔ UIM_VPP

UIM_RST ↔ UIM_RST

UIM_DATA ↔ UIM_DATA

UIM_VPP ↔ UIM_VPP

UIM_RST ↔ UIM_RST

UIM_DATA ↔ UIM_DATA

UIM_VPP ↔ UIM_VPP

UIM_RST ↔ UIM_RST

UIM_DATA ↔ UIM_DATA

UIM_VPP ↔ UIM_VPP

UIM_RST ↔ UIM_RST

UIM_DATA ↔ UIM_DATA

UIM_VPP ↔ UIM_VPP

UIM_RST ↔ UIM_RST

UIM_DATA ↔ UIM_DATA

UIM_VPP ↔ UIM_VPP

UIM_RST ↔ UIM_RST

UIM_DATA ↔ UIM_DATA

UIM_VPP ↔ UIM_VPP

UIM_RST ↔ UIM_RST

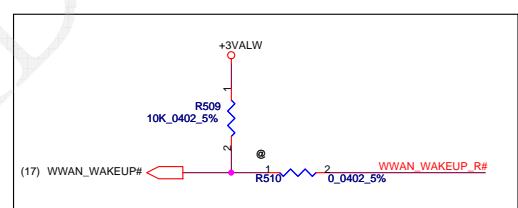
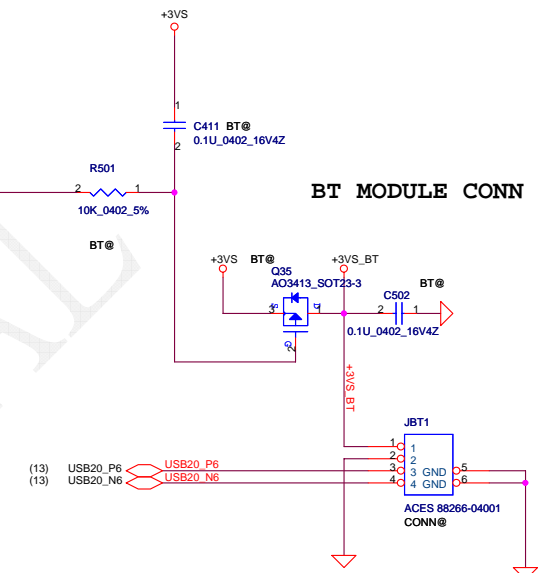
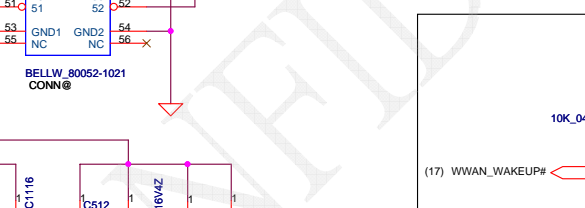
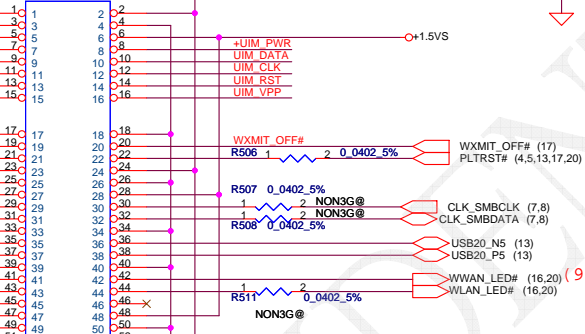
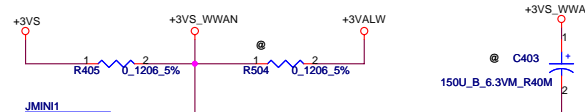
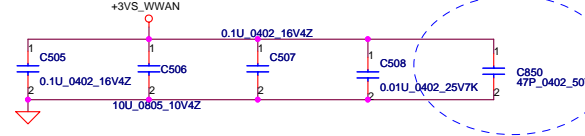
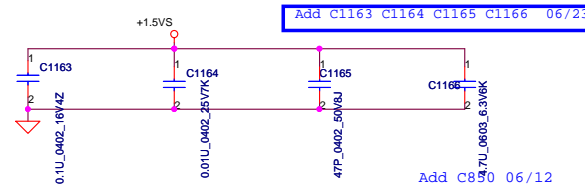
UIM_DATA ↔ UIM_DATA

UIM_VPP ↔ UIM_VPP

UIM_RST ↔ UIM_RST

UIM_DATA ↔ UIM_DATA

Reserve for SIM card does not meet rise time and pull-up is needed.

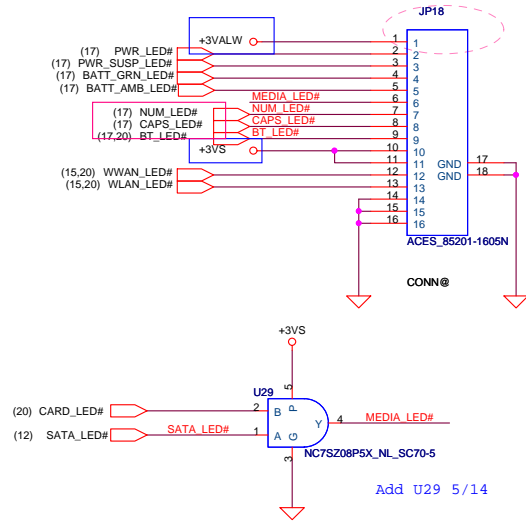


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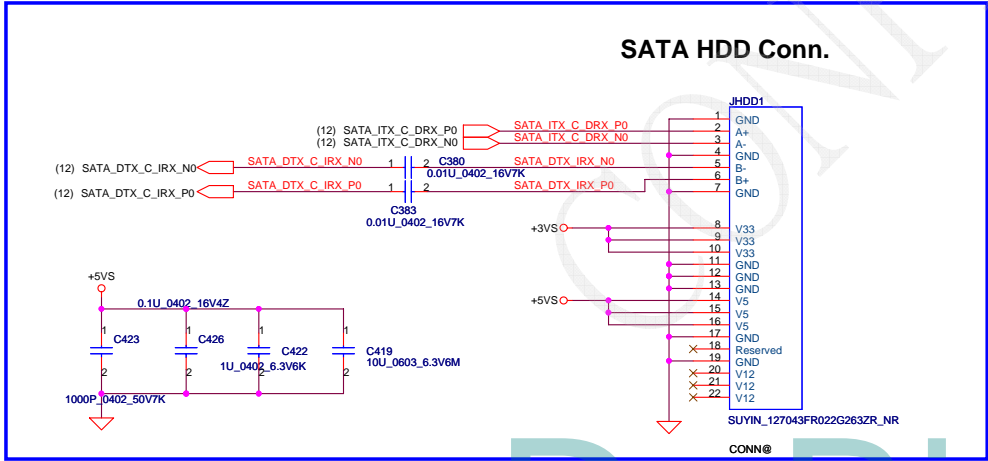
ADD LED PCB CONN 06/12

Change JP18 to NEW P/N 06/23
09/03 Change +5VALW , +5VS to +3VALW +3VS

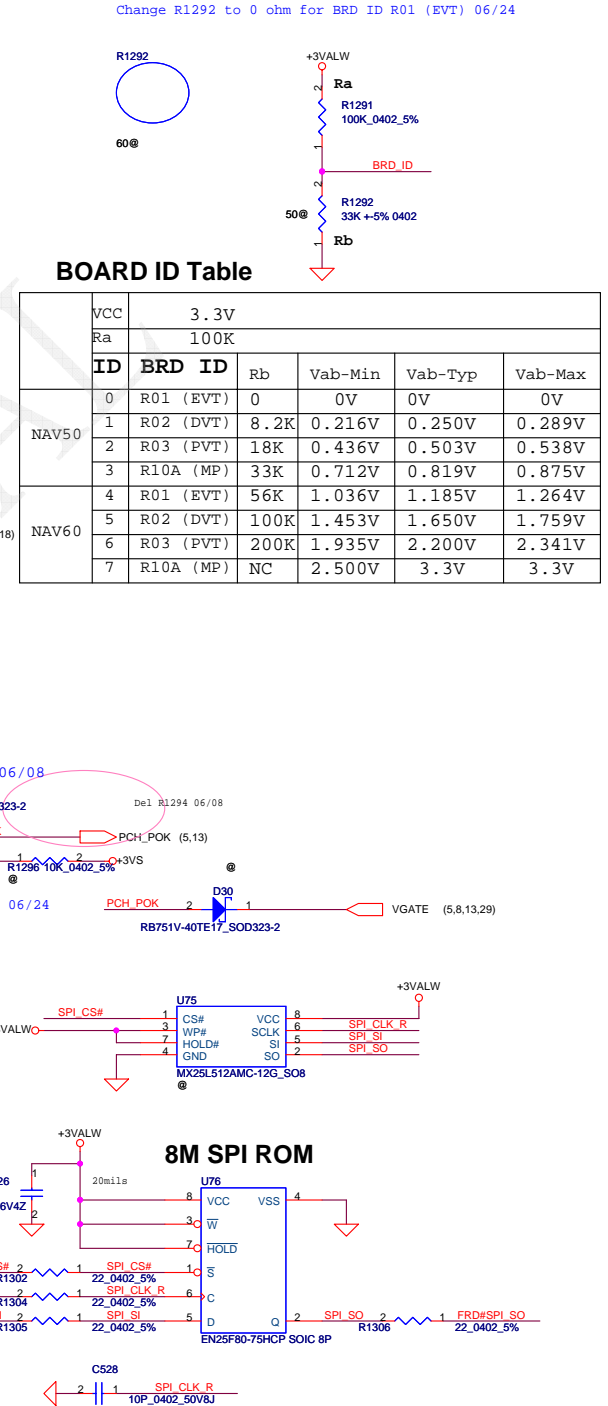
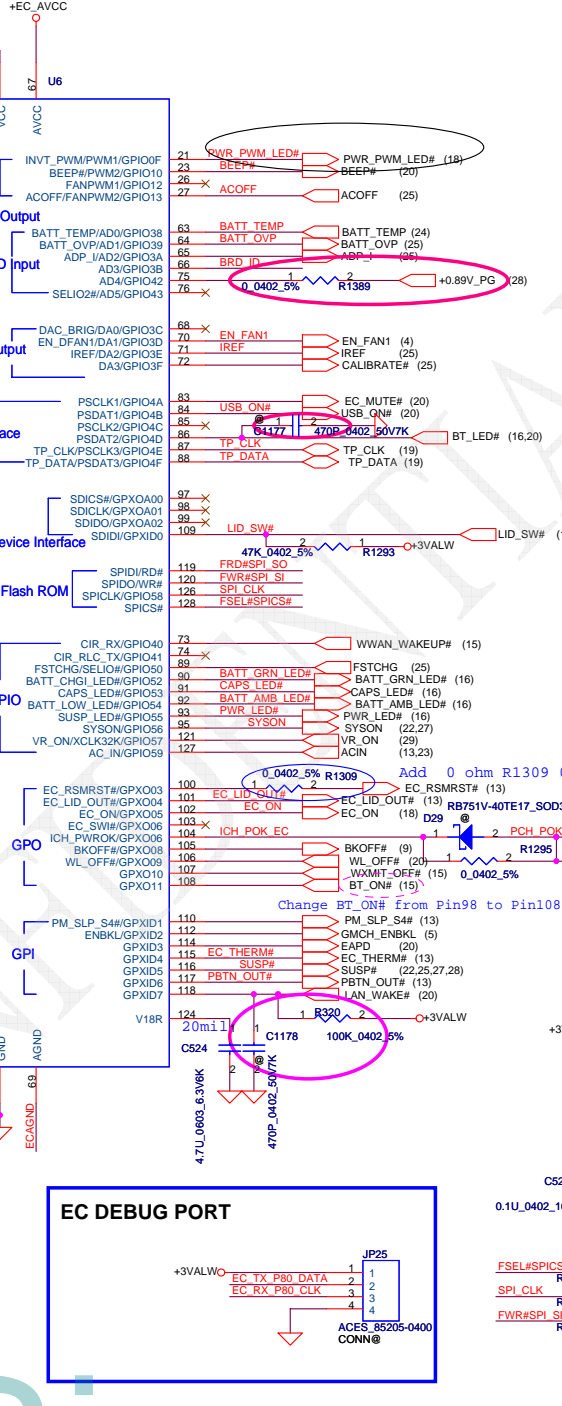
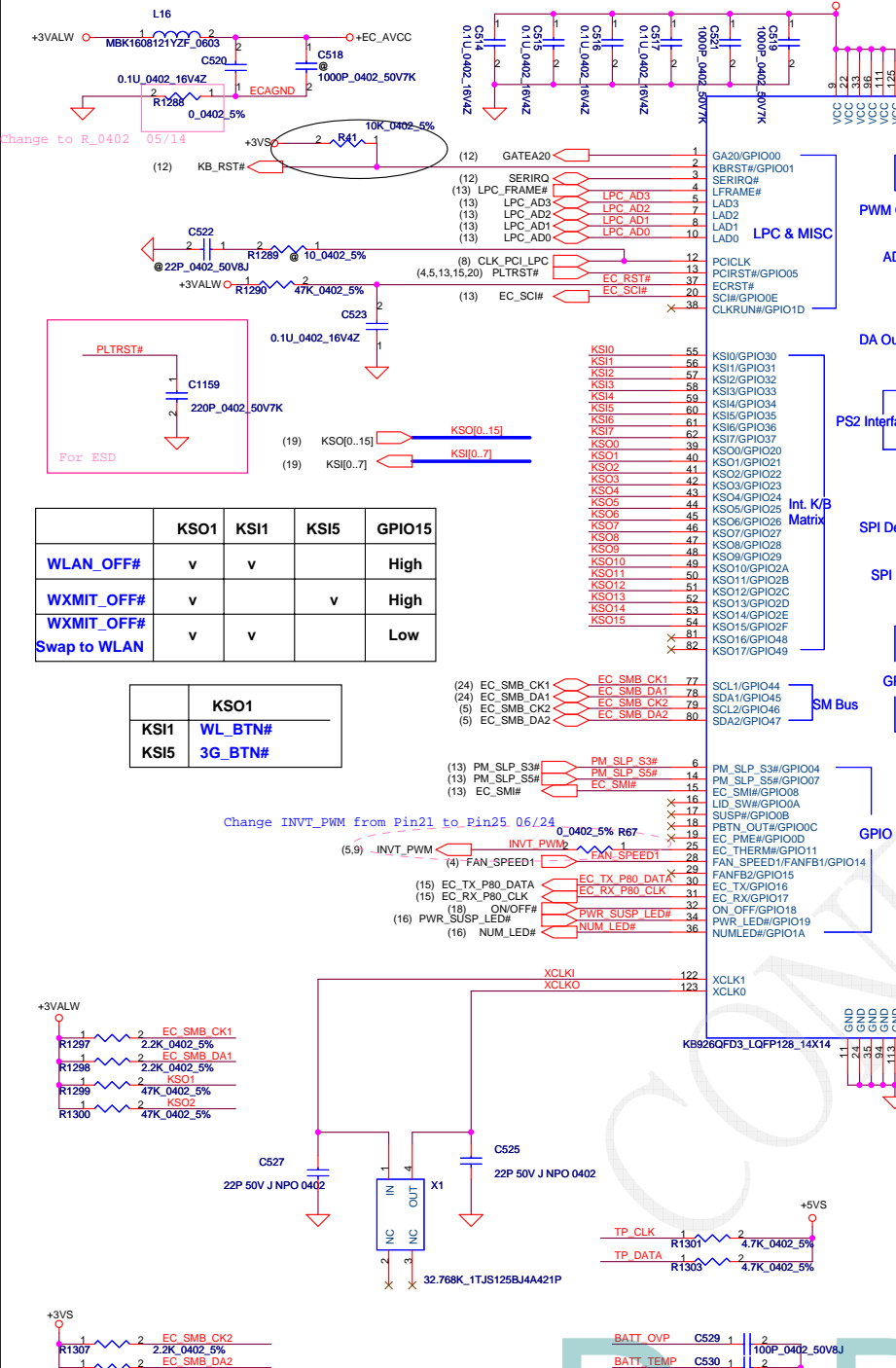
LED PCB CONN



SATA HDD Conn.



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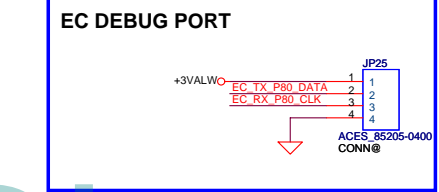


BOARD ID Table

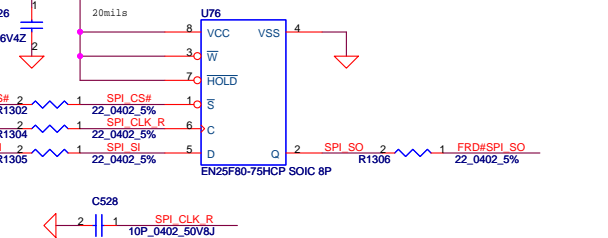
ID	BRD ID	VCC = 3.3V				
		Ra	Rb	Vab-Min	Vab-Typ	Vab-Max
NAV50	0	R01 (EVT)	0	0V	0V	0V
	1	R02 (DVT)	8.2K	0.216V	0.250V	0.289V
	2	R03 (PVT)	1.8K	0.436V	0.503V	0.538V
	3	R10A (MP)	33K	0.712V	0.819V	0.875V
NAV60	4	R01 (EVT)	56K	1.036V	1.185V	1.264V
	5	R02 (DVT)	100K	1.453V	1.650V	1.759V
	6	R03 (PVT)	200K	1.935V	2.200V	2.341V
	7	R10A (MP)	NC	2.500V	3.3V	3.3V

	KSO1	KSI1	KSI5	GPIO15
WLAN_OFF#	v	v		High
WXMIT_OFF#	v		v	High
WXMIT_TO WLAN	v	v		Low

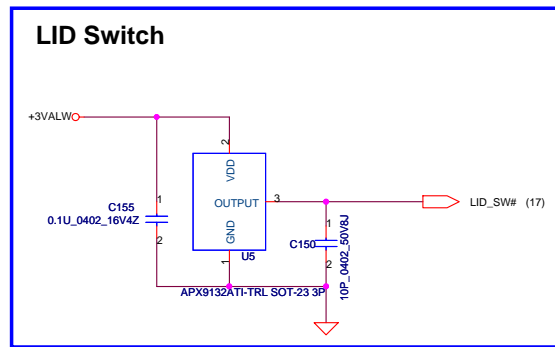
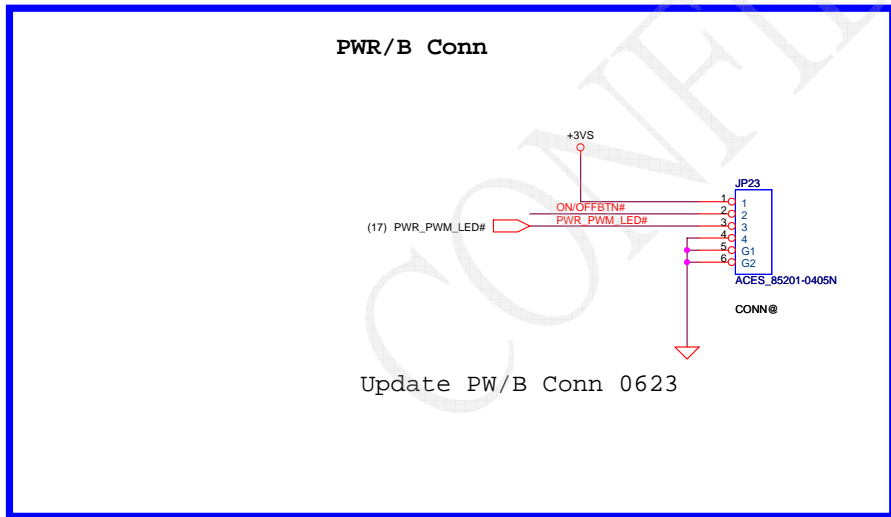
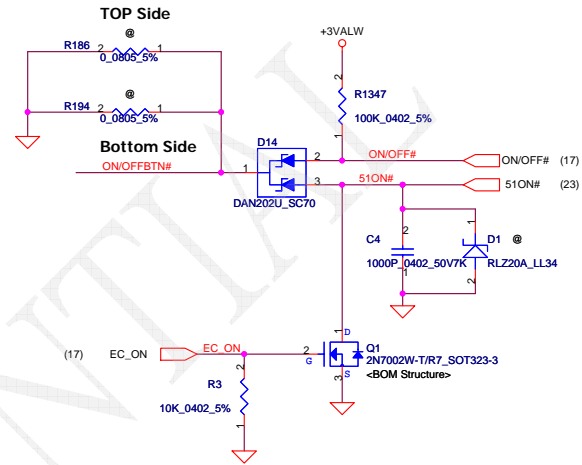
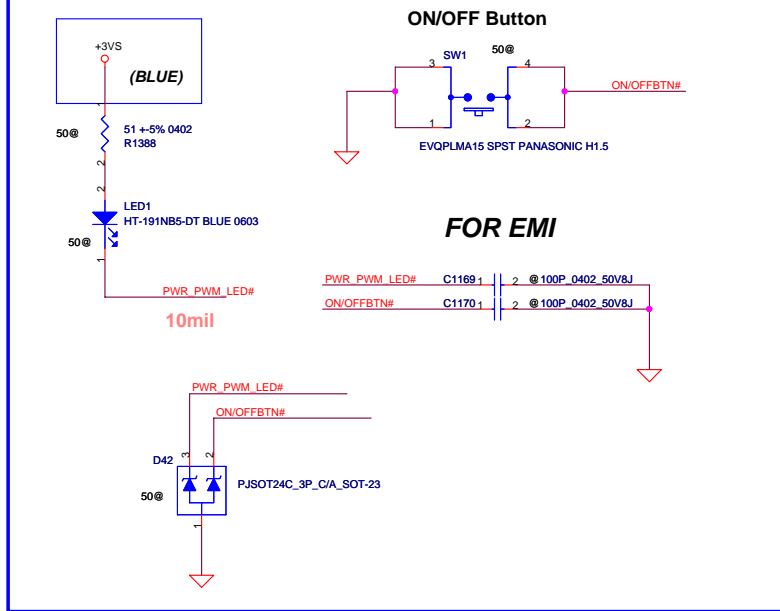
	KSO1
KSI1	WL_BTN#
KSI5	3G_BTN#



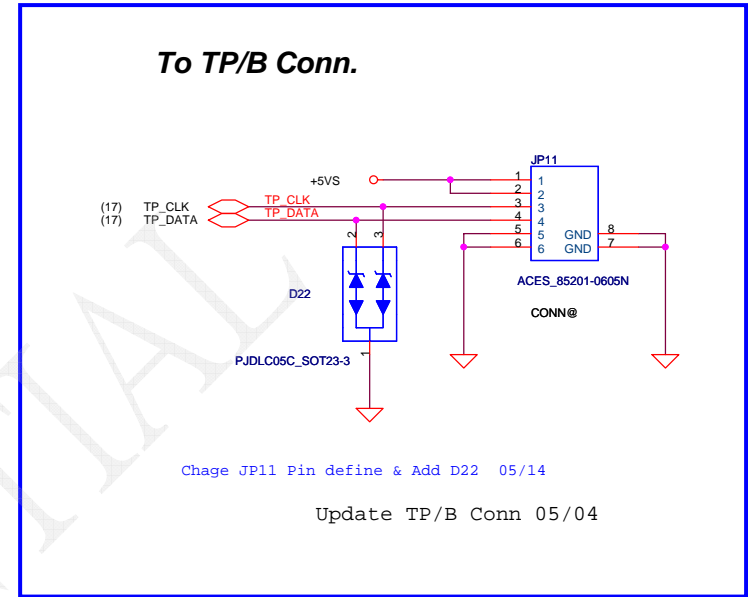
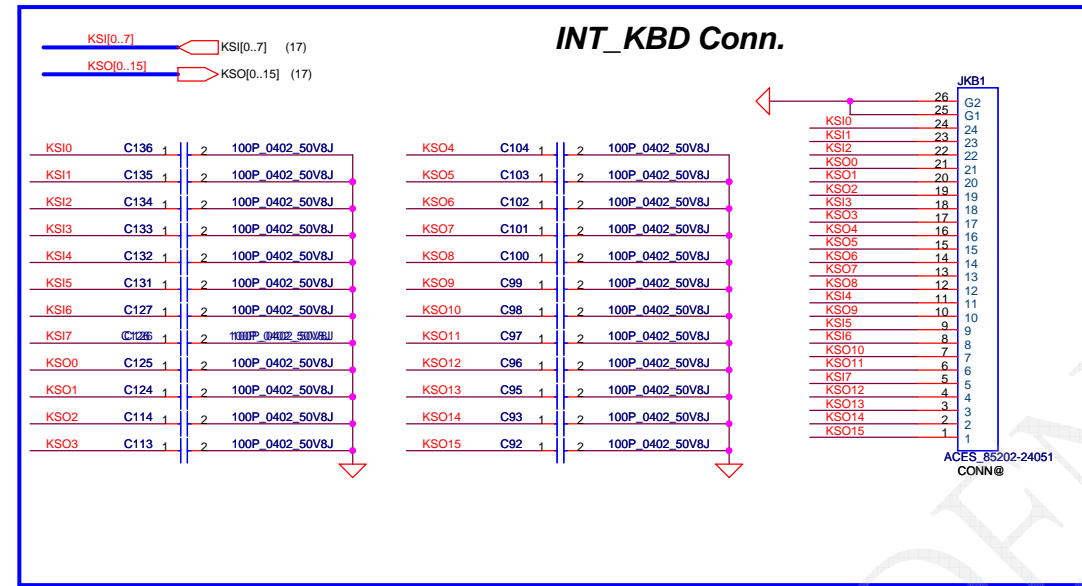
8M SPI ROM



Add For NAV50 07/06
09/03 Change +5VS to +3VS



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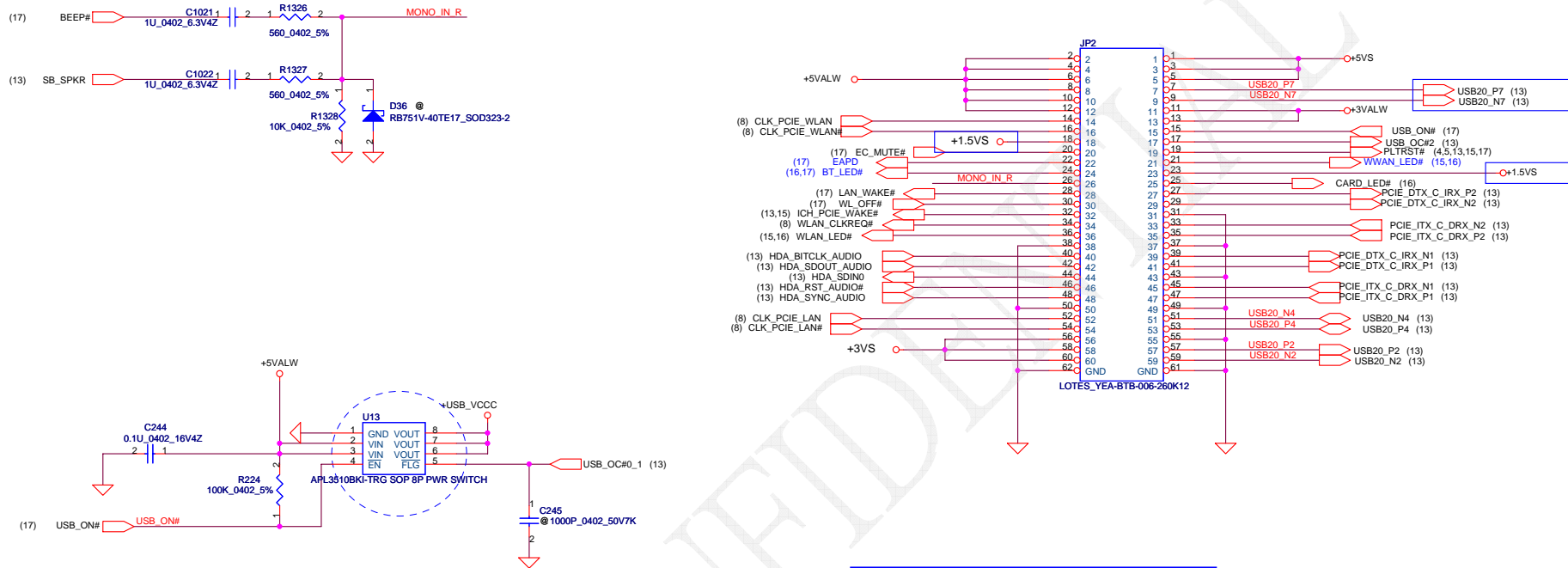
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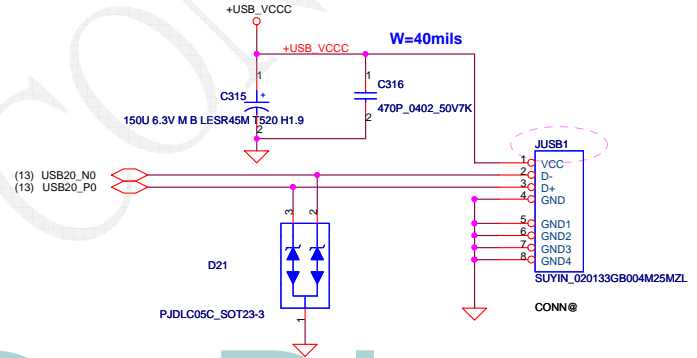
09/03 Change Pin 18, 23 to +1.5VS change Pin7 , 9 to USB20_P7 N7

I/O Board Conn.

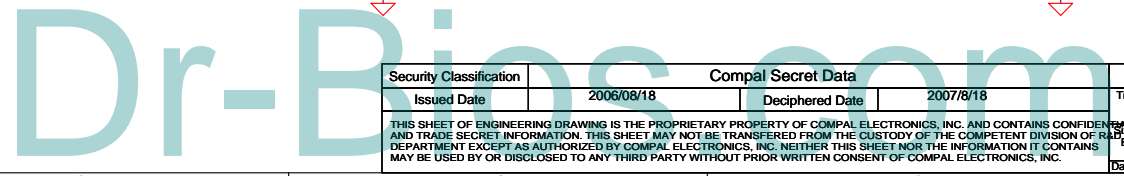
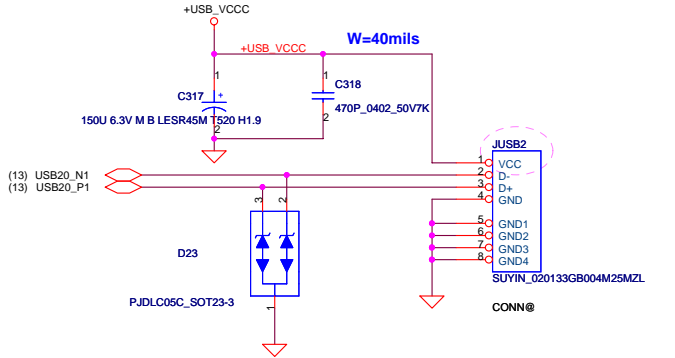


Change JUSB1 JUSB2 to NEW P/N SP010906181 06/21

USB CONN.1

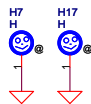
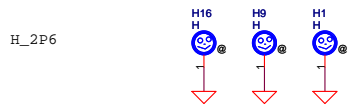


USB CONN.2

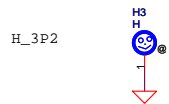
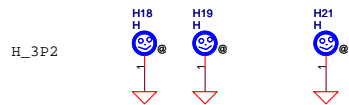


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Modify Hole location by (ME Drawing 06/12) 0615



09/03 Del H12



FIDUCIAL_C40M80

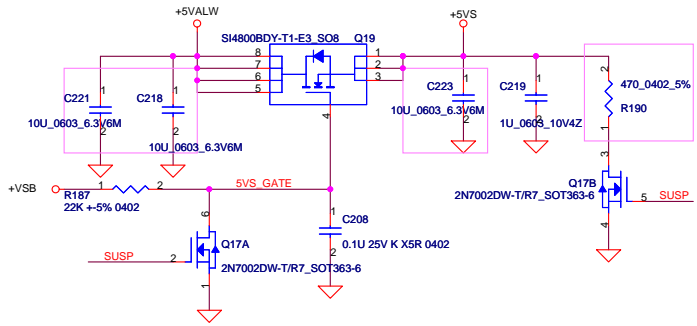
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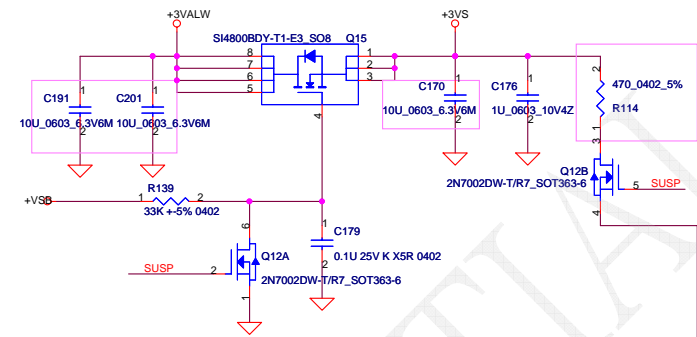
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Change R51 R57 R70 R63 R317 R114 R190 to 0402 SIZE 04/30
 Change C221 C218 C223 C 191 C201 C170 C392 C393 C394 to 0603 SIZE 04/30

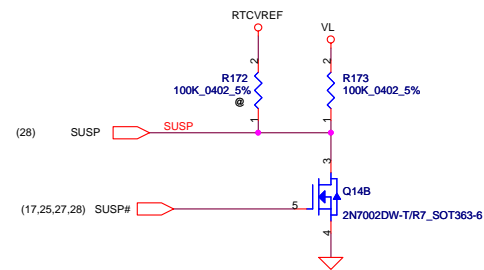
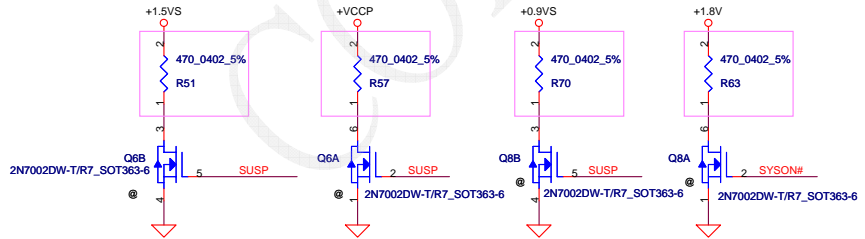
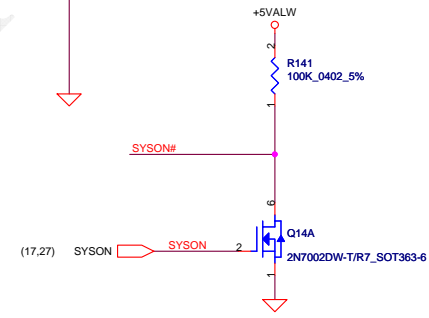
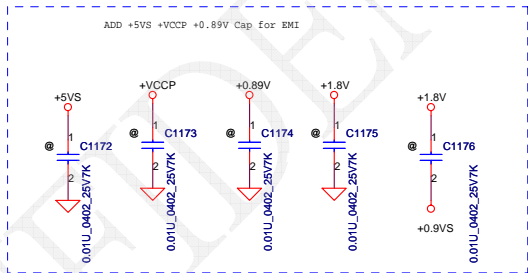
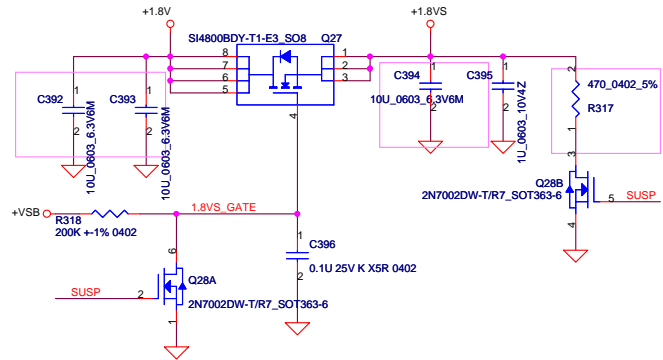
+5VALW TO +5VS



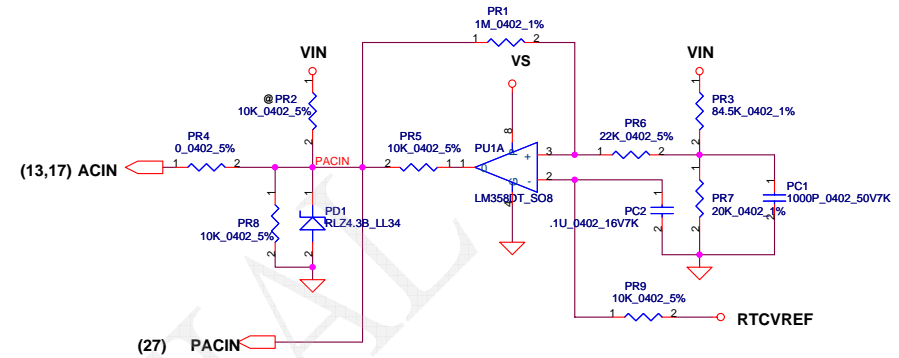
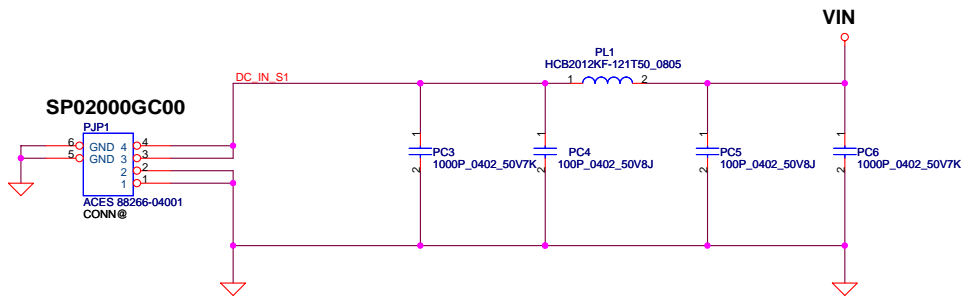
+3VALW TO +3VS



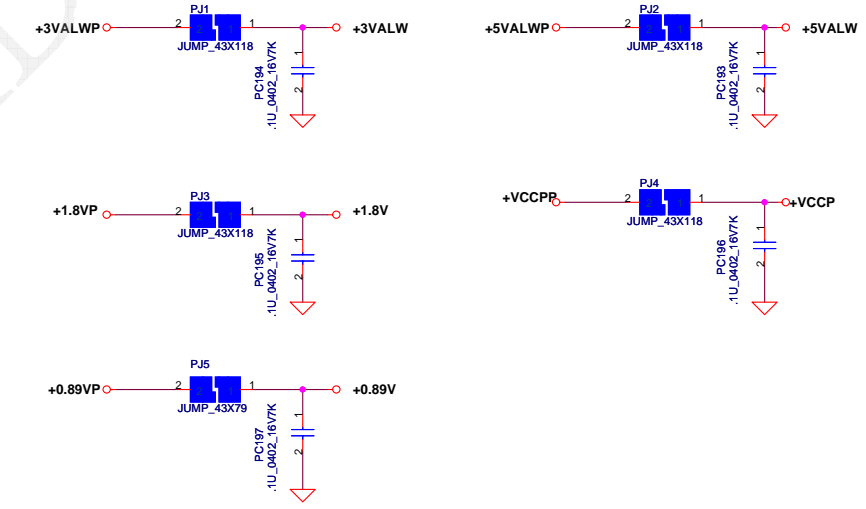
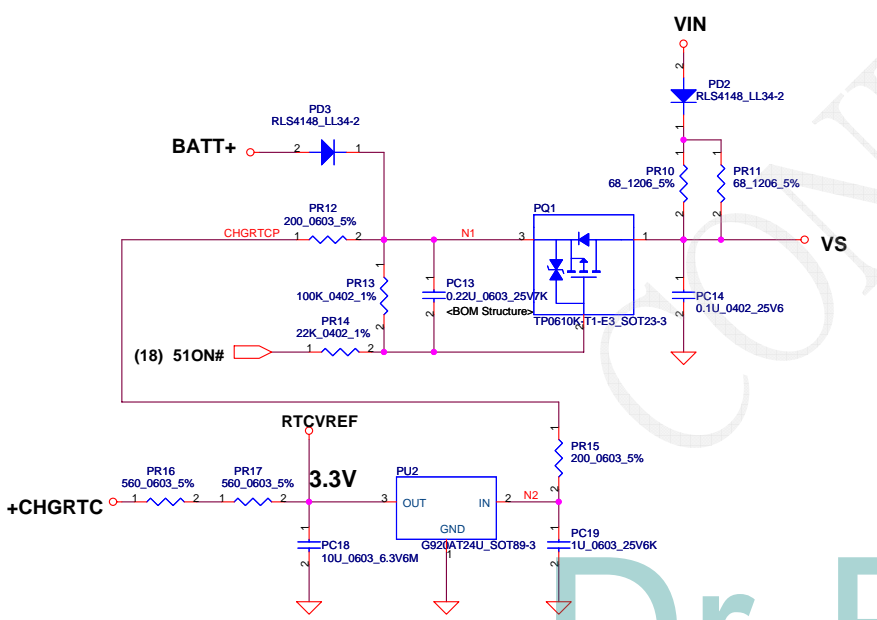
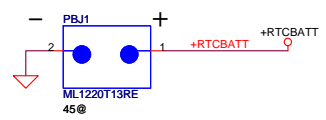
+1.8V to +1.8VS



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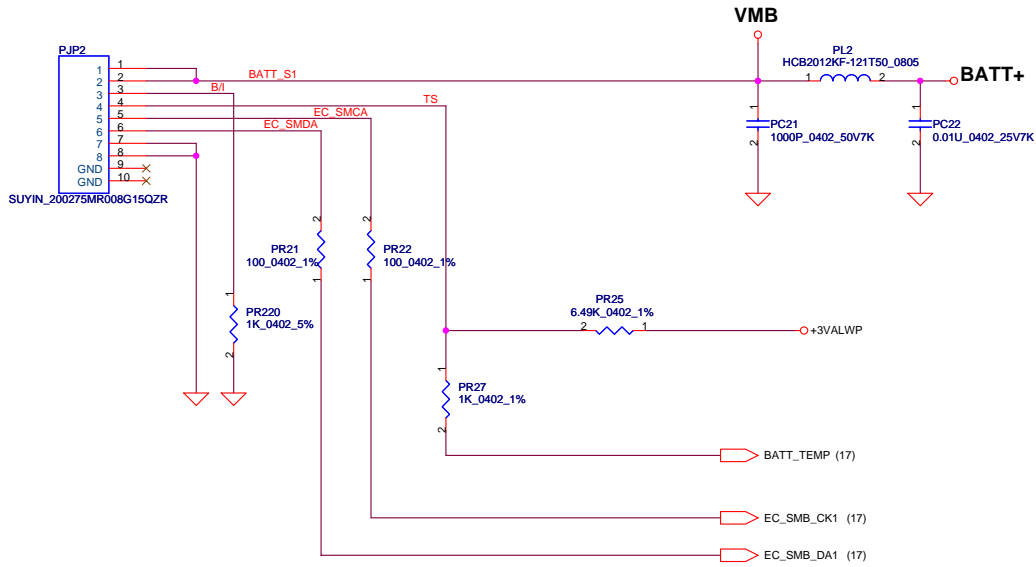


Vin Dectector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V

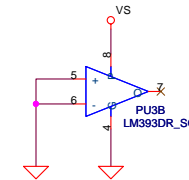
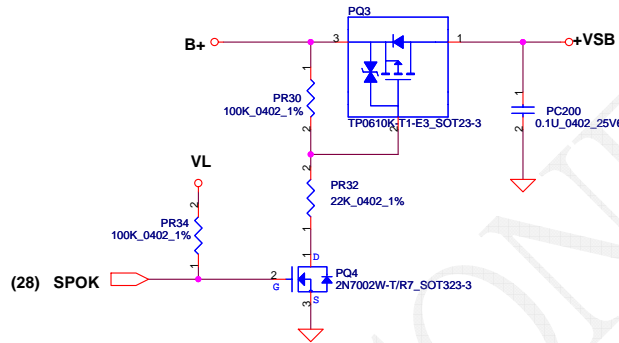
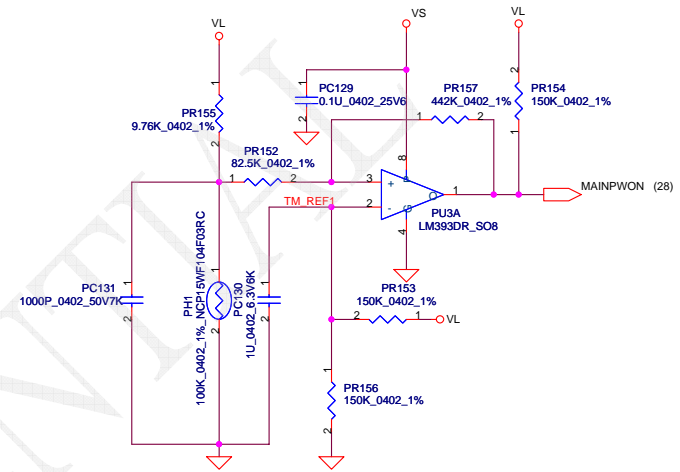


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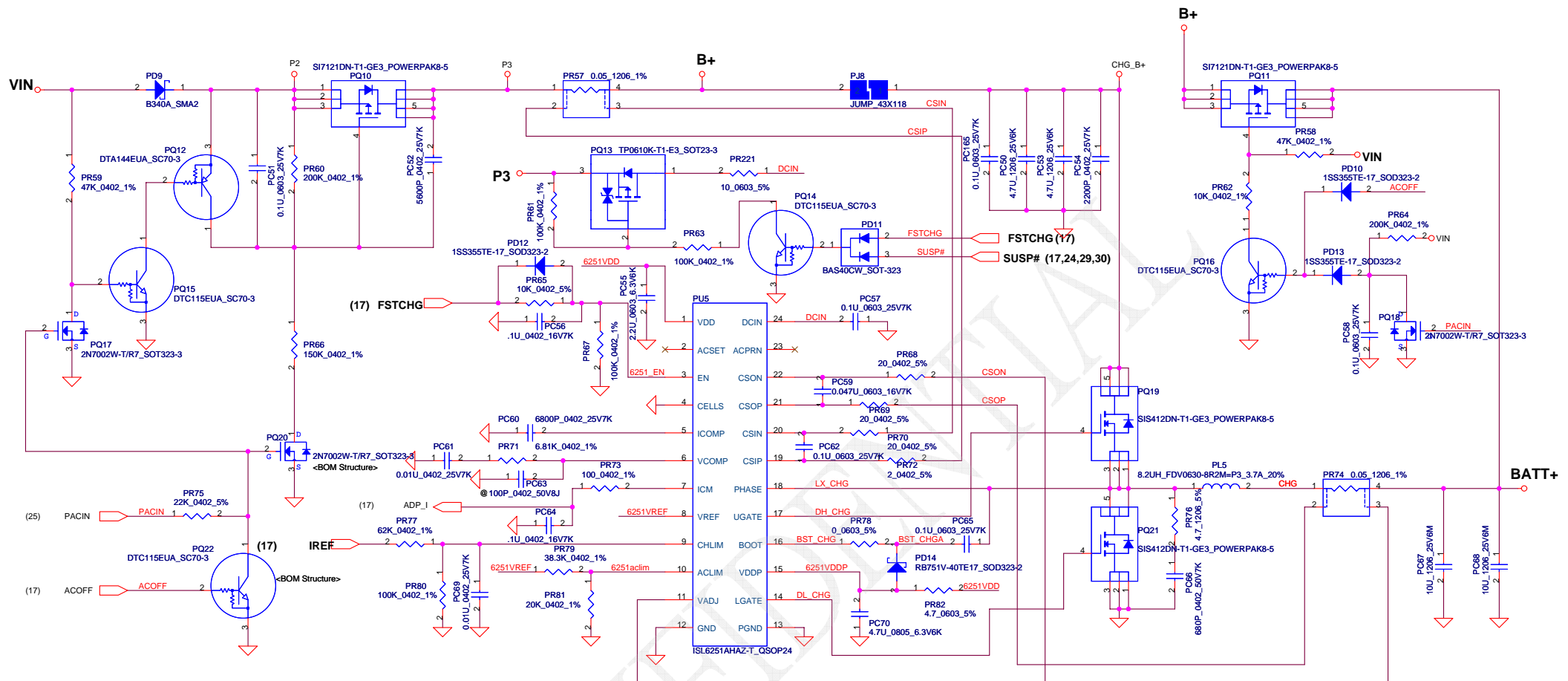


PH1 under CPU bottom side :
 CPU thermal protection at 90 degree C
 Recovery at 70 degree C



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$I_{ada} = 0 \sim 1.58A (30W)$ $CP = 85\% * I_{ada}$; $CP = 1.343A$

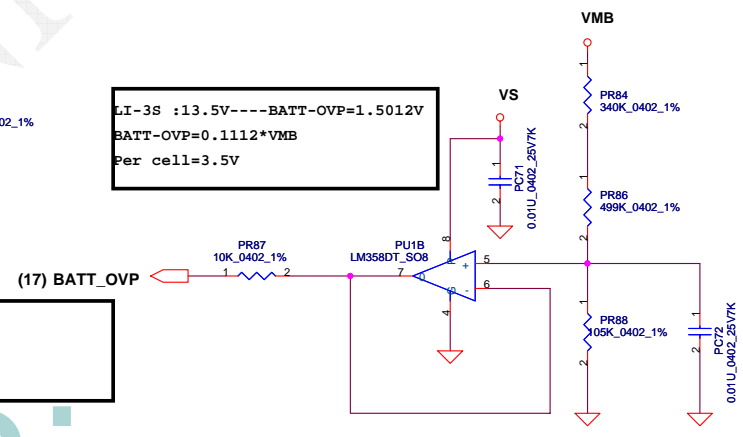
CP mode
 $V_{aclim} = 2.39 * (20K / (20K + 38.3K)) = 0.8199V$
 $I_{input} = (1 / 0.05) * ((0.05 * V_{aclim}) / 2.39 + 0.05)$
 where $V_{aclim} = 0.8199V$, $I_{input} = 1.343A$

$CC = 0.3 \sim 1.76A$
 $I_{REF} = 1.62 * I_{charge}$
 $I_{REF} = 0.486V \sim 2.85V$
 $3.24V \implies 2A$

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

$V_{ADJ} \rightarrow V_{REF} \rightarrow 4.41V$
 $V_{ADJ} \rightarrow \text{Ground} \rightarrow 3.99V$
 $V_{cell} = (0.175 * V_{ADJ} + 3.99)$

LI-3S : 13.5V --- BATT-OVP = 1.5012V
 $BATT-OVP = 0.1112 * V_{MB}$
 Per cell = 3.5V



(17) CALIBRATE#

(17) BATT_OVP

(17) FSTCHG

FSTCHG (17)
 SUSP# (17,24,29,30)

(25) PACIN

(17) ACOFF

(17) IREF

(17) ADP_1

(17) 6251VREF

(17) 6251VREF

(17) 6251VREF

(17) 6251VREF

(17) 6251VREF

(17) 6251VREF

(17) 6251VREF

(17) 6251VREF

(17) 6251VREF

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(17) 6251VREF

(17) 6251VREF

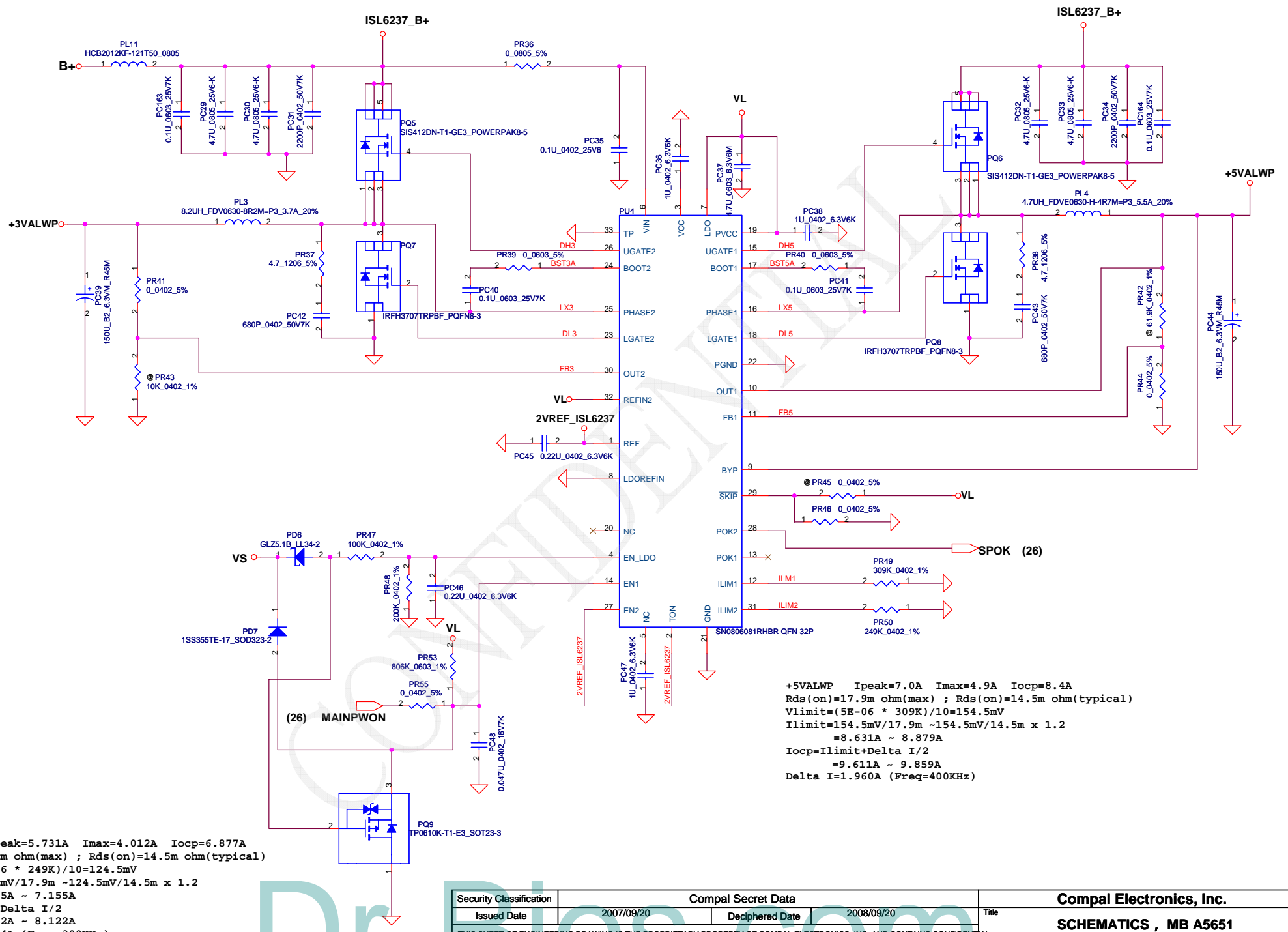
(17) 6251VREF

(17) 6251VREF

(17) 6251VREF

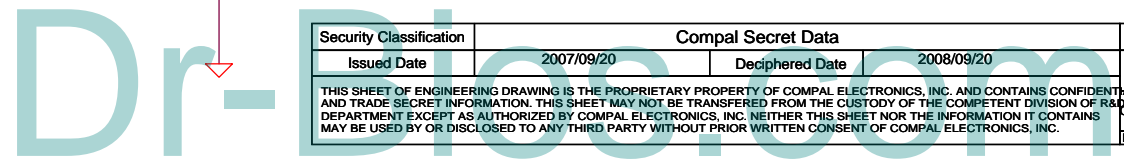
(17) 6251VREF

(17) 6251VREF

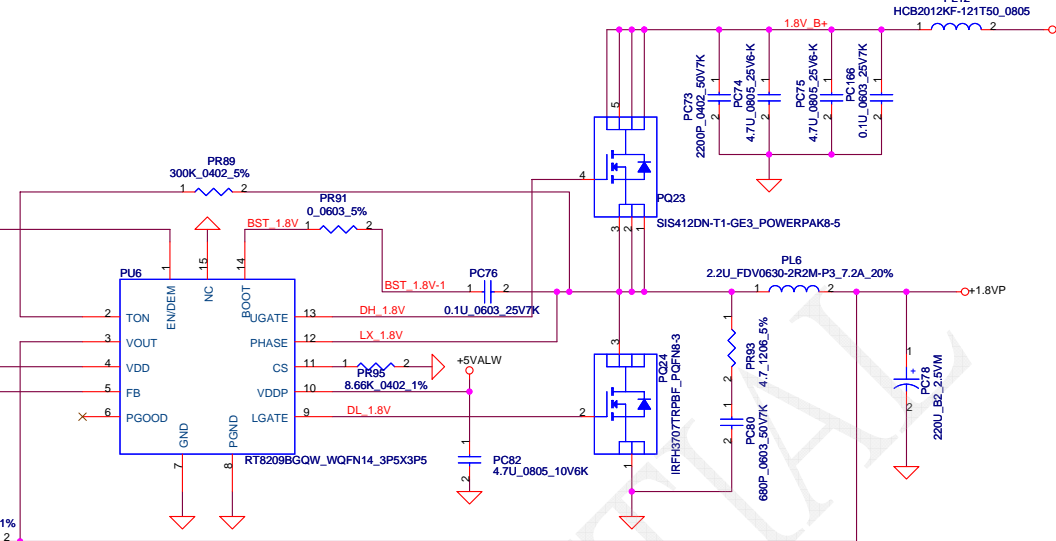
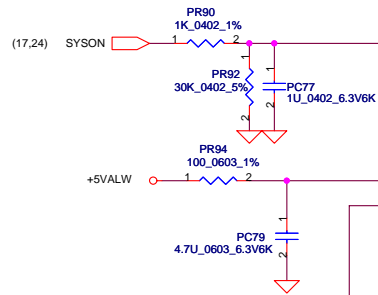


+3.3VALWP Ipeak=5.731A I_{max}=4.012A I_{ocp}=6.877A
 R_{ds(on)}=17.9m ohm(max) ; R_{ds(on)}=14.5m ohm(typical)
 V_{limit}=(5E-06 * 249K)/10=124.5mV
 I_{limit}=124.5mV/17.9m ~124.5mV/14.5m x 1.2
 =6.955A ~ 7.155A
 I_{ocp}=I_{limit}+Delta I/2
 =7.922A ~ 8.122A
 Delta I=1.934A (Freq=300KHz)

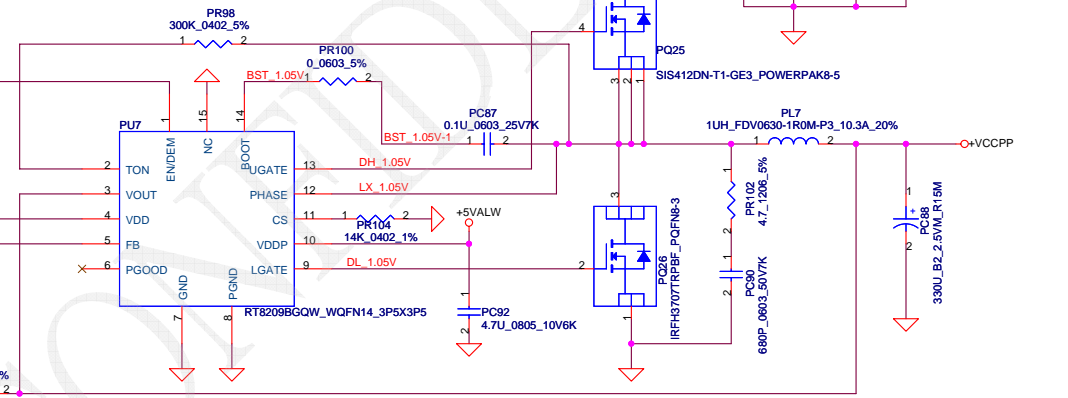
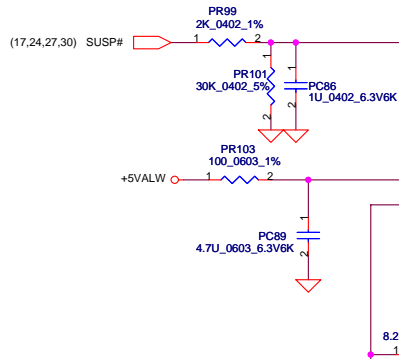
+5VALWP Ipeak=7.0A I_{max}=4.9A I_{ocp}=8.4A
 R_{ds(on)}=17.9m ohm(max) ; R_{ds(on)}=14.5m ohm(typical)
 V_{limit}=(5E-06 * 309K)/10=154.5mV
 I_{limit}=154.5mV/17.9m ~154.5mV/14.5m x 1.2
 =8.631A ~ 8.879A
 I_{ocp}=I_{limit}+Delta I/2
 =9.611A ~ 9.859A
 Delta I=1.960A (Freq=400KHz)



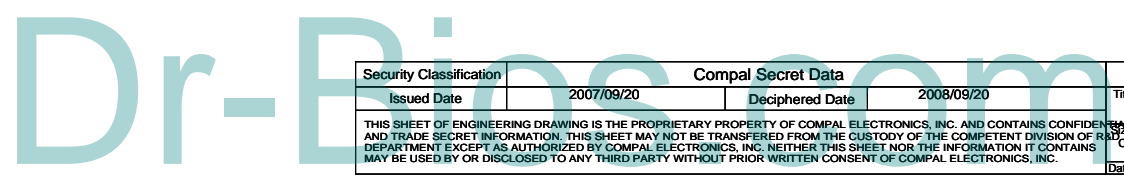
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Date:	Friday, May 21, 2010	Sheet	26	of	32



$V_o = 1.8V$ $V_{FB} = 0.75V$
 $V_o = V_{FB} * (1 + PR96/PR97) = 0.75 * (1 + 28.7K/20.5K) = 1.8V$
 $F_{sw} = 328KHz$
 $C_{out} ESR = 15m \text{ ohm}$ $R_{dson(max)} = 17.9m$ $R_{dson(typical)} = 14.5m$
 $I_{peak} = 4.97A$, $I_{max} = 3.479A$, $I_{ocp} = 5.964A$
 $\Delta I = ((19 - 1.8) * (1.8/19)) / (2.2u * 328K) = 2.259A$
 $\Rightarrow 1/2 \Delta I = 1.129A$
 $V_{trip} = R_{trip} * I_{0uA} = 8.66K * 10uA = 0.0866V$
 $I_{ocpmin} = V_{trip} / (R_{dsonmax}) + 1.129 = 0.0866 / (0.0179) + 1.129 = 5.967A$
 $I_{ocpmax} = (0.0866 / (0.0145 * 1.2)) + 1.129A = 6.106A$
 $I_{ocp} = 5.967A \sim 6.106A$



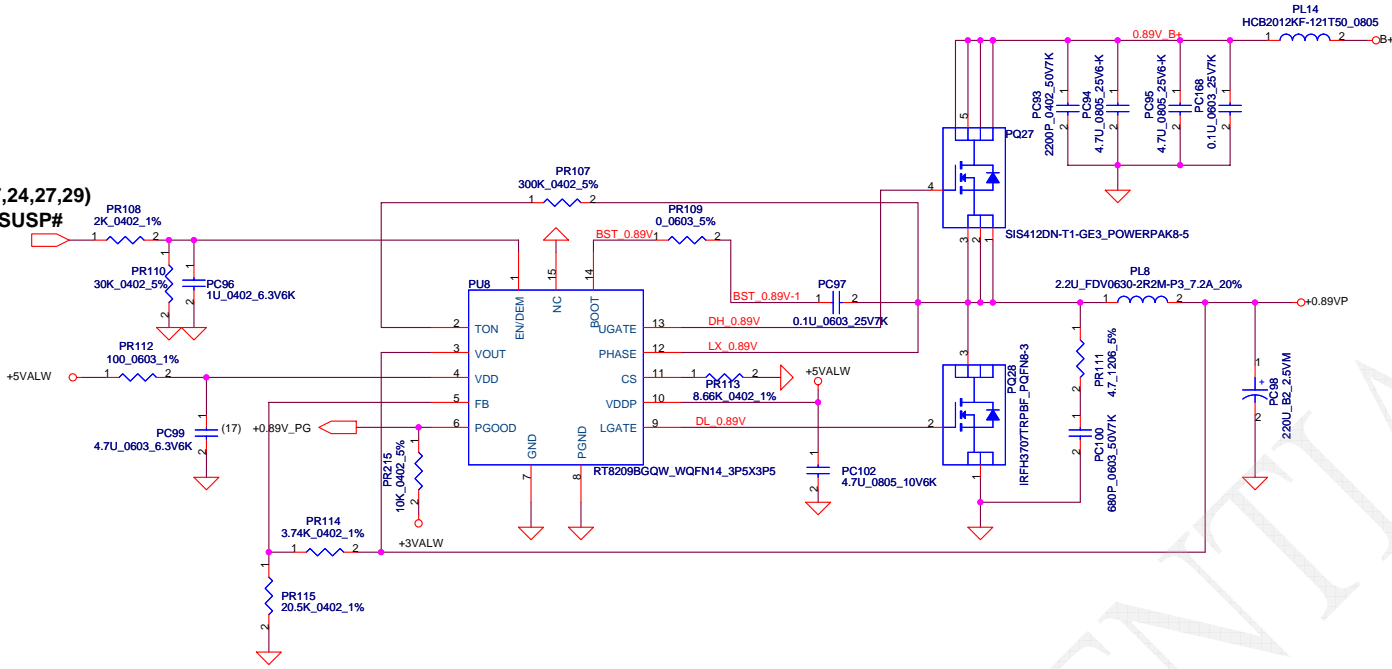
$V_o = 1.05V$ $V_{FB} = 0.75V$
 $V_o = V_{FB} * (1 + PR105/PR106) = 0.75 * (1 + 8.2K/20.5K) = 1.05V$
 $F_{sw} = 280KHz$
 $C_{out} ESR = 15m \text{ ohm}$ $R_{dson(max)} = 17.9m$ $R_{dson(typical)} = 14.5m$
 $I_{peak} = 3.124A$, $I_{max} = 2.187A$, $I_{ocp} = 3.749A$
 $\Delta I = ((19 - 1.05) * (1.05/19)) / (1.5u * 280K) = 3.549A$
 $\Rightarrow 1/2 \Delta I = 1.774A$
 $V_{trip} = R_{trip} * I_{0uA} = 14K * 10uA = 0.14V$
 $I_{ocpmin} = V_{trip} / (R_{dsonmax}) + 1.774 = 0.14 / (0.0179) + 1.774 = 9.596A$
 $I_{ocpmax} = (0.14 / (0.0145 * 1.2)) + 1.774A = 9.820A$
 $I_{ocp} = 9.596A \sim 9.820A$



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(17,24,27,29)

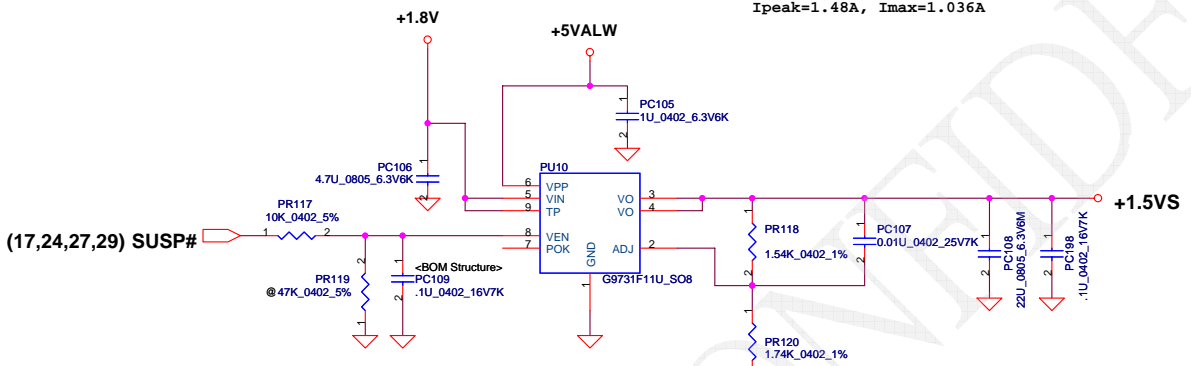
SUSP#



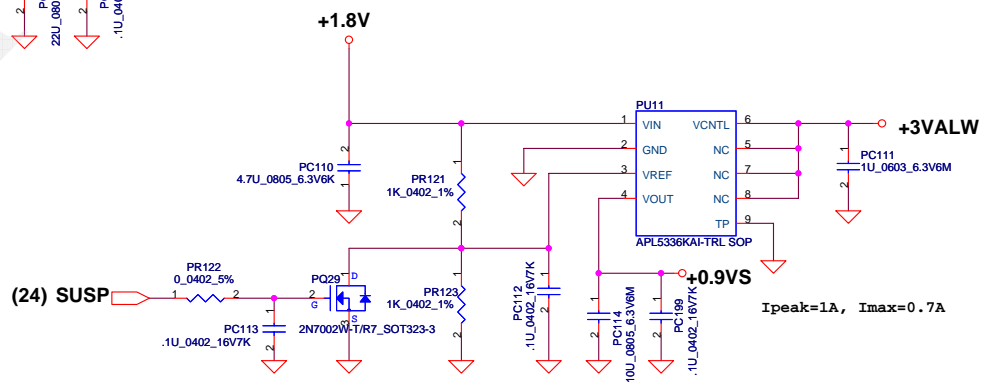
$V_o = 0.89V$ $V_{FB} = 0.75V$
 $V_o = V_{FB} * (1 + PR114 / PR115) = 0.75 * (1 + 28.7K / 20.5K) = 0.89V$
 $f_{sw} = 263KHz$
 $C_{out} ESR = 15m\ \Omega$ $R_{dson(max)} = 17.9m\ \Omega$ $R_{dson(typical)} = 14.5m\ \Omega$
 $I_{peak} = 1.38A$, $I_{max} = 0.966A$, $I_{ocp} = 1.656A$
 $\Delta I = ((19 - 1.8) * (1.8 / 19)) / (2.2u * 263K) = 1.467A$
 $\Rightarrow 1/2 \Delta I = 0.7335A$
 $V_{trip} = R_{trip} * I_{ouA} = 8.66K * 10uA = 0.0866V$
 $I_{ocpmin} = V_{trip} / (R_{dsonmax}) + 0.7335$
 $= 0.0866 / (0.0179) + 0.7335 = 5.572A$
 $I_{ocpmax} = (0.0866 / (0.0145 * 1.2)) + 0.7335A = 5.711A$
 $I_{ocp} = 5.572A - 5.711A$

Ipeak=1.48A, Imax=1.036A

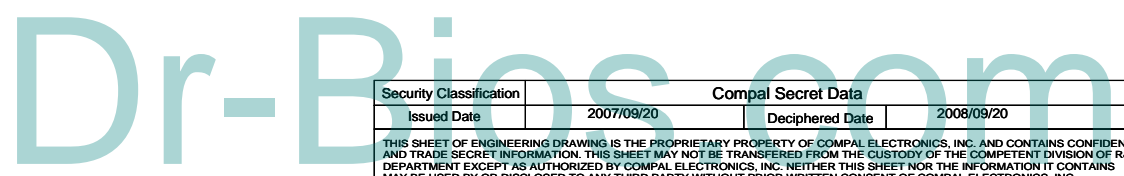
(17,24,27,29) SUSP#



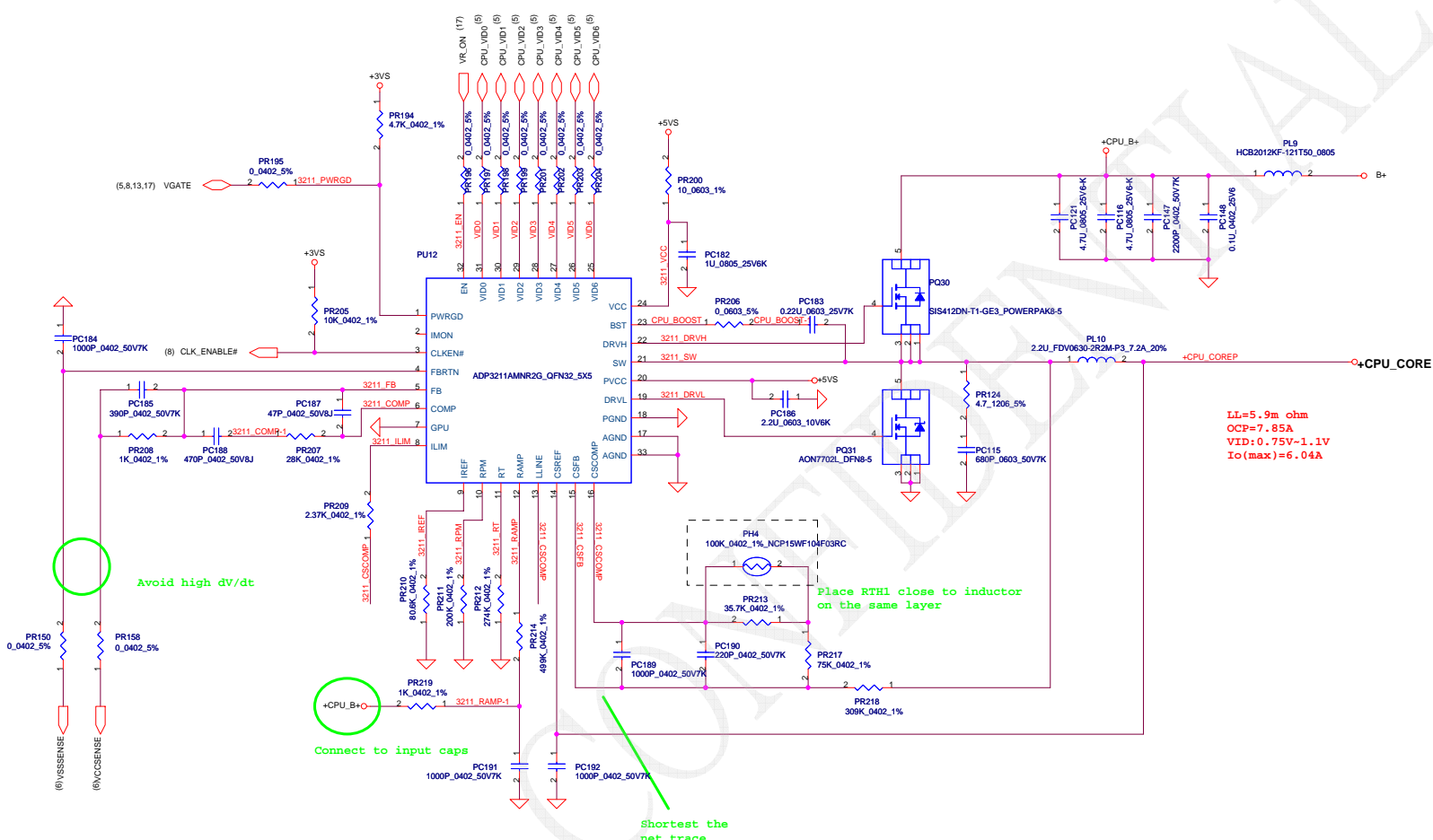
(24) SUSP



Ipeak=1A, Imax=0.7A



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LL=5.9m ohm
 OCP=7.85A
 VID=0.75V-1.1V
 Io(max)=6.04A

Place RTH close to inductor
 on the same layer

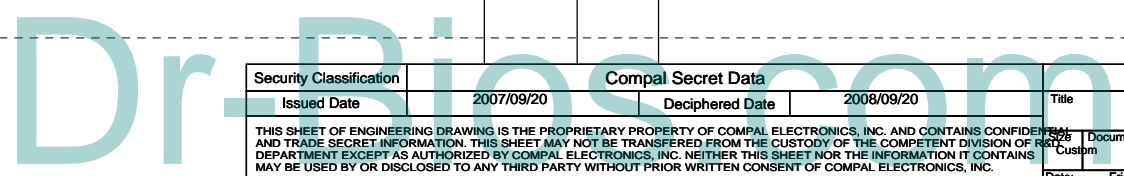
Dr-Bios.com

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	add PC200	For design change	0.1	24		2009.5.15	EVT
2	add PC193,PC194	For design change	0.1	26		2009.5.15	EVT
3	add PC195,PC196	For design change	0.1	27		2009.5.15	EVT
4	add PC197,PC198,PC199	For design change	0.1	28		2009.5.15	EVT
5	change PL3,PL4	For design change	0.1	26	change PL3,PL4 to 4.7uH	2009.5.15	EVT
6	change PQ10,PQ11	For design change	0.1	25	change PQ10,PQ11 to P-Chanel	2009.6.5	EVT
7	add PC165	Solution for 3G noise reduce	0.1	25		2009.6.5	EVT
8	add PC163,PC164	Solution for 3G noise reduce	0.1	26		2009.6.5	EVT
9	add PC166,PC167	Solution for 3G noise reduce	0.1	27		2009.6.5	EVT
10	add PC168	Solution for 3G noise reduce	0.1	28		2009.6.5	EVT
11	delete PC103,PC1120	For design change	0.1	29		2009.6.5	
12	change PR94,PR102	For design change	0.1	27	change PR94,PR102 to 100ohm	2009.6.5	
13	change PC79,PC89	For design change	0.1	27	change PC79,PC89 to 4.7uF	2009.6.5	
14	change PR112	For design change	0.1	28	change PR112 to 100ohm	2009.6.5	
15	change PC99	For design change	0.1	28	change PC99 to 4.7uF	2009.6.5	
16	change +5VALW/+3VALW OCP	For design change	0.1	26	change PR49 to 309ohm & PR50 to 249ohm	2009.6.5	
17	add PJ1,PJ2,PJ3,PJ4,PJ5,PJ6,PJ7	For design change	0.1	25		2009.6.15	
18	add PJ9,PJ10	For design change	0.1	28		2009.6.15	
19	Change net name	For design change	0.1	25	Change net name +1.05V to +VCCP	2009.6.15	
20	Change PJP2	For design change	0.1	24	Change PJP2 to DC040903020	2009.6.15	
21	Change PBJ1	For design change	0.1	23	Change PBJ1 to SP020008Y00	2009.6.15	
22	delete PJ6,PJ7,PJ9,PJ10	For design change	0.1	28		2009.6.18	
23	Change net name	For design change	0.1	29	Change net name GND_SIGNAL to GND	2009.6.18	

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Change PR194	For design change	0.1	29	change PR194 to 4.7K ohm	2009.6.30	EVT
2	add PR221	For design change	0.1	25		2009.6.30	EVT
3	Change PR4	For design change	0.1	23	change PR4 to 0 ohm	2009.7.2	EVT
4	Change PJP3 to PBJ1	For design change	0.1	23	change SP020008Y00 to SP093MX000	2009.8.4	EVT
5	Change PH1 & PH4	For design change	0.1	24	change SL210031F00 to SL200000V00	2009.8.12	EVT
6	Change PL10	For design change	0.1	29	change SH000006I80 to SH000000700	2009.8.12	EVT
7	Change PR99 & PR108	Modify power sequence	0.1	27	change SD028000080(0 ohm) to SD034200280(20K ohm)	2009.8.12	EVT
8	Change PR90	Modify power sequence	0.1	27	change SD028000080(0 ohm) to SD034100280(10K ohm)	2009.8.12	EVT
9	Change PR83	Modify ISL6251 Charger KV	0.1	25	change SD034182280(18.2 ohm) to SD034154280(15.4K ohm)	2009.8.24	EVT
10	Change PR117	Modify power sequence	0.1	28	change SD028000080(0 ohm) to SD034100280(10K ohm)	2009.8.24	EVT
11	Change PR99 & PR108	Modify power sequence	0.1	27	change SD034200280(20K ohm) to SD034200180(2K ohm)	2009.8.24	EVT
12	Change PR90	Modify power sequence	0.1	27	change SD034100280(10K ohm) to SD034100180 (1K ohm)	2009.8.24	EVT
13	Change PC77 & PC86 & PC96	Modify power sequence	0.1	27	Change PC77 & PC86 & PC96 to pop change SE076104KM8(0.1uf) to SE000000K80 (1uf)	2009.8.24	EVT
14	Change PC109	Change part number	0.1	27	change SE076104KM8(0.1uf) to SE076104K80(0.1uf)	2009.8.24	EVT
15	Change PL3.PL4	To slove high frequency noise	0.1	26	change SH00000BU00(4.7uH) to SH00000BS00(8.2uH)	2009.8.27	EVT
16	Change PL9	For design change	0.1	29	change SM01000BY00 to SM01000C000	2009.9.4	DVT
17	Change PL4	To improve +5VALWP efficiency	0.1	26	change SH00000BS00(8.2uH) to SH00000F900(4.7uH)	2009.9.10	DVT
18	Change PR209	Modify CPU CORE OCP	0.1	29	change SD028180180(1.8K ohm) to SD034237180 (2.37K ohm)	2009.9.30	PVT
19							
20							
21							
22							
23							



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<2009/4/28>
 Update new power schematic,
 release first version NAV50 schematic

<2009/04/29>
 . Add R1182 R1183 L3 on page 9
 . Change J3 to R1184 on page 13

<2009/04/30>
 . Change JDIM1 to SP07F001720 on page 7
 . Del SATA1 Port on page 12
 . Change R51 R57 R70 R63 R317 R314 R190 to 0402 Size on page 21

<2009/05/04>
 . Add WWAN_CLKREQ# and R107 pull-high to +3VS on page 8
 . Add CRT_DET# on page 10
 . Add CRT_DET# circuit on page 13
 . Add 3 LEDS on page 16
 . Add BT/BTN Board CONN. on page 16
 . Update TP/B CONN. to SP01000LB00 on page 19

<2009/05/11>
 . Add INVT_PWM on Page 5
 . Del R323 on page 5
 . C74 change to 2.2U_0603 on page 6
 . C267 change to 22U on page 6
 . C391 change to 0.1U on page 6
 . Del C67 C35 C33 C36 on page 6
 . Del +LGI_VID and U71.A21 direct connect to +VCCP on page 6
 . Follow Intel checklist, add R52 on FSB on page 8
 . Add D5 D7 D8 on page 4
 . Add R174 on page 9
 . Add PCI_RST# on page 11
 . Add C1115 C1114 C1116 C1117 C1118 on page 15

<2009/05/12>
 . Follow Intel Layout Checklist, Add C141 on VDDSPD on page 7
 . Modify SRC CLK PORT LIST on page 8
 . Del CLKREQ_LAN# on page 8
 . Change PCIE Port list on page 13
 . Change USB Port list on page 13
 . Add W/L 3G SW on page 16
 . Del R103 on page 18

<2009/05/13>
 . Change JMINI1 to PCIE Port 3 on page 15

<2009/05/14>
 . Page8 Change C174 C175 to 10U_0603

<2009/05/14>
 . Update New Power schematic
 . Del R376 R377 on page 8
 . Del D5 D7 D8 on page 4
 . Change JLVDS1 to SP010006810 on page 9
 . Add D6 for EMI on page 9
 . Change C1106 to C_0603 type on page 9
 . Change USB_OC# on page 13
 . Add USB Port2 on page 20
 . Change JP11 Pin define & Add D22 on page 19
 . Change C512 to 1u_0402 on page 15
 . Add U29 (MEDIA_LED#) on page 16

<2009/05/19>
 .Update new clock GEN co-lay schematic on page 8

<2009/06/05>
 .Update new clock GEN co-lay schematic on page 8
 .Follow Intel check list change C161 C165 to 27P on page 8
 .Follow Intel check list change C56 to 22uF on page 6

<2009/06/08>
 .Update New Power schematic 06/06 version
 Page 13- a. Del R203 (pull-up GPIO6 Resister)
 b. Change R1184 NU
 Page 17- a. Add VGATE
 b. Del R1294
 c. Change D30 NU
 d. Change R1295 to 0 ohm
 e. Add R1309 0 ohm on EC_RSMRST#
 f. Pull-up LAN_WAKE# +3VALW
 g. ICH_POK change to PCH_POK
 h. Pull-up KB_RST# to +3VS
 Page 10- a. Add R1283 R1284 ,Change R247 R249 to 10 ohm
 b. Add @ on U10 U11 C301 C298
 c. Del C302 C300 R1281 R1287

<2009/06/10>
 . Page 7- Add C116 @
 . Page 22- Modify USB_OC#1_2 to USB_OC#2
 . Page 17- Modify PLTRST# to PCI_RST#
 . Page 17- Add @ on R1311

<2009/06/12>
 . Page4 Add C314 C313 C1150 D19 on +VCC_FAN1
 . Page8 Add C1145 C1146 C1147
 . Page10 Move CRT_DET# from Page13 to Page10
 . Page13 Add +RTCVCC circuit

<2009/06/15>
 . Update New Power schematic (change PBJ1 to PJP3)
 . Page 10 modify C310 C308 C303 C307 C306 C304 Bom Structure
 . Page 22 Modify Hole location by (ME drawing 06/12)

<2009/06/16>
 . Page7 Modify DDR Command Control Pin pull-high Resister location
 . Page9 Change R577 to 0402 type

<2009/06/17>
 . Update New Power schematic 06/17
 . Page9 modify LVDS Conn. Pin define
 . Page9 Del C1110
 . Page4 Add EMI solution D38 D39 D40

<2009/06/18>
 . Update New Power schematic 06/18
 . Page8 modify U4 Pin define and Q31
 . Page13 Add R1376, R1377
 . Page15 Modify C403
 . Page23 Modify H11

<2009/06/19>
 . Page4 Add new signal CPU_ITP , CPU_ITP#
 . Page5 ADD R1378
 . Page6 ADD C1152,C1153,C1154 C1160,C1161,C1162
 . Page7 DDR_A_D8與DDR_A_D9互換
 . Page8 ADD R1379,R1380,U77,R1381,C1157,R1382,R1383,R1384,C1157
 . Page8 DEL C390
 . Page9 ADD C1156
 . Page11 DEL R1322, R1154
 . Page13 DEL U77, ADD C1158
 . Page17 ADD C1159

<2009/06/22>
 . Page22 change IO Conn. pin34 from 48M to USB_ON#
 . Page10 change JCRT1 P/N to SP010906182

<2009/06/23>
 . Page15 Add C1163 C1164 C1165 C1166
 . Page18 change PWR/B Conn. P/N to SP01000H300
 . Page22 change JUSB1 JUSB2 P/N

<2009/06/24>
 . Page8 Change C1350 C1351 to 0402 type
 . Page10 Add R1385 R1386 on JVGA_HS JVGA_VS

<2009/06/25>
 . Page22 move some parts to I/O Board , Add the MONO_IN_R on M/B

<2009/06/29>
 . Page16 Change JP24 to ACES_88266_05001
 . Page15 Change JMINI1 to FOX_AS0B246-S50U-7F_52P-T

<2009/06/30>
 . Page18 Change PWR_LED# to PWR_PWM_LED#
 . Page17 Add PWR LED DETECT PIN on Pin97

<2009/07/02>
 . Update New Power schematic 07/02
 . Page9 Add C1167 C1168 for RF request.
 . Page13 Change R223 to 100K
 . Page16 change JP24 to ACES_85201-0505N
 . Page17 Del R1387 R1388 on EC Pin97
 . Page17 Add New Board ID to separate NAV50 NAV60
 . Page17 Change 展頻IC to SA00003J400 (New)
 . Page18 Add D41 for ESD

<2009/07/03>
 . Page18 Add D41.2 to PWR_PWM_LED#
 . Page8 Change co-lay net name to +1.5VM_CK505
 . Page20 Change JP2 Pin42 to +5VS

<2009/07/06>
 . Page18 Add pwr switch for NAV50

<2009/07/08>
 . Page5 Add 470pf on H_SMI# for known issue.

<DVT START>

<2009/08/04>
 . Page5 CLK_CPU_HPLCLK CLK_CPU_HPLCLK# exchange
 . Page9 Change JLVDS1 to P/N ACES 88341-3001 30P
 . Page17 del PM_1.8V(U6.82) ,Del R1310 R1311
 . Page18 Del D41

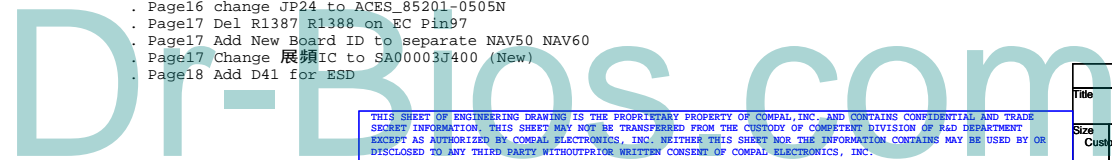
<2009/09/03>
 . Page7 Change C112 to 0402 type
 . Page8 Add T6 on CLK_48M_CR
 . Page16 Modify JP18 Pin define change +5VALW +5VS to +3VALW +3VS
 . Page20 Change Pin 18, 23 to +1.5VS change Pin7 , 9 to USB20_P7 N7
 . Page21 Del H12

<2009/09/08>
 Update Power schematic 0904
 . Page18 Change R1388 to 100 ohm 0402
 . Page18 Change LED1 to SC591NB5A00

<2009/09/10>
 Update Power schematic 0910
 . Page22 unmount Q6 Q8

<2009/10/07>
 . Page4 U71 Change to SA00003M800
 . Page6 R26 Change to SHI00009C00
 . Page13 R152 Change to SD034200A80
 . Page18 R1388 Change to SD028510A80

<2010/04/29>
 update new bom



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