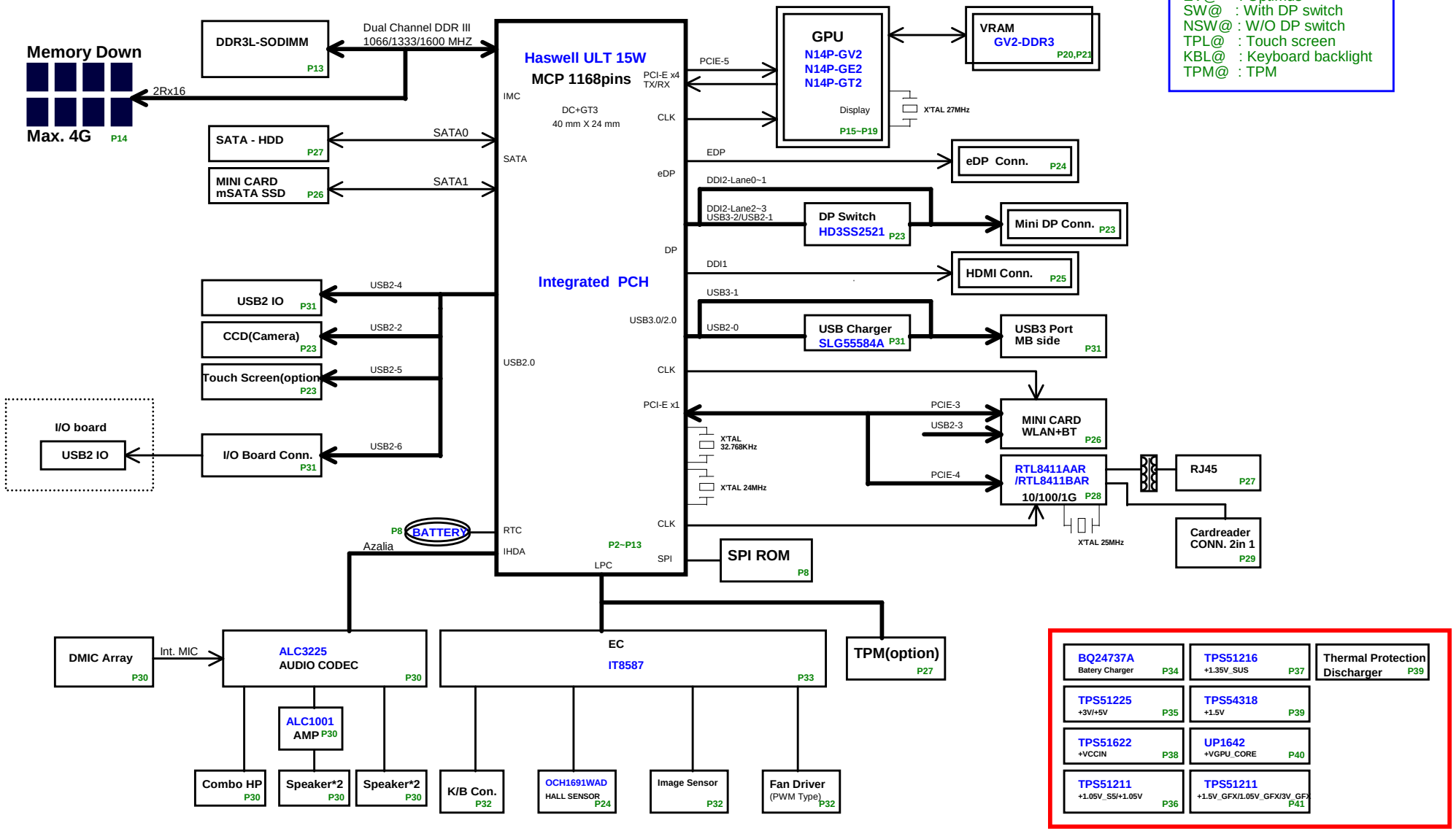
ZRQ GDDR3 SHB ULT SYSTEM BLOCK DIAGRAM

01

BOM

IV@ : iGPU
EV@ : Optimus
SW@ : With DP switch
NSW@ : W/O DP switch
TPL@ : Touch screen
KBL@ : Keyboard backlight
TPM@ : TPM



Quanta Computer Inc.
PROJECT : ZRQ
Block Diagram
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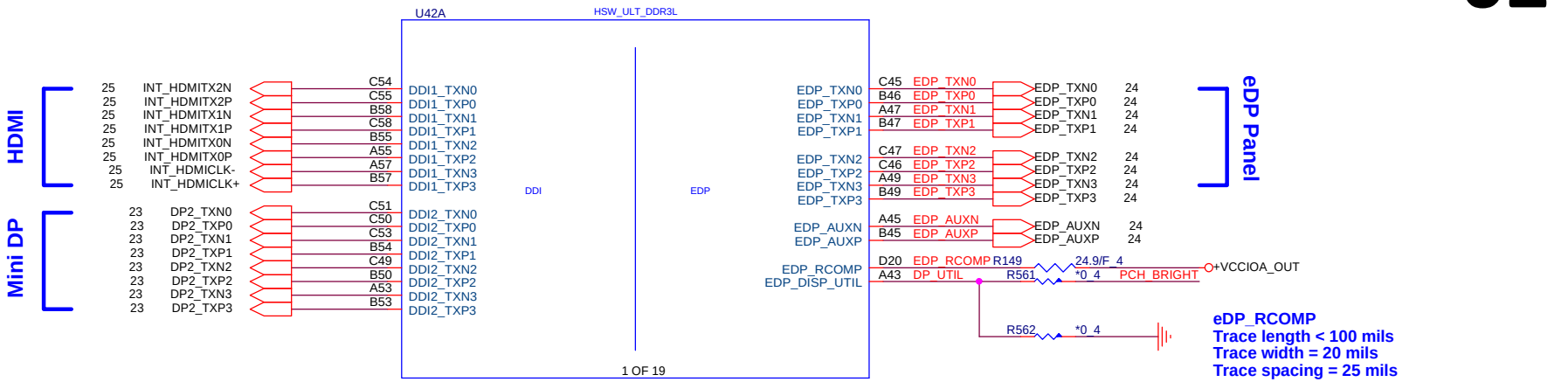
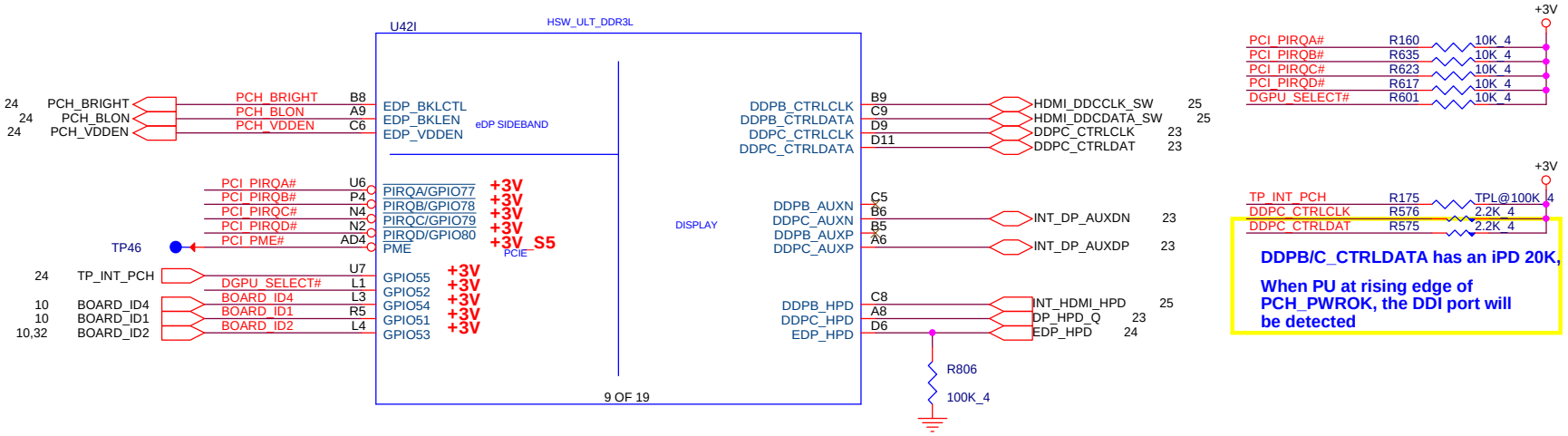
Haswell ULT (DISPLAY,eDP)

02





Quanta Computer Inc.		
PROJECT : ZRQ		
Size	Document Number: Haswell 3/5 (DDI/eDP)	Rev 3A
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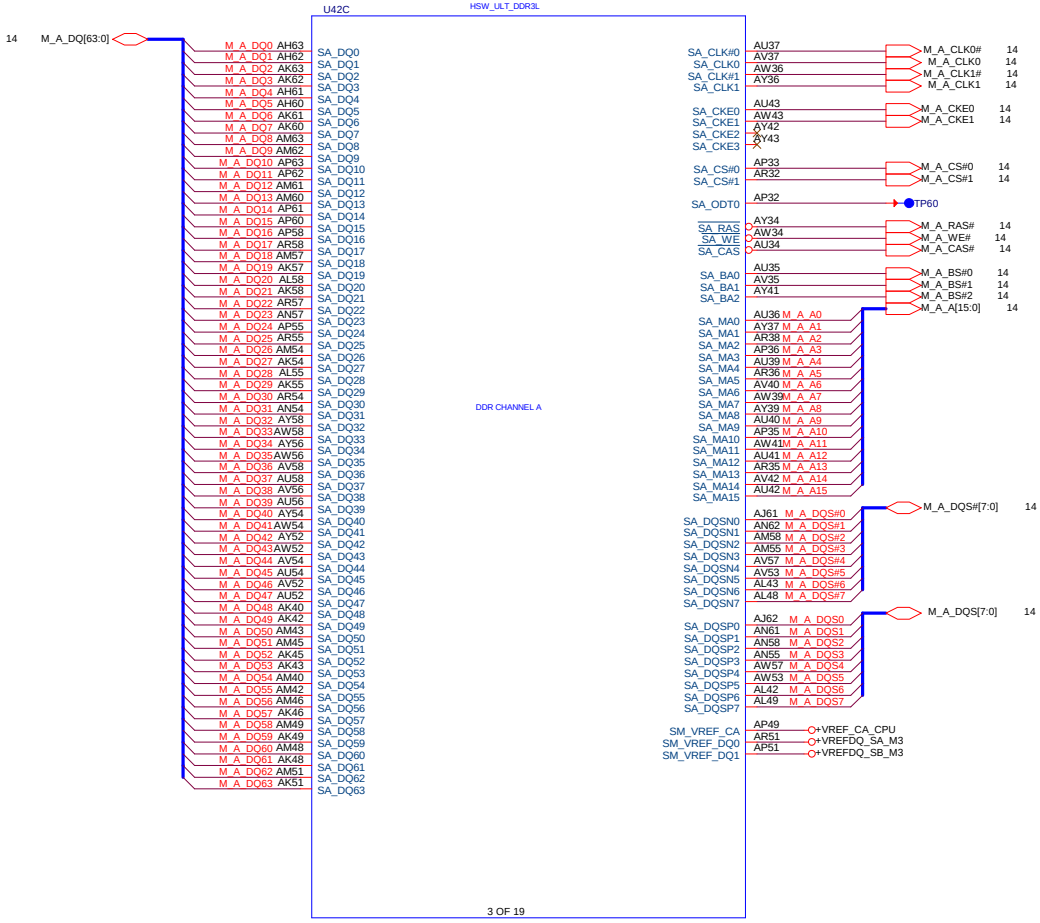
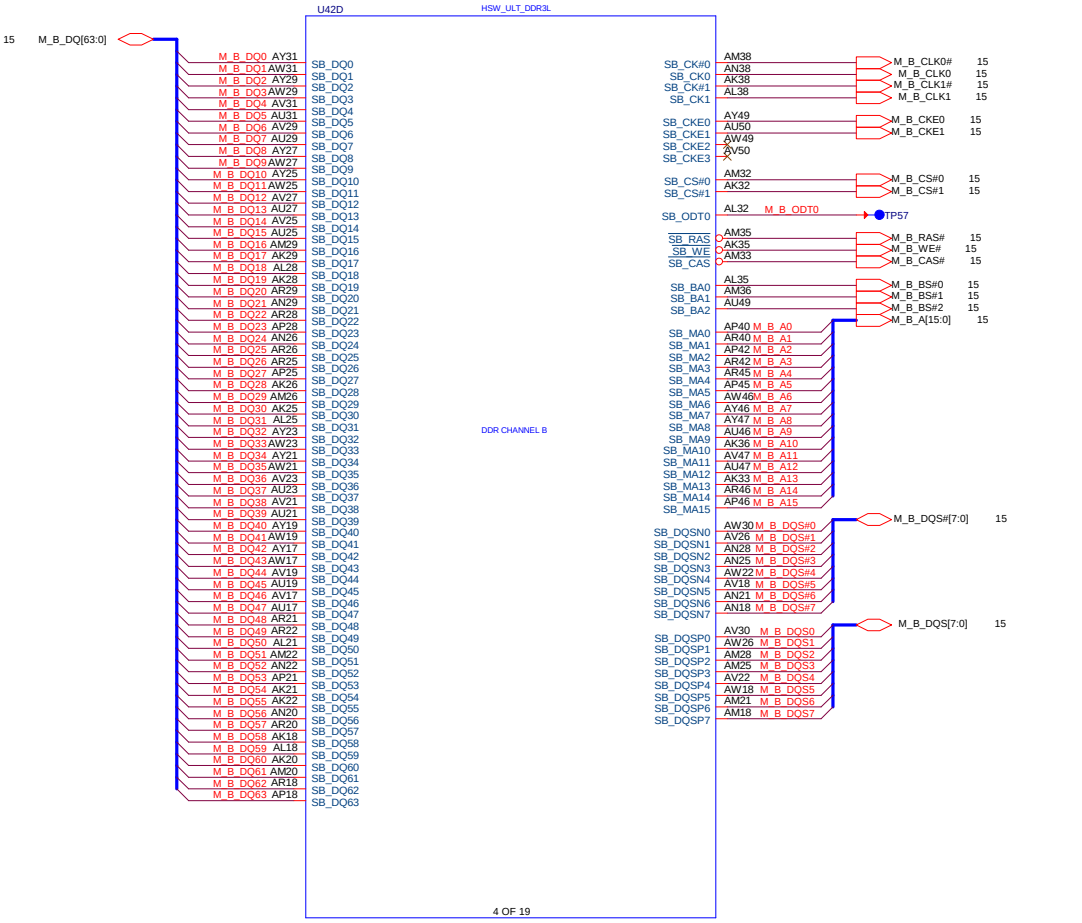
Haswell ULT (DDR3L)



Haswell Processor (DDR3)



03

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Size	Document Number	Rev
	Haswell 2/5 (DDR3 I/F)	3A

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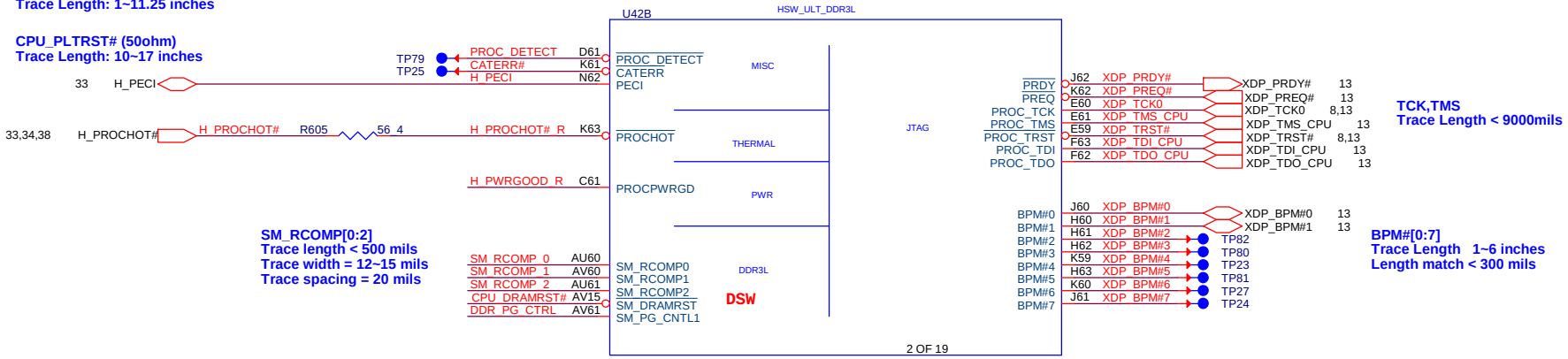
Haswell ULT (SIDEBAND)

H_PECI (50ohm)
Route on microstrip only
Spacing >18 mils
Trace Length: 0.4~6.125 iches

H_PWRGOOD (50ohm)
Trace Length: 1~11.25 inches

CPU_PLTRST# (50ohm)
Trace Length: 10~17 inches

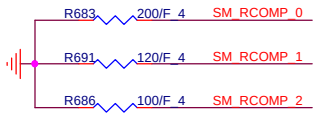


TCK,TMS
Trace Length < 9000mils

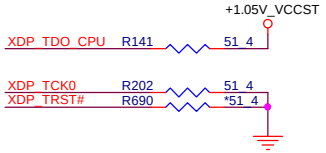
SM_RCOMP[0:2]
Trace length < 500 mils
Trace width = 12~15 mils
Trace spacing = 20 mils

BPM#[0:7]
Trace Length 1~6 inches
Length match < 300 mils

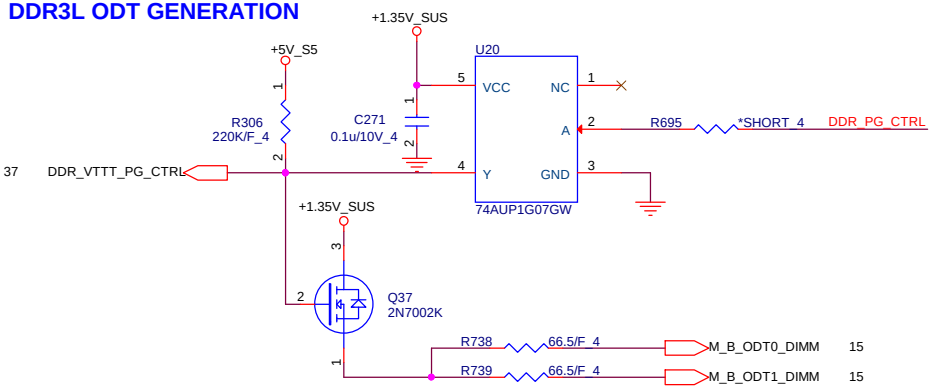
DRAM COMP



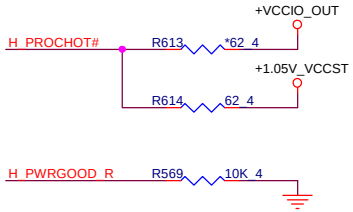
XDP PU/PD



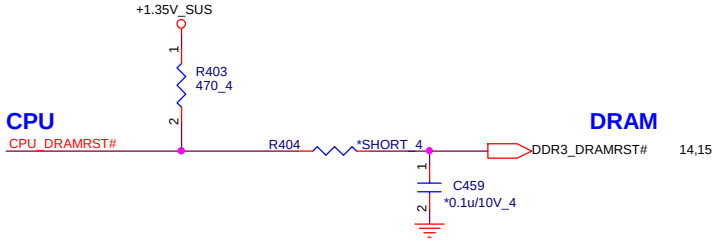
DDR3L ODT GENERATION



PU/PD of CPU



DRAMRST



Quanta Computer Inc.		
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Size	Document Number: Haswell 1/5 (PEG/DMI/FDI)	Rev: 3A
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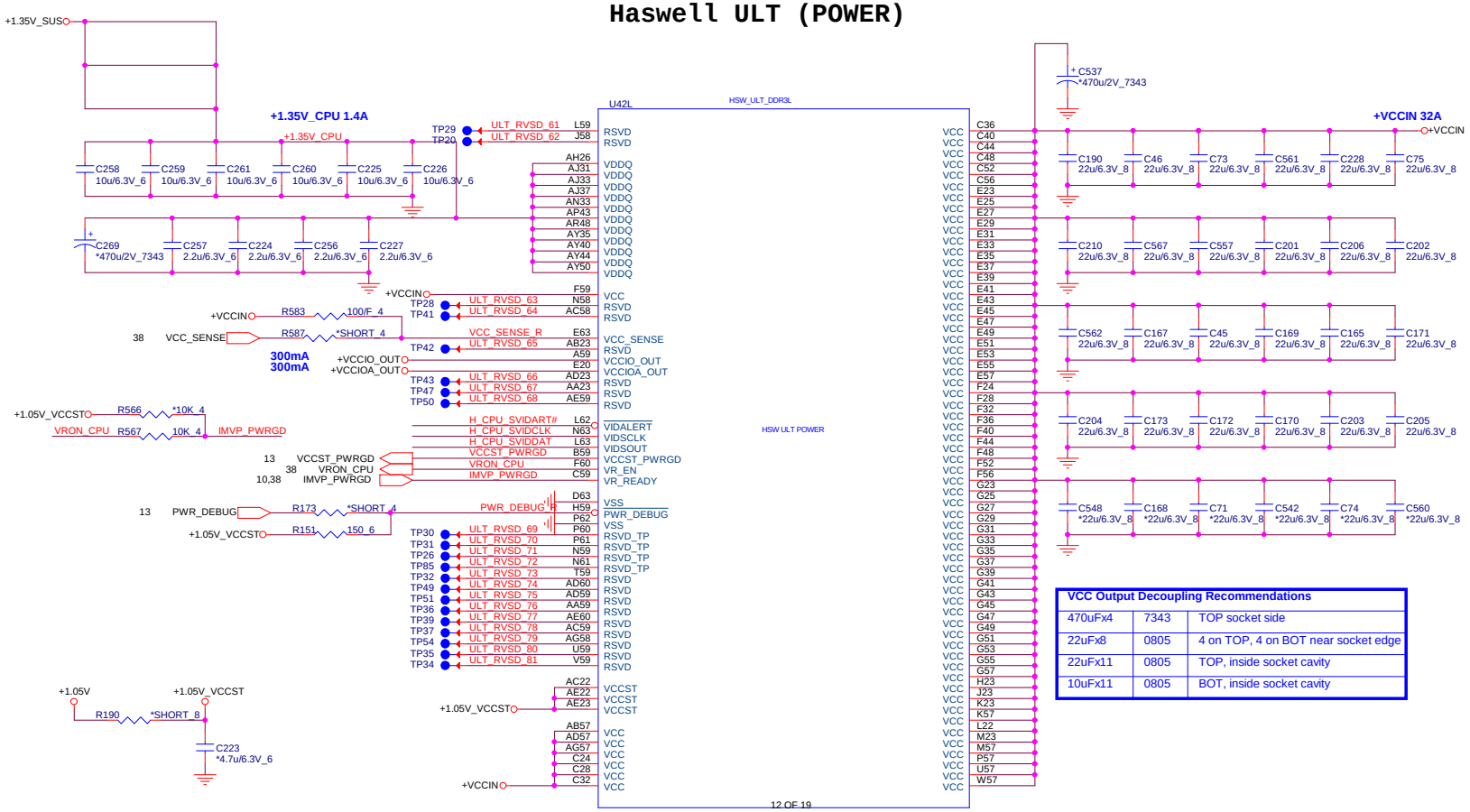
Haswell ULT (POWER)

VDDQ Output Decoupling Recommendations		
330uFx2	7343	BOT socket side
22uFx11	0805	5 onTOP, 6 on BOT inside socket cavity
10uFx10	0805	5 onTOP, 5 on BOT inside socket cavity

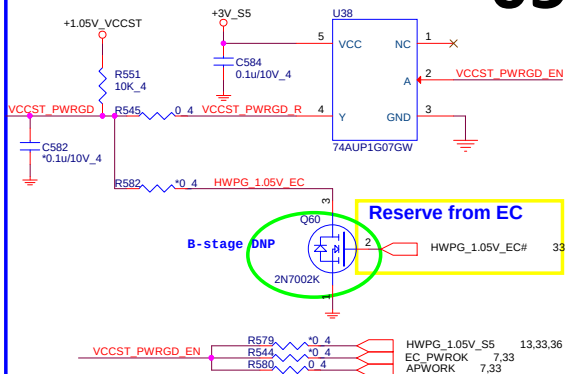


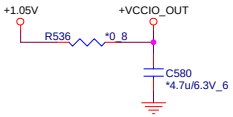
VCC Output Decoupling Recommendations		
470uFx4	7343	TOP socket side
22uFx8	0805	4 on TOP, 4 on BOT near socket edge
22uFx11	0805	TOP, inside socket cavity
10uFx11	0805	BOT, inside socket cavity

VCCST PWRGD

CRB is via +1.05V PG

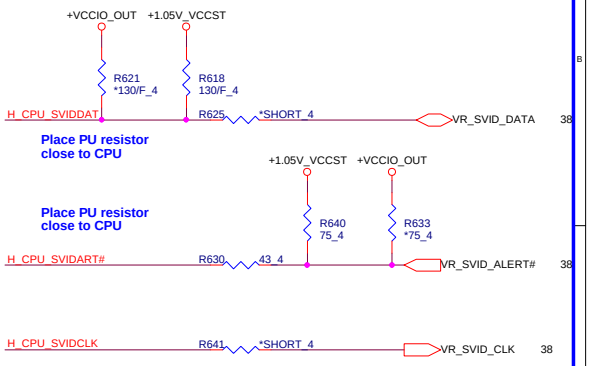
05



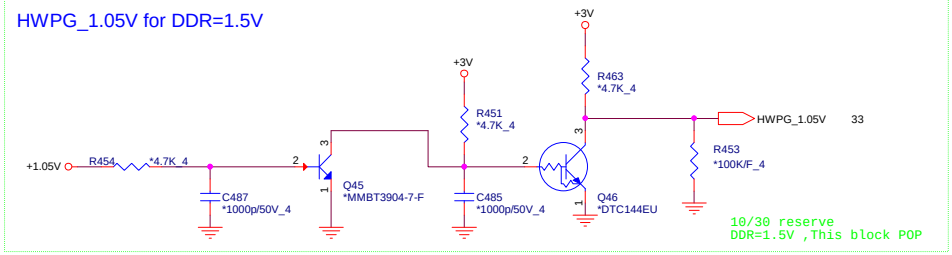


SVID

Layout note: need routing together and ALERT need between CLK and DATA.



HWPG_1.05V for DDR=1.5V



Quanta Computer Inc.
PROJECT : ZRQ

Size	Document Number	Rev
	Haswell 4/5 (POWER)	3A
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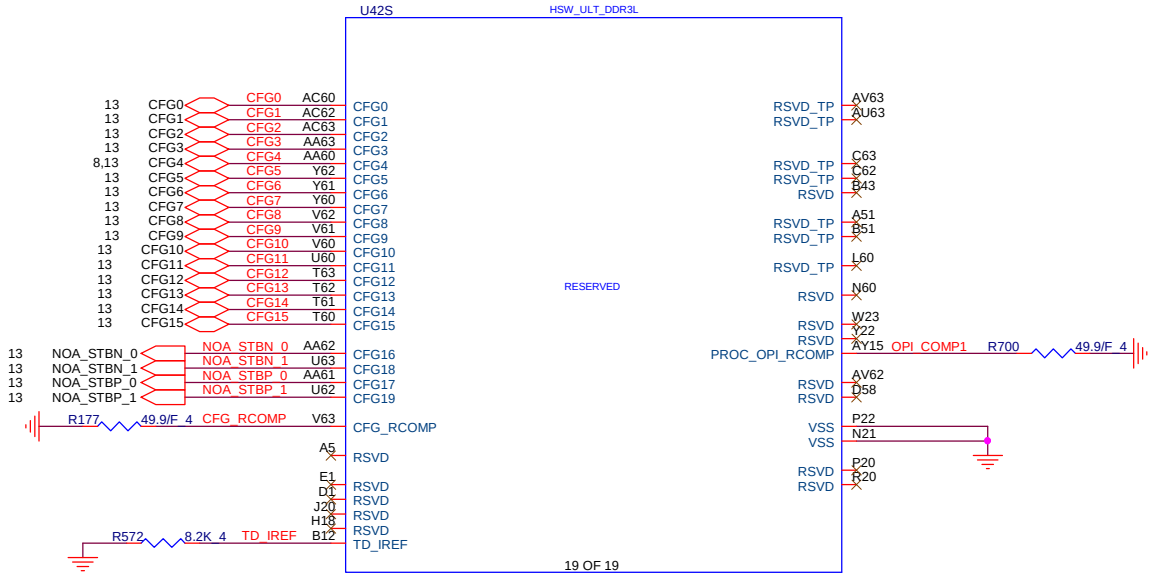
Haswell ULT (CFG,RSVD)

06



Processor Strapping

	1	0	
CFG0 EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED	**(DEFAULT) NORMAL OPERATION; NO STALL**	STALL	CFG0 R203 *1K_4
CFG1 PCH/ PCH LESS MODE SELECTION	**(DEFAULT) NORMAL OPERATION**	PCH-LESS MODE	CFG1 R184 *1K_4
CFG3 PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	**DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT**	ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT	CFG3 R192 *1K_4
CFG 8 ALLOW THE USE OF NOA ON LOCKED UNITS	**DISABLED(DEFAULT); IN THIS CASE, NOA WILL BE DISABLED IN LOCKED UNITS AND ENABLED IN UN-LOCKED UNITS**	ENABLED; NOA WILL BE AVAILABLE REGARDLESS OF THE LOCKING OF THE UNIT	CFG8 R171 *1K_4
CFG9 NO SVID PROTOCOL CAPABLE VR CONNECTED	**VRS SUPPORTING SVID PROTOCOL ARE PRESENT**	NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY	CFG9 R172 *1K_4
CFG10 SAFE MODE BOOT	**POWER FEATURES ACTIVATED DURING RESET**	POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED	CFG10 R183 *1K_4

Quanta Computer Inc.

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	Haswell 5/5 (CFG/GND)	3A

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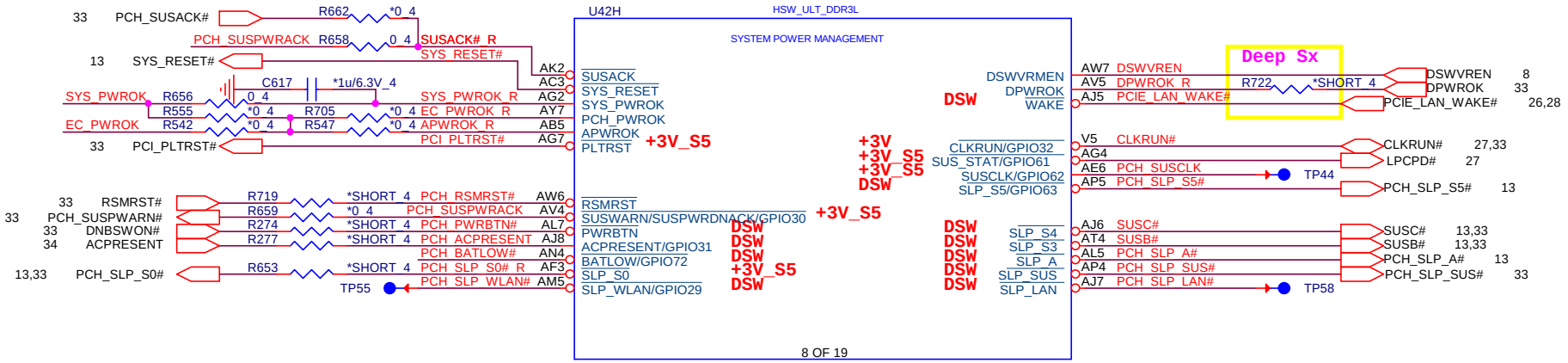
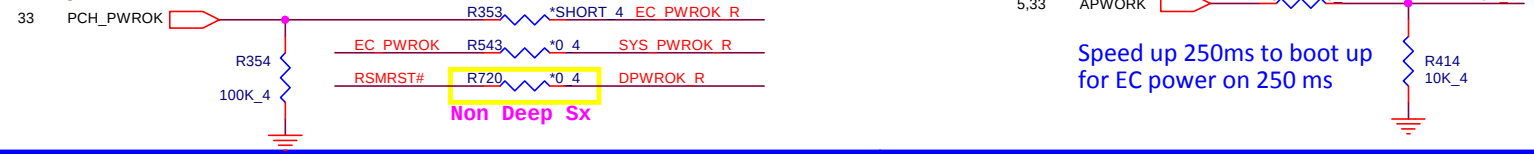
Haswell ULT PCH (PM)

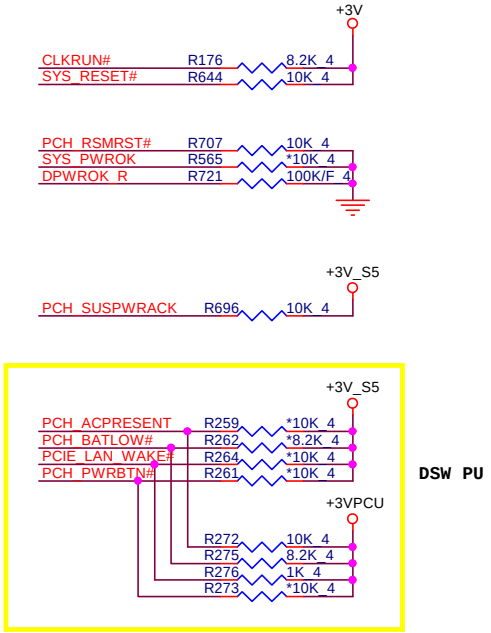
07



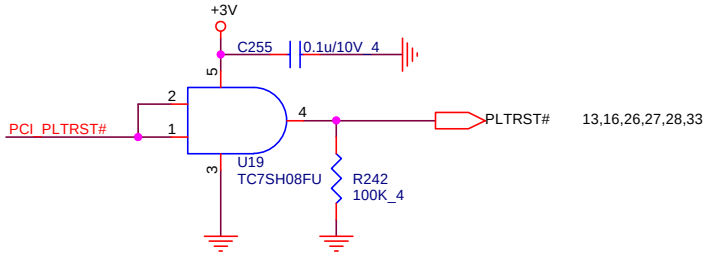
Power Sequence



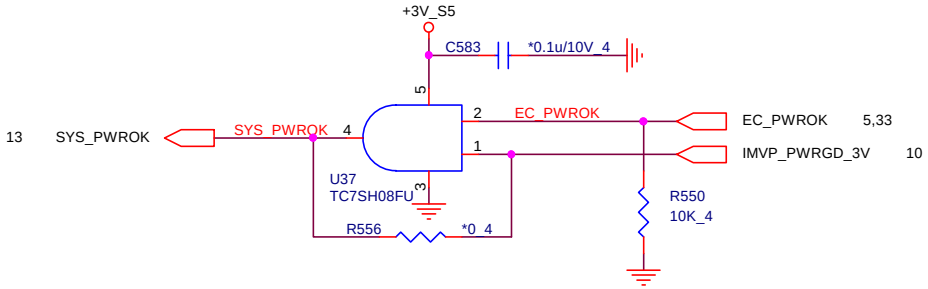
PCH PM PU/PD



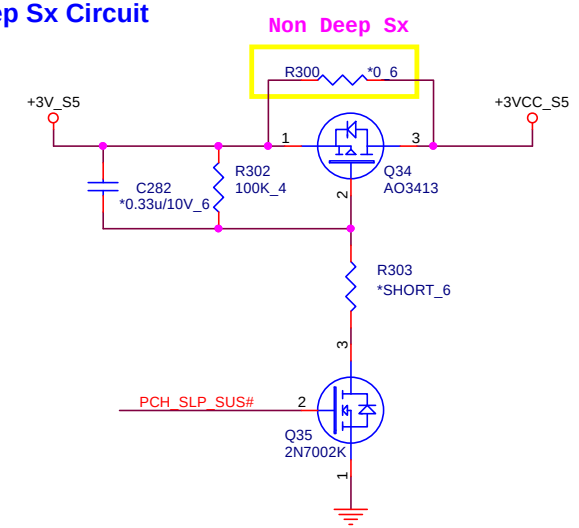
PLTRST# Buffer



SYSPWOK



Deep Sx Circuit



Quanta Computer Inc.		
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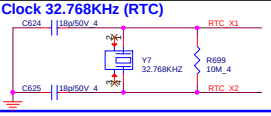
Haswell ULT PCH (RTC/HDA/SATA/SPI)

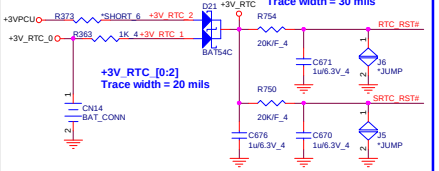
Haswell ULT PCH(LPC,SPI,SMBUS,C-LINK,THERMAL)

08

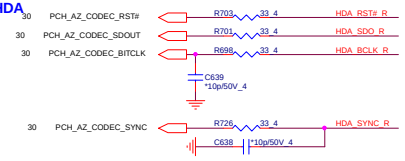
RTC Clock 32.768KHz (RTC)



RTC Circuitry (RTC)



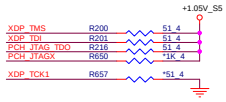
HDA

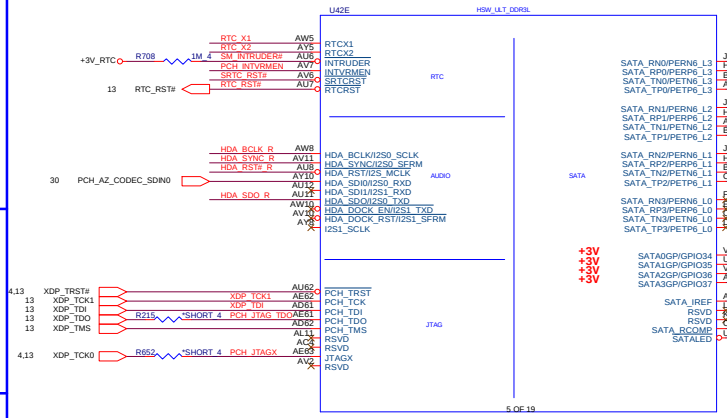


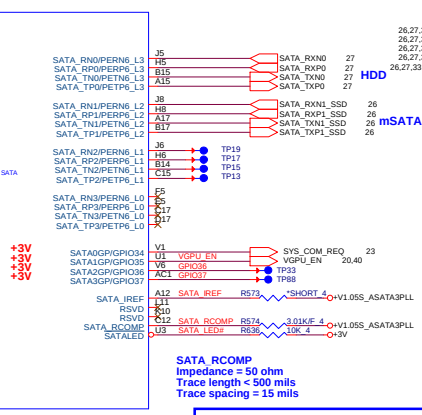
PCH JTAG

JTAG_TCK,JTAG_TMS
Trace Length < 9000mils

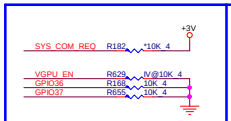
MP remove(Intel)



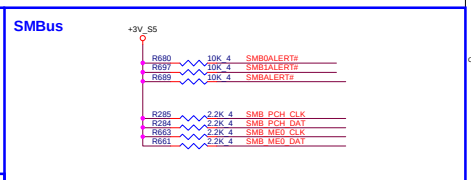




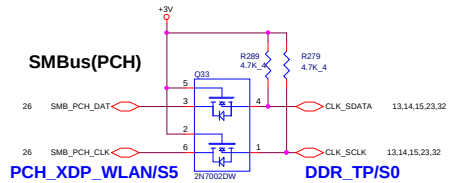
SATA_RCOMP
Impedance = 50 ohm
Trace length < 500 mils
Trace spacing = 15 mils



SMBus

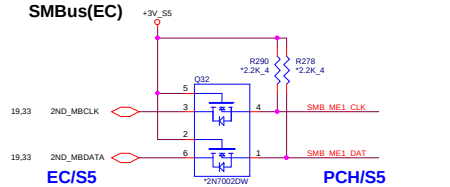


SMBus(PCH)



PCH_XDP_WLAN/S5 DDR_TP/S0

SMBus(EC)

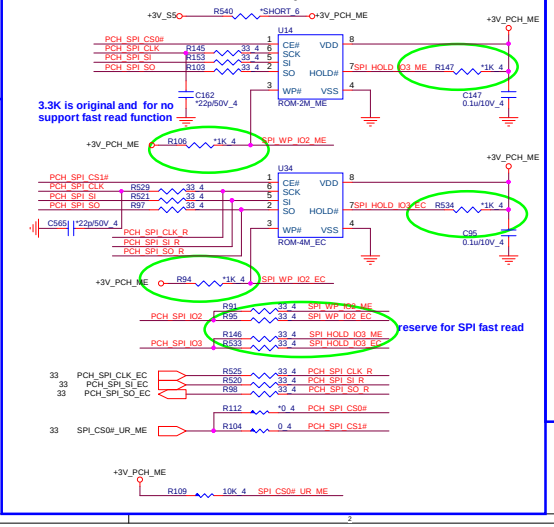


EC/S5 PCH/S5

PCH Quad SPI ROM

(Default for WIN8)

W25Q32BVSSIG / AKE391P0N00------>4MB
MX25L3206EM2I / AKE39FP0Z02----->4MB
MX25L1606EM2I / AKE38FP0Z01----->2MB
W25Q16BVSSIG / AKE38FPON01-----> 2MB



3.3K is original and for no support fast read function

reserve for SPI fast read

ULT Strapping Table

Pin Name	Strap description	Sampled	Configuration	note
GPIO81(SPKR)	No reboot on TCO Timer expiration	PWROK	0 = Default enable (iPD 20K) 1 =Disable No-Reboot mode	+3V R642 *1K_4 SPKR — SPKR 10,30
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	0 = Default can program ME (iPD 20K) 1 =can't program ME	HDA_SDO_R R702 *SHORT_4 ME_WR# 33
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	1=Should be always pull-up	+3V_RTC R717 330K_4 PCH_INTVRMEN R704 *330K_4
GPIO66	Top-Block Swap override		0 = Default disable (iPD 20K) 1 = Enable TBS function	10 GPIO66 +3V R578 *1K_4 GPIO66 R577 *1K_4
GPIO86	Boot BIOS Strap Bit		0 = Default SPI (iPD 20K) 1 =LPC	10 GPIO86 +3V R136 *1K_4 GPIO86 R129 *1K_4
GPIO15	TLS(Transport layer security)		0 = Default enable w/o confidentiality(iPD 20K) 1 =Default enable with confidentiality	10 GPIO15 +3V_S5 R195 8.2K_4 GPIO15 R189 *1K_4
CFG4	DP presence strap		0 = Enable an external display port is connected to the eDP 1 =disable	6,13 CFG4 CFG4 R193 1K_4
DSWVREN	Deep Sx well on die VR enable		1=Should be always pull-up	7 DSWVREN +3V_RTC R718 330K_4 DSWVREN R706 *330K_4

Quanta Computer Inc.
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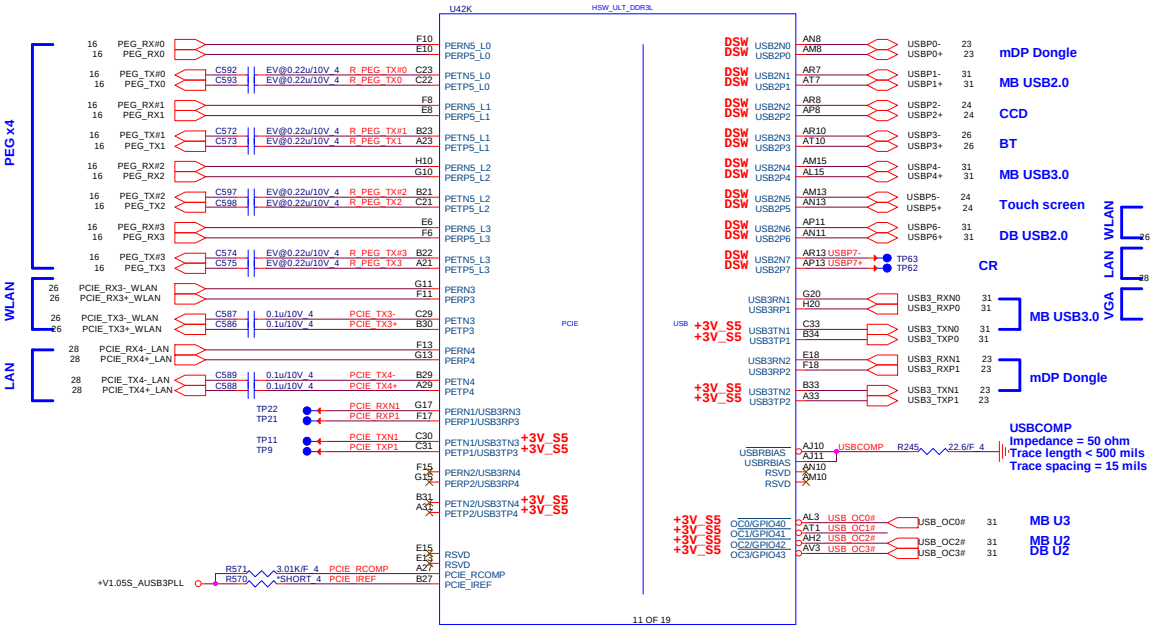
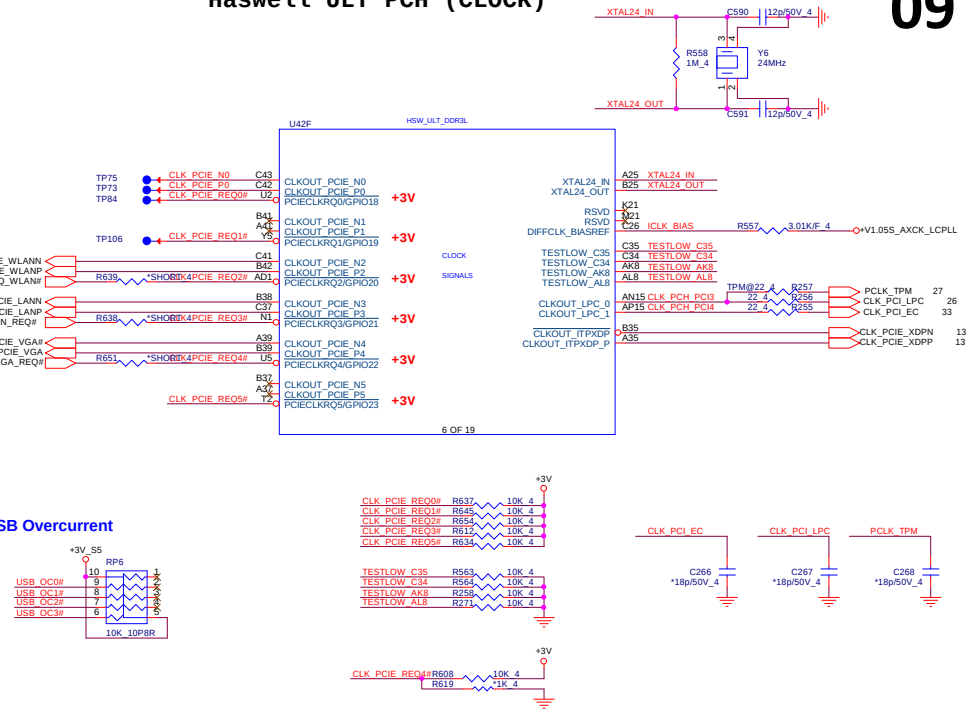
Haswell ULT PCH (PCIE,USB3.0,USB2.0)



Haswell ULT PCH (CLOCK)



09

Quanta Computer Inc.		
PROJECT : ZRQ		
Size	Document Number: LPT 3/6 (PCIE/USB/CLK)	Rev: 3A
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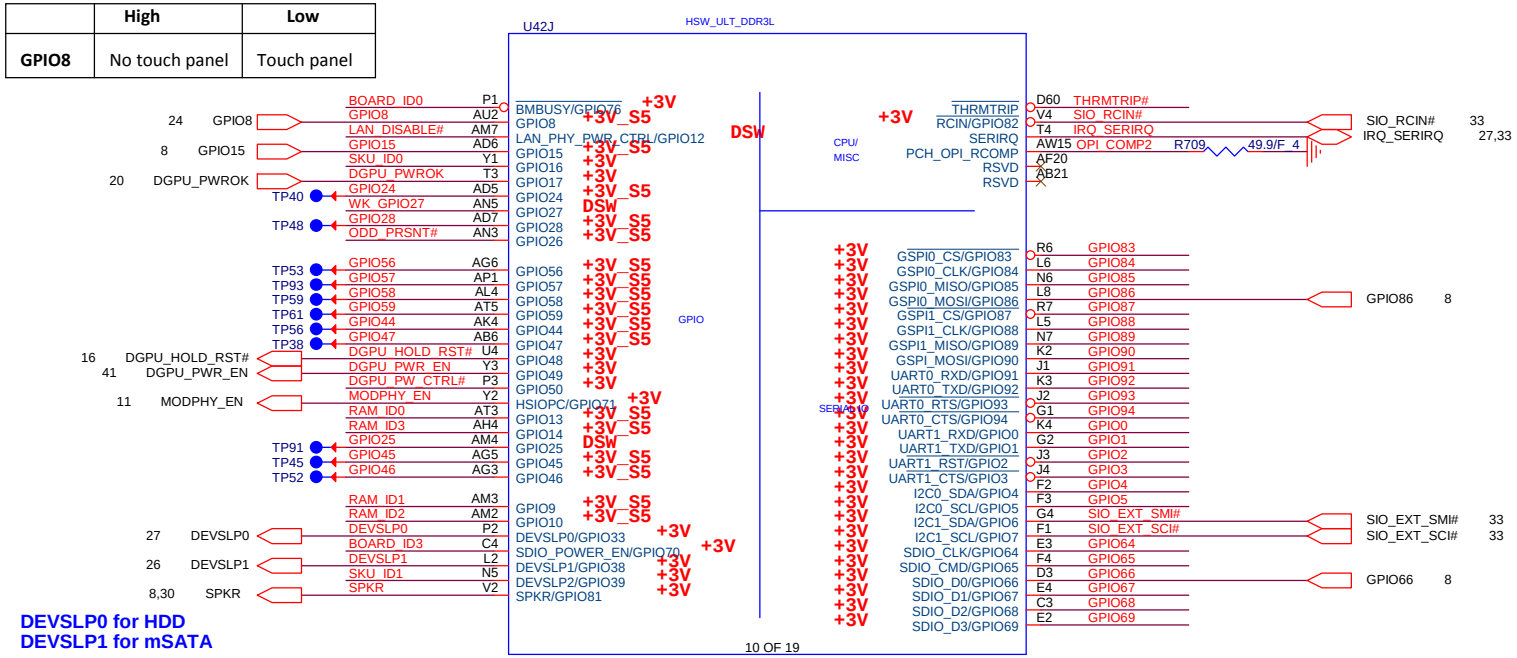
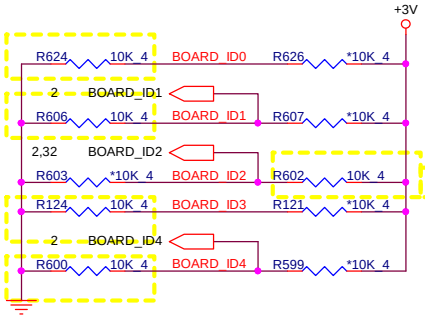
Haswell ULT PCH (GPIO,CPU/MISC,NCTF)

	High	Low
GPIO8	No touch panel	Touch panel

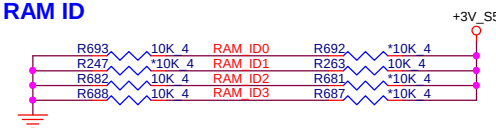


Board ID



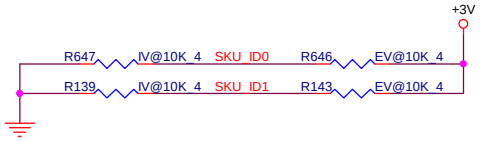
	Low	High
BOARD_ID0	DDR3	GDDR5
BOARD_ID1	Enable on board memory	Disable on board memory
BOARD_ID2	Pin8 of SYNAPTICS and ELAN are NC pin. BIOS maybe will use EEPROM detection. Default is pull high.	
BOARD_ID3	Reserved (Default)	Reserved
BOARD_ID4	Reserved (Default)	Reserved

RAM ID



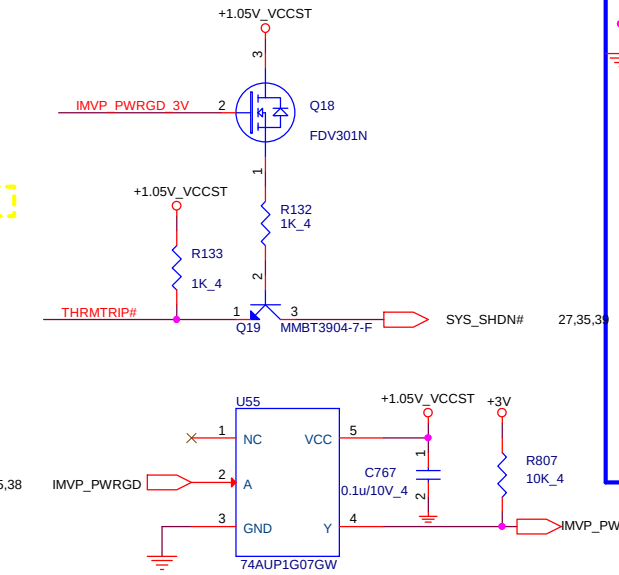
Vender	RAM_ID	Q PN	Mfr. PN	Freq.
Hynix	0000	AKD5JGETW04	H5TC4G63AFR-PRBA	1600MHz
Elpida	0001	AKD5JGST400	EDJ4216EBBG-DJ-F	1333MHz
Elpida	0010	AKD5JGST404	EDJ4216EFBG-GN-F	1600MHz

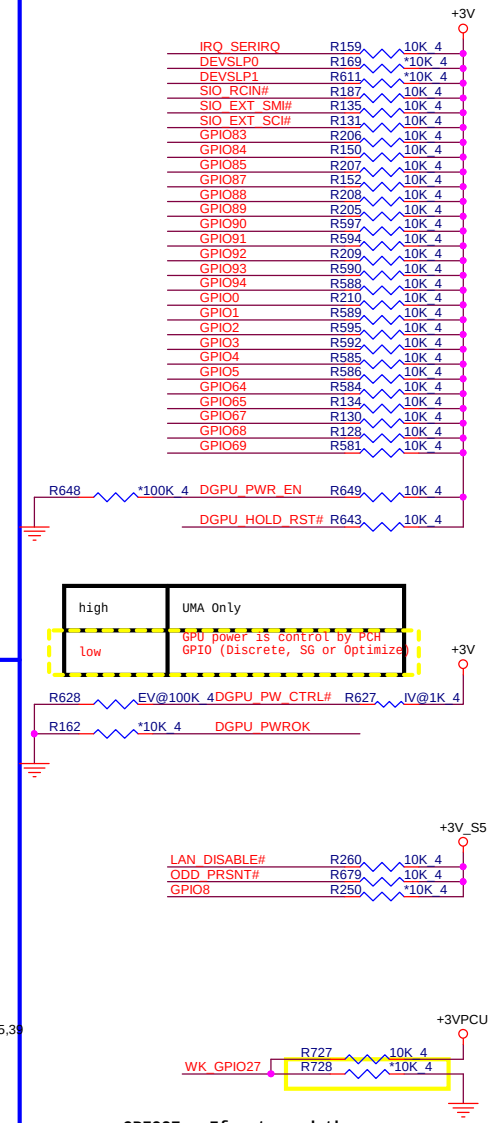
SKU ID



	SKU_ID1	SKU_ID0	VGA H/W Signal	Setup Menu	
UMA Only	0	0	UMA	Hidden	UMA boot
dGPU Only	0	1	GPU	Hidden	GPU boot
Switchable (Mux)	1	0	UMA+GPU	dGPU/SG	UMA boot
Optimize (Muxless)	1	1	UMA	UMA/SG	UMA boot

CPU thermal trip

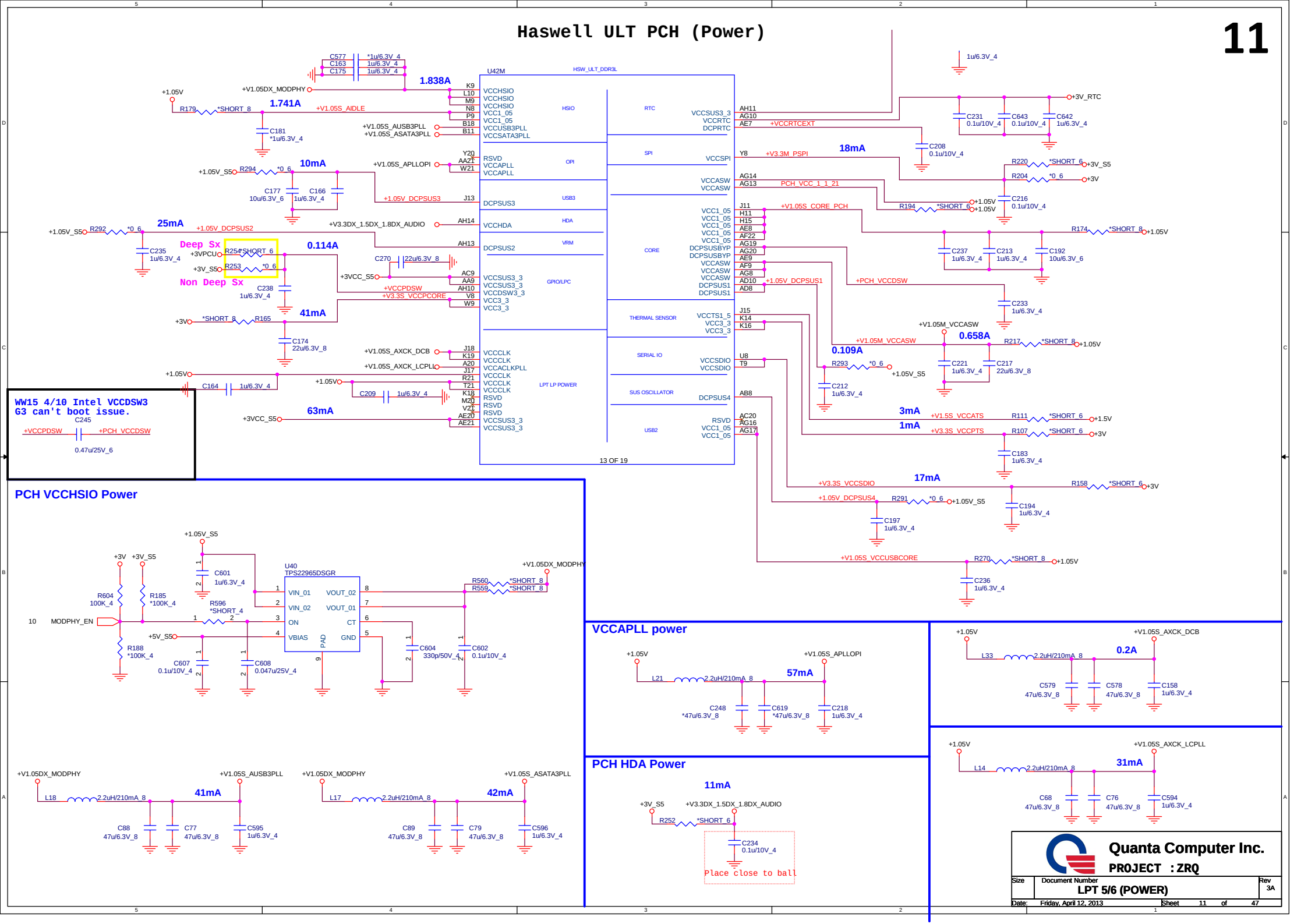




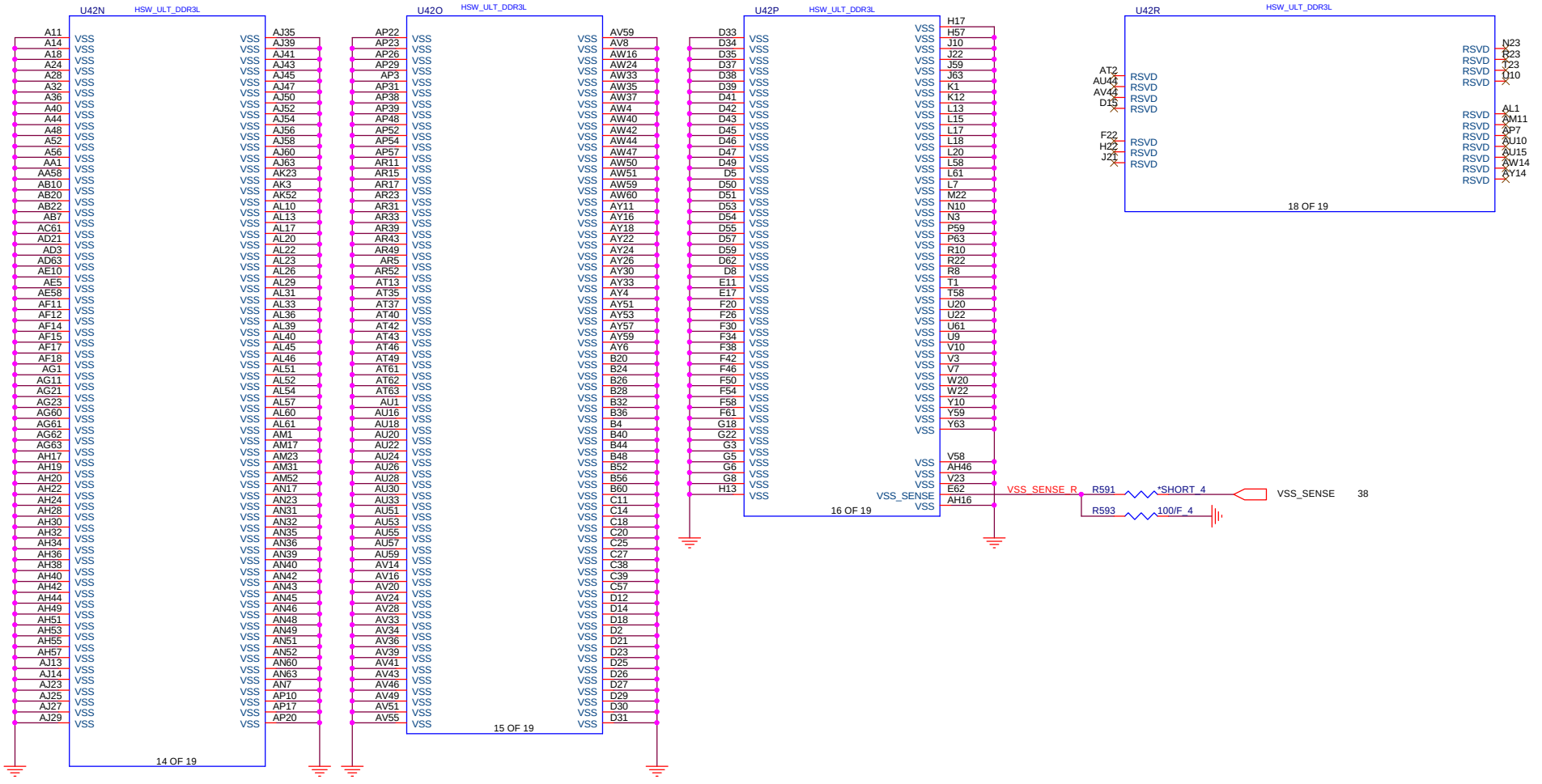
Quanta Computer Inc.
PROJECT : ZRQ

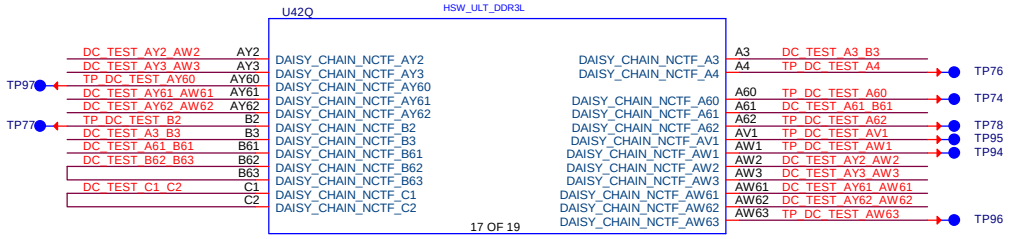
Size	Document Number	Rev
	LPT 4/6 (GPIO/MISC)	3A
Date: Friday, April 12, 2013	Sheet 10 of 47	

Haswell ULT PCH (Power)



Haswell ULT (GND)





Quanta Computer Inc.		
PROJECT : ZRQ		
Size	Document Number: LPT 6/6 (GND)	Rev: 3A
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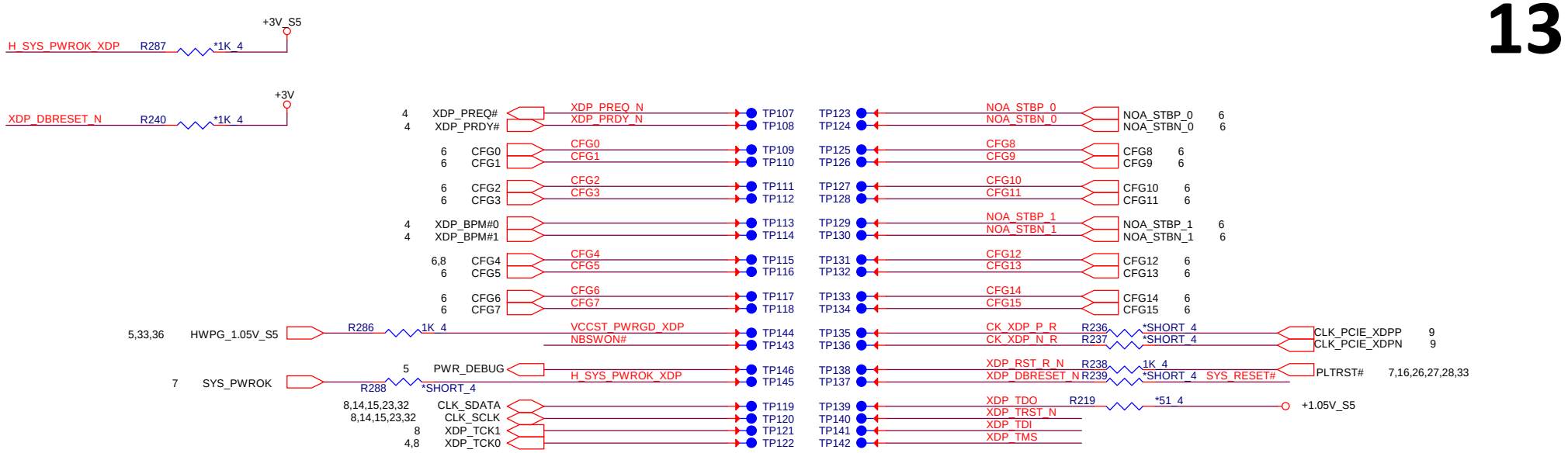
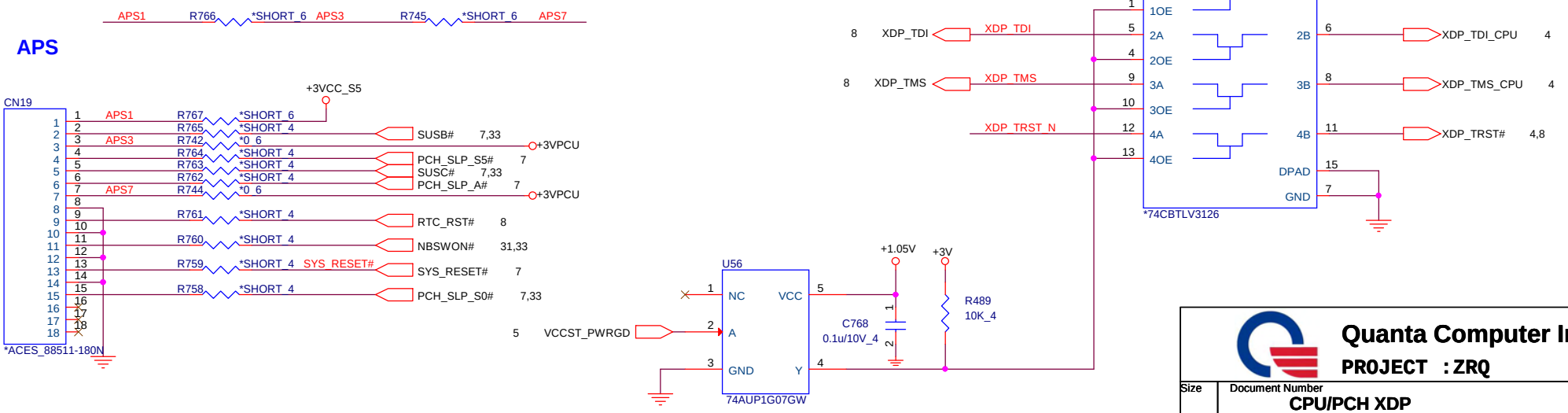


APS



Quanta Computer Inc.
PROJECT : ZRQ

Size	Document Number	Rev
	CPU/PCH XDP	3A
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<DDR>

BYTE1_8-15
BYTE3_24-31
BYTE5_40-47
BYTE6_48-55
BYTE0_0-7
BYTE2_16-23
BYTE4_32-39
BYTE7_56-63

SO-DIMMB SPD Address is 0XA4
SO-DIMMB TS Address is 0X34

Vendor	P/N	
Hynix		
Elpida	AKD5JGST400	DDR3L 1333Mhz 4Gb
	AKD5JGST404	DDR3L 1600Mhz 4Gb

SP : ELPIDA DRAM P/N : AKD5JGST400
HYNIX DRAM P/N : AKD5JGQTW01

Place these Caps near Memory Down

Place these Caps near Memory Down CA & DQ pin

M1 solution
M3 solution
Vref_CA
Vref_DQ

WP =1 : WRITE DISABLE
SPD address:A2

Quanta Computer Inc.
PROJECT : ZRQ
DDR3 MEMORY DOWNx16 A
Rev 3A
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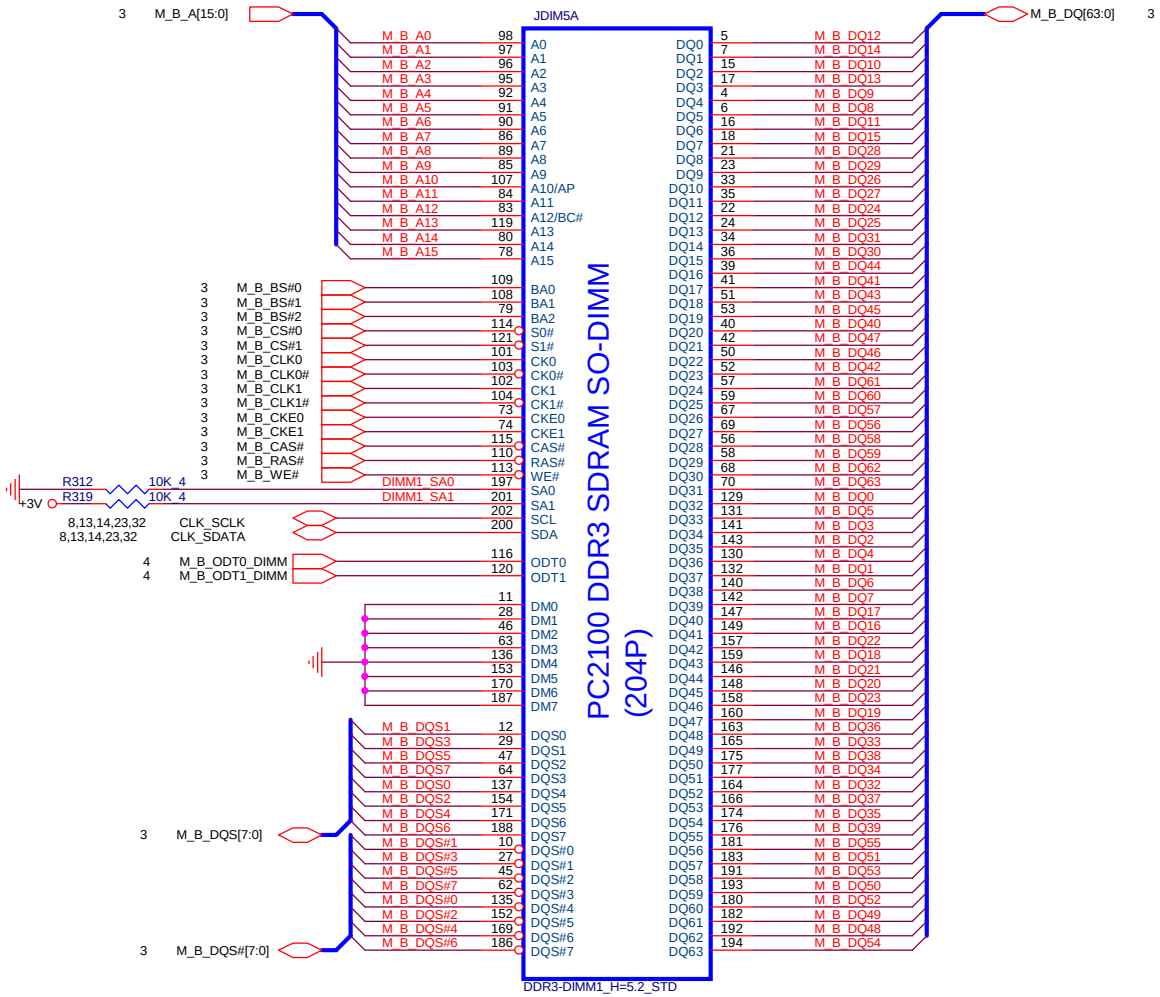
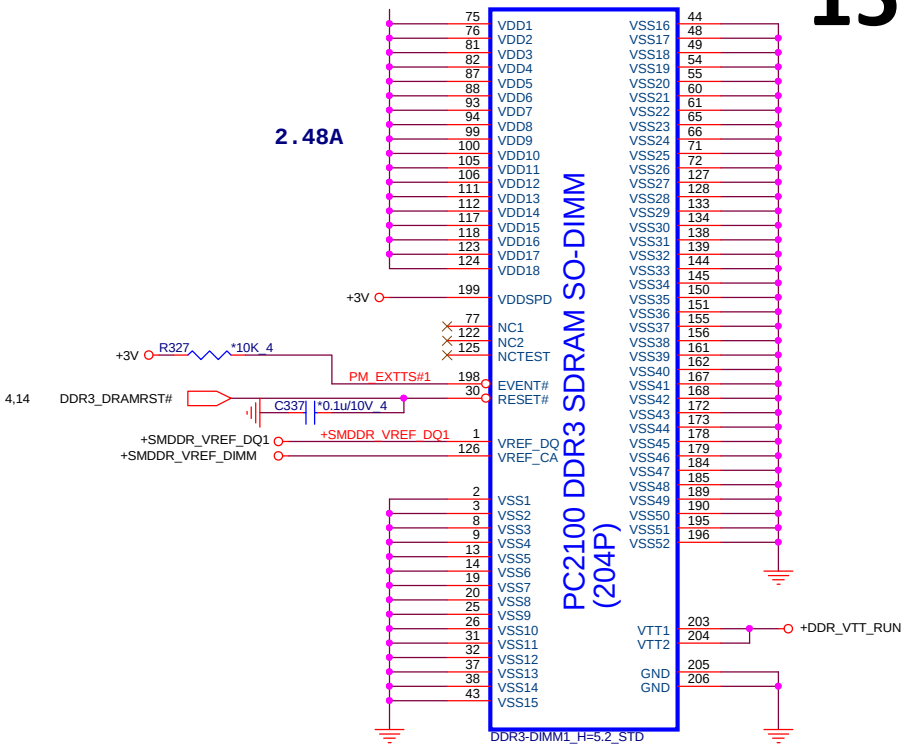
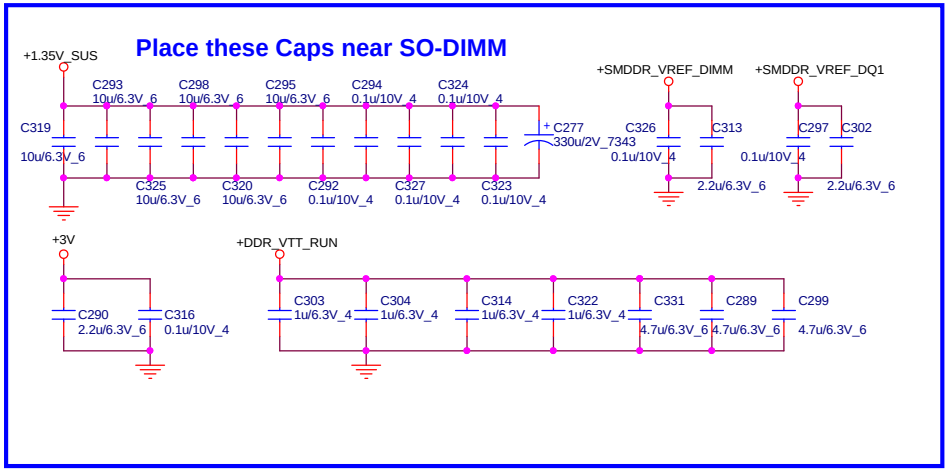
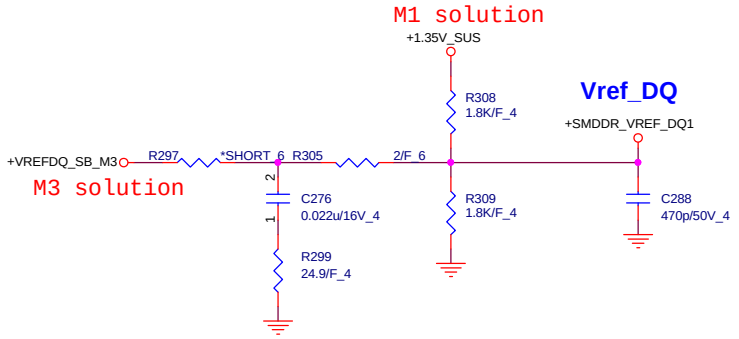








Quanta Computer Inc.		
PROJECT : ZRQ		
Size	Document Number: DDRIII SO-DIMM-1	Rev: 3A
Date: Friday, April 12, 2013	Sheet 15 of 47	

1000mA

+1.05V_GFX

To be placed no further from the GPU than bewteen BGA and Power supply
C564 EV@22u/6.3V_8
C563 EV@22u/6.3V_8
C153 EV@10u/6.3V_6
C109 EV@10u/6.3V_6
place near balls
C118 EV@4.7u/6.3V_6
C143 EV@1u/6.3V_4
place under BGA
C123 EV@1u/6.3V_4

+1.05V_GFX
To be placed no further from the GPU than bewteen BGA and Power supply
C570 EV@22u/6.3V_8
C569 EV@22u/6.3V_8
C98 EV@10u/6.3V_6
C70 EV@10u/6.3V_6
place near balls
C133 EV@4.7u/6.3V_6
C80 EV@1u/6.3V_4
place under BGA
C78 EV@1u/6.3V_4

2500mA

U39A

[PEG Interface]

AG19 PEX_IOVDD_1
AG21 PEX_IOVDD_2
AG22 PEX_IOVDD_3
AG24 PEX_IOVDD_4
AH21 PEX_IOVDD_5
AH25 PEX_IOVDD_6

AG13 PEX_IOVDDQ_1
AG15 PEX_IOVDDQ_2
AG16 PEX_IOVDDQ_3
AG18 PEX_IOVDDQ_4
AG25 PEX_IOVDDQ_5
AH15 PEX_IOVDDQ_6
AH18 PEX_IOVDDQ_7
AH26 PEX_IOVDDQ_8
AH27 PEX_IOVDDQ_9
AJ27 PEX_IOVDDQ_10
AK27 PEX_IOVDDQ_11
AL27 PEX_IOVDDQ_12
AM28 PEX_IOVDDQ_13
AN28 PEX_IOVDDQ_14

PEX_RX0 AN12 PEG_TX0 — PEG_TX0 9
PEX_RX0_N AM12 PEG_TX#0 — PEG_TX#0 9
PEX_RX1 AN14 PEG_TX1 — PEG_TX1 9
PEX_RX1_N AM14 PEG_TX#1 — PEG_TX#1 9
PEX_RX2 AP14 PEG_TX2 — PEG_TX2 9
PEX_RX2_N AP15 PEG_TX#2 — PEG_TX#2 9
PEX_RX3 AN15 PEG_TX3 — PEG_TX3 9
PEX_RX3_N AM15 PEG_TX#3 — PEG_TX#3 9
PEX_RX4 AN17
PEX_RX4_N AM17
PEX_RX5 AP17
PEX_RX5_N AP18
PEX_RX6 AN18
PEX_RX6_N AM18
PEX_RX7 AN20
PEX_RX7_N AM20
PEX_RX8 AP20
PEX_RX8_N AP21
PEX_RX9 AN21
PEX_RX9_N AM21
PEX_RX10 AN23
PEX_RX10_N AM23
PEX_RX11 AP23
PEX_RX11_N AP24
PEX_RX12 AN24
PEX_RX12_N AM24
PEX_RX13 AN26
PEX_RX13_N AM26
PEX_RX14 AP26
PEX_RX14_N AP27
PEX_RX15 AN27
PEX_RX15_N AM27

PEX_TX0 AK14 R_PEG_RX0 C142 EV@0.22u/10V_4 — PEG_RX0 9
PEX_TX0_N AJ14 R_PEG_RX#0 C135 EV@0.22u/10V_4 — PEG_RX#0 9
PEX_TX1 AH14 R_PEG_RX1 C131 EV@0.22u/10V_4 — PEG_RX1 9
PEX_TX1_N AG14 R_PEG_RX#1 C121 EV@0.22u/10V_4 — PEG_RX#1 9
PEX_TX2 AK15 R_PEG_RX2 C112 EV@0.22u/10V_4 — PEG_RX2 9
PEX_TX2_N AJ15 R_PEG_RX#2 C104 EV@0.22u/10V_4 — PEG_RX#2 9
PEX_TX3 AL16 R_PEG_RX3 C120 EV@0.22u/10V_4 — PEG_RX3 9
PEX_TX3_N AK16 R_PEG_RX#3 C115 EV@0.22u/10V_4 — PEG_RX#3 9
PEX_TX4 AK17
PEX_TX4_N AJ17
PEX_TX5 AH17
PEX_TX5_N AG17
PEX_TX6 AK18
PEX_TX6_N AJ18
PEX_TX7 AL19
PEX_TX7_N AK19
PEX_TX8 AK20
PEX_TX8_N AJ20
PEX_TX9 AH20
PEX_TX9_N AG20
PEX_TX10 AK21
PEX_TX10_N AJ21
PEX_TX11 AL22
PEX_TX11_N AK22
PEX_TX12 AK23
PEX_TX12_N AJ23
PEX_TX13 AH23
PEX_TX13_N AG23
PEX_TX14 AK24
PEX_TX14_N AJ24
PEX_TX15 AL25
PEX_TX15_N AK25

AC6 NC_1
AJ28 NC_2
AJ4 NC_3
AJ5 NC_4
AL11 NC_5
C15 NC_6
D19 NC_7
D20 NC_8
D23 NC_9
D26 NC_10
H31 NC_11
T8 NC_12
V32 NC_13

PEX_REFCLK AL13 — CLK_PCIE_VGA 9
PEX_REFCLK_N AK13 — CLK_PCIE_VGA# 9

PEX_TSTCLK_OUT AJ26 PEX_TSTCLK R114 *EV@200/F_4
PEX_TSTCLK_OUT_N AK26 PEX_TSTCLK#

0815 change R53 to 1% tolerance

PEX_WAKE AJ11
PEX_RST_N AJ12 PEGX_RST#

PEX_CLKREQ_N AK12 PEX_CLKREQ#

PEX_TERMP AP29 PEX_TERMP R523 EV@2.49K/F_4
TESTMODE R157 EV@10K/F_4
TESTMODE AK11

PEX_PLLVDD AG26
PEX_PLL_HVDD AH12
PEX_SVDD_3V3 AG12
3.3V_AUX_NC P8
VDD_SENSE L4
GND_SENSE L5

EV@N14P

N14P

J8/K8 0.4MM = 16mils

+3V_GFX

J8 VDD33_1
K8 VDD33_2
L8 VDD33_3
M8 VDD33_4

L8/M8 0.4MM = 16mils

PLACE CLOSE TO BGA L8/M8
+3V_GFX
C244 EV@4.7u/6.3V_6
C243 EV@1u/6.3V_4
C240 EV@0.1u/10V_4
C242 EV@0.1u/10V_4
C241 EV@0.1u/10V_4
PLACE CLOSE TO GPU BALLS L8/M8

RSVD R1 and C1 for GV2 co-layout sDDR3

PEX_PLLVDD : 0.3MM = 12mils (150mA)

R1
PEX_PLLVDD R110 EV@0_6 +1.05V_GFX
C96 EV@4.7u/6.3V_6
C87 EV@1u/6.3V_4
C84 EV@0.1u/10V_4
place near BGA
place near ball
C1
C72 *EV@GV2@1u/6.3V_4

C182 EV@0.1u/10V_4 +3V_GFX
C185 EV@4.7u/6.3V_6
C184 EV@4.7u/6.3V_6
PLACE NEAR BGA

AH12/AG12 need 210mA of +3V_GFX

GPU_VCCP_SENSE 40
GPU_VSSP_SENSE 40
8mils width
(0.2MM)

+3V_GFX +3V_GFX

R148 EV@10K/F_4

Follow Z09 to isolate CLK_REQ#

PEX_CLKREQ# 1 Q23 EV@2N7002K 3 CLK_PEGA_REQ# 9
PU at page 9

R154 *EV@0_4

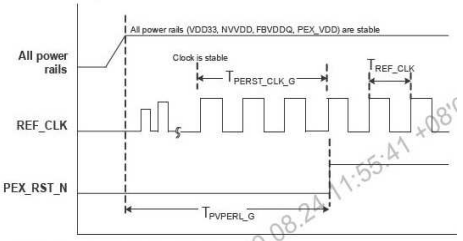


Figure 3-18. PEX_RST_N Timing for GPU

Table 3-8. N11x Reset Requirements for PCI Express 2.0

Constraint Parameter	Requirement	Notes
T_{PVPERL_G}	$T_{PVPERL\_G} \geq 1us$	
$T_{PERST\_CLK\_G}$	$T_{PERST\_CLK\_G} \geq 1T_{REF\_CLK}$	

NVIDIA Confidential Mon 0.08.24 11:55:41 +08

+3V

C622 EV@0.1u/10V_4

7,13,26,27,28,33 PLTRST#
10 DGPU_HOLD_RST#

U45 EV@TC7SH08FU

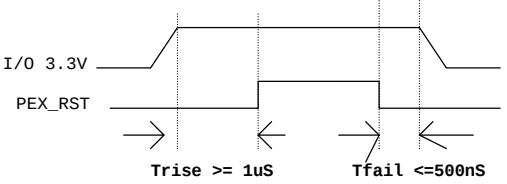
PEGX_RST# — PEGX_RST# 19

R694 EV@100K_4

R710 *EV@0_4

PCH control PEGX_RST#

PEX_RST timing



Quanta Computer Inc.
PROJECT : ZRQ

Size	Document Number	Rev
	DGPU 1/5 (PEG)	3A

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U39B

21 FBA_CMD[30:0]

FBA_CMD0	U30	FBA_CMD0 (FBA_CMD25)	[MEMORY I/F A]
FBA_CMD1	T31	FBA_CMD1 (FBA_CMD23)	
FBA_CMD2	U29	FBA_CMD2	
FBA_CMD3	R34	FBA_CMD3 (FBA_CMD0)	
FBA_CMD4	R33	FBA_CMD4 (FBA_CMD10)	
FBA_CMD5	U32	FBA_CMD5 (FBA_CMD26)	
FBA_CMD6	U33	FBA_CMD6 (FBA_CMD14)	
FBA_CMD7	U28	FBA_CMD7	
FBA_CMD8	V28	FBA_CMD8 (FBA_CMD1)	
FBA_CMD9	V29	FBA_CMD9 (FBA_CMD22)	
FBA_CMD10	V30	FBA_CMD10 (FBA_CMD20)	
FBA_CMD11	U34	FBA_CMD11 (FBA_CMD24)	
FBA_CMD12	U31	FBA_CMD12 (FBA_CMD18)	
FBA_CMD13	V34	FBA_CMD13 (FBA_CMD9)	
FBA_CMD14	V33	FBA_CMD14 (FBA_CMD29)	
FBA_CMD15	Y32	FBA_CMD15 (FBA_CMD8)	
FBA_CMD16	AA31	FBA_CMD16 (FBA_CMD27)	
FBA_CMD17	AA29	FBA_CMD17 (FBA_CMD15)	
FBA_CMD18	AA28	FBA_CMD18 (FBA_CMD11)	
FBA_CMD19	AC34	FBA_CMD19 (FBA_CMD16)	
FBA_CMD20	AC33	FBA_CMD20 (FBA_CMD28)	
FBA_CMD21	AA32	FBA_CMD21 (FBA_CMD3)	
FBA_CMD22	AA33	FBA_CMD22 (FBA_CMD17)	
FBA_CMD23	Y28	FBA_CMD23 (FBA_CMD5)	
FBA_CMD24	Y29	FBA_CMD24 (FBA_CMD4)	
FBA_CMD25	W31	FBA_CMD25 (FBA_CMD21)	
FBA_CMD26	Y30	FBA_CMD26 (FBA_CMD6)	
FBA_CMD27	AA34	FBA_CMD27 (FBA_CMD13)	
FBA_CMD28	Y31	FBA_CMD28 (FBA_CMD19)	
FBA_CMD29	Y34	FBA_CMD29 (FBA_CMD12)	
FBA_CMD30	Y33	FBA_CMD30	
TP10	V31	FBA_CMD31 (NC)	

21 VMA_DM[7..0]

DBI

VMA_DM0	P30	FBA_DQM0
VMA_DM1	F31	FBA_DQM1
VMA_DM2	F34	FBA_DQM2
VMA_DM3	M32	FBA_DQM3
VMA_DM4	AD31	FBA_DQM4
VMA_DM5	AL29	FBA_DQM5
VMA_DM6	AM32	FBA_DQM6
VMA_DM7	AF34	FBA_DQM7

21 VMA_WDQS[7..0]

EDC

VMA_WDQS0	M31	FBA_DQS_WP0
VMA_WDQS1	G31	FBA_DQS_WP1
VMA_WDQS2	E33	FBA_DQS_WP2
VMA_WDQS3	M33	FBA_DQS_WP3
VMA_WDQS4	AE31	FBA_DQS_WP4
VMA_WDQS5	AK30	FBA_DQS_WP5
VMA_WDQS6	AN33	FBA_DQS_WP6
VMA_WDQS7	AF33	FBA_DQS_WP7

21 VMA_RDQS[7..0]

VMA_RDQS0	M30	FBA_DQS_RN0
VMA_RDQS1	H30	FBA_DQS_RN1
VMA_RDQS2	E34	FBA_DQS_RN2
VMA_RDQS3	M34	FBA_DQS_RN3
VMA_RDQS4	AF30	FBA_DQS_RN4
VMA_RDQS5	AK31	FBA_DQS_RN5
VMA_RDQS6	AM34	FBA_DQS_RN6
VMA_RDQS7	AF32	FBA_DQS_RN7

+1.5V_GFX

AA27	FBVDDQ_1
AA30	FBVDDQ_2
AB27	FBVDDQ_3
AB33	FBVDDQ_4
AC27	FBVDDQ_5
AD27	FBVDDQ_6
AE27	FBVDDQ_7
AF27	FBVDDQ_8
AG27	FBVDDQ_9
B13	FBVDDQ_10
B16	FBVDDQ_11
B19	FBVDDQ_12
E13	FBVDDQ_13
E16	FBVDDQ_14
E19	FBVDDQ_15
H10	FBVDDQ_16
H11	FBVDDQ_17
H12	FBVDDQ_18
H13	FBVDDQ_19
H14	FBVDDQ_20
H15	FBVDDQ_21
H16	FBVDDQ_22
H18	FBVDDQ_23
H19	FBVDDQ_24
H20	FBVDDQ_25
H21	FBVDDQ_26
H22	FBVDDQ_27
H23	FBVDDQ_28
H24	FBVDDQ_29
H8	FBVDDQ_30
H9	FBVDDQ_31
L27	FBVDDQ_32
M27	FBVDDQ_33
N27	FBVDDQ_34
P27	FBVDDQ_35
R27	FBVDDQ_36
T27	FBVDDQ_37
T30	FBVDDQ_38
T33	FBVDDQ_39
V27	FBVDDQ_40
W27	FBVDDQ_41
W30	FBVDDQ_42
W33	FBVDDQ_43
Y27	FBVDDQ_44

Follow DG to place caps

+1.5V_GFX

PLACE CLOSE TO GPU BALLS

0.1u x 6 stuff x4

C132	EV@0.1u/10V_4
C83	EV@0.1u/10V_4
C161	EV@0.1u/10V_4
C148	EV@0.1u/10V_4
C108	*EV@0.1u/10V_4
C99	*EV@0.1u/10V_4

1u x 6 stuff x4

C155	EV@1u/6.3V_4
C110	EV@1u/6.3V_4
C63	EV@1u/6.3V_4
C86	EV@1u/6.3V_4
C141	*EV@1u/6.3V_4
C145	*EV@1u/6.3V_4

4.7u x 6 stuff x4

C107	EV@4.7u/6.3V_6
C55	EV@4.7u/6.3V_6
C130	EV@4.7u/6.3V_6
C62	EV@4.7u/6.3V_6
C57	*EV@4.7u/6.3V_6
C85	*EV@4.7u/6.3V_6

10u x 4 stuff x2

C53	EV@10u/6.3V_6
C49	EV@10u/6.3V_6
C52	*EV@10u/6.3V_6
C56	*EV@10u/6.3V_6

22u x 4 stuff x2

C100	EV@22u/6.3V_8
C47	EV@22u/6.3V_8
C90	*EV@22u/6.3V_8
C50	*EV@22u/6.3V_8

PLACE CLOSE TO BGA

EV@N14P

FBA_CLK0	R30	VMA_CLK0	VMA_CLK0 21
FBA_CLK0_N	R31	VMA_CLK0#	VMA_CLK0# 21
FBA_CLK1	AB31	VMA_CLK1	VMA_CLK1 21
FBA_CLK1_N	AC31	VMA_CLK1#	VMA_CLK1# 21

15mils width

(FBA_DEBUG) FBA_DEBUG0 — R28 FBA_DEBUG — R81 *EV@60.4/F_4 — +1.5V_GFX
(NC) FBA_DEBUG1 — AC28 FBA_DEBUG1 — R101 *EV@60.4/F_4
FB_VREF_NC — H26 — TP12

No stuff follow CRB

FBA_CMD_RFU0	R32	
FBA_CMD_RFU1	AC32	
FBA_WCK01	K31	
FBA_WCK01_N	L30	
FBA_WCK23	H34	
FBA_WCK23_N	J34	
FBA_WCK45	AG30	
FBA_WCK45_N	AG31	
FBA_WCK67	AJ34	
FBA_WCK67_N	AK34	
FBA_WCKB01	J30	
FBA_WCKB01_N	J31	
FBA_WCKB23	J32	
FBA_WCKB23_N	J33	
FBA_WCKB45	AH31	
FBA_WCKB45_N	AJ31	
FBA_WCKB67	AJ32	
FBA_WCKB67_N	AJ33	

GC6 connect to EC

R678 *EV@SHORT_4 — EC_FB_CLAMP 19,20,33
R677 EV@10K_4

RSVD	E1	FB_CLAMP
FB_DLL_AVDD	K27	+FB_PLLAVDD — C81 EV@0.1u/10V_4
FBA_PLL_AVDD	U27	+FB_PLLAVDD — L15 EV@PBY160808T-30Y-N/2A/300ohm_6 — +1.05V_GFX
FBVDDQ_PROBE	F1	FBVDDQ_SENSE_NC — TP92 — C82 EV@0.1u/10V_4 — C58 EV@22u/6.3V_8
GND_PROBE	F2	FB_GND_SENSE_NC — TP90 — C69 *EV@0.1u/10V_4
FB_CAL_PD_VDDQ	J27	FB_CAL_PD_VDDQ — R102 EV@40.2/F_4 — +1.5V_GFX
FB_CAL_PU_GND	H27	FB_CAL_PU_GND — R100 EV@42.2/F_4
FB_CALTERM_GND	H25	FB_CAL_TERM_GND — R115 EV@51.1/F_4

C70 close ball K27 35mA

C66/C67 close to ball U27
C45 close to BGA

+FB_PLLAVDD = 0.3mm 12mils
U27+H17 62mA

PLACE CLOSE TO GPU BALLS

GDDR5
R118 change to 40.2/F
R141 change to 60.4/F
sDDR3
R118=42.2/F
R141=51.1/F

+1.5V_GFX — C39 *EV@330u/2V_7343 — C546 EV@330u/2V_7343

RSVD 330u, ZQS have one

U39C

22 FBC_CMD[30:0]

FBC_CMD0	D13	FBB_CMD0 (FBC_CMD25)
FBC_CMD1	E14	FBB_CMD1 (FBC_CMD23)
FBC_CMD2	F14	FBB_CMD2
FBC_CMD3	A12	FBB_CMD3 (FBC_CMD0)
FBC_CMD4	B12	FBB_CMD4 (FBC_CMD10)
FBC_CMD5	C14	FBB_CMD5 (FBC_CMD26)
FBC_CMD6	B14	FBB_CMD6 (FBC_CMD14)
FBC_CMD7	G15	FBB_CMD7
FBC_CMD8	F15	FBB_CMD8 (FBC_CMD1)
FBC_CMD9	E15	FBB_CMD9 (FBC_CMD22)
FBC_CMD10	D15	FBB_CMD10 (FBC_CMD20)
FBC_CMD11	A14	FBB_CMD11 (FBC_CMD24)
FBC_CMD12	D14	FBB_CMD12 (FBC_CMD18)
FBC_CMD13	A15	FBB_CMD13 (FBC_CMD9)
FBC_CMD14	B15	FBB_CMD14 (FBC_CMD29)
FBC_CMD15	C17	FBB_CMD15 (FBC_CMD8)
FBC_CMD16	D18	FBB_CMD16 (FBC_CMD27)
FBC_CMD17	E18	FBB_CMD17 (FBC_CMD15)
FBC_CMD18	F18	FBB_CMD18 (FBC_CMD11)
FBC_CMD19	A20	FBB_CMD19 (FBC_CMD16)
FBC_CMD20	B20	FBB_CMD20 (FBC_CMD28)
FBC_CMD21	C18	FBB_CMD21 (FBC_CMD3)
FBC_CMD22	B18	FBB_CMD22 (FBC_CMD17)
FBC_CMD23	G18	FBB_CMD23 (FBC_CMD5)
FBC_CMD24	G17	FBB_CMD24(FBC_CMD4)
FBC_CMD25	F17	FBB_CMD25 (FBC_CMD21)
FBC_CMD26	D16	FBB_CMD26 (FBC_CMD6)
FBC_CMD27	A18	FBB_CMD27 (FBC_CMD13)
FBC_CMD28	D17	FBB_CMD28 (FBC_CMD19)
FBC_CMD29	A17	FBB_CMD29 (FBC_CMD12)
FBC_CMD30	B17	FBB_CMD30
TP16	E17	FBB_CMD31 (NC)

MEMORY I/F C

22 VMC_DM[7..0]

DBI

VMC_DM0	E11	FBC_DQM0
VMC_DM1	E3	FBC_DQM1
VMC_DM2	A3	FBC_DQM2
VMC_DM3	C9	FBC_DQM3
VMC_DM4	F23	FBC_DQM4
VMC_DM5	F27	FBC_DQM5
VMC_DM6	C30	FBC_DQM6
VMC_DM7	A24	FBC_DQM7

22 VMC_WDQS[7..0]

EDC

VMC_WDQS0	D10	FBC_DQS_WP0
VMC_WDQS1	D5	FBC_DQS_WP1
VMC_WDQS2	C3	FBC_DQS_WP2
VMC_WDQS3	B9	FBC_DQS_WP3
VMC_WDQS4	E23	FBC_DQS_WP4
VMC_WDQS5	E28	FBC_DQS_WP5
VMC_WDQS6	B30	FBC_DQS_WP6
VMC_WDQS7	A23	FBC_DQS_WP7

22 VMC_RDQS[7..0]

VMC_RDQS0	D9	FBC_DQS_RN0
VMC_RDQS1	E4	FBC_DQS_RN1
VMC_RDQS2	B2	FBC_DQS_RN2
VMC_RDQS3	A9	FBC_DQS_RN3
VMC_RDQS4	D22	FBC_DQS_RN4
VMC_RDQS5	D28	FBC_DQS_RN5
VMC_RDQS6	A30	FBC_DQS_RN6
VMC_RDQS7	B23	FBC_DQS_RN7

EV@N14P

FBC_DQ0	G9	VMC_DQ0
FBC_DQ1	E9	VMC_DQ1
FBC_DQ2	G8	VMC_DQ2
FBC_DQ3	F9	VMC_DQ3
FBC_DQ4	F11	VMC_DQ4
FBC_DQ5	G11	VMC_DQ5
FBC_DQ6	F12	VMC_DQ6
FBC_DQ7	G12	VMC_DQ7
FBC_DQ8	G6	VMC_DQ8
FBC_DQ9	F5	VMC_DQ9
FBC_DQ10	E6	VMC_DQ10
FBC_DQ11	F6	VMC_DQ11
FBC_DQ12	F4	VMC_DQ12
FBC_DQ13	G4	VMC_DQ13
FBC_DQ14	E2	VMC_DQ14
FBC_DQ15	F3	VMC_DQ15
FBC_DQ16	C2	VMC_DQ16
FBC_DQ17	D4	VMC_DQ17
FBC_DQ18	D3	VMC_DQ18
FBC_DQ19	C1	VMC_DQ19
FBC_DQ20	B3	VMC_DQ20
FBC_DQ21	C4	VMC_DQ21
FBC_DQ22	B5	VMC_DQ22
FBC_DQ23	C5	VMC_DQ23
FBC_DQ24	A11	VMC_DQ24
FBC_DQ25	C11	VMC_DQ25
FBC_DQ26	D11	VMC_DQ26
FBC_DQ27	B11	VMC_DQ27
FBC_DQ28	D8	VMC_DQ28
FBC_DQ29	A8	VMC_DQ29
FBC_DQ30	C8	VMC_DQ30
FBC_DQ31	B8	VMC_DQ31
FBC_DQ32	F24	VMC_DQ32
FBC_DQ33	G23	VMC_DQ33
FBC_DQ34	E24	VMC_DQ34
FBC_DQ35	G24	VMC_DQ35
FBC_DQ36	D21	VMC_DQ36
FBC_DQ37	E21	VMC_DQ37
FBC_DQ38	G21	VMC_DQ38
FBC_DQ39	F21	VMC_DQ39
FBC_DQ40	G27	VMC_DQ40
FBC_DQ41	A27	VMC_DQ41
FBC_DQ42	G26	VMC_DQ42
FBC_DQ43	E27	VMC_DQ43
FBC_DQ44	E29	VMC_DQ44
FBC_DQ45	F29	VMC_DQ45
FBC_DQ46	E30	VMC_DQ46
FBC_DQ47	D30	VMC_DQ47
FBC_DQ48	A32	VMC_DQ48
FBC_DQ49	C31	VMC_DQ49
FBC_DQ50	C32	VMC_DQ50
FBC_DQ51	B32	VMC_DQ51
FBC_DQ52	D29	VMC_DQ52
FBC_DQ53	A29	VMC_DQ53
FBC_DQ54	C29	VMC_DQ54
FBC_DQ55	B29	VMC_DQ55
FBC_DQ56	B21	VMC_DQ56
FBC_DQ57	C23	VMC_DQ57
FBC_DQ58	A21	VMC_DQ58
FBC_DQ59	C21	VMC_DQ59
FBC_DQ60	B24	VMC_DQ60
FBC_DQ61	C24	VMC_DQ61
FBC_DQ62	B26	VMC_DQ62
FBC_DQ63	C26	VMC_DQ63

VMA_DQ[63:0] — VMA_DQ[63:0] 21
VMC_DQ[63:0] — VMC_DQ[63:0] 22

FBC_CLK0	D12	VMC_CLK0 — VMC_CLK0 22
FBC_CLK0_N	E12	VMC_CLK0# — VMC_CLK0# 22
FBC_CLK1	E20	VMC_CLK1 — VMC_CLK1 22
FBC_CLK1_N	F20	VMC_CLK1# — VMC_CLK1# 22

(FBC_DEBUG) FBB_DEBUG0 — G14 FBC_DEBUG — R138 *EV@60.4/F_4 — +1.5V_GFX
(NC) FBB_DEBUG1 — G20 FBC_DEBUG1 — R125 *EV@60.4/F_4

No stuff follow CRB

FBB_CMD_RFU0	C12	
FBB_CMD_RFU1	C20	
FBB_WCK01	F8	
FBB_WCK01_N	E8	
FBB_WCK23	A5	
FBB_WCK23_N	A6	
FBB_WCK45	D24	
FBB_WCK45_N	D25	
FBB_WCK67	B27	
FBB_WCK67_N	C27	
FBB_WCKB01	D6	
FBB_WCKB01_N	D7	
FBB_WCKB23	C6	
FBB_WCKB23_N	B6	
FBB_WCKB45	F26	
FBB_WCKB45_N	E26	
FBB_WCKB67	A26	
FBB_WCKB67_N	A27	

FBB_PLL_AVDD — H17 +FB_PLLAVDD — C128 EV@0.1u/10V_4

C107 close to ball H17

For Fermi

FBA_CMD2	R7	EV@10K/F_4
FBA_CMD3	R8	EV@10K/F_4
FBA_CMD5	R15	EV@10K/F_4
FBA_CMD18	R466	EV@10K/F_4
FBA_CMD19	R464	EV@10K/F_4
FBC_CMD2	R161	EV@10K/F_4
FBC_CMD3	R167	EV@10K/F_4
FBC_CMD5	R137	EV@10K/F_4
FBC_CMD18	R535	EV@10K/F_4
FBC_CMD19	R541	EV@10K/F_4

0815 confirm with ZQS (sDDR3)

N14P-GV2	
N14P-GT	

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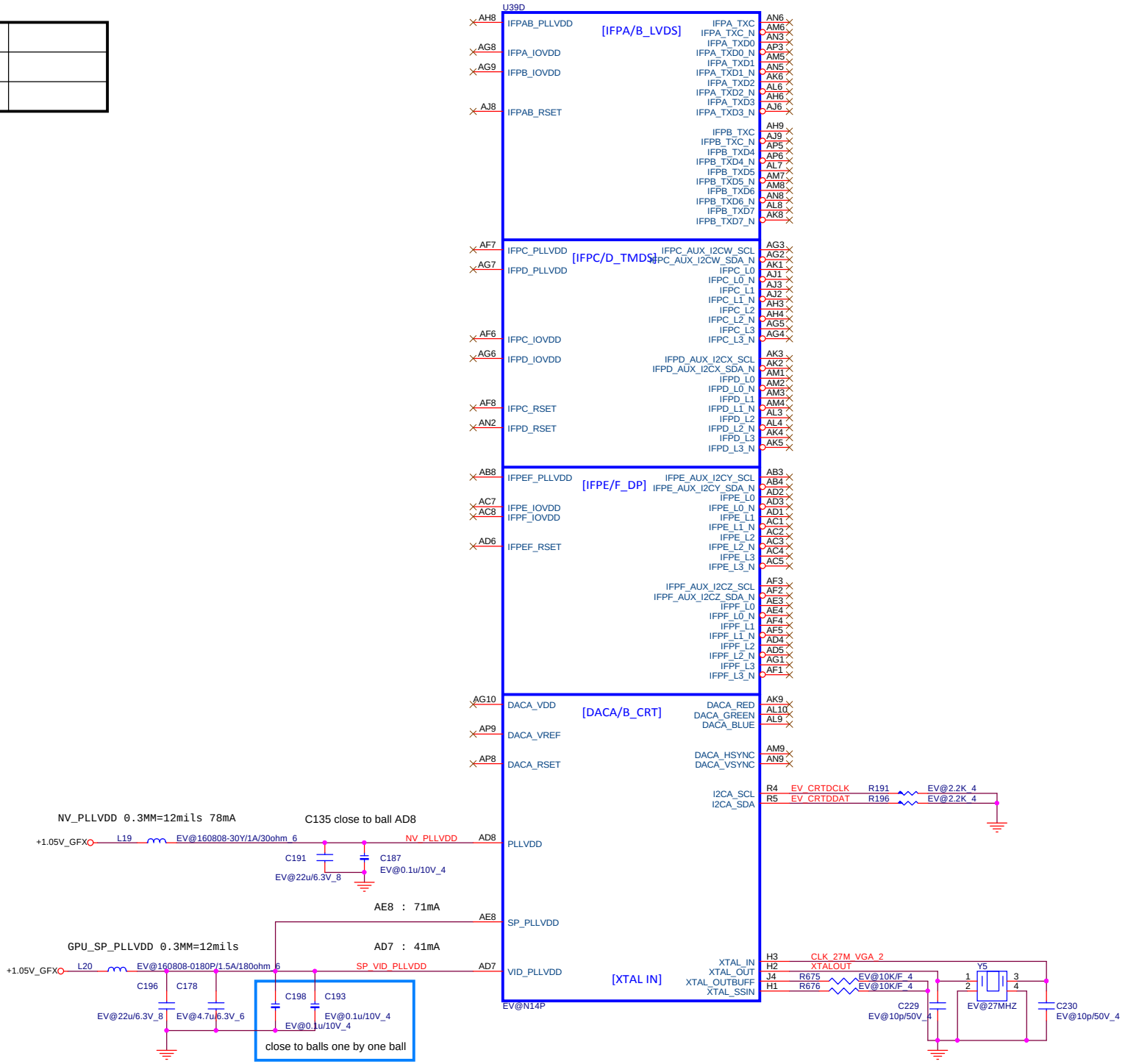
N14P-GV2	
N14P-GT	



Quanta Computer Inc.			
PROJECT : ZRQ			
Size	Document Number		Rev
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N14P-GV2	
N14P-GT	

A.ROM_SI - MEMORY STRAP
B.ROM_SO - 5K pull high

D.STRAP 0 - 45k pull high
E.STRAP 1 - 5K pull down
F.STRAP 3 - 5k pull down

C1.For N14P-GT sku
N14P-GT device ID=0x0FE4
1.ROM_SCLK =15K pull down
2.STRAP2 =25K pull down
3.STRAP4 = 45k pull down

C.For N14P-GV2 sku
N14P-GV2 QS device ID=0x1292
1.ROM_SCLK =5K pull high
2.STRAP2= 15k pull down
3.STRAP4=45 pull down
//For N14P-GV2 QS

N14P-GV2 ES device ID=0x12AD
1.ROM_SCLK =15K pull down
2.STRAP2= 30k pull high
3.STRAP4=10K pull down
//For N14P-GV2 ES

Logical Strap Bit Mapping

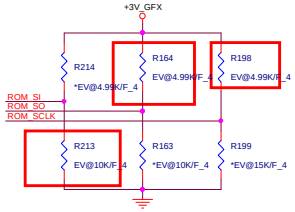
	PU-VDD	PD
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

STRAP3
Optimus ---> 4.99k PD
Discrete only ---> 15K PD

Resistor P/N
4.99K---> CS24992FB26
10K ---> CS31002FB26
15K ---> CS31502FB24
20K ---> CS32002FB29
24.9K---> CS32492FB16
30.1K---> CS33012FB18
34.8K---> CS33482FB22
45.3K---> CS34532FB18

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	FB_1	FB_0	SMB_ALT_ADDR	VGA_DEVICE	1000
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM	0010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0000
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	0100
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	0000
STRAP4	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX SPEED	DP_PLL_VDD33	0111

	ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N14P_GV	L_10K	H_4.99K	H_4.99K	H_45.3K	L_45.3K	L_15K	L_4.99K	L_45.3K
N14P_GE	L_10K	L_10K	L_10K	H_10K	H_10K	L_10K	L_10K	L_10K
N14P_GT	L_10K	H_4.99K	L_15K	H_45.3K	L_4.99K	L_24.9K	L_4.99K	L_45.3K



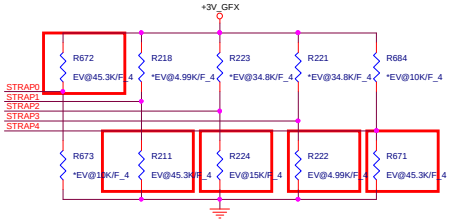
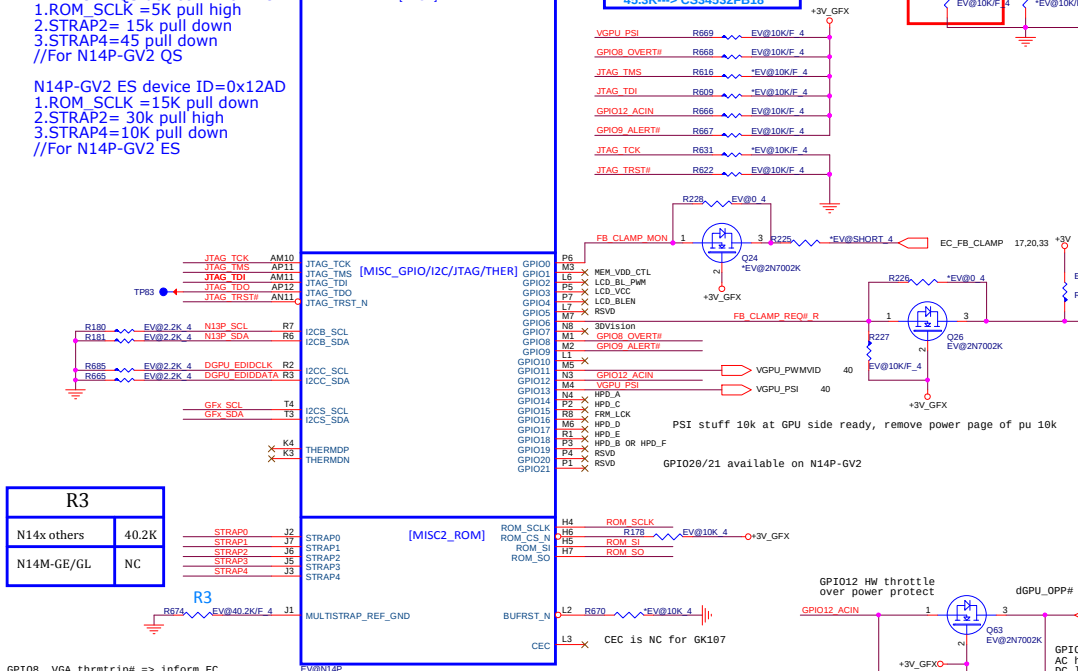


Table 9. N14P-GV/GT/GS/LP/GE GDDR5 Recommended Memories
128Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed WCK (MHz)	Memory Date Code Minimum	Status
128Mx16 GDDR5	Hynix	0x4	1.5 V/ 1.5 V	H5GQ2H24AFR-T2C	2500	N/A	Production Candidate
		0x6	1.35V/ 1.35V	H5GQ2H24AFR-T2C	2000	N/A	Production Candidate
	Samsung	0x5	1.5 V/ 1.5 V	K4G20325FD-FC04	2500	1219	Production Candidate
		0x7	1.35V/ 1.35V	K4G20325FD-FC04	2000	1219	Production Candidate

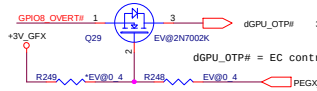
Vendor	P/N	Mfr. P/N	ROM_SI
Hynix	AKG5MWUTW13	H5GQ2H24AFR-T2C	0100
Samsung		K4G20325FD-FC04	0101



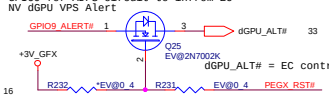
R3	
N14x others	40.2K
N14M-GE/GL	NC

R3
R674 EV@40.2K/F_4

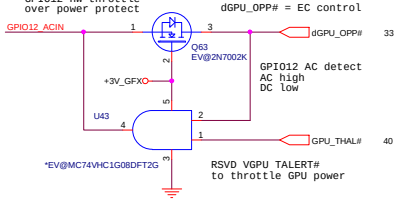
GPIO8 VGA thrmtrip# => inform EC over temperature protect



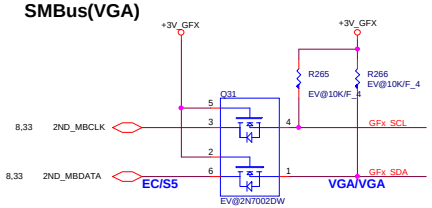
GPIO9 for ADPS circuit to infrom EC NV dGPU VPS Alert



GPIO12 HW throttle over power protect



SMBus(VGA)



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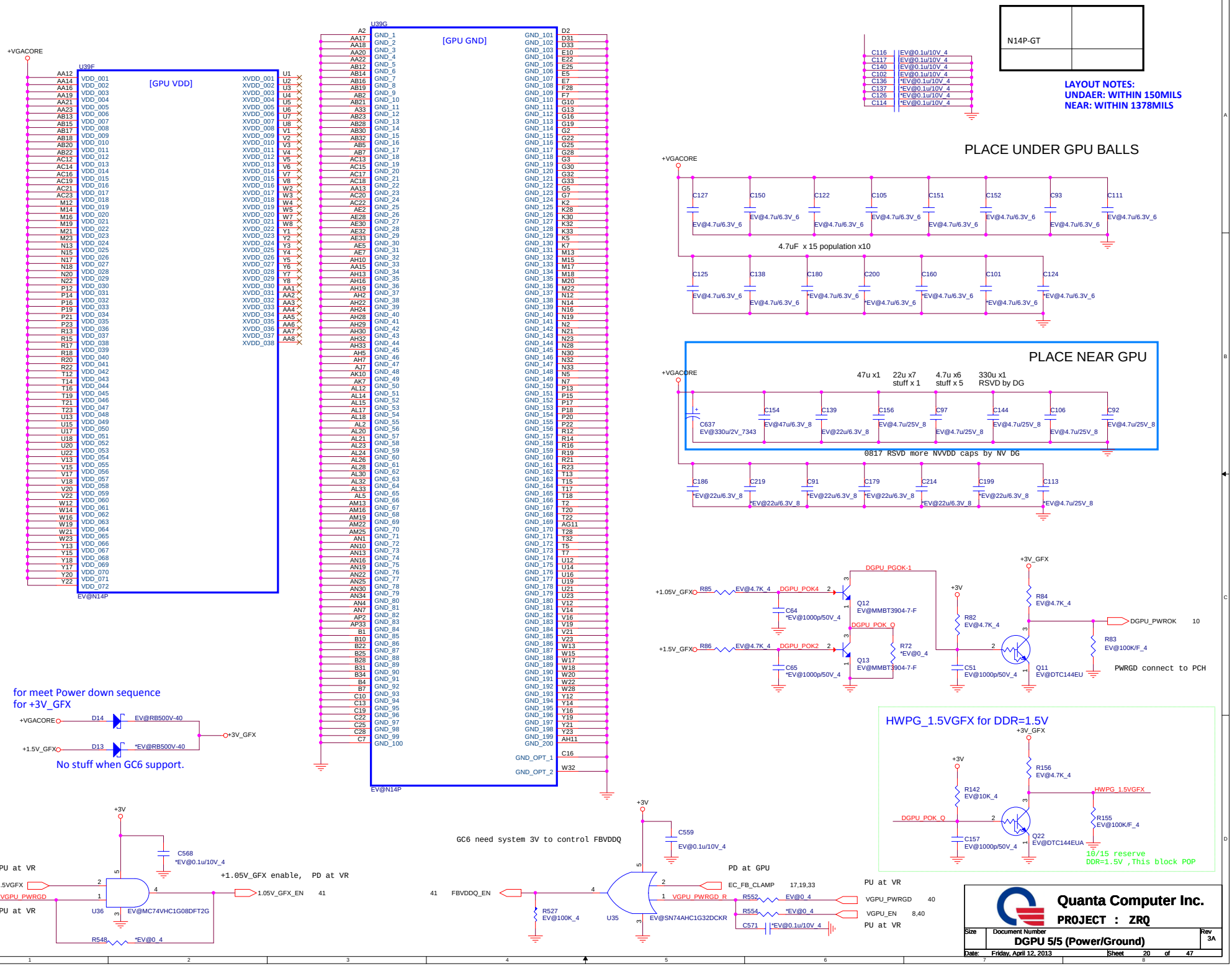
N14P-GT
LAYOUT NOTES:
UNDAER: WITHIN 150MILS
NEAR: WITHIN 1378MILS
PLACE UNDER GPU BALLS
4.7uF x 15 population x10
PLACE NEAR GPU
47u x1
22u x7
stuff x 1
4.7u x6
stuff x 5
330u x1
RSVD by DG
0817 RSVD more NVVDD caps by NV DG
[GPU VDD]
[GPU GND]
for meet Power down sequence
for +3V_GFX
No stuff when GC6 support.
PU at VR
+1.05V_GFX enable, PD at VR
GC6 need system 3V to control FBVDDQ
PD at GPU
HWPG_1.5VGFX for DDR=1.5V
10/15 reserve
DDR=1.5V ,This block POP
PWRGD connect to PCH
Quanta Computer Inc.
PROJECT : ZRQ
DGPU 5/5 (Power/Ground)
Rev 3A
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CHANNEL A: 1024MB DDR3X16

17 VMA_DQ[63..0]
17 VMA_DM[7..0]
17 VMA_WDQS[7..0]
17 VMA_RDQS[7..0]

VRAM6 / VRAM10 / VRAM5 / VRAM9 — 96-BALL SDRAM DDR3, EV@VRAM _DDR3

Should be 240 Ohms +-1%

R67 EV@243/F_4 (VRAM6)
R469 EV@243/F_4 (VRAM10)
R465 EV@243/F_4 (VRAM5)
R505 EV@243/F_4 (VRAM9)

+1.5V_GFX

R468 EV@162/F_4 (VMA_CLK0 / VMA_CLK0#)

Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

R5 EV@1.33K/F_4 — VREFC_VMA1
R6 EV@1.33K/F_4
C19 EV@0.1u/10V_4

R13 EV@1.33K/F_4 — VREFD_VMA1
R14 EV@1.33K/F_4
C9 EV@0.1u/10V_4

17 FBA_CMD17 — FBA_CMD17 — TP8
17 FBA_CMD1 — FBA_CMD1 — TP7
10/14 modify

R467 EV@162/F_4 (VMA_CLK1 / VMA_CLK1#)

Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

R12 EV@1.33K/F_4 — VREFC_VMA3
R11 EV@1.33K/F_4
C8 EV@0.1u/10V_4

R10 EV@1.33K/F_4 — VREFD_VMA3
R9 EV@1.33K/F_4
C7 EV@0.1u/10V_4

+1.5V_GFX decoupling:
C520 EV@1u/10V_4
C513 EV@1u/10V_4
C508 EV@1u/10V_4
C512 EV@1u/10V_4

C16 EV@10u/6.3V_6
C515 EV@1u/10V_4
C516 EV@1u/10V_4
C14 EV@1u/10V_4
C23 EV@1u/10V_4
C10 EV@1u/10V_4

C18 EV@10u/6.3V_6
C11 EV@1u/10V_4
C510 EV@1u/10V_4
C505 EV@1u/10V_4
C13 EV@1u/10V_4
C504 EV@1u/10V_4
C6 EV@1u/10V_4
C22 EV@1u/10V_4

C503 EV@10u/6.3V_6
C502 EV@10u/6.3V_6
C15 EV@0.1u/10V_4
C17 EV@0.1u/10V_4
C511 EV@0.1u/10V_4
C12 EV@0.1u/10V_4
C506 EV@0.1u/10V_4

C5 EV@10u/6.3V_6
C501 EV@10u/6.3V_6
C514 EV@0.1u/10V_4
C509 EV@0.1u/10V_4
C507 EV@0.1u/10V_4

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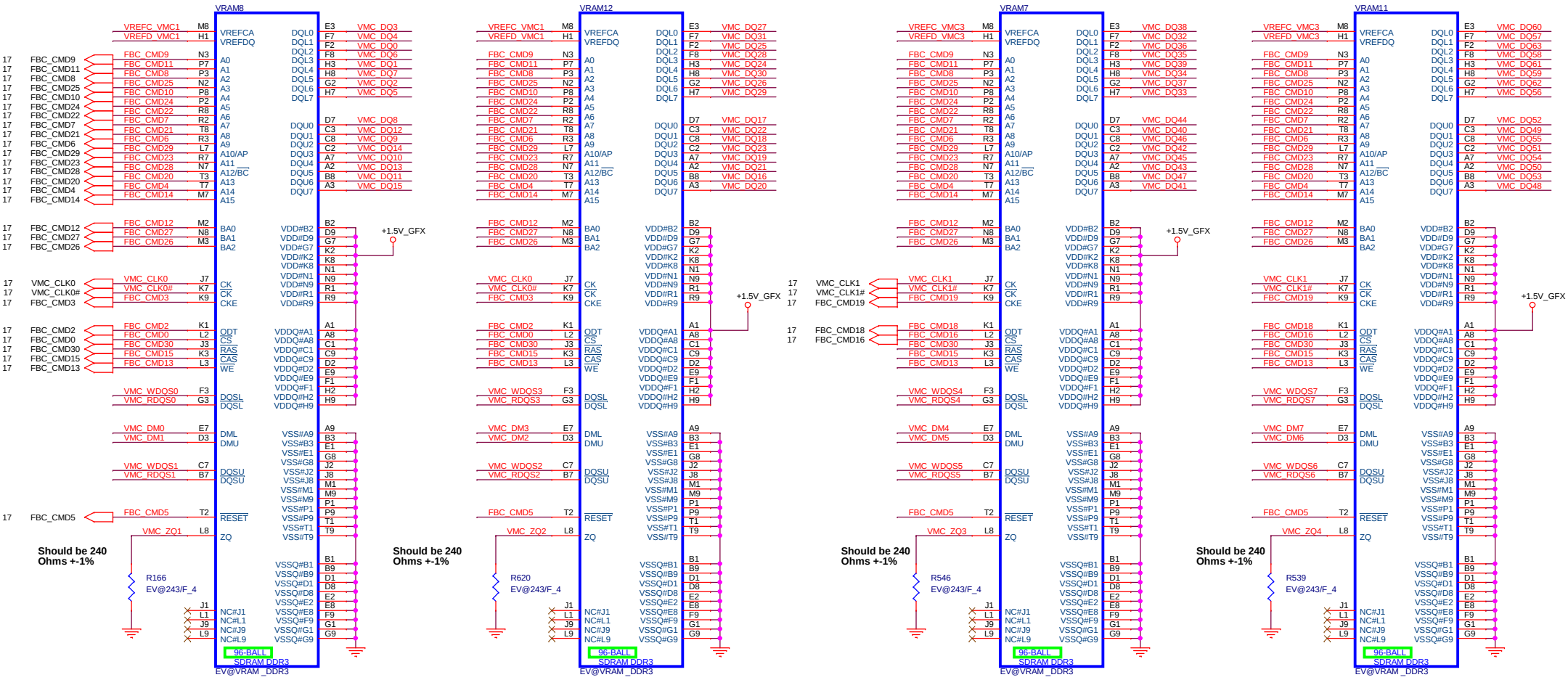
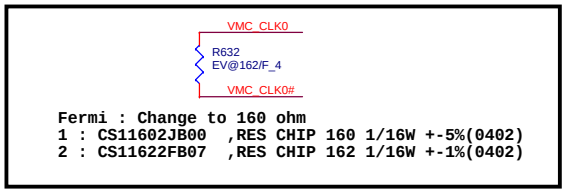
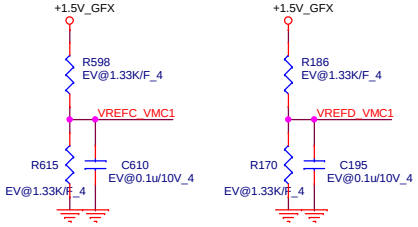
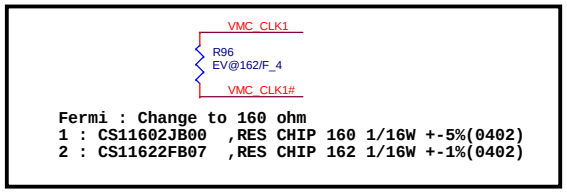
CHANNEL B: 1024MB DDR3X16

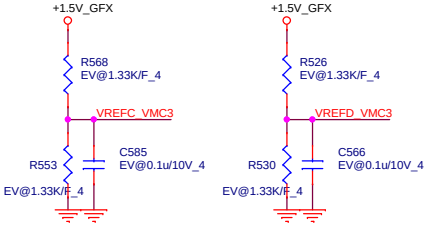
17 VMC_DQ[63..0]
17 VMC_DM[7..0]
17 VMC_WDQS[7..0]
17 VMC_RDQS[7..0]

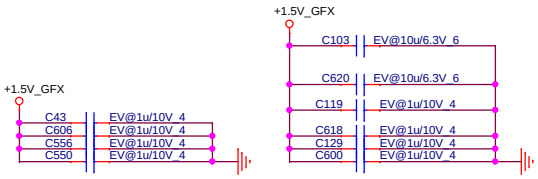












17 FBC_CMD17 FBC_CMD17 TP14
17 FBC_CMD1 FBC_CMD1 TP18

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Mini DP ML (DPP)

Layout Notes:
Place near Pin13 and Pin14

SEL/OE# polarity Control

DP AUX

DP_CAD	Behavior
Low	DP signal (AC couple)
High	TMDS signal (DC couple)

Reserve by CRB

mDP connector

30mil
500mA (Max.)

For leakage from connector

Connect to HS_SEL_IN(pin12)
Connect to SS_SEL_IN(pin7)

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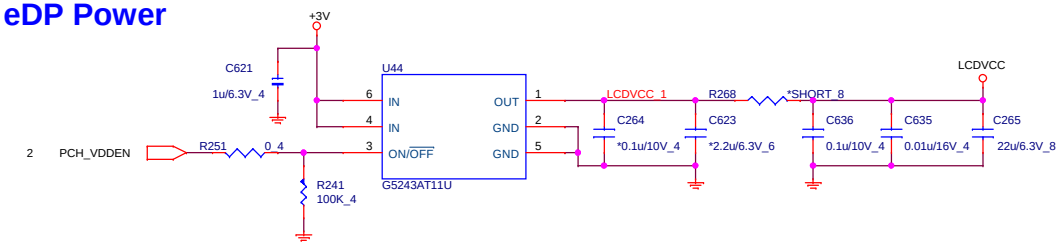
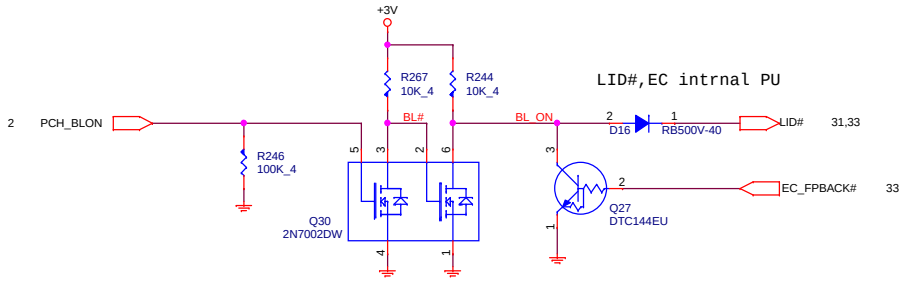
eDP Power

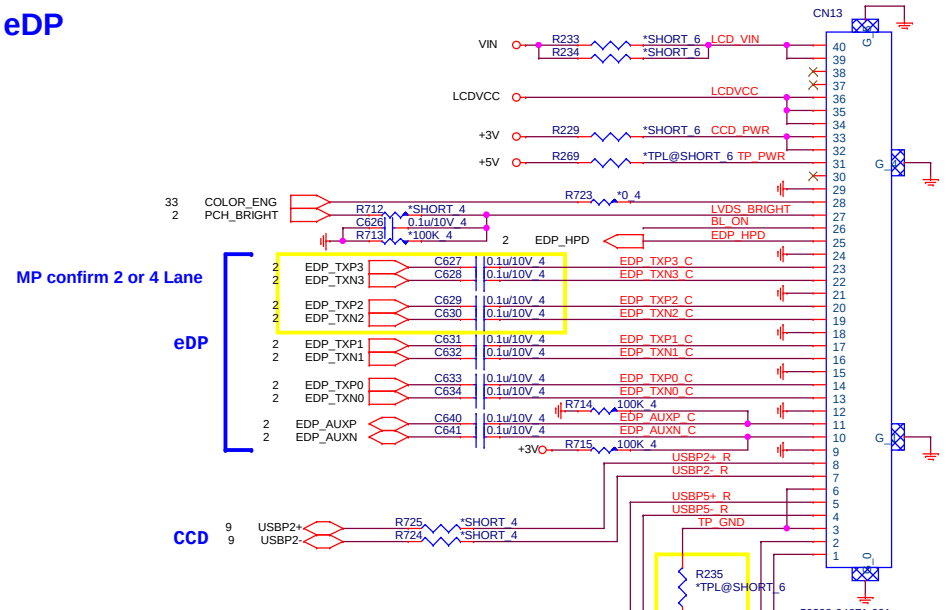


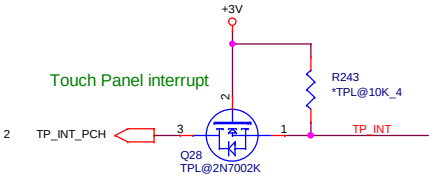
Backlight Control



Lid Switch (HSR)(move to USB/B)

eDP





Quanta Computer Inc.
PROJECT : ZRQ

Size	Document Number	Rev
	CRT/LVDS/CAMERA/LID	3A

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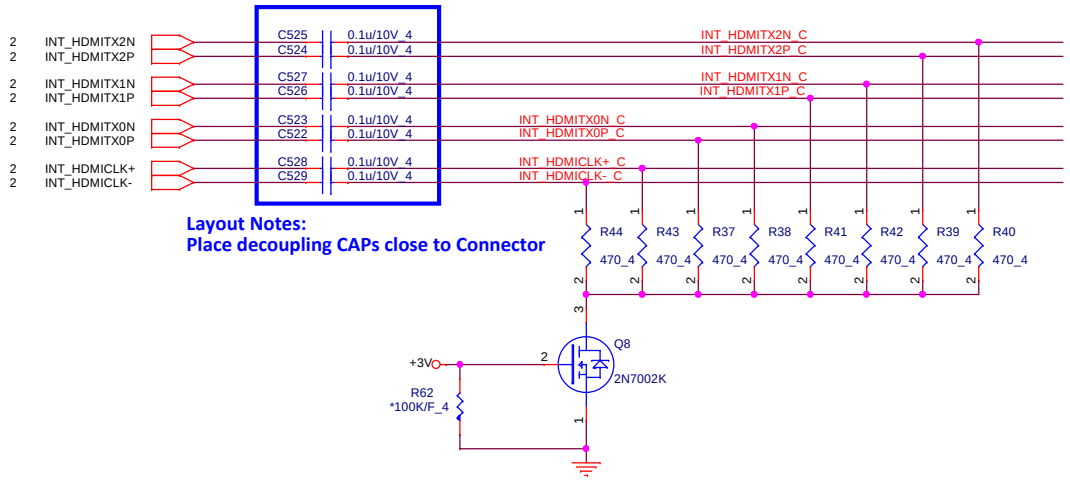
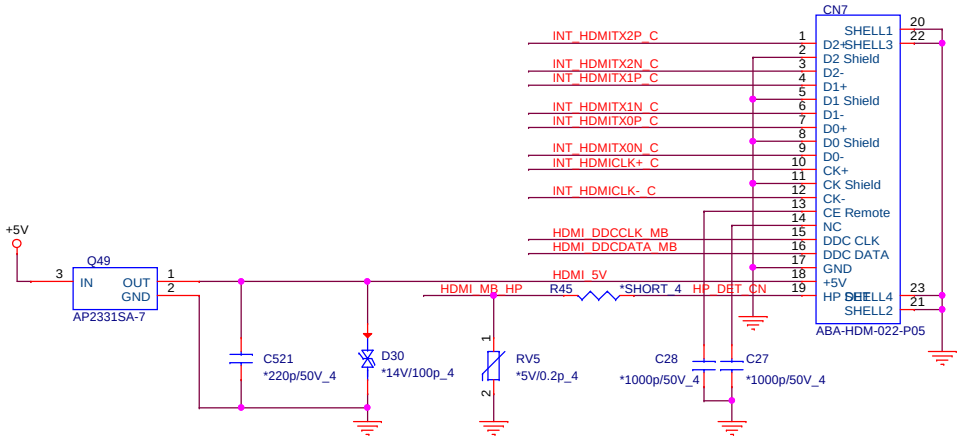
HDMI Cost Reduced level shift (HDM)

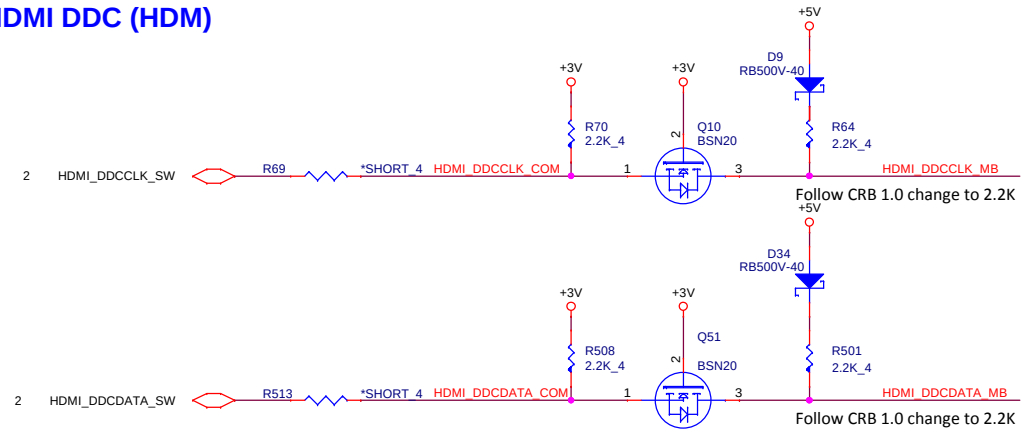


Layout Notes:
Place decoupling CAPs close to Connector

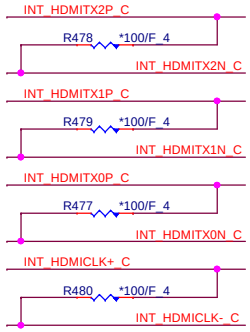
HDMI connector (HDM)



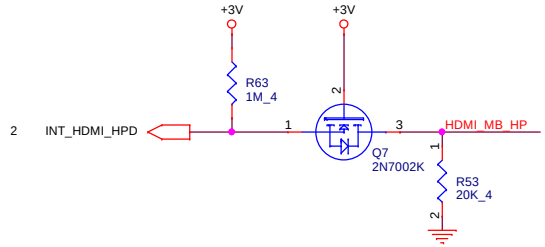
HDMI DDC (HDM)



EMI (EMC)



HDMI-detect (HDM)



Quanta Computer Inc.
PROJECT : ZRQ

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	HDMI (PS8101)	3A

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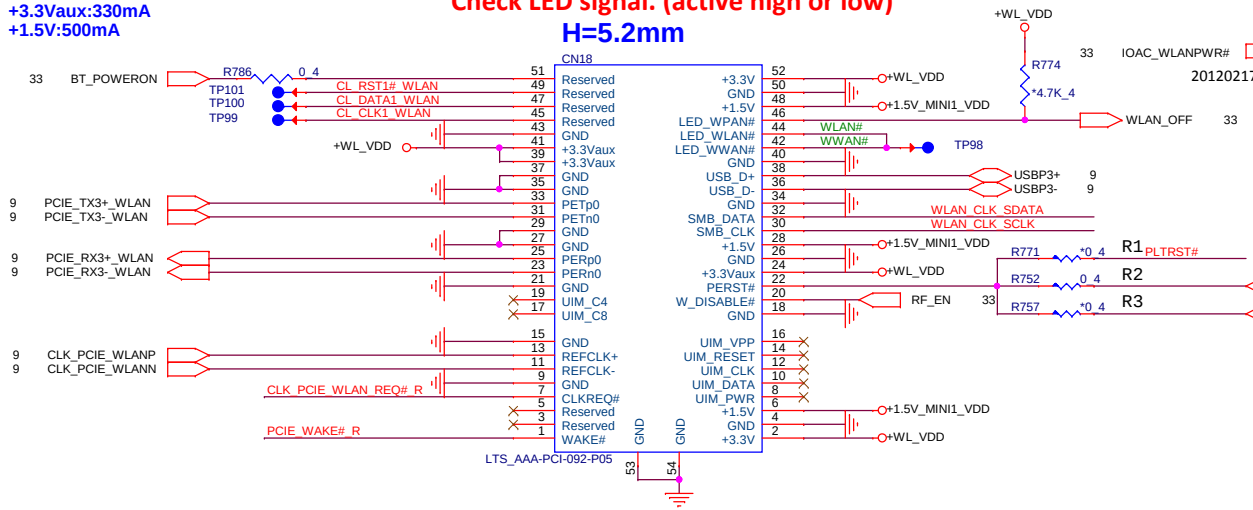
MINI-CARD WLAN(MPC)

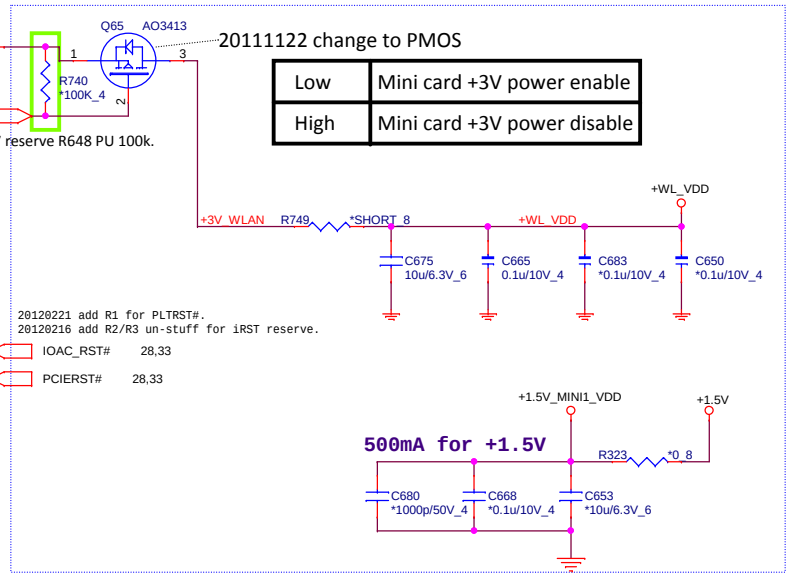
+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

Check LED signal. (active high or low)

H=5.2mm



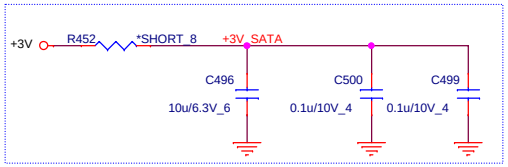
2011017 : stuff Q81 to enable wake function on WLAN for IOAC
check IOAC power rail can reduce Q81



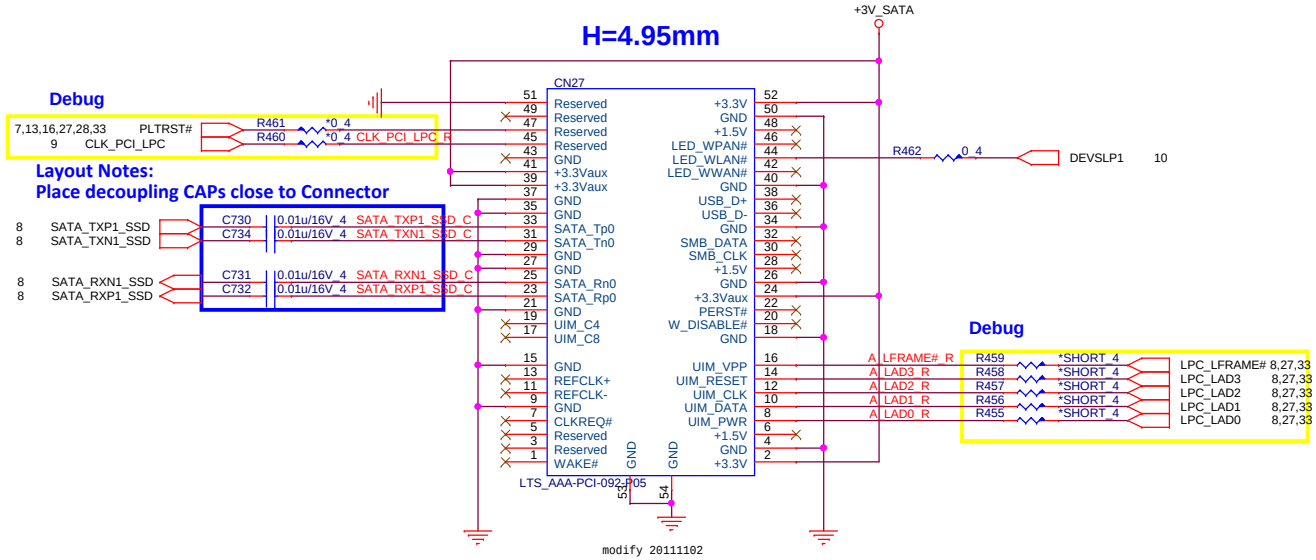
mSATA(MNC)

LAYOUT NOTE:
CLOSE TO CONNECTOR

rating = 1000mA @ 128G

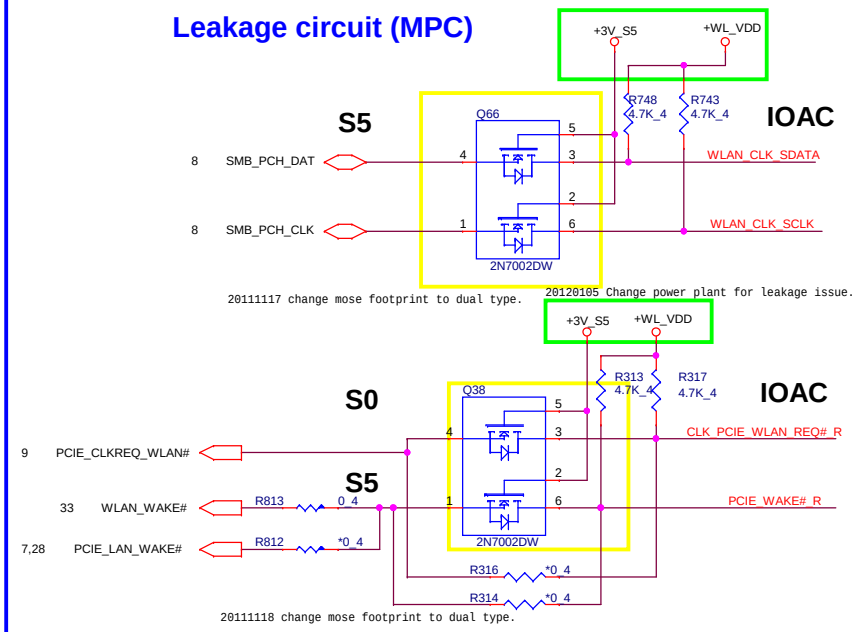


H=4.95mm



Leakage circuit (MPC)

20120105 Change power plant for leakage issue.



Quanta Computer Inc.	
PROJECT : ZRQ	
Size	Document Number: Mini Card/mSATA — Rev: 3A
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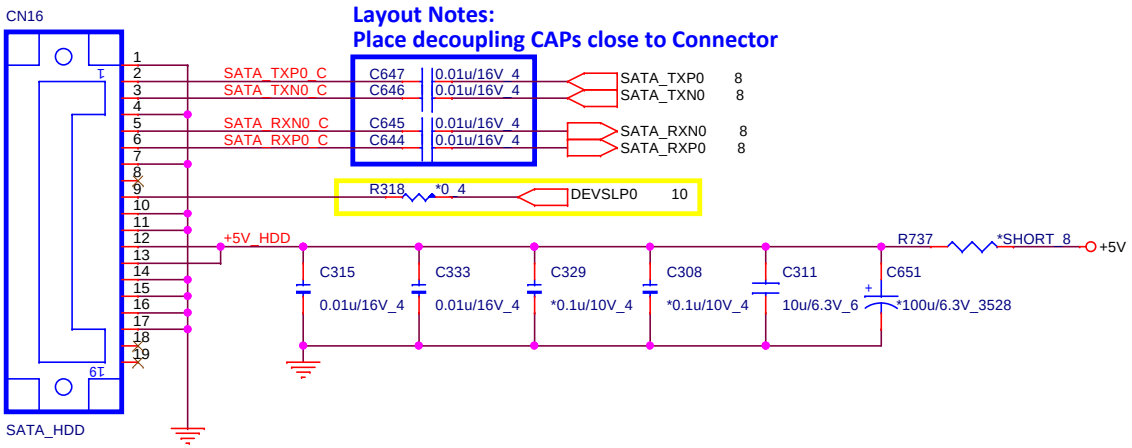
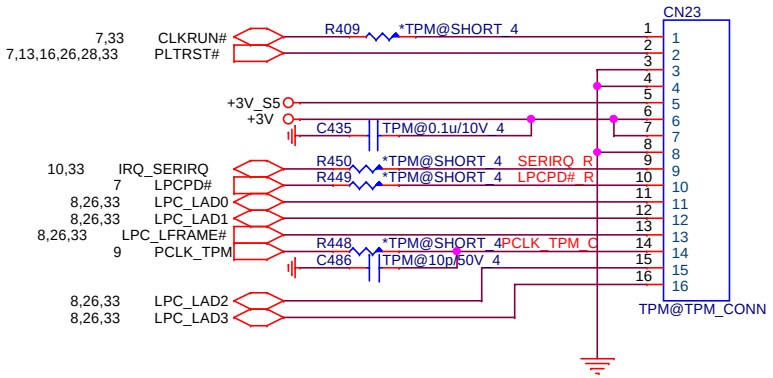
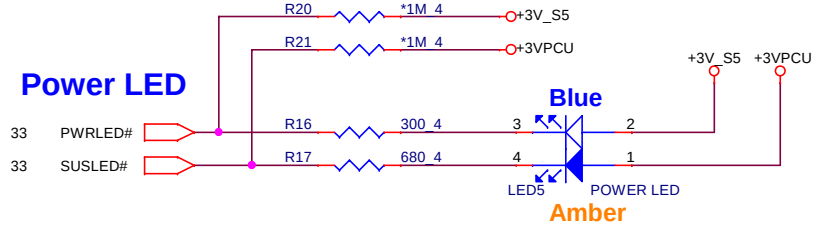
MAIN SATA HDD (HDD)

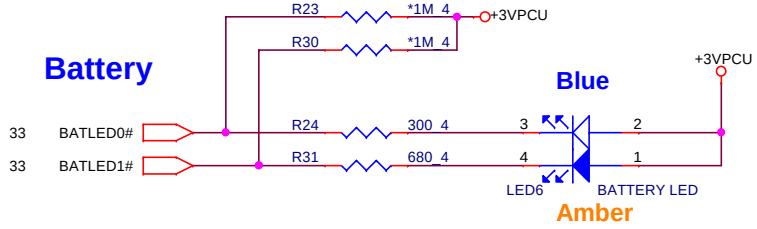


TPM (TPM)

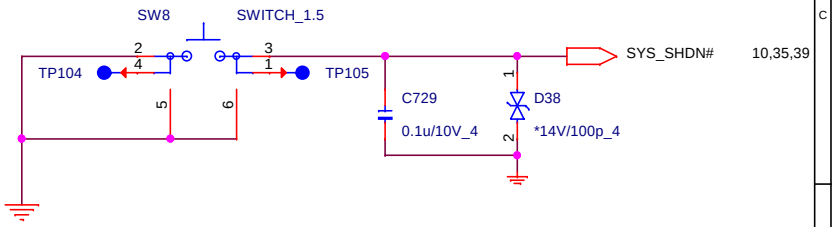


LED(UIF)





3/5VPCU reset switch (CLG)



Quanta Computer Inc.		
PROJECT : ZRQ		
Size	Document Number: SATA-HDD/ TPM	Rev: 3A
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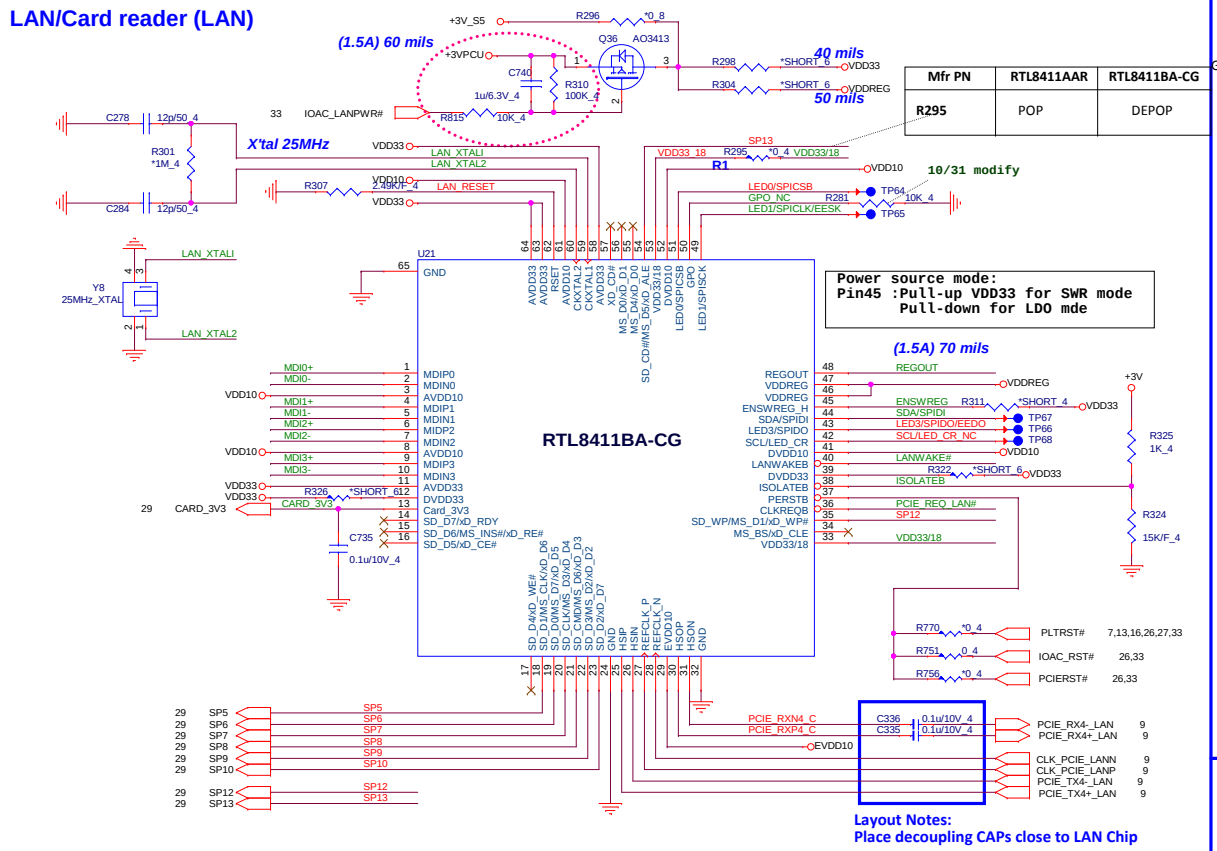
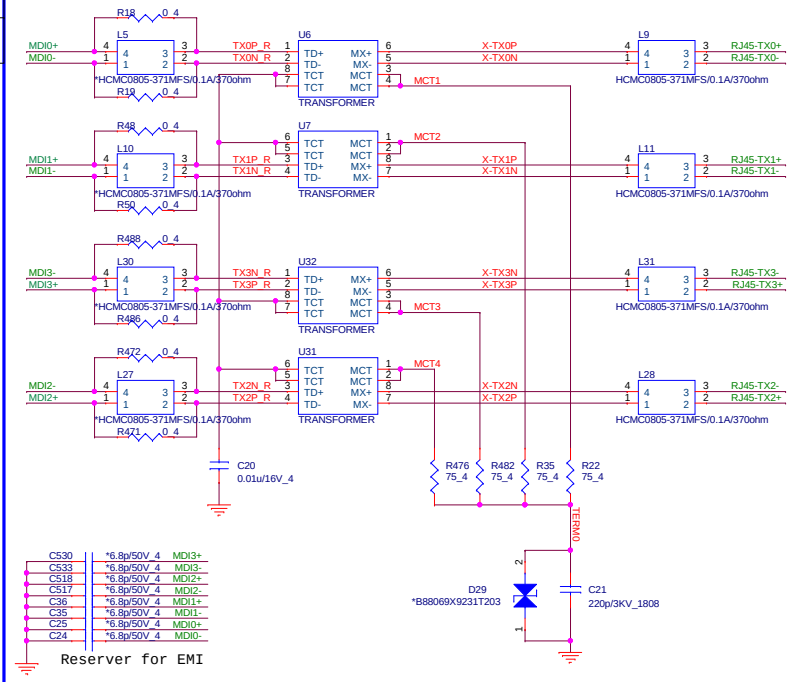
LAN/Card reader (LAN)



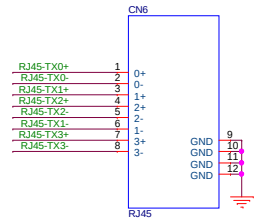
Mfr PN	RTL8411AAR	RTL8411BA-CG
R295	POP	DEPOP

High Transformer (LAN)

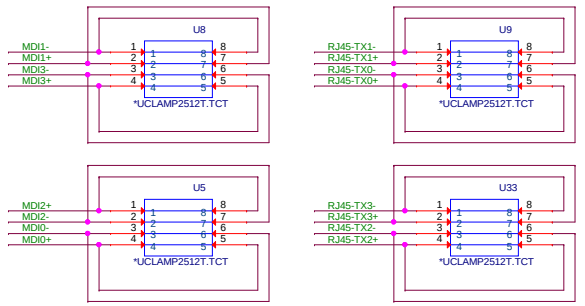
GDDR5

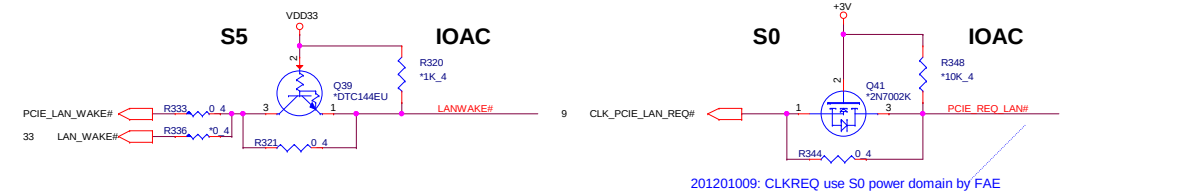


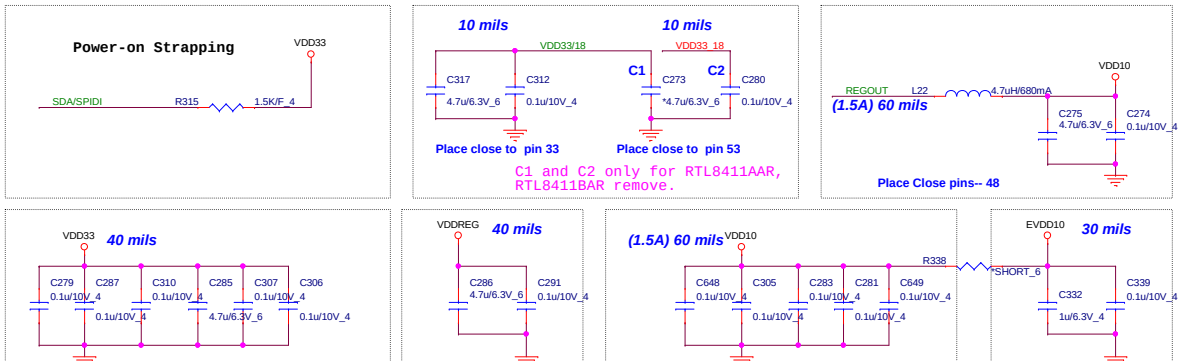
RJ45 CONNECTOR (LAN)



SURGE (LAN)







Quanta Computer Inc.			
PROJECT : ZRQ			
Size	Document Number	LAN-RTL8411/CARD READER	Rev 3A
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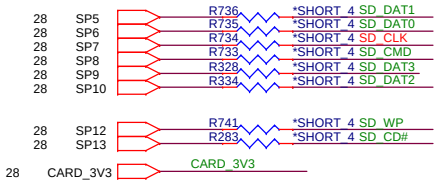
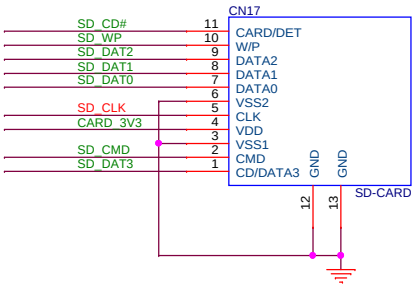
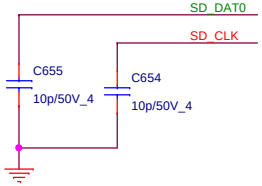
SD/MMC CARD READER CONNECTOR (MMC)

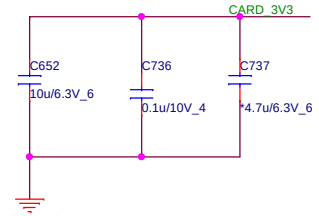




EMI



10 mils

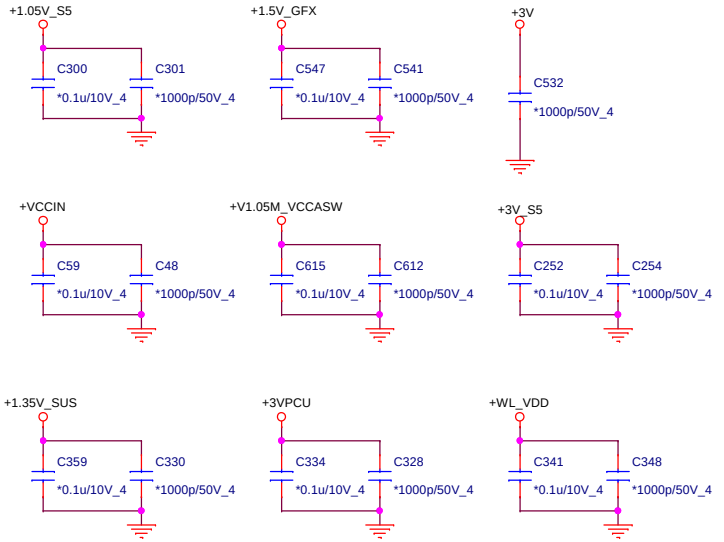


Place close to connector

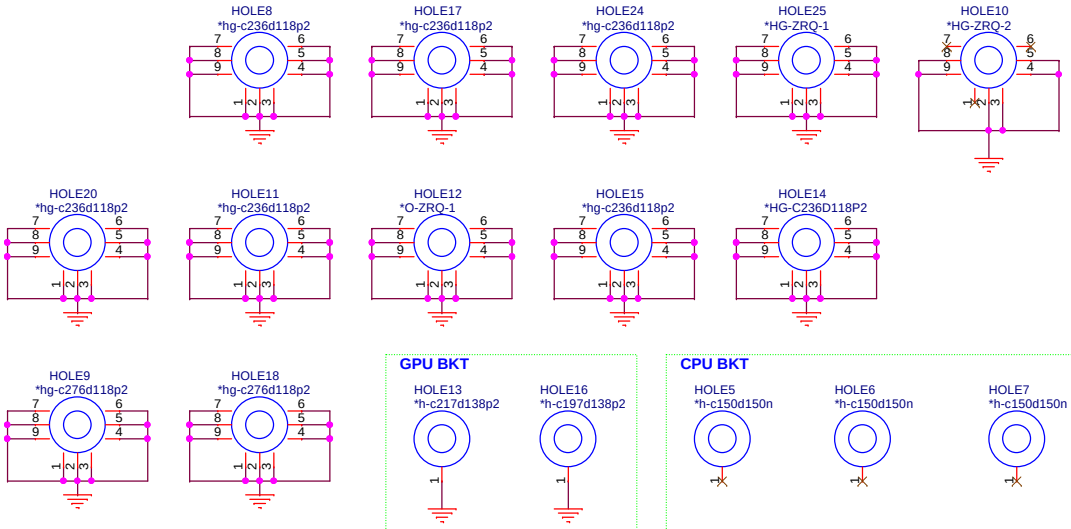
Share Pin

SP1	SD_D7		xD_RDY
SP2	SD_D6	MS_INS#	xD_RE#
SP3	SD_D5		xD_CE#
SP4	SD_D4		xD_WE#
SP5	SD_D1	MS_CLK	xD_D6
SP6	SD_D0	MS_D7	xD_D5
SP7	SD_CLK	MS_D3	xD_D4
SP8	SD_CMD	MS_D6	xD_D3
SP9	SD_D3	MS_D2	xD_D2
SP10	SD_D2		xD_D7
SP11		MS_BS	xD_CLE
SP12	SD_WP	MS_D1	xD_WP#
SP13	SD_CD#	MS_D5	xD_ALE
SP14		MS_D4	xD_D0
SP15		MS_D0	xD_D1
SP16			xD_CD#

Stitching cap (EMC)

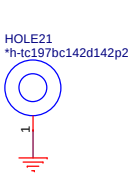


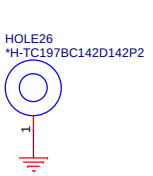
HOLE(OTH)



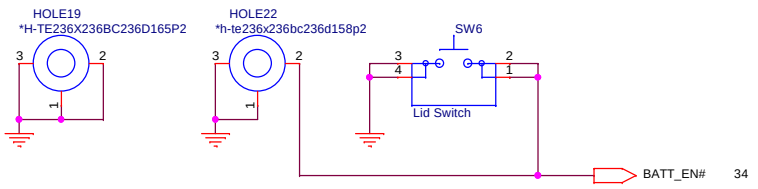
GPU BKT

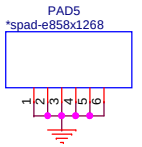
CPU BKT





BATT Enable short pad





Quanta Computer Inc.

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Size	Document Number	Rev
	CARD READER CONNECTOR	3A
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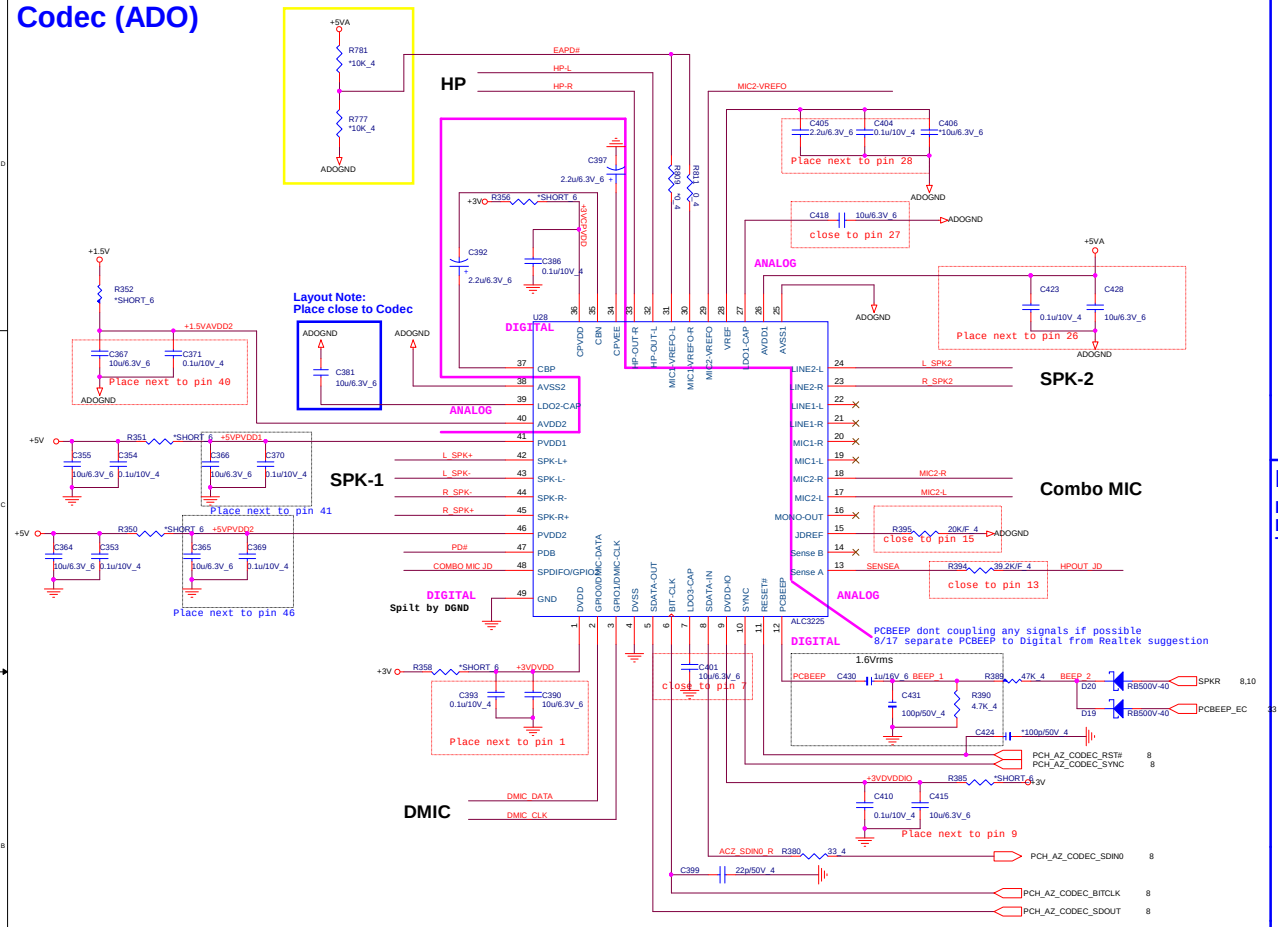
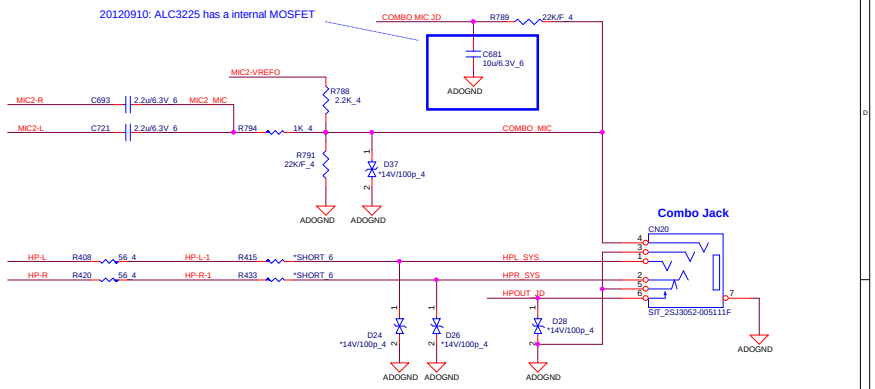
Codec (ADO)



HEADPHONE/Mic combo (AMP)

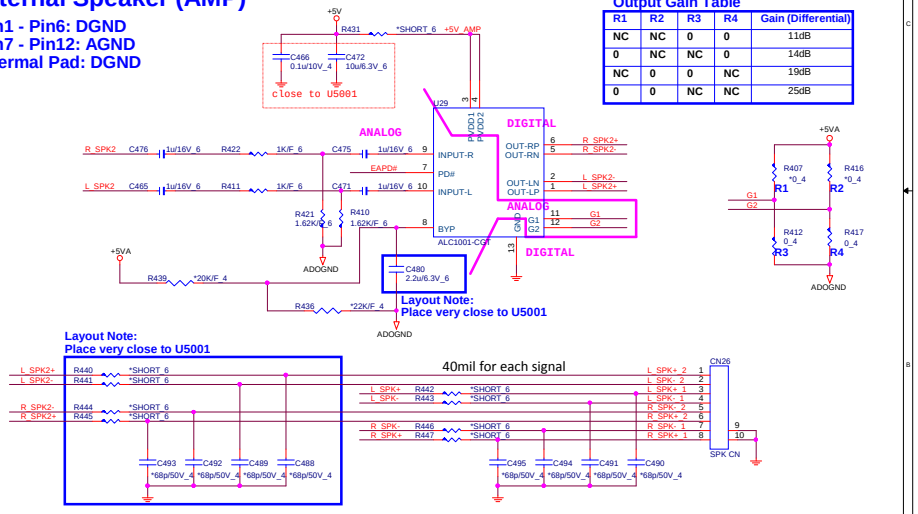


Internal Speaker (AMP)

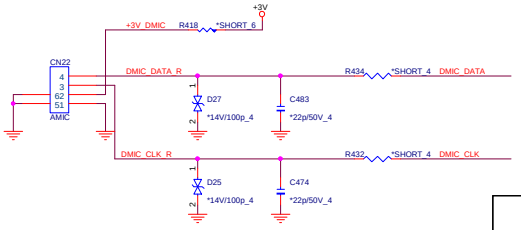
Pin1 - Pin6: DGND
Pin7 - Pin12: AGND
Thermal Pad: DGND

Output Gain Table

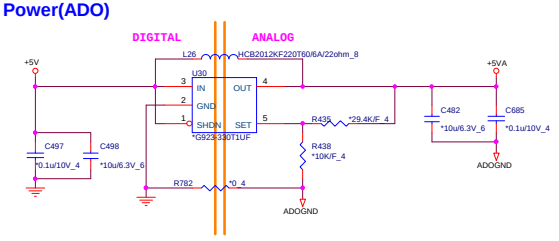
R1	R2	R3	R4	Gain (Differential)
NC	NC	0	0	11dB
0	NC	NC	0	14dB
NC	0	0	NC	19dB
0	0	NC	NC	25dB



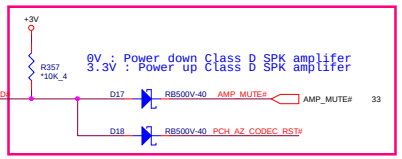
INT DMIC(AMP)



Power(ADO)



Mute(ADO)



Quanta Computer Inc.	
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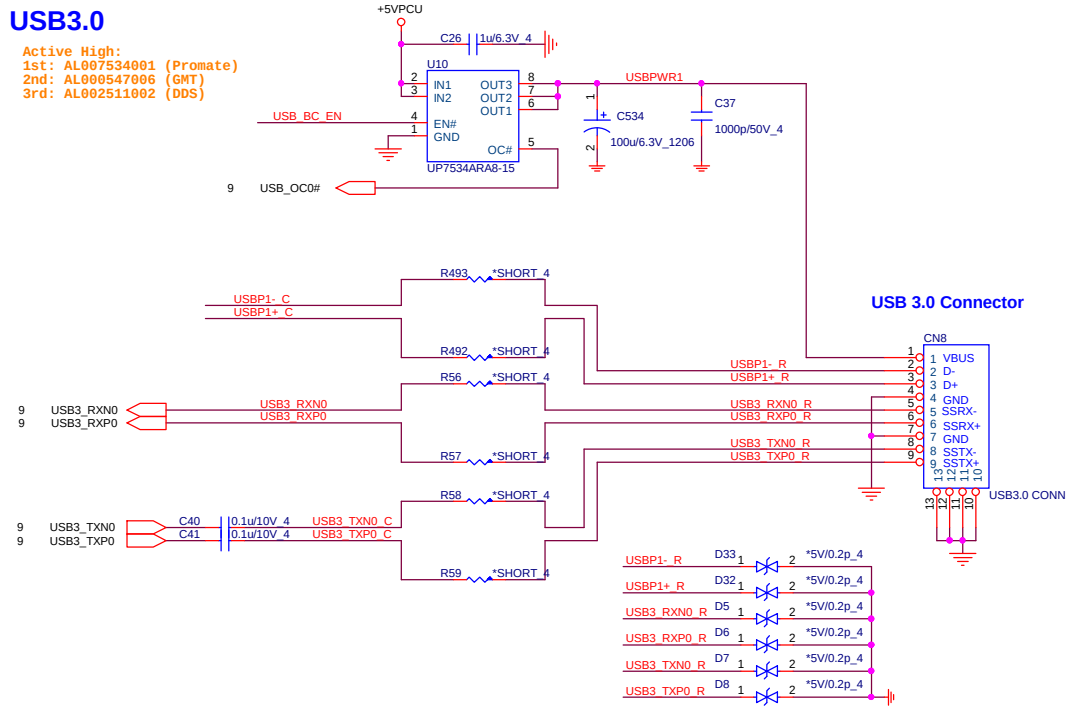
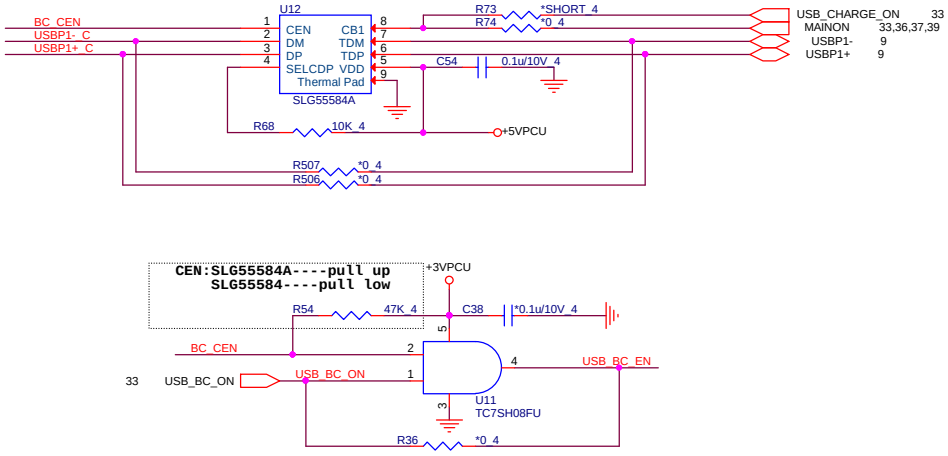
USB3.0

Active High:
1st: AL007534001 (Promate)
2nd: AL000547006 (GMT)
3rd: AL002511002 (DDS)

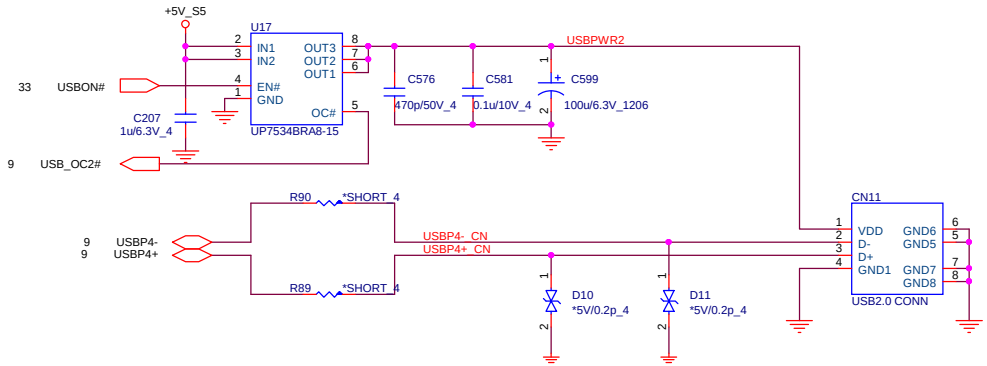


USB Charger to 3.0

CB	SELCDP	Funcion
0	X	DCP autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP only
1	1	S0 charging with CDP or SDP only (depending on external device)

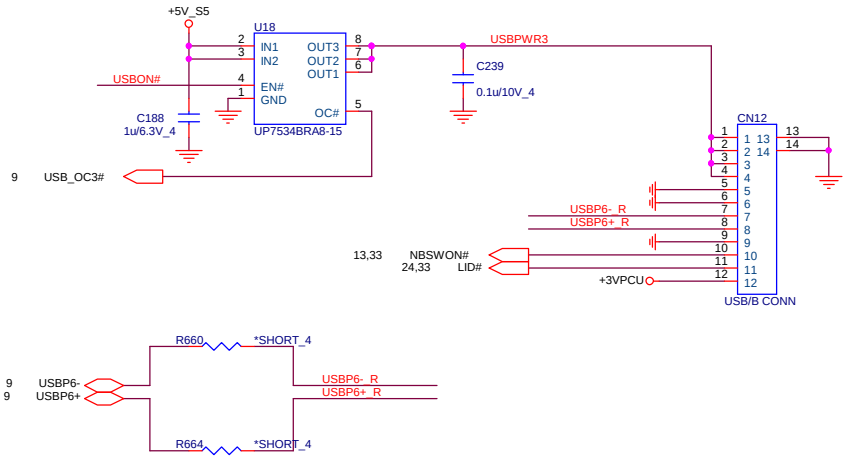


USB2.0



I/O board

1st source: AL007534000
2ns source: AL082025000



Quanta Computer Inc.
PROJECT : ZRQ

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	INT&EXT USB	3A
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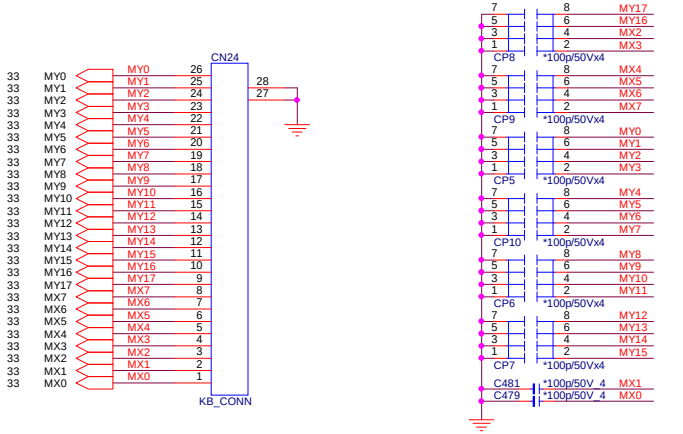
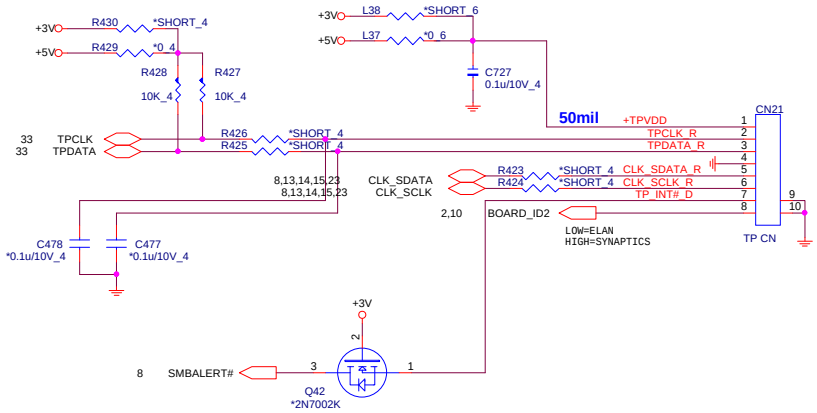
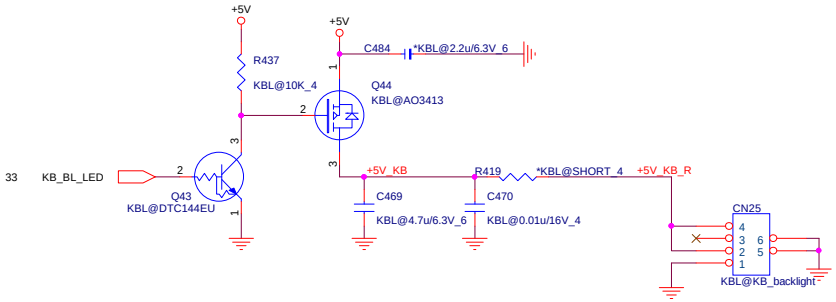
K/B (KBC)



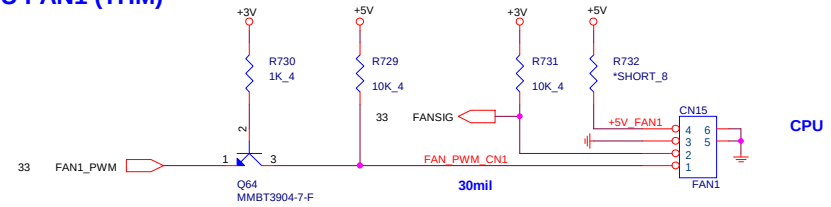
TOUCHPAD BOARD CONN (TPD)



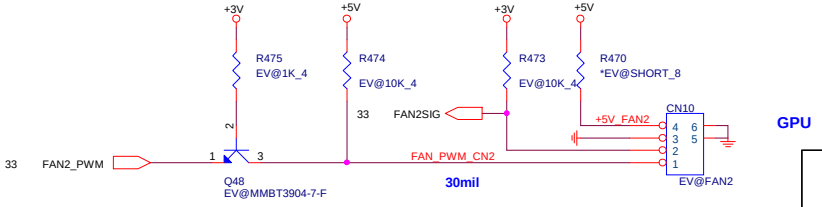
KB_BL LED (KBC)



CPU FAN1 (THM)



CPU FAN2 (THM)



Quanta Computer Inc.
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	KB/TP/FAN	3A

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EC(KBC)

+3VPCU_EC and +3V_RTC minimum trace width 12mils.

Please do not place any pull-up resistor on GPG0, GPG2, and GPG6 (Reserved hardware strapping).

IT8587

LPC · GPIO · CIR · UART port · EXTERNAL SERIAL FLASH · SPI ENABLE · KBMX · PWM · WAKE UP · A/D D/A · CLOCK · SM BUS · PS/2

IT8587E/FX

SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH/VGA
SM Bus 3	N/A
SM Bus 4	

SM BUS PU(KBC)

HWPG(KBC)

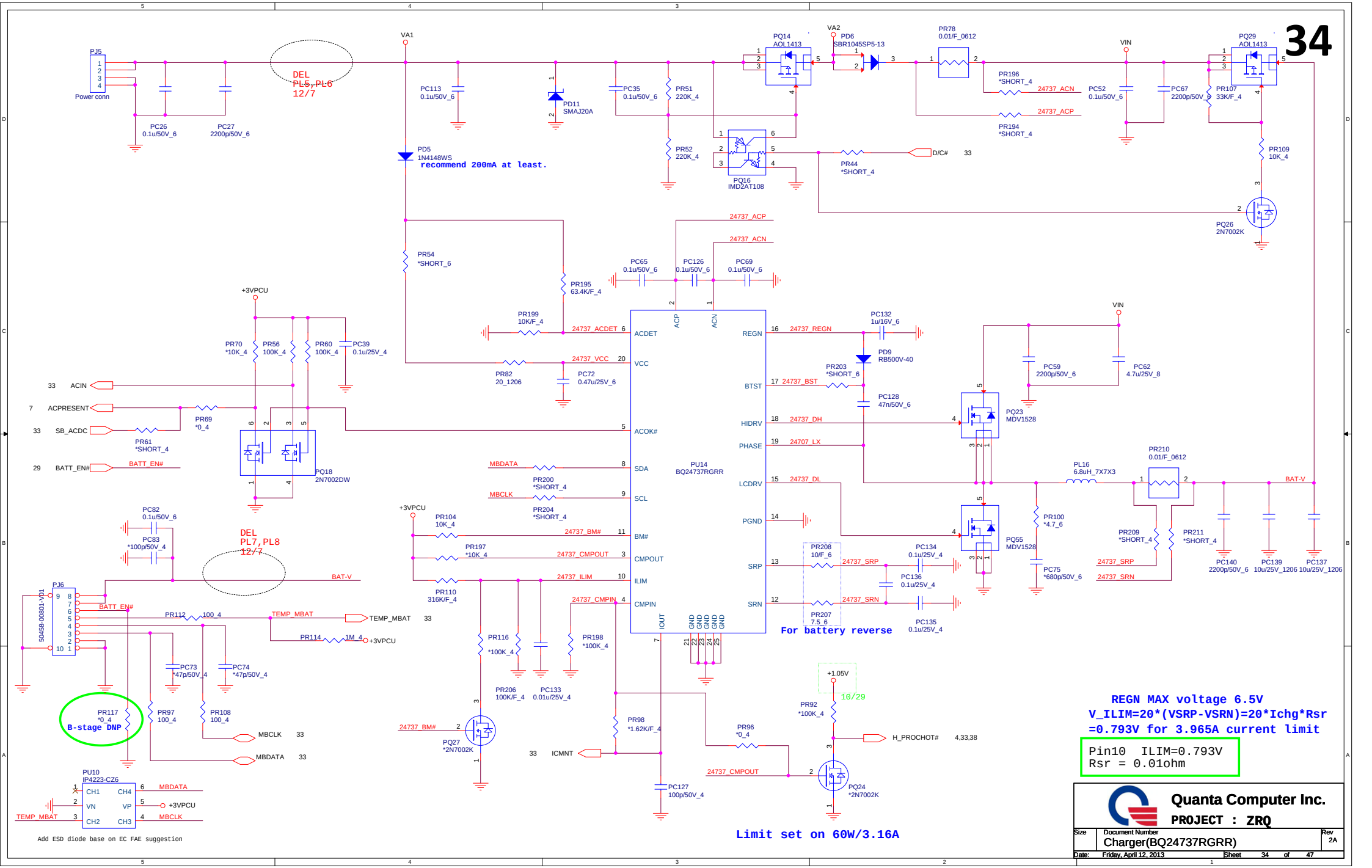
DDR=1.5V, D1 DNP and D2 POP
DDR=1.35V, D1 POP and D2 DNP

For test only

iRST

U22 *TC7SH08FU

Quanta Computer Inc.
PROJECT : ZRQ
Size | Document Number: KBC IT8587 | Rev 3A
Date: Friday, April 12, 2013 | Sheet 33 of 47


PJ5
Power conn
DEL
PL5,PL6
12/7
PC26
0.1u/50V_6
PC27
2200p/50V_6
VA1
PC113
0.1u/50V_6
PD11
SMAJ20A
PD5
1N4148WS
recommend 200mA at least.
PC35
0.1u/50V_6
PR51
220K_4
PR52
220K_4
PQ14
AOL1413
VA2
PD6
SBR1045SP5-13
PR78
0.01/F_0612
PR196
*SHORT_4
24737_ACN
PR194
*SHORT_4
24737_ACP
PQ16
IMD2AT108
PR44
*SHORT_4
D/C#
33
VIN
PC52
0.1u/50V_6
PC67
2200p/50V_6
PQ29
AOL1413
PR107
33K/F_4
PR109
10K_4
PQ26
2N7002K
PR54
*SHORT_6
PC65
0.1u/50V_6
PC126
0.1u/50V_6
PC69
0.1u/50V_6
PR195
63.4K/F_4
PR199
10K/F_4
+3VPCU
PR70
*10K_4
PR56
100K_4
PR60
100K_4
PC39
0.1u/25V_4
33
ACIN
7
ACPRESENT
33
SB_ACDC
PR69
*0_4
PR61
*SHORT_4
29
BATT_EN#
BATT_EN#
PQ18
2N7002DW
PR82
20_1206
PC72
0.47u/25V_6
24737_ACDET
24737_VCC
ACDET
VCC
ACOK#
SDA
SCL
BM#
CMPOUT
ILIM
CMPIN
IOUT
ACP
ACN
REGN
BTST
HIDRV
PHASE
LCDRV
PGND
SRP
SRN
PU14
BQ24737RGRR
MBDATA
MBCLK
PR200
*SHORT_4
PR204
*SHORT_4
24737_REGN
24737_BST
24737_DH
24707_LX
24737_DL
PC132
1u/16V_6
PD9
RB500V-40
PR203
*SHORT_6
PC128
47n/50V_6
PC59
2200p/50V_6
PC62
4.7u/25V_8
PQ23
MDV1528
PQ55
MDV1528
PR100
*4.7_6
PC75
*680p/50V_6
PL16
6.8uH_7X7X3
PR210
0.01/F_0612
BAT-V
PR209
*SHORT_4
PR211
*SHORT_4
24737_SRP
24737_SRN
PC140
2200p/50V_6
PC139
10u/25V_1206
PC137
10u/25V_1206
PR208
10/F_6
PR207
7.5_6
PC134
0.1u/25V_4
PC136
0.1u/25V_4
PC135
0.1u/25V_4
For battery reverse
PC82
0.1u/50V_6
PC83
*100p/50V_4
DEL
PL7,PL8
12/7
BAT-V
PJ6
50458-00801-V01
BATT_EN#
PR112
100_4
TEMP_MBAT
TEMP_MBAT
33
PR114
1M_4
+3VPCU
PC73
*47p/50V_4
PC74
*47p/50V_4
PR117
*0_4
B-stage DNP
PR97
100_4
PR108
100_4
MBCLK
33
MBDATA
33
PU10
IP4223-CZ6
CH1
CH4
VN
VP
CH2
CH3
MBDATA
+3VPCU
MBCLK
TEMP_MBAT
Add ESD diode base on EC FAE suggestion
PR104
10K_4
PR197
*10K_4
PR110
316K/F_4
24737_BM#
24737_CMPOUT
24737_ILIM
24737_CMPIN
PR116
*100K_4
PR206
100K/F_4
PC133
0.01u/25V_4
PR198
*100K_4
24737_BM#
PQ27
*2N7002K
33
ICMNT
PR98
*1.62K/F_4
PC127
100p/50V_4
PR96
*0_4
24737_CMPOUT
+1.05V
10/29
PR92
*100K_4
H_PROCHOT#
4,33,38
PQ24
*2N7002K
REGN MAX voltage 6.5V
V_ILIM=20*(VSRP-VSRN)=20*Ichg*Rsr
=0.793V for 3.965A current limit
Pin10 ILIM=0.793V
Rsr = 0.01ohm
Limit set on 60W/3.16A
Quanta Computer Inc.
PROJECT : ZRQ
Size
Document Number
Charger(BQ24737RGRR)
Rev
2A
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MAIND → MAIND 36,37,39

SYS_SHDN# → SYS_SHDN# 10,27,39

+5VPCU
5 Volt +/- 5%
TDC : 5.4A
PEAK : 7.2A
OCP : 9A
Width : 220mil

+3VPCU
3.3 Volt +/- 5%
TDC : 4.7A
PEAK : 6.2A
OCP : 7.5A
Width : 200mil

OCP:9A
L(ripple current)
=(9-5)*5/(2.2u*0.3M*9)
=3.367A
Iocp=9-(3.367/2)=7.32A
Vth=7.32A*14mOhm+1mV=103.43mV
R(Ilim)=(103.43mV*8)/10uA
=82.774K

OCP:7.5A
L(ripple current)
=(9-3.3)*3.3/(2.2u*0.355M*9)
~2.676A
Iocp=7.5-(2.676/2)=6.16A
Vth=6.16A*14mOhm+1mV=87.27mV
R(Ilim)=(87.27mV*8)/10uA
~69.81K

TDC : 1.5A
PEAK : 2A
Width : 80mil

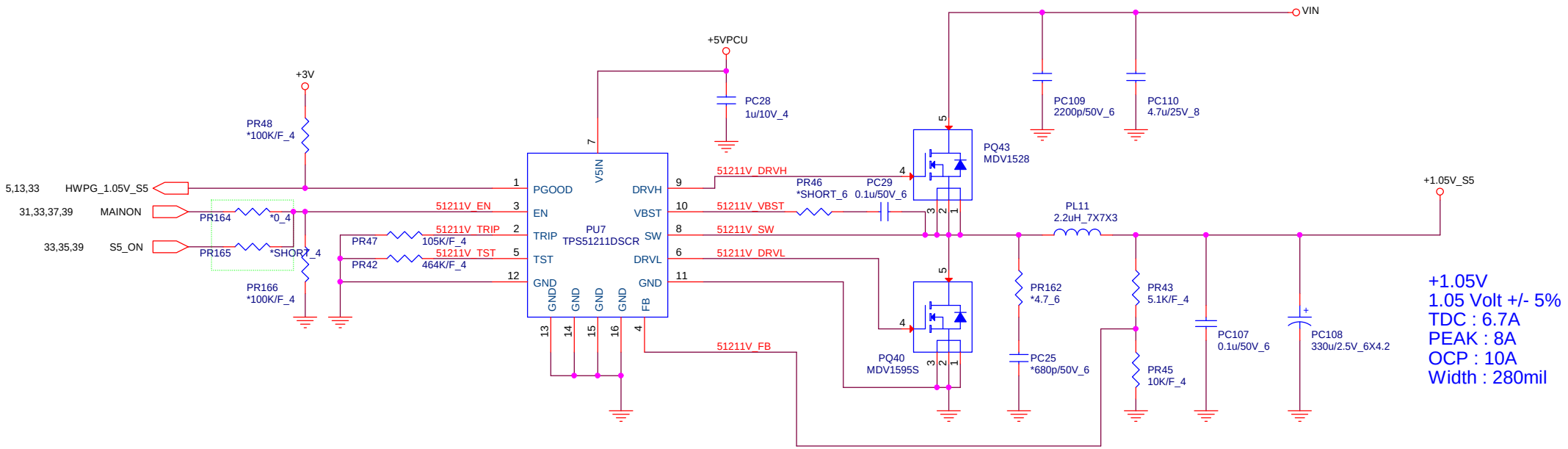
TDC : 2.4A
PEAK : 3.2A
Width : 100mil

TDC : 1.4A
PEAK : 1.8A
Width : 110mil

TDC : 1.2A
PEAK : 1.6A
Width : 60mil

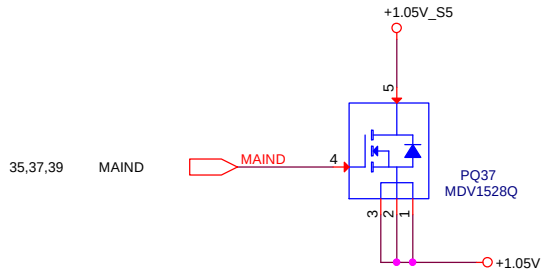
Quanta Computer Inc.
PROJECT : ZRQ

Size	Document Number	Rev
	SYSTEM 5V/3V (TPS51225)	2A
Date: Friday, April 12, 2013	Sheet 35 of 47	



+1.05V
1.05 Volt +/- 5%
TDC : 6.7A
PEAK : 8A
OCP : 10A
Width : 280mil

OCP=10A
L ripple current
=(19-1.05)*1.05/(2.2u*290k*19)
=1.555A
Vtrip=10-(1.555/2)*14mohm
=0.129V
Rlimit=0.129/10uA*8=103.293Kohm



TDC : 2.4A
PEAK : 3.2A
Width : 100mil

Quanta Computer Inc.
PROJECT : ZRQ

Size	Document Number	Rev
	+1.05V(TPS51211)	2A
Date: Friday, April 12, 2013	Sheet 36 of 47	

TDC : 0.75A
PEAK : 1A
Width : 40mil

+DDR_VTT_RUN

PC61 10u/6.3V_6
PC66 10u/6.3V_6

TDC : 0.38A
PEAK : 0.5A
Width : 20mil

DDR_VTTREF

PC70 0.22u/10V_4

Close to IC

Greater than or equal 40mil

+5VPCU

PC63 10u/6.3V_6
PC78 1u/10V_4

+3V

PR94 *100K/F_4

10/29

PU11
TPS51216RUKR

PAD PAD VTTREF VTTGND VTTSNS VTT VLDOIN
22 21 5 4 1 3 2

33 HWPG_VDDR — PGOOD 20
31,33,36,39 MAINON — PR103 *0_4 — 51216_S3 — S3 17
33 SUSON — PR106 *SHORT_4 — 51216_S5 — S5 16
PR95 200K/F_4 — 51216_MODE — MODE 19
PR99 15.4K/F_4 — 51216_TRIP — TRIP 18
PAD 26

V5IN 12
DRVH 14 — 51216_DRVH — PR111 2/F_6 — PC79 0.1u/50V_6
VBST 15 — 51216_VBST
SW 13 — 51216_SW
DRVL 11 — 51216_DRVL
PGND 10

REF REFIN VDDQSNS PAD PAD PAD GND
6 8 9 25 24 23 7

VREF=1.8V

51216_REF — PC71 0.1u/10V_4

51216_REFIN — PR102 10K/F_4

51216_S3 — PR202 *0_4 — 51216_S5

PR201 *SHORT_6

VIN

PC141 2200p/50V_4
PC142 4.7u/25V_8

PQ58
FDMS3660S
G1 S1/D2 G2 S2 S2 S2 D1 D1 D1
1 2 8 7 6 5

51216_SW — PL17 0.68uH_7X7X3 — +1.35V_SUS

PR119 *4.7_6 10/12 change
PC80 *680p/50V_6

RDSon=3.2mohm

PC138 0.1u/50V_6
PC143 330u/2.5V_6X4.2
PC84 *330u/2V_7343

+1.35V_SUS
1.35 Volt +/- 5%
TDC : 12.6A
PEAK : 16.8A
OCP : 20A
Width : 520mil

+1.35V_SUS — +1.35V_SUS 4,5,14,15,29,41

Close to output cap

stuff for C8 ODT power off

4 DDR_VTTT_PG_CTRL — PR205 *SHORT_4 — 51216_S3

PR101 30.1K/F_4
PC77 0.01u/25V_4

Mode	Frequency	Discharge mode
200K	400K	Tracking Discharge
100K	300K	Tracking Discharge

	S3	S5	+1.35VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

OCP=10A
L ripple current
=(19-1.35)*1.35/(0.68u*400k*19)
=4.611A
Vtrip=10-(4.611/2)*2.5mohm
=0.01923V
Rlimit=0.01923/10uA*8=15.389Kohm

OCP=20A
L ripple current
=(19-1.5)*1.5/(0.68u*400k*19)
=5.079A
Vtrip=20-(5.079/2)*2.5mohm
=0.04365V
Rlimit=0.04365/10uA*8=34.92Kohm

DDR=1.35V
OCP=10A
PR95=15.4K/F_4
PR97=30.1K/F_4

DDR=1.5V
OCP=20A
PR95=35.7K/F_4
PR97=51K/F_4

+1.35V_SUS

35,36,39 MAIND — MAIND 2 — PQ59 *AO3404 — +1.5V

TDC : 0.56A
PEAK : 0.75A
Width : 20mil

10/12 reserve
DDR=1.5V,PC9032 & PQ9016 POP

Quanta Computer Inc.
PROJECT : ZRQ

Size	Document Number	Rev
	DDR 1.35V(TPS51216)	2A

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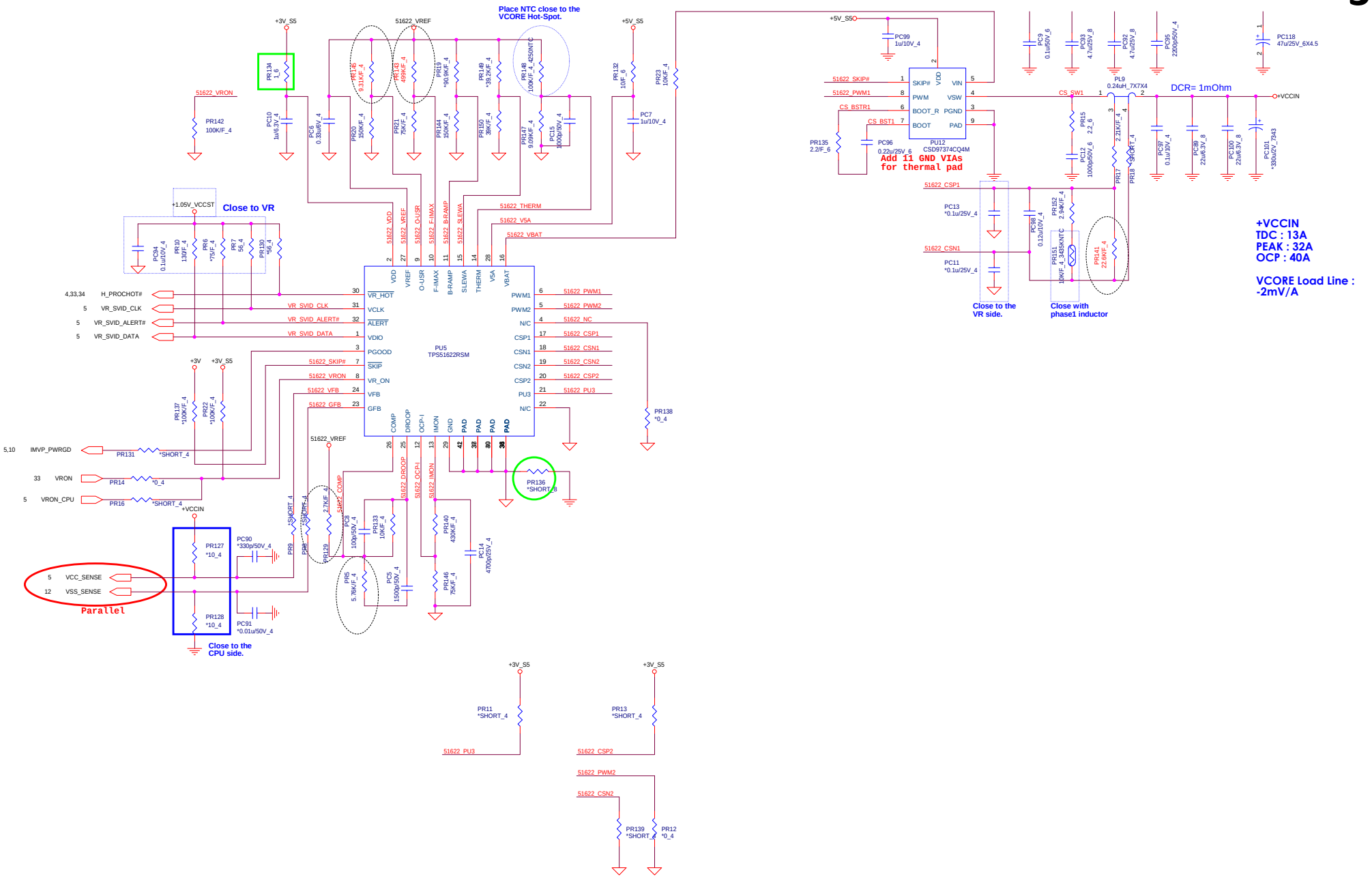
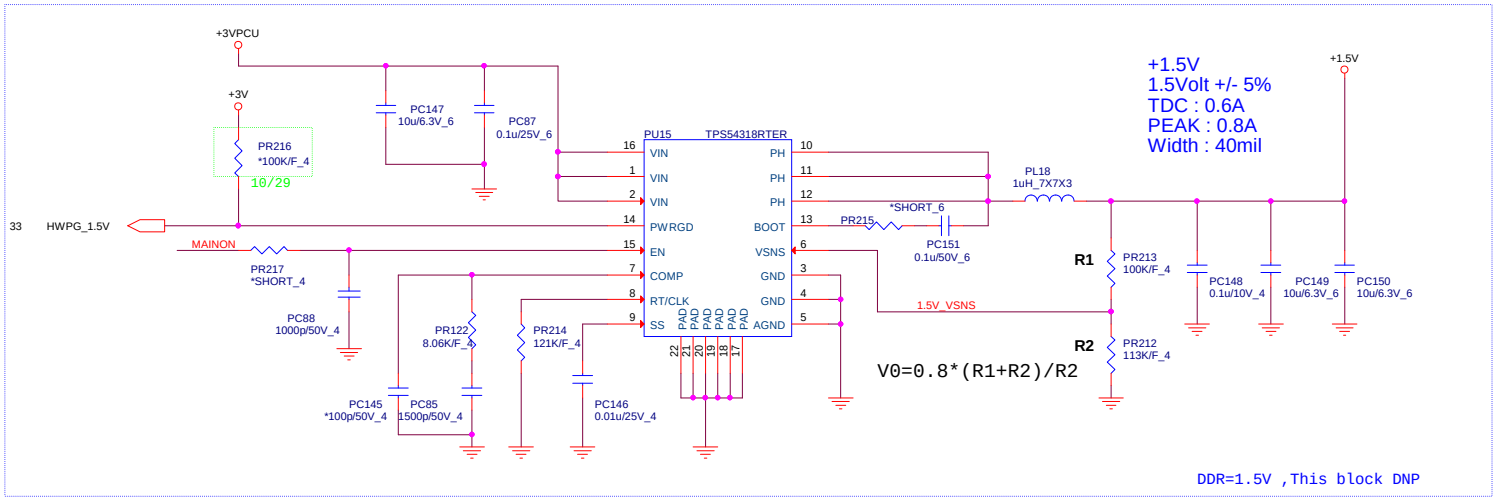
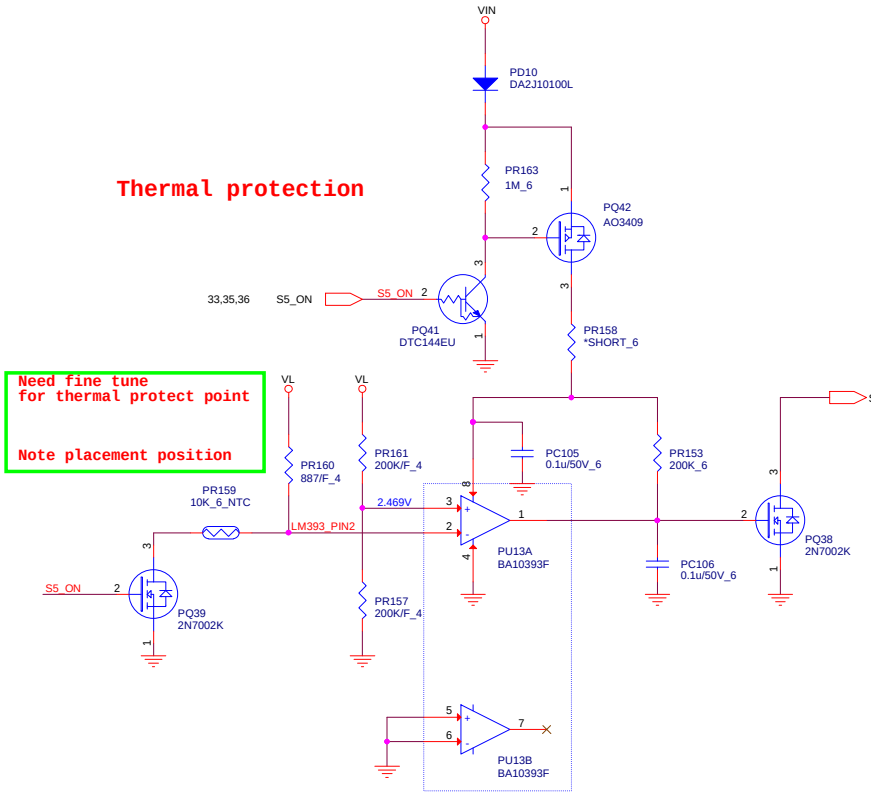
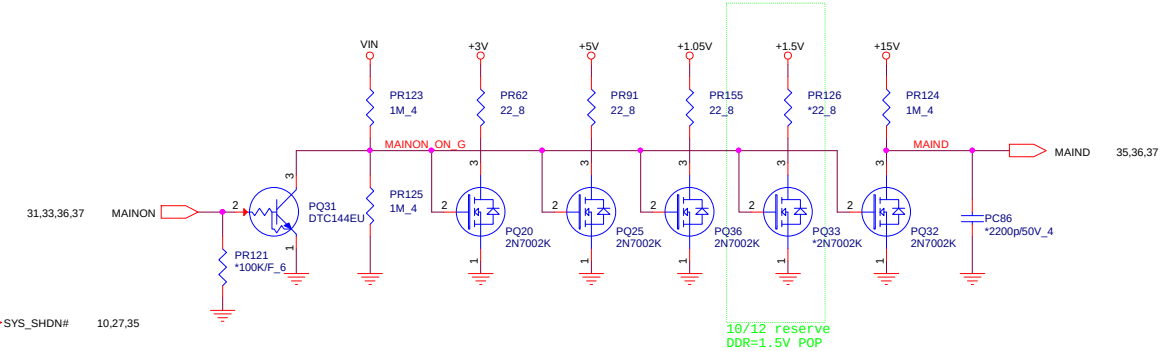


Quanta Computer Inc.	
PROJECT : ZRQ	
Size	Document Number: +VCCIN(TPS51622) — Rev: 2A
Date: Friday, April 12, 2013	Sheet 38 of 47



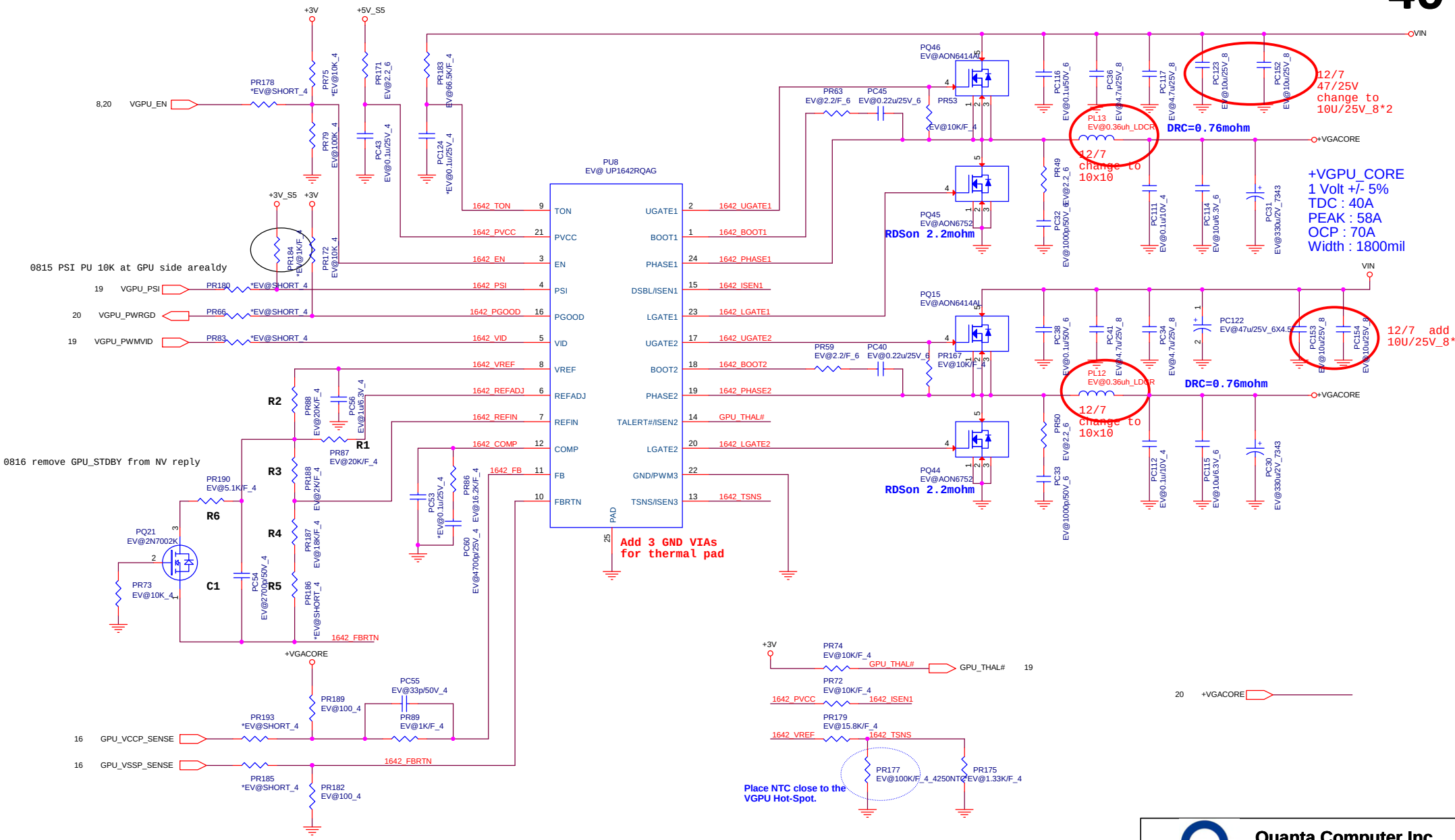
Thermal protection



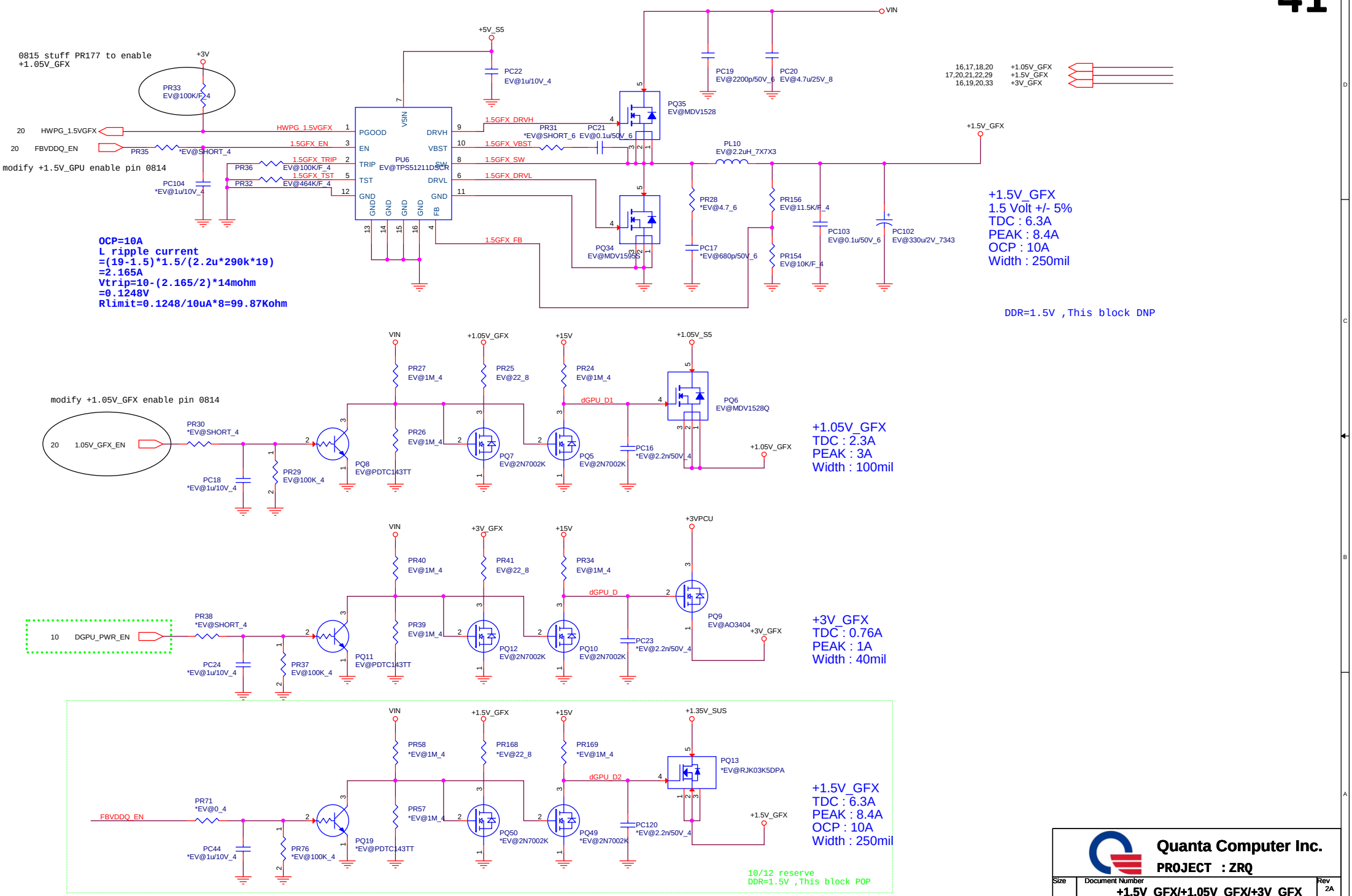


For EC control thermal protection (output 3.3V)

Quanta Computer Inc.			
PROJECT : ZRQ			
Size	Document Number		Rev
	+1.5V/+1.8V/Thermal protect		2A
Date: Friday, April 12, 2013		Sheet 39 of 47	



Quanta Computer Inc.			
PROJECT : ZRQ			
Size	Document Number		Rev
	+VGPU_CORE(UP1642PQAG)		2A
Date:	Friday, April 12, 2013	Sheet 40 of 47	



Quanta Computer Inc.			
PROJECT : ZRQ			
Size	Document Number		Rev
	+1.5V_GFX/+1.05V_GFX/+3V_GFX		2A
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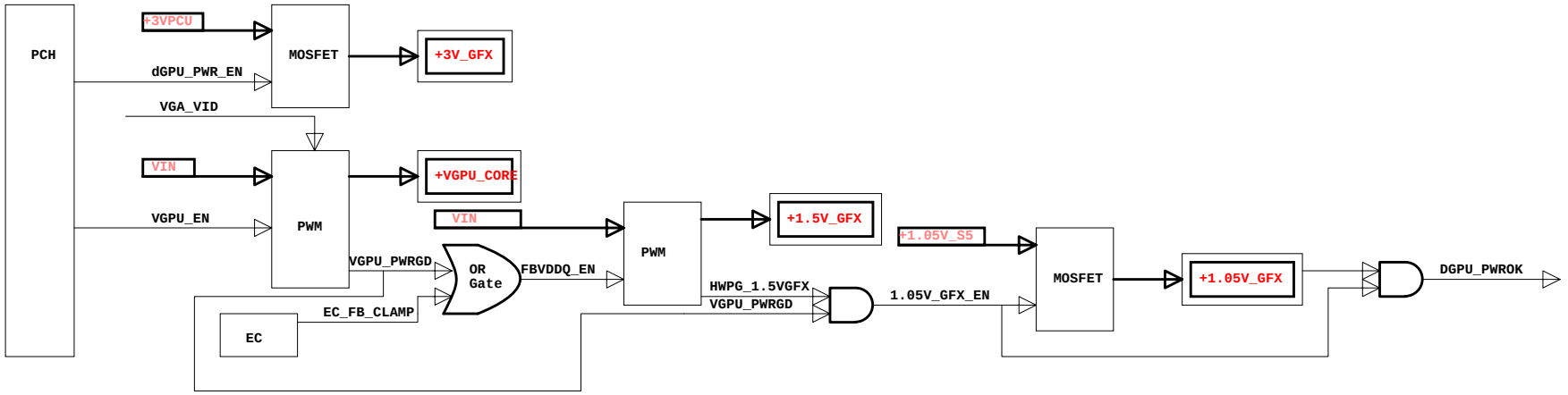
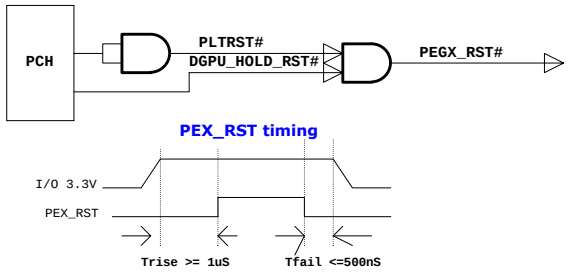
VGA power up sequence



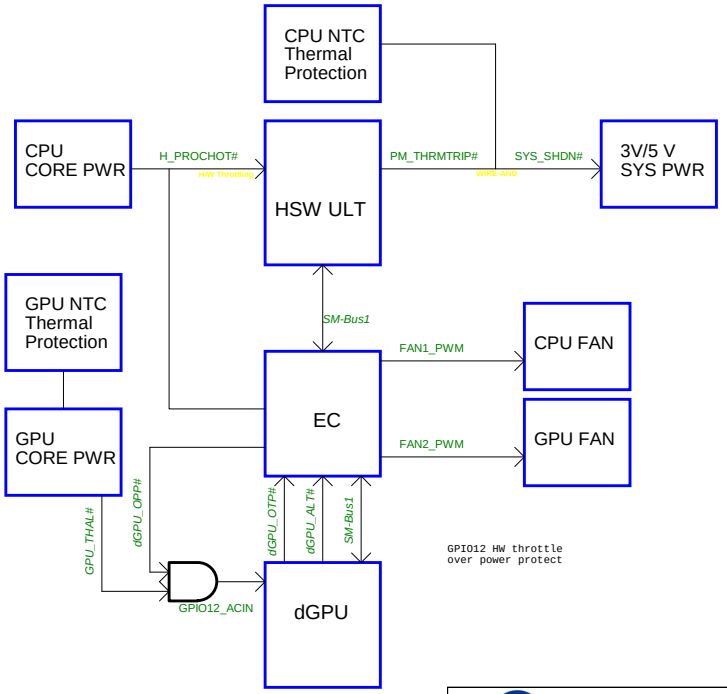
VGA Reset



Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+3V_RTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	USB CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/SPK/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.35VSUS	+1.35V	CPU/SODIMM/MD POWER	SUSON	S0-S3
+DDR_VTT_RUN	+0.675V	SODIMM/MD Termination POWER	MAINON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE VCCST POWER	MAINON	S0
+VCCIN	variation	CPU CORE POWER	VRON	S0
+VGPU_CORE	variation	External GPU POWER	VGPU_EN	S0
+3V_GFX	+3.3V	External GPU POWER	dGPU_PWR_EN	S0
+1.5V_GFX	+1.5V	External GPU POWER	FBVDDQ_EN	S0
+1.05V_GFX	+1.05V	External GPU POWER	1.05V_GFX_EN	S0

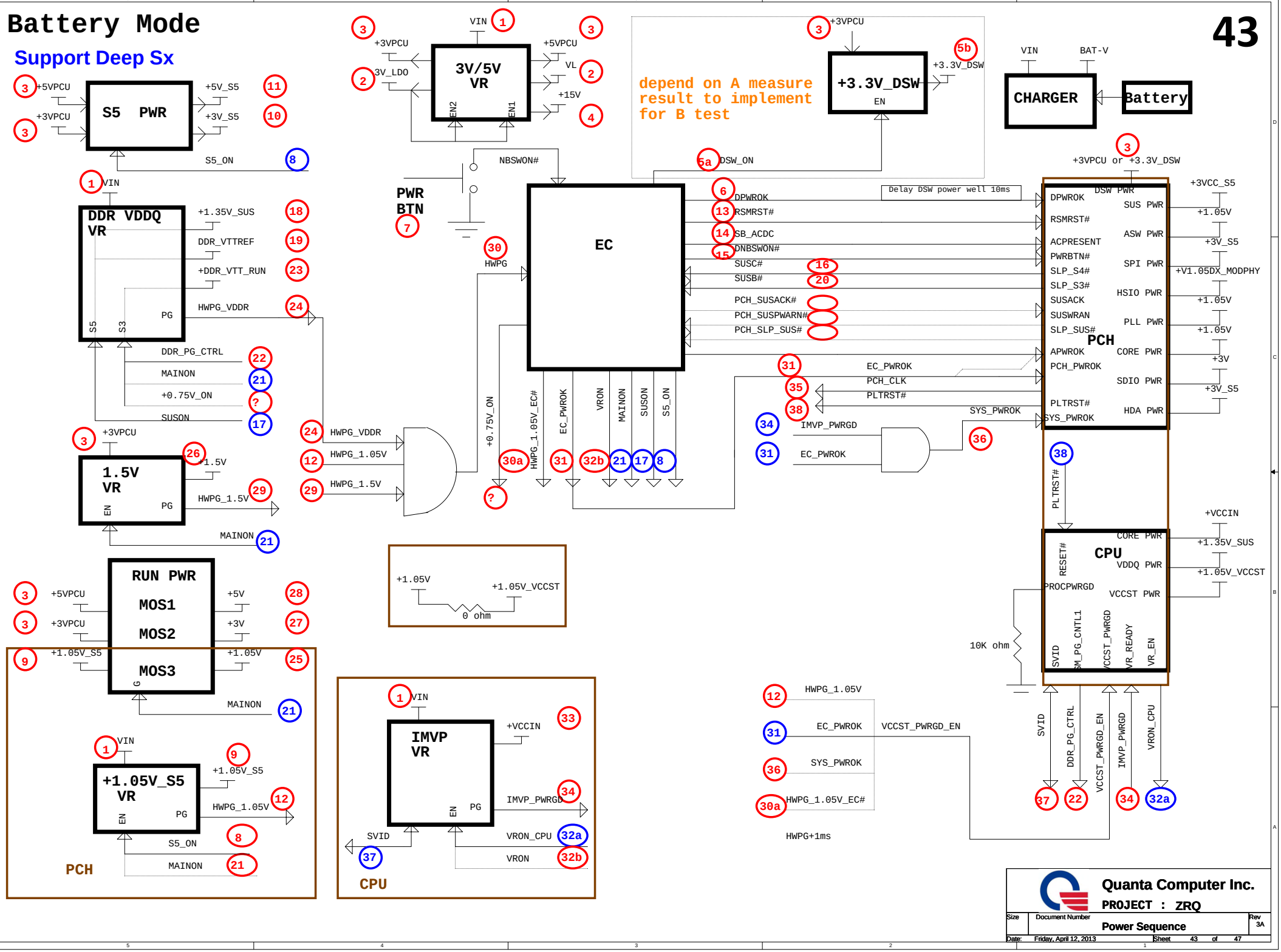
Thermal Follow Chart



dGPU_OPP# EC notify HW throttle over power protect
dGPU_ALT# for ADPS circuit to infrom EC NV dGPU VPS Alert
dGPU_OTP# VGA thrmtrip# => inform EC over temperature protect

Battery Mode

Support Deep Sx



Quanta Computer Inc.	
PROJECT : ZRQ	
Size	Document Number: Power Sequence
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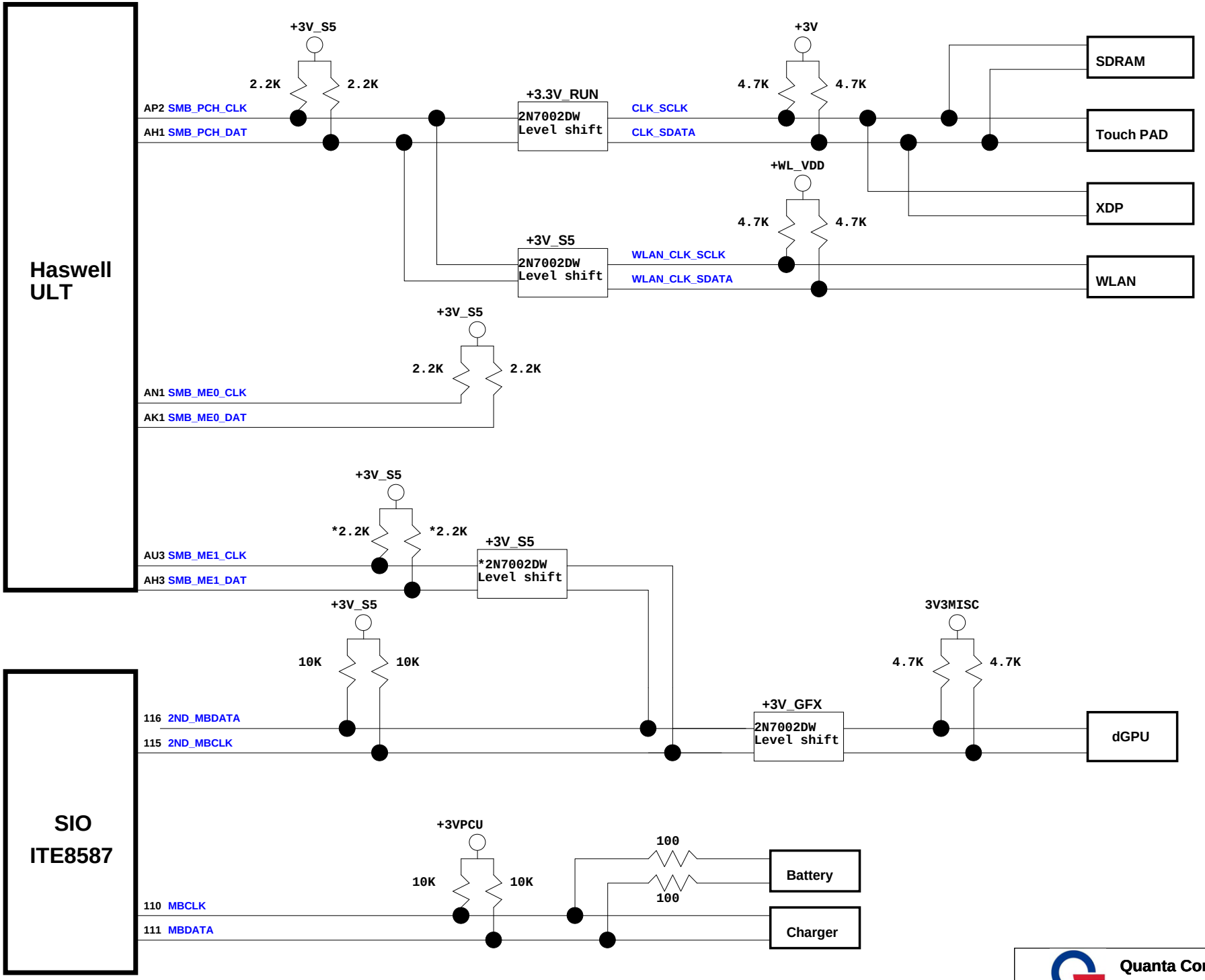

Quanta Computer Inc.

PROJECT : ZRQ

Size	Document Number	Rev
	Block Diagram	3A

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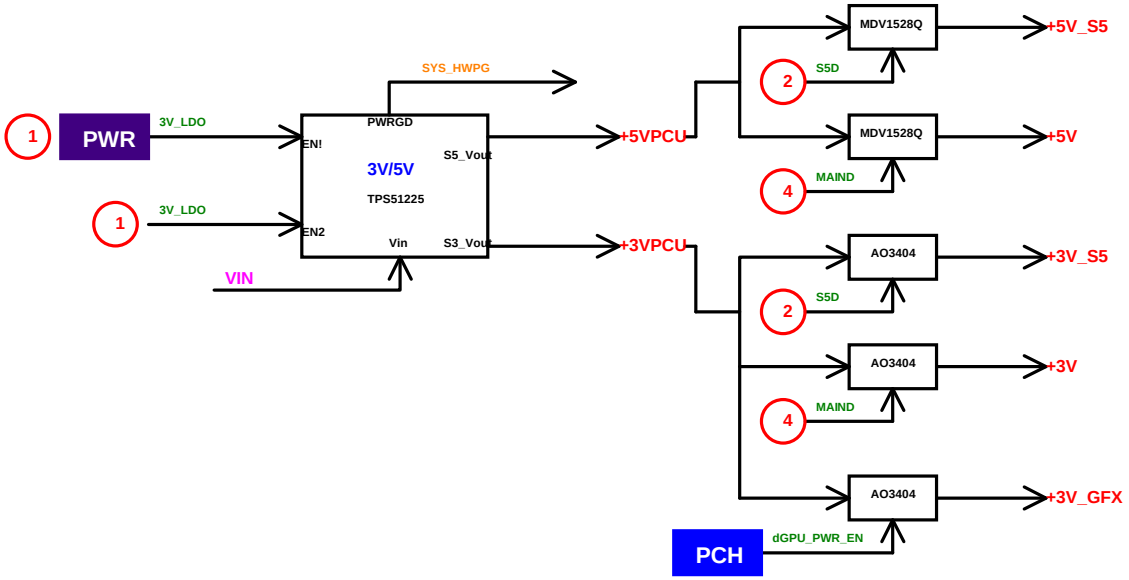

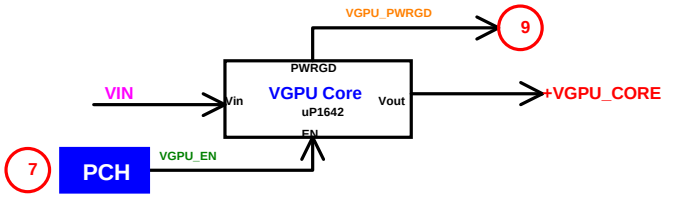

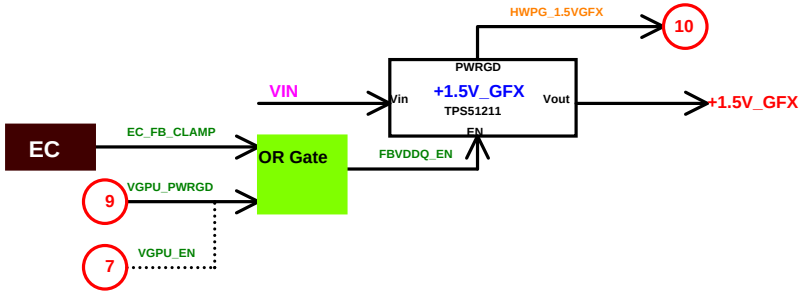

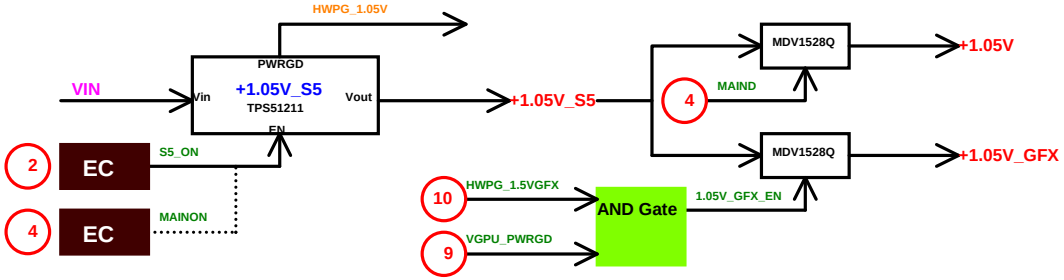

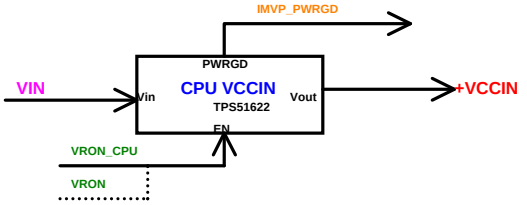

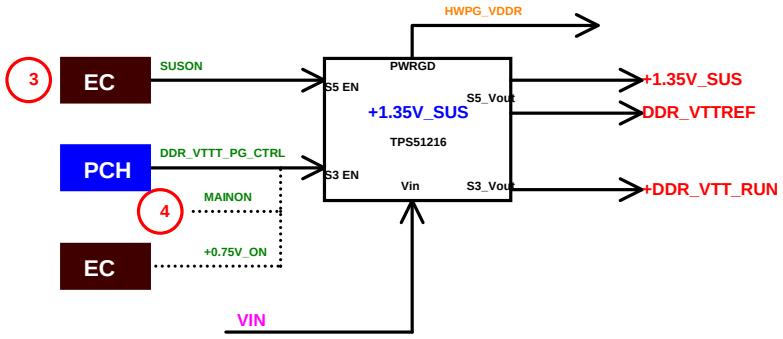

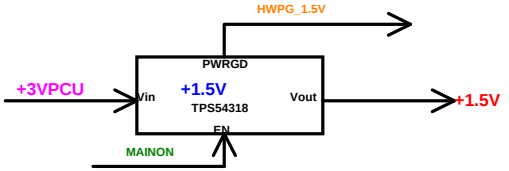

Quanta Computer Inc.
PROJECT : ZRQ

Size	Document Number	Rev
	ULT PWR CONTROL	3A

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Model	Version		CHANGE LIST
ZRQ	1A		
	2A	1	Add R806 Pull down for EDP_HPD(Intel check List).(Page 02)
		2	Add R811 and reserve R809 for Codec Vendor request.(Page 30)
		3	Change R345 footprint from 0402 to 0603.(Page 14)
		4	Change U10 to correct PN AL007534001.(Page 31)
		5	Improve IMVP_PWRGD voltage to low , so del R66,Q9 , R61,Q50 ,R495 and add U55 , C767 , R807. (Page 10)
		6	Change CN12 to 12 PIN connect_DFFC12FR034 (Page 31)
		7	Change SW6 from DHP08TEPV00 to DHPATE2CK03.(Page 29)
		8	Move Hall sensor funtion to USB/B.(Page 24)
		9	Add R828 100K PD for MAINON. Upgrade U27 from AJ085870F02 to AJ085870F03. (Page33)
		10	Collect netname +V1.05S_VCCPCPU to +V3.3S_VCCSDIO. (Page11)
		11	Q7 change from PMF780SN to BAM70020002. (Page25)
		12	Correct U41 footprint to ssop5-p-a-toshiba-b. (Page23)
		13	Change LED5,LED6 P/N from BEB00024ZA0 to BEB00028ZA0. (Page27)
		14	Del Q5, Q47,R51,R25 , add U56,C768 . (Page13)
		15	DEL PL5,PL6,PL7,PL8 . (Page34_power)
		16	Change PR145 from CS28872FB08 to CS29312FB13 . (Page38_Power)
		17	Change PR143 from CS45362FB00 to CS44092FB11 . (Page38_Power)
		18	Change PR129 from CS22672FB12 to CS22702FB14 . (Page38_power)
		19	Change PR5 from CS31002FB26 to CS25762FB01 . (Page38_Power)
		20	Change PR141 from CS32432FB19 to CS32262FB15 . (Page38_Power)
		21	Change PC123 from CC64704MZ10 to CH6104KEA00 . (Page40_Power)
		22	Add PC152,PC153,PC154 to CH6104KEA00 . (Page40_Power)
		23	Change PL12,PL13 from CV+24P0MZ00 to CV+36T0MZ01 10X10 size . (Page40_Power)
		24	SWAP USB0 and USB1 . (Page09)
		25	Change CN27 to DFHS52FR044 ,same as CN18 (Page 26)
		26	add CN12 PIN4 for USBPWR3. (Page 31)
		27	CN9 change frootprint to dp-adis0022-p001a-20p-smt. (Page 23)
		28	Depop R728 and Pop R727 to sove Deep S3 can't wakep issue. (Page 10)
		29	Del C429. (Page20)
		30	Add R826(VRON) ,R827SON) 100k to Gnd. (Page33)
		31	Change CN9 PN to DFTD20FR001 . (Page23)
		32	Add C735_0.1u for Vendor request . (Page28)
		33	Add C736_0.1u and reserve C727_4.7u for Vendor request . (Page29)
		34	Change R348 Pu hign to +3V . (Page28)
		35	TEMP_MBAT from battery connect pin 5 to pin 6 (BATT_EN#) . (Page34)
		36	Change R354(PCH_PWROK) from 10 k to 100K . (Page07)
		37	Reserve R808 ,R810_0 Ohm . (Page30)
		38	Change JP18 Packing and PN same as JP19 . (Page37)
		39	Add R835 for Vendor request. (Page23)
		40	Change R491 from 1M to 5.1M . (Page23)
		41	Change R691 from 121 to 120ohm(Intel Check list) . (Page04)
		42	Change SUSLED# power from +3V_S5 to +3V_PCU . (Page27)
		43	Change CN13 to DFHS40FS047 (H=4) ,due to PE request. Footprint is "gs12401-1011-40p-r-nh-smt. (Page24)
		44	VGPU_PSI Pull high from +3V to +3V_S5. (Page40)
		45	B-SMT USE RTL8411BA-CG need Depop R295 and change U21 PN to AL008411004. (Page28)
		46	C590,C591 change from 18P to 12P(Y6). (Page09)
		47	C278,C284 change from 27P to 12P(Y8). (Page28)
		48	Depop R147,R106,R94,R534 and Pop R91,R95,R146,R533 to support Qual Mode. (Page10)
		49	~~Pop PR104. (Page40_Power)~~ 內部行文
		50	Change PU8 from AL001642000 to AL001642001. (Page40_Power)_內部行文
		51	PC6 EOD Part change to CH4331K9B06. (Page38_Power)
		52	PC5,PC85 EOD Part change to CH21506KB14. (Page38,39_Power)
		53	Change U27 from AJ085870F03 to AJ085870F04. (Page33)_內部行文
		54	~~Add level Shift funtion. (Page25)~~
		55	Depop PR75. (Page40_Power)_內部行文
		56	Change PC15 to 1000p_50V(CH21006JB10). (Page38_Power)_內部行文
		57	Depop PR75. (Page40_Power)_內部行文
	3A	1	Depop R226, Pop Q26(BAM70020002) ,R795 (CS31002FB26) for CG6 funtion.(Page19)
		2	Swap Pin 25 and Pin 32.(Page33)
		3	Del D31,C519 , and Add Q69,C738,C822,C823,C824 for SDA request.(Page23)
		4	Add Test Pad on SW5 ,SW8 for SMT request.(Page27,33)
		5	Add C317_4.7u for Vendor request.(Page28)
		6	SWAP CLKOUT_PCIE.(Page09)
		7	Pop R477, R478, R479, R480 _100ohm(CS31002FB22)for HDMI EMI Issue.(Page25)
		8	Pop C655,C654_10p(CH01006JB08) for SD CLK EMI issue .(Page29)
		9	Pop Bitclk C399_22p(CH02206JB08) for EMI issue .(Page30)
		10	DePop PR117 .(Page34)
		11	C285 change from 0402 to 0603 size .(Page28)
		12	Del CN5,C272,C253 footprint .(Page13)
		13	Depop R336 ,Pop R333 for Lan can't link to exlorer .(Page28)
		14	Depop R348 .(Page28)
		15	Reserve R812 for PCIE_LAN_WAKE# .(Page26)
		16	Add R815,C740 and pop R310 for softstart of Lan VCC.(Page28)
		17	R608 connect to CLK_PCIE_REQ4# .(Page09)
		18	Depop SW5 .(Page33)
		19	Del JP Resistor 0.001/F_3720 (CS+0018FL00): JP5,JP6,JP10,JP11,JP12,JP13,JP14,JP15,JP17,JP18,JP19,JP20,JP21,JP16.
		20	Del 0_4 (CS00002JB38) to SHORT PAD_4 : PR8,PR9,PR11,PR13,PR16,PR18,PR30,PR35,PR38,PR44,PR61,PR66,PR83,PR106, PR131,PR139,PR165,PR170,PR178,PR180,PR185,PR191,PR193,PR194,PR196,PR200,PR204,PR205,PR209,PR211,PR217,PR186
		21	Del 0_6 (CS00003J951) to SHORT PAD_6 : PR31,PR46,PR54,PR77,PR90,PR181,PR201,PR203,PR215,PR158
		22	Del 0_8 (CS00004JA40) to SHORT PAD_8 : PR136
		23	Add R813_0 OHM.(Page26)
		24	Change C740 from 0603 ot 0402 size.(Page28)
		25	Depop Q39 , R276,Pop R321 and change R320 to 1K to meet Lanwake signal spec.(Page28)
			~~Depop L9,L11,L31,L28 , and Pop R34,R47,R49,R55,R490,R487,R485,R481.(Page28)~~
		26	Del JP7, JP8, JP9(CS+001AGM13).(Page05)
		27	Change to 0402 shortpad:R45,R69,R173,R215,R236,R237,R239,R274,R277,R283,R288,R311,R328,R334,R353,R404,R409,R419,R423,R424,R425,R426,R430,R432,R434,R448,R449,R450, R513,R570,R573,R587,R591,R596,R625,R641,R652,R653,R678,R695,R712,R719,R722,R733,R734,R735,R736,R741,R758,R759,R760,R761,R762,R763,R764,R765,
		28	Change to 0603 shortpad:R107,R111,R158,R194,R197,R212,R229,R233,R234,R252,R269,R298,R303,R304,R338,R350,R351,R352,R356,R358,RR411,415,R418,R422,R431,R433,R440,R441, R442,R443,R444,R445,R446,R447,R540,R745,R766,R767
		29	Change to 0805 shortpad:R165,R174,R179,R190,R217,R268,R270,R452,R470,R559,R560,R732,R737,R749
		30	Change R408,R420 from 47 ohm to 56 ohm.(Page30)
		31	Change R411, R422 from shortpad to 0603 footprint.(Page30)

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ZRQ	3B	1 R276 change fro m 10K to 1K , Depop R320. (PCIE_LAN_WAKE#)_內部行文 2 Change C24 KB Conn PN to DFFC26FR063 .(Page 32)_內部行文 3 Change U27 EC to E version AJ085870F05 .(Page 33)_內部行文. 4 Fine tune Amp Gain =>R422,R411 change from 0 ohm to 1k , and pop R421,R410 to 1.62K .(Page 30) 5 Change TEMP_MBAT from Pin 6 to Pin 5 of PJ1 .(Page 34) 6 Depop Q24 , and Add R228 to solve level abnormal issue for CG6 .(Page 19) 7 Add R816 and net "LB_PWR_CNN_Q" to stuff Q69 always for safety issue .(Page 19) 8 Reserve R855,R859 and add R854,R857 .(Page 23) 9 For WHQL Change USB Port1 and Port4 10 Add new on Board RAM HYNIX H5TC4G63AFR-PRBA RAM ID:0000 11 Del L35,L36,L6,L7,L8,L29,L12,L13,L32,L16,L34
	3C	1 Change to 0402 shortpad: R725,R724,R711,R716,R26,R27,R28,R29,R32,R33,R483,R484,R493,R492,R56,R57,R58,R59, R90,R89,R660,R664,R702,R638,R639,R651,R225,R346,R355,R778,R785,R790,R73 , R455,R456,R457,R458,R459,R343,R406,R596 2 For HDMI 7-2 issue change R37,R38,R39,R40,R41,R42,R43,R44 To 470 ohm and remove R478,R479,R477,R480 (Page 25) 3 For TI HD3SS2521 issue R77,R79,R502,R503 need mount 10K, change R528 from 100 ohm to 0 ohm and remove R854,R857 , add R855,R859. (Page 23) 4 Change to 0603 shortpad: R373,R337,R382,R297,R235,R326,R322,L38,R385,R220,R254,R359
	3F	1. Add C245 for intel request for G3 can't boot issue

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