

Compal Confidential

Model Name : Q5LJ1(MA51-HX)

File Name : LA-8203P

BOM P/N:43

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Q5LJ1 M/B Schematics Document

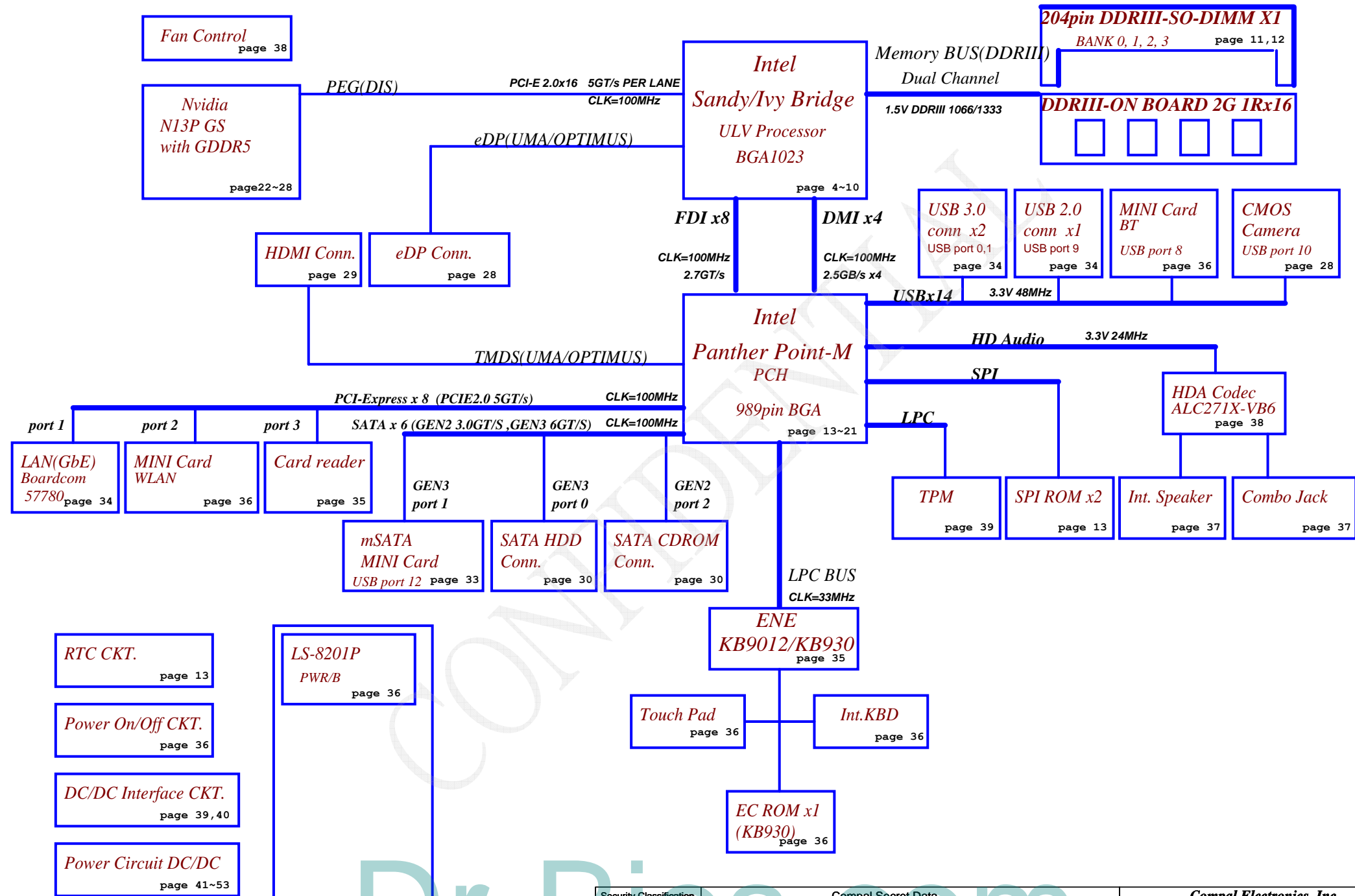
Intel Ivy Bridge ULV Processor + Panther Point PCH
Nvidia N13P-GS

2012-05-08

REV:1.0

Dr-Bios.com

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Issued Date	2011/06/24	Deciphered Date	2012/07/12	Title	SCHEMATIC MB A8203
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Power Rails

Power Plane	Description	AC	AC	AC	AC	DC	DC	DC	DC
		S0	S3	S4	S5	DS3	DS4	DS5	
+RTCVCC	RTC power	ON	ON	ON	ON	ON	ON	ON	
VIN	Adapter power supply (19V)	N/A	ON	ON	ON	OFF	OFF	OFF	
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A	N/A	ON	ON	ON	
B+	AC or battery power rail for power circuit.	ON	ON	ON	ON	ON	ON	ON	
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	OFF	OFF	OFF	OFF	OFF	
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF	OFF	OFF	OFF	OFF	
+VGF_X_CORE	Core voltage for UMA graphic	ON	OFF	OFF	OFF	OFF	OFF	OFF	
+5VALW	+5VALW to +5VALW power rail	ON	ON	ON	ON	ON	ON	ON	
+5VALW_PCH	+5VALW to +5VALW_PCH power rail for PCH	ON	ON	ON	OFF	OFF	OFF	OFF	
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF	OFF	OFF	OFF	OFF	
+3VALW	+3VALW always on power rail	ON	ON	ON	ON	ON	ON	ON	
+3VALW_PCH	+3VALW to +3VALW_PCH power rail for PCH	ON	ON	ON	OFF	OFF	OFF	OFF	
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF	OFF	OFF	OFF	OFF	
+VCCSA	+VCCSA POWER RAIL TO CPU	ON	OFF	OFF	OFF	OFF	OFF	OFF	
+1.8VS	+3VALW to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF	OFF	OFF	OFF	OFF	
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF	OFF	ON	OFF	OFF	
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF	OFF	OFF	OFF	OFF	
+1.05VS_VTT	+1.05VS_VTTP to +1.05VS_VTT switched power rail for CPU	ON	OFF	OFF	OFF	OFF	OFF	OFF	
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF	OFF	OFF	OFF	OFF	
+3V_LAN	LAN CHIP POWER RAIL	ON	ON	ON	ON	OFF	OFF	OFF	
+3VS_WLAN	WLAN MODULE POWER RAIL	ON	OFF*	OFF*	OFF*	OFF	OFF	OFF	
+USB3_VCCA	USB SLEEP CHARGER & PORT0 POWER POWER RAIL	ON*	ON	ON	ON	ON*	ON*	ON*	
+USB3_VCCB/C	USB PORT1/9 POWER POWER RAIL	ON	ON	OFF	OFF	OFF	OFF	OFF	
+3VSDGPU	+3VS to +3VSDGPU power rail	ON**	OFF	OFF	OFF	OFF	OFF	OFF	
+VGA_CORE	Core voltage for GPU	ON**	OFF	OFF	OFF	OFF	OFF	OFF	
+1.5VSDGPU	+1.5V to +1.5VSDGPU switched power rail for GPU	ON**	OFF	OFF	OFF	OFF	OFF	OFF	
+1.05VSDGPU	+1.05VSDGPU switched power rail for GPU	ON**	OFF	OFF	OFF	OFF	OFF	OFF	

Note : ON* WILL DEPEND ON BATTERY CAPACITY TO TURN ON OR OFF

Note : ON** Depend on Optimus ON/OFF.

Note : OFF* Depend on IOAC SPEC support or not.

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3(Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4(Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5(Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	
1	
2	0.1
3	0.2
4	1.0
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure	
Unpop	@	
EC 9012	9012@	
EC 930	930@	
Connector	CONN@	
ALC281	281@	
UMA Only	UMAO@	
OPT	DIS@	
HR CPU I3-2367M	I32367@	P.56
HR CPU I3-2377M	I32377@	P.56
HR CPU I5-2467M	I52467@	P.56
CR CPU I3-3217M	I33217@	P.56
CR CPU I5-3317M	I53317@	P.56
CR CPU I7-3517M	I73517@	P.56
GDDR5 HYNIX MFR	HYNMFR@	X76364BOL03 P.27
GDDR5 HYNIX AFR	HYNAFR@	X76364BOL04 P.27
DRAM	RAM@	for X76 RAM GPIO P.18
DRAM HYNIX	HYNIX@	for X76364BOL11: P.56
DRAM ELPIDA	ELPIDA@	for X76364BOL12: P.56
VRAM X76	VRAM@	MB VRAM X76 P.56
DRAM X76	DRAM@	MB DRAM X76 P.56

EC SM Bus1 address

Device	Address
Smart Battery	0001_011X b

EC SM Bus2 address

Device	Address
On Board Thermal Sensor	1001_101xb

PCH SM Bus address

Channel	DIMMO	A0	Address	JDIMM1(SPD)
ChannelA	DIMMO	A4	1010_000X	On Board RAM(SPD)
ChannelB	DIMMO	A4	1010_010X	

CPU BOM Config

I32367@	I3-2367M	HR	1.4G	SA000051H60(S IC AV8062701047904 SR0CV J1 1.4G ABOI)
I32377@	I3-2377M	HR	1.5G	SA00005MX10(S IC AV8062701048004 QAXQ J1 1.5G BGA)
I52467@	I5-2467M	HR	1.6G	SA00004X010(S IC AV8062701047504 SR0D6 J1 1.6G ABOI)
I33217@	I3-3217U	CR	1.8G	SA00005L5C0(S IC AV8063801058401 SR0N9 L1 1.8G BGA 1023 ABO I)
I53317@	I5-3317U	CR	1.7G	SA00005K6B0(S IC AV8063801058002 SR0N8 L1 1.7G ABO I)
I73517@	I7-3517U	CR	1.9G	SA00005K5B0(S IC AV8063801057605 SR0N6 L1 1.9G BGA 1023 ABO I)

GPU BOM Config + GPIO

N13P-GS-A2	R3	SA0000518A0(S IC N13P-GS-A2 FCBGA 908P GPU ABO I)
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VRAM BOM Config

X76364BOL03:	1G HYN	GDDR5	64*32	2G	SA00004GD30(S IC D5 64M32/2.5G H5GQ2H24MFR-T2C ABOI)	HYNMFR@/
X76364BOL04:	1G HYN	GDDR5	64*32	2G	SA00004GD50(S IC D5 64M32/2.5G H5GQ2H24AFR-T2C ABOI)	HYNAFR@/

RAM BOM Config

X76364BOL11:	2GB*4 HYNIX	HYNIX	2GB	1333	SA00005FV10(S IC D3 256MX16/1333 H5TC4G63MFR-H9A FBGA 96P ABO I)	RAM@//HYNIX@/
X76364BOL12:	2GB*4 ELPIDA	ELPIDA	2GB	1333	SA000059110(S IC D3 256M16 EDJ4216EBBG-DJ-F ABO I)	RAM@//ELPIDA@/

BOM Config

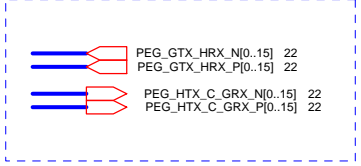
LA8203 UMA :	9012@/UMAO@/DRAM@/	+CPU config
LA8203 Optimus :	9012@/DIS@/DRAM@/VRAM@/	+CPU config

USB Port Table

USB 2.0	Port	3 External USB Port
EHCI1	0	USB Port(Right 2.0),USB Charger
	1	USB Port(Mid 2.0)
	2	
	3	
	4	
	5	
	6	
EHCI2	8	BT (WLAN)
	9	USB port(Left 2.0)
	10	Camera
	11	Mini Card(MSATA)
	12	
	13	

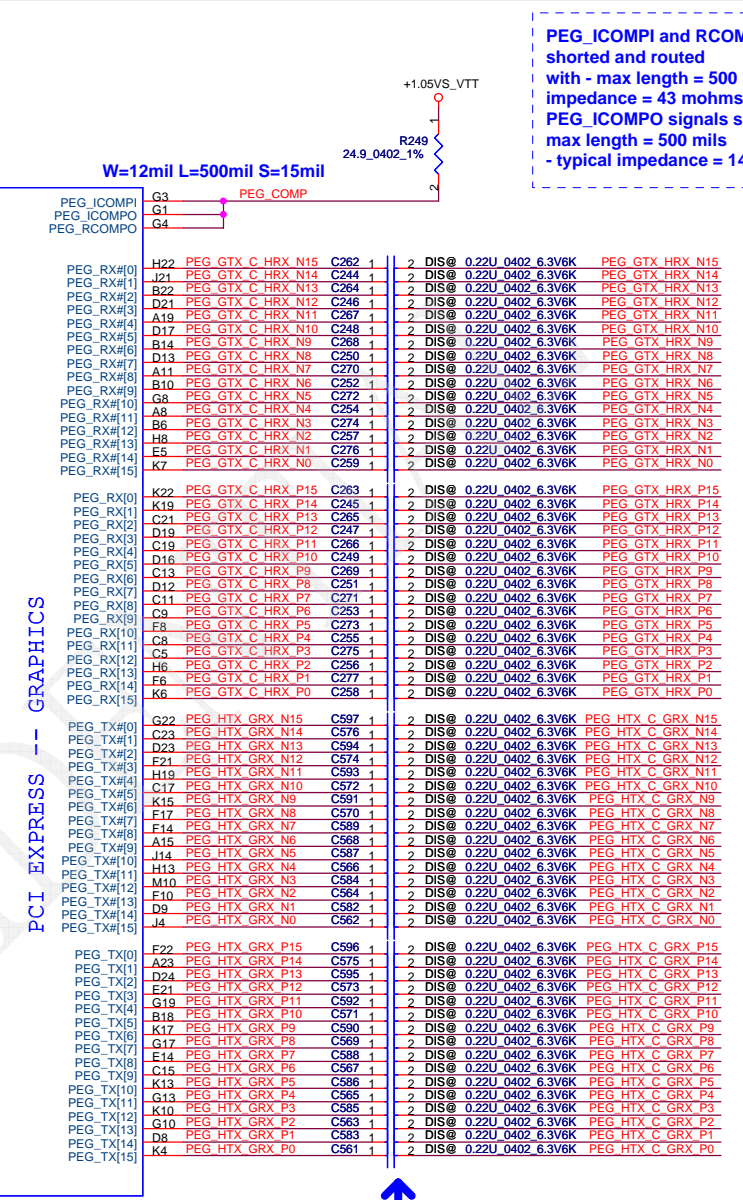
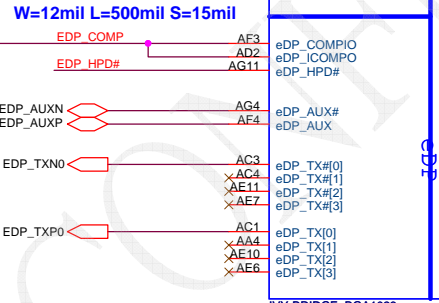
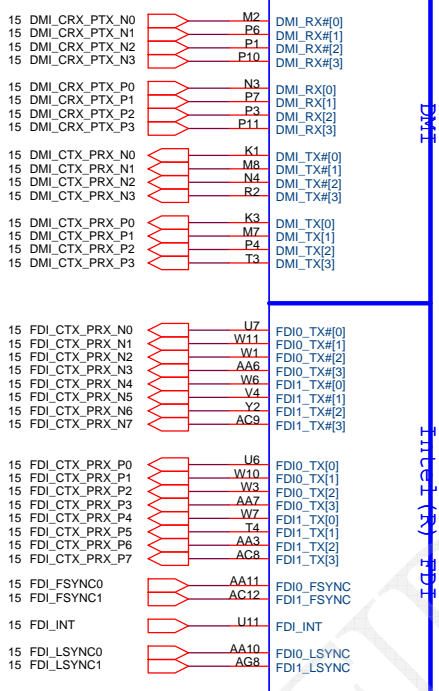
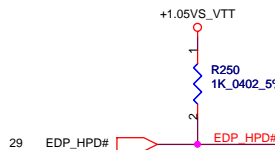
USB 3.0	Port	
XHCI	1	USB Port(Right 3.0)
	2	USB Port(Mid 3.0)
	3	
	4	

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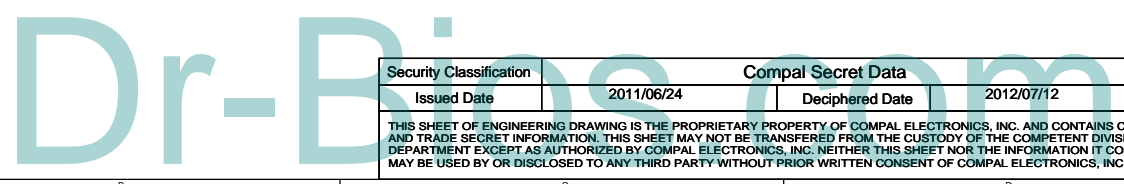
eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms ,even if disable eDP function...

Add eDP circuit



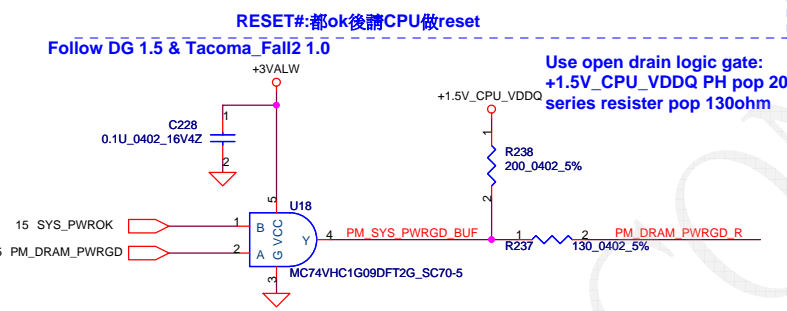
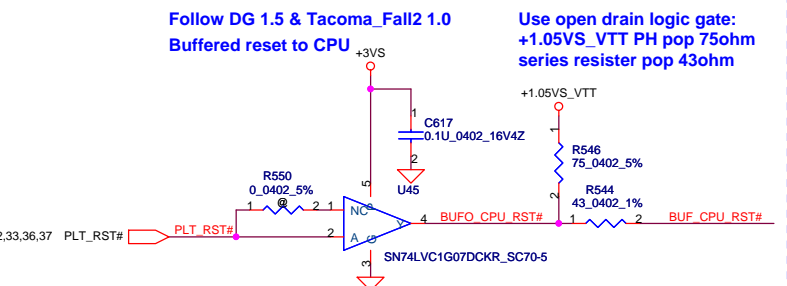
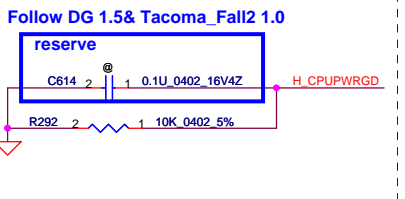
PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
 PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

Typ- suggest 220nF. The change in AC capacitor value from 100nF to 220nF is to enable compatibility with future platforms having PCIe Gen3 (8GT/s)



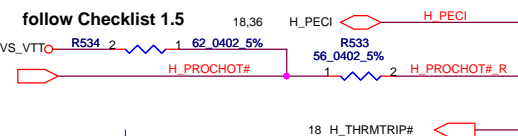
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PCH->CPU
 UNCOREPWRGOOD:非CORE外的電OK
 SM_DRAMPWROK:DRAM power ok
 RESET#:都ok後請CPU做reset

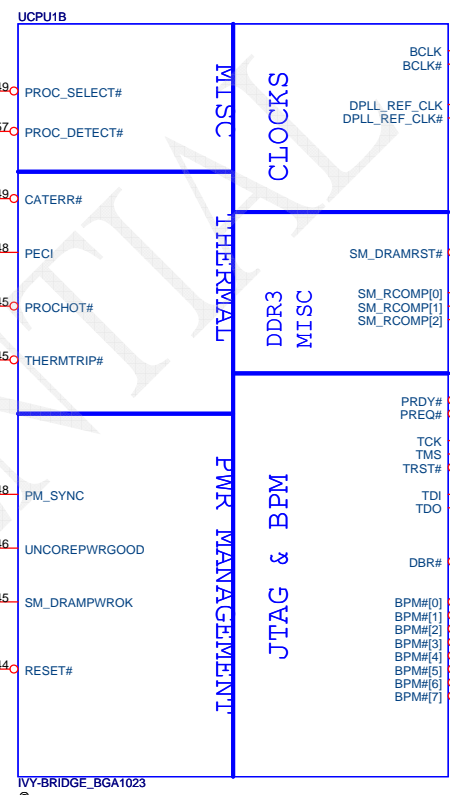


PROC_SELECT#
 PH VCPLL and connect to PCH DF_TV5

偵測CPU有無安裝
 XBOX 三紅功能



UNCOREPWRGOOD:非CORE外的電OK
 SM_DRAMPWROK:DRAM power ok



0921 LVDS->@

CLK_CPU_DPLL# R517 2 1K 0402 5%
 CLK_CPU_DPLL R516 2 1K 0402 5%

Checklist1.5 P.67 Graphis Disable Guide
 DIS only SKU eDP disable
 DPLL_REF_SSCLK PD 1K 5% to GND
 DPLL_REF_SSCLK# PH 1K 5% to +1.05VS_VTT

SM_RCOMP0,SM_RCOMP1
 W=20mil L=500mil S=13mil

SM_RCOMP2
 W=15mil L=500mil S=13mil

SM_DRAMRST# AT30 SM_DRAMRST# SM_DRAMRST# 6

SM_RCOMP0 R272 2 140 0402 1%
 SM_RCOMP1 R273 2 25.5 0402 1%
 SM_RCOMP2 R267 2 200 0402 1%

DDR3 Compensation Signals

PRDY# N53 X
 PREQ# N55 X

TCK L56 XDP TCK PAD T19
 TMS L55 XDP TMS PAD T20
 TRST# J58 XDP TRST# PAD T21

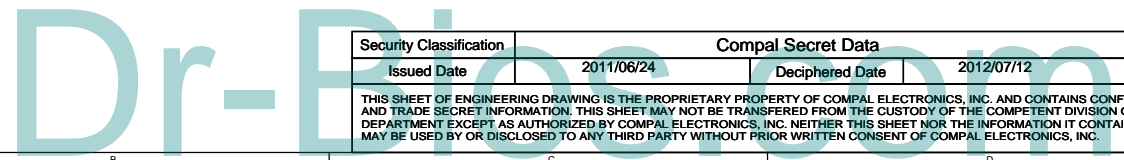
TDI M60 XDP TDI PAD T34
 TDO L59 XDP TDO PAD T35

DBR# K58 XDP DBRESET# XDP_DBRESET# 15

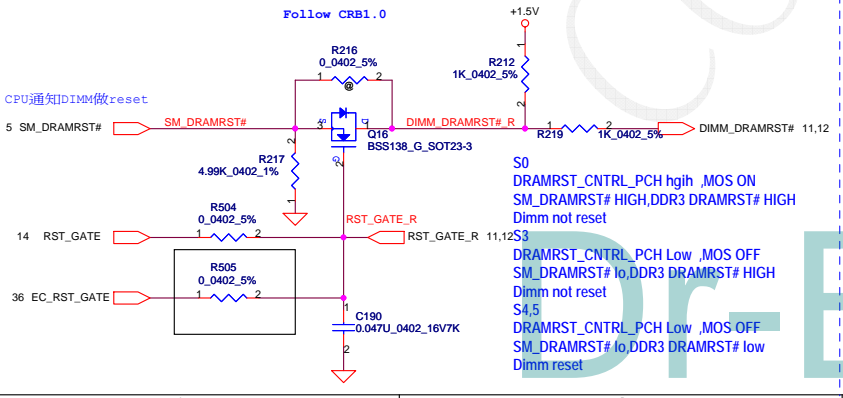
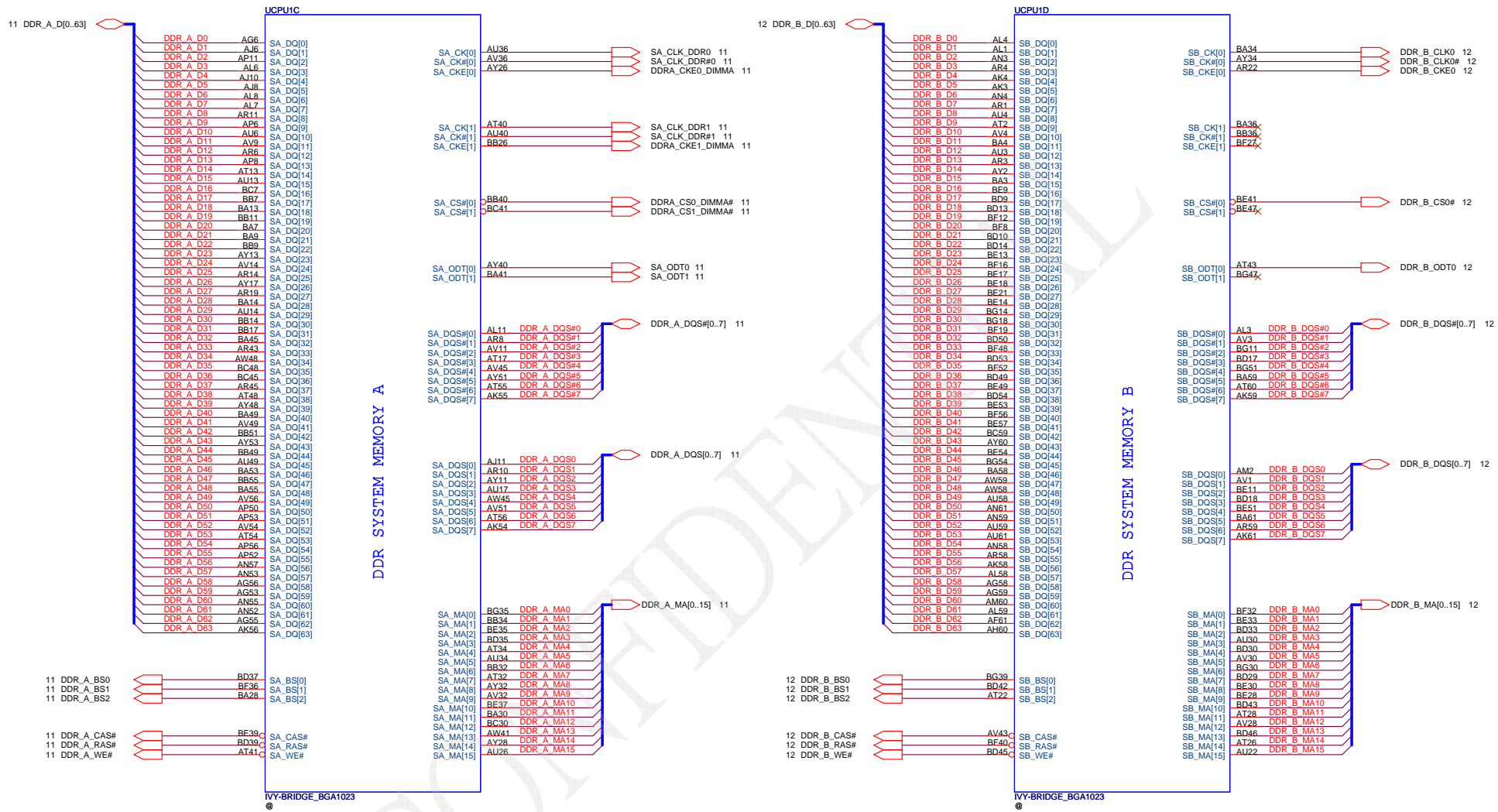
BPM#0 G58 X
 BPM#1 E55 X
 BPM#2 E59 X
 BPM#3 G55 X
 BPM#4 G59 X
 BPM#5 H60 X
 BPM#6 J59 X
 BPM#7 J61 X

XDP_DBRESET# R312 2 1K 0402 5%

Tacoma_Fall2 1.0 PH 1K +3VS
 Check list 1.5 PH 1K +3VS
 Debug port DG1.1-1.3 50-5K ohm



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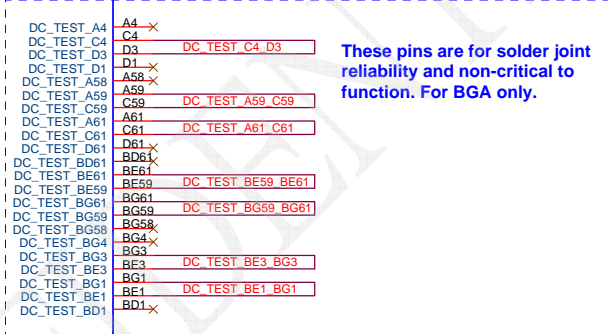
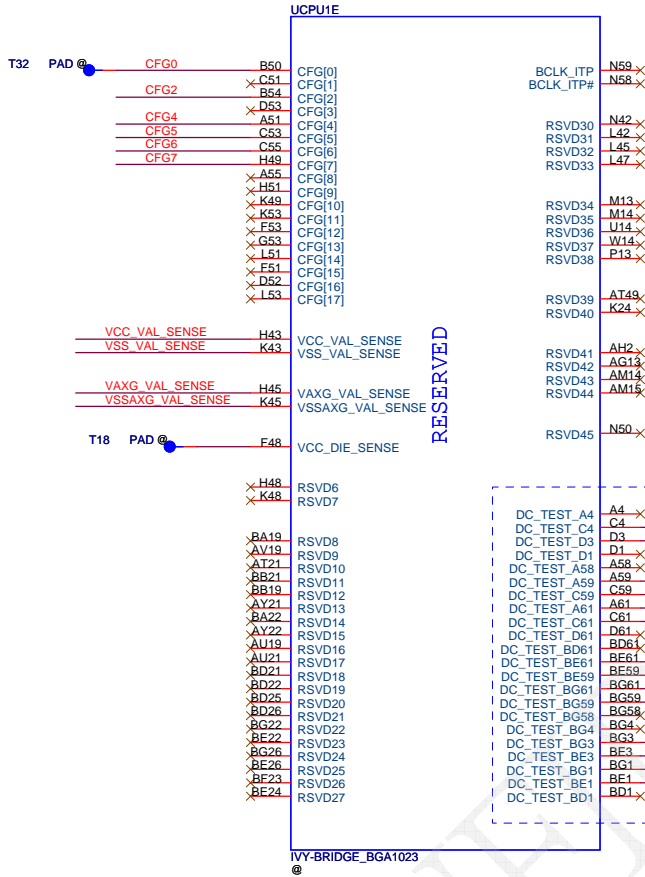
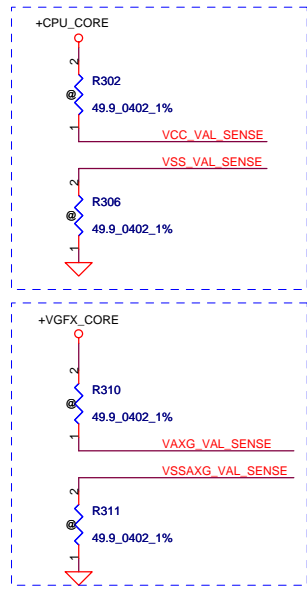
S0
 DRAMRST# CNTRL_PCH hgihh_MOS ON
 SM_DRAMRST# HIGH,DDR3 DRAMRST# HIGH
 Dimm not reset

S3
 DRAMRST# CNTRL_PCH Low_MOS OFF
 SM_DRAMRST# lo,DDR3 DRAMRST# HIGH
 Dimm not reset

S4,S5
 DRAMRST# CNTRL_PCH Low_MOS OFF
 SM_DRAMRST# lo,DDR3 DRAMRST# low
 Dimm reset

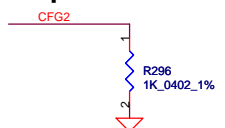
Address 0~13:For 128*16
 Address 0~14:For 256*16
 Address 0~15:For 512*16

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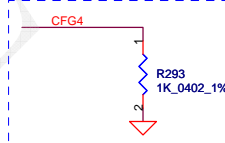


These pins are for solder joint reliability and non-critical to function. For BGA only.

CFG Straps for Processor

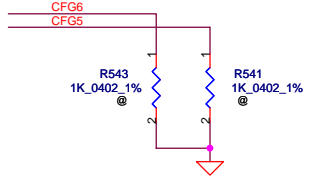


PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed

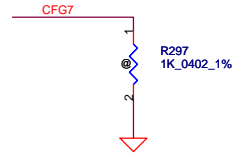


UMA, Optimus eDP 启动
DISO eDP 關閉

eDP enable	
CFG4	1: Disable * 0: Enable



PCIe Port Bifurcation Straps	
CFG[6:5]	*11: (Default) 1x16 PCI Express 10: 2x8 PCI Express 01: Reserved 00: 1x8, 2x4 PCI Express



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

Dr-B...
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INTEL Recommend VCC
4*470UF,12*22uF(0805) and 35*2.2uF(0402)
PD0.8
CAP at P.51

INTEL Recommend VCCIO
2*330UF,10*10uF(0603) and 26*1uF(0402)
PD0.8
CAP at P.51

POWER

ULV type
DC 33A

UCPU1F

8.5A

- A26 VCC[1]
- A29 VCC[2]
- A31 VCC[3]
- A34 VCC[4]
- A36 VCC[5]
- A38 VCC[6]
- A39 VCC[7]
- A42 VCC[8]
- C26 VCC[9]
- C27 VCC[10]
- C32 VCC[11]
- C34 VCC[12]
- C37 VCC[13]
- C39 VCC[14]
- C42 VCC[15]
- D27 VCC[16]
- D32 VCC[17]
- D34 VCC[18]
- D37 VCC[19]
- D39 VCC[20]
- D42 VCC[21]
- E26 VCC[22]
- E28 VCC[23]
- E32 VCC[24]
- E34 VCC[25]
- E37 VCC[26]
- E38 VCC[27]
- F25 VCC[28]
- F26 VCC[29]
- F28 VCC[30]
- F32 VCC[31]
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- H29 VCC[39]
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- H40 VCC[45]
- J25 VCC[46]
- J26 VCC[47]
- J28 VCC[48]
- J29 VCC[49]
- J32 VCC[50]
- J34 VCC[51]
- J35 VCC[52]
- J37 VCC[53]
- J38 VCC[54]
- J40 VCC[55]
- J42 VCC[56]
- K26 VCC[57]
- K27 VCC[58]
- K29 VCC[59]
- K32 VCC[60]
- K34 VCC[61]
- K35 VCC[62]
- K37 VCC[63]
- K39 VCC[64]
- K42 VCC[65]
- L25 VCC[66]
- L28 VCC[67]
- L33 VCC[68]
- L36 VCC[69]
- L40 VCC[70]
- N26 VCC[71]
- N30 VCC[72]
- N34 VCC[73]
- N37 VCC[74]
- N38 VCC[75]
- N39 VCC[76]

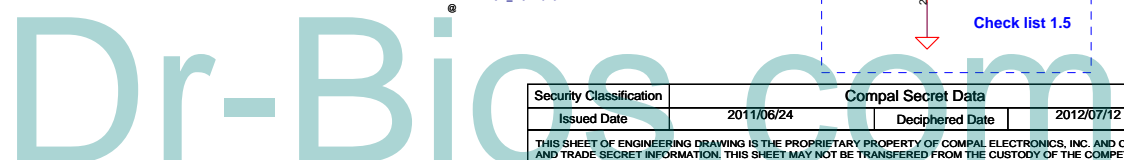
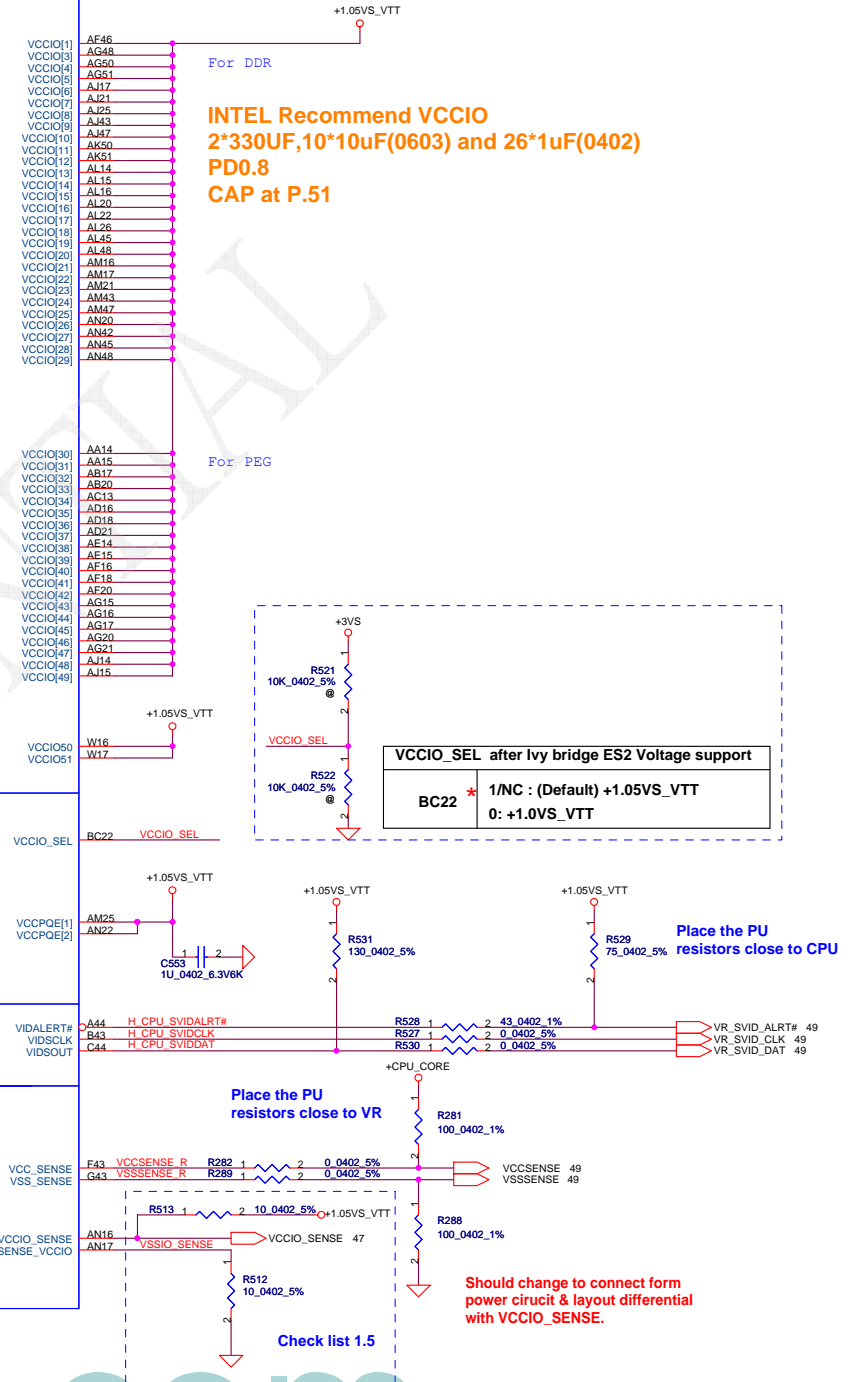
CORE SUPPLY

PEG IO AND DDR IO

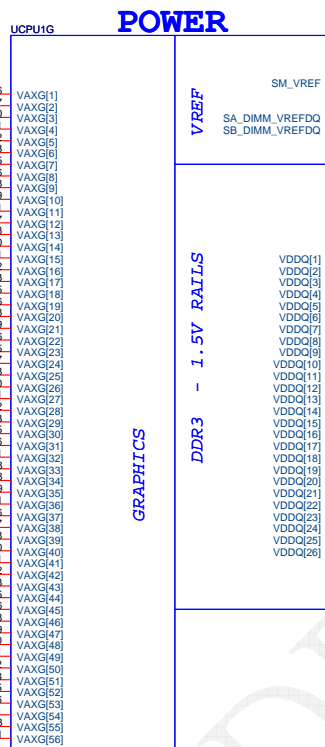
QUIET RAILS

SVID

SENSE LINES



INTEL Recommend VAXG
2*470uF,6*22uF(0805) and 6*10uF(0603)
11*1U(0402)
PD0.8



POWER

1.5V RAILS

1.8V RAIL

SA RAIL

VCCSA VID Lines

IY:BRIDGE_BGA1023

+V_SM_VREF should have 20 mil trace width

INTEL Recommend VDDQ
1*330uF,8*10uF(0603),10*1uF(0402)
PD0.8

Place TOP IN BGA

Place BOT OUT BGA

SGA20331E10 S POLY C 330U 2V Y D2 LESR9M EEF5X H1.9

INTEL Recommend VCCPLL
1*330uF,2*1uF(0402)
PD0.8

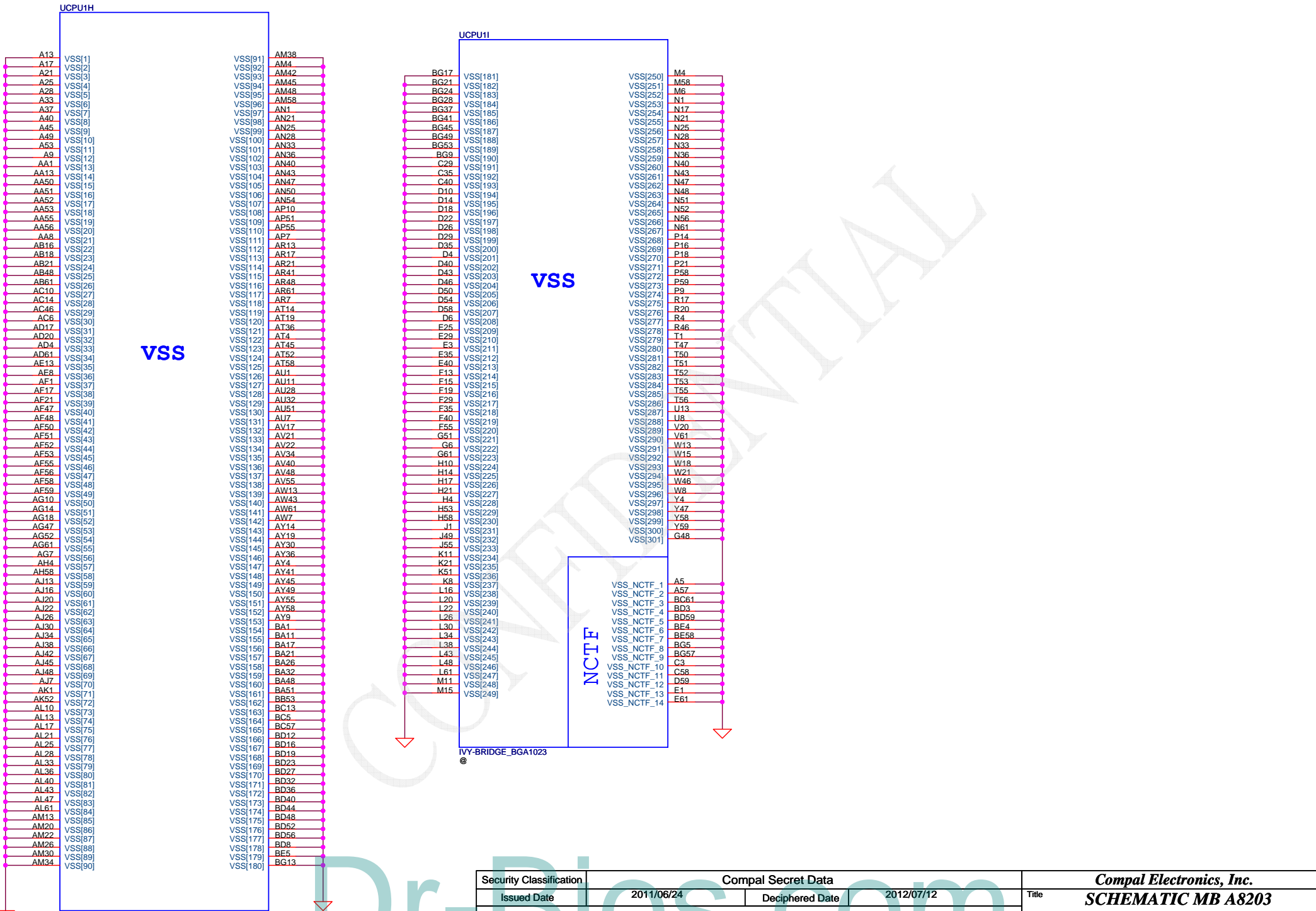
CR CheckList Rev1.5

SGA00001700 S POLY C 220U 220U 2.5V M B2 ESR35 TPE H1.9

SGA20331E10 S POLY C 330U 2V Y D2 LESR9M EEF5X H1.9

INTEL Recommend VCCSA
1*330uF,5*10uF(0603),5*1uF(0402)
PD0.8

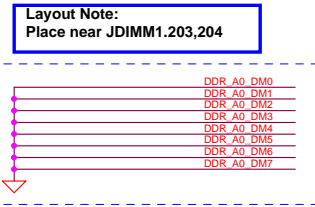
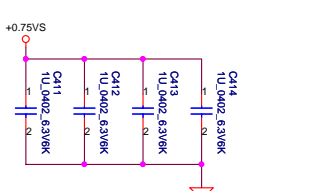
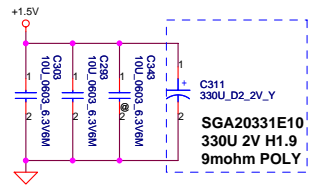
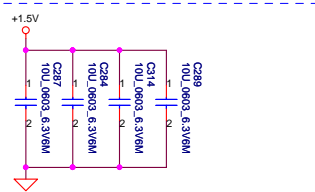
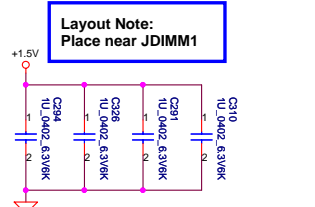
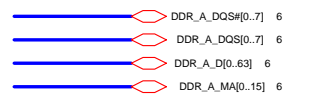
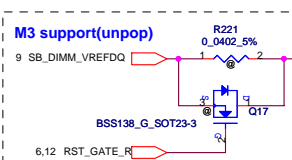
VCCSA				
VID0	VID1	Vout	HR	CR
0	0	0.9V	V	V
0	1	0.85V	V	V
1	0	0.775V	X	V
1	1	0.75V	X	V



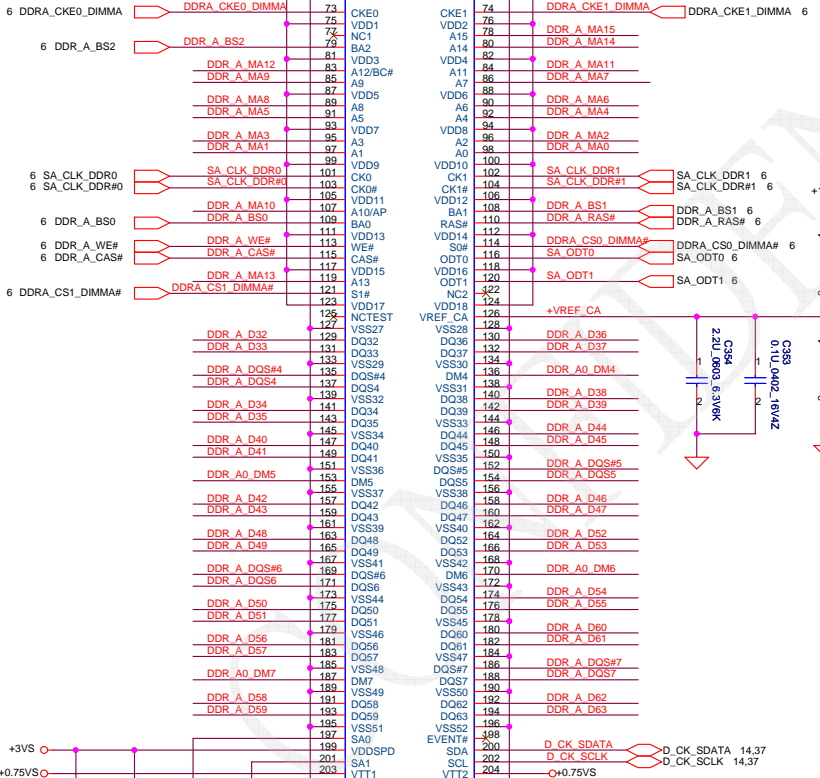
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Issued Date		Deciphered Date		4019J1	
2011/06/24		2012/07/12		Thursday, June 14, 2012	
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Compal Electronics, Inc.
SCHEMATIC MB A8203

Document Number
4019J1
Rev C

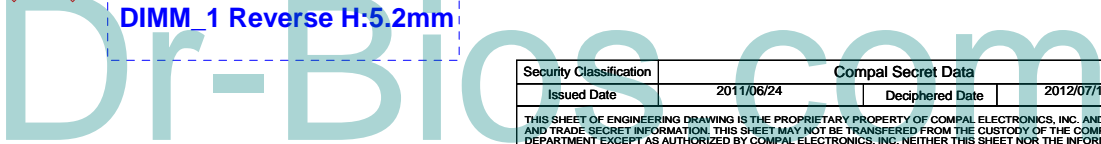


All VREF traces should have 10 mil trace width

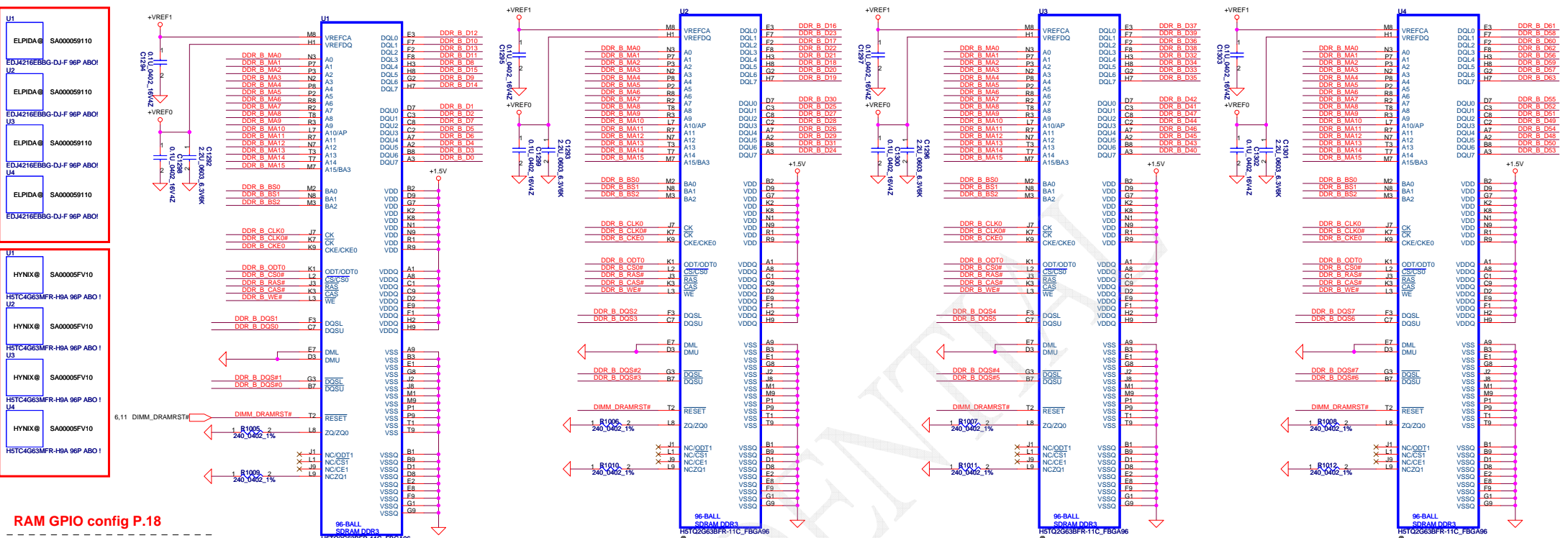


Channel A

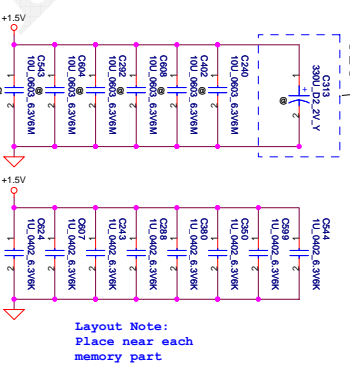
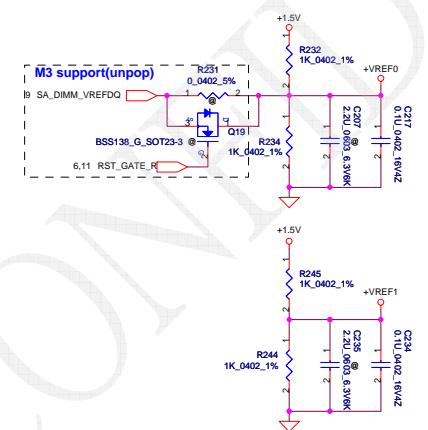
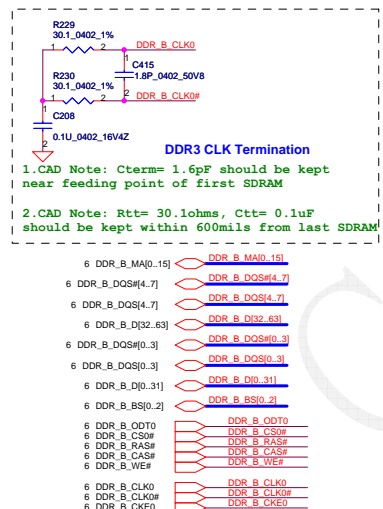
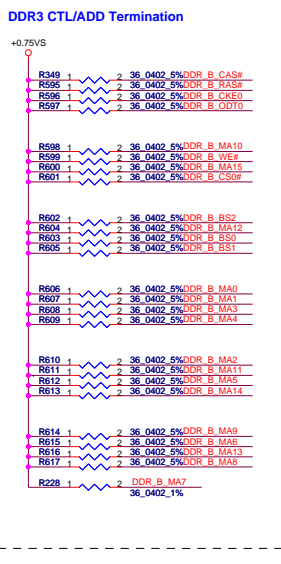
<Address: SA1:SA0=00>
DIMM 1 Reverse H:5.2mm



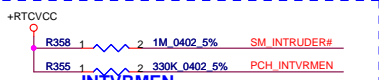
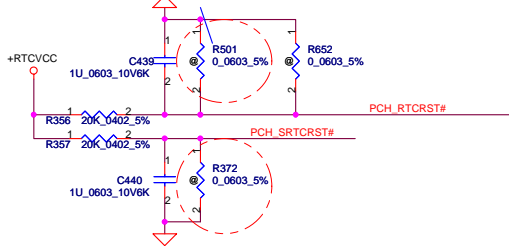
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RAM GPIO config P.18

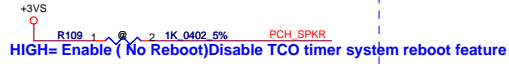


RTC/ST close RAM door J1



INTVRMEN

★ **H** : Integrated VRM enable
L : Integrated VRM disable
 (INTVRMEN should always be pull high.)



HIGH= Enable (No Reboot)Disable TCO timer system reboot feature

★ **LOW= Disable (Default internal PD)**



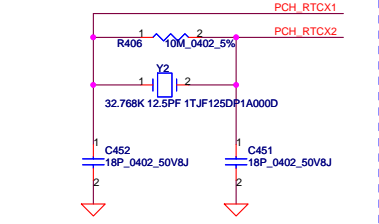
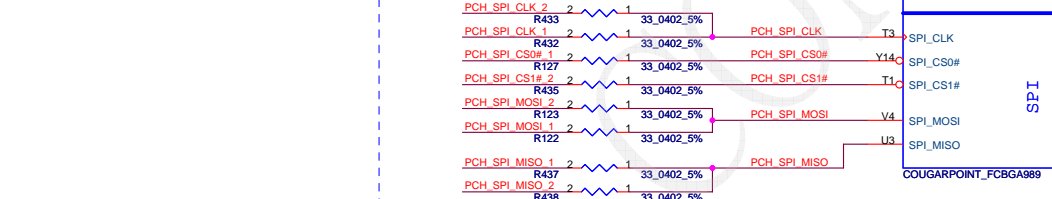
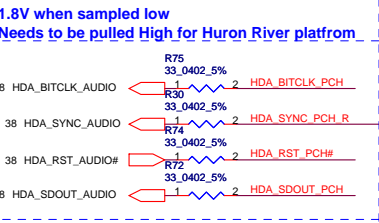
HDA_SDO
 ME debug mode this signal has a weak internal PD
 ★ **Low = Disabled (Default)**
High = Enabled (Flash Descriptor Security Override)



This signal has a weak internal pull-down

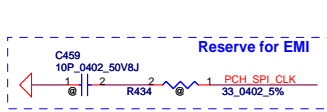
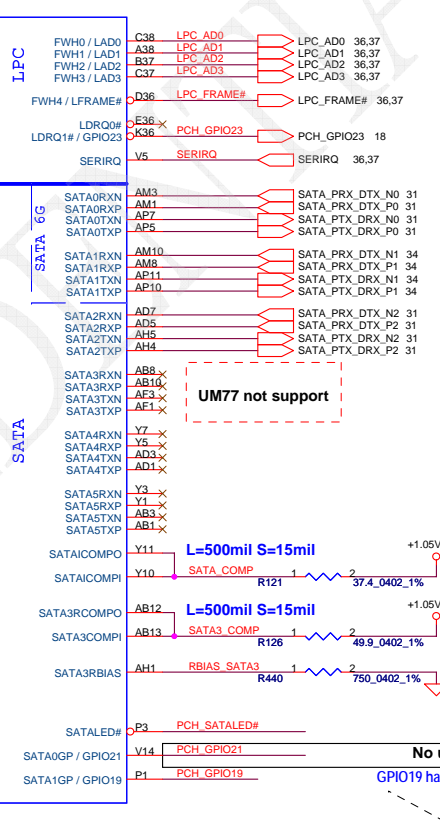
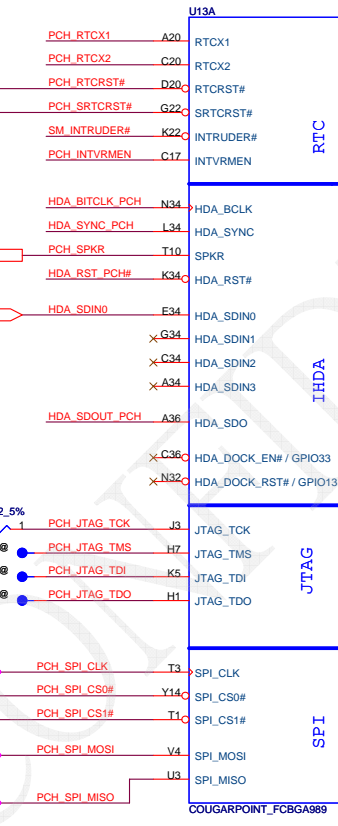
On Die PLL VR Select is supplied by
 ★1.5V when sampled high
 1.8V when sampled low
 Needs to be pulled High for Huron River platform

Prevent back drive issue.

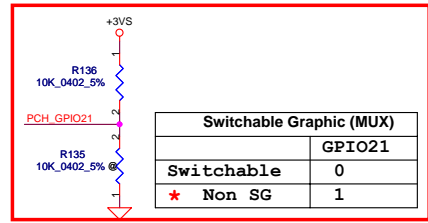
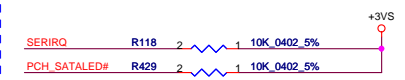
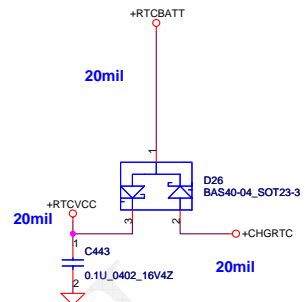


SPI ROM FOR ME (4MB)
 Footprint 200mil

SPI ROM FOR ME (2MB)
 Footprint 200mil



Reserve for EMI



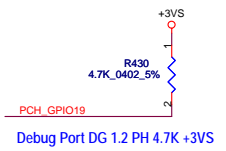
Switchable Graphic (MUX)	
Switchable	0
★ Non SG	1

L=500mil S=15mil

L=500mil S=15mil

No use PH 10K +3VS

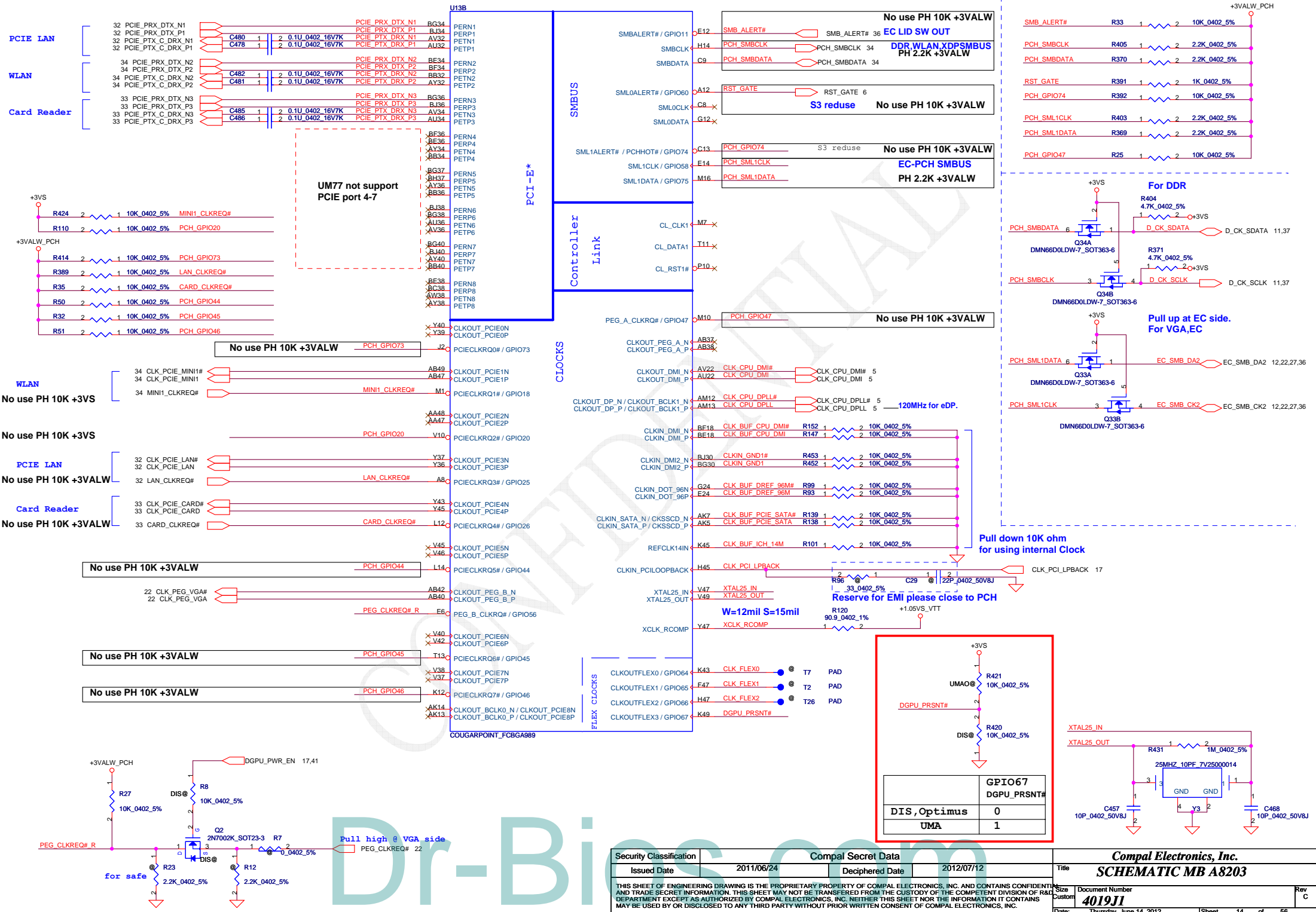
GPIO19 has internal Pull up



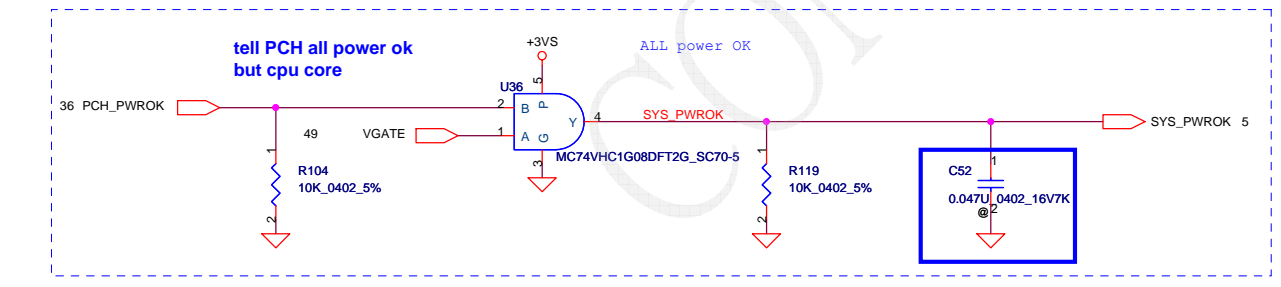
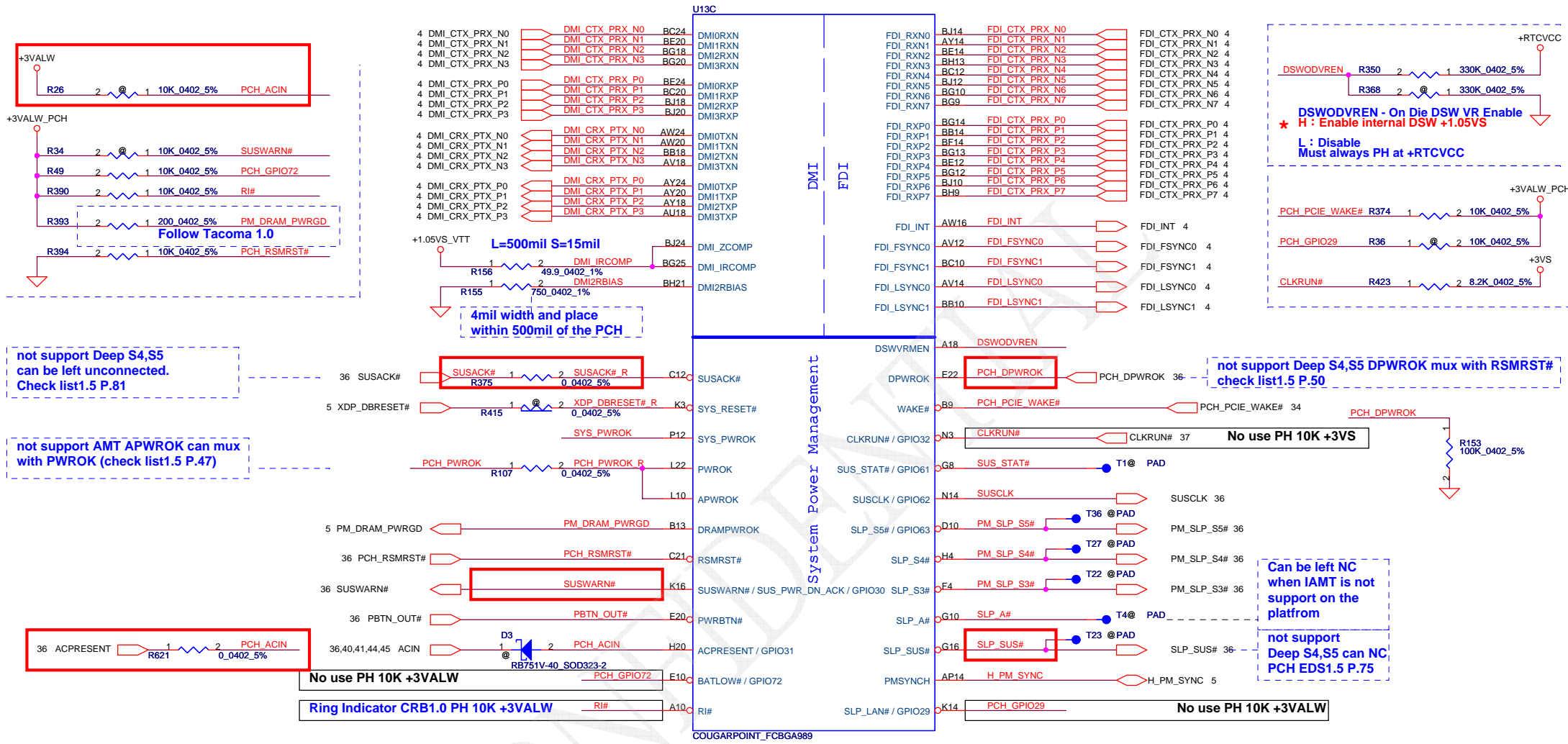
Debug Port DG 1.2 PH 4.7K +3VS

Boot BIOS Strap		
Boot BIOS	GPIO51	GPIO19
LPC	0	0
Reserved	0	1
-	1	0
★ SPI	1	1

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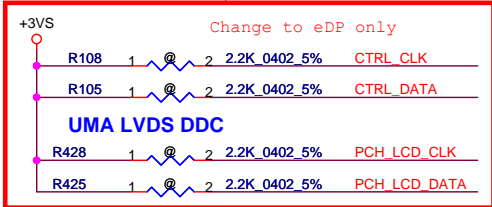
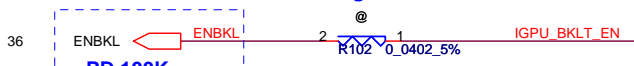
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				4019JI	C
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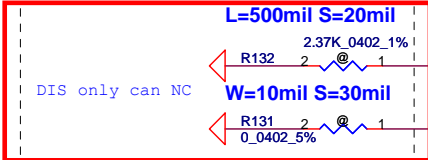
UMA Panel Backlight ON/OFF



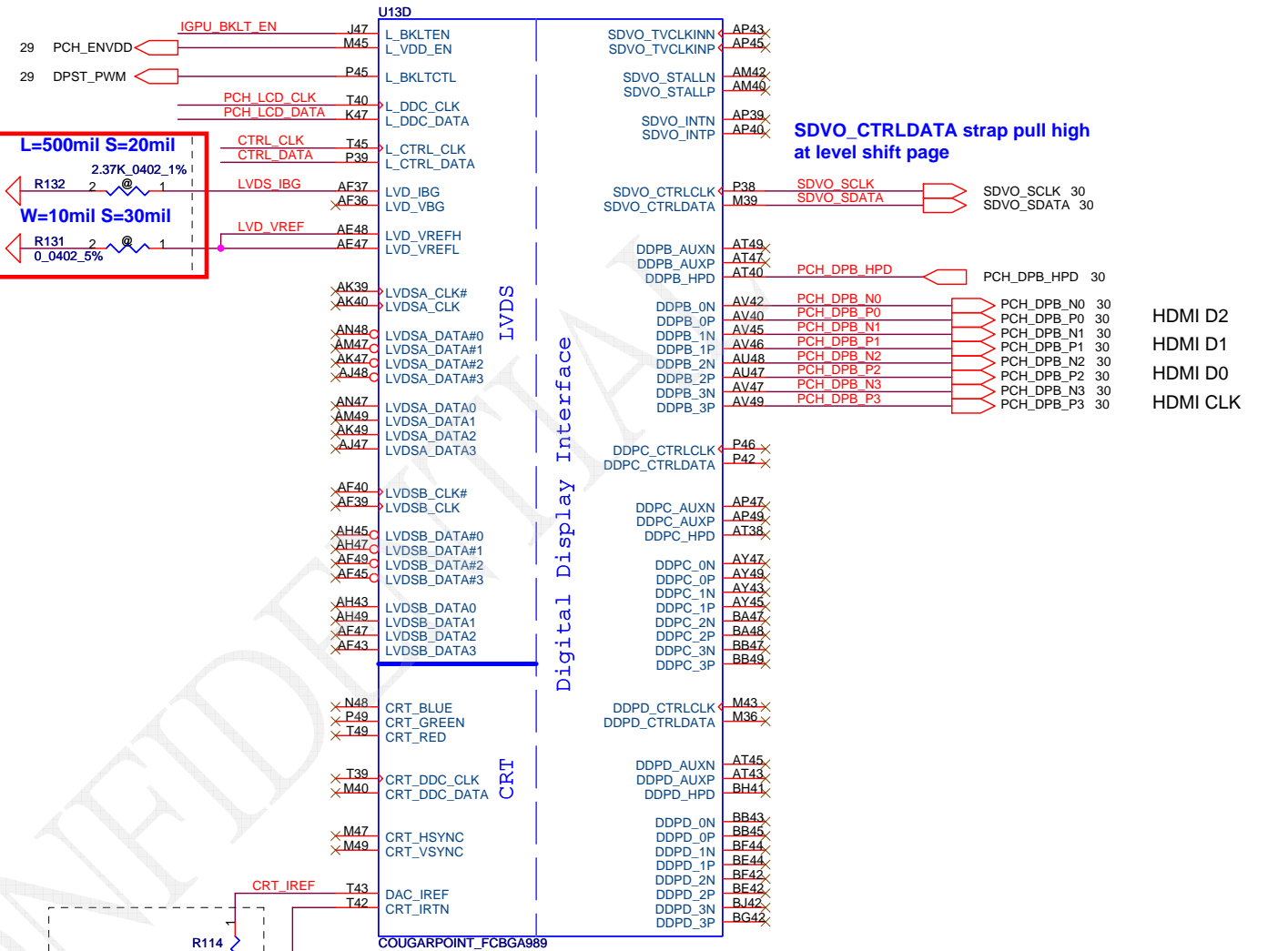
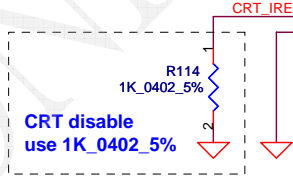
Check list1.5 P.60 disable Graphics
ALL Can NC
but DAC_IREF still need PD

LVDS disable:
DATA/Clock/Control an NC
VCC_TX_LVDS,VCCA_LVDS PD to GND

CRT disable:
DATA/Clock/Control an NC
VCCADAC connect to +3VS
DAC_IREF connect 1K_0402_5%

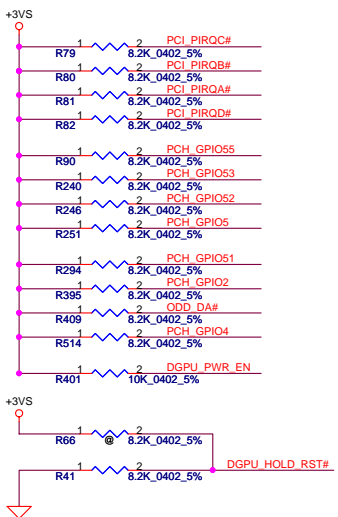


UM77 not support
LVDS/CRT



CONFIDENTIAL

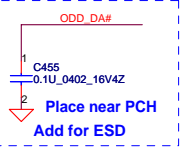
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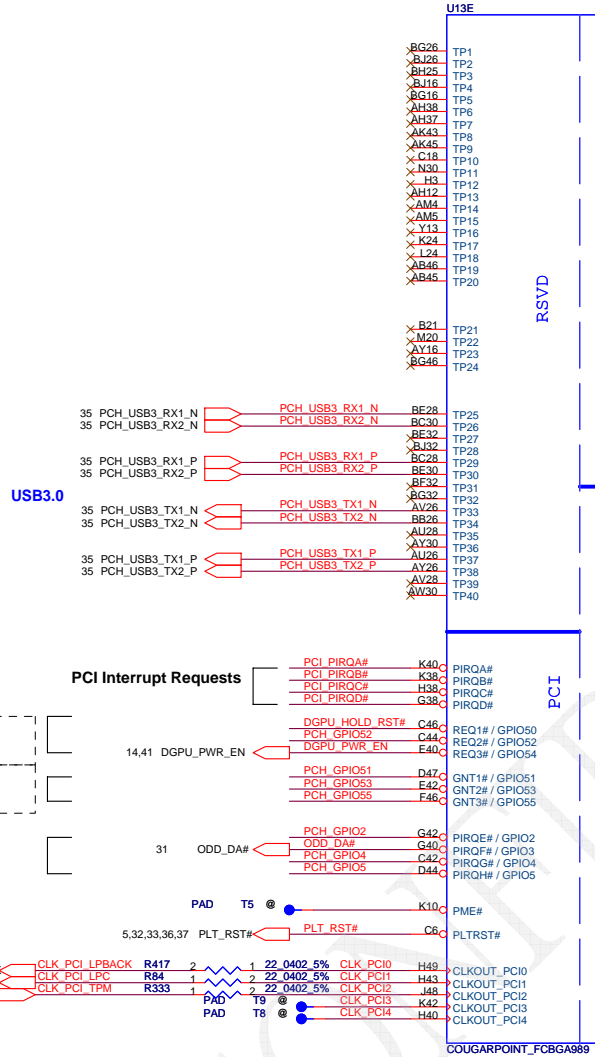
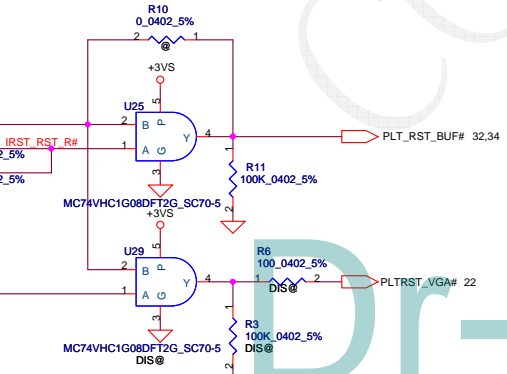
Boot BIOS Strap			
GNT1#/ GPIO51	GPIO19 GPIO51		Boot BIOS Destination
	Bit11	Bit10	
Internal	0	1	Reserved
PH	1	0	PCI
	0	0	SPI *
			LPC

CR Check list 1.5 only use for GPIO No use PH +3VS

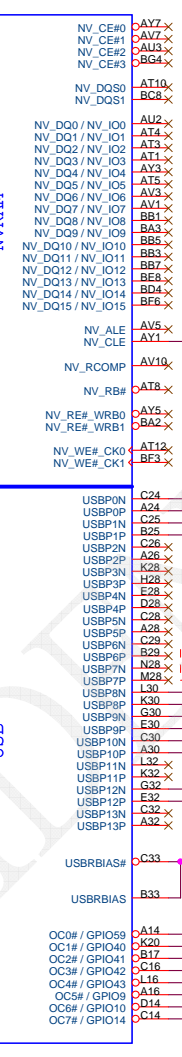
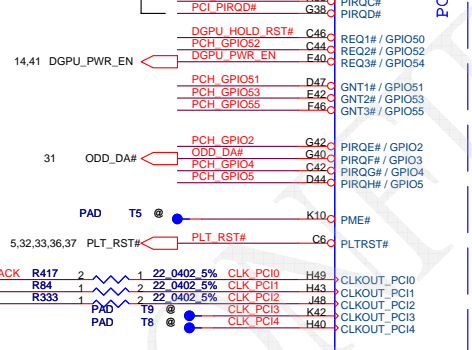
CR Check list 1.5 only use for GPIO 無須PH(Internal PH),如做GPIO PH +3VS



Place near PCH
Add for ESD

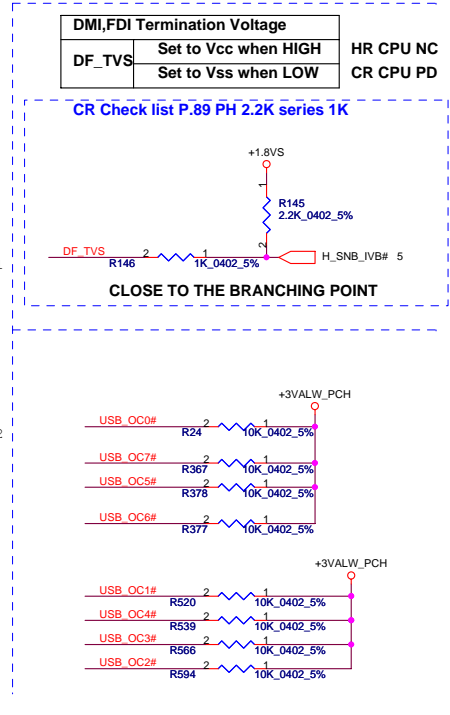


PCI Interrupt Requests



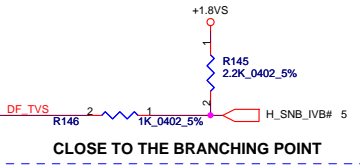
UM77, HM76, HM75 not support USB port 6 & 7, 12, 13

- Mini Card (WLAN)
- USB2 (Left side)
- CMOS Camera (LVDS)
- Mini Card (MSATA)
- Bluetooth

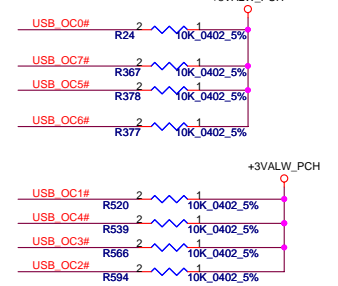


DMI, FDI Termination Voltage		
DF_TVSS	Set to Vcc when HIGH	HR CPU NC
	Set to Vss when LOW	CR CPU PD

CR Check list P.89 PH 2.2K series 1K



CLOSE TO THE BRANCHING POINT

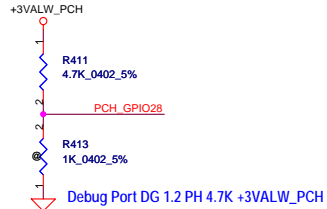


HDA_SYNC PH(PLL +=+1.5VS)

GPIO28

On-Die PLL Voltage Regulator

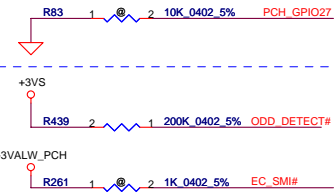
This signal has a weak internal pull up
 * H : On-Die PLL voltage regulator enable
 L : On-Die PLL Voltage Regulator disable



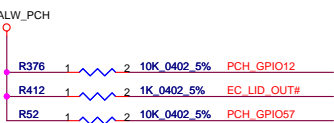
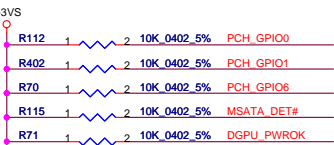
Fan Tachometer Inputs
 TACH1-7 only on server
 can insted to GPIO

No use PH 10K +3VS	PCH_GPIO00	TZ
No use PH 10K +3VS	PCH_GPIO1	A42
No use PH 10K +3VS	PCH_GPIO6	H36
No use PH 10K +3VS	36 EC_SCI#	EC_SCI# E38
No use PH 10K +3VALW	36 EC_SMI#	EC_SMI# C10
No use PH +3VALW	PCH_GPIO12	C4
No use PH +3VALW	36 EC_LID_OUT#	EC_LID_OUT# G2
No use PH +3VS	34 MSATA_DET#	MSATA_DET# U2
No use PH +3VS	50 VGA_PWROK	R45 1 2 0.0402 5% DGPU_PWROK D40
No use PH 10K +3VS	PCH_GPIO22	T5
No use PH +3VALW	PCH_GPIO24	E8
No use PD 10K to GND	PCH_GPIO27	E16
No use PH 10K +3VALW	PCH_GPIO28	P8
No use PH 10K +3VS	PCH_GPIO34	K1
No use can NC	PAD T12 @	PCH_GPIO35 K4
Can't PH	31 ODD_DETECT#	ODD_DETECT# V8
Can't PH	PAD T10 @	PCH_GPIO37 M5
No use PH 10K +3VS	Optimus(L)/ non optimus(H)	OPTIMUS_EN# N2
No use PH 10K +3VS	RAM flag	PCH_GPIO39 M3
No use PH 10K +3VS	PCH_GPIO48	V13
SATA5GP&TEMP_ALERT# CRB PH 10K +3VS	PCH_GPIO49	V3
No use PH +3VALW	PCH_GPIO57	D6

Deep S4,S5 wake event signal
 RTC alarm,Power BTN,GPIO27
 PCH_GPIO27 (Have internal Pull-High)
 Deep S4,S5 wake event signal



SATA2GP/GPIO36 & SATA3GP/GPIO37
 Sampled at Rising edge of PWROK.
 Weak internal pull-down.
 (weak internal pull-down is disabled
 after PLTRST# de-asserts)
 NOTE: This signal should NOT be
 pulled high when strap is sampled



GPIO24 Unmultiplexed
 NOTE: GPIO24 configuration
 register bits are not cleared by
 CF9h reset event.
 CRB1.0 PH10K to +3VALW

GPIO36/GPIO37 is Strap functionality
 that requires internal pull down to be sampled at rising PWROK.
 When uses as SATA2GP/SATA3GP for mechanical presence detect
 Use a external pull-up 150K-200K ohm to Vcc3_3
 When used as GP input
 Ensure GPI is not driven high during strap sampling window
 When Unused as GPIO or SATA*GP
 Use 8.2K-10K pull-down
 check list page 47

9/15 Layout request remove Test point They will route by itself

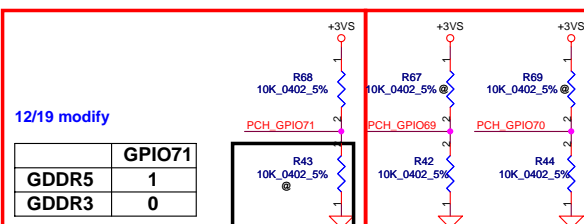
+3VS	
UMA0@	OPTIMUS_EN#
DIS@	
R427	1 2 10K 0.402 5%
R426	1 2 10K 0.402 5%

GPIO38	
OPTIMUS_EN#	
* Muxless	0
nonMuxless	1

9/15 Layout request remove Test point They will route by itself

+3VALW_PCH	
PCH_GPIO24	
R92	1 2 10K 0.402 5%
R94	1 2 10K 0.402 5%

GPIO24	
PCH_GPIO24	
* DDR3L	0
DDR3	1



Project ID	GPIO69	GPIO70
* X	0	0
X	0	1
X	0	0
X	1	1
X	1	0
X	0	1
X	0	0
X	1	1
X	1	0
X	1	1
X	1	0
X	1	1

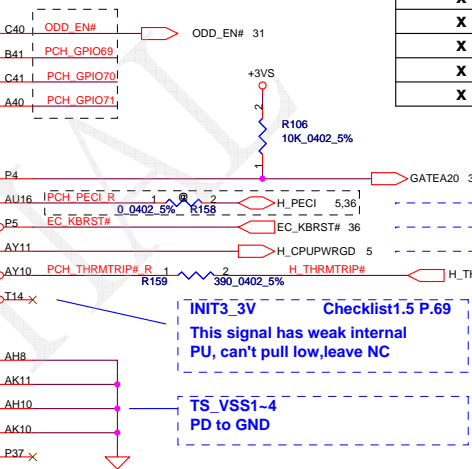
U13F

BMBUSY# / GPIO0	TACH4 / GPIO68
TACH1 / GPIO1	TACH5 / GPIO69
TACH2 / GPIO6	TACH6 / GPIO70
TACH3 / GPIO7	TACH7 / GPIO71
GPIO8	
LAN_PHY_PWR_CTRL / GPIO12	
GPIO15	
SATA4GP / GPIO16	
TACH0 / GPIO17	
SLOCK / GPIO22	
GPIO24 / MEM_LED	
GPIO27	
GPIO28	
STP_PC# / GPIO34	
GPIO35	
SATA2GP / GPIO36	
SATA3GP / GPIO37	
SLOAD / GPIO38	
SDATAOUT0 / GPIO39	
SDATAOUT1 / GPIO48	
SATA5GP / GPIO49	
GPIO57	

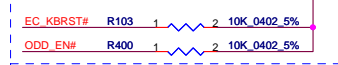
GPIO

CPU/MISC

NCTF



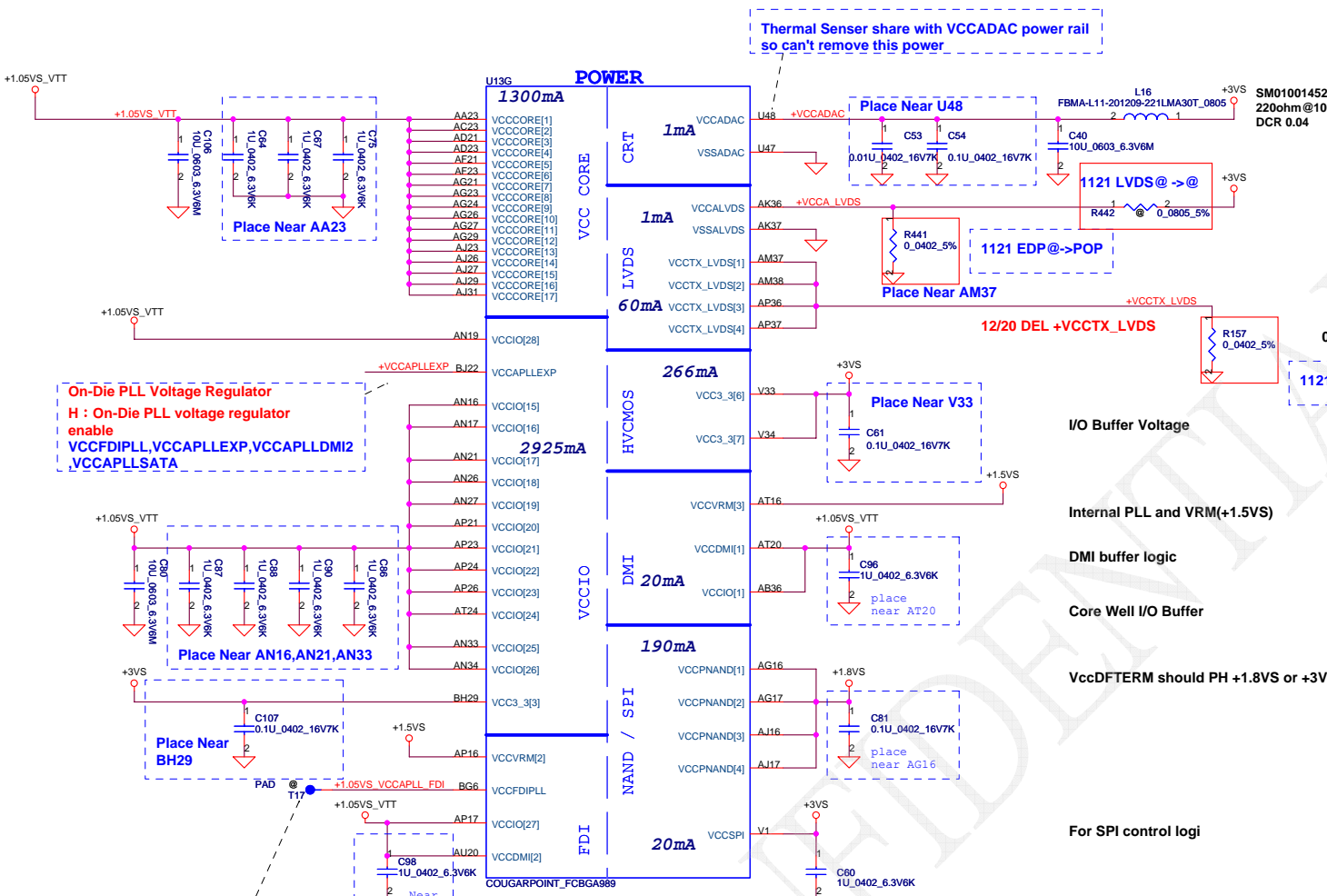
PECI CPU-EC
 CTRL+ALT+DEL
 non CPU power ok
 130c shut down



9/15 Layout request remove Test point They will route by itself

on board ram flag

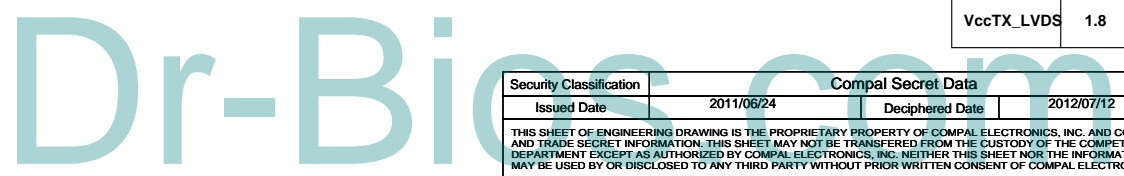
	GPIO39	GPIO23	GPIO22
EVT MICRON 4G	0	0	0
EVT ELPIDA 4G	0	0	1
DVT HYNIX 2G	0	1	0
DVT ELPIDA 2G	0	1	1

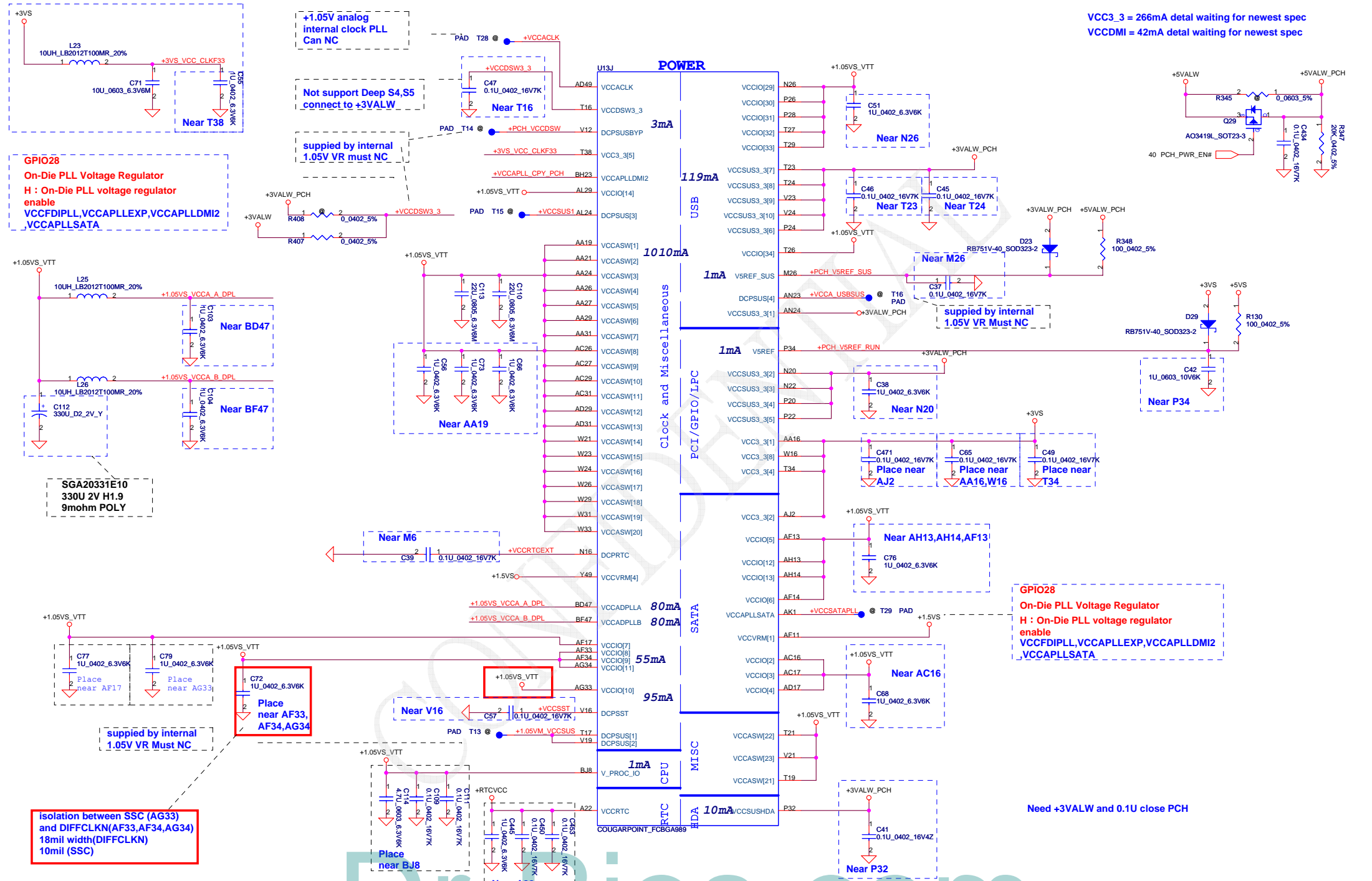


PCH Power Rail Table			
Voltage Rail	Voltage	S0 Iccmax Current(A)	
V_PROC_IO	1.05	0.001	Processor I/F
V5REF	5	0.001	PCH Core Well Reference Voltage
V5REF_Sus	5	0.001	Suspend Well Reference Voltag
Vcc3_3	3.3	0.266	I/O Buffer Voltage
VccADAC	3.3	0.001	Display DAC Analog Power. This power is supplied by the core well.
VccADPLLA	1.05	0.08	Display PLL A power
VccADPLLB	1.05	0.08	Display PLL B power
VccCore	1.05	1.3	Internal Logic Voltage
VccDMI	1.05	0.042	DMI Buffer Voltage
VccIO	1.05	2.925	Core Well I/O buffers
VccASW	1.05	1.01	1.05 V Supply for Intel R Management Engine and Integrated LAN
VccSPI	3.3	0.02	3.3 V Supply for SPI Controller Logic
VccDSW	3.3	0.003	3.3v supply for Deep S4/S5 well
VccpNAND	1.8	0.19	1.8V power supply for DF_TV5
VccRTC	3.3	6 uA	Battery Voltage
VccSus3_3	3.3	0.266	Suspend Well I/O Buffer Voltage
VccSusHDA	3.3 / 1.5	0.01	High Definition Audio Controller Suspend Voltage
VccVRM	1.8 / 1.5	0.16	1.8 V Internal PLL and VRMs (1.8 V for Desktop)
VccCLKDMI	1.05	0.02	DMI Clock Buffer Voltage
VccSSC	1.05	0.095	Spread Modulators Power Supply
VccDIFFCLKN	1.05	0.055	Differential Clock Buffers Power Supply
VccALVDS	3.3	0.001	Analog power supply for LVDS (Mobile Only)
VccTX_LVDS	1.8	0.06	Analog power supply for LVDS (Mobile Only)

On-Die PLL Voltage Regulator
H : On-Die PLL voltage regulator enable
VCCFDIPLL, VCCAPLLEXP, VCCAPLLDMI2, VCCAPLLSATA

On-Die PLL Voltage Regulator
H : On-Die PLL voltage regulator enable
VCCFDIPLL, VCCAPLLEXP, VCCAPLLDMI2, VCCAPLLSATA





VCC3_3 = 266mA detail waiting for newest spec
 VCCDMI = 42mA detail waiting for newest spec

GPIO28
 On-Die PLL Voltage Regulator
 H : On-Die PLL voltage regulator enable
 VCCFDIPLL,VCCAPLLEXP,VCCAPLLDMI2,VCCAPLLSATA

GPIO28
 On-Die PLL Voltage Regulator
 H : On-Die PLL voltage regulator enable
 VCCFDIPLL,VCCAPLLEXP,VCCAPLLDMI2,VCCAPLLSATA

SGA20331E10
 330U 2V H1.9
 9mohm POLY

isolation between SSC (AG33) and DIFFCLKN(AF33,AF34,AG34)
 18mil width(DIFFCLKN)
 10mil (SSC)

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4019J1			C	
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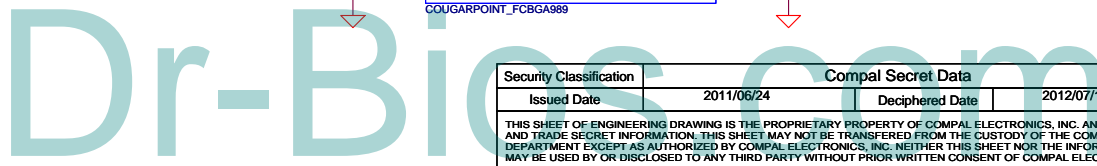
H5		U13H	
	VSS[0]		
AA17	VSS[1]		
AA2	VSS[2]		
AA3	VSS[3]		
AA33	VSS[4]		
AA34	VSS[5]		
AB11	VSS[6]		
AB14	VSS[7]		
AB39	VSS[8]		
AB4	VSS[9]		
AB43	VSS[10]		
AB5	VSS[11]		
AB7	VSS[12]		
AC19	VSS[13]		
AC2	VSS[14]		
AC21	VSS[15]		
AC24	VSS[16]		
AC33	VSS[17]		
AC34	VSS[18]		
AC48	VSS[19]		
AD10	VSS[20]		
AD11	VSS[21]		
AD12	VSS[22]		
AD13	VSS[23]		
AD19	VSS[24]		
AD24	VSS[25]		
AD26	VSS[26]		
AD27	VSS[27]		
AD33	VSS[28]		
AD34	VSS[29]		
AD36	VSS[30]		
AD37	VSS[31]		
AD38	VSS[32]		
AD39	VSS[33]		
AD4	VSS[34]		
AD40	VSS[35]		
AD42	VSS[36]		
AD43	VSS[37]		
AD45	VSS[38]		
AD46	VSS[39]		
AD8	VSS[40]		
AE2	VSS[41]		
AF3	VSS[42]		
AF10	VSS[43]		
AF12	VSS[44]		
AD14	VSS[45]		
AD16	VSS[46]		
AF16	VSS[47]		
AF19	VSS[48]		
AF24	VSS[49]		
AF26	VSS[50]		
AF27	VSS[51]		
AF29	VSS[52]		
AF31	VSS[53]		
AF38	VSS[54]		
AF4	VSS[55]		
AF42	VSS[56]		
AF46	VSS[57]		
AF5	VSS[58]		
AF7	VSS[59]		
AF8	VSS[60]		
AG19	VSS[61]		
AG2	VSS[62]		
AG31	VSS[63]		
AG48	VSS[64]		
AH11	VSS[65]		
AH3	VSS[66]		
AH36	VSS[67]		
AH39	VSS[68]		
AH40	VSS[69]		
AH42	VSS[70]		
AH46	VSS[71]		
AH7	VSS[72]		
AJ19	VSS[73]		
AJ21	VSS[74]		
AJ24	VSS[75]		
AJ33	VSS[76]		
AJ34	VSS[77]		
AK12	VSS[78]		
AK3	VSS[79]		

COUGARPOINT_FCBGA989

U13I			
AY4	VSS[159]		
AY42	VSS[160]		
AY46	VSS[161]		
AY8	VSS[162]		
B11	VSS[163]		
B15	VSS[164]		
B19	VSS[165]		
B23	VSS[166]		
B27	VSS[167]		
B31	VSS[168]		
B35	VSS[169]		
B39	VSS[170]		
B7	VSS[171]		
F45	VSS[172]		
BB12	VSS[173]		
BB16	VSS[174]		
AL2	VSS[175]		
BB22	VSS[176]		
BB24	VSS[177]		
BB28	VSS[178]		
BB30	VSS[179]		
BB38	VSS[180]		
BB4	VSS[181]		
BB46	VSS[182]		
BC14	VSS[183]		
BC18	VSS[184]		
BC2	VSS[185]		
BC22	VSS[186]		
AM39	VSS[187]		
BC32	VSS[188]		
BC34	VSS[189]		
BC36	VSS[190]		
AM7	VSS[191]		
BC42	VSS[192]		
BC48	VSS[193]		
BD46	VSS[194]		
BD5	VSS[195]		
BE2	VSS[196]		
BE26	VSS[197]		
BE40	VSS[198]		
BE10	VSS[199]		
BE12	VSS[200]		
BF16	VSS[201]		
BF20	VSS[202]		
BF22	VSS[203]		
BF24	VSS[204]		
BF26	VSS[205]		
BF28	VSS[206]		
BD3	VSS[207]		
AT11	VSS[208]		
AT13	VSS[209]		
BF40	VSS[210]		
BF8	VSS[211]		
AT26	VSS[212]		
BG31	VSS[213]		
BG33	VSS[214]		
BG44	VSS[215]		
BH11	VSS[216]		
BH15	VSS[217]		
BH17	VSS[218]		
BH19	VSS[219]		
H10	VSS[220]		
BH27	VSS[221]		
BH31	VSS[222]		
BH33	VSS[223]		
BH35	VSS[224]		
BH39	VSS[225]		
BH43	VSS[226]		
BH7	VSS[227]		
D3	VSS[228]		
D12	VSS[229]		
D16	VSS[230]		
D18	VSS[231]		
D18	VSS[232]		
D22	VSS[233]		
D24	VSS[234]		
D26	VSS[235]		
D30	VSS[236]		
D32	VSS[237]		
D34	VSS[238]		
D38	VSS[239]		
D42	VSS[240]		
D8	VSS[241]		
E18	VSS[242]		
E26	VSS[243]		
G18	VSS[244]		
G20	VSS[245]		
G26	VSS[246]		
G28	VSS[247]		
G36	VSS[248]		
G48	VSS[249]		
H12	VSS[250]		
H18	VSS[251]		
H22	VSS[252]		
H24	VSS[253]		
H26	VSS[254]		
H30	VSS[255]		
H32	VSS[256]		
H34	VSS[257]		
F3	VSS[258]		

COUGARPOINT_FCBGA989

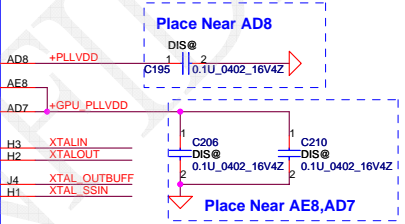
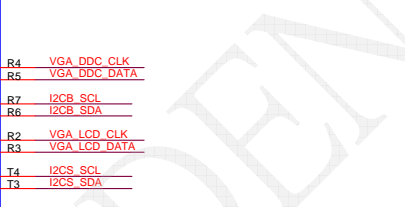
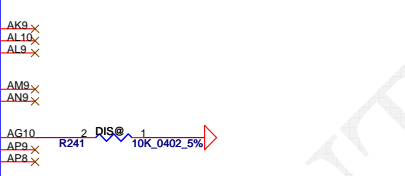
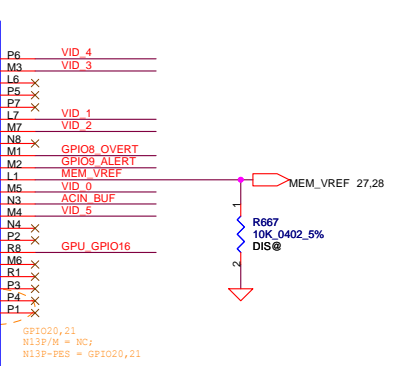
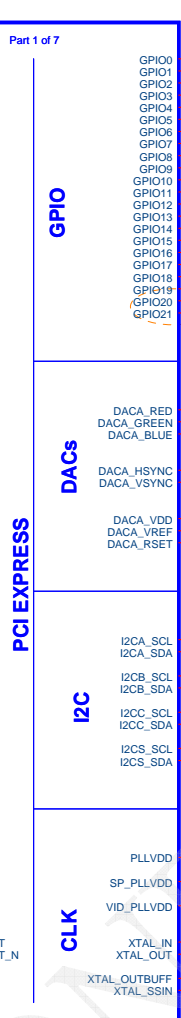
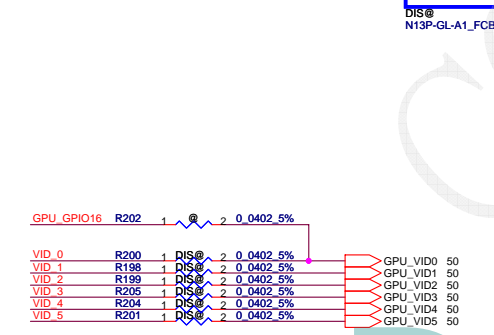
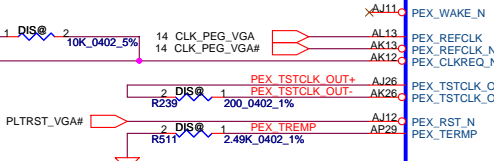
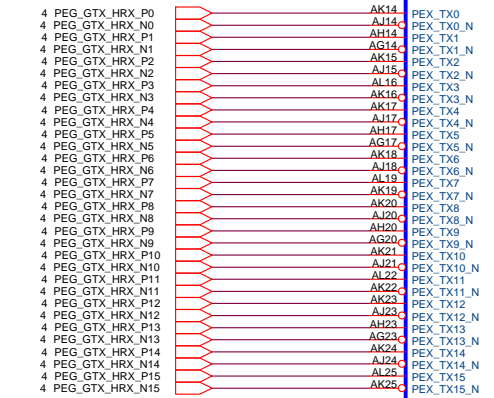
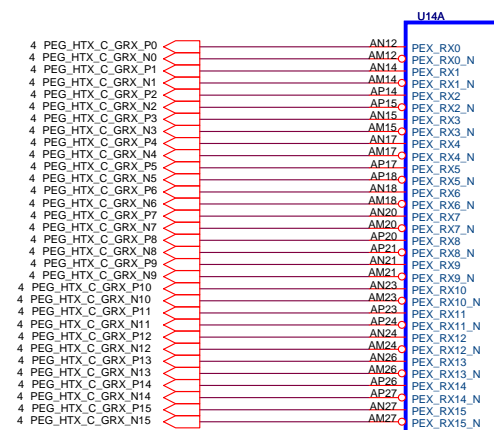
VSS[259]	H46
VSS[260]	K18
VSS[261]	K26
VSS[262]	K30
VSS[263]	K46
VSS[264]	K7
VSS[265]	L18
VSS[266]	L2
VSS[267]	L20
VSS[268]	L26
VSS[269]	L28
VSS[270]	L36
VSS[271]	L48
VSS[272]	M12
VSS[273]	P16
VSS[274]	M18
VSS[275]	M22
VSS[276]	M24
VSS[277]	M30
VSS[278]	M32
VSS[279]	M34
VSS[280]	M38
VSS[281]	M4
VSS[282]	M42
VSS[283]	M46
VSS[284]	M8
VSS[285]	N18
VSS[286]	P30
VSS[287]	N47
VSS[288]	P11
VSS[289]	P18
VSS[290]	T33
VSS[291]	P40
VSS[292]	P43
VSS[293]	P47
VSS[294]	P7
VSS[295]	R2
VSS[296]	R48
VSS[297]	T12
VSS[298]	T31
VSS[299]	T37
VSS[300]	T4
VSS[301]	W34
VSS[302]	T46
VSS[303]	T47
VSS[304]	T8
VSS[305]	V11
VSS[306]	V17
VSS[307]	V26
VSS[308]	V27
VSS[309]	V29
VSS[310]	V31
VSS[311]	V36
VSS[312]	V38
VSS[313]	V43
VSS[314]	V7
VSS[315]	W17
VSS[316]	W2
VSS[317]	W27
VSS[318]	W48
VSS[319]	Y12
VSS[320]	Y38
VSS[321]	Y4
VSS[322]	Y42
VSS[323]	Y46
VSS[324]	Y8
VSS[325]	BG29
VSS[326]	N24
VSS[327]	AJ3
VSS[330]	AD47
VSS[331]	B45
VSS[333]	BE10
VSS[334]	BG41
VSS[335]	G14
VSS[337]	H16
VSS[338]	T36
VSS[340]	BG22
VSS[342]	C22
VSS[343]	AP13
VSS[344]	M14
VSS[345]	AP1
VSS[346]	BE16
VSS[347]	BC16
VSS[348]	BG28
VSS[350]	RJ28
VSS[351]	
VSS[352]	



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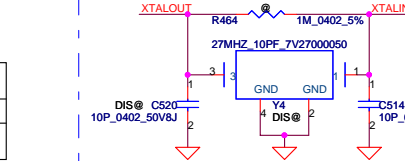
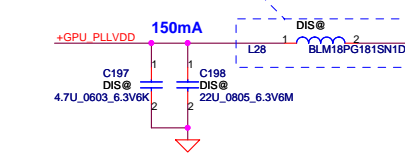
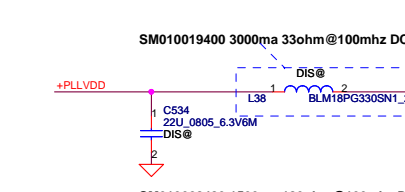
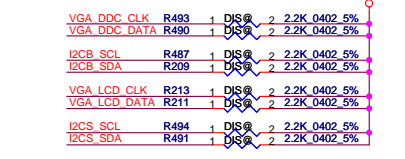
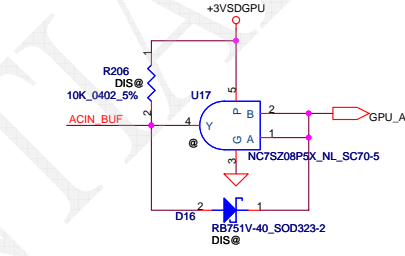
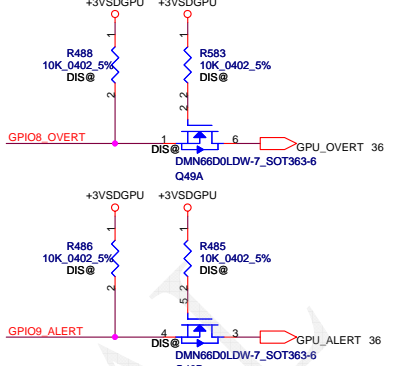
Compal Electronics, Inc.	
SCHEMATIC MB A8203	
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Date: Thursday, June 14, 2012	Sheet 21 of 56



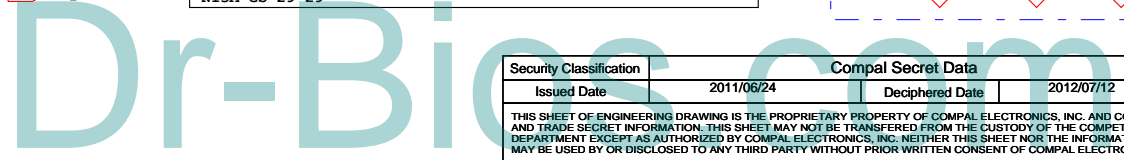
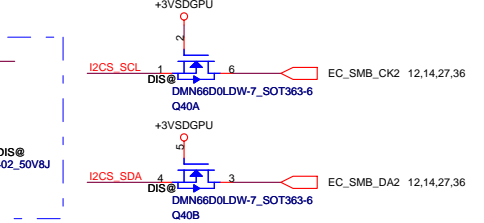
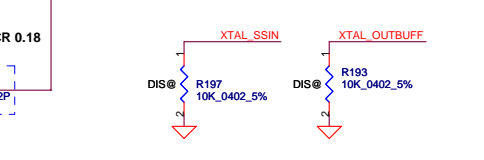
NV DG PLL_VDD
0.1Ux1
22Ux1 33ohm(ESR0.05)x1

NV DG SP_PLLVDD,VID_PLLVDD
0.1Ux2 Under GPU
4.7Ux1,22Ux1
180ohm(ESR0.2)x1

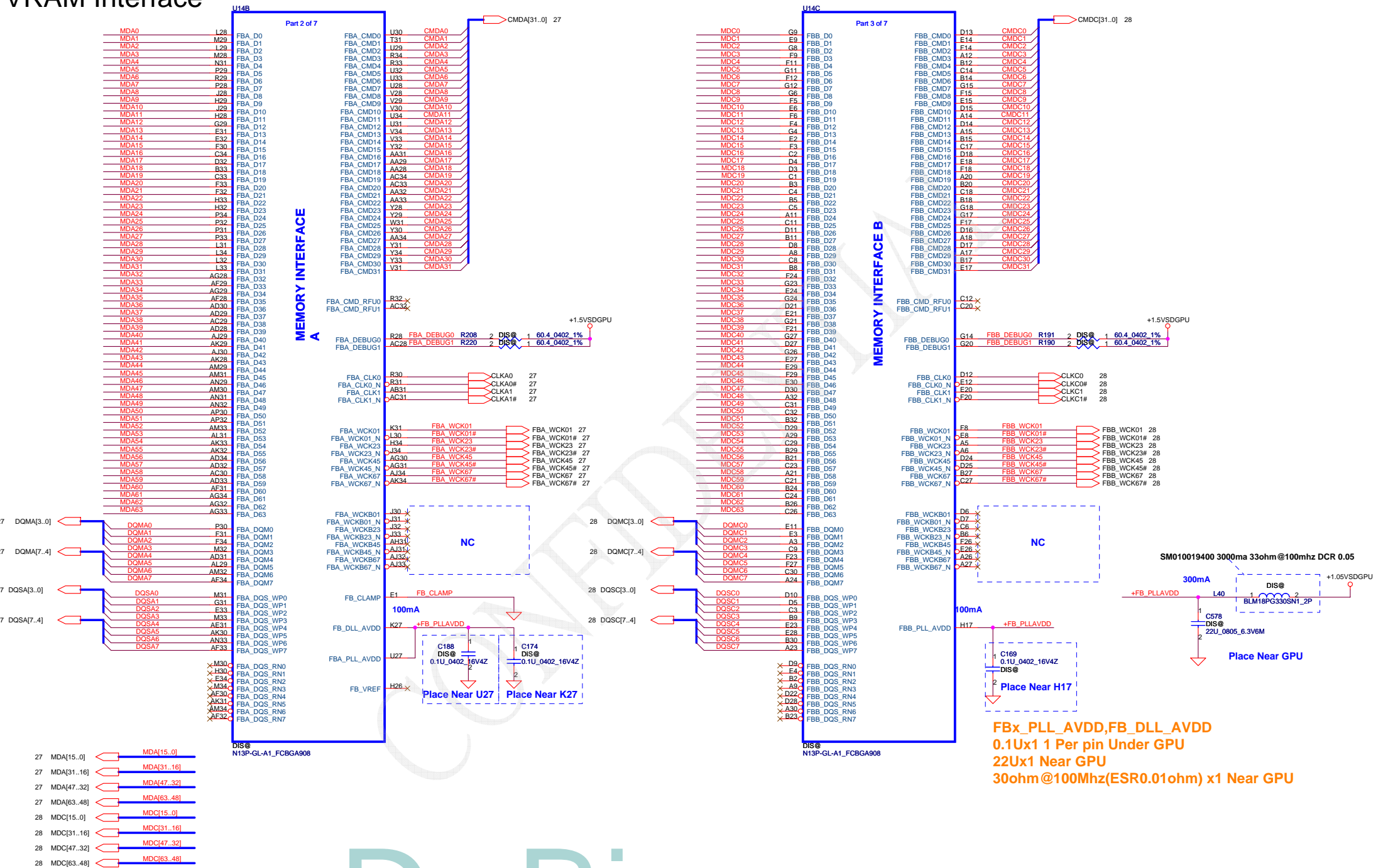
VGA Chipset	Default Voltage	VID0	VID1	VID2	VID3	VID4	VID5	VID6
N13P-GS 29*29	TBD	0	0	0	0	1	1	0
N13P-GV 29*29	0.9V	0	0	0	0	1	1	0
N13M-GS 29*29								



GPIO	I/O	USAGE
GPIO0	O	GPU_VID4
GPIO1	O	GPU_VID3
GPIO2	O	LCD_BL_PWM
GPIO3	O	LCD_VCC
GPIO4	O	LCD_BLEN
GPIO5	O	GPU_VID1
GPIO7	O	3D Vision
GPIO8	I/O	OVERT
GPIO9	I/O	ALERT
GPIO10	O	MEM_VREF_CTL
GPIO11	O	MEM_VDD_CTL(PES) GPU_VID0(Real N13P)
GPIO12	I	PWR_LEVEL
GPIO13	O	THERM_LOAD_STEP_DOWN
GPIO14	I	HPD_AB
GPIO15	I	HPD_C
GPIO16	O	THERM_LOAD_STEP_UP
GPIO17	I	HPD_D
GPIO18	I	HPD_E
GPIO19	I	HPD_F
GPIO20		Reserved
GPIO21		Reserved
GPIO23	I/O	SLI_RASTER_SYNC
GPIO24	O	SLI_SWAPRDY



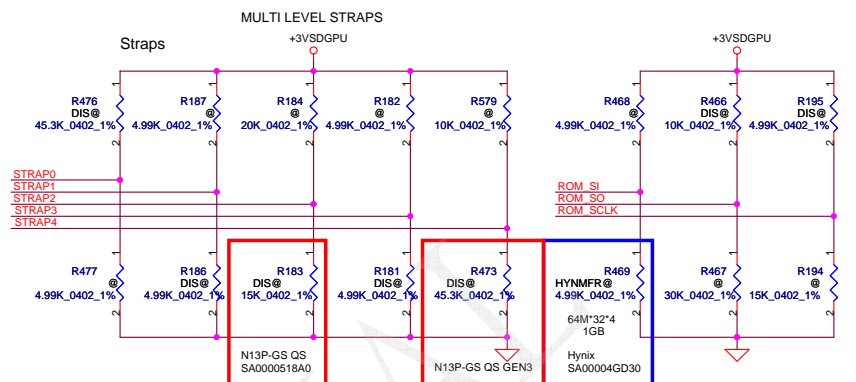
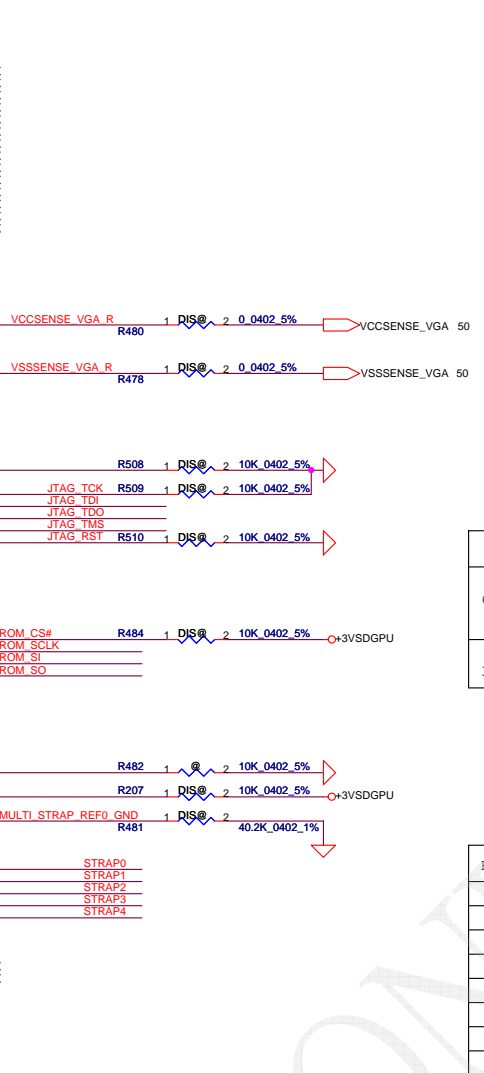
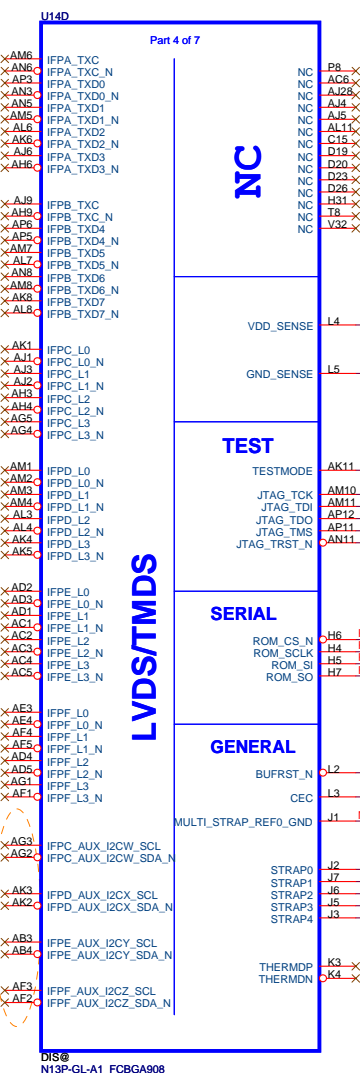
VRAM Interface



- 27 MDA[15..0] MDA[15..0]
- 27 MDA[31..16] MDA[31..16]
- 27 MDA[47..32] MDA[47..32]
- 27 MDA[63..48] MDA[63..48]
- 28 MDC[15..0] MDC[15..0]
- 28 MDC[31..16] MDC[31..16]
- 28 MDC[47..32] MDC[47..32]
- 28 MDC[63..48] MDC[63..48]

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DEPARTMENT OF ELECTRONIC ENGINEERING, INC. SHEET NO. 1				Rev C





VRAM BOM Config **VRAM P/N**
X76364BOL03: 64Mx32x4 **HYN 64*32 2000M SA00004GD30 (S IC D5 64M32/2.5G H5GQ2H24MFR-T2C ABO)**
X76364BOL04: 64Mx32x4 **HYN 64*32 2000M SA00004GD50 (S IC D5 64M32/2.5G H5GQ2H24AFR-T2C ABO)**

R469
HYNAFR@
64M*32*4
1GB
Hynix
SA00004GD50

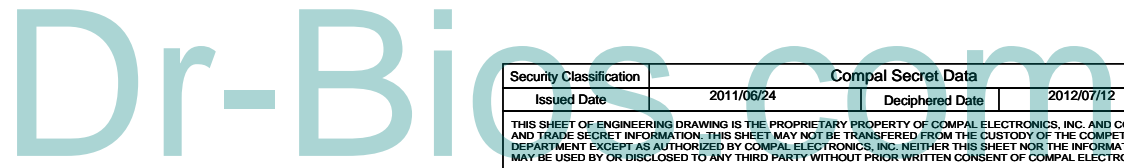
GDDR5	Vendor	Strap	ROM_SI
64M x 32	Hynix (M)	Ox0	PD 5K
	Samsung	Ox1	PD 10K
	Hynix (A)	Ox4	PD 25K
32M x 32	Hynix	Ox2	PD 15K
	Samsung	Ox3	PD 20K

For N13P-GS-A1 (ES2) A2 (QS) strap table Decive ID : 0x0FD2

GPU	Freq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13P-GS	2000 MHZ	64M* 32* 4 1GB	Hynix SA00004GD30						R PD 5K		
N13P-GS	2000 MHZ	64M* 32* 4 1GB	Samsung	R PU 45K	R PD 5K	R PD 15K	R PD 5K	R PD 45K	R PD 10K	R PU 5K	R PU 5K
N13P-GS	2000 MHZ	64M* 32* 4 1GB	Hynix SA00004GD50						R PD 25K		

Resistor Values	Pull-up to +3V	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

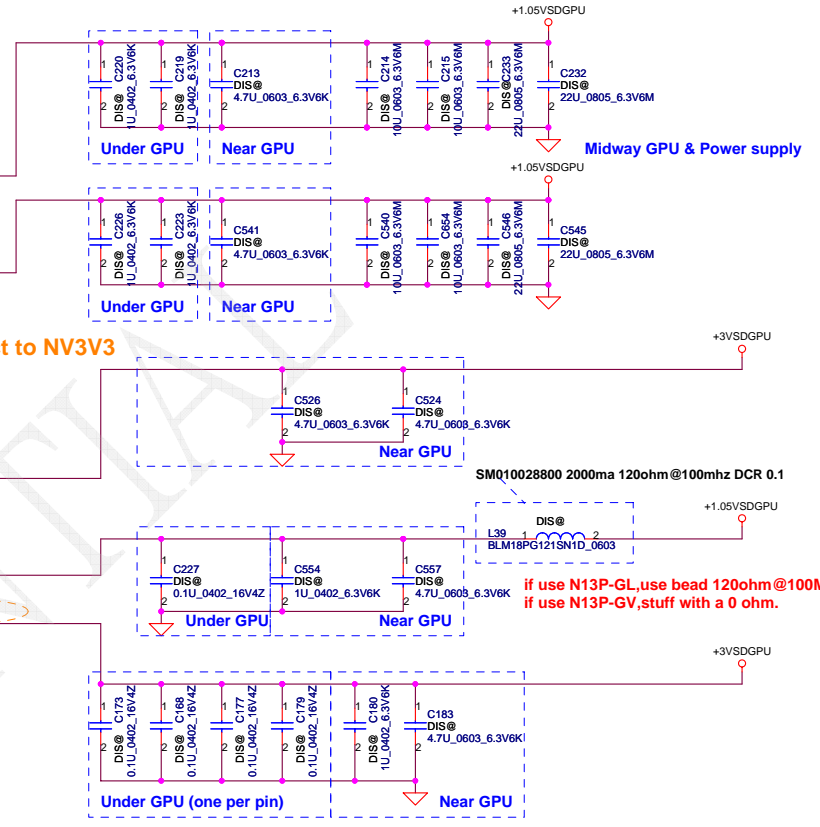
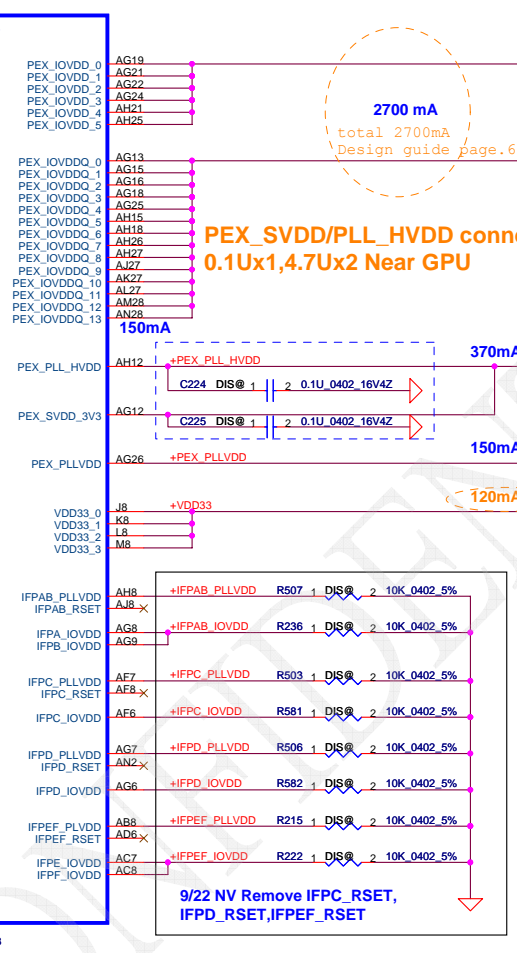
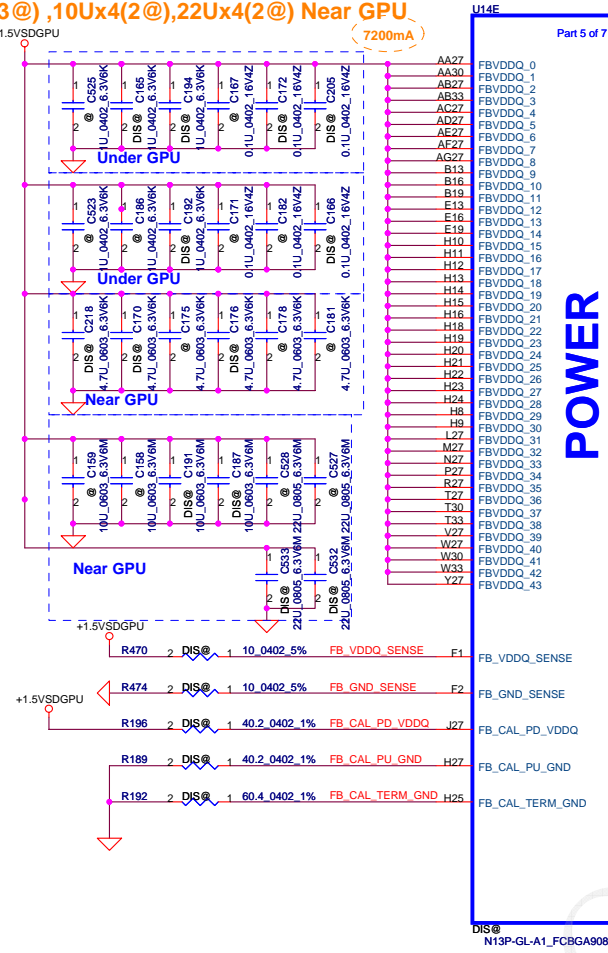
STRAP0	USER[3:0]
STRAP1	3GIO_PADCFG_LUT_ADR[3:0]
STRAP2	PCI_DEVID[3:0]
STRAP3	SOR[3:0]
STRAP4	PEX_MAX_SPEED, DP_PLLVDD33V
ROM_SCLK	PCI_DEV[4:5], SUB_VENDOR,PEX_PLL_EN_TERM
ROM_SI	RAM_CFG[3:0]
ROM_SO	FB_BAR_SIZE[1:0],SMB ALT_ADOOR, VGA_DEVICE



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NV DG FBVDDQ(DDR3)
 0.1Ux8,1Ux2,4.7Ux2 Under GPU
 10Ux4 Near GPU
NV DG FBVDDQ(GDDR5)
 0.1Ux6(3@),1Ux6(3@),Under GPU
 4.7Ux6(3@) ,10Ux4(2@),22Ux4(2@) Near GPU

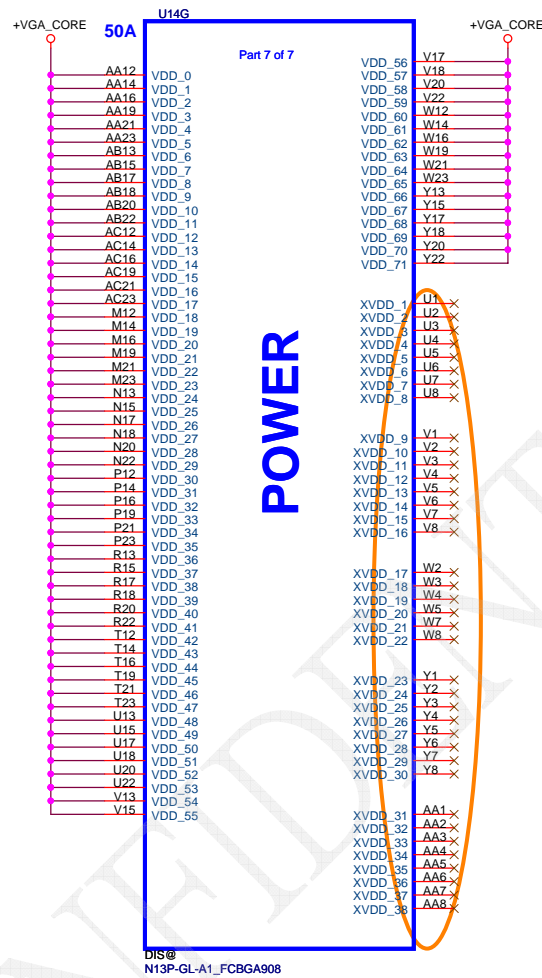
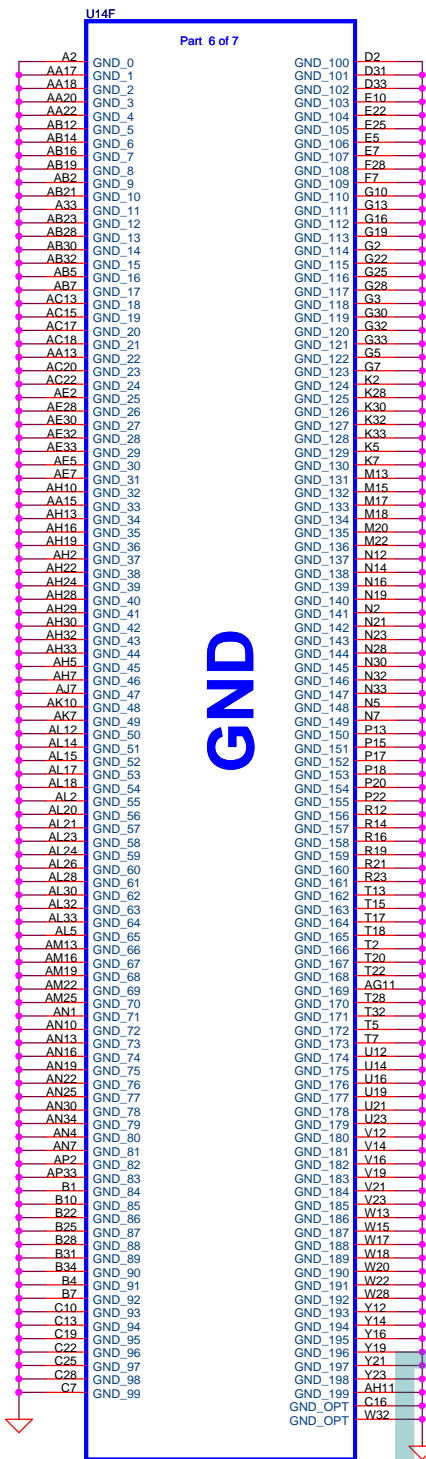
NV DG PEX_IOVVD/Q combined
 1Ux4 Under GPU
 4.7Ux2 Near GPU
 10Ux4,22Ux4 Midway GPU & Power supply



NV DG PEX_PLLVDD
 0.1Ux1 Under GPU
 1Ux1,4.7Ux1 Near GPU
NV DG VDD33/3VSMISC
 0.1Ux4 Under GPU 1Per pin
 1Ux1,4.7Ux1 Near GPU

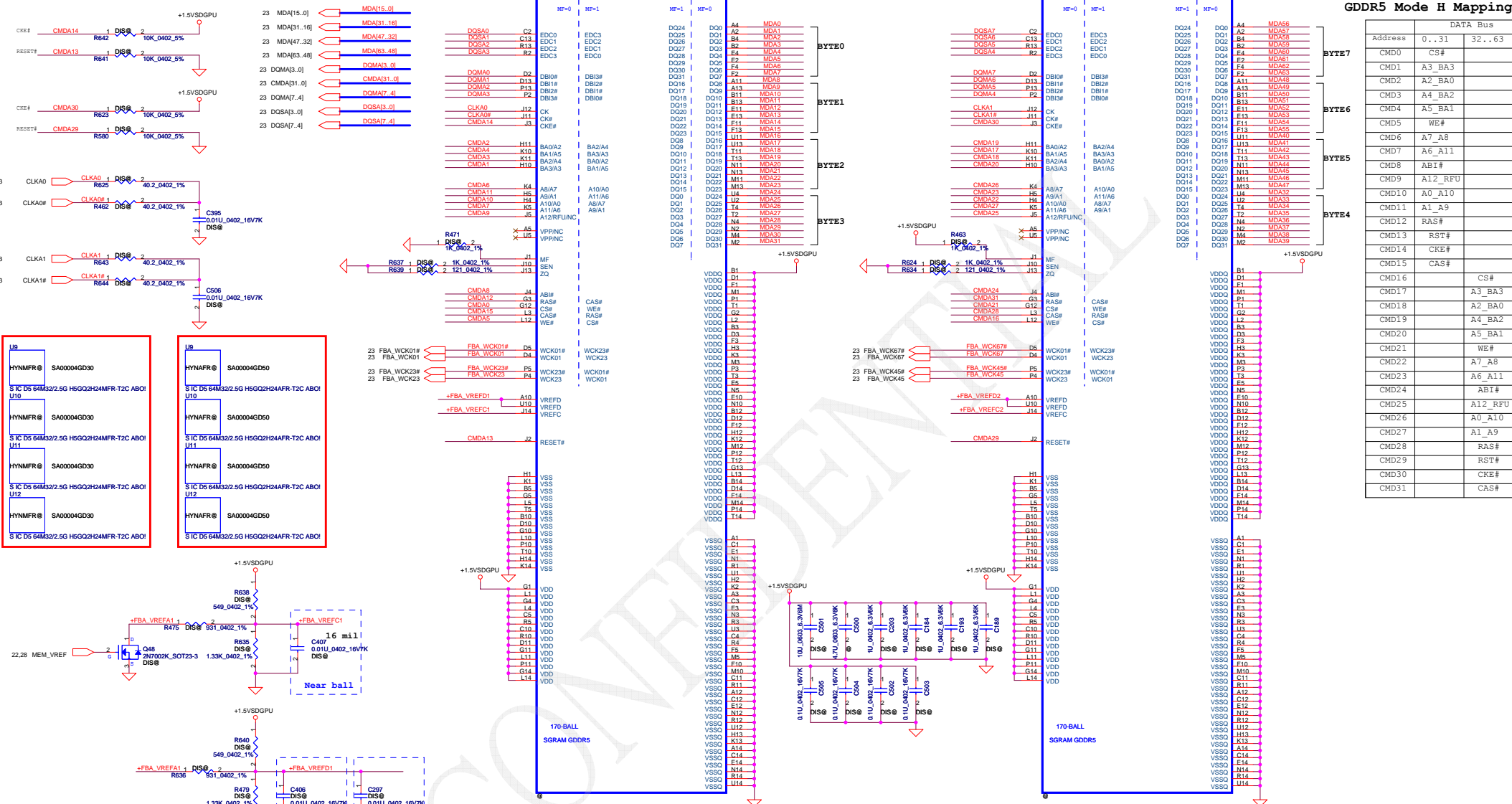
POWER

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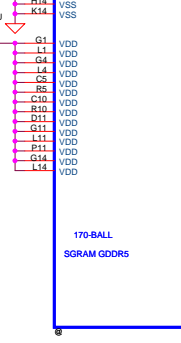
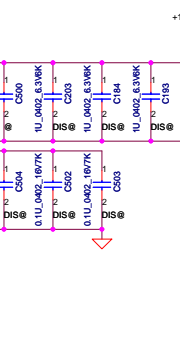
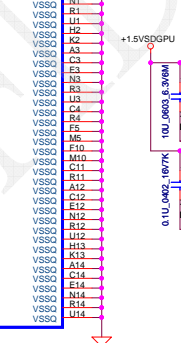
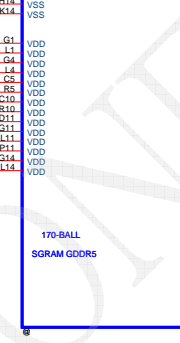
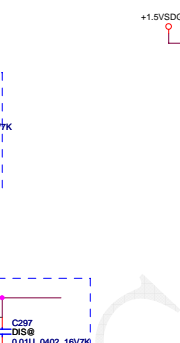
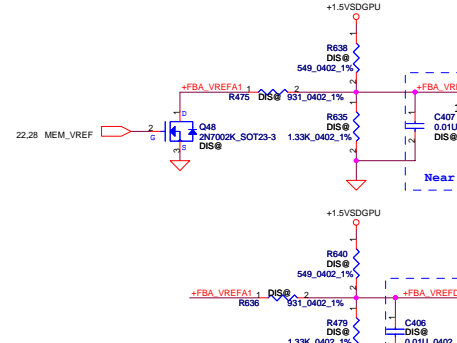
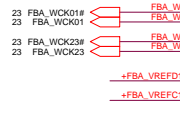
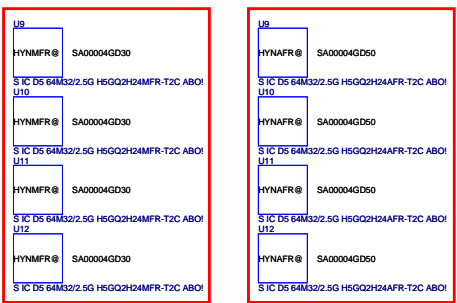
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Memory Partition A - 64 bits

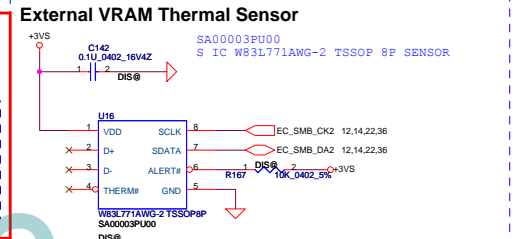


GDDR5 Mode H Mapping

Address	DATA Bus
0..31	32..63
CMD0	CS#
CMD1	A3_BA3
CMD2	A2_BA0
CMD3	A4_BA2
CMD4	A5_BA1
CMD5	WE#
CMD6	A7_A8
CMD7	A6_A11
CMD8	AB1#
CMD9	A12_RFU
CMD10	A0_A10
CMD11	A1_A9
CMD12	RAS#
CMD13	RST#
CMD14	CKE#
CMD15	CAS#
CMD16	CS#
CMD17	A3_BA3
CMD18	A2_BA0
CMD19	A4_BA2
CMD20	A5_BA1
CMD21	WE#
CMD22	A7_A8
CMD23	A6_A11
CMD24	AB1#
CMD25	A12_RFU
CMD26	A0_A10
CMD27	A1_A9
CMD28	RAS#
CMD29	RST#
CMD30	CKE#
CMD31	CAS#



建議線路
0.1u6x6,1u4x4,10u1x1 FBVDDQ
1u4x4,10u1x1 FBVDD
for 2pcs VRAM
目前
0.1u8x8+1u8x8+4.7u3x3 (@)+10u2

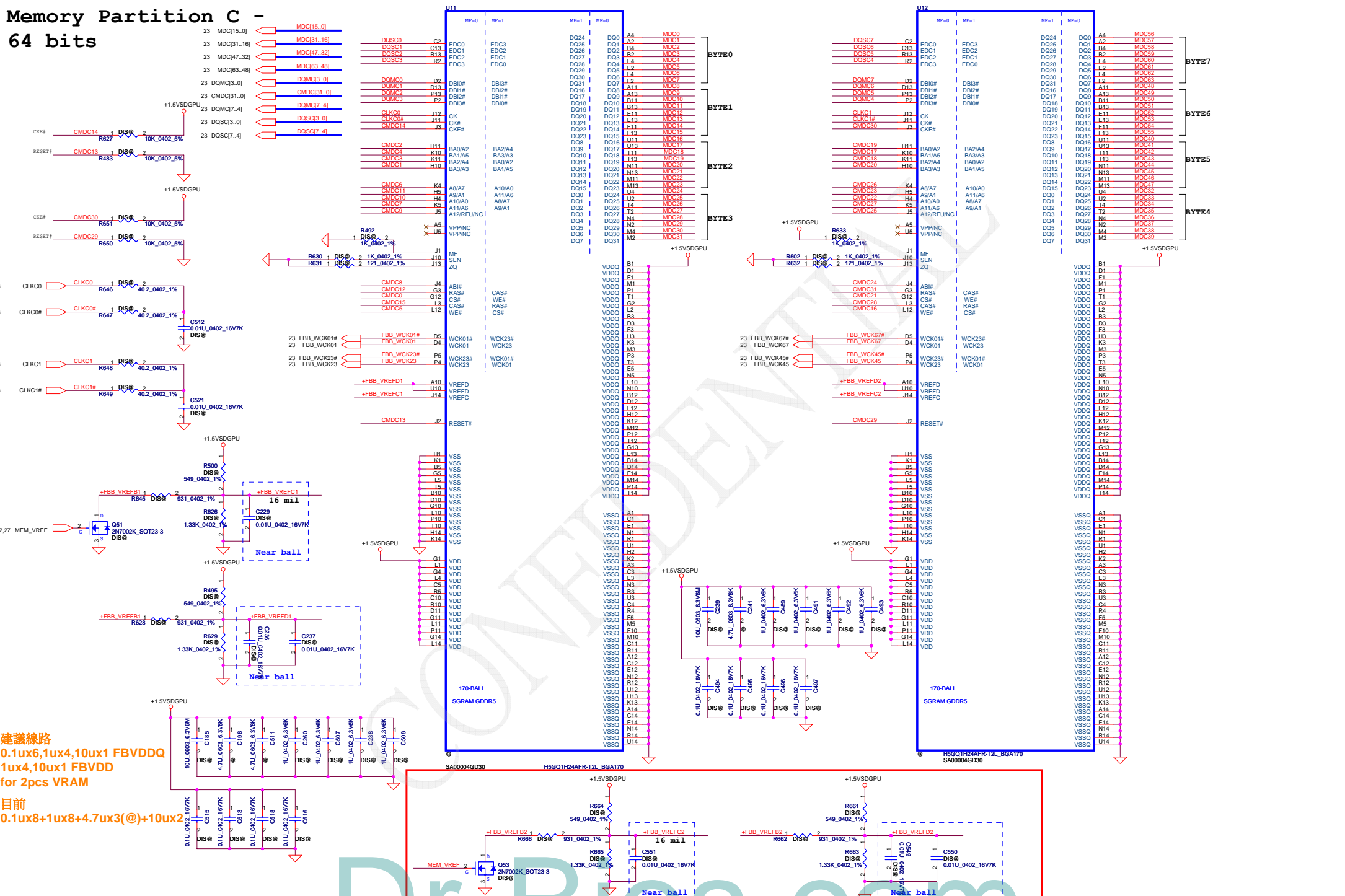


VRAM BOM Config
X7634B0L01: 1G HYN 128*16 2.5G SA00004GD30 (S IC D5 64M32/2.5G H5GQ2H24MFR-T2C ABO)

Memory Partition C - 64 bits

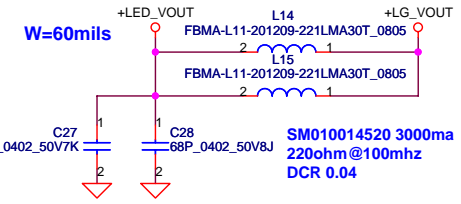
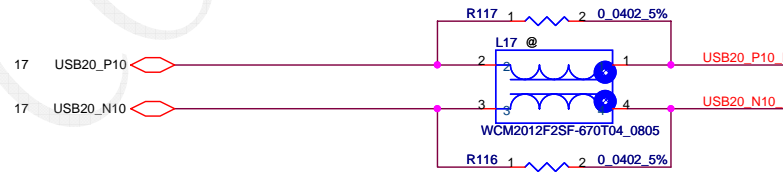
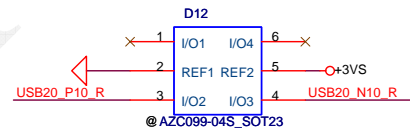
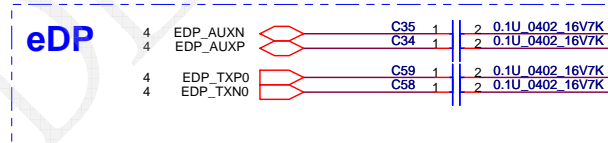
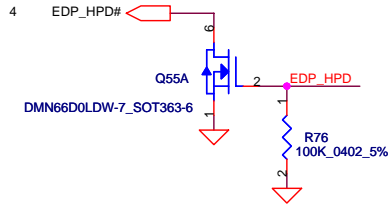
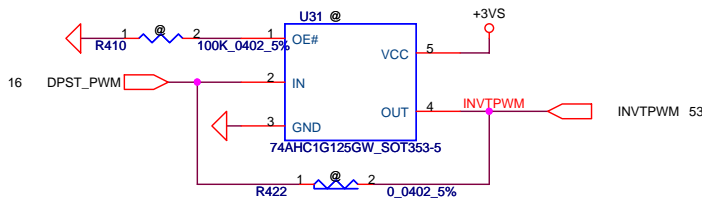
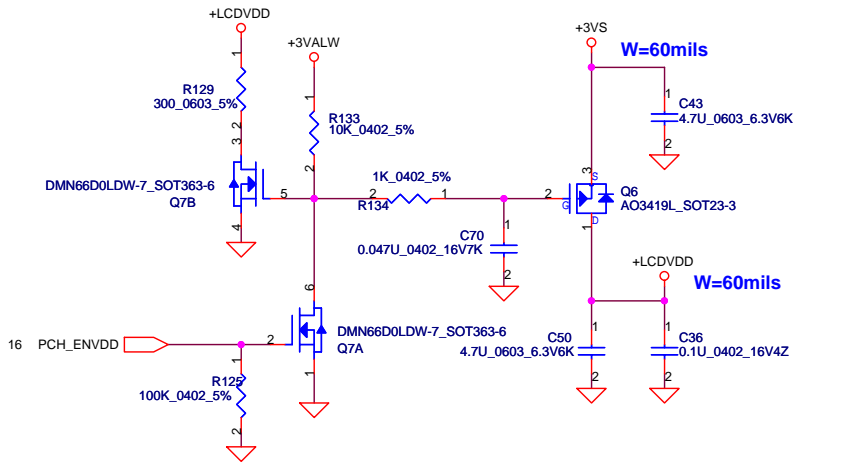
建議線路
0.1u6,1u4,10u1 FBVDDQ
1u4,10u1 FBVDD
for 2pcs VRAM

目前
0.1u8+1u8+4.7u3(@)+10u2

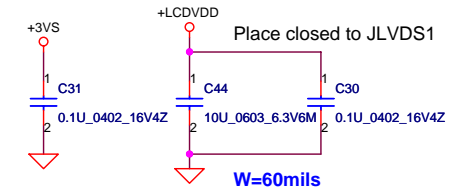
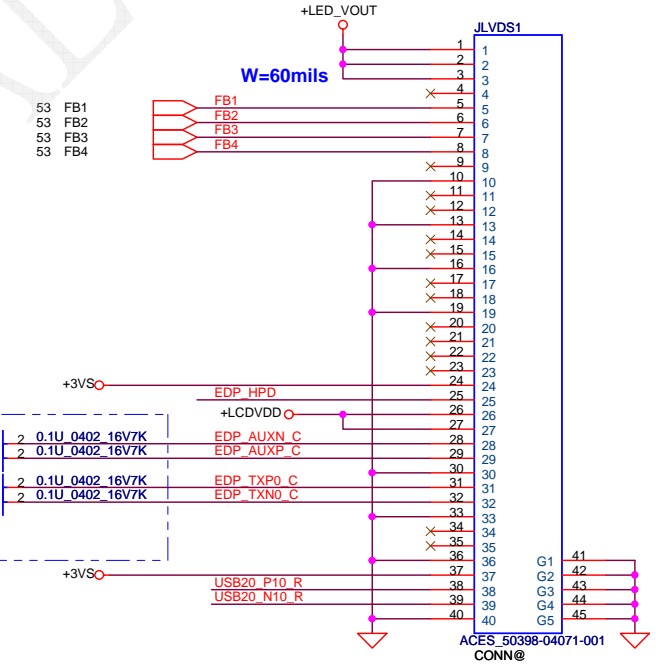


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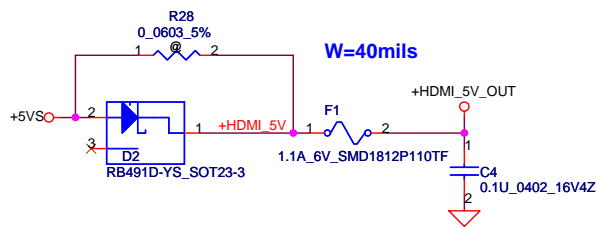
LCD POWER CIRCUIT



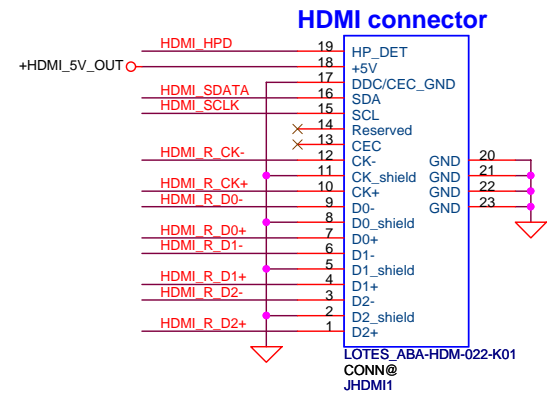
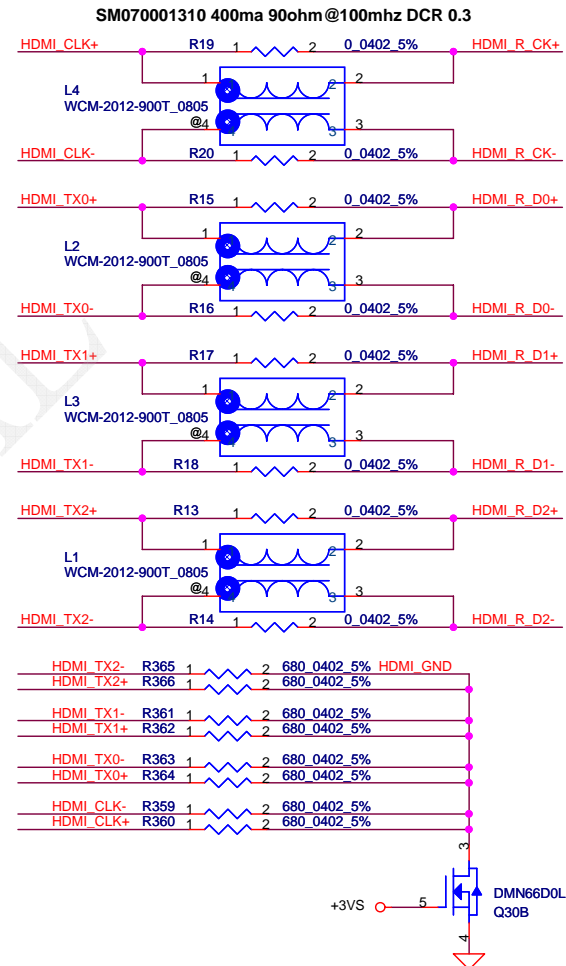
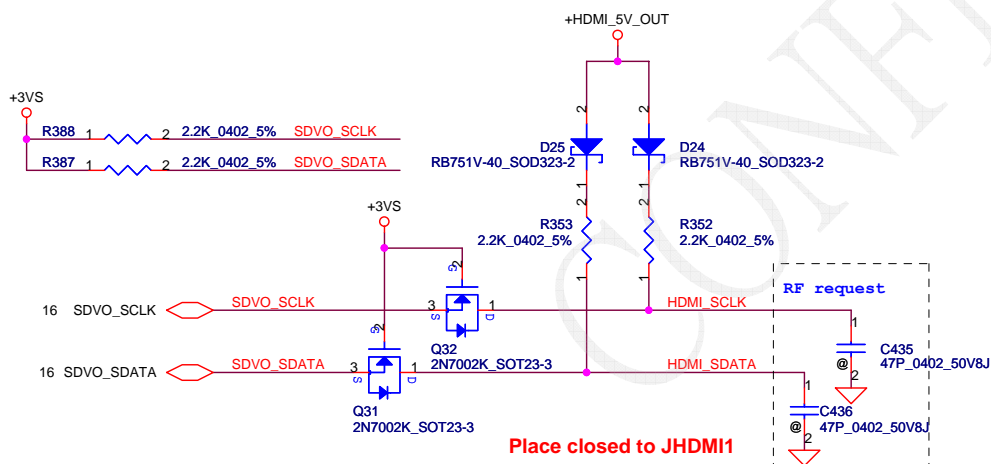
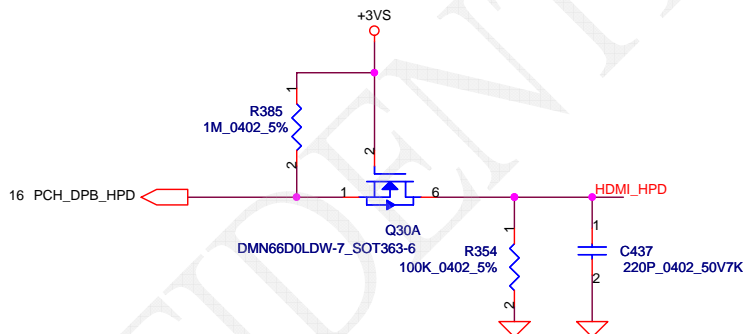
LCD/LED PANEL Conn.



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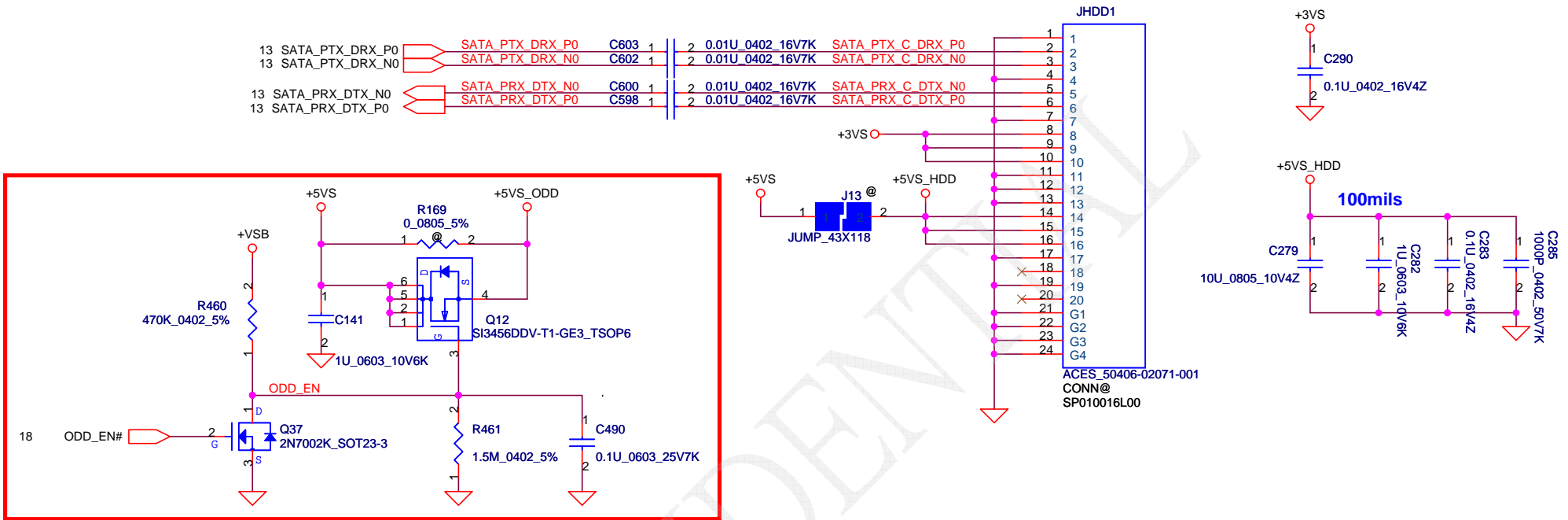


16 PCH_DPB_N0	C7	2	1	0.1U_0402_16V7K	HDMI TX2-
16 PCH_DPB_P0	C6	2	1	0.1U_0402_16V7K	HDMI TX2+
16 PCH_DPB_N1	C11	2	1	0.1U_0402_16V7K	HDMI TX1-
16 PCH_DPB_P1	C10	2	1	0.1U_0402_16V7K	HDMI TX1+
16 PCH_DPB_N2	C9	2	1	0.1U_0402_16V7K	HDMI TX0-
16 PCH_DPB_P2	C8	2	1	0.1U_0402_16V7K	HDMI TX0+
16 PCH_DPB_N3	C13	2	1	0.1U_0402_16V7K	HDMI CLK-
16 PCH_DPB_P3	C12	2	1	0.1U_0402_16V7K	HDMI CLK+

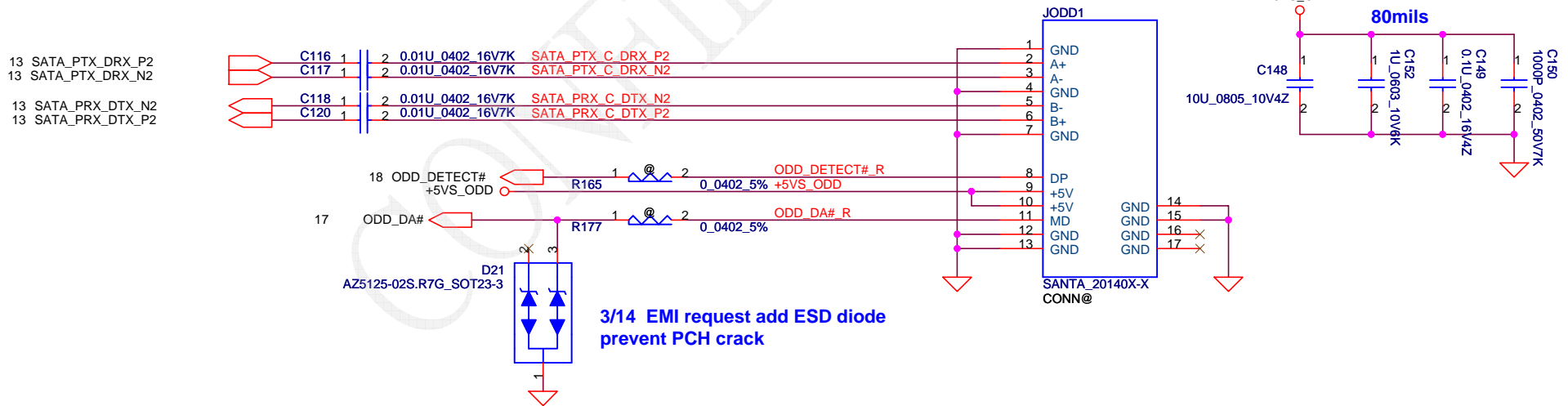


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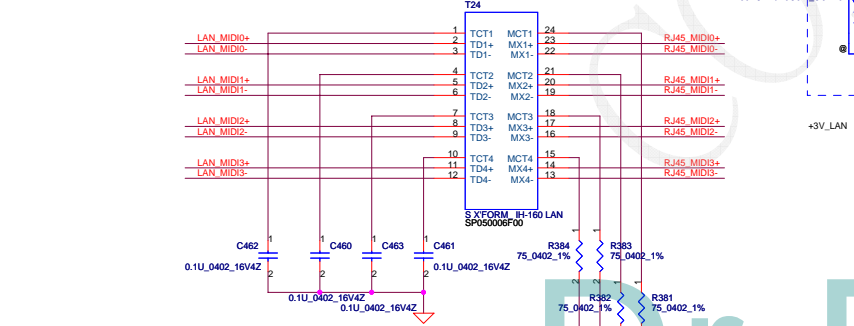
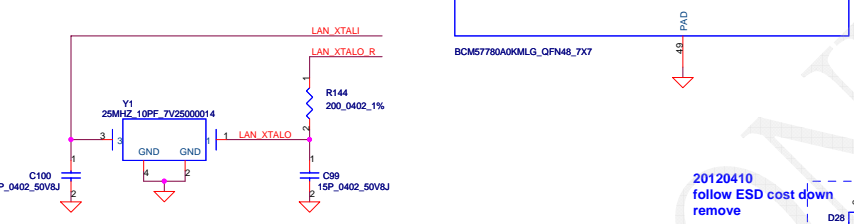
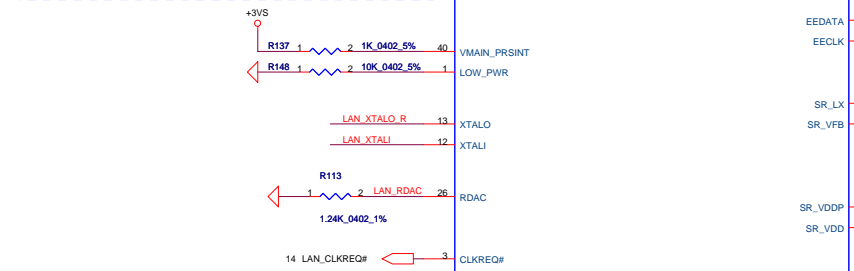
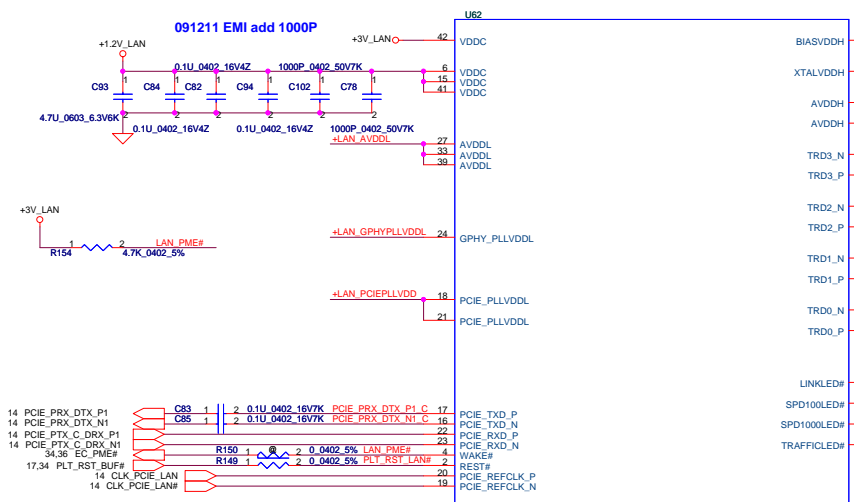
SATA HDD1 Conn.



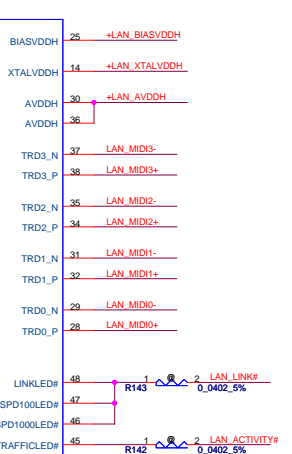
SATA ODD Conn.



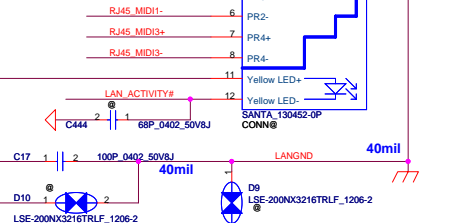
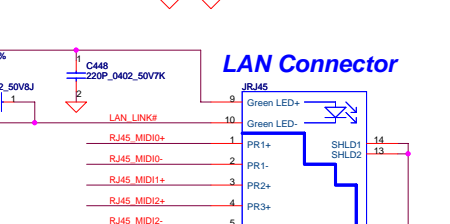
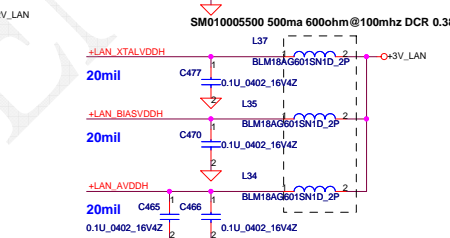
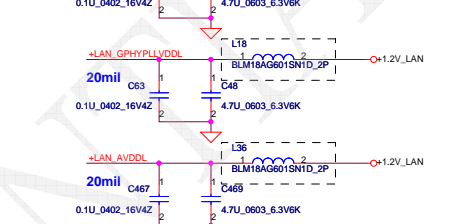
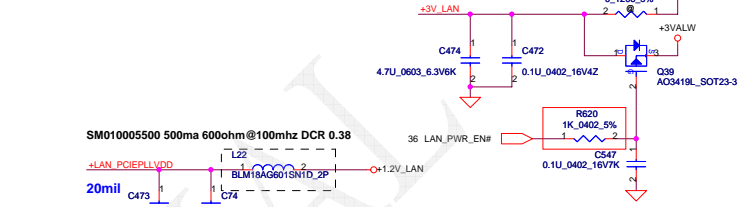
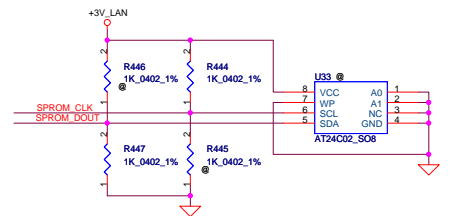
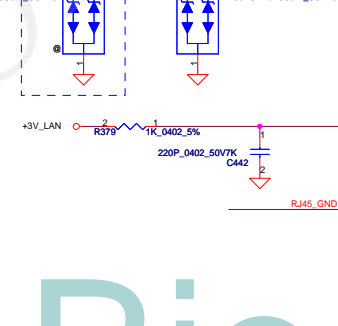
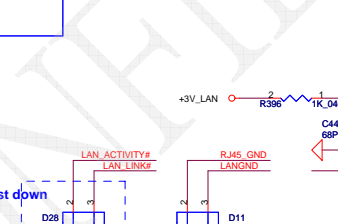
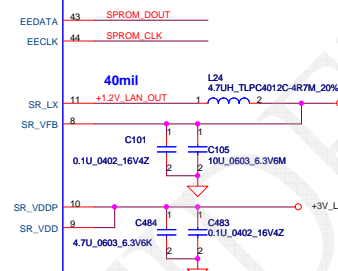
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Place close to TCT pin
 BOTHHAND: S_X'FORM_GST5009-D LFN LAN, SP050006B00 40mil
 TIMAG:S_X'FORM_IH-160 LAN, SP050006F00



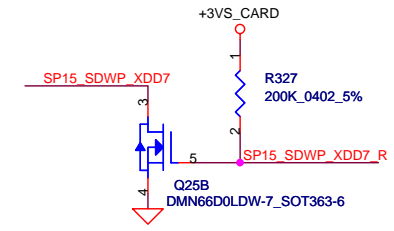
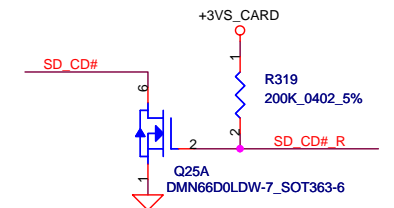
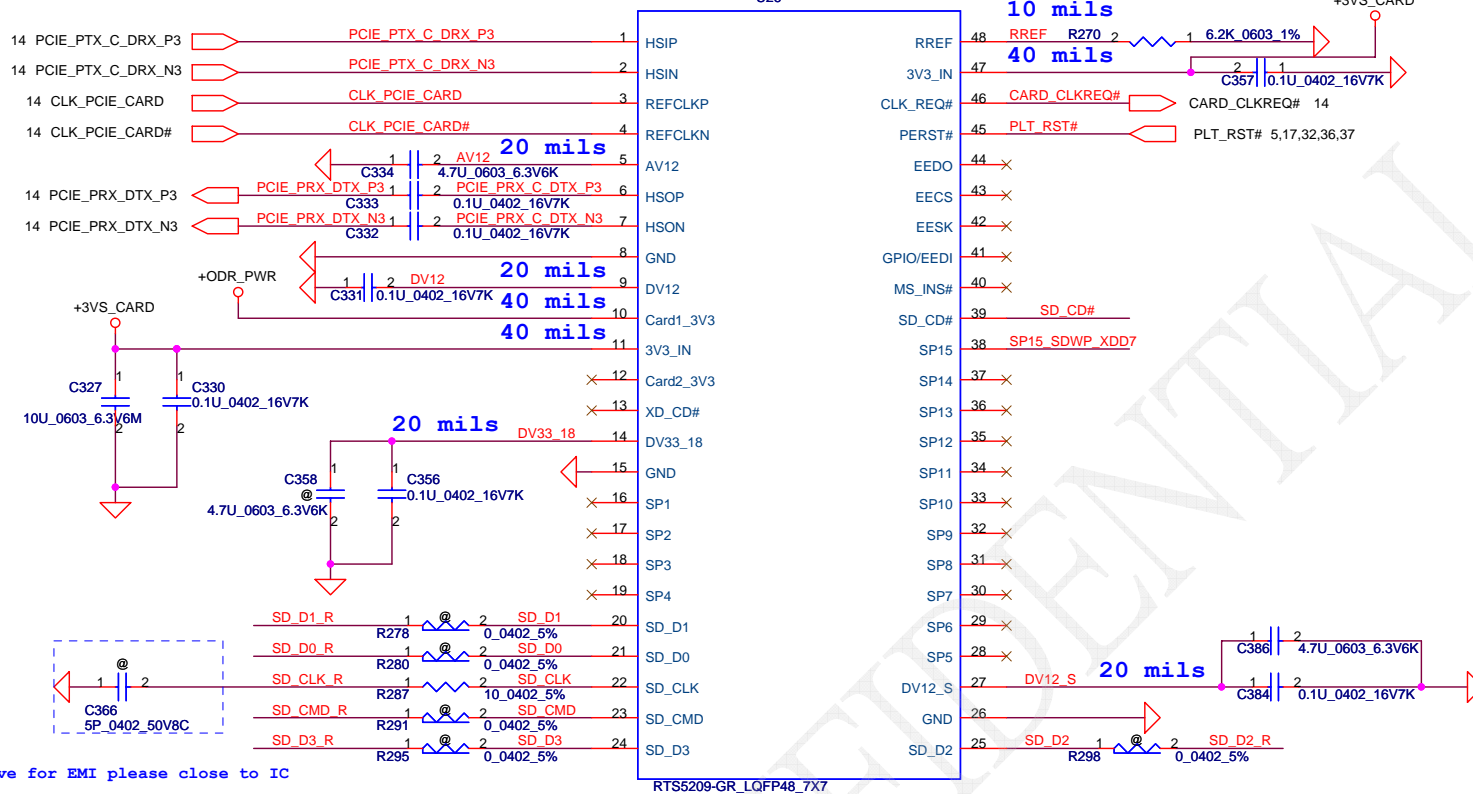
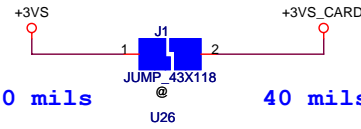
	SPROM_CLK (SECLP)	SPROM_DOUT (SECLP)
On chip	1	0
AT24C02	1	1



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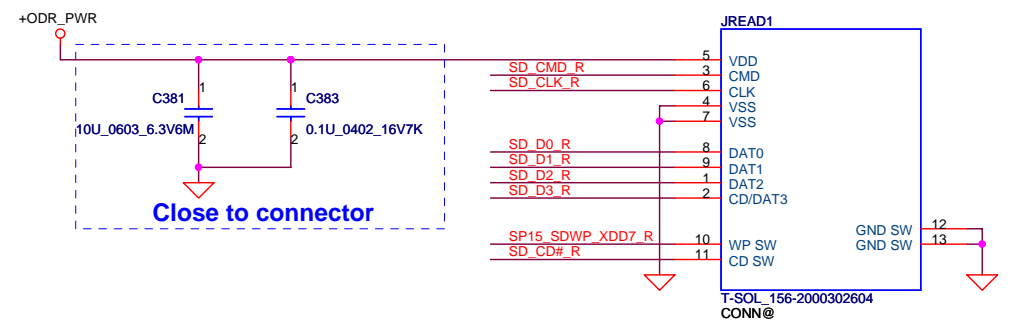
Card Reader

RTS5209-GR_LQFP48_7X7

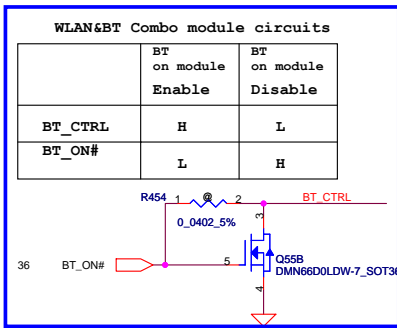


Reserve for EMI please close to IC

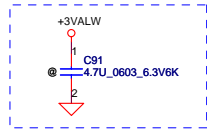
Pin No.	Name
1	DAT2
2	DAT3
3	CMD
4	VSS
5	VDD
6	CLK
7	VSS
8	DAT0
9	DAT1
10	WP Pin (Normal close)
11	CD Pin (Normal close)



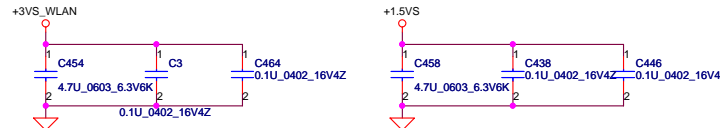
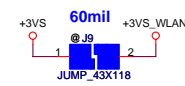
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/24	Deciphered Date	2012/07/12	Title	SCHMATIC MB A8203
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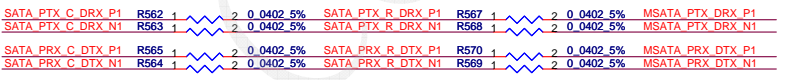
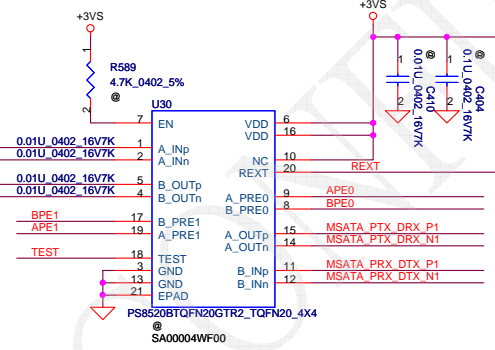
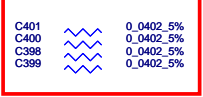
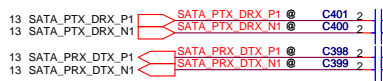
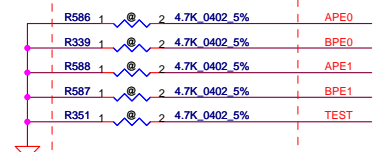
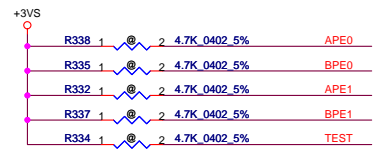
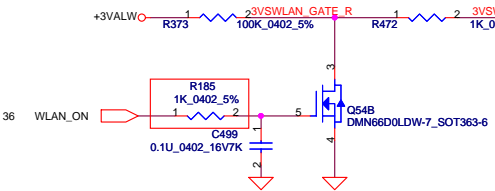
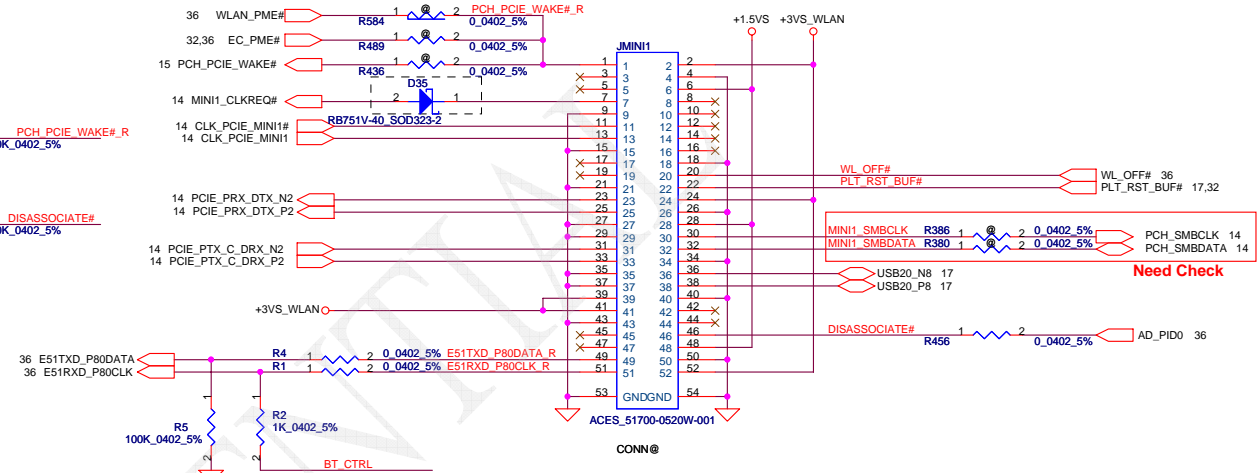
Place near Q47.3



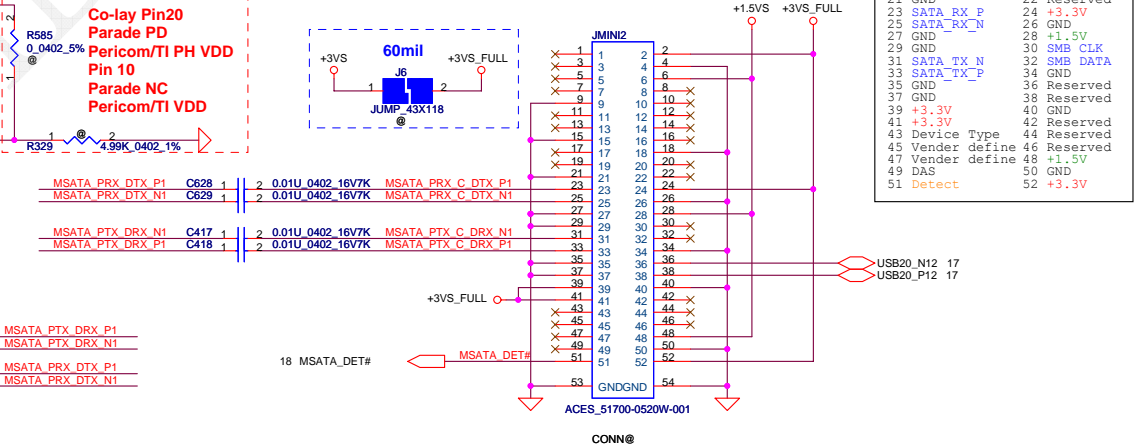
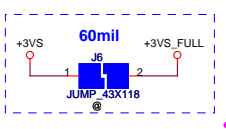
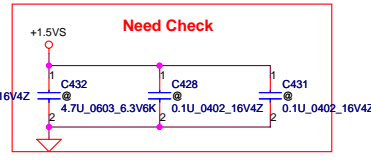
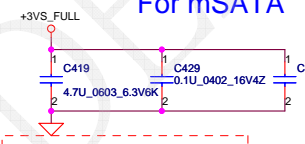
For Wireless LAN



Mini Card Power Rating



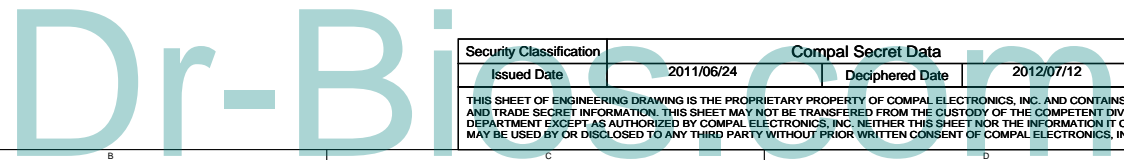
For mSATA



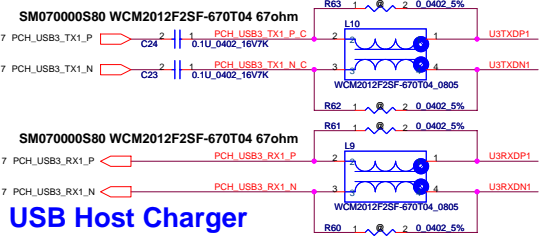
MSATA pin define

1	Reserved	2	+3.3V
3	Reserved	4	GND
5	Reserved	6	+1.5V
7	Reserved	8	Reserved
9	GND	10	Reserved
11	Reserved	12	Reserved
13	Reserved	14	Reserved
15	GND	16	Reserved
17	Reserved	18	GND
19	Reserved	20	Reserved
21	GND	22	Reserved
23	SATA_RX_P	24	+3.3V
25	SATA_TX_N	26	GND
27	GND	28	+1.5V
29	GND	30	SMB_CLK
31	SATA_TX_P	32	SMB_DATA
33	SATA_TX_P	34	GND
35	GND	36	Reserved
37	GND	38	Reserved
39	+3.3V	40	GND
41	+3.3V	42	Reserved
43	Device Type	44	Reserved
45	Vendor define	46	Reserved
47	Vendor define	48	+1.5V
49	DAS	50	GND
51	Detect	52	+3.3V

MSATA SATA3.0 Repeater

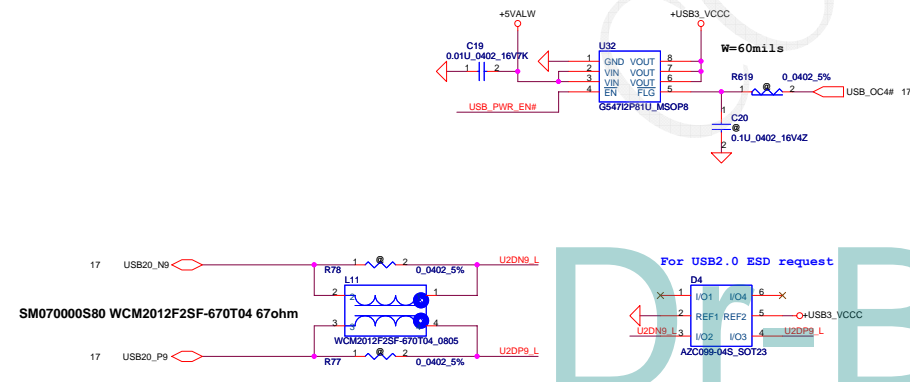
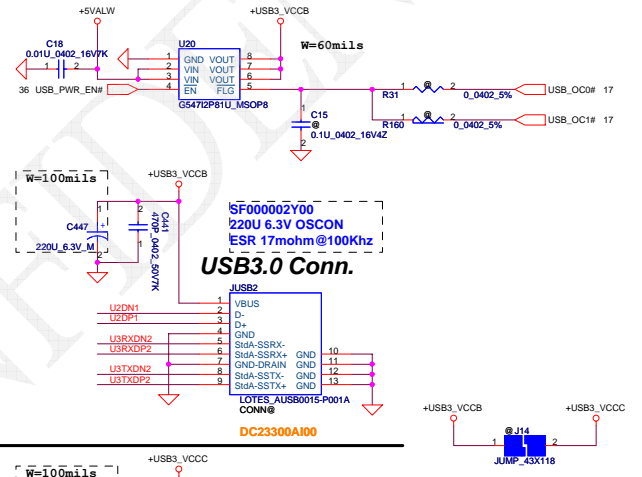
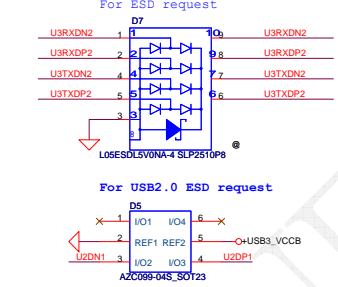
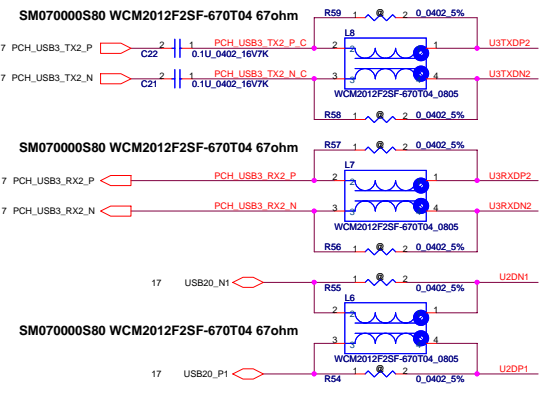
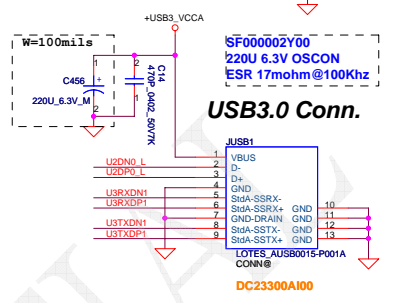
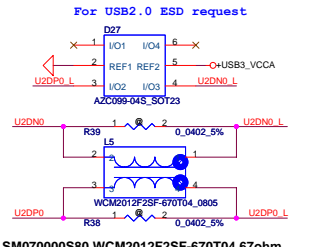
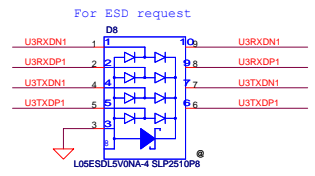
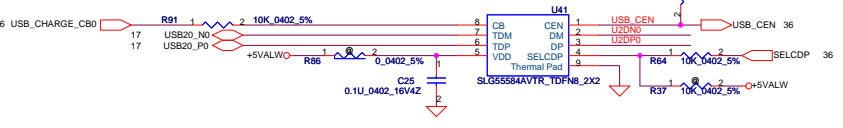


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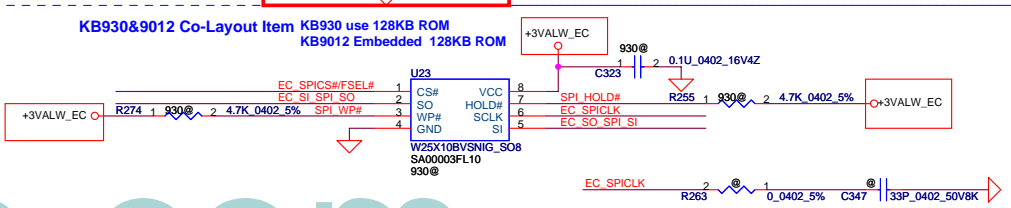
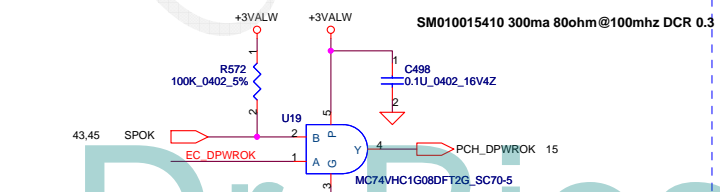
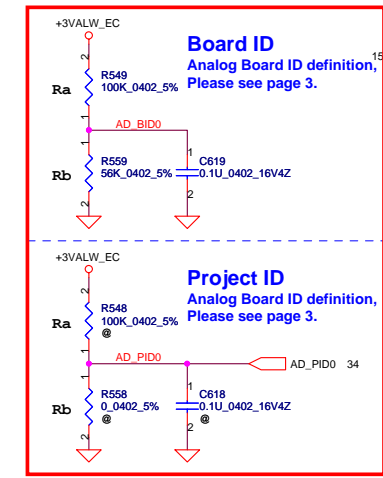
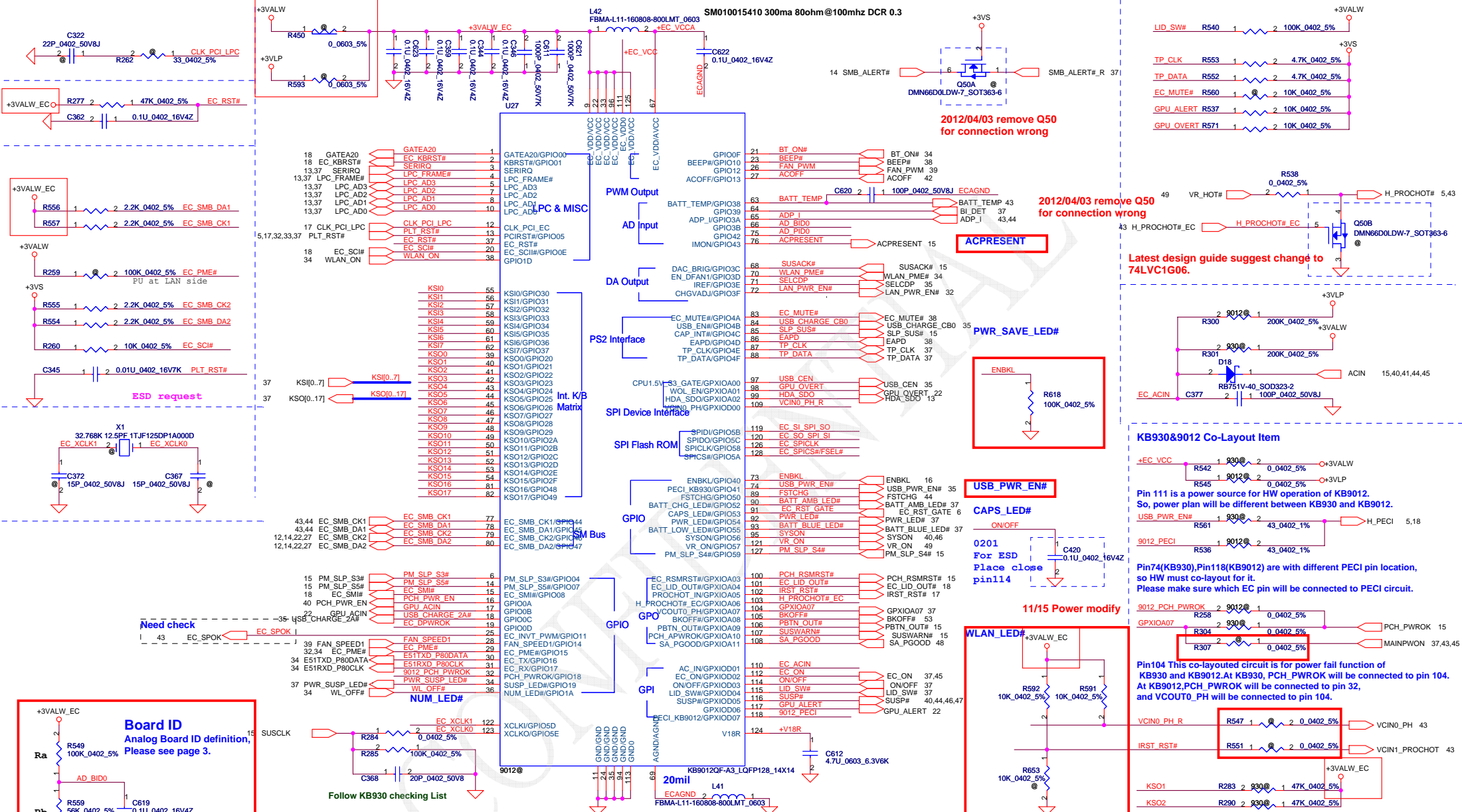


USB Host Charger

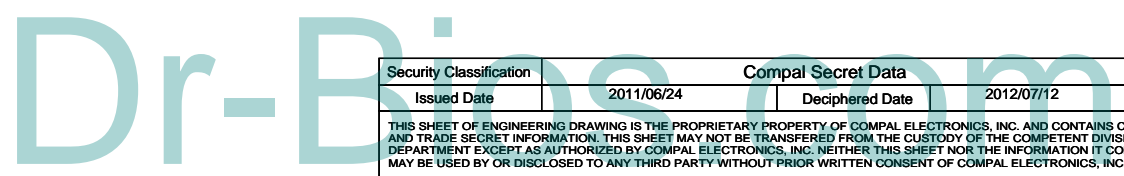
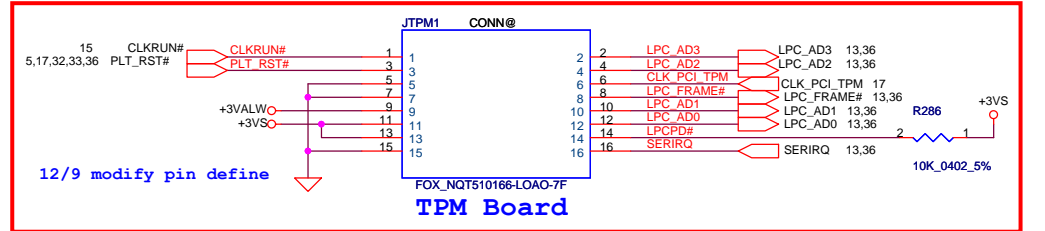
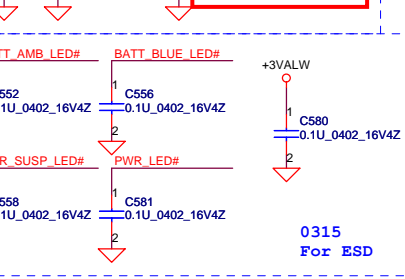
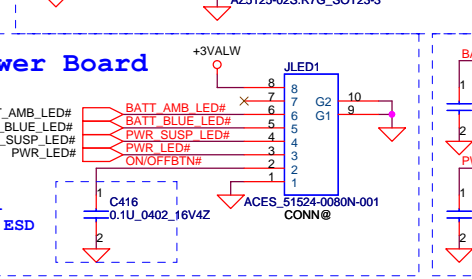
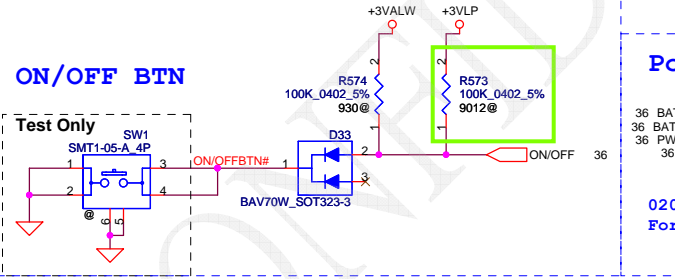
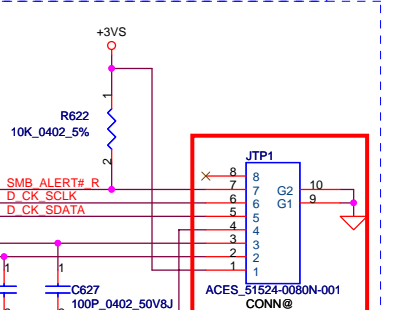
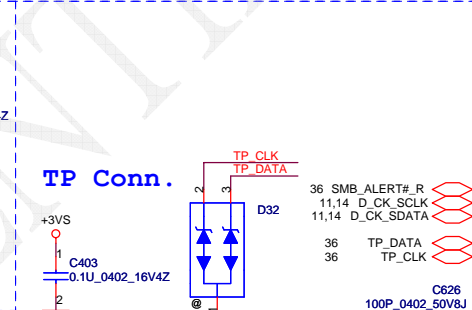
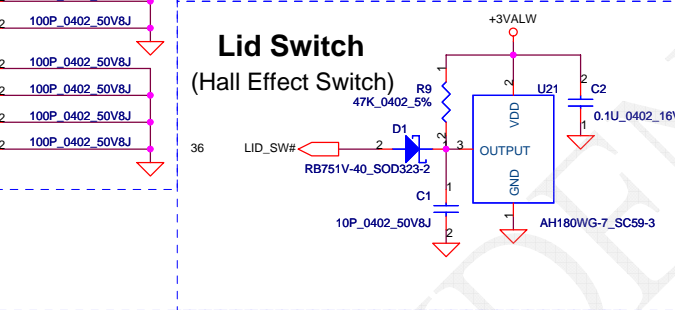
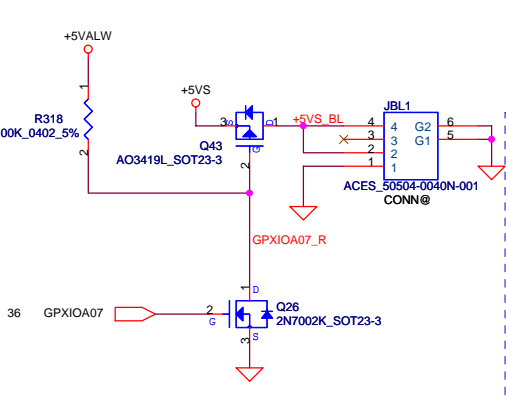
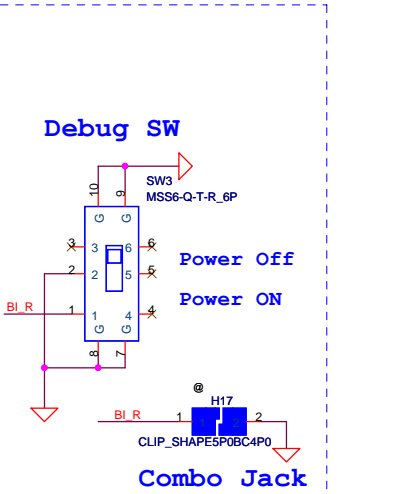
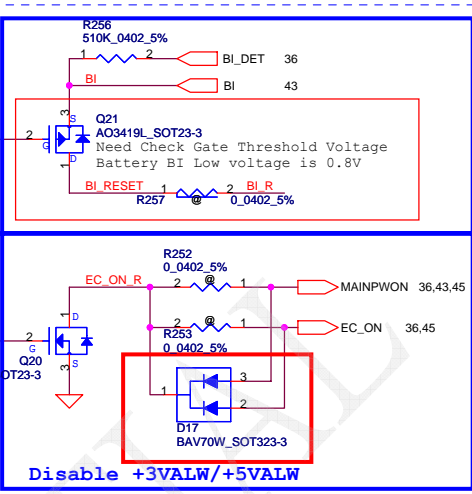
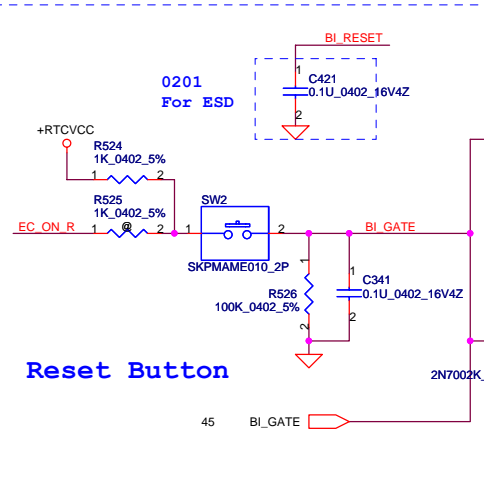
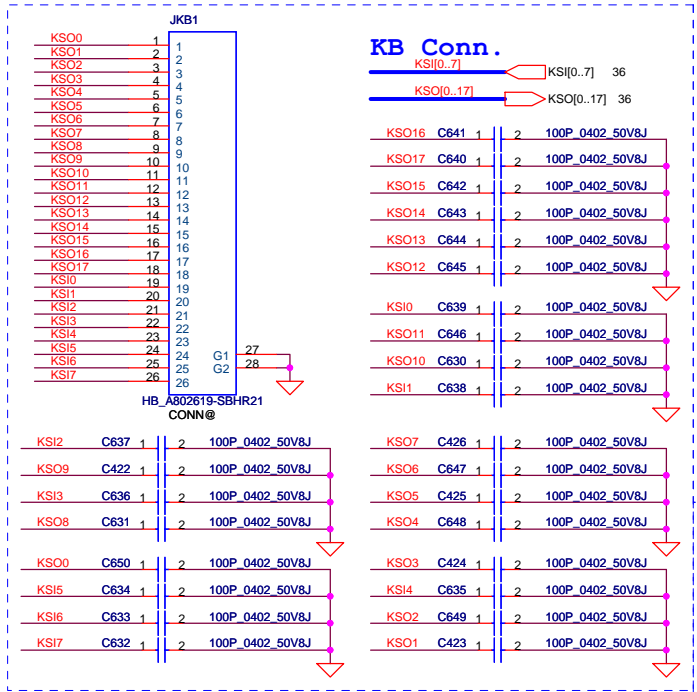
CB	SELCDP	
0	X	DCP(Dedicated Charging Port) autdetect with mouse/keyboard wakeup
1	0	S0 charging with SDP(Standard Downstream Port) only
1	1	S0 charging with CDP(Charging Downstream Port) or SDP only



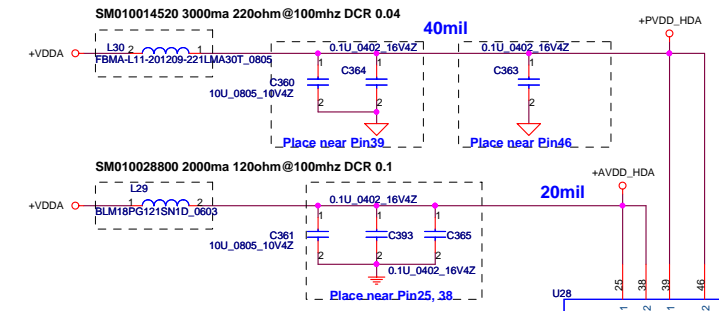
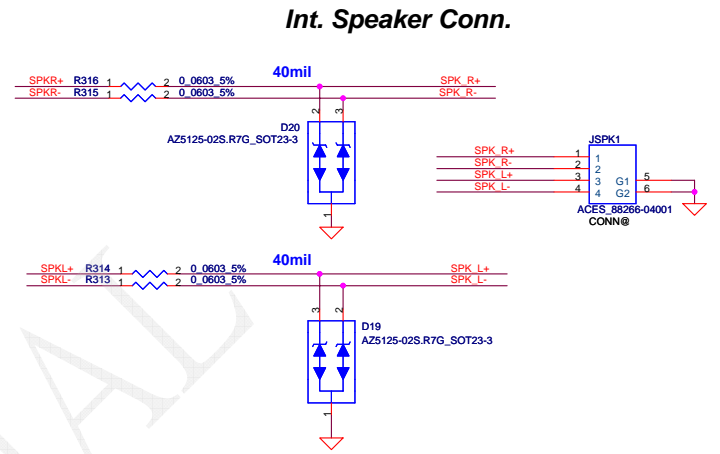
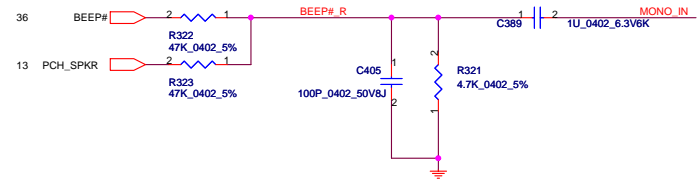
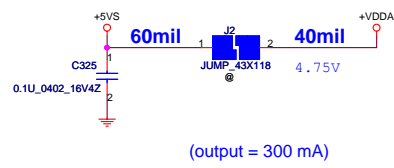
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Issued Date	2011/06/24	Deciphered Date	2012/07/12	Schematic MB A8203	
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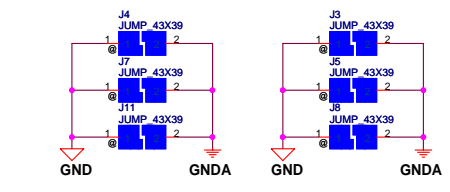
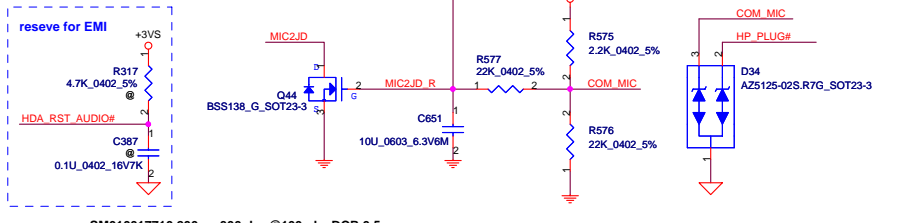
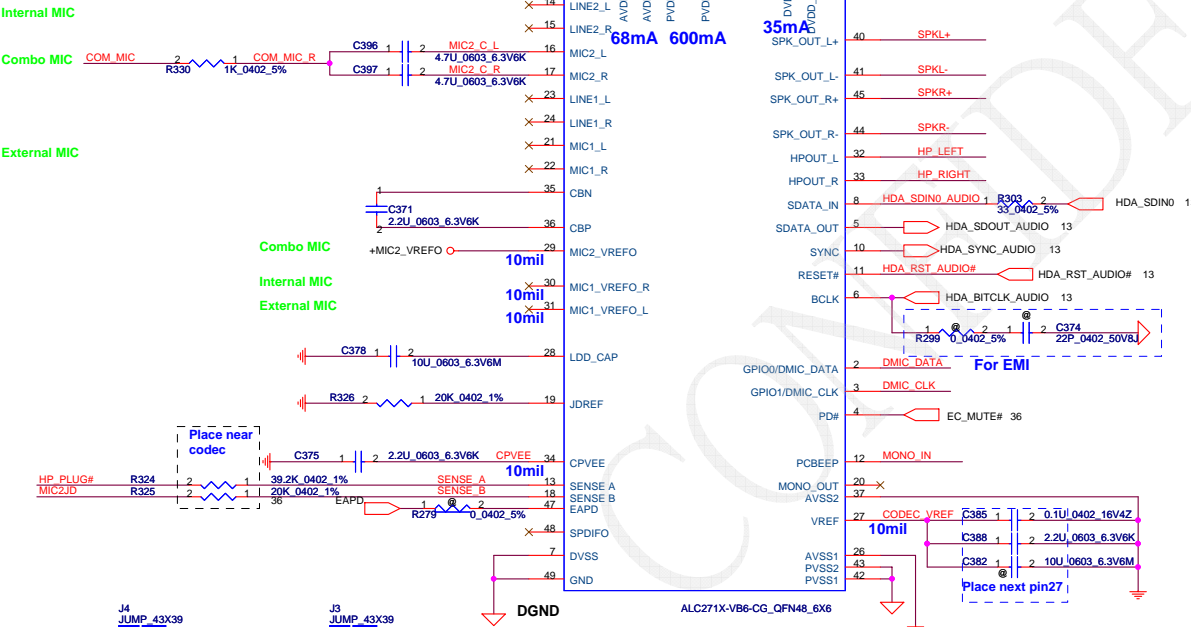
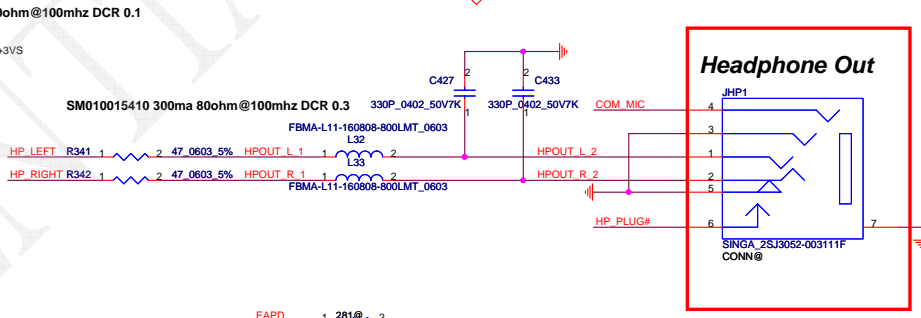
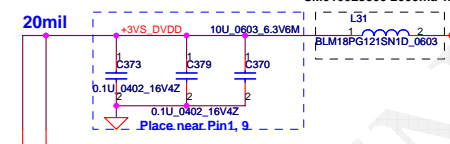
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Issued Date	2011/06/24	Deciphered Date	2012/07/12	SCHEMATIC MB A8203	
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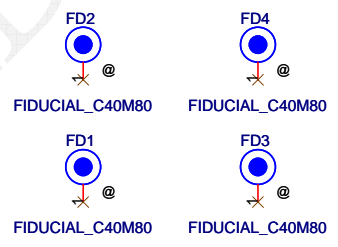
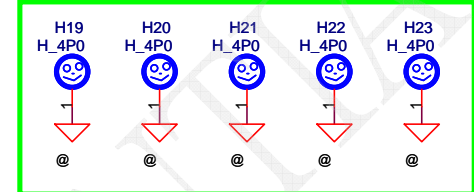
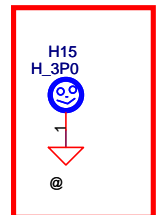
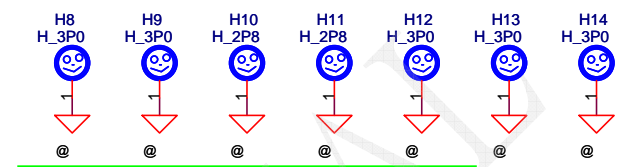
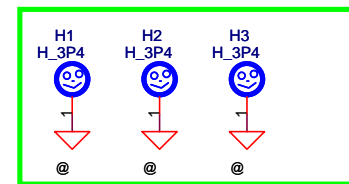
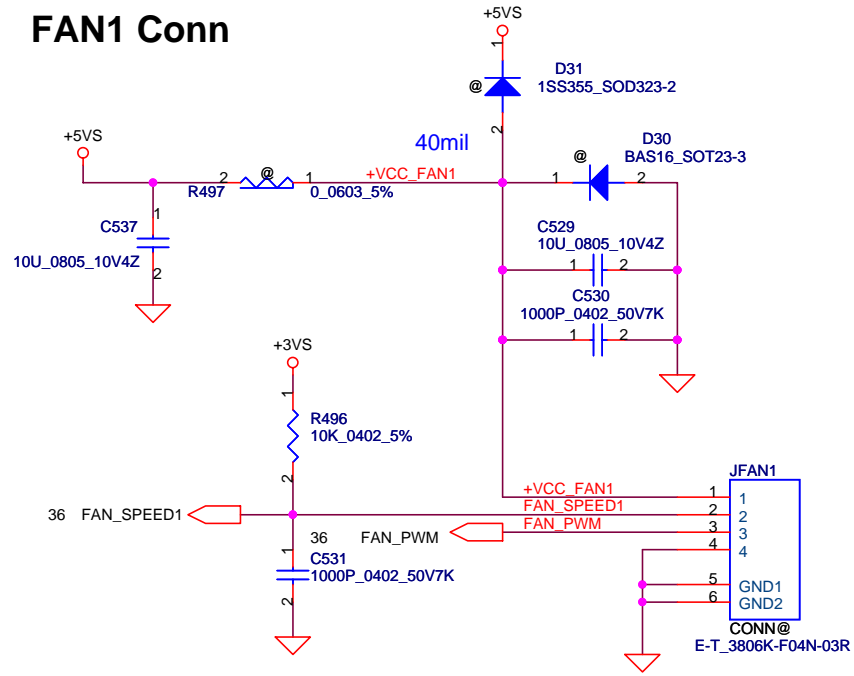


HD Audio Codec



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FAN1 Conn



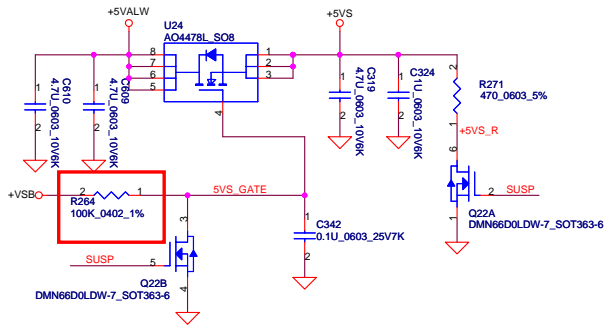
WLAN+MSATA Stand off

CPU,VGA support plate

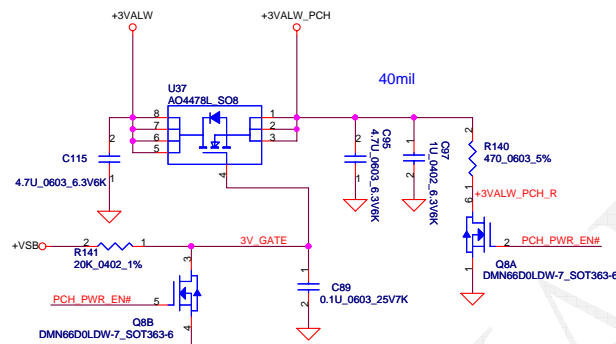
locate MB

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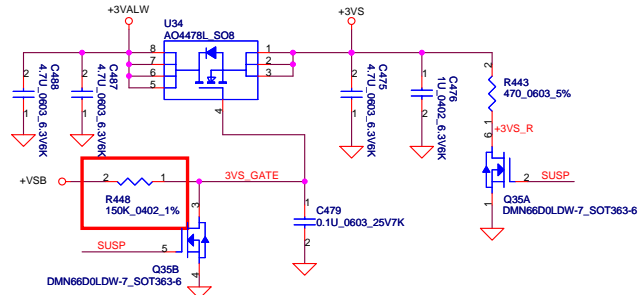
+5VALW TO +5VS



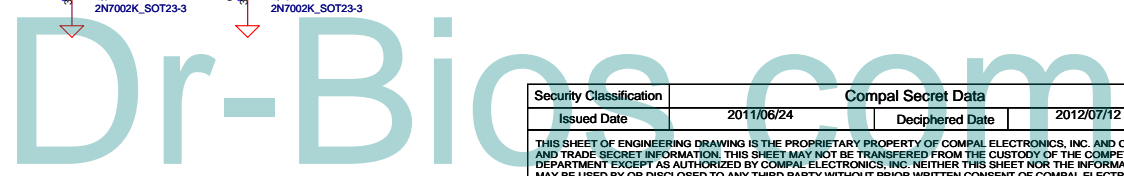
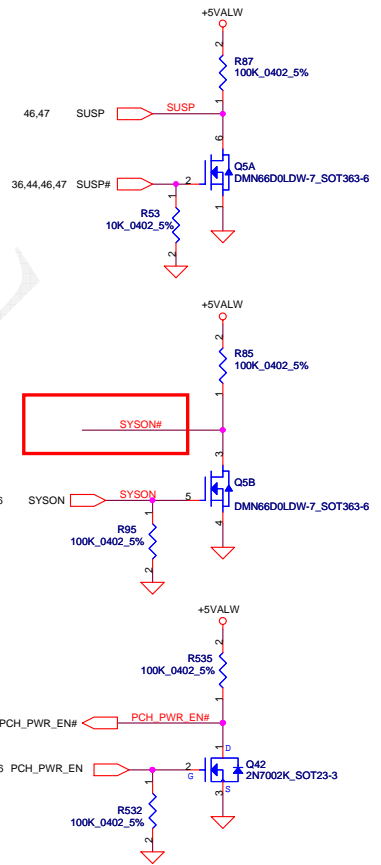
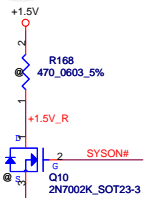
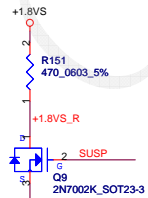
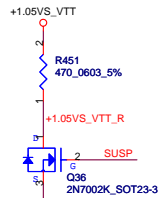
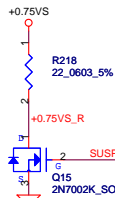
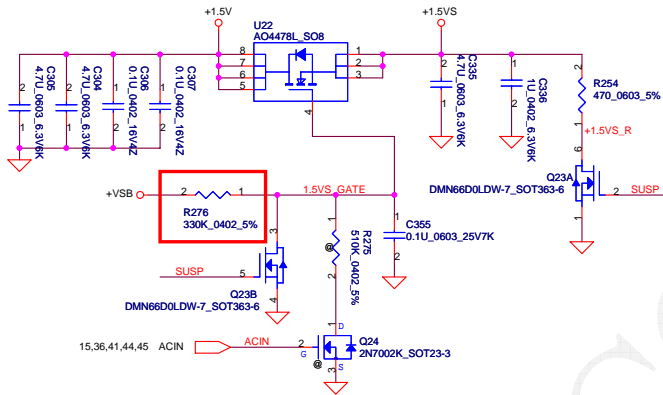
+3VALW TO +3VALW (PCH AUX Power)
Short J5 for PCH VCCSUS3.3



+3VALW TO +3VS

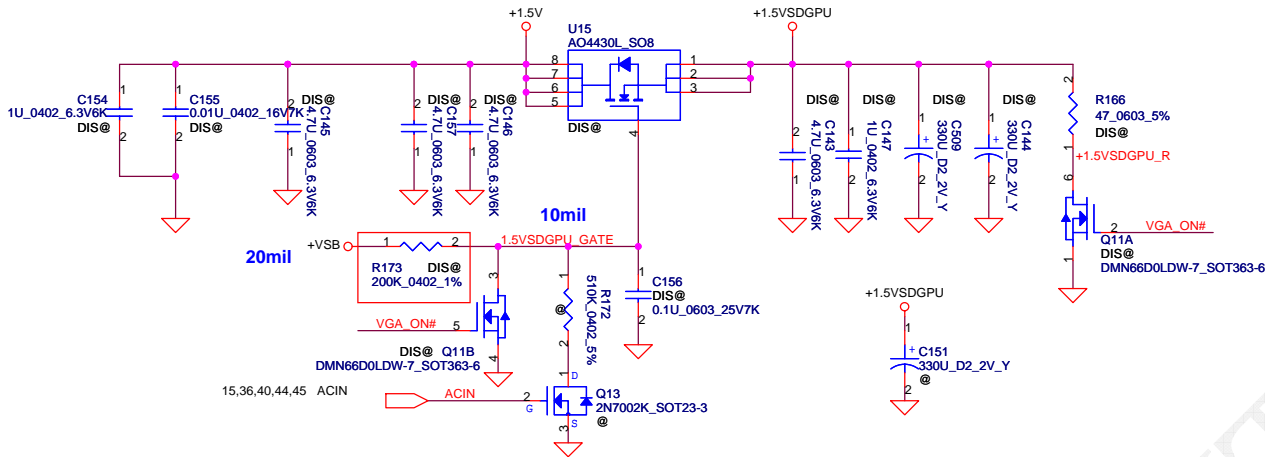


+1.5V to +1.5VS

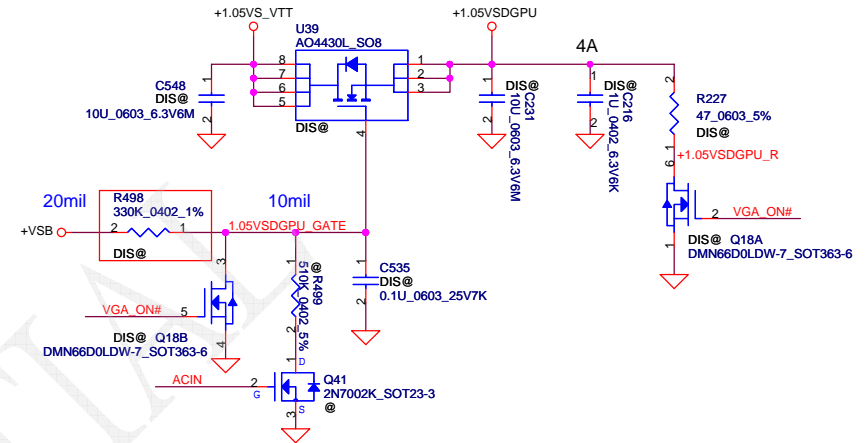


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			Rev C
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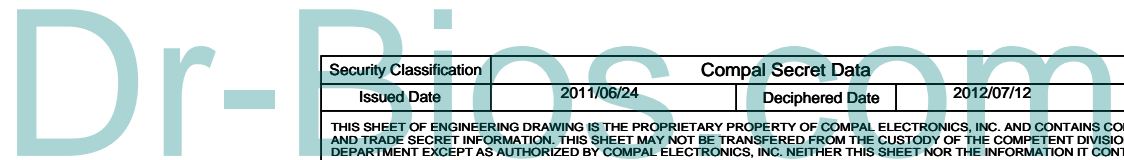
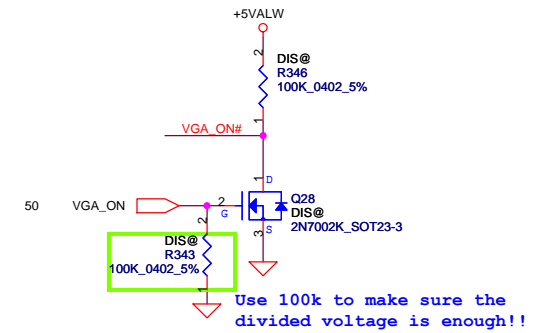
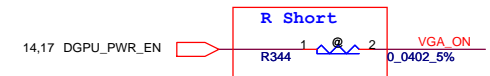
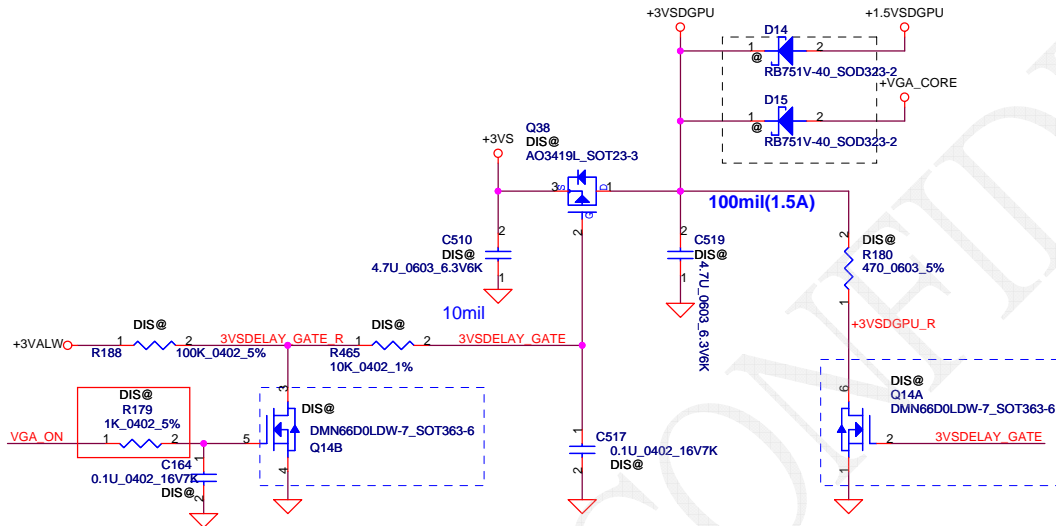
+1.5VSDGPU to +1.5VSDGPU for GPU



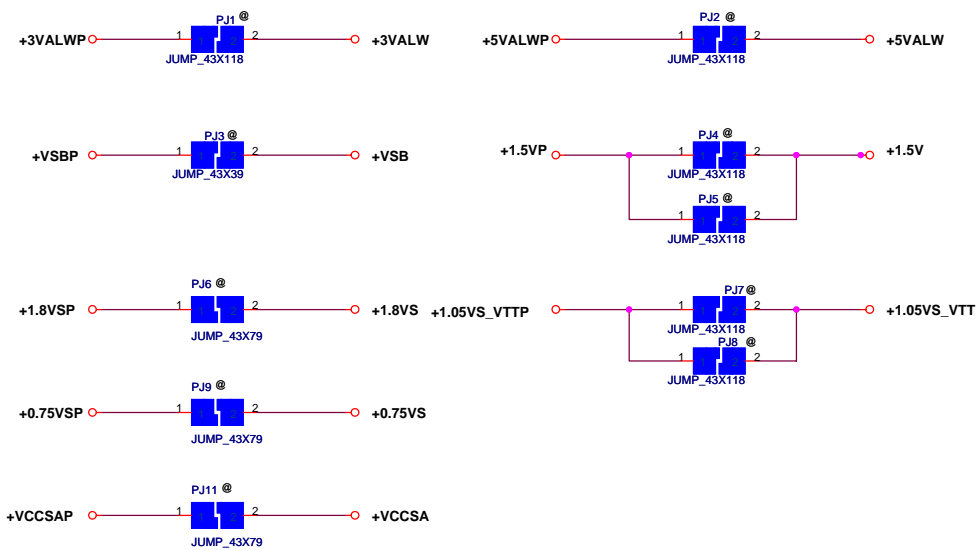
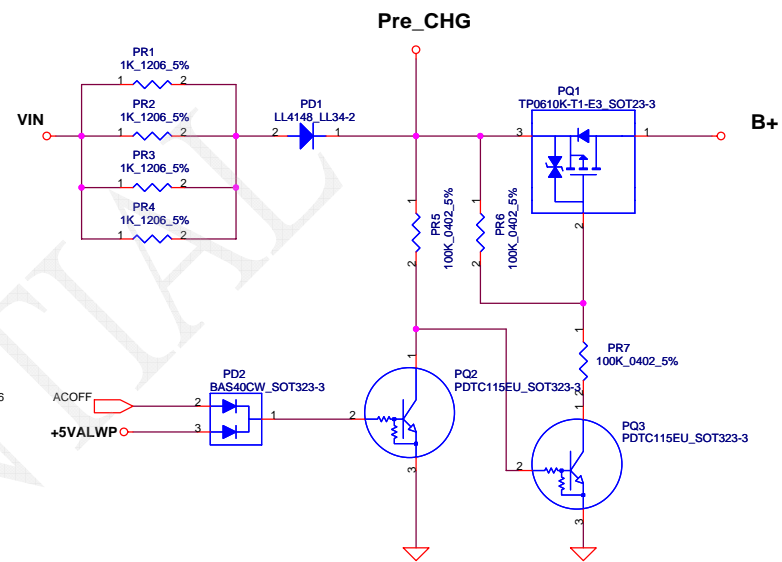
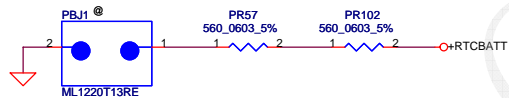
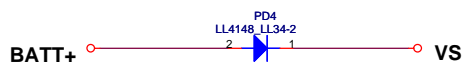
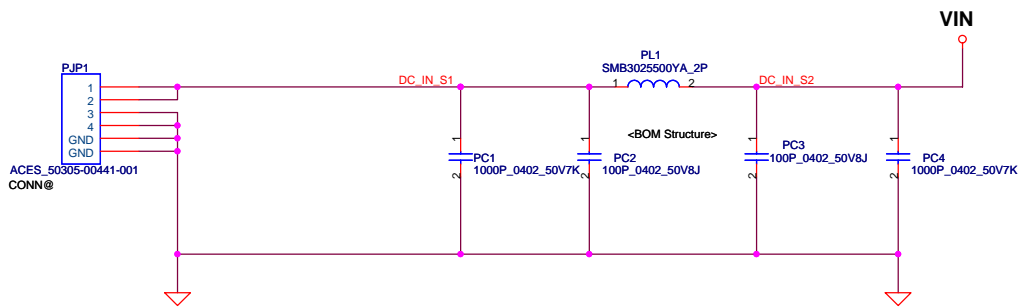
+1.05VS_VTT to +1.05VSDGPU for GPU



+3VS to +3VSDGPU for GPU



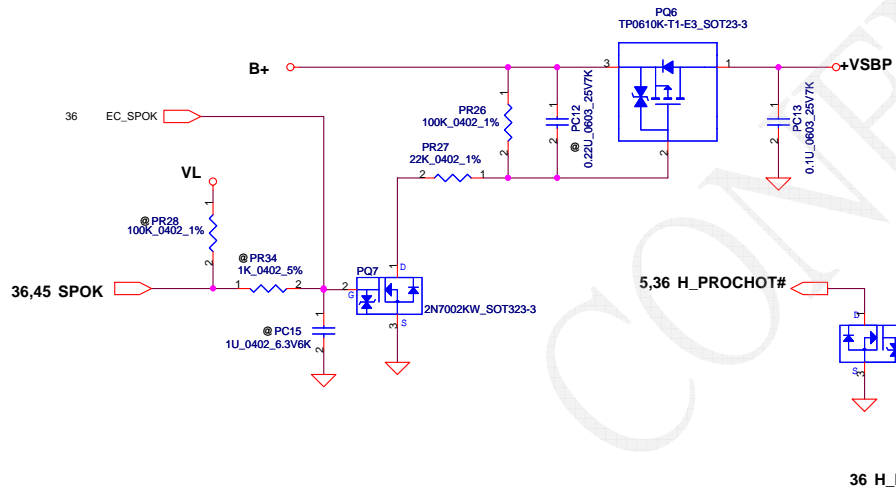
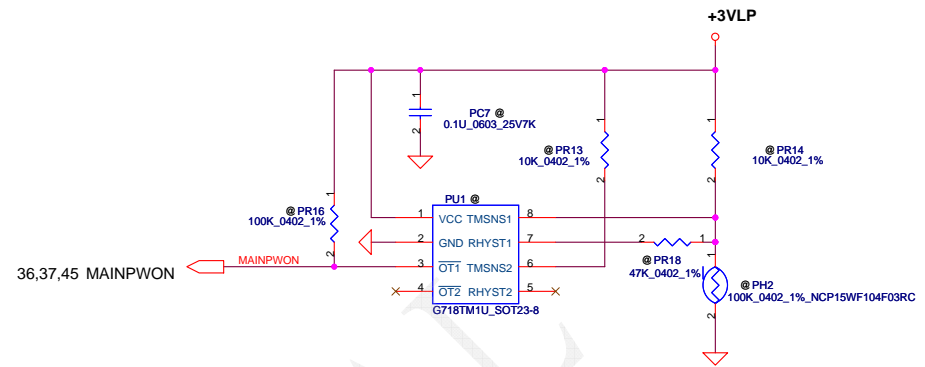
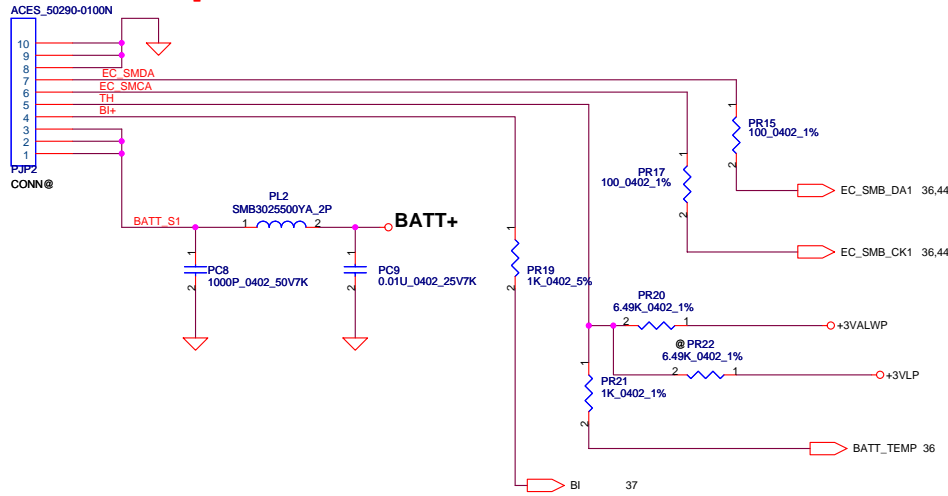
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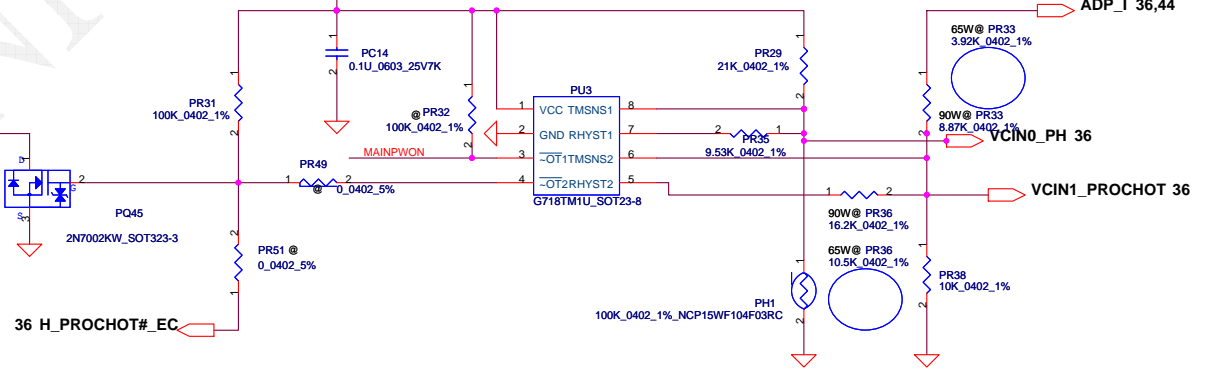
PJP3 has not link yet



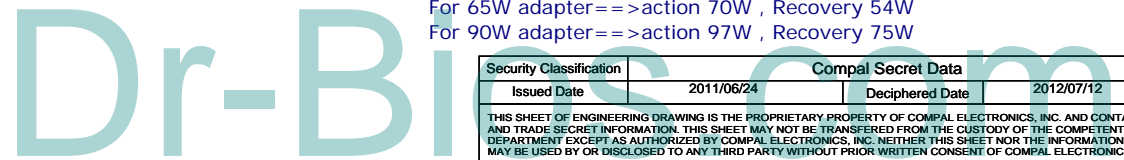
PH1 under CPU bottom side :
CPU thermal protection at 90 degree C (shutdown)

+3VLP Recovery at 56 degree C

ADP_I > 1.28V ,
CPU will throttling

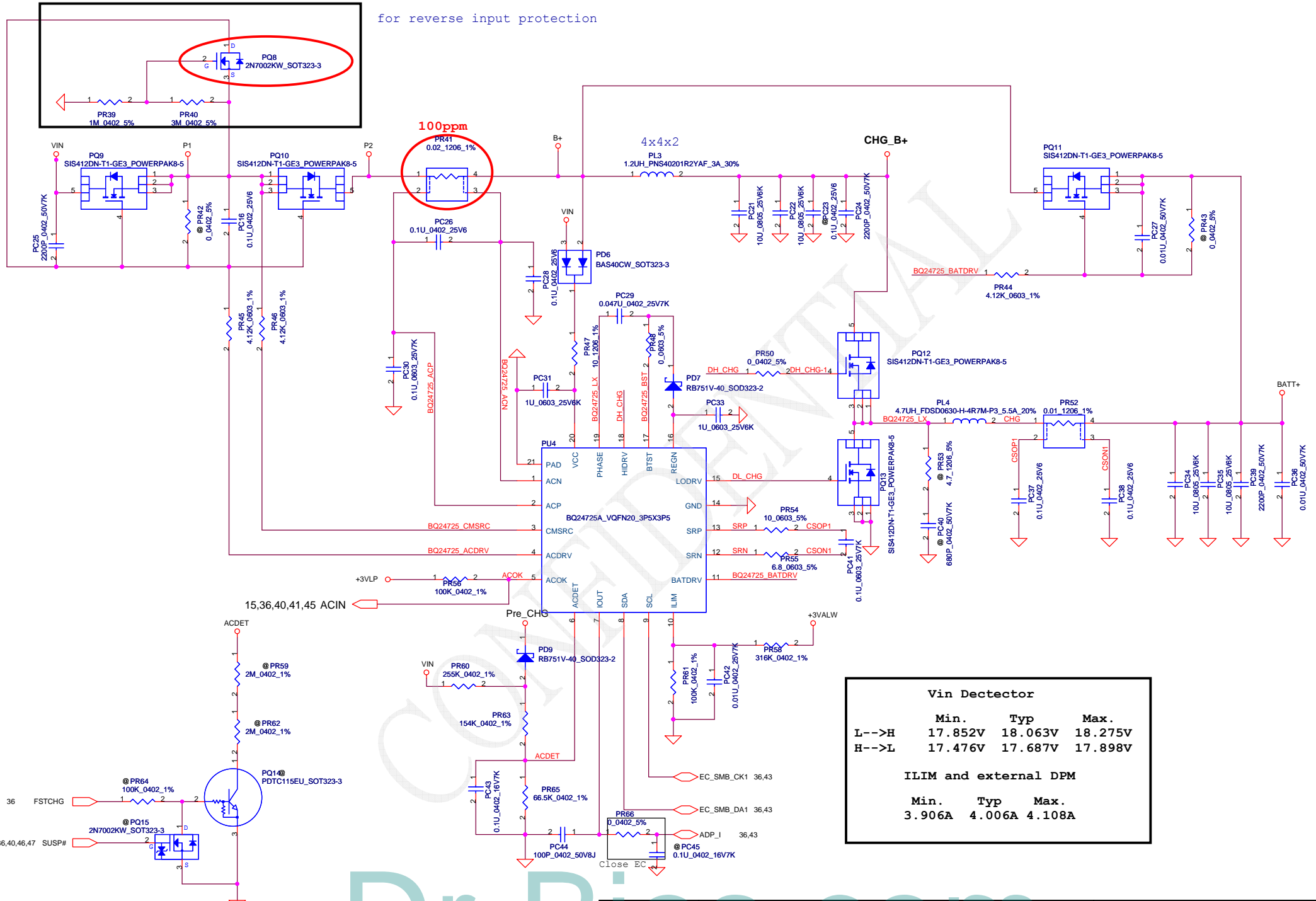


For 65W adapter ==> action 70W , Recovery 54W
For 90W adapter ==> action 97W , Recovery 75W



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for reverse input protection



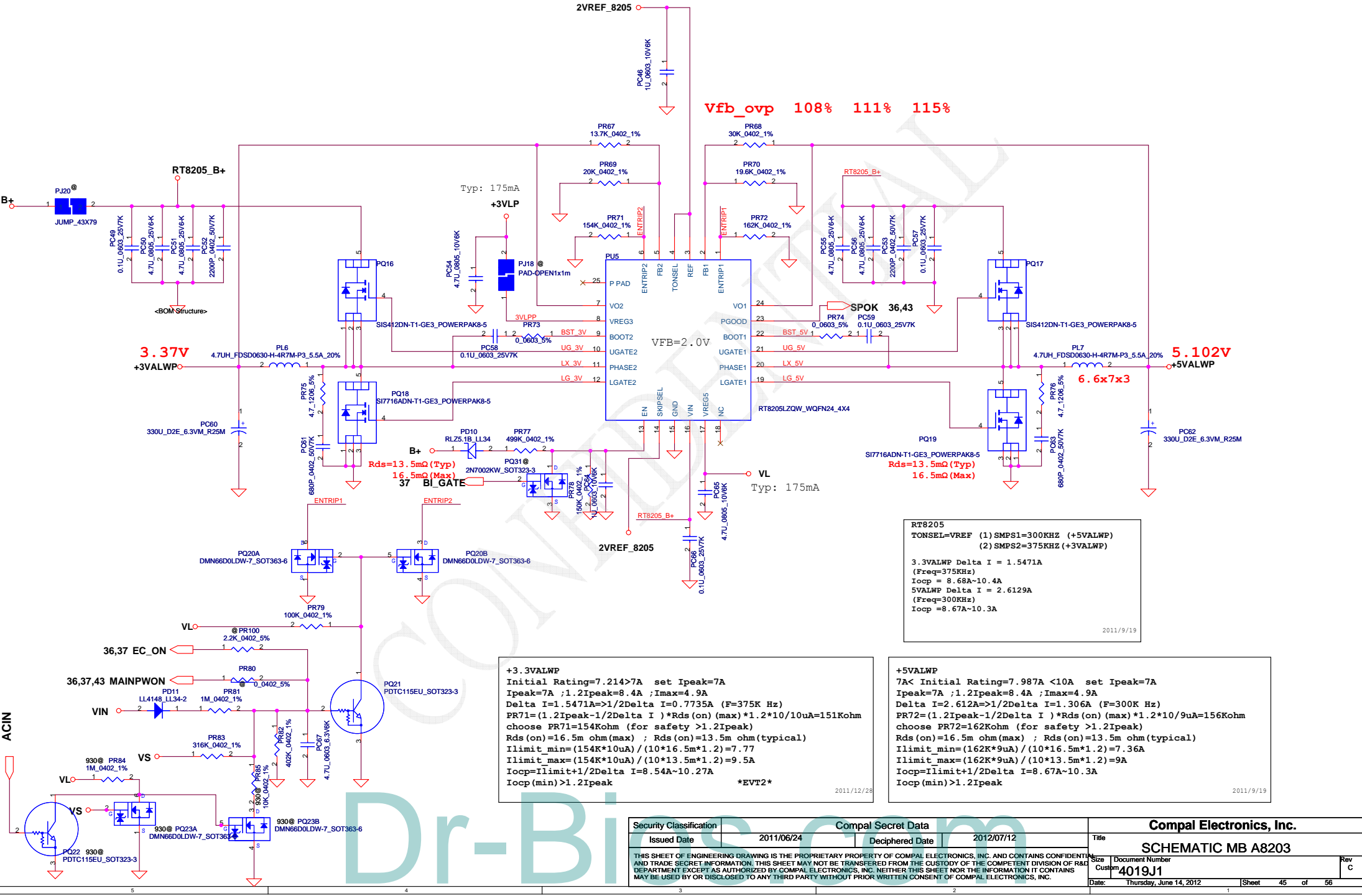
Vin Dectector			
	Min.	Typ	Max.
L-->H	17.852V	18.063V	18.275V
H-->L	17.476V	17.687V	17.898V

ILIM and external DPM			
	Min.	Typ	Max.
	3.906A	4.006A	4.108A

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Note:
 Use TPS51125 IC can remove RTC refernece LDO
 Use TPS51427 IC must keep RTC refernece LDO



Vfb_ovp 108% 111% 115%

3.37V
+3VALWP

5.102V
+5VALWP

VFB=2.0V

RT8205
 TONSEL=VREF (1) SMPS1=300KHZ (+5VALWP)
 (2) SMPS2=375KHZ (+3VALWP)
 3.3VALWP Delta I = 1.5471A
 (Freq=375KHz)
 Iocp = 8.68A-10.4A
 5VALWP Delta I = 2.6129A
 (Freq=300KHz)
 Iocp = 8.67A-10.3A
 2011/9/19

+3.3VALWP
 Initial Rating=7.214>7A set Ipeak=7A
 Ipeak=7A ; 1.2Ipeak=8.4A ; Imax=4.9A
 Delta I=1.5471A=>1/2Delta I=0.7735A (F=375K Hz)
 PR71=(1.2Ipeak-1/2Delta I) *Rds (on) (max) *1.2*10/10uA=151Kohm
 choose PR71=154Kohm (for safety >1.2Ipeak)
 Rds (on)=16.5m ohm(max) ; Rds (on)=13.5m ohm(typical)
 Ilimit_min=(154K*10uA) / (10*16.5m*1.2)=7.77
 Ilimit_max=(154K*10uA) / (10*13.5m*1.2)=9.5A
 Iocp=Ilimit+1/2Delta I=8.54A-10.27A
 Iocp (min)>1.2Ipeak *EVT2*
 2011/12/28

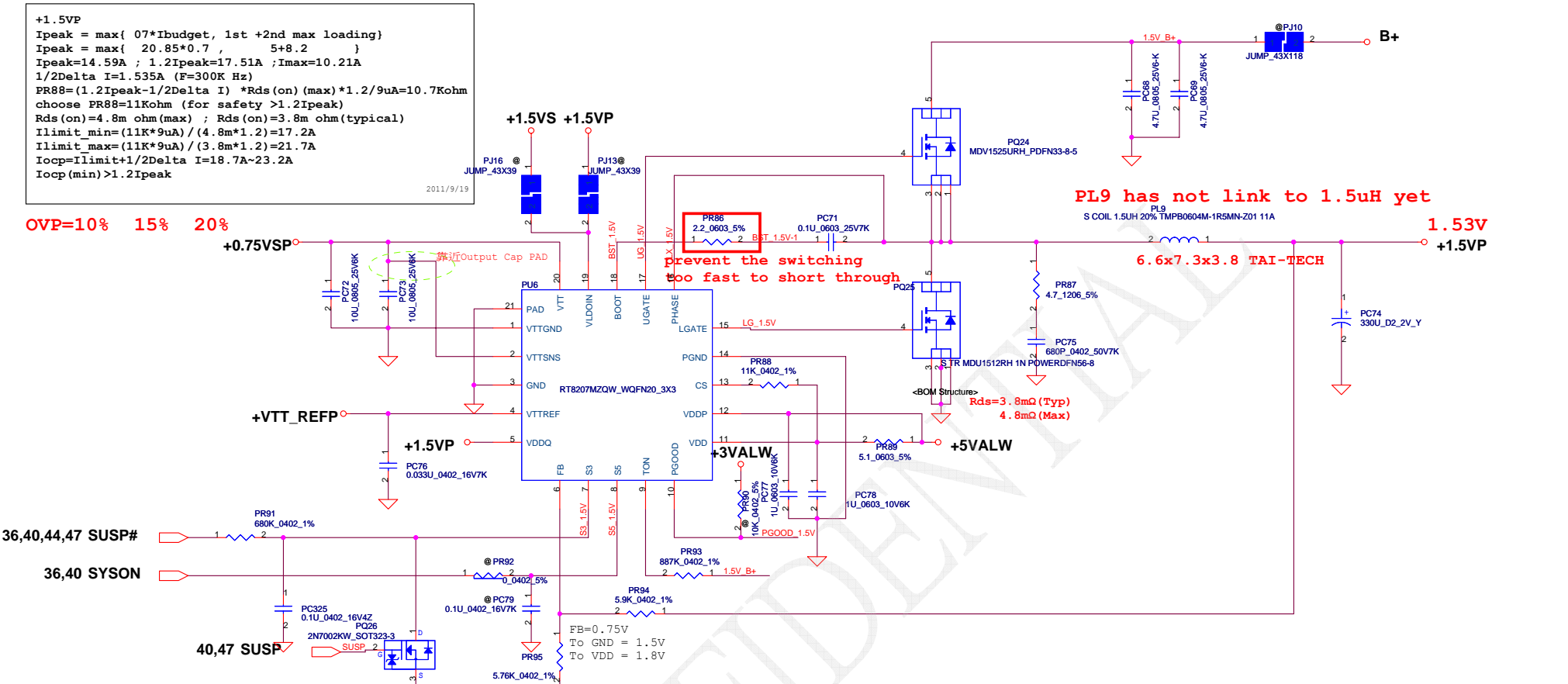
+5VALWP
 7A< Initial Rating=7.987A <10A set Ipeak=7A
 Ipeak=7A ; 1.2Ipeak=8.4A ; Imax=4.9A
 Delta I=2.612A=>1/2Delta I=1.306A (F=300K Hz)
 PR72=(1.2Ipeak-1/2Delta I) *Rds (on) (max) *1.2*10/9uA=156Kohm
 choose PR72=162Kohm (for safety >1.2Ipeak)
 Rds (on)=16.5m ohm(max) ; Rds (on)=13.5m ohm(typical)
 Ilimit_min=(162K*9uA) / (10*16.5m*1.2)=7.36A
 Ilimit_max=(162K*9uA) / (10*13.5m*1.2)=9A
 Iocp=Ilimit+1/2Delta I=8.67A-10.3A
 Iocp (min)>1.2Ipeak
 2011/9/19

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```

+1.5VP
Ipeak = max( 07*Ibudget, 1st +2nd max loading)
Ipeak = max( 20.85*0.7, 5+8.2 )
Ipeak=14.59A ; 1.2Ipeak=17.51A ;Imax=10.21A
1/2Delta I=1.535A (F=300K Hz)
PR88=(1.2Ipeak-1/2Delta I) *Rds(on) (max)*1.2/9uA=10.7Kohm
choose PR88=11Kohm (for safety >1.2Ipeak)
Rds(on)=4.8m ohm(max) ; Rds(on)=3.8m ohm(typical)
Ilimit_min=(11K*9uA) / (4.8m*1.2)=17.2A
Ilimit_max=(11K*9uA) / (3.8m*1.2)=21.7A
Iocp=Ilimit+1/2Delta I=18.7A~23.2A
Iocp (min) >1.2Ipeak
    
```

OVP=10% 15% 20%



36,40,44,47 SUSP#
36,40 SYSON

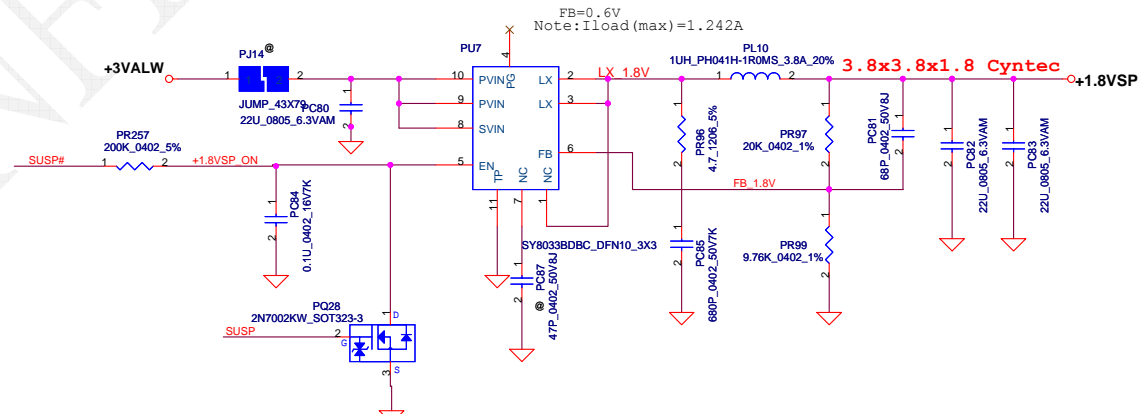
STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)

Note: S3 - sleep ; S5 - power off

UMA

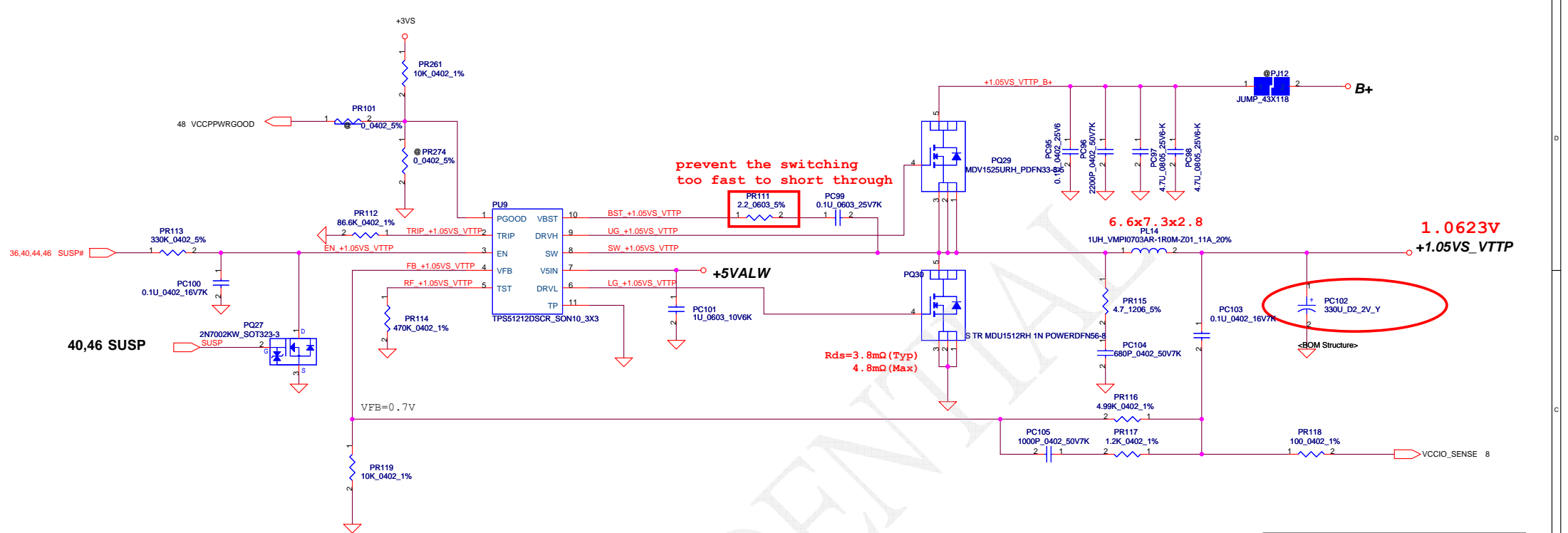
```

+1.5VP
Ipeak = max( 07*Ibudget, 1st +2nd max loading)
Ipeak = max( 15.05*0.7, 5+8.2 )
Ipeak=13.2A ; 1.2Ipeak=15.84A ;Imax=9.24A
1/2Delta I=1.535A (F=300K Hz)
PR88=(1.2Ipeak-1/2Delta I) *Rds(on) (max)*1.2/9uA=9.16Kohm
choose PR88=9.53Kohm (for safety >1.2Ipeak)
Rds(on)=4.8m ohm(max) ; Rds(on)=3.8m ohm(typical)
Ilimit_min=(11K*9uA) / (4.8m*1.2)=14.9A
Ilimit_max=(11K*9uA) / (3.8m*1.2)=18.8A
Iocp=Ilimit+1/2Delta I=16.4A~20.3A
Iocp (min) >1.2Ipeak
    
```



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Note: Use VCCSA_SEL to switch High & Low Level for VID[1]



prevent the switching too fast to short through

PR111
2.2_0603_5%
1 2

Rds=3.8mΩ (Typ)
4.8mΩ (Max)

1.0623V
+1.05VS_VTTP

VFB = 0.704V
Vo = VFB * (1 + PR116 + PR118 / PR119) = 1.05V
Freq = 266~314KHz, 290KHz (typ)

OVP 120% 125% 130%

+1.05VS
Ipeak = max(Ibudget*0.7=13.42, 8.5+6.842=15.34)
Ipeak=15.34A ; 1.2Ipeak=18.408A ; Imax=10.732A
1/2Delta I=1.7102A (F=290K Hz)
PR112=(1.2Ipeak-1/2Delta I) *Rds(on) (max) *1.2*8/9uA=85.5Kohm
choose PR112=86.6Kohm (for safety >1.2Ipeak)
Rds(on)=4.8m ohm(max) ; Rds(on)=3.8m ohm(typical)
Ilimit_min=(86.6K*9uA) / (8*4.8m*1.2)=16.9A
Ilimit_max=(86.6K*9uA) / (8*3.8m*1.2)=21.4A
Iocp=Ilimit+1/2Delta I=18.6A~23.1A
Iocp(min)>1.2Ipeak

2011/9/19

UMA Ipeak value equal to discrete

Dr-Bi

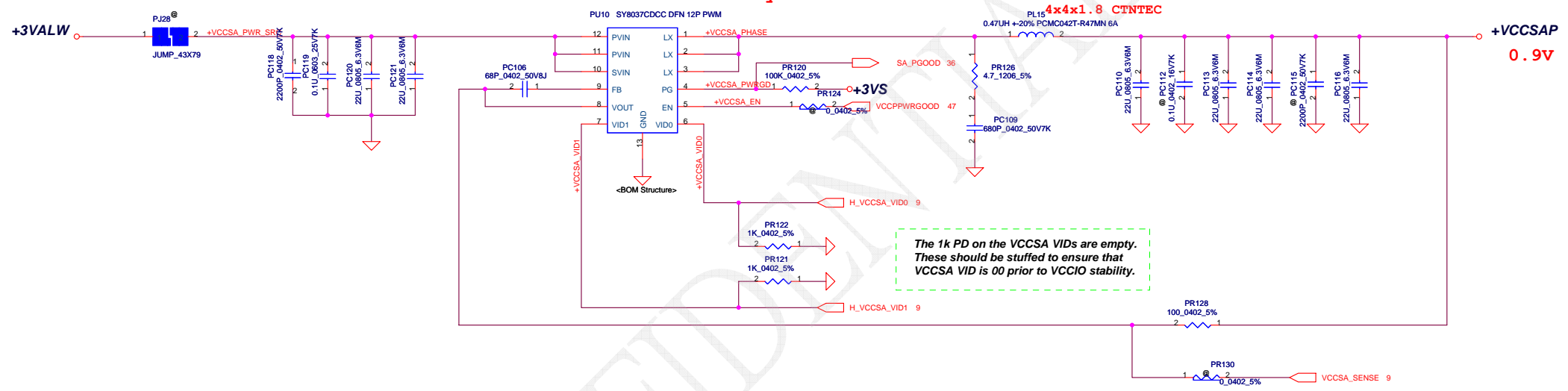
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VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

output voltage adjustable network

+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A

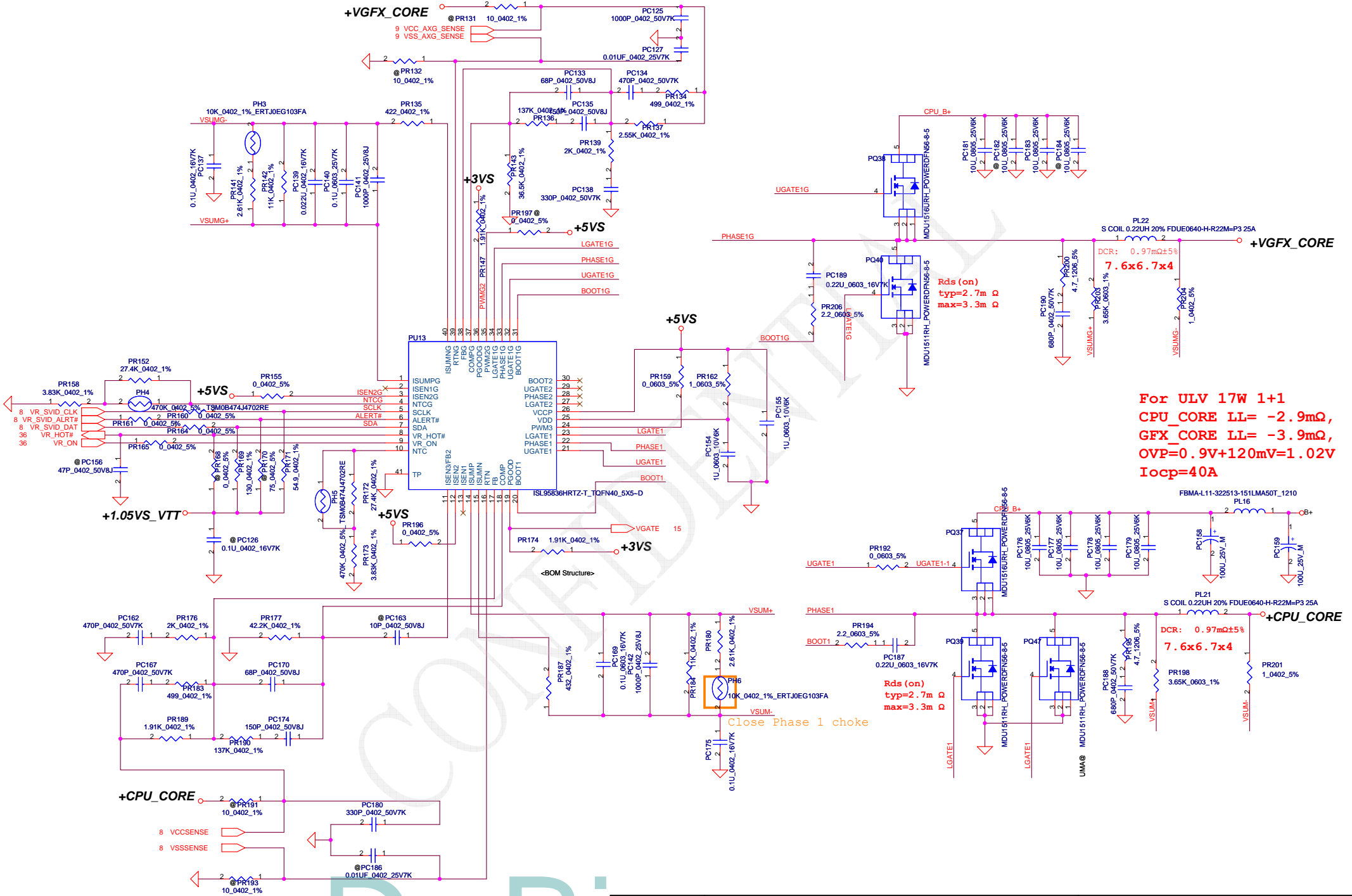
PU10 Has not Link 8037C yet



The 1k PD on the VCCSA VIDs are empty.
These should be stuffed to ensure that
VCCSA VID is 00 prior to VCCIO stability.

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For ULV 17W 1+1
 CPU_CORE LL= -2.9mΩ,
 GFX_CORE LL= -3.9mΩ,
 OVP=0.9V+120mV=1.02V
 Iocp=40A

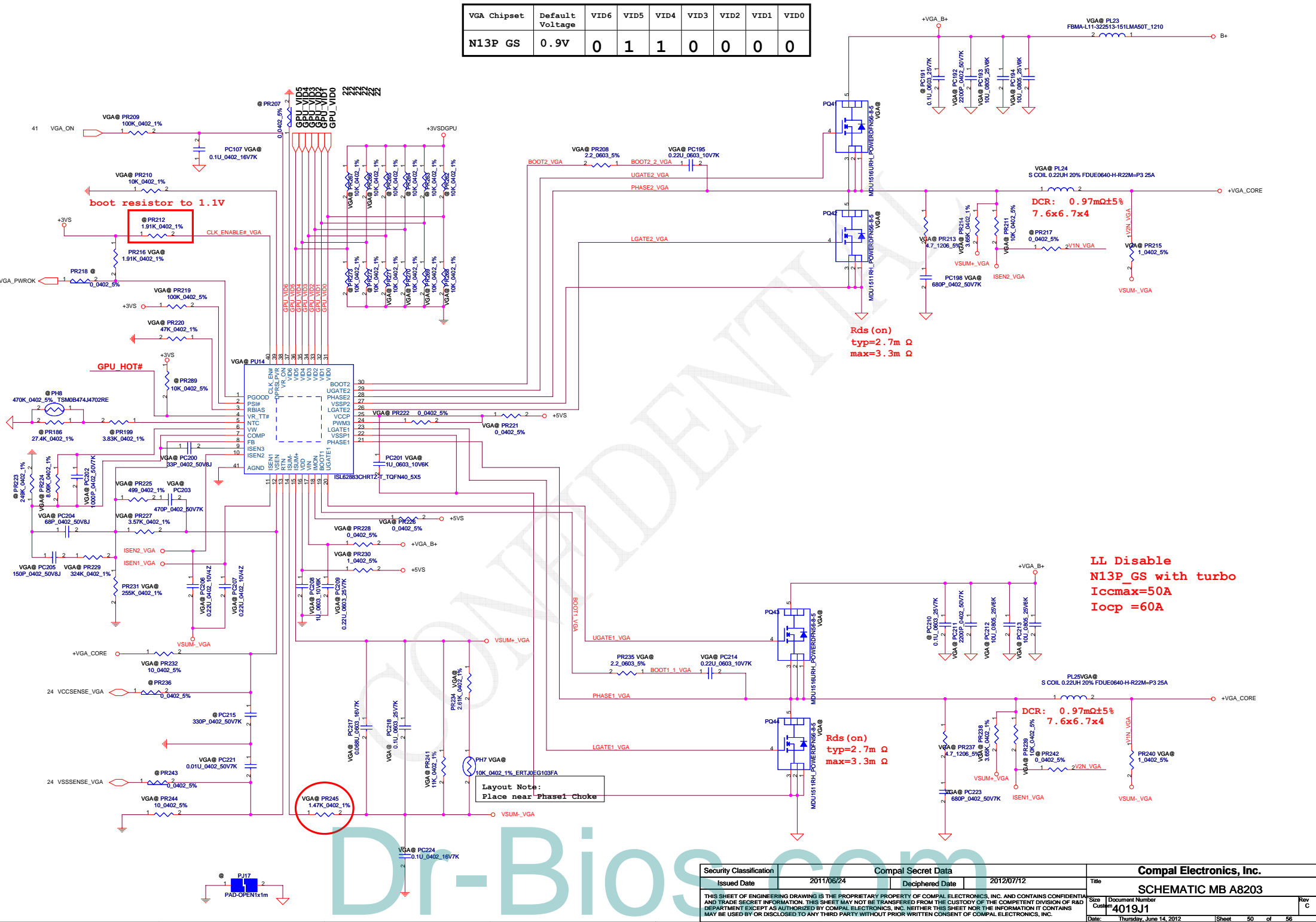
Rds (on)
 typ=2.7mΩ
 max=3.3mΩ

Rds (on)
 typ=2.7mΩ
 max=3.3mΩ

Close Phase 1 choke

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VGA Chipset	Default Voltage	VID6	VID5	VID4	VID3	VID2	VID1	VID0
N13P GS	0.9V	0	1	1	0	0	0	0



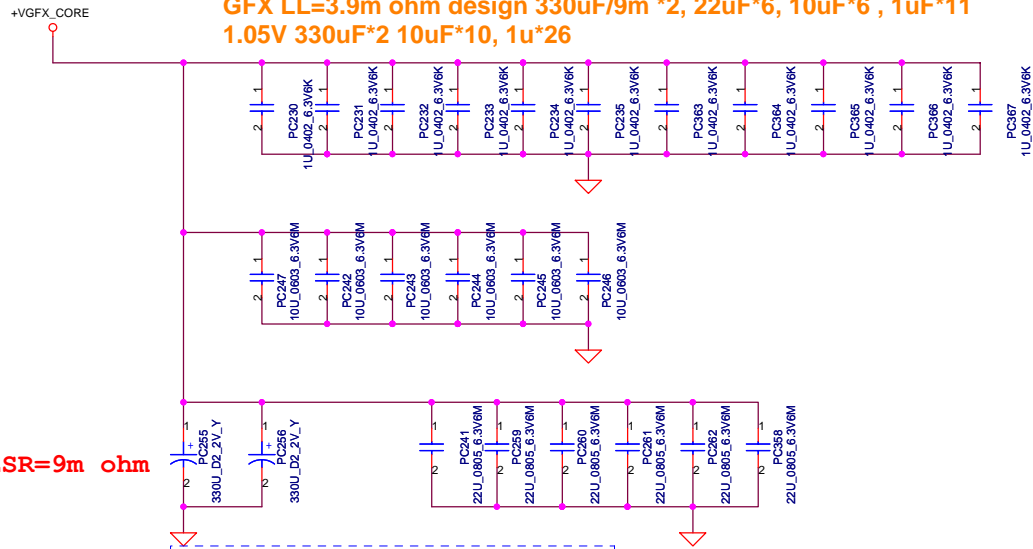
Rds (on)
typ=2.7m Ω
max=3.3m Ω

LL Disable
N13P_GS with turbo
Iccmax=50A
Iocp =60A

Layout Note:
Place near Phase1 Choke

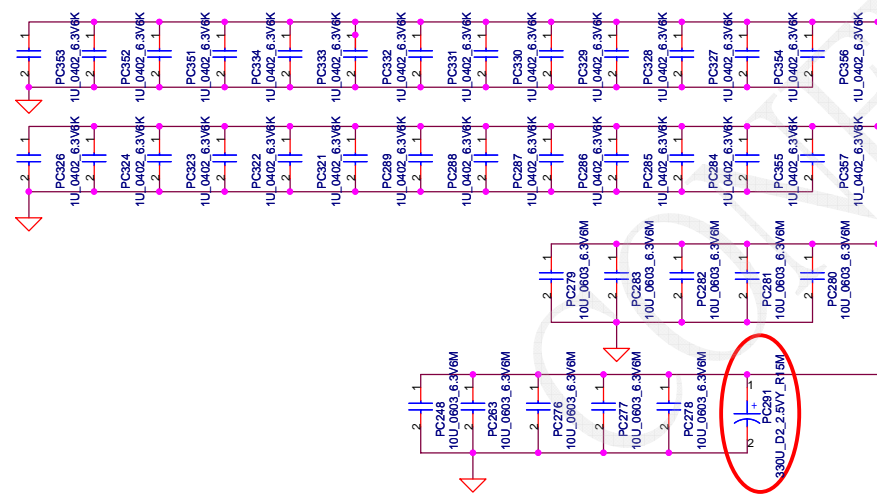
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PWR Rule
CPU LL=2.9m ohm dedign 330uF/9m *4, 22uF *12, 2.2uF*16
GFX LL=3.9m ohm design 330uF/9m *2, 22uF*6, 10uF*6 , 1uF*11
1.05V 330uF*2 10uF*10, 1u*26

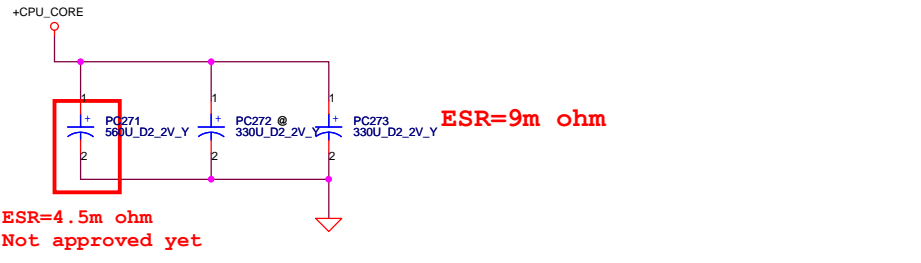
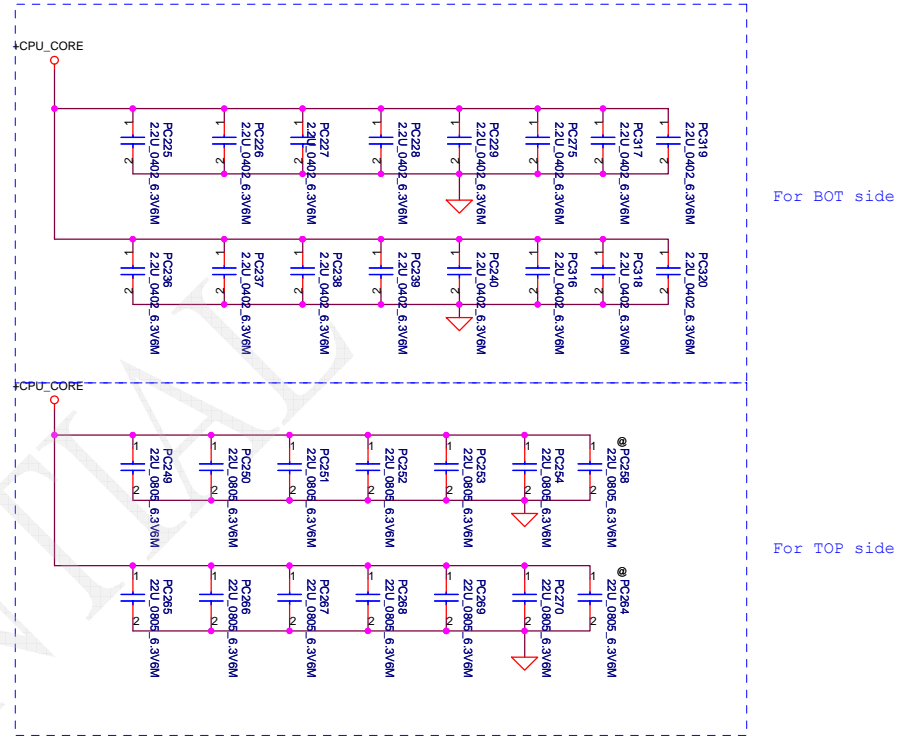


Vaxg

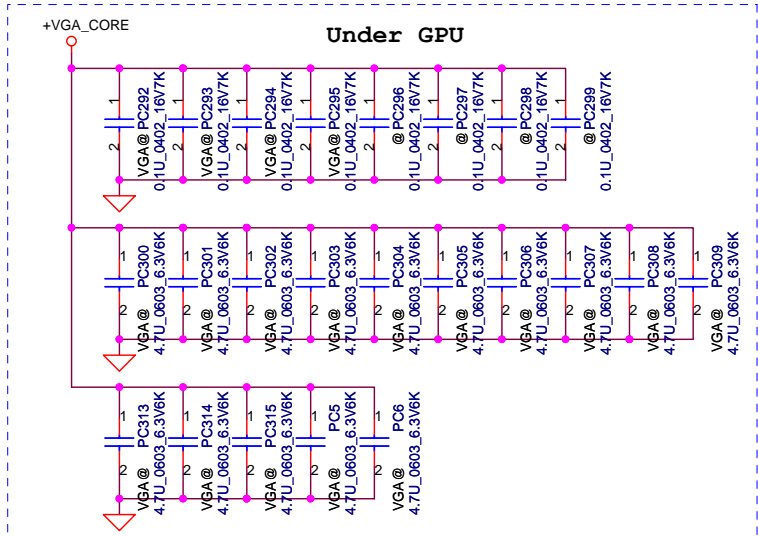
- Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed in a common motherboard design,
- VAXG can be left floating in a common motherboard design (Gfx VR keeps VAXG from floating) if the VR is stuffed



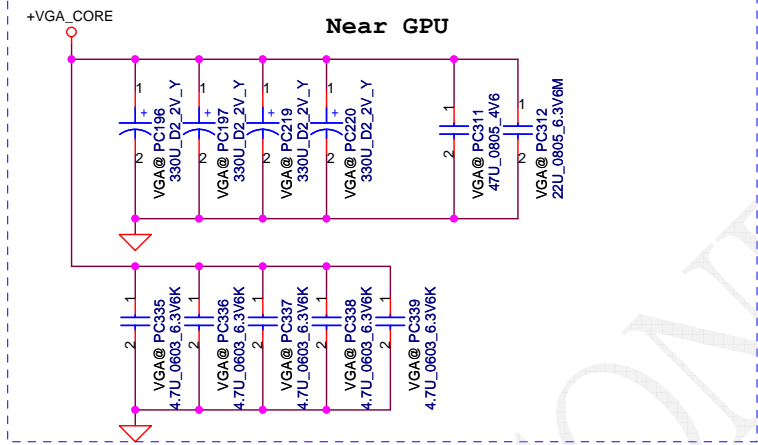
INTEL Recommend
3*330uF(1 in other page),12*22uF, 5 no stuff
from PDDG 1.0



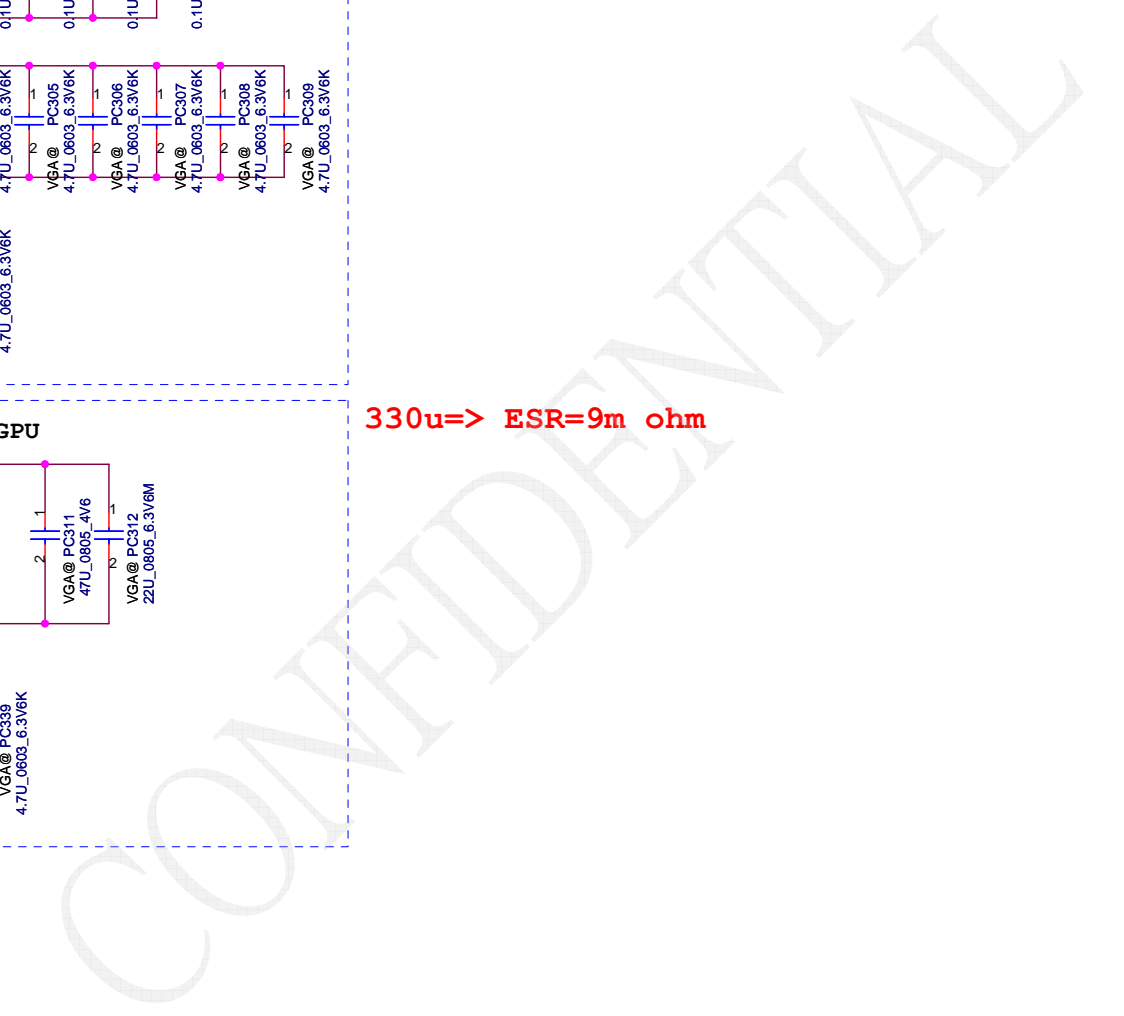
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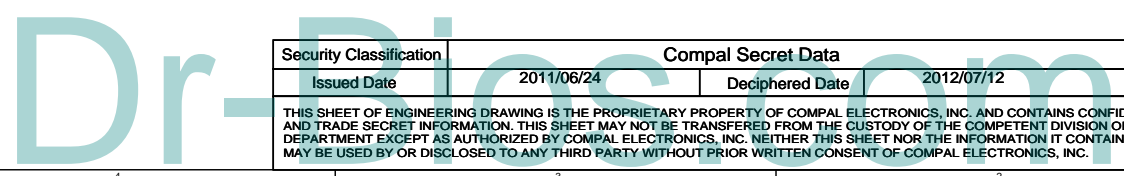
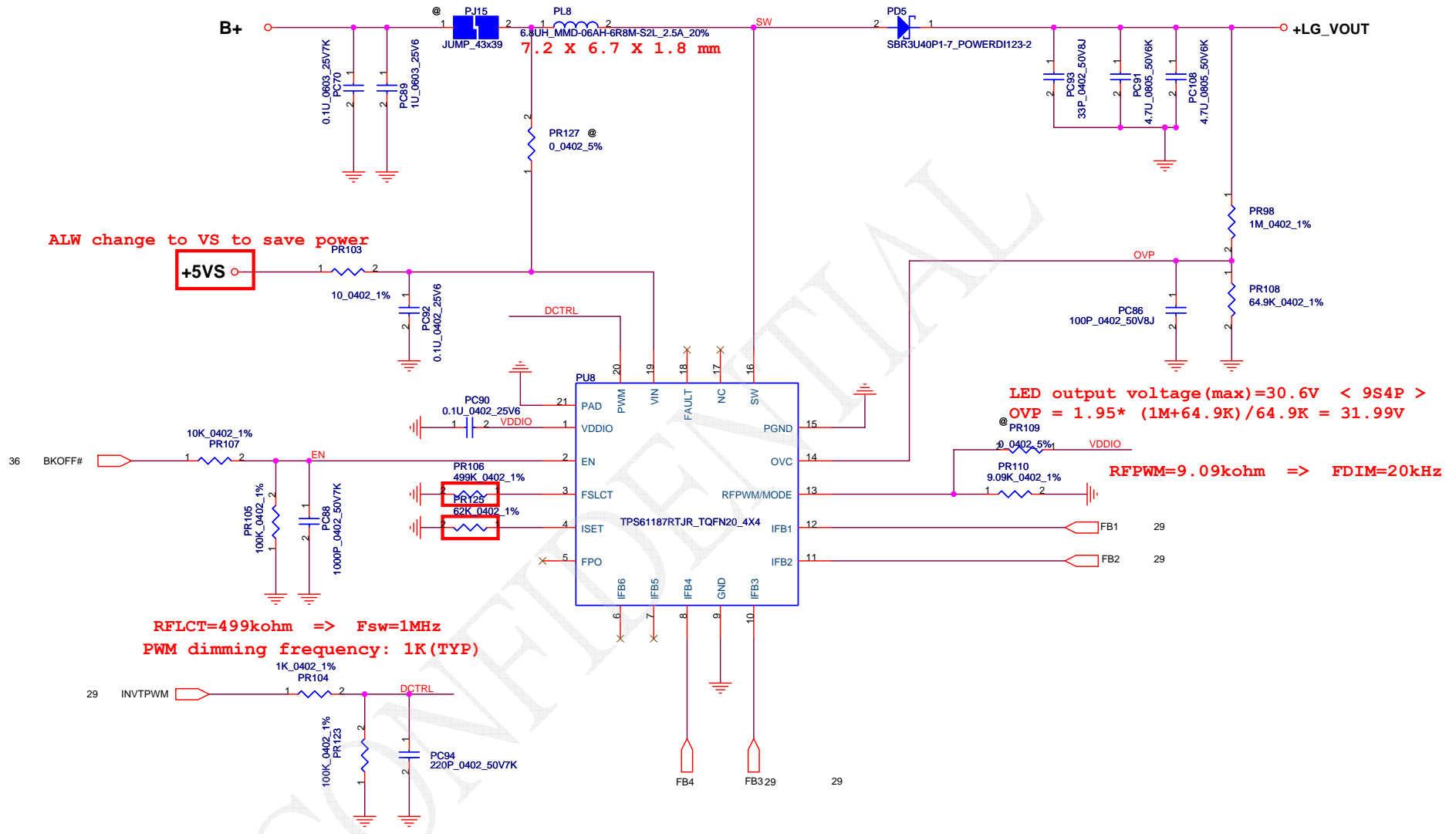
NV DG NVVDD
N13P-GS GB4-128
4.7Ux15,0.1Ux8(4@) Under GPU
330Ux4 , 47Ux1,22Ux1,4.7Ux5 Near GPU



330u=> ESR=9m ohm

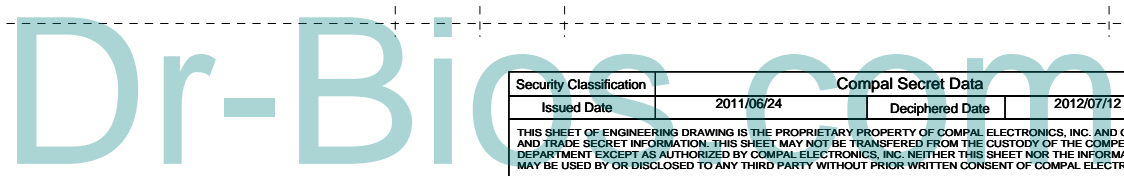


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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	VGA boot voltage	Vboot Voltage can not allow to boot to 1.1V		VGA	take off the PR212	11/22	EVT2
2	HW sequence	tune the correct sequence		VGA	PR209 set to 100k ohm ,PC107 set to 0.1u	11/22	EVT2
3	HW sequence	tune the correct sequence		1.05	put on the PQ27	11/20	EVT2
4	HW sequence	tune the correct sequence		1.8	put on the PQ28	11/20	EVT2
5	HW sequence	tune the correct sequence		0.75	put on the PR91 680k, Pc325 0.1u, PQ26, PJ16	11/20	EVT2
6	CPU overshoot	in order to follow the intel spec to reduce the overshoot		CPU	change the original 330u X3 to 330u + 560u	11/25	EVT2
7	HW sequence	tune the correct sequence		1.5V	add PJ16 and PQ26	11/22	EVT2
8	Panel demand	change the cap 35V to 50V		LED driver	change pc91 and pc108 to 50V cap	11/28	EVT2
9	ME demand	can see the cap throuth the thermal hole		CPU	take out the pc158 replace by pc159	3/13	PVT
10	acoustic demand	can't pass acoustic acer spec		CPU	add PC158 PC159	3/22	PVT2
11	component Vgs not satisfy	afraid Vgs is too small		charger	change PQ8 material	3/22	PVT2
12	0ohm resister cost down	PPM request cost down			R SHORT PR49, PR80, PR92, PR124, PR101, PR130, PR207, PR218, PR236, PR243	3/22	PVT2
13							
14							
15							
16							
17							



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Change R558 to @(0_0402),C618(0.1U_0402) for AD_PID0
 ADD R455 PH 4.7K_0402(SD028470180)(DISASSOCIATE#) <- ?K
 ADD R454(@) (0_0402) for cost down BT power control
 ADD R456 (0_0402)(SD028000080) for IOAC Pin46
 POP Q46,R590 for Boardcom WLAN discharge

1/31
 ADD R160 (0_0402) for USB_OC1# USB_OC0# colay

2/1
 R549.1,R548.1 change from +3VLP to +3VALW_EC
 remove stand along BT
 remove USB20_N13 USB20_P13

for ESD:
 ADD C416 0.1U_0402 ON/OFFBTN#
 ADD C420 0.1U_0402 ON/OFF
 ADD C421 0.1U_0402 BI_RESET
 POP C345 0.01U_0402 PLT_RST#

Y2,X1 main source change from SJ10000DM00 to SJ100004Z00

2/2
 ADD C151(@) 330U_D2
 change U13 from SA00005AGE0 to SA00005AG00 (QS PCH)

2/6
 ADD C91 @ 4.7U_0603 for WLAN Power CAP(SE107475K80)

2/7
 for N13P-GS QS,MP strap
 change R186 from 35K to 5K (Strap1 PD)

2/10
 ADD Q43 (S TR AO3419L 1P SOT23-3) and JBL2 (S H-CONN ACES 50578-0040N-001 4P P1) for back light

2/13
 for NV strap P.24
 Change R184 from ES2GPU@ to @ (strap 2)
 Delete R473 ES2GPU@ 10K_0402_1% (strap4)
 Delete R469 HYN2G@ 34.8K_0402_1% (ROM_SCLK)
 Add Hynix VRAM SA00004GD50 strap table (ROM_SI PD25K)

for Option Component
 Delete PCB 8202@
 Delete GPU U14 ES2GPU@ (SA000051800),QS2GPU@ (SA000051800)
 Delete VRAM GDDR3@
 Delete PCH U13 QSPCH@ (SA00005AG00),ES2PCH@ (SA00004NQB0)
 Change VRAM X76 GDDR5@ to VRAM@ and add X76364BOL04

for PCH
 Change U13 from SA00005AGE0 to SA00005AG00

for WLAN
 Change R328,R455 from 4.7K_0402_5% to 10K_0402_5%
 Change R73,R7,R102,R257,R279 from 0_0402_5% to 0 R_SHORT

2/14
 for KB back light
 Change location JBL2 to JBL1
 Add Q26 (2N7002K_SOT23-3) and R318 510K_0402_5%

for GDDR5 GPIO define
 Change R43 GDDR3@ to R43 @
 Change R68 GDDR5@ to R68 DIS@

For GPU strap
 Change R183 QSGPU@ to DIS@ (strap2)
 Change R473 QSGPU@ to DIS@ (strap4)
 Change R469 4.99K_0402_1% HYN2G@ to HYNMFR@ (ROM_SI)
 Add R469 24.9K_0402_1% HYNMFR@ for VRAM Hynix AFR strap

2/15
 for WLAN LED
 Change EC pin102 net name from VCIN1_PROCHOT_R to IRST_RST# P.38
 Add net IRST_RST_R# on U25 pin1 and link R162 0_0402_5% to IRST_RST# P.17
 Add R161 0_0402_5% on PLT_RST# P.17
 Add net name PLT_RST_R# between R161 and R10 P.17

for LAN
 Change net name from PLT_RST# to PLT_RST_BUF# P.34
 Add net name PLT_RST_BUF_R# between R149.2 and U62.2

for KB back light
 Add net name GPXIOA07_R between Q43.2 and Q26.1
 Change R559 18K_0402_5% to 33K_0402_5%

2/15A
 L27 change main source from SHI00007400 to SH00000JM00
 ADD R163(0_0402_5%) for PLT_RST_LAN#

2/16
 R422,R619,R65 change to 0ohm-Rshort
 C452 change from 15P to 18P
 Chang JBL1 footprint from 抽屜式 SP01000ZW00 to 掀蓋式 SP01000Z300
 SW1 change to unpop

02/17
 Q45,Q46 2N7002 change to Q54 dual 2N7002
 3VSWLAN_R change name to +3VS_WLAN_R trace 20mil

2/18
 R34 unpop(SUSWARN# PH 10K)
 R26 unpop(PCH_ACIN PH 10K)

2/21
 R466 change from 5K to 10K(for device manager 3D device)

Rev1.0
 3/14
 ADD D21 ESD diode near ODD prevent PCH crack
 Q1 Q4 2N7002 combine to Dual 2N7002 Q55
 R559 change 33K to 56K_0402_5% SD028560280(for Board ID 4)
 R318 change 510K to 100K (BL KB)

3/15
 R415 R150,R278,R280,R291,R295,R298 ,R584,R86,R160 change 0_0402_5# ot Rshort_0402
 R450,R497 0_0603_5% to Rshort_0603
 ADD C552,C556,C558,C580,C581 for ESD
 (BATT_AMB_LED#,BATT_BLUE_LED#,PWR_SUSP_LED#,PWR_LED#,+3VALW) Place near JLED1
 Q3,Q16,Q17,Q19,Q44 change from SB501380020 to SB501380050 (HF)

3/22
 change PCH to MP version to SA00005AGI0

4/5
 CR CPU P/N change to MP PN
 SA00005L5C0,SA00005K6B0,SA00005K5B0
 remove Q50 for PROCHOT# connection issue
 4/10
 follow ESD suggest remove D28,D13 for cost down

Rev1A 4/10 Fix Q50 PROCHOT# connection issue

5/8
 Change SA00005MX10 (S IC AV8062701048004 QAXQ J1 1.5G BGA) to SA00005MX60 (S IC AV8062701048004 SR0CW J1 1.5G ABO)
 Rev1A 5/9 Change R559 from 56K to 100K(Board ID update)

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PCB

ZZZ

LA-8203P MB Rev0: DA80000T600
LA-8203P MB Rev1: DA80000T610
LA-8203P MB with Small Board Rev1: DAZ00200100

LA-8203P REV1 M/B
DAZ00200100

CPU

UCPU1

132367@

S IC AV8062701047904 SR0CV J1 1.4G ABO!
SA000051H60

AV8062701047904 SR0CV J1 1.4G ABO!

UCPU1

132377@

S IC AV8062701048004 SR0CW J1 1.5G ABO!
SA00005MX60

AV8062701048004 SR0CW J1 1.5G ABO!

UCPU1

152467@

S IC AV8062701047504 SR0D6 J1 1.6G ABO!
SA00004X010

AV8062701047504 SR0D6 J1 1.6G ABO!

SANDY BRIDGE

UCPU1

133217@

S IC AV8063801058401 SR0N9 L1 1.8G BGA 1023 ABO !
SA00005L5C0

AV8063801058401 SR0N9 L1 1.8G BGA 1023 ABO !

UCPU1

153317@

S IC AV8063801058002 SR0N8 L1 1.7G ABO!
SA00005K6B0

AV8063801058002 SR0N8 L1 1.7G ABO!

UCPU1

173517@

S IC AV8063801057605 SR0N6 L1 1.9G BGA 1023 ABO !
SA00005K5B0

AV8063801057605 SR0N6 L1 1.9G BGA 1023 ABO !

IVY BRIDGE

UCPU1

QBP8@

S IC AV8063801057401 QBP8 K0 1.5G BGA
SA00005AZ00

AV8063801057401 QBP8 K0 1.5G BGA

UCPU1

QBP7@

S IC AV8063801057400 QBP7 K0 1.7G BGA
SA00005B000

AV8063801057400 QBP7 K0 1.7G BGA

EVT2

VRAM

ZZZ

VRAM@

ALT. GROUP PARTS VRAM X4 HYN 1G Q5LJ1
ALT. GROUP PARTS VRAMX4 HYN1G 38NM Q5LJ1
X76364BOL03|X76364BOL04

ALT. GROUP PARTS VRAM X4 HYN 1G Q5LJ1

DRAM

ZZZ

DRAM@

ALT. GROUP PARTS DRAM X4 ELP 2G Q5LJ1
ALT. GROUP PARTS DRAM X4 HYN 2G Q5LJ1
X76364BOL11|X76364BOL12

ALT. GROUP PARTS DRAM X4 HYN 2G Q5LJ1

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