

Domino_BA Schematics Document

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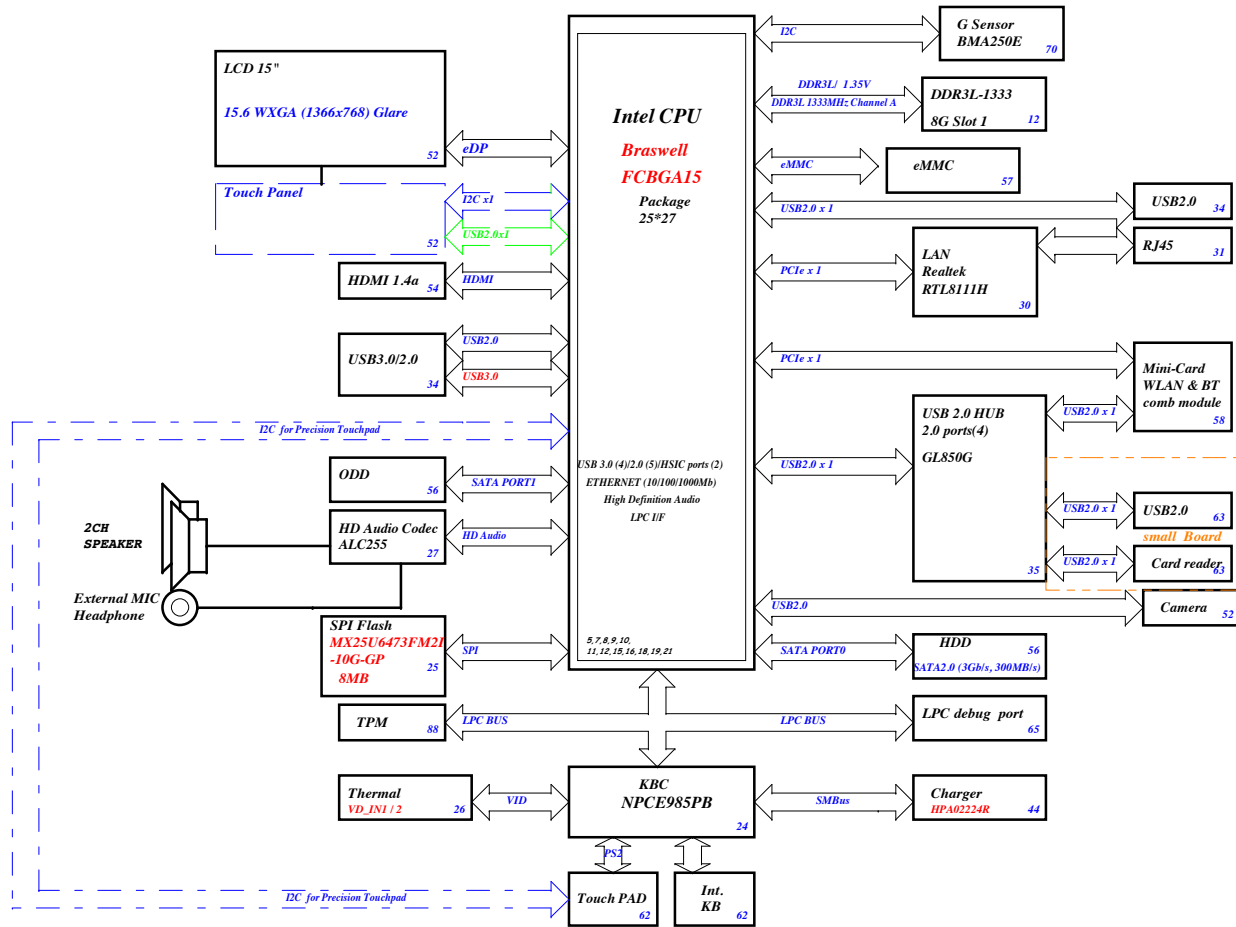
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Title Cover Page		
Size A3	Document Number Domino	Rev -1
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Domino_BA Board Block Diagram

Project code : 4PD053010001
 PCB P/N : 14285
 Revision : -1



CHARGER	
INPUTS	44
OUTPUTS	
DCBATOUT	BT+
SYSTEM DC/DC	
RT6575D 45	
INPUTS	
OUTPUTS	
DCBATOUT	5V_S5
	3D3V_S5
CPU DC/DC	
NCP81201MNTXG 46-47	
INPUTS	
OUTPUTS	
DCBATOUT	1V_CPU_CORE
CPU DC/DC	
NCP81201MNTXG 48	
INPUTS	
OUTPUTS	
DCBATOUT	6FX_CORE
SYSTEM DC/DC	
TPS51716 50	
INPUTS	
OUTPUTS	
DCBATOUT	1D05V_S5
SYSTEM DC/DC	
TPS51716 49	
INPUTS	
OUTPUTS	
DCBATOUT	1D35V_CPU_VDDQ_S5
SYSTEM LDO	
S-1339D15 51	
INPUTS	
OUTPUTS	
3D3V_S5	1D5V_S0
SYSTEM LDO	
RT9043GB 51	
INPUTS	
OUTPUTS	
1D8V_S5	1D24V_S5
SYSTEM DC/DC	
RT8068AZQWID 51	
INPUTS	
OUTPUTS	
3D3V_S5	1D8V_S5

PCB LAYER	
L1:Top	L4:Signal
L2:VCC	L5:GND
L3:Signal	L6:Bottom

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File: Block Diagram Rev: -1
 Date: Friday, 14/01/2012 Sheet: 2 of 102

SSID = CPU

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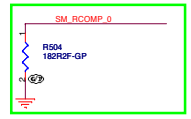
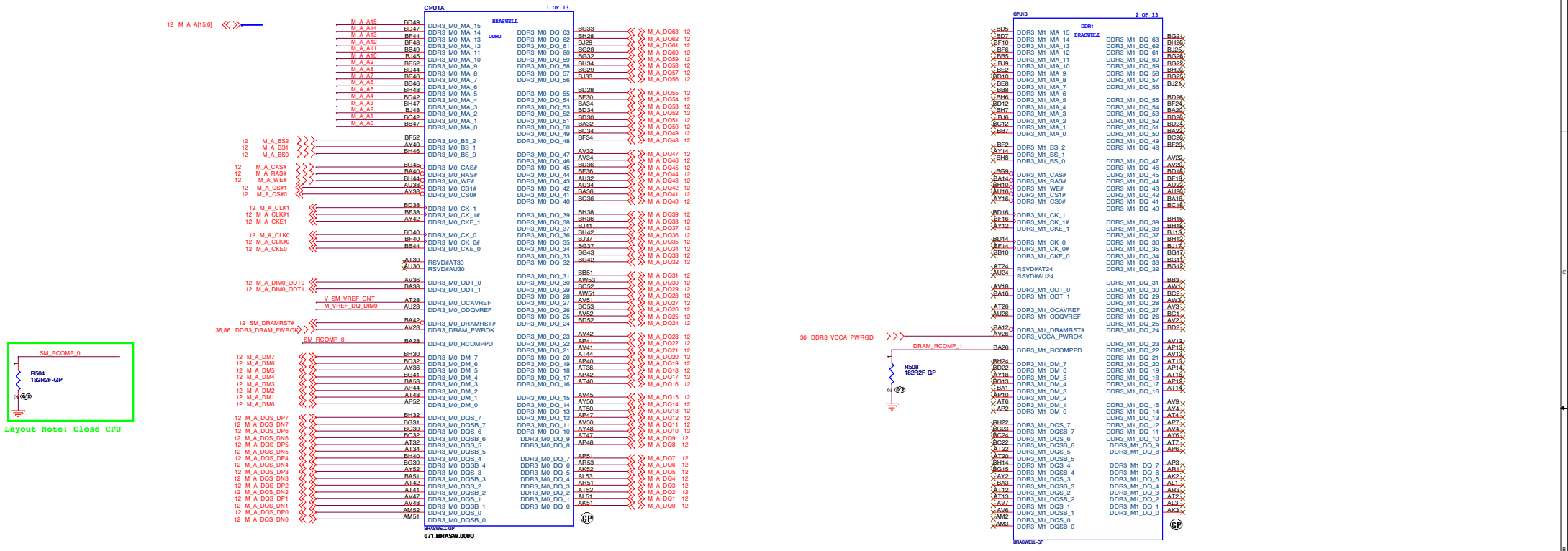
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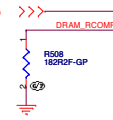
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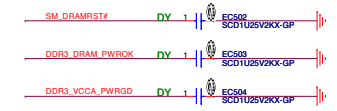
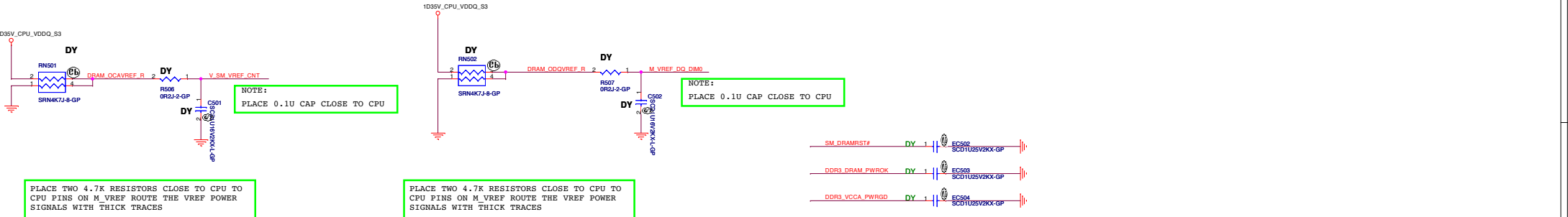
Layout Note: Close CPU



NOTE: PLACE 0.1u CAP CLOSE TO CPU

PLACE TWO 4.7K RESISTORS CLOSE TO CPU TO CPU PINS ON M_VREF ROUTE THE VREF POWER SIGNALS WITH THICK TRACES

PLACE TWO 4.7K RESISTORS CLOSE TO CPU TO CPU PINS ON M_VREF ROUTE THE VREF POWER SIGNALS WITH THICK TRACES



SSID = CPU

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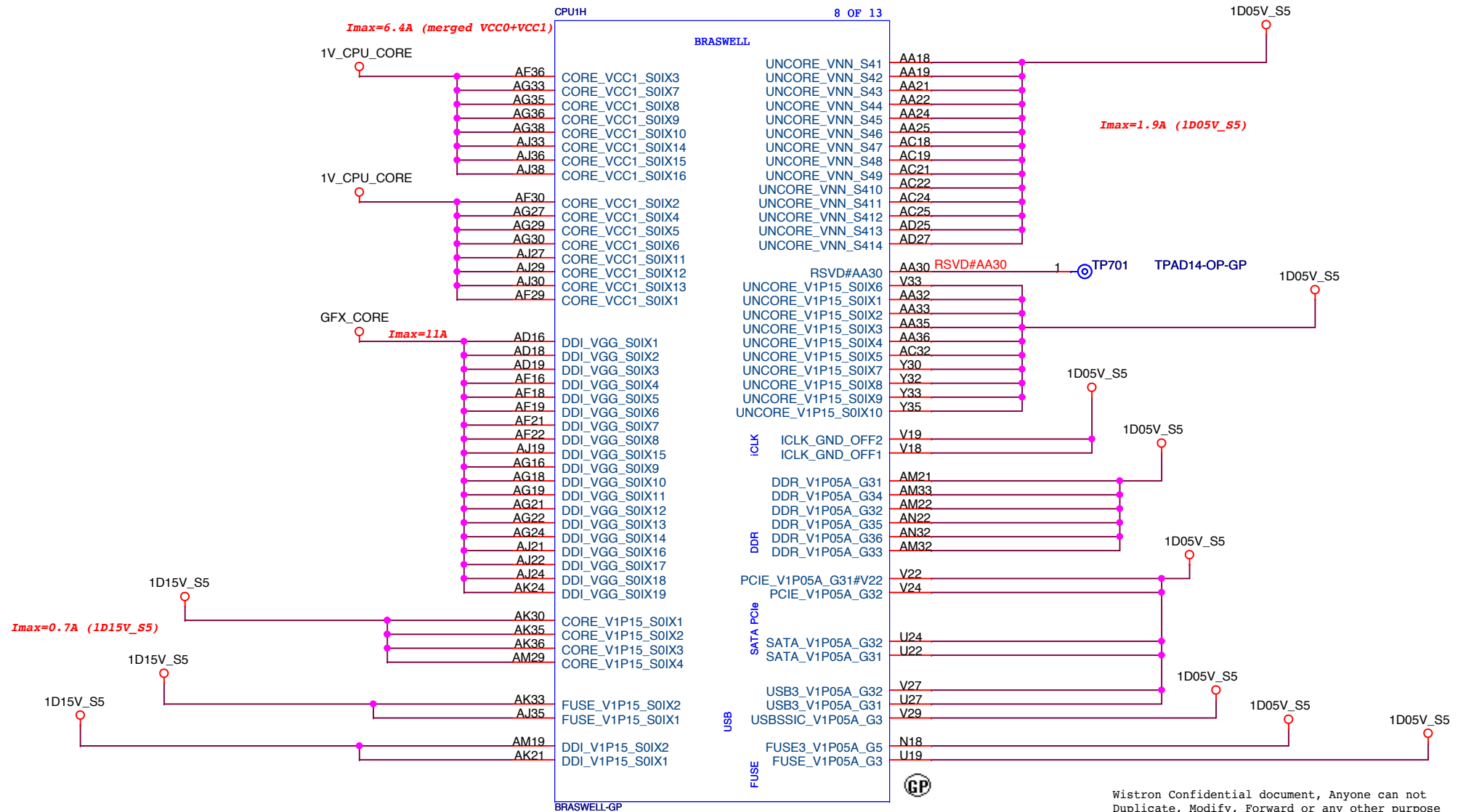
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Title		
CPU (CFG)		
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SSID = CPU

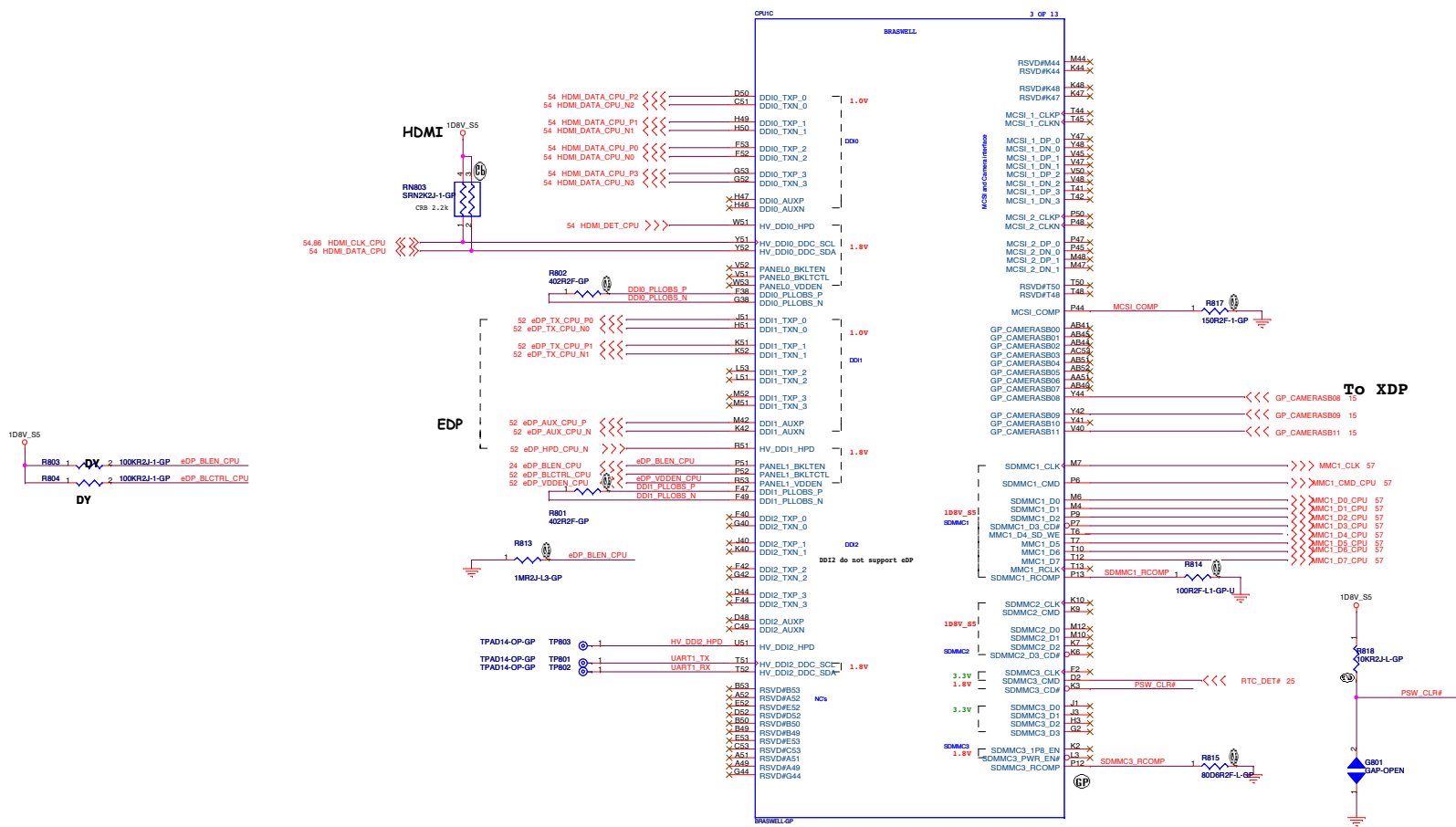


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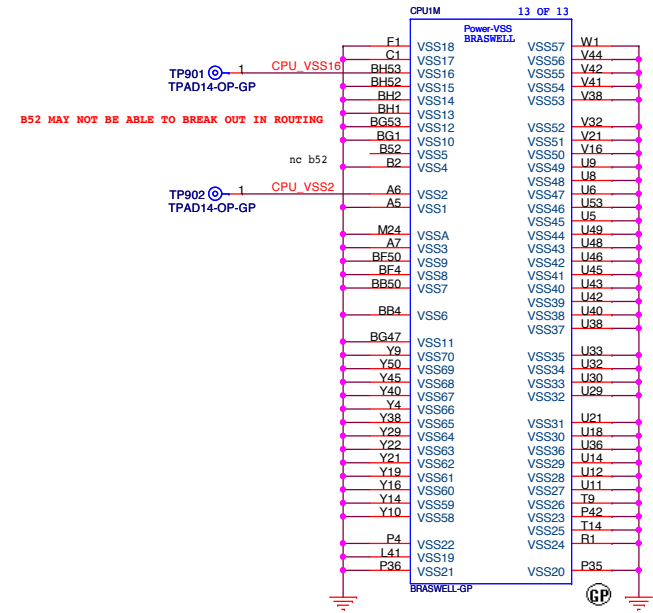
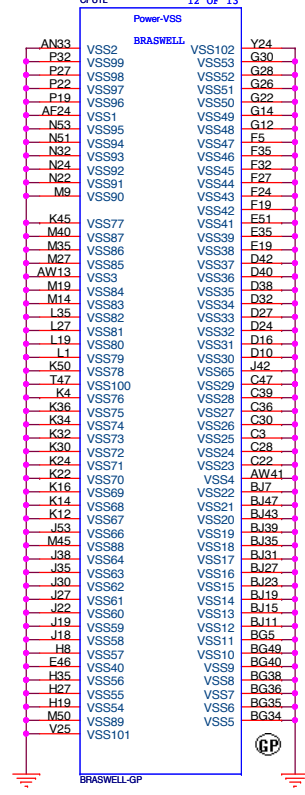
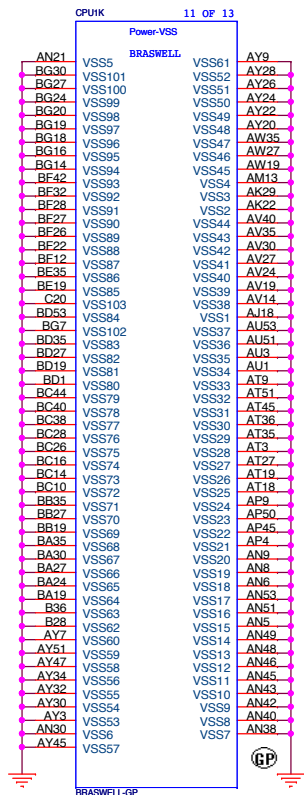
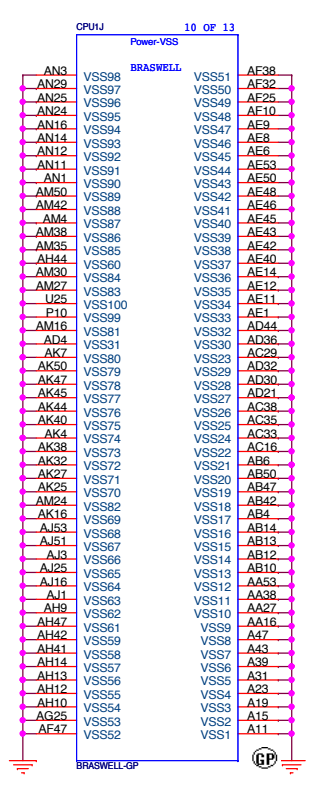
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Title		
CPU (VCC CORE)		
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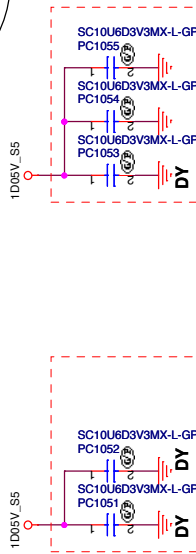
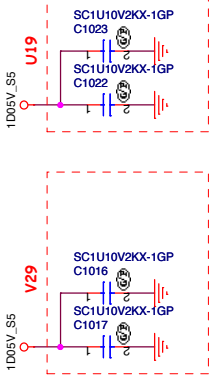
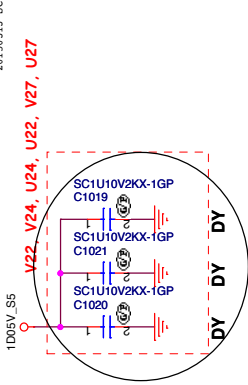
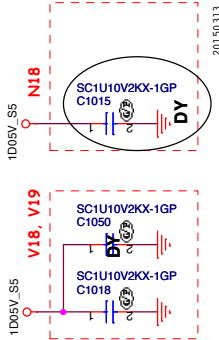
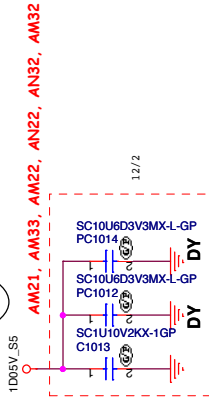
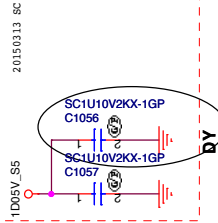
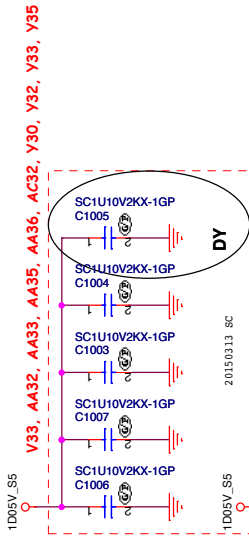
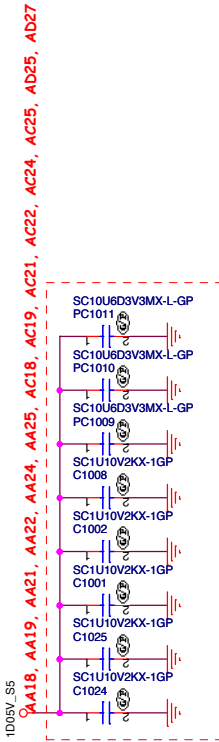
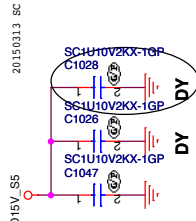
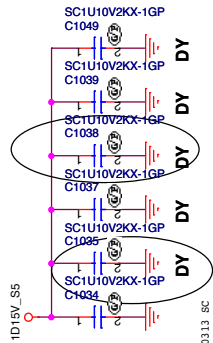
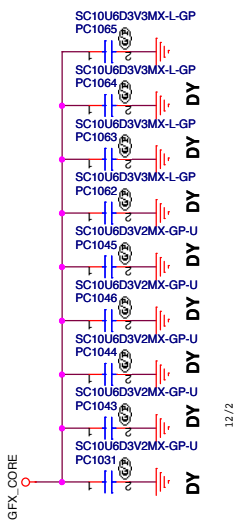
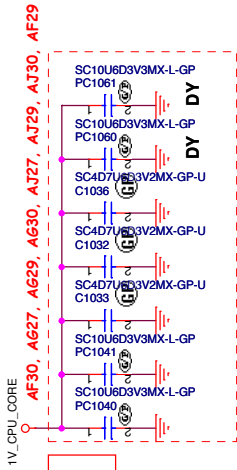
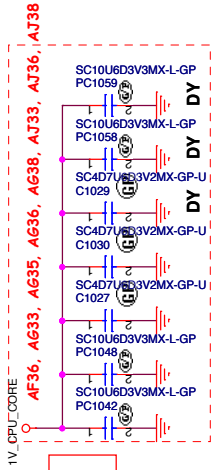
Title: **CPU (VSS)**

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PLACE ALL THE CAPS UNDER THE PKG SHADOW

PLACE ALL THE CAPS UNDER THE PKG SHADOW

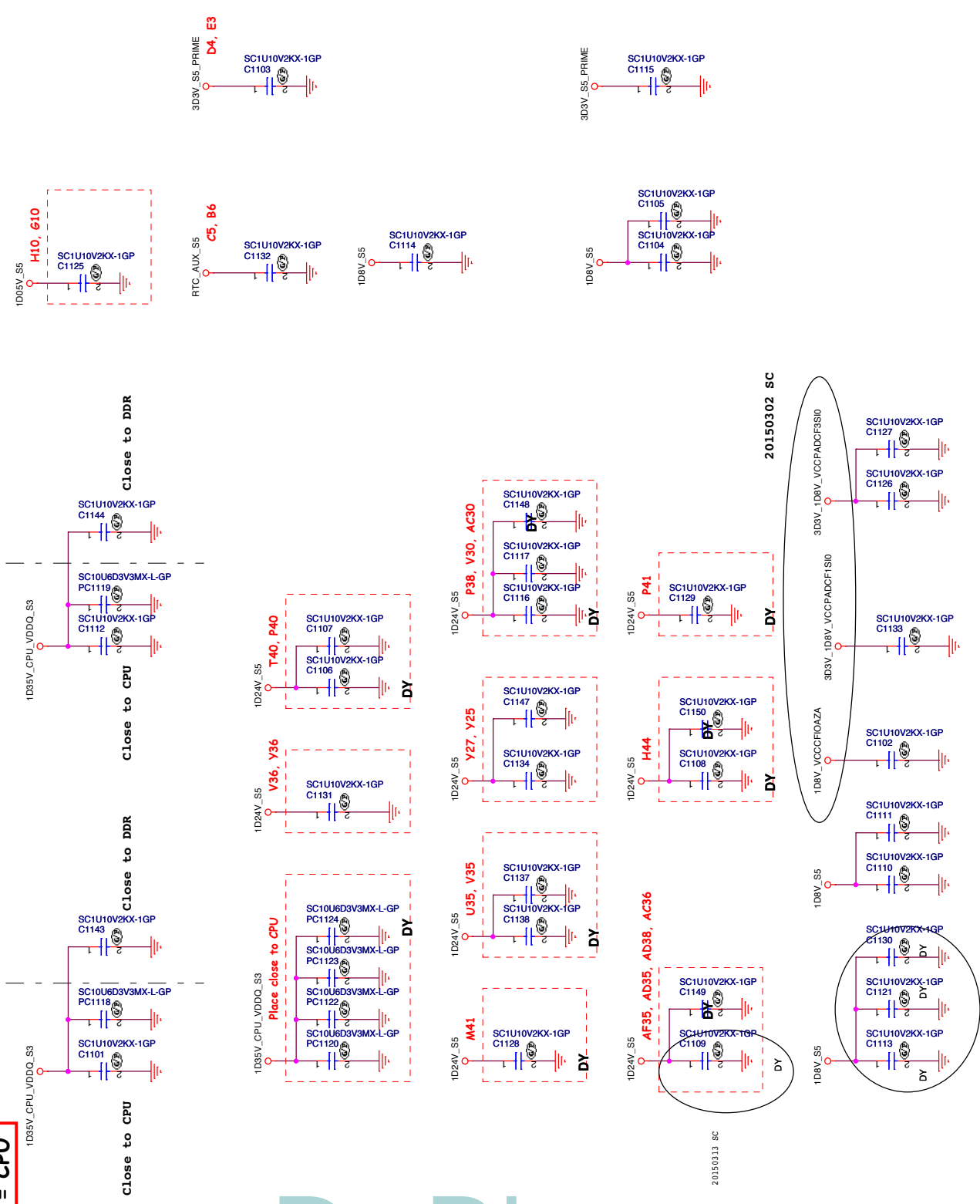


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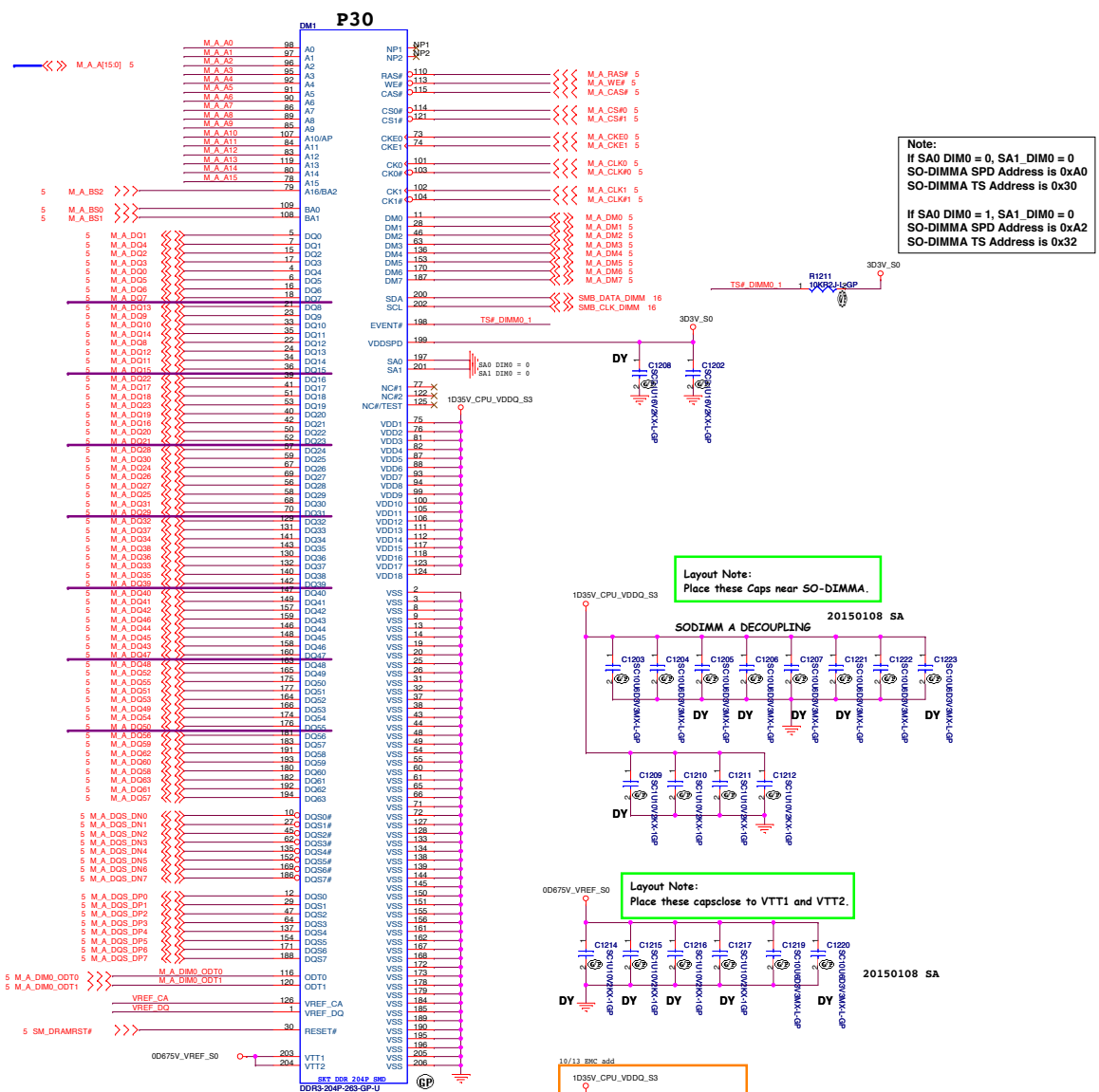
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SSID = CPU



20150313 SC

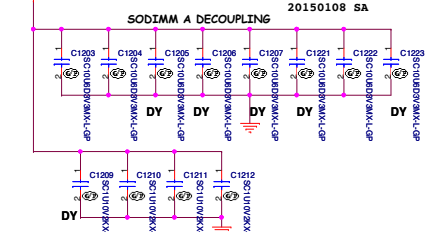
20150302 SC



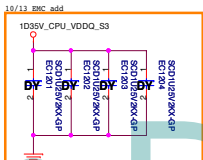
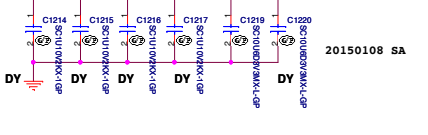
Note:
 If SA0_DIM0 = 0, SA1_DIM0 = 0
 SO-DIMMA SPD Address is 0xA0
 SO-DIMMA TS Address is 0x30

If SA0_DIM0 = 1, SA1_DIM0 = 0
 SO-DIMMA SPD Address is 0xA2
 SO-DIMMA TS Address is 0x32

Layout Note:
 Place these Caps near SO-DIMMA.

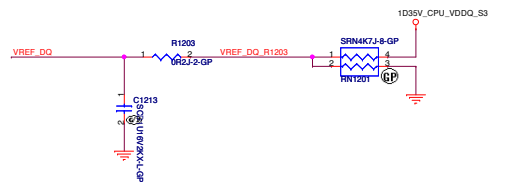


Layout Note:
 Place these caps close to VTT1 and VTT2.

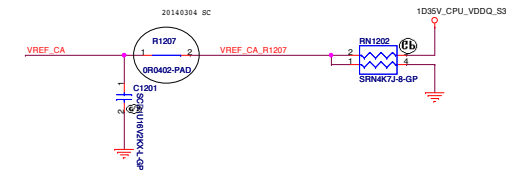


Reserve 0.1uF for ESD

For Intel Recommend Close to DIMM(Braswell)



For Intel Recommend Close to DIMM(Braswell)



2nd = 62.10024.M51
 62.10024.S61
 4th = 62.10017.L21
 3rd = 62.10024.Q71



SSID = MEMORY

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SSID = CPU

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STRAP RESISTORS SHOULD BE PLACED CLOSE TO SOC SHOULD BE PLACED OUTSIDE KOZ AREA

All the straps are controlled on the introduction of the PMC_RSMRST_N signal (controlled by the user)

Description	DDI0_Detected	DDI1_Detected	A16 Swap Override	DSI Display Detected	Boot BIOS Strap BBS	Flash Descriptor Security Override	DFX Boot Halt Strap & VISA Early POSM Debug Enable	DFX Sus Debug Strap	ICLK, USB2, DDI SFR Supply Select	ICLK SFR Bypass	POSM Select	ICLK Xtal OSC Bypass	CCU SUS RO Bypass	RTC OSC bypass
GPIO	GPIO_SUS0	GPIO_SUS1	GPIO_SUS2	GPIO_SUS3	GPIO_SUS4	GPIO_SUS5	GPIO_SUS6	GPIO_SUS7	SEC_GPIO_SUS8	SEC_GPIO_SUS9	SEC_GPIO_SUS10	GP_CAMERASB08	GP_CAMERASB09	GP_CAMERASB11
Schematic														
High	DDI0 Detect	DDI1 Detect	Normal Operation	DSI Detect	Boot from SPI	Weak internal pull-up Normal Operation	Normal	Weak internal pull-up Normal	1.35V	Weak internal pull-up Bypass with 1.05V	PMC	Bypass	Bypass	Bypass
Low	Disable	Disable	Change Boot Loader address (A16 Override)	Disable	Boot from LPC	Override	Halt boot enable	Sus Debug enable	1.25V	No bypass	Fuse controller	No bypass	No bypass	No bypass

Table 29. Straps (Sheet 1 of 2)

Signal Name	Purpose	Pull-Up/Pull-Down	Strap Description
GPIO_SUS[0]	DDI0 Detect	Weak internal pull-down	DDI0 Detect 0 = DDI0 not detected 1 = DDI0 detected
GPIO_SUS[1]	DDI1 Detect	Weak internal pull-down	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected
GPIO_SUS[2]	A16 swap override	Weak internal pull-up	Top Swap (A16 Override) 0 = Change Boot Loader address 1 = Normal Operation
GPIO_SUS[4]	Boot BIOS Strap BBS	Weak internal pull-up	BIOS Boot Selection 0 = - 1 = SPI
GPIO_SUS[5]	Flash Descriptor Security Override	Weak internal pull-up	Security Flash Descriptors 0 = Override 1 = Normal Operation

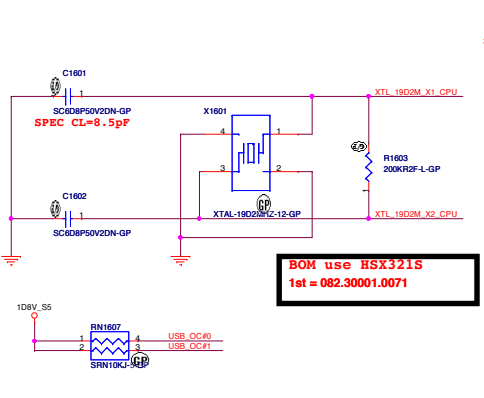
Table 29. Straps (Sheet 2 of 2)

Signal Name	Purpose	Pull-Up/Pull-Down	Strap Description
GPIO_SUS[8]	ICLK, USB2, DDI SFR Supply Select	Weak internal pull-down	0 = Supply is 1.25V 1 = Supply is 1.35V This strap also contains PLL LDO 0: supply is 1.25V; 1: supply is 1.35V. Selects supply voltage for LDOs used for PLLs, thermal oscillators, USB2, ICLK and DDI
GPIO_SUS[9]	ICLK, USB2, DDI SFR Bypass	Weak internal pull-up	0 = No bypass 1 = Bypass with 1.05V
GPIO_SUS[10]	POSM Select	Weak internal pull-down	Selects which POSM will be observed at time 0 0 = Fuse controller 1 = PMC
GPIO_CAMERASB08	ICLK Xtal OSC Bypass	Weak internal pull-down	0 = No Bypass 1 = Bypass
GPIO_CAMERASB09	CCU SUS RO Bypass	Weak internal pull-down	0 = No Bypass 1 = Bypass
GPIO_CAMERASB11	RTC OSC Bypass	Weak internal pull-down	0 = No Bypass 1 = Bypass

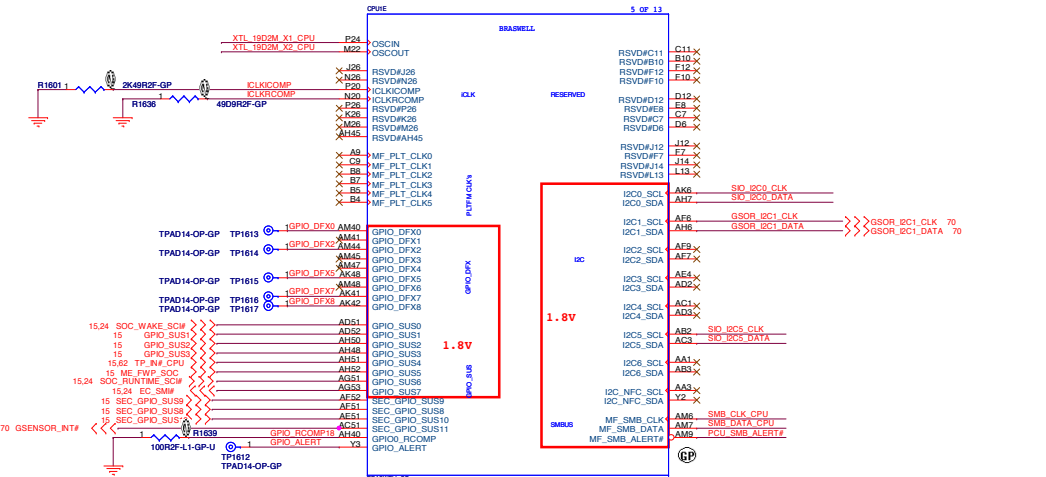
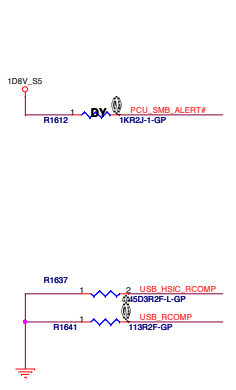
CHV Straps [CRB] -- strap detect @ RSMRST# assertion				
Purpose	CHV Pin Name (refer CHV symbol PIN)	PU/PD (internal - Weak)	Options	Default State on board?
DDI0 Detected	GPIO_SUS0	PD	1 - DDI0 Detect, 0 - Disable	High
DDI1 Detected	GPIO_SUS1	PD	1 - DDI1 Detect, 0 - Disable	High
A16 swap override	GPIO_SUS2	PU	1 - Default, 0 - A16 override	High
DSI Display Detected	GPIO_SUS3	PD	1 - DSI detect, 0 - Disable	Low
Boot BIOS Strap BBS	GPIO_SUS4	PU	1 - Boot from SPI, 0 - Boot from LPC	High
Flash Descriptor Security Override	GPIO_SUS5	PU	1 - Security enabled, 0 - Security disabled	High
DFX Boot Halt Strap & VISA Early POSM Debug Enable	GPIO_SUS6	PU	1 - normal, 0 - Halt boot enable	High
DFX Sus Debug Strap	GPIO_SUS7	PU	1 - Normal, 0 - Sus Debug enable	High
ICLK, USB2, DDI SFR Supply Select	SEC_GPIO_SUS8	PU	1 - 1.35V, 0 - 1.25V	Low
ICLK SFR Bypass	SEC_GPIO_SUS9	PD	1 - Bypass with 1.05V, 0 - No Bypass	Low
POSM Select	SEC_GPIO_SUS10	PD	1 - PMC, 0 - Fuse controller	Don't care, if GPIO_SUS6 is pulled high.
ICLK Xtal OSC Bypass	GP_CAMERASB08	PD	1 - Bypass, 0 - No bypass	Low
CCU SUS RO Bypass	GP_CAMERASB09	PD	1 - Bypass, 0 - No bypass	Low
RTC OSC Bypass	GP_CAMERASB11	PD	1 - Bypass, 0 - No bypass	Low



SSID = PCH

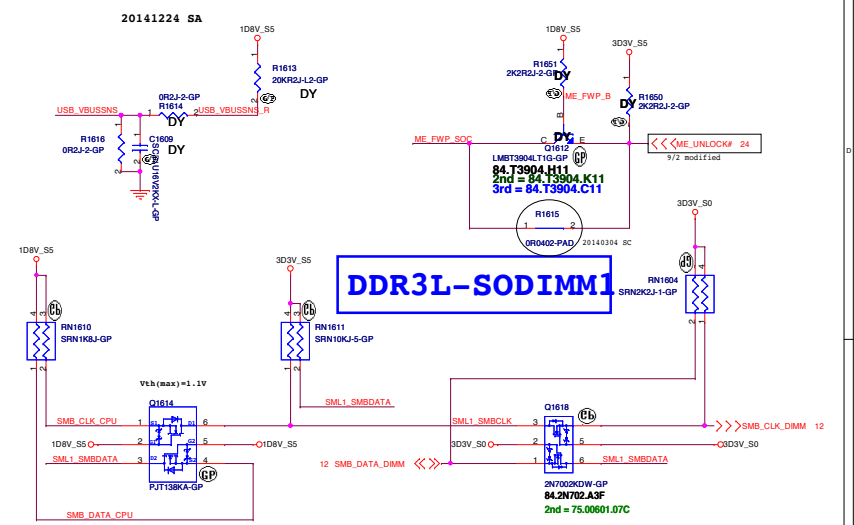


BOM use HX321S
1st = 082.30001.0071



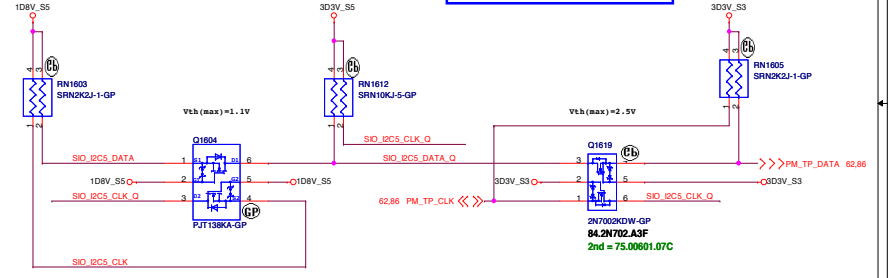
level-shift

Level shift

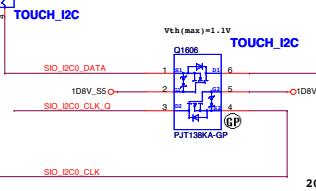
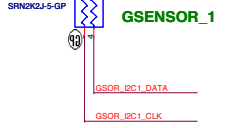
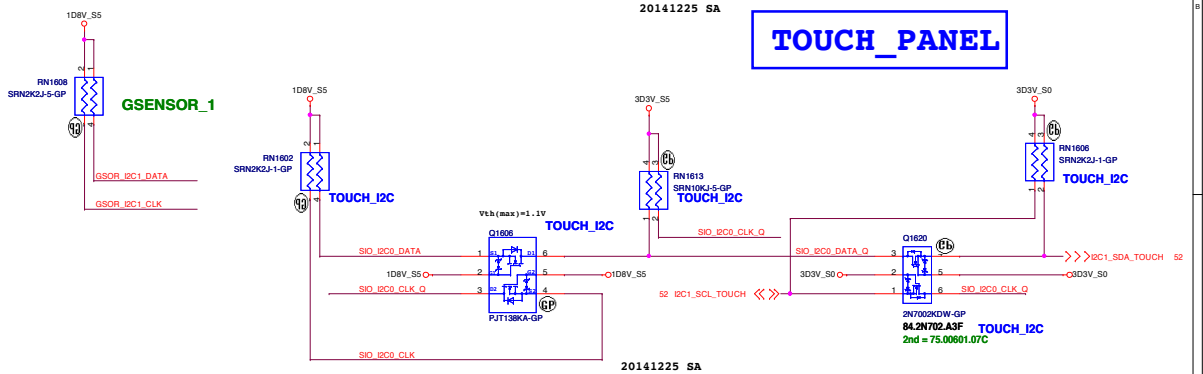


DDR3L-SODIMM

TOUCH_PAD



TOUCH_PANEL



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SSID = CPU

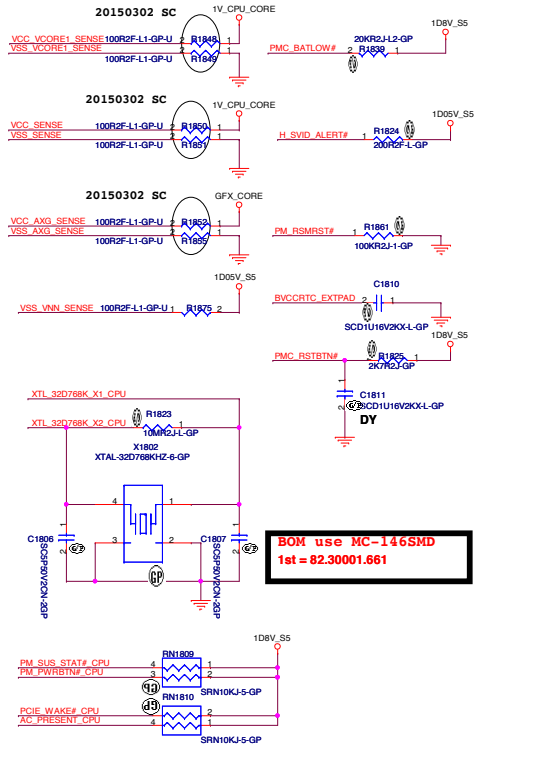
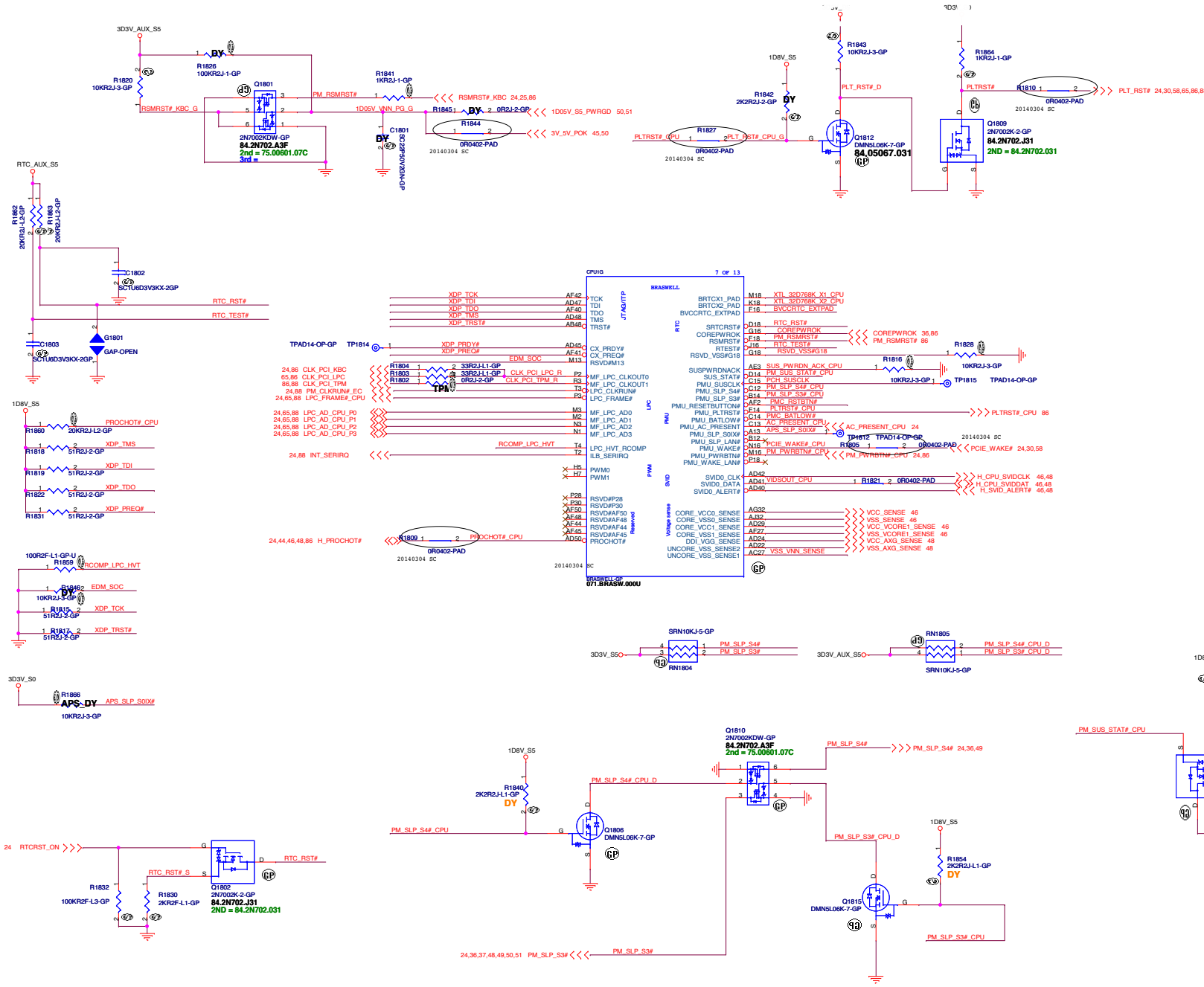
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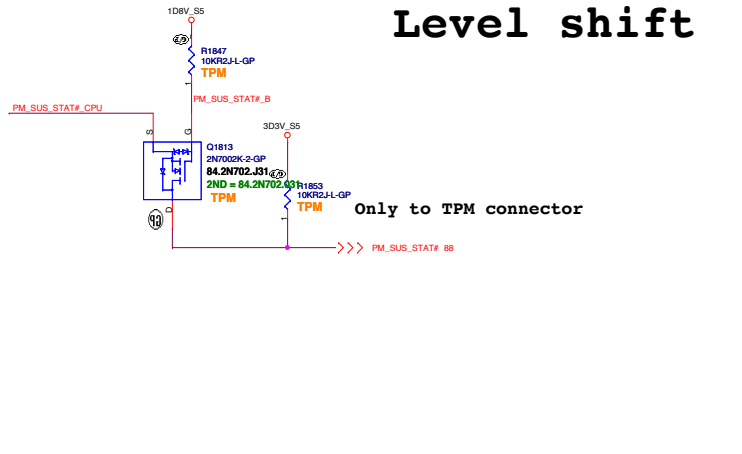
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**BOM use MC-146SMD
1st = 82.30001.661**

Level shift



Only to TPM connector

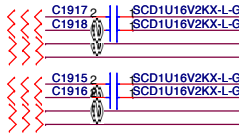


LAN

30 PCIE_TX_LAN_P0
30 PCIE_TX_LAN_N0
30 PCIE_RX_CPU_P0
30 PCIE_RX_CPU_N0

WLAN

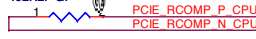
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58.86 PCIE_TX_WLAN_N1
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58.86 PCIE_RX_CPU_N1



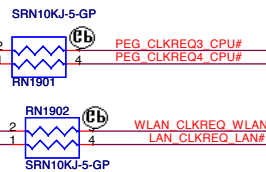
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58.86 WLAN_CLKREQ_WLAN#

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30 LAN_CLK_CPU#
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58.86 WLAN_CLK_CPU#

R1930
402R2F-GP

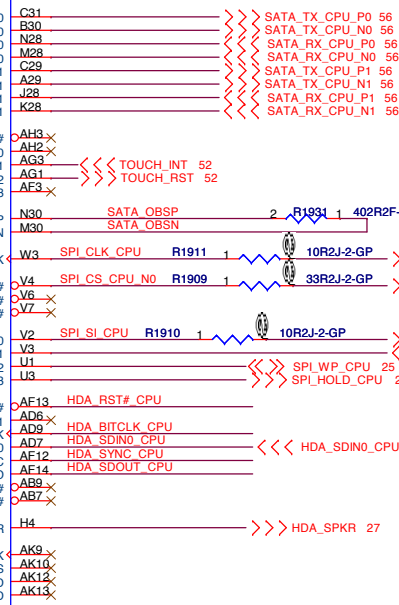
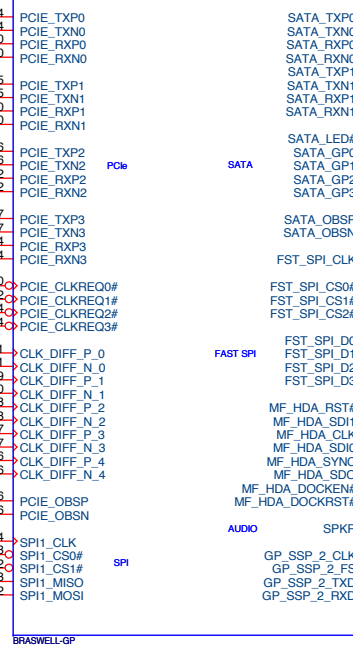


1D8V_S5



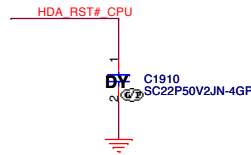
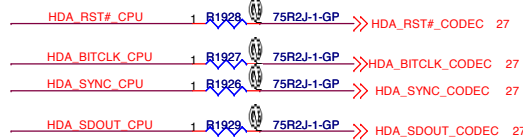
CPUID 4 OF 13

BRASWELL



HDD

ODD



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CPU (SATA/PCIE/HDA)	
Size A3	Document Number Domino
Date: Friday, March 20, 2015	Sheet 19 of 102

SSID = PCH

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Title

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Size

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Document Number

Domino

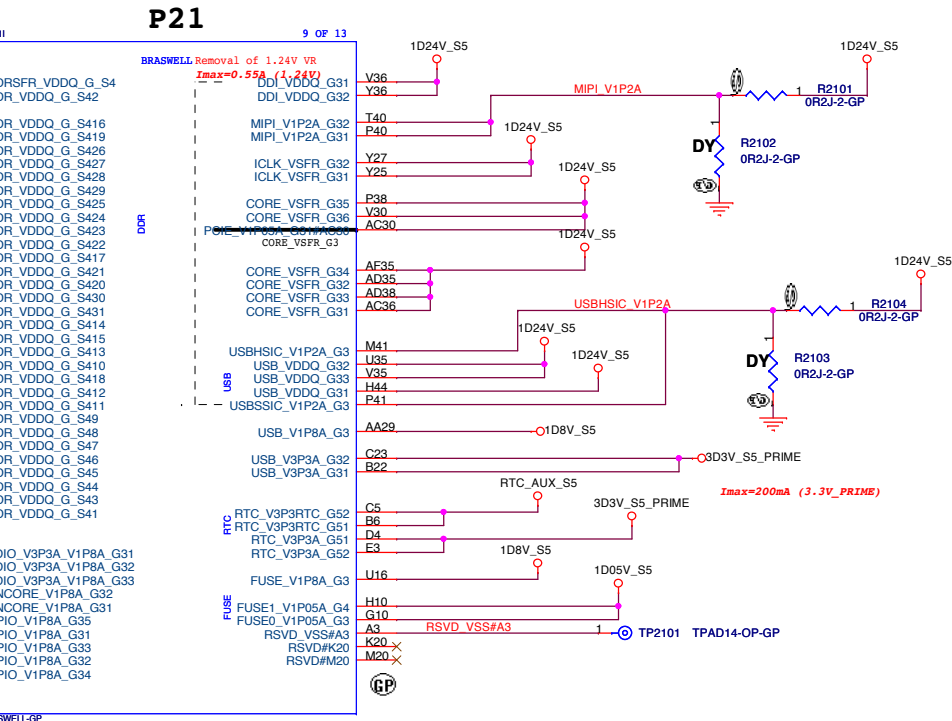
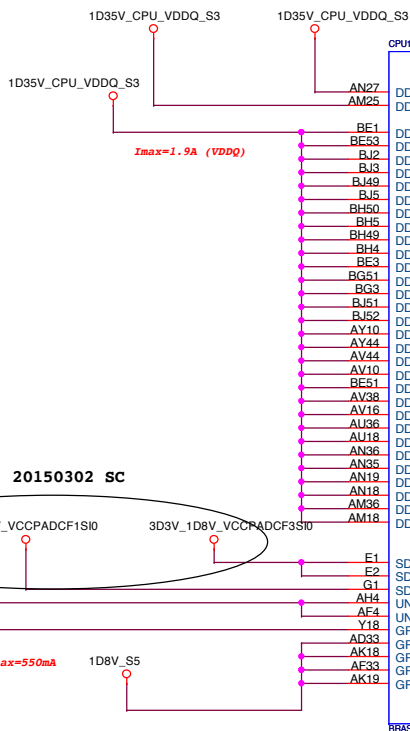
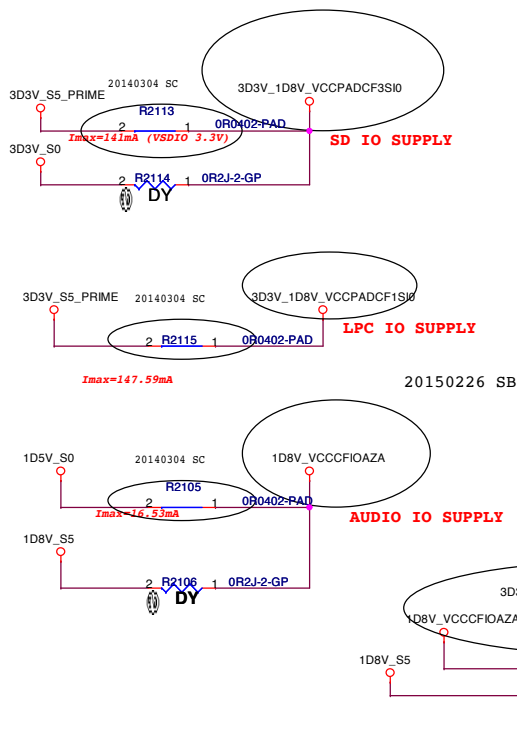
Rev

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Date: Friday, March 20, 2015

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Title CPU (POWER1)			
Size A3	Document Number	Domino	
Date: Friday, March 20, 2015	Sheet 21	of	102
			Rev -1

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Title		
(Reserved)		
Size A4	Document Number Domino	Rev -1
Date: Friday, March 20, 2015	Sheet 22 of	102

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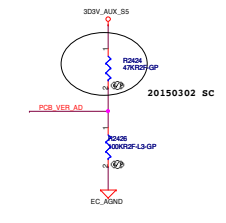
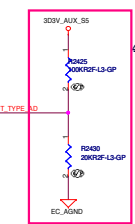
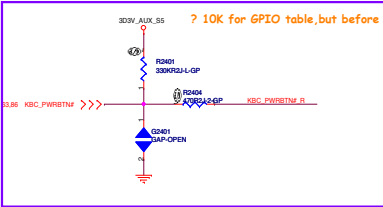
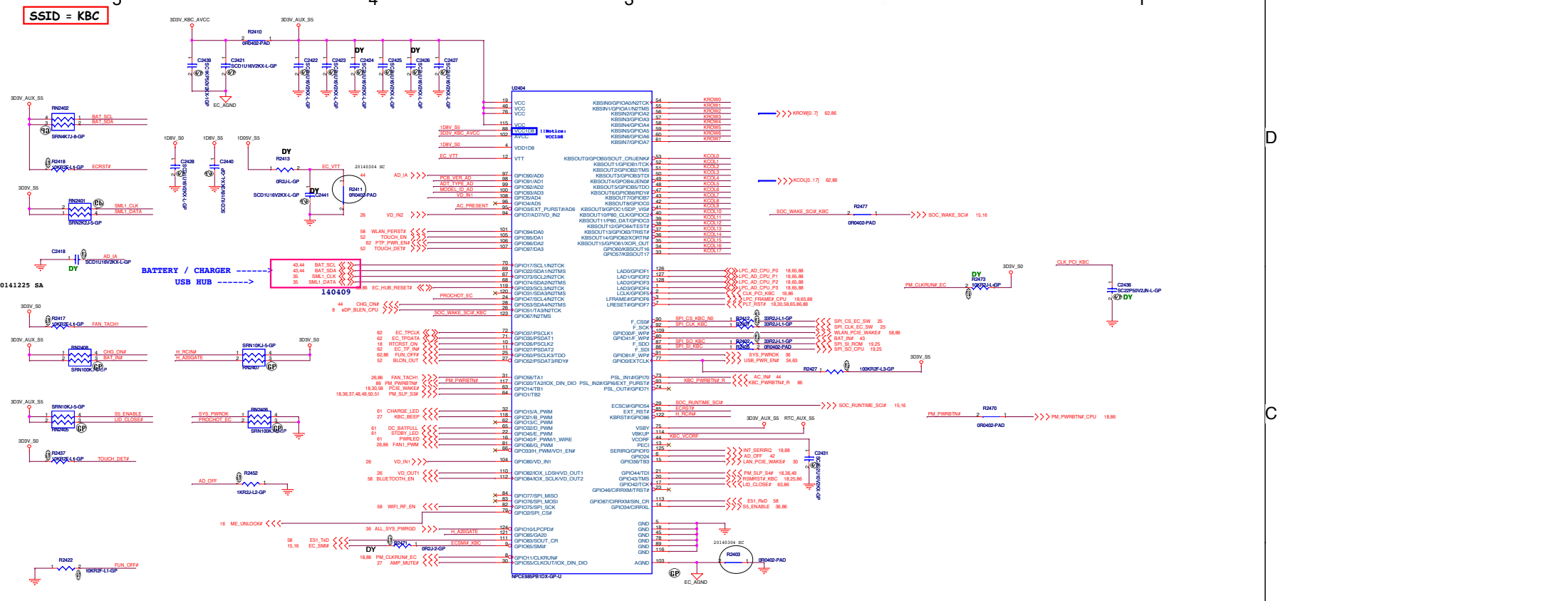
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Title			
(Reserved)			
Size	Document Number		Rev
A4	Domino		-1
Date:	Friday, March 20, 2015	Sheet 23 of	102

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SSID = KBC



PCB_VEB_AD	Pull-Low Register	Pull-High Register	KBC Firmware Setting
SA	100.0 K	10.0 K	
SB	100.0 K	20.0 K	< 2.875 V
SC	100.0 K	33.0 K	< 2.616 V
1	100.0 K	47.0 K	< 2.253 V
Reserved for project use	100.0 K	64.9 K	< 2.123 V
Reserved for project use	100.0 K	76.8 K	< 1.934 V

MODEL_ID_AD	Pull-Low Register	Pull-High Register	KBC Firmware Setting
N/A	100.0 K	10.0 K	
SA	100.0 K	20.0 K	< 2.875 V
SB	100.0 K	33.0 K	< 2.616 V
SC	100.0 K	47.0 K	< 2.253 V
Reserved for project use	100.0 K	64.9 K	< 2.123 V
Reserved for project use	100.0 K	76.8 K	< 1.934 V

ADT_TYPE	Pull-Low Register	Pull-High Register	KBC Firmware Setting
95W	100.0 K	N/A	< 0.150 V
80W	100.0 K	100.0 K	< 0.425 V
40W	20.0 K	100.0 K	< 0.684 V
120W	33.0 K	100.0 K	< 0.937 V
47.0 K	47.0 K	100.0 K	< 1.177 V
150W	64.9 K	100.0 K	< 1.398 V
Reserved	76.8 K	100.0 K	< 1.542 V
Reserved	100.0 K	100.0 K	< 1.842 V

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Wistron Corporation
 27F, 30F, 31F, 1st Floor, No. 10, Hsinchu
 Taipei Hsinchu 301, Taiwan, R.O.C.

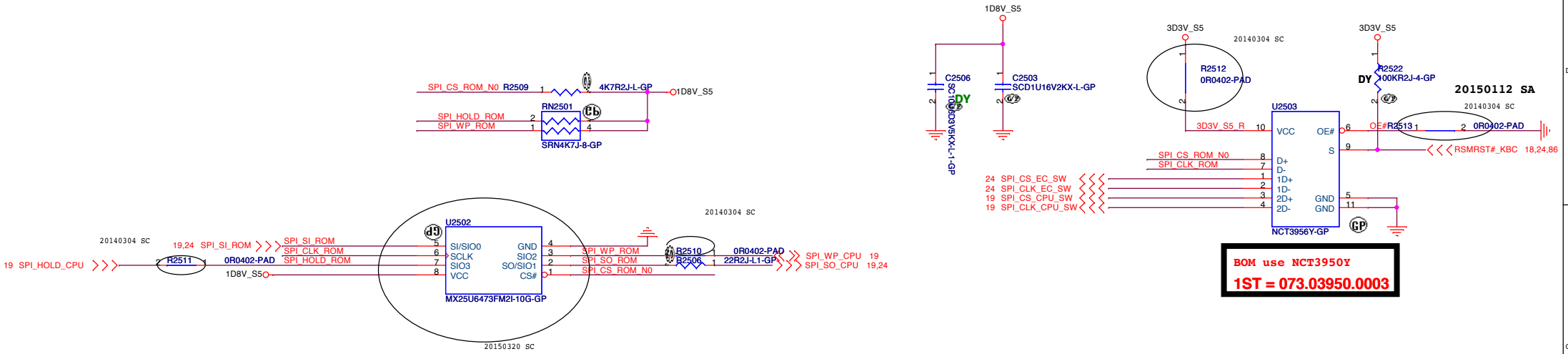
Project Name: **KBC NPCE985**

Rev: **Domino**

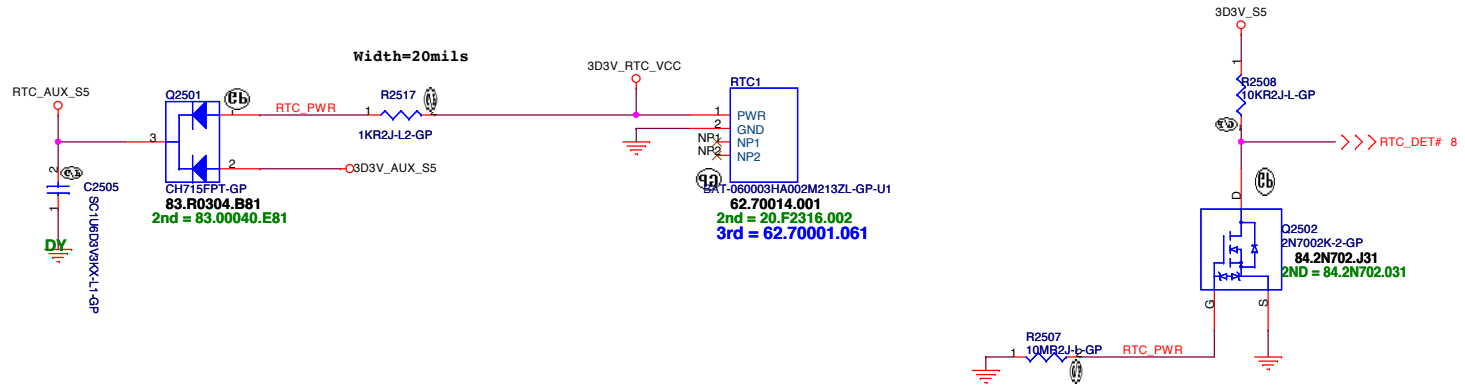
Page: 24 of 108

SSID = Flash.ROM

SPI FLASH ROM (8M BYTE) IC: PCH



SSID = RBAT



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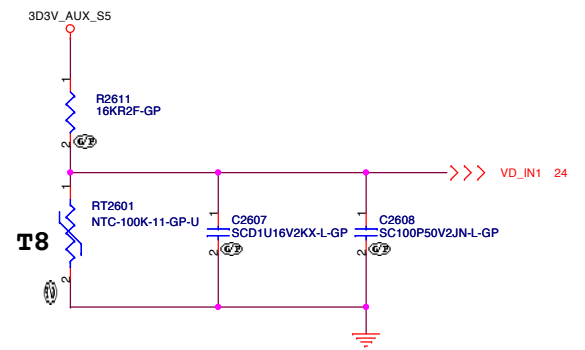
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Flash(KBC+PCH)/RTC**

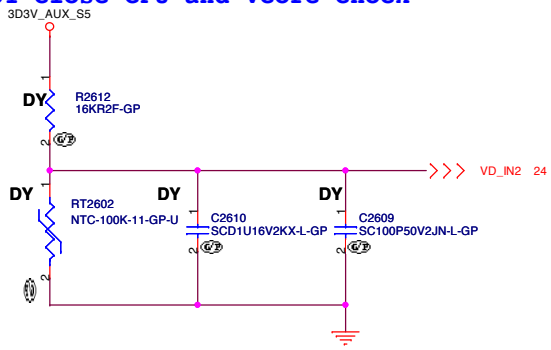
Size A3	Document Number	Rev -1
Date: Friday, March 20, 2015	Domino	Sheet 25 of 102

SSID = Thermal

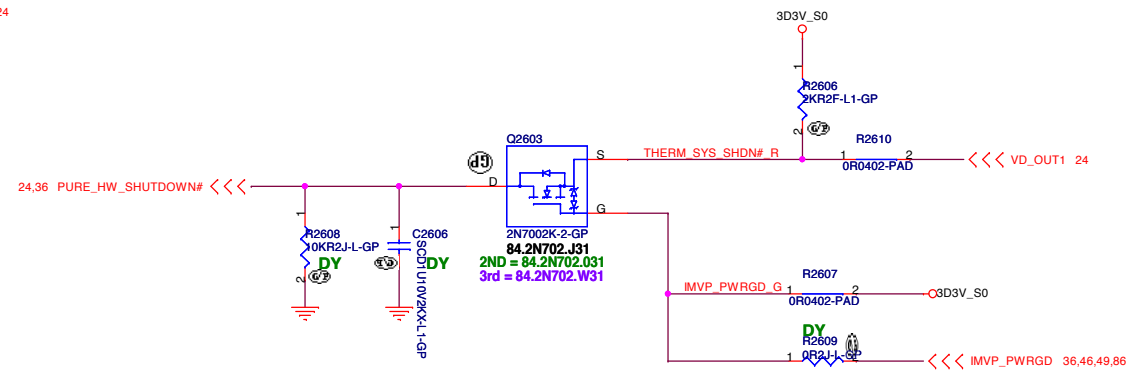
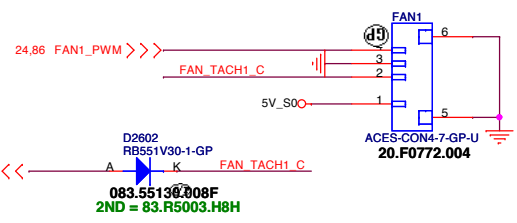
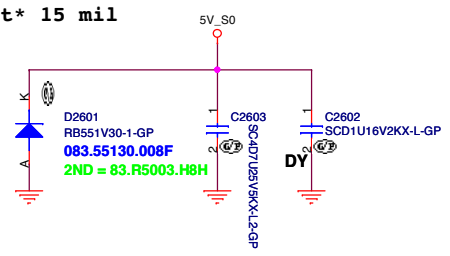
Layout 15 mil



PT2601 close CPU and Vcore chock



PT2602 close CPU and memory

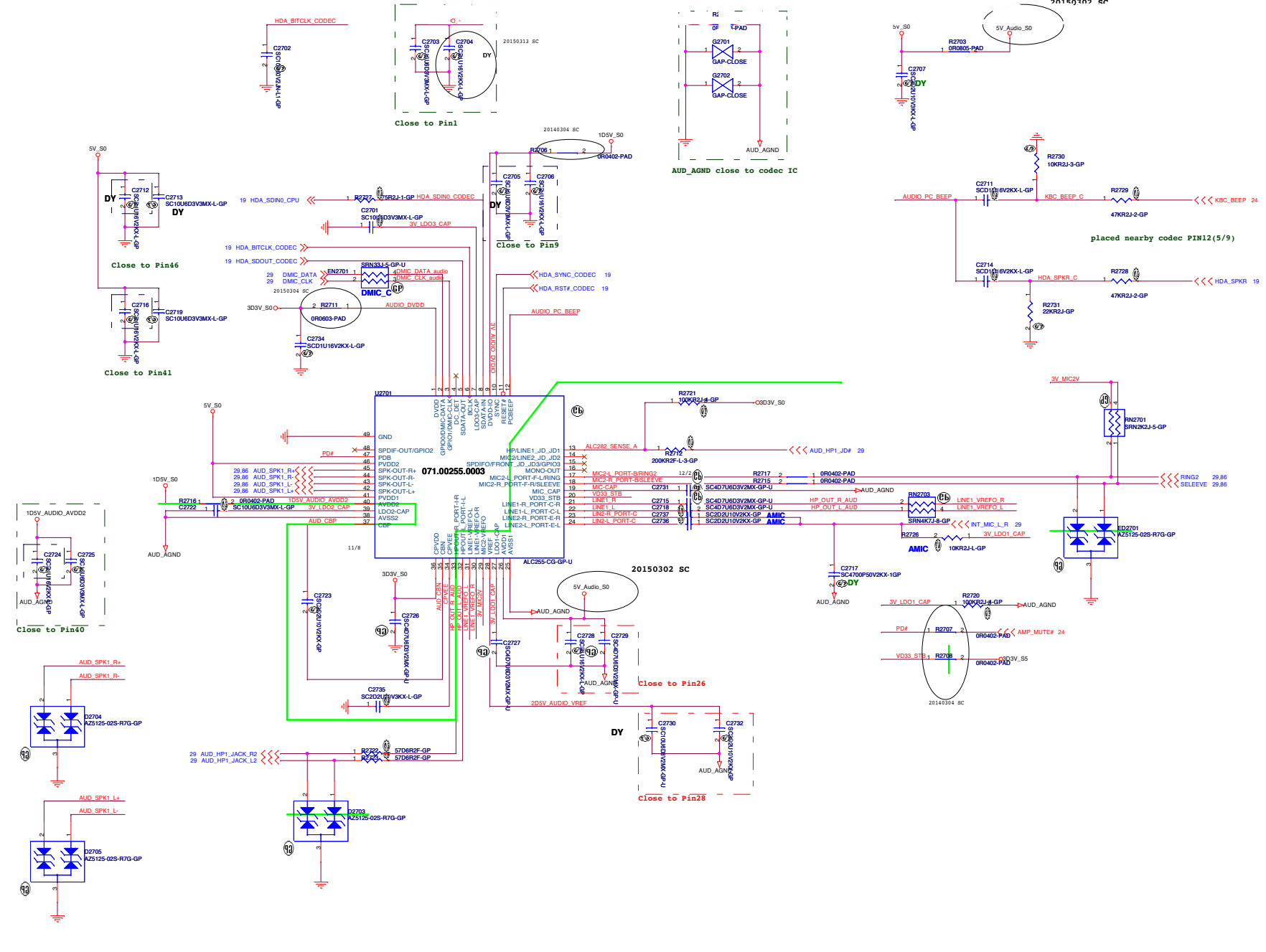


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Thermal 7718/Fan Controller P2793			
Title	Document Number		Rev
Size A3	Domino		-1
Date: Friday, March 20, 2015	Sheet 26	of 102	

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Title

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Size
A4

Document Number

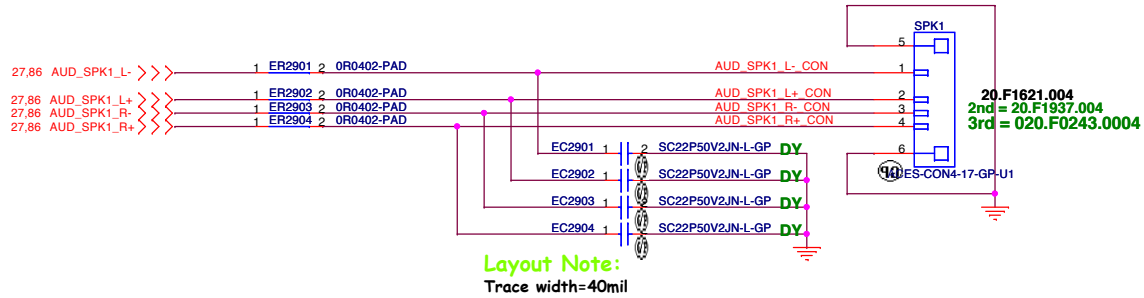
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Rev
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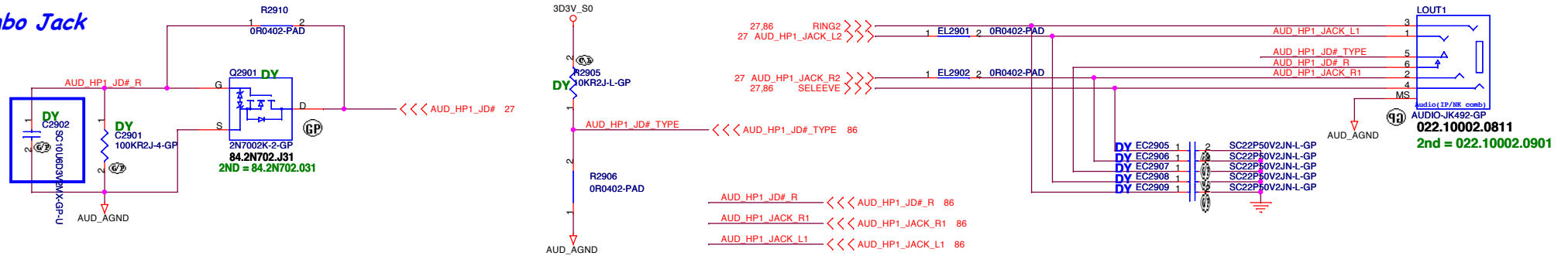
Date: Friday, March 20, 2015

Sheet 28 of 102

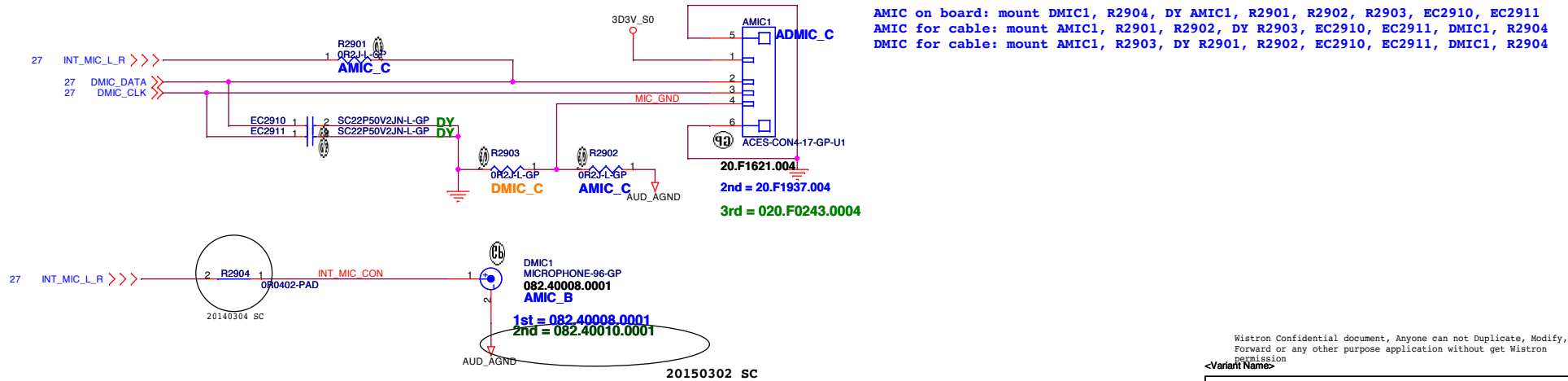
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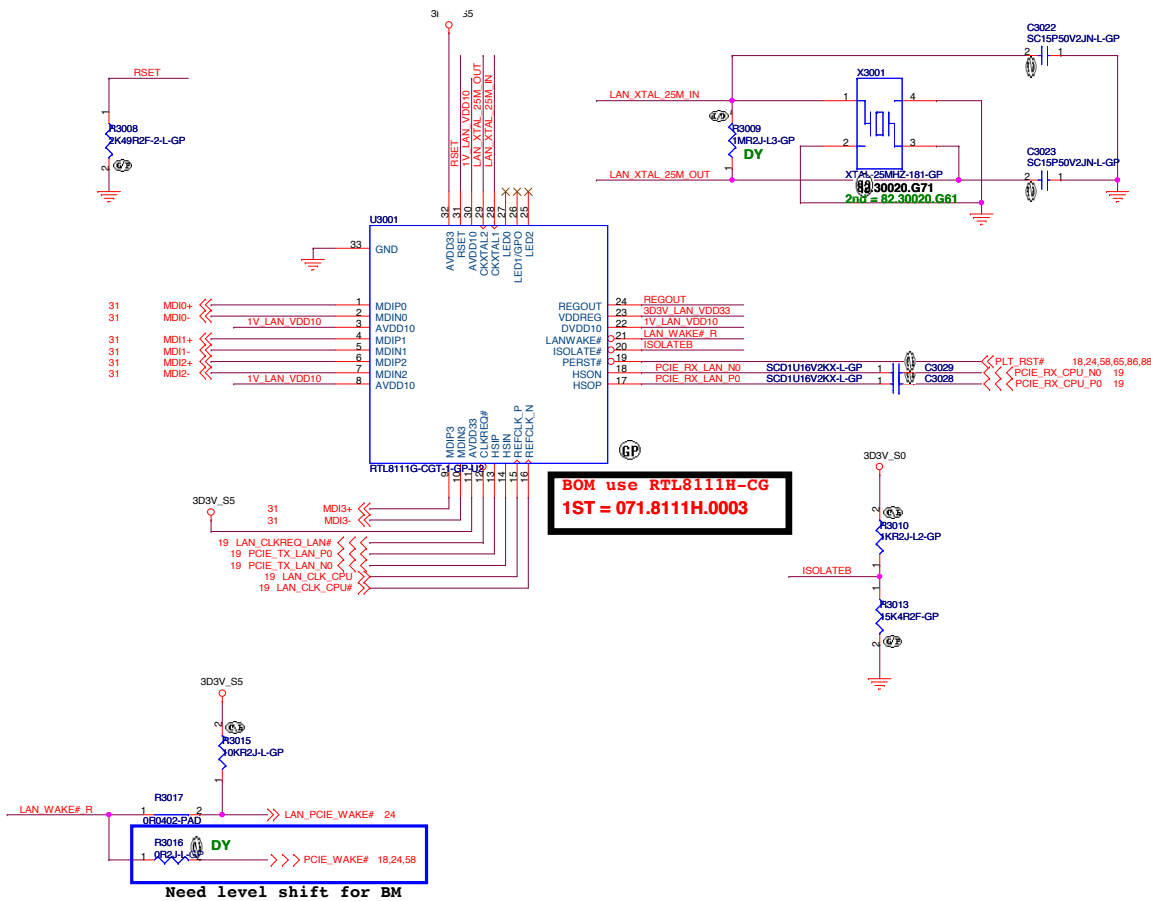
Combo Jack



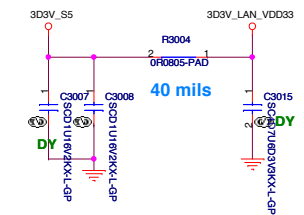
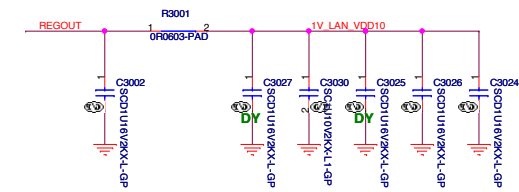
DMIC AMIC



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Layout:
 For RTL8111G(S)
 * Place C3021 to C3024 close to each VDD10 pin--3, 8,
 C3024: close to Pin8
 C3025: close to Pin30
 C3026: close to Pin3
 C3027: close to Pin22



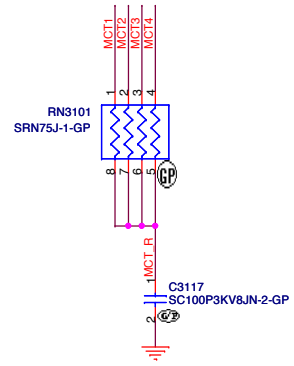
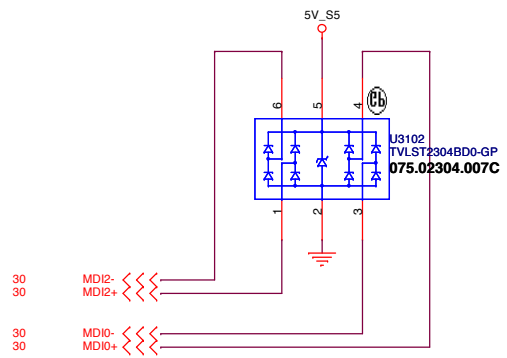
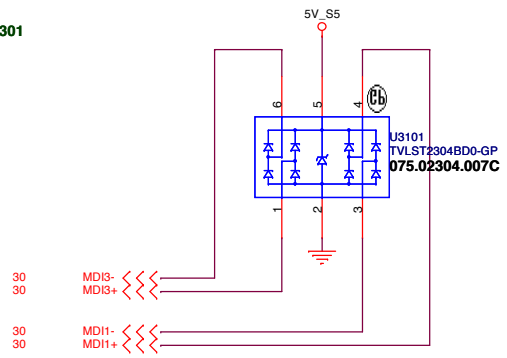
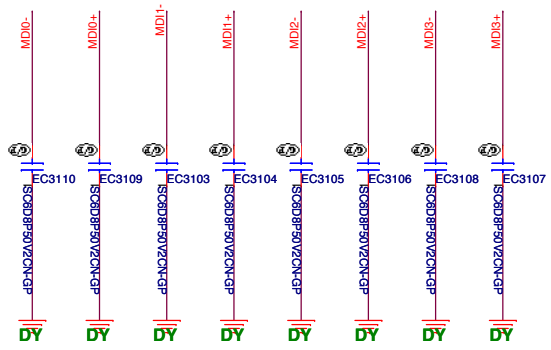
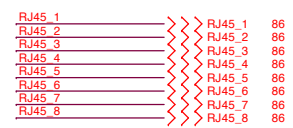
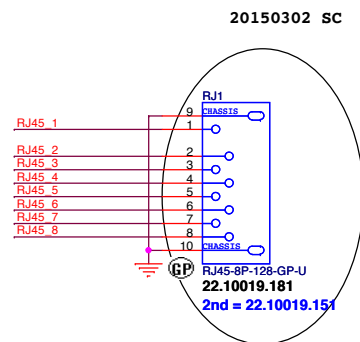
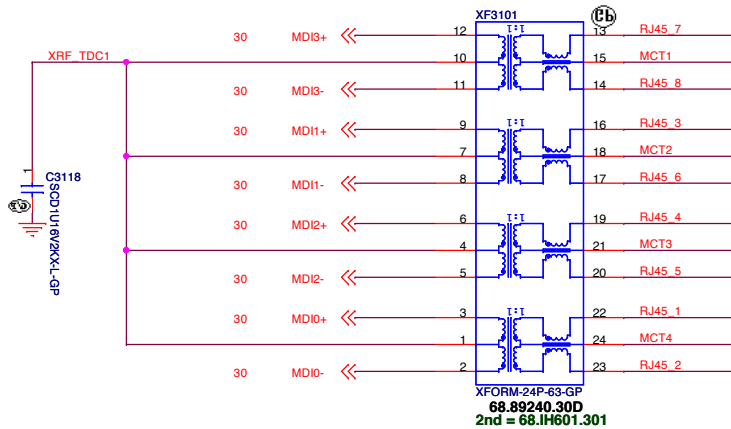
C3008: close to Pin32
 C3007: close to Pin11 (RTL8111 only)

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Title		
LAN(RTL8111)		
Size	Document Number	Rev
Custom	Domino	-1
Date:	Friday, March 20, 2015	Sheet 30 of 102

SSID = LAN



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Title: **(LAN+VGA) CONNECTOR**

Size A3 Document Number Rev -1

Date: Friday, March 20, 2015 Sheet 31 of 102

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Title **RTS5170(CARD READER)**

Size A4 Document Number **Domino** Rev **-1**

Date: Friday, March 20, 2015 Sheet 32 of 102

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SSID = SDIO

SD//MS Card Reader

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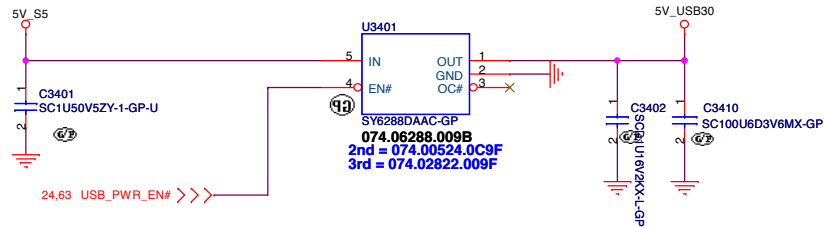
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Taipei Hsien 221, Taiwan, R.O.C.

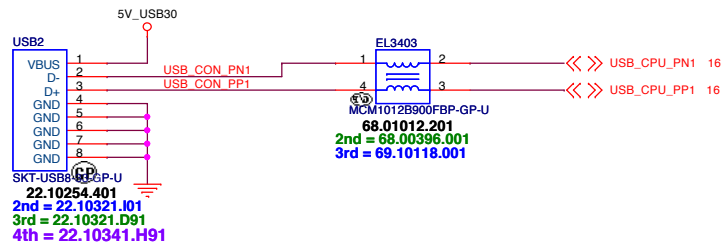
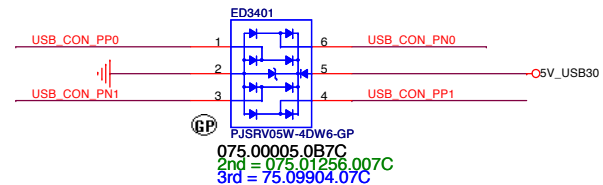
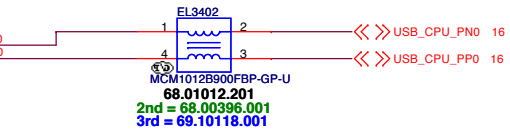
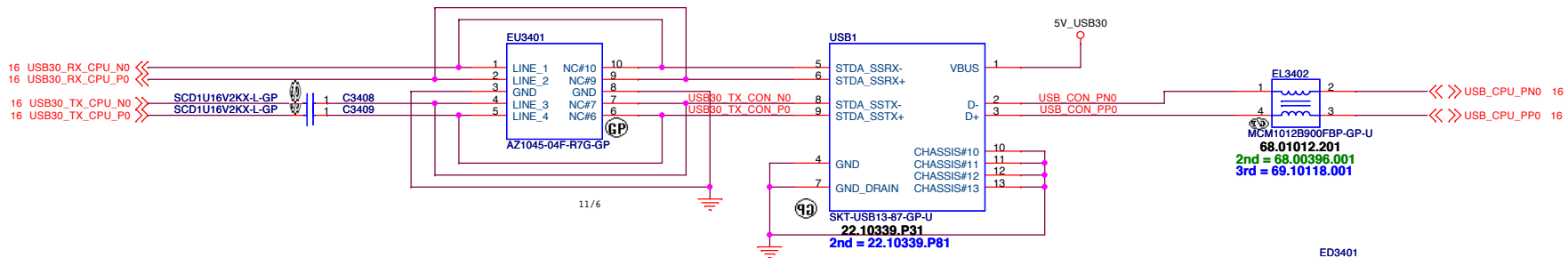
Title		
CARD Reader CONN		
Size	Document Number	Rev
Custom	Domino	-1
Date:	Friday, March 20, 2015	Sheet 33 of 102

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Low Active 2A



USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+



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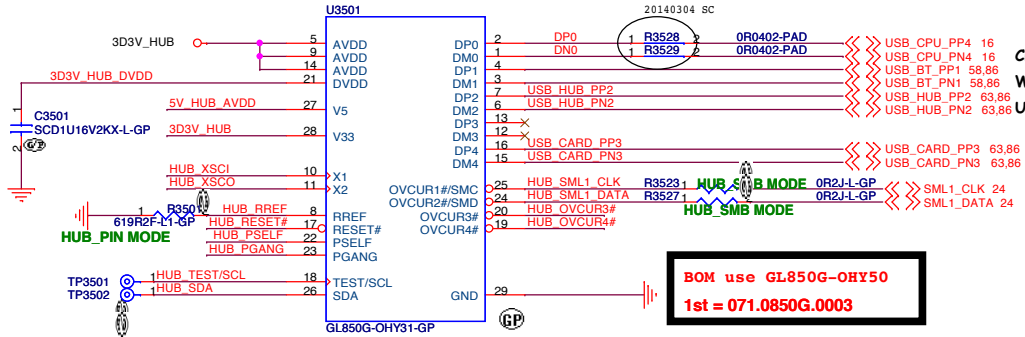
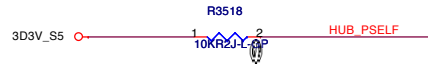
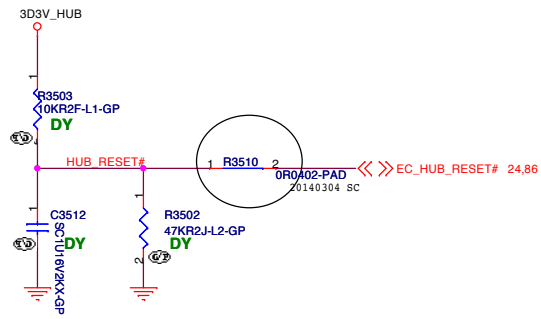
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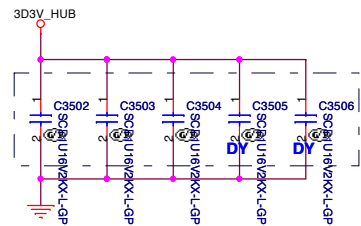
Title: **USB 2.0 / 3.0 Port**

Size A3 Document Number: **Domino** Rev: **-1**

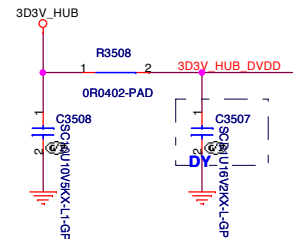
Date: Friday, March 20, 2015 Sheet 34 of 102



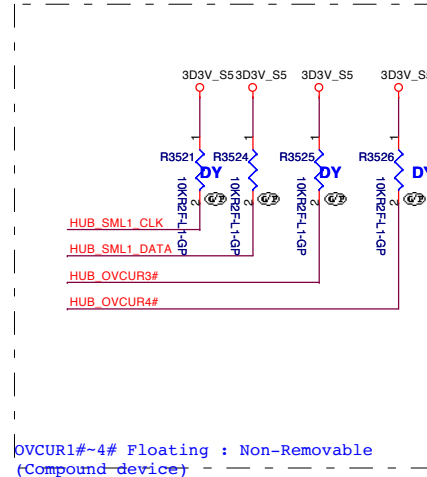
CPU
 WLAN(Bluetooth)
 USB 2.0(SMBD)
 not use
 Card reader



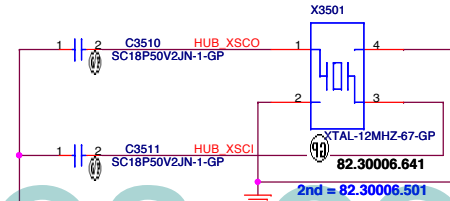
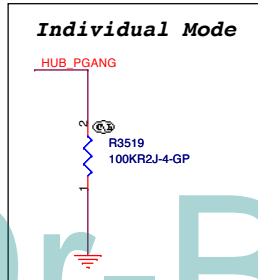
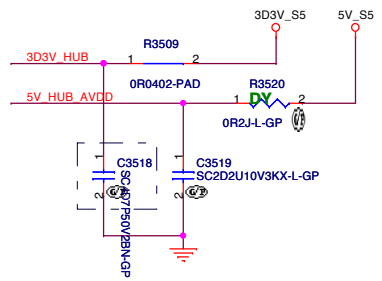
As close to GL850G-32



EC1 close to PIN28



OVCUR1#-4# Floating : Non-Removable (Compound device)



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Title		USB HUB	
Size	Document Number	Rev	
Custom	Domino	-1	
Date:	Friday, March 20, 2015	Sheet	35 of 102

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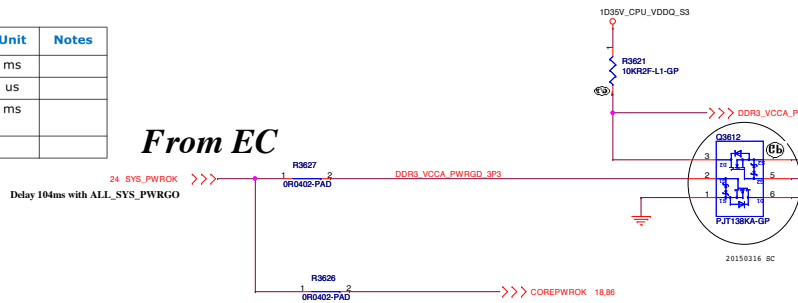
Power Sequence

Table 55. S4/S5 to S0 (Power Up) Sequence

Parameter		Min	Max	Unit	Notes
T0	RTC_VCC to ILB_RTC_TEST# de-assertion	9		ms	
T1	V3P3A valid to PMC_RSMRST# de-assertion	10		us	
T2	Core well stable to DRAM_CORE_PWRCK and PMC_CORE_PWRCK assertion	100		ms	
T3					

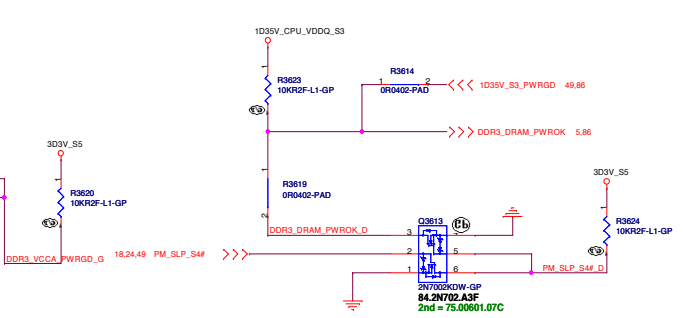
DDR3_VCCA_PWRGD

From EC

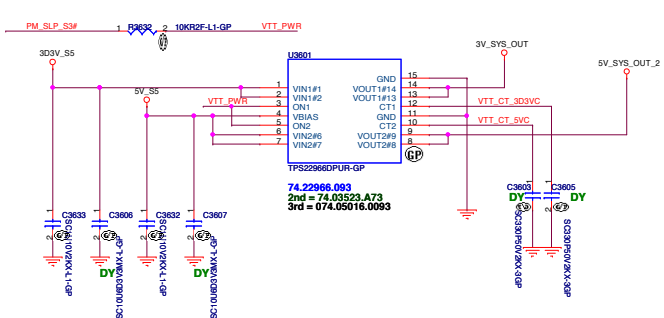


COREPWRCK

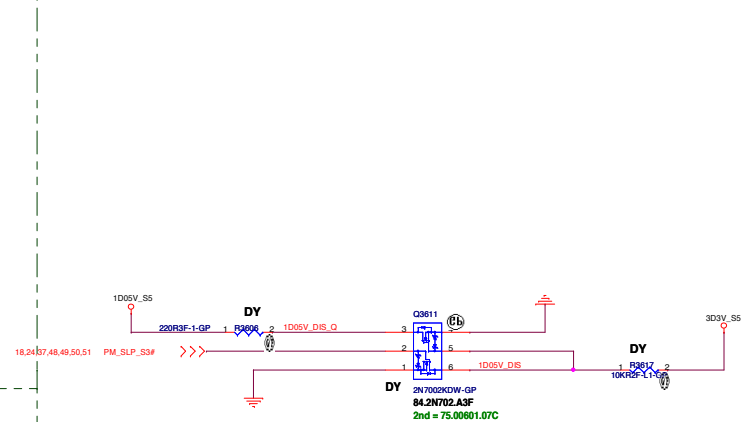
DDR3_DRAM_PWRCK



ANNIE Run Power

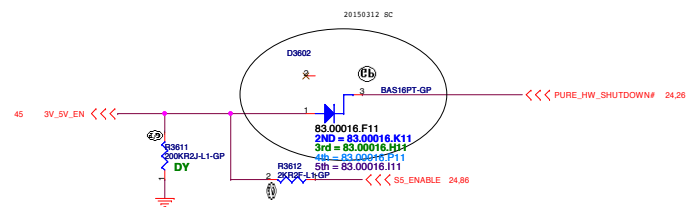
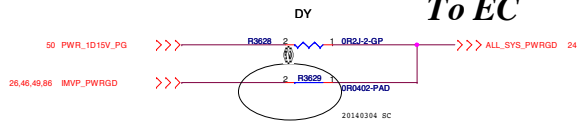


Discharge circuit

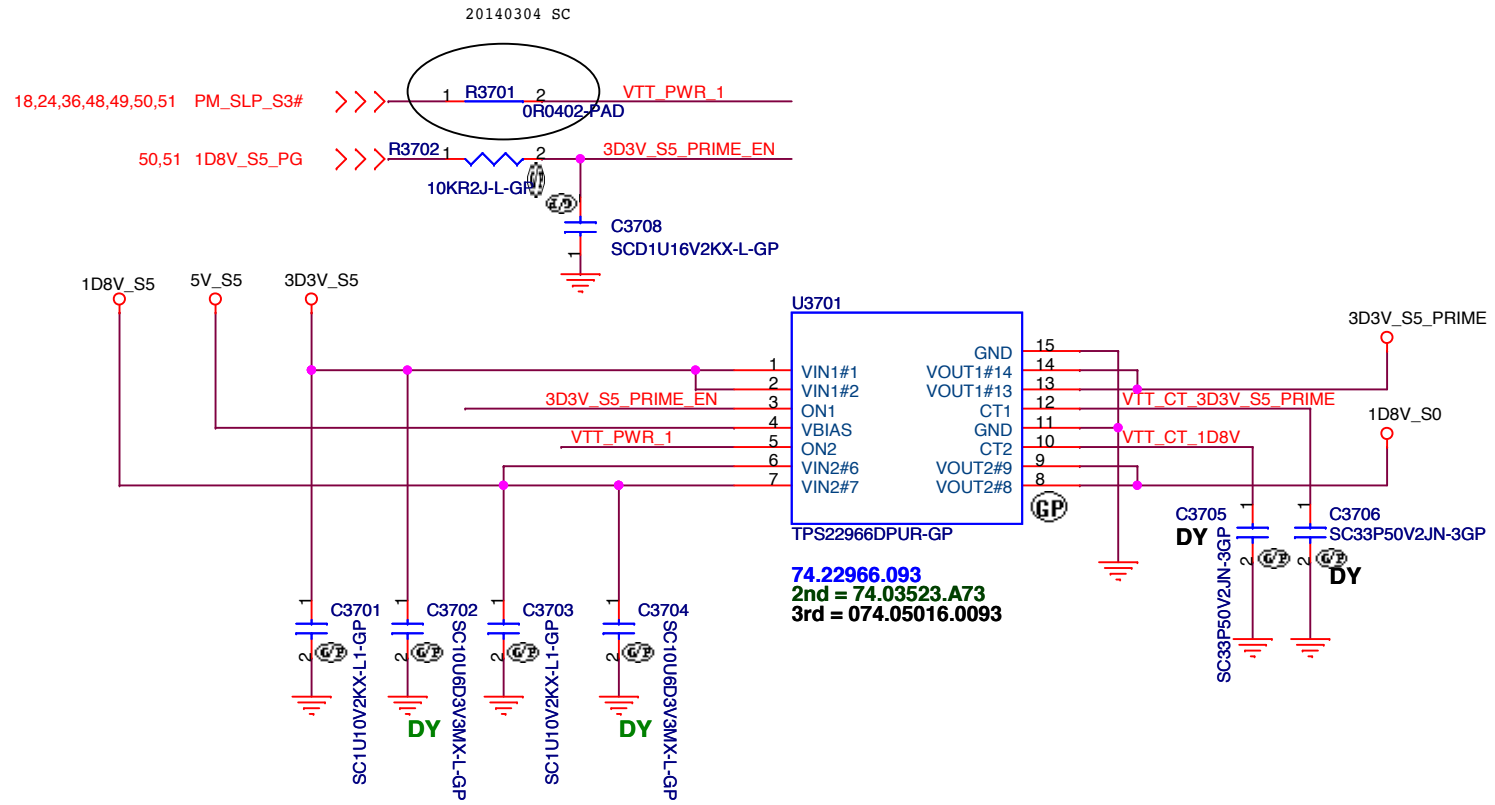


ALL_SYS_PWRGD

To EC



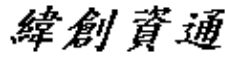
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74.22966.093
 2nd = 74.03523.A73
 3rd = 074.05016.0093

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Title	
ADAPTER OCP / S3 reduction	
Size	Document Number
A4	Domino
Date:	Rev
Friday, March 20, 2015	-1
Sheet	of
37	102

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Reserved			
Size A3	Document Number Domino	Rev -1	
Date: Friday, March 20, 2015	Sheet 40	of 102	

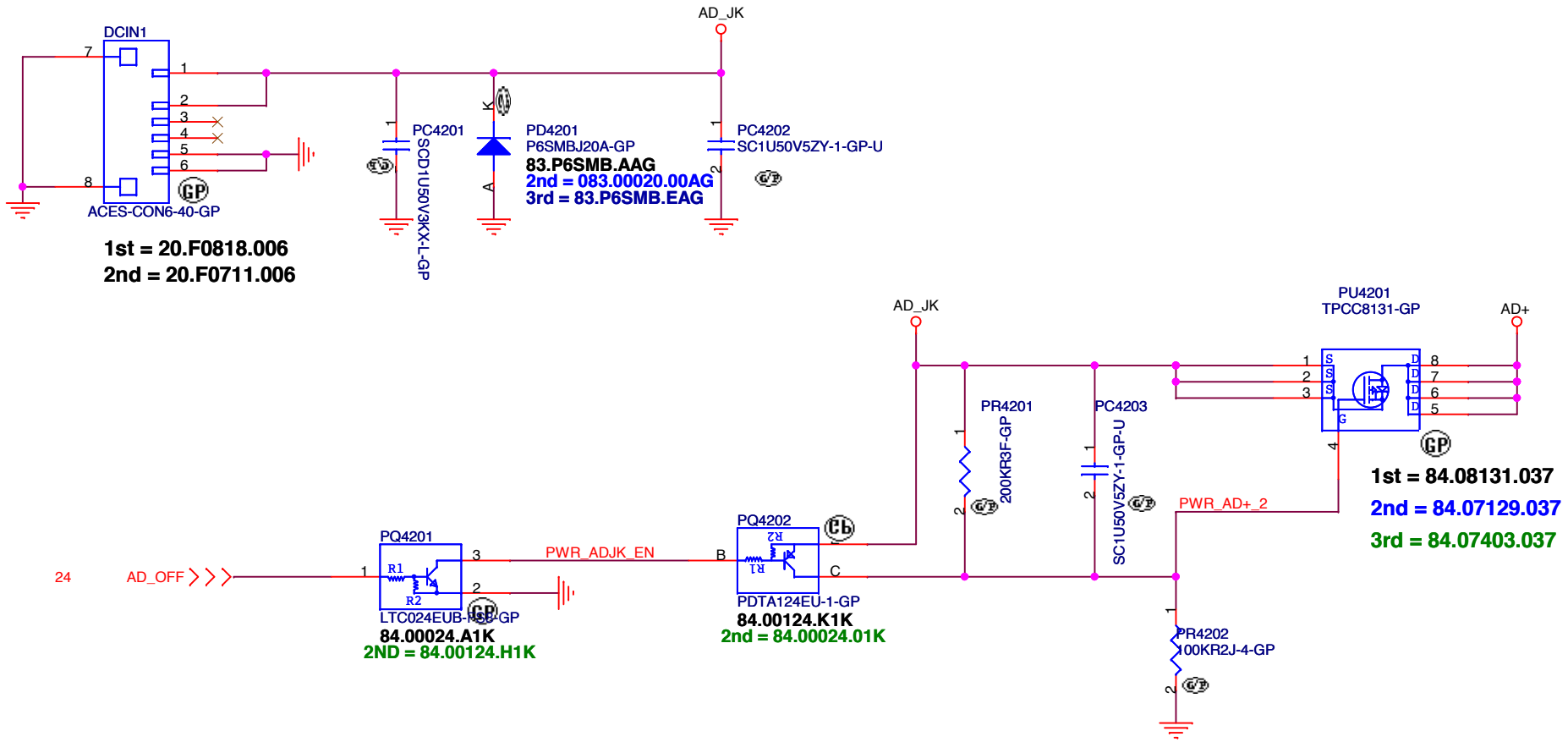
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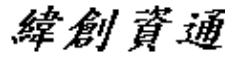
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		Reserved	
Size A4	Document Number	Rev -1	
Date: Friday, March 20, 2015		Sheet 41	of 102

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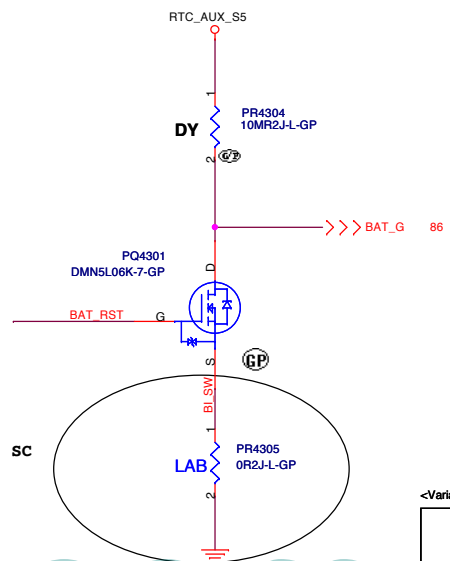
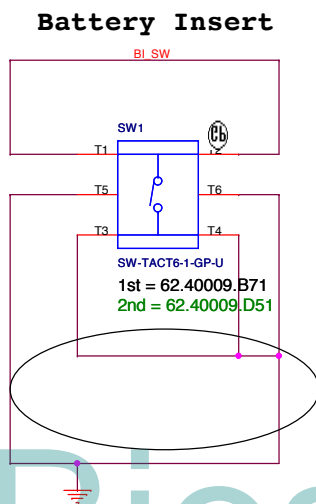
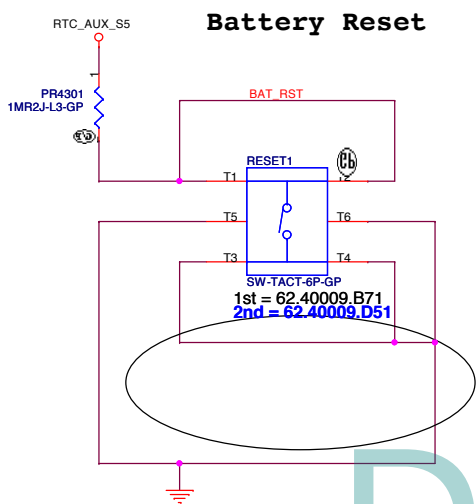
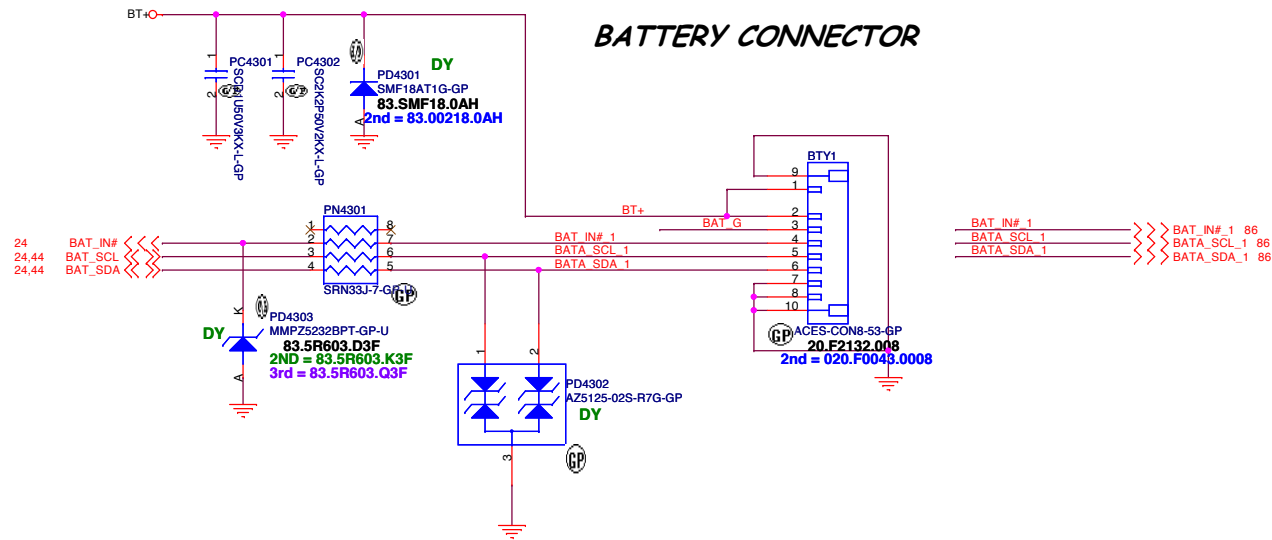
Adaptor in to generate DCBATOUT



<Variant Name>

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
DCIN JACK	
Title	
Size	Document Number
A4	Domino
Date:	Rev
Friday, March 20, 2015	-1
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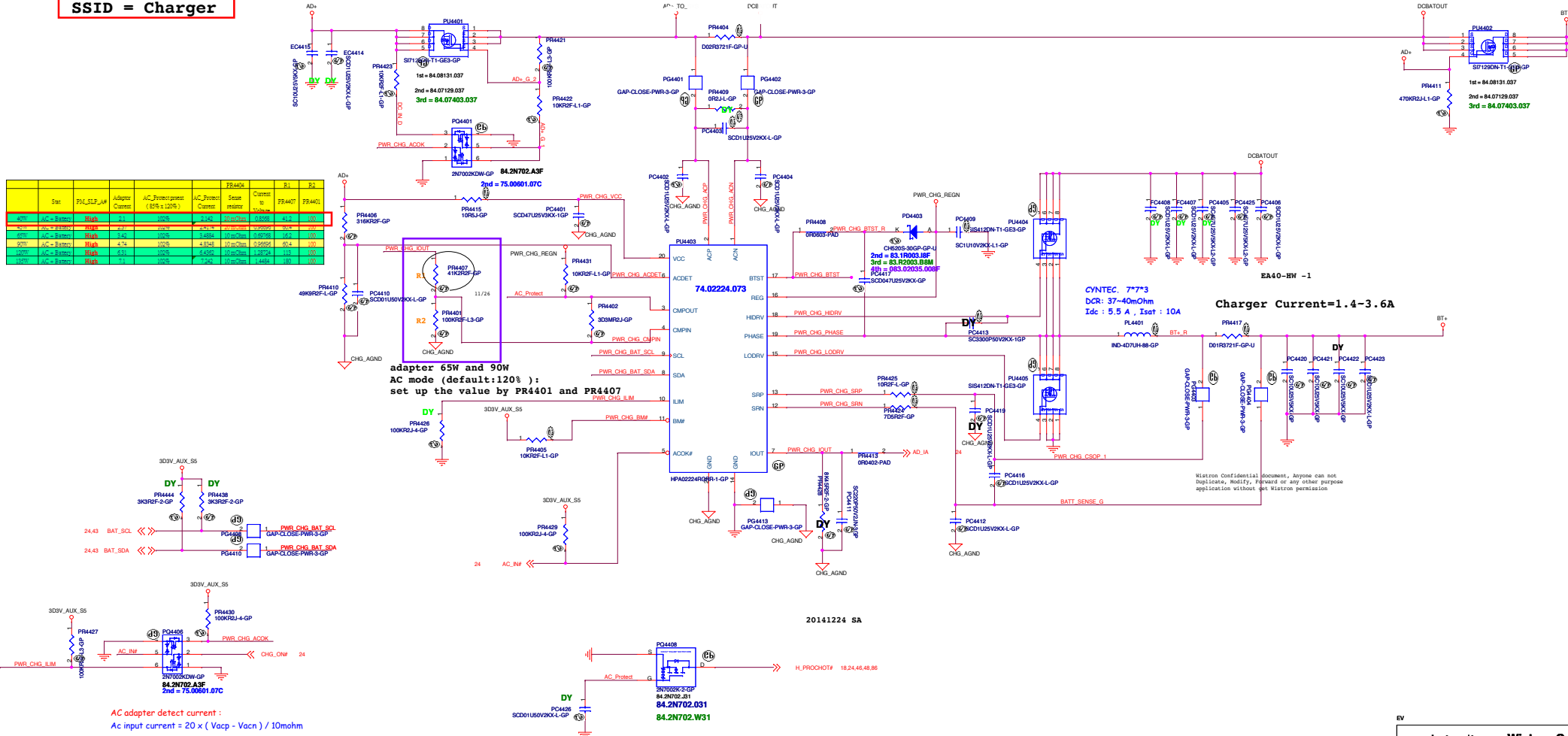


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Title BATT CONN		
Size A3	Document Number Domino	Rev -1
Date: Friday, March 20, 2015	Sheet 43 of 102	

SSID = Charger

Part	Qty	Ref	Value	Notes
PR4401	1	PR4401	10K	
PR4402	1	PR4402	10K	
PR4403	1	PR4403	10K	
PR4404	1	PR4404	10K	
PR4405	1	PR4405	10K	
PR4406	1	PR4406	10K	
PR4407	1	PR4407	10K	
PR4408	1	PR4408	10K	
PR4409	1	PR4409	10K	
PR4410	1	PR4410	10K	
PR4411	1	PR4411	10K	
PR4412	1	PR4412	10K	
PR4413	1	PR4413	10K	
PR4414	1	PR4414	10K	
PR4415	1	PR4415	10K	
PR4416	1	PR4416	10K	
PR4417	1	PR4417	10K	
PR4418	1	PR4418	10K	
PR4419	1	PR4419	10K	
PR4420	1	PR4420	10K	
PR4421	1	PR4421	10K	
PR4422	1	PR4422	10K	
PR4423	1	PR4423	10K	
PR4424	1	PR4424	10K	
PR4425	1	PR4425	10K	
PR4426	1	PR4426	10K	
PR4427	1	PR4427	10K	
PR4428	1	PR4428	10K	
PR4429	1	PR4429	10K	
PR4430	1	PR4430	10K	
PR4431	1	PR4431	10K	
PR4432	1	PR4432	10K	
PR4433	1	PR4433	10K	
PR4434	1	PR4434	10K	
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PR4436	1	PR4436	10K	
PR4437	1	PR4437	10K	
PR4438	1	PR4438	10K	
PR4439	1	PR4439	10K	
PR4440	1	PR4440	10K	
PR4441	1	PR4441	10K	
PR4442	1	PR4442	10K	
PR4443	1	PR4443	10K	
PR4444	1	PR4444	10K	
PR4445	1	PR4445	10K	
PR4446	1	PR4446	10K	
PR4447	1	PR4447	10K	
PR4448	1	PR4448	10K	
PR4449	1	PR4449	10K	
PR4450	1	PR4450	10K	



adapter 65W and 90W
AC mode (default:120%):
set up the value by PR4401 and PR4407

Charger Current=1.4-3.6A

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AC adapter detect current :
Ac input current = 20 x (V_{acc} - V_{accn}) / 10mohm

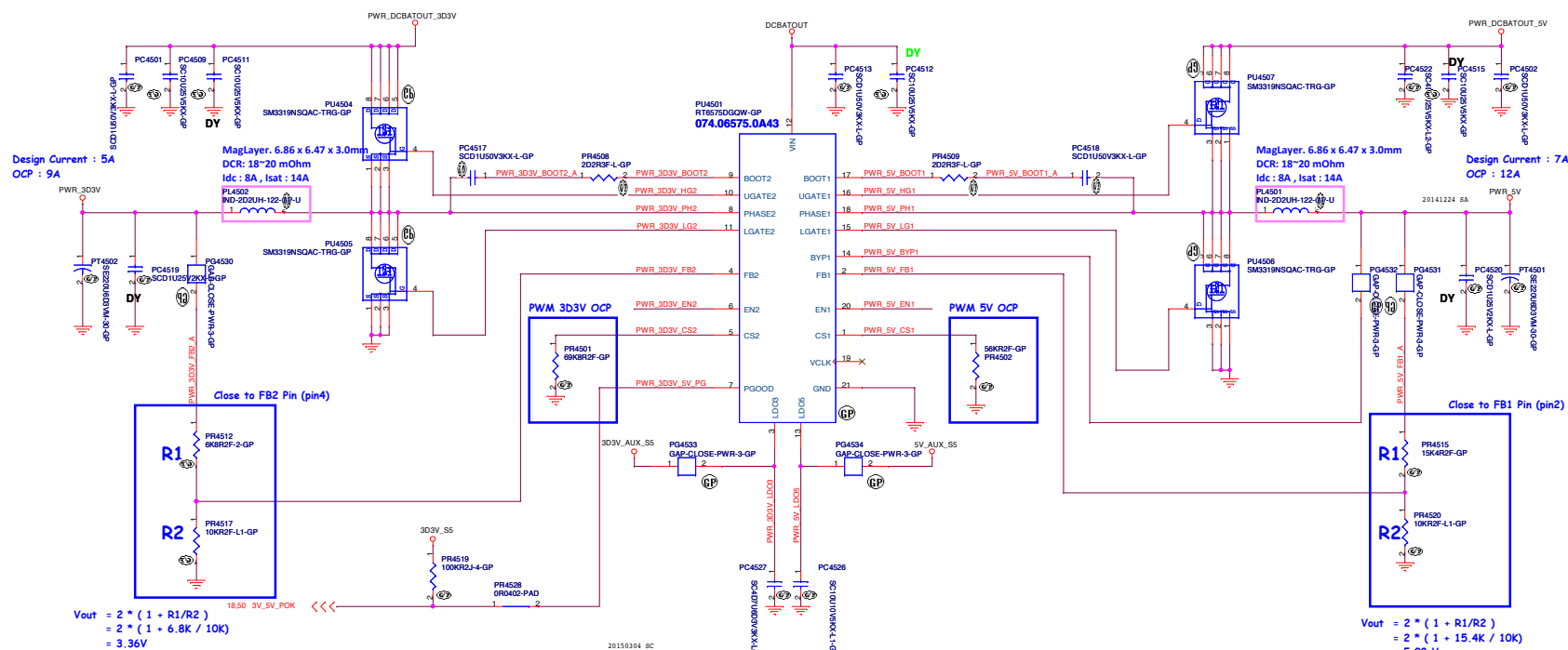
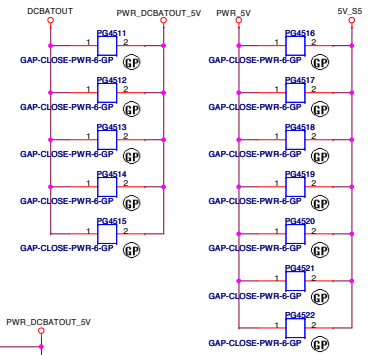
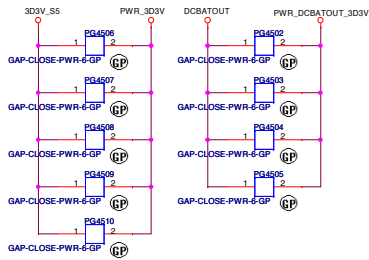
EV

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File: **CHARGER_HPA02224**

Doc: **Domino**

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$V_{out} = 2 * (1 + R1/R2)$
 $= 2 * (1 + 6.8K / 10K)$
 $= 3.36V$

$V_{out} = 2 * (1 + R1/R2)$
 $= 2 * (1 + 15.4K / 10K)$
 $= 5.08V$

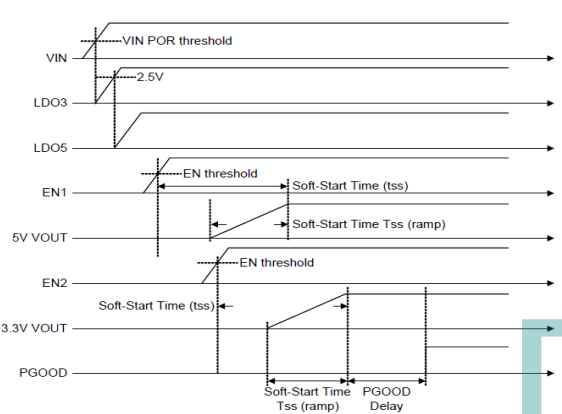
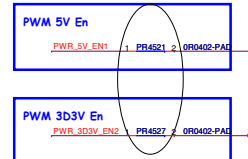


Figure 6. RT6575B Timing



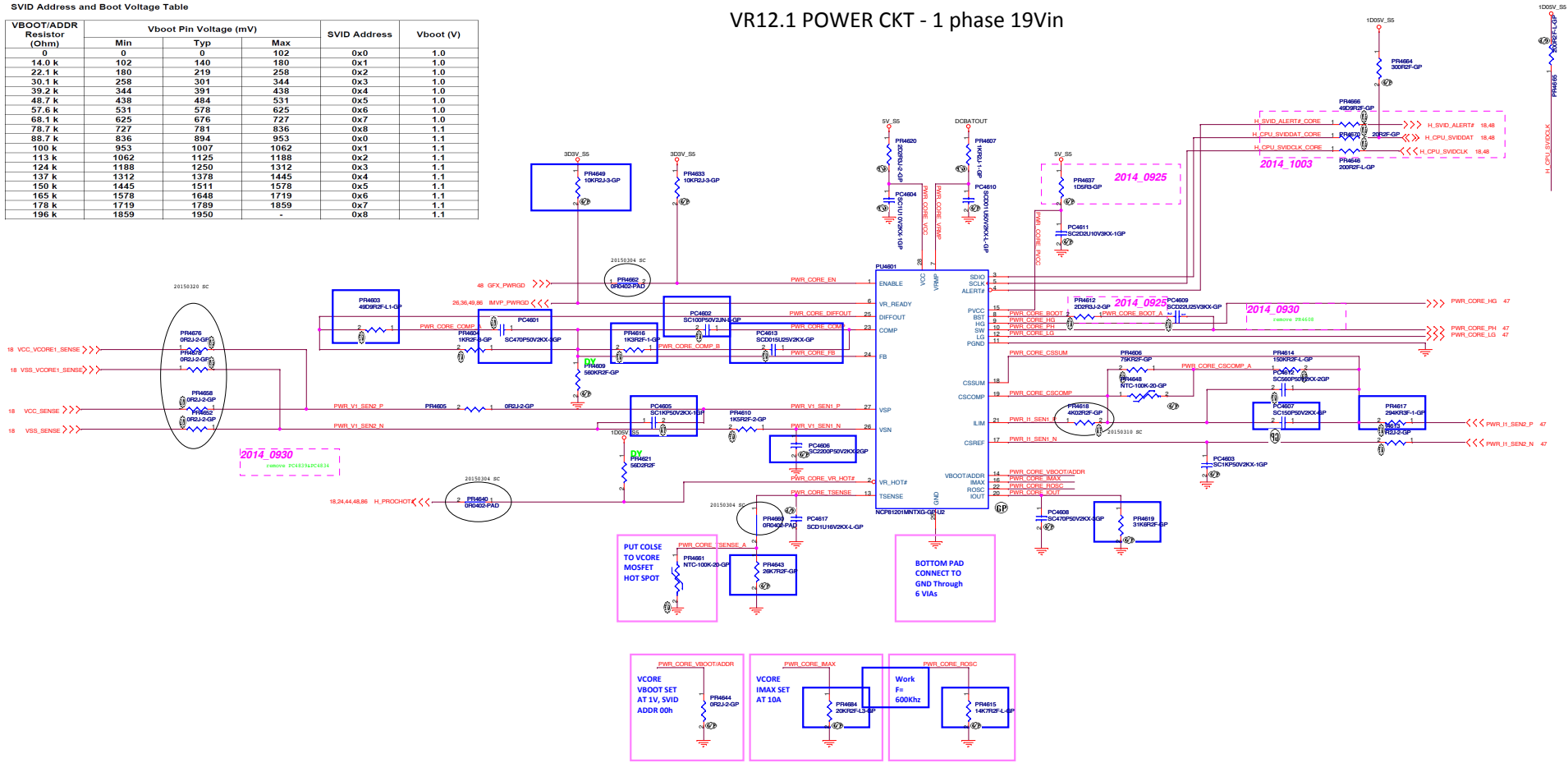
Vin POR threshold, Rising :4.6 V ; Failing : 3.7 V
 EN threshold Logic-High : 1.6 V
 EN threshold Logic-Low : 0.4 V

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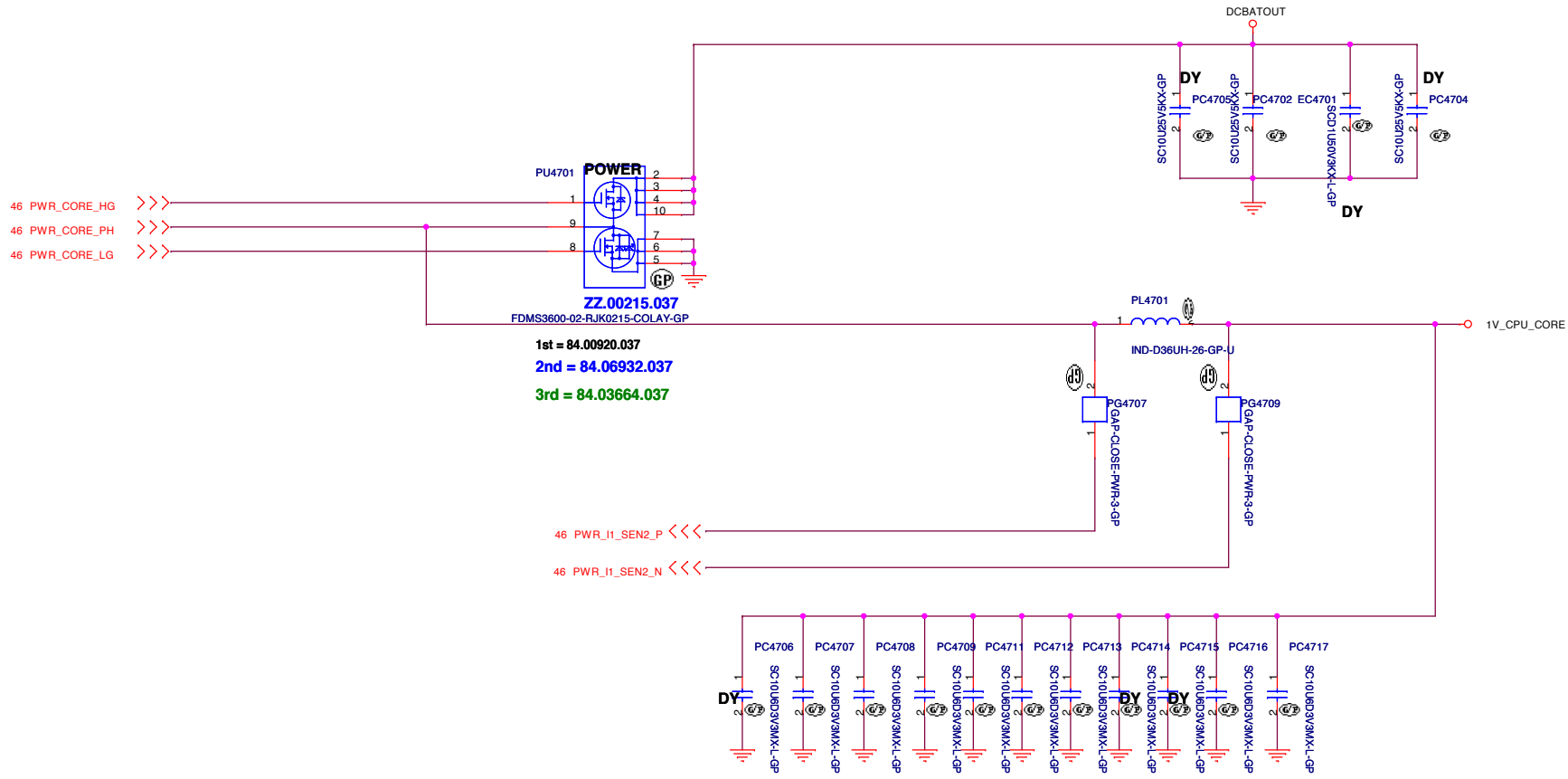
VR12.1 POWER CKT - 1 phase 19Vin

SVID Address and Boot Voltage Table

VBOOT/ADDR	Vboot Pin Voltage (mV)			SVID Address	Vboot (V)
	Resistor (Ohm)	Min	Typ		
0	0	0	102	0x0	1.0
14.0 k	102	140	180	0x1	1.0
22.1 k	180	219	258	0x2	1.0
30.1 k	258	301	344	0x3	1.0
39.2 k	344	391	438	0x4	1.0
48.7 k	438	484	531	0x5	1.0
57.6 k	531	578	625	0x6	1.0
68.1 k	625	676	727	0x7	1.0
78.7 k	727	781	836	0x8	1.1
88.7 k	836	894	953	0x0	1.1
100 k	953	1007	1062	0x1	1.1
113 k	1062	1125	1188	0x2	1.1
124 k	1188	1250	1312	0x3	1.1
137 k	1312	1378	1445	0x4	1.1
150 k	1445	1511	1578	0x5	1.1
165 k	1578	1648	1719	0x6	1.1
178 k	1719	1789	1859	0x7	1.1
196 k	1859	1950		0x8	1.1

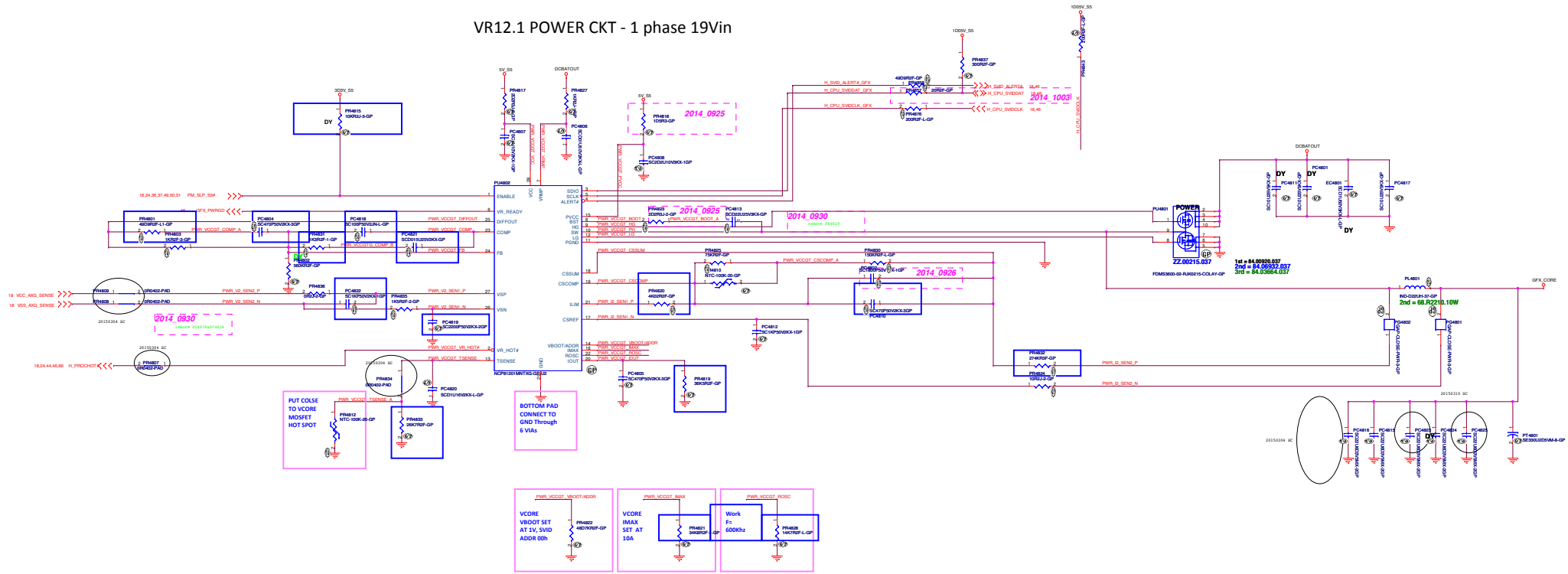


SSID = CPU Regulator



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VR12.1 POWER CKT - 1 phase 19Vin

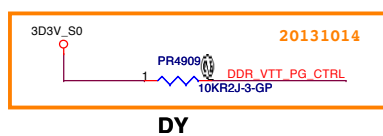
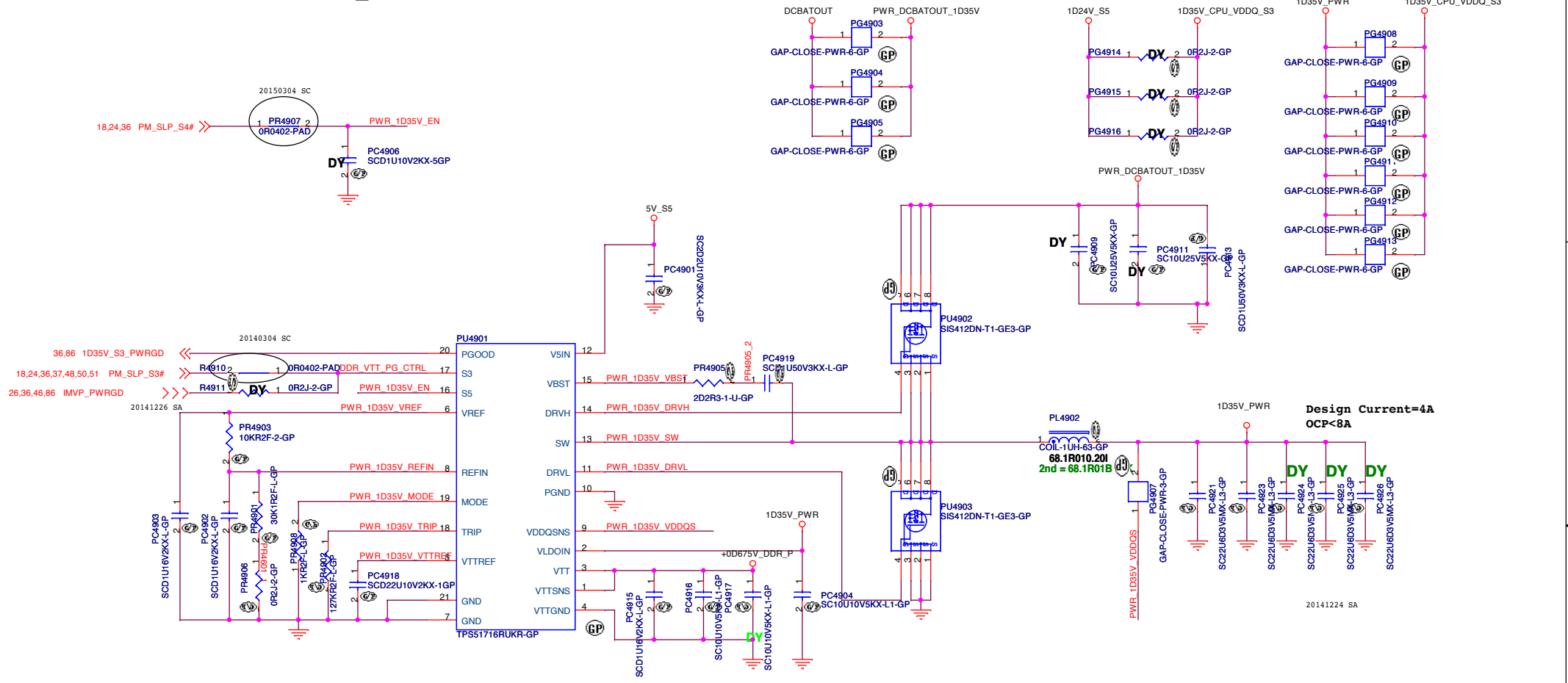


SVID Address and Boot Voltage Table

VBOOT/ADDR Resistor (Ohm)	Vboot Pin Voltage (mV)			SVID Address	Vboot (V)
	Min	Typ	Max		
0		0	102	0x0	1.0
14.0 k	102	140	180	0x1	1.0
22.1 k	180	219	258	0x2	1.0
30.1 k	258	301	344	0x3	1.0
39.2 k	344	391	438	0x4	1.0
49.7 k	438	494	531	0x5	1.0
57.6 k	531	578	625	0x6	1.0
68.1 k	625	676	727	0x7	1.0
78.7 k	727	781	836	0x8	1.1
88.7 k	836	894	953	0x0	1.1
100 k	953	1007	1062	0x1	1.1
113 k	1062	1125	1188	0x2	1.1
124 k	1188	1250	1312	0x3	1.1
137 k	1312	1378	1445	0x4	1.1
150 k	1445	1511	1578	0x5	1.1
165 k	1578	1648	1719	0x6	1.1
178 k	1719	1799	1859	0x7	1.1
196 k	1859	1950	-	0x8	1.1



SSID = PWR.Plane.Regulator_lp33v0p675v



DY

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

MODE

PR4608	Frequency	Discharge Mode
200k ohm	400kHz	Tracking Discharge
100k ohm	300kHz	
68k ohm	300kHz	Non-tracking Discharge
47k ohm	400kHz	

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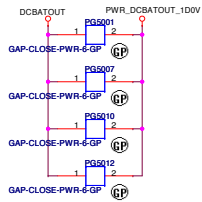
EV

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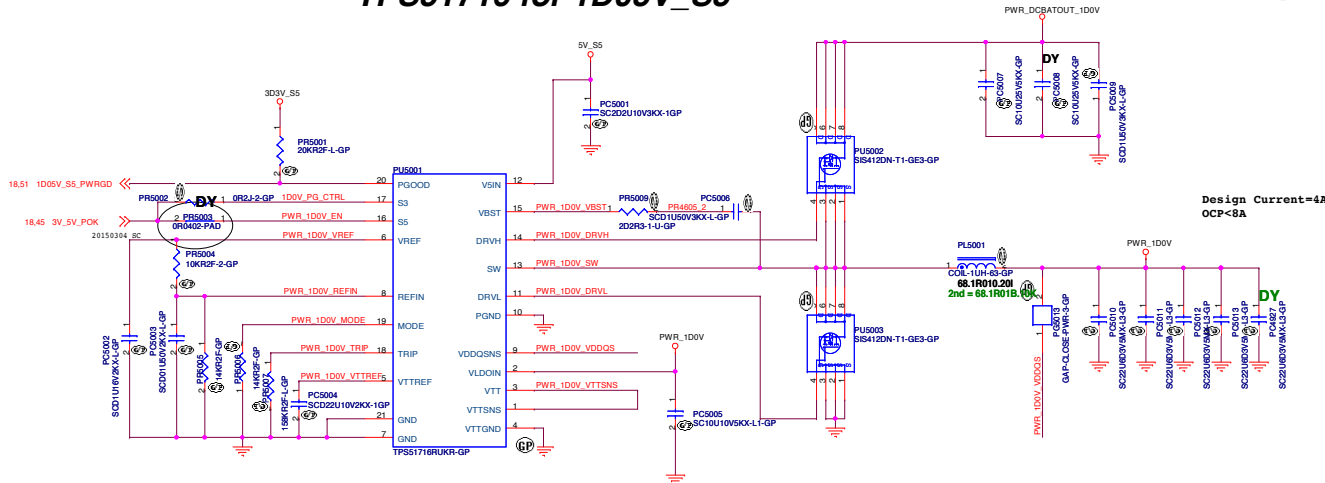
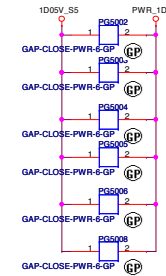
Title **TPS51716(1.35V_S3/0.675V_S0)**

Size A3 Document Number **Domino** Rev **-1**

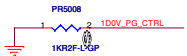
Date: Friday, March 20, 2015 Sheet 49 of 102



TPS51716 for 1D05V_S5



Design Current=4A
OCP=8A

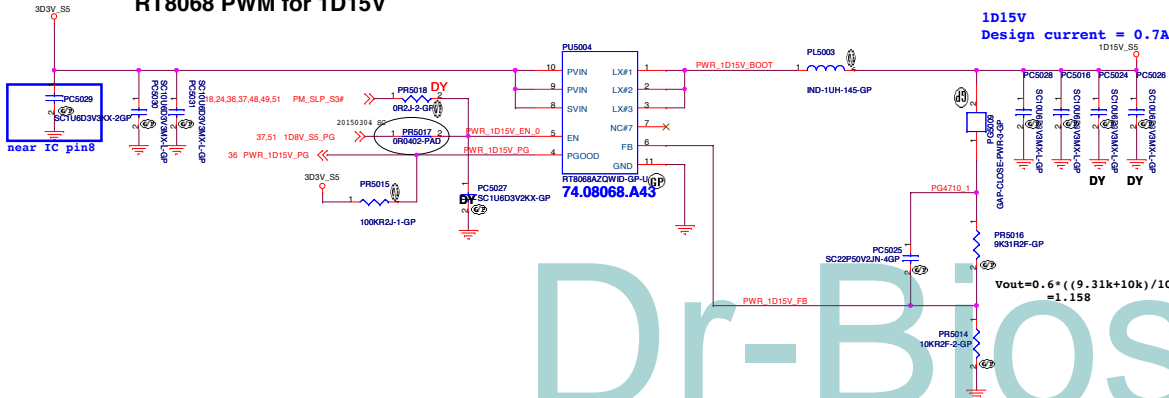


State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

MODE

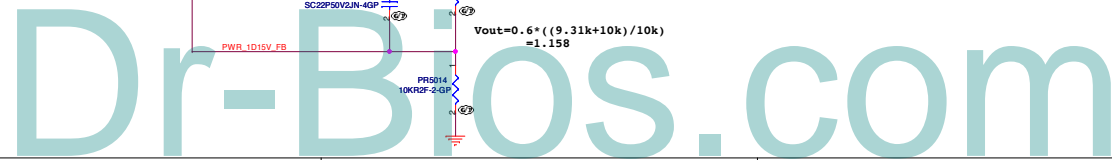
PR5006	Frequency	Discharge Mode
33k ohm	500kHz	Non-tracking Discharge
22k ohm	670kHz	
12k ohm	670kHz	Tracking Discharge
1k ohm	500kHz	

RT8068 PWM for 1D15V



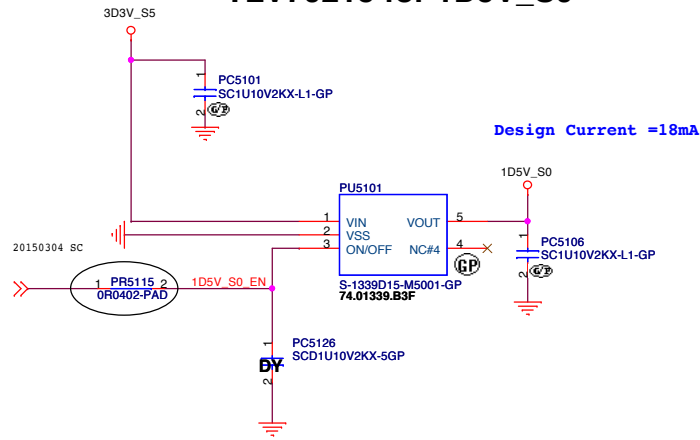
1D15V
Design current = 0.7A

$$V_{out} = 0.6 * ((9.31k + 10k) / 10k) = 1.158$$

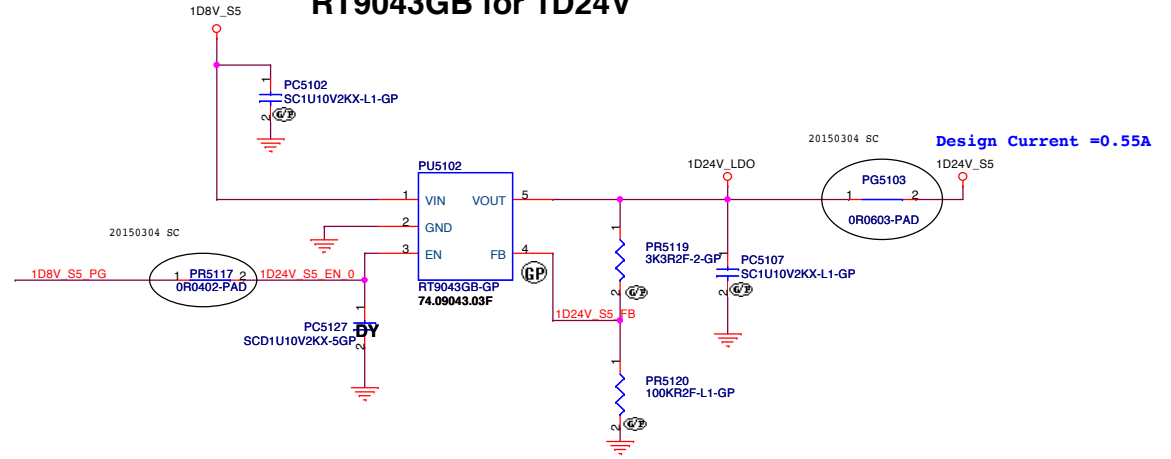


SSID = PWR.Plane.Regulator_1p5v

TLV70215 for 1D5V_S0

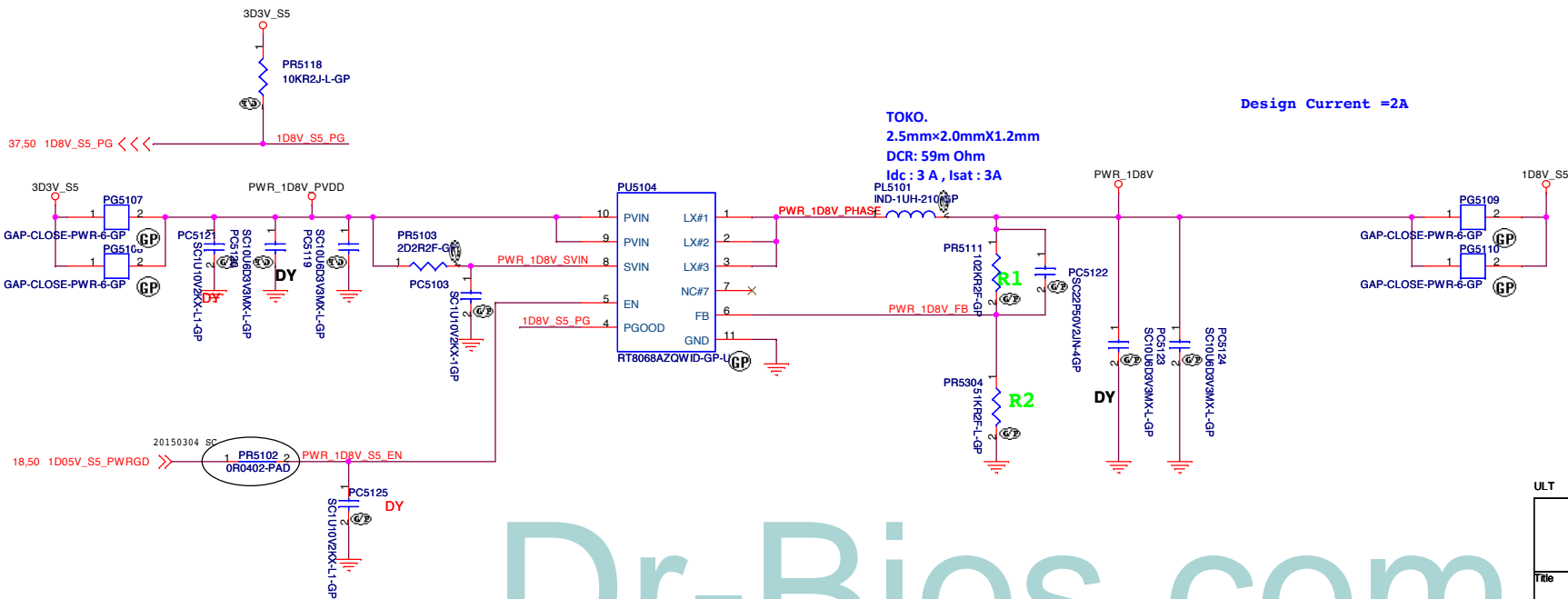


RT9043GB for 1D24V



SSID = PWR.Plane.Regulator_1p8v

RT8068AZQWID-GP-U for 1D8V_S5



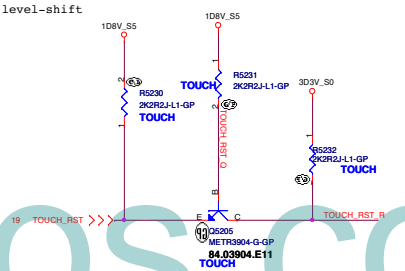
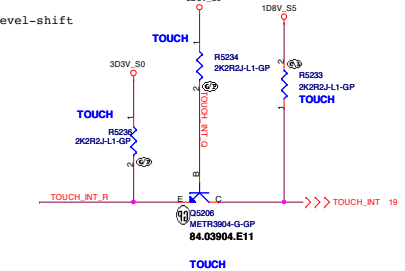
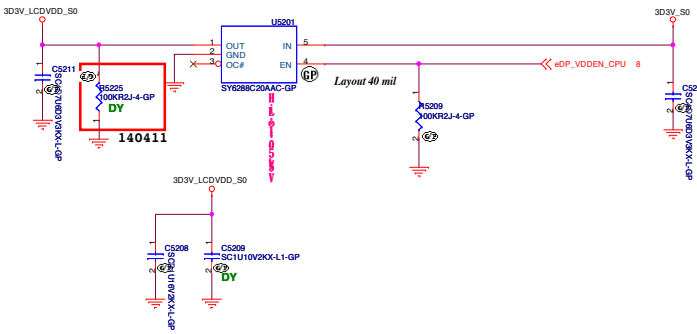
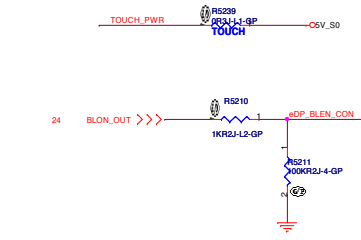
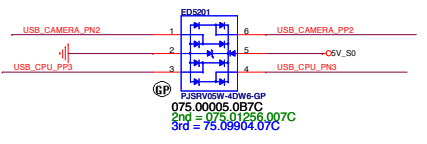
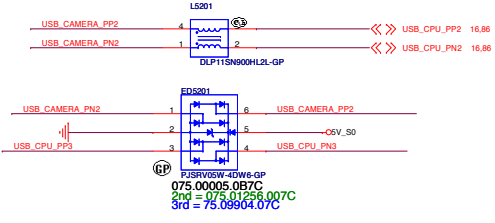
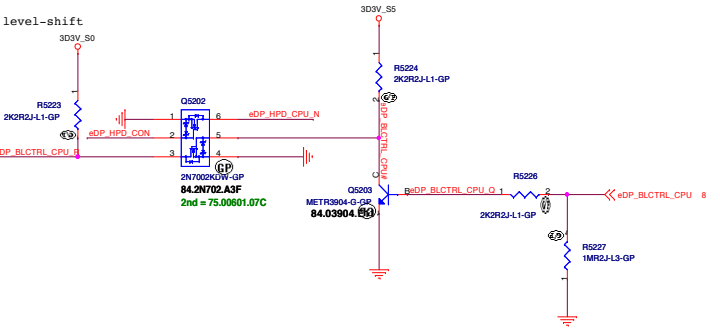
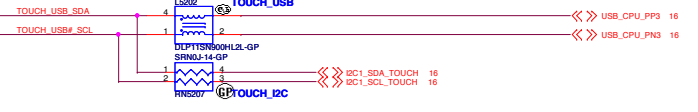
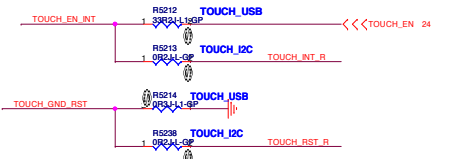
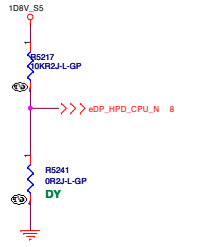
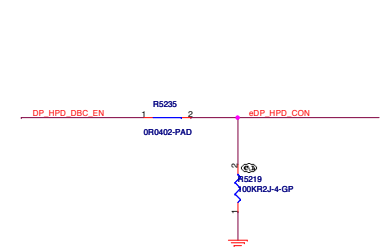
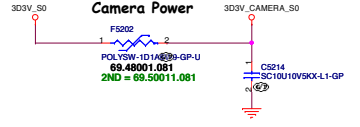
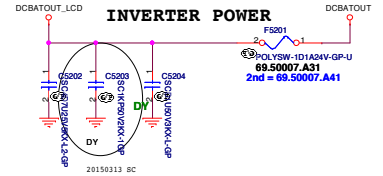
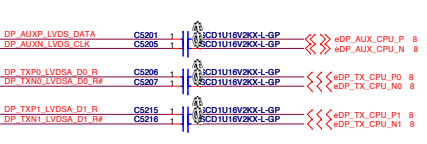
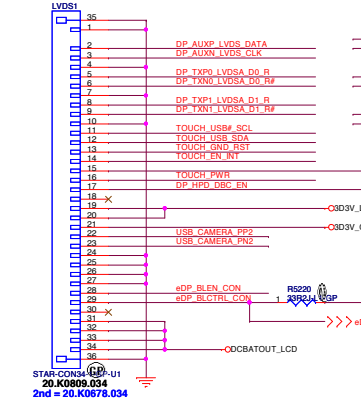
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ULT		緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		1D8V 1D5V 1D24V	
Size A3	Document Number	Domino	
Date: Friday, March 20, 2015	Sheet 51	of 102	Rev -1

SSID = VIDEO

DP_AUX#_LVDS_DATA	DP_AUXN_LVDS_CLK	DP_TXP0_LVDSA_D0_R	DP_TXN0_LVDSA_D0_RF	DP_TXP1_LVDSA_D1_R	DP_TXN1_LVDSA_D1_RF
DP_AUX#_LVDS_DATA	DP_AUXN_LVDS_CLK	DP_TXP0_LVDSA_D0_R	DP_TXN0_LVDSA_D0_RF	DP_TXP1_LVDSA_D1_R	DP_TXN1_LVDSA_D1_RF

Panel Conn.



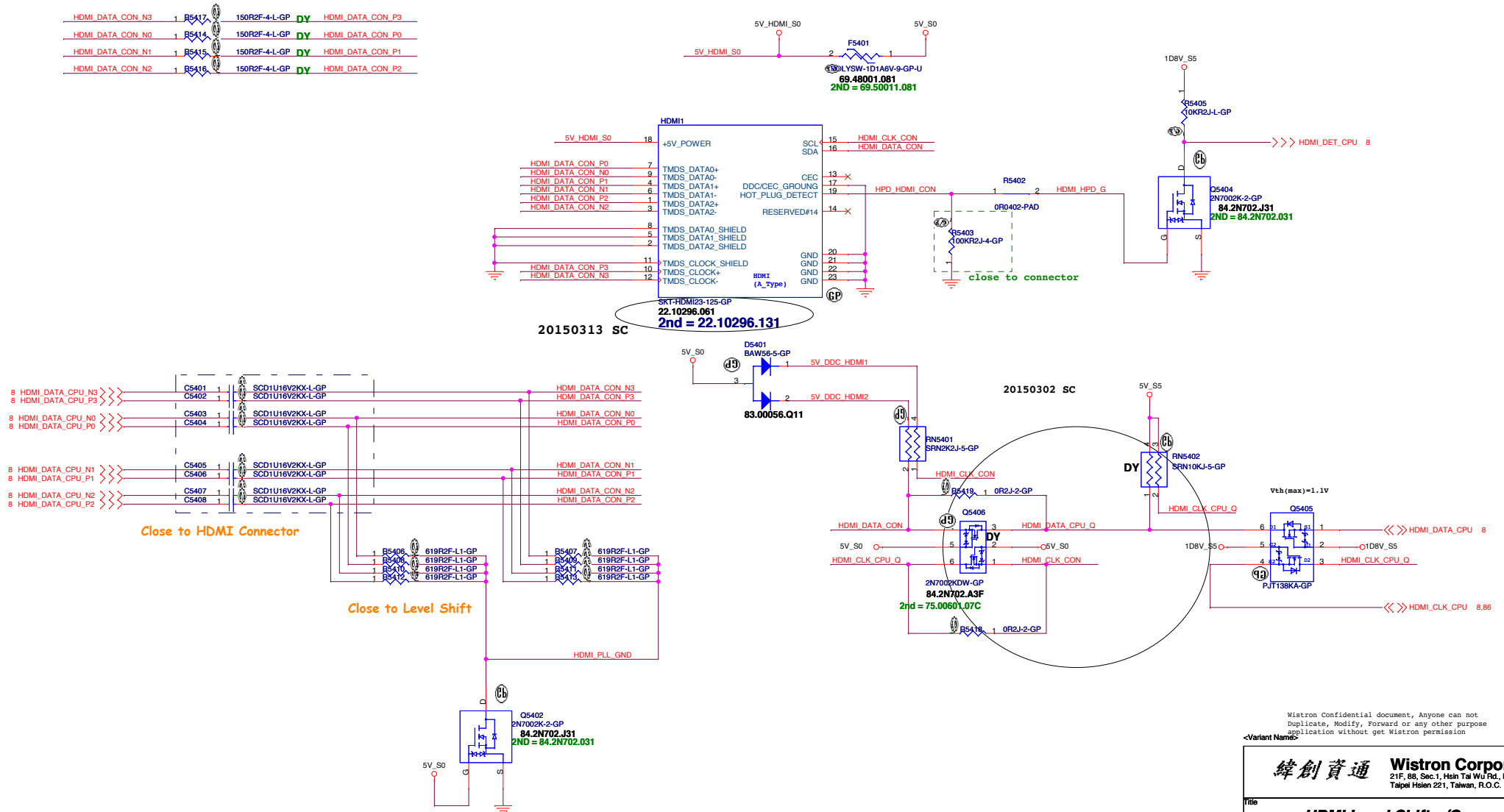
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Title CRT Connector		
Size A3	Document Number Domino	Rev -1
Date: Friday, March 20, 2015	Sheet 53 of 102	1



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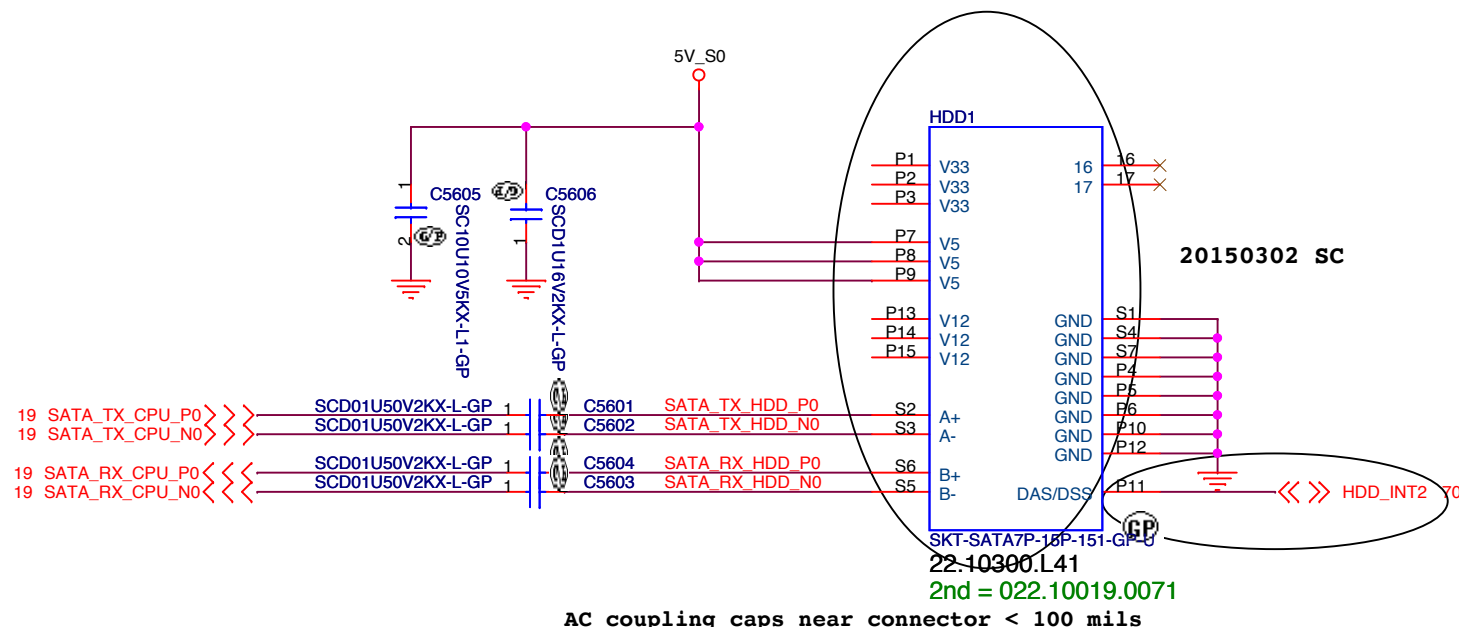
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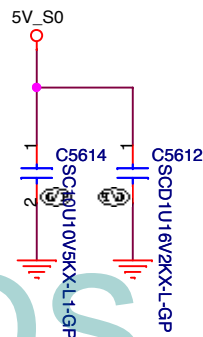
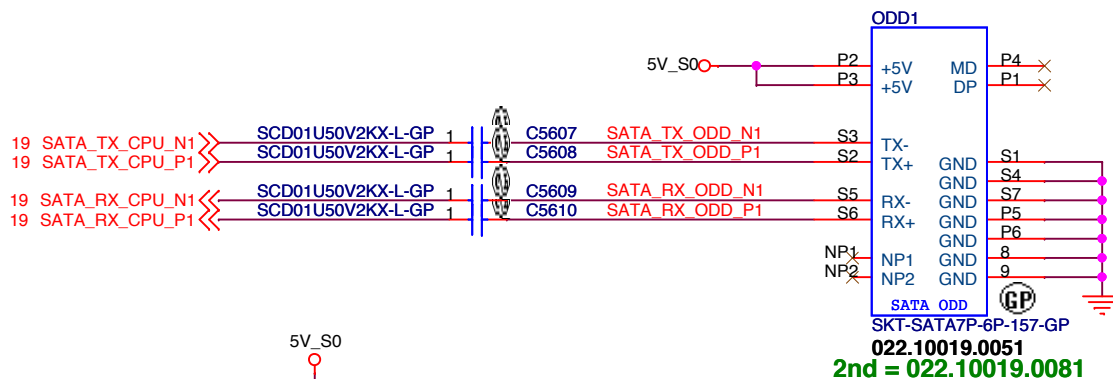
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Taipei Hsien 221, Taiwan, R.O.C.

Title		
Reserved		
Size A3	Document Number Domino	Rev -1
Date: Friday, March 20, 2015	Sheet 55 of	102

SATA HDD Connector



ODD Connector

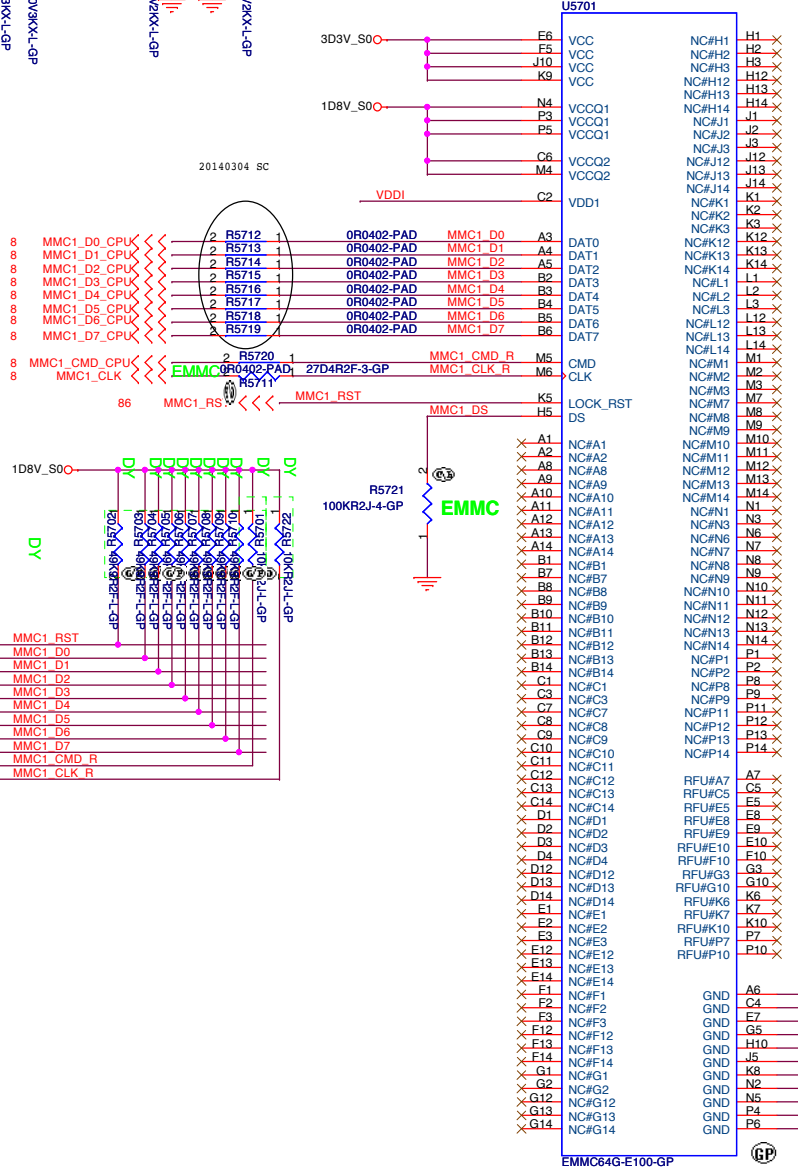
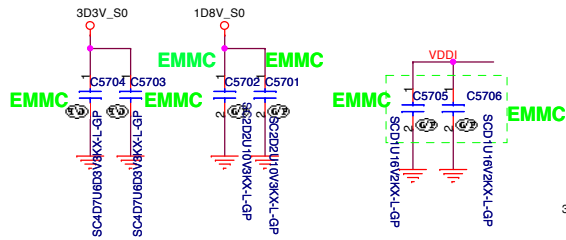


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<Variant Name>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
HDD / ODD / NGFF SSD			
Title	Document Number		Rev
Size A4	Domino		-1
Date:	Friday, March 20, 2015	Sheet 56 of	102

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1st = KN.0320G.008
 2nd = KN.06407.001
 3rd = KN.03207.007
 4th = KN.0640G.005

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<Variant Name>

緯創資通 Wistron Corporation
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 Taipei Hsien 221, Taiwan, R.O.C.

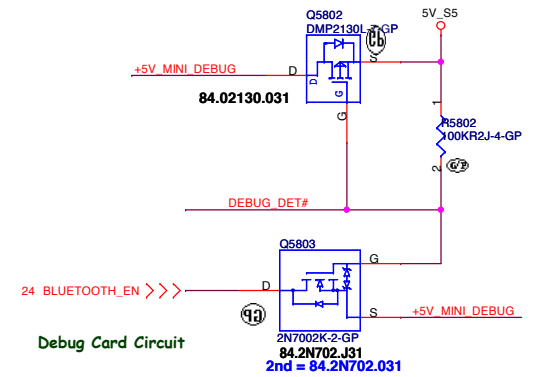
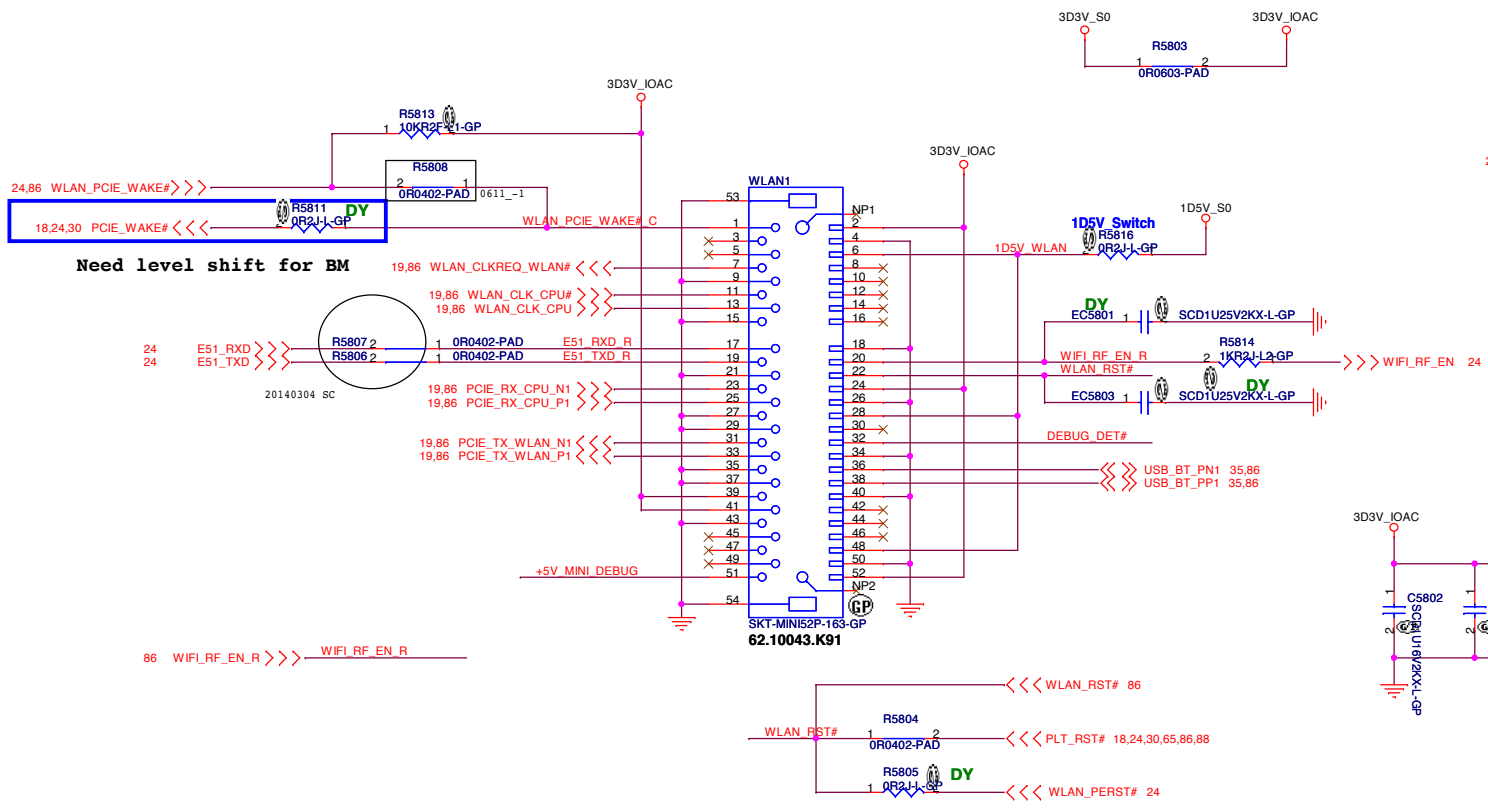
Title: **Reserved**

Size A3 Document Number **Domino** Rev **-1**

Date: Friday, March 20, 2015 Sheet 57 of 102

SSID = Wireless

Mini Card Connector (002.1.1u/v/g/r)



Debug Card Circuit

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Title		
MINICARD(WLAN)		
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SSID = 3G

Mini Card Connector(WWAN)

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<Variant Name>

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Title

WWAN CONN

Size

Document Number

Rev

A4

Domino

-1

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SSID = mSATA

Mini Card Connector(mSATA)

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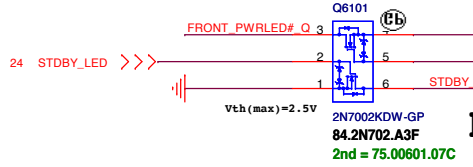
<Variant Name>

緯創資通 **Wistron Corporation**
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Title		
Reserved		
Size	Document Number	Rev
A4	Domino	-1
Date:	Friday, March 20, 2015	Sheet 60 of 102

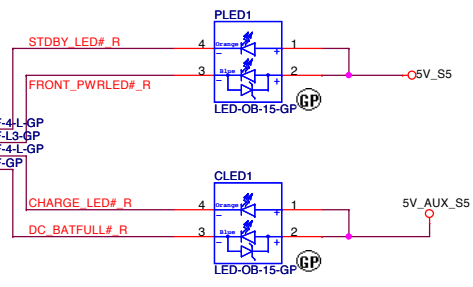
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Power button LED

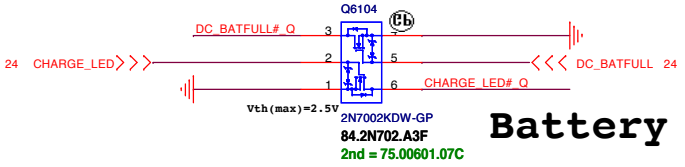


Power STDBY_LED

- STDBY_LED#_Q 1 R6101 150R2F-4-L-GP
- FRONT_PWRLED#_Q 1 R6102 100R2F-1.3-GP
- CHARGE_LED#_Q 1 R6103 150R2F-4-L-GP
- DC_BATFULL#_Q 1 R6104 249R2F-GP



Battery LED2 (DC_BATFULL)



Battery LED1 (CHARGE)

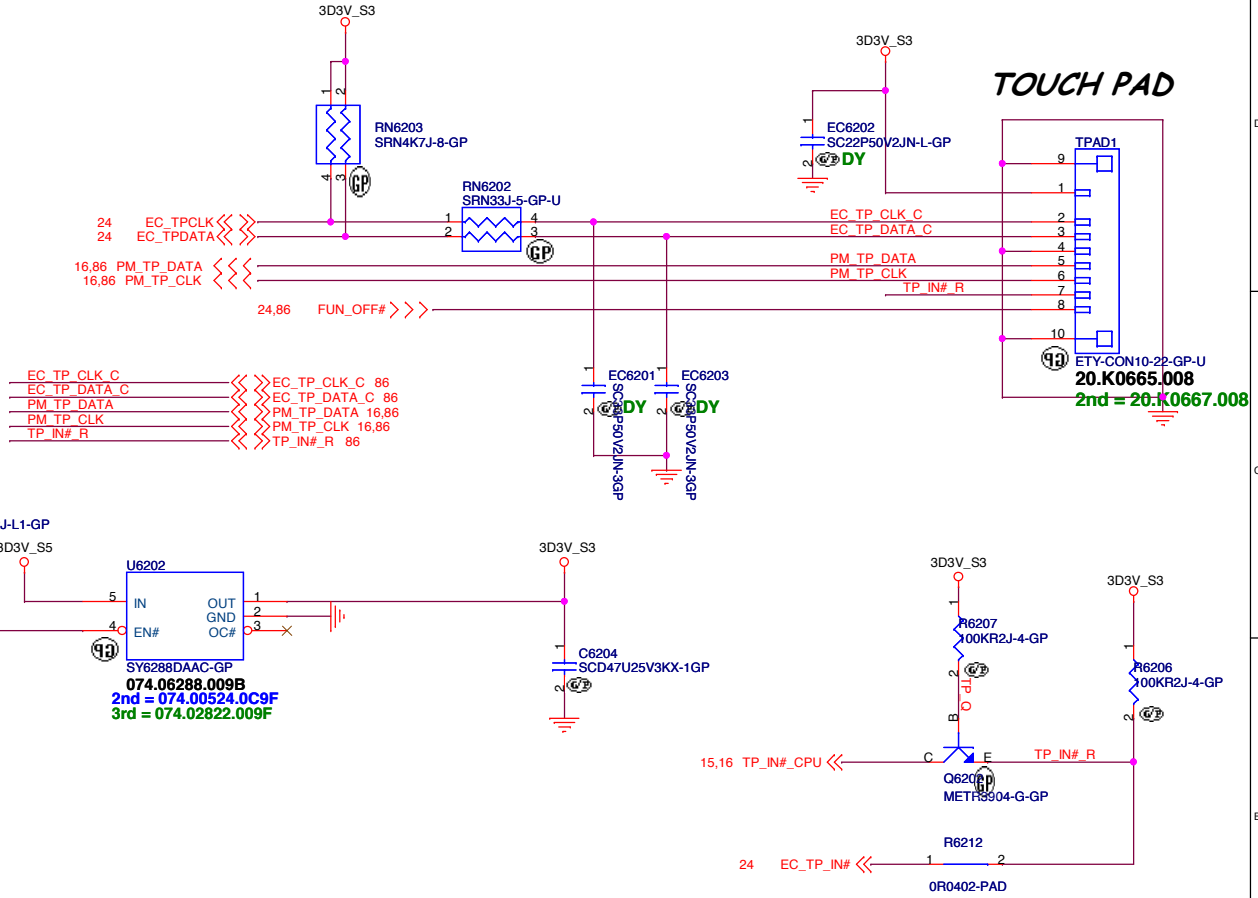
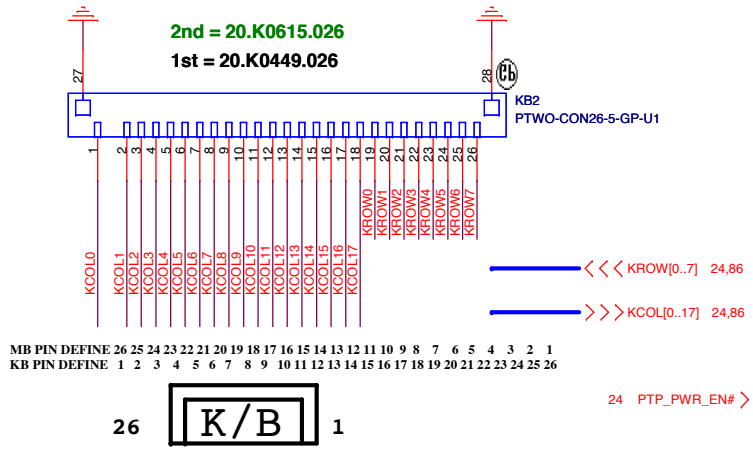
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Title		
LED Bard/Power Button		
Size A3	Document Number	Rev
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SSID = KBC

Internal Keyboard Connector



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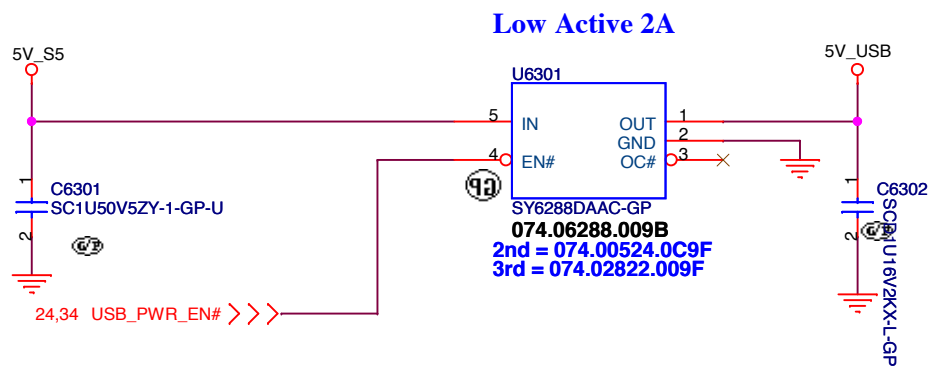
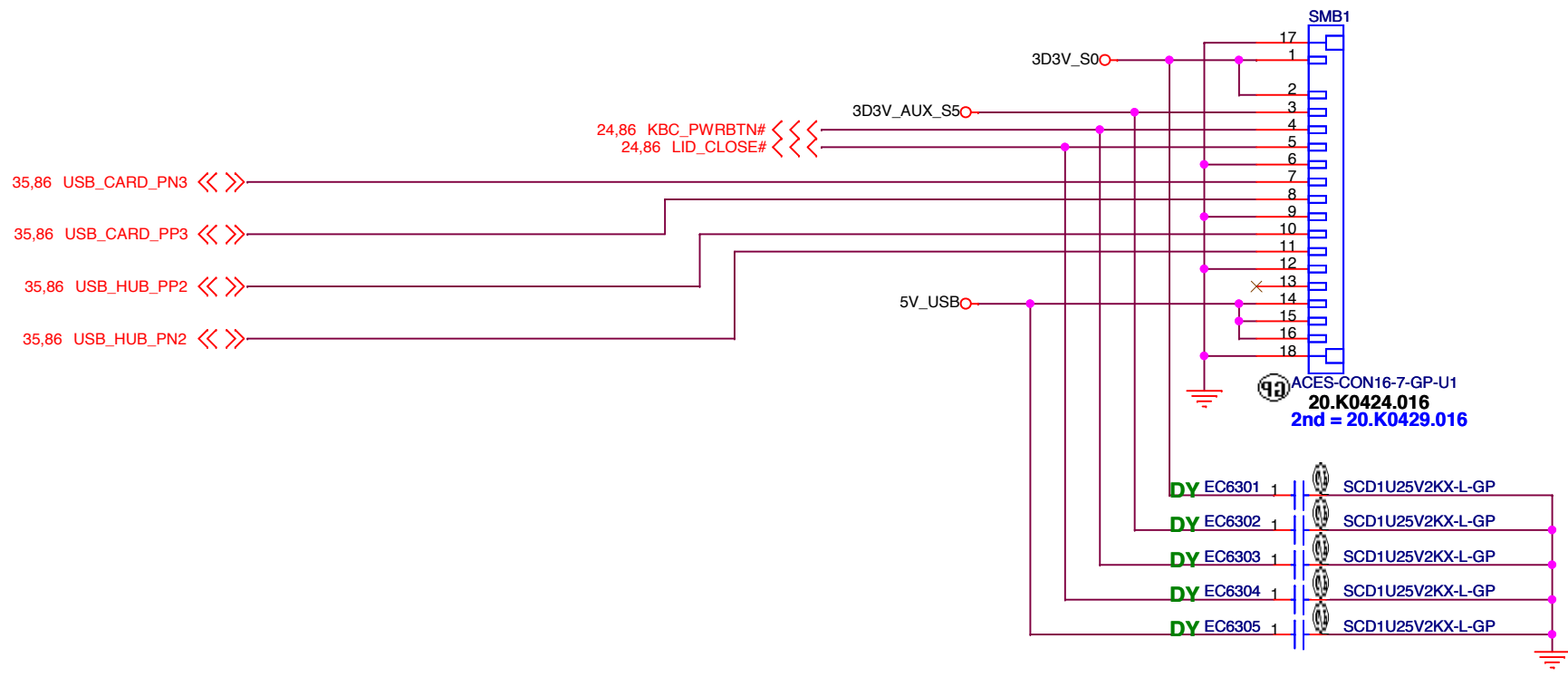
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Title **Key Board/Touch Pad**

Size B	Document Number	Rev
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IO Board Connector		
Title		
Size A4	Document Number	Rev -1
Date: Friday, March 20, 2015	Sheet 63 of 102	

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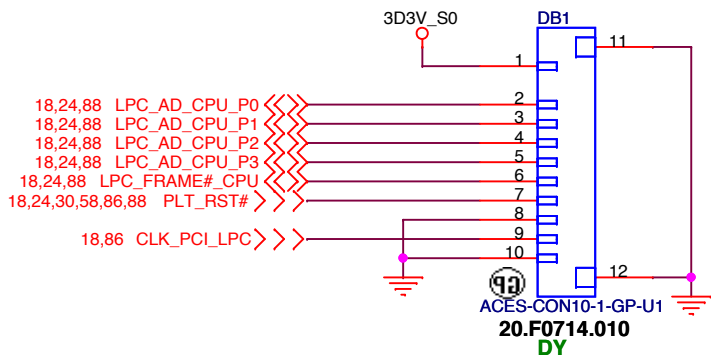
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Title **Hall Sensor**

Size A4	Document Number Domino	Rev -1
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Title **Dubug connector**

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Title **Reserved**

Size A4 Document Number **Domino** Rev **-1**

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Free Fall Sensor

Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

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SDO="H"; address="3Ah"
***SDO="L"; address="38h"**

***CS="H"; mode="I2C"**
CS="L"; mode="SPI"

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Title

G Sensor

Size
A

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Title		
Thunderbolt (1/5)		
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Title

Thunderbolt (2/5)

Size

A4

Document Number

Domino

Rev

-1

Date: Friday, March 20, 2015

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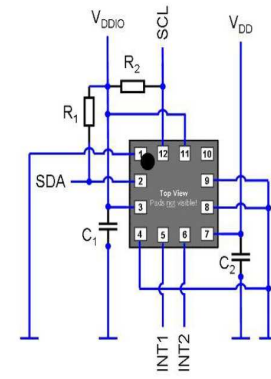
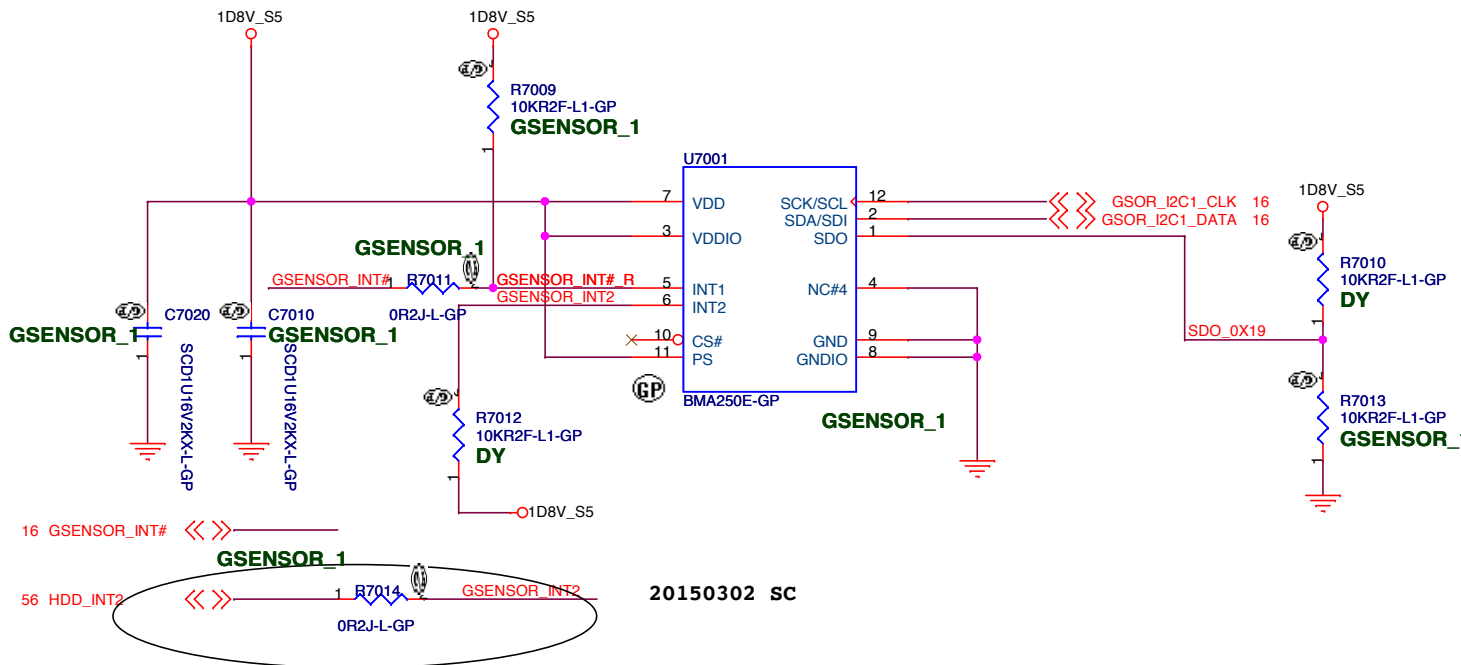
SSID = User.Interface

G Sensor

Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

The default I²C address of the device is 0011000b (0x18). It is used if the SDO pin is pulled to 'GND'. The alternative address 0011001b (0x19) is selected by pulling the SDO pin to 'V_{DDIO}'.



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Title			
GSENSOR			
Size	Document Number	Rev	
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Title		
GPU-VRAM7,8 (4/4)		
Size A3	Document Number Domino	Rev -1
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Title					
RT8812A VGA CORE					
Size		Document Number		Rev	
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Title		DISCRETE VGA POWER	
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Title **Switchable GFX LCD(1/2)**

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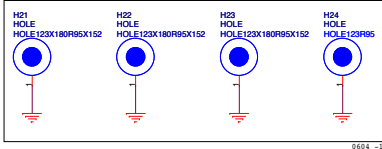
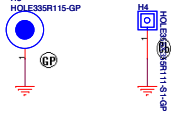
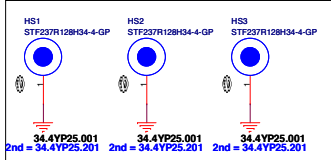
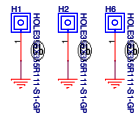
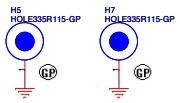
緯創資通 **Wistron Corporation**
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Title **Switchable GFX LCD(2/2)**

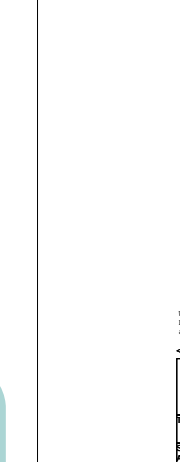
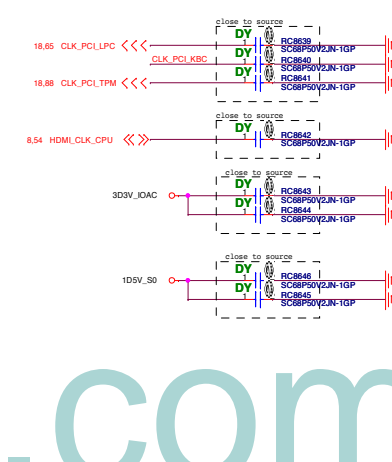
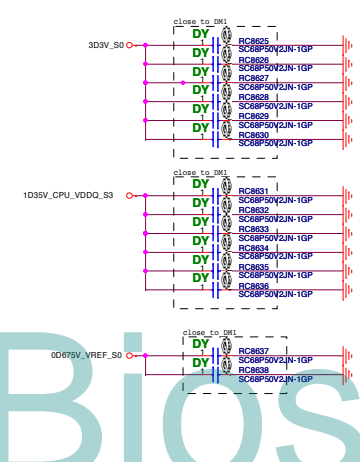
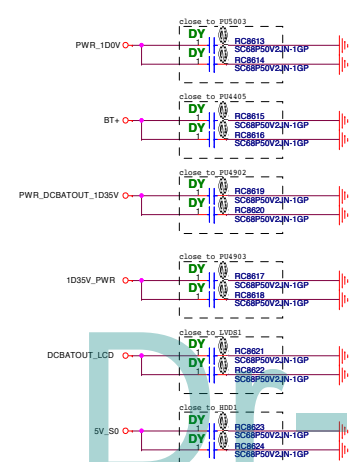
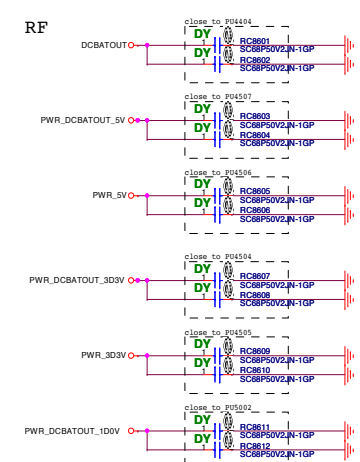
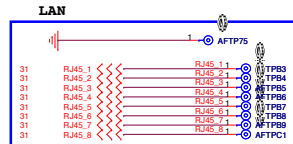
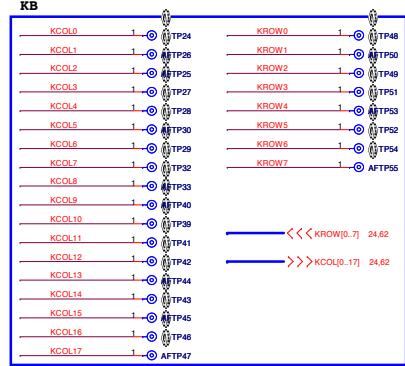
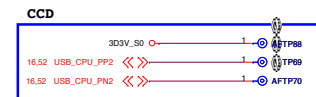
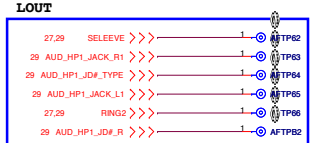
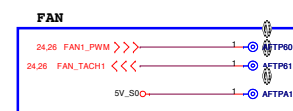
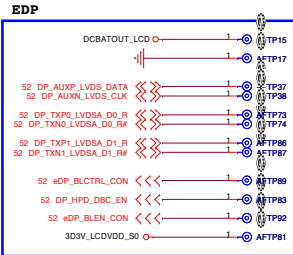
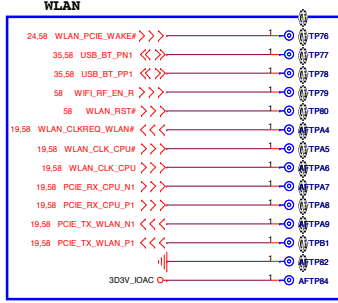
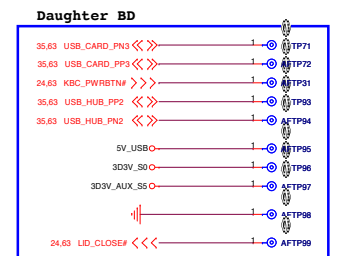
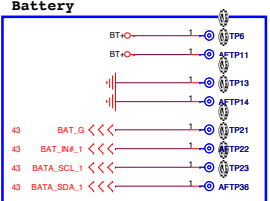
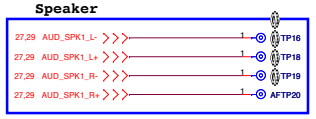
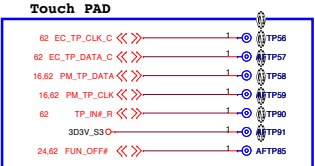
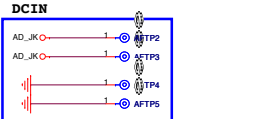
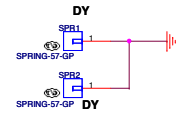
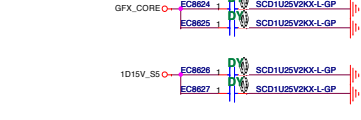
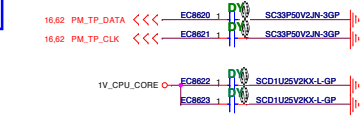
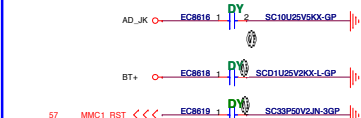
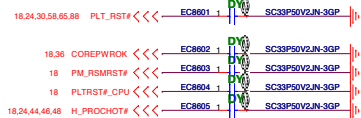
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Chr test point



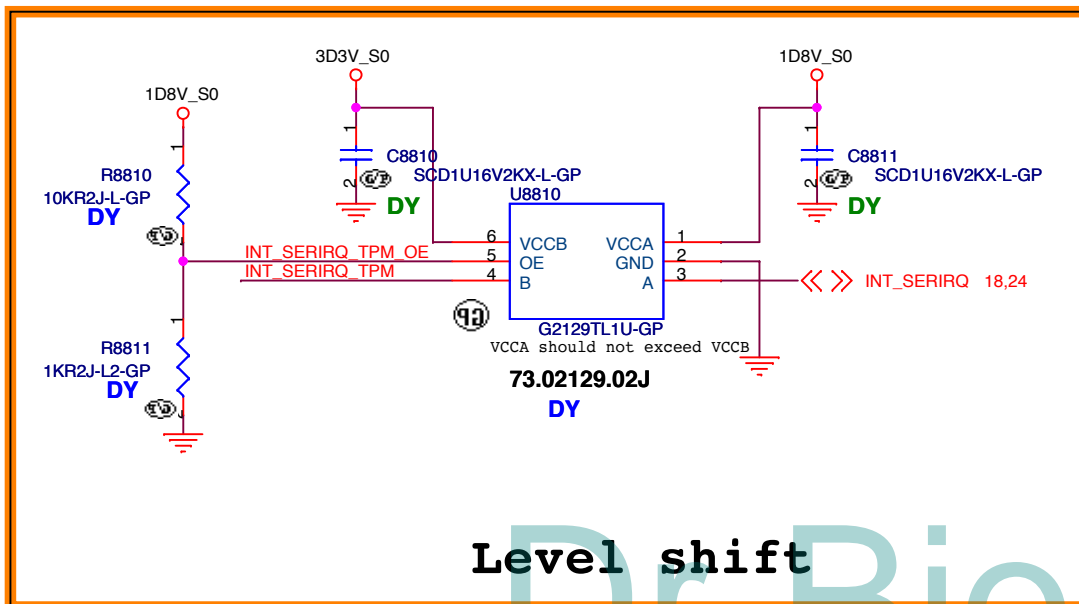
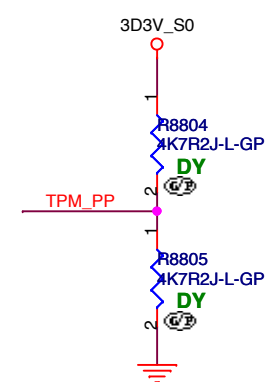
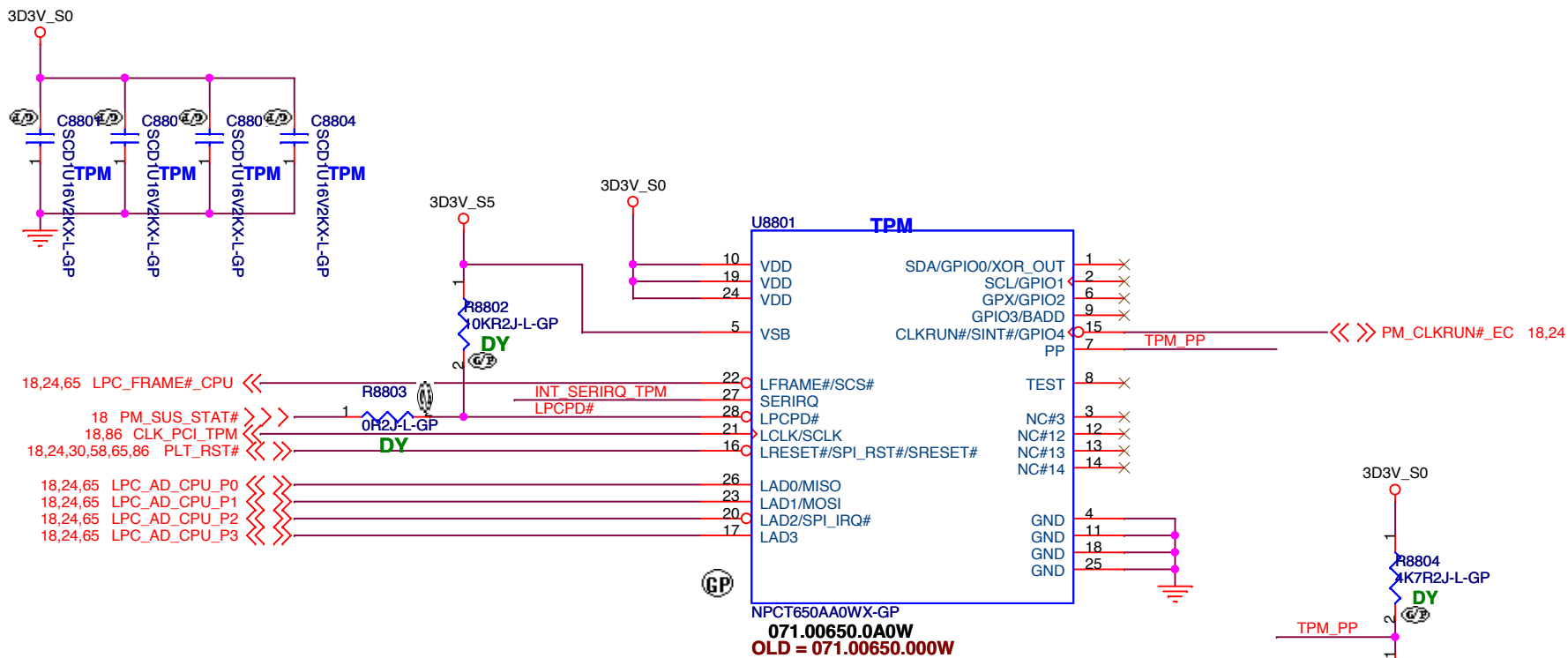
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Level shift

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SSID = Intel LAN

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Title			
LAN Switch			
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Pin	XDP Signal Name	Target Signal	I/O	Device	Pin	XDP Signal Name	Target Signal	I/O	Device
1	OBSFN_A0	Open	I/O		2	OBSFN_A1	Open	I/O	
3	GND	GND	NA		4	OBSDATA_A[0]	Open	I/O	
5	OBSDATA_A[1]	Open	I/O		6	GND	GND	NA	
7	OBSDATA_A[2]	Open	I/O		8	OBSDATA_A[3]	Open	I/O	
9	GND	GND	NA		10	HOOK0 ¹	RSMRST#	I	System
11	HOOK1	BP_PWRGD_RST# ¹	O	System	12	HOOK2	Open	NA	
13	HOOK3	Open	NA		14	HOOK4 ¹	1.05V core	NA	
15	HOOK5	Open	NA		16	VCCOBS_AB	3.3V SUS	I	System
17	HOOK6	RSMRST# ¹	O	System	18	HOOK7	DBR# ¹	O	System
19	GND	GND	NA		20	TDO	JTAG_TDO	I	PCH
21	TRSTn	Open	NA		22	TDI	JTAG_TDI	O	PCH
23	TMS	JTAG_TMS	O	PCH	24	TCK1	Open	NA	
25	GND	GND	NA		26	TCK0	JTAG_TCK	O	PCH

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Title			
PCH XDP			
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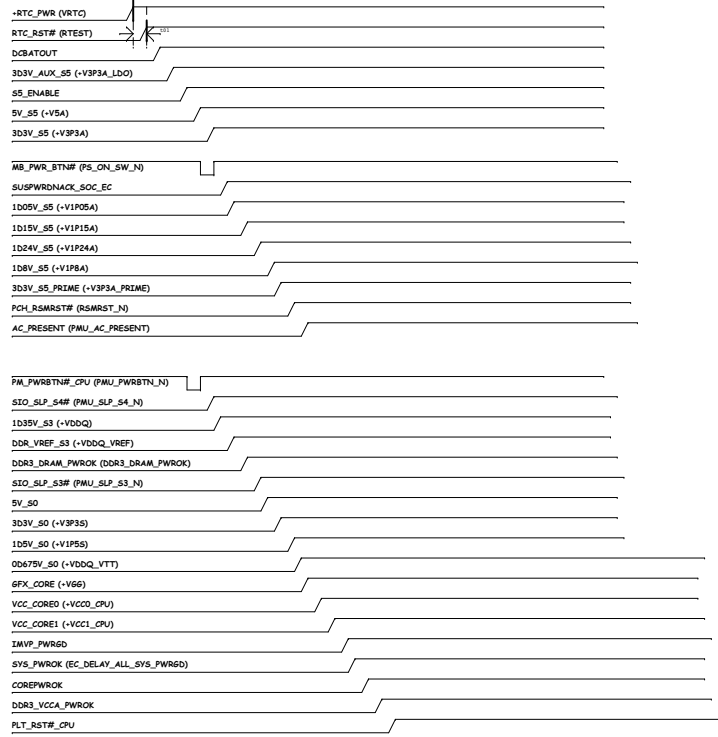
Change History

Size A4	Document Number Domino	Rev -1
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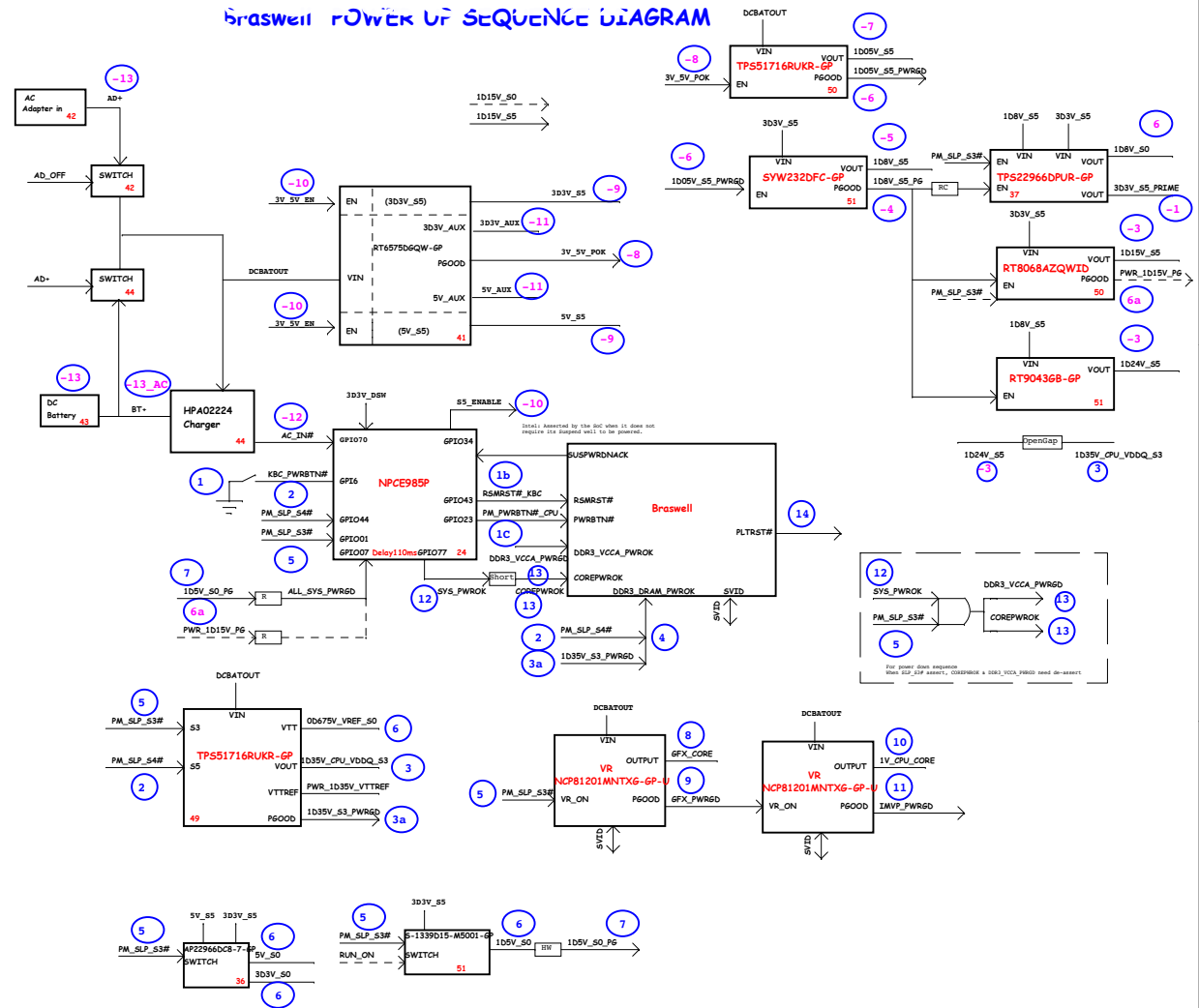
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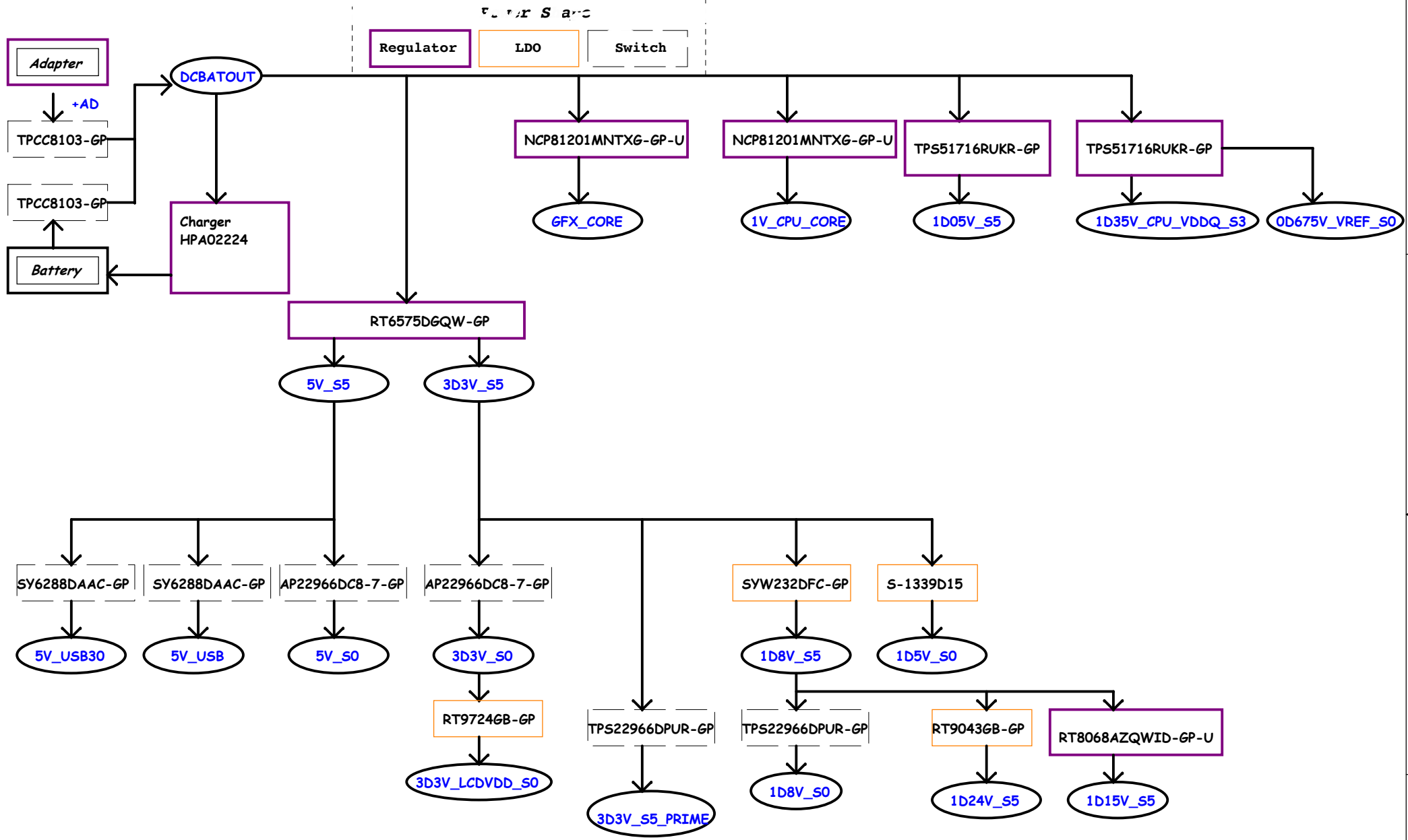
Intel-Power Up Sequence

(AC mode)



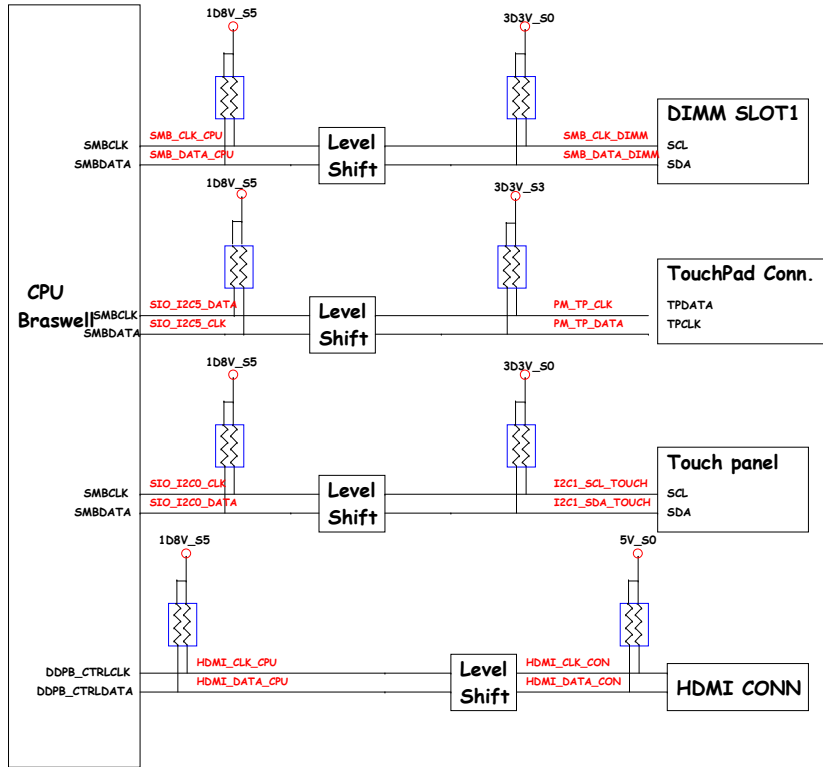
Braswell POWER UP SEQUENCE DIAGRAM



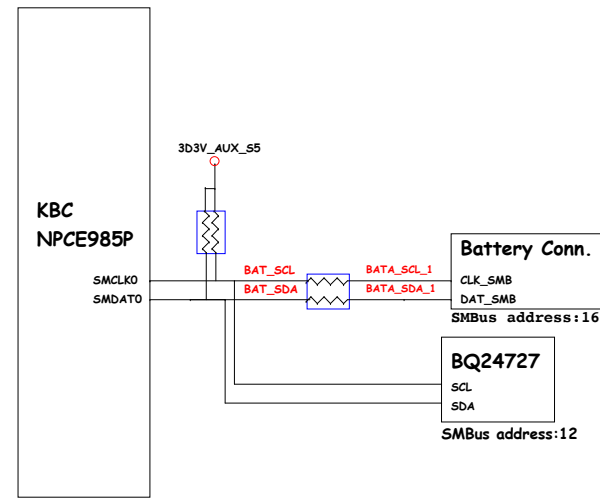


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PCH SMBus Block Diagram



KBC SMBus Block Diagram

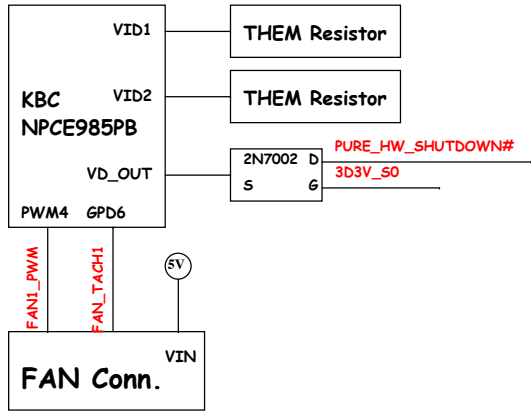


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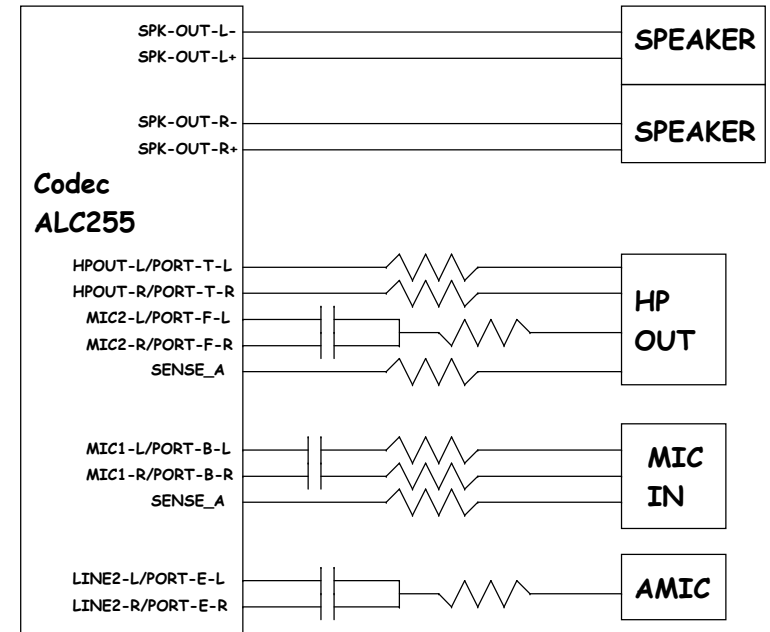
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<p>Title: SMBUS BLOCK DIAGRAM</p>	
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Thermal Block Diagram



Audio Block Diagram



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Title THERMAL/AUDIO BLOCK DIAGRAM			
Size Custom	Document Number Domino	Rev -1	
Date: Friday, March 20, 2015	Sheet 102	of 102	