

LAW_BA

Schematics Document

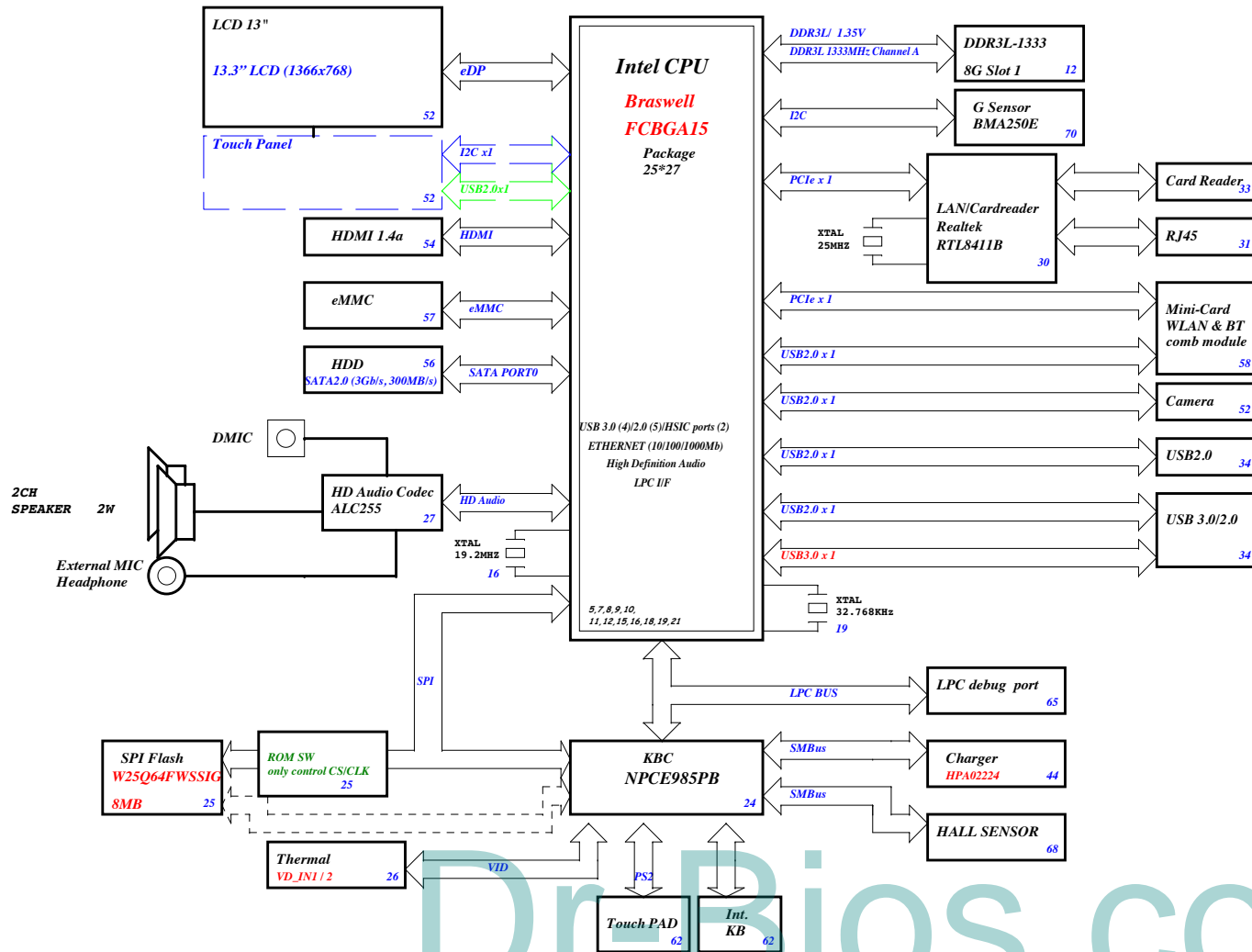
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Cover Page		
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LAW_BA Board Block Diagram

Project code : 4PD05T010001
 PCB P/N : 14295
 Revision : -1



CHARGER	
HPA02224	44
INPUTS	OUTPUTS
DCBATOUT	BT+
SYSTEM DC/DC	
RT6575D	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5
CPU DC/DC	
NCP81201MNTXG 46-47	
INPUTS	OUTPUTS
DCBATOUT	1V_CPU_CORE
CPU DC/DC	
NCP81201MNTXG 48	
INPUTS	OUTPUTS
DCBATOUT	6FX_CORE
SYSTEM DC/DC	
TPS51716	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S5
SYSTEM DC/DC	
TPS51716	
INPUTS	OUTPUTS
DCBATOUT	1D35V_CPU_VDDQ_S3
SYSTEM LDO	
S-1339D15	
INPUTS	OUTPUTS
3D3V_S5	1D5V_S0
SYSTEM LDO	
RT9043GB	
INPUTS	OUTPUTS
1D8V_S5	1D24V_S5
SYSTEM DC/DC	
RT8068AZQWID	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S5

PCB LAYER					
L1:Top	L4:Signal				
L2:VCC	L5:GND				
L3:Signal	L6:Bottom				

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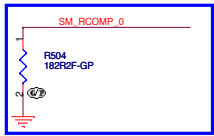
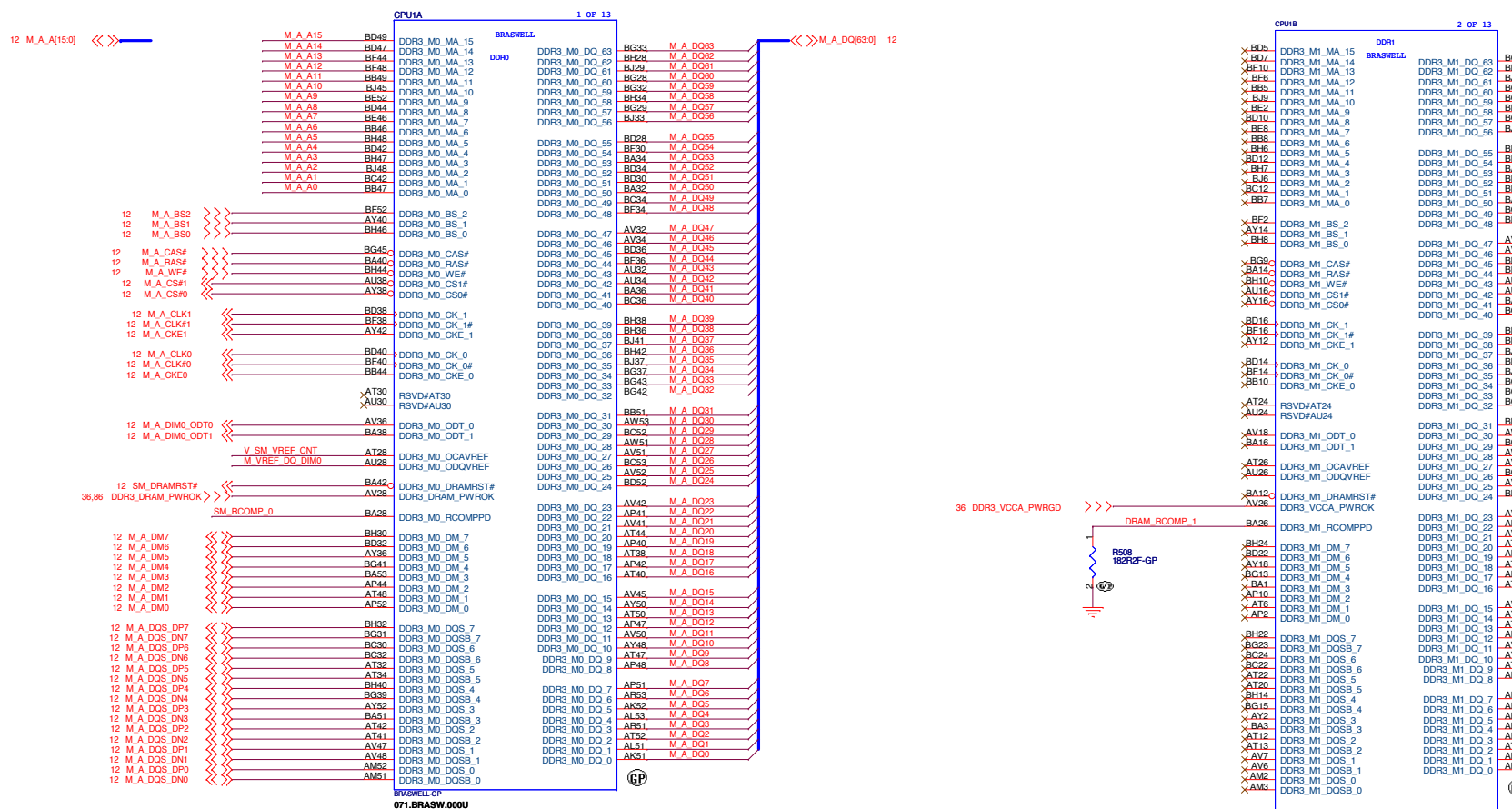
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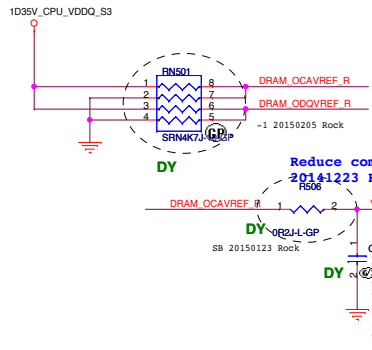
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SSID = CPU

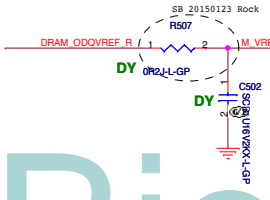


Layout Note: Close CPU

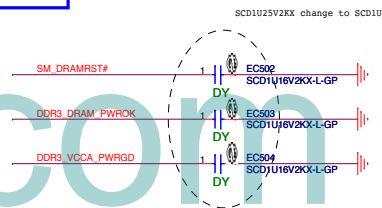


Reduce component connector (Delete RN502)

NOTE: PLACE 0.1U CAP CLOSE TO CPU



NOTE: PLACE 0.1U CAP CLOSE TO CPU



PLACE TWO 4.7K RESISTORS CLOSE TO CPU TO CPU PINS ON M_VREF ROUTE THE VREF POWER SIGNALS WITH THICK TRACES

PLACE TWO 4.7K RESISTORS CLOSE TO CPU TO CPU PINS ON M_VREF ROUTE THE VREF POWER SIGNALS WITH THICK TRACES

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Title: CPU (DDR)
Size: Custom Document Number: LAW BA Rev: -1
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SSID = CPU

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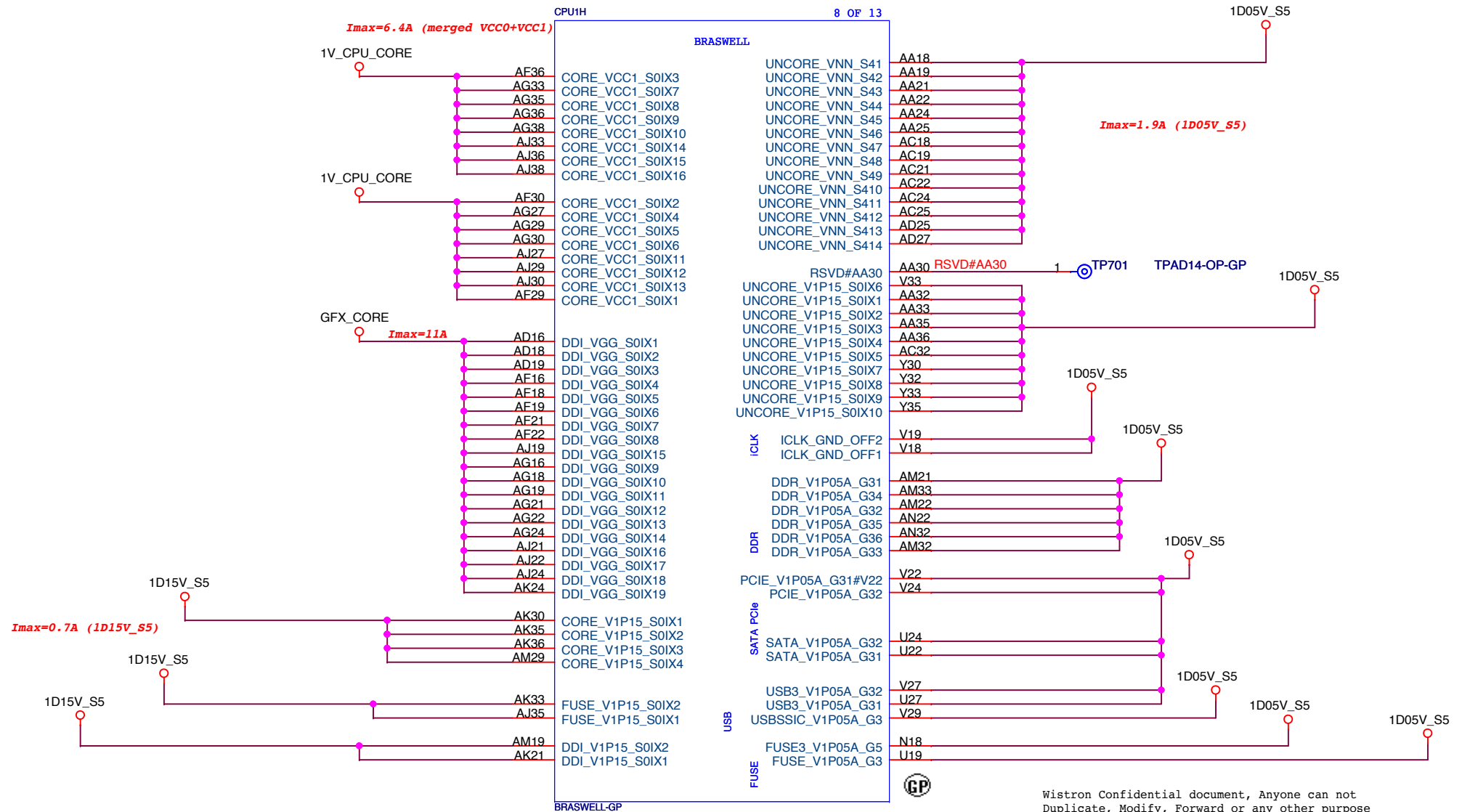
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Title		
CPU (CFG)		
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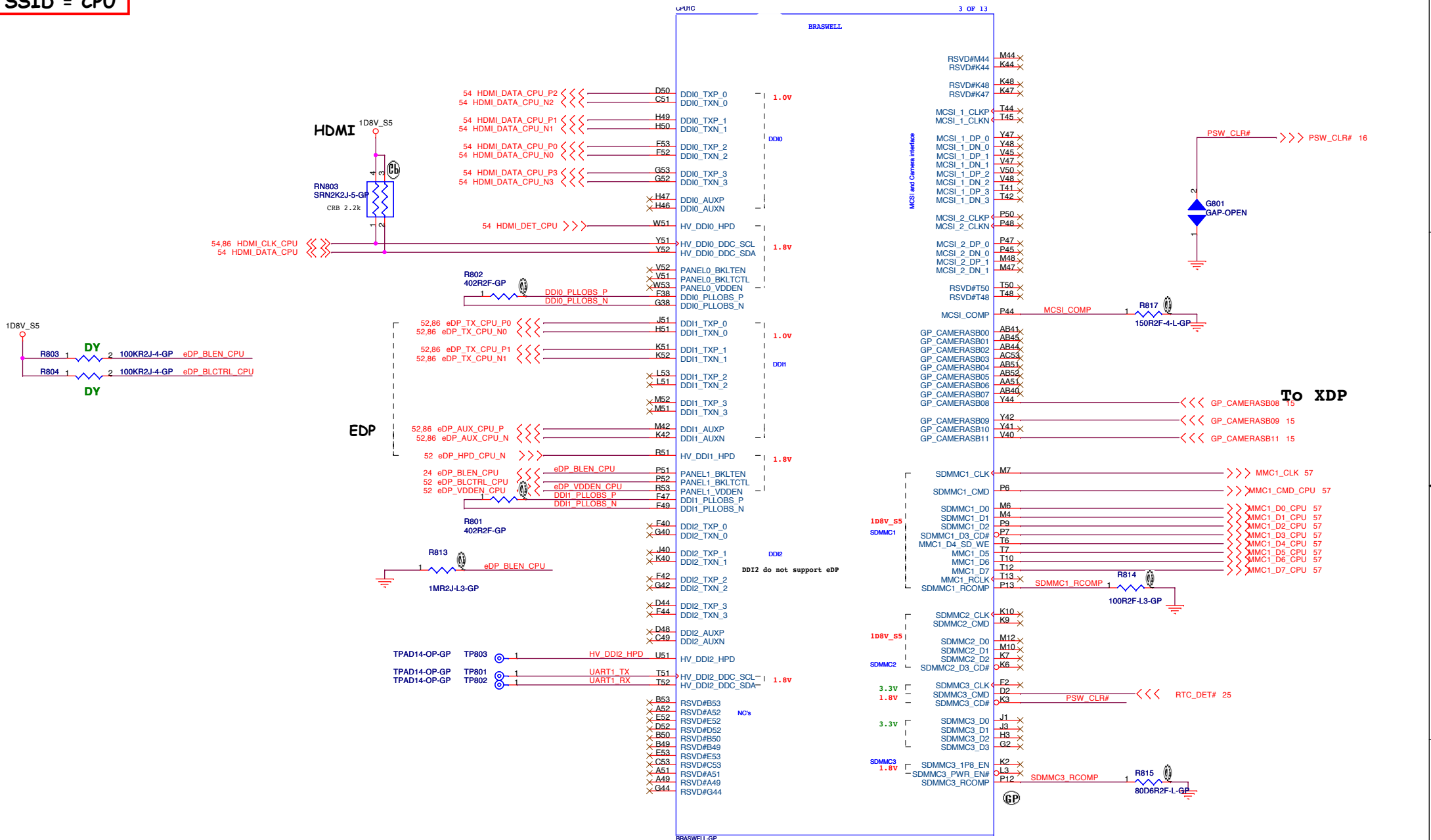


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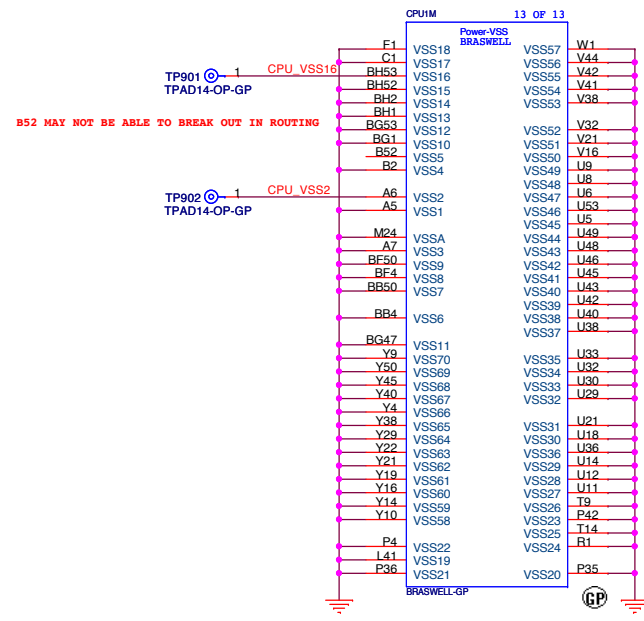
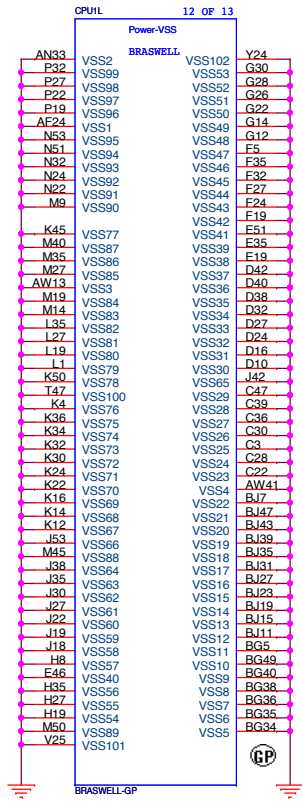
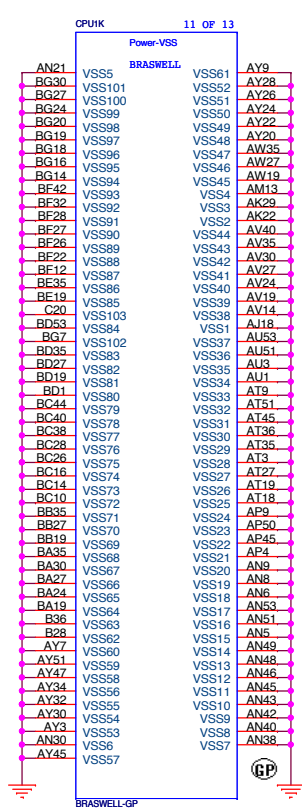
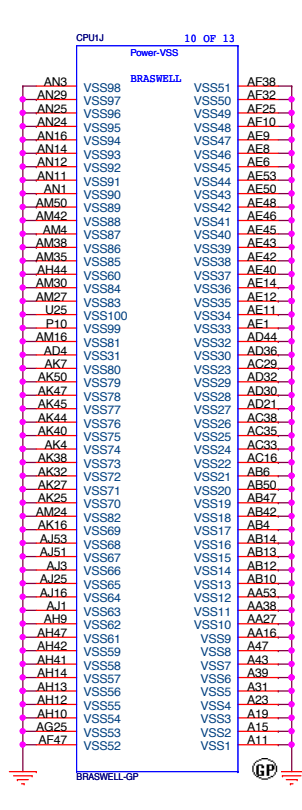
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CPU (VCC CORE)		
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CPU (DDI/EDP/GPIO)	
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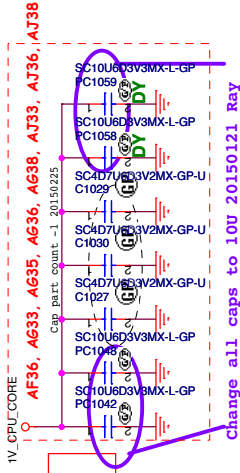
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Title: **CPU (VSS)**

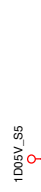
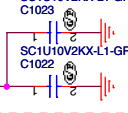
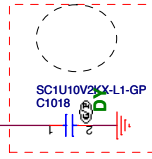
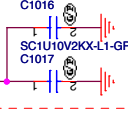
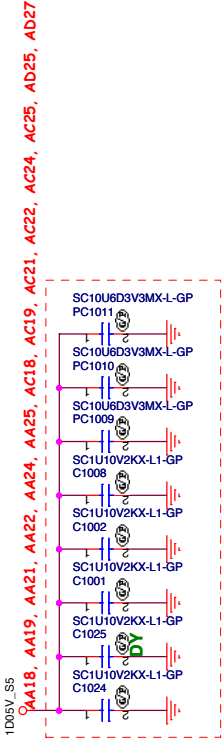
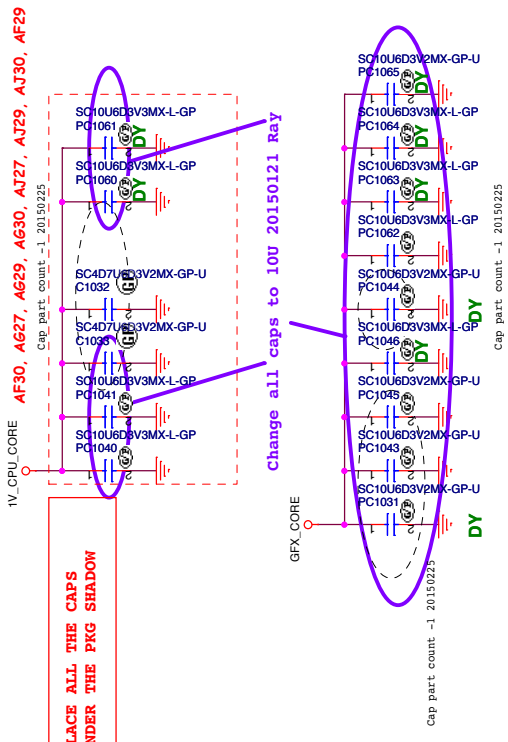
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SSID = CPU

PLACE ALL THE CAPS UNDER THE PKG SHADOW



PLACE ALL THE CAPS UNDER THE PKG SHADOW



PLACE CLOSE TO PIN 1 OF RB

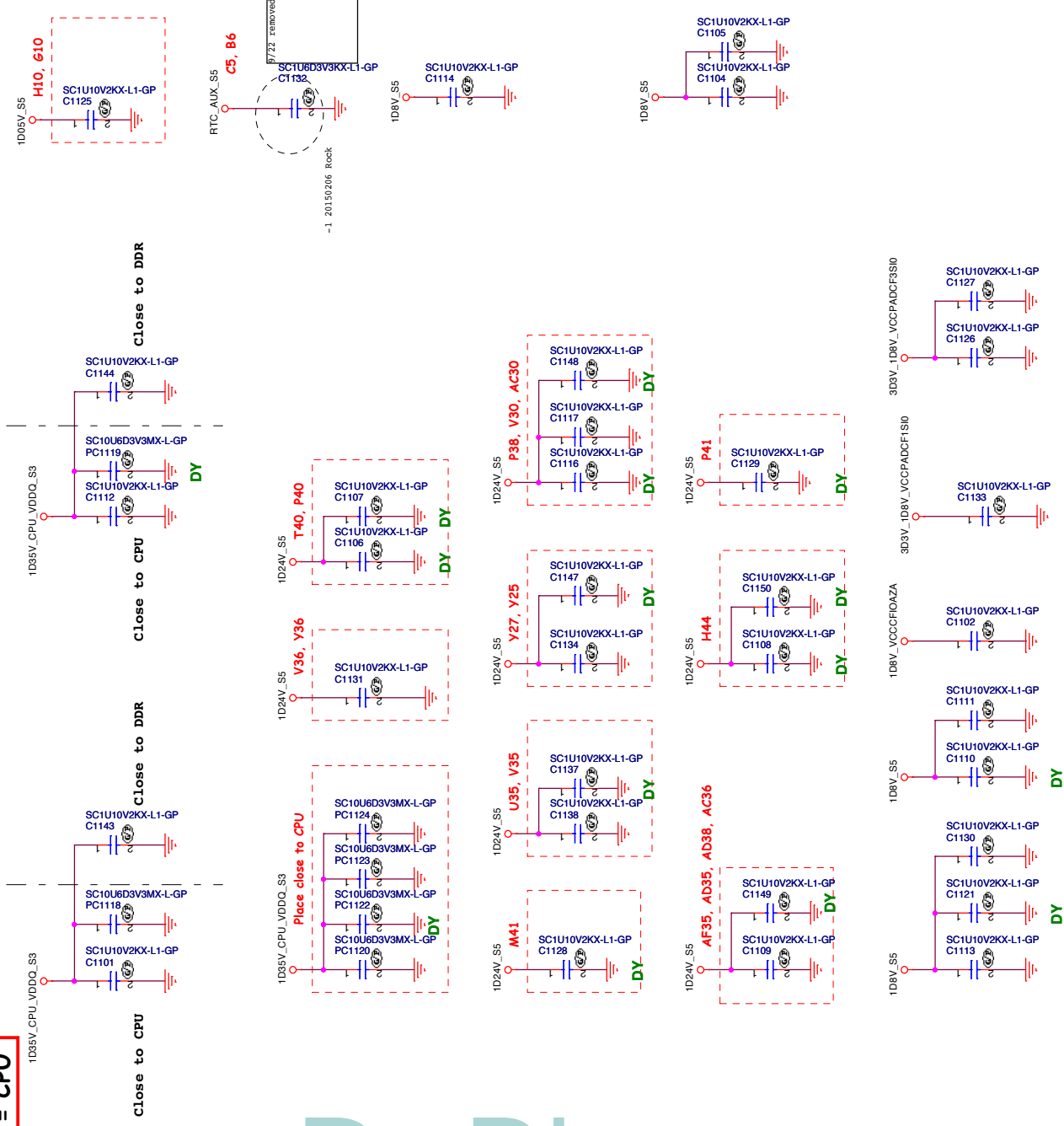
PLACE CLOSE TO PIN 1 OF RA

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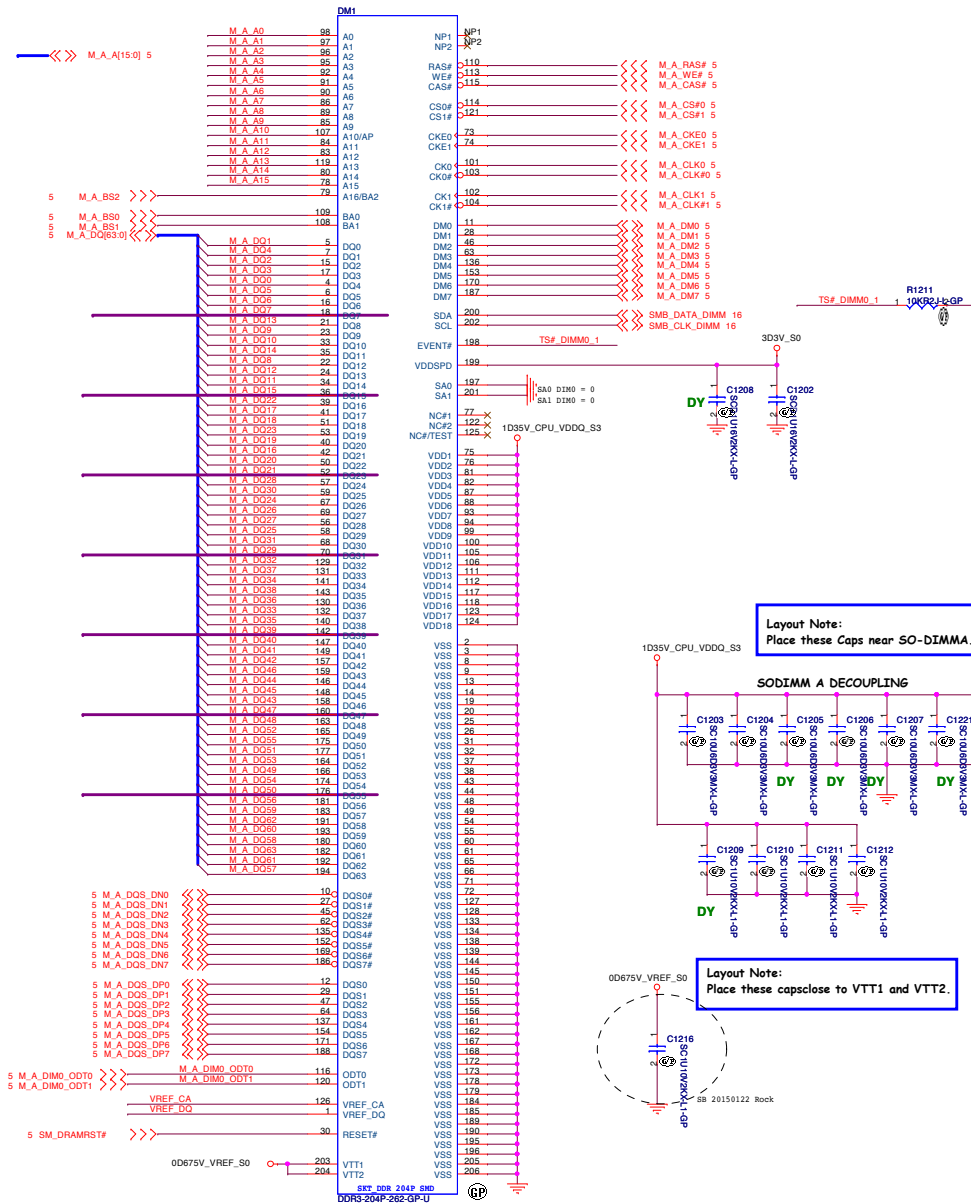
SSID = CPU



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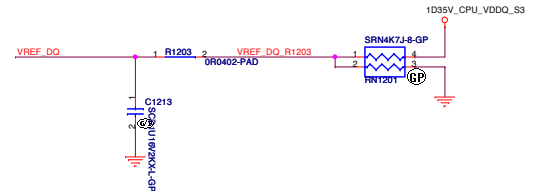
SSID = MEMORY



Note:
 If SA0_DIM0 = 0, SA1_DIM0 = 0
 SO-DIMMA SPD Address is 0xA0
 SO-DIMMA TS Address is 0x30

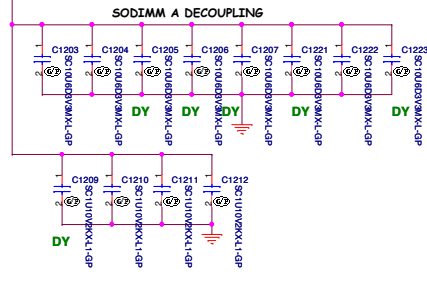
If SA0_DIM0 = 1, SA1_DIM0 = 0
 SO-DIMMA SPD Address is 0xA2
 SO-DIMMA TS Address is 0x32

For Intel Recommend Close to DIMM(Braswell)

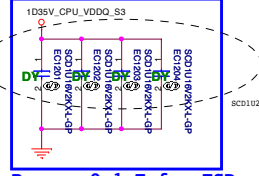
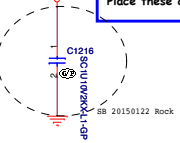


Layout Note:
 Place these Caps near SO-DIMMA.

For Intel Recommend Close to DIMM(Braswell)



Layout Note:
 Place these caps close to VTT1 and VTT2.



Reverse 0.1uF for ESD

SCD1025V2KX change to SCD1016V2KX -1 20150204 Rock

- 1st = 62.10024.S21
- 2nd = 62.10024.Q61
- 3rd = 62.10024.M31
- 4th = 62.10017.B31

Reverse Type

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SSID = MEMORY

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SSID = CPU

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SSID = STRAP

STRAP RESISTORS SHOULD BE PLACED CLOSE TO SOC SHOULD BE PLACED OUTSIDE KOZ AREA

All the straps are enabled on the initialization of the PMC_RSMRST_N signal (c...

Description	DDI0_Detected	DDI1_Detected	A16 Swap Override	DSI Display Detected	Boot BIOS Strap BBS	Flash Descriptor Security Override	DFX Boot Halt Strap & VISA Early POSM Debug Enable	DFX Sus Debug Strap	ICLK, USB2, DDI SFR Supply Select	ICLK SFR Bypass	POSM Select	ICLK Xtal OSC Bypass	CCU SUS RO Bypass	RTC OSC bypass
GPIO	GPIO_SUS0	GPIO_SUS1	GPIO_SUS2	GPIO_SUS3	GPIO_SUS4	GPIO_SUS5	GPIO_SUS6	GPIO_SUS7	SEC_GPIO_SUS8	SEC_GPIO_SUS9	SEC_GPIO_SUS10	GP_CAMERASB08	GP_CAMERASB09	GP_CAMERASB11
Schematic														
High	DDI0 Detect	DDI1 Detect	Normal Operation	DSI Detect	Boot from SPI	Weak internal pull-up Normal Operation	Normal	Weak internal pull-up Normal	1.35V	Weak internal pull-up Bypass with 1.05V	PMC	Bypass	Bypass	Bypass
Low	Disable	Disable	Change Boot Loader address (A16 Override)	Disable	Boot from LPC	Override	Halt boot enable	Sus Debug enable	1.25V	No bypass	Fuse controller	No bypass	No bypass	No bypass

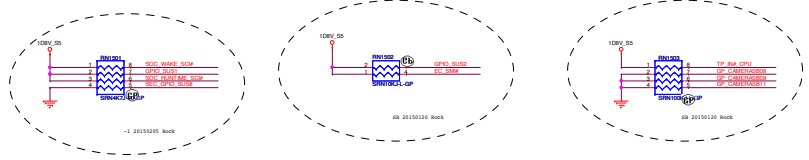


Table 29. Straps (Sheet 1 of 2)

Signal Name	Purpose	Pull-Up/Pull-Down	Strap Description
GPIO_SUS[0]	DDI0 Detect	Weak internal pull-down	DDI0 Detect 0 = DDI0 not detected 1 = DDI0 detected
GPIO_SUS[1]	DDI1 Detect	Weak internal pull-down	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected
GPIO_SUS[2]	A16 swap override	Weak internal pull-up	Top Swap (A16 Override) 0 = Change Boot Loader address 1 = Normal Operation
GPIO_SUS[4]	Boot BIOS Strap BBS	Weak internal pull-up	BIOS Boot Selection 0 = - 1 = SPI
GPIO_SUS[5]	Flash Descriptor Security Override	Weak internal pull-up	Security Flash Descriptors 0 = Override 1 = Normal Operation

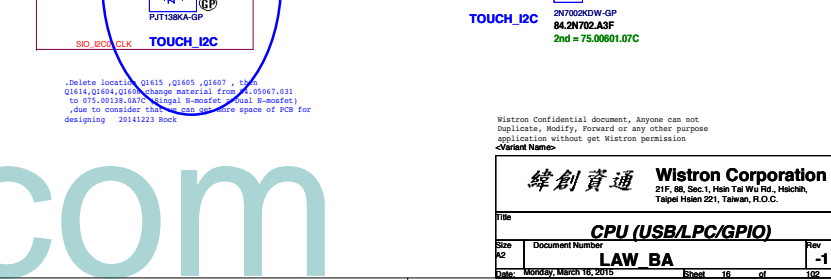
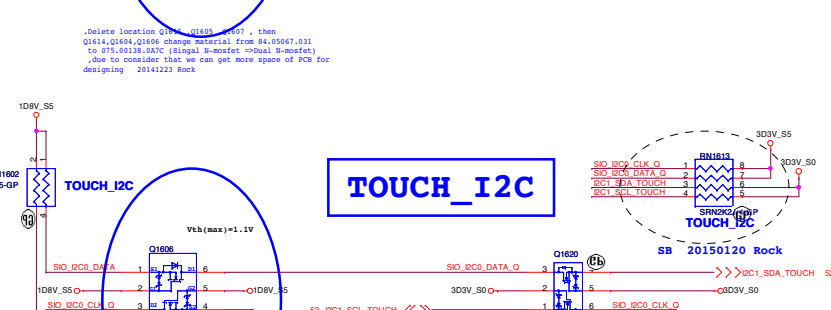
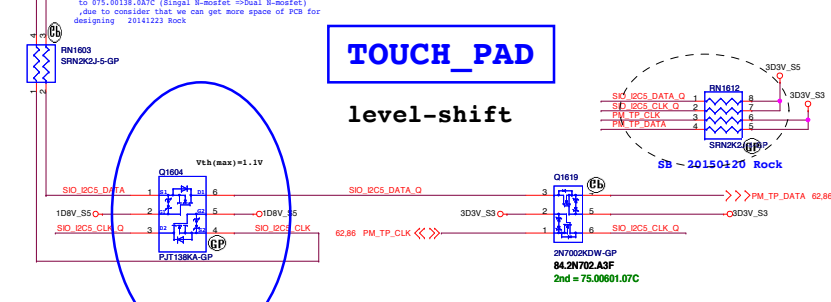
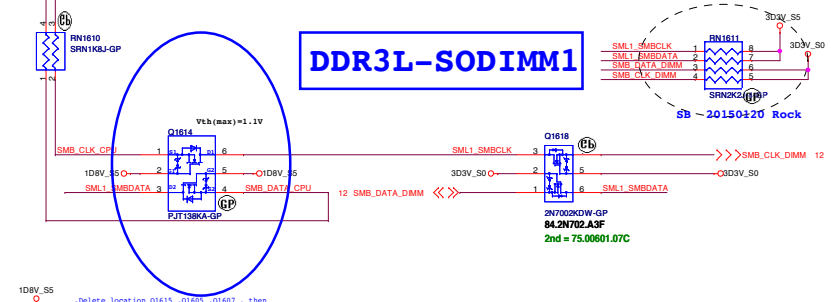
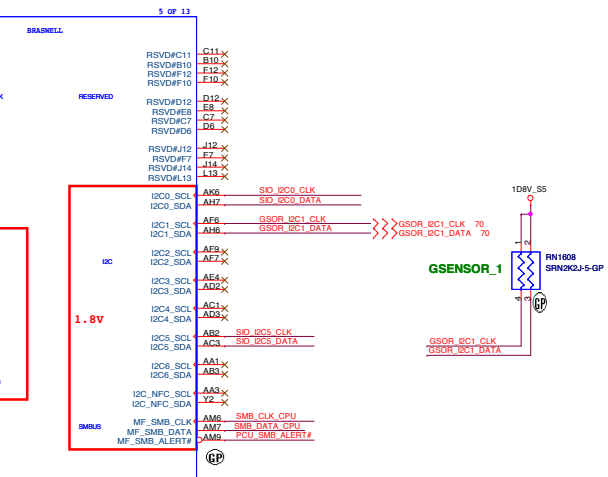
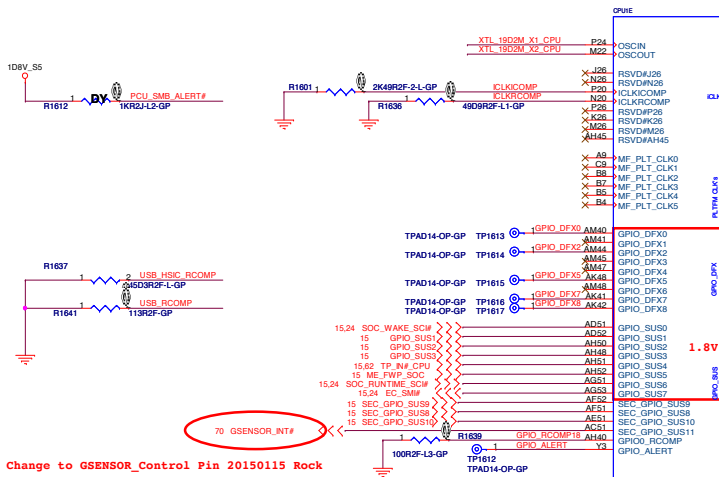
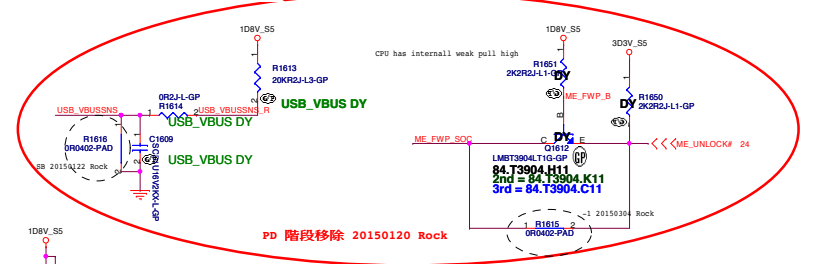
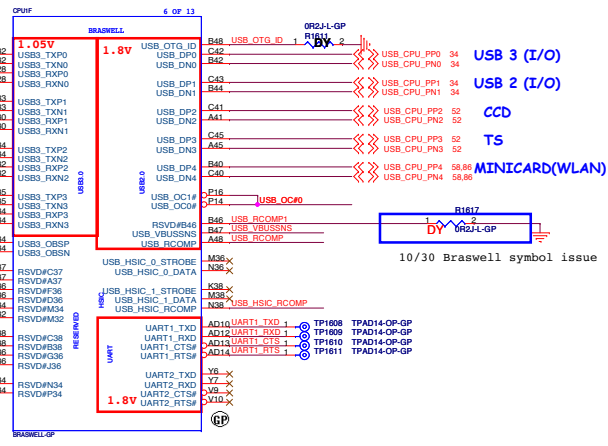
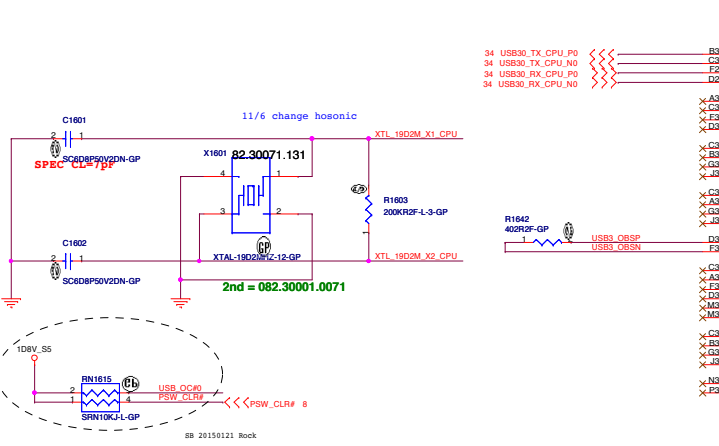
Table 29. Straps (Sheet 2 of 2)

Signal Name	Purpose	Pull-Up/Pull-Down	Strap Description
GPIO_SUS[8]	ICLK, USB2, DDI SFR Supply Select	Weak internal pull-down	0 = Supply is 1.25V 1 = Supply is 1.35V This strap also contains PLL LDO 0: supply is 1.25V; 1: supply is 1.35V. Selects supply voltage for LDOs used for PLLs, thermal oscillators, USB2, ICLK and DDI
GPIO_SUS[9]	ICLK, USB2, DDI SFR Bypass	Weak internal pull-up	0 = No bypass 1 = Bypass with 1.05V
GPIO_SUS[10]	POSM Select	Weak internal pull-down	Selects which POSM will be observed at time 0 0 = Fuse controller 1 = PMC
GPIO_CAMERASB08	ICLK Xtal OSC Bypass	Weak internal pull-down	0 = No Bypass 1 = Bypass
GPIO_CAMERASB09	CCU SUS RO Bypass	Weak internal pull-down	0 = No Bypass 1 = Bypass
GPIO_CAMERASB11	RTC OSC Bypass	Weak internal pull-down	0 = No Bypass 1 = Bypass

CHV Straps [CRB] -- strap detect @ RSMRST# assertion				
Purpose	CHV Pin Name (refer CHV symbol PIN)	PU/PD (internal - Weak)	Options	Default State on board?
DDI0 Detected	GPIO_SUS0	PD	0 - DDI0 Detect, 1 - Disable	High
DDI1 Detected	GPIO_SUS1	PD	0 - DDI1 Detect, 1 - Disable	High
A16 swap override	GPIO_SUS2	PU	0 - Default, 1 - A16 override	High
DSI Display Detected	GPIO_SUS3	PD	0 - DSI detect, 1 - Disable	Low
Boot BIOS Strap BBS	GPIO_SUS4	PU	0 - Boot from SPI, 1 - Boot from LPC	High
Flash Descriptor Security Override	GPIO_SUS5	PU	0 - Security enabled, 1 - Security disabled	High
DFX Boot Halt Strap & VISA Early POSM Debug Enable	GPIO_SUS6	PU	0 - normal, 1 - Halt boot enable	High
DFX Sus Debug Strap	GPIO_SUS7	PU	0 - Sus Debug enable, 1 - Normal	High
ICLK, USB2, DDI SFR Supply Select	SEC_GPIO_SUS8	PU	0 - 1.35V, 1 - 1.25V	Low
ICLK SFR Bypass	SEC_GPIO_SUS9	PD	0 - Bypass with 1.05V, 1 - No Bypass	Low
POSM Select	SEC_GPIO_SUS10	PD	0 - PMC, 1 - Fuse controller	Don't care, if GPIO_SUS6 is pulled high.
ICLK Xtal OSC Bypass	GP_CAMERASB08	PD	0 - Bypass, 1 - No bypass	Low
CCU SUS RO Bypass	GP_CAMERASB09	PD	0 - Bypass, 1 - No bypass	Low
RTC OSC Bypass	GP_CAMERASB11	PD	0 - Bypass, 1 - No bypass	Low



Pair	Device
0	USB3.0 Port 0(USB2.0)
1	USB 2.0 (debug port)
2	Camera
3	TS
4	WiFi + BT



SSID = CPU

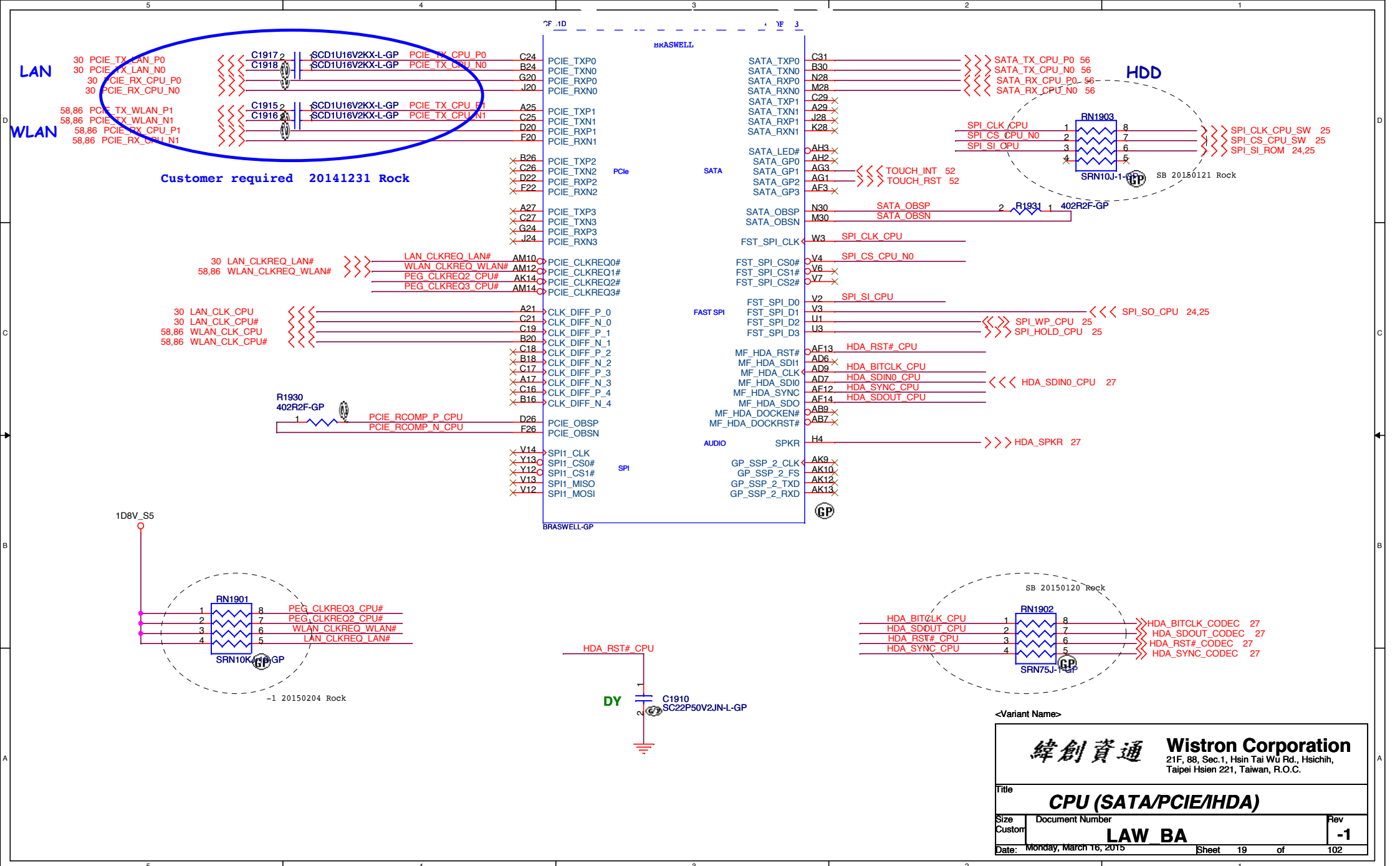
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SSID = PCH

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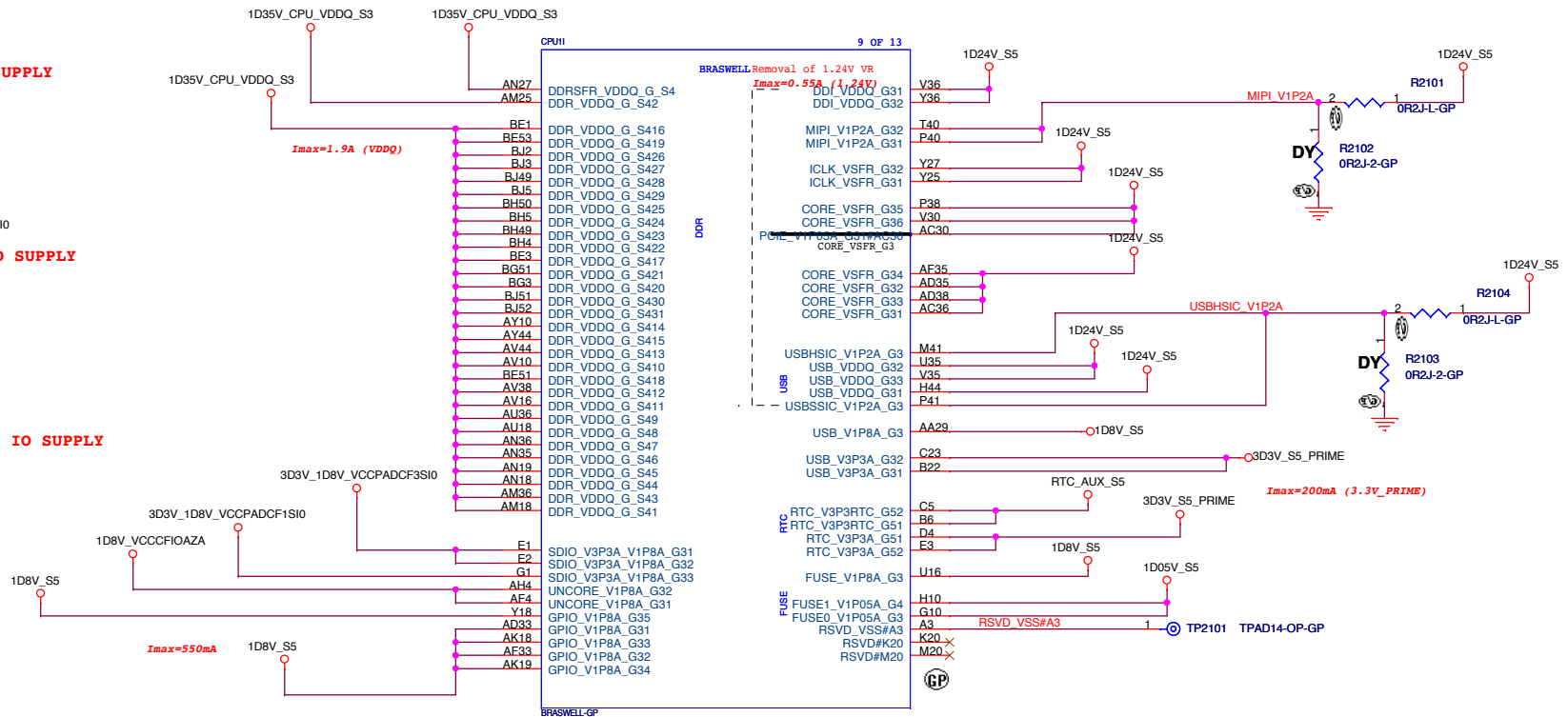
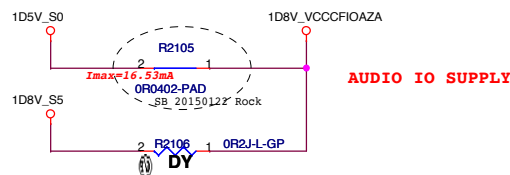
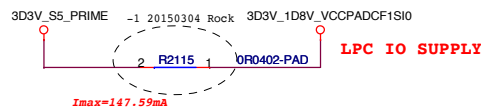
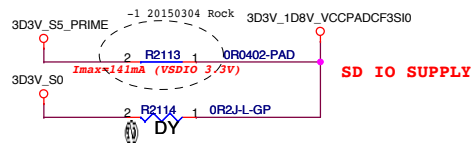
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SSID = CPU



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Size

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Document Number

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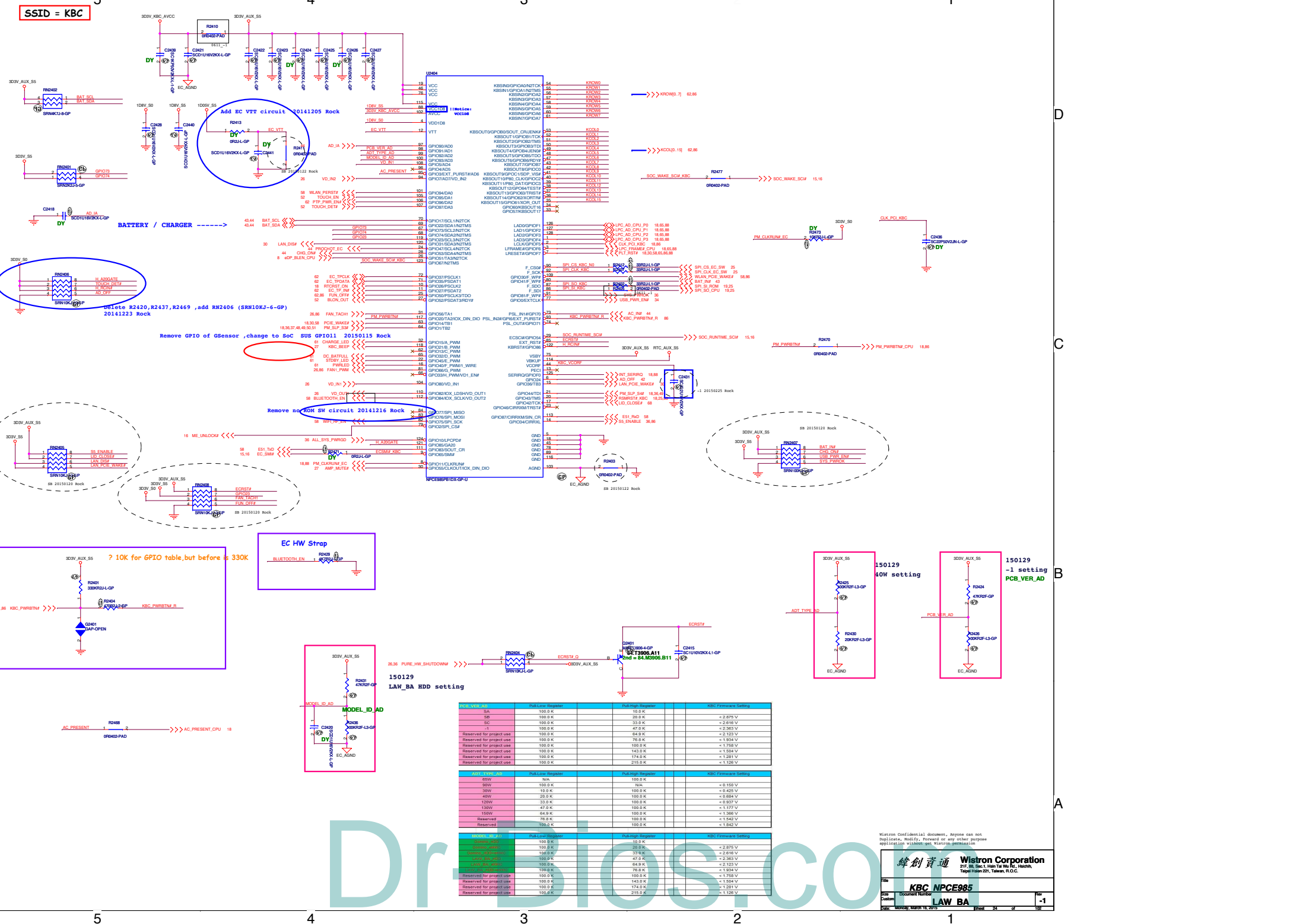
Rev

-1

Date: Monday, March 16, 2015

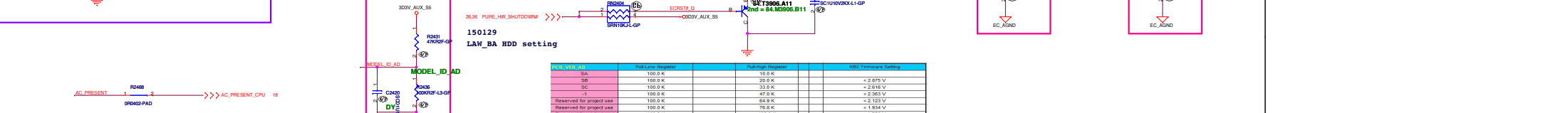
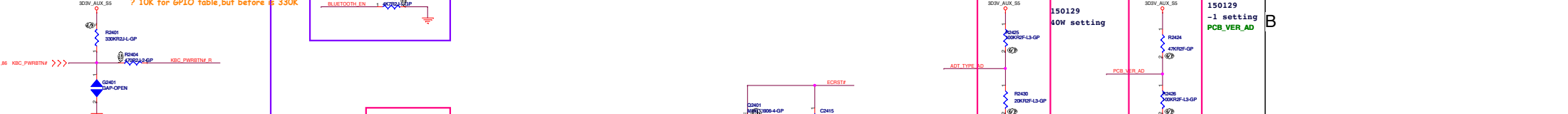
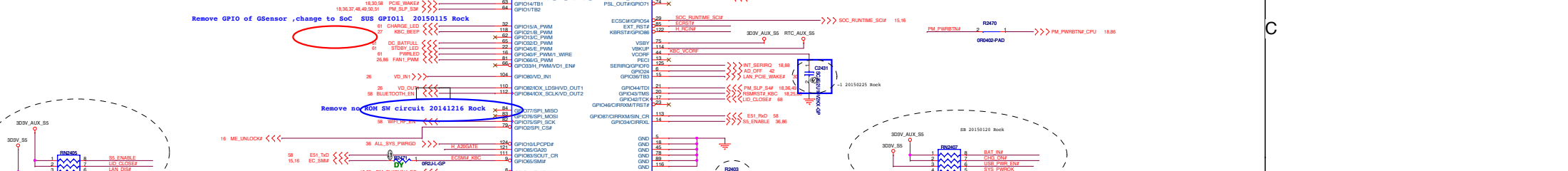
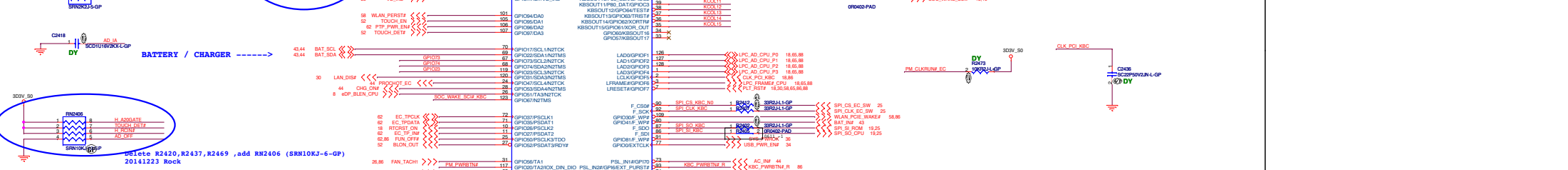
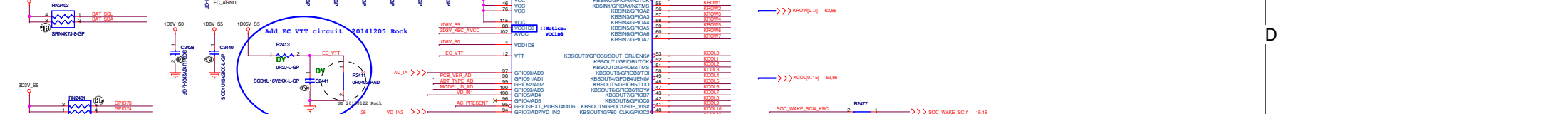
Sheet 23 of 102

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5 4 3 2 1

SSID = KBC



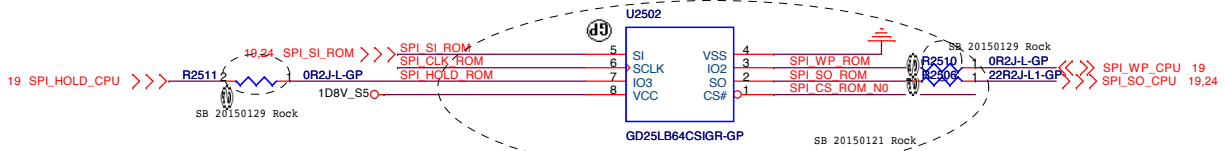
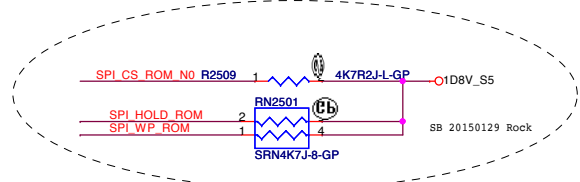
RES_VREF_AD	Full-Low Register	Full-High Register	KBC Firmware Setting
SA	100.0 K	10.0 K	
SB	100.0 K	20.0 K	+ 2.875 V
SC	100.0 K	20.0 K	+ 2.616 V
SD	100.0 K	20.0 K	+ 2.363 V
SE	100.0 K	20.0 K	+ 2.120 V
Reserved for project use	100.0 K	20.0 K	+ 1.934 V
Reserved for project use	100.0 K	20.0 K	+ 1.768 V
Reserved for project use	100.0 K	143.0 K	+ 1.524 V
Reserved for project use	100.0 K	174.0 K	+ 1.281 V
Reserved for project use	100.0 K	215.0 K	+ 1.128 V

RES_VREF_AD	Full-Low Register	Full-High Register	KBC Firmware Setting
500V	N/A	100.0 K	+ 0.152 V
300V	100.0 K	N/A	+ 0.452 V
400V	20.0 K	100.0 K	+ 0.684 V
1200V	33.0 K	100.0 K	+ 0.937 V
1300V	47.0 K	100.0 K	+ 1.177 V
1500V	64.0 K	100.0 K	+ 1.366 V
Reserved	78.0 K	100.0 K	+ 1.582 V
Reserved	100.0 K	100.0 K	+ 1.842 V

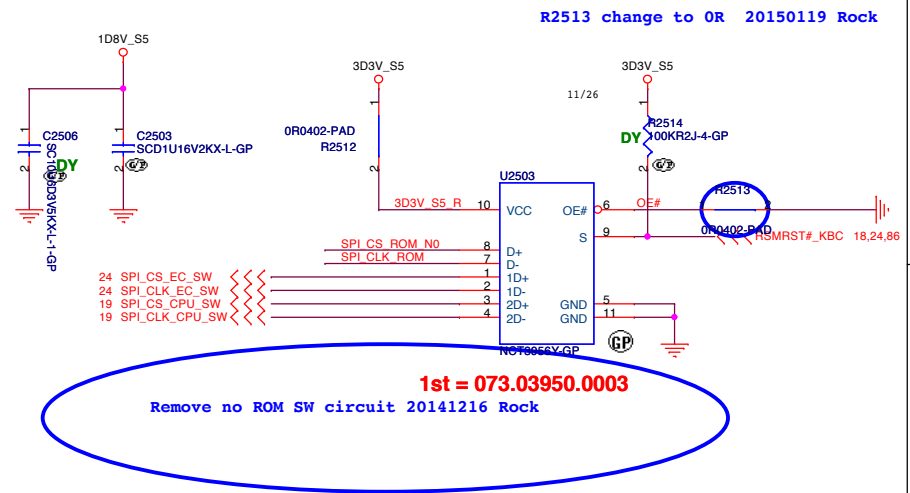
MODEL_ID_AD	Full-Low Register	Full-High Register	KBC Firmware Setting
0	100.0 K	10.0 K	
1	100.0 K	20.0 K	+ 2.875 V
2	100.0 K	20.0 K	+ 2.616 V
3	100.0 K	20.0 K	+ 2.363 V
4	100.0 K	20.0 K	+ 2.120 V
Reserved for project use	100.0 K	20.0 K	+ 1.934 V
Reserved for project use	100.0 K	20.0 K	+ 1.768 V
Reserved for project use	100.0 K	143.0 K	+ 1.524 V
Reserved for project use	100.0 K	174.0 K	+ 1.281 V
Reserved for project use	100.0 K	215.0 K	+ 1.128 V

SSID = Flash.ROM

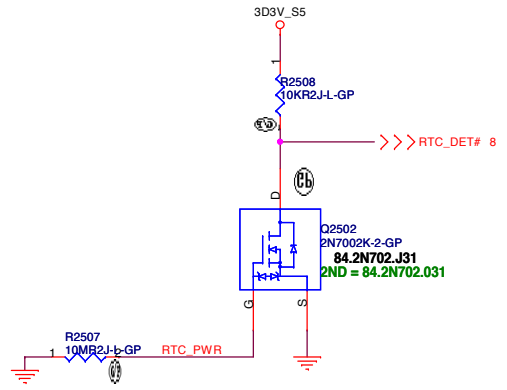
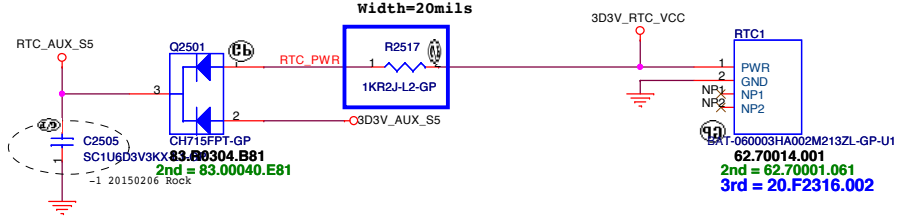
SPI FLASH ROM (8M BYTE) IC: PCH



1st : 072.02564.0A01 GIGADEVICE/ GD25LB64CSIGR
 2nd : 072.25647.0001 MXIC
 3rd : 072.25Q64.0E01 Winbond



SSID = RBAT

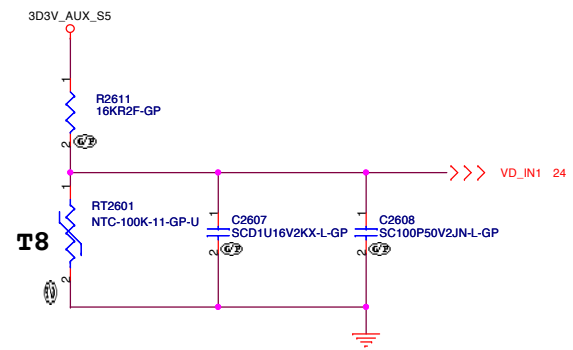


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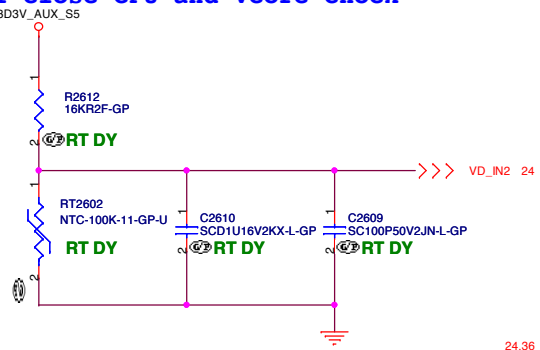
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Title: Flash(KBC+PCH)/RTC	
Size: Custom	Document Number: LAW BA
Date: Monday, March 16, 2015	Sheet 25 of 102
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SSID = Thermal

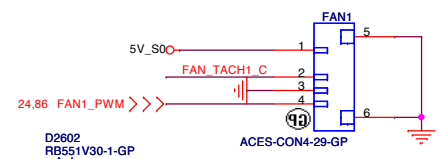
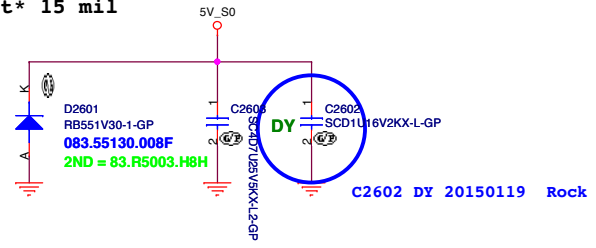
Layout 15 mil



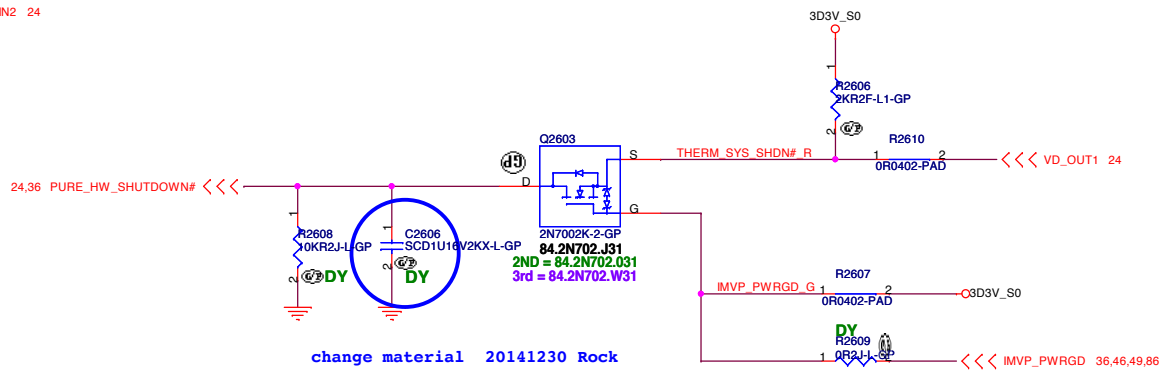
PT2601 close CPU and Vcore chock



PT2602 close CPU and memory



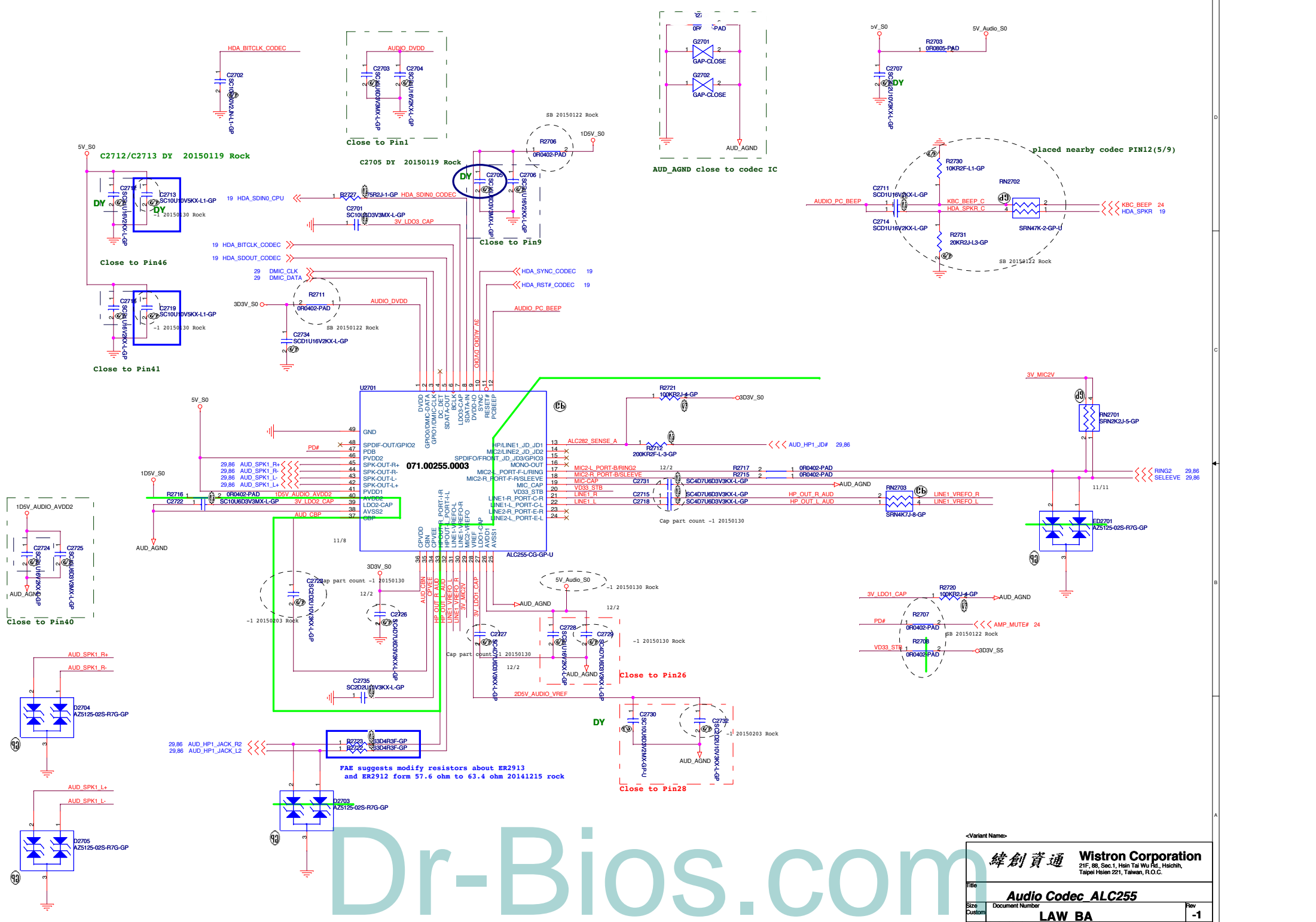
20.F0772.004
2nd = 20.F1804.004



change material 20141230 Rock

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Title			
Thermal 7718/Fan Controller P2793			
Size	Document Number	Rev	
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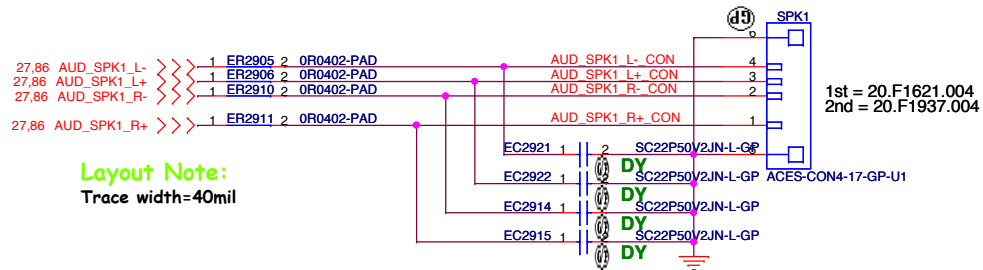
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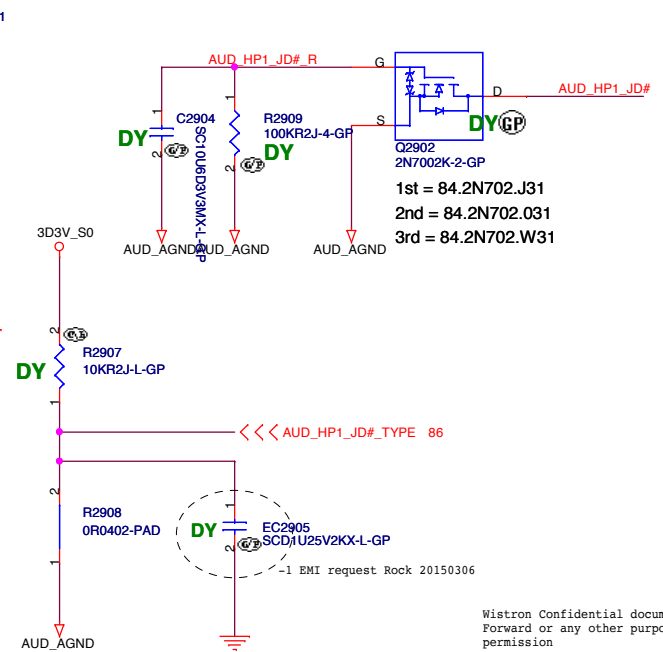
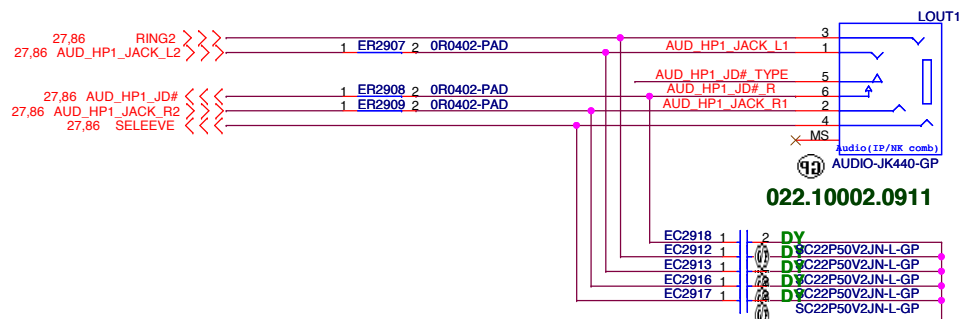
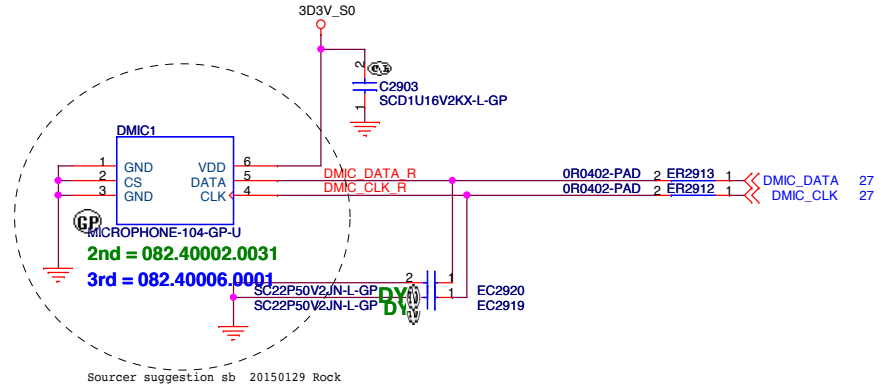
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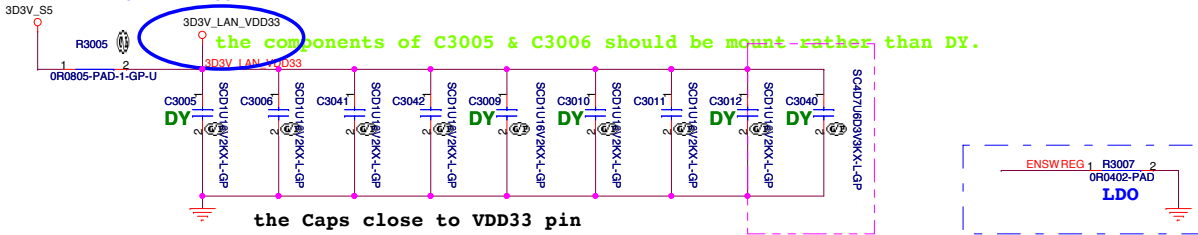


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Title			
Audio Jack			
Size	Document Number	Rev	
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3D3V_LAN_VDD33 rise time must be controlled between 0.5mS and 100mS
20141224 Rock

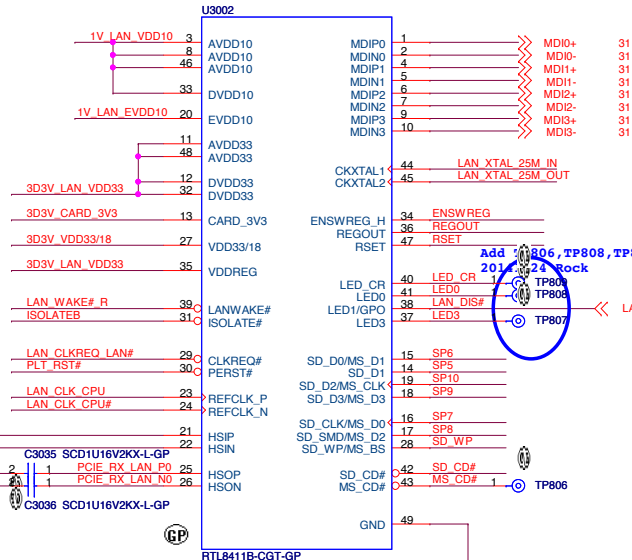
the components of C3005 & C3006 should be mount rather than DY.



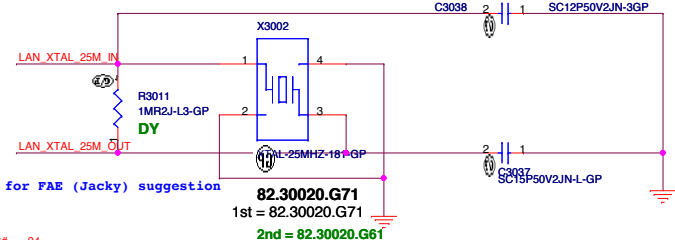
the Caps close to VDD33 pin

Close to VDDREG pin

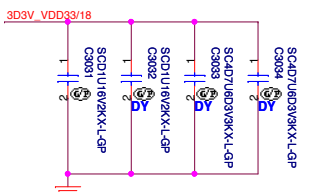
- SP5 2 ER3014 1 <<>> SD_DATA1 33,86
- SP6 2 ER3022 1 <<>> SD_DATA0 33,86
- SP7 2 22RF-1-GP ER3021 1 <<>> SD_CLK 33,86
- SP8 2 ER3024 1 <<>> SD_CMD 33,86
- SP9 2 ER3023 1 <<>> SD_DATA3 33,86
- SP10 2 ER3025 1 <<>> SD_DATA2 33,86
- SD_WP 0R0402-PAD <<>> SD_WP# 33
- SD_CD# 0R0402-PAD <<>> SD_CD# 33,86



Add TP806, TP808, TP809 for FAE (Jacky) suggestion



82.30020.G71
1st = 82.30020.G71
2nd = 82.30020.G61

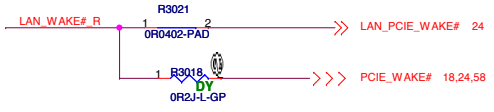


- LAN_CLKREQ_LAN# <<>> LAN_CLKREQ_LAN# 19
- LAN_CLK_CPU <<>> LAN_CLK_CPU 19
- LAN_CLK_CPU# <<>> LAN_CLK_CPU# 19
- PLT_RST# <<>> PLT_RST# 18,24,58,65,86,88

- PCIE_TX_LAN_P0 <<>> PCIE_TX_LAN_P0 19
- PCIE_TX_LAN_N0 <<>> PCIE_TX_LAN_N0 19
- PCIE_RX_CPU_P0 <<>> PCIE_RX_CPU_P0 19
- PCIE_RX_CPU_N0 <<>> PCIE_RX_CPU_N0 19

1st = 071.8411B.0003

注意BOM必須帶入071.8411B.0003此顆料號 20141229 Rock



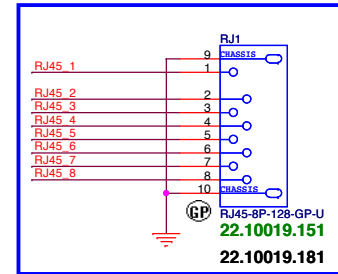
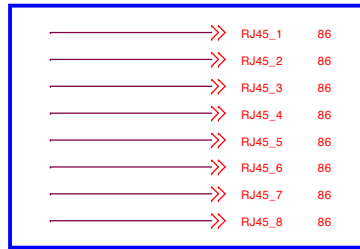
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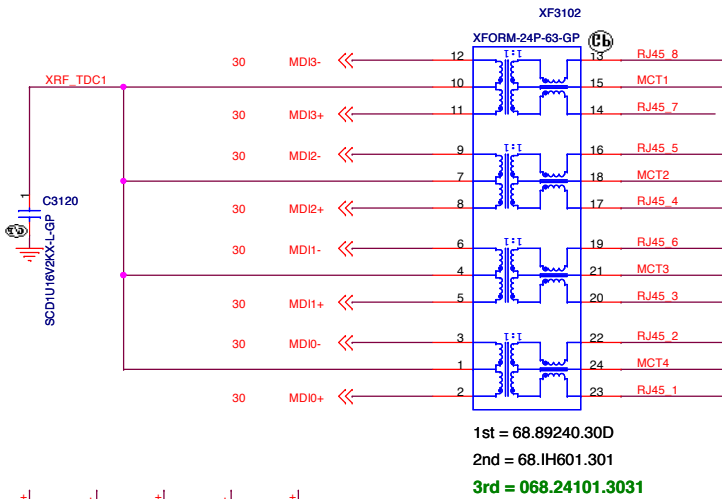
Title: LAN(RTL8411)
Size: Custom
Date: Monday, March 16, 2015

Document Number: LAW BA
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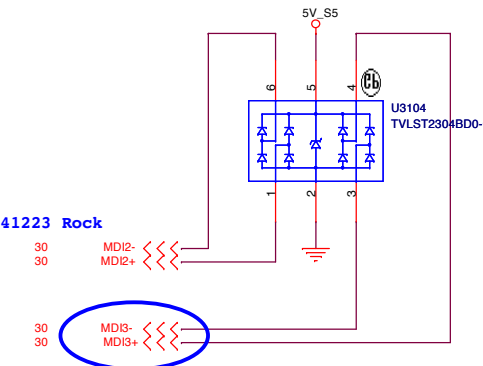
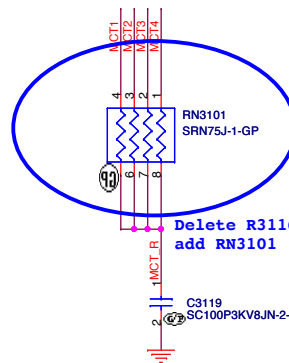
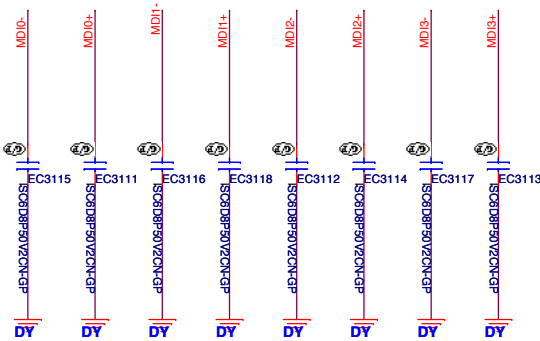
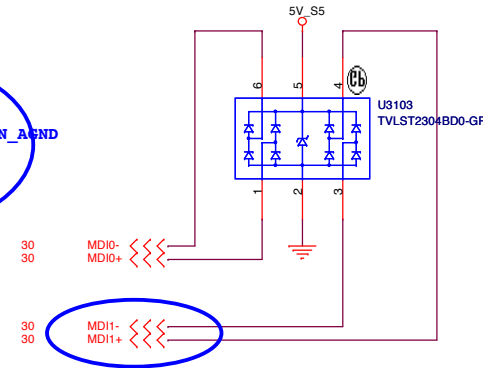
SSID = LAN



LAN_RJ45 connector



Delete EC3101, EC3102, LAN_AENB
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Title
RTS5170(CARD READER)

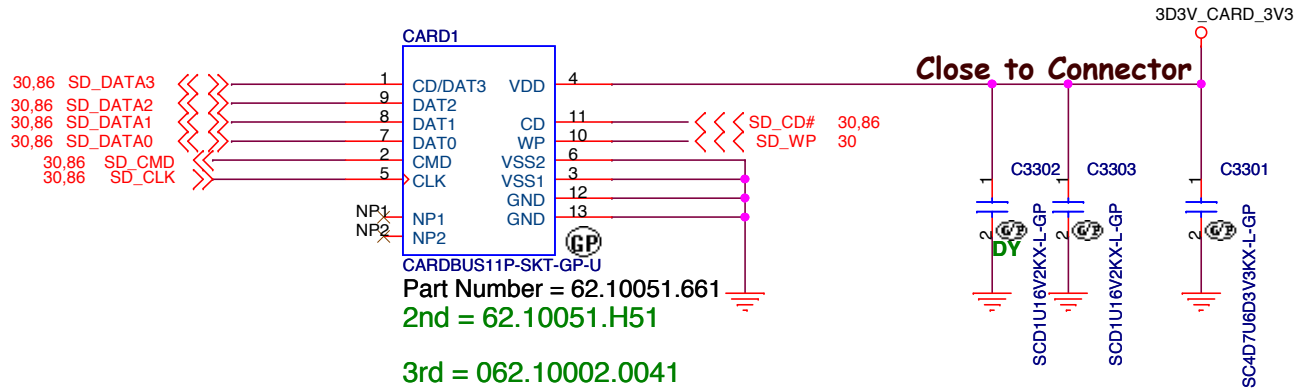
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SSID = SDIO

SD//MS Card Reader

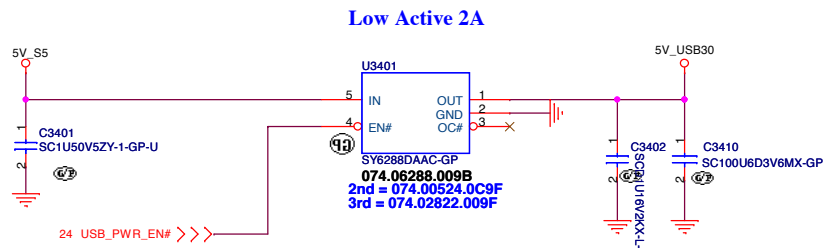


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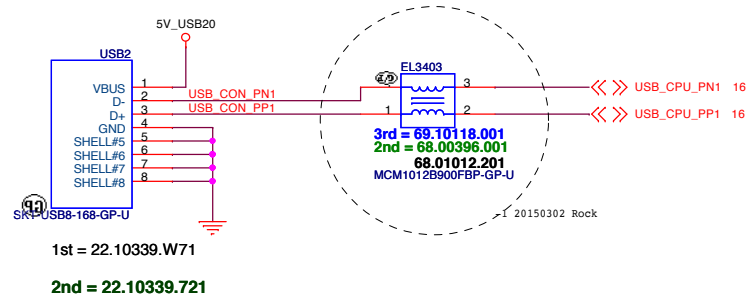
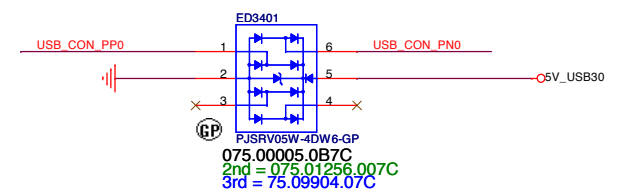
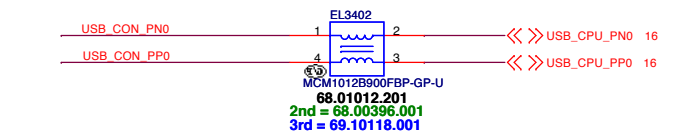
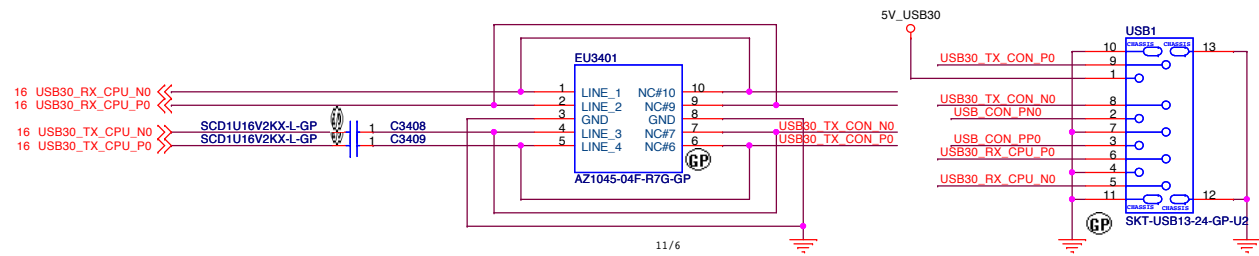
Title CARD Reader CONN		
Size Custom	Document Number LAW BA	Rev -1
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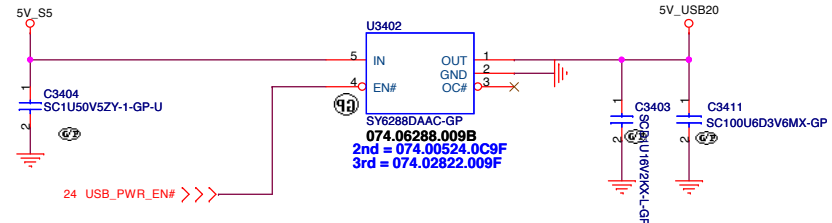


P/N 074.22802.0A9F change to 074.02822.009F 20141205 Rock

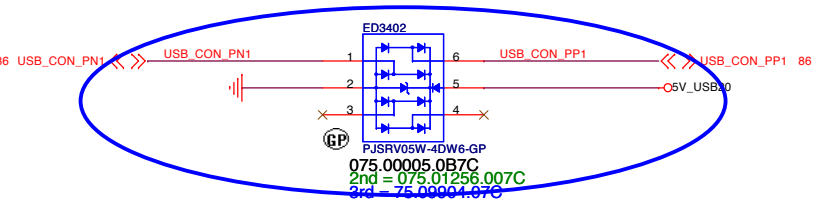
USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+



Low Active 2A



P/N 074.22802.0A9F change to 074.02822.009F 20141205 Rock



增加ED3402 給USB2 usb trace 使用 因為共用ED3401 兩組 usb 離太遠 分支過長 20141212 Rock

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USB 2.0 / 3.0 Port	
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Reserve			
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Power Sequence

Table 55. S4/S5 to S0 (Power Up) Sequence

Parameter		Min	Max	Unit	Notes
T0	RTC_VCC to ILB_RTC_TEST# de-assertion	9		ms	
T1	V3P3A valid to PMC_RSMRST# de-assertion	10		us	
T2	Core well stable to DRAM_CORE_PWROK and PMC_CORE_PWROK assertion	100		ms	
T3					

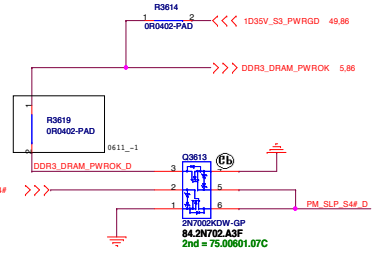
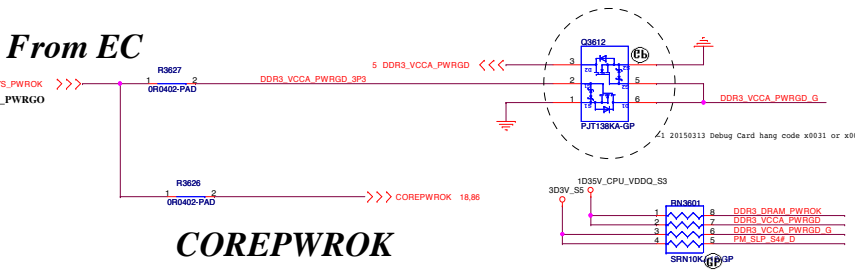
DDR3_VCCA_PWRGD

DDR3_DRAM_PWROK

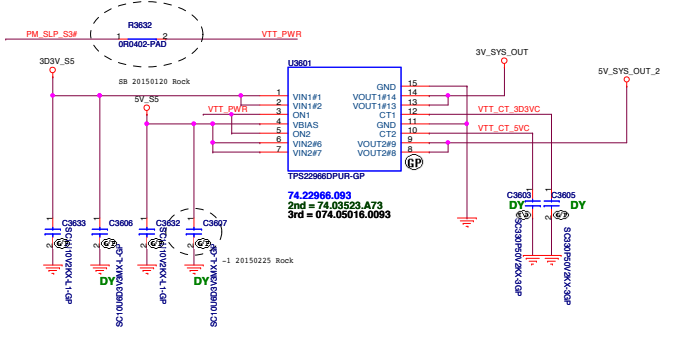
From EC

Delay 104ms with ALL_SYS_PWRGO

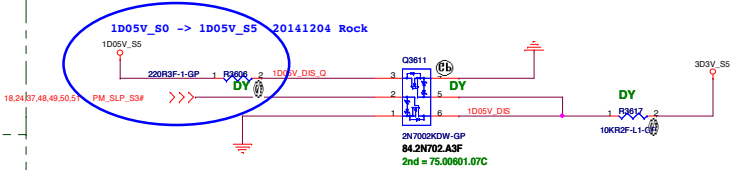
COREPWROK



ANNIE Run Power

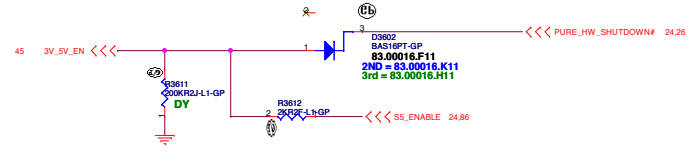
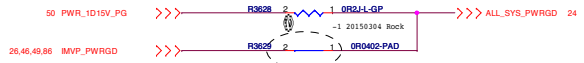


Discharge circuit

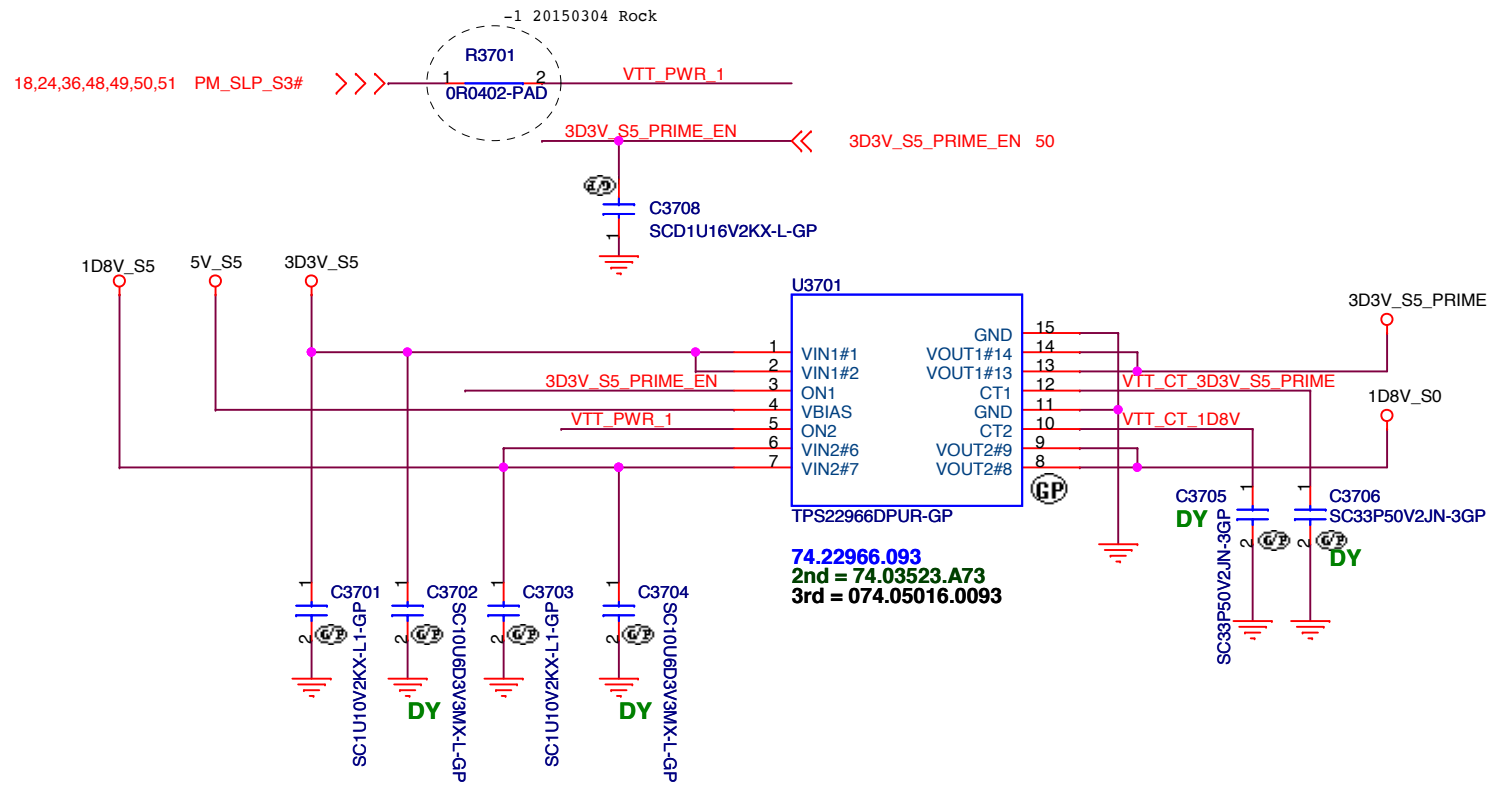


ALL_SYS_PWRGD

To EC



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ADAPTER OCP / S3 reduction			
Title			
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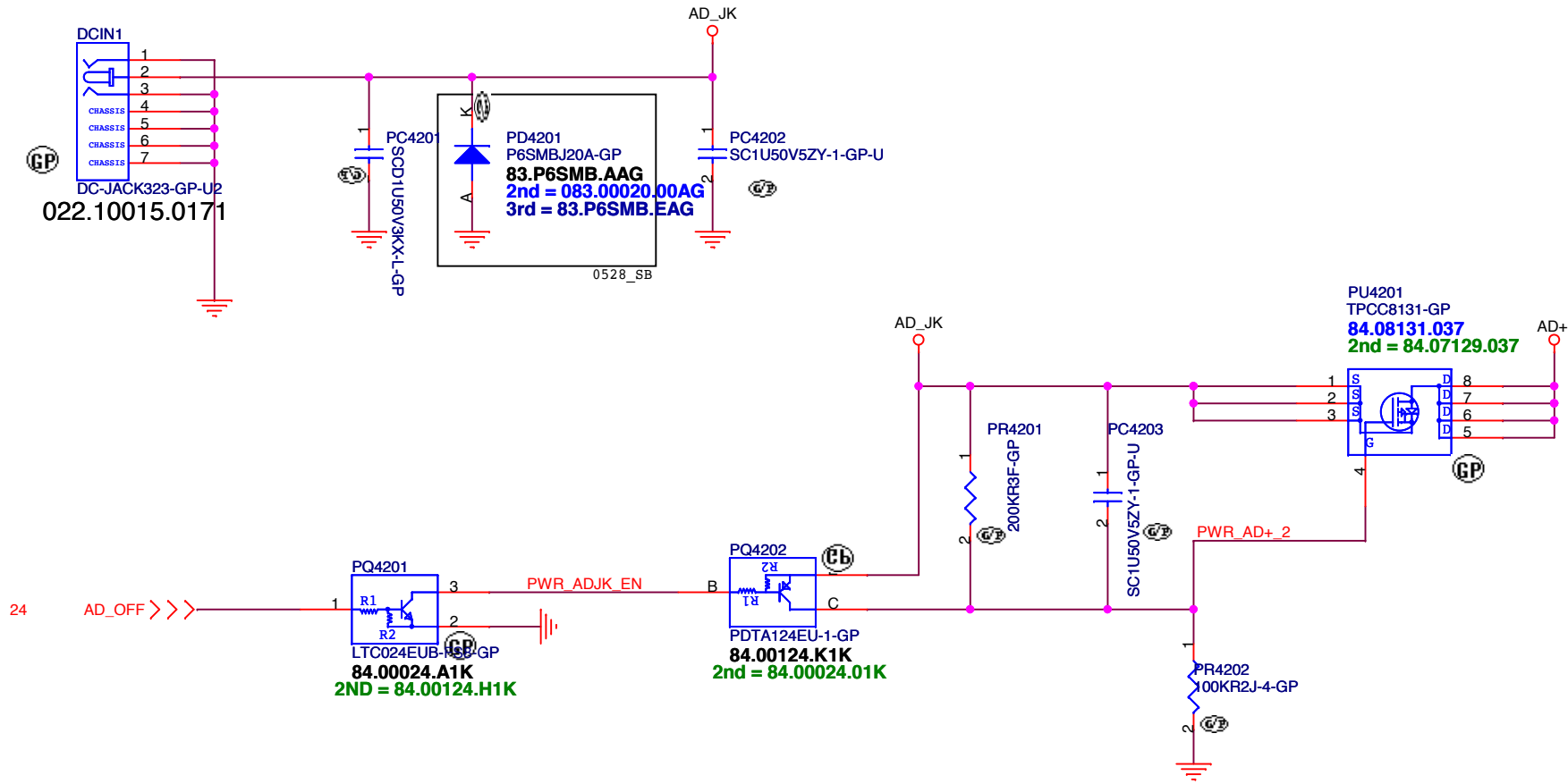
Date: Monday, March 16, 2015

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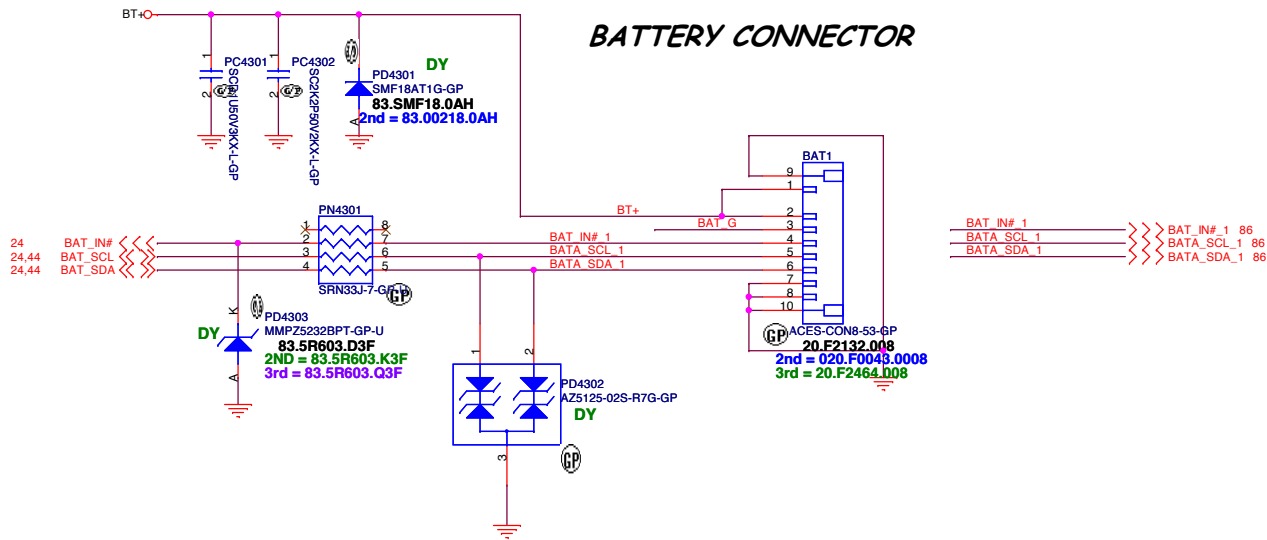
Adaptor in to generate DCBATOUT



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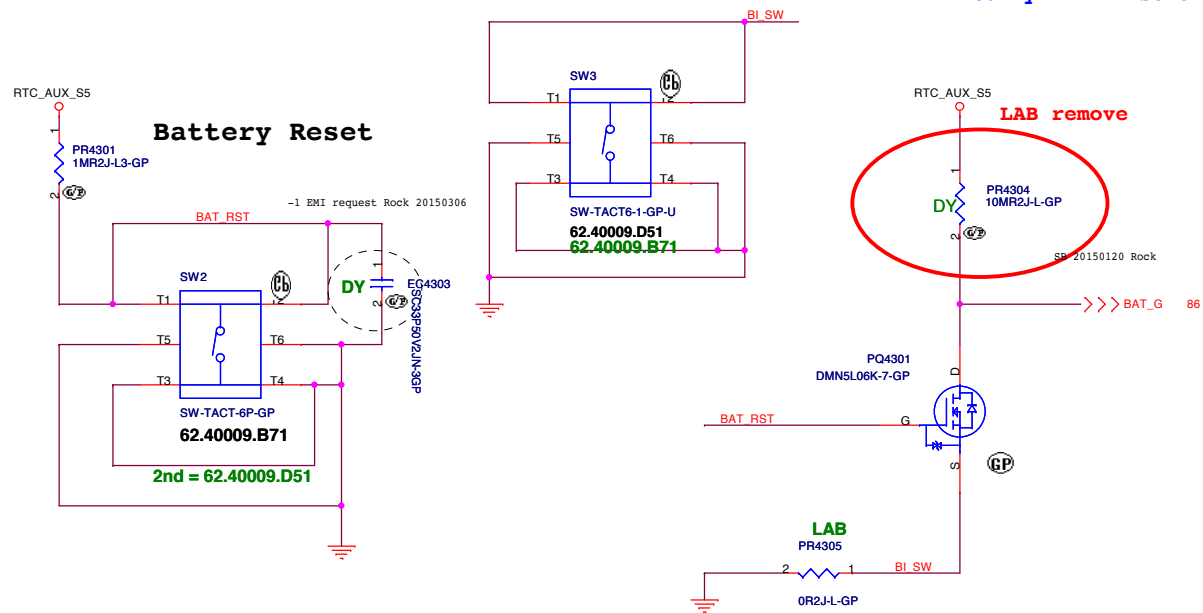
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Size	Document Number	Rev	
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Battery Insert

Modify BI Pin schematic circuit 20141205 Rock

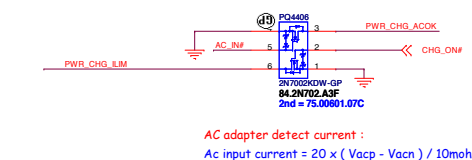
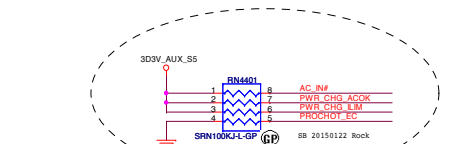
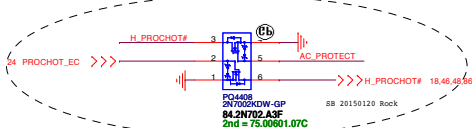
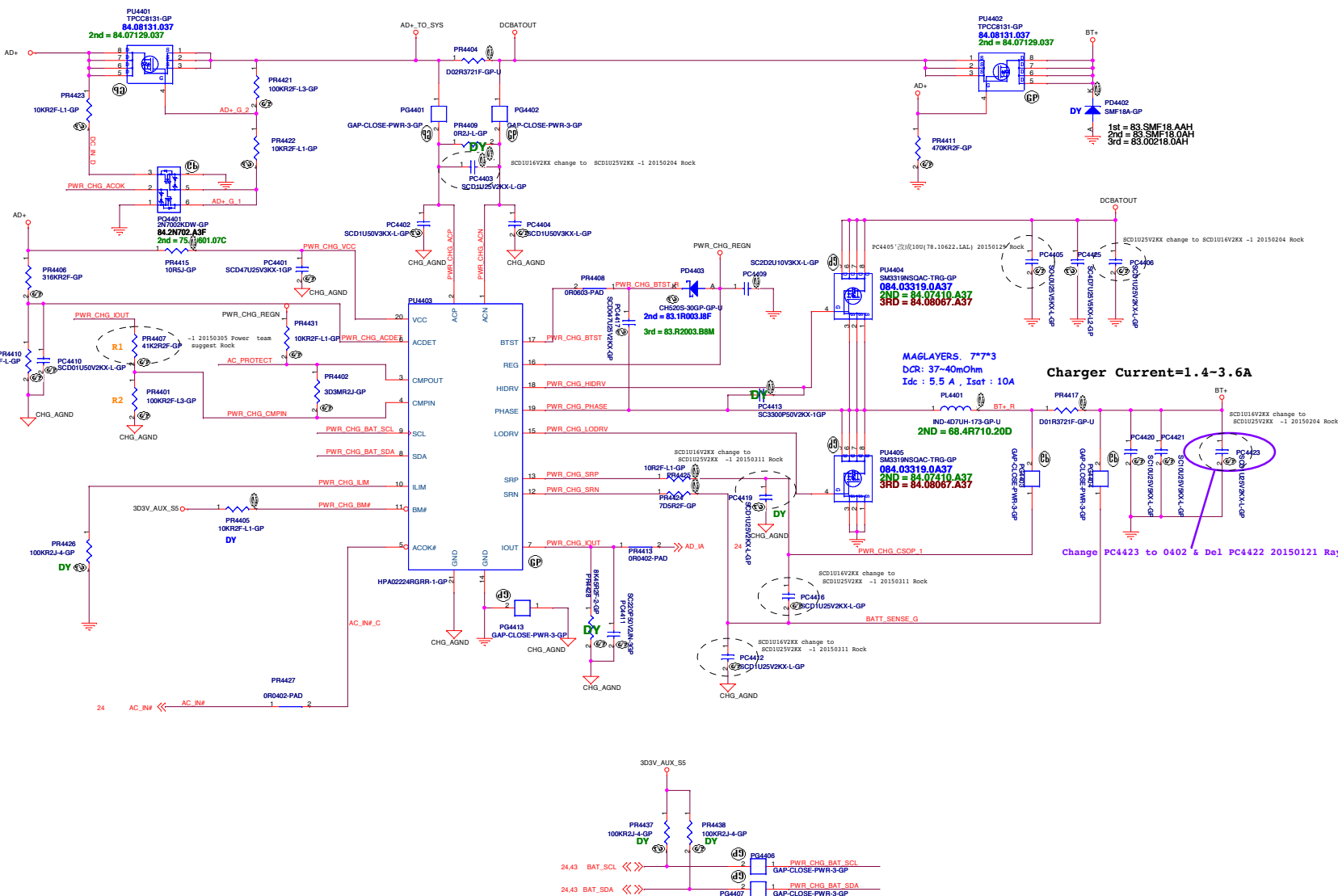


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SSID = Charger

AD+ total power	R1	R2
40W	41.2K	100K



MAGLAYERS, 7*7*3
DCR: 37~40mOhm
I_{dc} : 5.5 A , I_{so}t : 10A
Charger Current=1.4~3.6A

Change PC4423 to 0402 & Del PC4422 20150121 Ray

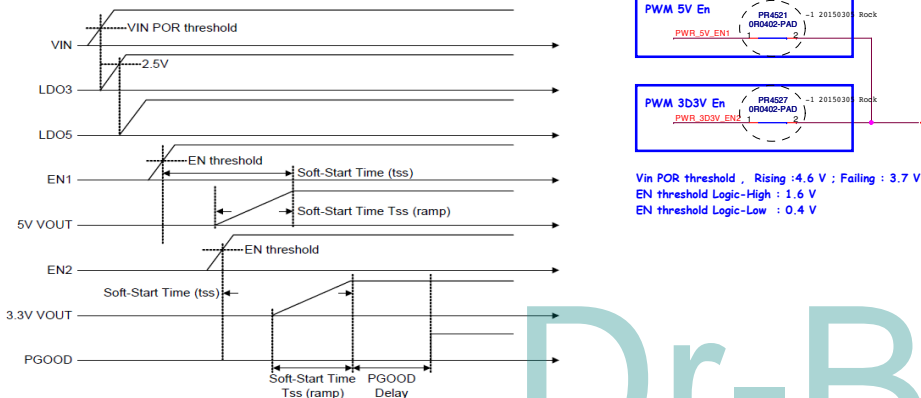
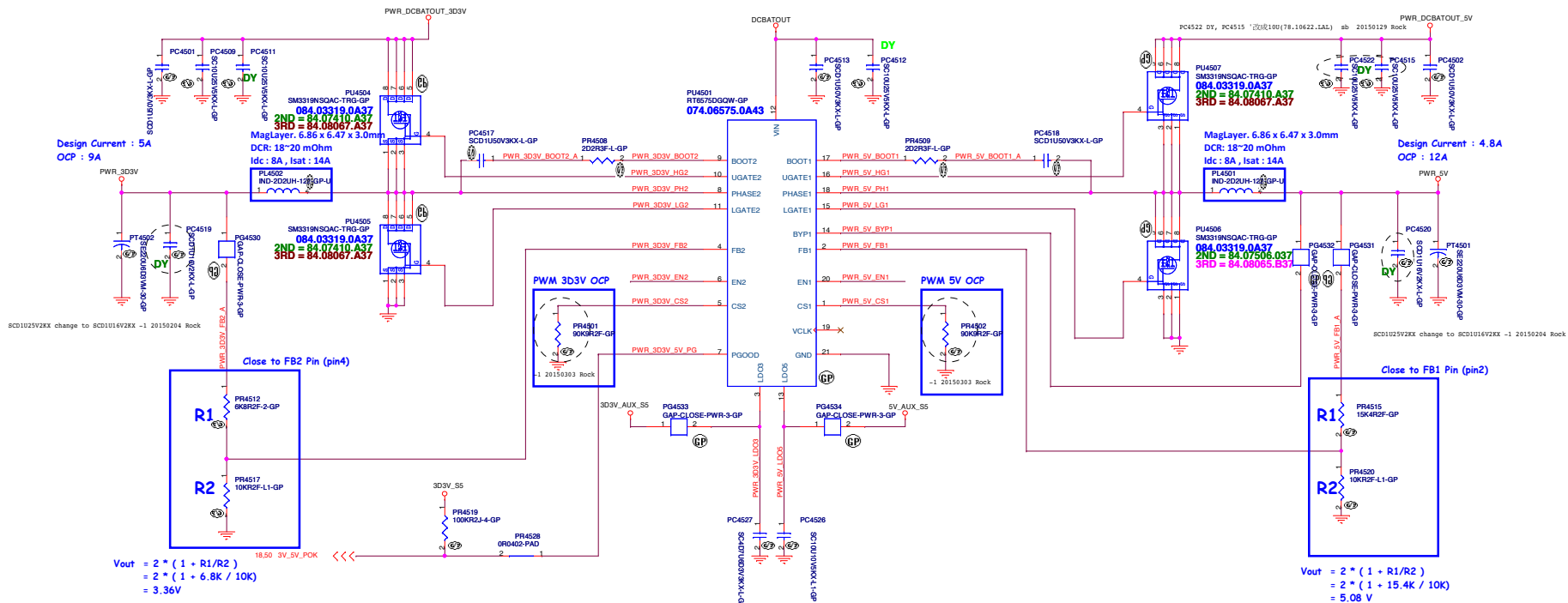
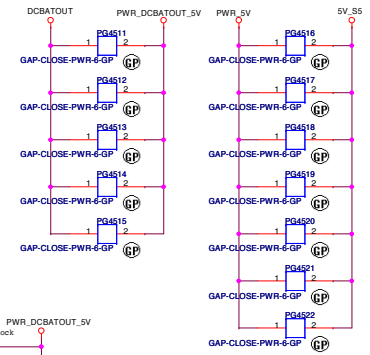
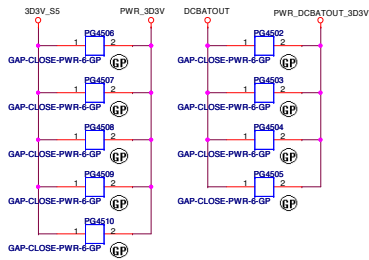


Figure 6. RT6575B Timing

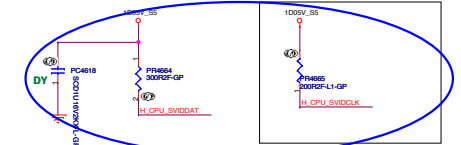
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SSID = CPU Regulator

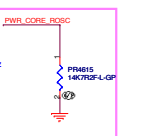
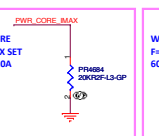
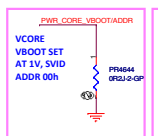
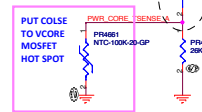
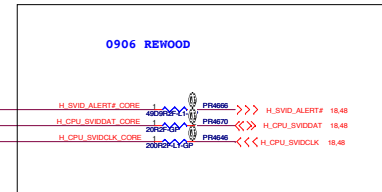
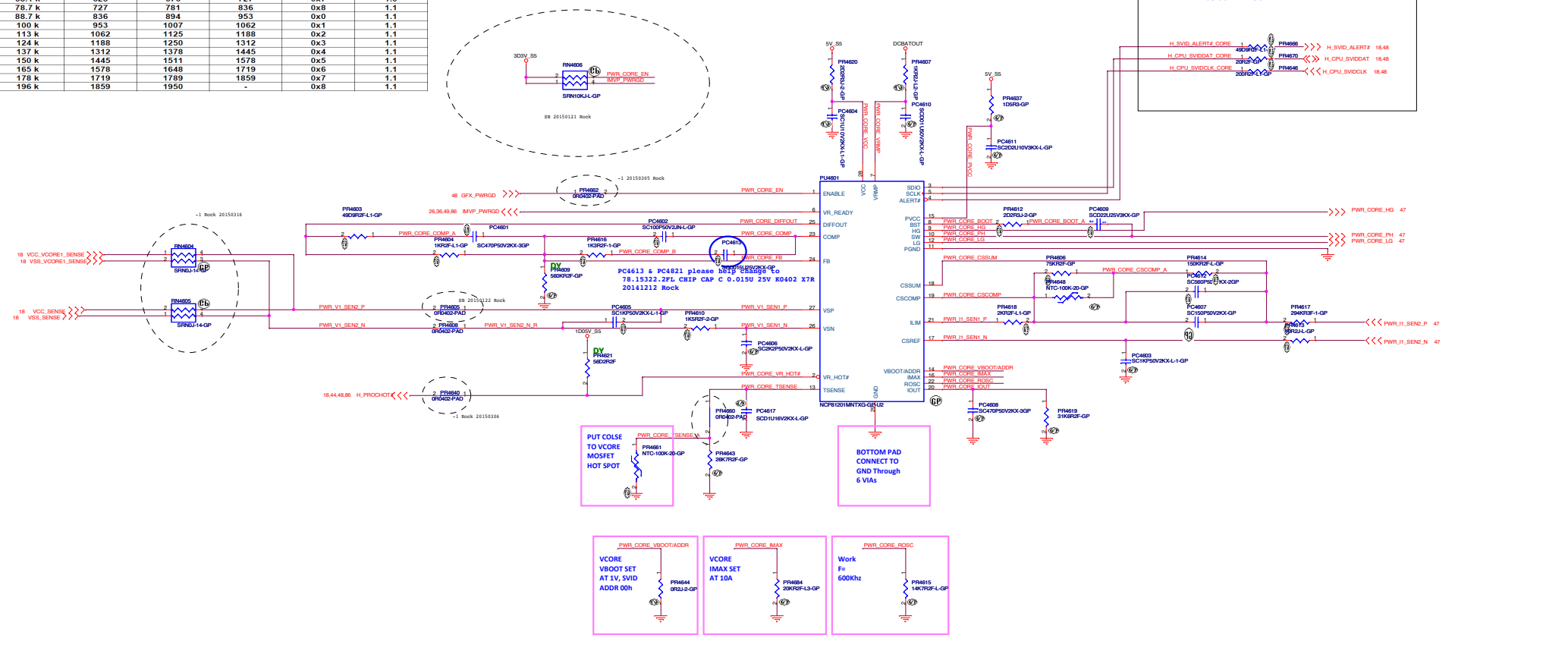
SVID Address and Boot Voltage Table

VBOOT/ADDR Resistor (Ohm)	Vboot Pin Voltage (mV)			SVID Address	Vboot (V)
	Min	Typ	Max		
0	0	0	102	0x0	1.0
14.0 k	102	140	180	0x1	1.0
22.1 k	180	219	258	0x2	1.0
30.1 k	258	301	344	0x3	1.0
39.2 k	344	391	438	0x4	1.0
48.7 k	438	484	531	0x5	1.0
57.6 k	531	578	625	0x6	1.0
68.1 k	625	676	727	0x7	1.0
78.7 k	727	781	836	0x8	1.1
88.7 k	836	894	953	0x0	1.1
100 k	953	1007	1062	0x1	1.1
113 k	1062	1125	1188	0x2	1.1
124 k	1188	1250	1312	0x3	1.1
137 k	1312	1378	1445	0x4	1.1
150 k	1445	1511	1578	0x5	1.1
165 k	1578	1648	1719	0x6	1.1
178 k	1719	1789	1859	0x7	1.1
196 k	1859	1950	-	0x8	1.1

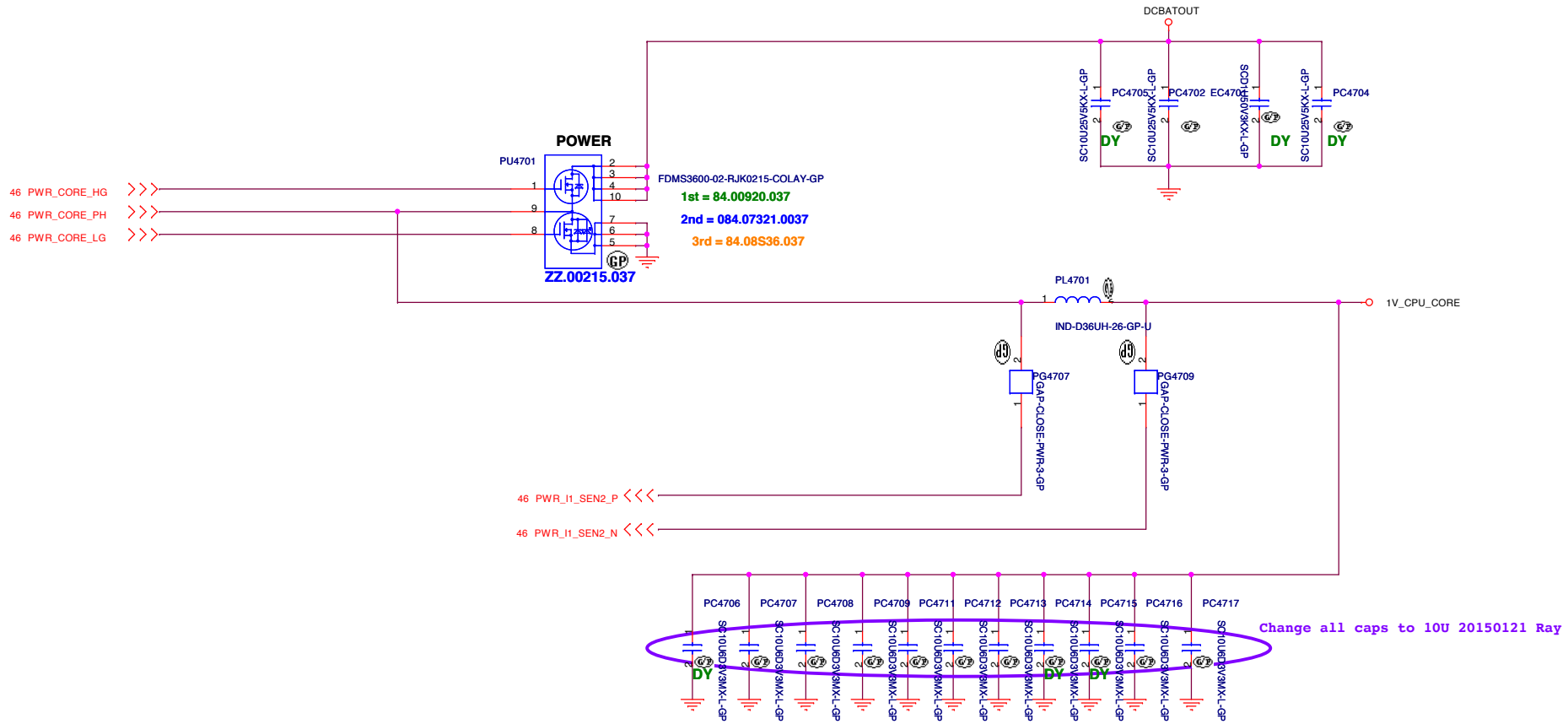
VR12.1 POWER CKT - 1 phase 19Vin



Change position of pull high from PMN IC side to soc side
20141225 Rock



SSID = CPU Regulator

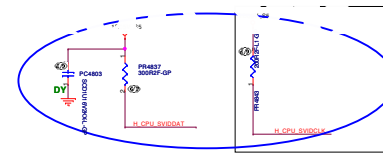


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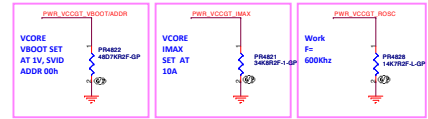
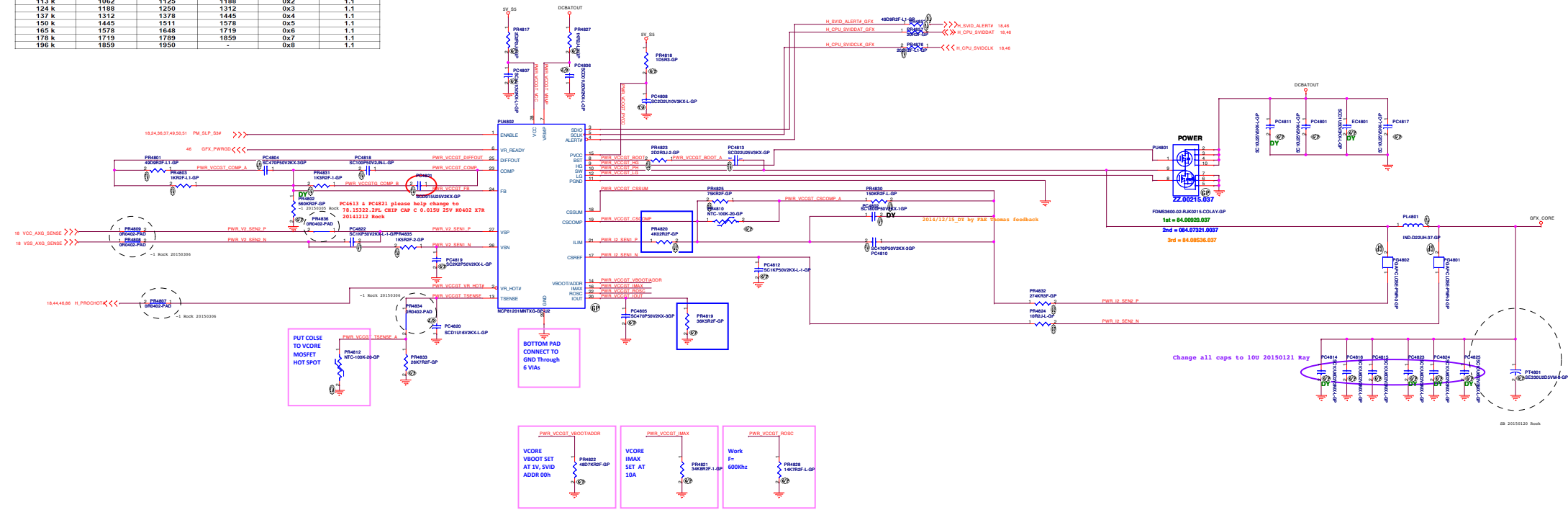
SVID Address and Boot Voltage Table

VBOOT/ADDR Resistor (Ohm)	Min	Typ	Max	SVID Address	Vboot (V)
0	0	102	102	0x0	1.0
14.0 k	102	140	180	0x1	1.0
22.1 k	180	210	250	0x2	1.0
30.1 k	250	301	344	0x3	1.0
39.2 k	344	391	438	0x4	1.0
48.7 k	438	484	531	0x5	1.0
57.6 k	531	578	625	0x6	1.0
68.1 k	625	676	727	0x7	1.0
78.7 k	727	781	836	0x8	1.1
88.7 k	836	894	953	0x0	1.1
100 k	953	1007	1062	0x1	1.1
113 k	1062	1125	1188	0x2	1.1
124 k	1188	1250	1312	0x3	1.1
137 k	1312	1378	1445	0x4	1.1
150 k	1445	1511	1578	0x5	1.1
165 k	1578	1648	1719	0x6	1.1
178 k	1719	1789	1859	0x7	1.1
196 k	1859	1950	-	0x8	1.1

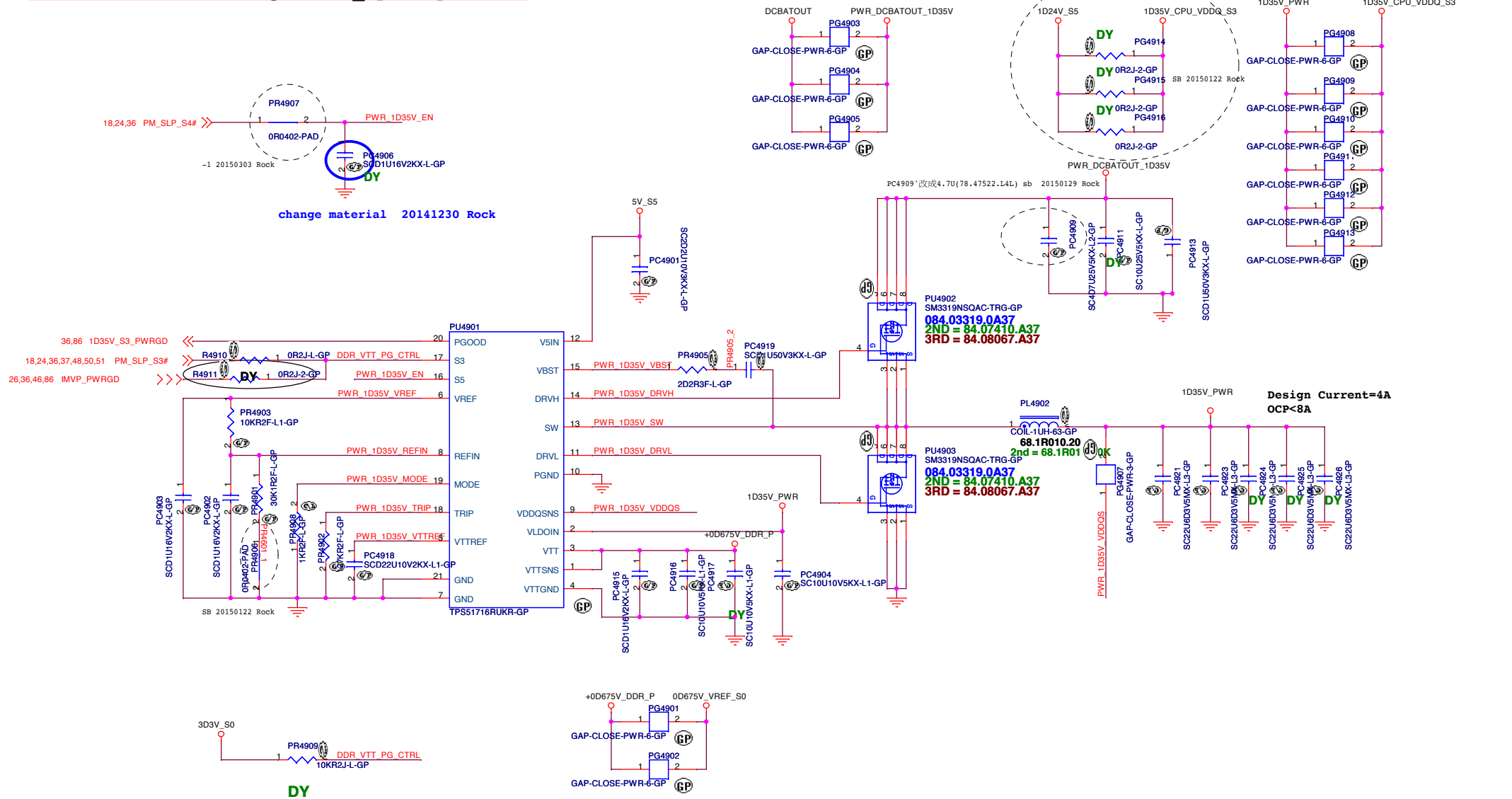
VR12.1 POWER CKT - 1 phase 19Vin



Change position of pull high from PMN IC side to SoC side 20141225 Rock



SSID = PWR.Plane.Regulator_1p3V0.675V



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

MODE

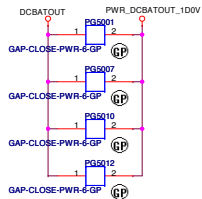
PR4608	Frequency	Discharge Mode
200k ohm	400kHz	Tracking Discharge
100k ohm	300kHz	
68k ohm	300kHz	Non-tracking Discharge
47k ohm	400kHz	

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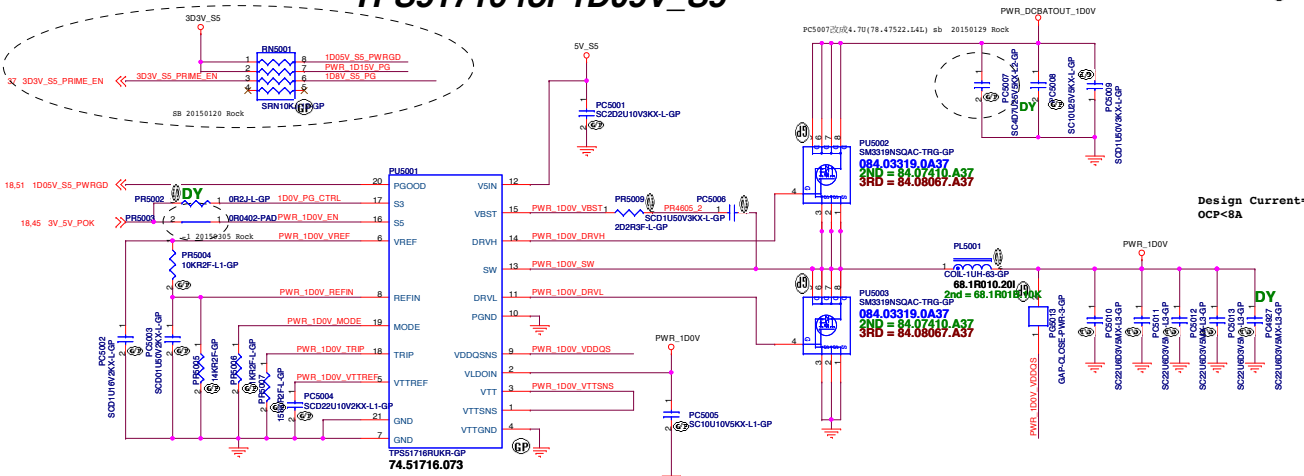
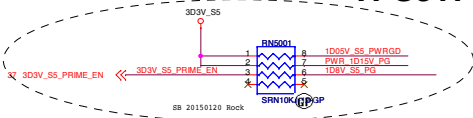
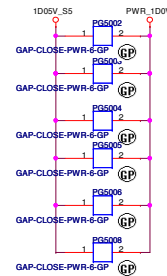
緯創資通 Wistron Corporation
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Title: **TPS51716(1.35V_S3/0.675V_S0)**

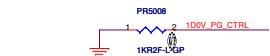
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TPS51716 for 1D05V_S5



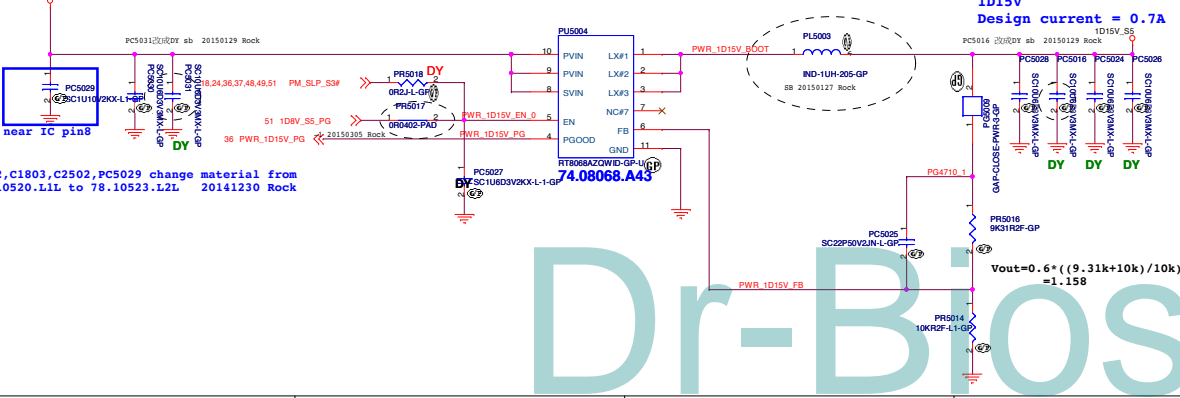
Design Current=4A
OCP=8A



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

MODE	PR5006	Frequency	Discharge Mode
	33k ohm	500kHz	Non-tracking Discharge
	22k ohm	670kHz	Non-tracking Discharge
	12k ohm	670kHz	Tracking Discharge
	1k ohm	500kHz	Tracking Discharge

RT8068 PWM for 1D15V



1D15V
Design current = 0.7A

$$V_{out} = 0.6 * ((9.31k + 10k) / 10k) = 1.158$$

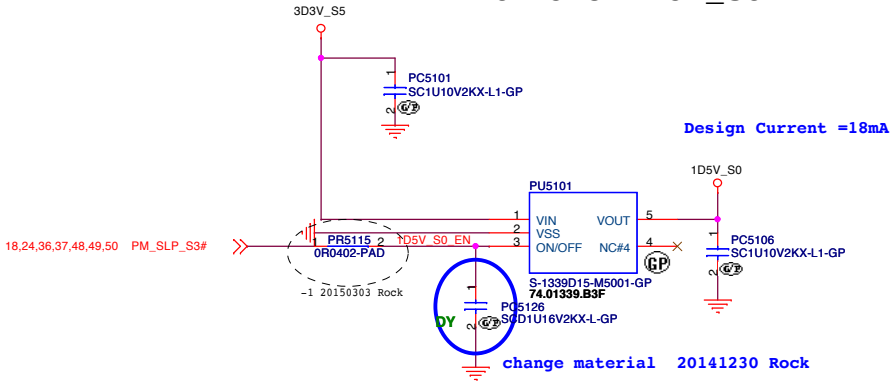
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Doc Number	LAW BA	Rev: 1
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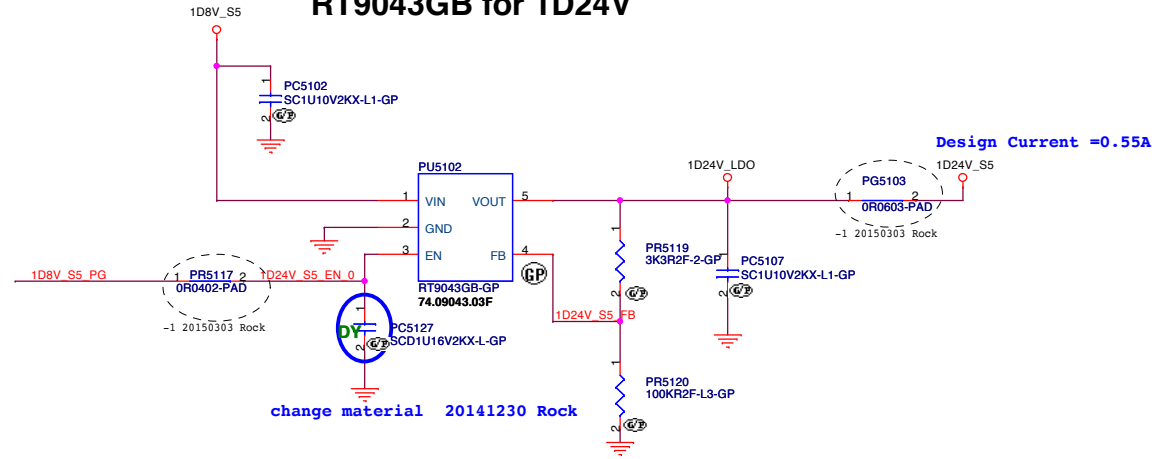
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SSID = PWR.Plane.Regulator_1p5v

TLV70215 for 1D5V_S0

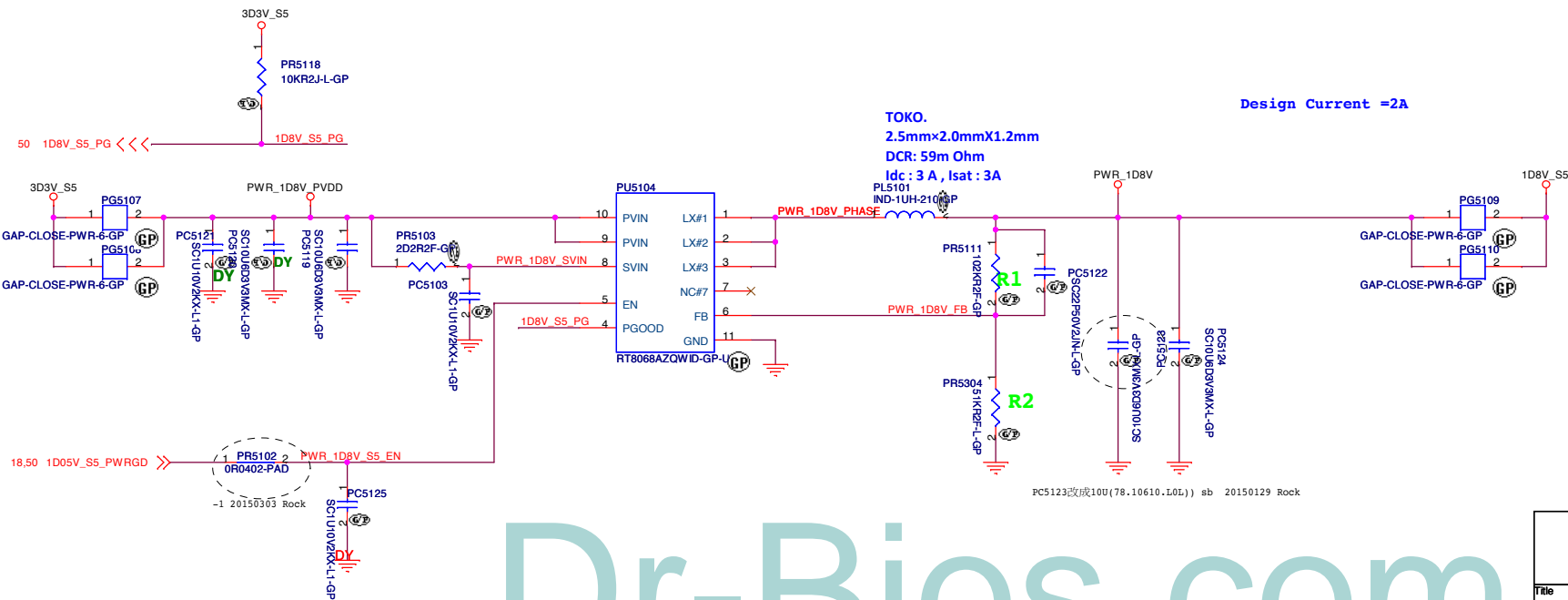


RT9043GB for 1D24V



SSID = PWR.Plane.Regulator_1p8v

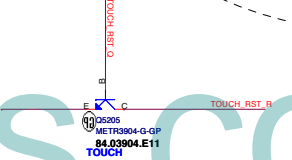
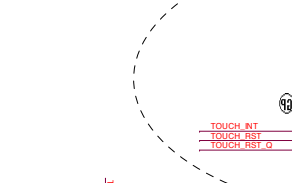
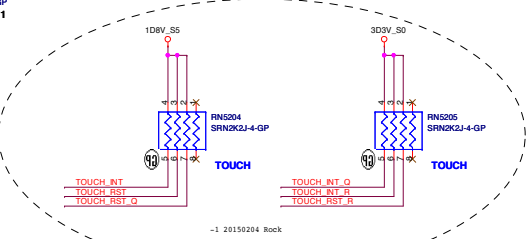
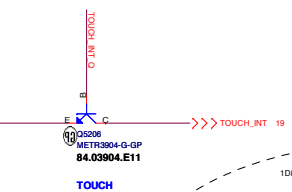
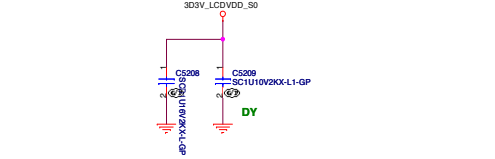
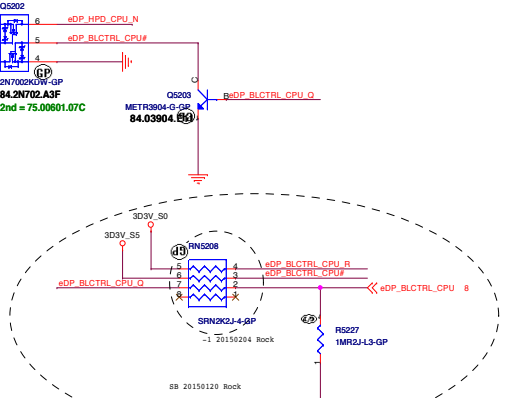
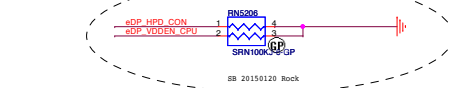
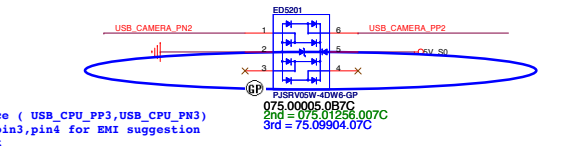
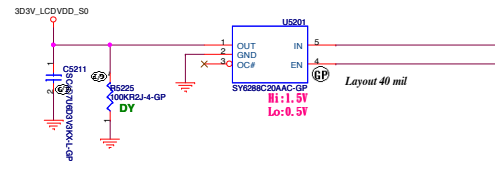
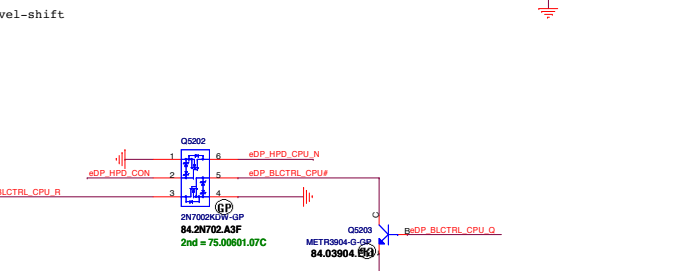
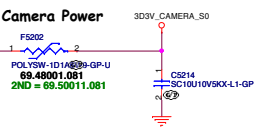
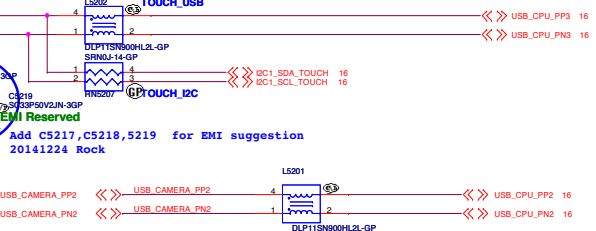
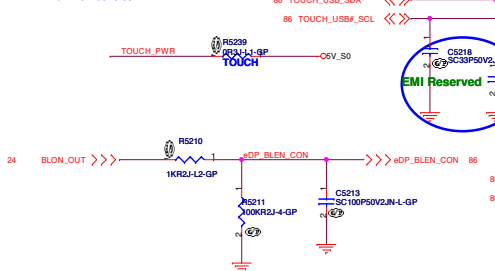
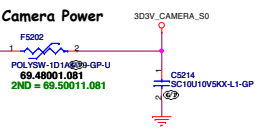
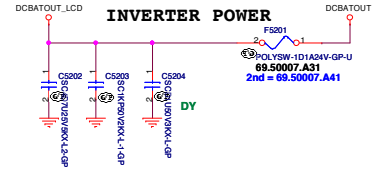
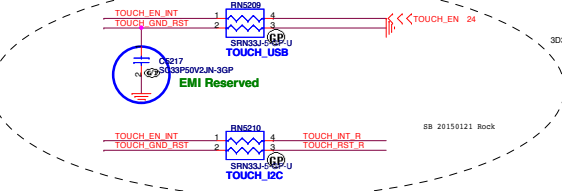
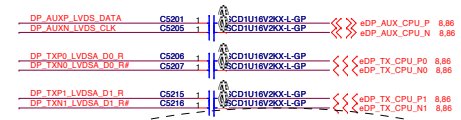
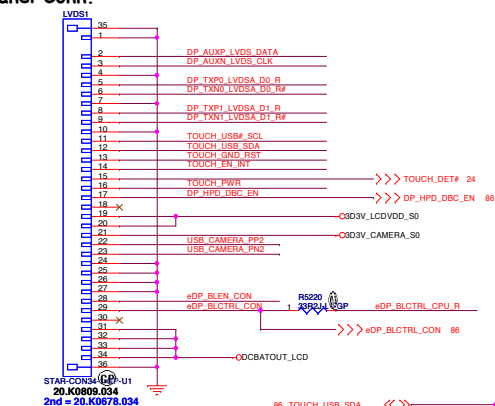
RT8068AZQWID-GP-U for 1D8V_S5



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Panel Conn.



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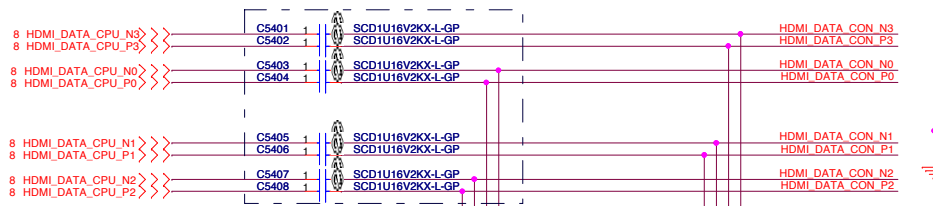
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		21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
CRT Connector			
Size	Document Number		Rev
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SSID = VIDEO

HDMI Level Shifter & CONNECTOR

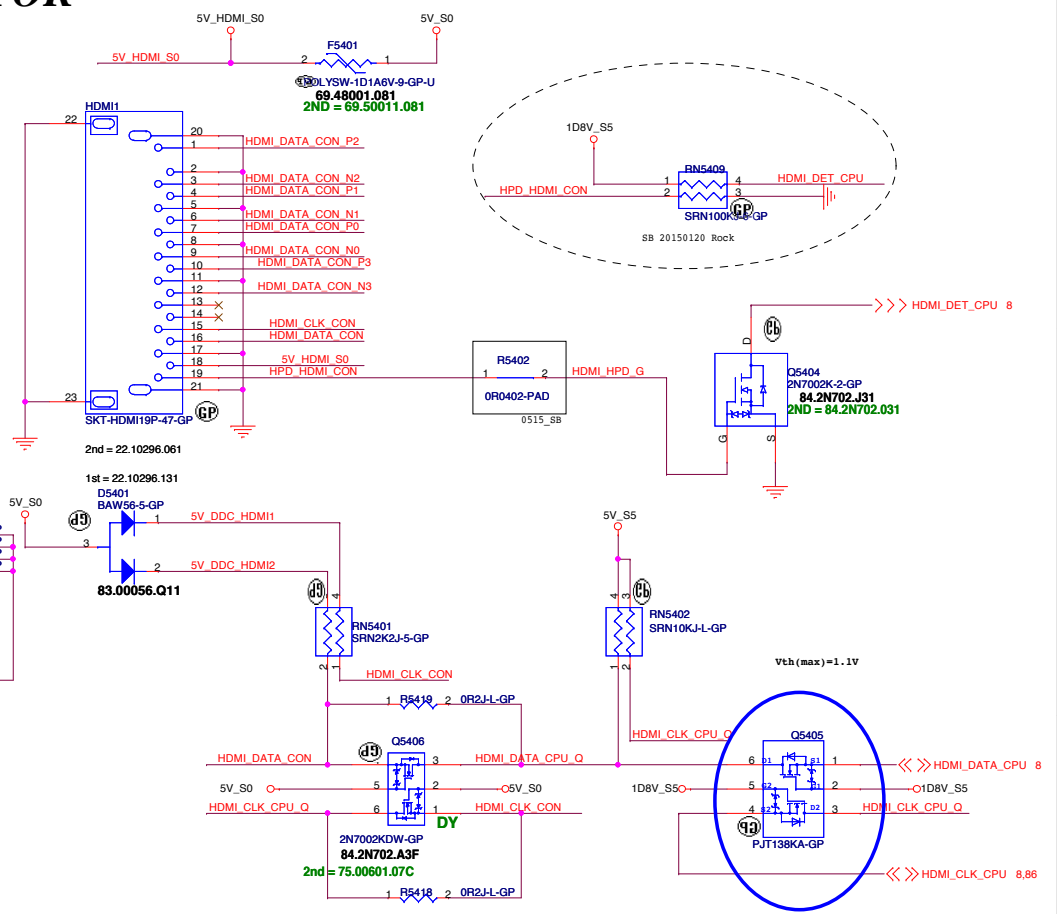
W I S T R O N

HDMI_DATA_CON_N3	1	R5417	150R2F-4-L-GP	DY	HDMI_DATA_CON_P3
HDMI_DATA_CON_N0	1	R5414	150R2F-4-L-GP	DY	HDMI_DATA_CON_P0
HDMI_DATA_CON_N1	1	R5415	150R2F-4-L-GP	DY	HDMI_DATA_CON_P1
HDMI_DATA_CON_N2	1	R5416	150R2F-4-L-GP	DY	HDMI_DATA_CON_P2



Close to HDMI Connector

Close to Level Shift



Delete Q5403 ,change Q5405 to PJT138KA-GP 20141229 Rock

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Title: **HDMI Level Shifter/Connector**

Size: Custom Document Number: LAW BA Rev: -1

Date: Monday, March 16, 2015 Sheet: 54 of 102

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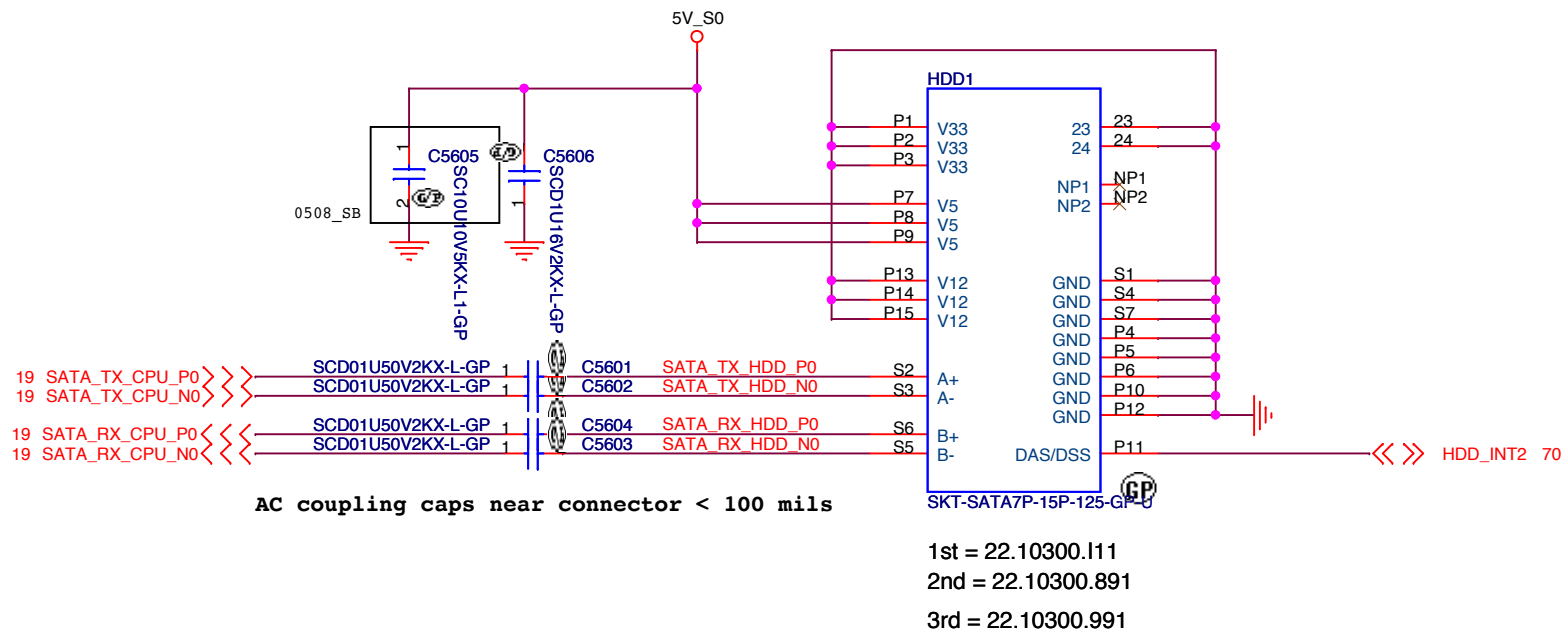
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Title		
Reserved		
Size A3	Document Number LAW BA	Rev -1
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SSID = SATA

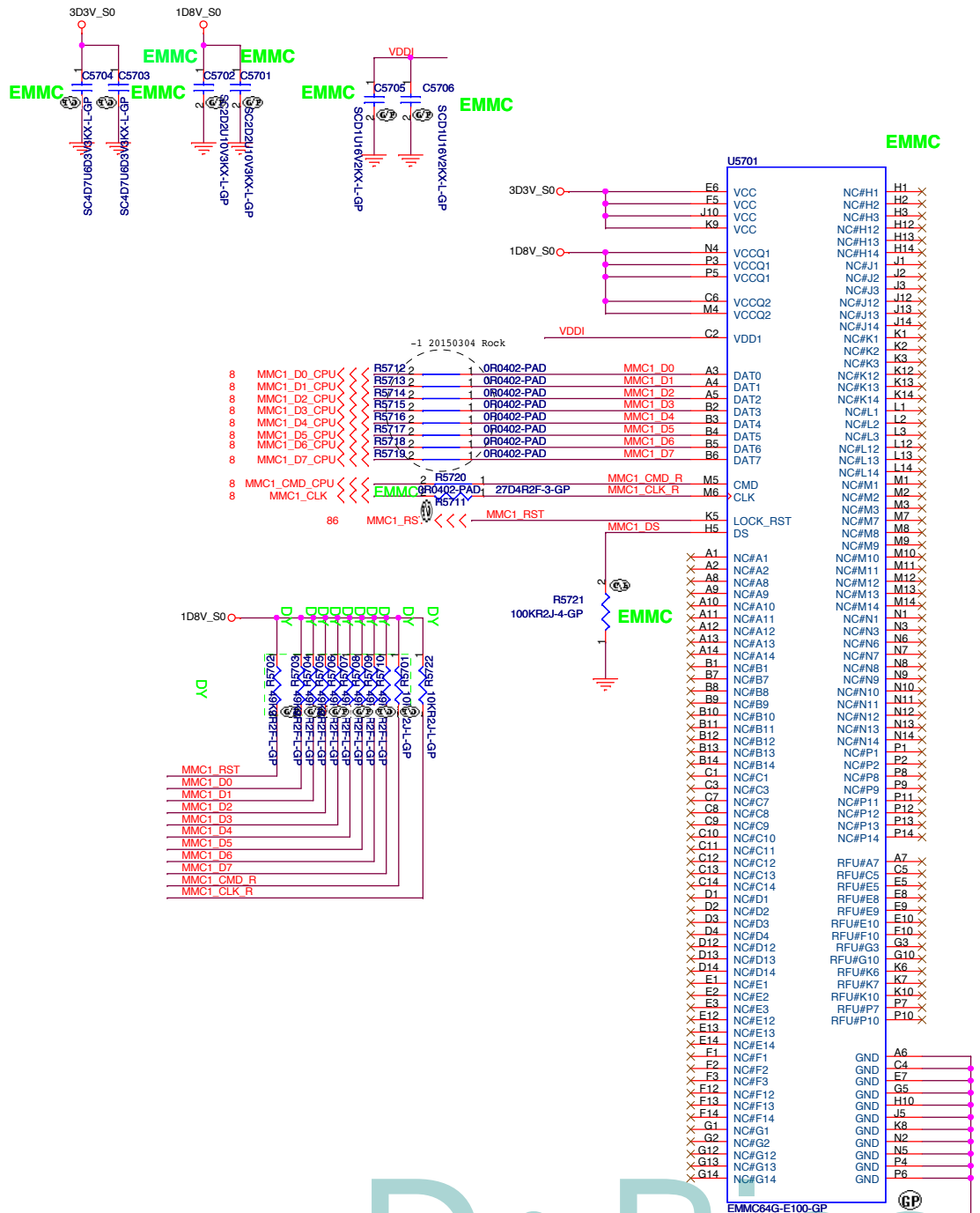
SATA HDD Connector



ODD Connector

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Title HDD / ODD / NGFF SSD			
Size A4	Document Number LAW BA		Rev -1
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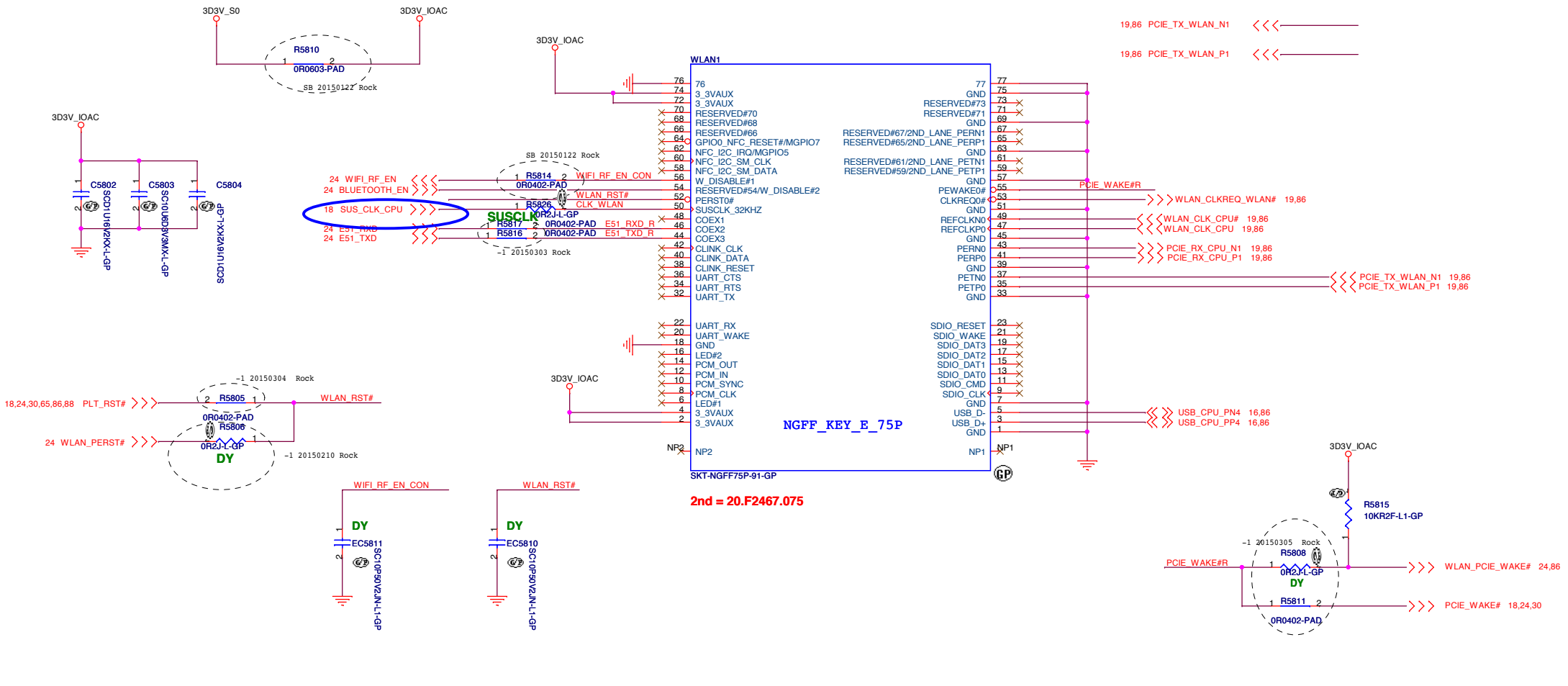
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1st = KN.0320G.008
 2nd = KN.0640G.001
 3rd = KN.03207.007
 4th = KN.0640G.005

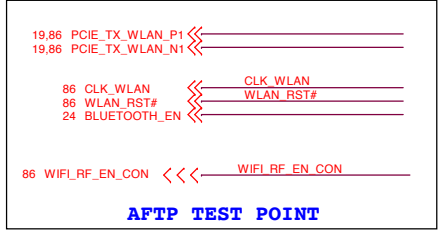
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EMMC LAW BA	
Title	Rev
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SSID = Wireless

Mini Card Connector(802.11a/b/g/n)



Remove IOAC function 20150115 Rock



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Title: **Mini Card-WLAN**

Size A3 Document Number: **LAW-BA** Rev: **-1**

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SSID = 3G

Mini Card Connector(WWAN)

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<Variant Name>

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Title		
WWAN CONN		
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SSID = mSATA

Mini Card Connector(mSATA)

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<Variant Name>

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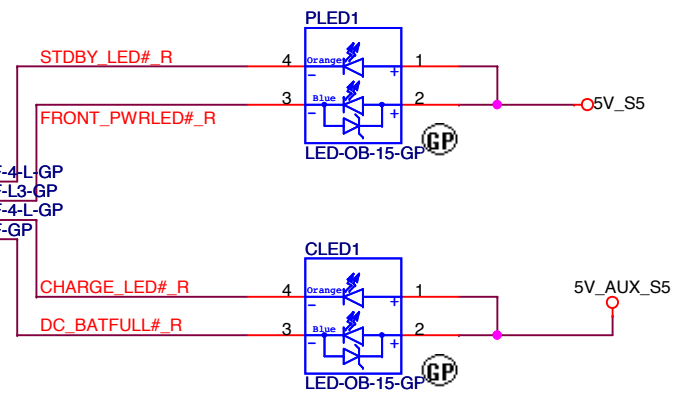
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Reserved		
Size	Document Number	Rev
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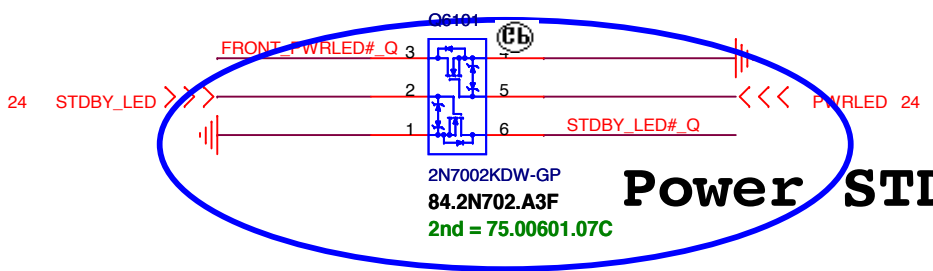
SSID = User.Interface

STDBY_LED#_Q	1	R6101	150R2F-4-L-GP
FRONT_PWRLED#_Q	1	R6102	100R2F-L3-GP
CHARGE_LED#_Q	1	R6103	150R2F-4-L-GP
DC_BATFULL#_Q	1	R6104	249R2F-GP

R6104 change to 249R (64.24905.6DL) , because Energy6 test 20150119 Rock

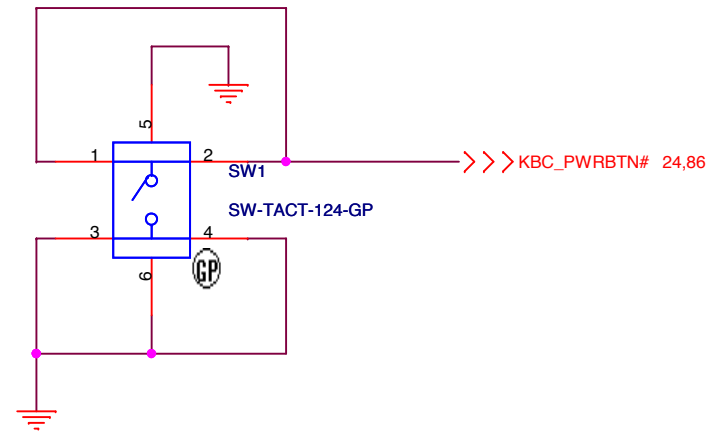


Power button LED

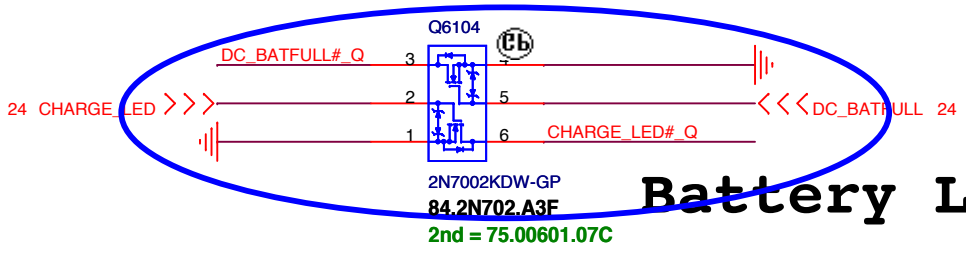


Power STDBY_LED

Delete Q6103, Q6106 , Q6101, Q6104 change to 2N7002KDW-GP 20141224 Rock



Battery LED2 (DC_BATFULL)



Battery LED1 (CHARGE)

Delete Q6103, Q6106 , Q6101, Q6104 change to 2N7002KDW-GP 20141224 Rock

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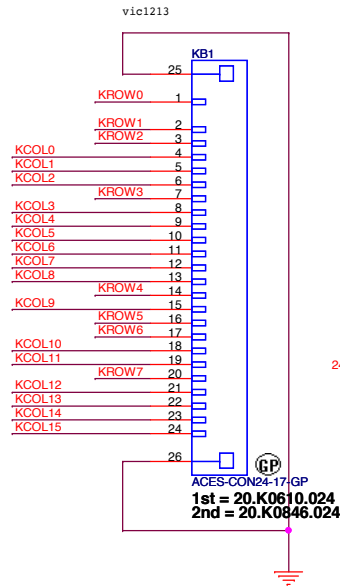
Title		
LED Bard/Power Button		
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SSID = KBC

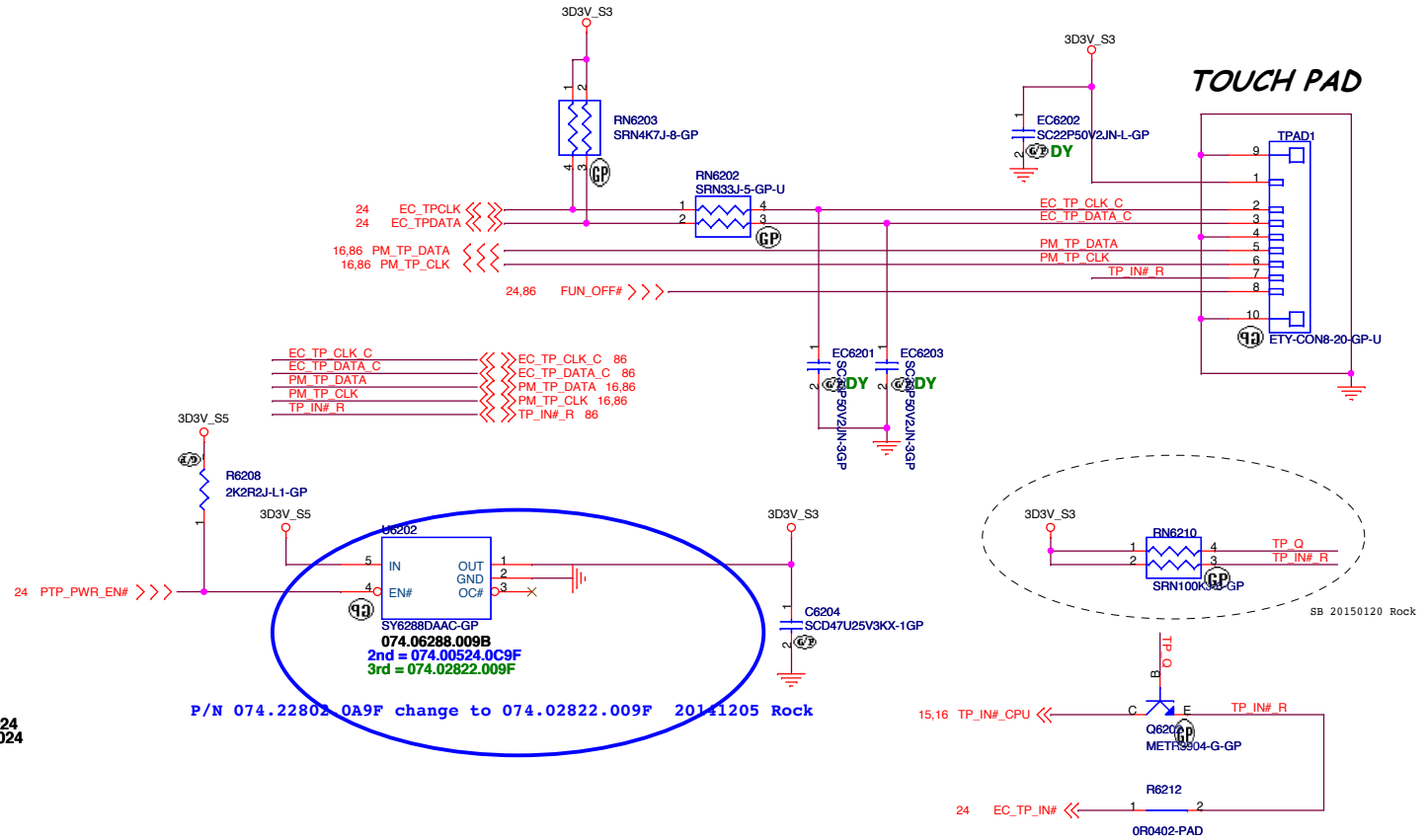
Internal Keyboard Connector

24,86 KROW[0..7] >>>
24,86 KCOL[0..15] >>>



MB PIN DEFINE 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
KB PIN DEFINE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26

26 K/B 1



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Title: **Key Board/Touch Pad**

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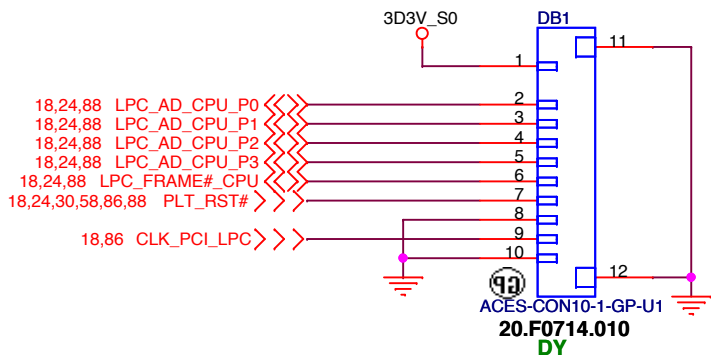
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Title **Hall Sensor**

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Title		
Dubug connector		
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Free Fall Sensor

Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

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SDO="H"; address="3Ah"
***SDO="L"; address="38h"**

***CS="H"; mode="I2C"**
CS="L"; mode="SPI"

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<Variant Name>

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Title

G Sensor

Size
A

Document Number

LAW BA

Rev

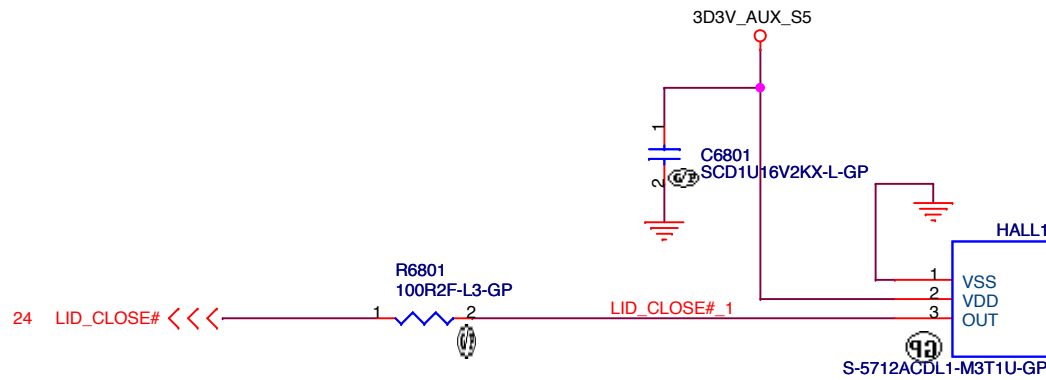
-1

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<Variant Name>

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Title

Thunderbolt (2/5)

Size

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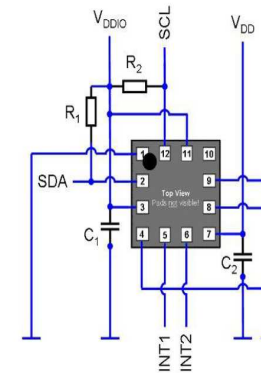
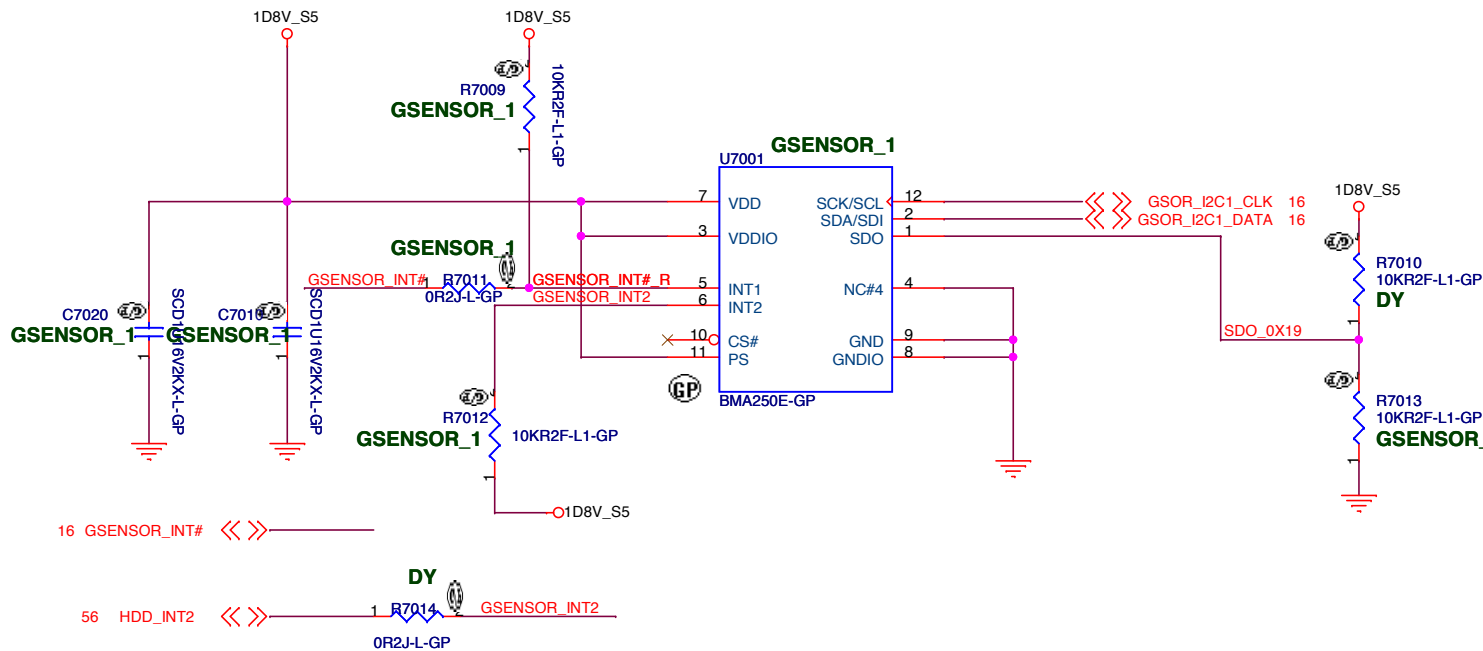
SSID = User.Interface

G Sensor

Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of the mass of the NB as possible as you can

The default I²C address of the device is 0011000b (0x18). It is used if the SDO pin is pulled to 'GND'. The alternative address 0011001b (0x19) is selected by pulling the SDO pin to 'V_{DDIO}'.



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Title		
GSENSOR		
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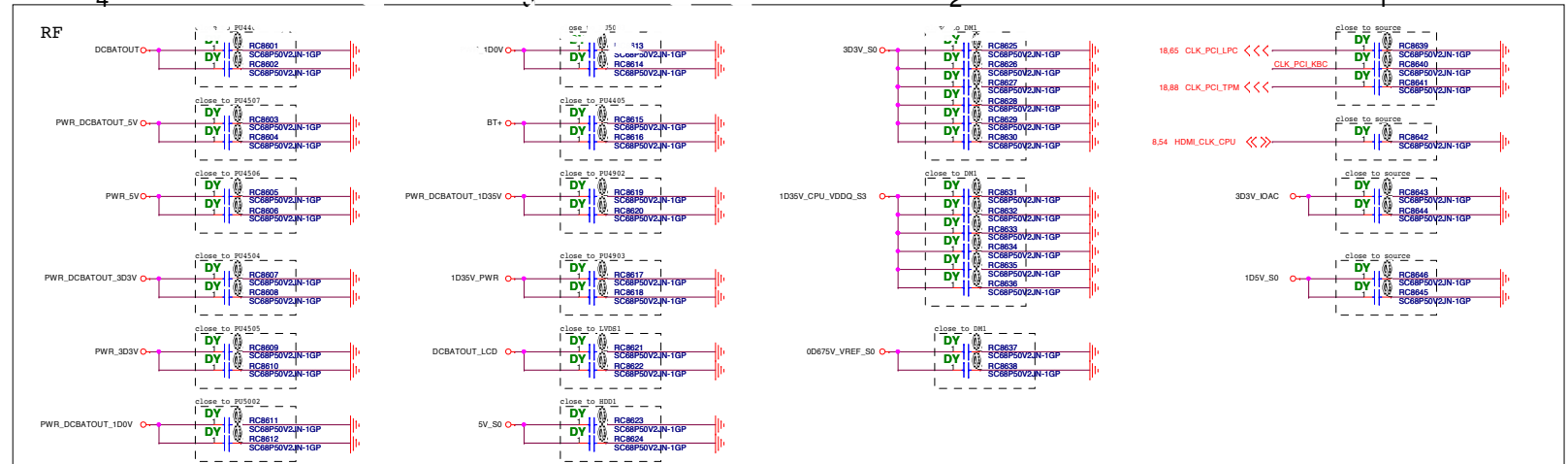
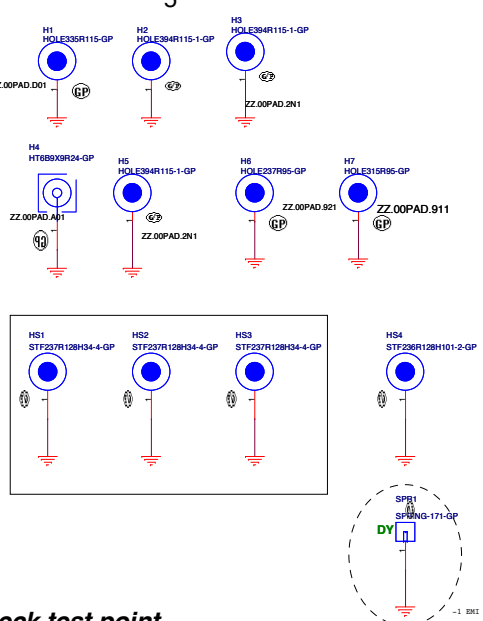
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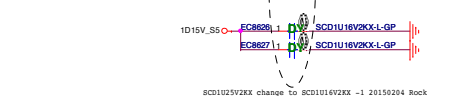
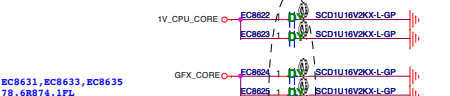
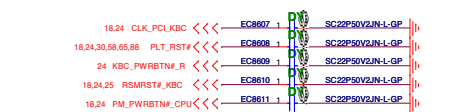
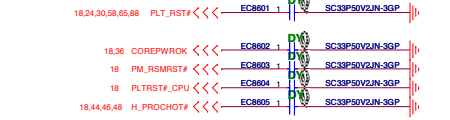
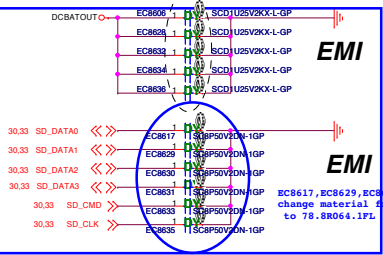
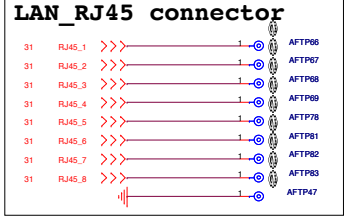
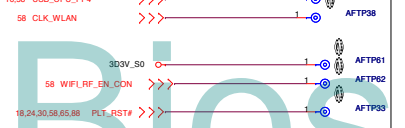
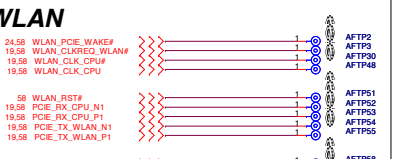
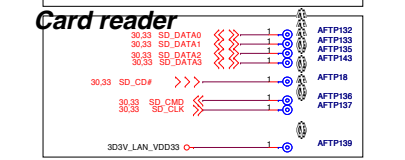
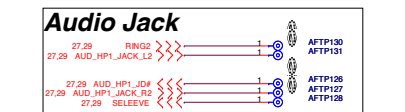
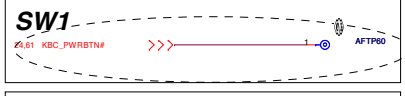
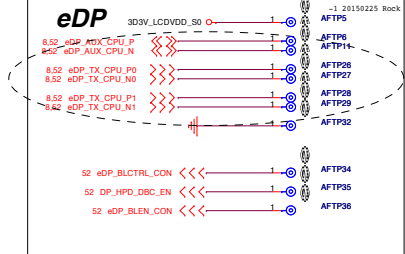
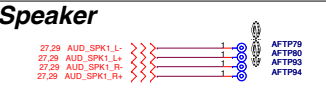
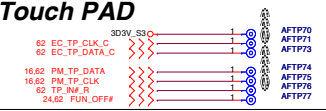
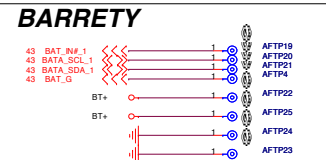
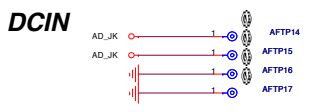
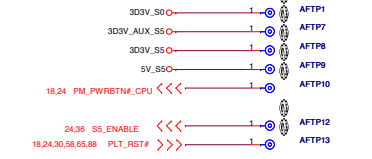
Title		
Switchable GFX LCD(2/2)		
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Check test point

Test Point放在 Bottom side 可量測處



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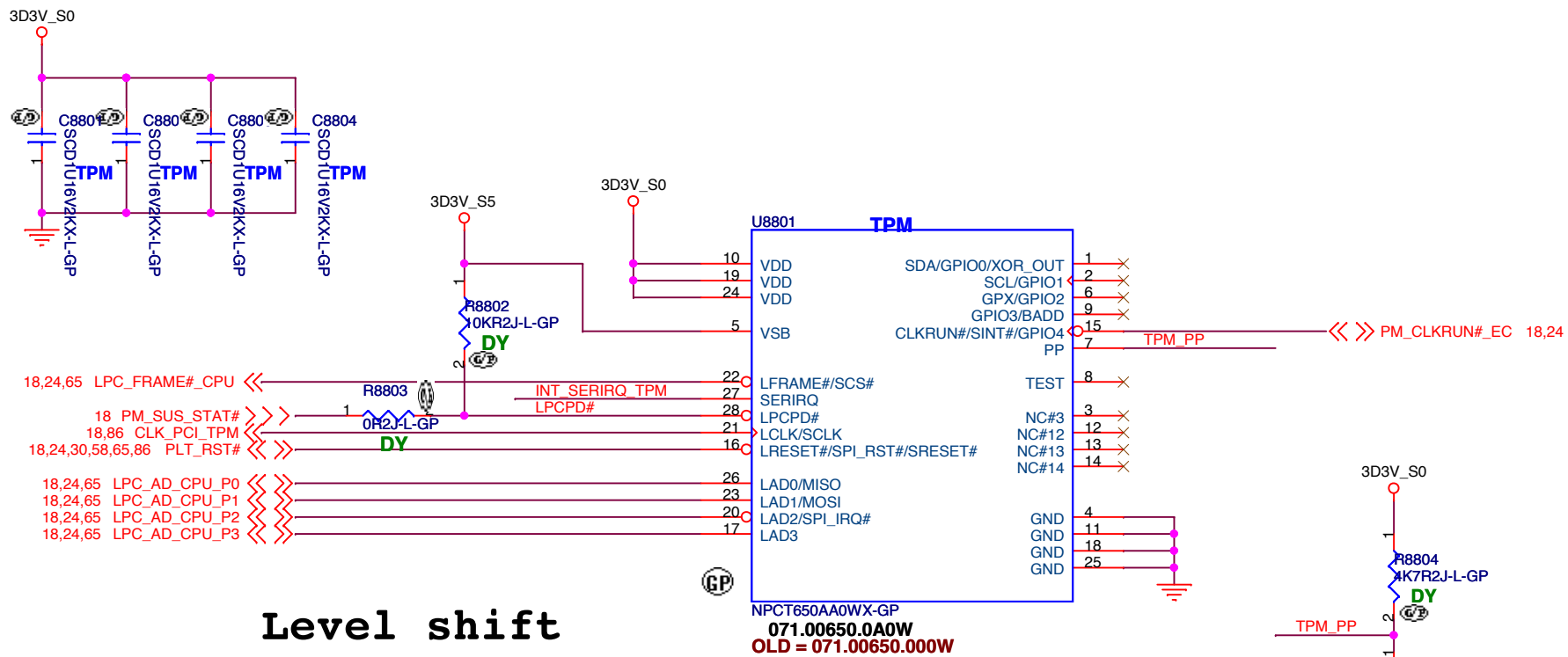
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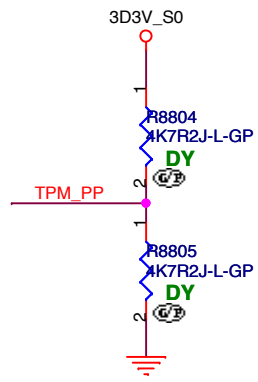
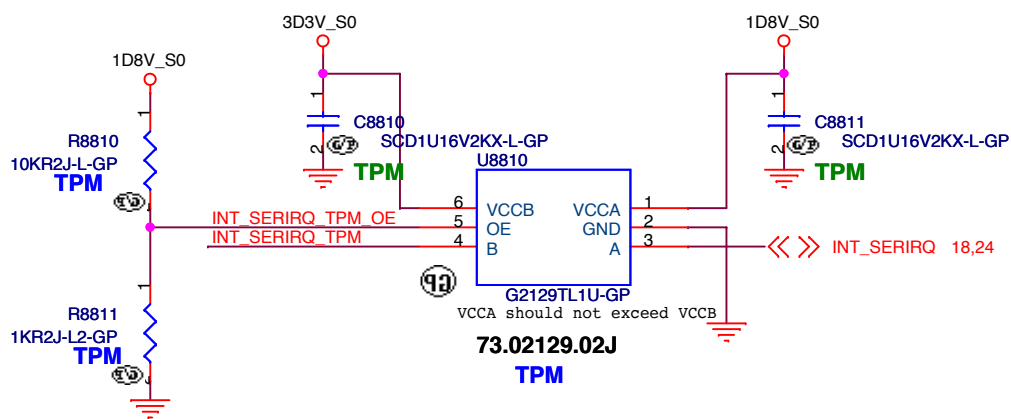
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Level shift



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SSID = Finger Print

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SSID = Express Card

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SSID = Smart Card

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SSID = Docking

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SSID = Intel LAN

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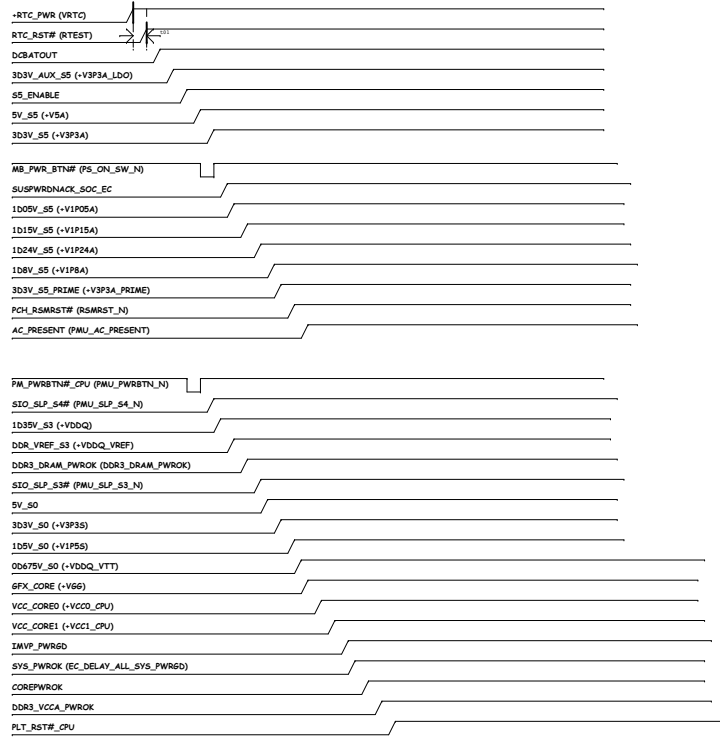
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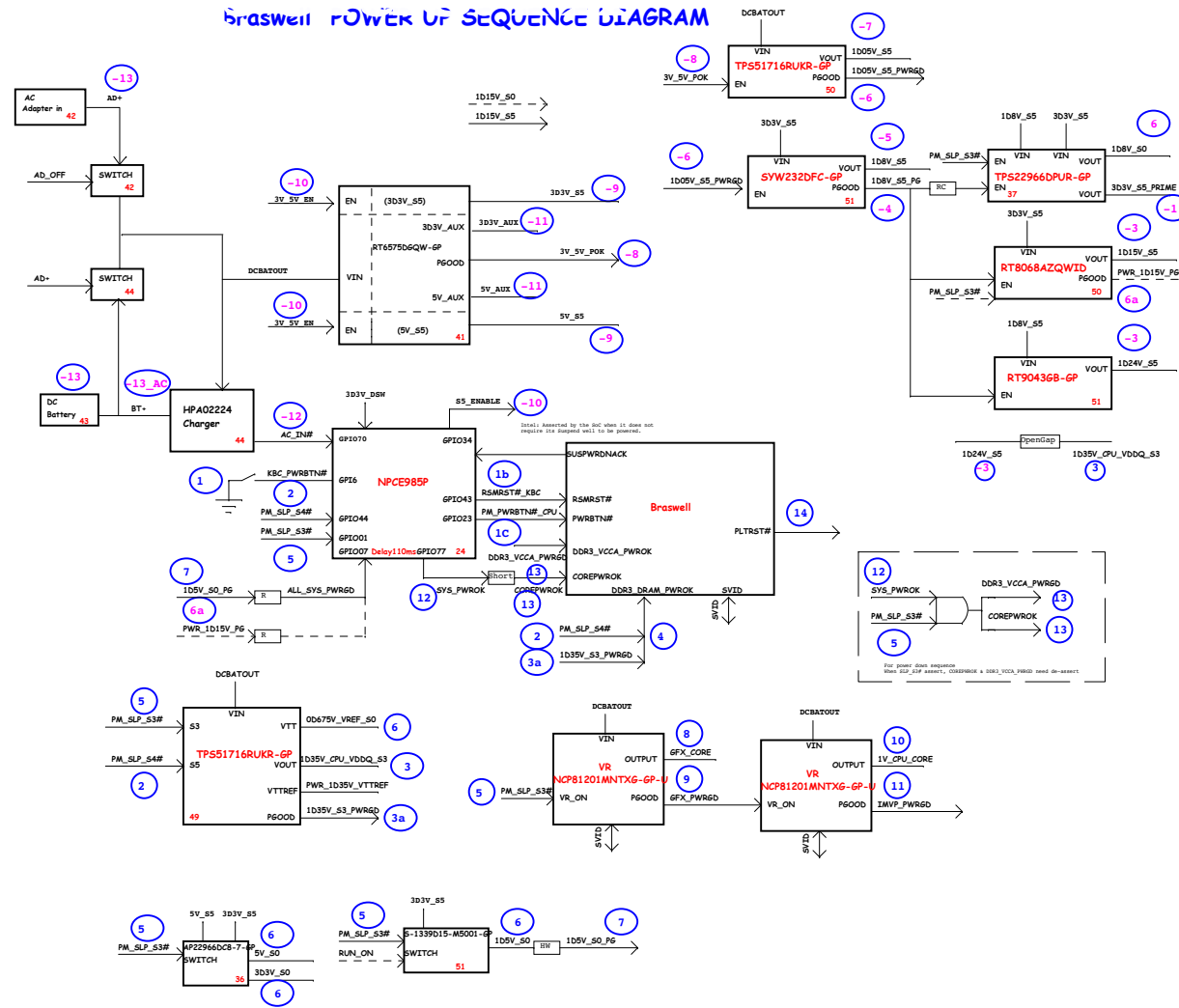
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Change History		
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Intel-Power Up Sequence

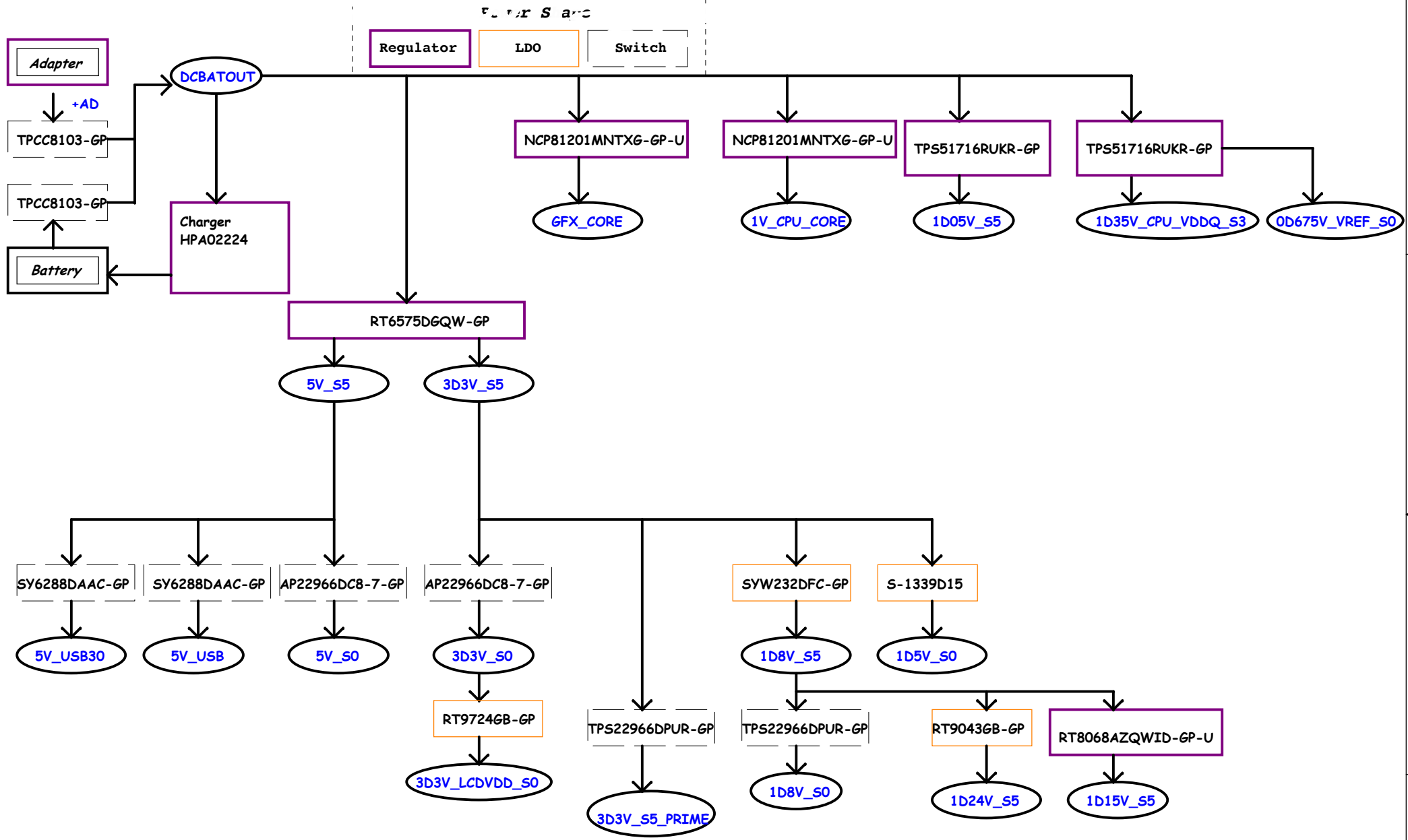
(AC mode)



Braswell POWER UP SEQUENCE DIAGRAM



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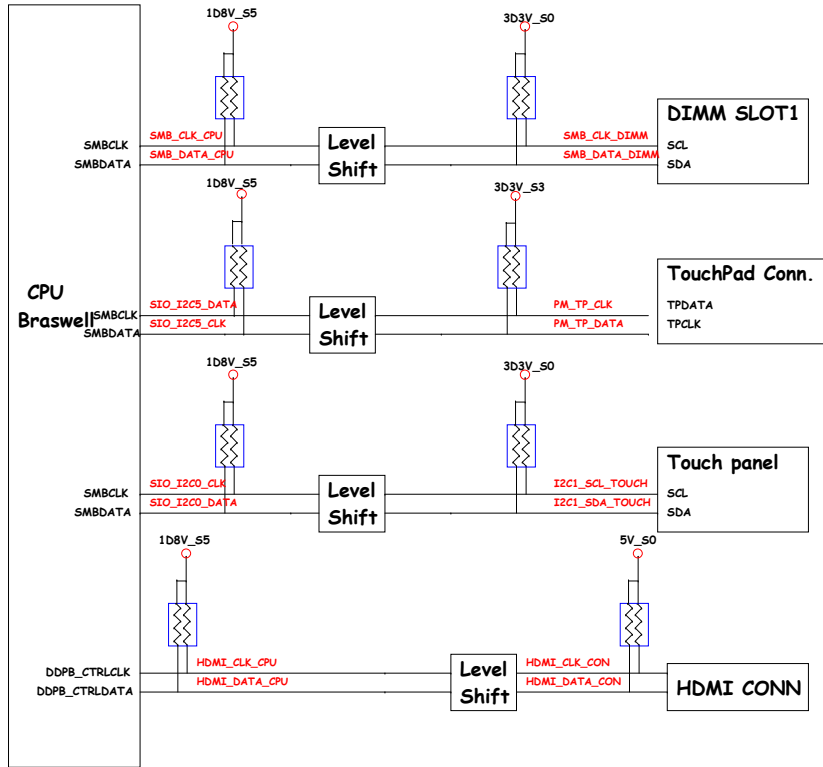


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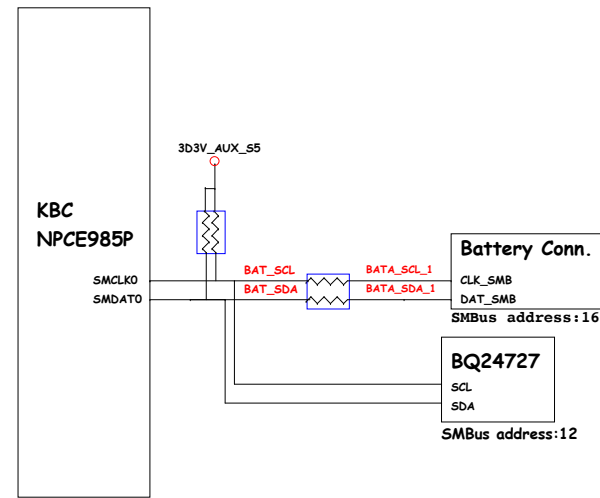
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Power Block Diagram	
Title Size A3 Date: Monday, March 16, 2015	Document Number LAW BA Sheet 100 of 102
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PCH SMBus Block Diagram



KBC SMBus Block Diagram

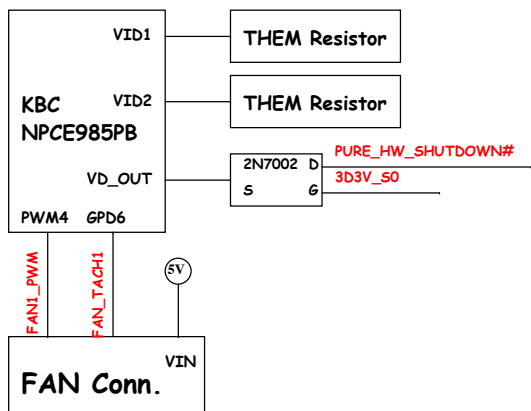


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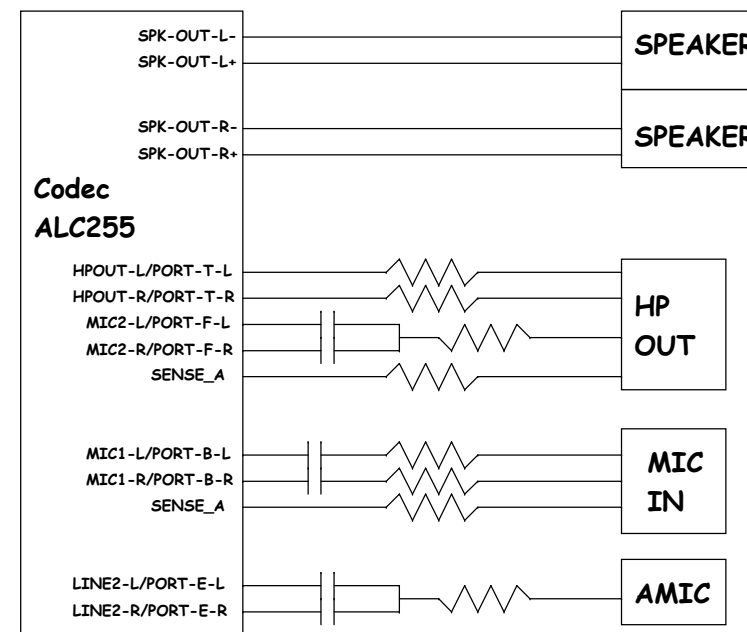
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Thermal Block Diagram



Audio Block Diagram



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Title THERMAL/AUDIO BLOCK DIAGRAM			
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