

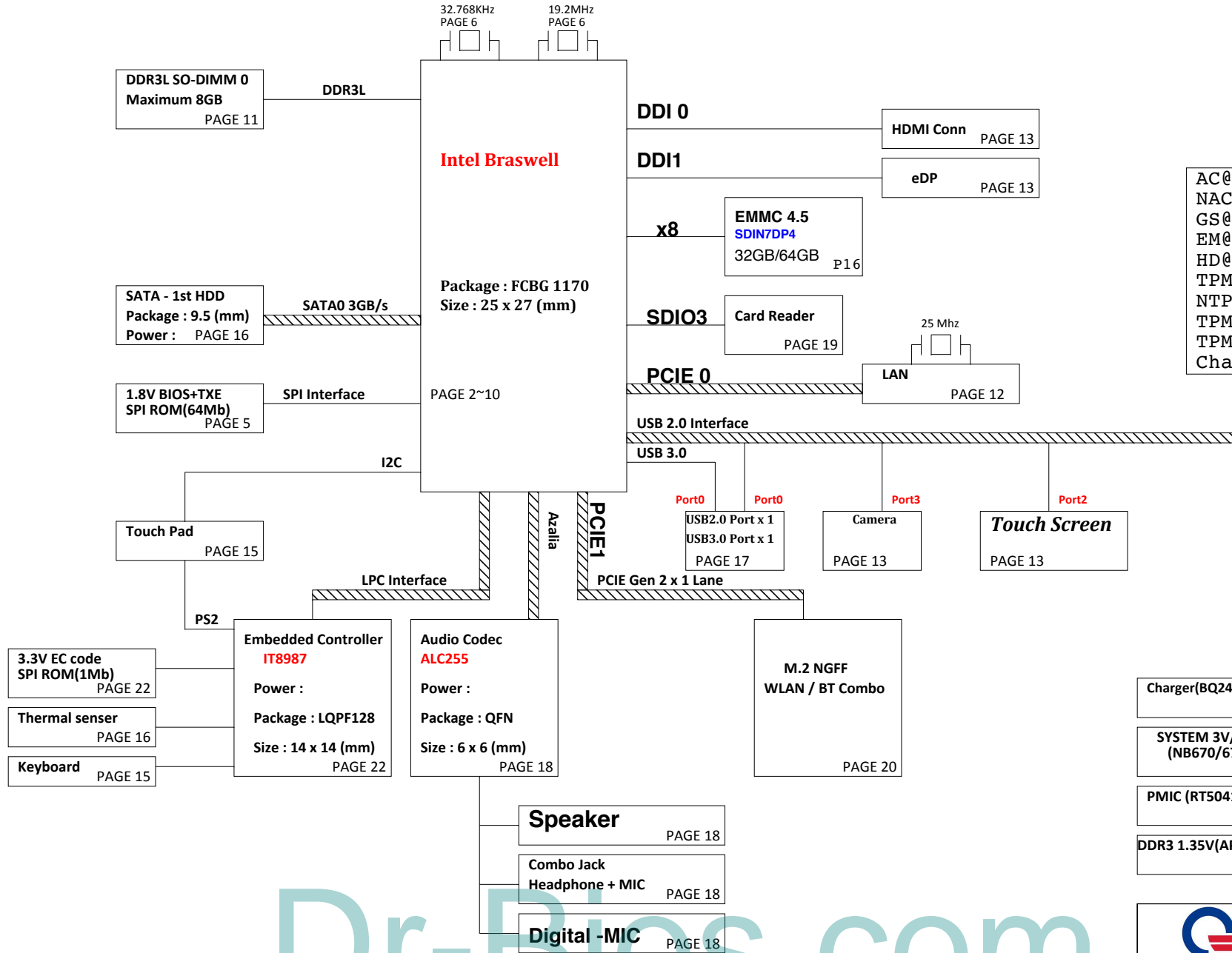
ZHKD UMA(11.6")

Intel Braswell Platform Block Diagram

PCB 6L STACK UP

LAYER 1 : TOP
 LAYER 2 : SGND
 LAYER 3 : IN1(High)
 LAYER 4 : IN2
 LAYER 5 : SVCC
 LAYER 6 : BOT

AC@ : IOAC
 NAC@ : Non-IOAC
 GS@ : G sensor
 EM@ : eMMC
 HD@ : HDD
 TPM@ : TPM
 NTPM@ : Non-TPM
 TPM_I@ : 英飛凌
 TPM_N@ : 新唐
 Change CPU & EMMC P/N



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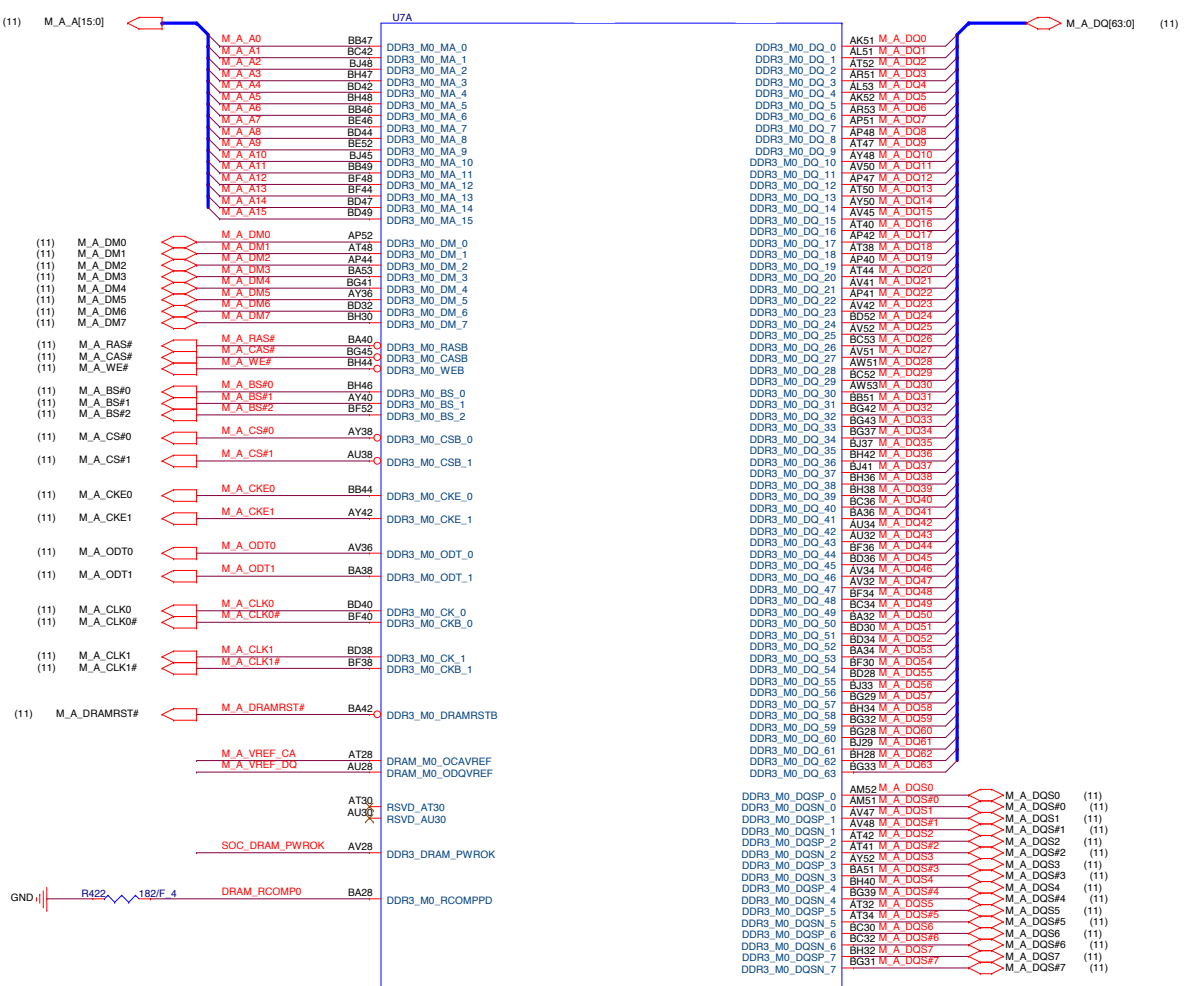
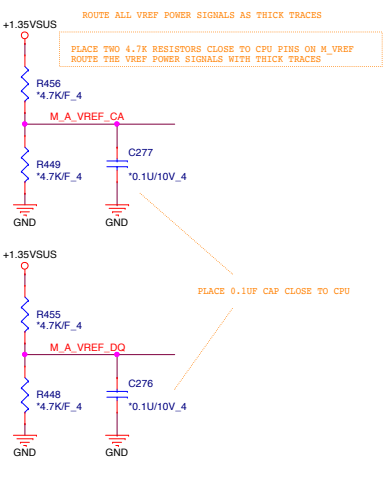
Charger(BQ24737RGR)	VCC0+1 (RT8171BGQW)
SYSTEM 3V/5V (NB670/671)	+VGG (RT8171BGQW)
PMIC (RT5041AGQW)	Thermal / Discharge
DDR3 1.35V(APW8819)	

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Size Document Number Rev 1A
Intel Block Diagram

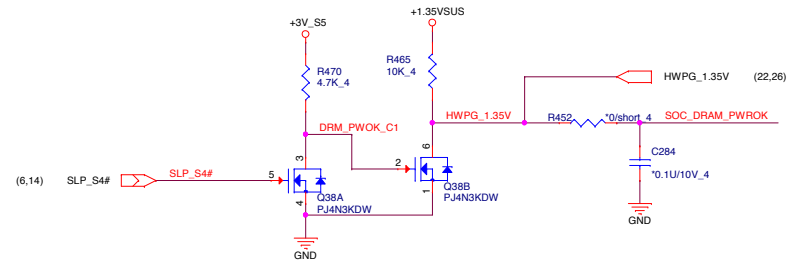
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+1.35VSUS (3,9,11,26)
+3V_S5 (3,5,9,12,14,15,16,19,22,25)



Channel 0	Channel 1	SOC Supported Memory Operation Speed
1333 MHz	X	1066 MHz
1600 MHz	X	1600 MHz
1333 MHz	1333 MHz	1066 MHz
1600 MHz	1600 MHz	1600 MHz

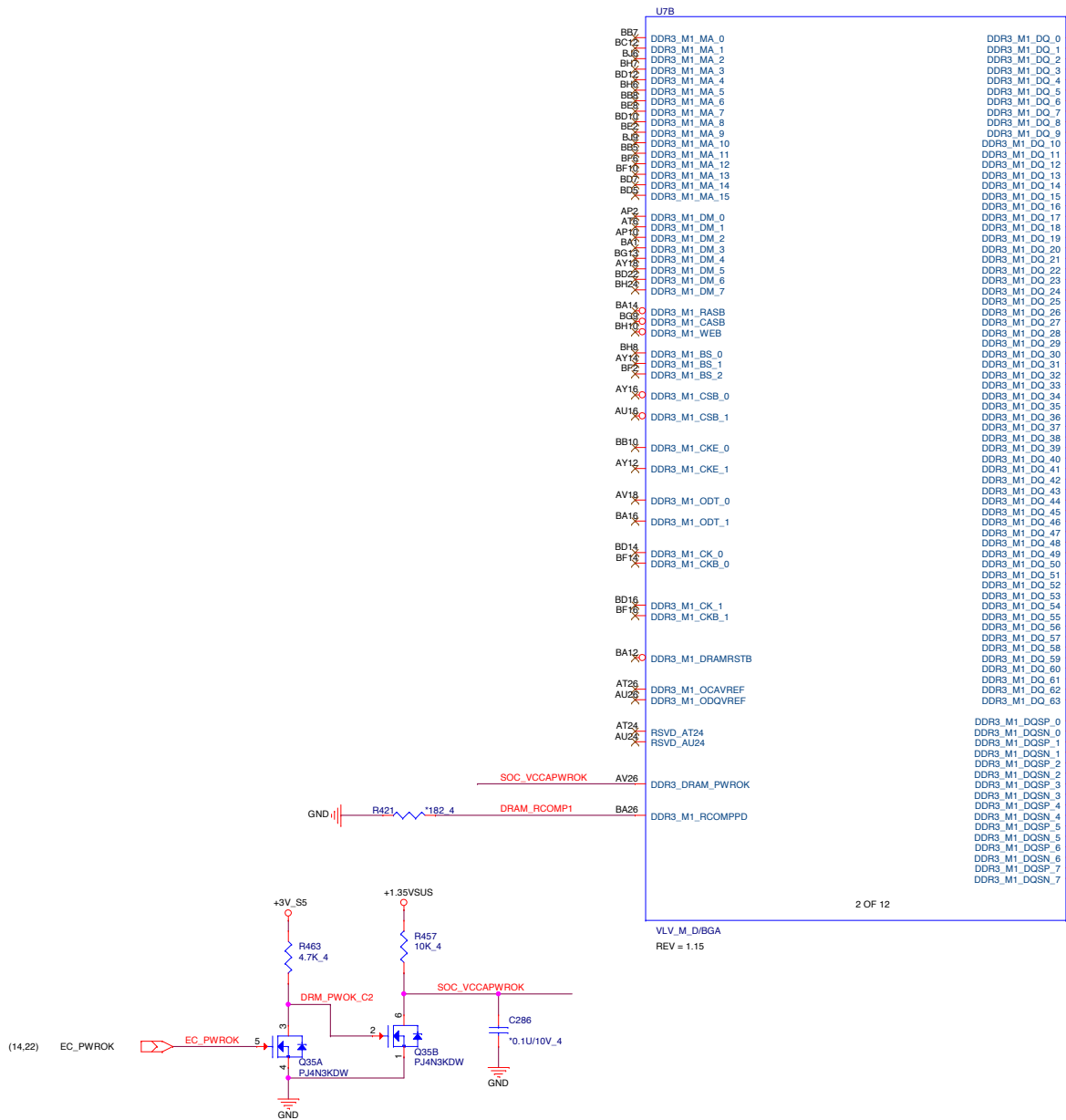
Channel 0 need to be populated first for the platform to power on



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	Valley 1/9 (DDR4)	1A

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U7B

BB7	DDR3_M1_MA_0	AK3
BC12	DDR3_M1_MA_1	AK3
B16	DDR3_M1_MA_2	AK2
BH7	DDR3_M1_MA_3	AK3
BD12	DDR3_M1_MA_4	AK1
BH6	DDR3_M1_MA_5	AK2
BB8	DDR3_M1_MA_6	AK1
BB8	DDR3_M1_MA_7	AK3
BD10	DDR3_M1_MA_8	AK6
BD5	DDR3_M1_MA_9	AK7
B15	DDR3_M1_MA_10	AK6
BB5	DDR3_M1_MA_11	AK4
BF8	DDR3_M1_MA_12	AK7
BF10	DDR3_M1_MA_13	AK4
BD7	DDR3_M1_MA_14	AK4
BD2	DDR3_M1_MA_15	AK9
BD5	DDR3_M1_MA_16	AK14
AP2	DDR3_M1_DM_0	AK12
AT6	DDR3_M1_DM_1	AK16
AP10	DDR3_M1_DM_2	AK18
BA1	DDR3_M1_DM_3	AK10
BG13	DDR3_M1_DM_4	AK13
AY18	DDR3_M1_DM_5	AK13
BD22	DDR3_M1_DM_6	AK12
BH24	DDR3_M1_DM_7	AK2
BA14	DDR3_M1_RASB	AK2
BH10	DDR3_M1_CASB	AK1
BH10	DDR3_M1_WEB	AK3
BH6	DDR3_M1_BS_0	AK2
AY18	DDR3_M1_BS_1	AK1
BF2	DDR3_M1_BS_2	AK3
AY16	DDR3_M1_CSB_0	AK12
AU16	DDR3_M1_CSB_1	AK13
BB10	DDR3_M1_CKE_0	AK18
AY18	DDR3_M1_CKE_1	AK18
AV18	DDR3_M1_ODT_0	AK18
BA16	DDR3_M1_ODT_1	AK20
BD14	DDR3_M1_CK_0	AK22
BF16	DDR3_M1_CKB_0	AK24
BD16	DDR3_M1_CK_1	AK20
BF16	DDR3_M1_CKB_1	AK24
BA12	DDR3_M1_DRAMRSTB	AK21
AT26	DDR3_M1_OCAVREF	AK25
AU26	DDR3_M1_ODQVREF	AK26
AT24	RSVD_AT24	AK21
AU24	RSVD_AU24	AK3
	DDR3_M1_DOSP_0	AK7
	DDR3_M1_DOSP_1	AK6
	DDR3_M1_DOSP_2	AK12
	DDR3_M1_DOSP_3	AK13
	DDR3_M1_DOSP_4	AK2
	DDR3_M1_DOSP_5	AK3
	DDR3_M1_DOSP_6	AK14
	DDR3_M1_DOSP_7	AK22
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	DDR3_M1_DOSP_9	AK24
	DDR3_M1_DOSP_10	AK22
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	DDR3_M1_DOSP_100	AK22

VLV_M_D/BGA
REV = 1.15

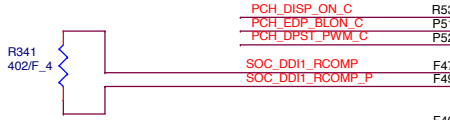
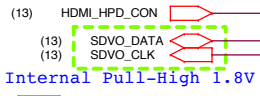
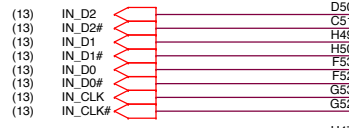
Quanta Computer Inc.
PROJECT : ZHKD

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	Valley 2/9 (DDR)	1A
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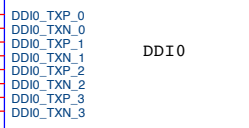
(7,9,11,12,13,14,15,16,17,18,19,20,22,24,26,27,28,29) +3V

U7C

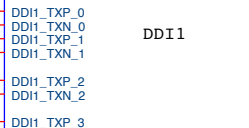
HDMI



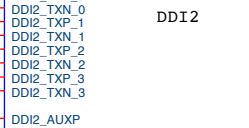
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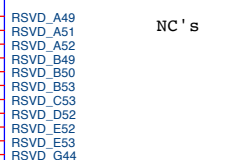
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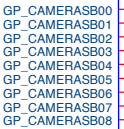
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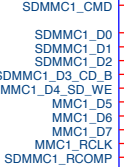
NC 's



MCSI and Camera interface



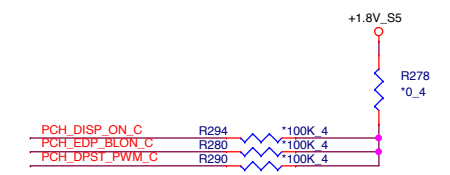
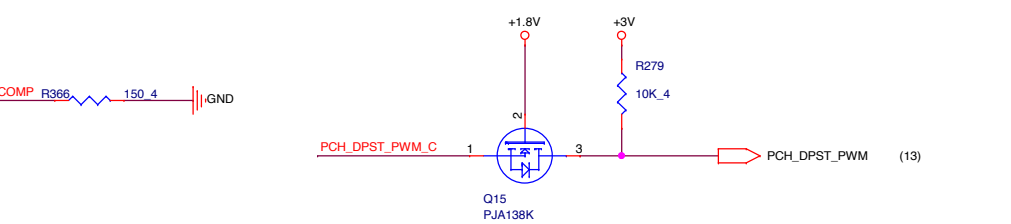
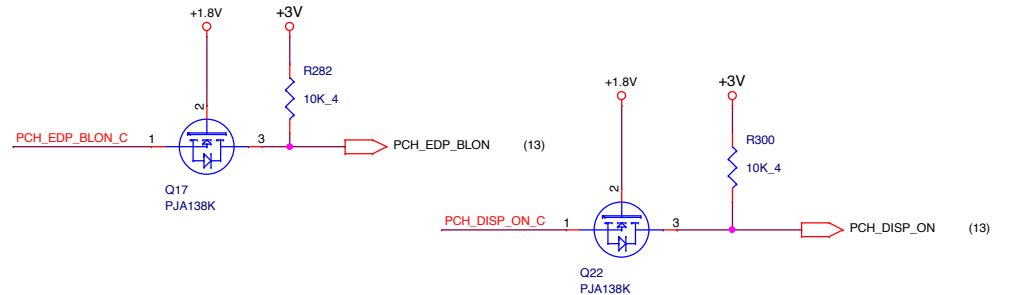
SDMMC1



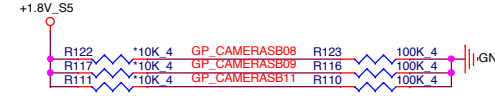
SDMMC2



SDMMC3



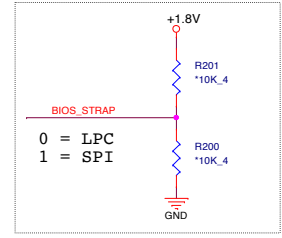
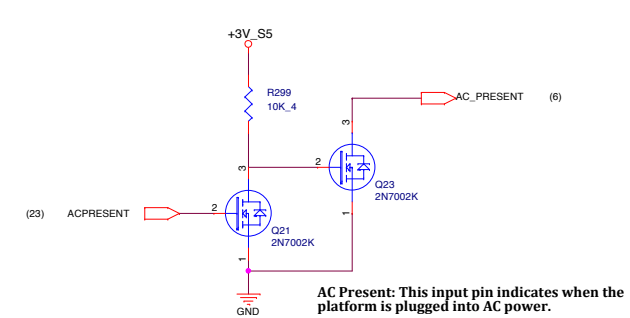
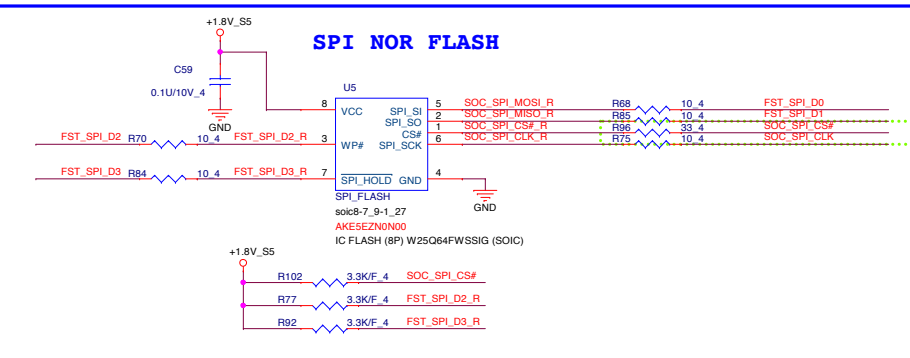
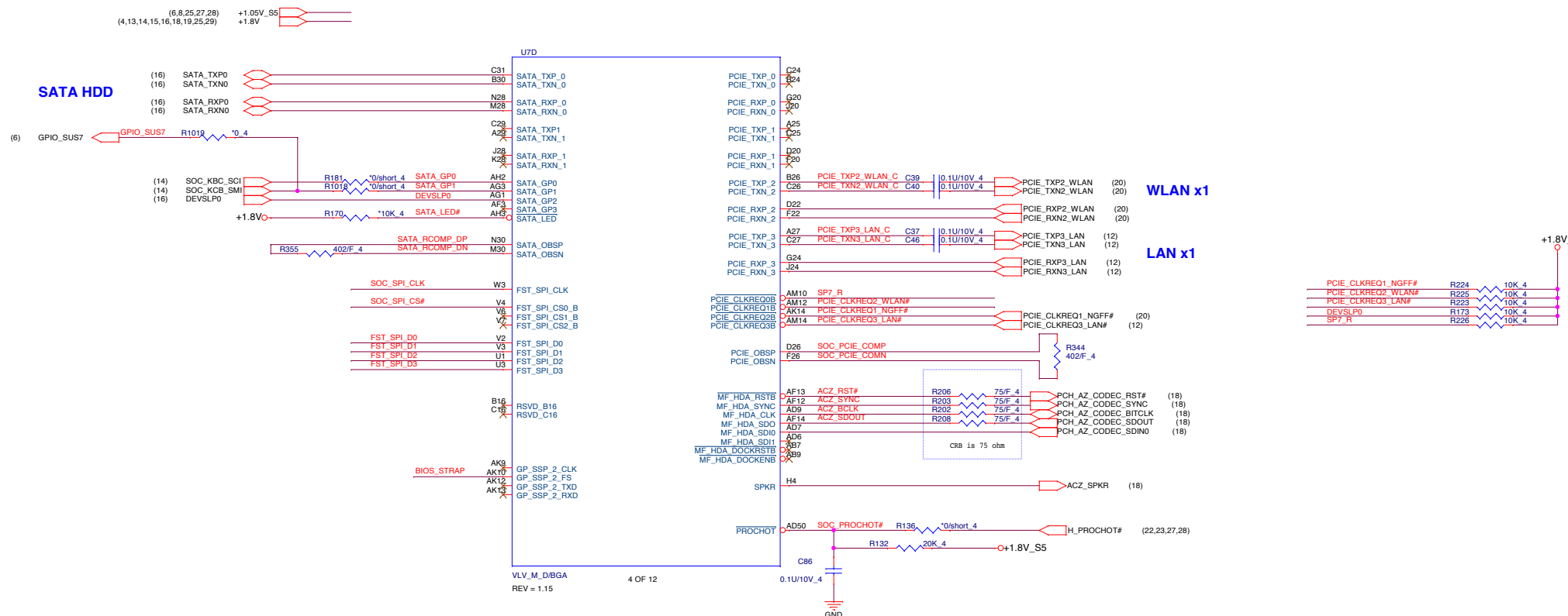
Hardware Strap table with columns: Hardware Strap, Strap Description. Rows include GP_CAMERA08, GP_CAMERA09, GP_CAMERA11.



VLV_M_D/BGA REV = 1.15

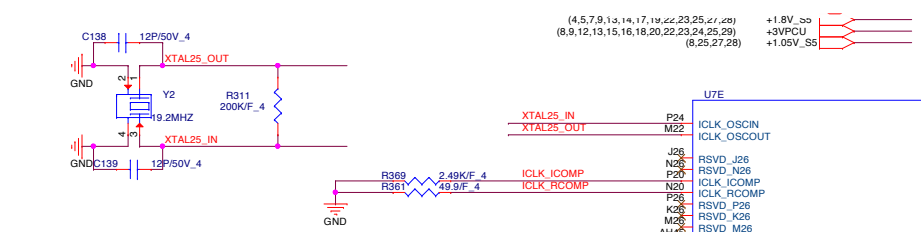
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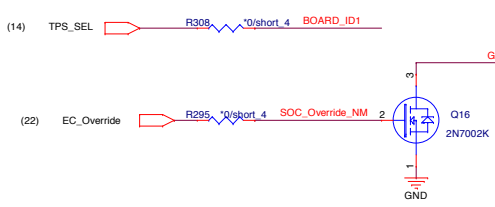
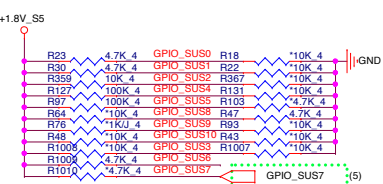
Quanta Computer Inc.
PROJECT : ZHRD
Valley 4/9 (SD/PCIE/SATA)

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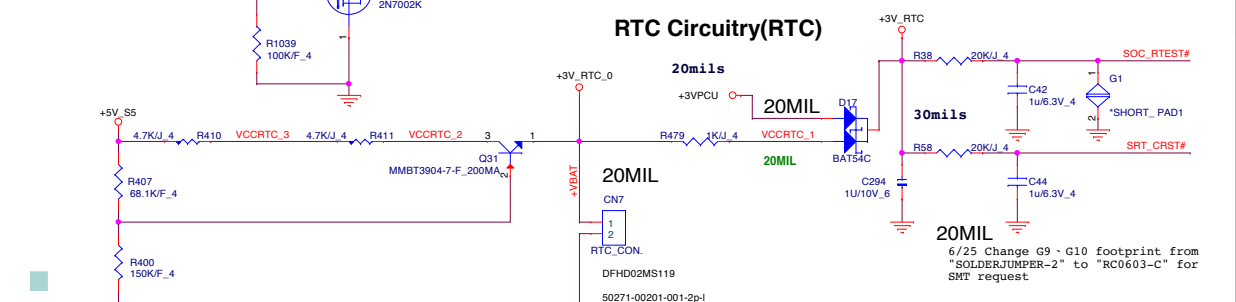
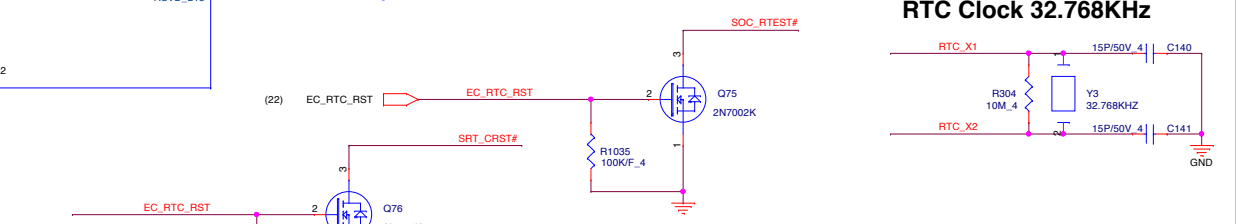
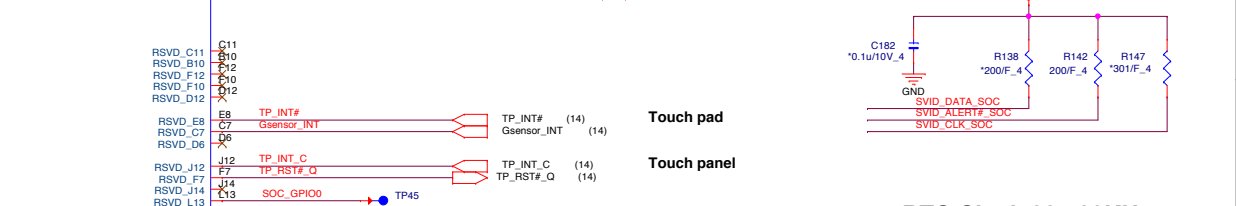
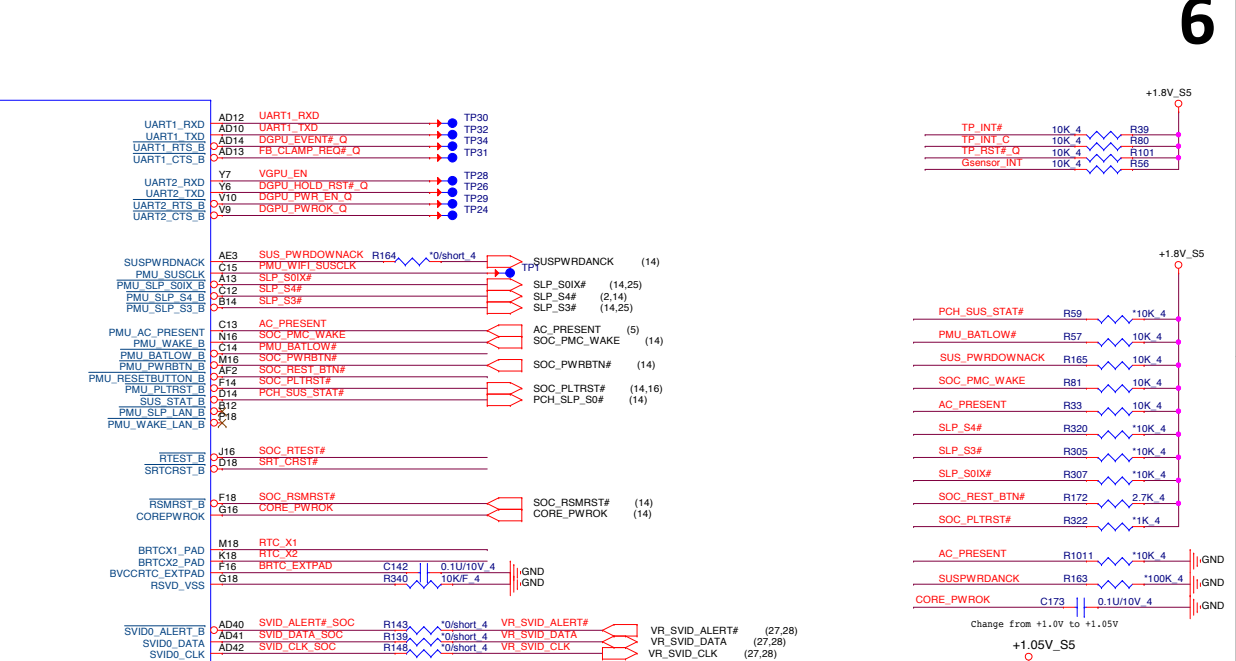
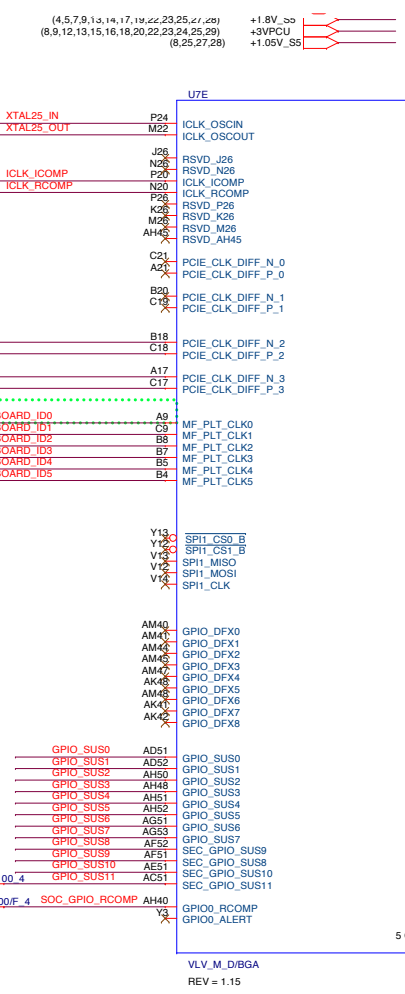
NGFF
WLAN
LAN

Hardware Strap	Strap Description
GPIO_SUS[0]	0 = DD10 not detected 1 = DD10 detected
GPIO_SUS[1]	0 = DD11 not detected 1 = DD11 detected
GPIO_SUS[2]	Top Swap(A15 Override) 0 = Change Boot Loader address 1 = Normal Operation
GPIO_SUS[4]	BIOS Boot Selection 0 = No SPI 1 = SPI
GPIO_SUS[5]	Security Flash Descriptors 0 = Override 1 = Normal Operation
GPIO_SUS[8]	ICLK_USB 2.0,DD1 SFR supply select 0 = Supply is 1.25V 1 = Supply is 1.25V
GPIO_SUS[9]	ICLK_USB 2.0,DD1 SFR Bypass 0 = No bypass 1 = Bypass with 1.05V (internal PU)
GPIO_SUS[10]	FSM Select 0 = Fuse controller 1 = PMC (internal PU)



BOARD ID

BOARD_ID0 : "H" W/ G-Sensor; "Low" W/O G-Sensor
 BOARD_ID1 : "H" W/ touch panel; "Low" W/O touch panel
 BOARD_ID2 : "H" is UMA ; "Low" is Dis
 BOARD_ID3 : TPM; HIGH=TPM; LOW=W/O TPM
 BOARD_ID4 : "Low" is for ZHKD,MB ID
 BOARD_ID5 : IOAC; High=IOAC,Low=non-IOAC

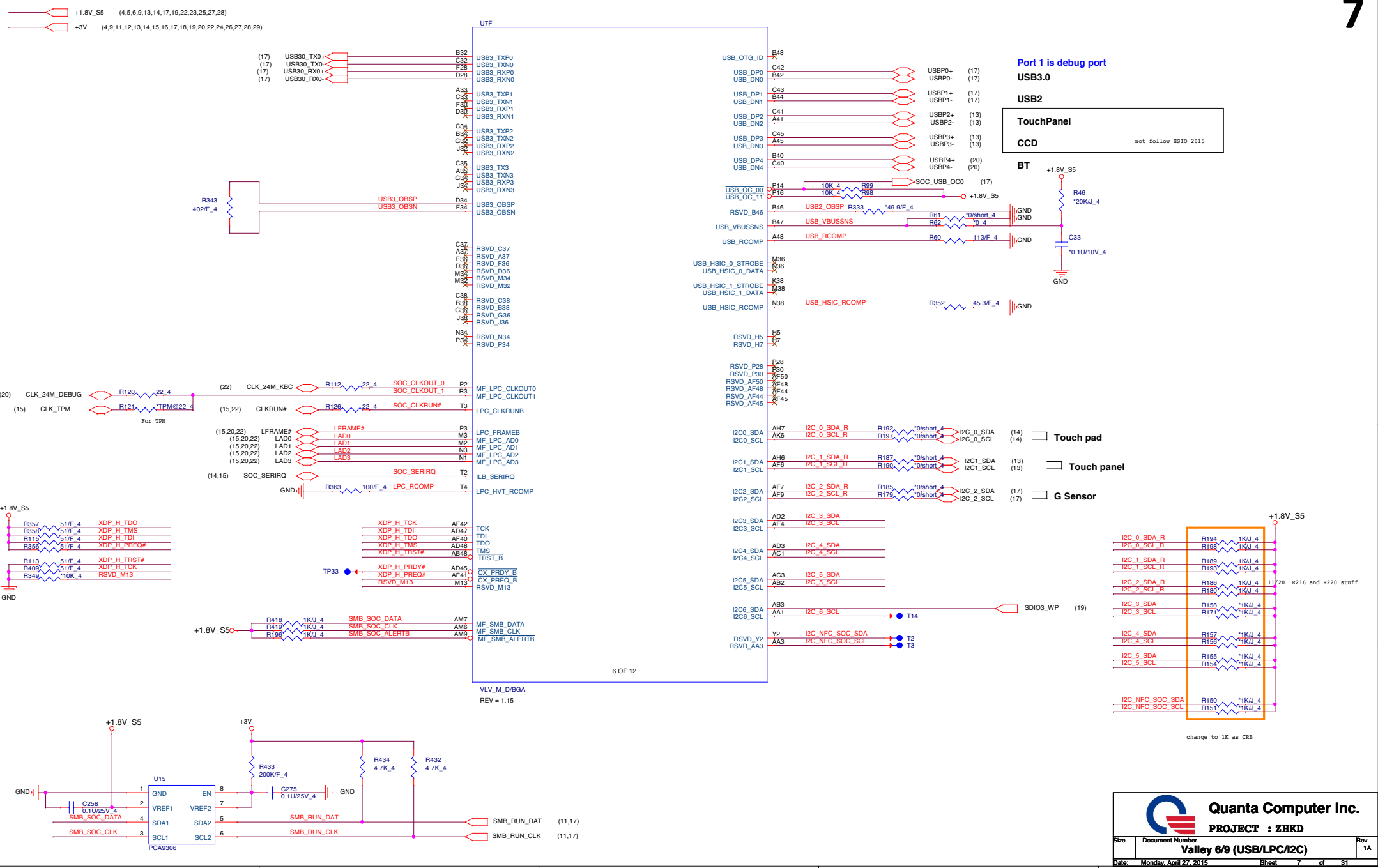


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PROJECT : ZHKD

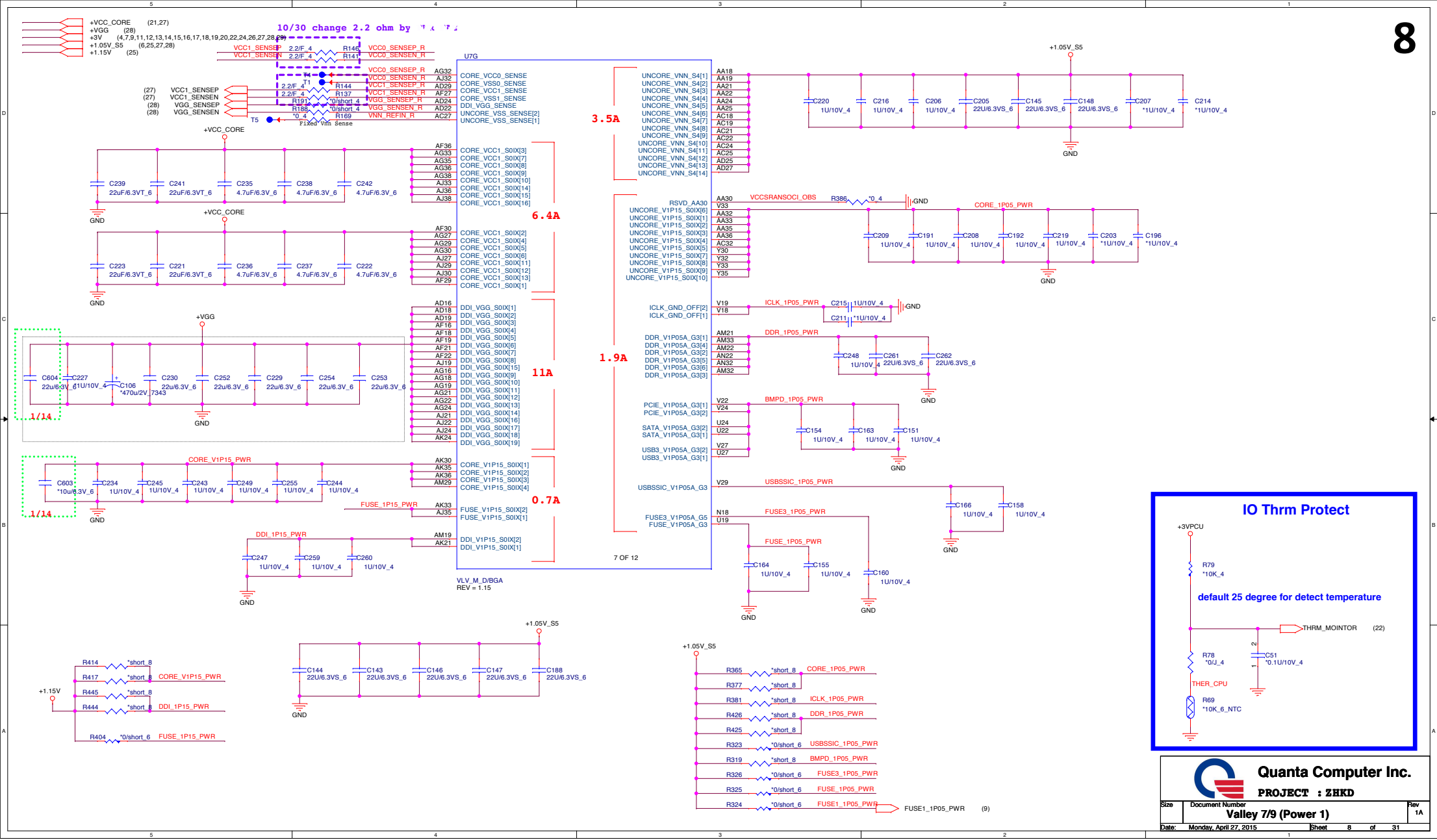
Size	Document Number	Rev
	Valley 5/9 (SPI/GPIO/CLK)	1A

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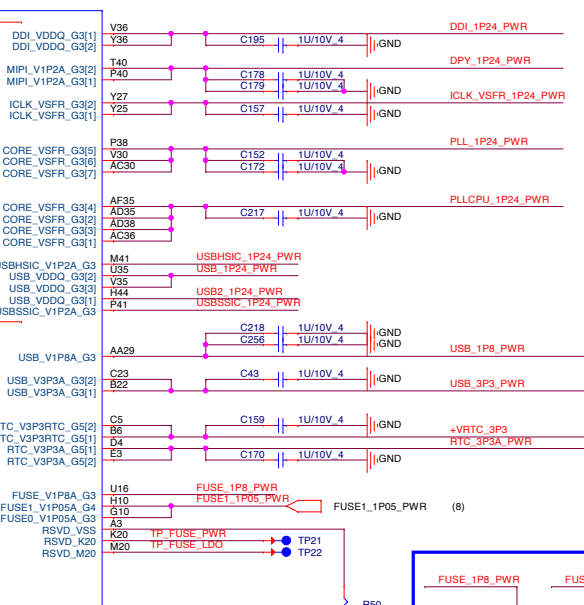
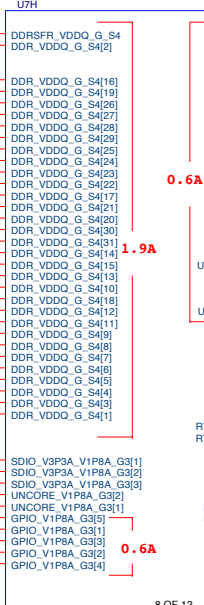
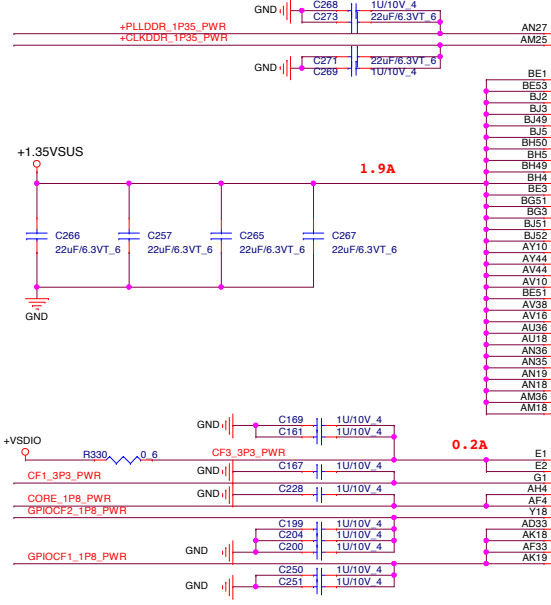


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PROJECT : ZHRD
Valley 6/9 (USB/LPC/I2C)

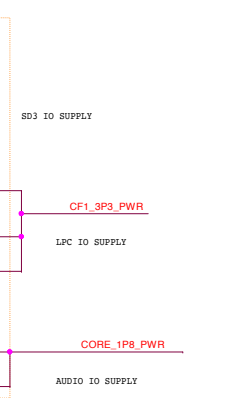
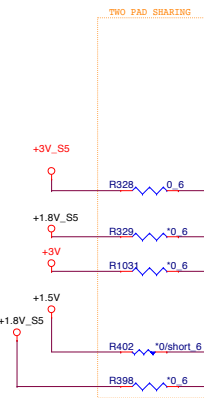
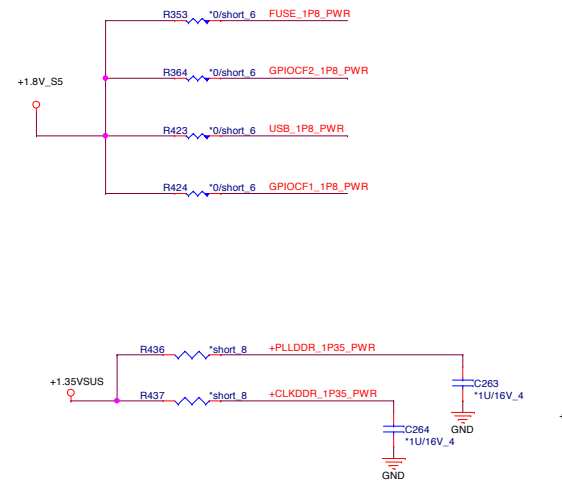
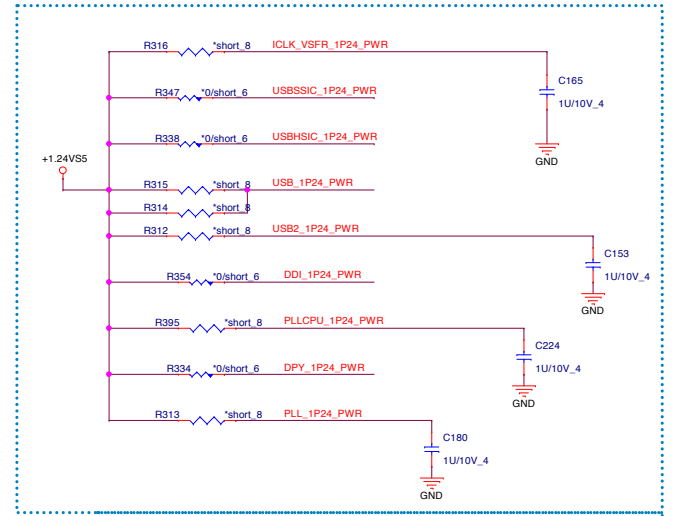
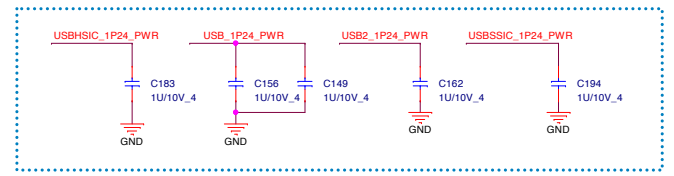
Size	Document Number	Rev
		1A
Date:	Monday, April 27, 2015	Sheet 7 of 31



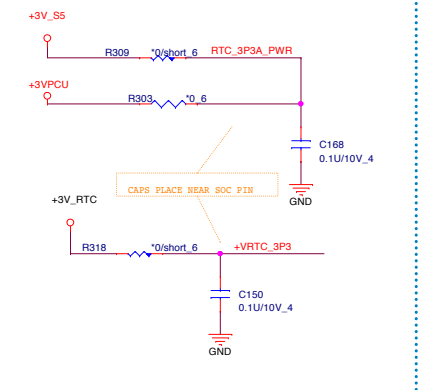
+1.35VSUS (2,3,11,26)
 +3V_RTC (6,29)
 +3V_S5 (2,3,5,12,14,15,16,19,22,25)
 +3VPCU (6,8,12,13,15,16,18,20,22,23,24,25,29)



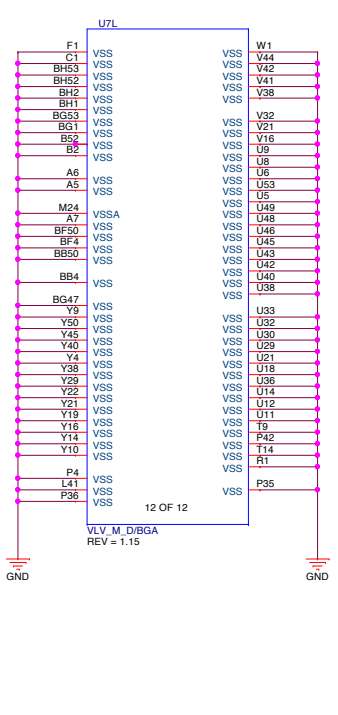
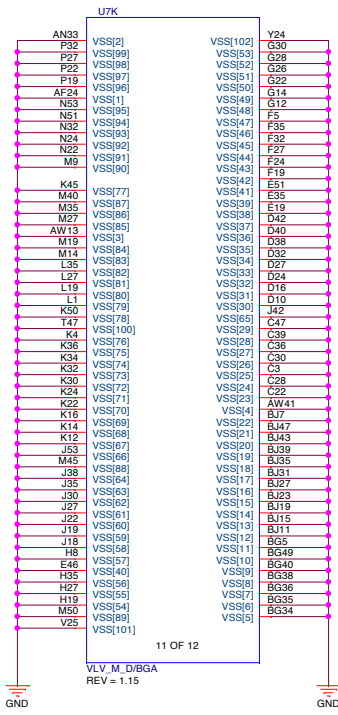
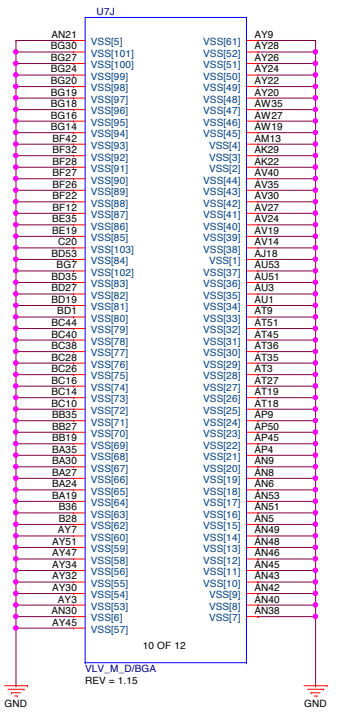
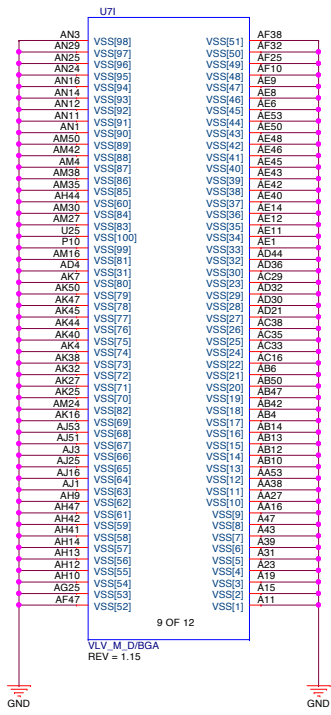
PLACE THE CAPS UNDER THE PKG SHADOW



VSDIO VOLTAGE SETTING (CF3_3P3_PWR)	
SDMMC3_PWR_EN_N	

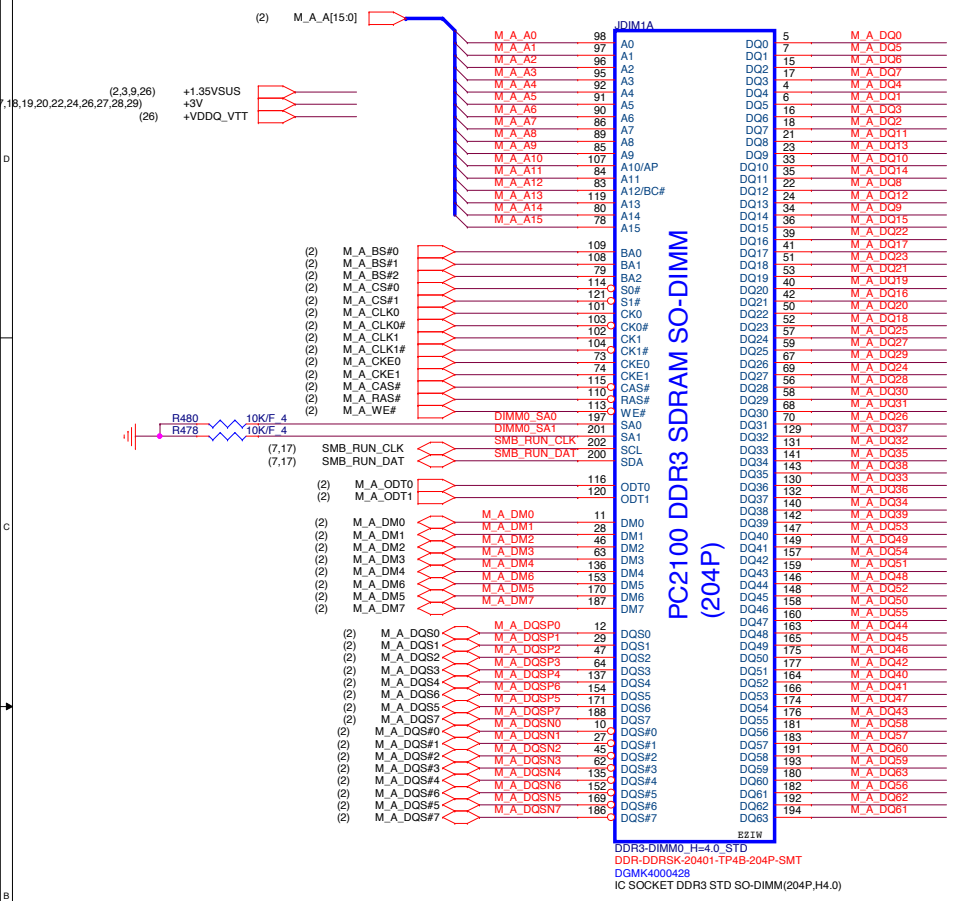


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PROJECT : ZHRD
 Size: _____ Document Number: _____ Rev: 1A
Valley 8/9 (Power 2)
 Date: Monday, April 27, 2015 Sheet 9 of 31

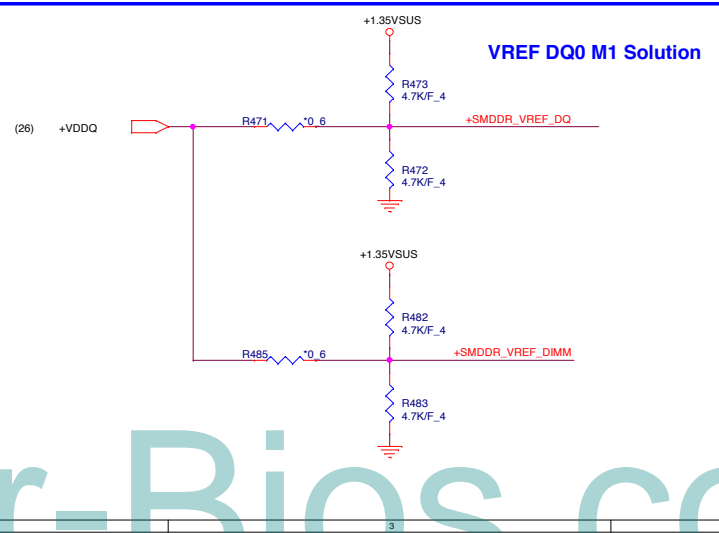
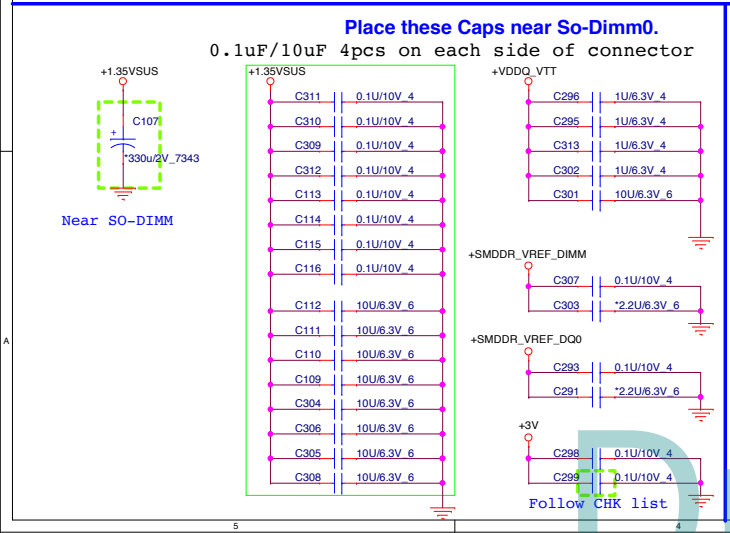
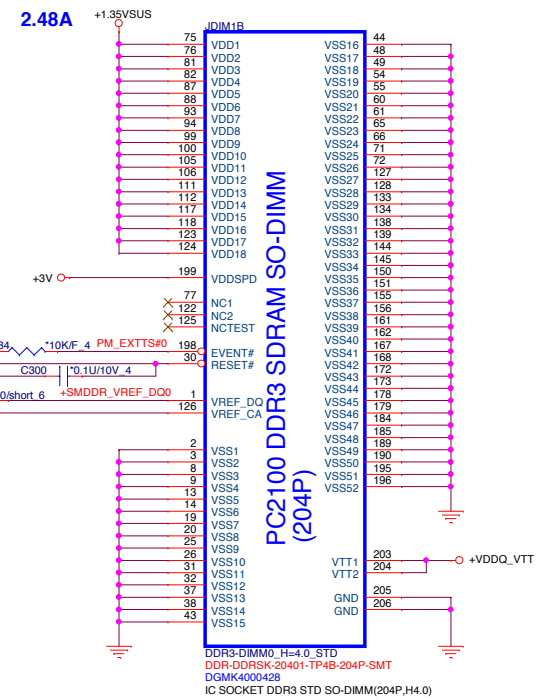


Quanta Computer Inc.
PROJECT : ZHKD

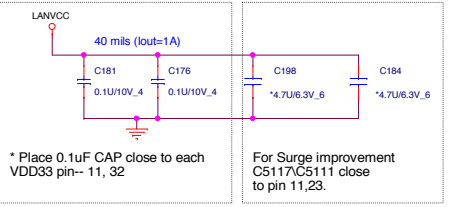
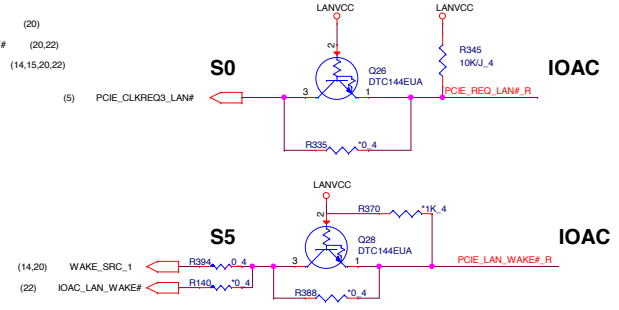
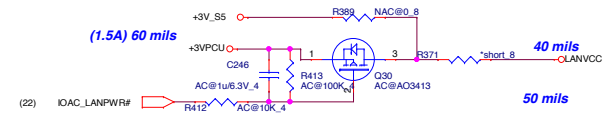
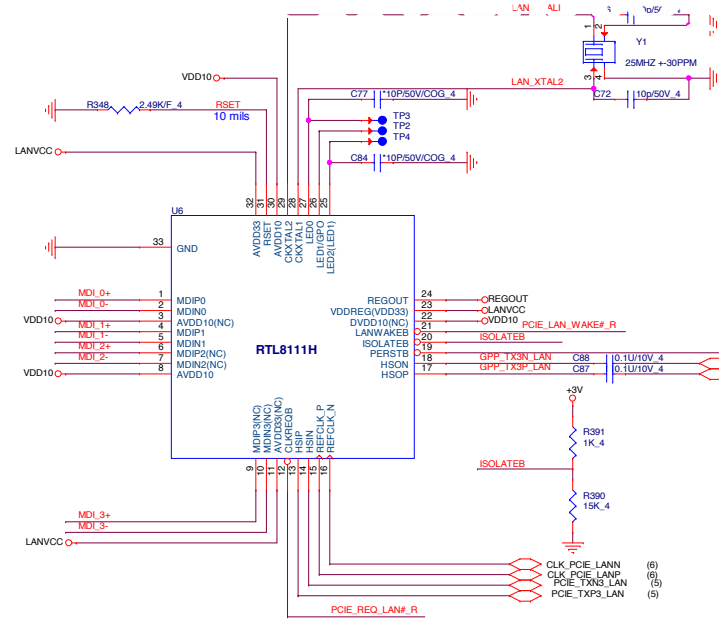
Size	Document Number	Rev
	Valley 9/9 (GND)	1A
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11/24:DDR pin define modify:
129,130,132,141,142,148,149,159,160,176,177,180,181,
191,193,194,211,33,34,39,40,41,42,45,46,47,50,51,52,53,
56,57,58,59,62,63,64,67,68,69,70,

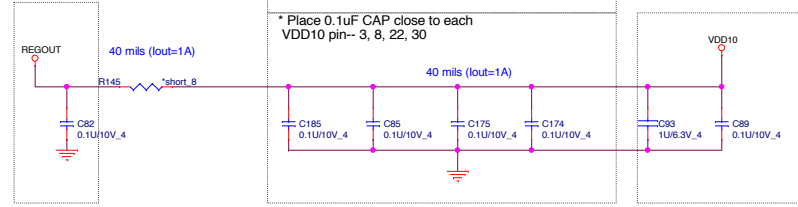


LAN

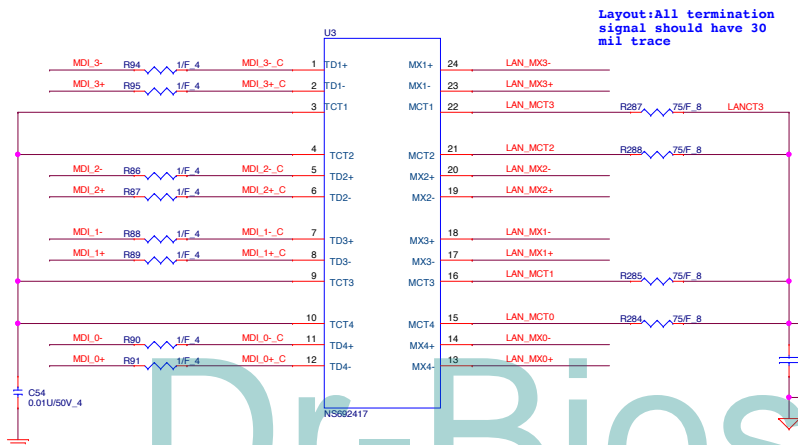


* Place 0.1uF CAP close to pin-- 24

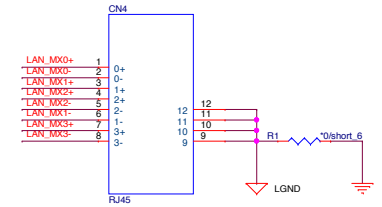
* Place 1uF CAP close to each VDD10 pin-- 22 (reserve)



Transformer

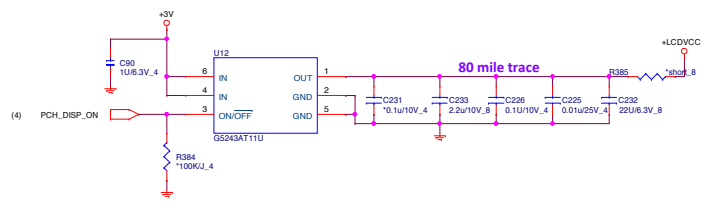


RJ45 Connector



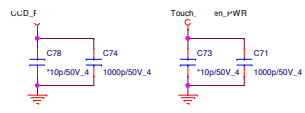
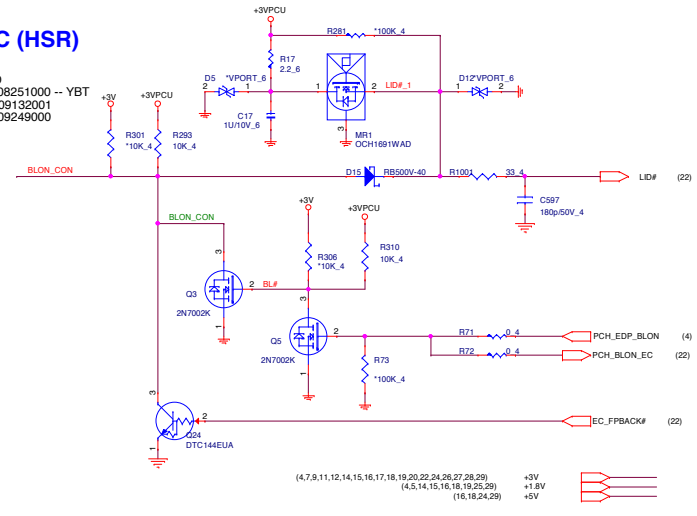
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LVDS Conn.

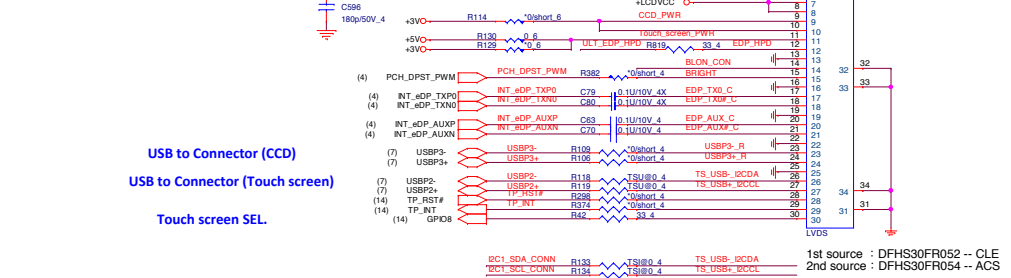


HALL IC (HSR)

1st source : EOD
 2nd source : AL008251000 -- YBT
 3rd source : AL009132001
 4th source : AL009248000

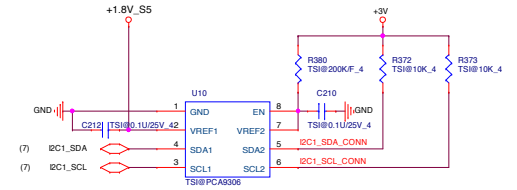


Touch screen ON/OFF

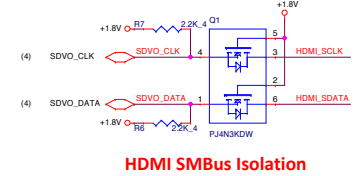


USB to Connector (CCD)
 USB to Connector (Touch screen)
 Touch screen SEL.

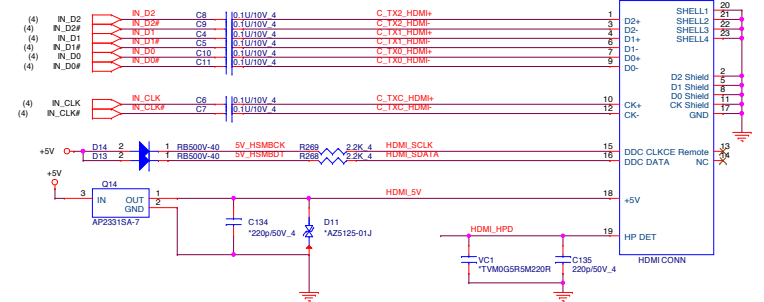
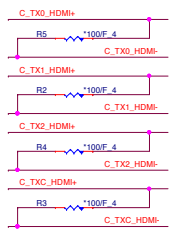
Touch screen level shift I2C(reserve)



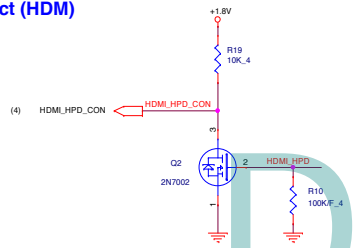
HDMI Conn.



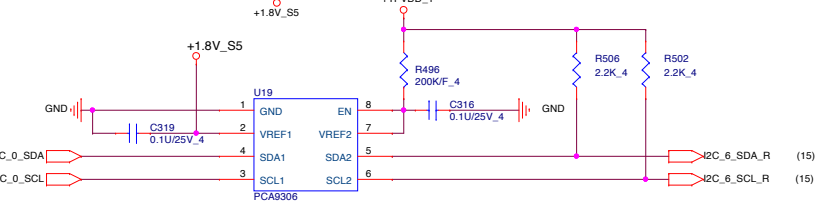
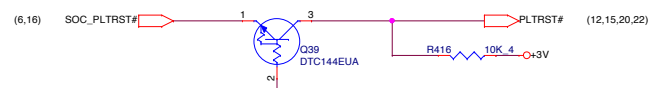
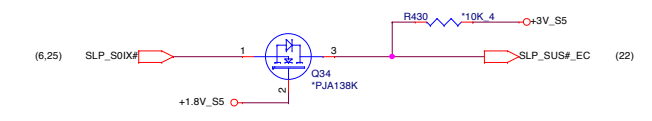
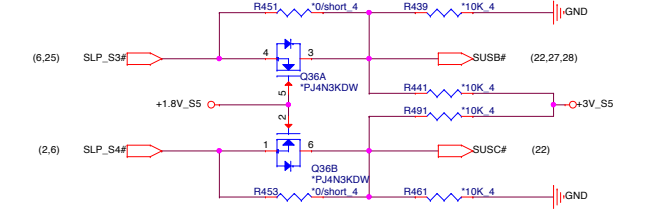
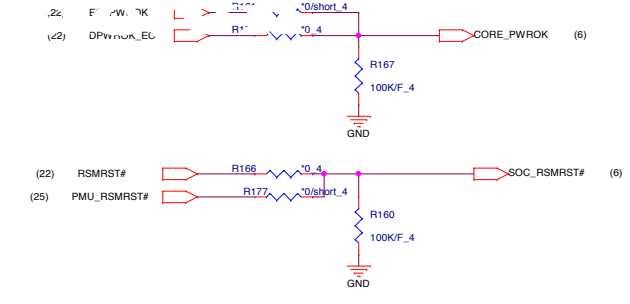
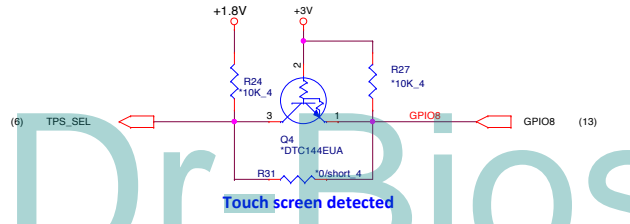
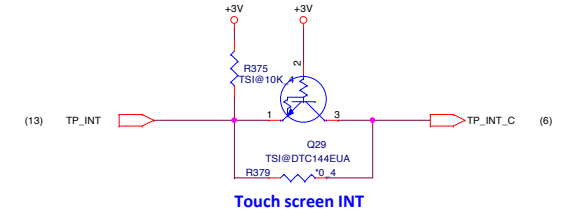
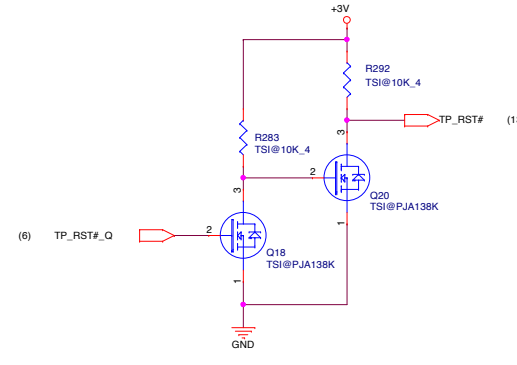
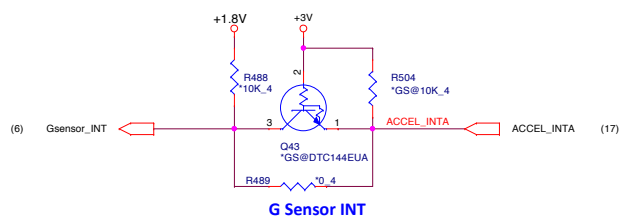
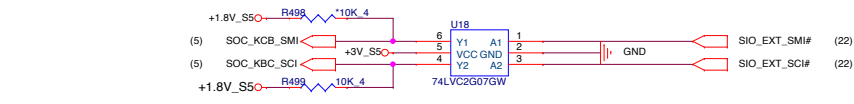
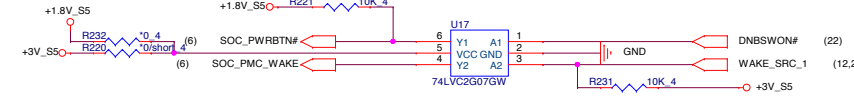
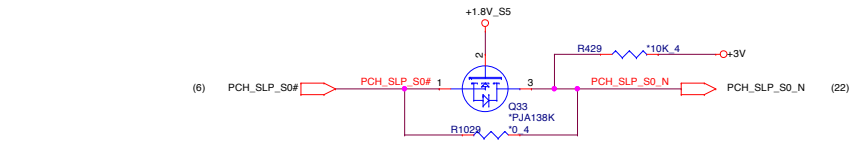
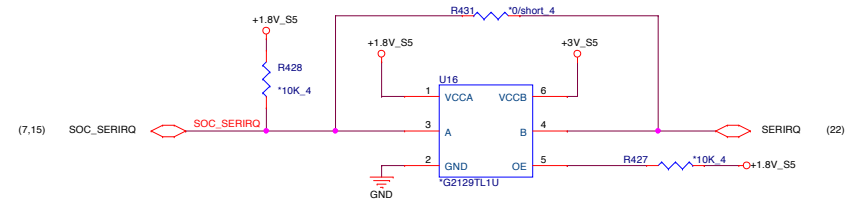
EMI (EMC)



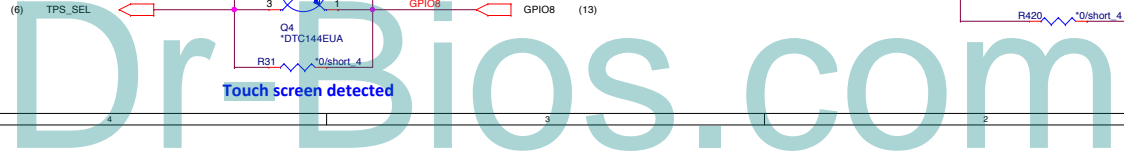
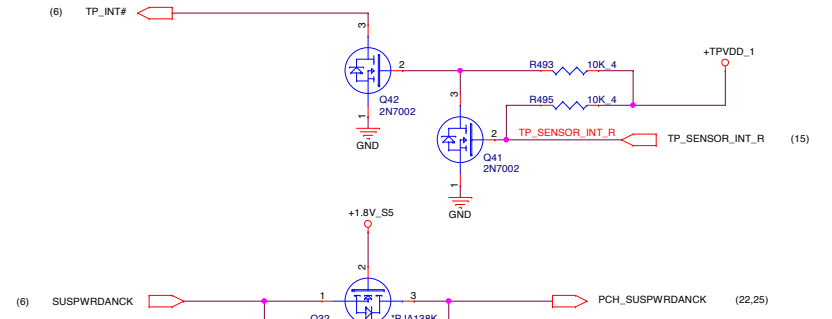
HDMI-detect (HDM)



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For Touch pad : POWER-A



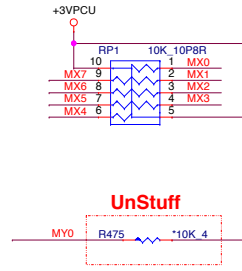
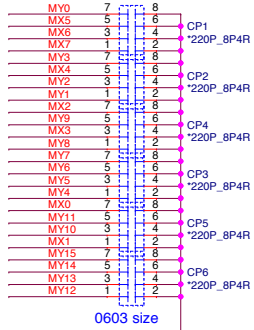
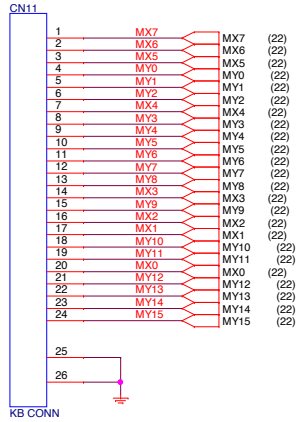
Quanta Computer Inc.
PROJECT : ZHKD
 Size: Document Number: Level Shifter Rev 1A
 Date: Monday, April 27, 2015 Sheet 14 of 31

KEYBOARD (KBC)

<20110214(E1A)>
Change CP1~CP6 footprint from 8p4r-0402-smt to 8P4R, for SMT open issue.

<EMI>

INTERNAL KEYBOARD STRIP SET (KBC)

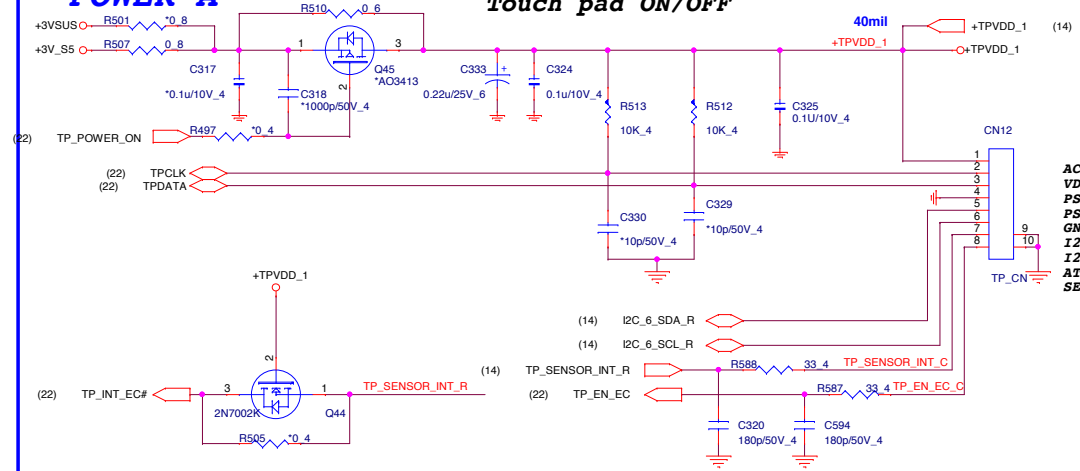


UnStuff

POWER-A

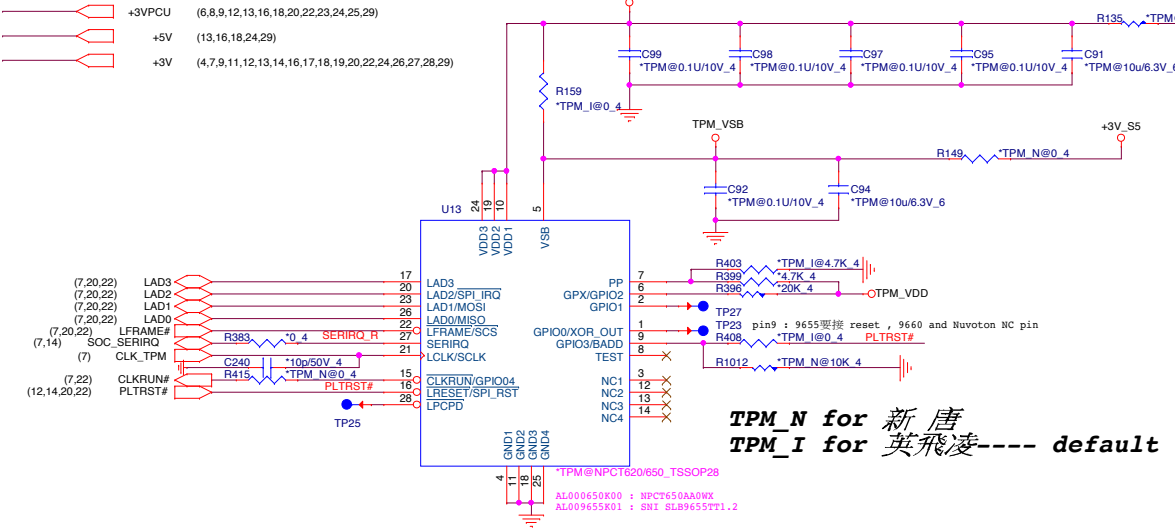
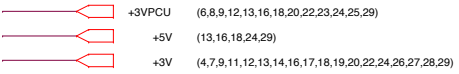
Touch pad I2C Touch pad INT Touch pad ON/OFF

15

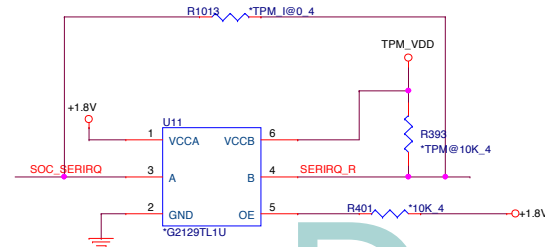


ACER DEFINE
VDD
PS2-CLK
PS2-DATA
GND
I2C-DATA
I2C-CLK
ATTN (INT)
SER-OFF.

TPM (TPM)



TPM_N for 新唐
TPM_I for 英飛凌---- default

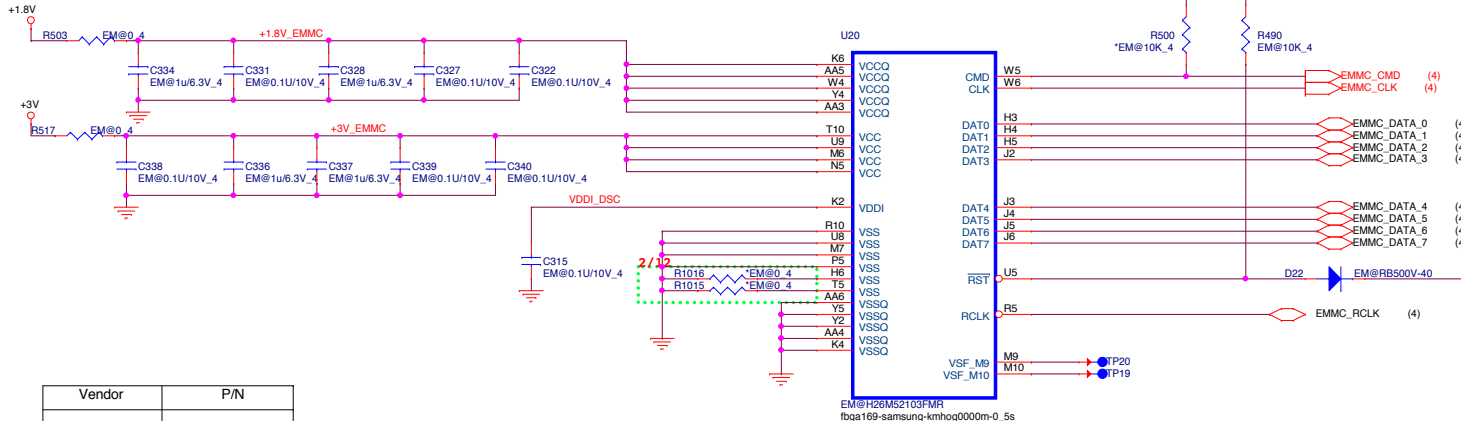
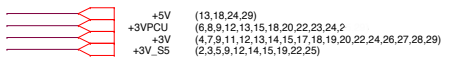


note: serie need to add level shift

		Quanta Computer Inc. PROJECT : ZHKD	
		Size Document Number KB/BT/TP	Rev 1A
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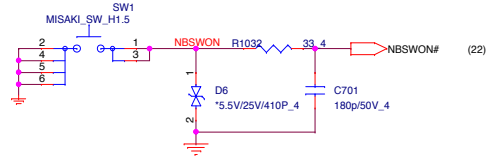
eMMC



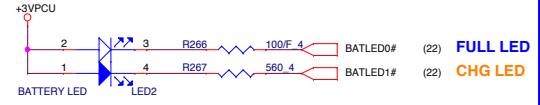
Vendor	P/N
SAMSUNG 64G	AKE3TZPT506
Samsung 32G	AKE5SZ0T501
HYNIX 64G	AKE34GPTW00
HYNIX 32G	AKE34ZPTW00
Sandisk 32G	AKE3SZ-T105

U20
EM@H26M52103FMR
fbga169-samsung-kmhog000m-0_5s

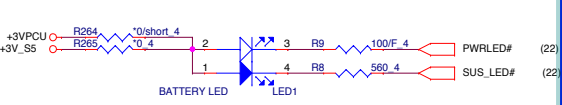
PWR button



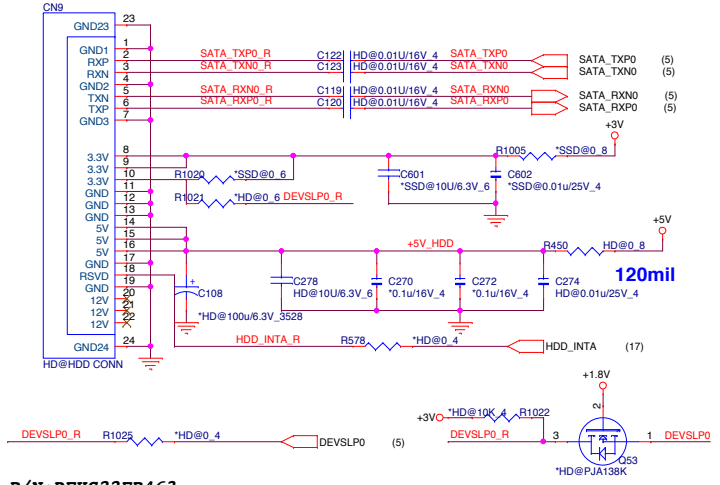
Battery indicator



PWR indicator

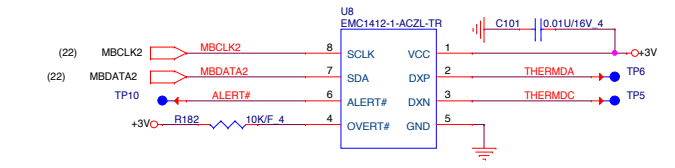


SATA HDD



P/N:DFHS22FR463
2nd source : DFHS22FR501

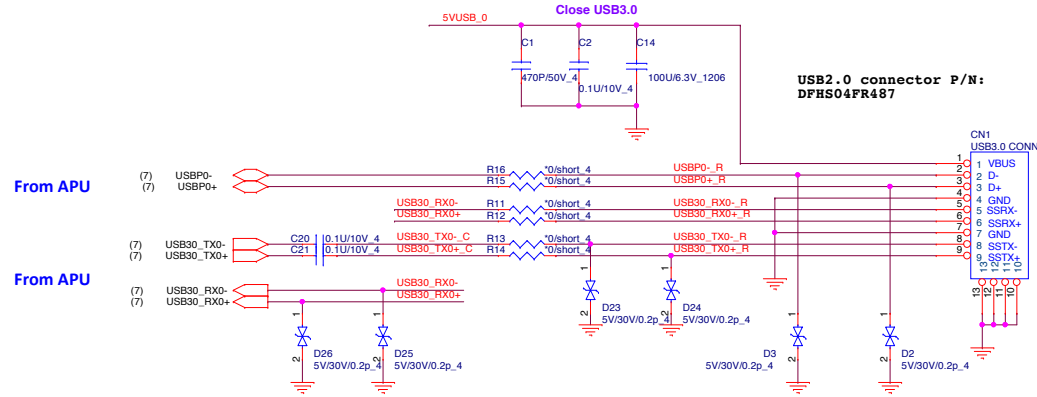
CPU Thermal sensor(THS) / MB Local TEMP



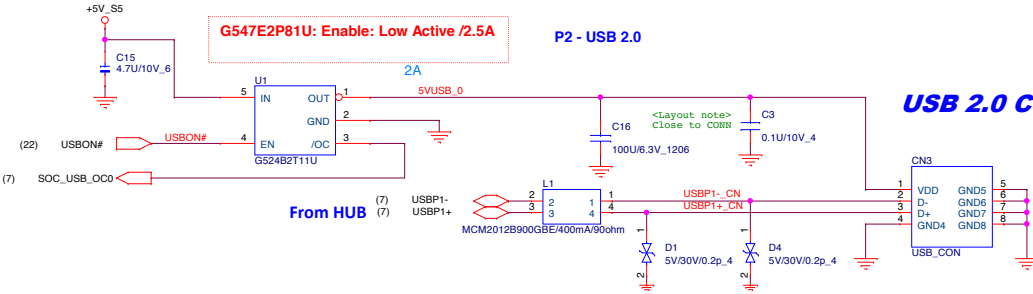
Main:AL001412003 EMC1412-1-ACZL-TR(98h)
2nd:AL000431014 TMP431ADGKR(98h)



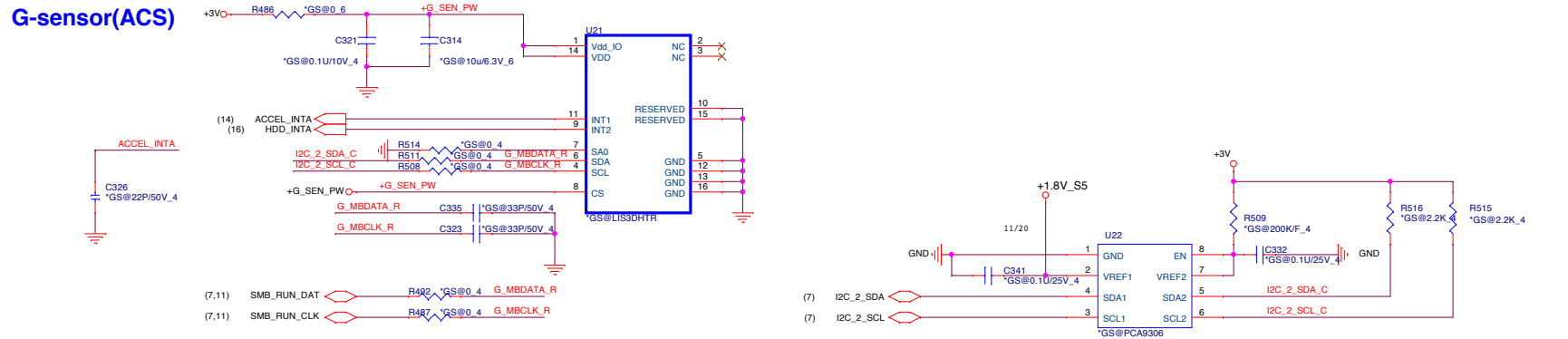
USB 3.0 Connector



USB 2.0 Connector



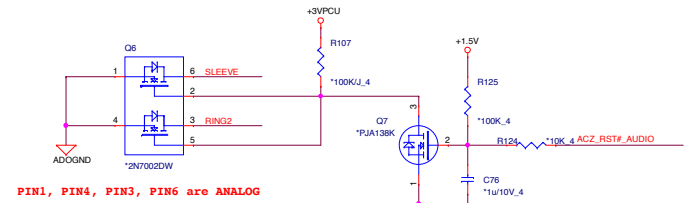
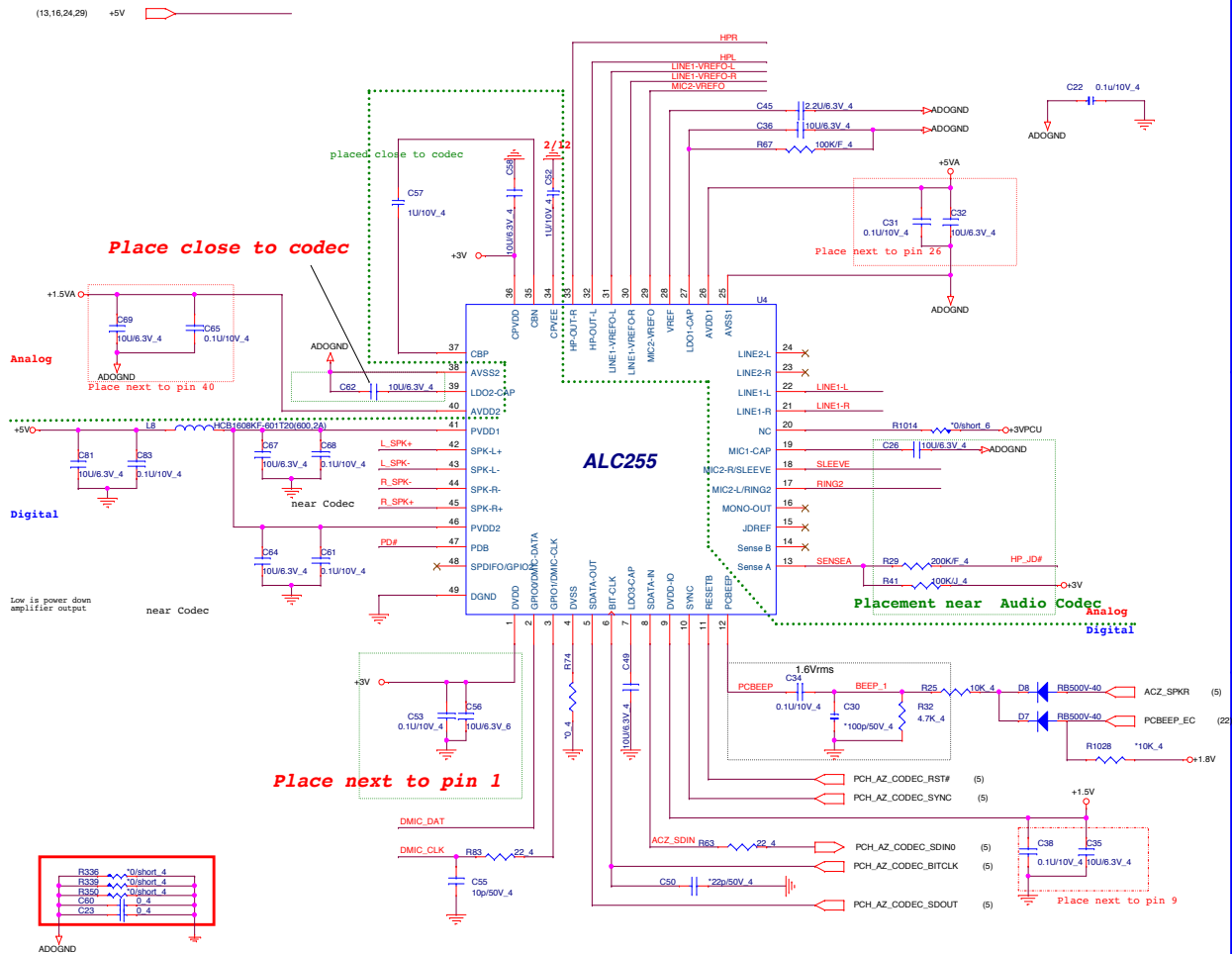
G-sensor(ACS)



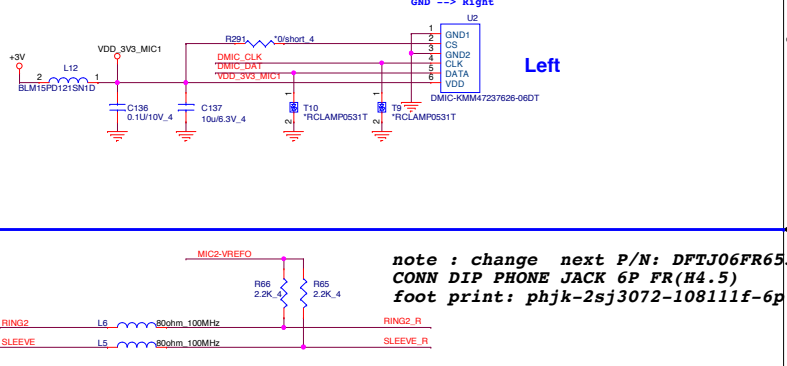
Quanta Computer Inc.
PROJECT : ZHRD

Size	Document Number	Rev
	USB BOARD / G_SENSOR	1A
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Codec(ADO)

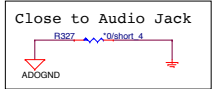
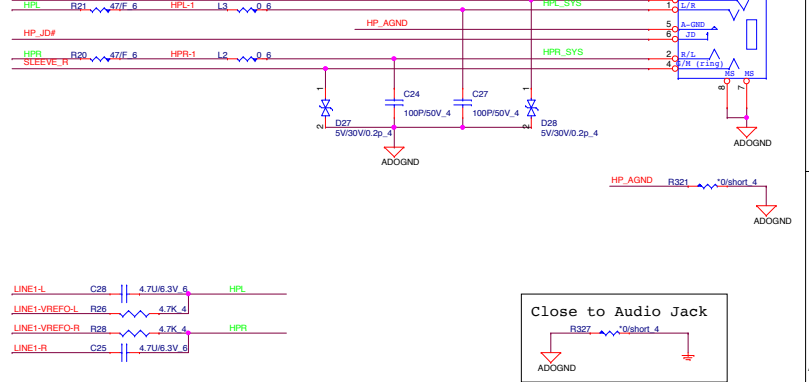


Microphone

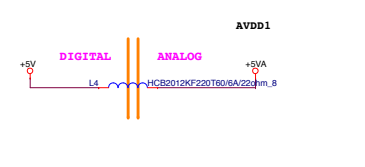


note : change next P/N: DFTJ06FR653
CONN DIP PHONE JACK 6P FR(H4.5)
foot print: phjk-2sj3072-108111f-6p

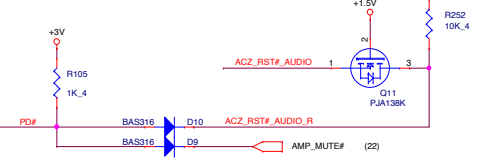
HP_MIC 上/下/左/右包覆AGND



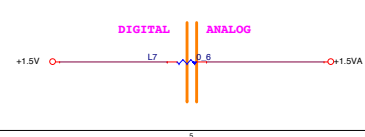
Codec PWR 5V(ADO)



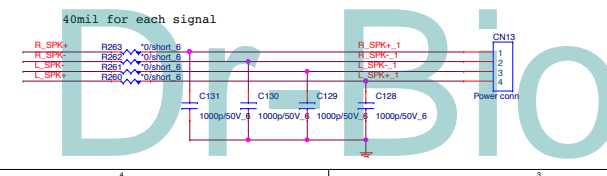
Mute(ADO)



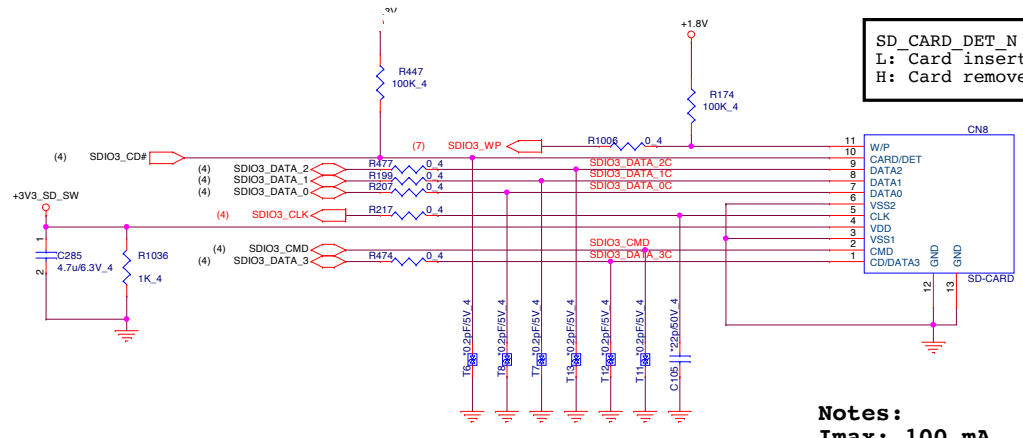
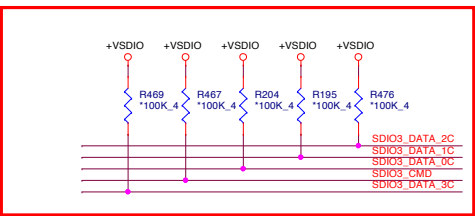
Codec PWR 1.5V(ADO)



Internal Speaker

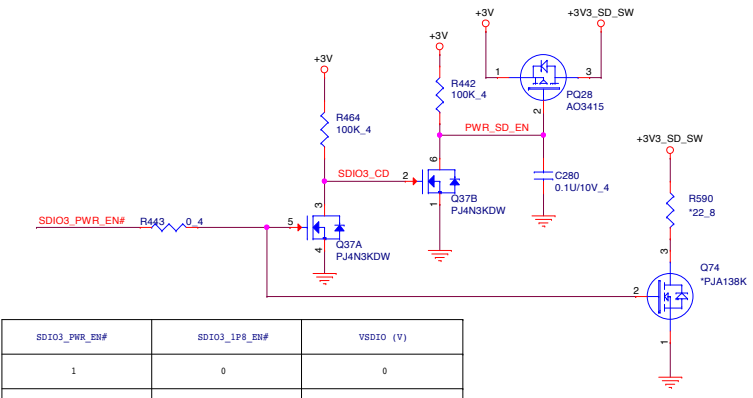


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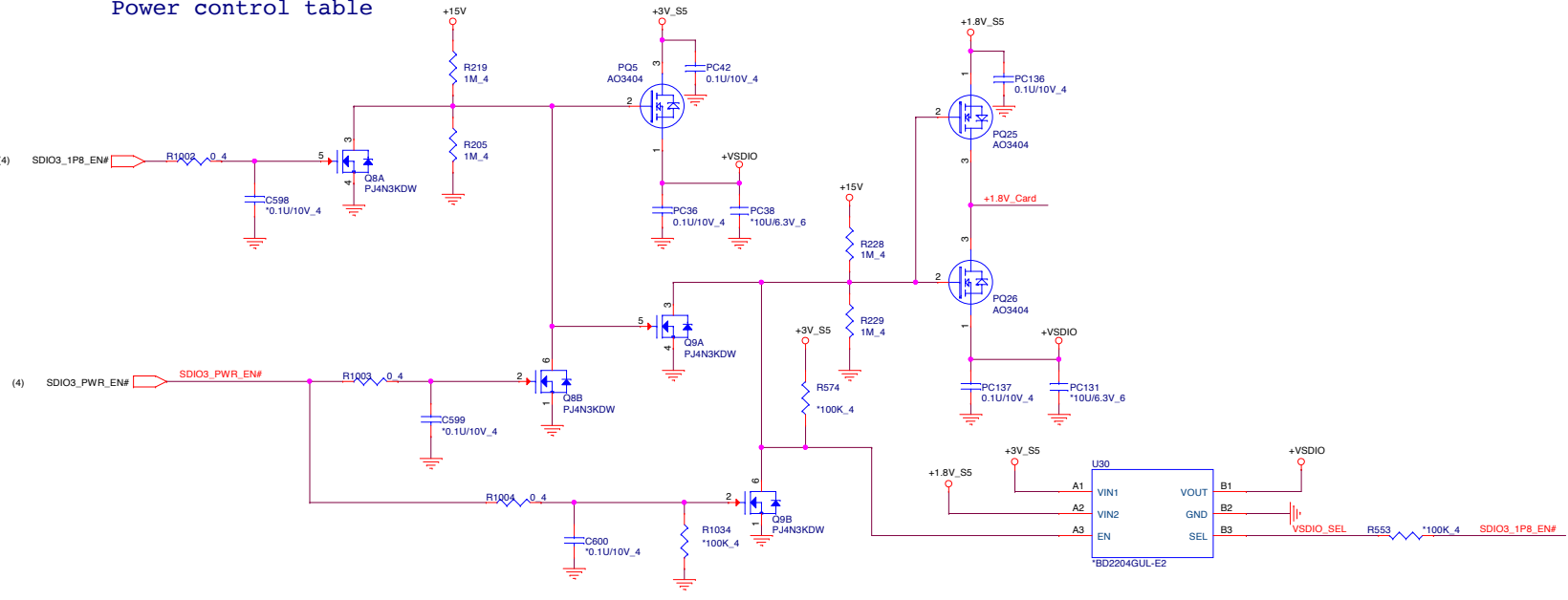
SD_CARD_DET_N
L: Card inserted
H: Card remove

Notes:
I_{max}: 100 mA
Rise time: 150 uSec



SDIO3_PWR_EN#	SDIO3_1P8_EN#	VSDIO (V)
1	0	0
1	1	0
0	0	3.3
0	1	1.8

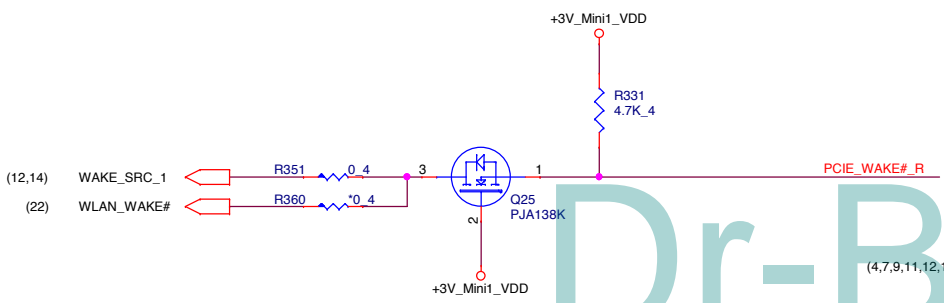
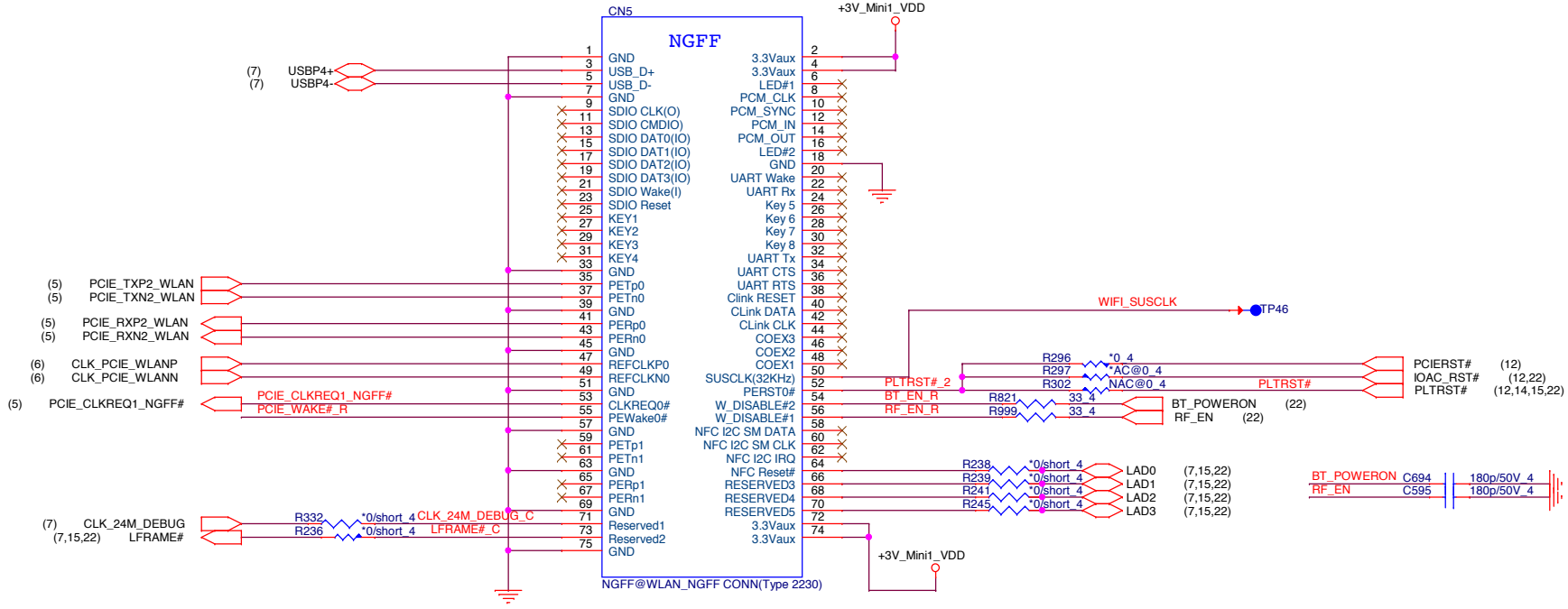
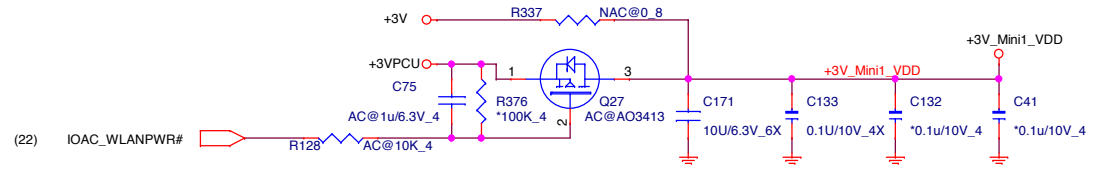
Power control table



Quanta Computer Inc.
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Cardreader GL834L

Size	Document Number	Rev
		1A

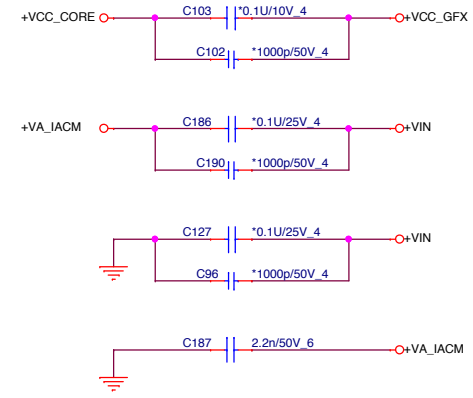
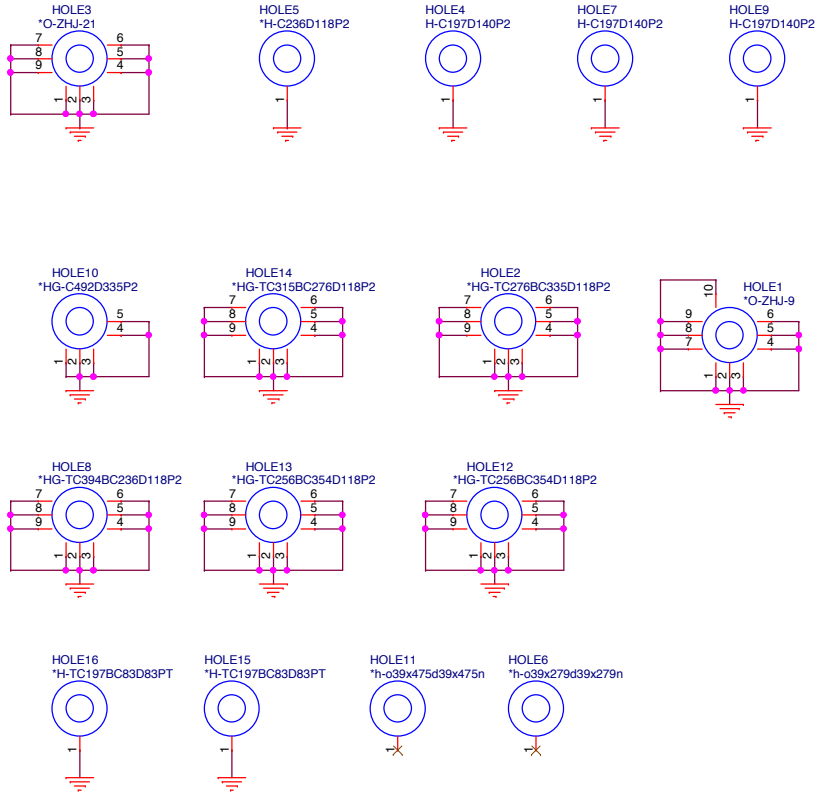
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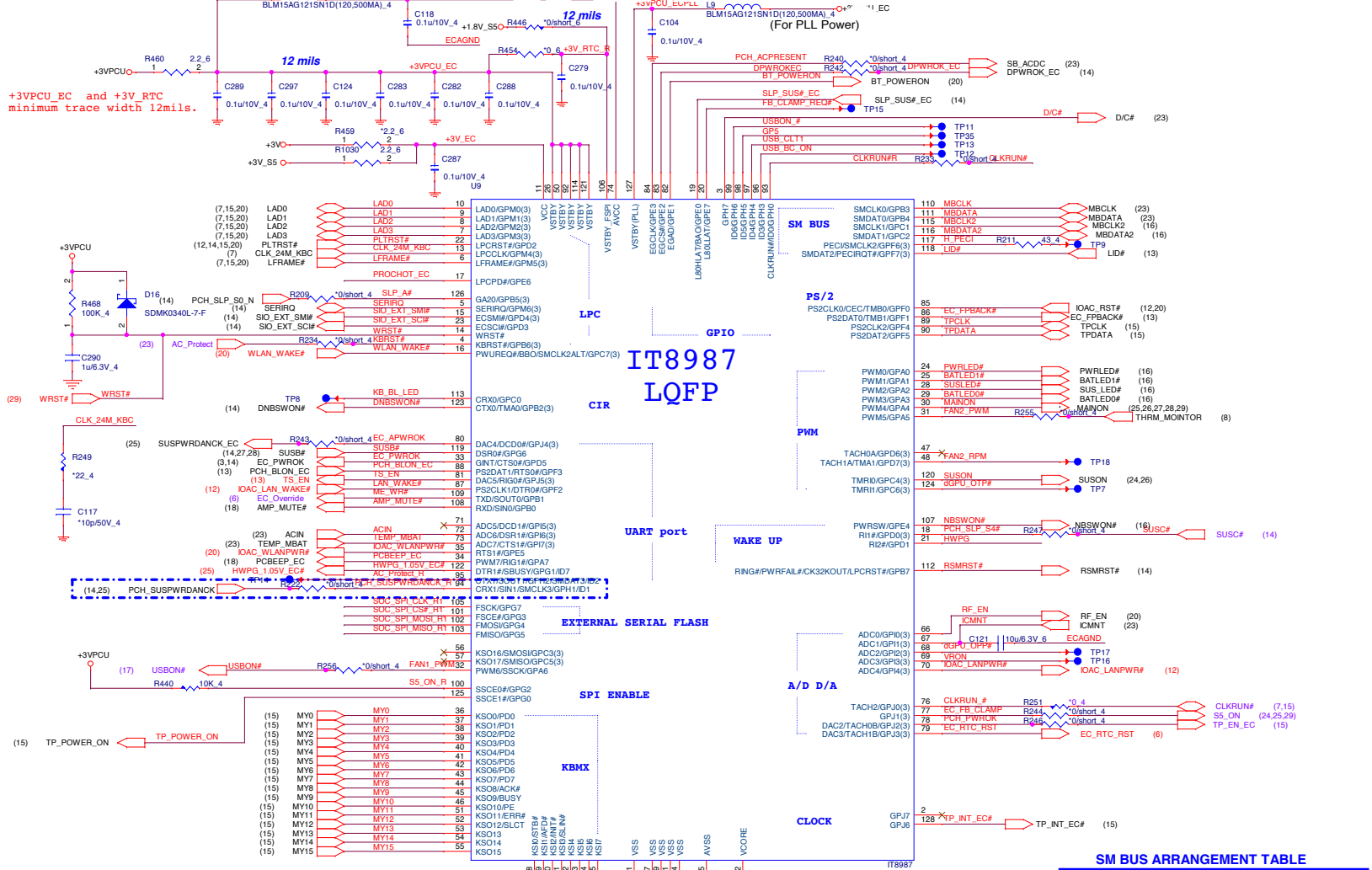
- (4,5,13,14,15,16,18,19,25,29) +1.8V
- (4,7,9,11,12,13,14,15,16,17,18,19,22,24,26,27,28,29) +3V
- (2,3,5,9,12,14,15,16,19,22,25) +3V_S5



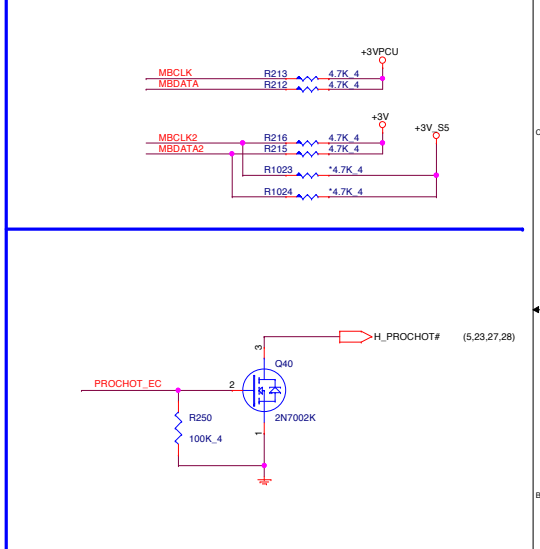

Quanta Computer Inc.
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Size	Document Number	Rev
	Thermal / Hole	1A
Date:	Monday, April 27, 2015	Sheet 21 of 31

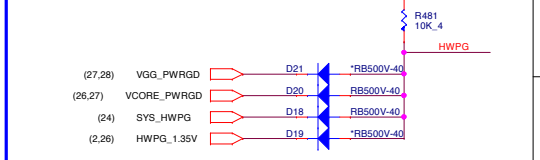
EC(KBC)



SM BUS PU(KBC)

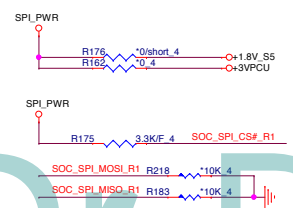
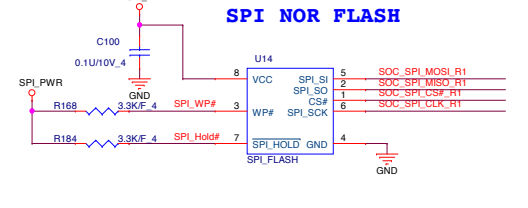


HWPG(KBC)

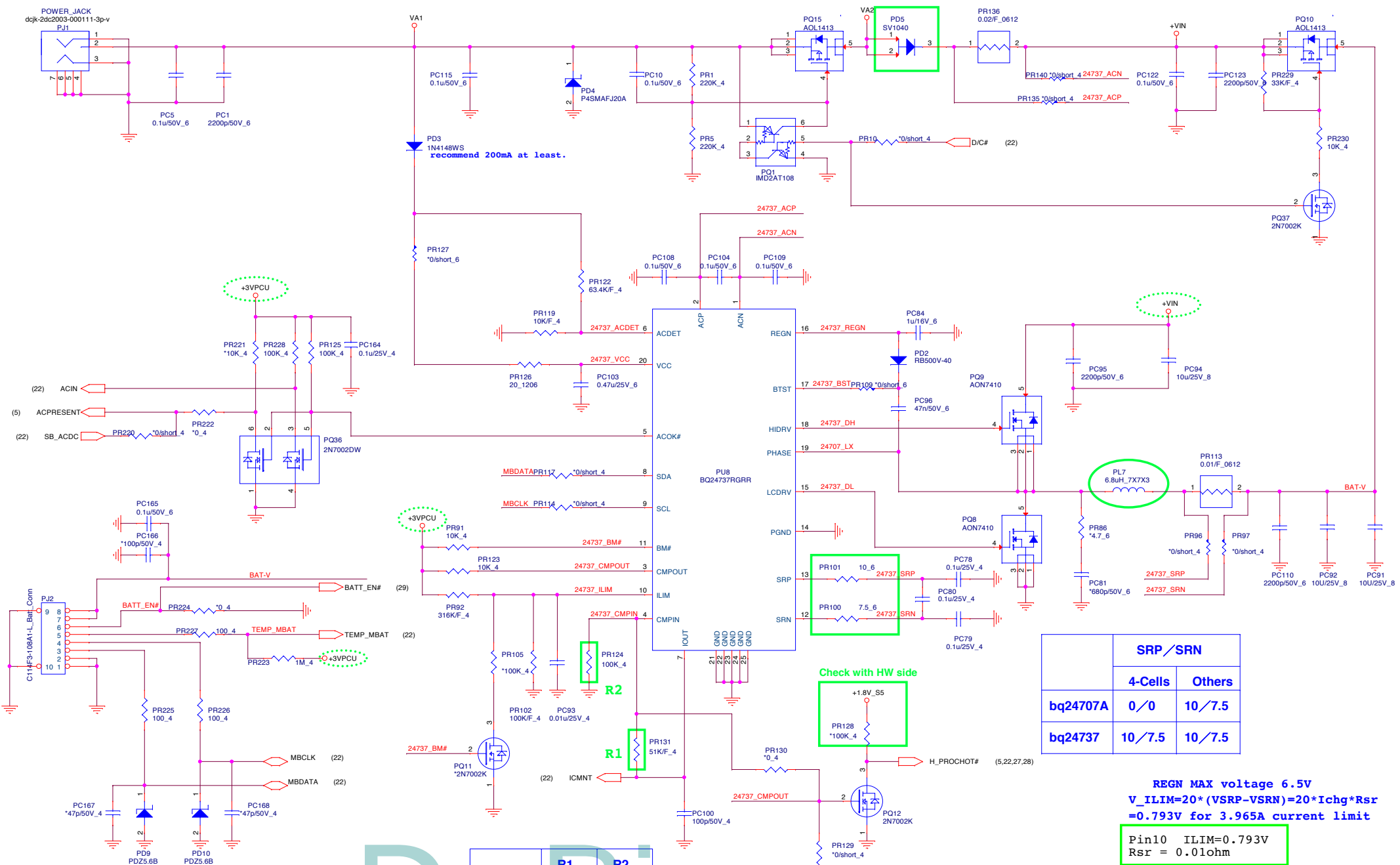


SM BUS ARRANGEMENT TABLE

SM Bus	Power Source
SM Bus 1	Battery
SM Bus 2	PCH/VGA
SM Bus 3	
SM Bus 4	



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KBC IT8987
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PD3 1N4148WS
recommend 200mA at least.

	SRP/SRN	
	4-Cells	Others
bq24707A	0/0	10/7.5
bq24737	10/7.5	10/7.5

REGN MAX voltage 6.5V
 $V_{ILIM} = 20 * (V_{SRP} - V_{SRN}) = 20 * I_{chg} * R_{sr}$
 = 0.793V for 3.965A current limit

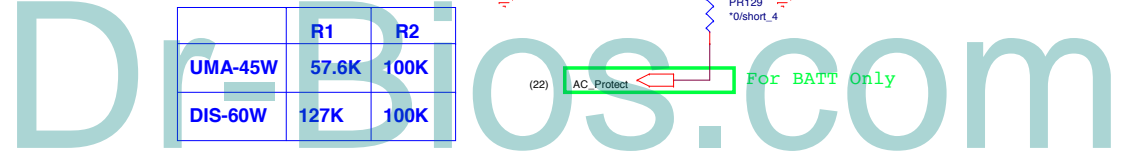
Pin10 ILIM=0.793V
 $R_{sr} = 0.01\text{ohm}$

	R1	R2
UMA-45W	57.6K	100K
DIS-60W	127K	100K

Check with HW side

+1.8V_S5
 PR128 *100K_4

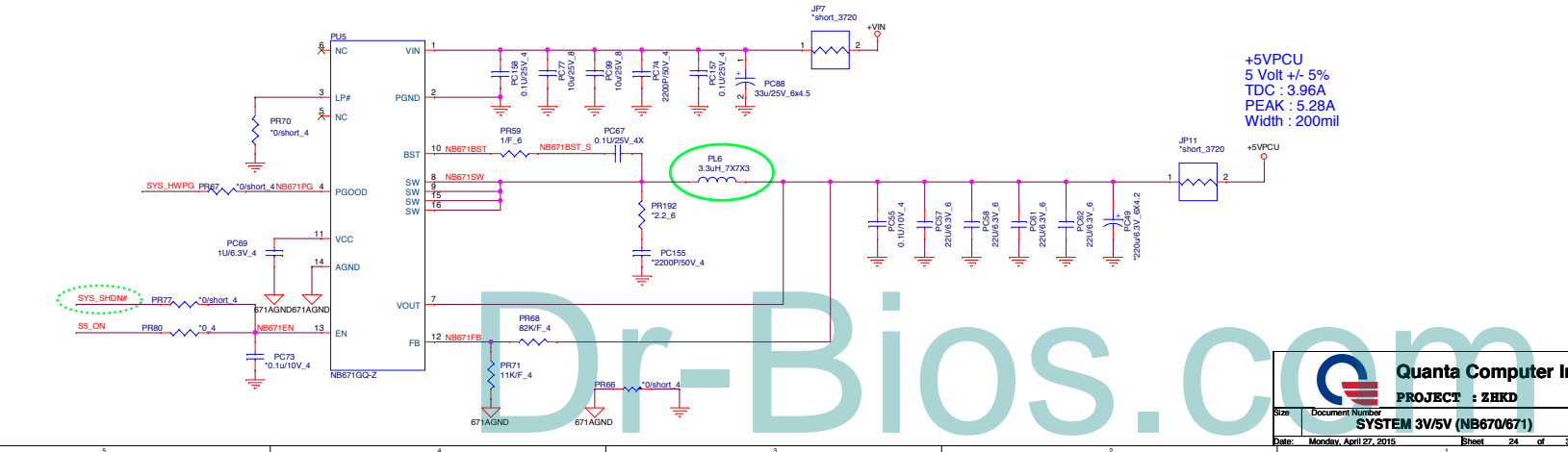
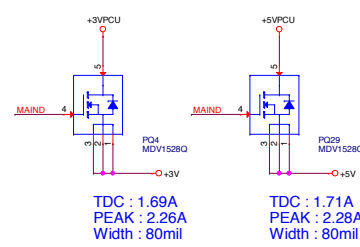
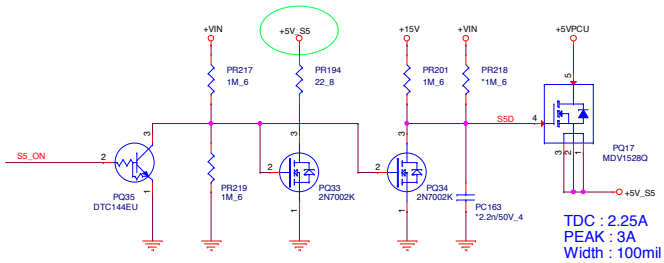
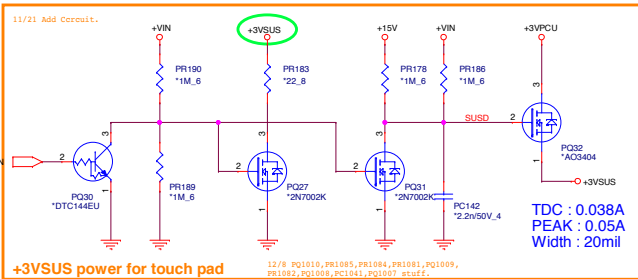
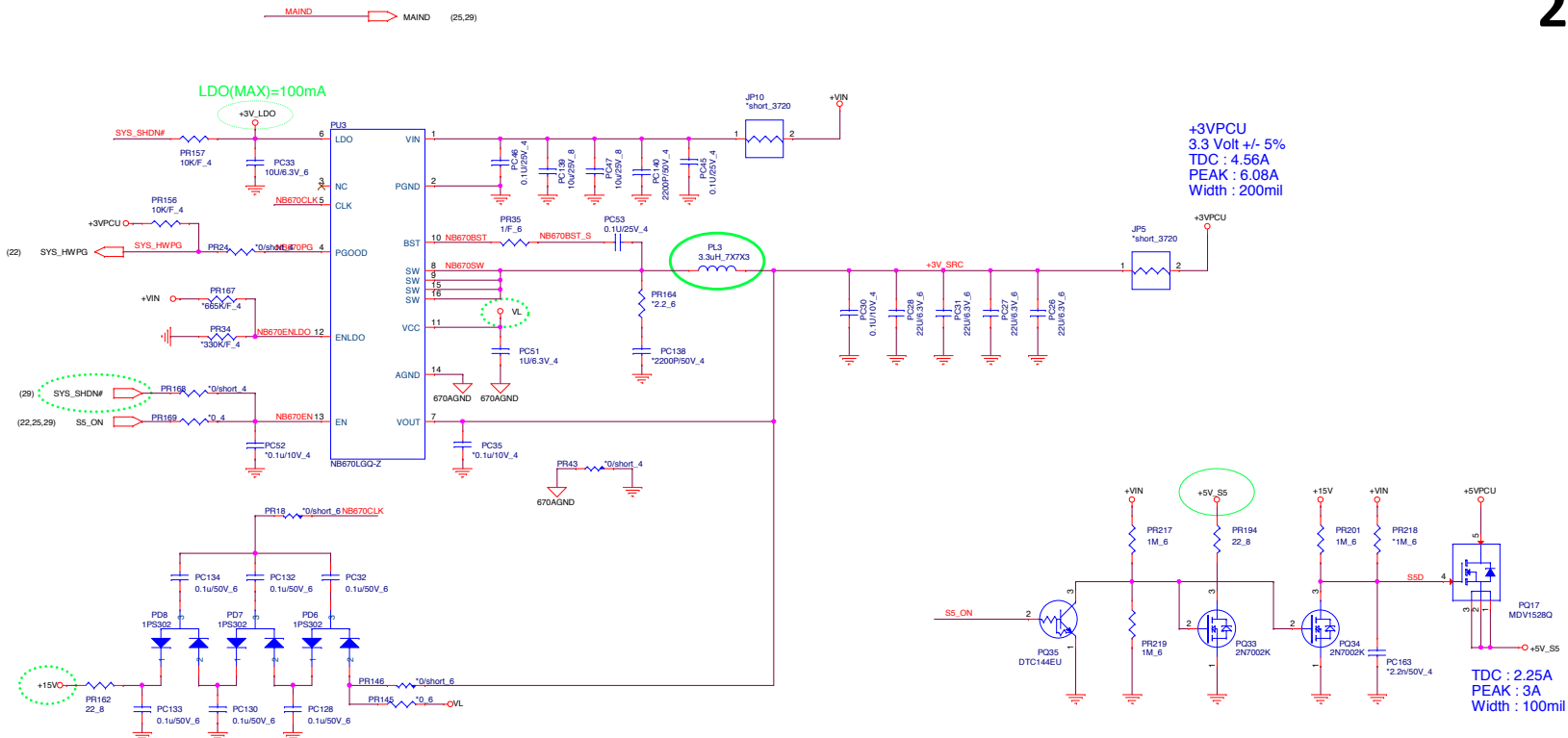
(22) AC Protect For BATT Only



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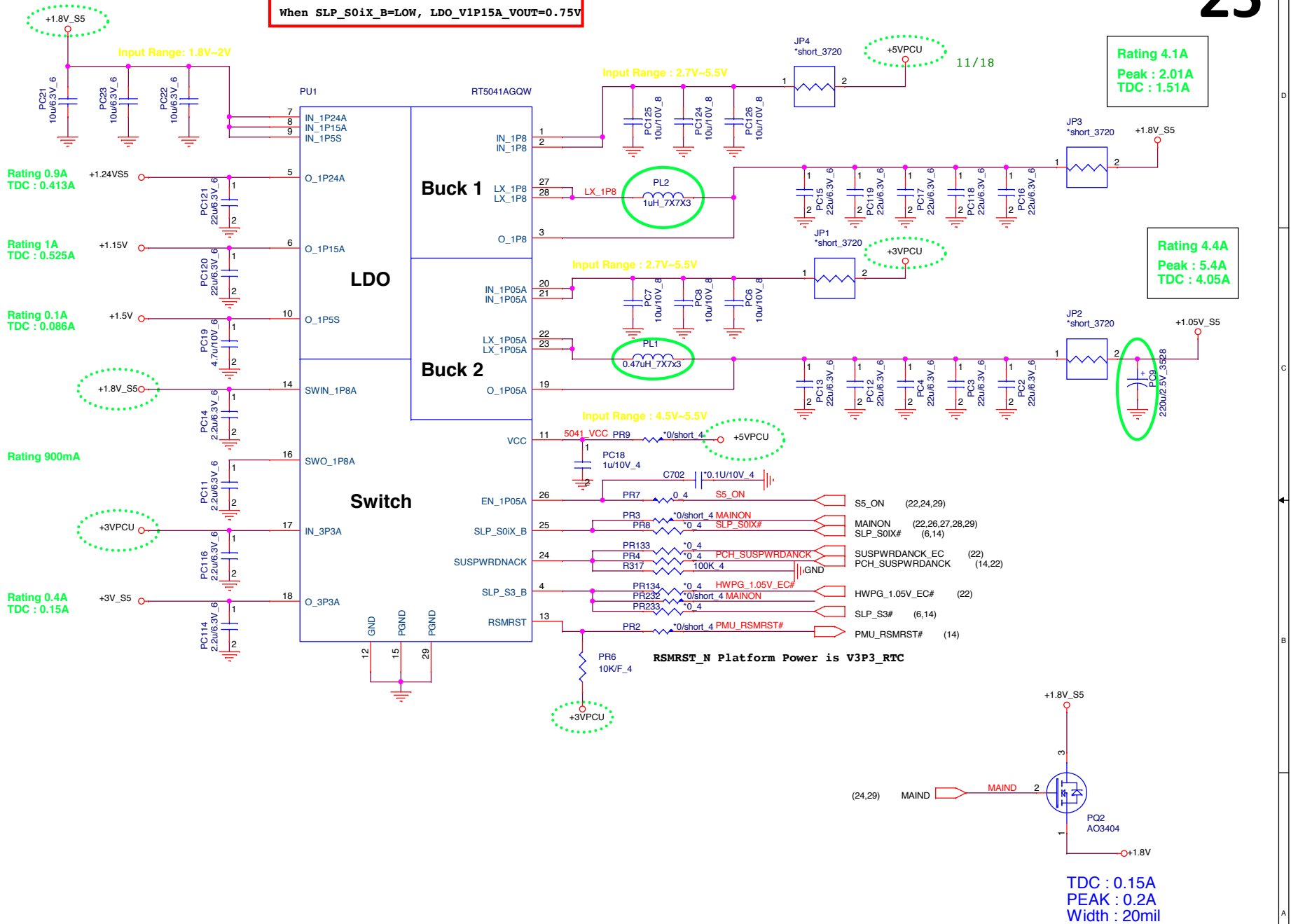
Size	Document Number	Rev
	Charger(BQ24737RGR)	1A

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When SLP_S0iX_B=High, LDO_V1P15A_VOUT=1.15V
When SLP_S0iX_B=LOW, LDO_V1P15A_VOUT=0.75V



Rating 4.1A
Peak : 2.01A
TDC : 1.51A

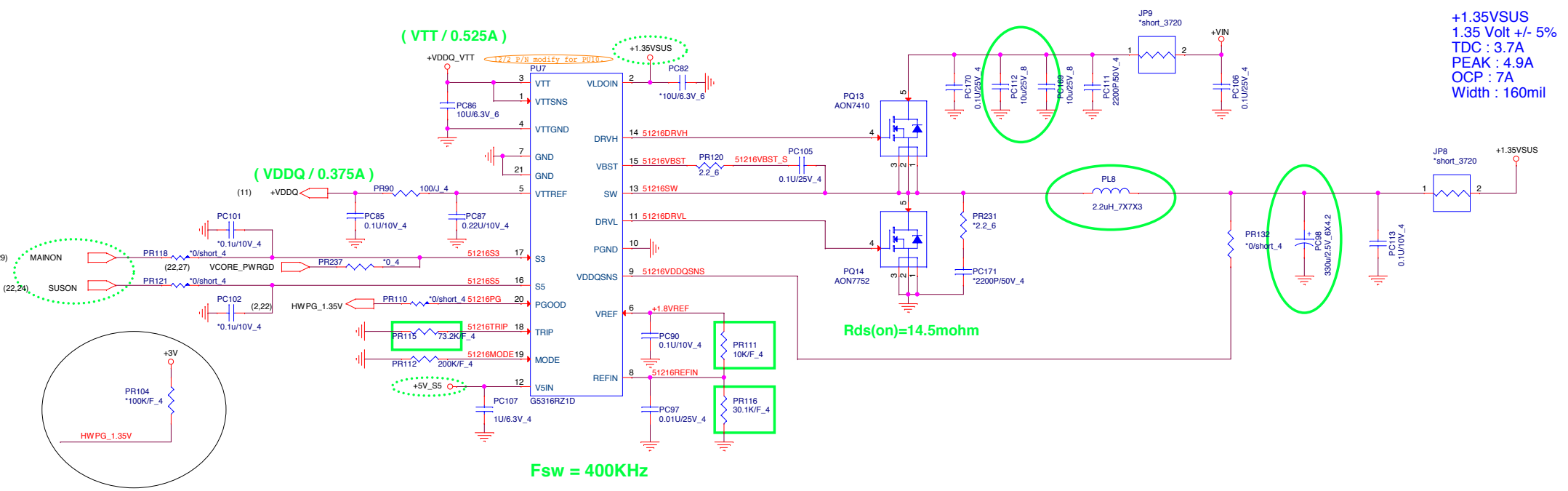
Rating 4.4A
Peak : 5.4A
TDC : 4.05A

TDC : 0.15A
PEAK : 0.2A
Width : 20mil

(2,3,9,11) +1.35VSUS
 (11) +VDDQ_VTT
 (6,17,24,27,28) +5V_S5

(VTT / 0.525A)

(VDDQ / 0.375A)



+1.35VSUS
 1.35 Volt +/- 5%
 TDC : 3.7A
 PEAK : 4.9A
 OCP : 7A
 Width : 160mil

Rds(on)=14.5mohm

Fsw = 400KHz

OCP=7A
 L ripple current
 $= (19-1.35) * 1.35 / (2.2u * 400k * 19)$
 $= 1.425A$
 $V_{trip} = 7 - (1.425 / 2) * 14.5mohm$
 $= 91.168mV$
 $R_{limit} = 91.168mV / 10uA * 8 = 72.93kohm$

DDR=1.35V
 PR266=10K/F_4
 PR268=30.1K/F_4

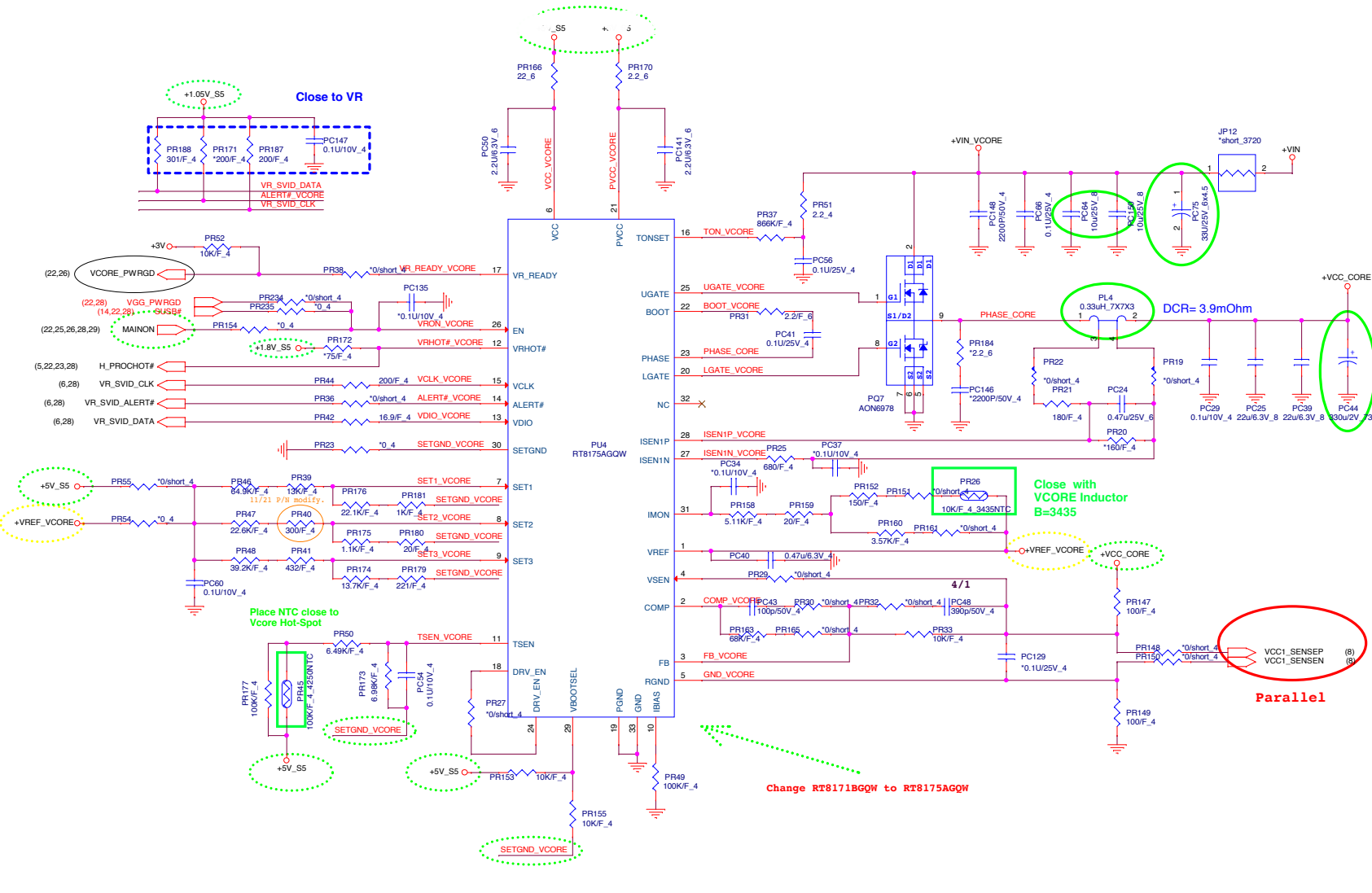
Mode	Frequency	Discharge mode
200K	400K	Tracking Discharge
100K	300K	Tracking Discharge

	S3	S5	+1.35VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (main on off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

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Size Document Number
DDR3L (APW8819) Rev 1A

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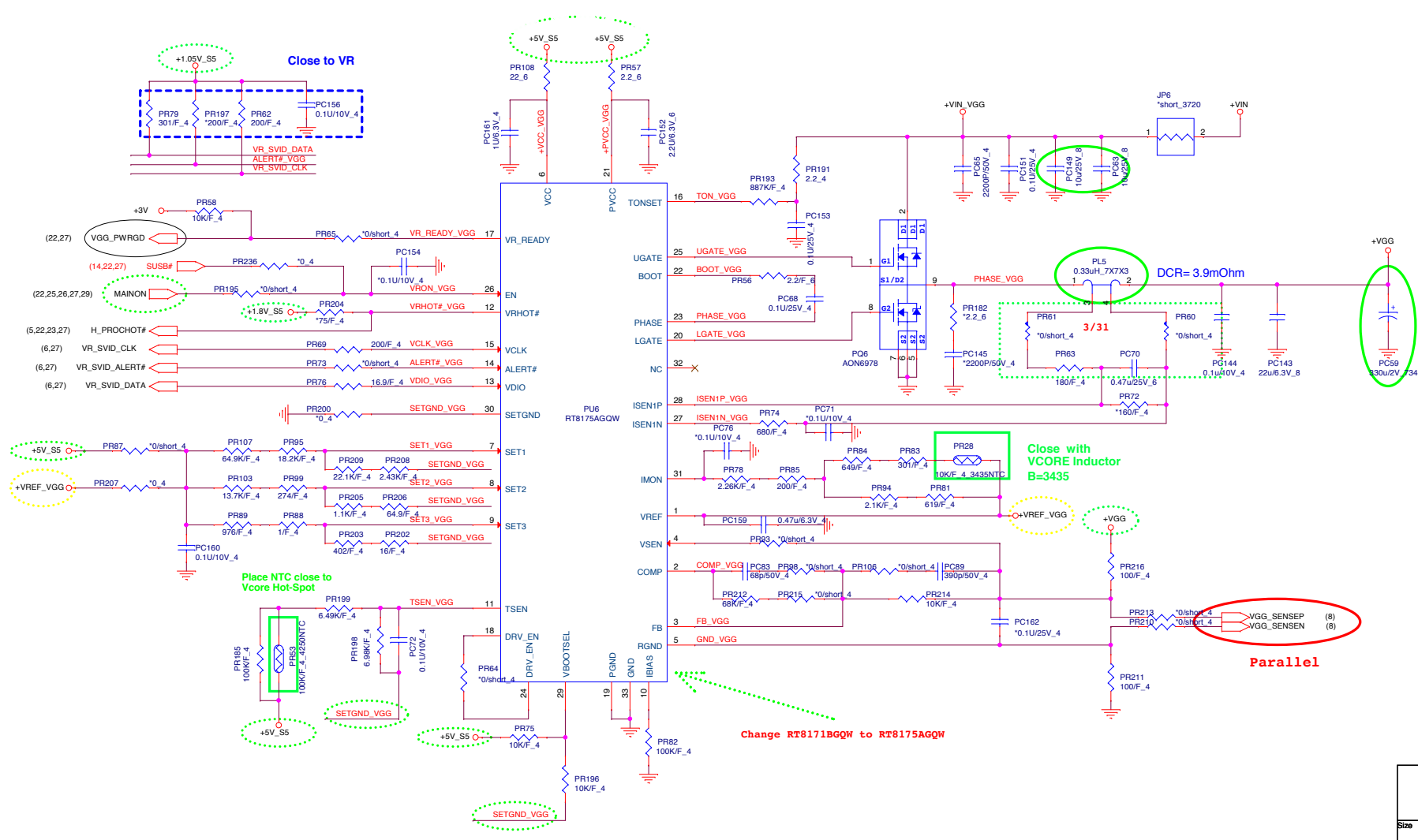
VR 12.1

Braswell - VCC0+1 (1 Phase)

Icc TDC PL2 : TBD
 Icc Max : 7A
 OCP : 12.4A
 Fsw : 800KHz
 Vboot : 1V
 VR address : 0

VCC0+1 L/L :
 R_DC_LL : 0 mV/A
 R_AC_LL : 0 mV/A

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		PROJECT : ZHKD	
Size	Document Number	VCC0+1 (RT8171BGQW)	
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VR 12.1

Braswell - VGG (1 Phase)

Icc TDC PL2 : TBD
 Icc Max : 15A
 OCP : 20.7A
 Fsw : 800KHz
 VR Address : 5

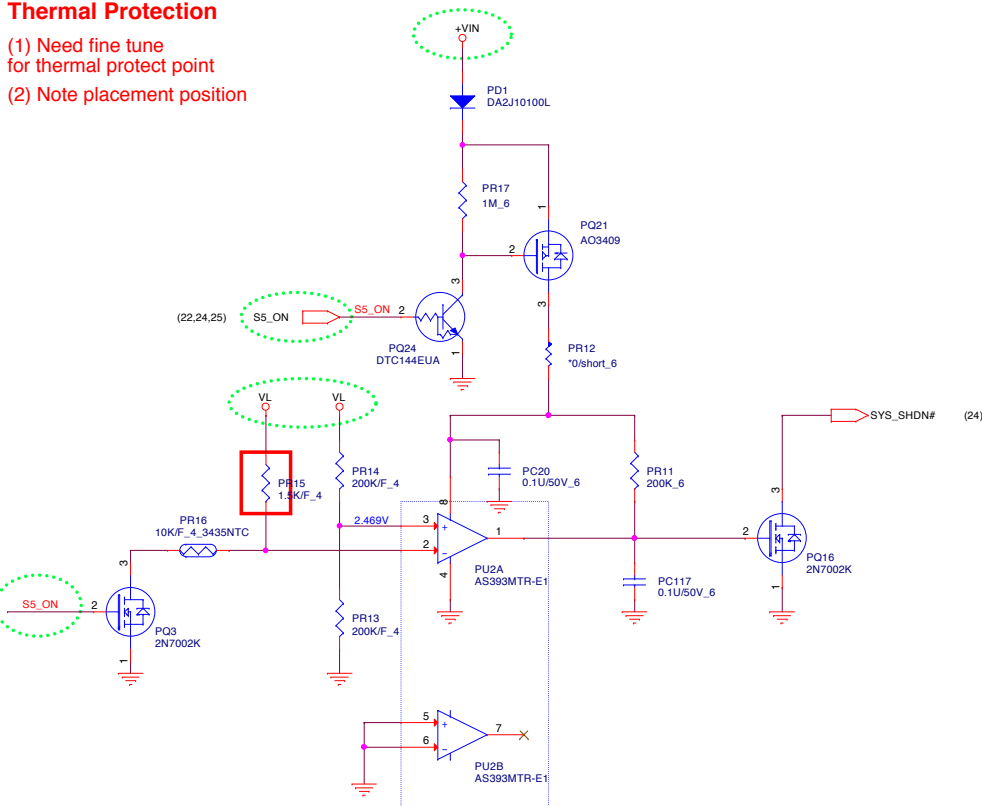
VCORE L/L :
 R_DC_LL : 0 mV/A
 R_AC_LL : 0 mV/A

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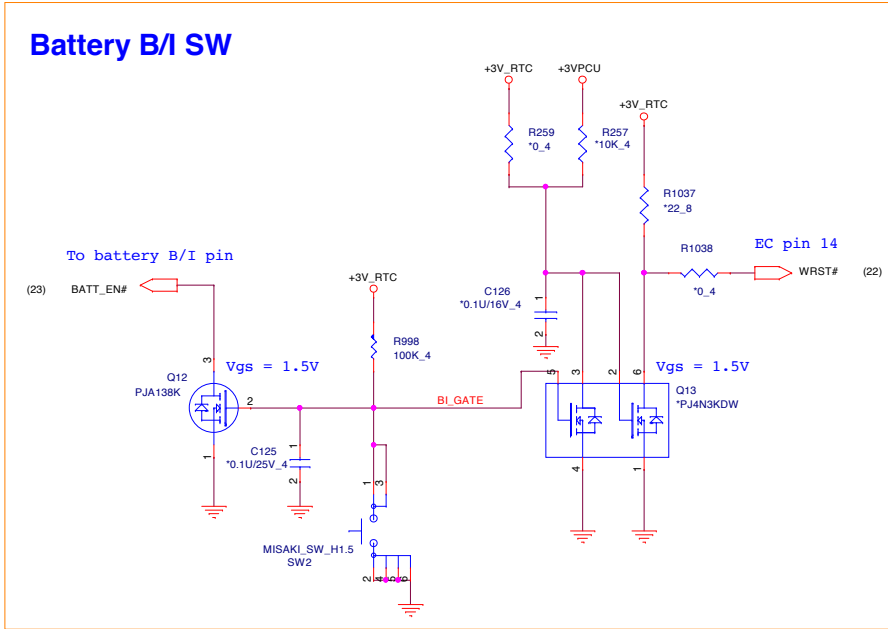
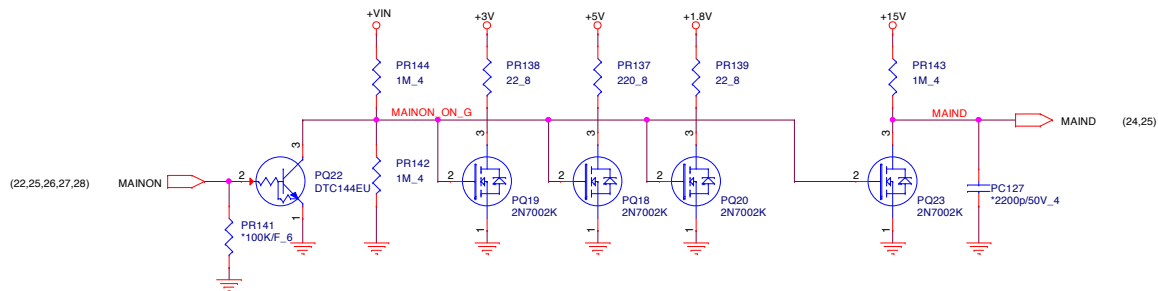
Size	Document Number	Rev
	+VGG (RT8171BGQW)	1A
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Thermal Protection

- (1) Need fine tune for thermal protect point
- (2) Note placement position

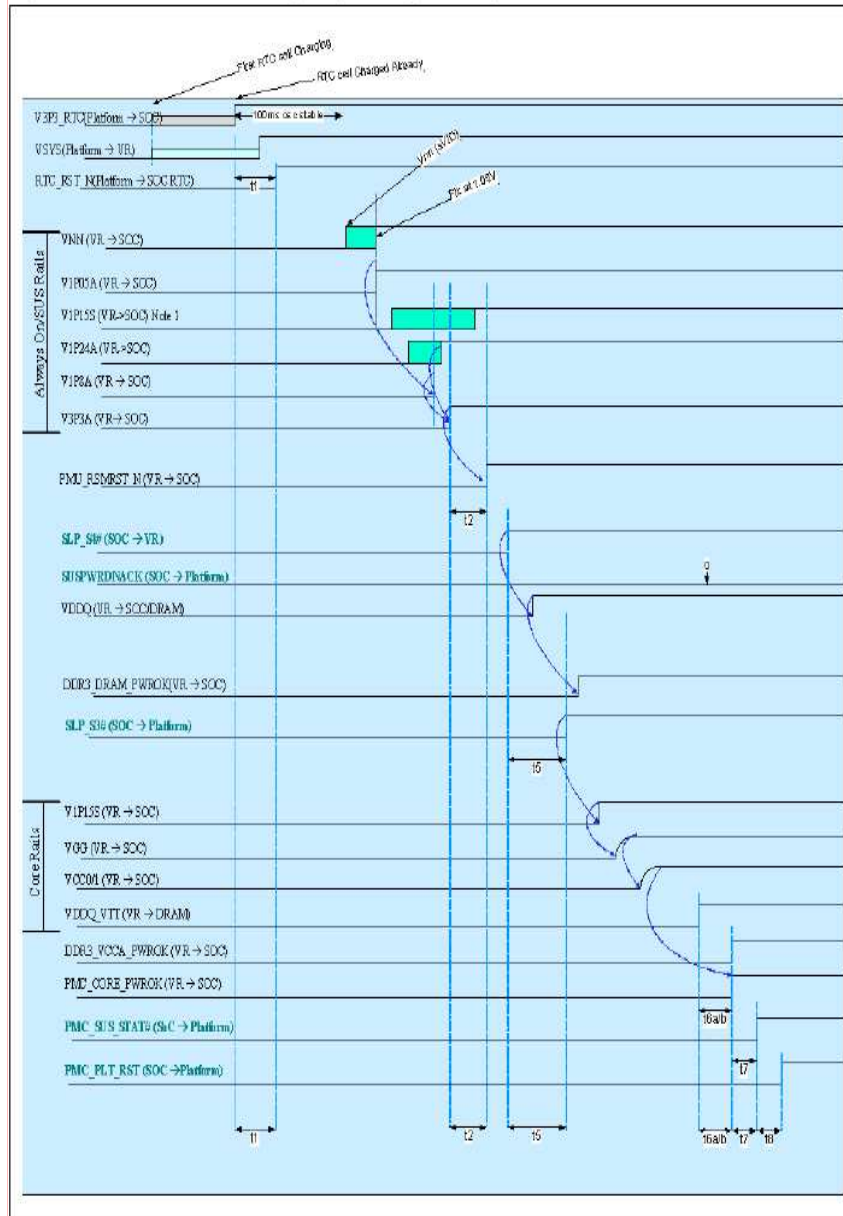


For EC control thermal protection (output 3.3V)



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	Thermal / Discharge	1A
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Figure 5-2. Platform Power Up Sequence (G3 to S0)



CHANGE LIST

Model	Rev.	
ZHKD	1A	2014/12/11 First Release

DOC NO.	PROJECT MODEL :	ZHKD	APPROVED BY:		DATE:	
	PART NUMBER:		DRAWING BY:		REVISION:	



Quanta Computer Inc.
PROJECT : ZHKD
Drawing Title : Change List
DATE : 2014/12/11

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