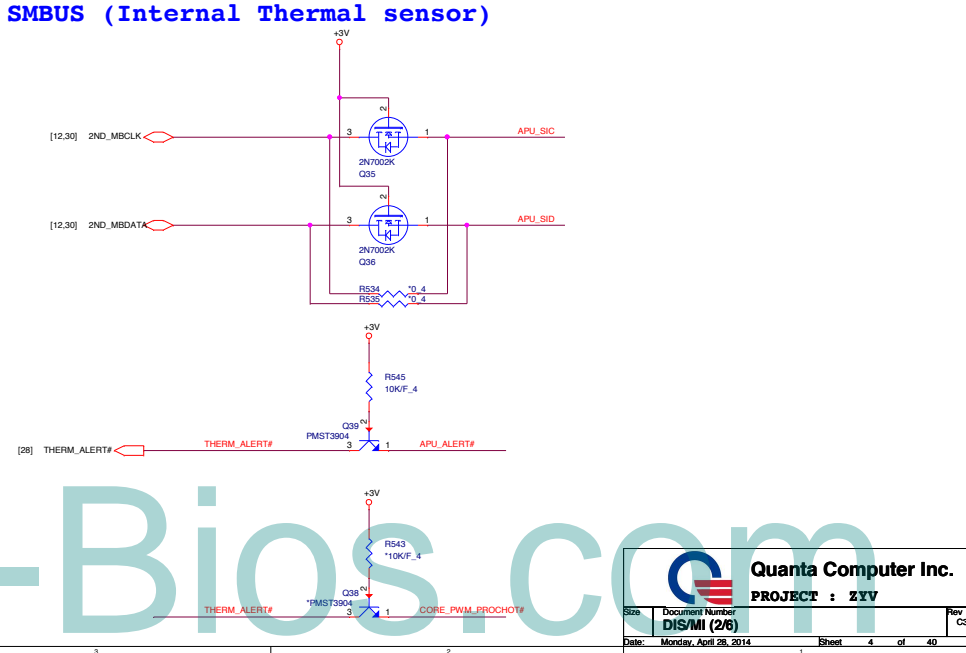
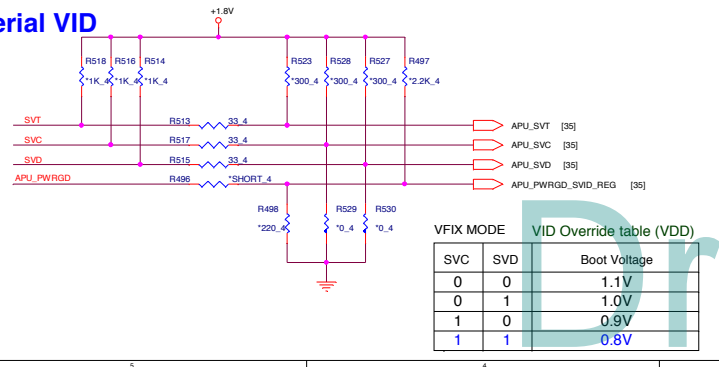
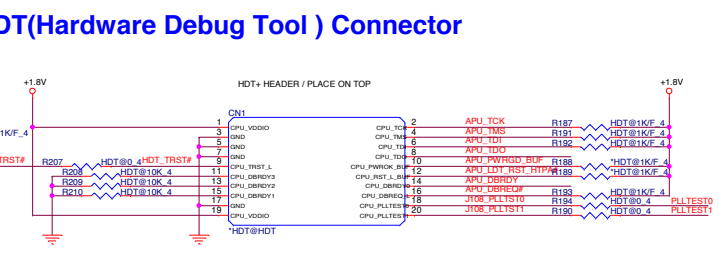
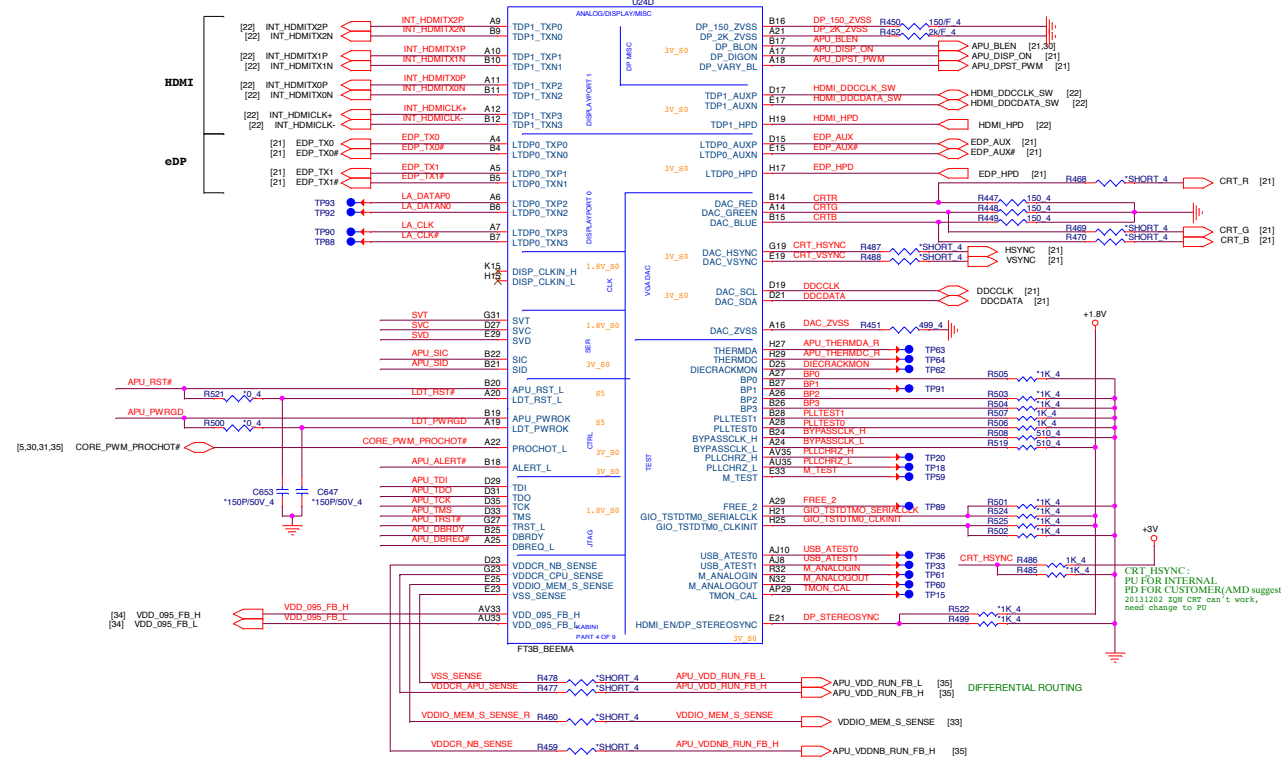
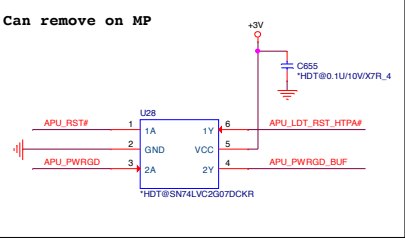
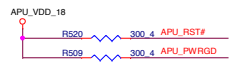
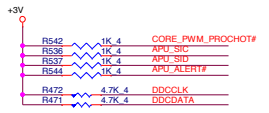


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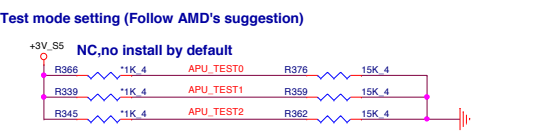
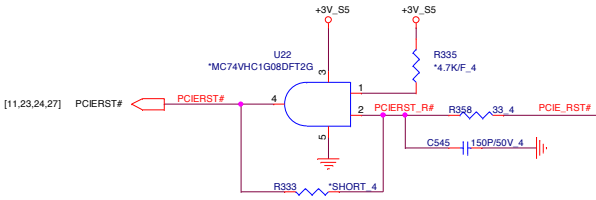
Quanta Computer Inc.
PROJECT : ZIV

Size: Document Number: MEM/PCIE (1/6) Rev: CSA
 Date: Monday, April 28, 2014 Sheet: 3 of 40



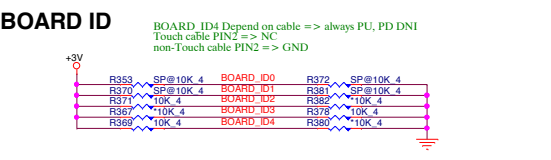
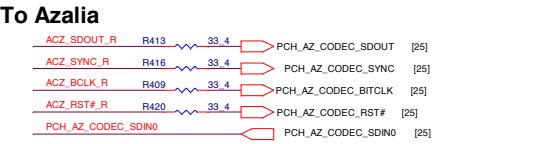
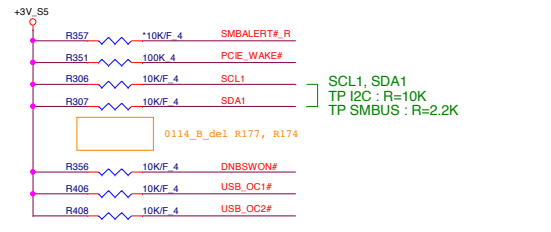
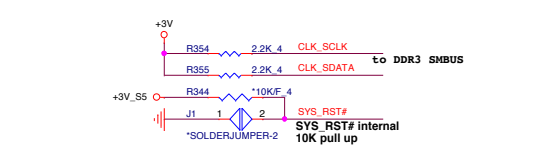
Quanta Computer Inc.
PROJECT : ZYV

Date: Monday, April 28, 2014
Sheet 4 of 40

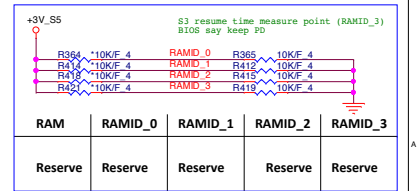
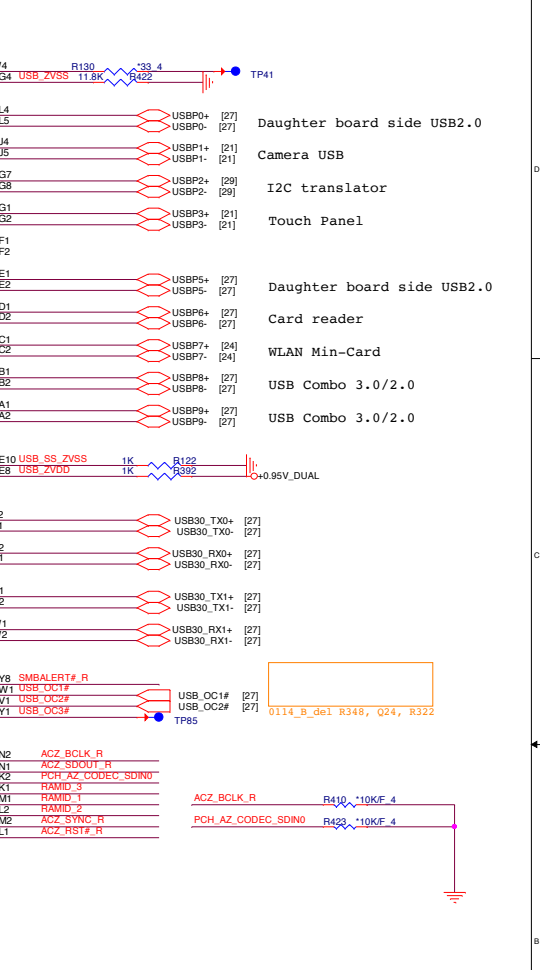
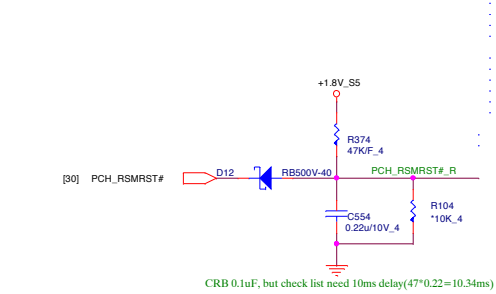
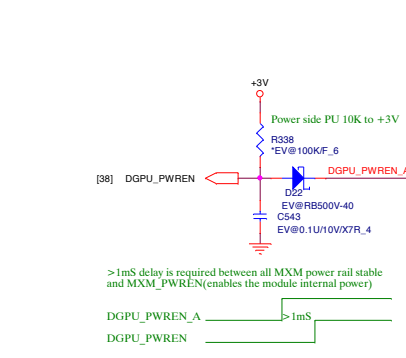
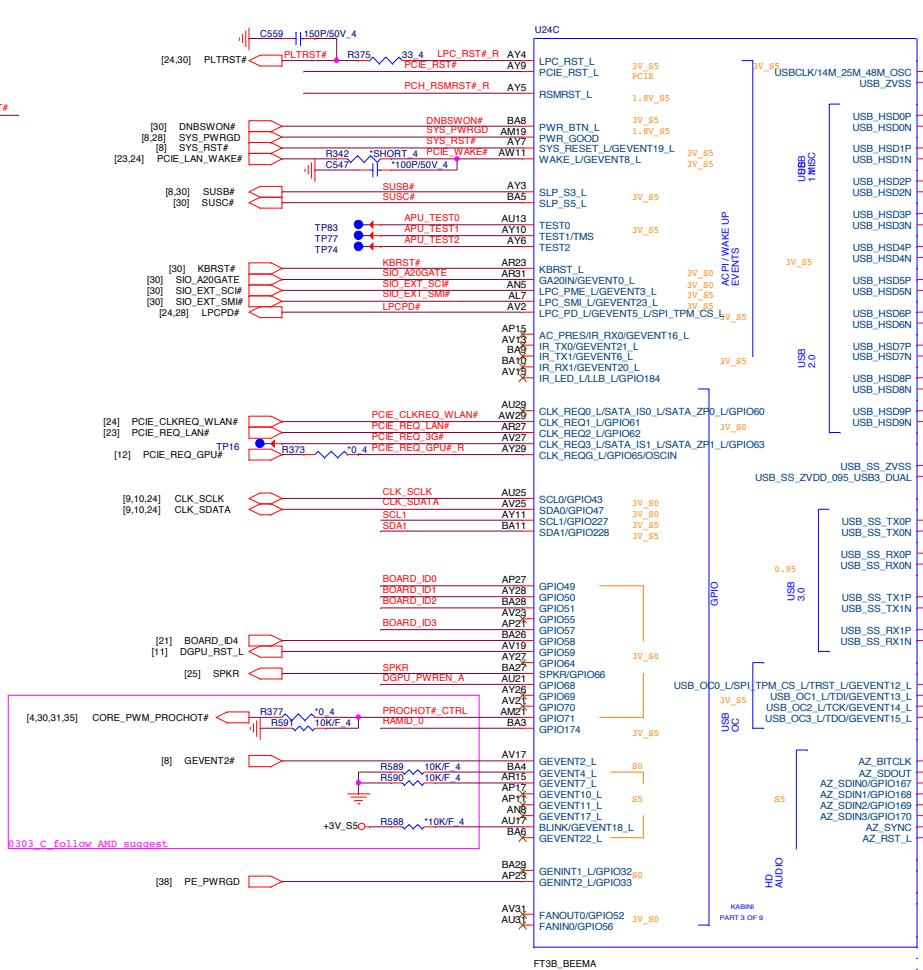


Test mode setting (Follow AMD's suggestion)

TEST2	TEST1	TEST0	Description
0	0	0	FCH JTAG accessible from APU when TAPEN is asserted FCH JTAG pins are overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserved
0	1	X	Reserved
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1	TMS	1	Use on ATE only Tuba JTAG enabled



GPIO	High	Low
BOARD_ID0	dTPM	iTPM
BOARD_ID1	dGPU	UMA
BOARD_ID2	17"	14"
BOARD_ID3	Reserve	Reserve
BOARD_ID4	Touch	non-Touch



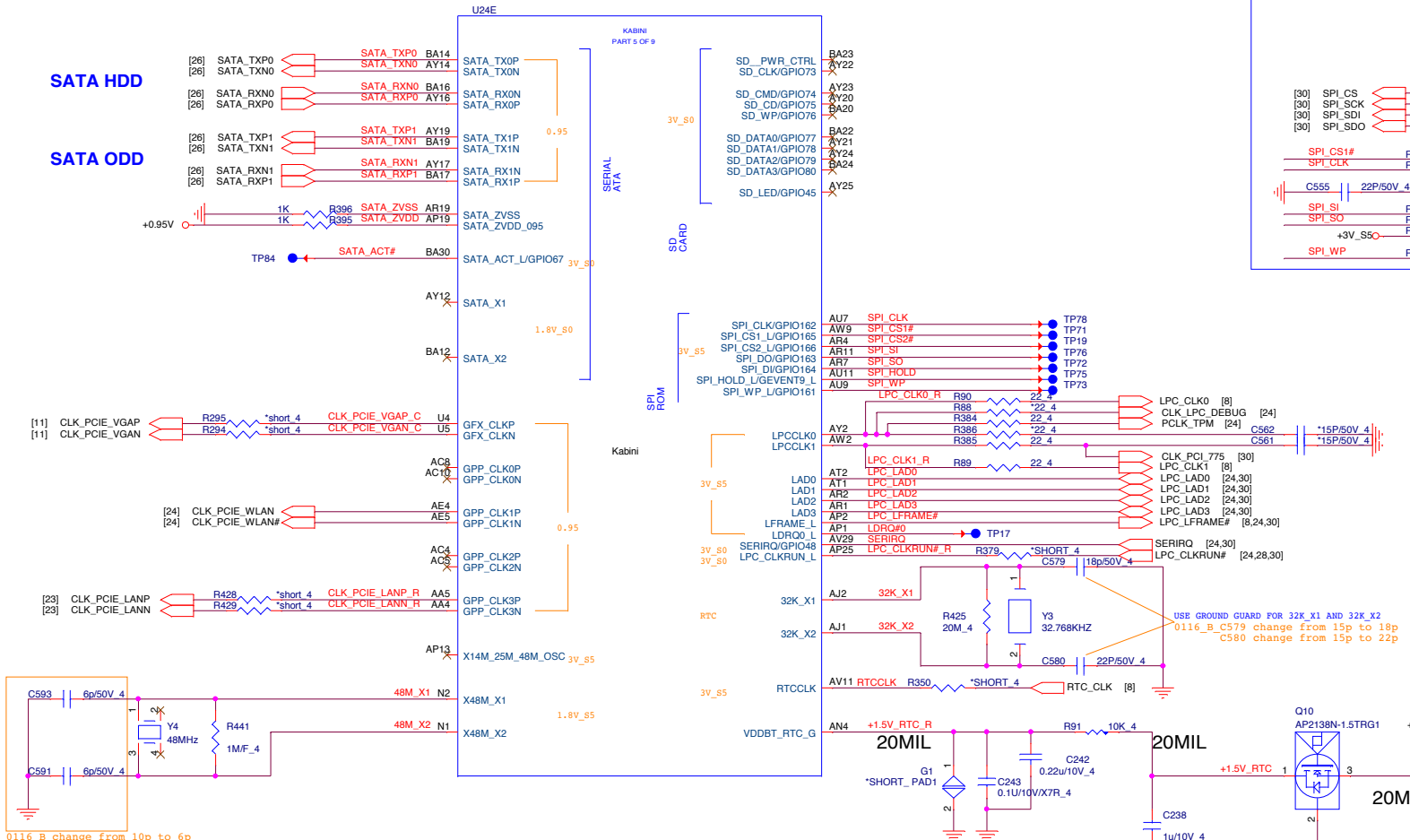
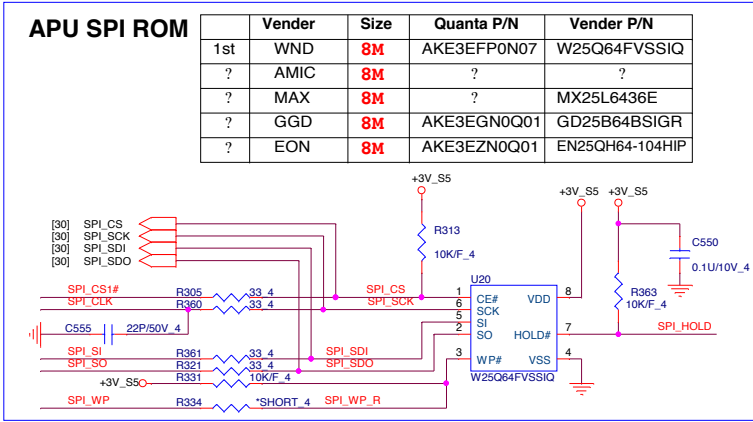
RAM	RAMID_0	RAMID_1	RAMID_2	RAMID_3
Reserve	Reserve	Reserve	Reserve	Reserve



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PROJECT : ZTV

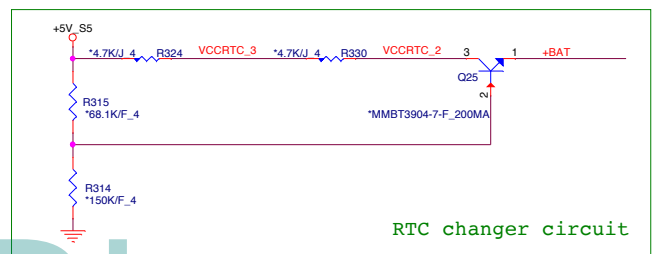
Size: Document Number: **GPIO/USB/AZ (3/6)** Rev: C3A

Date: Monday, April 28, 2014 Sheet: 5 of 40



0116_B_change from 10p to 6p

USB GROUND GUARD FOR 32K_X1 AND 32K_X2
0116_B_C579 change from 15p to 18p
C580 change from 15p to 22p

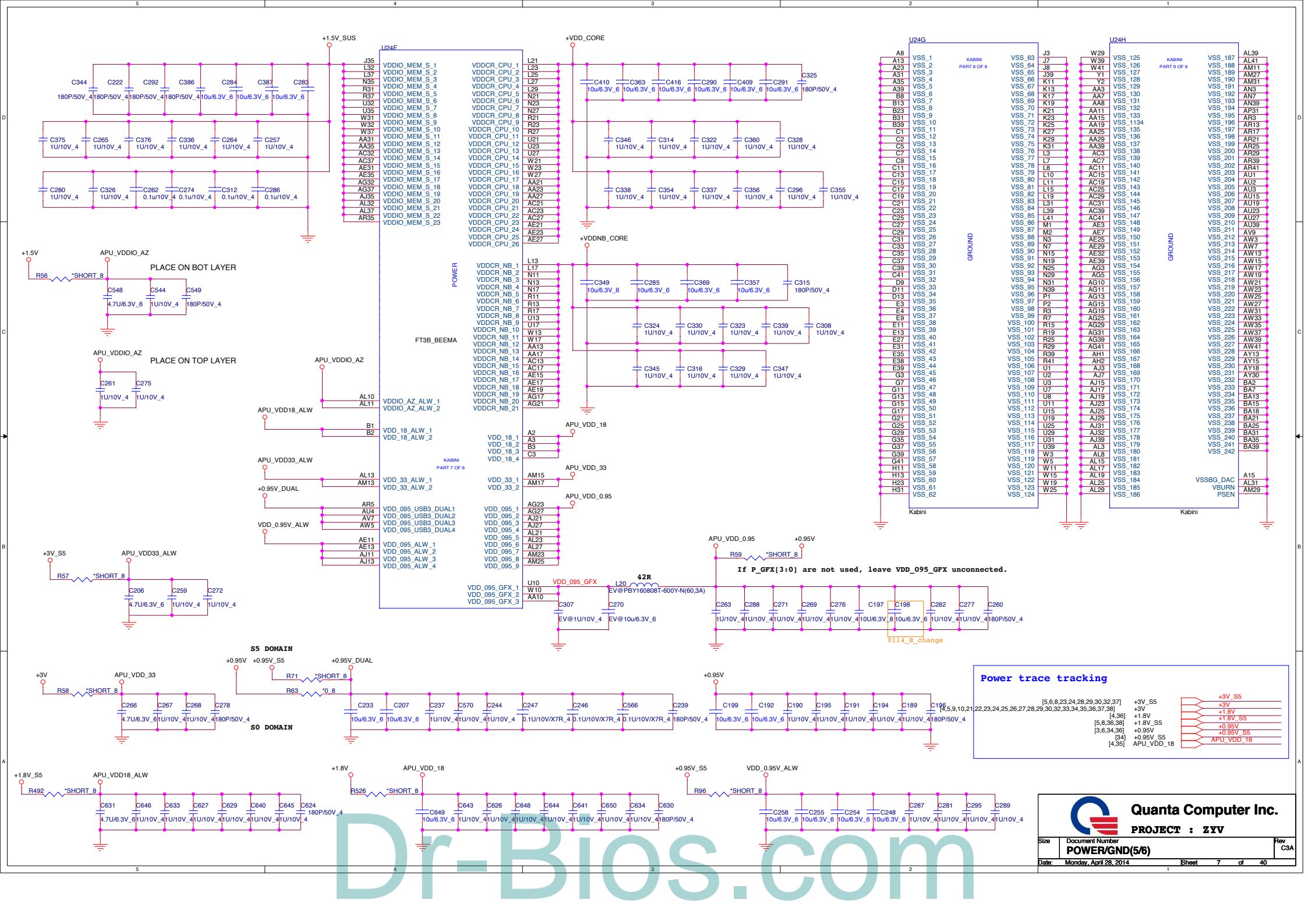


RTC CR2032 Coin Battery
DBV: AHL03003057
VDE: AHL03003003

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PROJECT : ZYV

Size	Document Number	Rev
	SATA/CLK (4/6)	C3A
Date:	Monday, April 28, 2014	Sheet 6 of 40

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POWER

J35	VDDIO_MEM_S_1	VDDCR_CPU_1
L32	VDDIO_MEM_S_2	VDDCR_CPU_2
L37	VDDIO_MEM_S_3	VDDCR_CPU_3
R31	VDDIO_MEM_S_4	VDDCR_CPU_4
R37	VDDIO_MEM_S_5	VDDCR_CPU_5
U35	VDDIO_MEM_S_6	VDDCR_CPU_6
U35	VDDIO_MEM_S_7	VDDCR_CPU_7
W31	VDDIO_MEM_S_8	VDDCR_CPU_8
W32	VDDIO_MEM_S_9	VDDCR_CPU_9
W37	VDDIO_MEM_S_10	VDDCR_CPU_10
AA31	VDDIO_MEM_S_11	VDDCR_CPU_11
AA35	VDDIO_MEM_S_12	VDDCR_CPU_12
AC32	VDDIO_MEM_S_13	VDDCR_CPU_13
AC37	VDDIO_MEM_S_14	VDDCR_CPU_14
AE31	VDDIO_MEM_S_15	VDDCR_CPU_15
AE35	VDDIO_MEM_S_16	VDDCR_CPU_16
AG32	VDDIO_MEM_S_17	VDDCR_CPU_17
AG37	VDDIO_MEM_S_18	VDDCR_CPU_18
AJ35	VDDIO_MEM_S_19	VDDCR_CPU_19
AL32	VDDIO_MEM_S_20	VDDCR_CPU_20
AL37	VDDIO_MEM_S_21	VDDCR_CPU_21
AR35	VDDIO_MEM_S_22	VDDCR_CPU_22
	VDDIO_MEM_S_23	VDDCR_CPU_23
		VDDCR_CPU_24
		VDDCR_CPU_25
		VDDCR_CPU_26

POWER

L21	VDDCR_CPU_1
L25	VDDCR_CPU_2
L26	VDDCR_CPU_3
L27	VDDCR_CPU_4
L29	VDDCR_CPU_5
N21	VDDCR_CPU_6
N23	VDDCR_CPU_7
R21	VDDCR_CPU_8
R23	VDDCR_CPU_9
R27	VDDCR_CPU_10
U23	VDDCR_CPU_11
U27	VDDCR_CPU_12
W21	VDDCR_CPU_13
W23	VDDCR_CPU_14
AA21	VDDCR_CPU_15
AA23	VDDCR_CPU_16
AA27	VDDCR_CPU_17
AC21	VDDCR_CPU_18
AC23	VDDCR_CPU_19
AC27	VDDCR_CPU_20
AE21	VDDCR_CPU_21
AE23	VDDCR_CPU_22
AE27	VDDCR_CPU_23

KABINI PART 7 OF 9

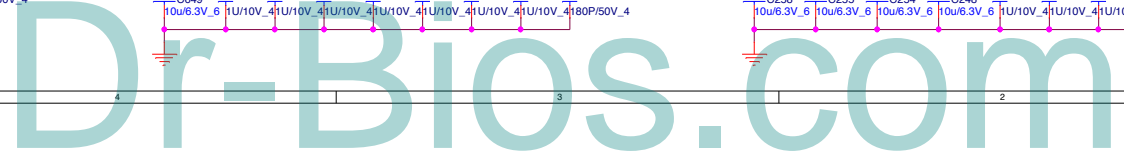
VDD_18_ALW_1	VDD_18_ALW_2
VDD_18_ALW_3	VDD_18_ALW_4
VDD_18_ALW_5	VDD_18_ALW_6
VDD_18_ALW_7	VDD_18_ALW_8
VDD_18_ALW_9	VDD_18_ALW_10
VDD_18_ALW_11	VDD_18_ALW_12
VDD_18_ALW_13	VDD_18_ALW_14
VDD_18_ALW_15	VDD_18_ALW_16
VDD_18_ALW_17	VDD_18_ALW_18
VDD_18_ALW_19	VDD_18_ALW_20
VDD_18_ALW_21	VDD_18_ALW_22
VDD_33_ALW_1	VDD_33_ALW_2
VDD_33_ALW_3	VDD_33_ALW_4
VDD_33_ALW_5	VDD_33_ALW_6
VDD_33_ALW_7	VDD_33_ALW_8
VDD_33_ALW_9	VDD_33_ALW_10
VDD_33_ALW_11	VDD_33_ALW_12
VDD_33_ALW_13	VDD_33_ALW_14
VDD_33_ALW_15	VDD_33_ALW_16
VDD_33_ALW_17	VDD_33_ALW_18
VDD_33_ALW_19	VDD_33_ALW_20
VDD_33_ALW_21	VDD_33_ALW_22
VDD_33_ALW_23	VDD_33_ALW_24
VDD_33_ALW_25	VDD_33_ALW_26
VDD_33_ALW_27	VDD_33_ALW_28
VDD_33_ALW_29	VDD_33_ALW_30
VDD_33_ALW_31	VDD_33_ALW_32
VDD_33_ALW_33	VDD_33_ALW_34
VDD_33_ALW_35	VDD_33_ALW_36
VDD_33_ALW_37	VDD_33_ALW_38
VDD_33_ALW_39	VDD_33_ALW_40
VDD_33_ALW_41	VDD_33_ALW_42
VDD_33_ALW_43	VDD_33_ALW_44
VDD_33_ALW_45	VDD_33_ALW_46
VDD_33_ALW_47	VDD_33_ALW_48
VDD_33_ALW_49	VDD_33_ALW_50
VDD_33_ALW_51	VDD_33_ALW_52
VDD_33_ALW_53	VDD_33_ALW_54
VDD_33_ALW_55	VDD_33_ALW_56
VDD_33_ALW_57	VDD_33_ALW_58
VDD_33_ALW_59	VDD_33_ALW_60
VDD_33_ALW_61	VDD_33_ALW_62
VDD_33_ALW_63	VDD_33_ALW_64
VDD_33_ALW_65	VDD_33_ALW_66
VDD_33_ALW_67	VDD_33_ALW_68
VDD_33_ALW_69	VDD_33_ALW_70
VDD_33_ALW_71	VDD_33_ALW_72
VDD_33_ALW_73	VDD_33_ALW_74
VDD_33_ALW_75	VDD_33_ALW_76
VDD_33_ALW_77	VDD_33_ALW_78
VDD_33_ALW_79	VDD_33_ALW_80
VDD_33_ALW_81	VDD_33_ALW_82
VDD_33_ALW_83	VDD_33_ALW_84
VDD_33_ALW_85	VDD_33_ALW_86
VDD_33_ALW_87	VDD_33_ALW_88
VDD_33_ALW_89	VDD_33_ALW_90
VDD_33_ALW_91	VDD_33_ALW_92
VDD_33_ALW_93	VDD_33_ALW_94
VDD_33_ALW_95	VDD_33_ALW_96
VDD_33_ALW_97	VDD_33_ALW_98
VDD_33_ALW_99	VDD_33_ALW_100

KABINI PART 8 OF 9

VDD_095_USB3_DUAL1	VDD_095_USB3_DUAL2
VDD_095_USB3_DUAL3	VDD_095_USB3_DUAL4
VDD_095_ALW_1	VDD_095_ALW_2
VDD_095_ALW_3	VDD_095_ALW_4
VDD_095_ALW_5	VDD_095_ALW_6
VDD_095_ALW_7	VDD_095_ALW_8
VDD_095_ALW_9	VDD_095_ALW_10
VDD_095_ALW_11	VDD_095_ALW_12
VDD_095_ALW_13	VDD_095_ALW_14
VDD_095_ALW_15	VDD_095_ALW_16
VDD_095_ALW_17	VDD_095_ALW_18
VDD_095_ALW_19	VDD_095_ALW_20
VDD_095_ALW_21	VDD_095_ALW_22
VDD_095_ALW_23	VDD_095_ALW_24
VDD_095_ALW_25	VDD_095_ALW_26
VDD_095_ALW_27	VDD_095_ALW_28
VDD_095_ALW_29	VDD_095_ALW_30
VDD_095_ALW_31	VDD_095_ALW_32
VDD_095_ALW_33	VDD_095_ALW_34
VDD_095_ALW_35	VDD_095_ALW_36
VDD_095_ALW_37	VDD_095_ALW_38
VDD_095_ALW_39	VDD_095_ALW_40
VDD_095_ALW_41	VDD_095_ALW_42
VDD_095_ALW_43	VDD_095_ALW_44
VDD_095_ALW_45	VDD_095_ALW_46
VDD_095_ALW_47	VDD_095_ALW_48
VDD_095_ALW_49	VDD_095_ALW_50
VDD_095_ALW_51	VDD_095_ALW_52
VDD_095_ALW_53	VDD_095_ALW_54
VDD_095_ALW_55	VDD_095_ALW_56
VDD_095_ALW_57	VDD_095_ALW_58
VDD_095_ALW_59	VDD_095_ALW_60
VDD_095_ALW_61	VDD_095_ALW_62
VDD_095_ALW_63	VDD_095_ALW_64
VDD_095_ALW_65	VDD_095_ALW_66
VDD_095_ALW_67	VDD_095_ALW_68
VDD_095_ALW_69	VDD_095_ALW_70
VDD_095_ALW_71	VDD_095_ALW_72
VDD_095_ALW_73	VDD_095_ALW_74
VDD_095_ALW_75	VDD_095_ALW_76
VDD_095_ALW_77	VDD_095_ALW_78
VDD_095_ALW_79	VDD_095_ALW_80
VDD_095_ALW_81	VDD_095_ALW_82
VDD_095_ALW_83	VDD_095_ALW_84
VDD_095_ALW_85	VDD_095_ALW_86
VDD_095_ALW_87	VDD_095_ALW_88
VDD_095_ALW_89	VDD_095_ALW_90
VDD_095_ALW_91	VDD_095_ALW_92
VDD_095_ALW_93	VDD_095_ALW_94
VDD_095_ALW_95	VDD_095_ALW_96
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VDD_095_ALW_99	VDD_095_ALW_100

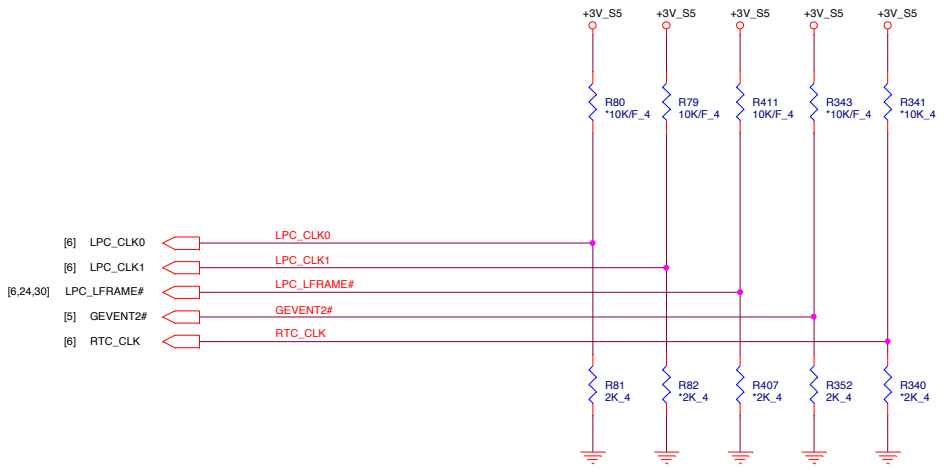
Power trace tracking

[5,6,8,23,24,28,29,30,32,37]	+3V_S5
[3,6]	+3V
[5,8,36,38]	+1.8V_S5
[9,6,34,36]	+1.8V_S5
[34]	+0.95V_S5
[4,35]	+0.95V_S5
[4,35]	APU_VDD_18



STRAPS PINS

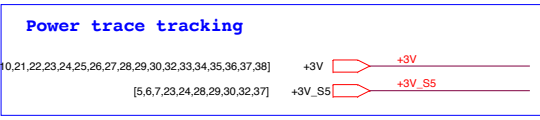
OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



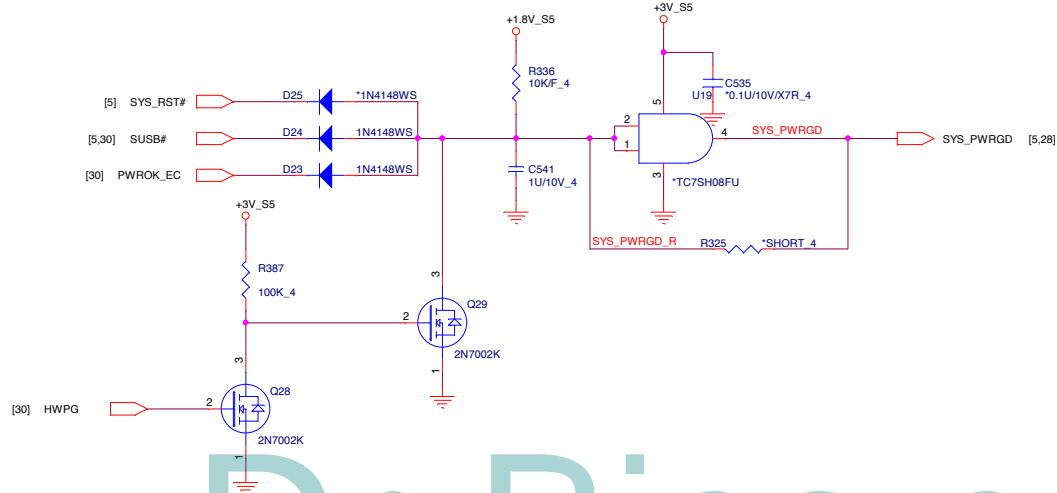
REQUIRED STRAPS

					RTC_CLK	LPC_CLK0	LPC_CLK1	LFRAME#	GEVENT2#
PULL HIGH					Normal power up	BOOT FAIL TIMER ENABLED	CLKGEN ENABLED	SPI ROM	1.8V SPI ROM
					DEFAULT		DEFAULT	DEFAULT	
PULL LOW					Fast power on	BOOT FAIL TIMER DISABLED	CLKGEN DISABLED	LPC ROM	3.3V SPI ROM
						DEFAULT			DEFAULT


DEBUG STRAPS

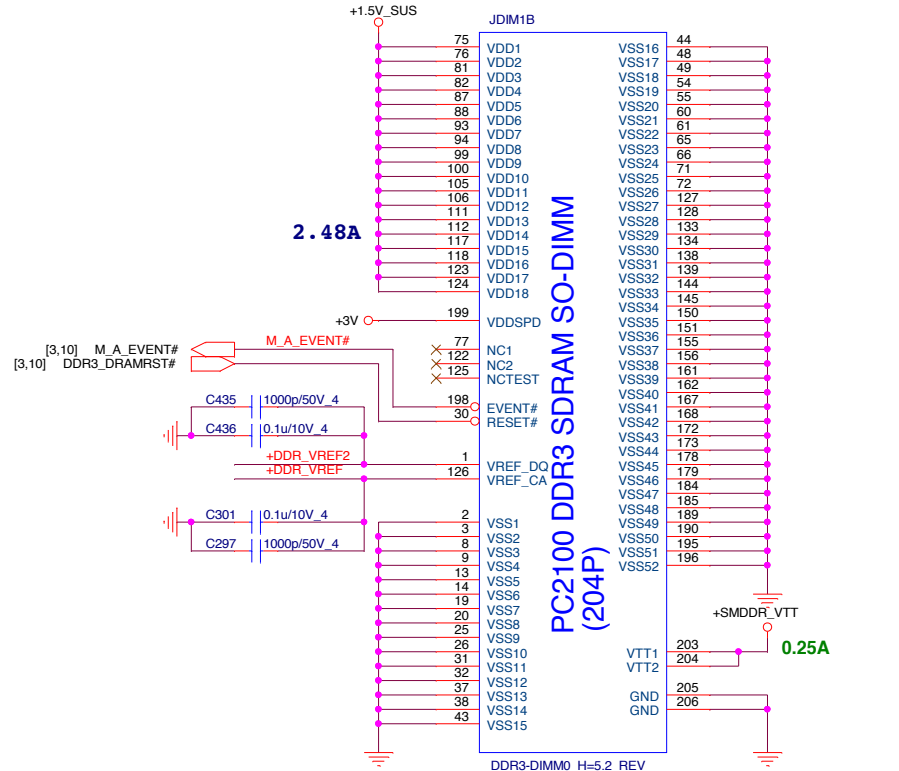
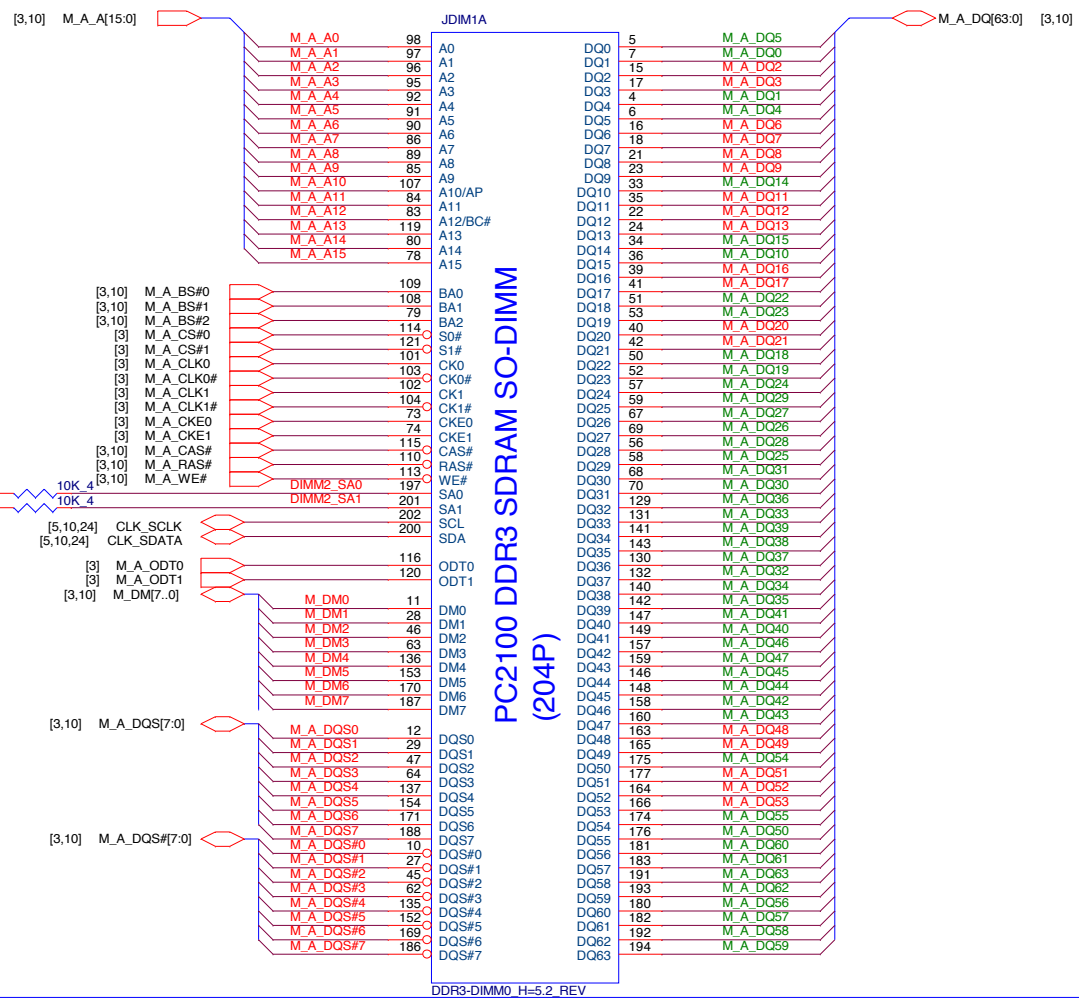


SYS_PWRGD

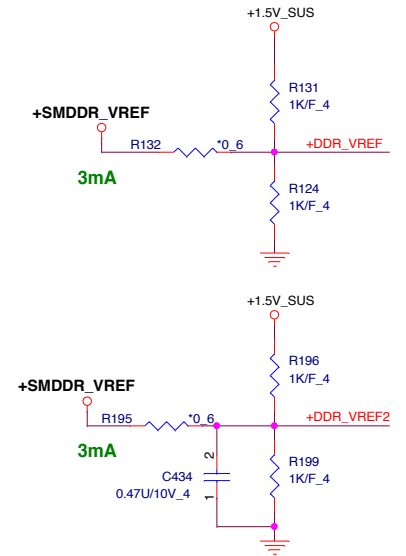
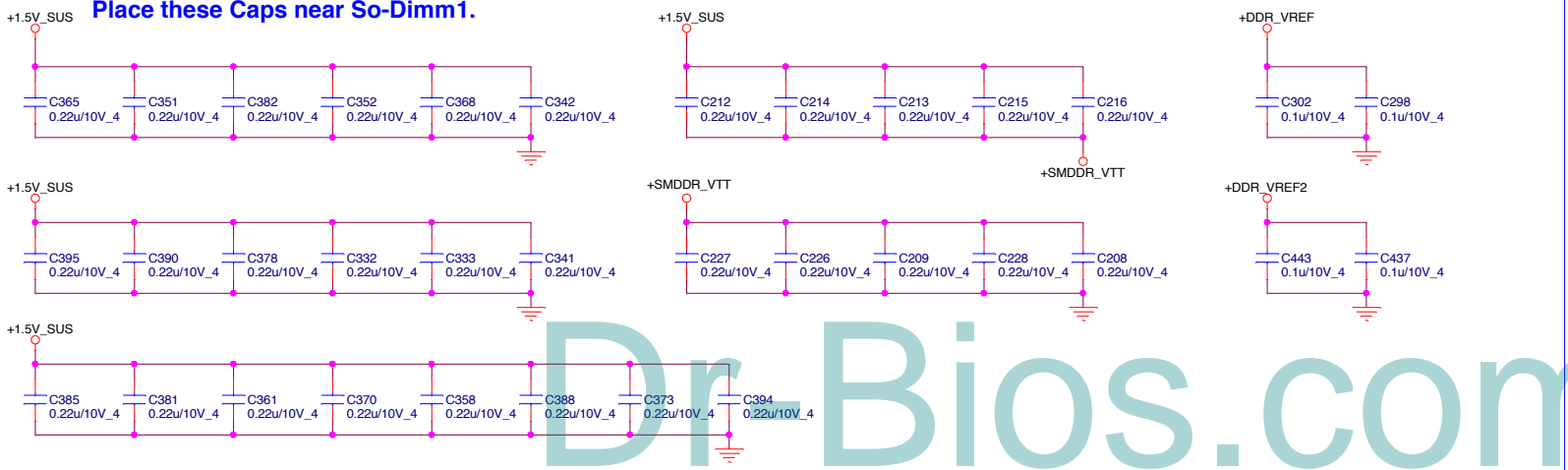


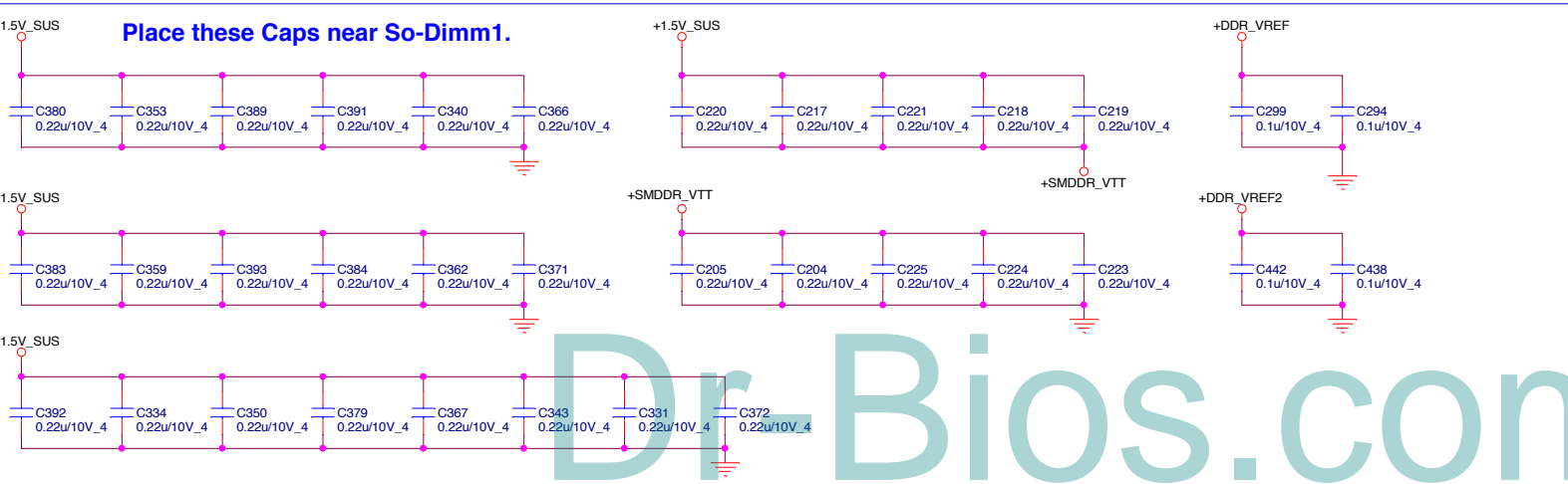
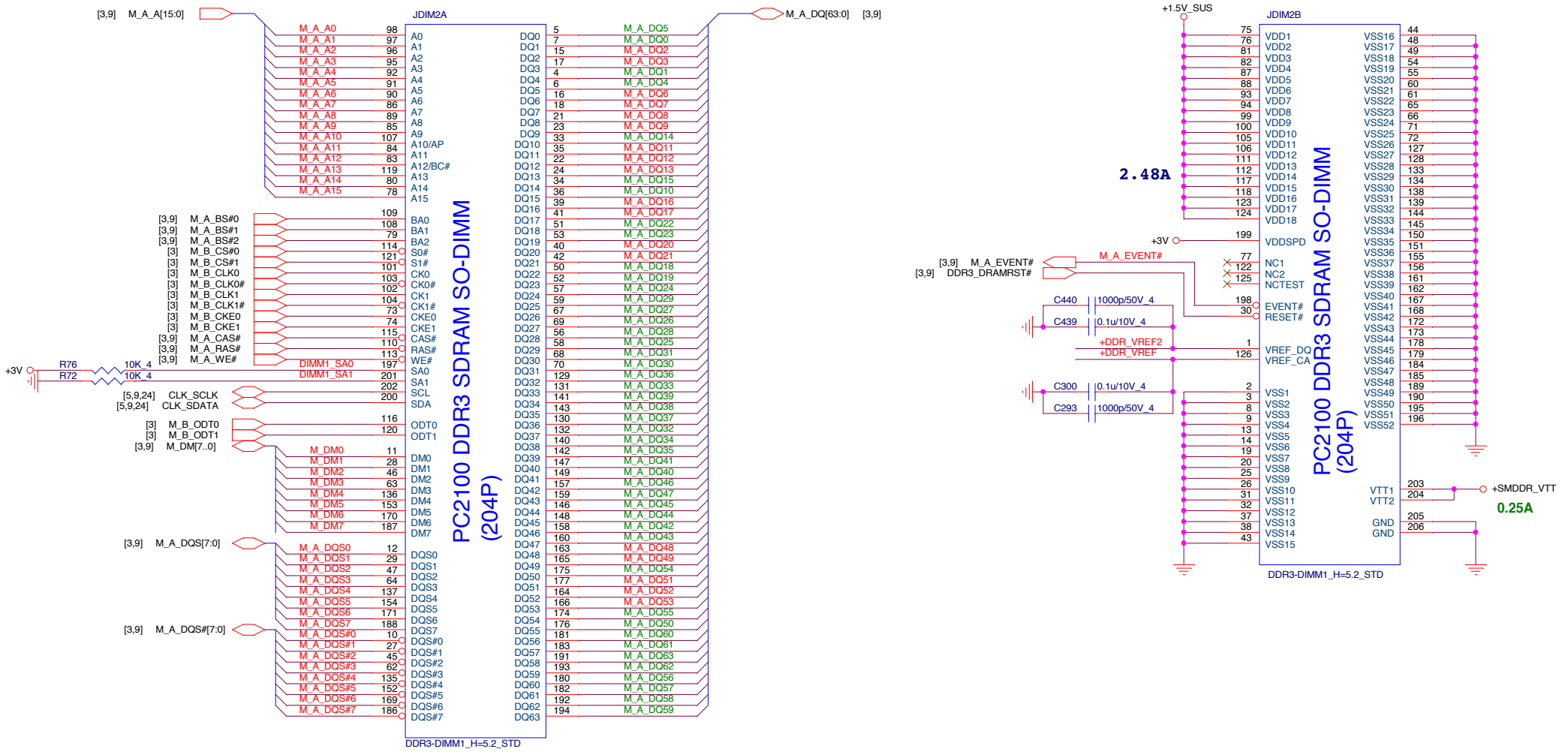
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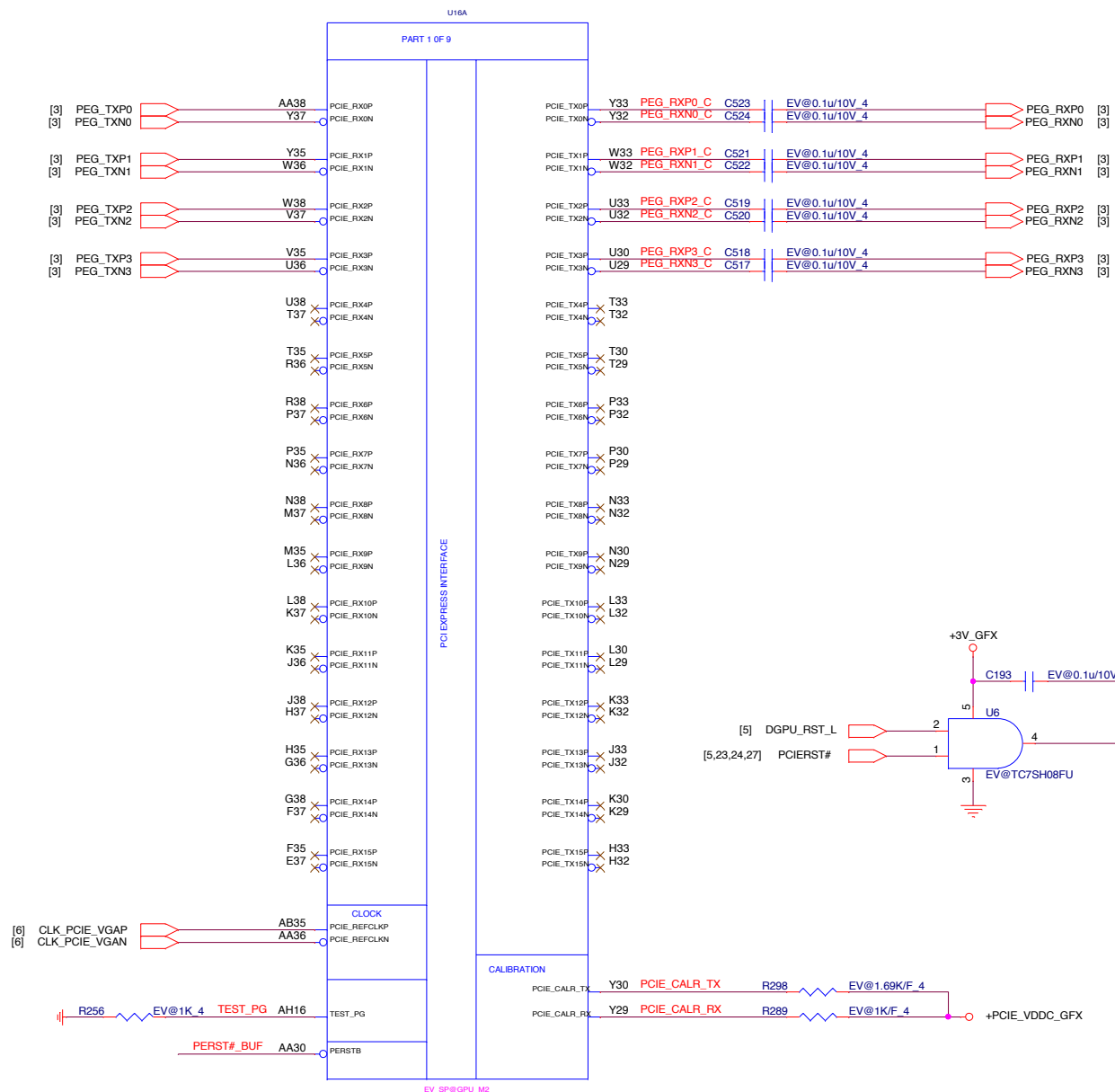

Quanta Computer Inc.
PROJECT : ZIV
 Size: Document Number
STRAP (6/6)
 Date: Monday, April 28, 2014 Sheet 6 of 40 Rev: CSA




Place these Caps near So-Dimm1.

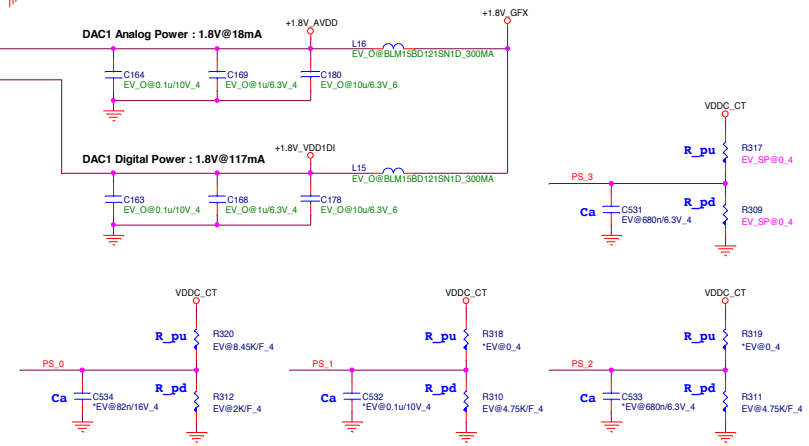
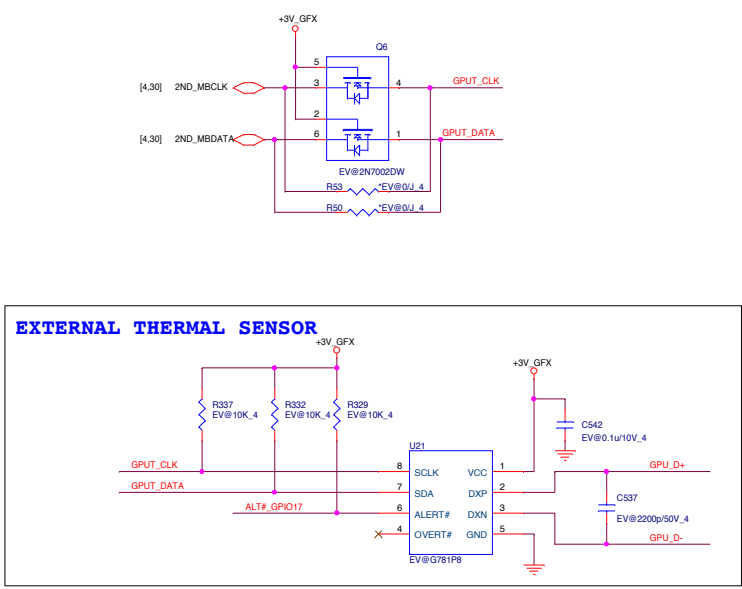
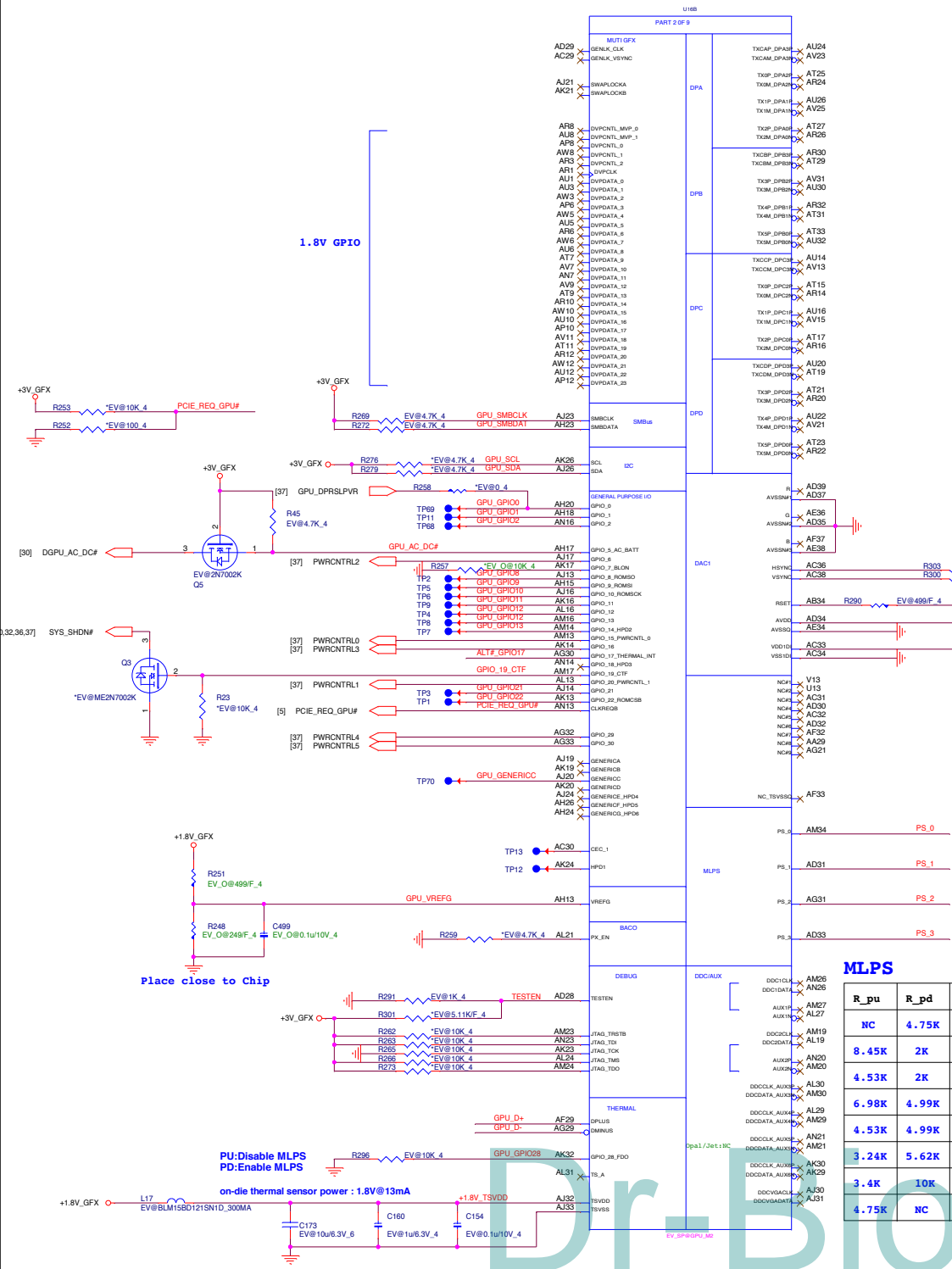






 Quanta Computer Inc. PROJECT : ZYV			Rev
			C3A
Size	Document Number	Opal(Jet)_M2/PEG*4	
Date:	Monday, April 28, 2014	Sheet	11 of 40

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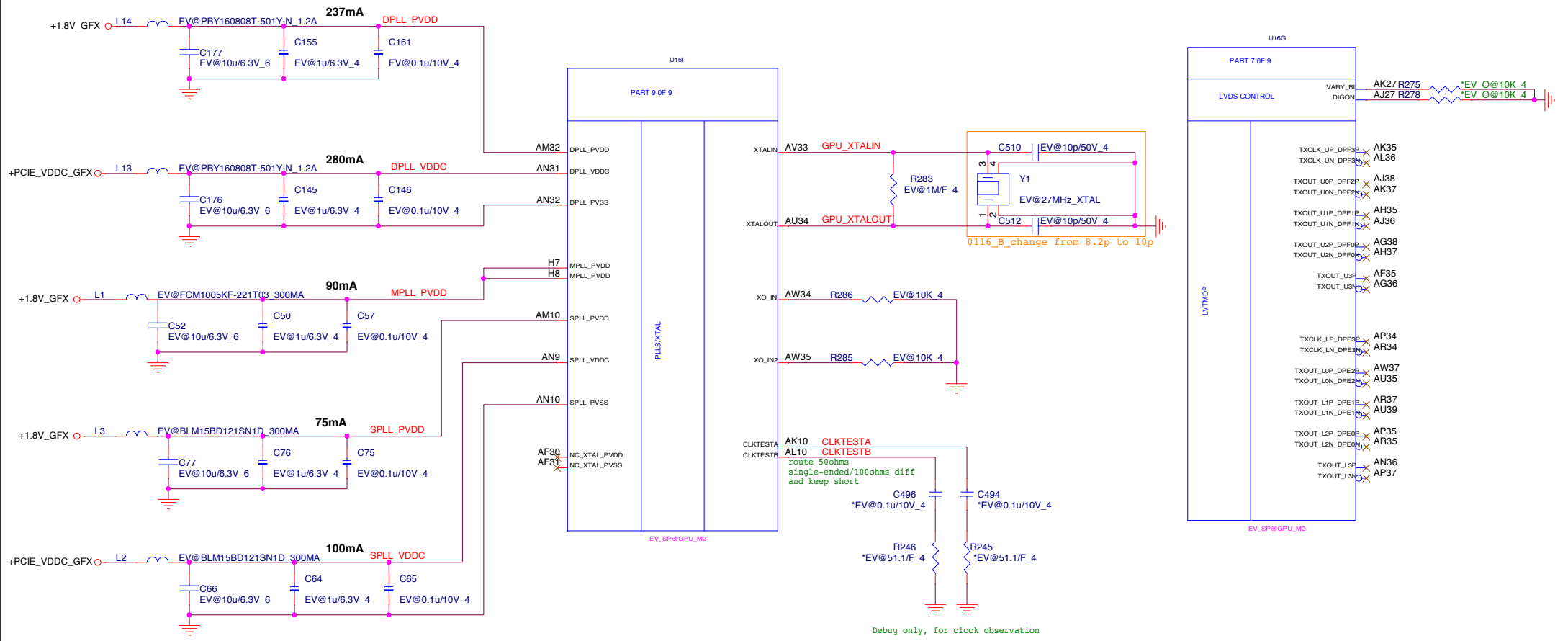
MLPS


R _{pu}	R _{pd}	Bits [3:1]
NC	4.75K	000
8.45K	2K	001
4.53K	2K	010
6.98K	4.99K	011
4.53K	4.99K	100
3.24K	5.62K	101
3.4K	10K	110
4.75K	NC	111

R _a	P/N
2K	CS22002PB19
3.24K	CS23242PB09
3.4K	CS23402PB08
4.53K	CS24532PB08
4.75K	CS24752PB12
4.99K	CS24992PB26
5.62K	CS25622PB18
6.98K	CS26982PB01
8.45K	CS28452PB12
10K	CS31002JB28

MLPS Bit	Bits [5:1]
PS_0	11001
PS_1	11000
PS_2	11000
PS_3	00XXX

Ca	Bits [5:4]	P/N
680nF	00	CH4681K9B00
82nF	01	CH3823K1B00
10nF	10	CH31003KB11
NC	11	



 Quanta Computer Inc. PROJECT : ZIV		
Size	Document Number	Rev
	Opal(Jet)_M2/XTAL_LVDS	C3A
Date:	Monday, April 28, 2014	Sheet 13 of 40

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PS_3 [3:1]

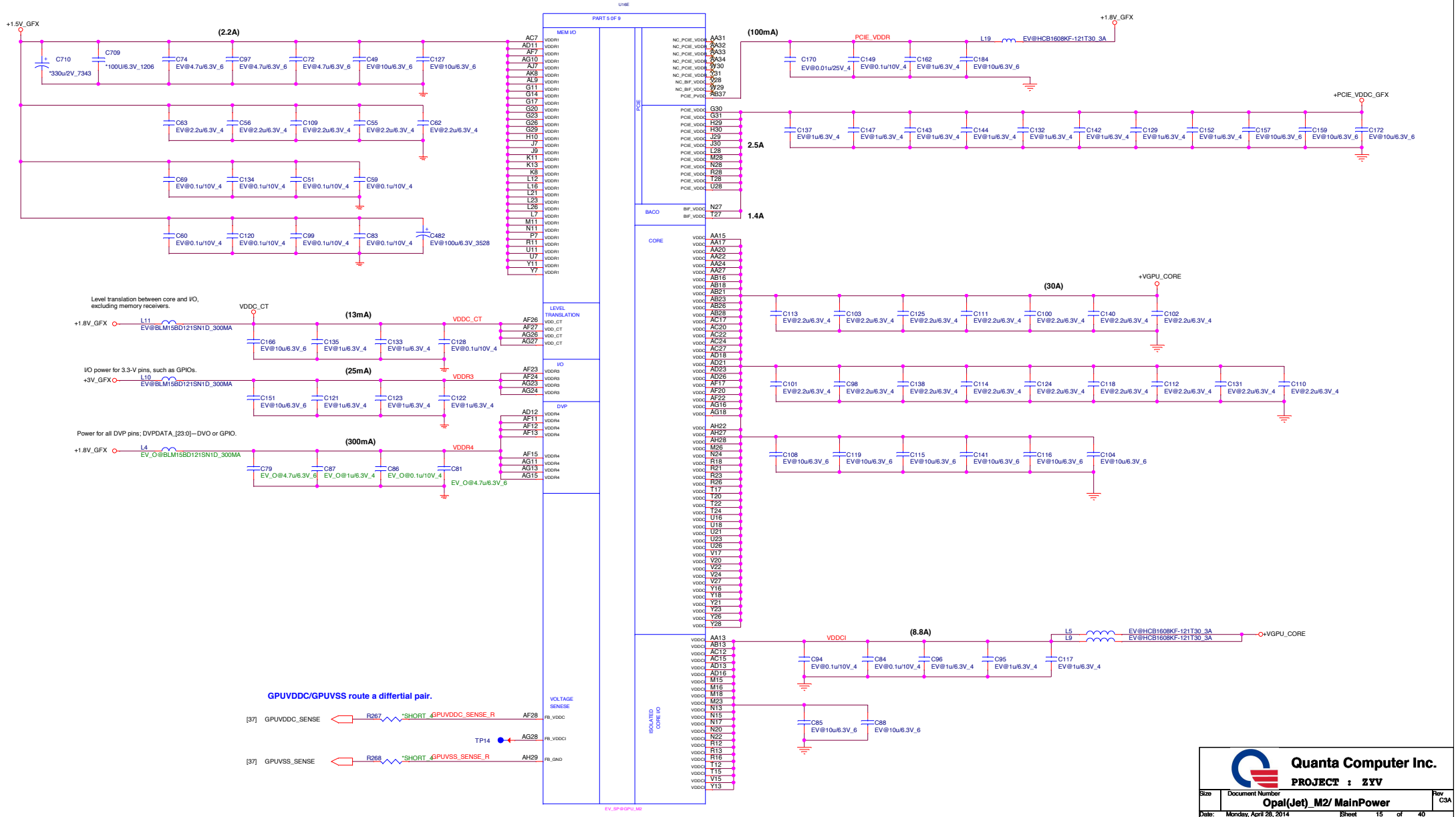
				Opal	Jet
Vendor	Vendor P/N	STN B/S P/N	Size	MLPS	MLPS
Hynix	H5TC2G63FFR-11C (128Mb*16) 2Gb	AKD5MZDTW05 *4	1G		000
		AKD5MZDTW05 *8	2G	001	
	H5TC4G63AFR-11C (256Mb*16) 4Gb	AKD5PGWTW13 *4	2G		
		AKD5PGWTW13 *8	4G		
Samsung	K4W2G1646Q-BC1A (128Mb*16) 2Gb	AKD5MGST513 *4	1G		010
		AKD5MGST513 *8	2G	011	
	K4W4G1646D-BC1A (256Mb*16) 4Gb	AKD5PGWT504 *4	2G		
		AKD5PGWT504 *8	4G		
Micron	MT41J128M16JT-093G:K (128Mb*16) 2Gb	AKD5MGSTL25 *4	1G		100
		AKD5MGSTL25 *8	2G	101	
	MT41J256M16HA-093G:E (256Mb*16) 4Gb	AKD5PZSTL02 *4	2G		
		AKD5PZSTL02 *8	4G		

CONFIGURATION STRAPS -- SEE EACH DATABOOK FOR STRAP DETAILS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET					Default Setting
STRAPS	MLPS	GPIO PIN	DESCRIPTION OF DEFAULT SETTINGS		Default Setting
MLPS_DISABLE	NA	GPIO_28_F00	Enable MLPS, NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP		X
TX_PWRS_ENB	PS_1[4]	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing		X
TX_DEEMPH_EN	PS_1[5]	GPIO1	PCIe Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled		X
BIF_GEN3_EN_A	PS_1[1]	GPIO2	PCIe Gen3 Enable (NOTE: RESERVED for Thames/Whistler/Seymour) 0: GEN3 not supported at power-on 1: GEN3 supported at power-on		1
BIF_VGA_DIS	PS_2[4]	GPIO9	VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU)		0
ROMIDCFG[2:0]	PS_0[3..1]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type 100 - 512Kbit M25P05A (ST) 101 - 1Mbit M25P10A (ST) 101 - 2Mbit M25P20 (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 100 - 512Kbit Pm25LV12 (Chingis) 101 - 1Mbit Pm25LV10 (Chingis)		XXX
BIOS_ROM_EN	PS_2[3]	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled		X
AUD[1] AUD[0]	NA NA	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.		XX
CEC_DIS	PS_0[4]	GENLK_VSYNCC	Enable CEC function. Reserved for Thames/Whistler/Seymour 0: Disabled 1: Enabled		X
RESERVED RESERVED RESERVED RESERVED	PS_1[3] PS_1[2] NA NA	GENLK_CLK GPIO8 GPIO21 GENERICCC	NOTE: ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR IF THESE GPIOs ARE USED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET Reserved Reserved Reserved Reserved (for Thames/Whistler/Seymour only)		0 0 0 0
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	NA NA NA	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable		XXX

System Memory Aperture size

GPIO9 BIOSROM		GPIO11 ROMIDCFG0	GPIO12 ROMIDCFG1	GPIO13 ROMIDCFG2
0	128MB	0	0	0
0	256MB (and above)	1	0	0
0	64MB	0	1	0
0	Reservd	1	1	0

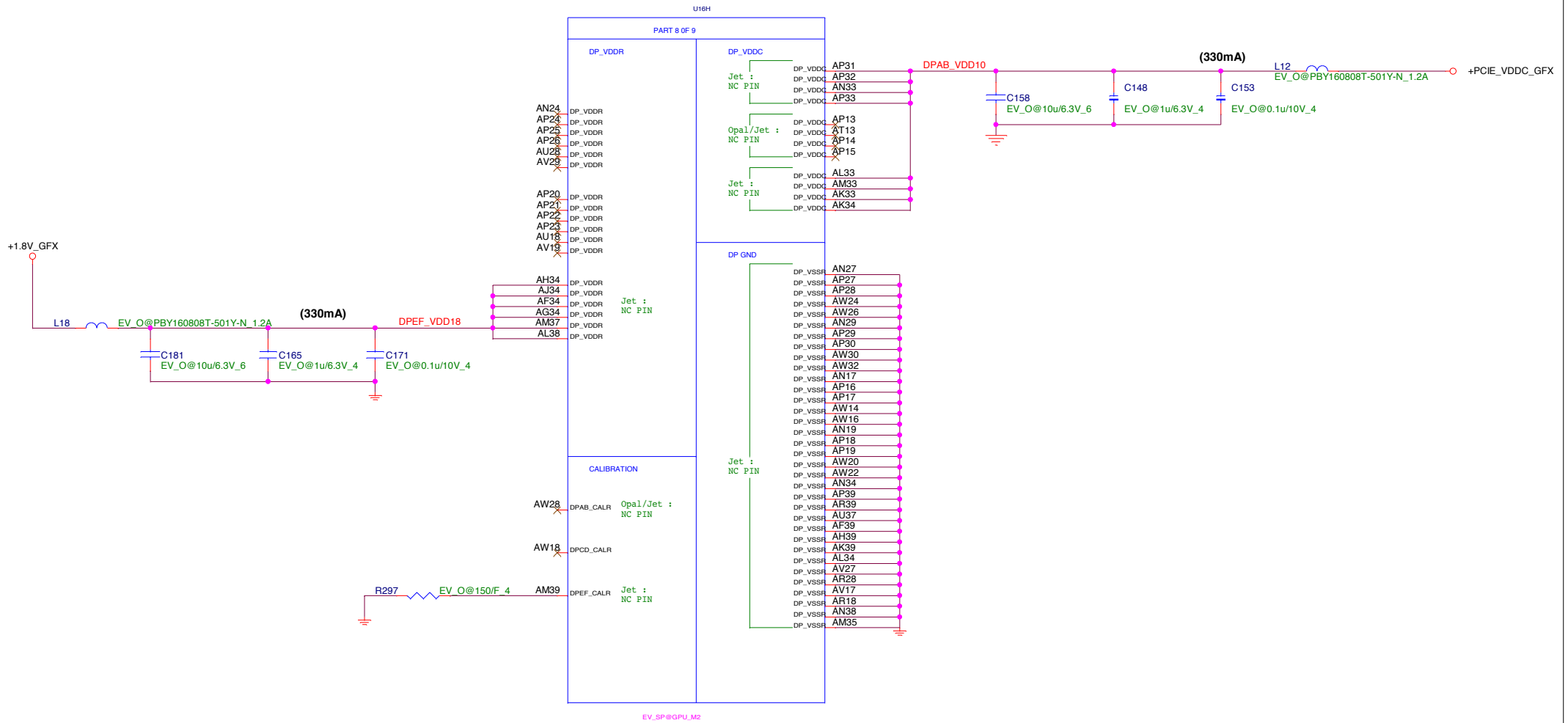





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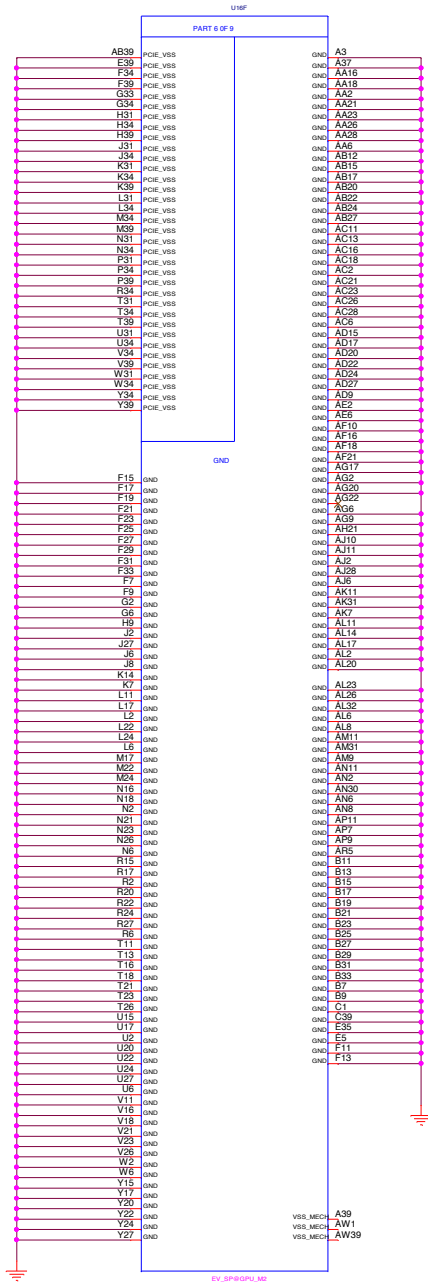
Quanta Computer Inc.
PROJECT : zyv

Size	Document Number	Rev
	Opal(Jet)_M2/ MainPower	C3A
Date:	Monday, April 28, 2014	Sheet 15 of 40



 Quanta Computer Inc. PROJECT : ZIV		
Size	Document Number	Rev
	Opal(Jet)_M2/ DP_Powers	C3A
Date:	Monday, April 28, 2014	Sheet 16 of 40

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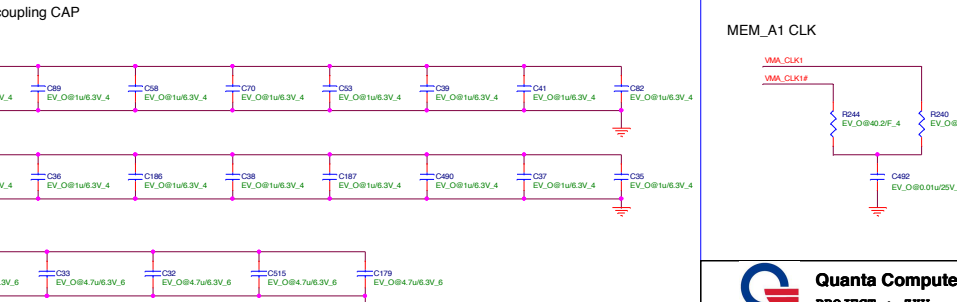
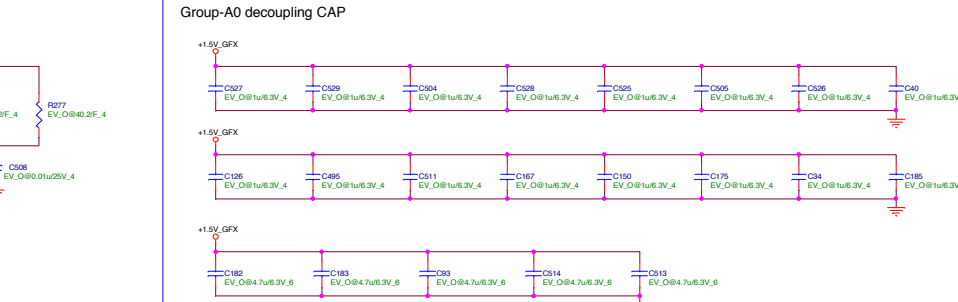
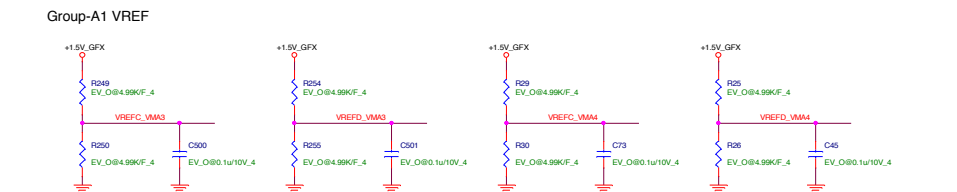
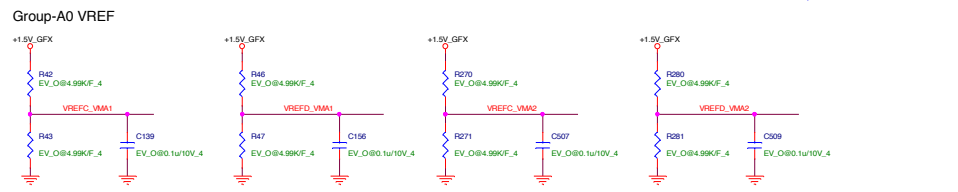
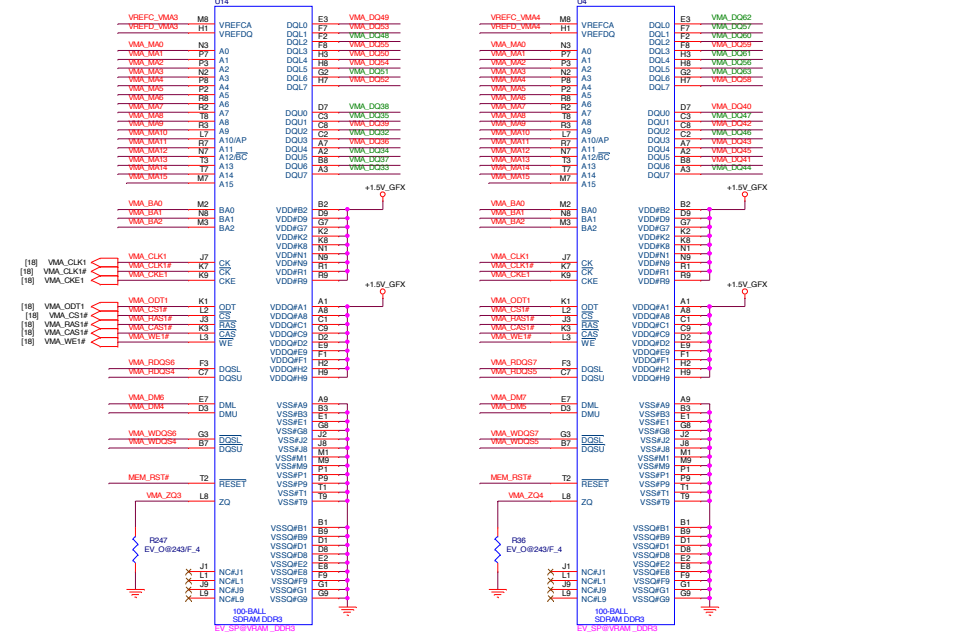
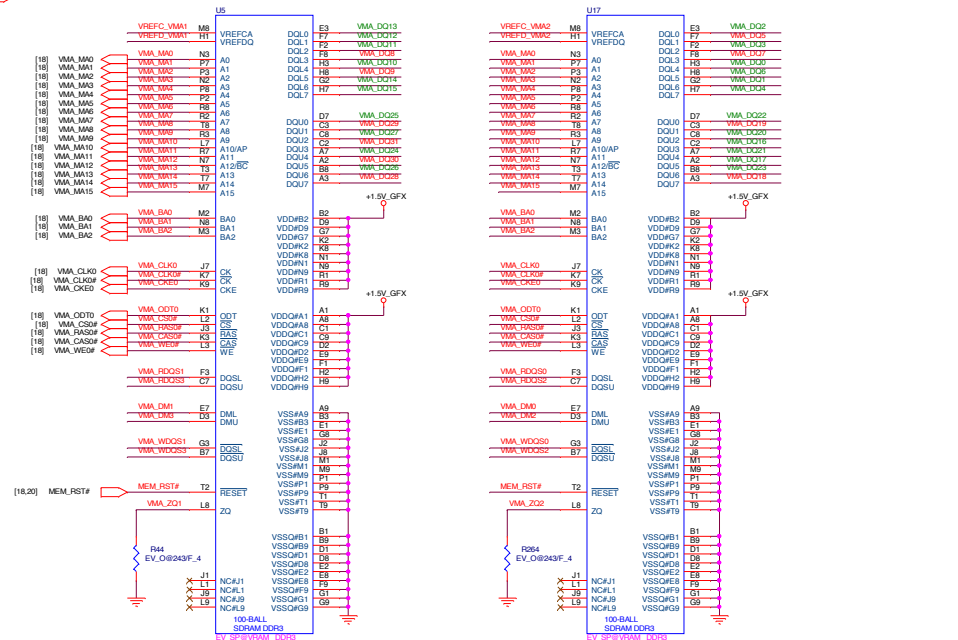


- [18] VMA_DQ[63..0]
- [18] VMA_DM[7..0]
- [18] VMA_RDQ[27..0]
- [18] VMA_WDQ[27..0]

Jet don't use Channel A

CHANNEL A: 1GB DDR3 (128M*16*4pcs) 2GB DDR3 (256M*16*4pcs)

Jet don't use Channel B

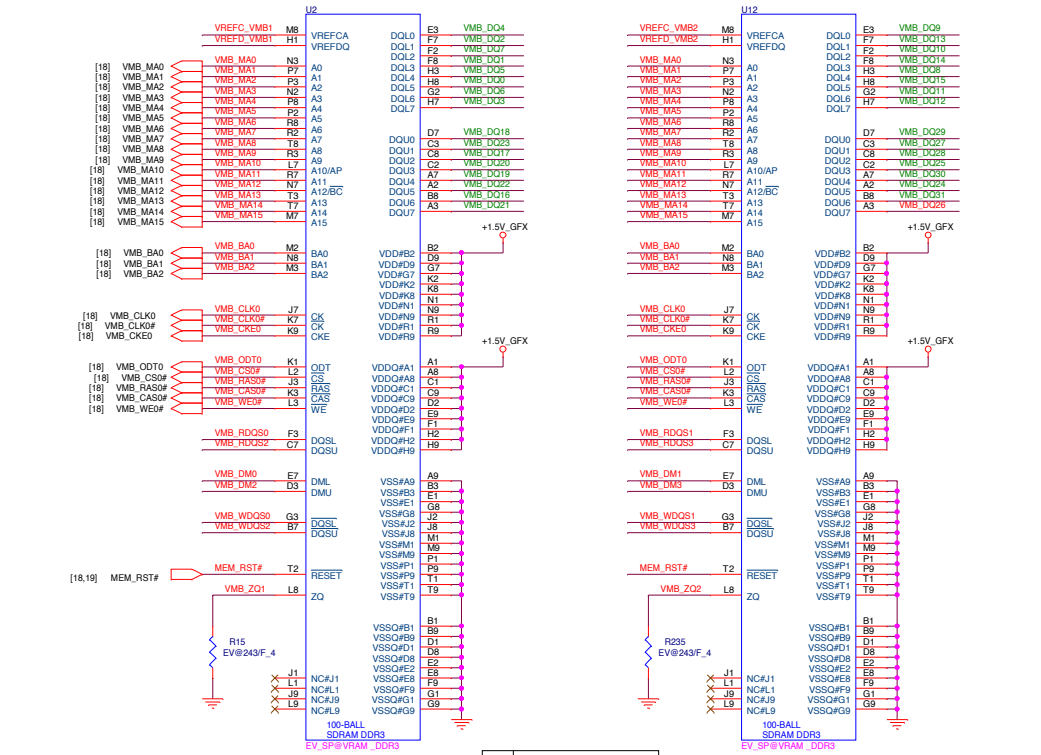


- [18] VMB_DM[63..0] VMB_DQ[63..0]
- [18] VMB_DM[7..0] VMB_DM[7..0]
- [18] VMB_RDQS[7..0] VMB_RDQS[7..0]
- [18] VMB_WDQS[7..0] VMB_WDQS[7..0]

Jet use Channel B only

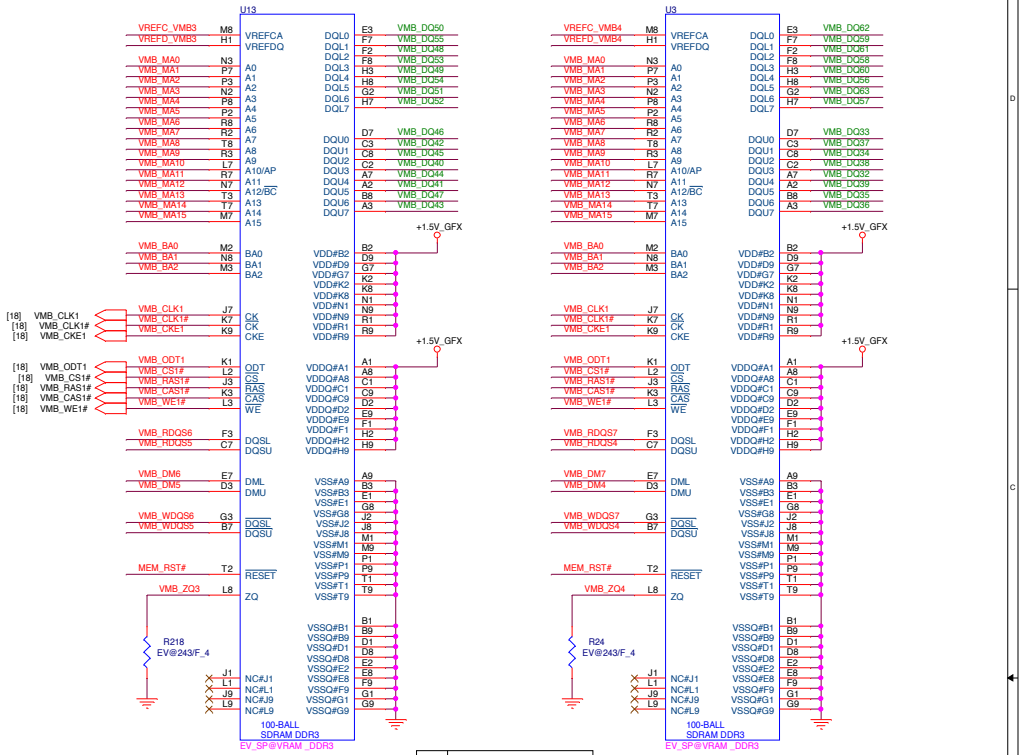
**CHANNEL B: 1GB DDR3 (128M*16*4pcs)
2GB DDR3 (256M*16*4pcs)**

Jet use Channel B only



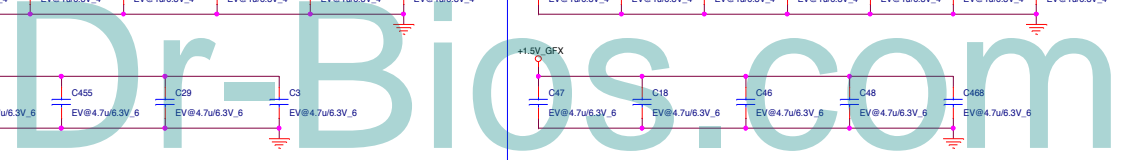
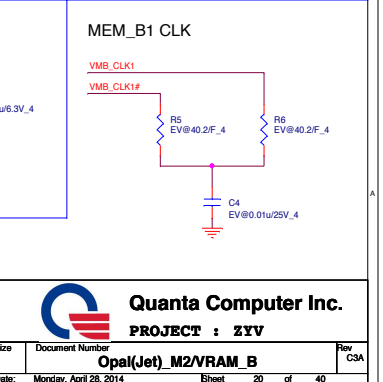
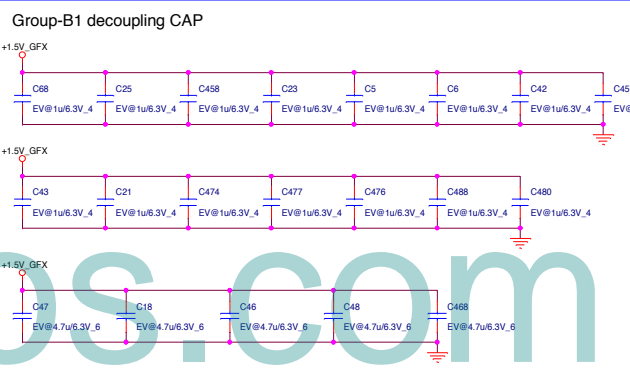
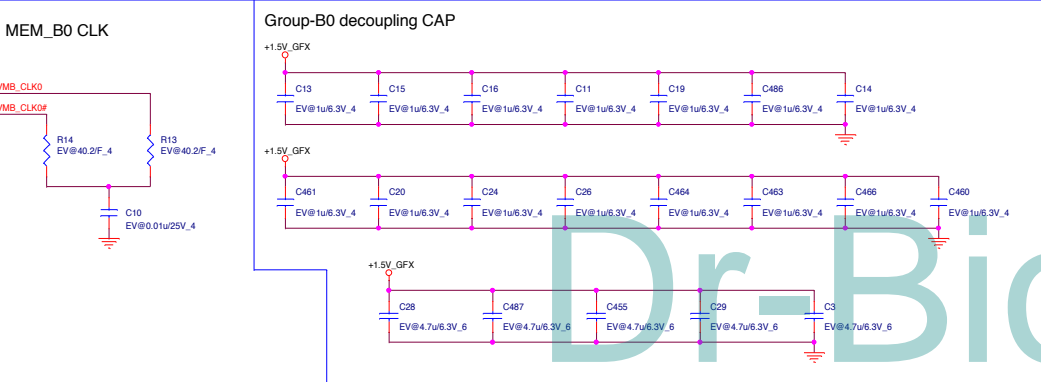
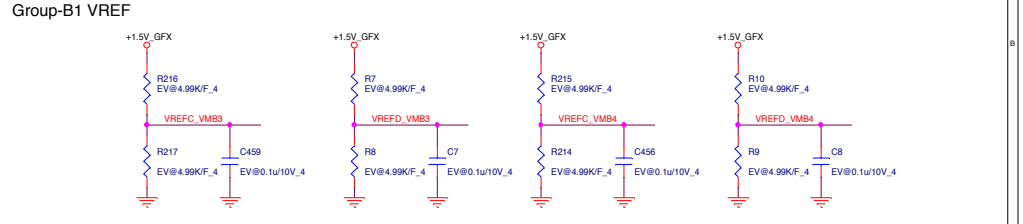
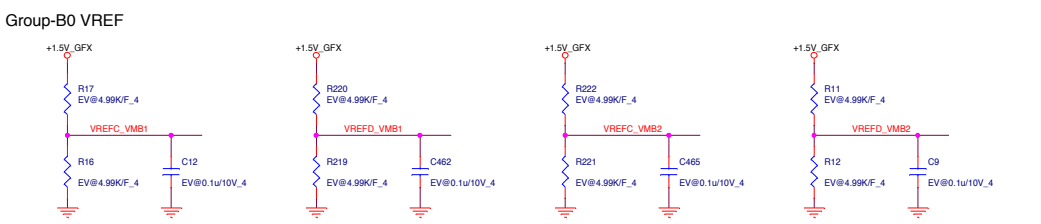
BOT Down

TOP Down

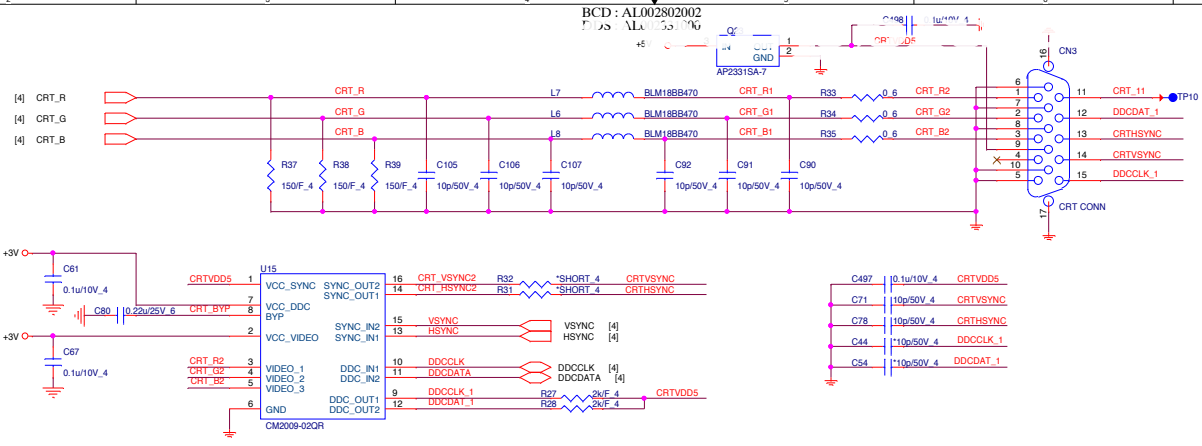


TOP Up

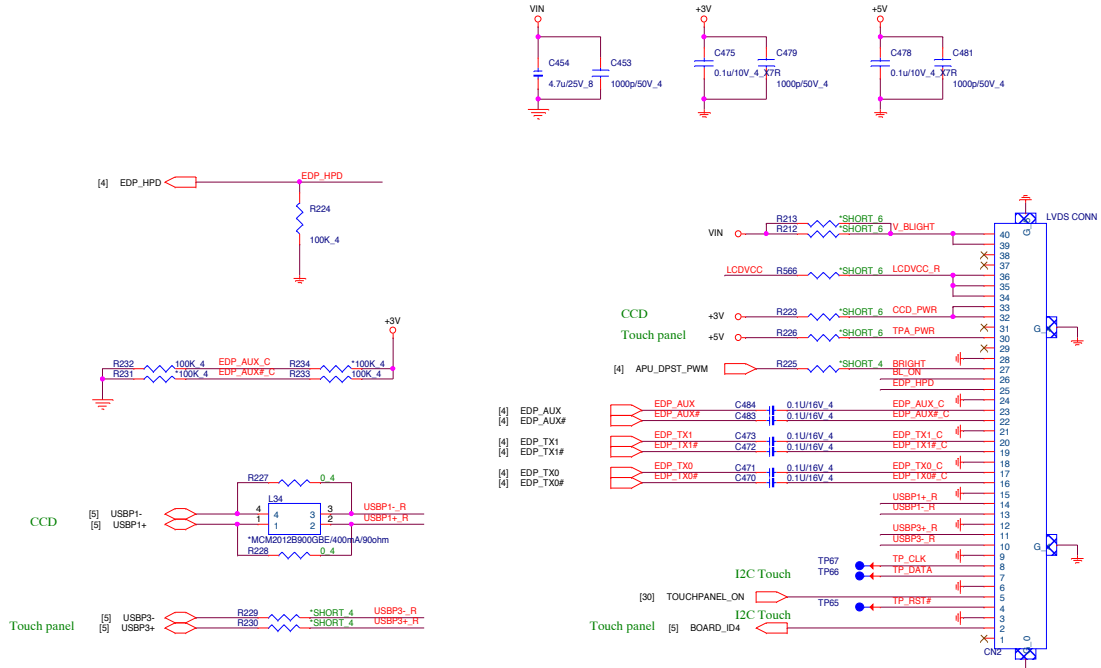
BOT Up



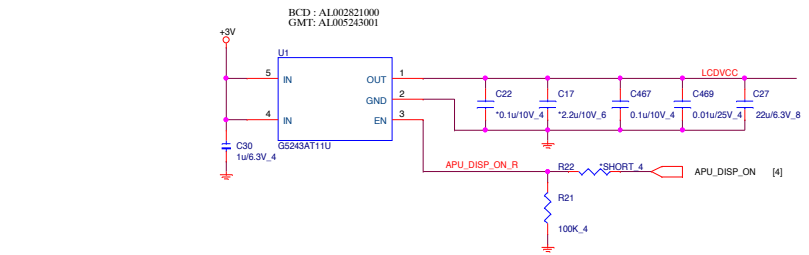
CRT



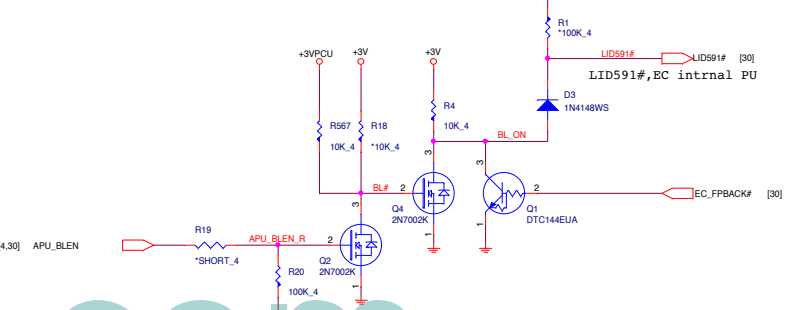
LCD CONNECTOR



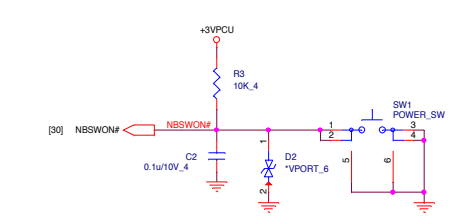
LCD Power



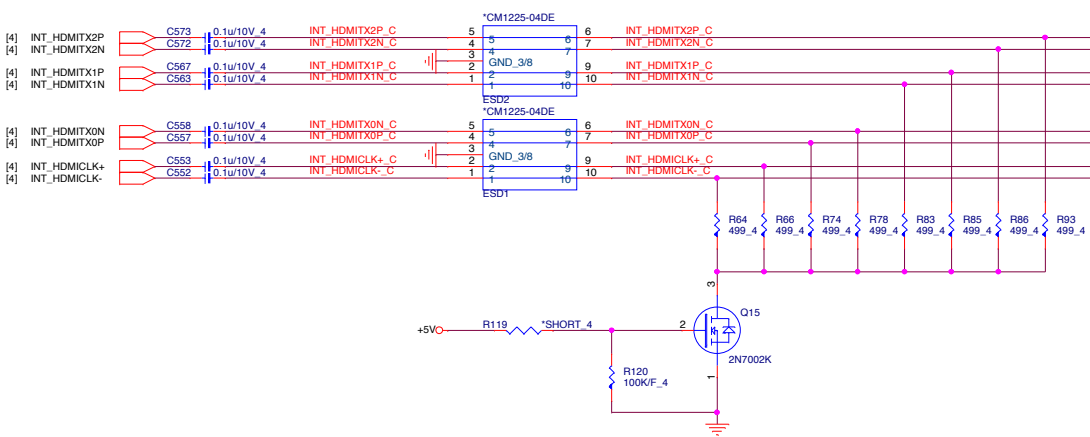
Backlight Control



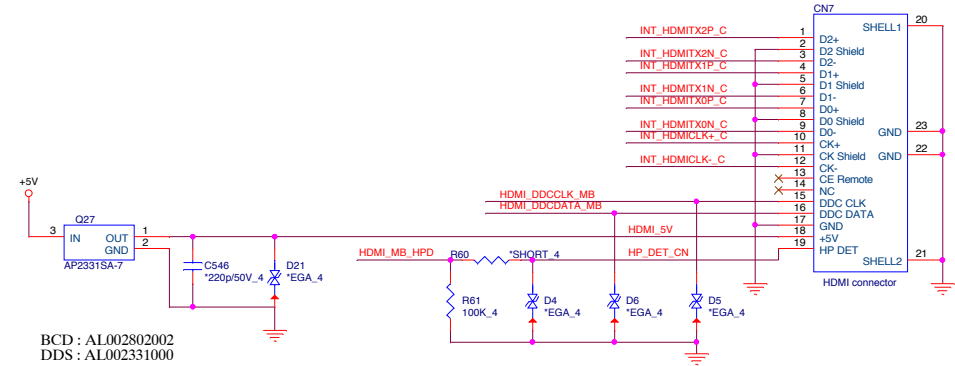
Power Switch.



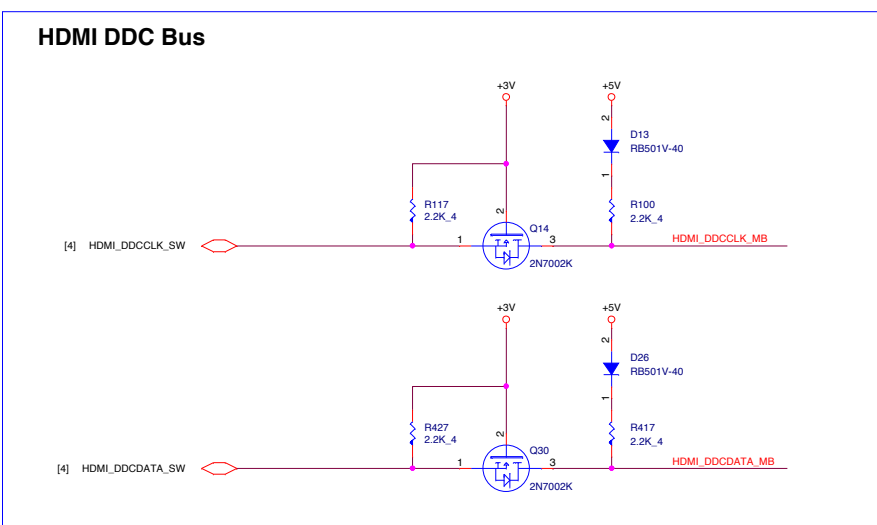
HDMI



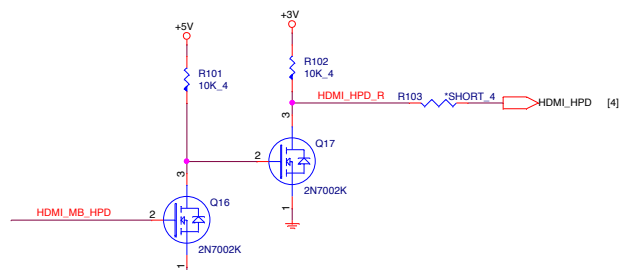
HDMI connector



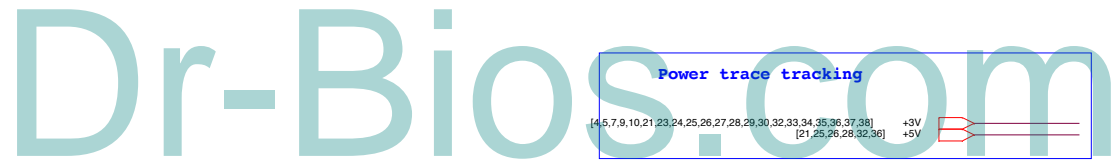
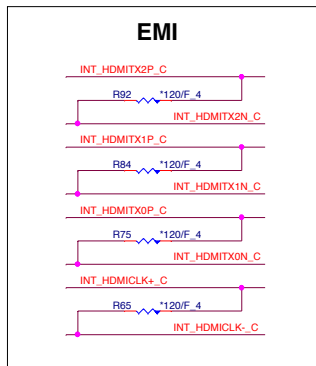
HDMI DDC Bus



HDMI-detect



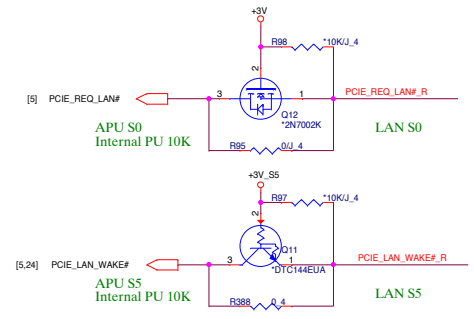
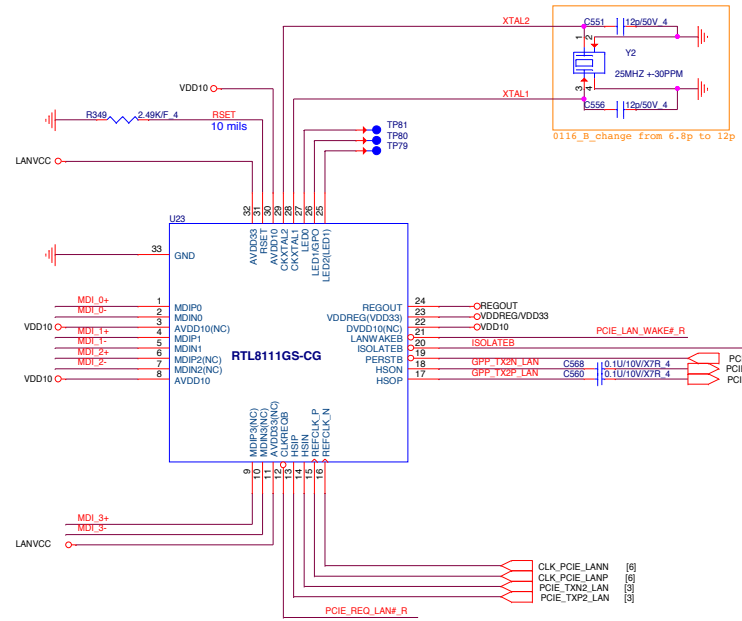
EMI



		Quanta Computer Inc. PROJECT : ZYV	
		HDMI (PS8101)	
Size	Document Number	Date: Monday, April 28, 2014	Sheet 22 of 40
		Rev C3A	

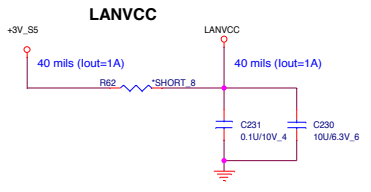
[4, 5, 7, 9, 10, 21, 23, 24, 25, 26, 27, 28, 29, 30, 32, 33, 34, 35, 36, 37, 38] +3V
 [21, 25, 26, 28, 32, 36] +5V

LAN

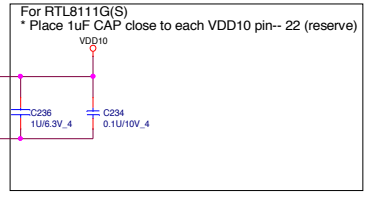
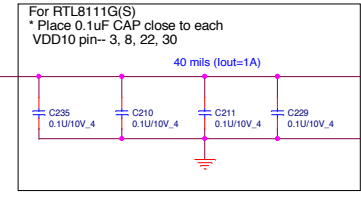
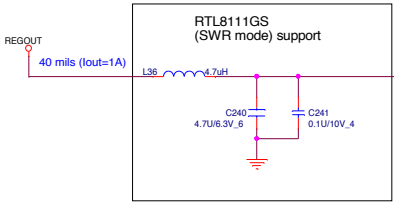
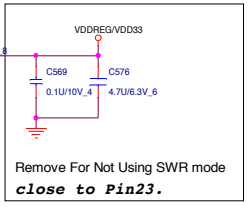
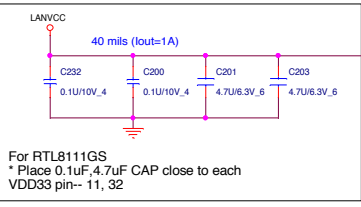
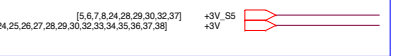


Consider VCC33 may be connected to Main Power or chipset/bios's GPIO, the pull-low resistor R14 can be NC only when Main Power or chipset/bios's GPIO can ensure to drive the ISOLATEB pin to a voltage level < 0.8V at the system state S1-S5.

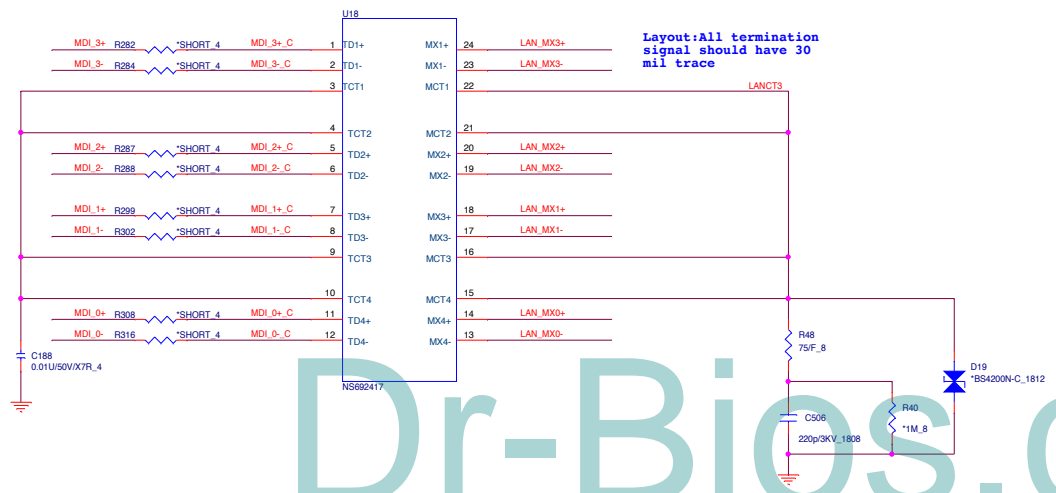
If the ISOLATEB pin can not be well-controlled to a voltage level < 0.8V at S1-S5, the pull-low resistor R14 is needed to make sure the LAN chip is well isolated.



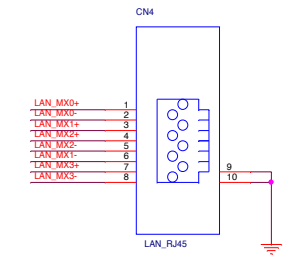
Power trace tracking



Transformer

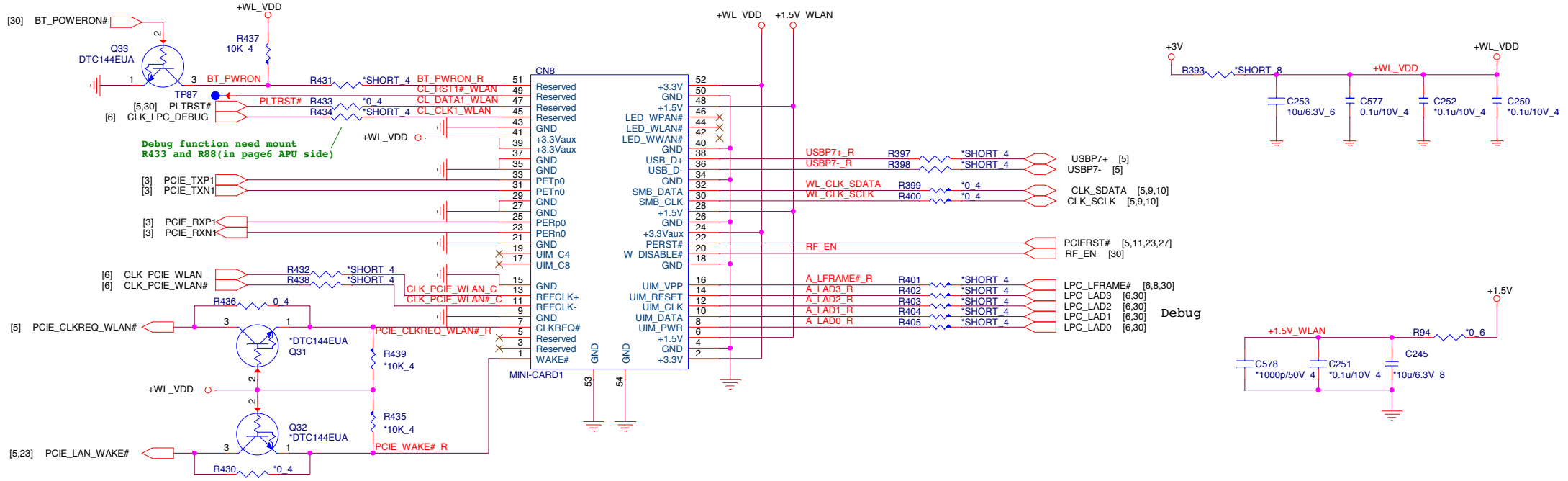


RJ45 Connector

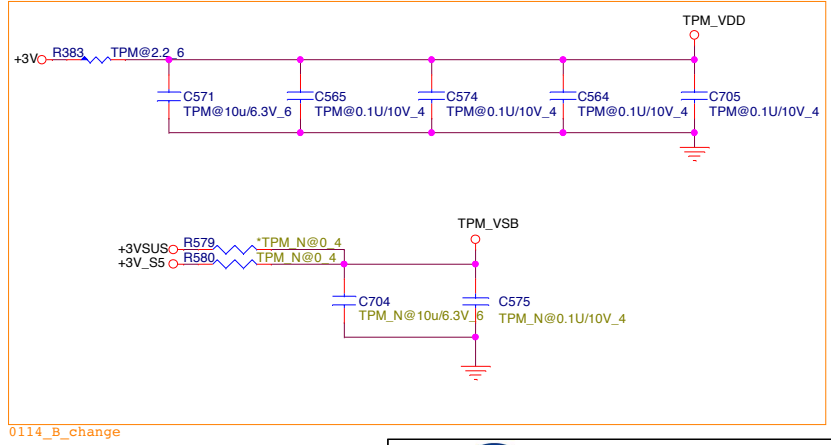
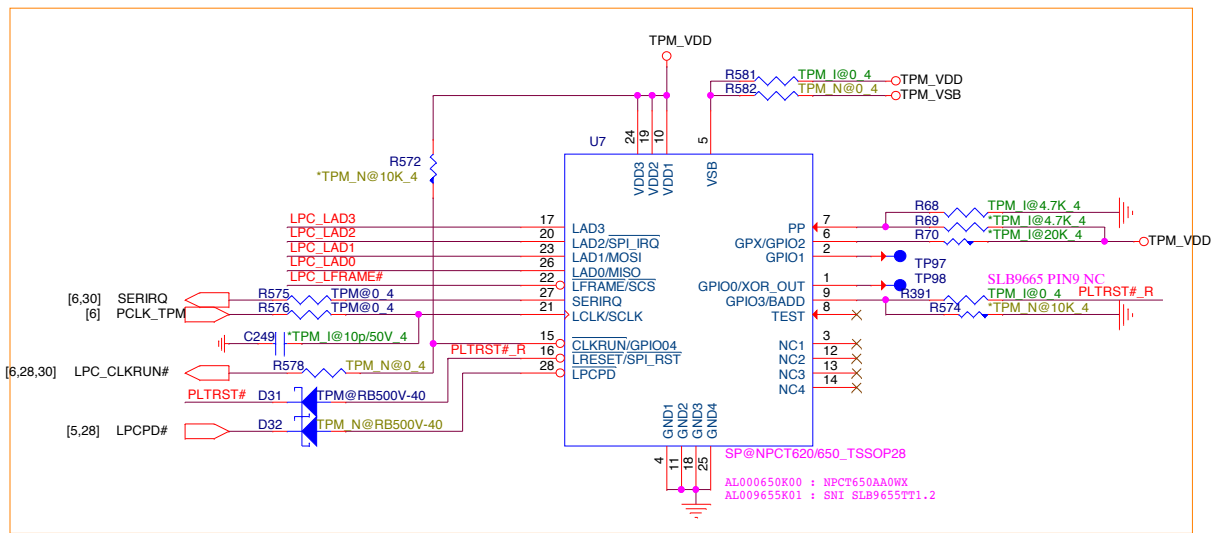



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Mini Card 1 (MPC)



TPM (TPM)

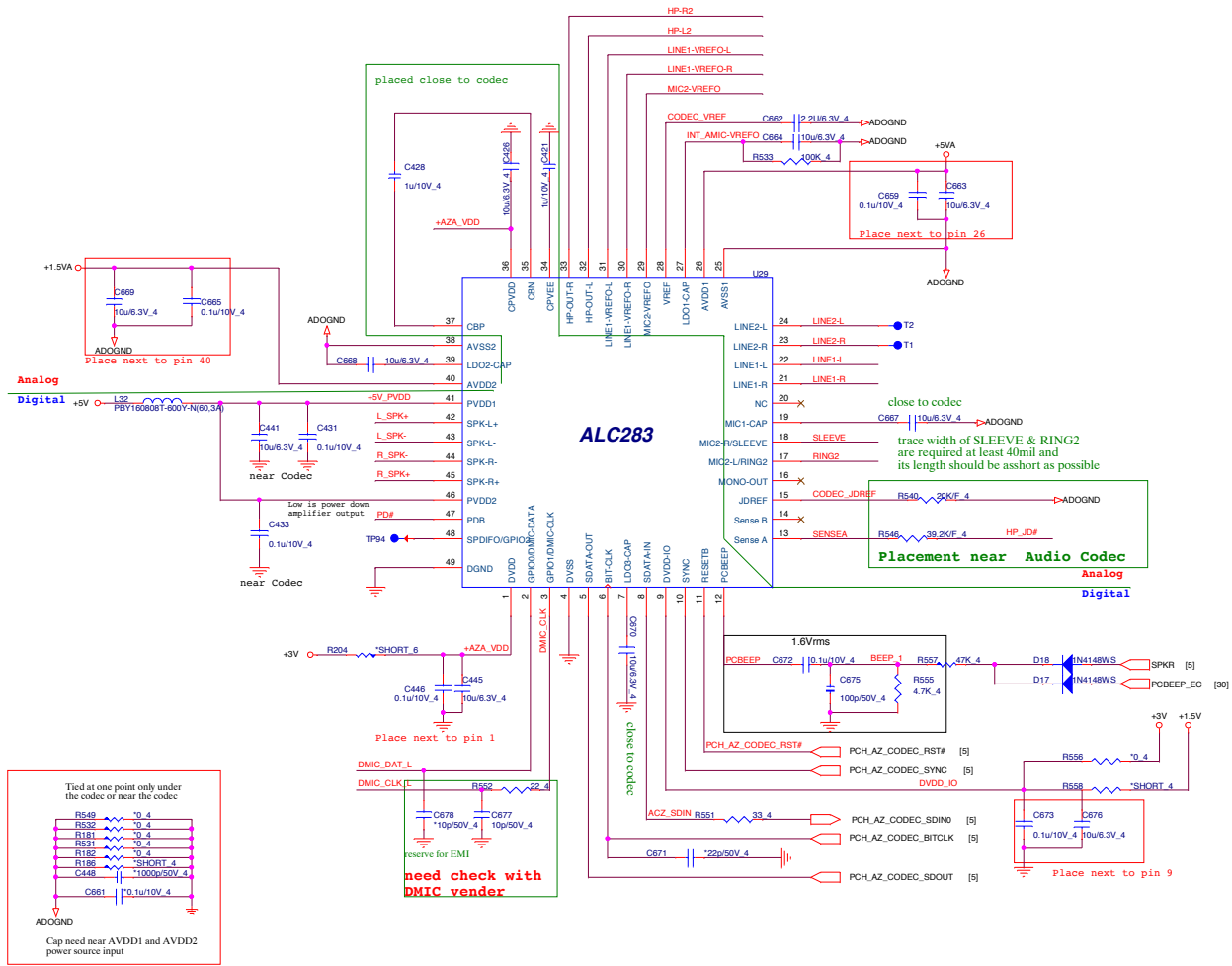




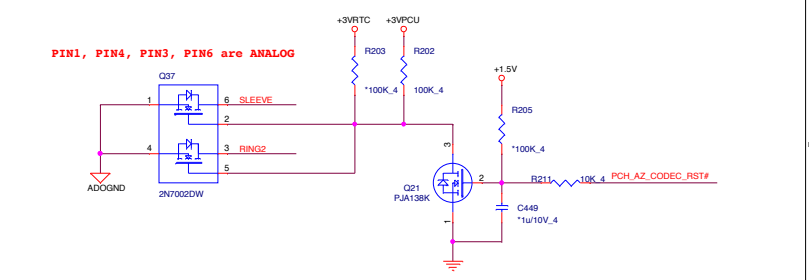
Quanta Computer Inc.
PROJECT : ZYV

Size	Document Number	Rev
	Mini-Card / TPM	C3A
Date:	Monday, April 28, 2014	Sheet 24 of 40

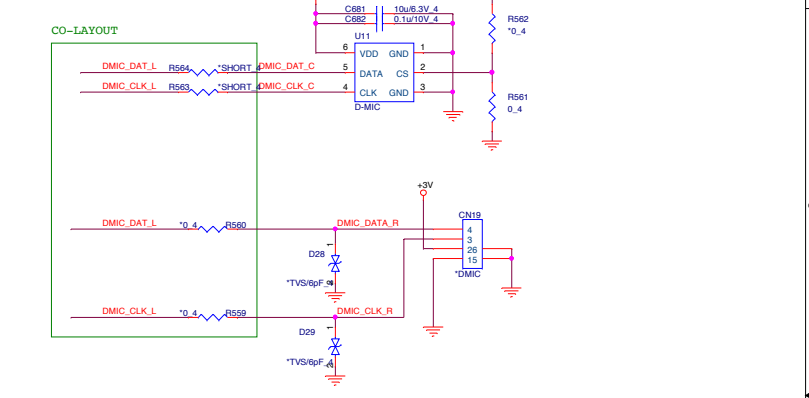
Codec(ADO)



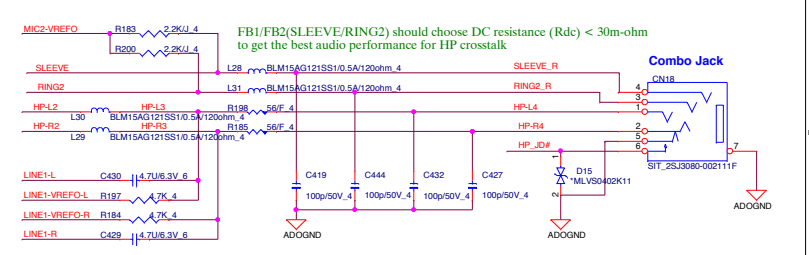
Grounding circuit(ADO)



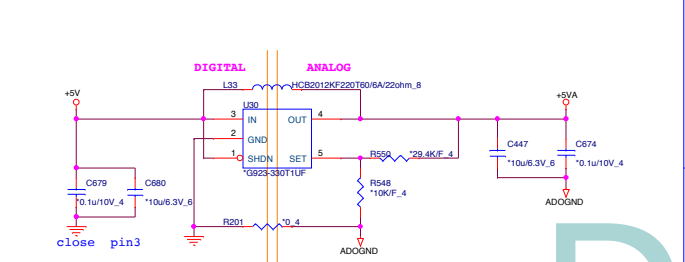
D-Mic



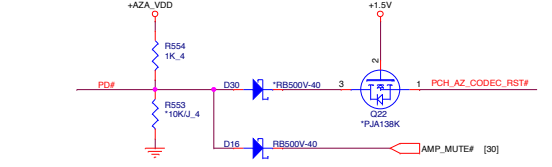
HEADPHONE/MIC/LINE combo (AMP)



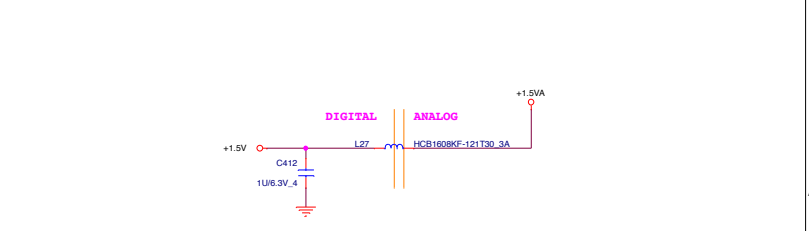
Codec PWR 5V(ADO)



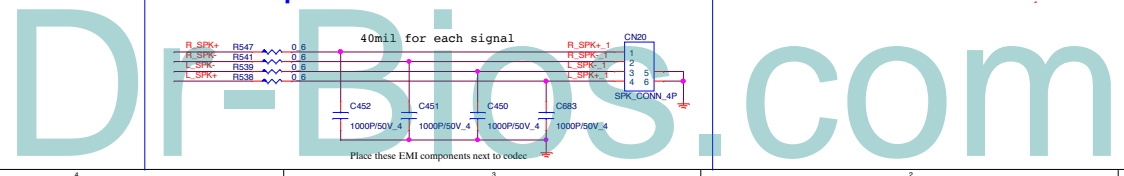
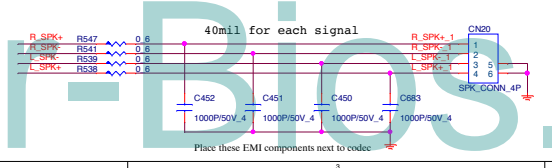
Mute(ADO)



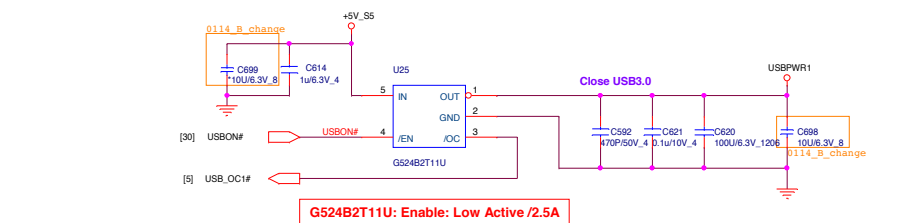
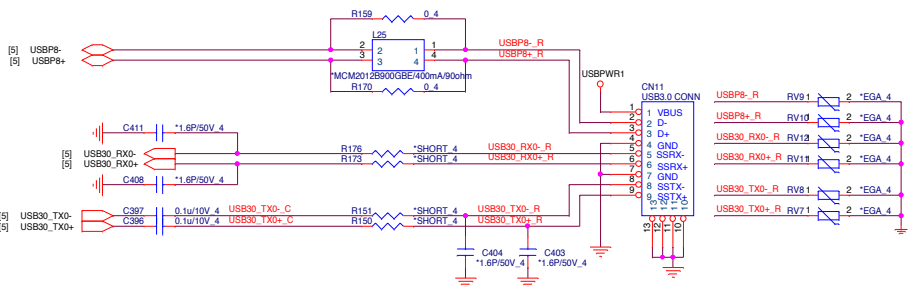
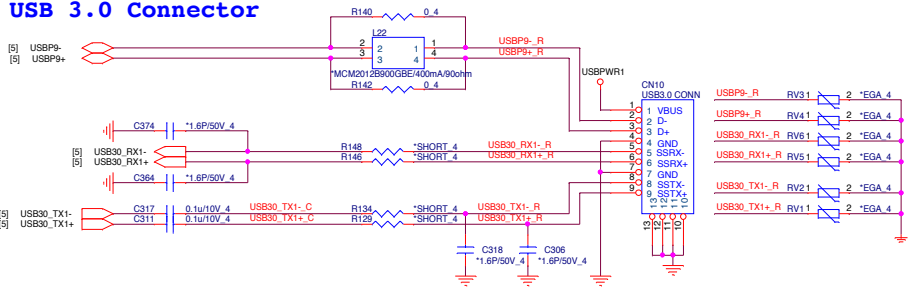
Codec PWR 1.5V(ADO)



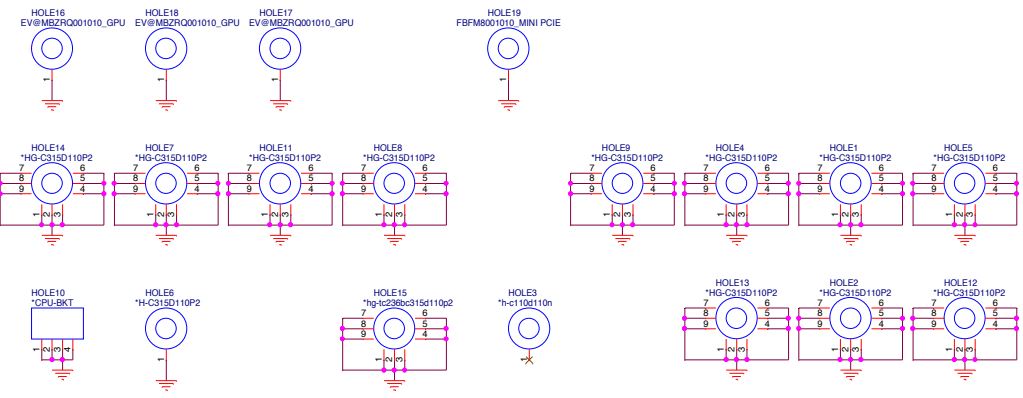
Internal Speaker



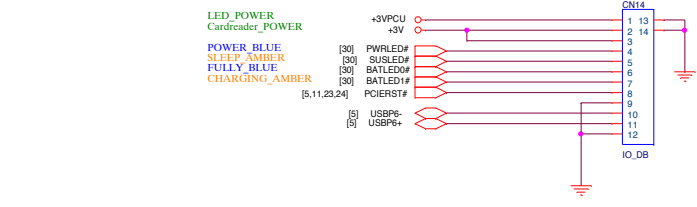
USB 3.0 Connector



HOLE(OTH)

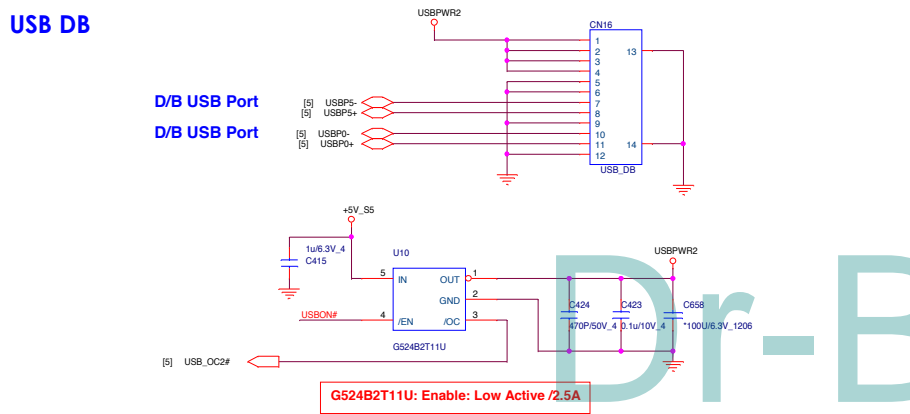


Card Reader and POWER LED DB



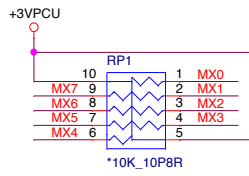
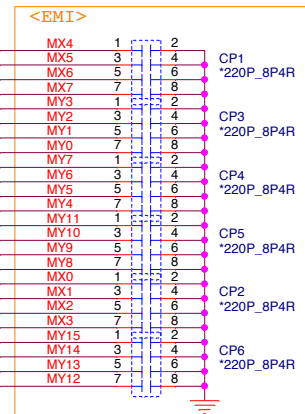
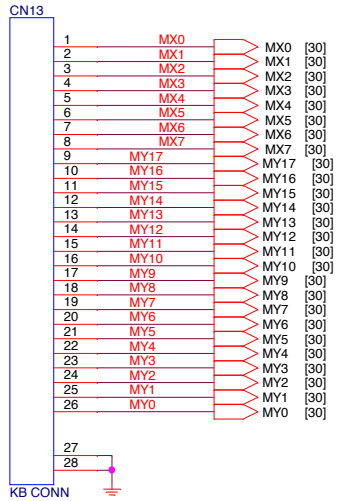
USB DB

D/B USB Port
D/B USB Port

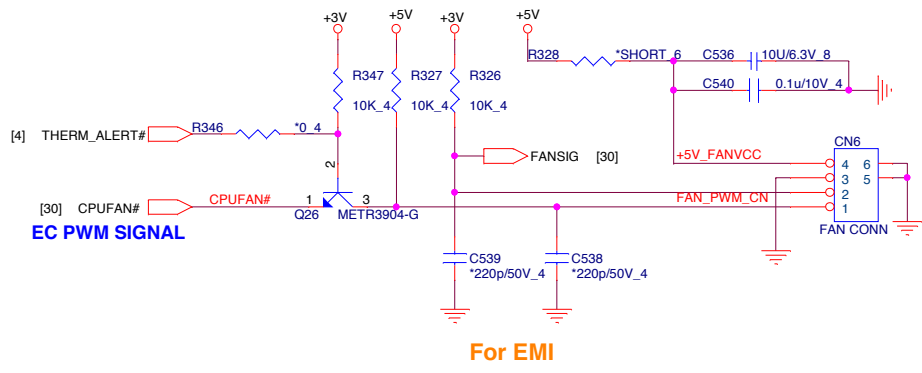


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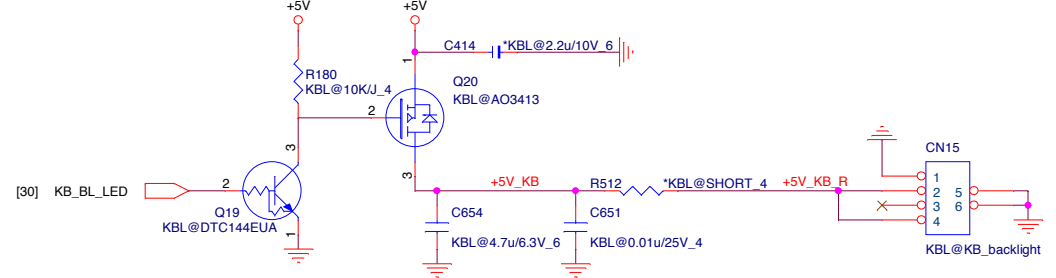
KEYBOARD (KBC)



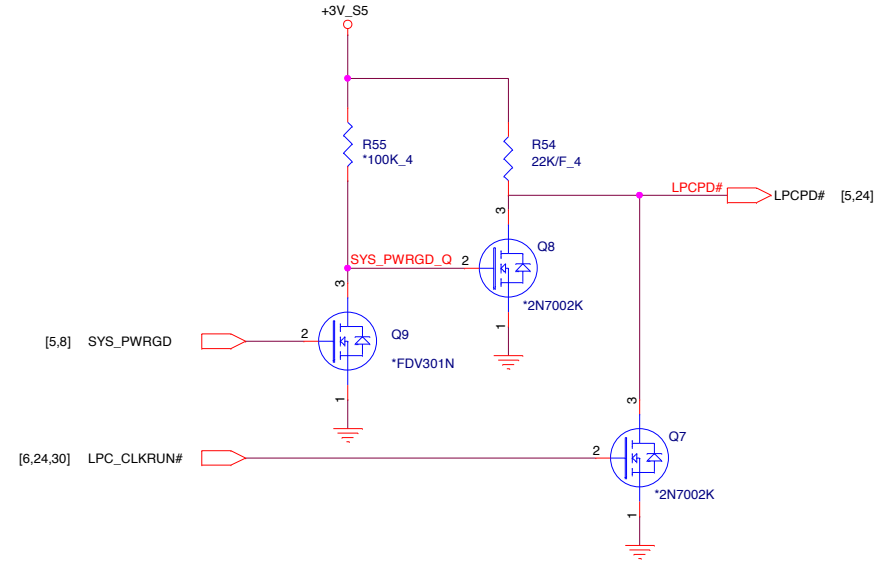
CPU FAN CTRL(THM)



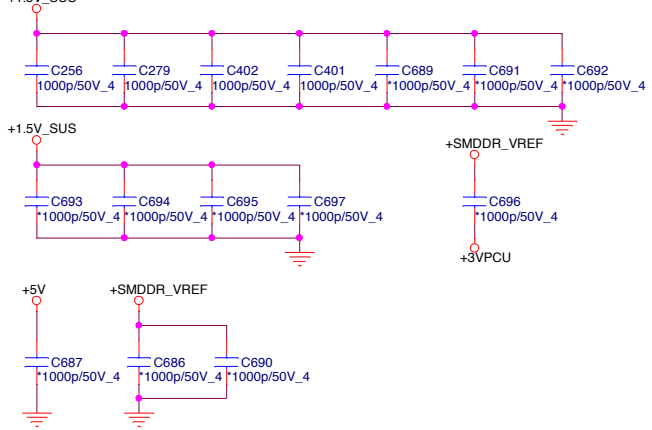
KB_BL LED (KBC)



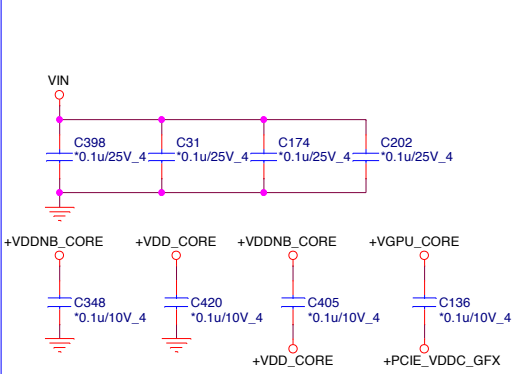
LPC Power down



EMI



Stitching cap

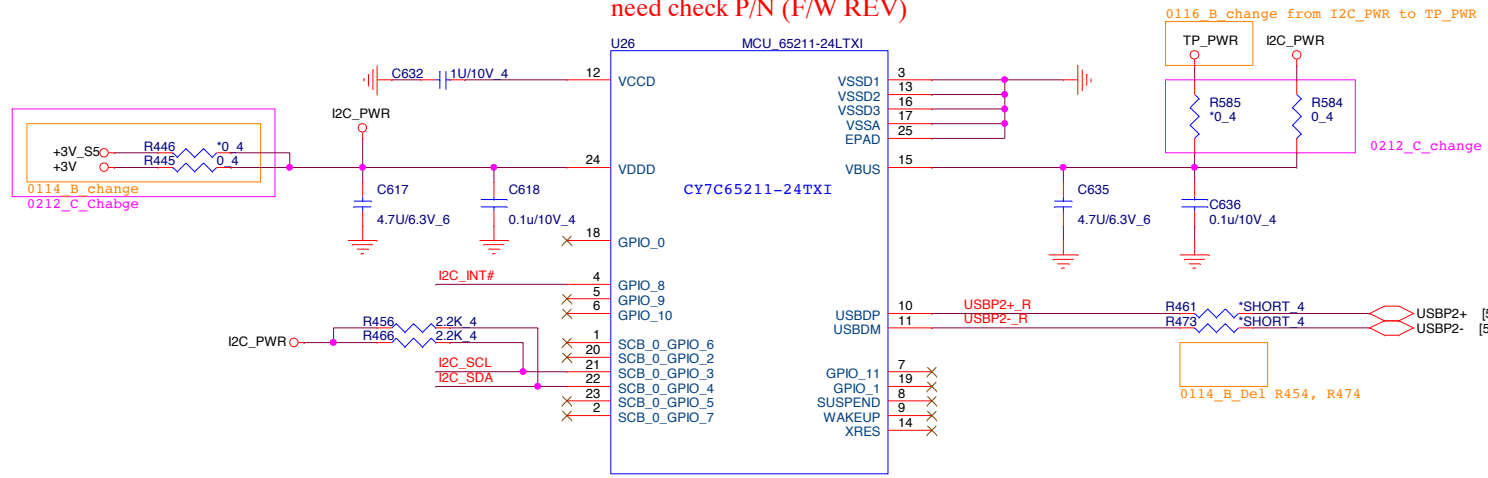


Quanta Computer Inc.
PROJECT : ZIV

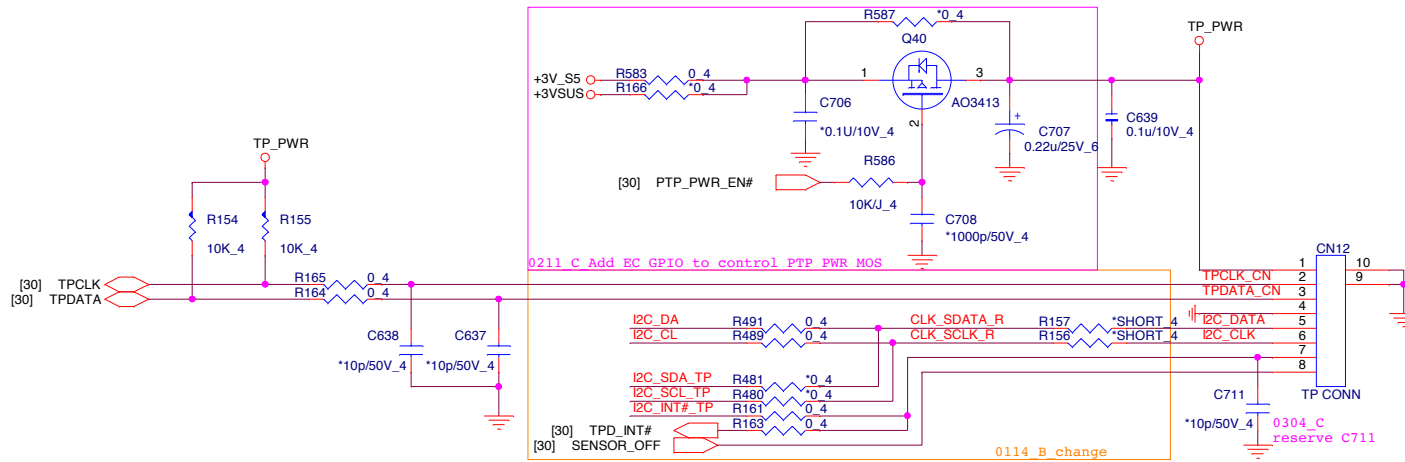
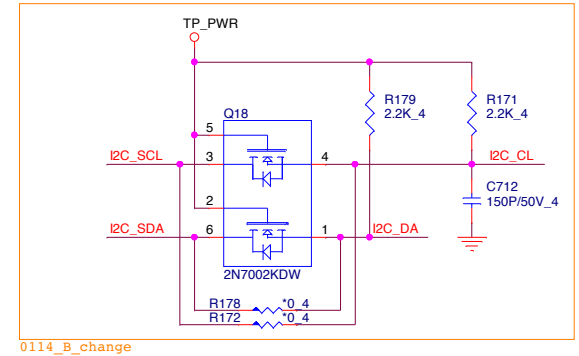
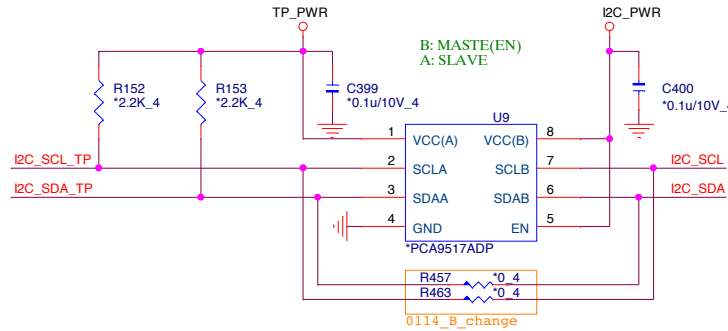
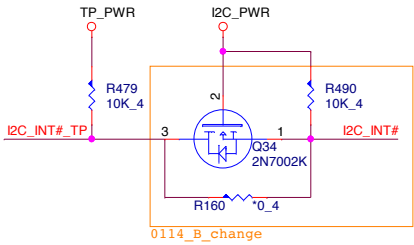
Size	Document Number	Rev
	KB/FAN/EMI	C3A
Date:	Monday, April 28, 2014	Sheet 28 of 40

I2C translator

need check P/N (F/W REV)



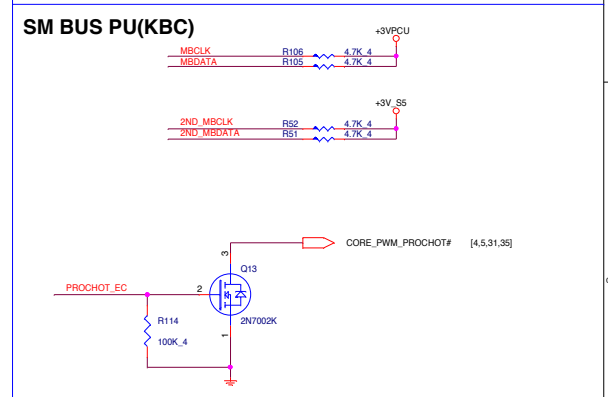
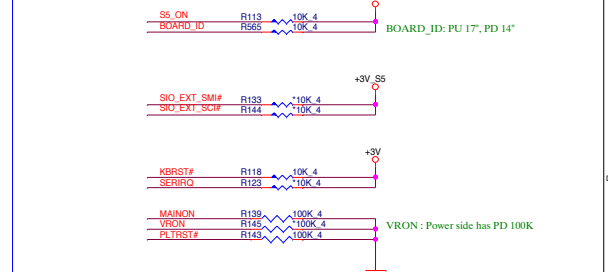
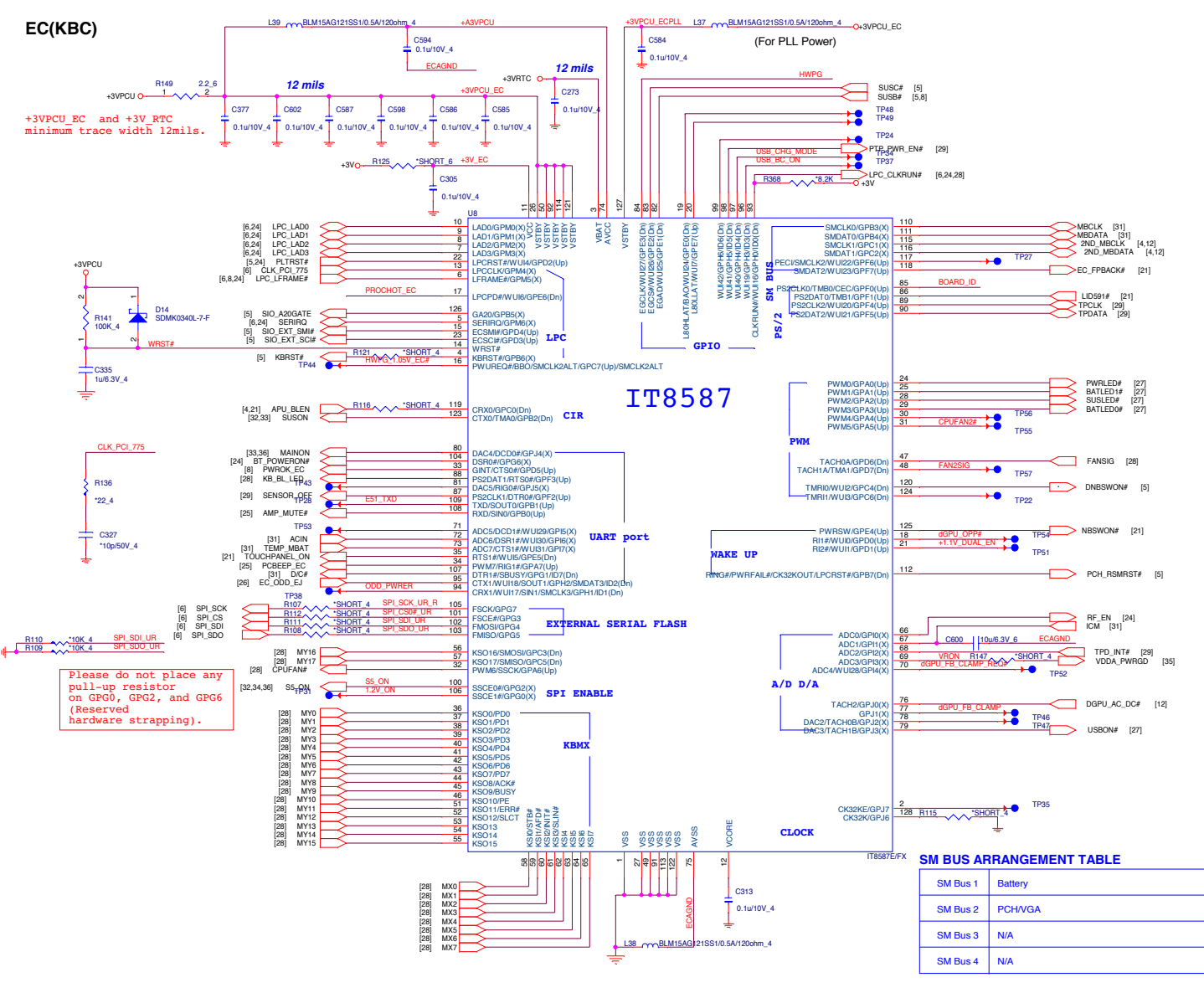
TOUCH PAD(TPD)



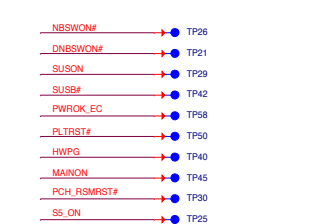
Quanta Computer Inc.
PROJECT : ZIV

Size	Document Number	Rev
	I2C translator/TP	C3A
Date:	Monday, April 28, 2014	Sheet 29 of 40

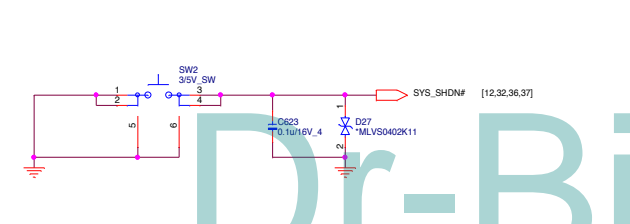
EC(KBC)

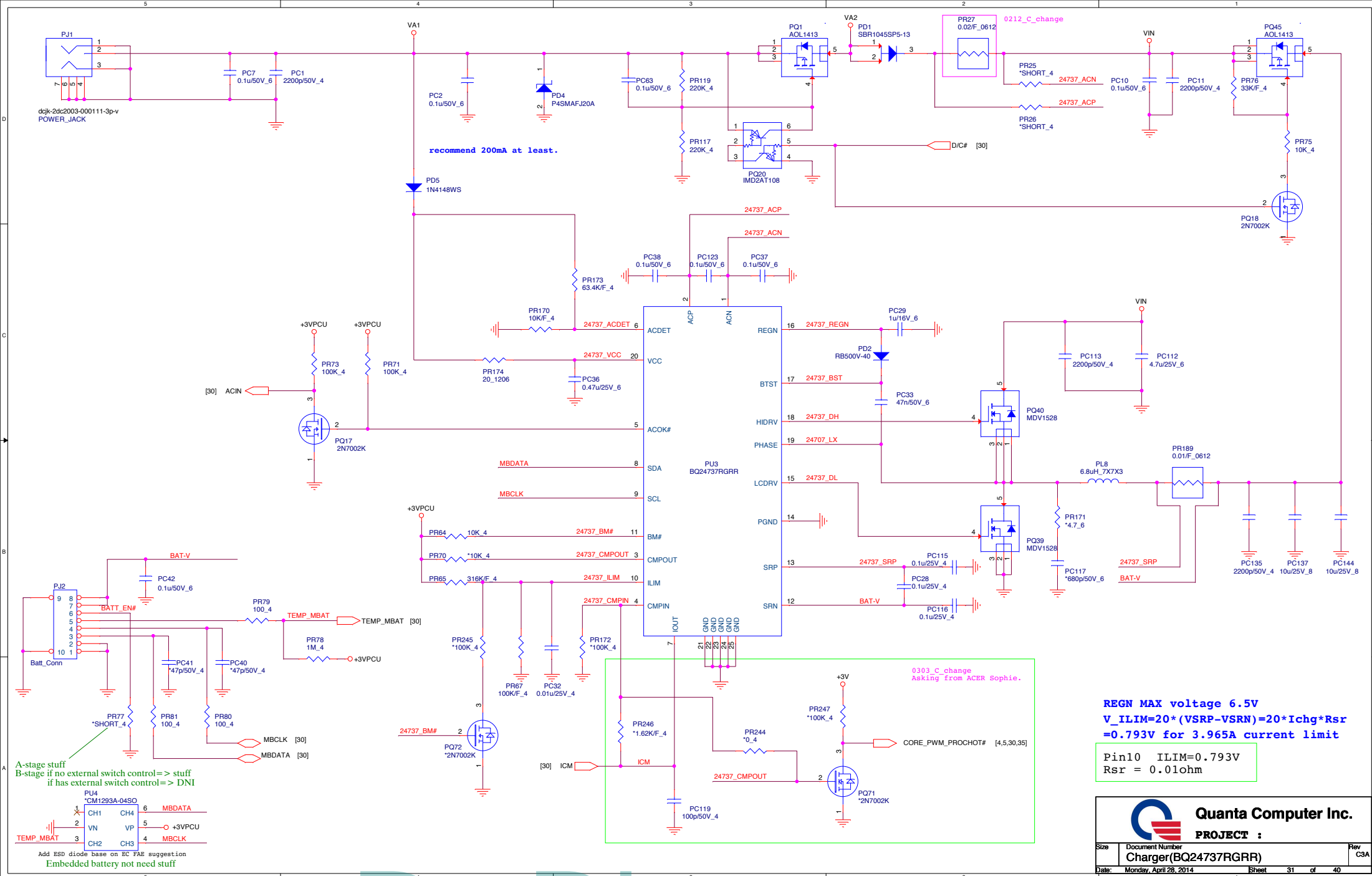


Power sequence



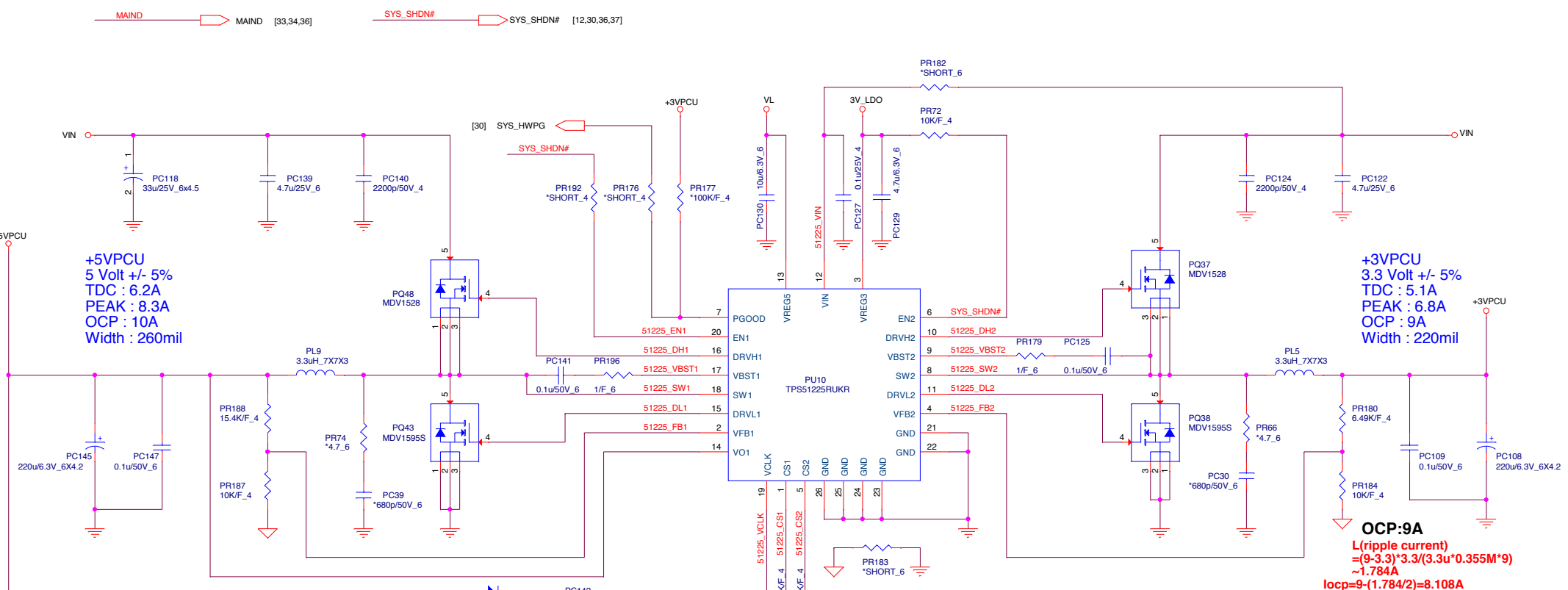
3/5VPCU reset switch (CLG)





Quanta Computer Inc.
PROJECT :

Size	Document Number	Rev
	Charger(BQ24737RGRR)	C3A
Date:	Monday, April 28, 2014	ESheet 31 of 40



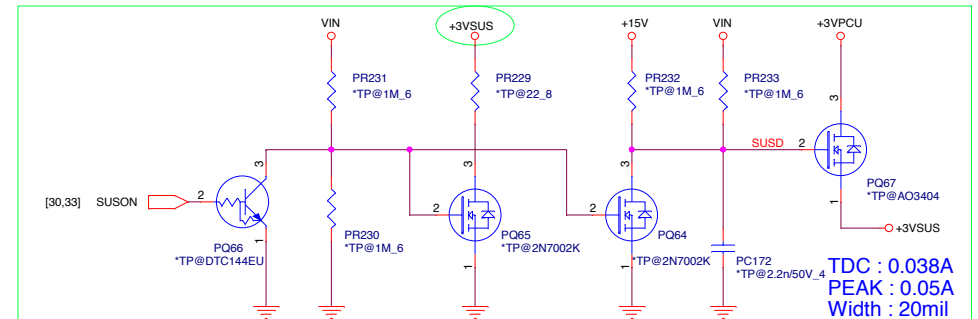
+5VPCU
 5 Volt +/- 5%
 TDC : 6.2A
 PEAK : 8.3A
 OCP : 10A
 Width : 260mil

+3VPCU
 3.3 Volt +/- 5%
 TDC : 5.1A
 PEAK : 6.8A
 OCP : 9A
 Width : 220mil

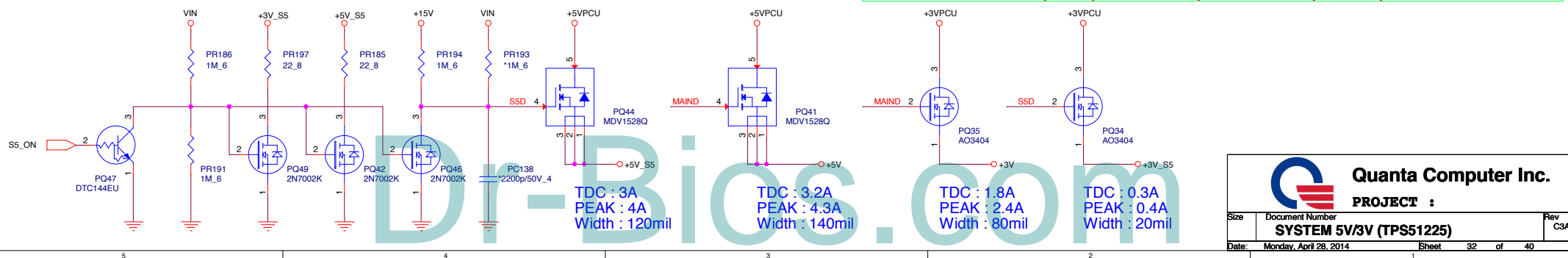
OCP:10A
 L(ripple current)
 $= (9-3.3) \cdot 5 / (3.3 \cdot 0.35 \cdot 9)$
 $= 2.244A$
 $l_{ocp} = 10 - (2.244/2) = 8.877A$
 $V_{th} = (8.877A \cdot 14m\Omega) + 1mV = 125.287mV$
 $R(lim) = (125.287mV \cdot 8) / 10\mu A$
 $\approx 100.23K$

OCP:9A
 L(ripple current)
 $= (9-3.3) \cdot 3.3 / (3.3 \cdot 0.355 \cdot 9)$
 $\approx 1.784A$
 $l_{ocp} = 9 - (1.784/2) = 8.108A$
 $V_{th} = (8.108A \cdot 14m\Omega) + 1mV = 114.512mV$
 $R(lim) = (114.512mV \cdot 8) / 10\mu A$
 $\approx 91.609K$

1/13 Adding +3VSUS power for touch pad
 (By acer request)



TDC : 0.038A
PEAK : 0.05A
Width : 20mil

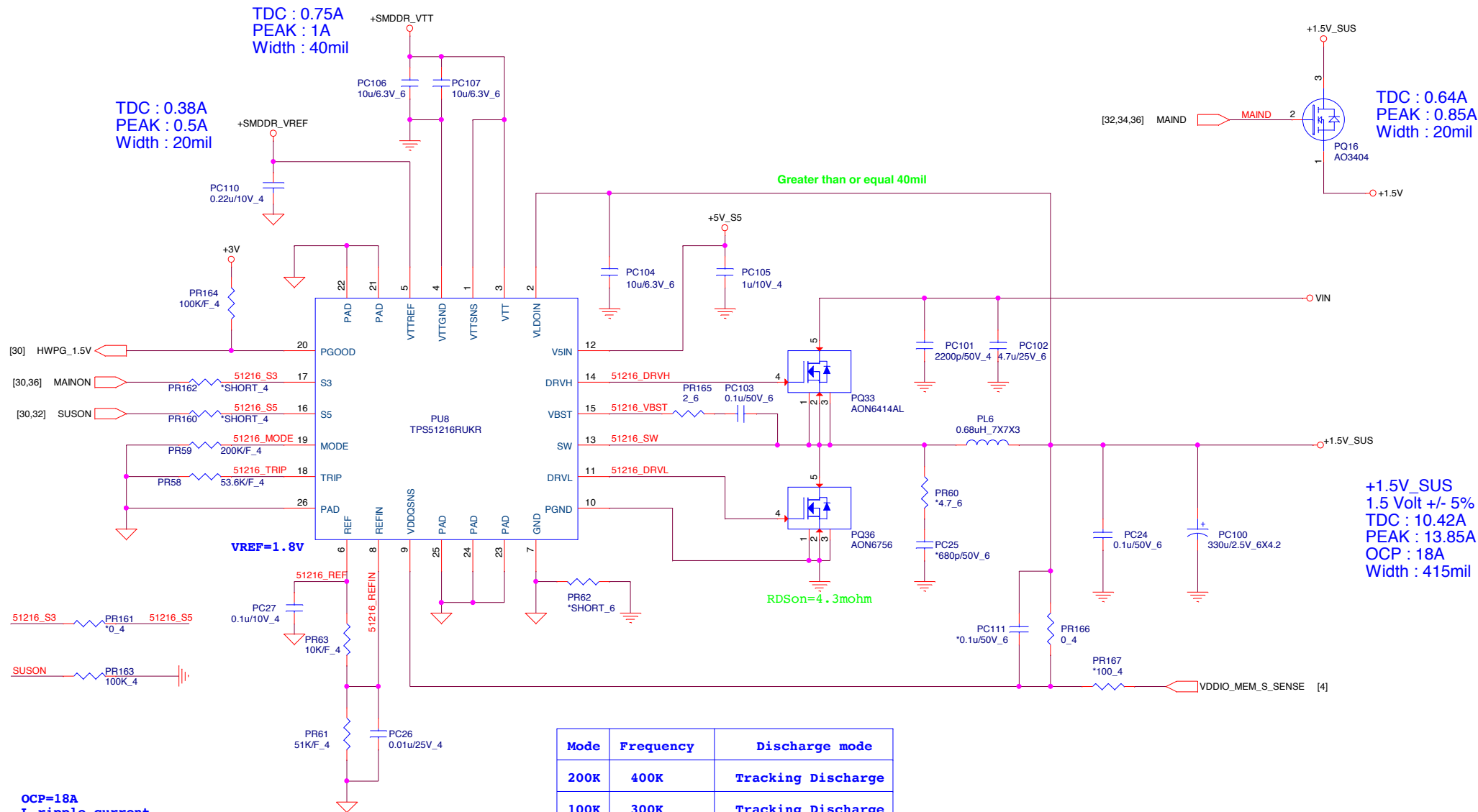


TDC : 3A
PEAK : 4A
Width : 120mil

TDC : 3.2A
PEAK : 4.3A
Width : 140mil

TDC : 1.8A
PEAK : 2.4A
Width : 80mil

TDC : 0.3A
PEAK : 0.4A
Width : 20mil



OCP=18A
 I ripple current
 $= (19-1.5) * 1.5 / (0.68u * 400k * 19)$
 $= 5.079A$
 $V_{trip} = 18 - (5.079 / 2) * 4.3mohm$
 $= 0.06647V$
 $R_{limit} = 0.06647 / 10uA * 8 - 53.183Kohm$

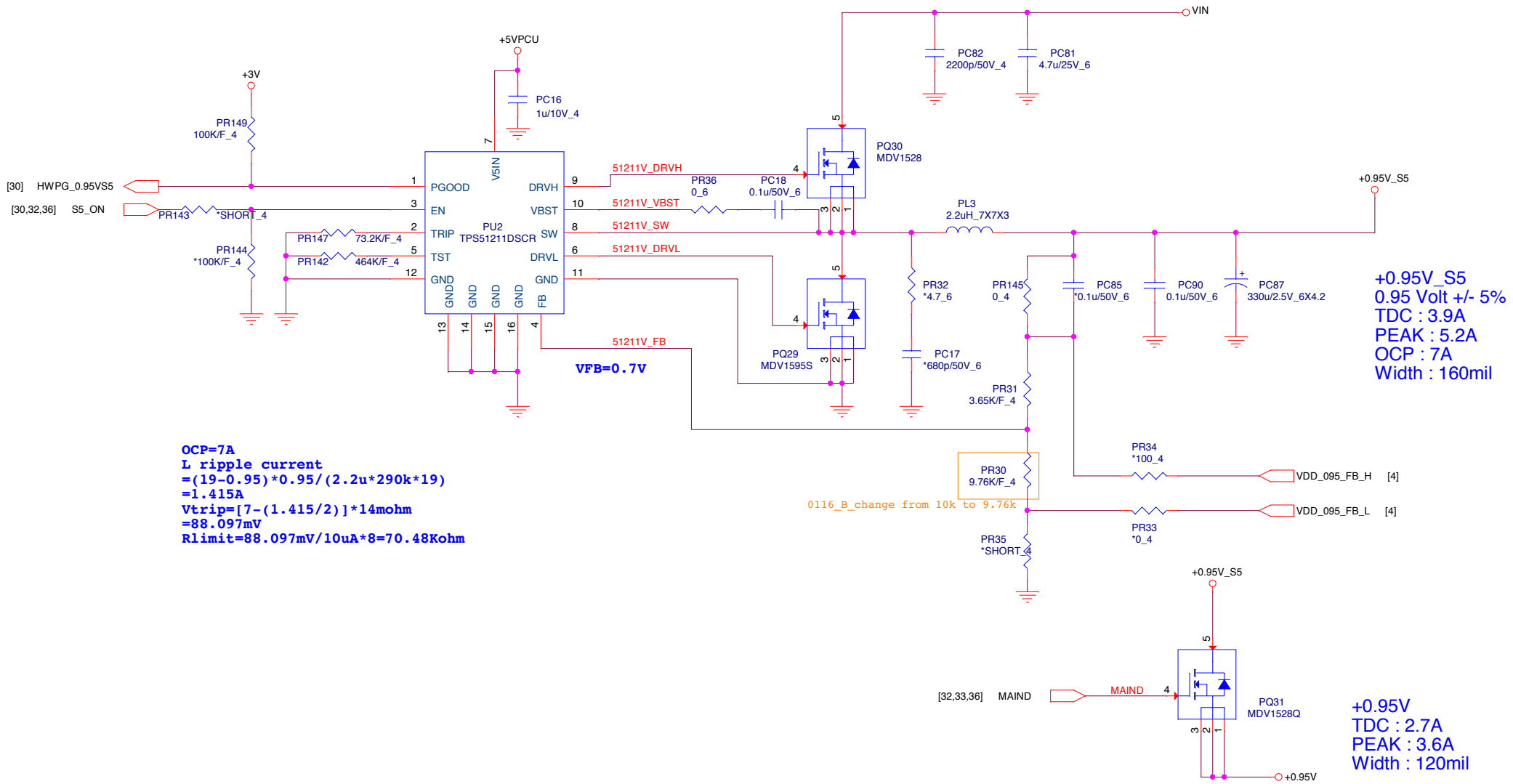
Mode	Frequency	Discharge mode
200K	400K	Tracking Discharge
100K	300K	Tracking Discharge

	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

Quanta Computer Inc.
PROJECT :

Size | Document Number | Rev
 | DDR 1.5V(TPS51216) | C3A

Date: Monday, April 28, 2014 | Sheet 33 of 40



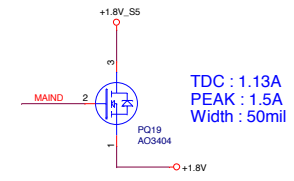
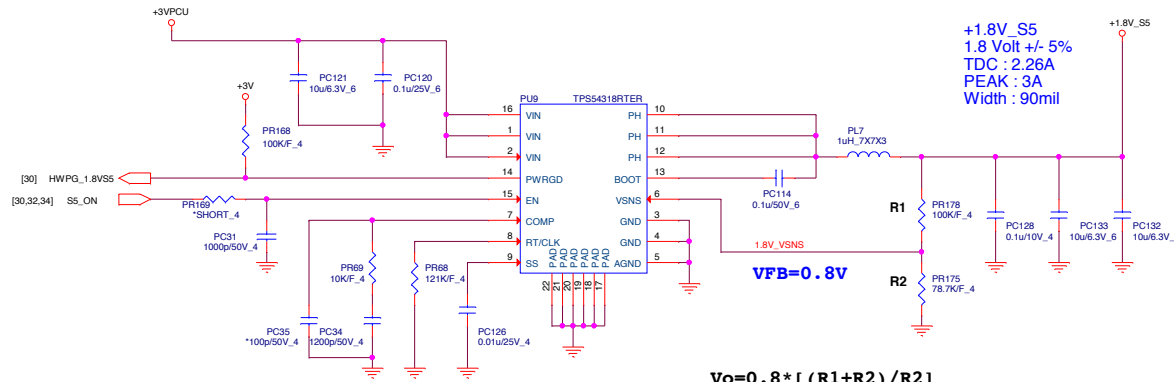
OCP=7A
 L ripple current
 $= (19 - 0.95) * 0.95 / (2.2u * 290k * 19)$
 $= 1.415A$
 $V_{trip} = [7 - (1.415 / 2)] * 14mohm$
 $= 88.097mV$
 $R_{limit} = 88.097mV / 10uA * 8 = 70.48Kohm$

+0.95V_S5
 0.95 Volt +/- 5%
 TDC : 3.9A
 PEAK : 5.2A
 OCP : 7A
 Width : 160mil

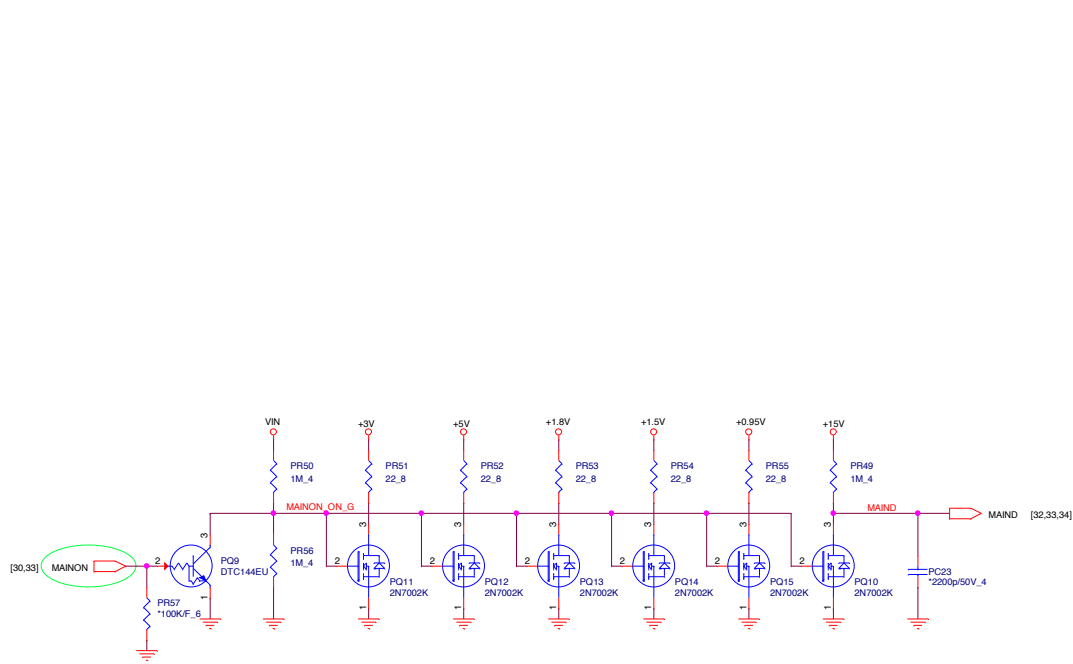
+0.95V
 TDC : 2.7A
 PEAK : 3.6A
 Width : 120mil

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PROJECT :

Size	Document Number	Rev
	+0.95V_S5(TPS51211)	C3A
Date:	Monday, April 28, 2014	Sheet 34 of 40



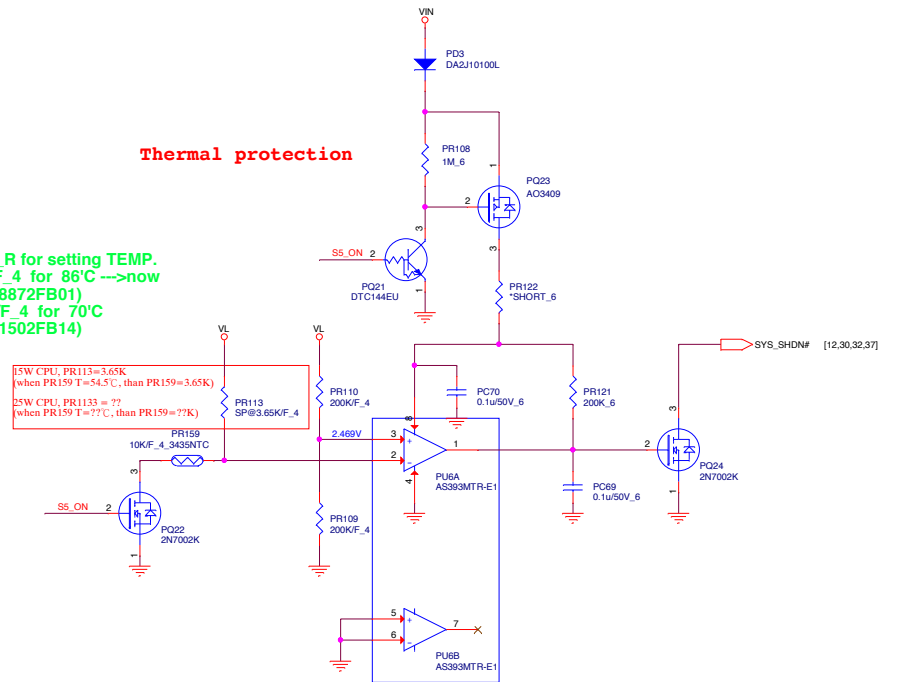
$$V_o = 0.8 * [(R1 + R2) / R2]$$



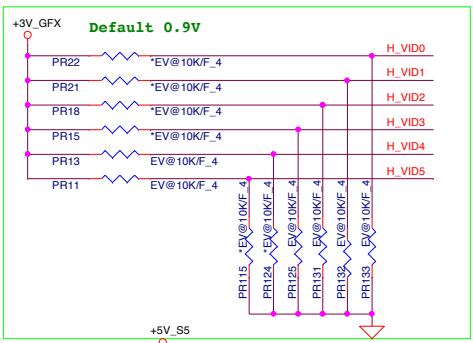
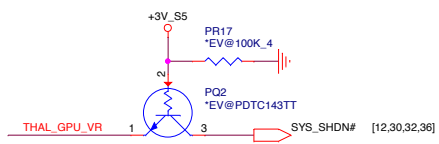
NTC_R for setting TEMP.
887/F_4 for 86°C -->now
(CS18872FB01)
1.5K/F_4 for 70°C
(CS21502FB14)

15W CPU, PR113=3.65K
(when PR159 T=54.5°C, than PR159=3.65K)
25W CPU, PR1133 = ??
(when PR159 T=?°C, than PR159=?K)

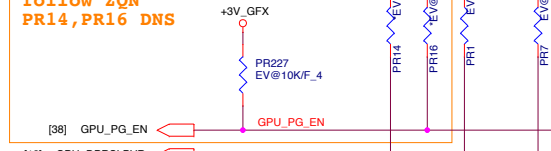
Thermal protection



For EC control thermal protection (output 3.3V)



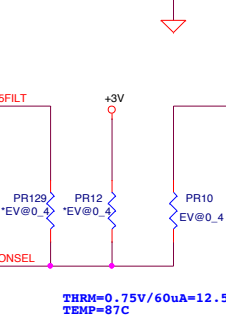
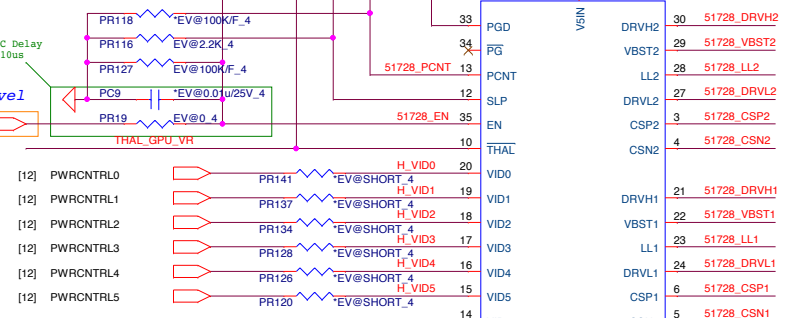
1/14 modify follow ZQN
PR14, PR16 DNS



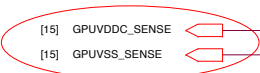
reserve 0.01uF for RC Delay
1.8v_GFX > GPU CORZ 10us

Check EN level

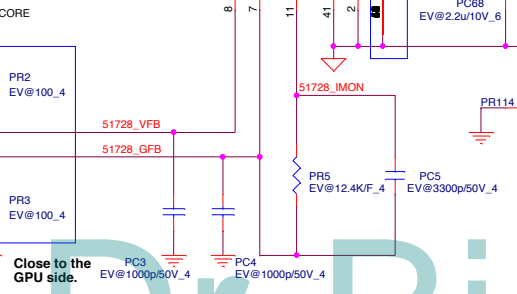
[38] 0.95_GFX_EN
1/14 modify follow ZQN



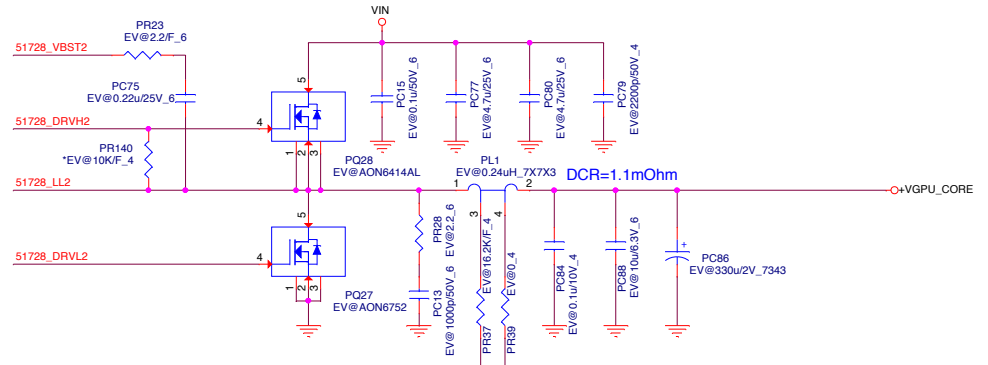
THRM=0.75V/60uA=12.5K
TEMP=87C



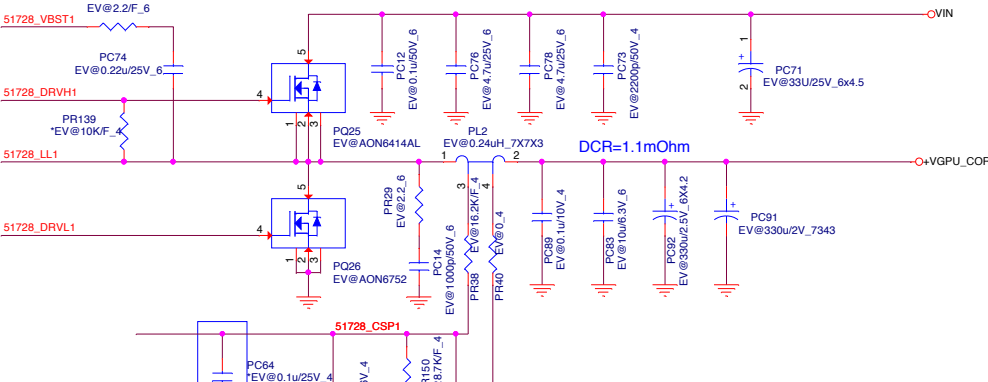
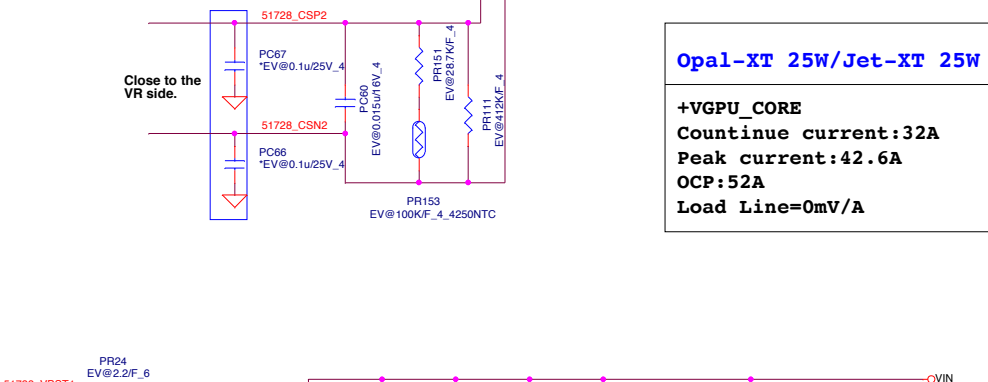
Parallel



Close to the GPU side.



Close to the VR side.



Close to the VR side.

Opal-XT 25W/Jet-XT 25W

+VGPU_CORE
Continue current:32A
Peak current:42.6A
OCP:52A
Load Line=0mV/A

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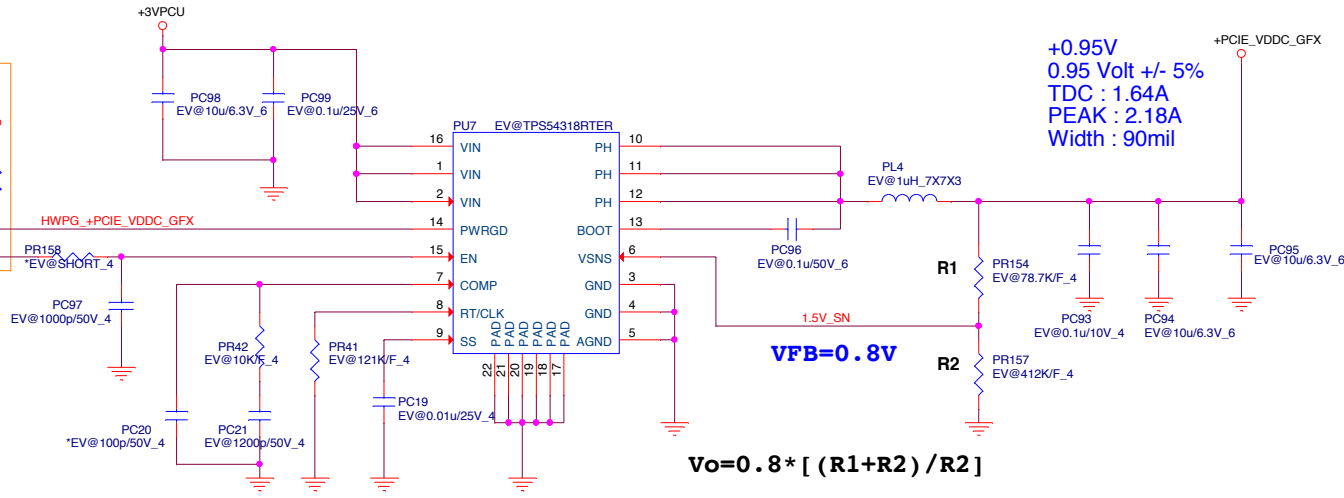
PROJECT :

+VGPU CORE(TP551728)

Size	Document Number	Rev
		C3A
Date:	Monday, April 28, 2014	Sheet 37 of 40

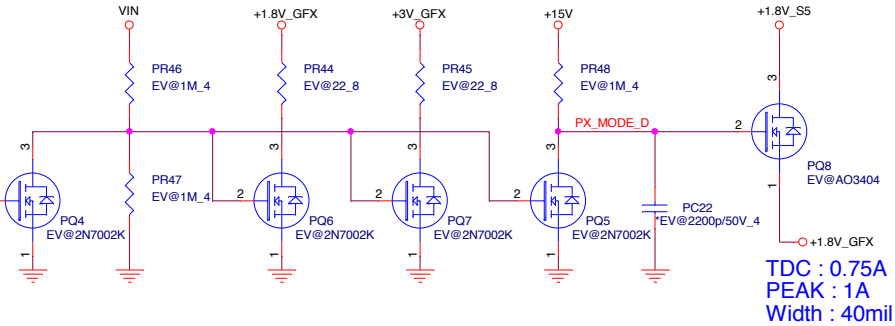
1/14 modify
follow ZQN
change PR156
to 10K

[37] 0.95_GFX_EN
PR155 *EV@SHORT_4
+3V_GFX

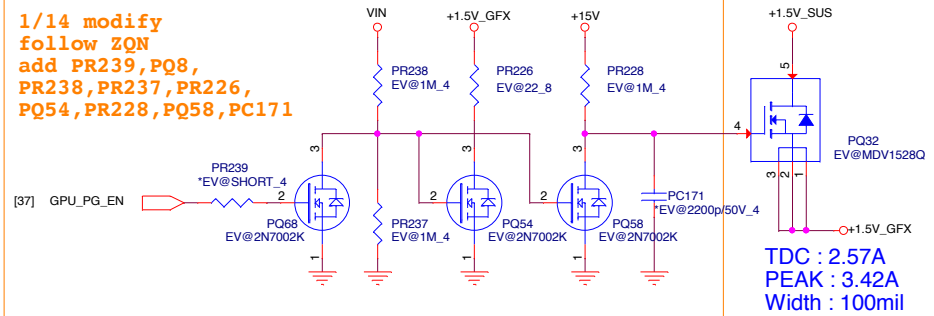


1/14 modify
follow ZQN

0.95_GFX_EN



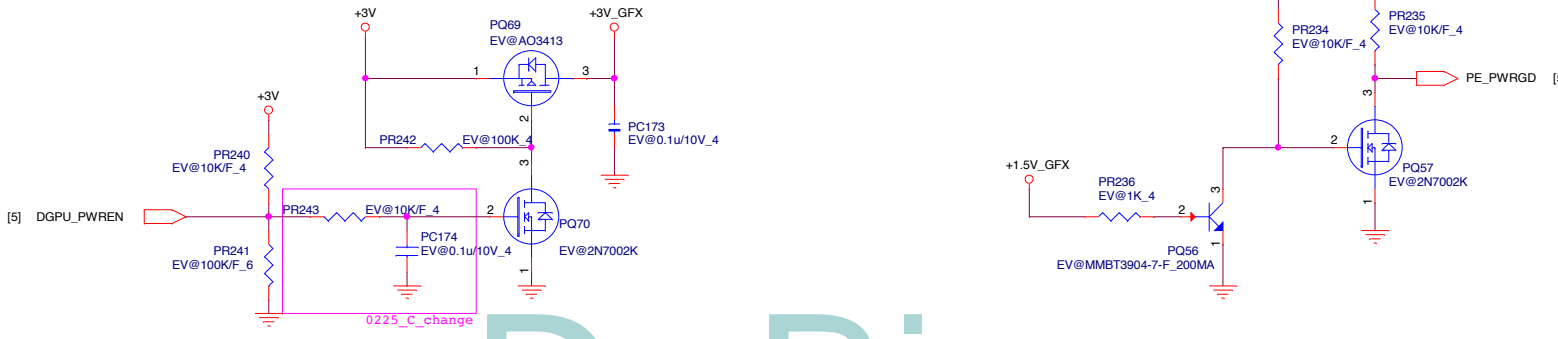
1/14 modify
follow ZQN
add PR239, PQ8,
PR238, PR237, PR226,
PQ54, PR228, PQ58, PC171



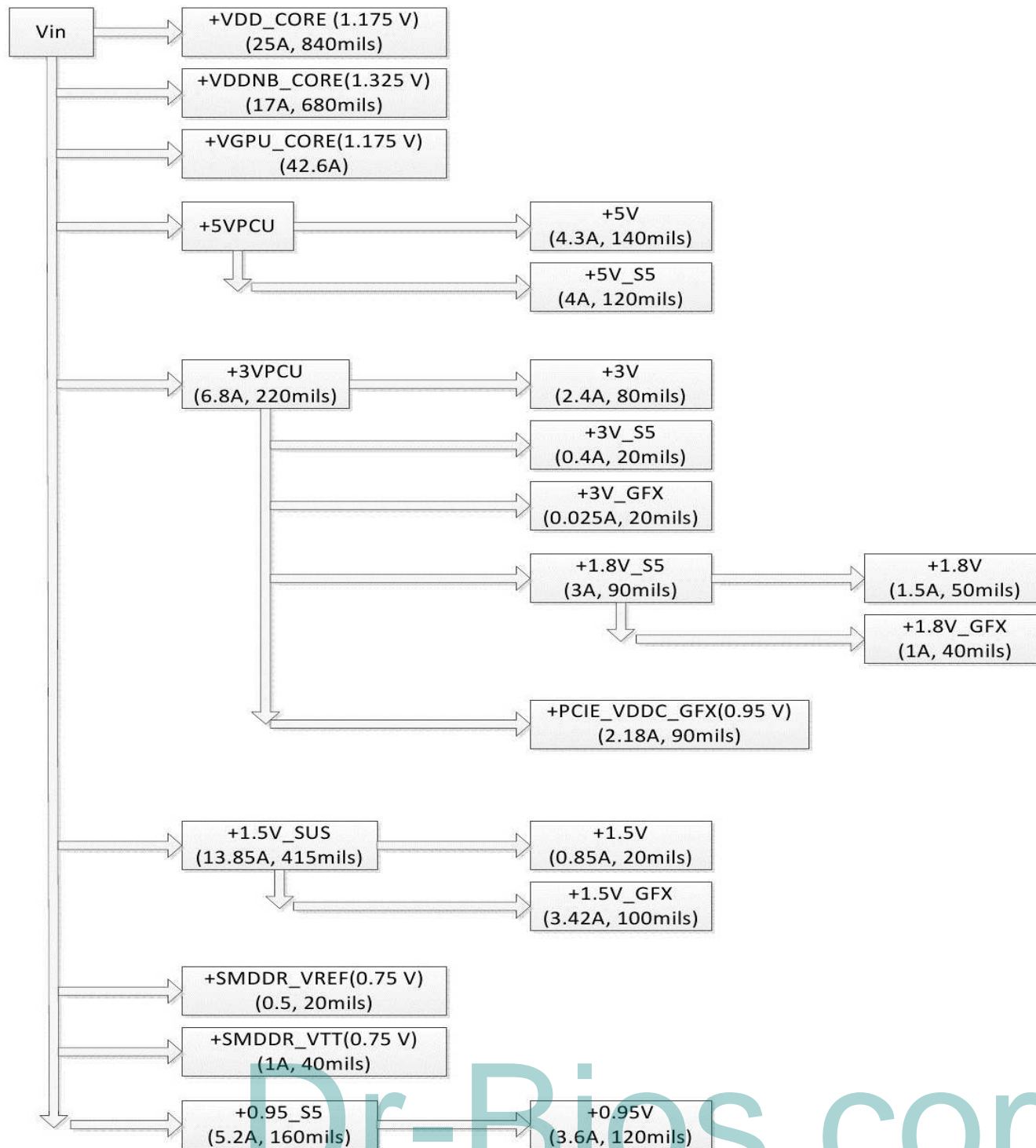
1/14 modify
follow ZQN, delete PQ3
add Q42, Q43, R569, PR240, PR241

TDC : 0.02A
PEAK : 0.025A
Width : 20mil

1/14 modify
follow ZQN
add PR234, PR235, PR236, PQ56, PQ57



PROJECT :		
Size	Document Number	Rev
	GPU_POWER/VDDC_GFX	CSA
Date:	Monday, April 28, 2014	Sheet 38 of 40



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